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SURFACE VEHICLE INFORMATION REPORT

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(R) Characterization, Conducted Immunity

Foreword

Some parts of this document are related to ISO 7637-2 in that the intent is to verify conducted immunity to transients. However the philosophy and methods are different.

1. Scope

This document establishes methods for characterizing the robustness of vehicle electronic modules to certain environmental stresses. They include:

Voltage-Temperature Design Margins
Voltage Interruptions-Transients Over Temperature
Voltage Dips
Current Draw Under a Number of Conditions

These methods can be applied during Development, Pre-Qualification, Qualification or for Conformity. This document does not address other environmental robustness stresses such as vibration, high temp exposure, load faults, ESD, etc.

1.1 Measurement Philosophy

The major causes for today's electronic systems issues are:

1. Requirements not properly defined (e.g. functionality, environment)
2. System interfaces
3. Trouble Not Indicated (TNI)

A major contributor to issues in these categories is Conducted Immunity (CI). The methods used in this document are designed to address the deficiencies inherent in other commonly used validation methods for CI. An alternate approach is specified to supplement those methods. It uses relatively simple and low cost techniques that does not require a laboratory environment. This makes it easier to identify concerns early during the development stage (although they can be used at any stage).

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Conducted Immunity is a major issue for todays electronics. That aspect of Electromagnetic Compatibility (EMC) has the highest potential for warranty and customer satisfaction issues. However, traditional validation testing for CI has major limitations. Specifically, CI testing is most often run at room temperature due to the nature of the test equipment and facilities - the response of the product could be different when cold or hot than at room temperature. Another limitation is that very repeatable, accurate and idealized signals are used to represent the "real world". While this would appear to be desirable, it is not necessarily the case. The "real world" contains randomness and other characteristics (e.g. complex impedances) not replicated by such idealized test signals. Randomness is extremely critical for a microprocessor type DUT since the stress event (e.g. transients) must often line up in time with a certain point(s) in software execution to have an effect.

In addition to CI, current draw under a number of conditions is also characterized since it is a good indication of proper module operation, degradation during environmental testing, detection of inadvertent changes to the design or manufacturing process (conformity) and detection of sneak paths.

It is important to note that many of these tests are not the "test for success" type where the results are classified as either pass or fail. Such testing is of limited value since it generates little information. The goal is to generate variable data or anomalies so that the maximum amount of information is obtained and an informed engineering judgement can be made.

1.2 Rationale

The methods in this document, using relatively simple and low cost techniques, are designed to address some of the deficiencies inherent in other commonly used testing methods for conducted immunity. Examples of such deficiencies - not tested throughout temperature range and use of idealized signals that do not adequately represent the real world. It also addresses other robustness issues not addressed elsewhere.

2. References

2.1 Applicable Publications

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of publications shall apply.

2.1.1 SAE PUBLICATION

Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1113-1—Electromagnetic Compatibility Measurement Procedures and Limits for Vehicle Components (Except Aircraft).

2.1.2 OTHER PUBLICATIONS

Available at www.fordemc.com.

Ford EMC Specification ES-XW7T-1A278-AC

2.2 Related Publications

The following publication is provided for information purposes only and is not a required part of this document.

2.2.1 SAE PUBLICATION

Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1113-11—Immunity to Conducted Transients on Power Leads

2.2.2 ISO PUBLICATION

Available from ANSI, 25 West 43rd Street, New York, NY 10036-8002.

ISO 7637-2—Road vehicles—Electrical disturbances from conduction and coupling, Electrical transient conduction along supply lines only

3. Definitions

3.1 Conformity

Periodic tests to detect an inadvertent change in design or process.

3.2 LOL, UOL-X (Y)

Lower and Upper Operating Limit (when DUT ceases to operate or is erratic) for parameter X at specified conditions Y. For example LOL-V (T-hi) = Lower Operating Limit for voltage at T-hi temperature.

3.3 T3, T4

Lower and Upper temperature for guaranteed performance (meets all specs). T1, T2 = Lower /Upper temperature for guaranteed operation (minimun function).

3.4 Trouble Not Indicated (TNI)

Potentially defective modules (e.g. field return) where the cause of concern cannot be identified with traditional test methods.

3.5 V1, V2

Lower and Upper voltage for guaranteed performance (meets all spec). V3, V4 = Lower/Upper voltage for guaranteed operation (minimum function).

4. Requirements Description

4.1 Voltage-Temperature Design Margins

This method evaluates Design Margins for voltage over temperature. It can be combined with noise immunity (see 4.2). This testing is especially useful for evaluating electronic design changes or degradation by comparing results before and after. The data can be used to give a graphical representation comparing the DUT specification limits (voltage, temp) with the Design Margin envelope.

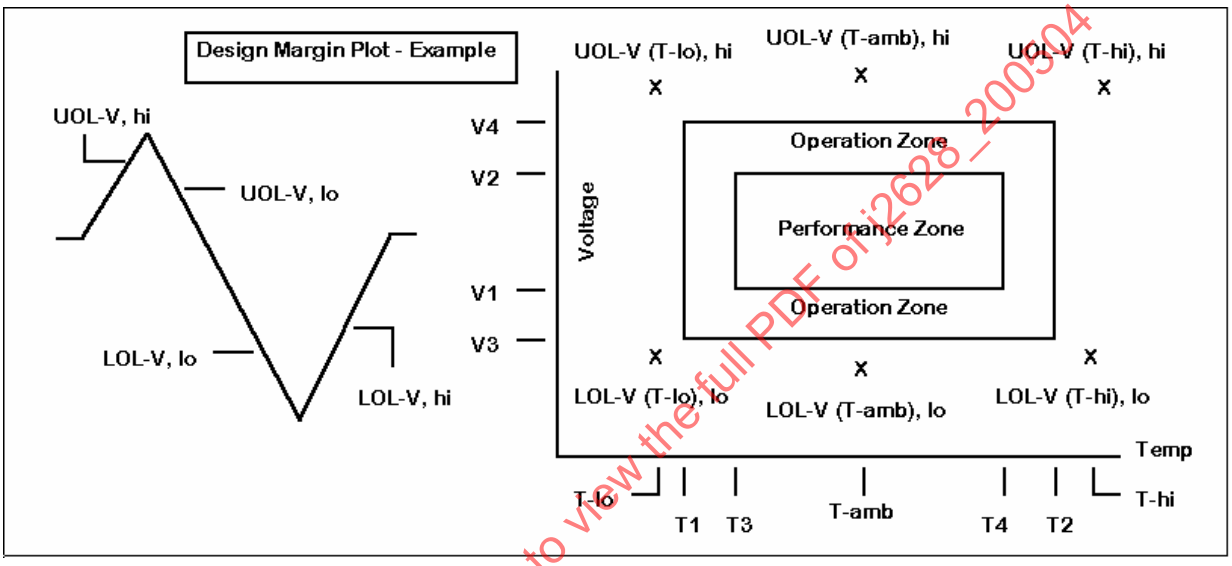

FIGURE 1—DESIGN MARGINS PLOT - EXAMPLE

4.2 Voltage Interruptions-Transients

4.2.1 GENERAL

a. Although this section is presented separately, this testing can be combined with the Voltage-Temperature design margin testing to obtain results over temperature.
b. A key enabler is the "chattering relay" (Normally Closed relay contacts connected in series with the relay coil). It has the following properties:
   - Creates randomness
   - Creates the actual complex mechanisms of the real event (e.g. contact arcing)
   - Simple, low in cost
   - Makes it practical to be used in multi temperature testing
c. R1-R2 simulate vehicle wiring inductance-resistance in the power and ground circuit and is important for developing voltage drops during transient conditions.
d. L1 simulates vehicle wiring inductance. R1 is to a degree redundant with L1.
e. L2 simulates vehicle inductive loads.

4.2.2 POWER CYCLE, POWER INTERRUPTIONS DURING START-UP

See Figure 2, 5, 12.

The purpose of this test is to verify proper DUT start-up during ignition key-on (ignition switch or relay bounce) which can be severe over the full vehicle temperature range. This is especially important for verifying proper software initialization. Relay 1 provides the power on-off cycle (Test 1) and relay 3 is connected in a chattering configuration to provide the random noise representing contact bounce at power up (Test 2). Relay 2 activates relay 3 during T1. Figure 5 shows a typical example of the output from this circuit. This test applies to DUT switched power input(s).

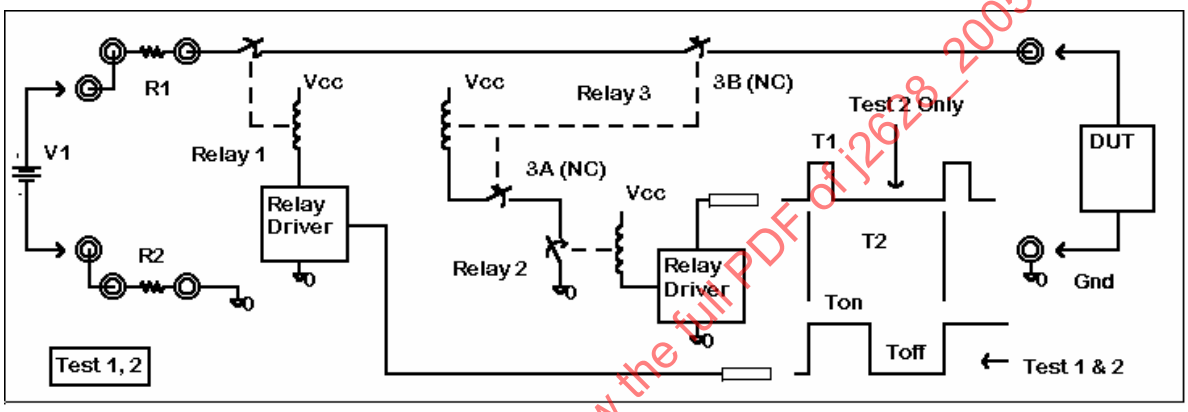

FIGURE 2—TEST 1,2 SCHEMATIC

4.2.3 INDUCTIVE TRANSIENTS - PULSE A1, A2, A1-A, C

See Figure 3, 6, 7, 8, 11.

Pulse A1 and A2 (reference 2.1.2), simulates the transients produced by switching off power to the DUT and an inductive load (L2) that is in parallel with the DUT. The pulse is produced at the start of period T1 when contact 3B opens. R3 provides adjustment of current through L2 to give different waveform characteristics (A1 = high current, A2 = low current). This test applies to DUT inputs connected to switched power.

Pulse A1-a is similar except that the opening of contact 3B is done by via a chattering relay to create a series of power interruptions during time T1 (also inductive transients due to L2). This simulates events due to intermittent connections - combination of contact fretting (corrosion) and vibration (e.g. hitting pothole) can cause such a connection (contributor to Trouble Not Indicated - TNI's). Figure 7 shows a typical example of the output from this circuit.

Pulse C (reference 2.1.2) is produced by switching off an inductive load that shares a common power feed with the DUT. This is the same configuration as for pulse A1-a except that the DUT connection point is different (power not removed from DUT). A1-a and C both apply to DUT inputs connected to switched power (when power is on) or directly to the vehicle battery.

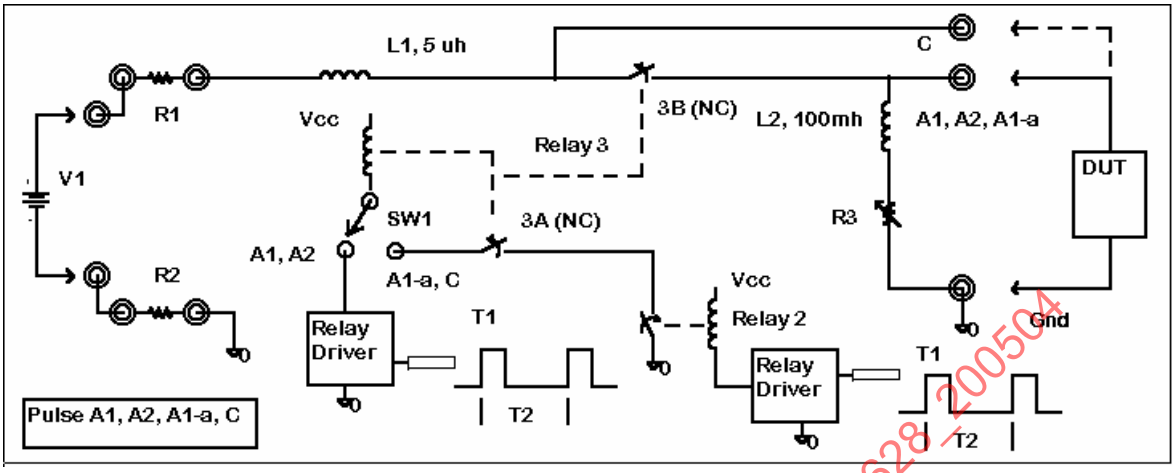

FIGURE 3—PULSE A1, A2, A1-A, C SCHEMATIC

4.2.4 INDUCTIVE TRANSIENTS - PULSE B1, B2

See Figure 4, 9, 10.

Pulse B1 and B2 (reference 2.1.2) simulates low side switching of an inductive load and applies to DUT signal inputs that are connected across the switch (e.g. A/C clutch monitor). The pulse is produced at the start of period T1 when relay 3 contact opens. R3 provides adjustment of current through L2 to give different waveform characteristics (B1 = high current, B2 = low current).

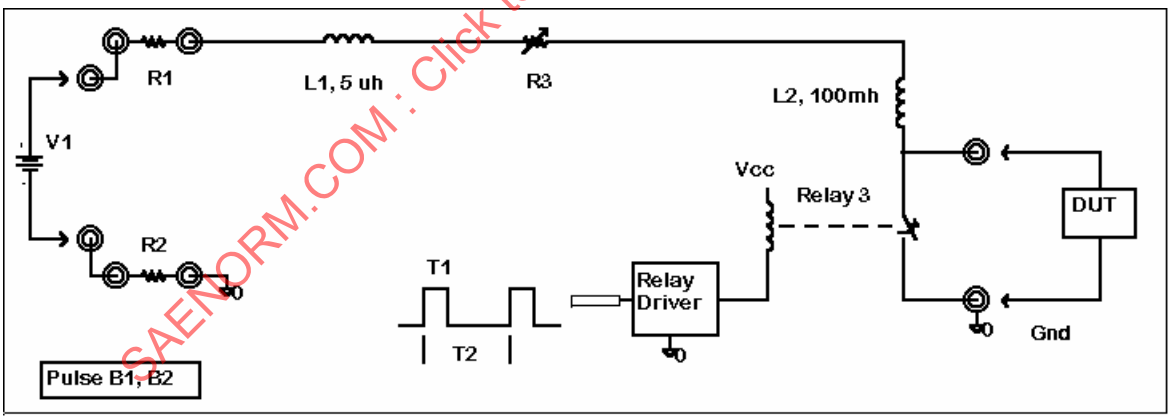

FIGURE 4—PULSE B1,B2 SCHEMATIC

4.2.5 VOLTAGE INTERRUPTIONS-TRANSIENTS WAVEFORMS

The following waveforms are examples of the various tests. Each waveform will vary due to the randomness of mechanical contacts. Waveforms are open circuit or loaded (100 ohms) as indicated, scale factors are per division.

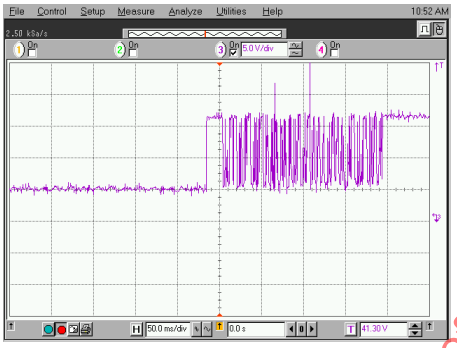

FIGURE 5—EXAMPLE OF POWER INTERRUPTIONS AT START UP (50ms, 5v)

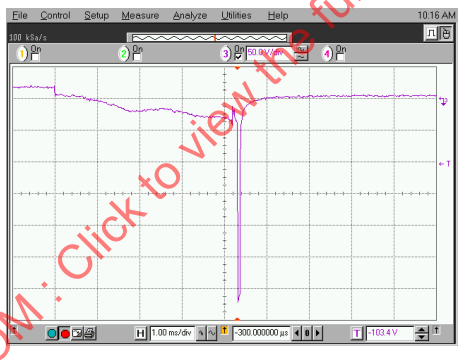

FIGURE 6A—EXAMPLE OF A1 (1ms, 50v)

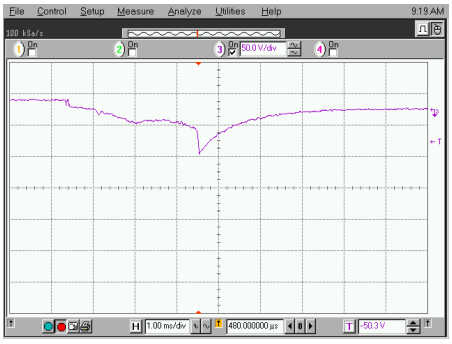

FIGURE 6B—A1 LOADED (1ms, 50v)

FIGURE 7A—EXAMPLE OF A1-a (2ms, 50v)

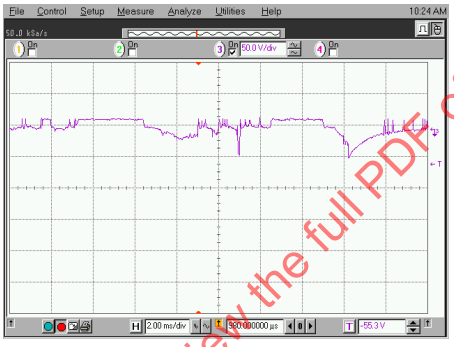

FIGURE 7B—A1-a LOADED (2ms, 50v)

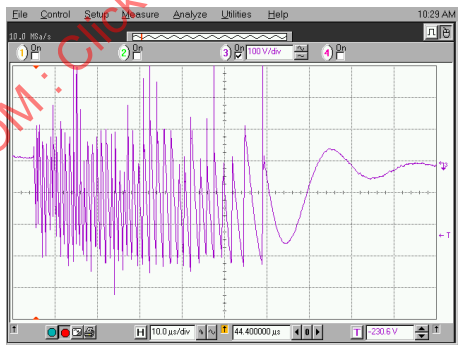

FIGURE 8—EXAMPLE OF A2 (10us, 100v),
MINIMAL TRANSIENT WHEN LOADED

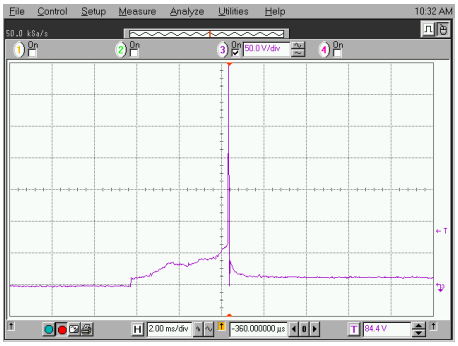

FIGURE 9A—EXAMPLE OF B1 (2ms, 50v)

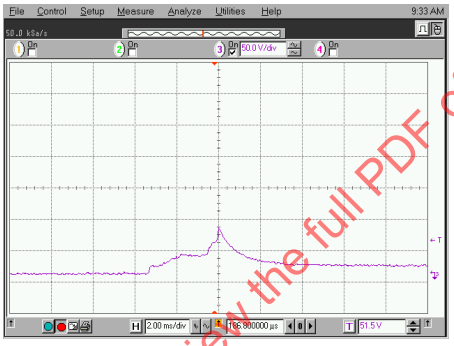

FIGURE 9B—B1 LOADED (2ms, 50v)

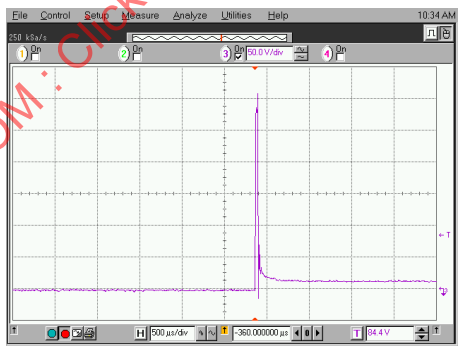

FIGURE 10—EXAMPLE OF B2 (500us, 50v)
MINIMAL TRANSIENT WHEN LOADED

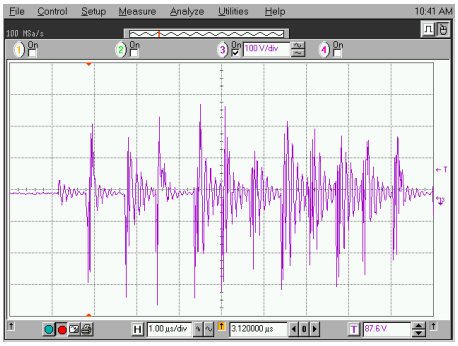

FIGURE 11A—EXAMPLE OF C (1us, 100v)

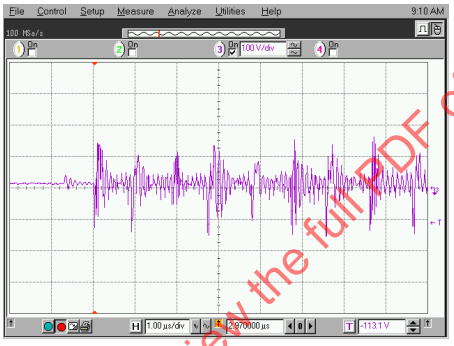

FIGURE 11B—C LOADED (1us, 100v)

4.3 Voltage Dips

This method verifies that a DUT is compatible with voltage dips most commonly experienced during engine starting. These dips can also occur as a result of a poor battery or connection condition when a high current load is activated. Voltage dips are different than dropouts in that drop outs are high impedance (open) while power dips are relatively low impedance. Voltage dips can also be used to evaluate DUT voltage regulator input step response by monitoring the regulator output and looking for stability (limited overshoot, limited ringing). Figure 12 shows two types of dips - single and double.

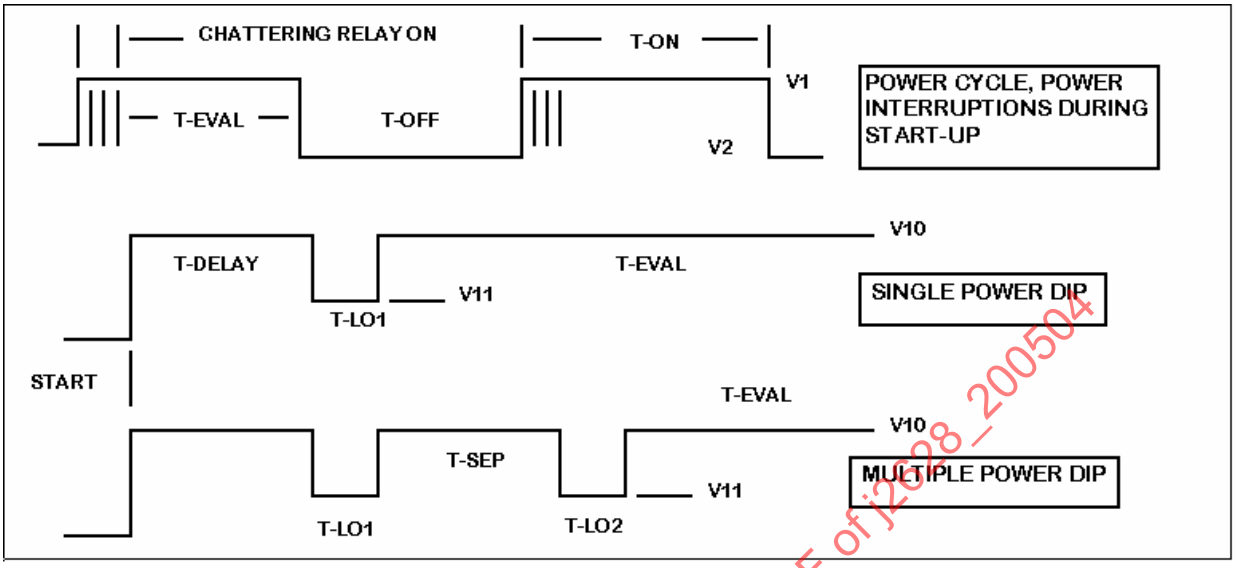

FIGURE 12—TIMING DIAGRAM

4.4 Current Draw

This method verifies that the DUT draws expected currents under a number of conditions. It is a good indicator for a number of things such as DUT degradation during environmental testing, detection of inadvertent changes to the design or manufacturing process, detection of sneak paths. Since the current can have a complex waveform, it is important to use a true RMS current meter with sufficient frequency response and resolution. In addition, sufficient time should be allowed for currents to stabilize.

5. Test Equipment

5.1 Simulator Components

a. Relay 1: Controls power on-off.
b. Relay 2: Controls activation of chattering relay 3.
c. Relay 3: Chattering relay characteristics:
   - Coil is 12 V AC (contains shading pole) operated at 12 V DC
   - R = 20 ohms nominal, Inductance = 100-150 mH @ 60 Hz
   - Contact rating = 10 amps (typical), DPDT
   - Example, P&B KUP-14A15-12
d. R1, R2 Ground, Power Resistors: Default = 10 watt, 0.1 ohms, wire wound.
e. L1 Series Inductance: Nominal = 5 microhenry. Osborne Transformer 8745.
f. L2 Inductive load used to create transients: Nominal = 100 mH at 100 Hz, 1 ohm. Osborne Transformer 32416.
g. R3: Controls current through inductors. High current = 6 ohms (25 watt), Low current = 106 ohms (5 watt).

h. DC Power Amplifier: DC - 20 kHz (3 dB), Range = 0-20 volts nominal (for 12 V systems), current capability consistent with DUT. Can be constructed with power Op Amps (e.g. LM12CLK) and switching power supplies (24 volt, 5 volt).
i. Arbitrary Waveform Generator (ARB): Able to create waveforms specified in this document.
j. Relay Drivers: Able to drive relay coils 1, 2, 3.

NOTE—Although separate circuits can be used, Figure 13 shows an all-inclusive version - Product Assurance Robustness (PAR) Tester. It includes 2 DC Power Amps and 2 ARB's (not required for this document but required for other similar type tests that need two different waveforms simultaneously - e.g. one for permanent battery feed and one for ignition switch feed).

5.2 Other Equipment

a. DUT exerciser-termination fixture. This provides DUT Input-Output terminations and a means of operating the DUT in its various modes.
b. Optional Setup: Since interface compatibility is a major issue, the DUT should also be tested with other DUT's that it interfaces with. Configure so that it will fit into a temperature chamber (e.g. if too big to lay out flat on a breadboard, configure as stacked multiple smaller sub-breadboards). It should also allow injection of test signals. See Figure 14 for example.
c. Variable DC Power Supply - Capable of providing specified voltages at DUT current requirements. Shall not be affected by simulator (e.g. chattering relay noise).
d. Data Acquisition - Capable of monitoring the DUT signals and tracking when the DUT response exceeds predetermined limits. Shall also log stress conditions when these limits are exceeded.
e. Thermal Chamber - Capable of temp range required and nominal ramp rate of 3-5 °C per minute.
f. True RMS current meter. Consistent with DUT frequency content and resolution requirements.

5.3 Test Equipment Tolerances - Characterization

Tolerances (unless otherwise specified): Voltage = ± 0.5 volts, Current = 10 mA or 0.1 mA depending on test, Time-Resistance = ± 10 %, Temperature = ± 2 °C.

Even though some of these tests are intentionally random in nature (its real advantage) experience has shown that the DUT responses are very repeatable. The voltage waveforms produced should be periodically observed for degradation with an oscilloscope to verify correct waveform characteristics (many new scopes allow measurement of average and standard deviation). The amount of degradation over time is a function of the currents that the relay contacts must provide to the DUT and how much the relay is used.

Use reference 2.1.2 for transient characteristics. For the tests requiring use of the DC power amplifier, verify accuracy of the output waveforms both open circuit and loaded. The loaded waveforms should draw similar currents that the DUT would (default = 10 ohms). Maximum change from open circuit to loaded (amplitude, frequency response) = 10 %.

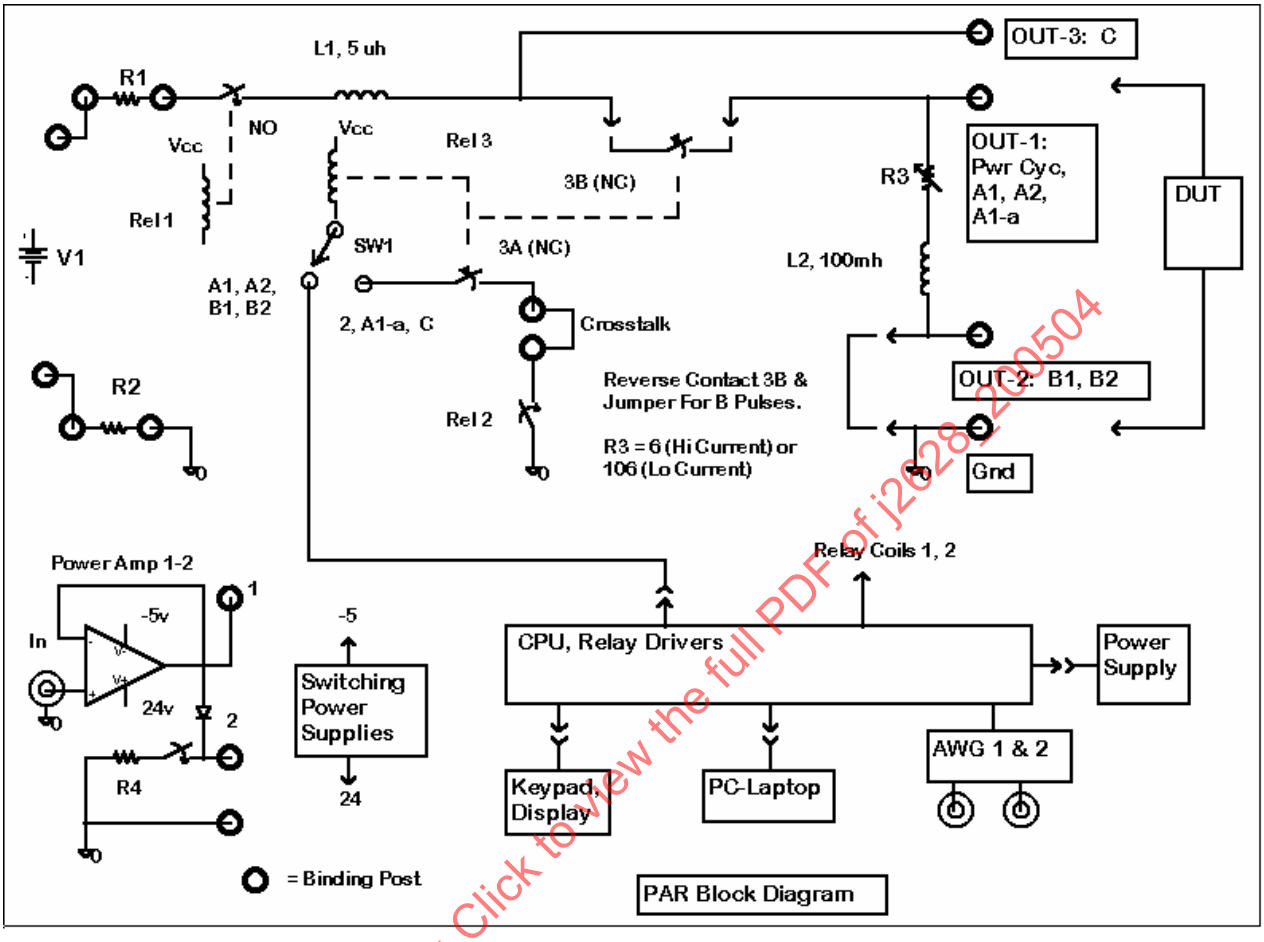

FIGURE 13—PAR TESTER

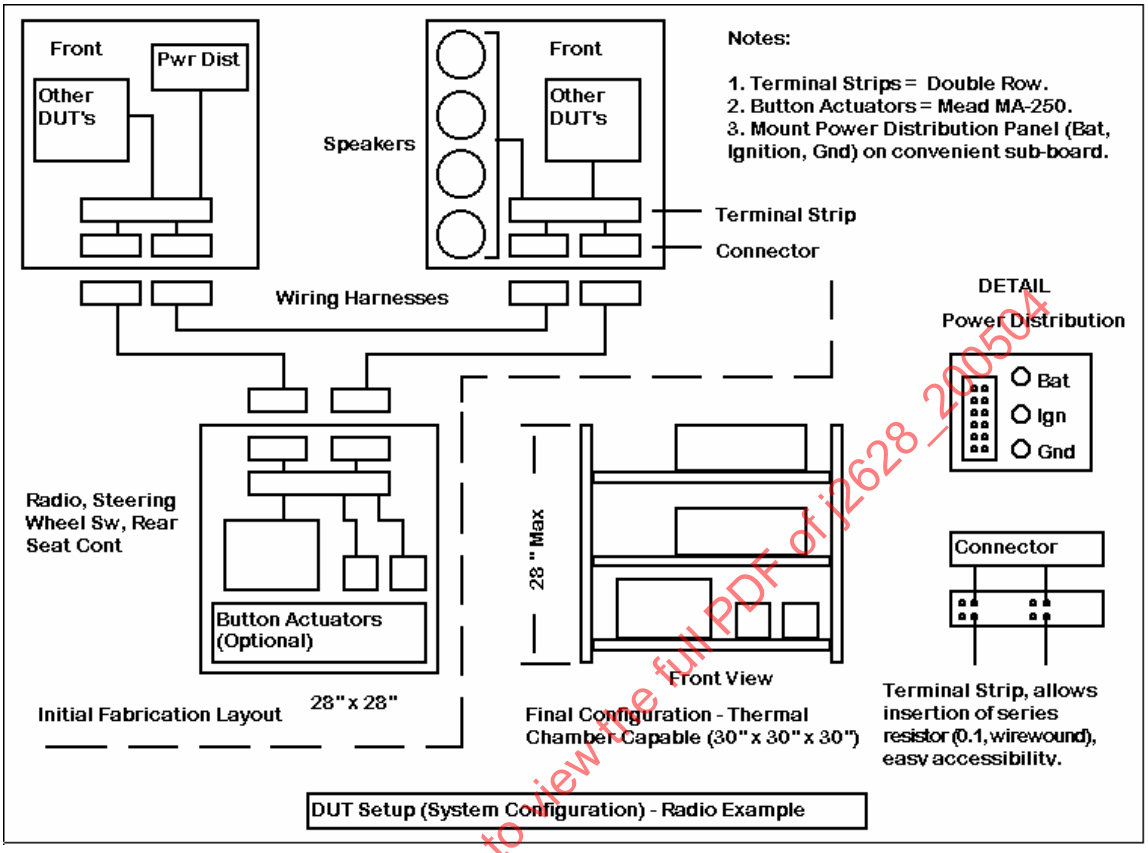

FIGURE 14—DUT SETUP - SYSTEM CONFIGURATION

6. Test Procedures

6.1 General

a. Before a test plan is developed, the DUT shall undergo a Design Review by technical experts to determine where testing should be focused.

b. The DUT shall be connected to the actual operating devices (loads, sensors, etc.) using a test harness or the production wiring harness, as agreed upon between the vendor and the customer. If the original operating devices are not available, they may be simulated by methods outlined in SAE J1113-1.

c. For many of these methods, system and interface issues shall be addressed. Typical examples are:
   - DUT output coil (e.g. solenoid) increase in resistance with temperature (may require placing load in thermal chamber with DUT).
   - Wiring-connector resistance-inductance in ground and/or power circuits.
   - DUT switch input resistance (default: closed switch = 50 ohms, open switch = 50k).

d. Due to R1 and R2, the voltage at the DUT may be different than the power supply voltage.

e. Place DUT in typical operating mode (most temp, voltage sensitive) and monitor key output signals.
f. For DUT's with communications bus, operate DUT in mode that creates near maximum bus activity. Note: Communications Bus analyzers can be sensitive to electrical noise and may need filtering or optical coupler.
g. If the DUT exhibits abnormal behavior during testing, monitor appropriate internal DUT signals to determine root cause (e.g. voltage regulator outputs, microprocessor resets).

6.2 Voltage-Temperature Design Margins

a. If practical, remove DUT temperature constraints to extend temp limits (e.g. instrument cluster plastic housing).
b. Determine applicable test method. Table 1 = More rigorous to determine design margin envelope. Table 2 = Abbreviated (e.g. Pre-Qual, Conformity) to verify at least a small design margin.

TABLE 1—EVALUATION METHOD A

Step	Action	Parameters	Result
	Ambient Temp		
1	Ramp voltage [1].	V-nom to 20 to 0 to V-nom, approx 10 v/minute. [2]	Predetermined response, No Lock-ups
2	Determine Voltage Limits		UOL-V (T-amb), hi/lo [3, 4] LOL-V (T-amb), lo/hi
3	Apply Voltage Interruptions, Transients.	Ref 6.3	Ref 6.3
4	Repeat on 2nd DUT		Verify similar results
	Low Temp		
5	Lower temp, power on	T3 – 5 °C, V-nom	Note DUT transition operation.
6	Turn power off	10 minutes	
7	Power on	V-nom	Verify proper DUT start-up.
8	Repeat voltage ramp and determine limits.		UOL-V (T3 – 5 °C), hi/lo [3, 4] LOL-V (T3 – 5 °C), lo/hi
9	Repeat Step 3.	T3 – 5 °C	
10	Step to lower temp with power on	T3 – 10 °C, V-nom	
11	Turn power off	10 minutes	
12	Power on	V-nom	Verify proper DUT start-up.
13	Repeat steps 10-12 until low temp limit found (Steps = 5 °C, limit to 15 °C beyond spec).	LOL-T (V-nom)	[4]
14	Compute T-lo = LOL-T (V-nom) + 5 C		T-lo
15	Repeat voltage ramp and determine limits.	T-lo	UOL-V (T-lo), hi/lo [3, 4] LOL-V (T-lo), lo/hi
16	Repeat step 15 (at T-lo) on 2nd DUT		Verify similar results
	High Temp		
17	Increase temp, power on	T4 + 5 °C, V-nom	Note DUT transition operation.
18	Turn power off	10 minutes	
19	Power on	10 minutes, V-nom	Verify proper DUT start-up.
20	Repeat voltage ramp and determine limits.		UOL-V (T4 + 5 °C), hi/lo [3, 4] LOL-V (T4 + 5 °C), lo/hi
21	Repeat Step 3.	T4 + 5 °C	
22	Step to next higher temp with power on	T4 + 10 °C, V-nom	
23	Turn power off	10 minutes	
24	Power on	10 minutes, V-nom	Verify proper DUT start-up.
25	Repeat steps 22-24 until high temp limit found (Steps = 5 °C, limit to 15 °C beyond spec).	UOL-T (V-nom)	[4]
26	Compute T-hi = UOL-T (V-nom) - 5 °C		T-hi
27	Repeat voltage ramp and determine limits.	T-hi	UOL-V (T-hi), hi/lo [3, 4] LOL-V (T-hi), lo/hi
28	Repeat step 27 (at T-hi) on 2nd DUT		Verify similar results

1. Ramp must be linear, not course digital steps. If applicable, connect Battery and Ignition inputs together.
2. 20 volts is considered reasonable upper limit. The only DC voltage higher than 20 volts in a vehicle is double voltage jump start (24 volts).
3. Hi-Lo values due to DUT hysteresis.
4. These limits are where DUT operation is erratic or ceases to operate.