

Submitted for recognition as an American National Standard

**Physical Layer, 250K bits/s, Twisted Shielded Pair**

**Foreword**—This series of SAE Recommended Practices have been developed by the Truck and Bus Control and Communications Network Subcommittee of the Truck and Bus Electrical Committee. The objectives of the subcommittee are to develop information reports, recommended practices, and standards concerned with the requirements design and usage of devices which transmit electronic signals and control information among vehicle components. The usage of these recommended practices is not limited to truck and bus applications. Other applications may be accommodated with immediate support being provided for construction and agricultural equipment, and stationary power systems.

These SAE Recommended Practices are intended as a guide toward standard practice and are subject to change to keep pace with experience and technical advances.

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**1. Scope**—These SAE Recommended Practices are intended for light- and heavy-duty vehicles on- or off-road as well as appropriate stationary applications which use vehicle derived components (e.g., generator sets). Vehicles of interest include but are not limited to: on- and off-highway trucks and their trailers; construction equipment; and agricultural equipment and implements.

The purpose of these documents is to provide an open interconnect system for electronic systems. It is the intention of these documents to allow electronic devices to communicate with each other by providing a standard architecture.

**2. References**—General information regarding this series of recommended practices is found in SAE J1939.

**2.1 Applicable Publications**—The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1113/13—Electromagnetic Compatibility Measurement Procedure for Vehicle Components—  
Part 13—Immunity to Electrostatic Discharge

(R) SAE J1128—Low-Tension Primary Cable

(R) SAE J1939 (Draft)—Recommended Practice for a Serial Control and Communication Vehicle Network

2.1.2 ISO Publication—Available from ANSI, 11 West 42nd Street, New York, NY 10036-8002.

(R) ISO 6722— Road vehicles—Unscreened low-tension cables

2.1.3 Military Publication—Available from DODSSP, Subscription Services Desk, Building 4D, 700 Robins Avenue, Philadelphia, PA 19111-5094.

(R) MIL-C-85485—Cable, Electric, Filter Line

2.2 Related Publication—The following publication is provided for information purposes only and is not a required part of this document.

2.2.1 ISO PUBLICATION—Available from ANSI, 11 West 42nd Street, New York, NY 10036-8002.

ISO 11898—Road vehicles—Interchange of digital information—Controller Area Network (CAN) for high speed communication.

### 3. Network Physical Description

**3.1 Physical Layer**—The physical layer is a realization of an electrical connection of a number of ECUs (Electronic Control Units) to a network. The total number of ECUs will be limited by electrical loads on the bus line. This maximum number of ECUs is fixed to 30, on a given segment, due to the definition of the electrical parameters given in the present specification

**3.2 Physical Media**—This document defines a physical median of shielded twisted pair. These 2 wires have a characteristic impedance of 120 Ω and are symmetrically driven with respect to the electrical currents. The designations of the individual wires are CAN\_H and CAN\_L. The names of the corresponding pins of the ECUs are also denoted by CAN\_H and CAN\_L, respectively. The third connection for the termination of the shield is denoted by CAN\_SHLD.

**3.3 Differential Voltage**—The voltages of CAN\_H and CAN\_L relative to ground of each individual ECU are denoted by  $V_{CAN\_H}$  and  $V_{CAN\_L}$ . The differential voltage between  $V_{CAN\_H}$  and  $V_{CAN\_L}$  is defined by Equation 1:

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad (Eq.1)$$

- 3.4 Bus Levels**—The bus lines can have one of the two logical states, recessive or dominant (see Figure 1). In the recessive state,  $V_{CAN\_H}$  and  $V_{CAN\_L}$  are fixed to a mean voltage level.  $V_{diff}$  is approximately zero on a terminated bus. The recessive state is transmitted during bus idle or a recessive bit.

The dominant state is represented by a differential voltage greater than a minimum threshold. The dominant state overwrites the recessive state and is transmitted during a dominant bit.

- 3.5 Bus Levels During Arbitration**—A dominant and recessive bit imposed on the bus lines during a given bit time by two different ECUs will result in a dominant bit.

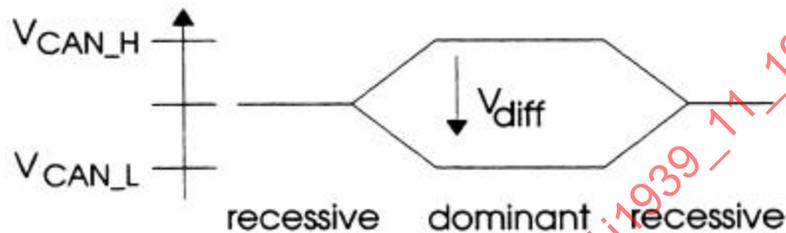


FIGURE 1—PHYSICAL BIT REPRESENTATION

- 3.6 Common Mode Bus Voltage Range**—The common mode bus voltage is defined as the boundary voltage levels of CAN\_H and CAN\_L, measured with respect to the individual ground of each ECU, for which proper operation is guaranteed when all ECUs are connected to the bus line.
- 3.7 Bus Termination**—The bus line is electrically terminated at each end with a load resistor denoted by  $R_L$ .  $R_L$  shall not be located within an ECU because the bus will lose termination if one of these ECUs is disconnected (see Figure 2). (Also see 5.2.3 for resistor characteristics.)
- 3.8 Internal Resistance**—The internal resistance,  $R_{in}$ , of an ECU is defined as the resistance seen between CAN\_H (or CAN\_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).
- 3.9 Differential Internal Resistance**—The differential internal resistance,  $R_{diff}$ , is defined as the resistance seen between CAN\_H and CAN\_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).
- 3.10 Internal Capacitance**—The internal capacitance,  $C_{in}$ , of an ECU is defined as the capacitance seen between CAN\_H (or CAN\_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).
- 3.11 Differential Internal Capacitance**—The differential internal capacitance,  $C_{diff}$ , of an ECU is defined as the capacitance seen between CAN\_H and CAN\_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).
- 3.12 Bit Time**—The bit time,  $t_B$ , is defined as the duration of one bit (see Figure 5). Bus management functions executed within this bit time, such as ECU synchronization behavior, network transmission delay compensation, and sample point positioning, are defined by the programmable bit timing logic of the CAN protocol IC (Integrated Circuit). The bit time for this document is 4  $\mu$ s corresponding to 250 Kbit/s.

Various names for the bit segments are used by suppliers of CAN protocol ICs and it is possible that two bit segments are defined as one.

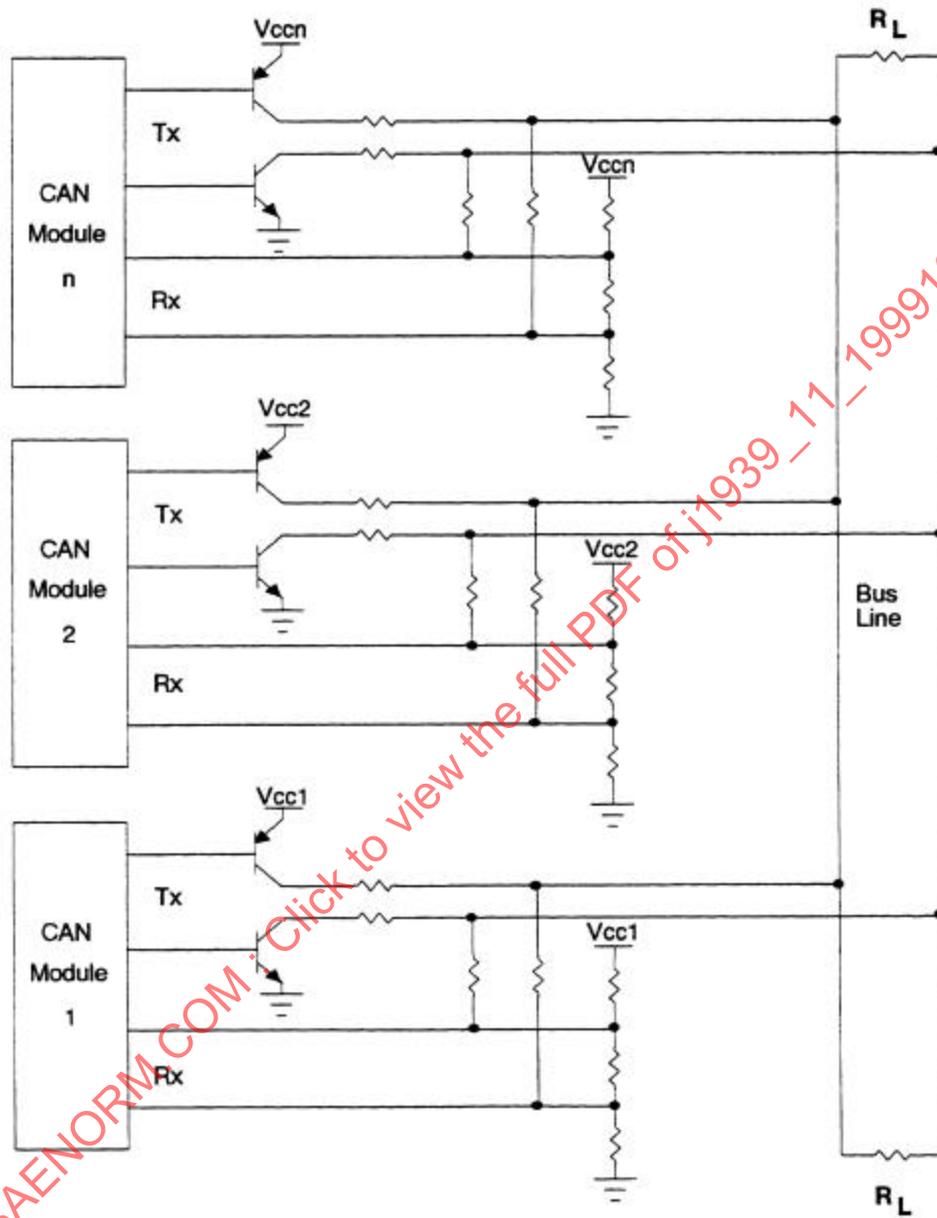


FIGURE 2—PHYSICAL LAYER FUNCTIONAL

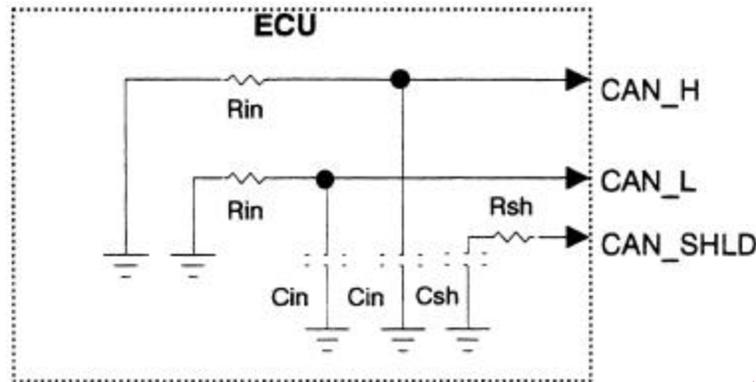


FIGURE 3—ILLUSTRATION OF INTERNAL CAPACITANCE AND RESISTANCE OF AN ECU IN THE RECESSIVE STATE

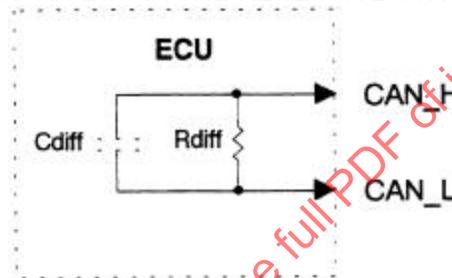


FIGURE 4—ILLUSTRATION OF DIFFERENTIAL INTERNAL CAPACITANCE AND RESISTANCE OF AN ECU IN THE RECESSIVE STATE

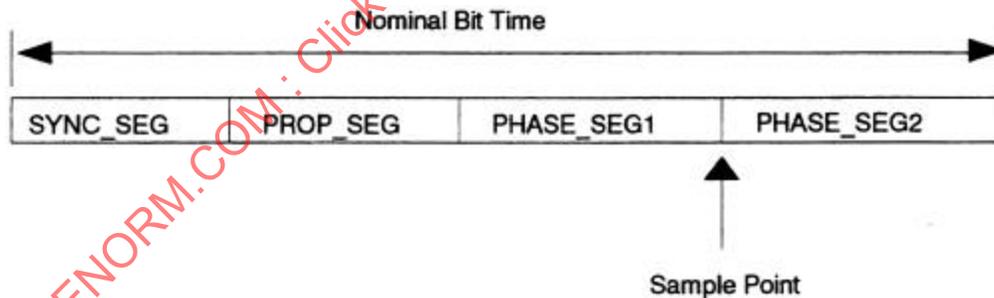
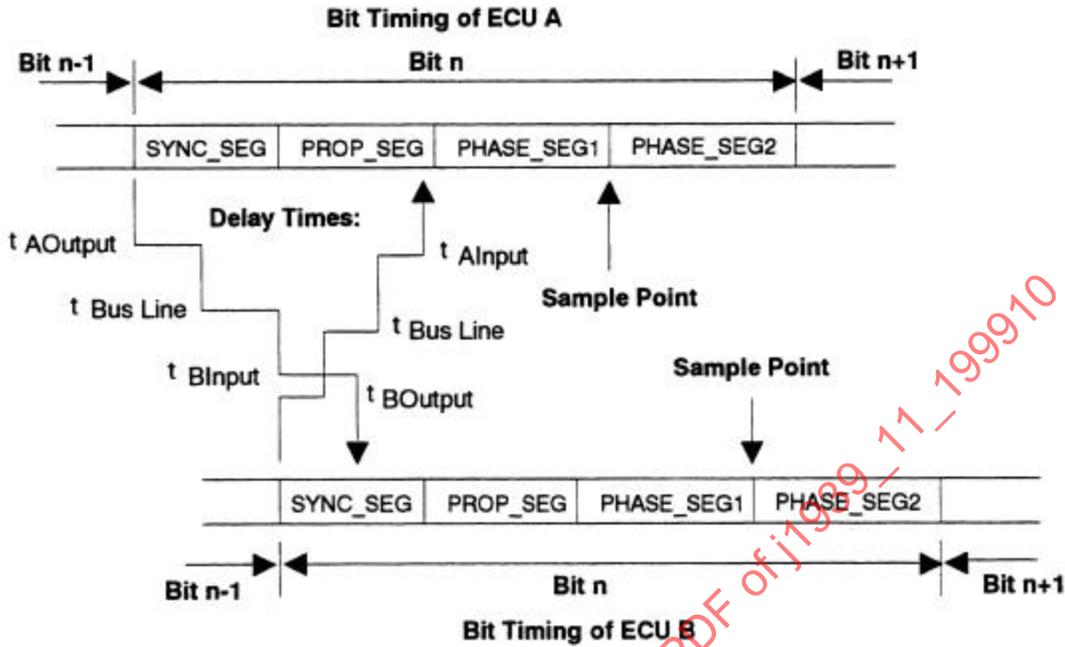


FIGURE 5—PARTITION OF THE BIT

- a. SYNC SEG—This part of the bit time is used to synchronize the various ECUs on the bus. An edge is expected within this bit segment.
- b. PROP SEG—This part of the bit time is used to compensate for the physical delay times within the network. These delay times are caused by the propagation time of the bus line and the internal delay time of the ECUs.
- c. PHASE SEG1, PHASE SEG2—These Phase-Buffer-Segments are used to compensate for phase-errors and can be lengthened or shortened by resynchronization.
- d. Sample-Point—The Sample-Point is the point of time at which the bus level is read and interpreted as the value of that respective bit. Its location is at the end of PHASE\_SEG1.

- 3.13 Internal Delay Time**—The internal delay time of an ECU,  $t_{\text{ECU}}$ , is defined as the sum of all asynchronous delays that occur along the transmission and reception path of the individual ECUs, relative to the bit timing logic unit of the protocol IC. For more details, see Figure 6.
- a. Synchronization—Hard Synchronization and Resynchronization are the two forms of synchronization. They obey the following rules:
    1. Only one Synchronization within one bit time is allowed.
    2. An edge will be used for Synchronization only if the value detected at the previous Sample Point (previously read bus value) differs from the bus value immediately after the edge.
    3. Hard Synchronization is performed during said edge whenever there is a 'recessive' to 'dominant' edge.
    4. All other 'recessive' to 'dominant' edges fulfilling rules 1 and 2 will be used for Resynchronization with the exception that a transmitter will not perform Resynchronization as a result of a 'recessive' to 'dominant' edge with a positive Phase Error if only 'recessive' to 'dominant' edges are used for Resynchronization.
  - b. Synchronization Jump Width (SJW)—As a result of Synchronization PHASE\_SEG1 may be lengthened or PHASE\_SEG2 may be shortened. The amount of lengthening or shortening of the Phase Buffer bit Segments has an upper bound given by the Synchronization Jump Width. The Synchronization Jump Width is less than or equal to PHASE\_SEG1.

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Notes:

- 1) The sum of output and input ECU delays, with ECU disconnected from the bus relative to the bit timing logic is critical. The important characteristic parameter of an ECU is (see 3.12)

$$t_{ECU} = t_{Output} + t_{Input} \quad [\text{Where } \_ = \text{ECU (A,B...)}]$$

- 2) For proper arbitration, the following condition must be met:

$$t_{AECU} + t_{BECU} + 2 \cdot t_{Bus\ line} \leq t_{PROP\_SEG} + (t_{PHASE\_SEG1} - t_{sJW})$$

SYNC\_SEG is not taken into account as it is possible that this segment is lost if there is a phase shift between modules.

$t_{sJW}$  is part of PHASE\_SEG1 to compensate phase-errors. It is subtracted from the available time as it is possible that a spike may cause a missynchronization with a phase shift of  $t_{sJW}$ .

That means the leading transmitting bit timing logic with respect to synchronization of ECU A must be able to know the correct bus level of bit n at the sample point. The tolerable values of  $t_{ECU}$  strongly depends on the bit rate and line length of the bus and of the possible bit timing as shown by the arbitration condition.

- 3) The acceptable crystal tolerances of the protocol ICs and the potential for missynchronization is determined by PHASE\_SEG1 and 2.

FIGURE 6—TIME RELATIONSHIP BETWEEN BIT TIMING LOGIC OF ECU A AND B DURING ARBITRATION

**3.14 CAN Bit Timing Requirements**—It is necessary to ensure that a reliable network can be constructed with components from multiple suppliers. Without any bit timing restrictions, different devices may not be able to properly receive and interpret valid messages. Under certain network conditions it may also be possible for a particular device to have unfair access to the network. In addition, it makes network management (system diagnostics) much more difficult. CAN chip suppliers also recommend that all devices on a given network be programmed with the same bit timing values.

(R) All CAN ICs divide the bit time into smaller sections defined as  $t_q$  (time quantum). For most CAN ICs  $1 t_q = 250 \text{ ns}$  (with a 16 MHz clock) (determined by oscillator frequency and baud rate prescaler).

(R) Therefore specific values for the bit timing registers need to be defined to ensure that a reliable network exists for all nodes based on the best tradeoffs between propagation delay and clock tolerance. Note that there are some differences in bit segment definition between manufacturers of CAN devices.

(R) It is recommended that a  $t_q$  be selected which permits the sample point (see Figure 5) to be located as close to but not later than  $7/8$  of a bit time ( $0.875 \times 4 \mu\text{s} = 3.5 \mu\text{s}$ ). This provides the best tradeoff between propagation delay and clock tolerance.

(R) The following values are recommended for typical controller ICs running at standard clock frequencies. At other frequencies, different values may have to be selected to maintain the sample point as close as possible but not later than the preferred time.

(R) 16 MHz  
 sample point =  $0.875 t_b$   
 $t_q = 250 \text{ ns}$  (16  $t_q/\text{bit}$ )  
 $t_{\text{sync}} = 250 \text{ ns}$  (1  $t_q$ )  
 $\text{TSEG1} = 3.25 \mu\text{s}$  (13  $t_q$ )  
 $\text{TSEG2} = 500 \text{ ns}$  (2  $t_q$ )

(R) 20 MHz  
 sample point =  $0.85 t_b$   
 $t_q = 200 \text{ ns}$  (20  $t_q/\text{bit}$ )  
 $t_{\text{sync}} = 200 \text{ ns}$  (1  $t_q$ )  
 $\text{TSEG1} = 3.2 \mu\text{s}$  (16  $t_q$ )  
 $\text{TSEG2} = 600 \text{ ns}$  (3  $t_q$ )

(R)  $\text{SJW} = 1 t_q$  (SJW is a part of TSEG1 and TSEG2)  
 Total Bit Time =  $\text{TSEG1} + \text{TSEG2} + t_{\text{sync}} = 13 + 2 + 1 = 16 t_q = 4 \mu\text{s}$   
 (Example for 16 MHz clock)

$\text{PROP\_SEG} + \text{PHASE\_SEG1} = \text{TSEG1}$   
 $\text{PHASE\_SEG2} = \text{TSEG2}$ ,  
 $\text{SYNC\_SEG} = \text{SYNC\_SEG}$

This selection for the bit timing registers generally requires the use of Crystal Oscillators at all nodes so that the clock tolerance given in Table 1 can be achieved.

(R)

TABLE 1<sup>3/4</sup> AC PARAMETERS OF AN ECU DISCONNECTED FROM THE BUS LINE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bit time <sup>(1)</sup>	$t_B$	3.998	4.000	4.002	$\mu\text{s}$	250 Kbit/s
Internal Delay Time <sup>(2)</sup>	$t_{\text{ECU}}$	0.0		0.9	$\mu\text{s}$	
Internal Capacitance <sup>(3)</sup>	$C_{\text{in}}$	0	50	100	pF	250 Kbit/s for CAN_H and CAN_L relative to Ground
Differential Internal Capacitance <sup>(3)</sup>	$C_{\text{diff}}$	0	25	50	pF	
Available Time <sup>(4)</sup>	$t_{\text{avail}}$	2.5			$\mu\text{s}$	40 m bus length
Signal Rise, Fall Time <sup>(5)</sup>	$t_R, t_F$	200		500	ns	measured from 10% to 90% of the signal

- Including initial tolerance, temperature, aging, etc.
- The value of  $t_{\text{ECU}}$  has to be guaranteed for a differential voltage of  $V_{\text{diff}} = 1.0 \text{ V}$  for a transition from recessive to dominant and of  $V_{\text{diff}} = 0.5 \text{ V}$  for a transition from dominant to recessive. With the bit timing from the example of note 1, a CAN-Interface delay of 500 ns is possible (controller not included) with a reserve of about 300 ns. This allows slower slopes (R3 and R4 in Figures A1 and A2) and input filtering (R5, R6, C1, C2 in Figures A1 and A2). It is recommended to use this feature due to EMC.  
The minimal internal delay time may be zero. The maximum tolerable value is determined by the bit timing and the bus delay time.
- In addition to the internal capacitance restrictions a bus connection should also have an inductance as low as possible. The minimum values of  $C_{\text{in}}$  and  $C_{\text{diff}}$  may be 0, the maximum tolerable values are determined by the bit timing and the network topology parameters  $l$  and  $d$  (see Table 8). Proper functionality is guaranteed if occurring cable resonant waves do not suppress the dominant differential voltage level below  $V_{\text{diff}} = 1 \text{ V}$  and do not increase the recessive differential voltage level above  $V_{\text{diff}} = 0.5 \text{ V}$  at each individual ECU (see Tables 3 and 4).
- The available time results from the bit timing unit of the protocol IC. For example, this time in most controller ICs corresponds to TSEG1. Due to missynchronization it is possible to lose the length of SJW. So the available time ( $t_{\text{avail}}$ ) with one missynchronization is TSEG1-SJW ms. A tq time of 250 ns and SJW = 1 tq, TSEG1 = 13 tq, TSEG2 = 2tq results in  $t_{\text{avail}} = 3.00 \mu\text{s}$ .
- The load on the ECU for the purpose of this parameter should be 60 ohms between CAN\_H and CAN\_L in parallel with 200 pf of capacitance

**4. Functional Description**—As shown in Figure 2, the linear bus line is terminated with a load resistor  $R_L$  on each end. These resistors suppress reflections.

The bus is in the recessive state if the bus transmitters of all ECUs on the bus are switched off. In this case, the mean bus voltage is generated by the passive biasing circuit in all ECUs on the bus. In Figure 2 this is realized by the resistor network that defines the reference for the receive operation.

A dominant bit is sent to the bus line if the bus driver circuit of at least one unit is switched on. This induces a current flow through the terminating resistors, and consequently, a differential voltage between the two wires. The dominant and recessive states are passed by a resistor network which transforms the differential voltages of the bus line to corresponding recessive and dominant voltage levels at the comparator input of the receiving circuitry for detection.

## 5. Electrical Specification

**5.1 Electrical Data**—The parameter specifications in these tables must be fulfilled throughout the operating temperature range of every ECU. These parameters allow up to a maximum of 30 ECUs to be connected to a given bus segment.

**5.1.1 ELECTRONIC CONTROL UNIT**—The limits given in the Tables 1 to 4, apply to the CAN\_H and CAN\_L pins of each ECU, with the ECU disconnected from the bus line (see Section 6).

**TABLE 2<sup>3/4</sup> LIMITS OF  $V_{CAN\_H}$  AND  $V_{CAN\_L}$  OF AN ECU DISCONNECTED FROM THE BUS LINE FOR NOMINAL BATTERY VOLTAGES OF 12 V AND 24 V**

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Max. Voltage	$V_{CAN\_H}$	-3.0		16.0	V	nominal battery voltage 12 V
	$V_{CAN\_L}$	-3.0		16.0	V	
Max. Voltage	$V_{CAN\_H}$	-3.0		32.0	V	nominal battery voltage 24 V
	$V_{CAN\_L}$	-3.0		32.0	V	

5.1.1.1 *Absolute Maximum Ratings*—The limits given in Table 2 are the absolute maximum DC voltages which can be connected to the bus lines without damage to transceiver circuits. Although the link is not guaranteed to operate at these conditions, there is no time limit (operating CAN ICs will go “error passive” after a period of time).

5.1.1.2 *DC Parameters*—Tables 3 and 4 define the DC parameters for the recessive and dominant states, respectively, of an ECU disconnected from the bus.

**TABLE 3<sup>3/4</sup> DC<sup>3/4</sup> PARAMETERS FOR THE RECESSIVE STATE OF AN ECU DISCONNECTED FROM THE BUS LINE<sup>3/4</sup> RECESSIVE STATE**

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Voltage	$V_{CAN\_H}$	2.0	2.5	3.0	V	no load
	$V_{CAN\_L}$	2.0	2.5	3.0	V	
Output Behavior						
Differential Voltage Output Behavior	$V_{diff\_or}$	-1200		50	mV	no load
Differential Internal Resistance	$R_{diff}$	10		100	k $\Omega$	no load
Internal Resistance <sup>(1)</sup>	$R_{in}$	5		15	k $\Omega$	no load
Input Range	$V_{diff}$	-1.0		0.5	V	(2) (3) (4)

- In order to generate symmetrical waveforms and minimize EMI radiation,  $R_{in}$  of CAN\_H and CAN\_L should have almost the same value. The deviation has to be less than 5% relative to each other.
- The equivalent of the two terminating resistors in parallel (60  $\Omega$ ) is connected between CAN\_H and CAN\_L.
- Reception must be ensured within the common mode voltage range defined in Table 5 and Table 6, respectively.
- Although  $V_{diff} < -1.0$  V is only possible during fault conditions it should be interpreted as recessive.

**TABLE 4<sup>3/4</sup> DC<sup>3/4</sup> PARAMETERS FOR THE DOMINANT STATE OF AN ECU DISCONNECTED FROM THE BUS LINE<sup>3/4</sup> DOMINANT STATE**

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Voltage Output Behavior	$V_{CAN\_H}$	3.0	3.5	5.0	V	(1)
	$V_{CAN\_L}$	0.0	1.5	2.0	V	
Differential Voltage Output Behavior	$V_{diff\_ld}$	1.5	2.0	3.0	V	(1)
Input Range	$V_{diff}$	1.0		5.0	V	(1) (2)

- The equivalent of the two terminating resistors in parallel (60  $\Omega$ ) is connected between CAN\_H and CAN\_L.
- Reception must be ensured within the common mode voltage range defined in Tables 5 and 6, respectively.

**TABLE 5<sup>3/4</sup> BUS VOLTAGE PARAMETERS FOR THE RECESSIVE STATE WITH ALL ECUs CONNECTED TO THE BUS LINE<sup>3/4</sup> RECESSIVE STATE**

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage on the bus line	$V_{CAN\_L}$	0.1	2.5	4.5	V	measured with respect to ground of each ECU
Differential Bus Voltage <sup>(1)</sup>	$V_{diff}$	-400	0	12	mV	measured at each ECU connected to the bus line

1. The differential bus voltage is determined by the output behavior of all ECUs during the recessive state. Therefore,  $V_{diff}$  is approximately zero (see Table 3). The minimum value is determined by the requirement that a single transmitter must be able to represent a dominant bit by a minimum value of  $V_{diff} = 1.2$  V.

**TABLE 6<sup>3/4</sup> BUS VOLTAGE PARAMETERS FOR THE DOMINANT STATE WITH ALL ECUs CONNECTED TO THE BUS LINE<sup>3/4</sup> DOMINANT STATE**

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage on Bus <sup>(1)</sup>	$V_{CAN\_H}$		3.5	7.0	V	measured with respect to ground of each ECU
	$V_{CAN\_L}$	-2.0	1.5			
Differential Bus Voltage <sup>(2)</sup>	$V_{diff}$	1.2	2.0	3.0	V	Measured at each ECU connected to the bus line
				5.0	V	

1. The minimum value of  $V_{CAN\_H}$  is determined by the minimum value of  $V_{CAN\_L}$  plus the minimum value of  $V_{diff}$ . The maximum value of  $V_{CAN\_L}$  is determined by the maximum value of  $V_{CAN\_H}$  minus the value of  $V_{diff}$ .

2. The bus load increases as ECUs are added to the network, due to  $R_{diff}$ . Consequently,  $V_{diff}$  decreases. The minimum value of  $V_{diff}$  determines the number of ECUs allowed on the bus. The maximum value of  $V_{diff}$  is defined by the upper limit during arbitration. This maximum value of  $V_{diff}$  for single operation must not exceed 3 V.

5.1.1.3 AC Parameters—Table 1 defines the AC Parameter requirements of the ECUs.

(R) 5.1.2 BUS VOLTAGES—OPERATIONAL—The parameters specified in Tables 5 and 6 apply when all ECUs (between 2 and 30) are connected to a correctly terminated bus line. The maximum allowable ground offset between any ECUs on the bus is 2 V. The voltage extremes associated with this offset would occur in the dominant state (see Table 6).

5.1.3 ELECTROSTATIC DISCHARGE (ESD)—CAN\_H and CAN\_L should be tested while disconnected from the bus line according to SAE J1113/13 for ESD using 15 kV.

(R) 5.1.4 EXAMPLE PHYSICAL LAYER CIRCUITS—There are many possible discrete and integrated physical layer circuits which meet the previous requirement. Examples of implementations are shown in Appendix A.

5.2 Physical Media Parameters—The following sections describe the characteristics of the cable, termination, and topology of the network. (See Table 7.)

(R)

TABLE 7¾ PHYSICAL MEDIA PARAMETERS FOR TWISTED SHIELDED CABLE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Impedance	Z	108	120	132	Ω	Three meter sample length measured at 1 Mhz between the two sig. wires, with shield grounded, using open/short method.
Specific Resistance	r <sub>b</sub>	0	25	50	mΩ/m	measured at 20 °C <sup>(1)</sup>
Specific Line Delay	t <sub>p</sub>		5.0		ns/m	67% V <sub>p</sub> <sup>(2)</sup>
Specific Capacitance	c <sub>b</sub>	0	40	75	pF/m	Between conductors
	c <sub>s</sub>	0	70	110	pF/m	Conductor to shield
Cable size						<sup>(3)</sup>
0.5mm <sup>2</sup> Conductor (20 AWG)	a <sub>c</sub>	0.508			mm <sup>2</sup>	<sup>(4)</sup>
Wire insul dia.	d <sub>ci</sub>	2.23		3.05	mm	
Cable diameter	d <sub>c</sub>	6.0		8.5	mm	
0.8mm <sup>2</sup> Conductor (18 AWG)	a <sub>c</sub>	0.760			mm <sup>2</sup>	<sup>(4)</sup>
Wire insul dia.	d <sub>ci</sub>	2.5		3.5	mm	
Cable diameter	d <sub>c</sub>	8.5		11.0	mm	
Shield Effectiveness			200	225	mΩ/m	Surface transfer impedance up to 1 MHz Test method per MIL-C-85485
Temperature Range	C	-40		+125	°C	Heat aging: 3000 hours per ISO 6722, Test with a mandrel 4-5x diameter of cable. <sup>(5)</sup>
Cable Bend Radius	r	4xdia of cable			mm	90 degree bend radius without cable performance or physical degradation

1. The differential voltage on the bus line seen by a receiving ECU depends on the line resistance between it and the transmitting ECU. Therefore, the total resistance of the signal wires is limited by the bus level parameters of each ECU.
2. The minimum delay time between two points of the bus line may be zero. The maximum value is determined by the bit time and the delay times of the transmitting and receiving circuitry.
3. Other conductor sizes available. Component insulation dimensions may be larger than those specified in SAE J1128. Design engineers should ensure compatibility between cables, connectors and contacts
4. Meet performance requirements of SAE J1128 for types GXL or SXL (includes drain wire where applicable)
5. 125°C or per OEM specification

5.2.1 BUS LINE—The bus line consists of a CAN\_H, CAN\_L and CAN\_SHLD conductors. The CAN\_H should be yellow in color while the CAN\_L should be green. In addition, the cable must meet the following minimum requirements.

(R)

5.2.2 TOPOLOGY—The wiring topology of this network should be as close as possible to a linear structure in order to avoid cable reflections. In practice, it may be necessary to connect short cable stubs to a main backbone cable, as shown in Figure 7. To minimize standing waves, nodes should not be equally spaced on the network and cable stub lengths, dimension S in Figure 7, should not all be the same length. The dimensional requirements of the network are shown in Table 8.

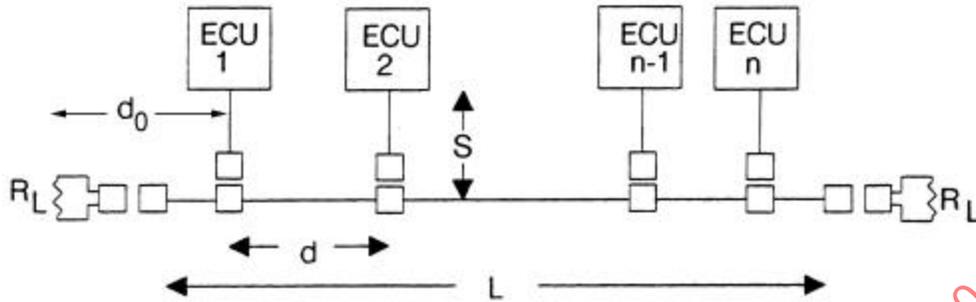


FIGURE 7—WIRING NETWORK TOPOLOGY

TABLE 8¾ NETWORK TOPOLOGY PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Length	L	0		40	m	not including cable stubs
Cable Stub Length <sup>(1)</sup>	S	0		1	m	Note 1
Node Distance	d	0.1		40	m	
Minimum Distance from R <sub>L</sub>	d <sub>0</sub>	0			m	R <sub>L</sub> shall not be located within an ECU

1. The cable stub length for the diagnostic connector is 0.66 m maximum for the vehicle and 0.33 m maximum for the off-board diagnostic tool.

5.2.3 TERMINATING RESISTOR—Each end of the main ‘backbone’ of the linear bus must be terminated with an appropriate resistance to provide correct termination of the CAN\_H and CAN\_L conductors. This termination resistance should be connected between the CAN\_H and CAN\_L conductors. The termination resistance should meet the characteristics specified in Table 9.

TABLE 9¾ TERMINATING RESISTOR PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Resistance	R <sub>L</sub>	110	120	130	Ω	minimum power dissipation 400 mW <sup>(1)</sup>
Inductance				1	μh	

1. Assumes a short of 16V to V<sub>CAN\_H</sub>

5.2.4 SHIELD TERMINATION—The shield should be terminated by a wire conductor and directly grounded at only one point.

General guidelines (in order of importance) for direct termination of the shield are:

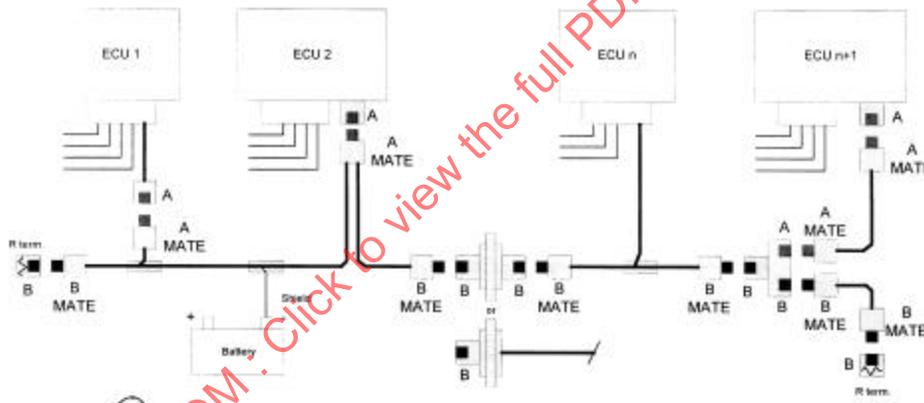
1. Connect to the point of least electrical noise
2. Use the lowest impedance connection possible
3. The closest connection to the center of the network should be used.

(R) It is the responsibility of the vehicle manufacturer to identify the shield termination implementation. Each node on the bus should also provide a shield ground; however, this connection of the CAN\_SHLD conductor should be by a series resistor and capacitor to the best ground connection within the node. Recommended values are  $R = 1 \Omega$  and  $C = 0.68 \mu\text{F}$ . (See Figures A1 and A2.)

(R) **5.3 Connector Specifications**—Two types of connectors are shown that are capable of implementing all aspects of the network. An ECU may be connected with either a hard splice (Appendix C) or connector. If a connector is to be used to connect an ECU to the 'backbone' of the network, it is called the Stub Connector and is designated "A" in Figure 8. The 'backbone' connector is shown in Figure 9. The connector used to connect the termination resistor to the ends of the 'backbone' cable or to pass through structural boundaries, such as cab bulkheads, or to extend the ends of the 'backbone' is called the 'Through Connector' and is designated "B" in Figure 8. The 'Through Connector' is shown in Figure 10.

These two connectors are very similar in design, with different keying structures to eliminate the possibility of connecting the network in a method that would be detrimental to proper communications. The connectors shall provide for the electrical connections of CAN\_H, CAN\_L, and drain wire CAN\_SHLD.

An example of the use of this connector concept is shown in Figure 8.



(R) FIGURE 8—AN EXAMPLE OF NETWORK CONNECTOR USAGE

5.3.1 CONNECTOR ELECTRICAL PERFORMANCE REQUIREMENTS—The connectors and their associated terminals shall meet the electrical requirements specified in Table 10.

TABLE 10<sup>3/4</sup> CONNECTOR PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage <sup>(1)</sup>	$V_{\text{CAN\_H}}$			16	V	nominal $V_{\text{BAT}} = 12 \text{ V}$
	$V_{\text{CAN\_L}}$			32	V	nominal $V_{\text{BAT}} = 24 \text{ V}$
Current	$I$	0	25	80	mA	
Peak Current	$I_p$			500	mA	Time restriction: $101t_B$ <sup>(1)</sup>
Characteristic Impedance	$Z_c$	100	120	140	$\Omega$	
Transmission Frequency	$f$	25			Mhz	
Contact Resistance	$R_T$			10	$\text{m}\Omega$	<sup>(2)</sup>

1. Bus fault.

2. The differential voltage on the bus line seen by a receiving ECU depends on the line resistance between this and the transmitting ECU. Therefore, the transmit resistance of the signal wires is limited by the bus level parameters at each ECU.

(R)

5.3.2 CONNECTOR MECHANICAL REQUIREMENTS—If connectors are used, these connectors should have locking, polarizing, and retention devices that meet the requirements of the specific application. These connectors should also incorporate environmental protection appropriate for the application. The dimensional characteristics of the Stub and Through connectors are shown in Figures 9 and 10, respectively.

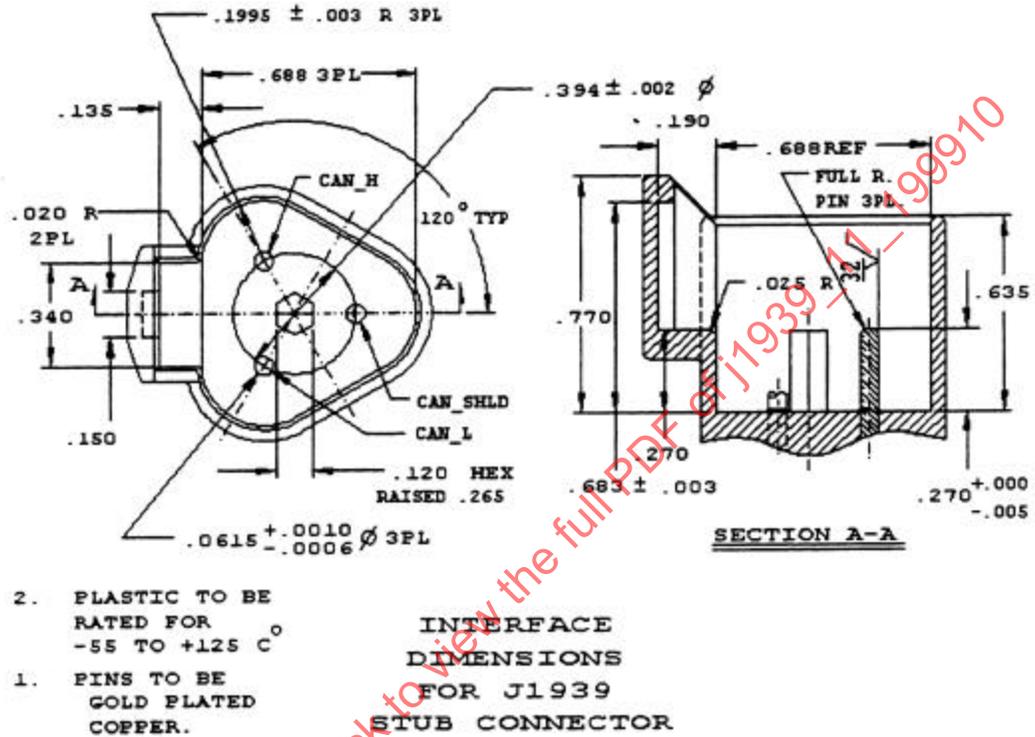
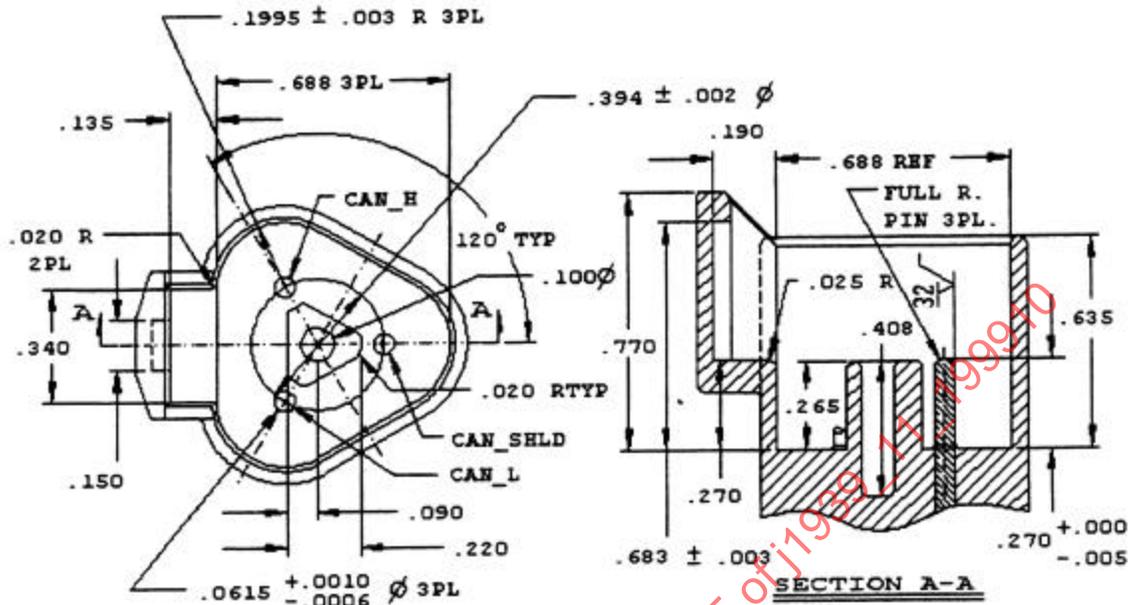


FIGURE 9—STUB CONNECTOR (WITH MALE KEY) DIMENSIONAL REQUIREMENTS (A)



- 2. PLASTIC TO BE RATED FOR -55 TO +125 C°
- 1. PINS TO BE GOLD PLATED COPPER.

**INTERFACE  
DIMENSIONS  
FOR J1939  
THROUGH CONNECTOR**

FIGURE 10—THROUGH CONNECTOR (WITH FEMALE KEY) DIMENSIONAL REQUIREMENTS (B)

(R)

**6. Conformance Tests**—The following figures and formulas show, in principle, how the parameters specified in Section 5.1 should be verified by component manufacturers. While there are many requirements of the physical layer, this section defines a portion of Transceiver compliance tests. Note that the ground connection is not the same as CAN\_SHLD. The measurement ground reference should be the ECU ground.

**6.1 Recessive Output of the ECUs**—The recessive output voltage can be measured as shown in Figure 11.

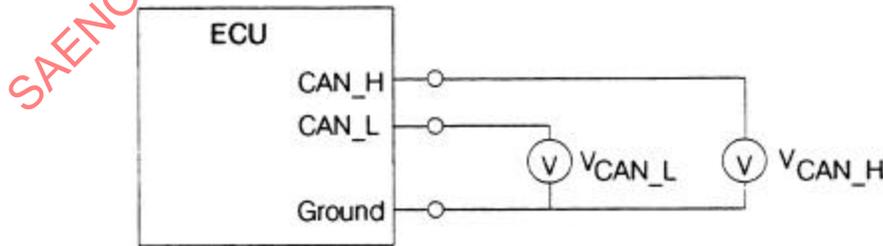


FIGURE 11—MEASUREMENT OF V<sub>CAN\_H</sub> AND V<sub>CAN\_L</sub> DURING THE BUS IDLE STATE

V<sub>CAN\_H</sub> and V<sub>CAN\_L</sub> are measured unloaded while the bus is idle. V<sub>diff</sub> is then determined by

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \tag{Eq.2}$$

Table 3 defines the limits during the recessive state.

NOTE— $V_{CAN\_H}$  and  $V_{CAN\_L}$  is measured with no load such that the worst case would be observed for the maximum recessive condition.

**6.2 Internal Resistance of CAN\_H and CAN\_L**—The internal resistance,  $R_{in}$ , of CAN\_H and CAN\_L can be measured as shown in Figure 12.

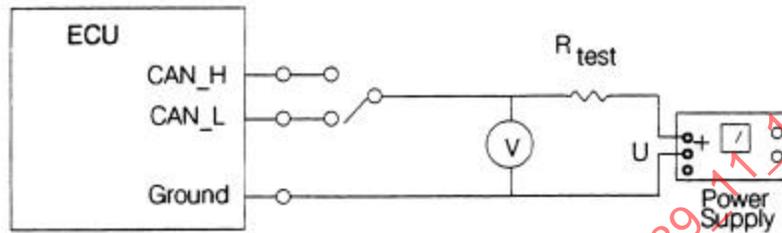


FIGURE 12—MEASUREMENT OF  $R_{in}$  WHILE THE ECU PROTOCOL IC IS SET TO BUS IDLE

$R_{in}$  of CAN\_H and CAN\_L is determined for  $U = 0$  V and  $U = 5$  V, respectively, with  $R_{test} = 5$  k $\Omega$ .  $R_{in}$  of CAN\_H and CAN\_L is then calculated by

$$R_{in} = R_{test} \frac{V_{CAN\_H,L} - V}{V - U} \quad (\text{Eq.3})$$

where:

$V_{CAN\_H}$  and  $V_{CAN\_L}$  are the open circuit voltages according to Figure 11.  $R_{in}$  is defined for the recessive state by Table 3, including Note 4, for DC - Parameters.

**6.3 Internal Differential Resistance**—The internal differential resistance  $R_{diff}$  can be measured as shown in Figure 13.

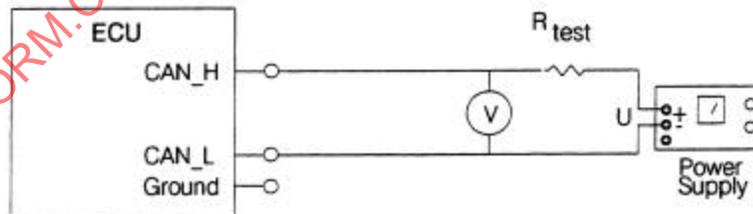


FIGURE 13—MEASUREMENT OF  $R_{DIFF}$  WHILE THE ECU PROTOCOL IC IS SET TO BUS IDLE

$R_{diff}$  is determined for  $U = 5$  V and  $R_{test} = 10$  k $\Omega$  during bus idle as shown in Equation 4:

$$R_{diff} = R_{test} \frac{(V_{diff} - V)}{V - U} \quad (\text{Eq.4})$$

where:

$V_{diff}$  is the differential open circuit voltage according to 6.1.

**6.4 Recessive Input Threshold of an ECU**—The recessive input threshold can be verified over the common mode range as shown in Figure 14.

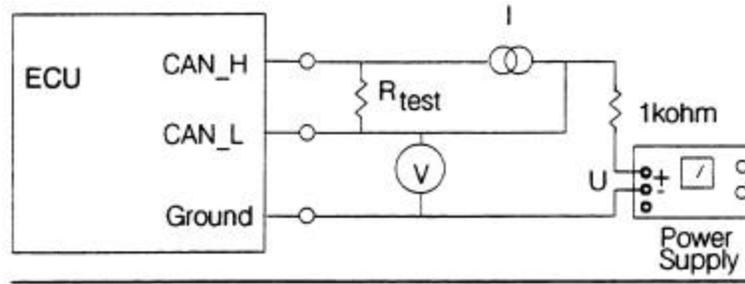


FIGURE 14—TESTING THE INPUT THRESHOLD FOR RECESSIVE BIT DETECTION

Current  $I$  is adjusted to a value which develops 0.5 V (the upper limit for detecting a recessive bit during the recessive state) across  $R_{test}$  with  $R_{test} = 60 \Omega$  (Bus Line Load Equivalent Resistance). In addition,  $U$  is set to two suitable values that produce  $V = -2 \text{ V}$  and  $V = 6 \text{ V}$  during bus idle. Under these conditions, the ECU must not stop transmitting. This indicates that every transmitted recessive bit is still detected as recessive by the protocol IC of the ECU. The level of the dominant bits is nearly independent of  $U$ .

(R) NOTE—The 6 V value is used instead of 7 V since the maximum threshold for receiving a recessive bit is 0.5 V per Table 2.

**6.5 Dominant Output of an ECU**—The dominant output of an ECU can be measured as shown in Figure 15.

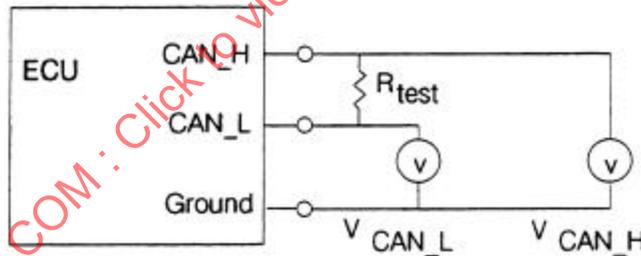


FIGURE 15—MEASUREMENT OF  $V_{CAN\_H}$  AND  $V_{CAN\_L}$  WHILE THE ECU SENDS A DOMINANT BIT

$V_{CAN\_H}$  and  $V_{CAN\_L}$  are measured during a dominant bit transmission.  $R_{test}$  is set to  $60 \Omega$ . The corresponding value of  $V_{diff}$  is given by

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad (\text{Eq.5})$$

(R) Note that the dominant state voltages of an ECU disconnected from the bus are defined in Table 4.

- 6.6 Dominant Input Threshold of an ECU**—The dominant input threshold of an ECU can be verified over the common mode range as shown in Figure 16.

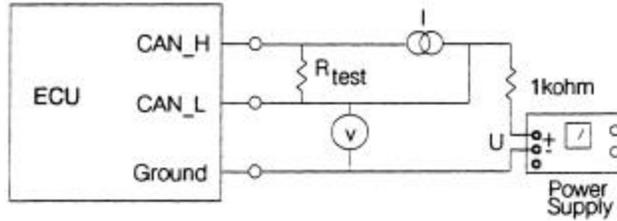


FIGURE 16—TESTING THE INPUT THRESHOLD FOR DOMINANT BIT DETECTION

Current  $I$  is adjusted to a value which induces, with  $R_{test} = 60 \Omega$  (Bus Line Load Equivalent Resistance), the upper threshold of 1 V required to detect a dominant bit during the recessive state. In addition,  $U$  is set to two values that produce  $V = -2 \text{ V}$  and  $V = 6 \text{ V}$  during bus idle. Under these conditions, the ECU must stop transmitting the message which demonstrates that arbitration has been acknowledged. This indicates that every transmitted recessive bit is detected as dominant by the protocol IC of the ECU. The level of dominant bits is nearly independent of  $U$ .

- (R) NOTE—The 6 V value is used instead of 7 V since the maximum threshold for receiving a dominant bit is 1 V per Table 4.

- 6.7 Internal Delay Time**—The internal delay time of an ECU can be measured as shown in Figure 17.

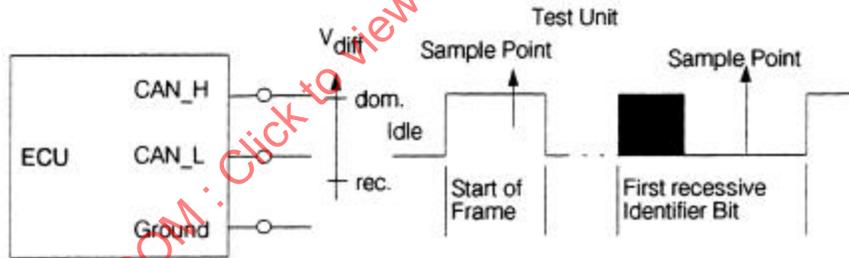


FIGURE 17—MEASUREMENT OF THE INTERNAL DELAY TIME  $T_{ECU}$  BY PARTLY OVERWRITING THE FIRST RECESSIVE IDENTIFIER BIT (SHADED AREA) BY A DOMINANT LEVEL UNTIL THE ARBITRATION IS LOST

- (R) The test unit shown in Figure 17 synchronizes itself to the start of frame bit transmitted by the protocol IC of the ECU. Upon detection of the first recessive identifier bit, the test unit partly overwrites this recessive bit for a time  $t_{overw}$  by a dominant level (shaded area in Figure 17). This overwriting is increased until the protocol IC of the ECU loses arbitration and stops transmitting. If this situation is reached, the available part of the bit time  $t_{avail}$  for delay time compensation is just exhausted (see also Figures 5 and 6 and Table 7). Then  $t_{ECU}$  is calculated by Equation 6.

$$t_{ECU} = t_{avail} - t_{overw} \quad (\text{Eq.6})$$

where:

$t_{avail}$  is known from the bit timing unit of the protocol IC and  $t_{overw}$  is known from the test unit.

The dominant and recessive voltage levels are set by the test unit to the corresponding threshold voltages for reception. This means that the dominant overwriting level is 1 V, and the recessive level is 0.5 V. This ensures a uniquely defined relationship between voltage levels and internal delay time.

## 7. Discussion of Bus Faults—

- a. Possible Failures—During normal operation, several bus failures can occur that may influence operation. These failures and the resulting network behavior are specified subsequently.

**7.1 Loss of Connection to Network**—If a node becomes disconnected from the network, the remaining nodes shall continue communication.

**7.2 Node Power or Ground Loss**—If a node loses power, or if it is in a low voltage condition, the network is not loaded down, and the remaining nodes shall continue communication.

If a node loses ground, the network shall not be biased up. The remaining nodes shall continue communication.

**7.3 Unconnected Shield**—In case the shield loses connection at one node, communication is possible but electromagnetic interference increases. Common mode voltages can be induced between the shield and the wires.

**7.4 Open and Short Failures**—In principle, failures are detectable if there is a significant message destruction rate, as interpreted by the electronic control units. Some external events that may cause failures are shown in Figure 18 and are discussed as follows:

- a. Case 1: CAN\_H is Interrupted—Data communication between nodes on opposite sides of an interruption is not possible. Data communication between nodes on the same side of an interruption may be possible, but with reduced signal-to-noise ratio.
- b. Case 2: CAN\_L is Interrupted—Data communication between nodes on opposite sides of an interruption is not possible. Data communication between nodes on the same side of an interruption may be possible, but with reduced signal-to-noise ratio.
- c. Case 3: CAN\_H is Shorted to VBat—Data communication is not possible if VBat is greater than the maximum allowed common mode bus voltage.
- d. Case 4: CAN\_L is Shorted to GND—Data communication is possible, because the bus voltages are within the allowed common mode voltage range. Signal-to-noise ratio is reduced and radiation is increased. The electromagnetic immunity is decreased.
- e. Case 5: CAN\_H is Shorted to GND—Data communication is not possible.
- f. Case 6: CAN\_L is Shorted to VBat—Data communication is not possible.
- g. Case 7: CAN\_H is Shorted to CAN\_L—Data communication is not possible.
- h. Case 8: Both Bus Lines are Interrupted at the Same Location—Data communication between nodes on opposite sides of an interruption is not possible. Data communication between nodes on the same side of an interruption may be possible, but with reduced signal-to-noise ratio.

- (R)
- i. Case 9: Loss of Termination Resistor—Data communication via the bus may be possible, but with reduced signal-to-noise ratio.
  - j. Case 10: Topology Parameter Violations (i.e., Bus Length, Cable Stub Length, Node Distribution)—Data communication via the bus may be possible, but with reduced signal-to-noise ratio.

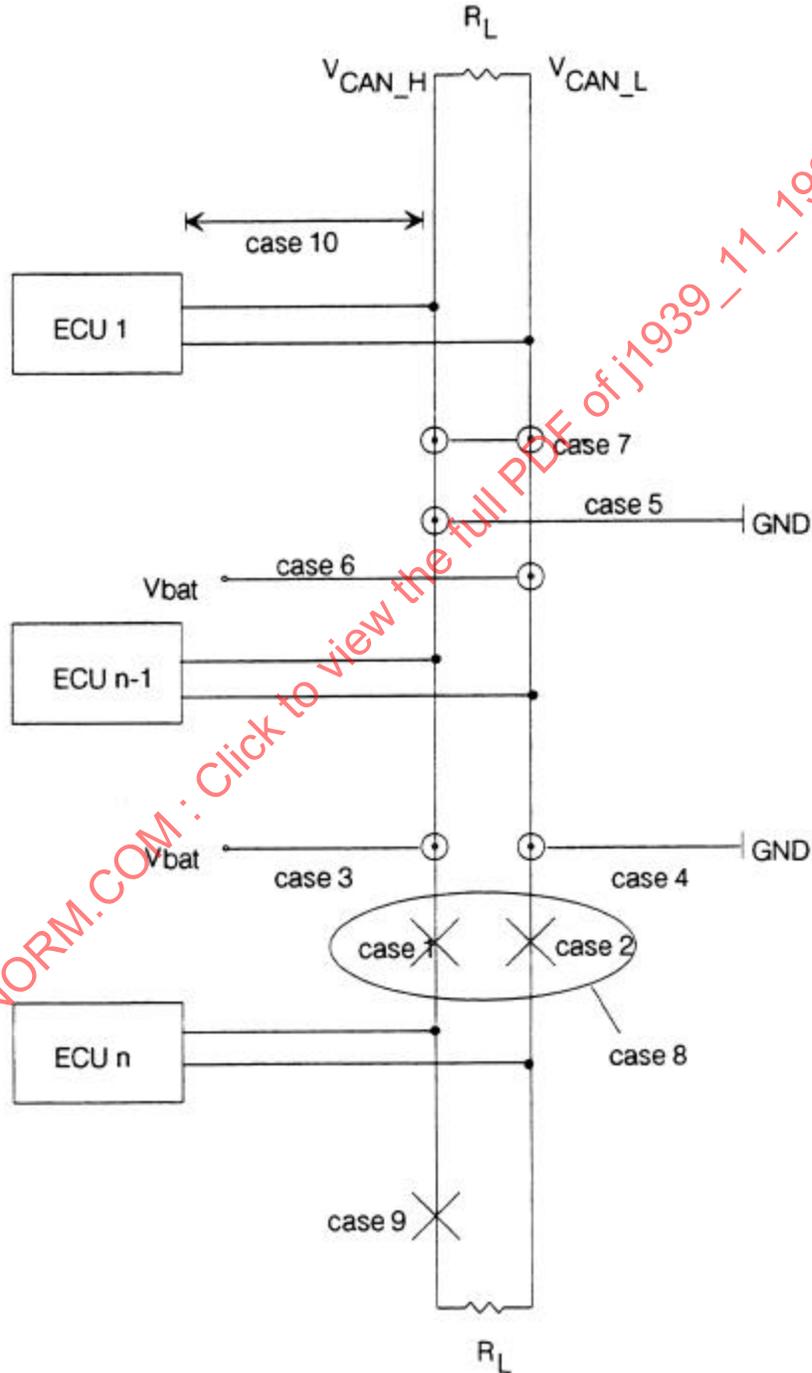


FIGURE 18—POSSIBLE FAILURES DUE TO EXTERNAL EVENTS

(R)

**8. Notes**

- 8.1 Marginal Indicia**—The (R) symbol is located in the left margin is for the convenience of the user in locating areas where technical revisions have been made to the previous issue of the report. An (R) symbol to the left of the document title indicates a complete revision of the report.

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## APPENDIX A

## EXAMPLE PHYSICAL LAYER CIRCUITS

(R) **A.1 Example 1 Physical Layer**—The following are three examples of physical layer circuits which meet the electrical specifications contained within this document.

(R) **A.1.1 Example 1 Physical Layer**—See Figure A1.

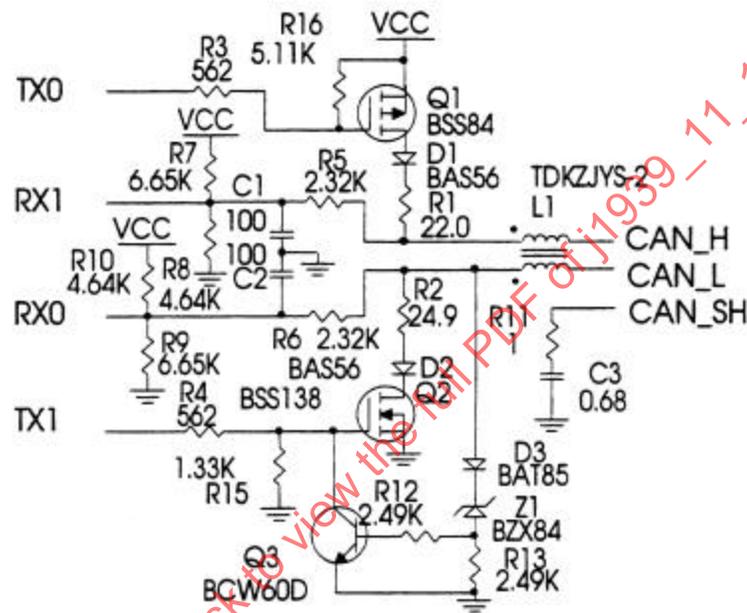


FIGURE A1—EXAMPLE 1 PHYSICAL LAYER CIRCUIT

The circuit has a special short-circuit protection for the CAN\_L path. Therefore it uses only low power components but withstands voltages up to +50 V on the bus lines (e.g., load dump). R7, R8, R9, R10 form the biasing network for the recessive state; R5, R6, C1, C2 together with the biasing network form an input filter with a corner frequency of about 1.2 MHz. R3, R4, R15, and R16 provide the drive impedance for Q1, Q2; they should be chosen so that the switching waveforms of CAN\_H and CAN\_L are symmetrical during transitions. R1 and R2, together with the on-resistance of Q1 and Q2, set the output impedance of the link for the dominant state; D1 and D2 are used for common mode decoupling. R12, R13, D3, Z1, and Q3 switch Q2 off if voltage levels at CAN\_L exceed +10V (Q1 is decoupled by D1 in this case). D3 isolates the capacitance of Z1 from the bus line.

(R) L1 is used to reduce the amount of high-frequency microprocessor switching noise coupled on the bus. Testing has shown this component to reduce radiated emissions over the test range of 10 KHz to 200 MHz, but particularly below 30 MHz. While this component improves radiated emissions performance, its use is not essential to meeting the requirements of SAE J1939-11 and therefore not required. The radiated emissions performance of ECU must be addressed on an individual basis.