SAE The Engineering Society For Advancing Mobility Land Sea Air and Space®
INTERNATIONAL
400 Commonwealth Drive, Warrendale, PA 15096-0001

SURFACE VEHICLE RECOMMENDED PRACTICE

SAE 1939/11

Issued 1994-12

Submitted for recognition as an American National Standard

PHYSICAL LAYER—250K bits/s, SHIELDED TWISTED PAIR

Foreword—This series of SAE Recommended Practices have been developed by the Truck & Bus Control and Communications Network Subcommittee of the Truck & Bus Electrical Committee. The objectives of the subcommittee are to develop information reports, recommended practices and standards concerned with the requirements design and usage of devices which transmit electronic signals and control information among vehicle components. The usage of these recommended practices is not limited to truck and bus applications. Other applications may be accommodated with immediate support being provided for construction and agricultural equipment, and stationary power systems.

These SAE Recommended Practices are intended as a guide toward standard practice and are subject to change to keep pace with experience and technical advances.

TABLE OF CONTENTS

1. ***Scope***—These SAE Recommended Practices are intended for light- and heavy-duty vehicles on- or off-road as well as appropriate stationary applications which use vehicle derived components (e.g., generator sets). Vehicles of interest include but are not limited to: on- and off-highway trucks and their trailers; construction equipment; and agricultural equipment and implements.

   The purpose of these documents is to provide an open interconnect system for electronic systems. It is the intention of these documents to allow electronic devices to communicate with each other by providing a standard architecture.

2. ***References***—General information regarding this series of recommended practices is found in SAE J1939.

2.1 Applicable Documents—The following publications form a part of this specificaiton to the extent specified herein. The latest issue of SAE publications shall apply.

2.1.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1113/13—Electromagnetic Compatibility Measurement Procedure for Vehicle Components—Part 13—Immunity to Electrostatic Discharge

2.2 Related Publication—The following publication is provided for information purposes only and is not a required part of this document.

2.2.2 ISO PUBLICATION—Available from ANSI, 11 West 42nd Street, New York, NY 10036-8002.

ISO 11898—Road vehicles—Interchange of digital information—Controller Area Network (CAN) for high speed communication.

3. Network Physical Description

3.1 Physical Layer—The physical layer is a realization of an electrical connection of a number of ECUs (Electronic Control Units) to a network. The total number of ECUs will be limited by electrical loads on the bus line. This maximum number of ECUs is fixed to 30, on a given segment, due to the definition of the electrical parameters given in the present specification.

3.2 Physical Media—This document defines a physical median of shielded twisted pair. These 2 wires have a characteristic impedance of 120 Ω and are symmetrically driven with respect to the electrical currents. The designations of the individual wires are CAN_H and CAN_L. The names of the corresponding pins of the ECUs are also denoted by CAN_H and CAN_L, respectively. The third connection for the termination of the shield is denoted by CAN_SHLD.

3.3 Differential Voltage—The voltages of CAN_H and CAN_L relative to ground of each individual ECU are denoted by V_{CAN_H} and V_{CAN_L}. The differential voltage between V_{CAN_H} and V_{CAN_L} is defined by Equation 1:

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \qquad \text{(Eq.1)}$$

3.4 Bus Levels—The bus lines can have one of the two logical states, recessive or dominant (see Figure 1). In the recessive state, V_{CAN_H} and V_{CAN_L} are fixed to a mean voltage level. V_{diff} is approximately zero on a terminated bus. The recessive state is transmitted during bus idle or a recessive bit.

The dominant state is represented by a differential voltage greater than a minimum threshold. The dominant state overwrites the recessive state and is transmitted during a dominant bit.

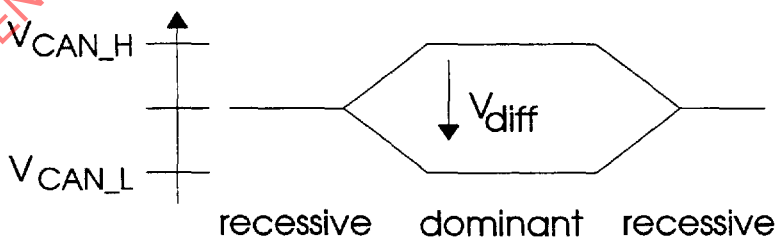


FIGURE 1—PHYSICAL BIT REPRESENTATION

3.5 Bus Levels During Arbitration—A dominant and recessive bit imposed on the bus lines during a given bit time by two different ECUs will result in a dominant bit.

3.6 Common Mode Bus Voltage Range—The common mode bus voltage is defined as the boundary voltage levels of CAN_H and CAN_L, measured with respect to the individual ground of each ECU, for which proper operation is guaranteed when all ECUs are connected to the bus line.

3.7 Terminating Resistor—The bus line is electrically terminated at each end with a load resistor denoted by R_L. R_L shall not be located within an ECU because the bus will lose termination if one of these ECUs is disconnected (see Figure 2). (Also see 5.2.3 for resistor characteristics.)

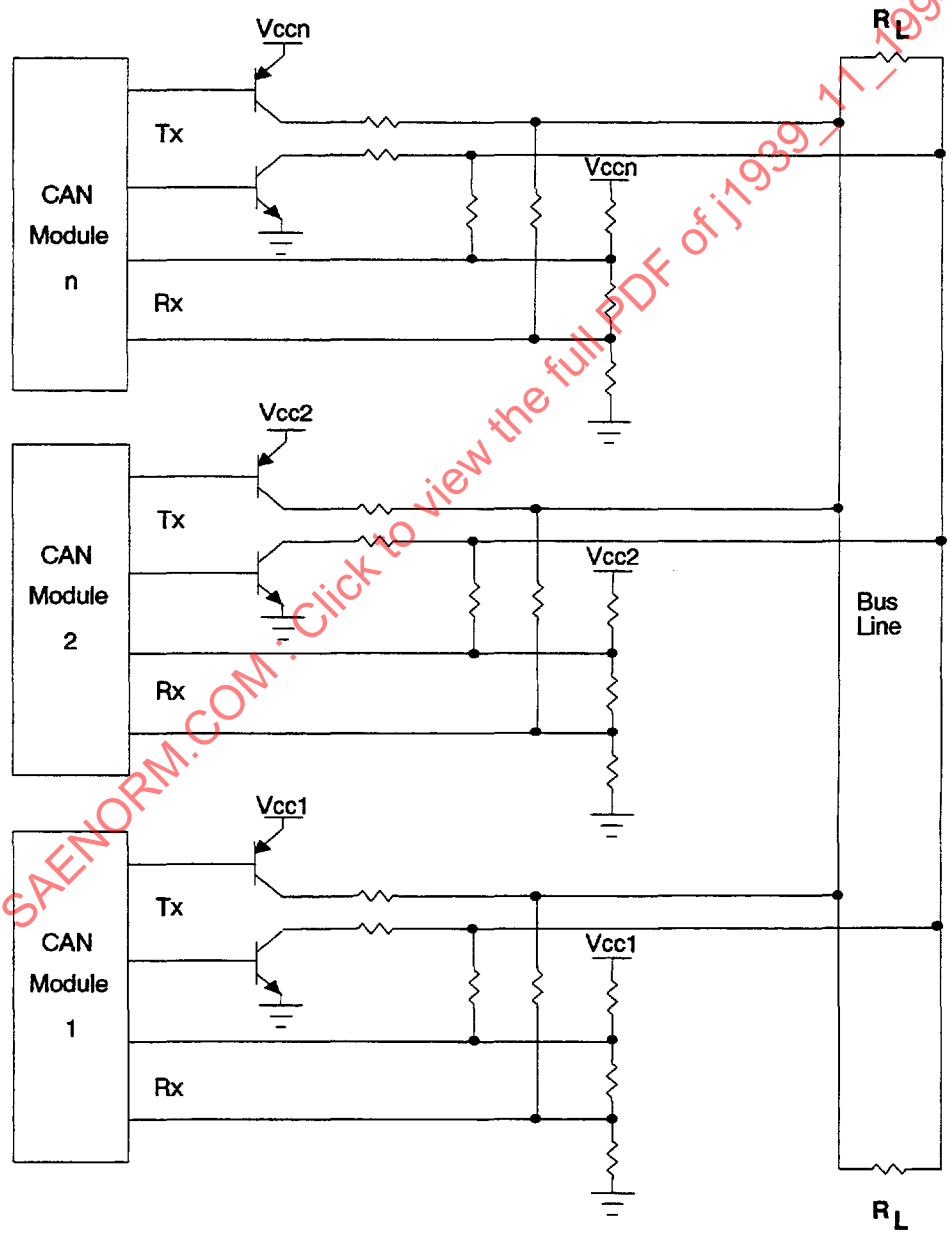


FIGURE 2—PHYSICAL LAYER FUNCTIONAL

3.8 Internal Resistance—The internal resistance, R_{in}, of an ECU is defined as the resistance seen between CAN_H (or CAN_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).

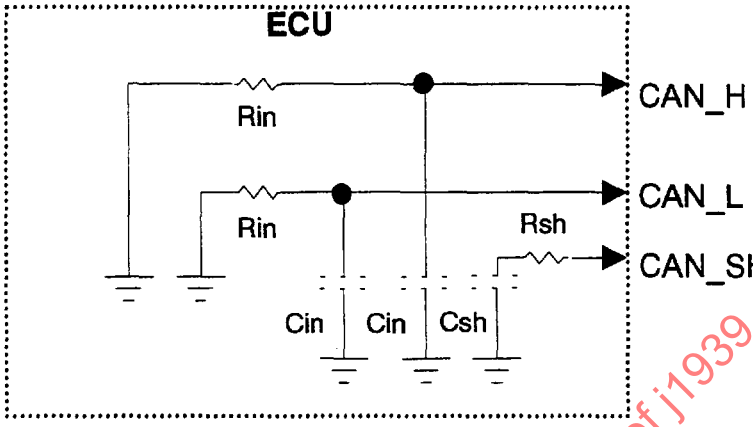


FIGURE 3—ILLUSTRATION OF INTERNAL CAPACITANCE AND RESISTANCE OF AN ECU IN THE RECESSIVE STATE

3.9 Differential Internal Resistance—The differential internal resistance, R_{diff}, is defined as the resistance seen between CAN_H and CAN_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).

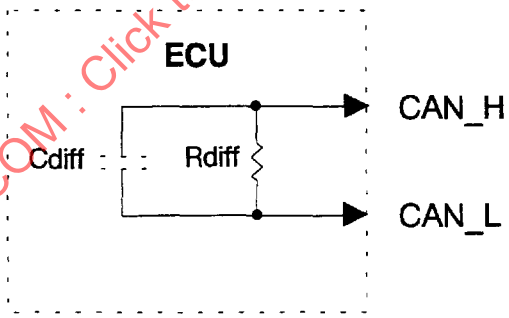


FIGURE 4—ILLUSTRATION OF DIFFERENTIAL INTERNAL CAPACITANCE AND RESISTANCE OF AN ECU IN THE RECESSIVE STATE

3.10 Internal Capacitance—The internal capacitance, C_{in}, of an ECU is defined as the capacitance seen between CAN_H (or CAN_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).

3.11 Differential Internal Capacitance—The differential internal capacitance, C_{diff}, of an ECU is defined as the capacitance seen between CAN_H and CAN_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).

3.12 Bit Time—The bit time, t_B, is defined as the duration of one bit (see Figure 5). Bus management functions executed within this bit time, such as ECU synchronization behavior, network transmission delay compensation, and sample point positioning, are defined by the programmable bit timing logic of the CAN protocol IC (Integrated Circuit). The bit time for this recommended practice is 4 µs corresponding to 250 Kbit/s.

Various names for the bit segments are used by suppliers of CAN protocol ICs and it is possible that two bit segments are defined as one.

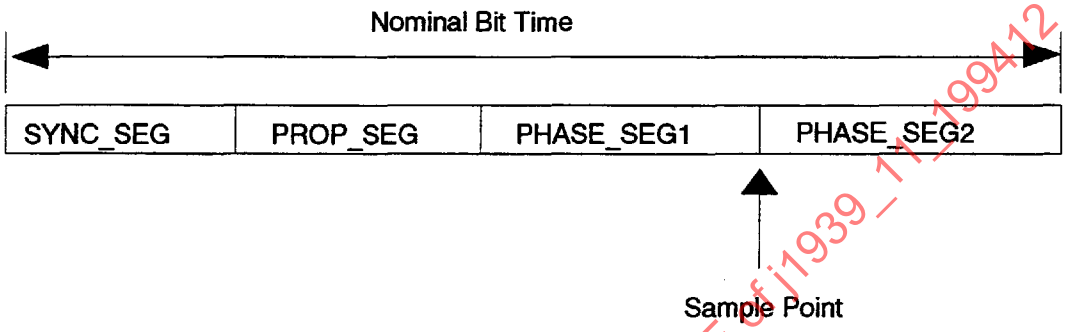


FIGURE 5—PARTITION OF THE BIT

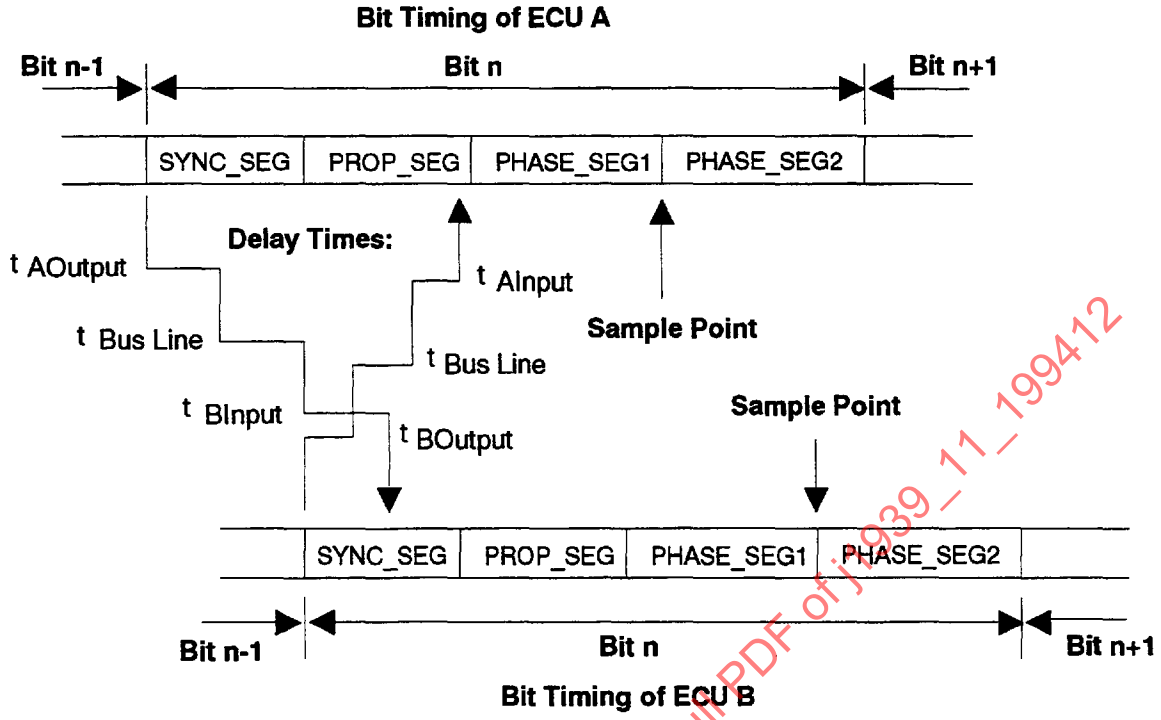
a. SYNC SEG—This part of the bit time is used to synchronize the various ECUs on the bus. An edge is expected within this bit segment.

b. PROP SEG—This part of the bit time is used to compensate for the physical delay times within the network. These delay times are caused by the propagation time of the bus line and the internal delay time of the ECUs.

c. PHASE SEG1, PHASE SEG2—These Phase-Buffer-Segments are used to compensate for phase-errors and can be lengthened or shortened by resynchronization.

d. Sample-Point—The Sample-Point is the point of time at which the bus level is read and interpreted as the value of that respective bit. Its location is at the end of PHASE_SEG1.

3.13 Internal Delay Time—The internal delay time of an ECU, t_{ECU}, is defined as the sum of all asynchronous delays that occur along the transmission and reception path of the individual ECUs, relative to the bit timing logic unit of the protocol IC. For more details see Figure 6.



Notes:

1) The sum of output and input ECU delays, with ECU disconnected from the bus relative to the bit timing logic is critical. The important characteristic parameter of an ECU is (see 3.12)

$$t\_ECU = t\_Output + t\_Input \quad [Where \_ = ECU (A,B...)]$$

2) For proper arbitration, the following condition must be met:

$$t_A ECU + t_B ECU + 2 * t_{Bus\ line} <= t_{PROP\_SEG} + (t_{PHASE\_SEG1} - t_{SJW})$$

SYNC_SEG is not taken into account as it is possible that this segment is lost if there is a phase shift between modules.

t_{SJW} is part of PHASE_SEG1 to compensate phase-errors. It is subtracted from the available time as it is possible that a spike may cause a missynchronization with a phase shift of t_{SJW}.

That means the leading transmitting bit timing logic with respect to synchronization of ECU A must be able to know the correct bus level of bit n at the sample point. The tolerable values of t_{ECU} strongly depends on the bit rate and line length of the bus and of the possible bit timing as shown by the arbitration condition.

3) The acceptable crystal tolerances of the protocol ICs and the potential for missynchronization is determined by PHASE_SEG1 and 2.

FIGURE 6—TIME RELATIONSHIP BETWEEN BIT TIMING LOGIC OF ECU A AND B DURING ARBITRATION

a. Synchronization—Hard Synchronization and Resynchronization are the two forms of synchronization. They obey the following rules:

1. Only one Synchronization within one bit time is allowed.

2. An edge will be used for Synchronization only if the value detected at the previous Sample Point (previously read bus value) differs from the bus value immediately after the edge.

3. Hard Synchronization is performed during said edge whenever there is a 'recessive' to 'dominant' edge.

4. All other 'recessive' to 'dominant' edges fulfilling rules 1 and 2 will be used for Resynchronization with the exception that a transmitter will not perform Resynchronization as a result of a 'recessive' to 'dominant' edge with a positive Phase Error if only 'recessive' to 'dominant' edges are used for Resynchronization.

b. Synchronization Jump Width (SJW)—As a result of Synchronization PHASE_SEG1 may be lengthened or PHASE_SEG2 may be shortened. The amount of lengthening or shortening of the Phase Buffer bit Segments has an upper bound given by the Synchronization Jump Width. The Synchronization Jump Width is less than or equal to PHASE_SEG1.

3.14 CAN Bit Timing Requirements—It is necessary to ensure that a reliable network can be constructed with components from multiple suppliers. Without any bit timing restrictions, different devices may not be able to properly receive and interpret valid messages. Under certain network conditions it may also be possible for a particular device to have unfair access to the network. In addition, it makes network management (system diagnostics) much more difficult. CAN chip suppliers also recommend that all devices on a given network be programmed with the same bit timing values.

All CAN ICs divide the bit time into smaller sections defined as tq (time quantum). For most CAN ICs 1tq = 250 ns (determined by oscillator frequency and baud rate prescaler).

Therefore specific values for the bit timing registers need to be defined to ensure that a reliable network exists for all nodes based on the best tradeoffs between propagation delay and clock tolerance. Note that there are some differences in bit segment definition between manufacturers of CAN devices. The end result is that for a 250 kbps, 40 m network, the following values are recommended for typical controller ICs.

SYNC = 0 (sync on recessive to dominant edge only)
SAMPLE = 0 (maximum time for external delays available)

TSEG1 = 13 tq
TSEG2 = 2 tq

SJW = 1 tq (SJW is a part of TSEG1 and TSEG2)
Total Bit Time = TSEG1 + TSEG2 + Tsyncseg = 13 + 2 + 1 = 16 tq = 4 ms

PROP_SEG + PHASE_SEG1 = TSEG1
PHASE_SEG2 = TSEG2,
SYNC_SEG = SYNC_SEG

This selection for the bit timing registers generally requires the use of Crystal Oscillators at all nodes so that the clock tolerance given in Table 1 can be achieved.

TABLE 1—AC PARAMETERS OF AN ECU DISCONNECTED FROM THE BUS LINE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bit time	t_B	3.995	4.000	4.005	ms	250 Kbit/s 1)
Internal Delay Time	t_{ECU}	0.0		0.9	ms	2)
Internal Capacitance 3)	C_{in}	0	50	100	pF	250 Kbit/s for CAN_H and CAN_L relative to Ground
Differential Internal Capacitance 3)	C_{diff}	0	25	50	pF	
Available Time	t_{avail}	2.5			ms	4) 40 m bus length

1) Including initial tolerance, temperature, aging, etc.

2) The value of t_{ECU} has to be guaranteed for a differential voltage of V_{diff} = 1.0V for a transition from recessive to dominant and of V_{diff} = 0.5V for a transition from dominant to recessive. With the bit timing from the example of note 1, a CAN-Interface delay of 500 ns is possible (controller not included) with a reserve of about 300 ns. This allows slower slopes (R3 and R4 in Figures A.1 and A.2) and input filtering (R5, R6, C1, C2 in Figures A.1 and A.2). It is recommended to use this feature due to EMC.

The minimal internal delay time may be zero. The maximum tolerable value is determined by the bit timing and the bus delay time.

3) In addition to the internal capacitance restrictions a bus connection should also have an inductance as low as possible. The minimum values of C_{in} and C_{diff} may be 0, the maximum tolerable values are determined by the bit timing and the network topology parameters o and d (see Table 8). Proper functionality is guaranteed if occurring cable resonant waves do not suppress the dominant differential voltage level below V_{diff} = 1V and do not increase the recessive differential voltage level above V_{diff} = 0.5V at each individual ECU (see Tables 3 and 4).

4) The available time results from the bit timing unit of the protocol IC. For example, this time in most controller ICs corresponds to TSEG1. Due to missynchronization it is possible to lose the length of SJW. So the available time (t_{avail}) with one missynchronization is TSEG1-SJW ms. A tq time of 250 ns and SJW = 1 tq, TSEG1 = 13 tq, TSEG2 = 2tq results in t_{avail} = 3.00 µs.

4. *Functional Description*—As shown in Figure 2, the linear bus line is terminated with a load resistor R_L on each end. These resistors suppress reflections.

The bus is in the recessive state if the bus transmitters of all ECUs on the bus are switched off. In this case, the mean bus voltage is generated by the passive biasing circuit in all ECUs on the bus. In Figure 2 this is realized by the resistor network that defines the reference for the receive operation.

A dominant bit is sent to the bus line if the bus driver circuit of at least one unit is switched on. This induces a current flow through the terminating resistors, and consequently, a differential voltage between the two wires. The dominant and recessive states are passed by a resistor network which transforms the differential voltages of the bus line to corresponding recessive and dominant voltage levels at the comparator input of the receiving circuitry for detection.

5. Electrical Specification

5.1 Electrical Data—The parameter specifications in these tables must be fulfilled throughout the operating temperature range of every ECU. These parameters allow up to a maximum of 30 ECUs to be connected to a given bus segment.

5.1.1 ELECTRONIC CONTROL UNIT—The limits given in the Tables 1 to 4, apply to the CAN_H and CAN_L pins of each ECU, with the ECU disconnected from the bus line (see Section 6).

TABLE 2—LIMITS OF V_{CAN_H} AND V_{CAN_L} OF AN ECU DISCONNECTED FROM THE BUS LINE FOR NOMINAL BATTERY VOLTAGES OF 12 V AND 24 V

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Max. Voltage	V_{CAN_H}	–3.0		16.0	V	nominal battery voltage 12 V
	V_{CAN_L}	–3.0		16.0	V	
Max. Voltage	V_{CAN_H}	–3.0		32.0	V	nominal battery voltage 24 V
	V_{CAN_L}	–3.0		32.0	V	

5.1.1.1 Absolute Maximum Ratings—The limits given in Table 2 are the absolute maximum DC voltages which can be connected to the bus lines without damage to transceiver circuits. Although the link is not guaranteed to operate at these conditions, there is no time limit (operating CAN ICs will go "error passive" after a period of time).

5.1.1.2 DC Parameters—Tables 3 and 4 define the DC parameters for the recessive and dominant states, respectively, of an ECU disconnected from the bus.

TABLE 3—DC—PARAMETERS FOR THE RECESSIVE STATE OF AN ECU DISCONNECTED FROM THE BUS LINE—RECESSIVE STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Voltage	V_{CAN_H}	2.0	2.5	3.0	V	no load
Output Behavior	V_{CAN_L}	2.0	2.5	3.0	V	
Differential Voltage Output Behavior	V_{diff_or}	–1200		50	mV	no load
Differential Internal Resistance	R_{diff}	10		100	kΩ	no load
Internal Resistance[3]	R_{in}	5		15	kΩ	no load
Input Range	V_{diff}	–1.0		0.5	V	1) 2) 4)

1) The equivalent of the two terminating resistors in parallel (60 Ω) is connected between CAN_H and CAN_L.

2) Reception must be ensured within the common mode voltage range defined in Table 5 and Table 6, respectively.

3) In order to generate symmetrical waveforms and minimize EMI radiation, R_{in} of CAN_H and CAN_L should have almost the same value. The deviation has to be less than 5% relative to each other.

4) Although Vdiff < -1.0 V is only possible during fault conditions it should be interpreted as recessive.

TABLE 4—DC—PARAMETERS FOR THE DOMINANT STATE OF AN ECU DISCONNECTED FROM THE BUS LINE—DOMINANT STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Voltage Output Behavior	V_{CAN_H}	3.0	3.5	5.0	V	1)
	V_{CAN_L}	0.0	1.5	2.0	V	
Differential Voltage Output Behavior	V_{diff_ld}	1.5	2.0	3.0	V	1)
Input Range	V_{diff}	1.0		5.0	V	1) 2)

1) The equivalent of the two terminating resistors in parallel (60 Ω) is connected between CAN_H and CAN_L.

2) Reception must be ensured within the common mode voltage range defined in Table 5 and Table 6, respectively.

TABLE 5—BUS VOLTAGE PARAMETERS FOR THE RECESSIVE STATE WITH ALL ECUs CONNECTED TO THE BUS LINE—RECESSIVE STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage on the bus line	V_{CAN_L}	0.1	2.5	4.5	V	measured with respect to ground of each ECU
Differential Bus Voltage[1)]	V_{diff}	–400	0	12	mV	measured at each ECU connected tothe bus line

1) The differential bus voltage is determined by the output behavior of all ECUs during the recessive state. Therefore, V_{diff} is approximately zero (see Table 3). The minimum value is determined by the requirement that a single transmitter must be able to represent a dominant bit by a minimum value of V_{diff} = 1.2 V.

TABLE 6—BUS VOLTAGE PARAMETERS FOR THE DOMINANT STATE WITH ALL ECUs CONNECTED TO THE BUS LINE—DOMINANT STATE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage on Bus[1)]	V_{CAN_H}		3.5	7.0	V	measured with respect to ground of each ECU
	V_{CAN_L}	–2.0	1.5			
Differential Bus Voltage[2)]	V_{diff}	1.2	2.0	3.0	V	measured at each ECU connected to the bus line during arbitration
				5.0	V	

1) The minimum value of V_{CAN_H} is determined by the minimum value of V_{CAN_L} plus the minimum value of V_{diff}. The maximum value of V_{CAN_L} is determined by the maximum value of V_{CAN_H} minus the value of V_{diff}.

2) The bus load increases as ECUs are added to the network, due to R_{diff}. Consequently, V_{diff} decreases. The minimum value of V_{diff} determines the number of ECUs allowed on the bus. The maximum value of V_{diff} is defined by the upper limit during arbitration. This maximum value of V_{diff} for single operation must not exceed 3 V.

5.1.1.3 AC—Parameters—Table 1 defines the AC Parameter requirements of the ECUs.

5.1.2 BUS VOLTAGES—OPERATIONAL—The parameters specified in the table below apply when all ECUs (between 2 and 30) are connected to a correctly terminated bus line. The maximum allowable ground offset between any ECUs on the bus is 2 V. The voltage extremes associated with this offset would occur in the dominant state (see Table 6).

5.1.3 ELECTROSTATIC DISCHARGE (ESD)—CAN_H and CAN_L should be tested while disconnected from the bus line according to SAE J1113/13 for ESD using 15 kV.

5.1.4 EXAMPLE PHYSICAL LAYER CIRCUITS—There are many possible discrete and integrated physical layer circuits which meet the previous requirement. Examples of two discrete implementations are shown in Appendix A.

5.2 Physical Media Parameters—The following sections describe the characteristics of the cable, termination, and topology of the network. (See Table 7.)

TABLE 7—PHYSICAL MEDIA PARAMETERS FOR TWISTED SHIELDED CABLE

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Impedance	Z	108	120	132	Ω	measured at 1 MHz between the two sig. wires with shield grounded
Specific Resistance	r_b	0	25	50	mΩ/m	1)
Specific Line Delay	t_p		5.0		ns/m	2)
Specific Capacitance	c_b	0	40	75	pF/m	Between conductors
	c_s	0	70	110	pF/m	Conductor to shield
Conductor Size	a_c		0.5		mm^2	cross section
Cable Size	d_c	6.0		8.5	mm	diameter
Conductor Insulation Size	d_{ci}	2.9	3.3	3.7	mm	diameter
Shield Effectiveness			200		mΩ/m	surface transfer impedance up to 1 MHz

1) The differential voltage on the bus line seen by a receiving ECU depends on the line resistance between it and the transmitting ECU. Therefore, the total resistance of the signal wires is limited by the bus level parameters of each ECU.

2) The minimum delay time between two points of the bus line may be zero. The maximum value is determined by the bit time and the delay times of the transmitting and receiving circuitry.

5.2.1 BUS LINE—The bus line consists of a CAN_H, CAN_L and CAN_SHLD conductors. The CAN_H should be yellow in color while the CAN_L should be green. In addition, the cable must meet the following minimum requirements.

5.2.2 TOPOLOGY—The wiring topology of this network should be as close as possible to a linear structure in order to avoid cable reflections. In practice, it may be necessary to connect short cable tails to a main backbone cable, as shown in Figure 7. To minimize standing waves, nodes should not be placed equally spaced on the network and cable tail lengths should not all be the same length. The dimensional requirements of the network are shown in Table 8.

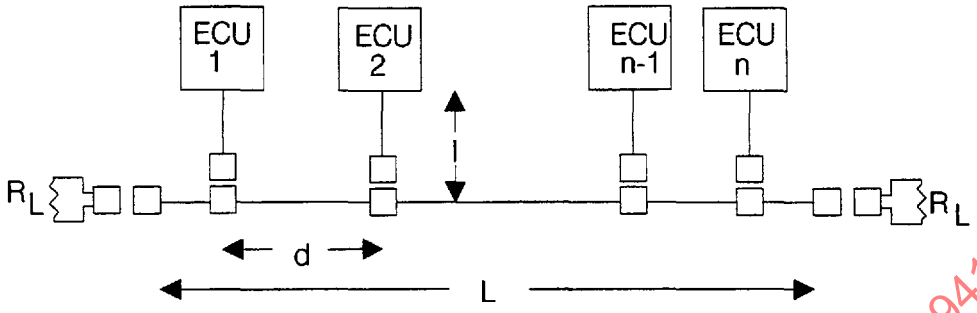


FIGURE 7—WIRING NETWORK TOPOLOGY

TABLE 8—NETWORK TOPOLOGY PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Bus Length	L	0		40	m	not including cable tails
Cable Tail Length	I	0		1	m	
Node Distance	d	0.1		40	m	

5.2.3 TERMINATING RESISTOR—Each end of the main 'backbone' of the linear bus must be terminated with an appropriate resistance to provide correct termination of the CAN_H and CAN_L conductors. This termination resistance should be connected between the CAN_H and CAN_L conductors. The termination resistance should meet the characteristics specified in Table 9.

TABLE 9—TERMINATING RESISTOR PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Resistance	R_L	110	120	130	Ω	minimum power dissipation 400 mW [1]
Inductance				1	µh	

[1] Assumes a short of 16V to V_{CAN_H}

5.2.4 SHIELD TERMINATION—The shield should be terminated by a wire conductor and directly grounded at one point. This ground point should be as electrically close to the vehicle battery ground as possible.

Each node on the bus should also provide a shield ground; however, this connection of the CAN_SHLD conductor should be by a series resistor and capacitor to the best ground connection within the node. Recommended values are R=1 Ω and C=0.68 µF. (See Figures A.1 and A.2.)

5.3 Connector Requirement—Two types of connectors are provided to implement all aspects of the network. The connector to be used to connect an ECU to the 'backbone' of the network is called the Stub Connector and is designated "A" in Figure 8. The connector used to connect the termination resistor to the ends of the 'backbone' cable or to pass through structural boundaries, such as cab bulkheads, or to extend the ends of the 'backbone' is called the Through Connector and is designated "B" in Figure 5.2.

These two connectors are very similar in design, with different keying structures to eliminate the possibility of connecting the network in a method that would be detrimental to proper communications. The connectors shall provide for the electrical connections of CAN_H, CAN_L and drain wire CAN_SHLD.

An example of the use of this connector concept is shown in Figure 8.

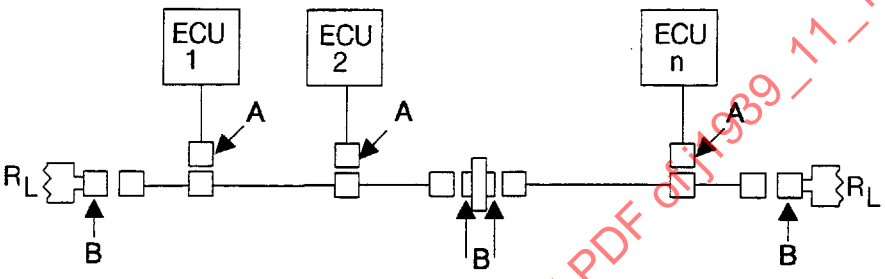


FIGURE 8—EXAMPLE OF CONNECTOR USAGE

5.3.1 CONNECTOR ELECTRICAL PERFORMANCE REQUIREMENTS—The connectors and their associated terminals shall meet the electrical requirements specified in Table 10.

TABLE 10—CONNECTOR PARAMETERS

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Voltage [2]	V_{CAN_H}			16	V	nominal VBAT =12 V
	V_{CAN_L}			32	V	nominal VBAT=24 V
Current	I	0	25	80	mA	
Peak Current	I_p			500	mA	Time restriction: $101t_B$ [2]
Characteristic Impedance	Z_c	100	120	140	Ω	
Transmission Frequency	f	25			Mhz	
Contact Resistance	R_T			10	mΩ	[1]

[1] The differential voltage on the bus line seen by a receiving ECU depends on the line resistance between this and the transmitting ECU. Therefore, the transmission resistance of the signal wires is limited by the bus level parameters at each ECU.

[2] Bus fault.

5.3.2 CONNECTOR MECHANICAL REQUIREMENTS—Connectors should be used at all points where two or more cables terminate. These connectors should have locking, polarizing, and retention devices that meet the requirements of the specific application. These connectors should also incorporate environmental protection appropriate for the application. The dimensional characteristics of the Stub and Through connectors are shown in Figures 9 and 10, respectively.

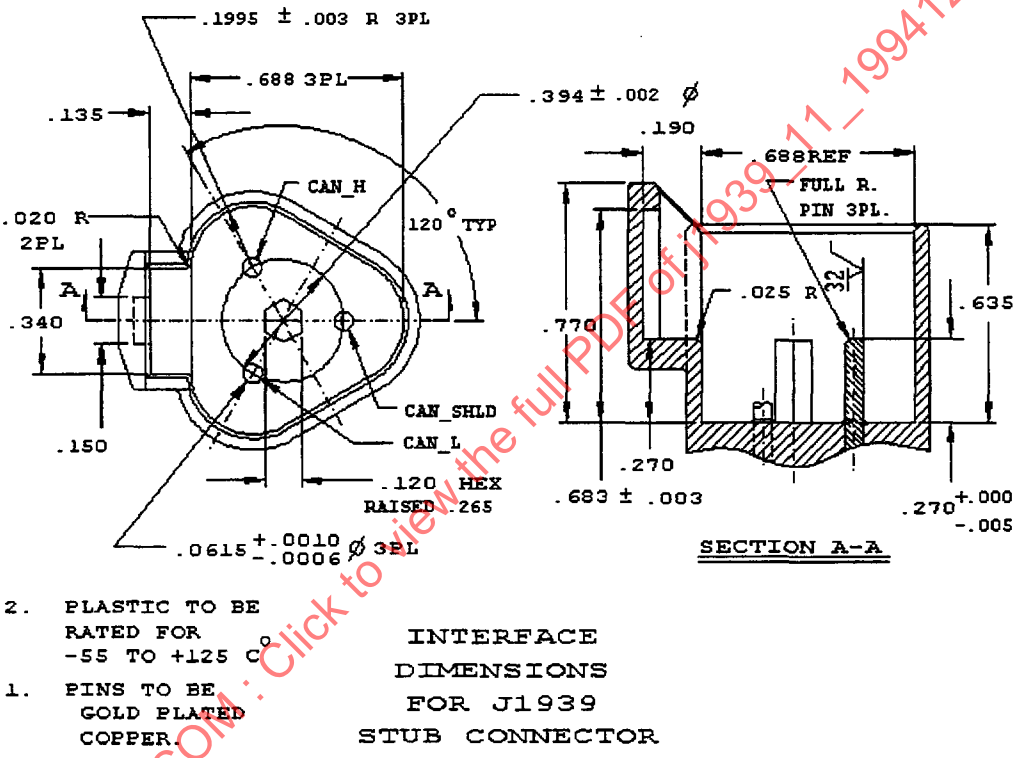


FIGURE 9—STUB CONNECTOR (WITH MALE KEY) DIMENSIONAL REQUIREMENTS (A)

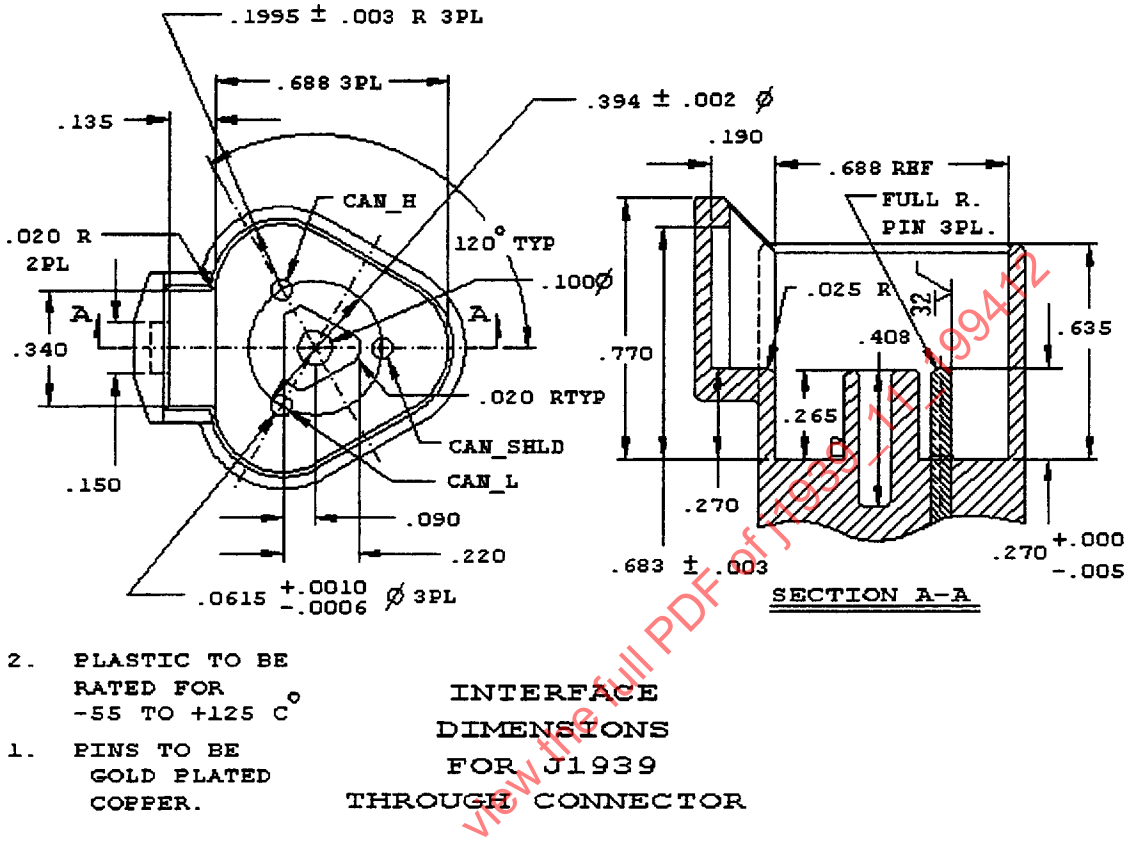


FIGURE 10—THROUGH CONNECTOR (WITH FEMALE KEY) DIMENSIONAL REQUIREMENTS (B)

6. Conformance Tests—The following figures and formulas show, in principle, how the parameters specified in Section 5 should be verified by component manufacturers. The ground connection is not the same as CAN_SHLD. It should be the ECU ground.

6.1 Recessive Output of the ECUs—The recessive output voltage can be measured as shown in Figure 11.

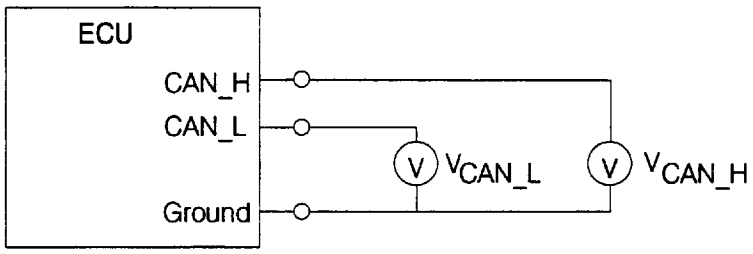


FIGURE 11—MEASUREMENT OF V_{CAN_H} AND V_{CAN_L} DURING THE BUS IDLE STATE

V_{CAN_H} and V_{CAN_L} are measured unloaded while the bus is idle. V_{diff} is then determined by

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad \text{(Eq.2)}$$

Table 3.2 defines the limits during the recessive state.

NOTE—V_{CAN_H} and V_{CAN_L} is measured with no load such that the worst case would be observed for the maximum recessive condition.

6.2 Internal Resistance of CAN_H and CAN_L—The internal resistance, R_{in}, of CAN_H and CAN_L can be measured as shown in Figure 12.

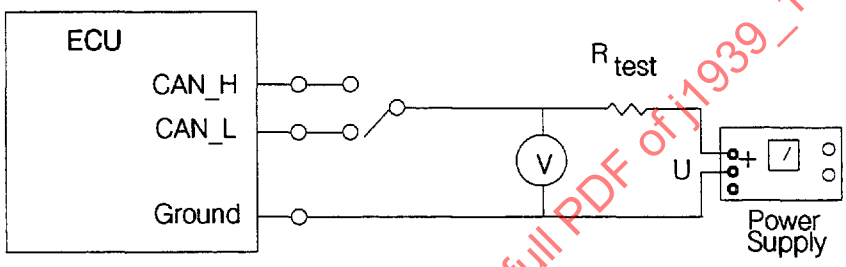


FIGURE 12—MEASUREMENT OF R_{IN} WHILE THE ECU PROTOCOL IC IS SET TO BUS IDLE

R_{in} of CAN_H and CAN_L is determined for U = 0 V and U = 5 V, respectively, with R_{test} = 5 kΩ. R_{in} of CAN_H and CAN_L is then calculated by

$$R_{in} = R_{test} \frac{V_{CAN\_H,L} - V}{V - U} \quad \text{(Eq.3)}$$

where:

V_{CAN_H} and V_{CAN_L} are the open circuit voltages according to Figure 2. R_{in} is defined for the recessive state by Table 3 and Note 4 for DC - Parameters.

6.3 Internal Differential Resistance—The internal differential resistance R_{diff} can be measured as shown in Figure 13.

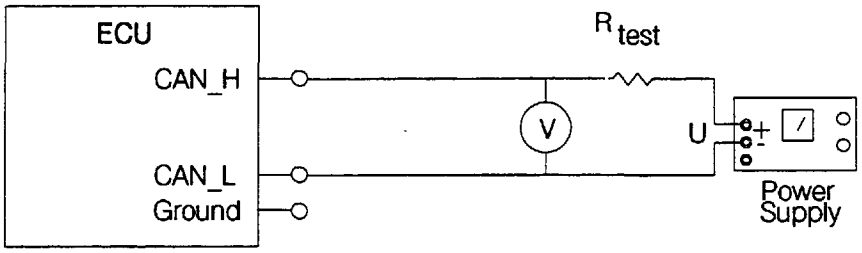


FIGURE 13—MEASUREMENT OF R_{DIFF} WHILE THE ECU PROTOCOL IC IS SET TO BUS IDLE

R_{diff} is determined for U = 5 V and R_{test} = 10 kΩ during bus idle as shown in Equation 4:

$$R_{diff} = R_{test} \frac{(V_{diff} - V)}{V - U} \quad \text{(Eq.4)}$$

where:

V_{diff} is the differential open circuit voltage according to 6.1.

6.4 Recessive Input Threshold of an ECU—The recessive input threshold can be verified over the common mode range as shown in Figure 14.

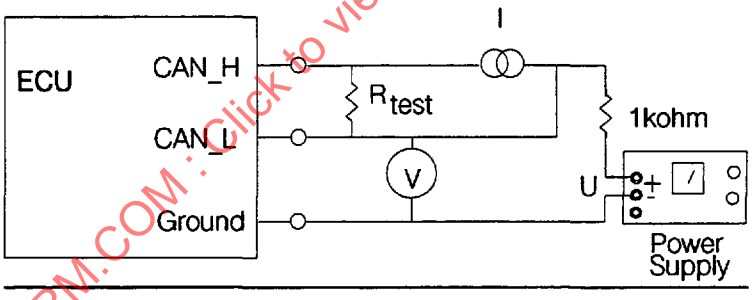


FIGURE 14—TESTING THE INPUT THRESHOLD FOR RECESSIVE BIT DETECTION

Current I is adjusted to a value which develops 0.5 V (the upper limit for detecting a recessive bit during the recessive state) across R_{test} with R_{test} = 60 Ω (Bus Line Load Equivalent Resistance). In addition, U is set to two suitable values that produce V = −2 V and V = 6 V during bus idle. Under these conditions the ECU must not stop transmitting. This indicates that every transmitted recessive bit is still detected as recessive by the protocol IC of the ECU. The level of the dominant bits is nearly independent of U.

NOTE—The 6 V value is used instead of 7 V since the maximum threshold for receiving a recessive bit is 0.5 V per Table 2.

6.5 Dominant Output of an ECU—The dominant output of an ECU can be measured as shown in Figure 15.

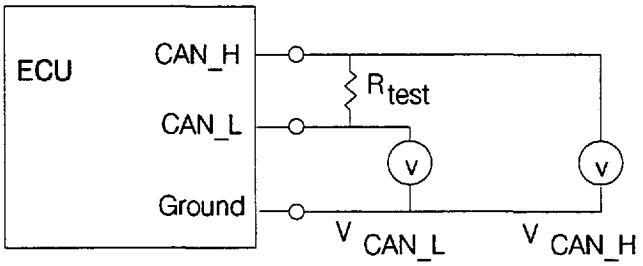


FIGURE 15—MEASUREMENT OF V_{CAN_H} AND V_{CAN_L} WHILE THE ECU SENDS A DOMINANT BIT.

V_{CAN_H} and V_{CAN_L} are measured during a dominant bit transmission. R_{test} is set to 60 Ω. The corresponding value of V_{diff} is given by

$$V_{diff} = V_{CAN\_H} - V_{CAN\_L} \quad \text{(Eq.5)}$$

6.6 Dominant Input Threshold of an ECU—The dominant input threshold of an ECU can be verified over the common mode range as shown in Figure 16.

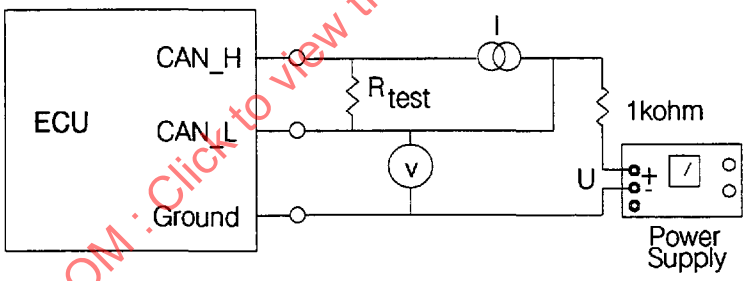


FIGURE 16—TESTING THE INPUT THRESHOLD FOR DOMINANT BIT DETECTION

Current I is adjusted to a value which induces, with R_{test} = 60 Ω (Bus Line Load Equivalent Resistance), the upper threshold of 1 V required to detect a dominant bit during the recessive state. In addition, U is set to two values that produce V = –2 V and V = 6 V during bus idle. Under these conditions, the ECU must stop transmitting the message which demonstrates that arbitration has been acknowledged. This indicates that every transmitted recessive bit is detected as dominant by the protocol IC of the ECU. The level of dominant bits is nearly independent of U.

NOTE—The 6 V value is used instead of 7 V since the maximum threshold for receiving a dominant bit is 1 V per Table 3.

6.7 Internal Delay Time—The internal delay time of an ECU can be measured as shown in Figure 17.

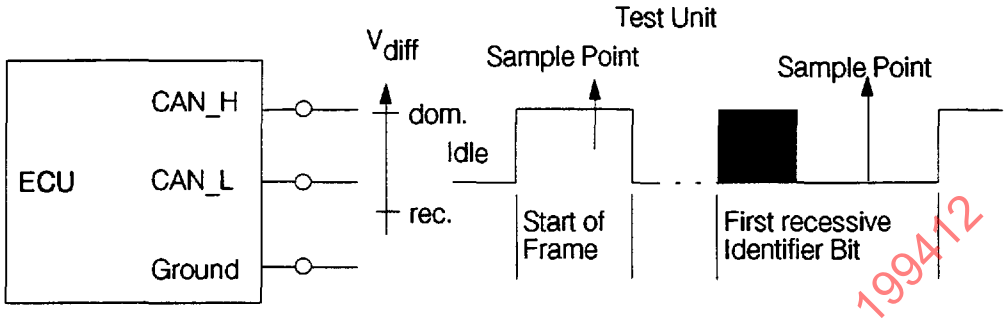


FIGURE 17—MEASUREMENT OF THE INTERNAL DELAY TIME T_{ECU} BY PARTLY OVERWRITING THE FIRST RECESSIVE IDENTIFIER BIT (SHADED AREA) BY A DOMINANT LEVEL UNTIL THE ARBITRATION IS LOST

The test unit shown in Figure 4.7 synchronizes itself to the start of frame bit transmitted by the protocol IC of the ECU. Upon detection of the first recessive identifier bit, the test unit partly overwrites this recessive bit for a time T_{overw} by a dominant level (shaded area in Figure 17). This overwriting is increased until the protocol IC of the ECU loses arbitration and stops transmitting. If this situation is reached, the available part of the bit time T_{avail} for delay time compensation is just exhausted (see also Figure 4). Then t_{ECU} is calculated by

$$t_{ECU} = t_{avail} - t_{overw} \quad \text{(Eq.6)}$$

where:

t_{avail} is known from the bit timing unit of the protocol IC and t_{overw} is known from the test unit.

The dominant and recessive voltage levels are set by the test unit to the corresponding threshold voltages for reception. This means that the dominant overwriting level is 1 V, and the recessive level is 0.5 V. This ensures a uniquely defined relationship between voltage levels and internal delay time.

7. Discussion of Bus Failures

a. Possible Failures—During normal operation, several bus failures can occur that may influence operation. These failures and the resulting network behavior are specified subsequently.

7.1 Loss of Connection to Network—If a node becomes disconnected from the network, the remaining nodes shall continue communication.

7.2 Node Power or Ground Loss—If a node loses power, or if it is in a low voltage condition, the network is not loaded down, and the remaining nodes shall continue communication.

If a node loses ground, the network shall not be biased up. The remaining nodes shall continue communication.