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SURFACE VEHICLE INFORMATION REPORT

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(R) Design/process Checklist for Vehicle Electronic Systems

Foreword—To obtain a high degree of quality and reliability, a wide variety of subjects needs to be addressed when designing a vehicle electronic system. No single designer can be expected to have the experience necessary to consider all aspects of a design. Such experience is often spread throughout an organization and not concentrated on any one project.

The main purpose of this checklist is to provide a guide for ensuring that the many aspects of an electronic systems design are addressed. Such a list would be useful for design reviews, "fresh eyes" reviews and for education/training.

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1. ***Scope—***The following subjects reflect the automotive environment and are based on good engineering practices and past ("lessons learned") experiences. Since it is impossible to be all inclusive and cover every aspect of quality and reliability, this document should be used as a basis for preparation of a more comprehensive and detailed checklist that reflects the accumulated "lessons learned" at a particular Company.

It is not the intent of this document to give a lot of detail, only to point out the type of subjects that need to be investigated and acted upon.

2. ***References***

2.1 Applicable Publications—The following publications form a part of the specification to the extent specified herein. Unless otherwise indicated the latest revision of SAE publications shall apply.

2.1.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE AE-9—Automotive Electronics Reliability Handbook, Feb., 1987
SAE J551 ALL PARTS—Performance Levels and Methods of Measurement of Electromagnetic Compatibility of Vehicles and Devices
SAE J1113 ALL PARTS—Electromagnetic Compatibility Measurement Procedures and Limits for Vehicle Components
SAE J1211—Recommended Environmental Practices for Electronic Equipment

2.1.2 MILITARY SPECIFICATIONS (LATEST VERSIONS)—Available from DODSSP, Subscripton Services Desk, Building 4D, 700 Robins Avenue, Philadelphia, PA 19111-5094.

Mil-Std 202—Test Methods for Electronic and Electrical Component Parts
Mil-Std 217—Reliability Prediction of Electronic Equipment
Mil-Std 781—Reliability Design Qualification and Production Acceptance Tests. Exponential Distribution
Mil-Std 810—Environmental Test Methods and Engineering Guidelines
Mil-Hdbk 251—Reliability Design Thermal Applications
Mil-Std 883—Test Methods and Procedures for Microelectronics
Mil-Std 461—Requirements for the Control of Electromagnetic Emissions and Susceptibility

2.2 Other Publications

Walker, The Design Analysis Handbook, ISBN 0-9641527-0-3
Horowitz and Winfield, The Art of Electronics, ISBN 0-521-37095-7
Paul, Introduction to Electromagnetic Compatibility, ISBN 0-471-54927-4
Ott, Noise Reduction Techniques in Electronic Systems, ISBN 0-471-85068-3
Johnson, Graham, High Speed Digital Design, ISBN 0-13-395724-1
Automotive Electronics Council, Stress Test Qualification for Automotive-Grade Integrated Circuits, CDF-AEC-Q100

3. Design Checklist

3.1 Component Selection/Application—One of the first major concerns for a reliable design is part selection and application. Vendor part quality is a major reliability concern. Efforts to use best in class suppliers cannot be overemphasized. Much of the input for this topic will come from the Corporate Electronic Components Department.

a. _____ Identify critical reliability components—e.g., power transistors/zeners.
b. _____ Determine special requirements for these critical components—derating, screening, handling, failure mode response.
c. _____ Identify components to avoid—e.g., variable resistors if fixed can be used, hand inserted parts if auto insertion viable.
d. _____ Establish part availability.
e. _____ Define part specifications—Part sheets should reflect use in actual automotive environment.
f. _____ Determine testing sample size—statistical significance, attribute or variable data, cost/time/test facility limitations.
g. _____ Address Electrostatic Discharge—most sensitive components, precautions, handling.
h. _____ Define vendor quality/reliability control program.
i. _____ Determine Acceptable Quality Level (AQL) in Parts/Million (PPM) required—how verified.
j. _____ Define process flow/control plans.
k. _____ Define process change procedures.
l. _____ Determine closed loop failure analysis, corrective action plan.
m. _____ Determine degree of component Statistical Process Control (SPC)—where used, adherence, effect on AQL.

3.2 Thermal Considerations (Components/Assemblies)—Temperature has a major effect on reliability. In fact, as the temperature of a system rises, thermal failures almost completely overweigh failures from other causes.

a. _____ Conduct thermal survey of environment (underhood, passenger compartment, etc.)—start temperature (heat, cold soak), warm up time, operational temperature (range, rate of temperature change, frequency of change), number of cycles, cooling effects.
b. _____ Determine assembly (module) temperature environment versus reliability—field experiences.
c. _____ Conduct component (resistor, capacitor, transistor, diode, etc.) thermal analysis—worst-case analysis (electrical loading, environment), heat sinking, derating (safety margins).
d. _____ Conduct assembly (module) thermal analysis—worst-case analysis (electrical loading, environment), heat sinking, derating (safety margins).
e. _____ Consider that thermal analysis using thermal resistance values is best case—does not consider non-linearity (hot spots), interface bonds <100% of area.
f. _____ Conduct thermal testing evaluation—e.g., thermocouple critical areas in module and test under worst-case electrical loading and environment in temperature chamber. Vehicle evaluation shall also be done (temperature chamber, wind tunnel, etc).
g. _____ Consider different expansion coefficient stresses—potting, conformal coating, Surface Mount Devices (SMD's), Leadless Chip Carriers (LCC's), PCB interfaces, etc.
h. _____ Define rules (thermal) for mounting components.
i. _____ Define rules (thermal) for mounting assemblies (modules).
j. _____ Address thermal shock (splash, cold start)—typical failure modes.
k. _____ Identify critical components and their special requirements.
l. _____ Define thermal stress test for Design Verification—tailored to find defects in new design, should be failure oriented (overstressed). Temperature cycling profile—extremes, number of cycles, rate of change, when powered, parameters monitored.
m. _____ Define thermal stress test for Qualification—mission life oriented. Temperature cycling profile—extremes, number of cycles, rate of change, when powered, parameters monitored.
n. _____ Define thermal stress test for Production Acceptance—should include Environmental Stress Screening (ESS) tailored to reduce infant mortality and precipitate process problems. Temperature cycling profile—extremes, number of cycles, rate of change when powered, parameters monitored.
o. _____ Consider that combined thermal stress with other tests (e.g., thermal, vibration, humidity, voltage) more realistic.
p. _____ Define testing sample size—statistical significance, attribute or variable data, cost/time/test facility limitations.

3.3 Vibration/Shock Considerations (Components/Assemblies)

a. _____ Conduct vibration/shock survey of environment (underhood, passenger compartment, etc.)—conditions (bumps/potholes, road vibration, handling, rail shock), type (sine, random, complex), frequency range, amplitude/Power Spectral Density (PSD), axis, duration.
b. _____ Address stresses on components, bonds, mounting brackets, etc.—concerns, typical failure modes.
c. _____ Define rules for mounting components—e.g., part size/mass versus mounting technique.
d. _____ Define module mounting techniques—consider mounting bracket effects (e.g., resonance's).
e. _____ Consider resonance's—conduct resonant search, failure modes, solutions.
f. _____ Define vibration test for Design Verification—tailored to find defects in new design, should be failure oriented (overstressed). Type (sine, random, complex), frequency range, amplitude/PSD, axis, duration, monitored to detect intermittents.
g. _____ Define vibration test for Qualification—mission life oriented. Type (sine, random, complex), frequency range, amplitude/PSD, axis, duration, monitored to detect intermittents.
h. _____ Define vibration test for Production Acceptance—should include Environmental Stress Screening (ESS) tailored to reduce infant mortality and precipitate process problems. Type (sine, random, complex), frequency range, amplitude/PSD, axis, duration, monitored to detect intermittents.
i. _____ Define shock test for Design Verification, Qualification, and Production Acceptance—similar to vibration above.
j. _____ Conduct vibration/shock testing before climatic testing (if done separately).
k. _____ Consider that vibration/shock combined with temperature cycling, humidity more realistic.
l. _____ Define testing sample size—statistical significance, attribute or variable data, cost/time/test facility limitations.

3.4 Humidity/Splash/Dust Considerations (Components/Assemblies)

a. _____ Address component/assembly sealing—gasketing, potting, etc.
b. _____ Address connector integrity—type of connector (open, sealed, greased, etc).
c. _____ Determine failure modes—shunt or series impedance.
d. _____ Define test procedure for Design Verification—similar to 3.2, 3.3.
e. _____ Define test procedure for Qualification—similar to 3.2, 3.3.
f. _____ Define test procedure for Production Acceptance—similar to 3.2, 3.3.
g. _____ Consider that more realistic if combined with temperature cycling, vibration.
h. _____ Define testing sample size—statistical significance, attribute or variable data, cost/time/test facility limitations.

3.5 Burn In

a. _____ Determine need, component versus assembly or both—field correlation, experiences, cost analysis.
b. _____ Determine component burn-in requirements—which ones, more stress than assembly, minimizes rework. If ppm failure rates low, burn-in may make worse (handling, ESD).
c. _____ Determine assembly burn-in requirements—thermal mass test considerations.
d. _____ Define test conditions—elevated temperature and voltage accelerates failure modes (different times for different failure modes). Static, dynamic operation.
e. _____ Determine optimum burn-in empirically—time versus temperature/voltage failure rates.
f. _____ Consider combined powered thermal cycle and burn-in.
g. _____ Define testing sample size—statistical significance, attribute or variable data, cost/time/test facility limitations.

3.6 Electromagnetic Compatibility (EMC)

3.6.1 Component (Module) Level

a. ____ Define Radiated Immunity requirements:

1. Low RF level (25 V/m)—represents low power (<10 W) transmitters located in/near vehicle. Also Radio, TV, Amateur, Land Mobile, etc., in vicinity of vehicle
2. Moderate RF level (50 V/m)—represents nearby transmitters (30 to 100 W), low power on-board transmitters in close proximity to electronics
3. High RF level (100 V/m)—represents high power (100 W) on-board transmitters.
4. Test procedures—SAE J1113

b. ____ Define Conducted Immunity requirements:

Supply Voltage:

1. Normally 10 to 16 V (at battery)—Reference charging system voltage versus temp.
2. Reverse battery (–14 V, includes servicing and vehicle assembly conditions).
3. Overvoltage—Failed regulator (19), double voltage jump start (24 V).
4. Cold start = 5 to 6 V.
5. Voltage dropouts—Contact bounce, ignition switch rotation, intermittent connections
6. Vehicle electrical system noise (e.g., Alternator ripple, load dump, switch arcing, inductive transients, groundshifts).
7. Address temperature for above conditions.
8. Test procedure—SAE J1113.

c. ____ Define Radiated Emissions requirements:

1. On-board entertainment/communications antennas and radio sensitivities determine specification limit.
2. Test procedures—SAE J1113

d. ____ Define Conducted Emissions requirements:

1. Similar intent as Radiated Emissions.
2. Test Procedures—SAE J1113

e. ____ Define Electrostatic Discharge (ESD) requirements:

1. Test for occupant touching in normal use, shipping/handling
2. Test procedure—SAE J1113

3.6.2 PCB Layout Rules for EMC

a. ____ Use ground plane for interconnecting circuit grounds—ideally greater than 50% of PCB area.
b. ____ Minimize loop areas especially in high-speed digital circuits.
c. ____ Minimize common impedance—sensitive circuits not shared with high rate of current change (dI/dT) circuits. E = L * dI/dT (typically, L = 25 nh/in).
d. ____ Use decoupling capacitors very near IC's, especially microprocessors and high dI/dT circuits. Use ground plane between capacitor and IC ground.
e. ____ Input/Output filtering configurations—near entry of Input/Output, grounded via ground plane.

3.6.3 VEHICLE LEVEL CHECKLIST

3.6.3.1 Address vehicle EMC wiring guidelines:

a. _____ Low level signals—do not use sheet metal return.
b. _____ Maintain low resistance between body panels/structures.
c. _____ Avoid unterminated wires—acts as antenna.
d. _____ Sensitive wiring >5 cm from secondary ignition parts (e.g., ignition wires, coil, plugs, distributor).
e. _____ Test for wiring cross-coupling and correct (separation, twisting, etc).
f. _____ Twisted wires—effective low cost option for noise reduction.
g. _____ Wire shielding—verify need (usually needed for wire cross-coupling), insure coverage in area of noise, single point ground (drain wire short).
h. _____ Optimize wire routing near sheet metal.
i. _____ Analyze multiple grounds—ground loops.
j. _____ Inductive loads—test for noise and if excessive suppress.
k. _____ Insure reliability of ground connections to sheet metal.
l. _____ Ignition arc over—maintain separation, "non-conductors" may be conductive (e.g., carbon-loaded hoses, wet plastic).

3.6.3.2 Define vehicle EMC test procedures:

a. _____ Internally generated EMI—check interactions of subsystems under various conditions.
b. _____ Radiated immunity—10 KHz to 1 GHz or higher, powerlines, nearby lightning.
c. _____ Radiated emissions
d. _____ ESD
e. _____ Charging system anomalies—disconnected battery (engine running), load dump, malfunctioning regulator, reverse battery.
f. _____ Test Procedures—SAE J551

3.7 Circuit Design Checklist

3.7.1 GENERAL

a. _____ Implement Design Process:

1. Must put emphasis on “Up-Front” part of process.
2. Test for confirmation, not “catch all” at end of process.
3. Technical Design Reviews, audits at various stages.
4. Design change procedures.
5. Closed loop failure analysis and corrective action plan—concern description, define root cause, containment, corrective actions, verification of containment/corrective actions, prevent recurrence.
6. Analyze warranty returns—"non-defective returns" often >50% of returns. Normal reliability testing will often not find problems. Testing must emphasize module functionality (continuously monitored).

b. _____ Identify critical characteristics from customer perspective—Quality Functional Deployment (QFD).
c. _____ Conduct Fault Tree Analysis—Module, Subsystem, System (Before Circuit design).
d. _____ Conduct Failure Modes and Effects analysis—Module, Subsystem, System level (After circuit design).
e. _____ Conduct Criticality analysis (severity/probability of occurrence)—module, subsystem, system level.
f. _____ Define Limited operation strategy.

g. _____ Consider that wiring harness reliability affects module warranty.
h. _____ Address design for manufacturability—see process guidelines, Section 4.
i. _____ Address design for testability.
j. _____ Consider that breadboards may aggravate problems—long leads, poor ground(s).
k. _____ Determine use of discrete versus custom circuits—cost, reliability, volume tradeoffs. For custom circuits, use pessimistic cost/timing.
l. _____ Determine redundancy requirements—critical circuits.
m. _____ Use bookshelf circuits where possible.
n. _____ Maximize use of proven circuits.
o. _____ Minimize number of parts.
p. _____ Maximize use of standard parts and widest tolerances.
q. _____ Use slowest speed technology consistent with function.
r. _____ Where possible, include hysteresis on analog/digital circuits.
s. _____ Terminate unused inputs to I.C.'s.
t. _____ Consider relay precautions—e.g., diode increases dropout time, contact arcing, transients, contact sticking.
u. _____ Determine potting, conformal coating requirements—where used, types, limitations.
v. _____ Limit standby current.
w. _____ Determine load power management strategy—when different loads turned on/off as voltage varies.
x. _____ Allow for impedance buildup during system life.
y. _____ Consider Derating.

3.7.2 COMPONENTS—SPECIFIC DEVICES

3.7.2.1 Resistors:

a. _____ Address reliability concerns
b. _____ Consider failure modes (e.g., opens most common)
c. _____ Consider tolerances (initial, aging, temp)
d. _____ Use in Safe Operating Area (power dissipation, volt, temp)
e. _____ Consider ESD.

3.7.2.2 Capacitors:

a. _____ Address reliability concerns
b. _____ Consider failure modes (e.g., shorts, value change most common)
c. _____ Consider tolerances (initial, aging, temp)
d. _____ Use in Safe Operating Area (DC/transient voltage, temp, ripple current)
e. _____ Consider ESD.

3.7.2.3 Connectors/interconnects:

a. _____ Types: Between PCB's (e.g., individual wires, flat cable, flex cable), Pin/socket connector to wiring harness. Blade/socket connector to wiring harness.
b. _____ Address reliability concerns, failure modes.
c. _____ Address "Dry" circuits—low voltage, film buildup (low current = gold)
d. _____ Consider insertion force.
e. _____ Avoid IC sockets.
f. _____ Account for voltage drops, intermittent connections, aging (increased resistance).

3.7.2.4 Printed Circuit Boards (PCB's):

a. _____ Address reliability concerns, failure modes—Opens, shorts, warpage.
b. _____ Avoid use of edge connectors (if applicable) to wiring harness—reliability subject to many parameters, e.g., plating uniformity, tolerances.
c. _____ Define material selection.
d. _____ Determine copper thickness (1 oz, 2 oz, 3 oz).
e. _____ Consider tolerances.
f. _____ Address thermal considerations (e.g., max temp rating, matching of thermal expansions, localized heating = delamination).
g. _____ Address manufacturability criteria (see Section 4). Allow for process cleanliness (shunt resistance).
h. _____ Address EMC criteria (see 3.6.2).

3.7.2.5 Thick Film Substrates:

a. _____ Address reliability concerns, failure modes.
b. _____ Determine material selection.
c. _____ Consider tolerances.
d. _____ Address thermal considerations (e.g., max temp rating, matching of thermal expansions).
e. _____ Address manufacturability criteria (see Section 4).
f. _____ Address EMC criteria (see 3.6.2).

3.7.2.6 Transistors/Diodes/MOSFET's:

a. _____ Address reliability concerns, failure modes.
b. _____ Consider tolerances (initial, aging, temp).
c. _____ Consider diode/zener response time to transients.
d. _____ Use within Safe Operating Area (SOA). Transient conditions, temperature.
e. _____ Use transistor base to emitter resistor.
f. _____ Consider collector to housing stray capacitance for switching circuits—may cause radiated emissions.
g. _____ Limit base/gate drive—fast drive into saturation creates noise, balance Electromagnetic Interference (EMI) with heat dissipation.
h. _____ Consider ESD on MOSFET's—one of major failure modes.

3.7.2.7 Linear (Op Amps, etc):

a. _____ Consider single supply limitations—input range usually does not include power supply rails, output loading determines voltage range.
b. _____ Do not overdrive inputs—may drive output to power supply rail (transmits power supply noise).
c. _____ High gain amplifier—stability, oscillations, stray capacitance, and inductance varies with temperature/sample.
d. _____ Use Bode gain/phase plot analysis to determine stability margin.
e. _____ Differential amps—consider all sources of unbalance to ground, DC and AC (e.g., capacitors, source impedance).
f. _____ Differential amps limited in rejection of common mode signals at higher frequencies.
g. _____ Use op amp internal compensation capacitor, if accessible, for filtering (acts as non-linear filter).
h. _____ Voltage follower latch up—input levels too high.
i. _____ Avoid high impedances.

3.7.2.8 Digital (microprocessors, etc.):

a. _____ Consider fanout limitations—e.g., loading affects propagation delays especially for CMOS.
b. _____ Verify logic levels compatible over min. and max. temperature/specification limits.
c. _____ Maximize logic levels margins (e.g., V low max and V high min).
d. _____ CMOS—latchup when input > power supply or < ground.
e. _____ Microprocessor clock—verify operation, including start up, under all temperature and power supply transitions.
f. _____ Other microprocessor topics—address reset, low voltage inhibit, I/O pin assignment, A/D inputs, interrupts, timer/PWM.

3.7.3 MODULE INPUTS

a. _____ Protect for shorts to ground/power.
b. _____ Switch requirements—consider contact material/pressure, type of connector, minimum voltage/current for oxidation burn through (dry circuits).
c. _____ Allow for contact resistance, shunt resistance (connectors, harness).
d. _____ Maximize input thresholds for noise immunity.
e. _____ Maximize input filtering considering maximum signal information delay, minimum signal pulse width to be recognized, fastest signal rate of change (dV/dT).
f. _____ Verify shared sensors compatible—i.e., one sensor to multiple modules.

3.7.4 MODULE OUTPUTS

a. _____ Protect for shorts to ground/power.
b. _____ Verify inductive driver transient protection.
c. _____ Output driver current source versus current sink considerations—current source has same failure mode (wiring short or open).
d. _____ Limit high-current actuator transition times (without overheating)—generates noise, wiring harness ringing.
e. _____ H—Bridge driver—ensure both drivers in each leg not on simultaneously during transitions.

3.7.5 POWER SUPPLY RELATED

a. _____ Verify circuits compatible with run—start—run cycle (starting) et al.
b. _____ Verify power up/down sequence.
c. _____ Consider overvoltage, undervoltage, reverse voltage, load dump.
d. _____ Address power supply protection schemes.
e. _____ Address power supply regulator response time—not too fast or may be noise sensitive.
f. _____ Verify stability over temp—transient response on input and output.
g. _____ Power supply capacitor design—e.g., aluminum electrolytic voltage/temperature, ripple calculations.
h. _____ Avoid voltage divider circuits, if used consider worst-case power supply voltages.
i. _____ Minimum current draw may deregulate power supply.
j. _____ Consider that two power supplies may cause latch up if not tracking.
k. _____ For mixed technologies (e.g., CMOS, TTL), power up/down may produce errors due to different valid/invalid levels.

3.7.6 ELECTRICAL OVERSTRESS

a. _____ Address ignition arc over design considerations for underhood applications.
b. _____ Address transient protection—Resistor, Capacitor, R/C, clamps (e.g., zener, diode).
c. _____ All circuits connected to main power, or through loads to main power, must withstand electrical overstress.
d. _____ Shutdown circuits must have fast response.
e. _____ Address ESD protection: Often misanalyzed as electrical overstress. Part (e.g., IC) protection limited—too slow (ESD <5 ns). Use Resistor, Capacitor, R/C, clamps—consider high peak voltage.

3.7.7 CIRCUIT TOLERANCE/ANALYSIS

a. _____ Conduct circuit/tolerance analysis:

1. Use combination of Worst-Case Analysis (WCA), Probabilities, Sensitivities, Risk Assessment and Design Centering.
2. Monte Carlo method—determines "likely" performance, useful for complex circuits.
3. Design of Experiments, Taguchi methods.

b. _____ Determine simulation requirements—Realistic assumptions, must correlate with bench, not substitute for analysis.
c. _____ Determine Reliability Prediction models used for assembly:

1. Major concerns for electronic modules are not catastrophic—mainly functionality issues.
2. Use field experience—reliability growth model, similar equipment, complexity/function, physics of failure.
3. Mil-Std 217—Limited use, narrow focus, does not address major "real world" concerns.

d. _____ Conduct sneak circuit analysis.

3.8 Software

a. _____ Use modularization.
b. _____ Optimize decoupling with other software modules.
c. _____ Design for testability.
d. _____ Determine documentation requirements.
e. _____ Allow sufficient time for testing and debug—can be as much as design and coding.
f. _____ Determine software module testing—simulation on mainframe.
g. _____ Define static (change inputs manually) bench testing of system (total program).
h. _____ Define dynamic (many combinations of inputs) design verification on mainframe simulator.
i. _____ Address fault tolerance—e.g., inputs within realistic limits (e.g., dV/dT, dFreq./dT, edges, change in A/D counts), revert to old data, ignore, try again.
j. _____ Define watchdog timer strategy and implementation.
k. _____ Define low voltage reset strategy.
l. _____ Define software noise immunity strategies and limitations.
m. _____ Define switch contact bounce strategy.
n. _____ Determine software development tools—portable engineering and calibration consoles.
o. _____ Determine vehicle testing program.

3.9 Diagnostics

a. _____ Determine what functions to check—assign probability/severity index.
b. _____ Determine diagnostic troubleshooting procedures—philosophy, documentation.
c. _____ Diagnostics considered in warranty analysis.
d. _____ Define built in monitor circuits.
e. _____ Determine warning indicator requirements—e.g., instrument panel light.
f. _____ Address intermittents—how to precipitate, store in non-volatile memory.
g. _____ Define self test methodology—factory and field service.
h. _____ Determine test equipment requirements.
i. _____ Define software memory allocation.

3.10 Repairability

a. _____ Determine level (module replace versus sub-module replace).
b. _____ Consider module partitioning for repair.
c. _____ Consider cost models based on warranty forecasting.
d. _____ Factor accessibility—harder to replace item within system will have better warranty.
e. _____ Address, remanufacturing (if applicable), rework considerations, including vehicle In-Plant repair.

4. Process Checklist—The manufacture of electronic components/modules is a process that is continually being changed. These guidelines are basically intended for the module design engineer so that a greater appreciation of what is involved can be obtained and considered in the early design stages.

4.1 Through Hole (TH) Technology

4.1.1 General TH Design Checklist

a. _____ For single-sided PCB, conductor width = 0.012 in minimum (conservative), 0.008 in (realistic).
b. _____ For double-sided PCB, power/ground conductor width = 0.016 in minimum. Signal conductor width = 0.012 in minimum (conservative), 0.008 in (realistic).
c. _____ Plated through hole (PTH) pad diameter = or > 2 x hole diameter.
d. _____ PTH diameter = or > 40% of material thickness.
e. _____ PTH double-sided—hole diameter 0.010 to 0.028 in > lead diameter.
f. _____ PTH single-sided—hole diameter 0.005 to 0.020 in > lead diameter.
g. _____ Do not use sharp corners for conductor traces.
h. _____ Web between holes—for punched holes = 0.060 in minimum or 1.5 times hole diameter, whichever is greater. For drilled holes = 0.035 in minimum.
i. _____ Warpage—balance copper density within 30% both sides. For large copper areas (e.g., ground plane), use voids at random intervals.
j. _____ Use thermal relief around component holes in large copper areas.
k. _____ Auto insertion—hole diameter > 0.015 in over lead diam min.
l. _____ Lead formed double kink parts for PTH—euroform type preferred, stress relief, trapped gas in PTH area.
m. _____ For clinched leads, use tear drop pads—more bonding area.
n. _____ Solder mask—types (screened, dry film).