SURFACE VEHICLE RECOMMENDED PRACTICE

J1879 FEB2014

Issued 1988-10
Revised 2014-02

Superseding J1879 OCT2007

(R) Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications

RATIONALE

Error and issue corrections with latest state of art updates.

FOREWORD

The quality of the vehicles we buy and the competitiveness of the automotive industry depend on being able to make quality and reliability predictions. Qualification measures must provide useful and accurate data to provide added value. Increasingly, manufacturers of semiconductor components must be able to show that they are producing meaningful results for the reliability of their products under defined mission profiles from the whole supply chain.

Reliability is the probability that a semiconductor component will perform in accordance with expectations for a predetermined period of time in a given environment. To be efficient reliability testing has to compress this time scale by accelerated stresses to generate knowledge on the time to fail. To meet any reliability objective requires comprehensive knowledge of the interaction of failure modes, failure mechanisms, the mission profile and the design of the product 10 years ago you could read: “Qualification tests of prototypes must ensure that quality and reliability targets have been reached”.

This approach is no longer sufficient to guarantee robust electronic products for a failure free life of the car, which is the intention of the Zero-Defect-Approach. The emphasis has now shifted from merely the detection of failures to their prevention.

We started this way by introducing screening methods after the product had been produced after product has successfully survived a standard qualification. Then the focus shifted to reliability methodologies applied on technology level during development.

Now product qualification again changes from the detection of defects based on predefined sample sizes towards the generation of knowledge by generating failure mechanisms specific data, combined with the knowledge from the technology field. Now we can generate real knowledge on the robustness of products.

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Qualification focuses on intrinsic topics of products and technologies, requiring only small sample sizes. Defectivity issues now put a big load on monitoring measures, which are now needed to demonstrate manufacturability and the control of extrinsic defects.

This handbook should give guidance to engineers how to apply robustness validation during development and qualification of semiconductor components. It was made possible because many companies, semiconductor manufacturers, component manufacturers (Tier1) and car manufacturers (OEMs) worked together in a joint working group to bring in the knowledge of the complete supply chain.

I would like to thank all teams, organizations and colleagues for actively supporting the robustness validation approach.

Andreas Preussger
Core Team Leader RV Group
Editor in Chief 1st revision

ACKNOWLEDGEMENT

We would like to thank the team members of various committees and their associates for their important contributions to the completion of the 1st revision this handbook. Without their commitment, enthusiasm, and dedication, the timely compilation of the handbook would not have been possible.

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1. INTRODUCTION

In 2006 members of SAE International Automotive Electronic Systems Reliability Standards Committee, ZVEI (German Electrical and Electronic Manufacturers` Association), AEC (Automotive Electronics Council) and JSAE (Japanese Society of Automotive Engineers) formed a joint task force and published the first version of the Robustness Validation Handbook (RVHB) together with an update of the corresponding SAE document (SAE Recommended Practice J1879, General Qualification and Production Acceptance Criteria for Integrated Circuits in Automotive Applications), which was a content copy of the RVHB.

The RVHB was based on information from a wide number of sources including international Automotive OEMs and their full supply chain, engineering societies, and other related organizations.

This Robustness Validation Handbook provides the automotive electronics community with a common qualification methodology to demonstrate acceptable reliability. The Robustness Validation approach requires testing the component to failure, or end-of-life (EOL), avoiding invalid failure mechanisms, and evaluation of the Robustness Margin between the outer limits of the customer specification and the actual performance of the component.

Since then the principles defined in this handbook have been applied in modules, systems and other application areas. For details see section 19.

2. SCOPE

This document will primarily address intrinsic reliability of electronic components for use in automotive electronics. Where practical, methods of extrinsic reliability detection and prevention will also be addressed. The current handbook primarily focuses on integrated circuit subjects, but can easily be adapted for use in discrete or passive device qualification with the generation of a list of failure mechanisms relevant to those components. Semiconductor device qualification is the main scope of the current handbook.

Other procedures addressing extrinsic defects are particularly mentioned in the monitoring chapter. Striving for the target of Zero Defects in component manufacturing and product use it is strongly recommended to apply this handbook. If it gets adopted as a standard, the term “shall” will represent a binding requirement.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.

3. TERMS, DEFINITIONS AND ABBREVIATIONS

3.1 Terms and Definitions

3.1.1 Accelerated Test

A test using test conditions that are more severe than usual operating conditions.

3.1.2 Acceleration Factor

The ratio between the times necessary to obtain the same portion of failure in two equal samples under two different sets of stress conditions, involving the same failure modes and mechanisms.

3.1.3 Commodity Product

A product for which there is a demand without qualitative differentiation across a market. It is produced for a group of customers or one or several markets or application segments e.g., Standard Logic IC’s or small signal transistors. For details see RVManual.

3.1.4 Component (general)

A constituent part.

NOTE 1: Examples include source and drain regions as components of transistors, lead frames and dies as components of packaged integrated circuits, resistors and integrated circuits as components of printed circuit boards, motherboards as components of computers, LCD screens as components of monitors, ac and dc components of complex waveforms, and loops and algorithms as components of software programs.

NOTE 2: Unless the context identifies the thing of which a component is a part, a descriptive prepositional phrase identifying the thing should follow the word “component”.

3.1.5 Defect

A deviation in an item from some ideal state. The ideal state is usually given in a formal specification.

3.1.6 Degradation

A gradual deterioration in performance as a function of time.

3.1.7 De-rating

The intentional reduction of stress/strength ratio in the application of an item, usually for the purpose of reducing the occurrence of stress related failures.

3.1.8 Device

A piece of equipment, a mechanism, or another entity designed to serve a special purpose or perform a special function.

3.1.9 Electronic Component

A self-contained combination of electronic parts, subassemblies, or assemblies that perform an electronic function in the overall operation of equipment.

3.1.10 Extrinsic Reliability

The reliability not related to intrinsic failure mechanisms; but to process induced deviations, being random in nature.

3.1.11 Failure Mechanism

The physical, chemical or other process that results in a failure. A failure mechanism describes how a degradation process precedes, e.g., oxidation, cracking. If the driving forces are known, e.g., electric field, current density, temperature, an empirical or theoretically based acceleration model can be proposed or derived that allows for failure rate modeling.

3.1.12 Failure Mode

The effect or manner by which a failure is observed to occur. It is the effect of the failure mechanism.

3.1.13 FMEA

Failure Mode and Effects Analysis. A systematized group of activities intended to recognize, evaluate, and prioritize the potential failure of a product or process and its effects, and to identify actions that could eliminate or reduce the chance of the potential failure occurring, listed in the order of effect on the customer.

3.1.14 Go, No-Go

Attribute data, which is data that results from counting items or classifying items into distinct non-overlapping categories; in this case, pass/fail data.

3.1.15 Intrinsic Reliability

The reliability related to the inherent material properties or design, being systematic in nature.

3.1.16 Component Life Cycle

Time period between the completion of the manufacturing process of the semiconductor component and the end of life of the vehicle.

3.1.17 Life Cycle

The time span between the beginning of development (specification) and the end of production (withdrawal from the market).

3.1.18 Lifetime

The time span between initial operation and failure.

3.1.19 Matrix Lot

A wafer lot manufactured in such a way that groups of wafers are intentionally processed to create high and low extremes in several parameters important to yield, functionality and/or reliability. Examples include transistor threshold voltage, effective channel length, conductor sheet resistance and transistor beta.

3.1.20 Matrix Lot Plan

A description of the parameters and extremes of the matrix lot per wafer.

3.1.21 Mission Profile

The simplified representation of all of the relevant conditions to which the devices will be exposed in all of its intended application throughout the full life time covering production, handling, storage and transportation.

3.1.22 Operating Conditions

The conditions of environmental parameters, voltage bias, and other electrical parameters whose limits are defined in the datasheet and within which the device is expected to operate reliable.

3.1.23 Product Robustness

The ability of a product to remain in control and capable within the expected variations of inputs (application, manufacturing, transport and storage conditions).

3.1.24 Qualification

The entire process by which products or production technologies are obtained, examined and tested, and then identified as qualified.

3.1.25 Reliability Characteristic

A parameter that characterizes the probability that a device will function without failure over a specified time period or amount of use at stated conditions.

3.1.26 Reliability Characterization

The process that characterizes the probability that a device will function without failure over a specified time period or amount of usage at stated conditions.

3.1.27 Reliability Parameter

See reliability characteristic.

3.1.28 Robust Condition

A condition at which the product remains in control and capable within the expected variations of inputs (application, manufacturing, transport and storage conditions).

3.1.29 Robustness Target Value

Target of the robustness validation process.

3.1.30 Robustness Validation

The process to demonstrate the robustness of a device under a defined mission profile.

3.1.31 Safe Operating Area

The process, product, and environmental characteristics within whose limits in extremes the component is expected to operate to maintain functionality and reliability (distinguish from SOA for power transistors).

3.1.32 Semiconductor Component

Synonym for solid-state component.

3.1.33 Solid-State Component

A solid-state device that is a constituent part of a higher order assembly.

NOTE: Examples of solid-state components include DRAMs as parts of memory modules and microprocessors as parts of motherboards.

3.1.34 Solid-State Device

An electronic device whose operation depends on the properties of the integral solid semiconductor materials.

NOTE 1: Examples of solid-state devices include transistors, thyristors, transient voltage suppressors, semiconductor pressure sensors, integrated circuits, modules consisting mainly of integrated circuits such as multichips and hybrids, and memory modules such as DIMMs and SIMMs.

NOTE 2: Electromechanical devices, e.g., solenoids, breakers, wire relays, are not considered to be solid-state devices.

3.1.35 Test Vehicle

Device used for evaluating a specific failure mechanism.

3.1.36 Use Condition

Operating or environmental condition during the use time of a device.

3.1.37 Use Time

Time the product is used in the field.

3.2 Abbreviations

AEC	Automotive Electronics Council
APQP	Advanced Product Quality Planning
ASIC	Application-Specific IC
DFMEA	Design Failure Mode and Effects Analysis
DOE	Design of Experiments
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EM	Electro Migration
EOS	Electrical Overstress
FLL	Frequency Locked Loop
FMEA	Failure Mode and Effects Analysis
IC	Integrated Circuit
JSAE	Society of Automotive Engineers of Japan
OEM	Original Equipment Manufacturer (e.g., car makers are called OEMs)
PAT	Part Average Testing
PFA	Physical Failure Analysis
PFMEA	Process Failure Mode and Effects Analysis
PLL	Phase-Locked Loop
POR	Process of Record
RIF	Robustness Indicator Figure
SAE	Society of Automotive Engineers
SBA	Statistical Bin Analysis
SOA	safe operating area
TC	Temperature Cycling
TDDB	Time-Dependent Dielectric Breakdown
TTF	Time to Failure
ZVEI	Zentralverband Elektrotechnik- und Elektronikindustrie e.V. (German Electrical and Electronic Manufacturers´ Association)

3.3 Definition of Robustness Validation

Robustness Validation is a process by which to demonstrate the robustness of a semiconductor component under a defined mission profile. Robustness Validation represents an approach to qualification and validation that is based on knowledge of failure mechanisms and relates to specific Mission Profiles. The knowledge gained by applying this approach leads to improvement that extends beyond the component and its manufacturing process under consideration. RV contains great potential for re-use, which contributes in its entirety to a significant increase in quality and reliability, time to market and reduction of costs. Last but not least, this will result in improvement of the competitiveness of all involved participants from the value adding chain.

A mission profile defines the conditions of use for the component in the intended application (see section 5). The mission profile establishes the basis for the Robustness Validation approach, providing necessary additional information that is not described in the datasheet. Experience shows that a simple passing on of specifications down the supply chain is inadequate for and incapable of capturing the necessary information. Rather, an interactive process including the entire value chain is needed to achieve a common understanding of and a mutual agreement on the requirements, which is a key factor for success of a project. This interactive process has to be started in the early concept and definition phase of the project. Cross-functional and inter-company communication across the entire value chain shall, therefore, be established as good practice.

TABLE 3.1 - ILLUSTRATES THE MEANING OF ROBUSTNESS VALIDATION BY CONTRASTING POSITIVE (IS) AND NEGATIVE (IS NOT) STATEMENTS

Robustness Validation IS	**Robustness Validation IS NOT**
A methodology	A regulation or specification
A test to failure process or end-of-life process	A test to pass/limit process
Validation of “fit for use”	Validation of “fit to standard”
An iterative process	A one off process
A process to gain knowledge of the failure mechanisms of a semiconductor component	A process to gain knowledge of where the part is functional
A measurement of product lifetime	A go/no go (attribute) measurement

4. ROBUSTNESS VALIDATION BASICS

4.1 Robustness Validation Summary

Robustness is the capability of functioning correctly or not failing under varying application and production conditions. Robustness Validation relies heavily on expertise and knowledge, and, therefore, requires detailed explanation and intensive communication among the specialists of the participants along the entire value adding chain.

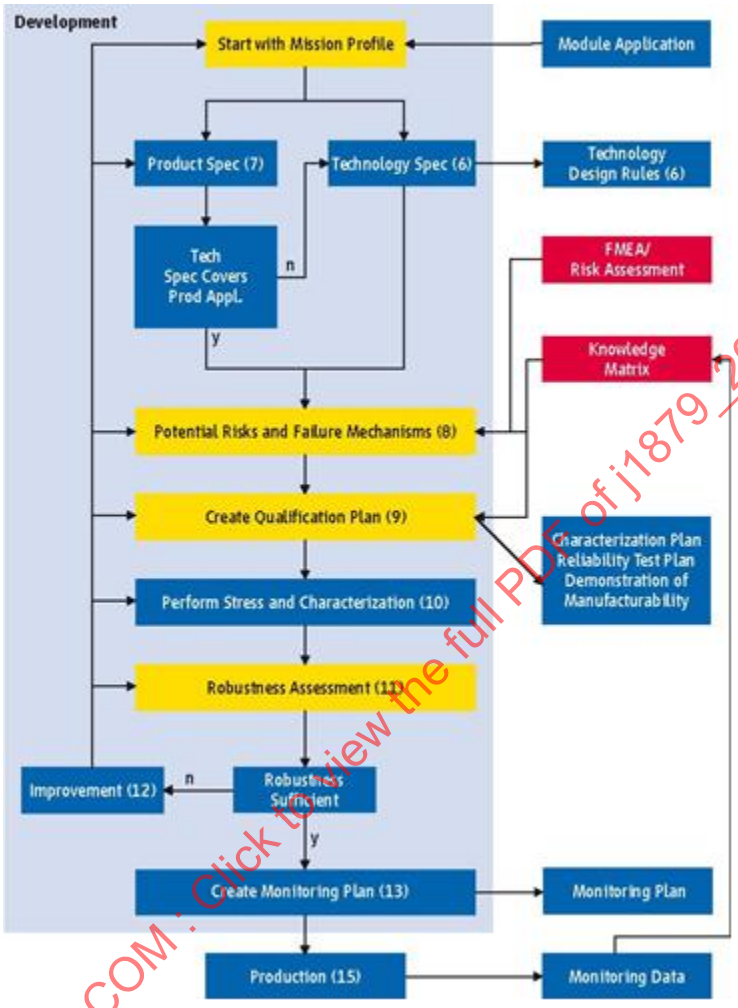
This methodology is based on three key components:

- Knowledge of the conditions of use (mission profile, see section 5)
- Knowledge of the failure mechanisms and failure modes and the possible interactions between different failure mechanisms
- Knowledge of acceleration models for the failure mechanisms needed to define and assess accelerated tests.

Robustness Validation is a knowledge-based approach [1,7,8] utilizing stress tests that are defined to address dedicated failure mechanisms using suitable test vehicles (e.g., wafer test structures, packaged parts) and specific stress conditions. If accurately applied this approach results in a product being qualified as “fit for use”, and not “fit for standard” only.

4.2 Robustness Validation Flow

The Robustness Validation flow (Figure 4.1) is part of the development process. It starts with the transfer of the mission profile from the module level to the level of the semiconductor component. For details of this transfer, see Section 5. The process ends with release for mass production and definition of the related monitoring plan.



The numbers in the figure refer to sections of this document.

FIGURE 4.1 - RV QUALIFICATION PROCESS FLOW

4.3 Robustness Diagrams

Results of Robustness Validation can be represented by the use of Robustness Diagrams.

The Commodity Component Robustness Diagram, shown in figure 4.2, represents the first use of a robustness diagram, and is initiated at the conclusion of the finalization of the Mission Profile. At this point, the Semiconductor Component Supplier investigates whether the mission profile requirement can be achieved by using the relevant commodity device.

Figure 4.2 provides such a pictorial representation for two parameters, A and B, which have a certain relationship, such as voltage and temperature. Many parameters may be simple enough to plot one-dimensionally. The red box represents the area of the application's specification, which the commodity component must meet or exceed. The light blue area represents the commodity components actual performance. The Robustness Margin is the distance between any point of application specification and the point of failure of the commodity component, taking into account all variations of the product and the application's environment. The failure could result in different failure modes X, Y, Z, depending on the values of the parameters A and B. A robust component is a component that is able to maintain all the required characteristics under the conditions of use over the lifecycle without degradation to out-of spec-values.

The Commodity Component Robustness Diagram should be reviewed with the customer to demonstrate the actual robustness of the component when developing the application FMEA.

The Application-Specific Component Robustness Diagram, shown in figure 4.3, represents the second use of a robustness diagram and is initiated at the conclusion of the Robustness Validation Stress Test. At this point, the Component Supplier demonstrates to his customer the robustness of the semiconductor component to exceed the application specification requirement.

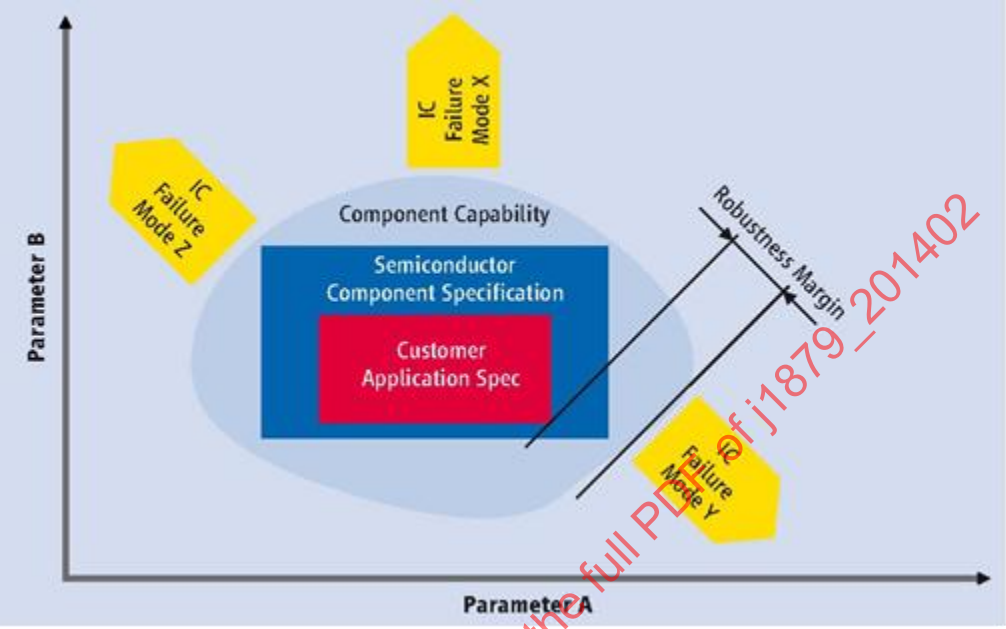


FIGURE 4.2 - ROBUSTNESS DIAGRAM FOR A COMMODITY SEMICONDUCTOR COMPONENT

The IC specification for parameters A and B can be represented by a box (in blue) that displays the minimum and maximum allowed values. Naturally, the range of parameter values for a certain application must lie within this box. However, the specification limit does not imply that the product will fail at this point. Robustness Validation identifies the point of failure for the values of (A, B). The line connecting all points of failure gives the component capability as shown by the light blue area. When any point (Ai, Bj) lies outside the component capability a failure criterion related to A, B or both parameters is violated and the semiconductor component fails. The type of failure mechanism that causes the failure depends on the parameter values and can vary along this component capability curve. Examples for parameters A and B are given in Table 4.2.

TABLE 4.2 - EXAMPLES OF PARAMETERS OF A TWO-DIMENSIONAL ROBUSTNESS DIAGRAM

Parameter A	**Parameter B**
Lifetime	gate oxide area
Lifetime	supply voltage
Maximum current density	junction temperature (max)
Lifetime	number of temperature cycles
Supply voltage	ambient temperature (min)
Number of temperature cycles	temperature range of cycles (Tmax – Tmin)
Number of critical vias	lifetime

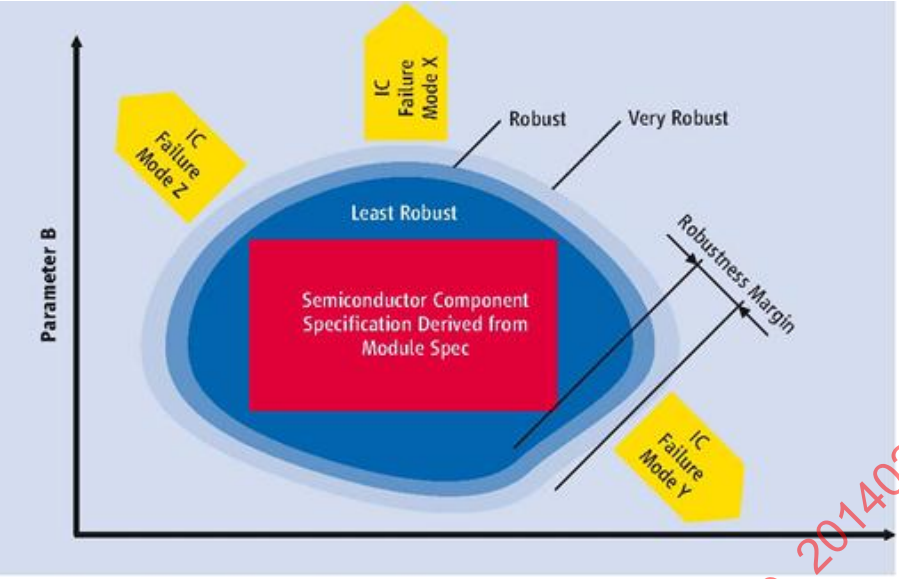


FIGURE 4.3 - APPLICATION-SPECIFIC COMPONENT ROBUSTNESS DIAGRAM.

4.4 Difference between Robustness Validation Approach and Stress Test Driven Qualification Standards

The stresses address multiple failure mechanisms and the test itself being considered pass when NO stress relevant failure occurs. Particular business fields usually require specific stress recipes, prescribed by standards specific to each of them, promoting in the most cases single failures with extrinsic defect nature. At the end these are almost neither systematic, nor relevant for the real application, and only very few intrinsic defects being triggered with relevance to the actual service life of the component. Investigations of the failures triggered by these generic tests usually require substantial effort on failure analysis and to yields almost in root cause information with less or no importance for component's actual service life. Both, effectiveness and efficiency of the stress test driven qualification may be therefore questionable.

On the other hand, the Robustness Validation approach requires the institution of wear out studies on particularly chosen tests promoting specific intrinsic failure modes and provides significant amounts of failure mechanism specific information. Detailed studies on the accordingly triggered failure mechanisms and activation energies will successfully yield in accumulation of valuable knowledge on relevant failures. This represents in consequence the basis for the Robustness Assessment and supports the calculation of the actual Robustness Margin relevant to the component application specific Mission Profile.

Thus, all the accumulated knowledge generated through testing, requested by Robustness Validation, represents is added value and the owning organization being invited to re-use it as often as requested.

In stress-based standards, all tests have fixed stress conditions over a predefined period of time (5). Only a few of the stress tests really focus on single failure mechanisms. The sample sizes are selected as a compromise between failure mechanism detection and the economies of testing and material sets. Stress time is typically chosen to address the anticipated design life of the part based on acceleration models for temperature, voltage, and humidity using mean acceleration factors. As an example, temperature acceleration is typically addressed by "average" activation energy of 0.7 eV, while the spectrum of failure mechanisms ranges from -0.2 eV to 3.3 eV. Depending on the dominating failure mechanism, the use of average values for Ea could result in misleading interpretations of stress test results. The information gleaned from these tests, while comforting when detecting zero defects, may be misleading to the customer. This is caused by the fact, that if no failures are generated:

- The actual robustness of the product being NOT known
- Acceleration factors are NOT measured
- There is no proof that the intended failure mechanisms have been triggered
- The dominant failure mechanism may not be sufficiently accelerated to demonstrate the lifetime requirements.

In the past, this approach helped the customer to compare products from different suppliers and to generate a large database of stress test results performed under identical conditions. As the robustness was not known, the quality, reliability and robustness margins could not be improved effectively, or may even have been unintentionally reduced. Some examples for which traditional stress-test methodologies have been unable to detect subsequent field issues are described in section 15.1.

Development activity is now required to generate a failure mechanism risk assessment and a stress methodology that is able to characterize the failure mechanisms.

Failure Mechanism

Reliability physics differentiates between intrinsic and extrinsic failure mechanisms. The intrinsic failures can be characterized by a small sample of test devices stressed to failure, because they can be considered as physical properties of the materials used.

Extrinsic failures, on the other hand, are random in nature and a large sample size is needed to characterize the critical part of the distribution.

Defect density related failures are typical examples for the last group. Therefore, the sample size must be chosen depending on the type of failure to be addressed by a specific test and the failure rate target to be demonstrated. Extrinsic failures are mainly dominated by manufacturing performance issues and not by the product itself. Therefore, in most of the cases, a complex component like an IC does not necessarily the best vehicle to characterize or measure extrinsic kinds of failures.

On the other hand it is the main task of the IC design to ensure the expected semiconductor robustness by addressing all known intrinsic failure mechanisms and where ever possible the particular manufacturing process disturbances, too, through the accurate application of accordingly developed and engineered design rules and simulation tools integrated in the design flow.

Intrinsic failure	**Extrinsic failure**
Related to the inherent material properties or design	Related to process induced deviations
Systematic	Random
Wearout	Early life failures
Small sample sizes sufficient	Large sample sizes needed

Acceptance criteria

Acceptance criteria of stress-test-driven approaches are typically “test to pass”, which means that the value of the qualification statement is completely dependent on the validity of the model parameters, because quality and the reliability are not really measured. Therefore, the robustness of the product is actually not known after performing this kind of qualification. The result evaluation being of qualitative nature, as the relationship between the applied stress during the stress-test-driven qualification conditions and lifetime at conditions of use are usually not established. The sensitivity of stress-test-driven methods with respect to new or changed materials or technologies being insufficient to demonstrate robustness of a component in the harsh automotive environment.

5. MISSION PROFILE/VEHICLE REQUIREMENTS

As mentioned in the previous section, the knowledge on the actual conditions of use in the overall system of the semiconductor device under investigation represents one of the key components of Robustness Validation. The Robustness Validation process for any relevant component shall start always with the generation of the Mission Profile based on its actual conditions of use in the environment of the current, and next higher level of the component hierarchy. The supplier of the semiconductor component will develop a set of profile assumptions based on market research and/or interactions with customers to capture the majority of user application scenarios. The generation process of the Mission Profile for the component in question represents a detailed, back and forward oriented communication process across the entire value adding chain on each detail of the actual Conditions of Use in the chosen application. The primary and

overarching objective is to ensure the requested/expected quality and reliability over the entire service life of the final product of the OEM. Therefore the BEST known PRACTICE to mutually conclude in good faith for the actual realization on the best technical, reliable and cost saving trade off shall be established in order to ensure competitiveness and the necessary margin to each of the involved partners.

The ideal flow for the generation of these conditions of use is illustrated in Figure 5.1. Starting from the mission profile for the vehicle (such as a car or truck), the corresponding high-level requirements are defined. These requirements are then transferred from the different system levels, module level, and electronic control unit to the level of the semiconductor component (see Figure 5.1).

As mentioned before this shall not represent a one-direction process along the chain, but rather an interactive, iterative agile communication, up and down the entire supply chain, as specification development proceeds. Thereby the requirements become step by step more clear and shall be finally and mutually concluded by all involved parties at the point of freezing of the specification. This is still valid for the mission profile, too.

Examples of the contents of a mission profile on ECU level can be found in the paper "Automotive Application Questionnaire for Electronic Control Units and Sensors", published by ZVEI (9).

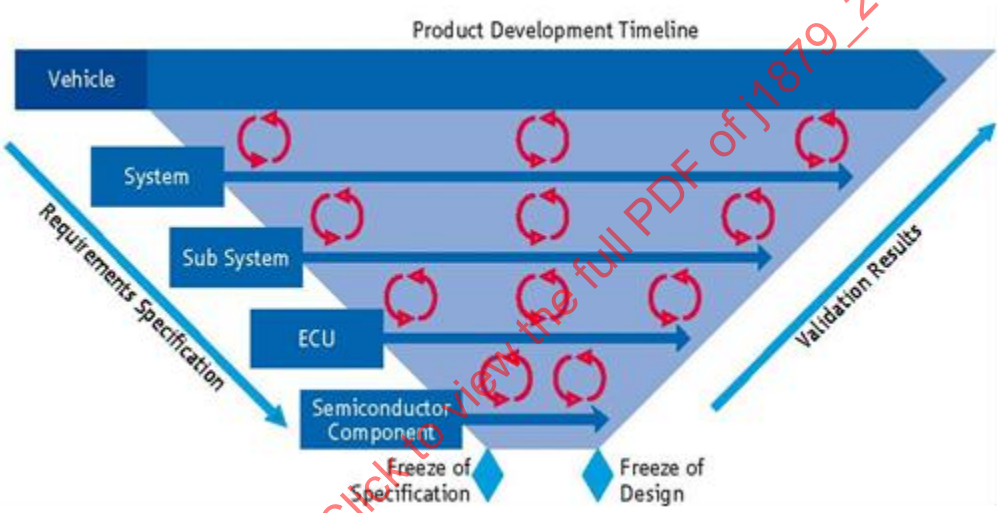


FIGURE 5.1 - PRODUCT DEVELOPMENT PROCESS

The mission profile represents the collection of all relevant environmental load/stress and conditions of use to which a component will be exposed during its full life cycle.

Life cycle is defined as the time period between the completion of the manufacturing process of the semiconductor component and the end of life of the vehicle.

The mission profile includes:

- Transport
- Storage
- Processing
- Operations in the intended application

Each of the profile items listed above can occur more than once. It is not state-of-the-art methodology to replace field application conditions by specific stress conditions. A stress test plan cannot replace the mission profile. A specific example of lifetime prediction that could be made based on mission profile is shown in reference 13.

Commodity Products vs. ASICs

In the case of commodity products, these mission profiles are usually defined without a specific user (as in the case of an ASIC), based on the intended customer base and applications. This case is similar to the case of an ASIC; the difference being that the input does not come directly from the customer but instead from internal sources (such as marketing and product definition). The definition of mission profiles for commodity products requires information and experience by the semiconductor supplier for certain applications. Contents of the mission profile shall be documented for communication to users.

Conditions of Use

The conditions of use are affected by various parameters, such as service life or mounting location. The following section provides an overview of the conditions of use and the corresponding requirements.

In the same way, a new evaluation is required if the conditions of use change for a current component; for instance, if this component shall be used in a new application.

In the following text, aspects of the mission profile are discussed in more detail.

Vehicle Service Life

The most general data concerns the vehicle service life. This comprises information on

- **Service Lifetime**

The total lifetime of the car

- **Mileage**

The total number of miles/kilometers that the car is assumed to be driven during its service life

- **Engine On Time**

The amount of time that the engine and component is switched on (key-on time) and operational during the service lifetime

- **Engine Off Time**

The amount of time that the engine is switched off while several applications are running (such as the radio on)

- **Non-operating time**

The amount of time remaining by subtracting engine-on and engine-off time from the total service lifetime

An example of this kind of data is given in Table 5.1 below.

TABLE 5.1 - EXAMPLE OF OEM VEHICLE MISSION PROFILE PARAMETERS – (HIGH-LEVEL)

Service Lifetime	Mileage	Engine On Time	Engine Off Time	Non-operating Time	Engine On/Off Cycles
15 years	600,000 km	12,000 h	3,000 h	116,400 h	50k (w/o start-stop) > 300 k (w start-stop

NOTE: There are applications that operate continuously during, non-operating" time (such as, theft protection, alarm system)

Environmental Conditions and Stress/Load Factors

The environmental conditions can be classified into four main categories as listed below:

Thermal Conditions

- Seasonal/daily variation of outside temperature and extremes
- Ambient temperature inside ECU
- Junction temperature

Electrical Conditions

- Voltage
- Current
- Energy (transients)
- Electric field
- Magnetic field

Mechanical Conditions

- Vibration
- Shock
- External load, such as pressure or tensile forces

Other Conditions

- Chemical reactions
- Humidity
- Radiation
- Electromagnetic radiation
- Particle radiation

NOTE: All load factors can be static or dynamic and can have spatial gradients that must be taken into account.

Thermal Conditions

The various levels of component integration require a clear understanding and definition of the meaning of the temperature under consideration. Figure 5.2 indicates the locations of different possible points for temperature measurement for different levels of integration.

The temperature measurement locations at the points defined in the Figure 5.2 can be used to describe the thermal conditions in the ECU and the semiconductor components. The temperatures are defined as follows:

$T_{\text{Vehicle Mounting Location Ambient:}}$

Temperature at 1 cm distance from the ECU package.

$T_{ECU\ Package}$:

Temperature at the ECU package.

$T_{ECU\ Ambient}$:

Temperature of the free air inside the ECU.

$T_{ECU\ PCB}$:

Temperature on the PC board

$T_{Comp.Case}$:

Temperature at the component case surface.

$T_{Comp.Pins}$:

Temperature at the component pins.

$T_{Junction}$:

Junction temperature of the semiconductor component (or substrate).

Thermal conditions include information about these temperatures.

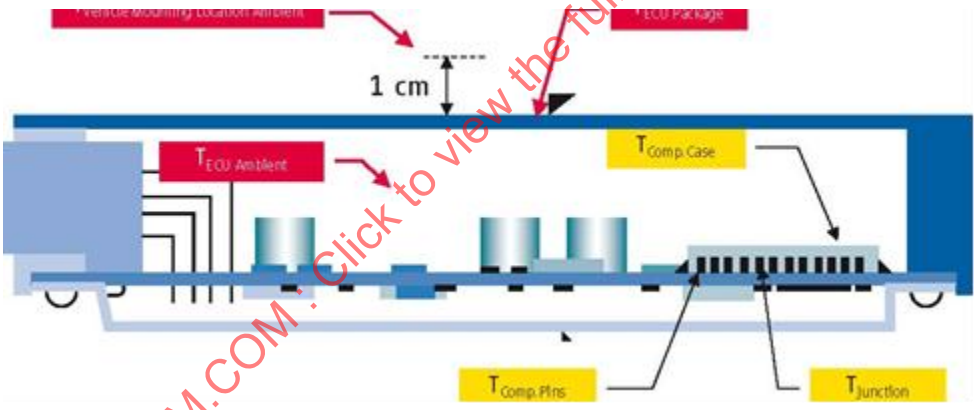


FIGURE 5.2 - MEASUREMENT POINTS AND TEMPERATURES FOR TEMPERATURE CLASSIFICATION WITHIN AN ECU MODULE BOX

Actual component temperature depends not only on the outside temperature, but is heavily dependent on the way of mounting (such as proximity to power devices) and the way of cooling (for example, air flow, heat sinks, etc.). Electrical operation of the device itself leads to an additional active heating of the device, which must be taken into account.

Temperature variation results in thermo mechanical stress on the component. These variations are caused by several factors, such as outside temperature variation and drive conditions. Information about the outside temperature is essential to evaluate thermal conditions for cold starts. Information about electrical operation conditions is needed for operating temperatures. The relevant temperature is dependent on the element and the failure mechanism under consideration.

Electrical Conditions

Operation of the semiconductor component requires subjecting it to electrical loads. These loads are voltages (resulting internally in electric fields) and currents. The parameters are either essentially static (such as supply voltages) or dynamic (such as switching conditions) or a combination of both. Several operation modes may need to be considered, such as engine on/off conditions. Special conditions, such as jump-start and transients, must also be defined if they are relevant for the component. For certain semiconductor components, such as Hall sensors, magnetic fields also must be specified.

Mechanical Conditions

External mechanical loads originate from vibration and shock. The possible effects of vibration depend strongly on the way in which the semiconductor component is mounted. Mechanical fatigue of bonding wires or bonding pads, for instance, could be caused by vibrations at the resonance frequency of hermetically sealed devices, but also structural changes, fractures and loosening of connections could be caused and result in opens, shorts, contact problems or noise. As well as vibration, mechanical shock may also be an influencing factor. These failure mechanisms result in the same failures as vibration but are different from the ones stimulated by mechanical stress due to temperature cycling [14].

For specific components, such as sensors, mechanical loads - such as pressure - are inherent in their intended use.

Other Conditions

Other factors include chemical environments. For instance, components may be exposed to corrosive substances that lead to material degradation.

Humidity, especially in combination with temperature, is a very important environmental factor. The profiles are typically site dependant; for example, the humidity in the US ranges from 93% RH and 37°C in August in Orlando down to 13% RH and 47°C in June in Tucson. Humidity is not only involved in corrosive reactions, but has several other detrimental effects such as degradation of adhesion or hygroscopic swelling resulting in mechanical stress. Humidity also influences other material parameters.

Radiation is another environmental factor that bears on the operation and reliability of the semiconductor component. Electromagnetic and particle radiation are two types. The widely differing effects caused by these types of radiation depend also on the kind of device (for example, logic or memory).

General Remarks on Environmental Conditions

Obtaining a comprehensive definition of environmental stress factors is often very difficult, and requires close communication with all parties involved in the supply chain, the more as conditions may change during the course of development (see also Figure 5.1).

Care must be taken to gather as much information as possible, because lack of such information often results in simplistic worst case assumptions. The consequences of such worst-case assumptions may be over-design of the product or selection of a product that is more expensive than others that serve the same need.

6. TECHNOLOGY DEVELOPMENT

Technology Development is the activity that creates a process flow and design rules; in most cases, this is in combination with a cell library. Details are described in section 3 (Process) of the Robustness Validation Manual. The input for this process is created from the mission profile of the products or generic applications, which are planned to be produced with that technology. It is documented in the Technology Specification. A basic part of the qualification of a technology is the characterization of its variability.

To improve the time to market, some new technology development uses a new product as test vehicle. In this case, both qualifications are performed in parallel. A multidisciplinary team approach shall be used to link the two parallel development flows and to check their progress. Risk management at the design and technology levels shall lead the qualification process.

The design rules are defined based on process line capability, elementary device simulations, reliability evaluations, and historical experience. The design rules must be validated by characterization and reliability testing of library elements or specifically designed test structures. Worst case and marginal structures should be considered as well as process variations. The results of these validations are part of the robustness validation result for each product manufactured on the evaluated technology. The same generic validation procedure should be used for technology levels as for products. Suggestions for design strategies related to identified potential failure mechanisms should be extracted from the Knowledge Matrix (see section 16).

Technology characterization and wafer level reliability results measure the performance for each failure mechanism (see also section 14). The technology characterization and wafer level reliability also allow validation and updates of the simulation models. Simulations, preliminary test vehicle characterizations, and preliminary reliability results allow validation of the design strategy. During the pre-production phase, product reliability and characterization shall specially focus on the risks identified by risk assessments (FMEA) during product and technology developments. Data collection and analysis validate the process ability of the technology.

Prior to technology development projects, the reliability knowledge must be developed in reliability methodology projects. These projects should focus on:

- New materials (such as metal gates)
- New application areas
- New process recipes
- New transistor designs (such as FinFet)
- New device elements (such as solenoids).

Deliverables of methodology projects could be:

- Physical degradation models
- Phenomenological models in cases where the degradation physics is not known
- Model parameters for new materials or technologies
- Spectrum of failure mechanisms for new materials and technologies

After qualification has been achieved, the development phase ends with the readiness for high volume production. Major deliverables at this point in time are:

- Fully documented POR
- Evaluated monitoring plan (see section 13)
- Evaluated control plan
- SPC operational, including evaluated control limits
- Process and Product FMEA
- Evaluated and qualified design library

7. PRODUCT DEVELOPMENT

With the exception of pilot products for development of new technologies, products are usually developed using already qualified technologies and libraries. Re-use of qualified elements shall be extensively encouraged. Previous production data concerning the technology to be used, including production reject analysis, shall be inserted in the Knowledge Matrix. Risk assessment should be focused on differences between new product and products already in production.

The development flow starts with a planning phase in which detailed plans are generated and validated, including the necessary resources. Experiences from previous product developments should be taken into account.

Validated design rules, libraries, and simulation models should be singled out. Suggestions for design solutions related to identified potential failure mechanisms should be extracted from the Knowledge Matrix.

Design reviews ensure that the design meets the requirements in an effort to catch errors before they become defects in the design. Simulations, preliminary test vehicle characterization, and preliminary reliability results such as pre-qualification data allow validation of the design concept. Risk and robustness assessment shall be regularly reviewed taking these results into account. More rigorously accelerated stress testing can be used to find the “weakest links” in early development phase. During the pre-production phase, product reliability and characterization shall specially focus on risks identified by risk assessments (FMEA) during product development.

Finally, the robustness assessment shall be done for each failure mechanism. Adequate test, detection, screening, and monitoring strategies should be implemented in line with the final robustness assessment, before mass production.

If the measured robustness is below expectation, there are several possible reactions (see section 12).

The results of the characterization are used to finalize the data sheet and set up the testing required, assuring that all devices produced comply with the functional requirements established for the application. It should be noted that the characterization activities, as a whole or in part, might go through various iterations before they reach the final stage. The number of iterations depends on the device maturity and the findings from bench testing and especially application testing by the user.

From lessons learned and best practices, it is believed that joint user-supplier emphasis on several key development areas will help achieve best application performance. It is therefore expected that extended development tasks will be a normal part of a supplier’s process and be defined and executed according to their internal processes. Those key areas are defined below.

8. POTENTIAL RISKS AND FAILURE MECHANISMS

The mission profile of an electronic component and the manufacturing technology used constitutes the basis for identification of potential risks to fail in the application together with the potential failure mechanisms. The decision base and the result of this risk assessment should be documented for further reporting. The Knowledge Matrix provides a database to support this risk assessment process.

8.1 The Knowledge Matrix

The Knowledge Matrix is a publicly accessible database containing data on the current state of knowledge of failure mechanisms. Extended versions could exist based on company specific data; some of this data may be confidential.

Weblink to the Knowledge Matrix: The Knowledge Matrix can be found on the website at http://www.sae.org/standardsdev/robustnessvalidation/km.htm Or http://www.zvei.org/fachverbaende/electronic_components_and_systems/alias/device_level/knowledge_matrix_sc/

The application of Robustness Validation and the interpretation of the results require knowledge of the basic failure mechanisms. The root causes of these failure mechanisms and effects on the electronic component must be known to relate the failure mechanisms to the product performance and its conditions of use. The knowledge matrix is used to identify potential risks and to generate a qualification plan based on the mission profile.

In this database, every failure mechanism is described with the following information:

- Name of the failure mechanism
- Typical cause of the failure mechanism
- Typical effect of the failure mechanism (considered at the product level of the electronic component)
- Material(s) affected by the failure mechanism
- The method to detect the failure

- The parameter to characterize the failure mechanism
- Characteristics of the product and application known to calculate reliability figures
- Design of a structure to characterize the failure mechanism
- Methods to prevent the failure mechanism by design or preventive methods during fabrication
- Optimum stress method to stimulate the failure mechanism
- Acceleration model for the failure mechanism
- Reference describing the physical degradation model of the failure mechanism

8.2 How to Use the Knowledge Matrix

To prepare the qualification plan, the potential risk and failure mechanisms must be identified. Selecting valid fail mechanisms from the Knowledge Matrix requires a review of the entire Knowledge Matrix based on previous qualification efforts and anything new for the part to be considered. The cause and the failure column could contribute some ideas that could help to make this list of failure mechanisms as complete as possible. To check whether requirements are affected, the effect column, which gives information about the effect at the product level, should be taken into account. The application column delivers additional information about whether certain failure mechanisms are relevant because they are accelerated by certain environmental conditions, like temperature or voltage. Before the failure mechanism is chosen for the risk list, it should be determined if it is related to only a specific material.

For the project at hand, make a list of applicable known potential failure mechanisms using the matrices for each semiconductor group:

- Technology/process (supported by PFMEA)
- Device (supported by DFMEA)
- Assembly/package (supported by DFMEA)
- Application/environment

To complete the list with additional potential failures, check the following topics:

What is new (compared to the most similar process available, for instance)?

Technology/process

- Process step (etch, deposition, etc.)
- Material

Device

- New circuit configuration
- New voltage/current levels
- New element (such as a capacitor)

Design

- New structure
- New layout
- Feature size (for example, from 90 to 65 nm)

Specification

- New parameters (AC, DC, timing)
- Changed parameters (limits, extremes)

Application environment

- Determine the new environmental stress for the application
- Determine how each stress/combination of stresses affects the device

For each additional failure mechanism determine

- The characteristics/elements in accordance with the various categories
- As a minimum: the reliability test that would stimulate/precipitate the failure mechanism
- Determine if it is possible to accelerate the additional failure mechanism without introducing new failure mechanisms, which would be unexpected under normal use conditions.

The following is an example of how to use the contents of the Knowledge Matrix:

If the supply voltage is defined in the semiconductor component specification, the risk discussion of voltage effects on reliability can be started. The necessary activities are (column headers of Knowledge Matrix in bold)

1. Find the failure mechanism related to the failure cause or Affecting Operating Conditions voltage and select the subsystem chip

No	Sub-System	Material	Failure mechanism	Failure cause	Failure mode	Detection Method	Character of Degrad	Affecting Operting Conditions
37	chip	SiO2	additional charges	mobile ions	Vth shift causing spec violation	weak comp. spec violation	Vth shift after stress	V, T,
44	chip	poly Si NVM	charge loss	SILC ESD	bit flip or retention fails	Vfh Cell	? Vfh	V
74	chip	High k dielectrics	Gate delectric hard BD	surface roughness contamination ESD lattice defects charge trapping local GOX thinning variation of oxide thickness mobile ions dielectric defectivity	leak increase & G short	IG leak	IG leak	A, V, T
51	chip	SiO2<=4nm	GOX hard BD	surface roughness contamination ESD lattice defects charge trapping local GOX thinning variation of oxide thickness mobile ions dielectric defectivity	G short	IG leak	IG leak	A, V, T
52	chip	SiO2<=4nm	GOX hard BD	surface roughness contamination high E-field lattice defects pinholes charge trapping local GOX thinning mobile ions dielectric defectivity ESD	G short	IG leak	IG leak	A, V, T
66	chip	SiO2<=4nm	GOX soft BD	surface roughness contamination high voltage lattice defects charge trapping local GOX thinning variation of oxide thickness mobile ions dielectric defectivity ESD	leak increase	IG leak	IG leak	A, V, T
75	chip	PMOS gate dielectric	hot carrier injection (HCI) field induced injection and trapping of electrons in gate oxide near drain region of device	variation of oxide thickness variation in work function and dopant profile line edge roughness	ID, gm, Vth changes (increase or decrease depending on channel length)	ID subthreshold slope	PMOS IDS vs. VDS vs. VGS charac-terization	V (VDS, VGS); T; f
76	chip	NMOS gate dielectric	hot carrier injection (HCI) field induced injection and trapping of electrons in gate oxide near drain region of device	variation of oxide thickness variation in dopant profile line edge roughness	ID, gm reduction Vth increase	ID subthreshold slope	NMOS IDS vs. VDS vs. VGS charac-terization	V (VDS, VGS); T; f
61	chip	IMD, ILD	IMD/ILD hard BD	contamination, CU-diffusion high E-field charge trapping local oxide thinning mobile ions ESD line edge roughness	G short	IG leak	IG leak	A, V, T
89	chip	Cu, AiCu(Si)	Metal residues causing latent defects	metal scratch, litho defect	increased leakage current	defect inspection	leakage current	V
77	chip	PMOS gate dielectric esp. nitrided oxides	NBTI, charge trapping	process induced or preexisting traps variation of oxide thickness variation in dopant profile surface roughness	increase in absolute value of Vth degradation of mobility	Vfh	PMOS IDS vs. VDS vs. VGS charac-terization	V (VDS, VGS); T; f; duty cycle
93	chip	NMOS gate dielectric; esp. nitrided oxides	PBTI, charge trapping	process induced or pre-existing traps variation of oxide thickness variation in dopant profile surface roughness	Increase in absolute value of Vth, decrease in Id	Vth	NMOS IDS vs. VDS, vs. VGS charac-terization	V (VGS, VGD); T; f, duty cycle

2. One failure mechanism to be taken into account is gate oxide hard breakdown.

3. If the material is thick SiO2 gate oxide soft break down can be ignored.

No	Sub-systen	Material	Failure mechanism	Failure cause	Failure mode	Detection Method	Character of Degrad	Affecting Operting Conditions
52	chip BD	SiO2>4nm	GOX hard	surface roughness contamination high E-field lattice defects pinholes charge trapping local GOX thinning mobile ions dielectric defectivity ESD	G short	IG leak	IG leak	A, V, T

4. The potential effect on IC level is a gate substrate short.

Failure mode
G short

5. The characteristic for detection and characterization is the same: the gate leakage current.

Detection Method	Character of Degrad
IG leak	IG leak

6. The extrapolation from test to product/application level must be done for the voltage, the temperature and the area, which means that temperature and gate-oxide area are the other two limiting factors for gate oxide reliability.

Affecting Operting Conditions
A, V, T

7. The optimum design of the test structure is a transistor array. For this test structure, the failure criterion of the gate leakage current must be specified.

Test Struct for Evaluation
transistor array or capacitor

8. Stress method for qualification is Time-Dependent Dielectric Breakdown (TDDB).

Stress Method
TDDB

9. At this point in time, an overview of all failure modes triggered by TDDB stress can be generated. The sum of all these aspects gives a full picture of the coverage of the failure mechanisms for the qualification plan.

10. For this particular example the physical model describing oxide breakdown is the percolation model and the acceleration model to be used should be the E-model, if gate oxide thickness less than 4nm. For additional details, see references in the Knowledge Matrix. Figure 8.1 illustrates how a cumulative failure distribution measured on a test structure must be transformed to the condition in the semiconductor component.

Ref (Stress Method)	Acceleration Model	Ref (accel model in JEP122F)
JP001	Percolation E-model	5.1.2.1

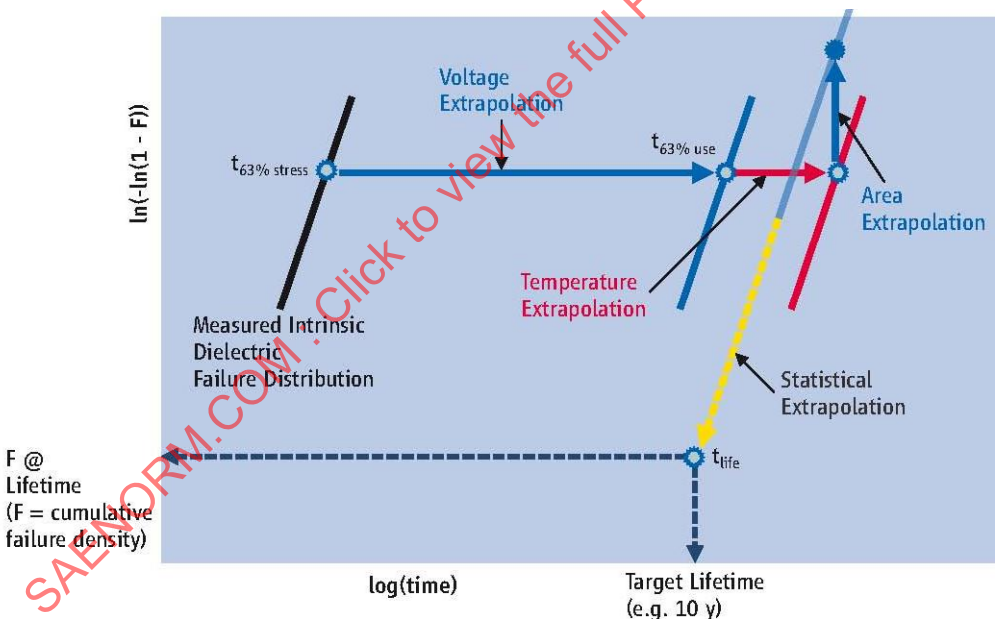


FIGURE 8.1 EXTRAPOLATION OF FAILURE DISTRIBUTION

8.3 Limits of accelerated reliability testing

When creating a stress test plan certain physical and procedural limitations have to be taken into account.

8.3.1 Limited load capacity (stress ability) of devices and test structures

Test structures are used because of their specific properties like

- Sensitivity to a single failure mechanism
- Easy to analyze
- Easy to characterize and measure
- High load capacity (much higher than a normal product)

They are used in qualification tests which are designed to generate degradation under accelerated stress conditions in a very short time. The load one can apply to test structures is physically limited by the maximum value before the failure mechanism changes. Typical examples for these limits are:

- Local heating resulting in material structure changes, diffusion path changes
- Avalanche region of pn junctions for standard voltage acceleration
- Breakdown voltage of dielectrics if degradation is evaluated
- ESD failures if ESD is not the topic of investigation
- Current densities in EM tests of interconnects which generate melting

8.3.2 Library elements

Library elements are also used in stress tests. Their specific properties are

- Basic design elements
- Easy to analyze
- Easy to characterize and measure
- No overstress capability

They are used in qualification tests which are designed to generate parameter degradation under elevated operating conditions in a short time. Their stress capability is limited because

- No ESD protection
- Current density and voltage stress limited by design rules

8.3.3 Electronic components (products)

In some cases the electronic component is best suited for being used in a qualification tests due to the following properties

- Performance according to spec
- Robust under operating conditions
- Protection circuitry

Limits for the application of electronic components are

- T stress limited by mould compound or bonding
- V stress limited by protection circuitry
- I stress limited by voltage regulation
- Failure analysis limited by available resources
- Stress coverage of el function hard to evaluate

8.3.4 Limits of application range of test methods

Stress tests could be restricted to

- Certain technologies
- Certain materials
- Certain parameter ranges

Example Helium Fine Leak Test

- Designed to evaluate hermeticity of MEMS packages
- Perfect for metallic seals
- For polymer sealed packages of no use due to absorption properties of polymers

8.3.5 Limited resources for reliability evaluation

Resources for reliability evaluation are limited because high level experts, test equipment are needed. On the other hand the project schedule limits the available time for these activities. Time when information for production decision has to be available is defined by market, not related to the complexity of the problem. Therefore resources have to be concentrated on the most critical issues and during the early phase of development. Activities which do not generate information have to be avoided. The trade-off between residual risk, costs and time-to-market has to be found for every product

8.3.6 Limited time for implementation of lessons learnt

The number of new materials and process recipes increases with every new technology generation.

With every new material or process

- The criticality of failure mechanisms have to be reviewed. New failure mechanisms are very rare, but what has been totally uncritical in the past can be a major issue in the future.
- The degradation model parameters have to be evaluated and verified.
- The statistical model has to be evaluated and verified.
- Stress test conditions have to be developed
- Analysis technologies have to be developed

The frequency of introducing new technologies stays constant or might increase in the future.

- The time for implementing the results of the new reliability methodology has to be used more efficient to reach the targets.
- The resources have to be focused.

8.3.7 Limited knowledge on models and failure mechanisms

Keep in mind that the qualification statement is statistical in nature:

- Extrapolation from stress to operating conditions
- The qualification statement describes the situation at a certain point in time
- Defects and maverick phenomena on low failure level have to be covered by containment activities

RV performed correctly generates the basic information to achieve PPM levels but qualification cannot demonstrate these levels statistically see also section 9.5. A lot of progress has been made to understand the physics behind the failures, but a continuous effort is needed.

9. CREATION OF THE QUALIFICATION PLAN

Each Qualification Plan consists of three basic elements:

- Characterization plan (section 9.4)
- Reliability test plan (section 9.1)
- Demonstration of manufacturability (section 9.4.1)

9.1 Reliability Test Plan

All failure mechanisms that have been identified as potential risks must be addressed by reliability data. Information already existing from previous investigations or data from the development work could be used to confirm low risk levels (see also section 6). The applicability of generic data must be demonstrated. Some types of input to the Qualification Plan could be extracted from the knowledge database:

- The test structure that could be used for reliability characterization. Circuits, sub circuits, library elements, or the complete semiconductor component should be considered as the appropriate test structure. Criteria such as availability or analyzability should also be taken into account.
- The stress method that could be used to address and accelerate the failure mechanism.

Special attention must be given to the failure rate of the specific test structure. There is no generic rule about the manner in which this number is calculated from the failure rate target of the product because of the potential difference in the failure paretos. If, for example, one failure mechanism dominates the failure rate of the product, the assumption that more than 50% of the product failure rate may be due to this dominant mechanism is reasonable. However, if several failure mechanisms have comparable failure rates, the product failure rate must be distributed among them. For the assessment of reliability, the Qualification Plan shall contain the following information for every stress test:

- Targeted failure mechanism(s), including an explanation of relevance (give rationale if the typical failure mechanisms are rated as irrelevant)
- Acceleration model used
- Vehicle (= test structure): The test structure must be representative of or related to the product design and the application conditions that the product may experience in the field. This may require detailed documentation.
- Stress method
- Stress conditions (parameterization of the stress test): Stress conditions must be optimized with respect to the failure mechanism to be addressed.
- Sample size or number of lots: Qualification shall provide statistically valid data for the demonstration of intrinsic failure mechanisms. Failure rates in the range of ppm at the product level cannot be demonstrated in the qualification phase.
- Parameter for characterization (P) of the test structure
- Method of failure analysis for characterization, if needed
- Fail criteria (P_{fail}) or acceptance criteria
- Readout times or intervals and criteria for the end of test

In certain instances, reliability validation may also require verification at the ECU level. This can only be accomplished by the user of the component and requires agreement and cooperation between the manufacturer of the component and the user.

An example and template that includes these elements in a Qualification Plan is shown in section 17. For every reliability characterization, a target value is needed as a gate to separate the failure case from the expected performance according to its requirement. This target value is applied to the parameter P that is used for characterization of the degradation during stress. In some cases, P_{target} is not directly defined as a requirement. In such cases, the relationship between the requirement and P must be known. The target value could be a lower or upper limit or a range and shall include the relevant tolerances.

The characterization column of the Knowledge Matrix indicates which parameter should be measured during stress to generate the degradation over time. To calculate the lifetime under stress conditions, a fail criterion must be defined that is related to the requirements or the spec values. Examples for degradation parameters are:

- Leakage current for gate oxide related failure mechanisms
- Resistance for electro- and stress migration
- Transistor parameters (such as threshold voltage, drain current or trans conductance)

Acceleration may be limited due to items such as competing failure mechanisms or the intrinsic robustness of the system or design. An insufficient number of failures may occur during economically acceptable test duration (for example, due to physical boundary conditions). There is no generic solution that fits all cases, but potential options are:

- Choose more sensitive failure criteria and correlate the results
- Increase the sample size and stop the test after the first part of the failure distribution has been measured
- When only a portion of the distribution fails, the statistical solution for lognormal distributions is described in JESD 37; for other cases, see, e.g., [15]
- If there is no failure, one could make the following assumptions and estimate the lifetime of the failure mechanism:
- Use a known model and typical parameters (such as for lognormal distribution)
- Assume that the first device under test fails right at the end of stress time

Before performing many expensive and time-consuming qualification tests, it should be determined whether data are already available that demonstrate the robustness of the semiconductor component with respect to a certain failure mechanism. These generic data could have been generated by testing an object different from the one under discussion, but the data may be valid for a group of objects. An object could be a semiconductor component, a package, a wafer – or a package technology. These groups of objects –called qualification families– could consist of wafer technologies or parts of it, assembly technologies or parts of it, packages, or semiconductor components with similar functions, specifications or application conditions. The relevance of the application of generic data must be supported by other documents or data.

A qualification family will be defined by its manufacturing attributes (material, site and processes).

Examples:

- A die family will be defined by its wafer fab attributes
- A package family will be defined by its assembly attributes only

Family definitions, test results, and the applicability of those must be clearly communicated to the customer.

Example for one failure mechanism - electromigration

A certain functionality required by the customer of an electronic component can be achieved only if the product has a certain complexity. The minimum feature size of the technology could be defined from the required complexity. This minimum feature size is associated with a maximum current density in interconnects, which together with a corresponding lifetime and failure rate, is a reliability target for the reliability qualification of the technology. The failure mechanism related to current density is electromigration. The failure criterion is defined by the maximum resistance change tolerated by the design of the product. In this case, the critical parameter for reliability qualification is $\Delta P = \Delta R$. By applying reduced current densities to a design, the target failure rate could be reduced or the lifetime could be prolonged by keeping the failure rate constant.

9.2 Definition of a Qualification Family

9.2.1 Wafer Fab

All semiconductor components using the same technology, process and materials with common major elements (such as 90 nm effective channel length, Cu metallization, intermetal dielectric material, shallow trench isolation), are categorized as one qualification family and are qualified by association when one family member is successfully qualified. Family re-qualification is required when the process or material is changed significantly (major process changes). Typical considerations for wafer fab process descriptions are: design rules, lithography technique, metallization, polysilicon, dielectrics etc.

9.2.2 Assembly Processes

The processes for plastic and hermetic package technologies must be considered and qualified separately. All semiconductor components using the same process and materials, with common major elements (such as biphenyl mold compound, Alloy 42 lead frame material, Pb-free lead plating), are categorized as one qualification family and are qualified by association when one family member is successfully qualified. Family re-qualification is required when the process or material is changed significantly (major process changes). Typical considerations for assembly process description: lead frame, die attach, package material, bonding, external lead finish etc.

9.3 Qualification Envelope

For ASICs, the alignment of requirement with the specification of technology and semiconductor component can be done by direct correlation. For cases in which a broad spectrum of applications must be addressed, an adapted approach for generating the qualification plan must be applied. Taking the worst-case values for each specified characteristic separately is one way to create this envelope (specification X in Figure 9.1). In many cases, however, this procedure leads to overly conservative specification, unnecessarily increasing the cost of development and qualifications. It is advantageous to define the envelope in more detail to generate an efficient solution (specification R). Figure 9.1 illustrates the difference between the two approaches for two spec parameters A and B.

The more efficient approach fulfils the same requirement from Applications 1 and 2 and prevents over-engineering.

In cases where specific applications are not known, it becomes a strategic decision as to how to define the spec area of the semiconductor component and the correspondent qualification envelope. The trade-off between costs, robustness margin, and spec area must be found based on generic market information. In this case, the robustness of the semiconductor component must be measured with respect to this generic specification, so that the robustness for an intended application can be calculated in the process of choosing a semiconductor component for a specific module design. This means, for instance, that the same product could fit into a safety relevant application with lower spec values and high robustness and fit into an uncritical application with a higher spec value and lower robustness margin.

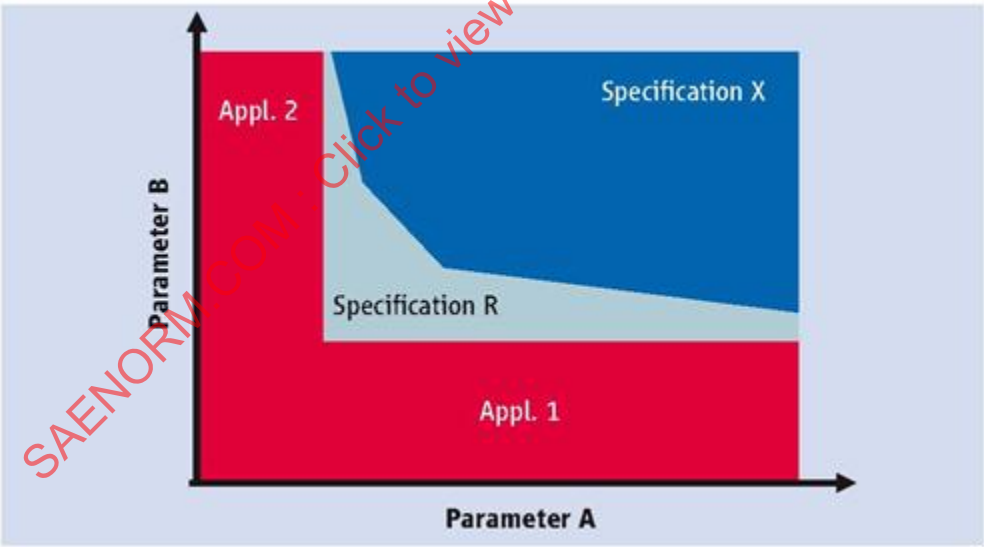


FIGURE 9.1 - SPECIFICATION OPTIONS FOR DIFFERENT APPLICATIONS

9.4 Characterization Plan

The Characterization Plan should include the plan for material and testing to ensure the functionality of the product over all production variations and all temperatures and voltage ranges. Testing should be at both spec limits and beyond (as appropriate) to determine the margins. The plan should include process variability (that is, corner lot details) to show the range of production material. Data should be statistically summarized to show Cpk of each parameter. Any data from previous characterizations is also useful. The purpose of this is to make sure that the design and production are capable of maintaining specified Cpk values for all specified parameters.

NOTE: The user shall not exceed agreed upon specification limits under any circumstances. Characterization beyond specification limits is for information on robustness only. If at any time a part is found to operate, during the application, beyond the agreed upon limits, requires agreement by both parties, especially legal and financial indemnification to the supplier on the part of the user:

9.4.1 Process Characterization

Process variability characterization may take the form of process corner matrix lots containing groups of wafers that have one or more process steps varied by plus or minus several sigma's. If process variations cannot be produced in a dedicated manner, test samples may be selected by using SPC data to identify wafers or test samples near or beyond the limits. The chosen process steps should be known to directly correlate to specific functions or electrical parameters affecting the performance of the device in a given application. The packaged devices from this material can then be assembled into an automotive system to understand which region of the process space yields the best performing devices. This type of characterization should be performed for new supplier semiconductor component designs that have little or no relation to previous designs, the first automotive application of an existing semiconductor component design, or a more demanding automotive application for an existing design. The characterization requirements may be reduced if appropriate data exists from other project(s).

1. Determine relevant failure modes of the semiconductor component that can affect the application

2. Correlate these failure modes with the corresponding process parameters that affect them

3. Determine if there is independence between the failure modes and the corresponding process parameter. If not, a design-of-experiments may need to be performed.

4. Assign statistically significant sample sizes to each process corner split when performing electrical testing.

5. Record variable electrical parameter data over extremes of temperature, voltage, frequency, and/or loading. The variables data for each parametric test should include a summary of mean, standard deviation, minimum, maximum, Cpk, and upper and lower spec limits for each process corner and extreme sampling.

These variability considerations should be done by appropriate simulations of critical sub circuits. Typical characterization plans may include the demonstration of process variability. This may be in the form of a corner lot plan including device parameters (threshold voltage Vt, effective channel length L_{eff}, etc.) to be varied and the expected effect on semiconductor component performance. The yield values shall be assessed with respect to the target yield and potential yield detractors should be used as a starting point for continuous improvement planning.

9.4.2 Device (semiconductor component) Characterization

The characterization conditions depend on the component under consideration. For digital circuits, typical characterization plans may include:

- Min/Max operating parameters – tests that find min/max conditions for supply voltage, bus timing, frequency, etc.
- Margin testing – voltage will be characterized to find the potential fail levels (I/O levels)
- Current level characterization – measure all leakage, Idd, etc. currents to determine margins to the specification
- Power supply current level characterization – measure Idd, and ΔIddg, to determine static test pattern and power supply current margins to the spec.
- Leakage current level characterization – measure all leakage currents. Measuring leakage as a condition of connecting Vcc/GND directly to CMOS gate and determining the spec limit, in order to detect potential defects, helps to improve robustness.
- PLL characterization (stabilization time, lock, jitter)
- Oscillator parametric tests

TABLE 9.1 - REQUIRED SAMPLE SIZE FOR DIFFER ENT FAILURE TARGETS ASSUMING 90% CL

samples	failure (dmp)
24	100000
231	10000
462	5000
2304	1000
4606	500
23027	100
115130	20
230260	10

9.4.3 Production Part Lot Variation Characterization

Production parts from a centered process can be characterized over temperature, voltage, frequency and loading to understand its inherent variance. Devices from specific parametric extremes can then be assembled into a system to observe if the process centering yields weak regions in the process space. This type of characterization can also be used if process corner matrix lot characterization proves to be too ex-pensive or time consuming for the anticipated benefit in yield and performance.

1. Decide on a statistically significant sample size if the entire lot is not to be tested.

2. Record variable electrical parameter data over extremes of temperature, voltage, frequency, and/or loading for each part tested. The variables data for each parametric test may include a summary of mean, standard deviation, minimum, maximum, Cpk, and upper and lower spec limits for each extreme sampling.

3. If attribute data is to be taken, electrical tests over extremes of temperature, voltage, frequency and/or loading may result in Schmoo plots diagramming the functional parameter space within which the part will operate.

9.5 Sample size and basic statistics

Typically sample sizes available for qualification are small compared to the failure target which should be achieved under high volume production of the electronic component. A Zero-Fail @ stress strategy is only able to demonstrate that catastrophic problems are not expected to happen. This can easily be seen in table 9.1 where the number of test devices are listed which are needed to demonstrate a certain failure number with 90% confidence assuming that after the test no failure is detected. To give an example: 0/77 failures at 90% CL demonstrates 30000 dpm failures.

A failure distribution as shown in figure 9.2 with 50 failed devices out of 77 samples could be used for extrapolating down to the ppm target level at a specific stress test time.

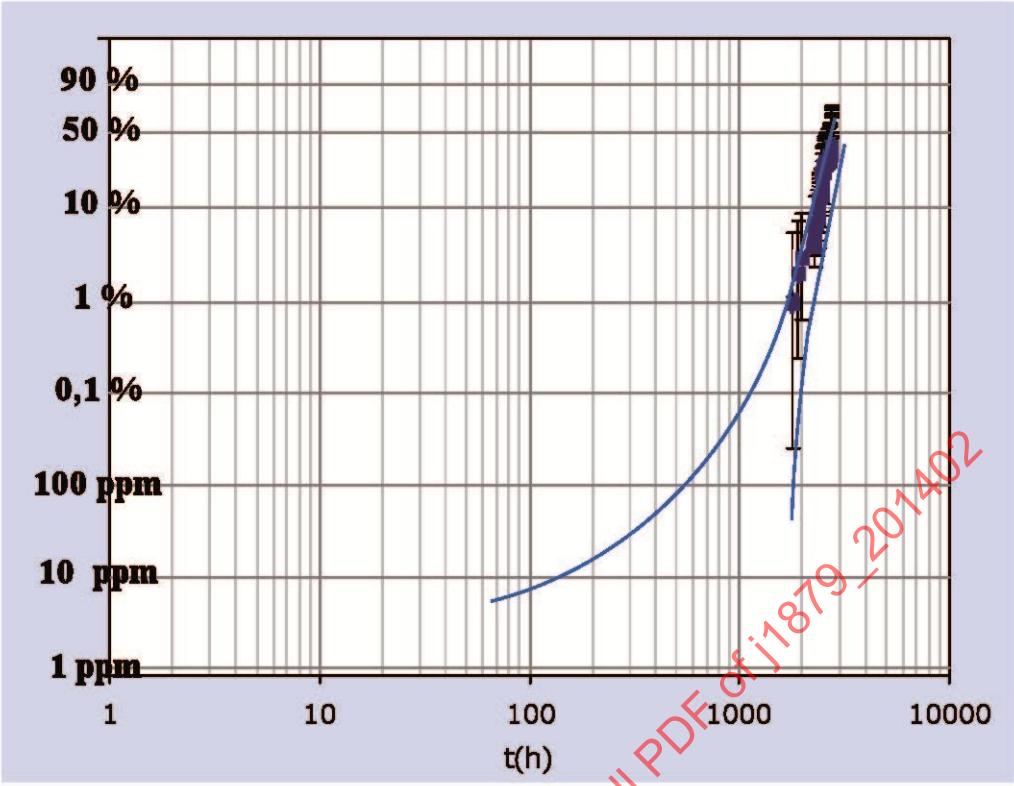


FIGURE 9.2 - EXAMPLE OF A WEIBULL PROBABILITY PLOT FOR 50/77 FAILED DEVICES INCLUDING 90% CONFIDENCE CURVE

Besides the knowledge on the failure mechanism the RV concept generates statistical data, for a Weibull distribution the shape and the scale parameter (t63), to perform more powerful statistical analysis compared to the zero fail approach. Calculation of the 90% CL curve of the extrapolation is also possible.

The RV-Method generates statistics knowledge which could be used for better risk analysis. With known acceleration factor the extrapolation from stress to operating condition could be done.

10. STRESS AND CHARACTERIZATION

The stress tests must be performed according to the requirements specified in the Qualification Plan. The equipment must satisfy the requirements with respect to the stress test parameters as defined in the Qualification Plan, and the tolerances of the parameters must be known. The reference column of the Knowledge Matrix contains a detailed description of the method and how to perform the test.

Characterization data must be completely logged for all readouts. The test at readout must comprise the full program. There must not be a stop-on-first-fail nor must parameter values be substituted by error log values. The latter should only help to identify problems during testing. The parameter values will be needed for further drift/fail analysis. Critical parameters may be monitored continuously during the entire characterization procedure in order to react quickly and in a focused way in case of failures. The measurement frequency must be adapted to the level of acceleration.

NOTE: It is not useful to log parameters not related to the applied stress for all readouts.

The output of the qualification test shall be documented with the parameters listed:

- P = P(t), the change of the parameter over the time of stress if there is a continuous degradation or
- Pi = P(ti), if there are discrete readout intervals, denoted by the subscript i
- Fail distribution (TTF) under stress condition
- Confirmation is needed that the intended failure mechanism has really been activated. Different failures that may occur but are not correlated to the addressed failure mechanism must receive special attention and must be treated separately in the lifetime/risk assessment. Such failure mechanisms may show up as irregularities in the degradation curve or failure distribution, such as bimodality.
- Model used to convert results from stress test to lifetime at use conditions
- Other factors that must be taken into account, such as duty cycle

NOTE: In some cases, only the time to (catastrophic) fail is recorded (example: in many cases, TC leads to catastrophic failures; for example, electrical failure due to cracking, that cannot be observed during degradation, that is the crack initiation and propagation). In such cases, only the time to fail, tf, is available.

Based on this information, the lifetime per failure mechanism can be calculated:

- Lifetime under stress conditions t_{stress}
- Lifetime under use conditions t_{use}

In case of an unexpected behavior, updating the knowledge base must be taken into consideration. In cases where only a comparison is needed, a qualitative evaluation could be used. This procedure requires knowledge from previous Robustness Validations.

11. ROBUSTNESS ASSESSMENT

The robustness assessment must be done separately for each identified failure mechanism using the Knowledge Matrix when the potential risks and failure mechanisms for this qualification were assessed. Failure mechanisms that were not identified but did occur in the qualification will also be assessed for robustness. The robustness assessment is done by compiling a Robustness Diagram and comparing stress test and characterization data to the requirements.

11.1 Lifetime as a Function of Stress Value

During reliability qualification, the reliability characteristic P has been measured over time as a function of the stress value Si (see Figure 11.1).

Examples for such degradation curves could be:

- Resistance degradation at various current densities and temperatures
- Degradation of the 1-level vs. read/write cycles of non-volatile memories
- Degradation of the small signal gain of a common source amplifier at various stress voltages
- Degradation of the output current of a current source at various stress temperatures

Whenever the degradation curve reaches the failure criteria $P_{target}t$, the lifetime tP(Si) corresponding to the stress value Si is determined.

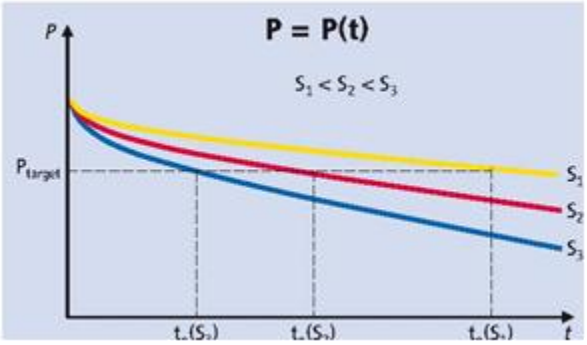


FIGURE 11.1 - RELIABILITY CHARACTERISTIC AS A FUNCTION OF TIME

11.2 Determine Boundary of the Safe Operating Area

The boundary of the safe operating area can be calculated from the stress lifetime values tp(Si) (see Figure 11.2). Stress/time values below the measured curve do not result in a failure; values on and above the curve will result in a failure.

The stress-lifetime curve can be extrapolated to use conditions if the acceleration model is known (see Knowledge Matrix). If the model is not available from the knowledge matrix or relevant standards, one should apply the method described in JESD91A (Method for Developing Acceleration Models for Electronic Component Failure Mechanisms)[2].

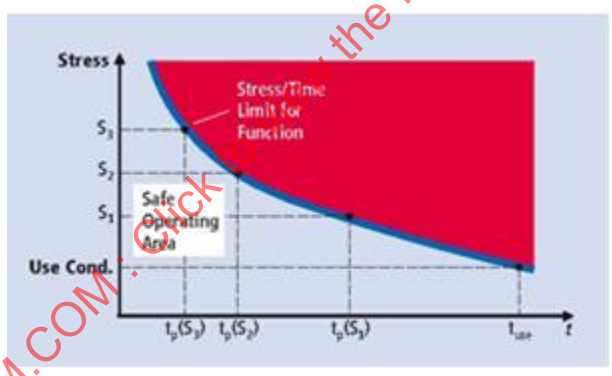


FIGURE 11.2 - SAFE OPERATING AREA

11.3 Determine Robustness Target and Area

The robustness target could be specified in terms of either lifetime or use/stress conditions. Depending on the sensitivity, the robustness target should be specified (see Figure 11.3). Defining the robustness target requires the following steps:

- Define robust lifetime t_{robust} under use conditions
- Define robust condition P_{robust} at target lifetime
- Draw robustness area around the point of use taking into account t_{robust} and P_{robust} (black line in Figure 11.3)

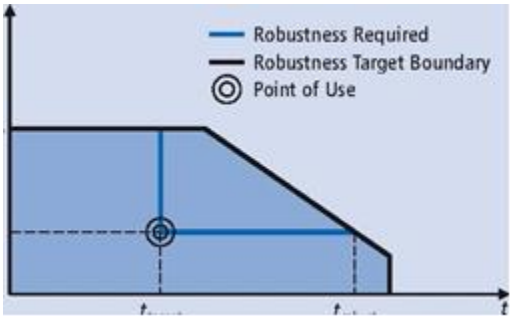


FIGURE 11.3 - ROBUSTNESS TARGET DEFINITION

The robustness area around the point of use is bordered by the robustness limit (P, t). Within the robustness area, the product should be safe against the related failure mechanisms, which means that applying a value P over time t, with (P, t) lying inside the robustness area does not result in a failure. The limit also gives the designer the opportunity to choose the point of use according to different safety requirements.

An example for such a type of robustness target could be the maximum allowed leakage current calculated based on the maximum allowed quiescent current over a use time of ten years of operation. The robustness target could be found by defining the robust value for the leakage current after 10 years of operation and by defining the operation time without violation of the leakage current target. Values between this robustness targets could be found by interpolation.

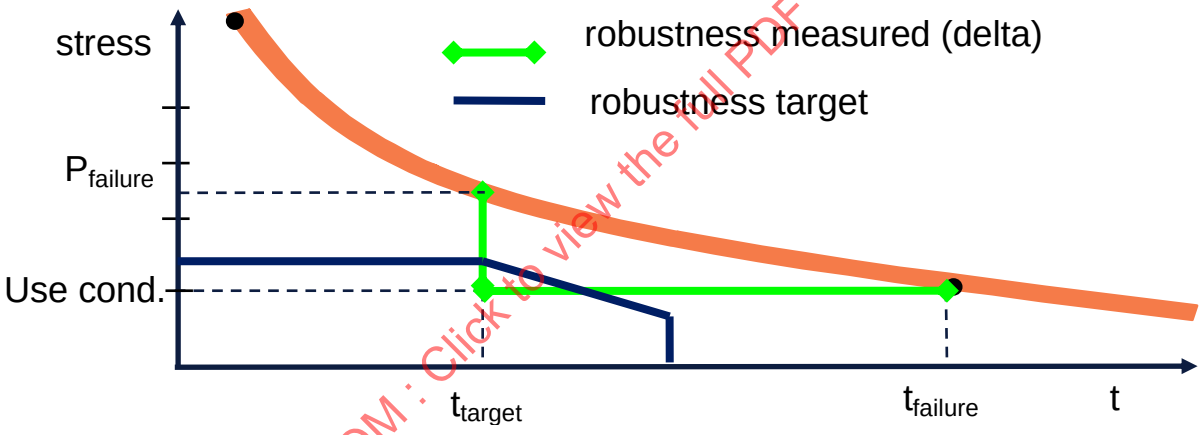


FIGURE 11.4 - ROBUSTNESS EVALUATION

11.4 Determine Robustness Margin

The robustness area is the reference for the robustness comparison (Figure 11.4). The measured data for P = P(t) (brown curve) shall be compared to the robustness target.

If the measured robustness curve (brown curve in Figure 11.4) is outside the target area (blue boundary in Figure 11.4), the robustness per failure mechanism is sufficient. The green bar defines the measured robustness margin with respect to a specific failure mechanism and a target value (see also Figure 4.2).

If the measured robustness is less than the target, measures for improvement of insufficient robustness must be applied. These measures are weighted by the severity of the effect of the failure.

Robustness margin can be represented using the Robustness Indicator Figure (RIF). RIF is defined as the distance between the failure point ($P_{failure}$ or $t_{failure}$) and the requirements (P at use conditions or t_{target}). Taking the time to measure robustness margin, then

$$RIF = t_{failure} - t_{target}$$

Because in general robustness of a parameter means that the parameter is less sensitive to the change in the statistics of the input parameters (conditions of use, process variations, etc.). Therefore, it is useful to introduce a deviation parameter σ to the RIF. Furthermore, because reliability lifetimes are often Weibull or log-normal distributed, so ln(t) is used which is (approximately) normally distributed. In analogy with Cpk, an RIF of a reliability parameter is defined by

$$RIF = [\ln(t_{failure}) - \ln(t_{target})]/ 3\sigma$$

- $t_{failure}$ = mean stress failure time of different sample sets at required failure rate
- t_{target} = required lifetime at stress conditions
- σ = standard deviation of stress failure time [ln(t)] of different sample sets and also may include deviation from use conditions.

Robustness margin calculated with this RIF indicates not only the distance to the required target but also the sensitivity of response to the external variations.

12. IMPROVEMENT

If the measured robustness is less than the target, there are several possible reactions. Some of the measures could be applied before the robustness measurement in the development phase. In all cases, this is the preferred approach. The following options for improvement are not sorted by priorities or effectiveness. Each option must be checked to determine which measure is the most effective and the most efficient and therefore has to receive top priority.

a. Stress Set-up Review

When the evaluated robustness does not match the targeted level, the first step (least expensive) consists of a review of the set-up and the data. The following points should be checked:

- Confirmation of data:
    - Are the stress conditions correctly defined (for example to avoid overstress that stimulates irrelevant failure mechanisms)? Is the equipment calibrated?
    - Are the measurements conditions under control?
- Review of sample selection:
    - Are the samples representative for the production?
    - Were weak engineering samples selected for test?
    - Are the already stressed samples identified?
- Feasibility of failure mode:
    - Is there a good matching between targeted and obtained failure mode?
    - What is the model used?
    - How are the model parameters used from the extrapolation chosen?

- Review of stress method:
    - Is there a good matching between applied stress and targeted failure mechanism?
    - Did the test comply with the appropriate industry standard test method (i.e., JEDEC, IEC)?
- etc.

If the insufficient robustness is confirmed, improvement measures must be defined.

b. Mission Profile Review

A more detailed review of the mission profile, especially for the critical topics with low robustness values, should be performed to identify safety margins that have been added due to the lack of knowledge or data. The result of this activity could be a newly defined point of use. A tool like FMEA could support this activity to quantify the risks associated with critical topics.

c. Application Review

The robustness of a product is reflected in the application. Improvements could be made by alignment of the system design with the user application through co-engineering activities between the supplier and the user. Design-related issues could be addressed if the supplier and the user are involved and understand the use application and requirements. Also, both design teams can become educated on proper device use and specification.

- Check if a robustness target is required in detail
- More robust system design
- Part de-rating

d. Screening Strategy

The screening strategy should be adapted to the failure rate target. It should address the failure mechanisms identified during the reliability qualification. The failure mechanism Knowledge Matrix could be used in the adapted stress method.

The screening strategy should be based on:

- Deployment of Part Average Testing to detect and eliminate the outlier devices
- Deployment of Statistical Yield Analysis and Statistical Bin Limit to separate the abnormal wafers
- Standardization of tests programs: definition of a basic test program template, based on frontend technology, blocks functionality, product and application specificities

If burn-in is used to reduce failure rates, it must be demonstrated by a burn-in study that the relevant failure mechanism is really addressed. In some cases, the weak parts are related to certain locations on the edge of the wafer. If this is the case, the wafer edge exclusion zone can be changed to solve the problem [10].

e. Design for Reliability (DfR)

DfR is a powerful approach to prevent reliability problems in the application by early application of design measures. Therefore, the measures listed below should have been applied already during the design phase. Depending on the reasons for insufficient robustness, the enhancement of these measures should be discussed in this phase. Potential measures are:

- Redundant design
- Combined with an adequate simulation tool and the data of the Robustness Validation, the weak links in the design could be identified and mitigated. Examples are redundant vias and broadened lines in the interconnect part of the semiconductor component.
- Reliability simulation
- Simulation should be performed again using the Robustness Validation results to improve the accuracy of the simulation data
- Part de-rating

f. Technology/Design Solution

Technology solutions are the set of smart solutions (coupling process, design, and application) able to resolve the Robustness Validation gap. The comprehensive list cannot be provided here as these solutions require a case-by-case definition, but examples could be:

- Junction temperature watchdog. This device monitors the product operating junction temperature and is able to activate a low power mode with reduced functionality mode when the junction temperature is above a defined limit.
- Lowering voltage for voltage driven risks. (pushing the process to its capability limit)
- Multiplying or removing critical elements, like decoupling capacitors, if they do not meet the mission profile requirements.
- Critical element redundancy and switch capability: The critical element (like a capacitor) is controlled via a defined circuitry able to switch to a new capacitor if the first one fails.
- Use chip parasitic structures to clamp or bypass critical stress conditions.
- Use stress relief packages to absorb and limit damages related to mechanical constraints if present in the application.
- Tighten process limit
- Chip redesign to address robustness issues

The robustness, a trade-off must be found. The solution depends on the weight of these factors:

- Cost
- Schedule
- Quality
- Performance

When robustness improvement cannot be achieved by the means indicated above, the project situation and the related risks must be reviewed between the customer and the semiconductor component supplier.

The preferred strategy is to perform iterations in the definition of the product mission critical elements in order to offer a more effective trade-off between risks, performance, development timing, development costs, semiconductor component cost, and end-user requirements.

A typical example of such a situation would be if the current prevention techniques do not enable the expected target in the mission profile to be met. A potential trade-off in such a situation is to increase the silicon size, and costs, to add error detection and correction circuitry, for instance at embedded DRAM specific failure modes.

Before implementing the solution for improving robustness, the proposed solution must be reviewed with respect to several aspects:

- Is the expected improvement good enough with respect to the robustness target?
- Does the solution influence the robustness with respect to other failure mechanisms?
- What is the implementation risk (probability that the implementation fails)?

In most cases, the solution of a problem of low robustness generates some basic knowledge. This could be:

- New design strategies
- Better understanding of degradation or extrapolation models
- Better understanding of mission profiles

This knowledge should be fed back to the corresponding knowledge base to be made available for the next generation of projects. New failure mechanisms or their model descriptions should be used to update the Knowledge Matrix (see section 8.1).

NOTE: Continuous improvement to achieve the concept of “Zero Defects” [6], while important and comprehensive in scope, is outside the purview If there is more than one option to improve of this document.

13. MONITORING

13.1 Planning

Qualification reflects the status of the product/technology at a certain point in time, based on a certain limited sample size. The information and knowledge gathered during qualification serves to evaluate the parameters reviewed during Robustness Validation with respect to their criticality during ramp-up and volume production. This evaluation is the basis of the definition of monitoring that is needed to control the stability in the production phase. A template for the monitoring plan is included in the reporting template.

Monitoring shall be based on a risk assessment that must identify potential failure mechanisms for the production phase including intrinsic and extrinsic failures, analogously to qualification. Identification may be based on, but is not restricted to:

- Observation of failure mechanisms during development and qualification
- Mechanisms covered in a FMEA
- Previous experience with products using comparable materials and/or processes and production tools.

NOTE: A monitoring parameter may address more than one failure mechanism.

A monitor for each failure mechanism must be established. This monitor can address the parameters relevant to the failure mechanism at different levels. The monitoring parameters are typically chosen from different groups of parameters:

- In-line process parameters using SPC
- Electrical parameters at the wafer level with special focus on Key Parameters using SPC
- Final test parameters of the semiconductor component with special focus on Key Parameters using SPC
- Defect related tests, like Iddq or ΔIddq
- Highly accelerated stress tests, such as fast wafer level reliability (fWLR) tests
- Defect density monitors
- High voltage tests with the semiconductor component
    - Specific tests on flash cells, such as erratic
- bit, moving bit, cycling endurance
- PAT, SBA
- Burn-in
- Reliability monitoring using the semiconductor component

Monitoring of intrinsic failure mechanisms usually needs only small sample sizes, as in qualification. Sampling for extrinsic failure mechanisms may require the use of cumulative monitoring data, aggregated over a certain period of time, as large sample sizes are needed to detect PPM levels of defects.

- A reliability monitoring plan must be set up before the start of production. This monitoring plan should contain:
- Frequency of monitoring: The frequency of the monitoring must be aligned with the ramp-up/production volume.
- Sample size: to be aligned with the ramp-up/production volume.
- Response rules in case of deviations in the monitoring results
- Rationale in case of referencing to other technologies/products
- Stress tests/parameter measurements and test structures to be used. Test structure could be a specifically designed vehicle or the semiconductor component itself.
- List of components in the same relevant family that are to be monitored to cover the qualified component.

These elements are usually recorded and shared with the user in a Process Control Plan. Monitoring data should be checked continuously for indication of deviation in performance or reliability with respect to the robustness status at qualification. Special focus should be given to any extrinsic mechanisms that could not be evaluated during qualification.

Generally, unexpected behavior or anomalies shall trigger analysis or problem solving activities like 8D. In case of new knowledge generated by monitoring data, this information shall be fed back to the appropriate knowledge data base like FMEA or the Knowledge Matrix.

There will be occasions on which the supplier will want to implement a change to a qualified product in production to improve the product, throughput, manufacturing capacity and/or cost. While there are a number of industry standards and individual user and supplier requirements for qualifying these changes [3, 4, 5], these are outside the scope of this document. Suffice it to say that the user and supplier will need to agree on a robustness validation plan for changes using the concepts outlined in this document. In case of changes in the product or new application conditions, the monitoring plan must be reviewed.

14. REPORTING AND KNOWLEDGE EXCHANGE

The section defines documentation contents as well as communication paths along the value chain for clear understanding and agreement among the partners. Focus is set on the basic relationship between the semiconductor component and the ECU manufacturer. Special cases, such as direct communication Tier2 to OEM or intermediate steps from Tier1 to OEM regarding component aspects need to be described and contracted individually at the beginning of the cooperation.

Reporting differentiates between Commodity Components and ASICs

14.1 Content, Structure

For reporting during the module development and semiconductor component introduction phase, it is recommended to use the basic structure and form of the APQP method. The report must cover all relevant failure modes, no matter if the robustness was validated by test structures, at the product level, or based on process monitoring data. A link to the template for documenting the RV of semiconductor components is given in annex section 17. For commodity parts, the robustness validation report should be based on an assumed mission profile, which is to be documented in the report. For details on parameters which have to be specified for commodity products see RV-Manual.

14.2 Documents for Communication, Handouts and General Remarks

The contact partners and addresses or functional entities in the organizations of the involved parties must be agreed and documented at the start of the project. Restrictions to information that is considered to be confidential must be clearly identified and documented in detail during project start.

Generally, the share of confidential information is regulated and described by a Non-Disclosure Agreement between the supplier and the customer.

15. EXAMPLES

15.1 Examples of the Lack of or Poor Qualification

15.1.1 Delamination between Mould Compound and Die/lead Frame

This example shows that end-of-life testing is needed in order to correctly assess the risk of potential delamination between the mould compound and die/lead frame.

After being used for two years with 2 million parts in a safety critical application without displaying any prior trouble, the semiconductor component suddenly displayed a sharp increase of catastrophic failures due to lifted bond wires.

Temperature cycling using standard stress test qualification procedures did not show any failed parts, which means that the material in use in the field would have passed qualification because the standard stress test resulted in no fails after the required stress time. This demonstrates the weakness of the standard method [5] because either the automotive application was not covered by the stress condition or the acceleration factors were different from the ones used in the standard. Both weaknesses would have become obvious if end-of-life testing as required by Robustness Validation would have been chosen.