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AMENDMENT 9
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Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks —

Part 3: Standard for Ethernet

AMENDMENT 9: Physical layer specifications and management parameters for 25 Gb/s and 50 Gb/s passive optical networks

Télécommunications et échange entre systèmes informatiques — Exigences pour les réseaux locaux et métropolitains —

Partie 3: Norme pour Ethernet

AMENDEMENT 9: Spécifications de couche physique et paramètres de gestion pour réseaux optiques passifs à 25 Gb/s et 50 Gb/s

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IEEE Std 802.3ca™-2020
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018,
IEEE Std 802.3bt™-2018,
IEEE Std 802.3cd™-2018,
IEEE Std 802.3cn™-2019,
IEEE Std 802.3cg™-2019,
IEEE Std 802.3cq™-2020,
IEEE Std 802.3cm™-2020,
and IEEE Std 802.3ch™-2020)

IEEE Standard for Ethernet

Amendment 9: Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks

Developed by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 4 June 2020

IEEE SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2018 extends the operation of Ethernet passive optical networks (EPONs) to multiple channels of 25 Gb/s providing both symmetric and asymmetric operation for the following data rates (downstream/upstream): 25/10 Gb/s, 25/25 Gb/s, 50/10 Gb/s, 50/25 Gb/s, and 50/50 Gb/s. This standard specifies the 25 Gb/s EPON Multi-Channel Reconciliation Sublayer (MCRS), Nx25G-EPON Physical Coding Sublayers (PCSs), Physical Media Attachment (PMA) sublayers, and Physical Medium Dependent (PMD) sublayers that support both symmetric and asymmetric data rates while maintaining backward compatibility with already deployed 10 Gb/s EPON equipment. Backward compatibility with deployed 1G-EPON and ITU-T G.984 GPON is maintained with 25GBASE-PQ for the specific case of 1G-EPON and GPON ONUs using reduced-band (40 nm) lasers. The EPON operation is defined for distances of at least 20 km, and for a split ratio of at least 1:32.

Keywords: 25 Gb/s Ethernet passive optical networks (25G-EPON), 50 Gb/s Ethernet passive optical networks (50G-EPON), amendment, forward error correction (FEC), IEEE 802.3™, IEEE 802.3ca™, Multi-Channel Reconciliation Sublayer (MCRS), Multipoint MAC Control (MPMC), Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Physical Medium Dependent (PMD), PON, Point-to-Multipoint (P2MP)

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Introduction

This introduction is not part of IEEE Std 802.3ca-2020, IEEE Standard for Ethernet. Amendment 9: Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of IEEE Std 802.3ca-2020 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines

services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb™-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt™-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

IEEE Std 802.3cn™-2019

Amendment 4—This amendment includes changes to IEEE Std 802.3-2018 and adds 50 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications and management parameters for operation over single-mode fiber with reaches of at least 40 km.

IEEE Std 802.3cg™-2019

Amendment 5—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 146 through Clause 148 and Annex 146A and Annex 146B. This amendment adds 10 Mb/s Physical Layer specifications and management parameters for operation on a single balanced pair of conductors.

IEEE Std 802.3cq™-2020

Amendment 6—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 33 and related portions of the standard.

IEEE Std 802.3cm™-2020

Amendment 7—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 150. This amendment adds Physical Layer (PHY) specifications and management parameters for 400 Gb/s operation on four pairs (400GBASE-SR4.2) and eight pairs (400GBASE-SR8) of multimode fiber, over reaches of at least 100 m.

IEEE Std 802.3ch™-2020

Amendment 8—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 149, Annex 149A, Annex 149B, and Annex 149C. This amendment adds physical layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3ca™-2020

Amendment 9—This amendment to IEEE Std 802.3-2018 extends the operation of Ethernet passive optical networks (EPONs) to multiple channels of 25 Gb/s providing both symmetric and asymmetric operation for the following data rates (downstream/upstream): 25/10 Gb/s, 25/25 Gb/s, 50/10 Gb/s, 50/25 Gb/s, and 50/50 Gb/s. This amendment specifies the 25 Gb/s EPON Multi-Channel Reconciliation Sublayer (MCRS), Nx25G-EPON Physical Coding Sublayers (PCSs), Physical Media Attachment (PMA) sublayers, and Physical Medium Dependent (PMD) sublayers that support both symmetric and asymmetric data rates while maintaining backward compatibility with already deployed 10 Gb/s EPON equipment. The EPON operation is defined for distances of at least 20 km, and for a split ratio of at least 1:32.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 9: Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018, IEEE Std 802.3bt™-2018, IEEE Std 802.3cd™-2018, IEEE Std 802.3cn™-2019, IEEE Std 802.3cg™-2019, IEEE Std 802.3cq™-2020, IEEE Std 802.3cm™-2020, and IEEE Std 802.3ch™-2020.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[1]

[1] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Change the references for ITU-T Recommendations G.652 and G.657 as follows:

ITU-T Recommendation G.652, ~~2009~~2016—Characteristics of a single-mode optical fibre and cable.[2]

ITU-T Recommendation G.657, ~~2009~~2016—Characteristics of a bending-loss insensitive single-mode optical fibre and cable ~~for the access network~~.

1.4 Definitions

Insert the following two new definitions after 1.4.90 "200GXS":

1.4.90a 25/10G-EPON: An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (asymmetric rate).

1.4.90b 25/25G-EPON: An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in both downstream and upstream directions (symmetric rate).

Insert the following new definition after 1.4.100 "25GBASE-T":

1.4.100a 25G-EPON: An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 25/10G-EPON and 25/25G-EPON architectures.

Insert the following three new definitions before 1.4.128aa "50GBASE-CR" as inserted by IEEE Std 802.3cd-2018:

1.4.128aaa 50/10G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (asymmetric rate).

1.4.128aab 50/25G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in the downstream direction and 25 Gb/s in the upstream direction (asymmetric rate).

1.4.128aac 50/50G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in both downstream and upstream directions (symmetric rate).

Insert the following new definition after 1.4.128ah "50 Gb/s Media Independent Interface (50GMII)" as inserted by IEEE Std 802.3cd-2018:

1.4.128ai 50G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 50/10G-EPON, 50/25G-EPON, and 50/50G-EPON architectures.

Insert the following three new definitions after 1.4.244 "Energy-Efficient Ethernet (EEE)":

1.4.244a envelope: In the Multi-Channel Reconciliation Sublayer (MCRS, see IEEE Std 802.3, Clause 143), an envelope encapsulates data belonging to a specific LLID being transmitted on a specific

[2]ITU-T publications are available from the International Telecommunications Union (https://www.itu.int/).

MCRS channel, i.e., the data or idles sourced from a specific MAC instance and sent over a specific MCRS channel.

1.4.244b envelope allocation: In Nx25G-EPON, an envelope allocation represents a transmission window allocated to a single LLID (including GLID). A single GATE MPCPDU can carry up to seven envelope allocations.

1.4.244c envelope descriptor: A set of parameters consisting of LLID, StartTime, and EnvLength. An envelope descriptor defines a specific envelope pending transmission. Envelope descriptors are generated by the local MPCP sublayer and are passed to MCRS at the appropriate time to start the envelope transmission.

Insert the following three new definitions after 1.4.245 "envelope frame":

1.4.245a envelope header: An MCRS-specific marker that is inserted at the beginning of every envelope (envelope start header) and in place of every frame preamble (envelope continuation header). The envelope header includes fields that identify the LLID that sourced the encapsulated data and the length of the data (in units of EQ). Envelope headers also include a CRC8 field used to detect bit errors.

1.4.245b envelope quantum: A unit of information volume. Each envelope quantum represents 64 bits of data plus the layer-specific encoding. Thus, at the MAC Control sublayer and above, an envelope quantum is equal to 64 bits. Within the MCRS, an envelope quantum contains 72 bits (i.e., 64 bits of data and 8 bits of control). Within the PCS, after the 64B/66B encoding, an envelope quantum contains 66 bits, and after 256B/257B encoding, four envelope quanta are packed into a single 257-bit block.

1.4.245c EQT: The unit of measurement of time for time-related parameters specified in IEEE Std 802.3, Clause 144 Multipoint MAC Control for Nx25G-EPON. Each EQT is equal to the time required to transmit one EQ between the MCRS and the PCS across 25GMII, and equal to 2.56 ns.

Insert the following new definition after 1.4.277 "Gigabit Media Independent Interface (GMII)":

1.4.277a GPON: A Gigabit-capable Passive Optical Network, as specified in ITU-T G.984.2.

NOTE—ITU-T G.984.2 [B48a].

Change definition 1.4.278 as shown below:

1.4.278 grant: Within P2MP protocols, a permission to transmit at a specific time, for a specific duration. Grants are issued by the OLT (master) to ONUs (slaves) by means of GATE messages. In IEEE Std 802.3, Clause 64 and Clause 77, a GATE MPCPDU contains one or multiple grants issued to a single LLID, with each grant resulting in one or multiple upstream bursts transmitted by the ONU. In Clause 144, a grant includes envelope allocations for multiple LLIDs and there is a one-to-one correspondence between the grants issued to an ONU and upstream bursts transmitted by that ONU.

Change 1.4.312 (renumbered from 1.4.313 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018) as follows:

1.4.312 Logical Link Identifier (LLID): A numeric identifier assigned to a P2MP association between an OLT and ONU established through the Point-to-Point Emulation sublayer. Each P2MP association is assigned a unique LLID. The P2MP association is bound to an ONU DTE, where ~~a~~ the ONU MAC ~~would~~ is to observe a private association. In Nx25G-EPON, an LLID is also a collective term that refers to a Physical Layer ID (PLID), management link ID (MLID), user link ID (ULID), and a group link ID (GLID).

Insert the following new definition after 1.4.319 "maximum differential input" (renumbered from 1.4.320 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018):

1.4.319a MCRS channel: In IEEE Std 802.3, Clause 143, an MCRS channel represents one of a number of defined paths along which data passes in an MCRS.

Insert the following new definition after 1.4.332 "modulation error ratio (MER)" (renumbered from 1.4.333 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018):

1.4.332a Multi-Channel Reconciliation Sublayer (MCRS): The MCRS provides a mapping function that reconciles the signals at a specific Media Independent Interface (xMII) to a specific Media Access Control (MAC) Physical Signaling Sublayer (PLS) service definitions.

Insert the following new definition after 1.4.350 "NRZI" (renumbered from 1.4.351 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018):

1.4.350a Nx25G-EPON: An EPON architecture operating at a number of different downstream and upstream speeds. This term collectively refers to 25/10G-EPON, 25/25G-EPON, 50/10G-EPON, 50/25G-EPON, and 50/50G-EPON architectures.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphabetical order:

ECH	envelope continuation header
EQ	envelope quantum
EQT	envelope quantum time
ESH	envelope start header
GLID	group link ID
GPON	Gigabit-capable Passive Optical Network (see ITU-T G.984.2 [B48a])
MACI	MA_CONTROL.indication
MACR	MA_CONTROL.request
MADI	MA_DATA.indication
MADR	MA_DATA.request
MCRS	Multi-Channel Reconciliation Sublayer
MLID	management link ID
PLID	Physical Layer ID
QC-LDPC	quasi-cyclic low-density parity check
ULID	user link ID

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 25GBASE-T as follows:

…
25GBASE-PQ Clause 142 25/25G-EPON 256B/257B
25/10GBASE-PQ Clause 142 25/10G-EPON 256B/257B
…

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 50GBASE-R (inserted by IEEE Std 802.3cd-2018) as follows:

…
50GBASE-PQ Clause 142 50/50G-EPON 256B/257B
50/25GBASE-PQ Clause 142 50/25G-EPON 256B/257B
50/10GBASE-PQ Clause 142 50/10G-EPON 256B/257B
…

30.3.2.1.3 aPhyTypeList

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 25GBASE-T as follows:

…
25GBASE-PQ Clause 142 25/25G-EPON 256B/257B
25/10GBASE-PQ Clause 142 25/10G-EPON 256B/257B
…

Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 50GBASE-R (inserted by IEEE Std 802.3cd-2018) as follows:

…
50GBASE-PQ Clause 142 50/50G-EPON 256B/257B
50/25GBASE-PQ Clause 142 50/25G-EPON 256B/257B
50/10GBASE-PQ Clause 142 50/10G-EPON 256B/257B
…

30.3.5 MPCP managed object class

30.3.5.1 MPCP Attributes

30.3.5.1.2 aMPCPAdminState

Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.2 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational state of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, Clause 77, ~~or~~ Clause 103, or Clause 144 is enabled to do so when this attribute has the enumeration "enabled". When this attribute has the enumeration "disabled", the interface acts as it would if it had no Multipoint MAC Control sublayer. The operational state of the Multipoint MAC Control sublayer can be changed using the acMPCPAdminControl action.;

30.3.5.1.3 aMPCPMode

Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.3 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational mode of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, Clause 77, ~~or~~ Clause 103, or Clause 144. When this attribute has the enumeration "OLT", the interface acts as an OLT. When this attribute has the enumeration "ONU", the interface acts as an ONU. When this attribute has the enumeration "CLT", the interface acts as a CLT. When this attribute has the enumeration "CNU", the interface acts as a CNU.;

30.3.5.1.4 aMPCPLinkID

Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.3 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that identifies the Logical Link identity (LLID) associated with the MAC port as specified in 65.1.3.2.2, ~~or~~ 76.2.6.1.3.2, or 144.3.4, as appropriate.;

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 25GBASE-T as follows:

…

25/10GBASE-PQG-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141

25/10GBASE-PQG-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
25/10GBASE-PQG-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
25/10GBASE-PQG-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
25/10GBASE-PQX-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141
25/10GBASE-PQX-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
25/10GBASE-PQX-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
25/10GBASE-PQX-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
25GBASE-PQG-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
25GBASE-PQG-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
25GBASE-PQG-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
25GBASE-PQG-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
25GBASE-PQX-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
25GBASE-PQX-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
25GBASE-PQX-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
25GBASE-PQX-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141

…

Insert new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 50GBASE-ER (inserted by IEEE Std 802.3cn-2019) as follows:

...

50/10GBASE-PQG-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141

50/10GBASE-PQG-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
50/10GBASE-PQG-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/10GBASE-PQG-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
50/10GBASE-PQX-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141
50/10GBASE-PQX-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
50/10GBASE-PQX-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/10GBASE-PQX-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
50/25GBASE-PQG-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50/25GBASE-PQG-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50/25GBASE-PQG-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/25GBASE-PQG-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50/25GBASE-PQX-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50/25GBASE-PQX-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50/25GBASE-PQX-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/25GBASE-PQX-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50GBASE-PQG-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50GBASE-PQG-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50GBASE-PQG-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141

50GBASE-PQG-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50GBASE-PQX-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50GBASE-PQX-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50GBASE-PQX-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50GBASE-PQX-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141

...

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change rows for 1.29 and 1.901 through 1.1099 in Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.29	~~Reserved~~PMA/PMD control 3	45.2.1.23a
…		
1.901 through 1.~~1099~~999	Reserved	
1.1000 through 1.1002	Nx25G-EPON PMA/PMD extended ability	45.2.1.134a
1.1003 through 1.1099	Reserved	
…		

Insert 45.2.1.23a after 45.2.1.23 as follows:

45.2.1.23a PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–26a.

45.2.1.23a.1 Downstream differential encoding (1.29.15)

Downstream differential encoding is selected using bit 1.29.15. This bit is read/write in the OLT and read only in the ONU with the default value of 0 (indicating that downstream differential encoding is not enabled).

In the OLT, this bit controls whether downstream differential encoding is selected for the transmit PMA output.

In the ONU, this bit indicates whether the downstream differential decoding is enabled in the ONU receive PMA.

45.2.1.23a.2 PMA/PMD type selection (1.29.5:0)

The PMA/PMD type of the PMA/PMD is selected using bits 5 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in the Nx25G-EPON PMA/PMD extended ability registers (Registers 1.1000 through 1.1002, see 45.2.1.134a). A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

Table 45–26a—PMA/PMD control 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.29.15	Downstream differential encoding	1 = Downstream differential encoding enabled 0 = Downstream differential encoding disabled	R/W in OLT RO in ONU
1.29.14:6	Reserved	Value always 0	RO
1.29.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = Reserved 1 0 1 x x x = Reserved 1 0 0 1 1 1 = 50GBASE-PQX-U3 1 0 0 1 1 0 = 50GBASE-PQX-U2 1 0 0 1 0 1 = 50GBASE-PQX-D3 1 0 0 1 0 0 = 50GBASE-PQX-D2 1 0 0 0 1 1 = 50GBASE-PQG-U3 1 0 0 0 1 0 = 50GBASE-PQG-U2 1 0 0 0 0 1 = 50GBASE-PQG-D3 1 0 0 0 0 0 = 50GBASE-PQG-D2 0 1 1 1 1 1 = 50/25GBASE-PQX-U3 0 1 1 1 1 0 = 50/25GBASE-PQX-U2 0 1 1 1 0 1 = 50/25GBASE-PQX-D3 0 1 1 1 0 0 = 50/25GBASE-PQX-D2 0 1 1 0 1 1 = 50/25GBASE-PQG-U3 0 1 1 0 1 0 = 50/25GBASE-PQG-U2 0 1 1 0 0 1 = 50/25GBASE-PQG-D3 0 1 1 0 0 0 = 50/25GBASE-PQG-D2 0 1 0 1 1 1 = 50/10GBASE-PQX-U3 0 1 0 1 1 0 = 50/10GBASE-PQX-U2 0 1 0 1 0 1 = 50/10GBASE-PQX-D3 0 1 0 1 0 0 = 50/10GBASE-PQX-D2 0 1 0 0 1 1 = 50/10GBASE-PQG-U3 0 1 0 0 1 0 = 50/10GBASE-PQG-U2 0 1 0 0 0 1 = 50/10GBASE-PQG-D3 0 1 0 0 0 0 = 50/10GBASE-PQG-D2 0 0 1 1 1 1 = 25GBASE-PQX-U3 0 0 1 1 1 0 = 25GBASE-PQX-U2 0 0 1 1 0 1 = 25GBASE-PQX-D3 0 0 1 1 0 0 = 25GBASE-PQX-D2 0 0 1 0 1 1 = 25GBASE-PQG-U3 0 0 1 0 1 0 = 25GBASE-PQG-U2 0 0 1 0 0 1 = 25GBASE-PQG-D3 0 0 1 0 0 0 = 25GBASE-PQG-D2 0 0 0 1 1 1 = 25/10GBASE-PQX-U3 0 0 0 1 1 0 = 25/10GBASE-PQX-U2 0 0 0 1 0 1 = 25/10GBASE-PQX-D3 0 0 0 1 0 0 = 25/10GBASE-PQX-D2 0 0 0 0 1 1 = 25/10GBASE-PQG-U3 0 0 0 0 1 0 = 25/10GBASE-PQG-U2 0 0 0 0 0 1 = 25/10GBASE-PQG-D3 0 0 0 0 0 0 = 25/10GBASE-PQG-D2	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.134a after 45.2.1.134 as follows:

45.2.1.134a Nx25G-EPON PMA/PMD extended ability register (Registers 1.1000 through 1.1002)

The assignment of bits in the Nx25G-EPON PMA/PMD extended ability register is shown in Table 45–103a.

Table 45–103a—Nx25G-EPON PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1000.15	25GBASE-PQX-U3	1 = PMA/PMD is able to perform 25GBASE-PQX-U3 0 = PMA/PMD is not able to perform 25GBASE-PQX-U3	RO
1.1000.14	25GBASE-PQX-U2	1 = PMA/PMD is able to perform 25GBASE-PQX-U2 0 = PMA/PMD is not able to perform 25GBASE-PQX-U2	RO
1.1000.13	25GBASE-PQX-D3	1 = PMA/PMD is able to perform 25GBASE-PQX-D3 0 = PMA/PMD is not able to perform 25GBASE-PQX-D3	RO
1.1000.12	25GBASE-PQX-D2	1 = PMA/PMD is able to perform 25GBASE-PQX-D2 0 = PMA/PMD is not able to perform 25GBASE-PQX-D2	RO
1.1000.11	25GBASE-PQG-U3	1 = PMA/PMD is able to perform 25GBASE-PQG-U3 0 = PMA/PMD is not able to perform 25GBASE-PQG-U3	RO
1.1000.10	25GBASE-PQG-U2	1 = PMA/PMD is able to perform 25GBASE-PQG-U2 0 = PMA/PMD is not able to perform 25GBASE-PQG-U2	RO
1.1000.9	25GBASE-PQG-D3	1 = PMA/PMD is able to perform 25GBASE-PQG-D3 0 = PMA/PMD is not able to perform 25GBASE-PQG-D3	RO
1.1000.8	25GBASE-PQG-D2	1 = PMA/PMD is able to perform 25GBASE-PQG-D2 0 = PMA/PMD is not able to perform 25GBASE-PQG-D2	RO
1.1000.7	25/10GBASE-PQX-U3	1 = PMA/PMD is able to perform 25/10GBASE-PQX-U3 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U3	RO
1.1000.6	25/10GBASE-PQX-U2	1 = PMA/PMD is able to perform 25/10GBASE-PQX-U2 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U2	RO
1.1000.5	25/10GBASE-PQX-D3	1 = PMA/PMD is able to perform 25/10GBASE-PQX-D3 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D3	RO
1.1000.4	25/10GBASE-PQX-D2	1 = PMA/PMD is able to perform 25/10GBASE-PQX-D2 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D2	RO
1.1000.3	25/10GBASE-PQG-U3	1 = PMA/PMD is able to perform 25/10GBASE-PQG-U3 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U3	RO
1.1000.2	25/10GBASE-PQG-U2	1 = PMA/PMD is able to perform 25/10GBASE-PQG-U2 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U2	RO
1.1000.1	25/10GBASE-PQG-D3	1 = PMA/PMD is able to perform 25/10GBASE-PQG-D3 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D3	RO
1.1000.0	25/10GBASE-PQG-D2	1 = PMA/PMD is able to perform 25/10GBASE-PQG-D2 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D2	RO
1.1001.15	50/25GBASE-PQX-U3	1 = PMA/PMD is able to perform 50/25GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U3	RO

Table 45–103a—Nx25G-EPON PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1001.14	50/25GBASE-PQX-U2	1 = PMA/PMD is able to perform 50/25GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U2	RO
1.1001.13	50/25GBASE-PQX-D3	1 = PMA/PMD is able to perform 50/25GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D3	RO
1.1001.12	50/25GBASE-PQX-D2	1 = PMA/PMD is able to perform 50/25GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D2	RO
1.1001.11	50/25GBASE-PQG-U3	1 = PMA/PMD is able to perform 50/25GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U3	RO
1.1001.10	50/25GBASE-PQG-U2	1 = PMA/PMD is able to perform 50/25GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U2	RO
1.1001.9	50/25GBASE-PQG-D3	1 = PMA/PMD is able to perform 50/25GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D3	RO
1.1001.8	50/25GBASE-PQG-D2	1 = PMA/PMD is able to perform 50/25GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D2	RO
1.1001.7	50/10GBASE-PQX-U3	1 = PMA/PMD is able to perform 50/10GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U3	RO
1.1001.6	50/10GBASE-PQX-U2	1 = PMA/PMD is able to perform 50/10GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U2	RO
1.1001.5	50/10GBASE-PQX-D3	1 = PMA/PMD is able to perform 50/10GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D3	RO
1.1001.4	50/10GBASE-PQX-D2	1 = PMA/PMD is able to perform 50/10GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D2	RO
1.1001.3	50/10GBASE-PQG-U3	1 = PMA/PMD is able to perform 50/10GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U3	RO
1.1001.2	50/10GBASE-PQG-U2	1 = PMA/PMD is able to perform 50/10GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U2	RO
1.1001.1	50/10GBASE-PQG-D3	1 = PMA/PMD is able to perform 50/10GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D3	RO
1.1001.0	50/10GBASE-PQG-D2	1 = PMA/PMD is able to perform 50/10GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D2	RO
1.1002.15:8	Reserved	Value always 0	RO
1.1002.7	50GBASE-PQX-U3	1 = PMA/PMD is able to perform 50GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50GBASE-PQX-U3	RO
1.1002.6	50GBASE-PQX-U2	1 = PMA/PMD is able to perform 50GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50GBASE-PQX-U2	RO
1.1002.5	50GBASE-PQX-D3	1 = PMA/PMD is able to perform 50GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50GBASE-PQX-D3	RO
1.1002.4	50GBASE-PQX-D2	1 = PMA/PMD is able to perform 50GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50GBASE-PQX-D2	RO
1.1002.3	50GBASE-PQG-U3	1 = PMA/PMD is able to perform 50GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50GBASE-PQG-U3	RO

Table 45–103a—Nx25G-EPON PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1002.2	50GBASE-PQG-U2	1 = PMA/PMD is able to perform 50GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50GBASE-PQG-U2	RO
1.1002.1	50GBASE-PQG-D3	1 = PMA/PMD is able to perform 50GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50GBASE-PQG-D3	RO
1.1002.0	50GBASE-PQG-D2	1 = PMA/PMD is able to perform 50GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50GBASE-PQG-D2	RO

[a]RO = Read only

45.2.1.134a.1 25GBASE-PQX-U3 (1.1000.15)

When read as a one, bit 1.1000.15 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.15 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U3 PMA/PMD type.

45.2.1.134a.2 25GBASE-PQX-U2 (1.1000.14)

When read as a one, bit 1.1000.14 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.14 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U2 PMA/PMD type.

45.2.1.134a.3 25GBASE-PQX-D3 (1.1000.13)

When read as a one, bit 1.1000.13 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.13 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D3 PMA/PMD type.

45.2.1.134a.4 25GBASE-PQX-D2 (1.1000.12)

When read as a one, bit 1.1000.12 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.12 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D2 PMA/PMD type.

45.2.1.134a.5 25GBASE-PQG-U3 (1.1000.11)

When read as a one, bit 1.1000.11 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.11 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U3 PMA/PMD type.

45.2.1.134a.6 25GBASE-PQG-U2 (1.1000.10)

When read as a one, bit 1.1000.10 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.10 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U2 PMA/PMD type.

45.2.1.134a.7 25GBASE-PQG-D3 (1.1000.9)

When read as a one, bit 1.1000.9 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.9 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D3 PMA/PMD type.

45.2.1.134a.8 25GBASE-PQG-D2 (1.1000.8)

When read as a one, bit 1.1000.8 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.8 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D2 PMA/PMD type.

45.2.1.134a.9 25/10GBASE-PQX-U3 (1.1000.7)

When read as a one, bit 1.1000.7 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.7 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U3 PMA/PMD type.

45.2.1.134a.10 25/10GBASE-PQX-U2 (1.1000.6)

When read as a one, bit 1.1000.6 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.6 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U2 PMA/PMD type.

45.2.1.134a.11 25/10GBASE-PQX-D3 (1.1000.5)

When read as a one, bit 1.1000.5 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.5 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D3 PMA/PMD type.

45.2.1.134a.12 25/10GBASE-PQX-D2 (1.1000.4)

When read as a one, bit 1.1000.4 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.4 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D2 PMA/PMD type.

45.2.1.134a.13 25/10GBASE-PQG-U3 (1.1000.3)

When read as a one, bit 1.1000.3 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.3 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U3 PMA/PMD type.

45.2.1.134a.14 25/10GBASE-PQG-U2 (1.1000.2)

When read as a one, bit 1.1000.2 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.2 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U2 PMA/PMD type.

45.2.1.134a.15 25/10GBASE-PQG-D3 (1.1000.1)

When read as a one, bit 1.1000.1 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.1 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D3 PMA/PMD type.

45.2.1.134a.16 25/10GBASE-PQG-D2 (1.1000.0)

When read as a one, bit 1.1000.0 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.0 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D2 PMA/PMD type.

45.2.1.134a.17 50/25GBASE-PQX-U3 (1.1001.15)

When read as a one, bit 1.1001.15 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.15 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U3 PMA/PMD type.

45.2.1.134a.18 50/25GBASE-PQX-U2 (1.1001.14)

When read as a one, bit 1.1001.14 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.14 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U2 PMA/PMD type.

45.2.1.134a.19 50/25GBASE-PQX-D3 (1.1001.13)

When read as a one, bit 1.1001.13 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.13 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D3 PMA/PMD type.

45.2.1.134a.20 50/25GBASE-PQX-D2 (1.1001.12)

When read as a one, bit 1.1001.12 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.12 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D2 PMA/PMD type.

45.2.1.134a.21 50/25GBASE-PQG-U3 (1.1001.11)

When read as a one, bit 1.1001.11 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.11 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U3 PMA/PMD type.

45.2.1.134a.22 50/25GBASE-PQG-U2 (1.1001.10)

When read as a one, bit 1.1001.10 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.10 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U2 PMA/PMD type.

45.2.1.134a.23 50/25GBASE-PQG-D3 (1.1001.9)

When read as a one, bit 1.1001.9 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.9 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D3 PMA/PMD type.

45.2.1.134a.24 50/25GBASE-PQG-D2 (1.1001.8)

When read as a one, bit 1.1001.8 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.8 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D2 PMA/PMD type.

45.2.1.134a.25 50/10GBASE-PQX-U3 (1.1001.7)

When read as a one, bit 1.1001.7 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.7 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U3 PMA/PMD type.

45.2.1.134a.26 50/10GBASE-PQX-U2 (1.1001.6)

When read as a one, bit 1.1001.6 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.6 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U2 PMA/PMD type.

45.2.1.134a.27 50/10GBASE-PQX-D3 (1.1001.5)

When read as a one, bit 1.1001.5 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.5 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D3 PMA/PMD type.

45.2.1.134a.28 50/10GBASE-PQX-D2 (1.1001.4)

When read as a one, bit 1.1001.4 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.4 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D2 PMA/PMD type.

45.2.1.134a.29 50/10GBASE-PQG-U3 (1.1001.3)

When read as a one, bit 1.1001.3 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.3 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U3 PMA/PMD type.

45.2.1.134a.30 50/10GBASE-PQG-U2 (1.1001.2)

When read as a one, bit 1.1001.2 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.2 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U2 PMA/PMD type.

45.2.1.134a.31 50/10GBASE-PQG-D3 (1.1001.1)

When read as a one, bit 1.1001.1 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.1 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D3 PMA/PMD type.

45.2.1.134a.32 50/10GBASE-PQG-D2 (1.1001.0)

When read as a one, bit 1.1001.0 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.0 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D2 PMA/PMD type.

45.2.1.134a.33 50GBASE-PQX-U3 (1.1002.7)

When read as a one, bit 1.1002.7 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1002.7 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U3 PMA/PMD type.

45.2.1.134a.34 50GBASE-PQX-U2 (1.1002.6)

When read as a one, bit 1.1002.6 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1002.6 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U2 PMA/PMD type.

45.2.1.134a.35 50GBASE-PQX-D3 (1.1002.5)

When read as a one, bit 1.1002.5 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1002.5 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D3 PMA/PMD type.

45.2.1.134a.36 50GBASE-PQX-D2 (1.1002.4)

When read as a one, bit 1.1002.4 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1002.4 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D2 PMA/PMD type.

45.2.1.134a.37 50GBASE-PQG-U3 (1.1002.3)

When read as a one, bit 1.1002.3 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1002.3 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U3 PMA/PMD type.

45.2.1.134a.38 50GBASE-PQG-U2 (1.1002.2)

When read as a one, bit 1.1002.2 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1002.2 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U2 PMA/PMD type.

45.2.1.134a.39 50GBASE-PQG-D3 (1.1002.1)

When read as a one, bit 1.1002.1 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1002.1 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D3 PMA/PMD type.

45.2.1.134a.40 50GBASE-PQG-D2 (1.1002.0)

When read as a one, bit 1.1002.0 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1002.0 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D2 PMA/PMD type.

45.2.3 PCS registers

Change the rows for registers 3.76 through 3.199 in Table 45–176 as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
…		
3.76, 3.77	~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter	45.2.3.41
3.78, 3.79	~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter	45.2.3.42
3.80	10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval~~timer~~ control	45.2.3.43
3.81	10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status	45.2.3.44
3.82	10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control	45.2.3.45
3.83 through 3.134	Nx25G-EPON synchronization pattern	45.2.3.45a
~~3.83~~3.135 through 3.199	Reserved	
…		

45.2.3.1 PCS control 1 register (Register 3.0)

Change the row for bits 3.0.5:2 in Table 45–177 (as modified IEEE Std 802.cd-2018) as follows (unchanged rows not shown):

Table 45–177—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = ~~Reserved~~25/10 Gb/s 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45–180 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.cd-2018) as follows (unchanged rows not shown):

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:~~4~~5	Reserved	Value always 0	RO
3.7.~~3~~4:0	PCS type selection	~~4~~ 3 2 1 0 1 1 x x x = reserved 1 0 1 x x = reserved 1 0 0 1 1 = Select 25GBASE-PQ PCS type 1 0 0 1 0 = Select 25/10GBASE-PQ PCS type 1 0 0 0 1 = Select 25GBASE-PQ PCS type, Tx only 1 0 0 0 0 = Select 25GBASE-PQ PCS type, Rx only 0 1 1 1 1 = Select 5GBASE-R PCS type 0 1 1 1 0 = Select 2.5GBASE-X PCS type 0 1 1 0 1 = Select 400GBASE-R PCS type 0 1 1 0 0 = Select 200GBASE-R PCS type 0 1 0 1 1 = Select 5GBASE-T PCS type 0 1 0 1 0 = Select 2.5GBASE-T PCS type 0 1 0 0 1 = Select 25GBASE-T PCS type 0 1 0 0 0 = Select 50GBASE-R PCS type 0 0 1 1 1 = Select 25GBASE-R PCS type 0 0 1 1 0 = Select 40GBASE-T PCS type 0 0 1 0 1 = Select 100GBASE-R PCS type 0 0 1 0 0 = Select 40GBASE-R PCS type 0 0 0 1 1 = Select 10GBASE-T PCS type 0 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

Change the title and text of 45.2.3.6.1 as follows:

45.2.3.6.1 PCS type selection (3.7.~~3~~4:0)

The PCS type shall be selected using bits ~~3~~4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.9~~:0, 3.8.7:0,~~ and 3.9.~~1~~7:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register or the PCS status 3 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.8 PCS status 3 register (Register 3.9)

Change the row for bits 3.9.15:4 in Table 45–182 (as modified by IEEE Std 802.3cb-2018) as follows (unchanged rows not shown):

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.9.15:4~~8~~	Reserved	Value always 0	RO
3.9.7	25GBASE-PQ capable	1 = PCS is able to support 25GBASE-PQ PCS type 0 = PCS is not able to support 25GBASE-PQ PCS type	RO
3.9.6	25/10GBASE-PQ capable	1 = PCS is able to support25/10GBASE-PQ PCS type 0 = PCS is not able to support 25/10GBASE-PQ PCS type	RO
3.9.5	25GBASE-PQ Rx only capable	1 = PCS is able to support 25GBASE-PQ Rx only PCS type 0 = PCS is not able to support 25GBASE-PQ Rx only PCS type	RO
3.9.4	25GBASE-PQ Tx only capable	1 = PCS is able to support 25GBASE-PQ Tx only PCS type 0 = PCS is not able to support 25GBASE-PQ Tx only PCS type	RO
…			

[a]RO = Read only

Insert 45.2.3.8.aa through 45.2.3.8.ad (before 45.2.3.8.a as inserted by IEEE Std 802.3cb-2018) as follows:

45.2.3.8.aa 25GBASE-PQ capable (3.9.7)

When read as a one, bit 3.9.7 indicates that the PCS is able to support the 25GBASE-PQ PCS type. When read as a zero, bit 3.9.7 indicates that the PCS is not able to support the 25GBASE-PQ PCS type.

45.2.3.8.ab 25/10GBASE-PQ capable (3.9.6)

When read as a one, bit 3.9.6 indicates that the PCS is able to support the 25/10GBASE-PQ PCS type. When read as a zero, bit 3.9.6 indicates that the PCS is not able to support the 25/10GBASE-PQ PCS type.

45.2.3.8.ac 25GBASE-PQ Rx only capable (3.9.5)

When read as a one, bit 3.9.5 indicates that the PCS is able to support the 25GBASE-PQ Rx only PCS type. When read as a zero, bit 3.9.5 indicates that the PCS is not able to support the 25GBASE-PQ Rx only PCS type.

45.2.3.8.ad 25GBASE-PQ Tx only capable (3.9.4)

When read as a one, bit 3.9.4 indicates that the PCS is able to support the 25GBASE-PQ Tx only PCS type. When read as a zero, bit 3.9.4 indicates that the PCS is not able to support the 25GBASE-PQ Tx only PCS type.

Change the title, text and tables for 45.2.3.41 through 45.2.3.45 as follows:

45.2.3.41 ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter register is shown in Table 45–213. See 76.3.3.3.2 for a definition of ~~this~~the

10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–213—~~10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.76.15:0	corrected FEC codewords lower	corrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.77.15:0	corrected FEC codewords upper	corrected_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.42 ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter register is shown in Table 45–214. See 76.3.3.3.2 for a definition of ~~this~~the 10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–214—~~10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.78.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.79.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[32:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.43 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval ~~timer~~ control register (Register 3.80)

The assignment of bits in the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval ~~timer~~ control register is shown in Table 45–215. This register is defined only when 10GBASE-PR, ~~or~~ 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON QC-LDPC BER Monitor is described in 142.3.5.6.

Table 45–215—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval ~~timer~~ control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.15:8	Reserved	Value always 0	RO
3.80.7:0	~~10G~~ EPON BER monitor ~~timer~~ interval	For 10GBASE-PR and 10/1GBASE-PRX: Duration (in units of 5 microseconds) of the timer used by the ~~10G EPON~~ BER monitor function. Default value is 25 (i.e., 125 microseconds). A value of zero indicates that the BER monitor function is disabled. For Nx25G-EPON: QC-LDPC codeword count (in units of 16 codewords) of the monitoring interval used by the BER Monitor function. Default value is 12 (i.e., 192 codewords).	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.44 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status (Register 3.81)

The assignment of bits in the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status register is shown in Table 45–216. This register is defined only when 10GBASE-PR ~~or~~, 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported.

Table 45–216—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.81.15:2	Reserved	Value always 0	RO
3.81.1	Latched high BER	10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON PCS: 1 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ reported a high BER. 0 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ did not report a high BER.	RO, LH
3.81.0	high BER	10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON PCS: 1 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ reporting a high BER. 0 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ not reporting a high BER.	RO

[a]RO Read only, LH = Latching high

45.2.3.44.1 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS high BER (3.81.0)

In the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4 for 10GBASE-PR and, 10/1GBASE-PRX, and the HiBer variable in 142.3.5.2 for Nx25G-EPON.

45.2.3.44.2 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS latched high BER (3.81.1)

In the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

This bit is a latching high version of the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON high BER status bit (3.81.0).

45.2.3.45 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control (Register 3.82)

The assignment of bits in the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control register is shown in Table 45–217. This register is defined only when 10GBASE-PR~~or~~, 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON QC-LDPC BER Monitor is described in 142.3.5.6.

Table 45–217—10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15:0	~~10G-~~EPON BER monitor threshold	For 10G-EPON: n~~N~~umber of sync header errors within a timer interval that triggers a high BER condition for the ~~10G-EPON~~ BER monitor function. Default value is 1600. A value of zero indicates that the BER monitor function is disabled. For Nx25G-EPON: number of invalid QC-LDPC codeword parity checks within a BER monitor interval that triggers a high BER condition for the BER Monitor function. Default value is 18. A value of zero indicates that the BER Monitor function is disabled.	R/W

[a]R/W = Read/Write

Insert 45.2.3.45a and subclauses after 45.2.3.45 as follows:

45.2.3.45a Nx25G-EPON synchronization pattern registers (Registers 3.83 through 3.134)

The assignment of bits in registers 3.83 through 3.134 is shown in Table 45–217a. The Nx25G-EPON synchronization pattern (see 142.1.3 and 144.3.6.7) is used in the upstream data transmissions to facilitate the OLT in locking to the incoming data burst.

Table 45–217a—Nx25G-EPON synchronization pattern registers bit definitions

Bit(s)	Name	Description	R/W[a]
3.83.15:6	Reserved	Value always 0	RO
3.83.5	SP3 bit 257	The MSB of the 257-bit SP3.	R/W
3.83.4	SP3 balanced	Balance setting for SP3.	R/W
3.83.3	SP2 bit 257	The MSB of the 257-bit SP2.	R/W

Table 45–217a—Nx25G-EPON synchronization pattern registers bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.83.2	SP2 balanced	Balance setting for SP2.	R/W
3.83.1	SP1 bit 257	The MSB of the 257-bit SP1.	R/W
3.83.0	SP1 balanced	Balance setting for SP1.	R/W
3.99.15 through 3.84.0	SP1 pattern	The lower 256 bits of SP1. Bit 0 is stored in 3.84.0, and bit 255 is stored in 3.99.15.	R/W
3.100.15:0	SP1 length	The number of times SP1 is to be repeated.	R/W
3.116.15 through 3.101.0	SP2 pattern	The lower 256 bits of SP2. Bit 0 is stored in 3.101.0, and bit 255 is stored in 3.116.15.	R/W
3.117.15:0	SP2 length	The number of times SP2 is to be repeated.	R/W
3.133.15 through 3.118.0	SP3 pattern	The lower 256 bits of SP3. Bit 0 is stored in 3.118.0, and bit 255 is stored in 3.133.15.	R/W
3.134.15:0	SP3 length	The number of times SP3 is to be repeated.	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.45a.1 SP3 bit 257 (3.83.5)

In the Nx25G-EPON PCS, bit 3.83.5 indicates the value to be used for the 257th bit of SP3. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.2 SP3 balanced (3.83.4)

In the Nx25G-EPON PCS, bit 3.83.4 indicates that repeating SP3 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP3 is to remain unbalanced, i.e., SP3 is always transmitted using the values from 3.83.5 and 3.118.0 through 3.133.15. When this bit is set to a one SP3 is to be balanced, i.e., each 257-bit block of SP3 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.3 SP2 bit 257 (3.83.3)

In the Nx25G-EPON PCS, bit 3.83.3 indicates the value to be used for the 257th bit of SP2. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.4 SP2 balanced (3.83.2)

In the Nx25G-EPON PCS, bit 3.83.2 indicates that repeating SP2 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP2 is to remain unbalanced, i.e., SP2 is always transmitted using the values from 3.83.3 and 3.101.0 through 3.116.15. When this bit is set to a one SP2 is to be balanced, i.e., each 257-bit block of SP2 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.5 SP1 bit 257 (3.83.1)

In the Nx25G-EPON PCS, bit 3.83.1 indicates the value to be used for the 257th bit of SP1. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.6 SP1 balanced (3.83.0)

In the Nx25G-EPON PCS, bit 3.83.0 indicates that repeating SP1 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP1 is to remain unbalanced, i.e., SP1 is always transmitted using the values from 3.83.1 and 3.84.0 through 3.99.15. When this bit is set to a one SP1 is to be balanced, i.e., each 257-bit block of SP1 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.7 SP1 pattern (3.84.0 through 3.99.15)

In the Nx25G-EPON PCS, bits 3.84.0 through 3.99.15 indicate the value to be used for the lower 256 bits of the initial SP1 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP1 are determined by bit 3.83.0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.8 SP1 length (3.100.15:0)

In the Nx25G-EPON PCS, bits 3.100.15:0 indicate the number of times the 257-bit SP1 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.9 SP2 pattern (3.101.0 through 3.116.15)

In the Nx25G-EPON PCS, bits 3.101.0 through 3.116.15 indicate the value to be used for the lower 256 bits of the initial SP2 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP2 are determined by bit 3.100.15:0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.10 SP2 length (3.117.15:0)

In the Nx25G-EPON PCS, bits 3.117.15:0 indicate the number of times the 257-bit SP2 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.11 SP3 pattern (3.118.0 through 3.133.15)

In the Nx25G-EPON PCS, bits 3.118.0 through 3.133.15 indicate the value to be used for the lower 256 bits of the initial SP3 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP3 are determined by bit 3.117.15:0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.45a.12 SP3 length (3.134.15:0)

In the Nx25G-EPON PCS, bits 3.134.15:0 indicate the number of times the 257-bit SP3 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[3]

45.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 45, MDIO interface, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

45.5.2 Identification

45.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

45.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ca-2020, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ca-2020.)	

Date of Statement	

[3] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.3 PMA/PMD management functions

Insert a new row at the end of the table in 45.5.3.3 after MM229 inserted by IEEE Std 802.3ch-2020 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
MM230	PMA/PMD type selection	45.2.1.23a.2	Device ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised	M	Yes [ ]

45.5.3.7 PCS management functions

Change item RM23 in the table in 45.5.3.7 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
RM23	PCS type is selected using bits 4~~1~~ through 0	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
…					

56. Introduction to Ethernet for subscriber access networks

56.1 Overview

Change the second paragraph in 56.1 as follows:

In addition, a mechanism for network Operations, Administration, and Maintenance (OAM) is included to facilitate network operation and troubleshooting. 100BASE-LX10 extends the reach of 100BASE-X to achieve 10 km over conventional single-mode two-fiber cabling. The relationships between these EFM elements and the ISO/IEC Open System Interconnection (OSI) reference model are shown in Figure 56–1 for point-to-point topologies, Figure 56–2 for 1G-EPON topologies, Figure 56–3 for 10/10G-EPON topologies, Figure 56–4 for 10/1G-EPON topologies, ~~and~~ Figure 56–5 for EPoC topologies, and Figure 56–6 for Nx25G-EPON topologies.

Insert new Figure 56–6 (as shown on the next page) after Figure 56–5.

Change the last paragraph in 56.1 as follows:

The EFM architecture is further extended in:

— ~~in~~ Clause 75 and Clause 76 by the addition of 10G–EPON~~. 10G–EPON includes the 10/10G-EPON (10 Gb/s downstream and 10 Gb/s upstream) as well as 10/1G-EPON (10 Gb/s downstream and 1 Gb/s upstream) PONs. The EFM architecture is further extended in~~

— Clause 100, Clause 101, and Clause 102 by the addition of EPoC.

— Clause 141, Clause 142, and Clause 143 by the addition of Nx25G-EPON.

56.1.2 Summary of P2MP sublayers

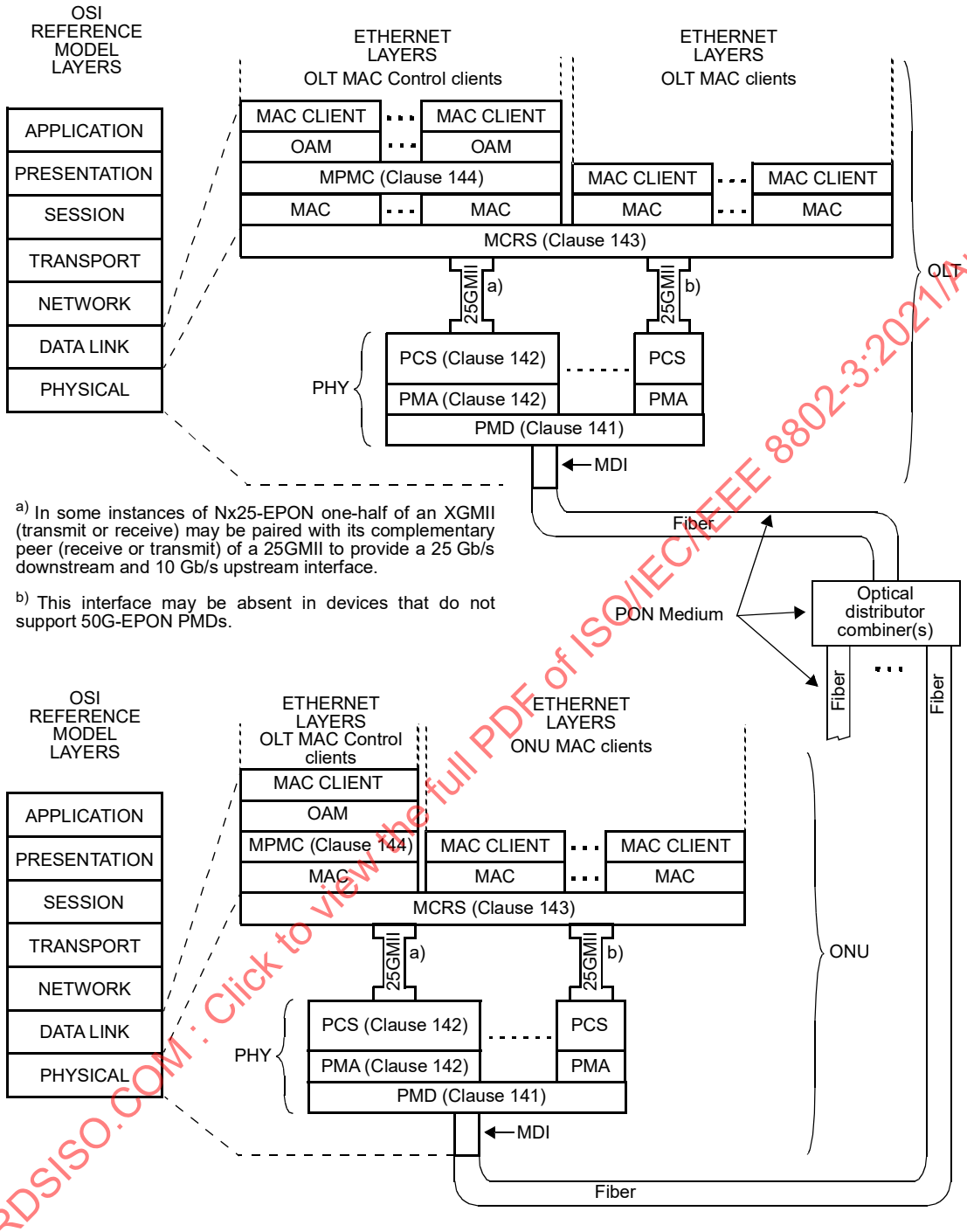
Change the first paragraph and lettered list in 56.1.2 as follows:

For P2MP optical fiber topologies, EFM supports ~~two~~the following systems:

a) PON with a nominal ~~bit~~MAC data rate of ~~1000 M~~1 Gb/s in both downstream and upstream directions (1G-EPON), shared amongst the population of Optical Network Units (ONUs) attached to the P2MP topology. The P2MP PHYs use the 1000BASE-PX Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA) sublayer defined in Clause 65 and an optional forward error correction (FEC) function defined in Clause 65.

b) PON with a nominal ~~bit~~MAC data rate of 10 Gb/s in both the downstream and upstream directions (10/10G-EPON) as well as PON with ~~a~~the nominal ~~bit~~MAC data rate of 10 Gb/s in the downstream direction and 1 Gb/s in the upstream direction (10/1G-EPON), shared amongst the population of ONUs attached to the P2MP topology, and collectively referred to as 10G-EPON. The P2MP PHYs for the 10/10G-EPON use the 10GBASE-PR PCS and PMA (see ~~Clause 75~~Clause 76). The P2MP PHYs for 10/1G-EPON use the 10GBASE-PRX PCS and PMA (see Clause 76). EPONs using a nominal 10 Gb/s bit rate use a mandatory FEC function defined in Clause 76 in any direction running at the 10 Gb/s bit rate.

c) PON with a nominal MAC data rate of 25 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (25/10G-EPON), 25 Gb/s in both the downstream and upstream directions (25/25G-EPON), 50 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (50/10G-EPON), 50 Gb/s in the downstream direction and 25 Gb/s in the upstream direction (50/25G-EPON), and 50 Gb/s in both the downstream and upstream directions (50/50G-EPON), shared amongst the population of ONUs attached to the P2MP topology, and collectively referred to as Nx25G-EPON. The P2MP PHYs for the 25/10G-EPON and 25/25G-EPON use a single channel in each direction. The P2MP PHYs for the 50/10G-EPON and 50/25G-EPON use two channels in the downstream direction and a single channel in the upstream direction. The P2MP PHYs for the



[a] In some instances of Nx25-EPON one-half of an XGMII (transmit or receive) may be paired with its complementary peer (receive or transmit) of a 25GMII to provide a 25 Gb/s downstream and 10 Gb/s upstream interface.

[b] This interface may be absent in devices that do not support 50G-EPON PMDs.

25GMII=25 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–6—Architectural positioning of EFM: P2MP Nx25G-EPON architecture

50/50G-EPON uses two channels in each direction. Each PMA channel in the downstream direction operates at a 25.78125 GBd line rate. Each PMA channel in the upstream direction operates at either a 25.78125 GBd or a 10.3125 GBd line rate. Each channel implements a mandatory FEC function in each direction (see Clause 142).

56.1.2.1 Multipoint MAC Control Protocol (MPCP)

Change the first two paragraphs in 56.1.2.1 as follows:

The Multipoint MAC Control Protocol (MPCP) for 1G-EPON uses messages, state diagrams, and timers, as defined in Clause 64, to control access to a P2MP topology~~;~~; ~~while~~ Clause 77 defines the messages, state diagrams, and timers required to control access to a P2MP ODN topology in 10G-EPON; and Clause 144 defines the messages, state diagrams, and timers required to control access to a P2MP ODN topology in Nx25G-EPON. The issues related to coexistence of 1G-EPON and 10G-EPON on the same fiber plant are described in 77.4.

Every P2MP ODN topology consists of one Optical Line Terminal (OLT) and~~plus~~ one or more ONUs, as shown in Figure 56–2, Figure 56–3, ~~and~~ Figure 56–4, and Figure 56–6 for 1G-EPON, 10/10G-EPON ~~and~~, 10/1G-EPON, and Nx25G-EPON, respectively. One of several instances of the MPCP in the OLT communicates with the instance of the MPCP in the ONU. A pair of MPCPs that communicate between the OLT and ONU are a distinct and associated pair.

56.1.2.2 Reconciliation Sublayer (RS) and media independent interfaces

Change the first and fourth paragraphs 56.1.2.2 as follows:

The Clause 22 RS and MII, Clause 35 RS and GMII, and Clause 46 RS and XGMII are all employed for the same purpose in EFM, that being the interconnection between the MAC sublayer and the PHY sublayers. Extensions to the Clause 35 RS for P2MP topologies are described in Clause 65, the RS for 10G-EPON P2MP topologies is described in Clause 76, the RS for Nx25G-EPON P2MP topologies is described in Clause 143, and the RS for EPoC P2MP topologies is described in Clause 101.

This is described in Clause 65 for EPON, in Clause 76 for 10G-EPON, in Clause 143 for Nx25G-EPON, and in Clause 101 for EPoC. EFM copper links use the MII of Clause 22 operating at 100 Mb/s. This is described in 61.1.4.1.2.

56.1.3 Physical Layer signaling systems

Insert a new paragraph in 56.1.3 after the paragraph "All 10G-EPON PMDs are defined in Clause 75" as follows:

Additionally, EFM introduces a family of Physical Layer signaling systems that are derived from 25GBASE-R, but which include RS, PCS and PMA sublayers adapted for Nx25G-EPON, along with a mandatory FEC function, as defined in Clause 142. All these systems employ PMDs defined in Clause 141.

Insert new rows at the end of Table 56–1 (below the 10GPASS-XR-U row), as follows (unchanged rows and footnotes not shown):

Table 56–1—Summary of EFM Physical Layer signaling systems

Name	Location	Rate[a]	Nominal reach (km)	Medium	Clause
…					
25/10GBASE-PQG-D2	OLT	25 Gb/s (tx) 10 Gb/s (rx)	20	One single-mode fiber PON	141
25/10GBASE-PQG-D3					
25/10GBASE-PQX-D2					
25/10GBASE-PQX-D3					
25/10GBASE-PQG-U2	ONU	10 Gb/s (tx) 25 Gb/s (rx)			
25/10GBASE-PQG-U3					
25/10GBASE-PQX-U2					
25/10GBASE-PQX-U3					
25GBASE-PQG-D2	OLT	25 Gb/s	20	One single-mode fiber PON	141
25GBASE-PQG-D3					
25GBASE-PQX-D2					
25GBASE-PQX-D3					
25GBASE-PQG-U2	ONU				
25GBASE-PQG-U3					
25GBASE-PQX-U2					
25GBASE-PQX-U3					
50/10GBASE-PQG-D2	OLT	50 Gb/s (tx) 10 Gb/s (rx)	20	One single-mode fiber PON	141
50/10GBASE-PQG-D3					
50/10GBASE-PQX-D2					
50/10GBASE-PQX-D2					
50/10GBASE-PQG-U2	ONU	10 Gb/s (tx) 50 Gb/s (rx)			
50/10GBASE-PQG-U3					
50/10GBASE-PQX-U2					
50/10GBASE-PQX-U2					

Table 56–1—Summary of EFM Physical Layer signaling systems *(continued)*

Name	Location	Rate[a]	Nominal reach (km)	Medium	Clause
50/25GBASE-PQG-D2	OLT	50 Gb/s (tx) 25 Gb/s (rx)	20	One single-mode fiber PON	141
50/25GBASE-PQG-D3					
50/25GBASE-PQX-D2					
50/25GBASE-PQX-D2					
50/25GBASE-PQG-U2	ONU	25 Gb/s (tx) 50 Gb/s (rx)			
50/25GBASE-PQG-U3					
50/25GBASE-PQX-U2					
50/25GBASE-PQX-U2					
50GBASE-PQG-D2	OLT	50 Gb/s	20	One single-mode fiber PON	141
50GBASE-PQG-D3					
50GBASE-PQX-D2					
50GBASE-PQX-D3					
50GBASE-PQG-U2	ONU				
50GBASE-PQG-U3					
50GBASE-PQX-U2					
50GBASE-PQX-U3					

[a]For ~~10/1G-EPON~~ Physical Layer signaling systems the transmit rate is denoted with the abbreviation "(tx)" to the location whereas the receive rate is denoted with the abbreviation "(rx)".

Change the last paragraph in 56.1.3, change Table 56–3, and insert a new Table 56–4 as follows:

Table 56–2 specifies the correlation between nomenclature and clauses for P2P systems, while Table 56–3 specifies the correlation between nomenclature and clauses for optical P2MP systems, and Table 56–4 specifies the correlation between nomenclature and clauses for coaxial P2MP systems. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Table 56–3—Nomenclature and clause correlation for optical P2MP systems[a]

Nomenclature	Clause															
	57	60				64	65		66	75	76	77	~~Clause 100~~ 141	~~Clause 101~~ 142	~~Clause 102~~ 143	~~Clause 103~~ 144
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	1000BASE-PX30 PMD	1000BASE-PX40 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX or 10GBASE-PR PMDs	P2MP RS, PCS, PMA, FEC	10G-EPON P2MP MPMC	~~10GPASS-XR~~Nx25GBASE-PQ PMD	~~EPoC~~Nx25GBASE-PQ P2MP ~~RS~~, PCS, PMA, FEC	~~EPoC PHY Link~~Nx25GBASE-PQ M2MP MC~~R~~S	~~EPoC~~Nx25GBASE-PQ P2MP MPMC
1000BASE-PX10-D	O	M				M	M	O	M							
1000BASE-PX10-U	O	M				M	M	O								
1000BASE-PX20-D	O		M			M	M	O	M							
1000BASE-PX20-U	O		M			M	M	O								
1000BASE-PX30-D	O			M		M	M	O	M							
1000BASE-PX30-U	O			M		M	M	O								
1000BASE-PX40-D	O				M	M	M	O	M							
1000BASE-PX40-U	O				M	M	M	O								
10/1GBASE-PRX-D1	O			M		M				M	M	M				
10/1GBASE-PRX-U1	O			M		M				M	M	M				
10/1GBASE-PRX-D2	O				M	M				M	M	M				
10/1GBASE-PRX-U2	O				M	M				M	M	M				
10/1GBASE-PRX-D3	O					M				M	M	M				
10/1GBASE-PRX-U3	O					M				M	M	M				
10/1GBASE-PRX-D4	O					M				M	M	M				
10/1GBASE-PRX-U4	O					M				M	M	M				
10GBASE-PR-D1	O									M	M	M				
10GBASE-PR-U1	O									M	M	M				
10GBASE-PR-D2	O									M	M	M				
10GBASE-PR-D3	O									M	M	M				
10GBASE-PR-U3	O									M	M	M				
10GBASE-PR-D4	O									M	M	M				
10GBASE-PR-U4	O									M	M	M				

Table 56–3—Nomenclature and clause correlation for optical P2MP systems[a] *(continued)*

Nomenclature	Clause														
	57	60				64	65		66	75	76	77	~~Clause 100~~ 141	~~Clause 101~~ 142	~~Clause 102~~ 143	~~Clause 103~~ 144
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	1000BASE-PX30 PMD	1000BASE-PX40 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX or 10GBASE-PR PMDs	P2MP RS, PCS, PMA, FEC	10G-EPON P2MP MPMC	~~10GPASS-XR~~Nx25GBASE-PQ PMD	~~EPoC~~Nx25GBASE-PQ P2MP ~~RS,~~ PCS, PMA, FEC	~~EPoC PHY Link~~Nx25GBASE-PQ M2MP MCRS	~~EPoC~~Nx25GBASE-PQ P2MP MPMC
~~10GPASS-XR-D~~ 25/10GBASE-PQG-U2	O												M	M	M	M
~~10GPASS-XR-U~~ 25/10GBASE-PQG-U3	O												M	M	M	M
25/10GBASE-PQG-D2	O												M	M	M	M
25/10GBASE-PQG-D3	O												M	M	M	M
25/10GBASE-PQX-U2	O												M	M	M	M
25/10GBASE-PQX-U3	O												M	M	M	M
25/10GBASE-PQX-D2	O												M	M	M	M
25/10GBASE-PQX-D3	O												M	M	M	M
25GBASE-PQG-U2	O												M	M	M	M
25GBASE-PQG-U3	O												M	M	M	M
25GBASE-PQG-D2	O												M	M	M	M
25GBASE-PQG-D3	O												M	M	M	M
25GBASE-PQX-U2	O												M	M	M	M
25GBASE-PQX-U3	O												M	M	M	M
25GBASE-PQX-D2	O												M	M	M	M
25GBASE-PQX-D3	O												M	M	M	M
50/10GBASE-PQG-U2	O												M	M	M	M
50/10GBASE-PQG-U3	O												M	M	M	M
50/10GBASE-PQG-D2	O												M	M	M	M
50/10GBASE-PQG-D3	O												M	M	M	M
50/10GBASE-PQX-U2	O												M	M	M	M
50/10GBASE-PQX-U3	O												M	M	M	M
50/10GBASE-PQX-D2	O												M	M	M	M

Table 56–3—Nomenclature and clause correlation for optical P2MP systems[a] *(continued)*

Nomenclature	Clause														
	57	60				64	65		66	75	76	77	~~Clause 100~~ 141	~~Clause 101~~ 142	~~Clause 102~~ 143	~~Clause 103~~ 144
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	1000BASE-PX30 PMD	1000BASE-PX40 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX or 10GBASE-PR PMDs	P2MP RS, PCS, PMA, FEC	10G-EPON P2MP MPMC	~~10GPASS-XR~~Nx25GBASE-PQ PMD	~~EPoC~~Nx25GBASE-PQ P2MP ~~RS~~, PCS, PMA, FEC	~~EPoC PHY Link~~Nx25GBASE-PQ M2MP MCRS	~~EPoC~~Nx25GBASE-PQ P2MP MPMC
50/10GBASE-PQX-D3	O												M	M	M	M
50/25GBASE-PQG-U2	O												M	M	M	M
50/25GBASE-PQG-U3	O												M	M	M	M
50/25GBASE-PQG-D2	O												M	M	M	M
50/25GBASE-PQG-D3	O												M	M	M	M
50/25GBASE-PQX-U2	O												M	M	M	M
50/25GBASE-PQX-U3	O												M	M	M	M
50/25GBASE-PQX-D2	O												M	M	M	M
50/25GBASE-PQX-D3	O												M	M	M	M
50GBASE-PQX-U2	O												M	M	M	M
50GBASE-PQX-U3	O												M	M	M	M
50GBASE-PQX-D2	O												M	M	M	M
50GBASE-PQX-D3	O												M	M	M	M
50GBASE-PQG-U2	O												M	M	M	M
50GBASE-PQG-U3	O												M	M	M	M
50GBASE-PQG-D2	O												M	M	M	M
50GBASE-PQG-D3	O												M	M	M	M

[a]O = Optional, M = Mandatory

Table 56–4—Nomenclature and clause correlation for coaxial P2MP systems[a]

Nomenclature	Clause				
	57	100	101	102	103
	OAM	10GPASS-XR	EPoC P2MP RS, PCS, PMA, FEC	EPoC PHY-Link	EPoC P2MP MPMC
10GPASS-XR-D	O	M	M	M	M
10GPASS-XR-U	O	M	M	M	M

[a]O = Optional, M = Mandatory

67. System considerations for Ethernet subscriber access networks

67.1 Overview

Change Table 67–1 as follows:

Table 67–1—Characteristics of the various EFM network media segments

Media type	Rate ~~(Mb/s)~~	Number of PHYs per segment	Nominal reach (km)
Optical 100 Mb/s fiber segment (100BASE-LX10, 100BASE-BX10)	100 Mb/s	2	10
Optical 1000 Mb/s fiber segment (1000BASE-LX10, 1000BASE-BX10)	1~~000~~ Gb/s	2	10
Optical 1000 Mb/s P2MP segment (1000BASE-PX10)	1~~000~~ Gb/s[a]	17[b,c]	10
Optical 1000 Mb/s P2MP segment (1000BASE-PX20)		17[b,c]	20
Optical 1000 Mb/s P2MP segment (1000BASE-PX30)		33[b,c]	20
Optical 1000 Mb/s P2MP segment (1000BASE-PX40)		65[b,c]	20
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX10)	~~10 000 / 1000~~ 10 / 1 Gb/s[d]	17[b,c]	10
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX20)		17[b,c]	20
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX30)		33[b,c]	20
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX40)		65[b,c]	20
Optical 10 Gb/s P2MP segment (10GBASE-PR10)	10 ~~000~~Gb/s[e]	17[b,c]	10
Optical 10 Gb/s P2MP segment (10GBASE-PR20)		17[b,c]	20
Optical 10 Gb/s P2MP segment (10/1GBASE-PR30)		33[b,c]	20
Optical 10 Gb/s P2MP segment (10GBASE-PR40)		65[b,c]	20
Copper high-speed segment (10PASS-TS)	10 Mb/s[f]	2	0.75
Copper long reach segment (2BASE-TL)	2 Mb/s[c]	2	2.7
EPoC coaxial segment (10GPASS-XR)	Up to 10 Gb/s downstream	variable[g]	2.9[h]
	Up to 1.6 Gb/s upstream	variable[g]	2.9[h]

Table 67–1—Characteristics of the various EFM network media segments *(continued)*

Media type	Rate ~~(Mb/s)~~	Number of PHYs per segment	Nominal reach (km)
Optical Nx25-EPON P2MP segment (50/50-PQ20*, 50/25-PQ20*, 25/25-PQ20*) [i]	50 / 50 Gb/s [j] 50 / 25 Gb/s 25 / 25 Gb/s	17 [b,c]	20
		33 [b,c]	10
Optical Nx25-EPON P2MP segment (50/10-PQ20*, 25/25-PQ20*) [i]	50 / 10 Gb/s [j] 25 / 10 Gb/s	17 [b,c]	20
		33 [b,c]	10
Optical Nx25-EPON P2MP segment (50/50-PQ30*, 50/25-PQ30*, 25/25-PQ30*) [i]	50 / 50 Gb/s [j] 50 / 25 Gb/s 25 / 25 Gb/s	33 [b,c]	20
Optical Nx25-EPON P2MP segment (50/10-PQ30*, 25/25-PQ30*) [i]	50 / 10 Gb/s [j] 25 / 10 Gb/s	33 [b,c]	20

[a] 1~~000~~ ~~M~~Gb/s in downstream direction, 1~~000~~ ~~M~~Gb/s in upstream direction.
[b] P2MP segments may be implemented with a trade off between link span and split ratio listed. Refer to 67.2.1.
[c] The number of PHYs in the P2MP segment includes the OLT PHY.
[d] 10~~-000~~ ~~M~~Gb/s in downstream direction, 1~~000~~ ~~M~~Gb/s in upstream direction (asymmetric data rate in 10/1G-EPON).
[e] 10~~-000~~ ~~M~~Gb/s in downstream direction, 10~~-000~~ ~~M~~Gb/s in upstream direction (symmetric data rate in 10/10G-EPON).
[f] Nominal rate stated at the nominal reach in this table. Rate and reach can vary depending on the plant. For 2BASE-TL please refer to Annex 63B for more information. For 10PASS-TS, please refer to Annex 62A for more information.
[g] Based on the cable operator's CCDN configuration, the number of PHYs will be the CLT PHY plus each CNU PHY.
[h] Maximal differential distance between CNUs. Reach may vary depending on the CCDN.
[i] For brevity, the two Nx25G-EPON PMD coexistence class designators "X" and "G" have been abbreviated in this table with an asterisk ("*") as they are equivalent with respect to rate, number of PHYs per segment, and nominal reach (see 141.1.3 and 141.2.5).
[j] For Nx25G-EPON possible downstream rates are either 25 Gb/s or 50 Gb/s and possible upstream rates are 10 Gb/s, 25 Gb/s, or 50 Gb/s. The format shown in the table is the downstream rate followed by a forward slash ("/") followed by the upstream rate (see 141.2.2).

Insert new Clause 141, Clause 142, Clause 143, and Clause 144 as follows:

141. Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks

141.1 Overview

This clause describes the Physical Medium Dependent (PMD) sublayer for Nx25G Ethernet passive optical networks (Nx25G-EPON) operating at a MAC data rate of 25 Gb/s or 50 Gb/s in the downstream direction and a MAC data rate of 10 Gb/s, 25 Gb/s, or 50 Gb/s in the upstream direction. These PMDs are collectively referred to by the term Nx25G-EPON. All Nx25G-EPON PMDs supporting the downstream MAC data rate of 50 Gb/s are collectively referred to as 50G-EPON PMDs while Nx25G-EPON PMDs supporting the downstream MAC data rate of 25 Gb/s are collectively referred to as 25G-EPON PMDs.

141.1.1 Terminology

Nx25G-EPON operates over a point-to-multipoint (P2MP) topology, also called a tree or trunk-and-branch topology. The device connected at the root of the tree is called an optical line terminal (OLT) and the devices connected as the leaves are referred to as optical network units (ONUs). The direction of transmission from the OLT to ONUs is referred to as the downstream direction, while the direction of transmission from the ONU to the OLT is referred to as the upstream direction.

141.1.2 Positioning of the PMD sublayer within the IEEE 802.3 architecture

Figure 141–1 depicts the relationships of Nx25G-EPON PMD sublayers (shown hatched) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

141.1.3 PHY link types

Characteristics of Nx25G-EPON PHY link types are summarized in Table 141–1 through Table 141–5. The indicated characteristics of PHY link types are the results of specific pairings of an OLT PMD and an ONU PMD. The supported PMD pairs are specified in Table 141–8 and Table 141–9. Nx25G-EPON PHY link types supporting 50 Gb/s use wavelength division multiplexing on two wavelengths and hence two wavelengths are listed for these links in Table 141–1 through Table 141–5.

Table 141–1—PHY links supporting 25 Gb/s downstream and 10 Gb/s upstream

Description	25/10-PQ20G	25/10-PQ20X	25/10-PQ30G	25/10-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	10.3125				GBd
Downstream wavelength	1358 ± 2				nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

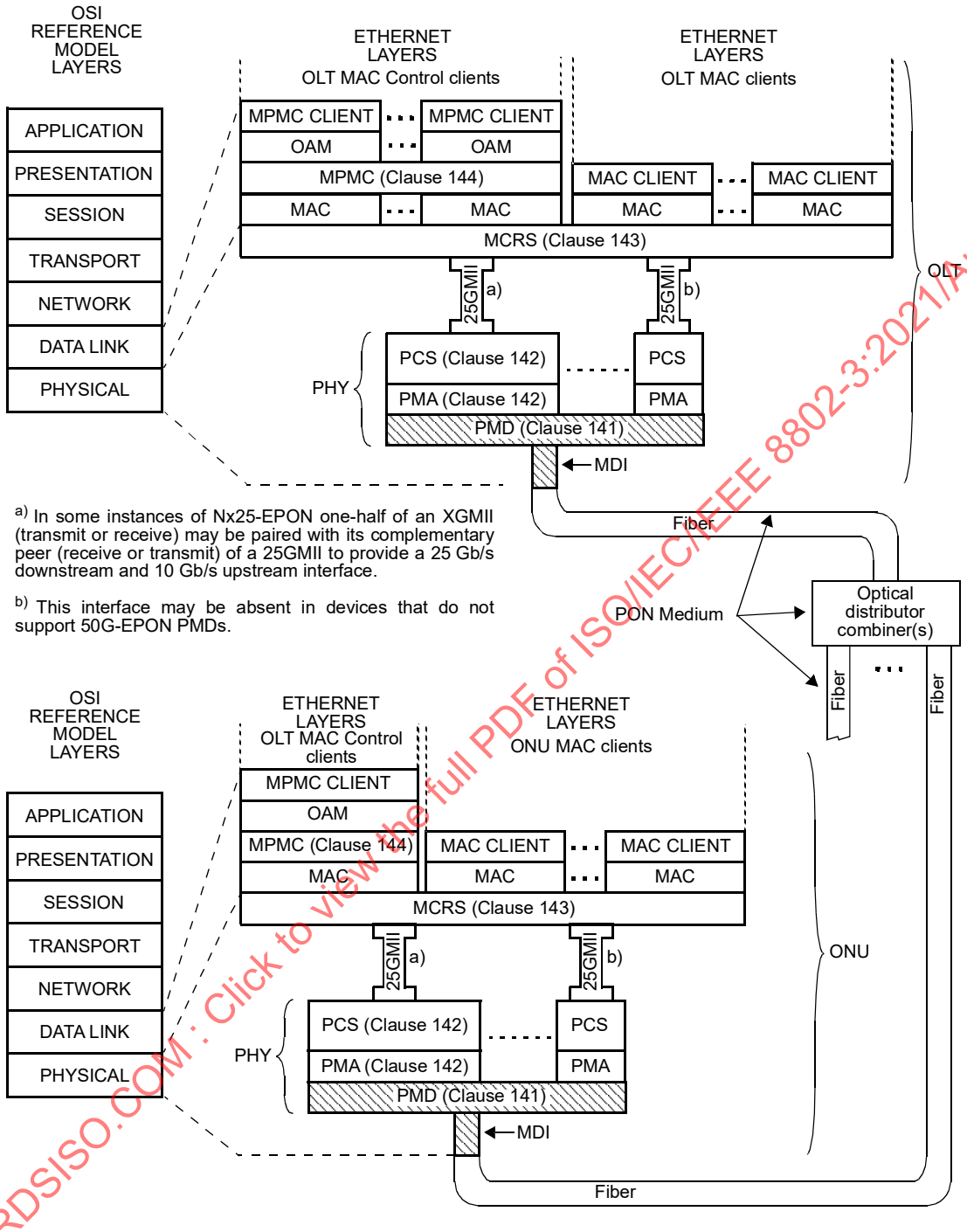


Figure 141–1—Relationship of Nx25G-EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

Table 141–2—PHY links supporting 25 Gb/s downstream and 25 Gb/s upstream

Description	25/25-PQ20G	25/25-PQ20X	25/25-PQ30G	25/25-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	25.78125				GBd
Downstream wavelength	1358 ± 2				nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

Table 141–3—PHY links supporting 50 Gb/s downstream and 10 Gb/s upstream

Description	50/10-PQ20G	50/10-PQ20X	50/10-PQ30G	50/10-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	10.3125				GBd
Downstream wavelength	1358 ± 2 1342 ± 2				nm nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

Table 141–4—PHY links supporting 50 Gb/s downstream and 25 Gb/s upstream

Description	50/25-PQ20G	50/25-PQ20X	50/25-PQ30G	50/25-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	25.78125				GBd
Downstream wavelength	1358 ± 2 1342 ± 2				nm nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

Table 141–5—PHY links supporting 50 Gb/s downstream and 50 Gb/s upstream

Description	50/50-PQ20G	50/50-PQ20X	50/50-PQ30G	50/50-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	25.78125				GBd
Downstream wavelength	1358 ± 2 1342 ± 2				nm nm
Upstream wavelength	1270 ± 10 1300 ± 10	1300 ± 10 1320 ± 2	1270 ± 10 1300 ± 10	1300 ± 10 1320 ± 2	nm nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	N/A	10G-EPON	N/A	10G-EPON	—

141.2 PMD nomenclature

141.2.1 Introduction

Nx25G-EPON PMDs are classified based on transmit and receive rate, coexistence type, transmission direction, and power level.

141.2.2 PMD rate classes

Nx25G-EPON PMDs defined in this clause fall into several rate classes depending on the upstream and downstream aggregate rate supported. Possible downstream rates are either 25 Gb/s or 50 Gb/s. Possible upstream rates are 10 Gb/s, 25 Gb/s, or 50 Gb/s. The rate(s) at which a PMD operates is indicated in the PMD name.

141.2.3 PMD coexistence classes

Nx25G-EPON PMDs defined in this clause support WDM coexistence with 10G-EPON or GPON. PMDs coexisting with 10G-EPON are denoted with the letter X in the PMD name while PMDs coexisting with GPON are denoted with the letter G.

141.2.4 PMD transmission direction classes

Nx25G-EPON PMDs defined in this clause are defined for either the OLT and face the downstream direction or for the ONU and face the upstream direction. OLT PMDs are denoted with the letter D in the PMD name while ONU PMDs are denoted with the letter U.

141.2.5 PMD power classes

Nx25G-EPON PMDs defined in this clause are defined as being in one of two power classes (a power class is a differentiator for PMD specifications based of their launch powers and sensitivities); the medium or the high power budget class:

— The medium PMD power class supports a P2MP media channel insertion loss of ≤ 24 dB e.g., a PON with a split ratio of 1:16 and the distance of 20 km or a PON with a split ratio of 1:32 and the distance of 10 km.

— The high PMD power class supports a P2MP media channel insertion loss of ≤ 29 dB e.g., a PON with a split ratio of 1:32 and the distance of 20 km.

The medium PMD power class is indicated in the PMD name with the numeral 2 while the high PMD power class is indicated with the numeral 3.

141.2.6 PMD naming

Nx25G-EPON PMD naming conforms to the following semantic convention, with individual elements shown in Table 141–6:

r_1/r_2GBASE-PQc-db

Table 141–6—PMD naming elements

Parameter	Description	Allowed values
r_1	PMD downstream rate class (see 141.2.2)	25, 50
r_2[a]	PMD upstream rate class (see 141.2.2)	10, 25, 50
G	PMDs operate at Gb/s rates	
BASE		
P	PMD for PON (P2MP media)	
Q	256B/257B line code	
c	Coexistence class (see 141.2.3)	G, X
d	Transmission direction class (see 141.2.4)	D, U
b	Power class (see 141.2.5)	2, 3

[a]If r_1 is equal to r_2 (i.e., symmetric-data rate PMDs), r_2 is omitted.

141.2.7 Supported combinations of OLT and ONU PMDs

The PHY link power budget (a power budget is a characteristic of a link type and depends on the paired PMDs' transmitter launch powers and receiver sensitivities) is determined by the PMDs located at the ends of the physical media. This subclause describes how OLT (D type) and ONU (U type) PMDs may be combined to achieve the power budgets listed in Table 141–1 through Table 141–5. Table 141–7 shows the list of all supported PMD types. Connection between G and X coexistence type PMDs is not supported, e.g., 25/10GBASE-PQG-D2 OLT PMD is not interoperable with 25/10GBASE-PQX-U2 due to non-overlapping OLT receiver sensitivity window and ONU transmitter wavelength range.

Table 141–7—List of supported PMD types

Upstream/ Downstream MAC data rate	Downstream wavelengths[a]	Upstream wavelengths[b]	OLT PMDs	ONU PMDs
25G/10G	DW0	UW0	25/10GBASE-PQG-D2 25/10GBASE-PQG-D3	25/10GBASE-PQG-U2 25/10GBASE-PQG-U3
	DW0	UW1	25/10GBASE-PQX-D2 25/10GBASE-PQX-D3	25/10GBASE-PQX-U2 25/10GBASE-PQX-U3
25G/25G	DW0	UW0	25GBASE-PQG-D2 25GBASE-PQG-D3	25GBASE-PQG-U2 25GBASE-PQG-U3
	DW0	UW1	25GBASE-PQX-D2 25GBASE-PQX-D3	25GBASE-PQX-U2 25GBASE-PQX-U3

Table 141–7—List of supported PMD types *(continued)*

Upstream/ Downstream MAC data rate	Downstream wavelengths[a]	Upstream wavelengths[b]	OLT PMDs	ONU PMDs
50G/10G	DW0 + DW1	UW0	50/10GBASE-PQG-D2 50/10GBASE-PQG-D3	50/10GBASE-PQG-U2 50/10GBASE-PQG-U3
	DW0 + DW1	UW1	50/10GBASE-PQX-D2 50/10GBASE-PQX-D3	50/10GBASE-PQX-U2 50/10GBASE-PQX-U3
50G/25G	DW0 + DW1	UW0	50/25GBASE-PQG-D2 50/25GBASE-PQG-D3	50/25GBASE-PQG-U2 50/25GBASE-PQG-U3
	DW0 + DW1	UW1	50/25GBASE-PQX-D2 50/25GBASE-PQX-D3	50/25GBASE-PQX-U2 50/25GBASE-PQX-U3
50G/50G	DW0 + DW1	UW0 + UW1	50GBASE-PQG-D2 50GBASE-PQG-D3	50GBASE-PQG-U2 50GBASE-PQG-U3
	DW0 + DW1	UW1 + UW2	50GBASE-PQX-D2 50GBASE-PQX-D3	50GBASE-PQX-U2 50GBASE-PQX-U3

[a]Downstream wavelengths are defined in Table 141–13.
[b]Upstream wavelengths are defined in Table 141–14.

141.2.7.1 PHY Links supporting medium power budget

Table 141–8 illustrates pairings of OLT PMDs with ONU PMDs to achieve the medium power budgets as shown in Table 141–1 through Table 141–5.

Table 141–8—Supported combinations of OLT and ONU PMDs and the resulting PHY link types, medium power budget[a]

		ONU PMD				
		25/10GBASE-PQ*-U2	50/10GBASE-PQ*-U2	25GBASE-PQ*-U2	50/25GBASE-PQ*-U2	50GBASE-PQ*-U2
OLT PMD	25/10GBASE-PQ*-D2	25/10-PQ20	25/10-PQ20	N/A		
	50/10GBASE-PQ*-D2	25/10-PQ20	50/10-PQ20			
	25GBASE-PQ*-D2	N/A		25/25-PQ20	25/25-PQ20	25/25-PQ20
	50/25GBASE-PQ*-D2			25/25-PQ20	50/25-PQ20	50/25-PQ20
	50GBASE-PQ*-D2			25/25-PQ20	50/25-PQ20	50/50-PQ20

[a](*) - On an ODN, OLT and ONU PMDs support the same coexistence mode, either X or G.

141.2.7.2 PHY Links supporting high power budget

Table 141–9 illustrates pairings of OLT PMDs with ONU PMDs to achieve the high power budgets as shown in Table 141–1 through Table 141–5.

Table 141–9—Supported combinations of OLT and ONU PMDs and the resulting PHY link types, high power budget[a]

		ONU PMD				
		25/10GBASE-PQ*-U3	50/10GBASE-PQ*-U3	25GBASE-PQ*-U3	50/25GBASE-PQ*-U3	50GBASE-PQ*-U3
OLT PMD	25/10GBASE-PQ*-D3	25/10-PQ30	25/10-PQ30	N/A		
	50/10GBASE-PQ*-D3	25/10-PQ30	50/10-PQ30			
	25GBASE-PQ*-D3	N/A		25/25-PQ30	25/25-PQ30	25/25-PQ30
	50/25GBASE-PQ*-D3			25/25-PQ30	50/25-PQ30	50/25-PQ30
	50GBASE-PQ*-D3			25/25-PQ30	50/25-PQ30	50/50-PQ30

[a](*) - On an ODN, OLT and ONU PMDs support the same coexistence mode, either X or G.

141.3 PMD functional specifications

The Nx25G-EPON PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

141.3.1 PMD service interface

The following specifies the services provided by Nx25G-EPON PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD service interface supports the exchange of a continuous stream of bits between the PMA[*i*] and PMD entities. The PMD translates the serialized data received from the compatible PMA to and from signals suitable for the specified medium. The following primitives are defined:

— PMD_UNITDATA[*i*].request
— PMD_UNITDATA[*i*].indication
— PMD_SIGNAL[*i*].request
— PMD_SIGNAL[*i*].indication

where "[*i*]" represents the PMA Channel: 0 or 1.

141.3.1.1 Channel-to-wavelength mapping

An Nx25G-EPON PMD provides multiple instances of the PMD service interface that connect to multiple PMA channels (see 142.4.1). Within the PMD sublayer, each instance of the PMD service interface maps to a specific pair of wavelengths. This mapping is different for the two coexistence classes, and shall be as defined in Table 141–10 for the OLT and in Table 141–11 for the ONU.

Table 141–10—OLT Channel-to-wavelength mapping

PMA channel	PMD service primitives	Wavelength (coexistence class G)	Wavelength (coexistence class X)
0	PMD_UNITDATA[0].request PMD_SIGNAL[0].request	DW0	DW0
	PMD_UNITDATA[0].indication PMD_SIGNAL[0].indication	UW0	UW1
1	PMD_UNITDATA[1].request PMD_SIGNAL[1].request	DW1	DW1
	PMD_UNITDATA[1].indication PMD_SIGNAL[1].indication	UW1	UW2

Table 141–11—ONU Channel-to-wavelength mapping

PMA channel	PMD service primitives	Wavelength (coexistence class G)	Wavelength (coexistence class X)
0	PMD_UNITDATA[0].request PMD_SIGNAL[0].request	UW0	UW1
	PMD_UNITDATA[0].indication PMD_SIGNAL[0].indication	DW0	DW0
1	PMD_UNITDATA[1].request PMD_SIGNAL[1].request	UW1	UW2
	PMD_UNITDATA[1].indication PMD_SIGNAL[1].indication	DW1	DW1

141.3.1.2 Delay constraints

The Nx25G-EPON PMD delay variation within the PMD shall be less than 0.25 EQT (see 1.4.245c).

141.3.1.3 PMD_UNITDATA[*i*].request

This primitive defines the transfer of a serial data stream from the PMA defined in 142.4 to the PMD.

The semantics of the service primitive are PMD_UNITDATA[*i*].request(tx_bit) (where $i = 0$ or 1). The data conveyed by PMD_UNITDATA[*i*].request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO. The PMA defined in 142.4 continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling rate of 25.78125 GBd in the case of Nx25G-EPON OLT and ONU PMDs. The PMA defined in 142.4 continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling rate of 10.3125 GBd in the case of 25/10G-EPON and 50/10G–EPON ONU PMDs. Upon the receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

141.3.1.4 PMD_UNITDATA[*i*].indication

This primitive defines the transfer of data from the PMD to the PMA defined in 142.4.

The semantics of the service primitive are PMD_UNITDATA[*i*].indication(rx_bit) (where *i* = 0 or 1). The data conveyed by PMD_UNITDATA[*i*].indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the PMA defined in 142.4 corresponding to the signals received from the MDI, at the nominal signaling rate of 25.78125 GBd in the case of Nx25G–EPON OLT and ONU PMDs or to the PMA defined in 142.4 at the nominal signaling rate of 10.3125 GBd in the case of 25/10G–EPON and 50/10G-EPON OLT PMDs.

141.3.1.5 PMD_SIGNAL[*i*].request

In the upstream direction, this primitive is generated by the PMA defined in 142.4 to turn on and off the transmitter according to the granted time. A signal for laser control is generated as described in 142.2.5.4.3 for the PCS defined in 142.2.

The semantics of the service primitive are PMD_SIGNAL[*i*].request(tx_enable) (where *i* = 0 or 1). The tx_enable parameter can take on one of two values: ENABLE or DISABLE, determining whether the PMD transmitter is on (enabled) or off (disabled). The PMA defined in 142.4 generates this primitive to indicate a change in the value of tx_enable. Upon the receipt of this primitive, the PMD turns the transmitter on or off as appropriate.

141.3.1.6 PMD_SIGNAL[*i*].indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI. The semantics of the service primitive are PMD_SIGNAL[*i*].indication(SIGNAL_DETECT) (where *i* = 0 or 1). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA[*i*].indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA[*i*].indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio. PMD_SIGNAL[*i*].indication(SIGNAL_DETECT) has different characteristics for upstream and downstream links, see 141.3.5.

141.3.2 PMD block diagram

The PMD sublayer is defined at the reference points shown in Figure 141–2 for Nx25G-EPON PMDs. For any indexed test point (e.g., TP1[*i*]), [*i*] indicates the channel index, where *i* = 0 or 1.

For Nx25G-EPON PMDs, test points TP1[*i*], TP2, TP3, and TP4[*i*] refer to the downstream channel, while test points TP5[*i*], TP6, TP7, and TP8[*i*] refer to the upstream channel. In the downstream channel, TP2 and TP3 are compliance points, while in the upstream channel TP6 and TP7 are compliance points. TP1[*i*], TP4[*i*], TP5[*i*], and TP8[*i*] are reference points for use by implementers, defined on a per-channel basis. The optical transmit signal is defined at the output end of a patch cord (TP2 for the downstream channel and TP6 for the upstream channel), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 141.7 are made at TP2 or TP6. The optical receive signal is defined at the output of the fiber optic cabling (TP3 for the downstream channel and TP7 for the upstream channel) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 141.7 are made at TP3 or TP7.

The electrical specifications of the PMD service interface (TP1[*i*] and TP4[*i*] for the downstream channel and TP5[*i*] and TP8[*i*] for the upstream channel) are not system compliance points (these are not readily testable in a system implementation).

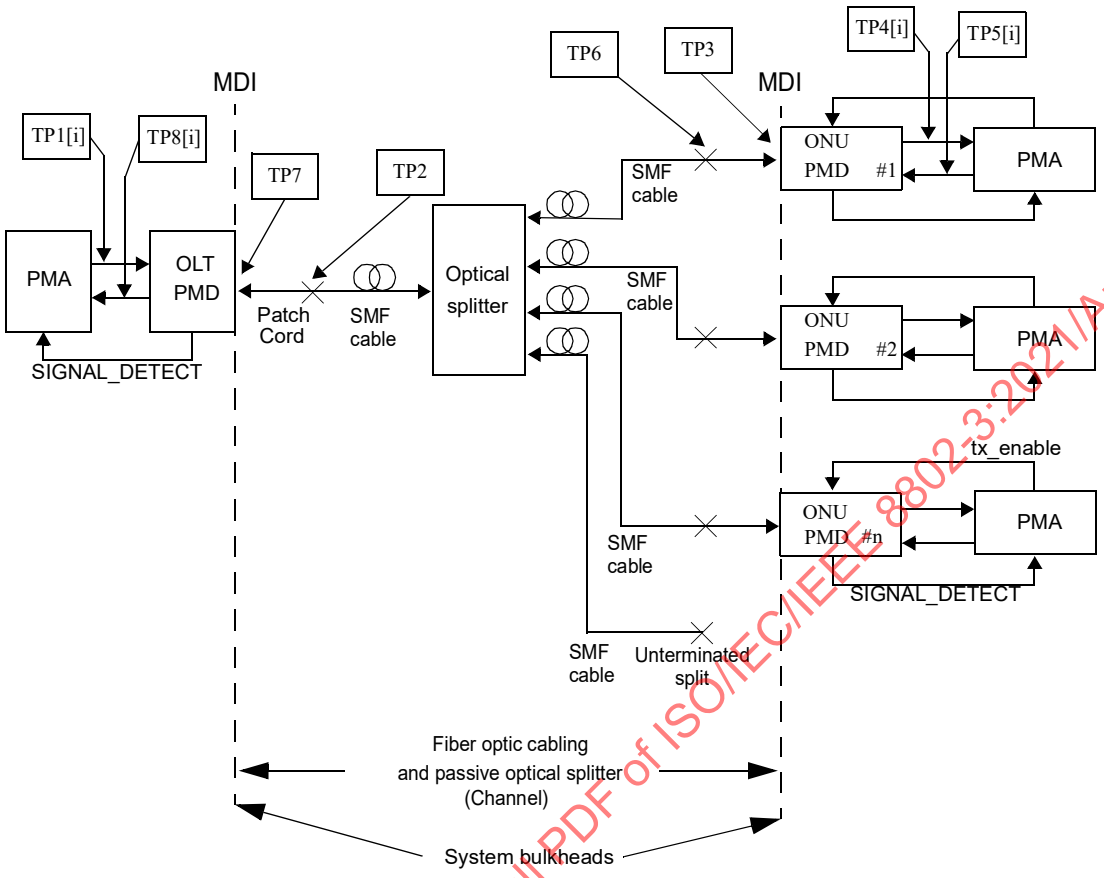


Figure 141–2—Nx25G-EPON PMD test points

141.3.3 PMD transmit function

The PMD transmit function shall convey the bits requested by the PMD service interface primitive PMD_UNITDATA[*i*].request(tx_bit) to the MDI according to the optical specifications in this clause. In the upstream direction, the flow of bits is interrupted according to PMD_SIGNAL[*i*].request(tx_enable). This implies three optical levels, 1, 0, and dark, the latter corresponding to the transmitter being in the OFF state. The highest optical power level shall correspond to tx_bit = ONE.

141.3.4 PMD receive function

The PMD receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the primitive PMD_UNITDATA[*i*].indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

141.3.5 PMD signal detect function

141.3.5.1 ONU PMD signal detect

The PMD signal detect function for the continuous mode downstream signal shall report to the PMD service interface, using the primitive PMD_SIGNAL[*i*].indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL[*i*].indication is intended to be an indicator of the presence of the optical

signal. The ONU PMD receiver is not required to verify whether a compliant Nx25G-EPON signal is being received.

141.3.5.2 OLT PMD signal detect

The response time for the PMD signal detect function for the burst mode upstream signal may be longer or shorter than a burst length; thus, it may not fulfill the traditional requirements placed on signal detect. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. The signal detect function in the OLT may be realized in the PMD or the PMA defined in 142.4. The OLT PMD receiver is not required to verify whether a compliant Nx25G-EPON signal is being received.

141.3.5.3 Nx25G-EPON signal detect functions

The value of the SIGNAL_DETECT parameter for Nx25G–EPON PMDs shall be generated according to the conditions defined in Table 141–12.

Table 141–12—SIGNAL_DETECT value definitions for Nx25G-EPON PMDs

PMD type	Receive conditions	SIGNAL_DETECT value
Nx25G-EPON PMD	Average input optical power ≤ Signal detect threshold (min) in Table 141–17 or Table 141–18 at the specified receiver wavelength, as applicable	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 141–17 or Table 141–18 with a compliant signal input at the specified receiver wavelength, as applicable	OK
	All other conditions	Unspecified

141.4 Wavelength allocation

Downstream wavelength assignments are defined in Table 141–13. Upstream wavelength assignments are defined in Table 141–14.

Table 141–13—Downstream wavelength assignments

Wavelength name	Center wavelength (nm)	Wavelength range (nm)
DW0	1358	± 2
DW1	1342	± 2

Table 141–14—Upstream wavelength assignments

Wavelength name	Center wavelength (nm)	Wavelength range (nm)
UW0	1270	± 10
UW1	1300	± 10
UW2	1320	± 2

141.5 PMD to MDI optical specifications for OLT PMDs

This subclause details the PMD to MDI optical specifications for OLT PMDs. Specifically, 141.5.1 defines the OLT transmit parameters, while 141.5.2 defines the OLT receive parameters.

The operating parameters for Nx25G-EPON PHY link types are defined in Table 141–1 through Table 141–5. An Nx25G-EPON compliant transceiver operates over the media meeting the dispersion shown in Table 141–23 according to the specifications described in 141.9. A transceiver that exceeds the maximum reach requirement while meeting all other optical specifications is considered compliant.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

141.5.1 Transmitter optical specifications

A medium power class Nx25G-EPON OLT PMD transmitter shall comply with the parameters shown in Table 141–15. A high power class Nx25G-EPON OLT PMD transmitter shall comply with the parameters shown in Table 141–16.

141.5.2 Receiver optical specifications

A medium power class Nx25G-EPON OLT PMD receiver shall comply with the parameters shown in Table 141–17. A high power class Nx25G-EPON OLT PMD receiver shall comply with the parameters shown in Table 141–18.

Table 141–15—OLT transmit characteristics, medium power class

Parameter	25/10GBASE-PQG-D2 25/10GBASE-PQX-D2 25GBASE-PQG-D2 25GBASE-PQX-D2	50/10GBASE-PQG-D2 50/10GBASE-PQX-D2 50/25GBASE-PQG-D2 50/25GBASE-PQX-D2 50GBASE-PQG-D2 50GBASE-PQX-D2	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Channel wavelength ranges	1356 to 1360	1356 to 1360 1340 to 1344	nm
Side-mode suppression ratio (SMSR) (min)	30		dB
Total average launch power (max)	—	8	dBm
Average launch power, each channel (max)	5		dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	2.6		dBm
Difference in launch power between any two channels (OMA) (max)	—	3	dB
Launch power in OMA minus TDP, each channel (min)[b] for extinction ratio ≥ 9 dB for extinction ratio < 9 dB	 2 2.1		 dBm dBm
Transmitter and dispersion penalty (TDP), each channel (max)	1.5		dB
Average launch power of OFF transmitter, each channel (max)	–39		dBm
Extinction ratio (min)	8		dB
$RIN_{15}OMA$ (max)	–128		dB/Hz
Optical return loss tolerance (max)	15		dB
Transmitter reflectance[c] (max)	–10		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[d]	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		UI

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 2 dBm. This minimum average launch power value is informative only.
[c] Transmitter reflectance is defined looking into the transmitter.
[d] As defined in Figure 86–4.

Table 141–16—OLT transmit characteristics, high power class

Parameter	25/10GBASE-PQG-D3 25/10GBASE-PQX-D3 25GBASE-PQG-D3 25GBASE-PQX-D3	50/10GBASE-PQG-D3 50/10GBASE-PQX-D3 50/25GBASE-PQG-D3 50/25GBASE-PQX-D3 50GBASE-PQX-D3 50GBASE-PQG-D3	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Channel wavelength ranges	1356 to 1360	1356 to 1360 1340 to 1344	nm
Side-mode suppression ratio (SMSR) (min)	30		dB
Total average launch power (max)	—	10.8	dBm
Average launch power, each channel (max)	7.8		dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	4.9		dBm
Difference in launch power between any two channels (OMA) (max)	—	3	dB
Launch power in OMA minus TDP, each channel (min)[b] for extinction ratio ≥ 9 dB for extinction ratio < 9 dB	 4.8 4.9		 dBm dBm
Transmitter and dispersion penalty (TDP), each channel (max)	1.5		dB
Average launch power of OFF transmitter, each channel (max)	–39		dBm
Extinction ratio (min)	8		dB
RIN15OMA (max)	–128		dB/Hz
Optical return loss tolerance (max)	15		dB
Transmitter reflectance[c] (max)	–10		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[d]	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		UI

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 4.8 dBm. This minimum average launch power value is informative only.
[c] Transmitter reflectance is defined looking into the transmitter.
[d] As defined in Figure 86–4.

Table 141–17—OLT receive characteristics, medium power class

Parameter	25GBASE-PQG-D2 50/25GBASE-PQG-D2	25GBASE-PQX-D2 50/25GBASE-PQX-D2	50GBASE-PQG-D2	50GBASE-PQX-D2	25/10GBASE-PQG-D2 50/10GBASE-PQG-D2	25/10GBASE-PQX-D2 50/10GBASE-PQX-D2	Unit
Signaling rate (range)	25.78125 ± 100 ppm				See Table 75–6[a]		GBd
Channel wavelengths (range)	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322	See Table 75–6[a]	1290 to 1310	nm
Bit error ratio (max)[b]	10^{-2}						—
Damage threshold[c]	–2				See Table 75–6[a]		dBm
Average receive power, each channel (max)	–3						dBm
Receiver reflectance (max)	–12						dB
Receiver sensitivity (OMA), each channel[d] (max)	–22.7						dBm
Signal detect threshold, each channel (min)	–40						dBm
Stressed receiver sensitivity (OMA), each channel[e] (max)	–21.2						dBm
Receiver settling time (max)	800						ns
Conditions of stressed receiver sensitivity test:							
Vertical eye closure penalty,[f] each channel	2				See Table 75–6[a]		dB
Stressed eye J2 Jitter,[e,f] each channel	0.3				—		UI
Stressed eye J9 Jitter,[e,f] each channel	0.47				—		UI

[a] Individual 10G-EPON PMD parameters are reused without change at a higher pre-FEC bit error ratio shown in Table 141–17.
[b] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[c] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level.
[d] Receiver sensitivity (OMA), each channel (max) is informative and is defined for a transmitter with VECP = 0.5 dB. For reference, this implies that the maximum average power unstressed receiver sensitivity measured with an ideal transmitter signal at minimum extinction ratio is –22 dBm. This value is informative only.
[e] Measured with conformance test signal at TP3 (see 141.7.11) for BER = 10^{-2}.
[f] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Table 141–18—OLT receive characteristics, high power class

Parameter	25GBASE-PQG-D3 50/25GBASE-PQG-D3	25GBASE-PQX-D3 50/25GBASE-PQX-D3	50GBASE-PQG-D3	50GBASE-PQX-D3	25/10GBASE-PQG-D3 50/10GBASE-PQG-D3	25/10GBASE-PQX-D3 50/10GBASE-PQX-D3	Unit
Signaling rate (range)	25.78125 ± 100 ppm				See Table 75–6[a]		GBd
Channel wavelength ranges	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322	See Table 75–6[a]	1290 to 1310	nm
Bit error ratio (max)[b]	10^{-2}						—
Damage threshold[c]	–5				See Table 75–6[a]		dBm
Average receive power, each channel (max)	–6				—		dBm
Receiver reflectance (max)	–12				See Table 75–6[a]		dB
Receiver sensitivity (OMA), each channel[d] (max)	–24.3						dBm
Signal detect threshold, each channel (min)	–40						dBm
Stressed receiver sensitivity (OMA), each channel[e] (max)	–22.8						dBm
Receiver settling time (max)	800						ns
Conditions of stressed receiver sensitivity test:							
Vertical eye closure penalty,[f] each channel	2				See Table 75–6[a]		dB
Stressed eye J2 Jitter,[e,f] each channel	0.3				—		UI
Stressed eye J9 Jitter,[e,f] each channel	0.47				—		UI

[a] Individual 10G-EPON PMD parameters are reused without change at a higher pre-FEC bit error ratio shown in Table 141–17.
[b] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[c] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level. Direct ONU–OLT connection may result in damage of the receiver.
[d] Receiver sensitivity (OMA) is measured with a signal with VECP = 0.5 dB and is informative. For reference, this implies that the maximum average power unstressed receiver sensitivity measured with an ideal transmitter signal at minimum extinction ratio is –25 dBm. This value is informative only.
[e] Measured with conformance test signal at TP7 (see 141.7.11) for BER = 10^{-2}.
[f] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

141.6 PMD to MDI optical specifications for ONU PMDs

This subclause details the PMD to MDI optical specifications for ONU PMDs. Specifically, 141.6.1 defines the ONU transmit parameters, while 141.6.2 defines the ONU receive parameters.

The operating parameters for Nx25G-EPON PHY link types are defined in Table 141–1 through Table 141–5. An Nx25G-EPON compliant transceiver operates over the media meeting the dispersion shown in Table 141–23 according to the specifications described in 141.9. A transceiver that exceeds the maximum reach requirement while meeting all other optical specifications is considered compliant.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

141.6.1 Transmitter optical specifications

A medium power class Nx25G-EPON ONU PMD transmitter shall comply with the parameters shown in Table 141–19. A high power class Nx25G-EPON ONU PMD transmitter shall comply with the parameters shown in Table 141–20.

Table 141–19—ONU transmit characteristics, medium power class

Parameter	25GBASE-PQG-U2 50/25GBASE-PQG-U2	25GBASE-PQX-U2 50/25GBASE-PQX-U2	50GBASE-PQG-U2	50GBASE-PQX-U2	25/10GBASE-PQG-U2 50/10GBASE-PQG-U2 25/10GBASE-PQX-U2 50/10GBASE-PQX-U2	Unit
Signaling rate (range)	25.78125 ± 100 ppm				See Table 75–8	GBd
Channel wavelengths (range)	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322		nm
Side-mode suppression ratio (SMSR) (min)	30					dB
Total average launch power (max)	—		10			dBm
Average launch power, each channel (max)	7					dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	1.3					dBm
Difference in launch power between any two channels (OMA) (max)	—		3			dB
Launch power in OMA minus TDP, each channel (min)[b] for extinction ratio ≥ 5.5 dB for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	0.2 0.5 0.8					dBm
Transmitter and dispersion penalty (TDP), each channel (max)	2					dB
Average launch power of OFF transmitter, each channel (max)	–45					dBm
Extinction ratio (min)	3.5					dB
$RIN_{15}OMA$ (max)	–128					dB/Hz
Optical return loss tolerance (max)	15					dB
Transmitter reflectance[c] (max)	–10					dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[d]	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}					UI
Turn-on time (max)	128					ns
Turn-off time (max)	128					ns

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 4 dBm. This minimum average launch power value is informative only.
[c] Transmitter reflectance is defined looking into the transmitter.
[d] As defined in Figure 86–4.

Table 141–20—ONU transmit characteristics, high power class

Parameter	25GBASE-PQG-U3 50/25GBASE-PQG-U3	25GBASE-PQX-U3 50/25GBASE-PQX-U3	50GBASE-PQ22G-U3	50GBASE-PQ22X-U3	Unit
Signaling rate (range)	25.78125 ± 100 ppm				GBd
Channel wavelength ranges	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322	nm
Side-mode suppression ratio (SMSR) (min)	30				dB
Total average launch power (max)	—		12		dBm
Average launch power, each channel (max)	9				dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	4.7				dBm
Difference in launch power between any two channels (OMA) (max)	—		3		dB
Launch power in OMA minus TDP, each channel (min)[b] for extinction ratio ≥ 6 dB for extinction ratio < 6 dB	4 4.2				dBm
Transmitter and dispersion penalty (TDP), each channel (max)	2				dB
Average launch power of OFF transmitter, each channel (max)	–45				dBm
Extinction ratio (min)	5				dB
$RIN_{15}OMA$ (max)	–128				dB/Hz
Optical return loss tolerance (max)	15				dB
Transmitter reflectance[c] (max)	–10				dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[d]	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				UI
Turn-on time (max)	128				ns
Turn-off time (max)	128				ns

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 6 dBm. This minimum average launch power value is informative only.
[c] Transmitter reflectance is defined looking into the transmitter.
[d] As defined in Figure 86–4.

141.6.2 Receiver optical specifications

A medium power class Nx25G-EPON ONU PMD receiver shall comply with the parameters shown in Table 141–21. A high power class Nx25G-EPON ONU PMD receiver shall comply with the parameters shown in Table 141–22.

Table 141–21—ONU receive characteristics, medium power class

Parameter	25/10GBASE-PQG-U2 25/10GBASE-PQX-U2 25GBASE-PQG-U2 25GBASE-PQX-U2	50/10GBASE-PQG-U2 50/10GBASE-PQX-U2 50/25GBASE-PQG-U2 50/25GBASE-PQX-U2 50GBASE-PQX-U2 50GBASE-PQG-U2	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Channel wavelengths (range)	1356 to 1360	1356 to 1360 1340 to 1344	nm
Bit error ratio (max)[a]	10^{-2}		—
Damage threshold[b]	–4		dBm
Average receive power, each channel (max)	–5		dBm
Receiver reflectance (max)	–12		dB
Receiver sensitivity (OMA), each channel[c] (max)	–21.4		dBm
Detect threshold, each channel (min)	–40		dBm
Stressed receiver sensitivity (OMA), each channel[d] (max)	–20.4		dBm
Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty,[e] each channel	1.5		dB
Stressed eye J2 Jitter,[e] each channel	0.3		UI
Stressed eye J9 Jitter,[e] each channel	0.47		UI

[a] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[b] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level.
[c] Receiver sensitivity (OMA), each channel (max) is informative and is defined for a transmitter with VECP = 0.5 dB. For reference, this implies that the maximum average power unstressed receiver sensitivity measured with an ideal transmitter signal at minimum extinction ratio is –23.5 dBm. This value is informative only.
[d] Measured with conformance test signal at TP3 (see 141.7.11) for BER = 10^{-2}.
[e] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Table 141–22—ONU receive characteristics, high power class

Parameter	25/10GBASE-PQG-U3 25/10GBASE-PQX-U3 25GBASE-PQG-U3 25GBASE-PQX-U3	50/10GBASE-PQG-U3 50/10GBASE-PQX-U3 50/25GBASE-PQG-U3 50/25GBASE-PQX-U3 50GBASE-PQX-U3 50GBASE-PQG-U3	Unit
Channel wavelength ranges	1356 to 1360	1356 to 1360 1340 to 1344	nm
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Bit error ratio (max)[a]	10^{-2}		—
Damage threshold[b]	–6.2		dBm
Average receive power, each channel (max)	–7.2		dBm
Receiver reflectance (max)	–12		dB
Receiver sensitivity (OMA), each channel[c] (max)	–24.1		dBm
Detect threshold, each channel (min)	–40		dBm
Stressed receiver sensitivity (OMA), each channel[d] (max)	–22.6		dBm
Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty,[e] each channel	1.5		dB
Stressed eye J2 Jitter,[e] each channel	0.3		UI
Stressed eye J9 Jitter,[e] each channel	0.47		UI

[a] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[b] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level. Direct ONU–OLT connection may result in damage of the receiver.
[c] Receiver sensitivity (OMA), each channel (max) is informative.
[d] Measured with conformance test signal at TP3 (see 141.7.11) for BER = 10^{-2}.
[e] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

141.7 Definitions of optical parameters and measurement methods

The following subclauses describe definitive patterns and test procedures for Nx25G-EPON PMDs. Implementers using alternative verification methods need to ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods. All optical measurements, except TDP and $RIN_{15}OMA$ shall be made through a short patch cable between 2 m and 5 m in length.

141.7.1 Insertion loss

Insertion loss for SMF fiber optic cabling (channel) is defined at the wavelengths specified in Table 141–13 and Table 141–14, depending on the particular PMD. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280–4–2.

141.7.2 Test patterns

The test patterns used in this clause shall be the same as those used for 100GBASE-LR4, as described in 88.8.1 and shown in Table 88–10, with the exception of Pattern 5. Table 88–11 shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. A valid 25G-EPON signal is substituted for the 100GBASE-R signal specified in Table 88–11.

141.7.3 Wavelength and spectral width measurement

The center wavelength and spectral width (RMS) shall meet the specifications when measured according to the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3 under modulated conditions using an appropriate PRBS or a valid Nx25G-EPON signal, or another representative test pattern.

NOTE—The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

141.7.4 Optical power measurements

Optical power shall meet specifications according to the methods specified in IEC 61280–1–1. A measurement may be made with the port transmitting any valid Nx25G-EPON signal.

141.7.5 Extinction ratio measurements

The extinction ratio shall meet the specifications when measured according to IEC 61280–2–2 with the port transmitting a valid Nx25G-EPON signal, and with minimal back reflections into the transmitter, lower than –20 dB. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

141.7.6 Optical Modulation Amplitude (OMA) test procedure

See 88.8.4.

141.7.7 Relative intensity noise optical modulation amplitude ($RIN_x OMA$) measuring procedure

See 88.8.7, with exception of the optical return loss value of 15 dB.

141.7.8 Transmit optical waveform (transmit eye)

The required transmitter pulse shape characteristics for Nx25G-EPON PMDs are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4 and the test method shall be according to 88.8.8.

141.7.9 Transmitter and dispersion penalty (TDP) for 25G

TDP measurement tests transmitter impairments, including chromatic dispersion effects, due to signal propagation in SMF used in PON. Possible causes of impairment include intersymbol interference, jitter, and RIN. Meeting the separate requirements (e.g., eye mask, spectral characteristics) does not in itself guarantee the TDP. The TDP limit shall be met. TDP is measured as defined in 88.8.5 with the exceptions in 141.7.9.2 and 141.7.9.4.

141.7.9.1 Reference transmitter requirements

The reference transmitter shall meet the requirements listed in 88.8.5.1.

141.7.9.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed below.

An Nx25G-EPON OLT or ONU transmitter is to be compliant with a total dispersion at least as negative as the minimum dispersion given by Equation (141–1) and at least as positive as the maximum dispersion given by Equation (141–2) for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

$$D_{\min} = \min\left(0,\ 0.465 \times \lambda \times \left(1 - \left(\frac{1324}{\lambda}\right)^4\right)\right) \quad (141\text{–}1)$$

$$D_{\max} = \max\left(0,\ 0.465 \times \lambda \times \left(1 - \left(\frac{1300}{\lambda}\right)^4\right)\right) \quad (141\text{–}2)$$

where

λ is the wavelength of the device under test in nm

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss of 15 dB. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than 0.8 ps.

141.7.9.3 Reference receiver requirements

The reference receiver shall meet the requirements listed in 88.8.5.3.

141.7.9.4 Test procedure

The test procedure is as defined in 88.8.5.4, with the exception that a BER of 10^{-2} shall be used for the channel (wavelength) under test.

141.7.10 Receive sensitivity

The test patterns in 75.7.3 (10G) and 141.7.2 (25G) are used to test receiver sensitivity.

The test signal is required to have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter, and RIN. The measurement procedure is described in 52.9.8 for 10 Gb/s PHYs and 88.8.9 for 25 Gb/s PHYs. The sensitivity shall be met for the bit error ratio defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate.

141.7.11 Stressed receiver conformance test

Compliance with stressed receiver sensitivity is mandatory for PMDs listed in Table 141–7. The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics that could cause errors when combined with a distorted but compliant signal. To be compliant with stressed receiver sensitivity, the receiver shall meet the specified bit error ratio at the power level and signal quality defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate, according to the measurement procedures of 52.9.9 for 10 Gb/s PHYs and 88.8.10 for 25 Gb/s PHYs.

141.7.12 Jitter measurements

When measuring jitter at TP1[*i*] and TP5[*i*], it is recommended that jitter contributions at frequencies below receiver corner frequencies (i.e., 10 MHz for 25.78125 GBd receiver and 4 MHz for 10.3125 GBd receiver) are filtered at the measurement unit.

141.7.13 Laser on/off timing measurement

T_{on} is defined in 141.7.13.1 and has the value of less than or equal to 128 ns (defined in Table 141–19 and Table 141–20).

T_{off} is defined in 141.7.13.1 and has the value of less than or equal to 128 ns (defined in Table 141–19 and Table 141–20).

141.7.13.1 Definitions

For each of the channels, T_{on} is denoted as the time beginning from the falling edge of the tx_enable line to the ONU PMD and ending at the time that the optical signal at TP2 of the ONU PMD is within 15% of its steady-state parameters (average launched power, wavelength, RMS spectral width, transmitter and dispersion penalty, optical return loss tolerance, jitter, $RIN_{15}OMA$, extinction ratio and eye mask opening) as defined in Table 141–19 and Table 141–20. T_{on} is presented in Figure 141–3. The data transmitted may be any valid 256B/257B symbols.

For each of the channels, T_{off} is denoted as the time beginning from the rising edge of the tx_enable line to the ONU PMD and ending at the time that the optical signal at TP2 of the ONU PMD reaches the specified maximum average launch power of OFF transmitter as defined in Table 141–19 and Table 141–20. T_{off} is presented in Figure 141–3. The data transmitted may be any of the patterns listed in Table 88–10.

141.7.13.2 Test specification

The test setup for measuring T_{on} and T_{off} is shown in Figure 141–4. An O/E converter is used to convert the optical signal at TP3 to an electrical signal at TP4[*i*] where it is assumed that the response time of the converter is considerably shorter that the T_{on} value under measurement. A scope, with a variable delay, is able to measure the time from the tx_enable trigger to the time the optical signal reaches all its specified conditions. The delay to the scope trigger is adjusted until the point that the received signal meets all its specified conditions. This is the T_{on} in question.

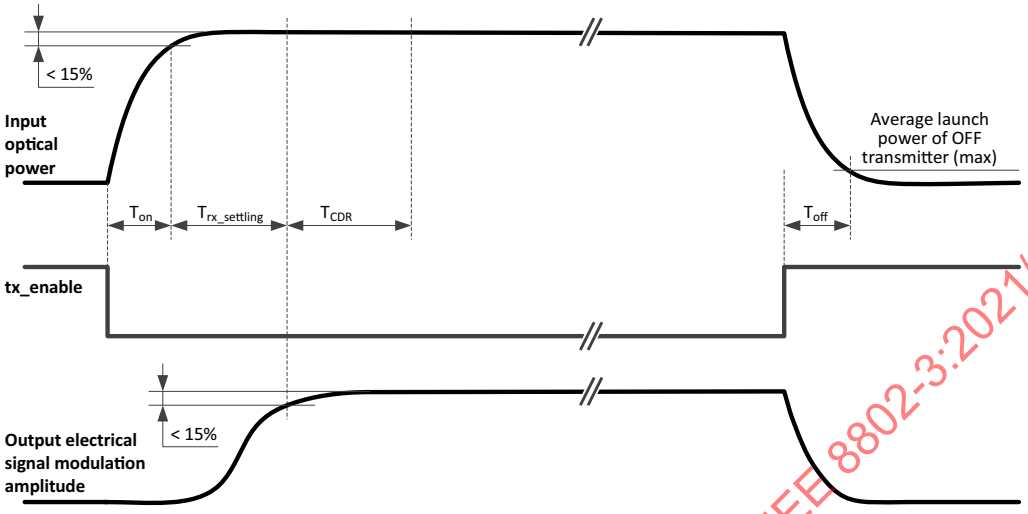


Figure 141–3—P2MP timing parameter definition, per channel

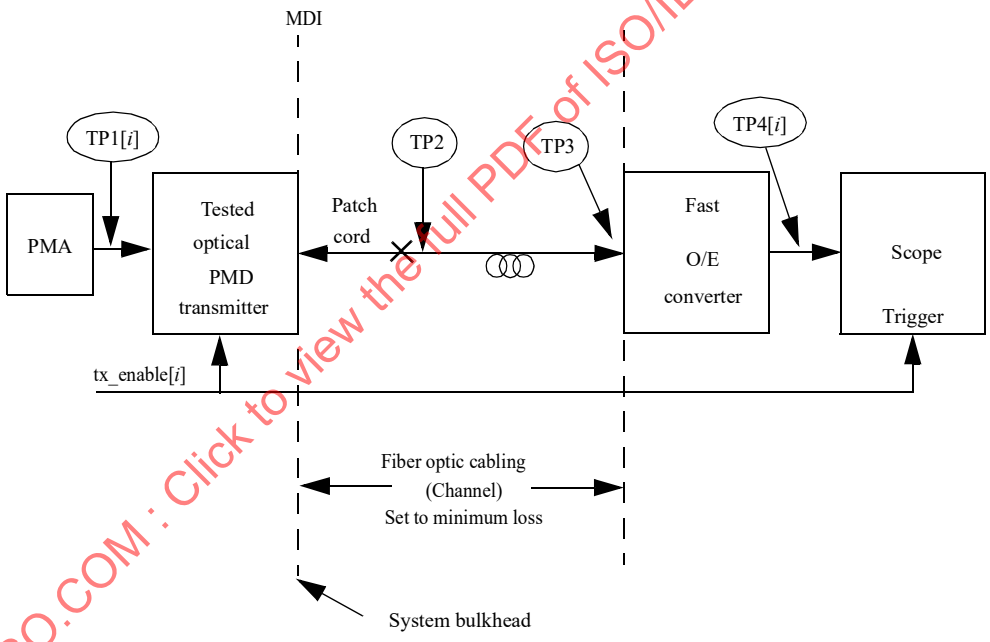


Figure 141–4—ONU PMD laser on/off time measurement setup

A non-rigorous way to describe this test setup would be: for a PMD with a declared T_{on} and T_{off}, measure all PMD optical parameters after T_{on} and T_{off} from the tx_enable trigger, confirming their conformance to being within 15% of the steady-state values. Notice that only the average launch power being below the average launch power of OFF transmitter is confirmed when measuring T_{off} time, since that is the only relevant parameter.

141.7.14 Receiver settling timing measurement

$T_{rx\_settling}$ is defined in 141.7.14.1 and has a value of less than 800 ns (defined in Table 141–17 and Table 141–18). A method for measuring $T_{rx\_settling}$ is illustrated in Figure 141–5.

141.7.14.1 Definitions

$T_{rx\_settling}$ is defined to be the time between the moment when the optical power at TP7 reaches the conditions specified in 141.7.13.1 for T_{on} and the moment after which the electrical modulation (peak-to-peak) at TP8[*i*] remains within 15% of its steady-state amplitude and jitter (see Table 141–17 and Table 141–18). The $T_{rx\_settling}$ time interval is illustrated in Figure 141–3. The data transmitted may be any valid 256B/257B symbols (or a specific power synchronization sequence). The optical signal at TP7, at the beginning of the locking, may have any valid 256B/257B pattern, optical power level, jitter, or frequency shift matching the standard specifications.

141.7.14.2 Test specification

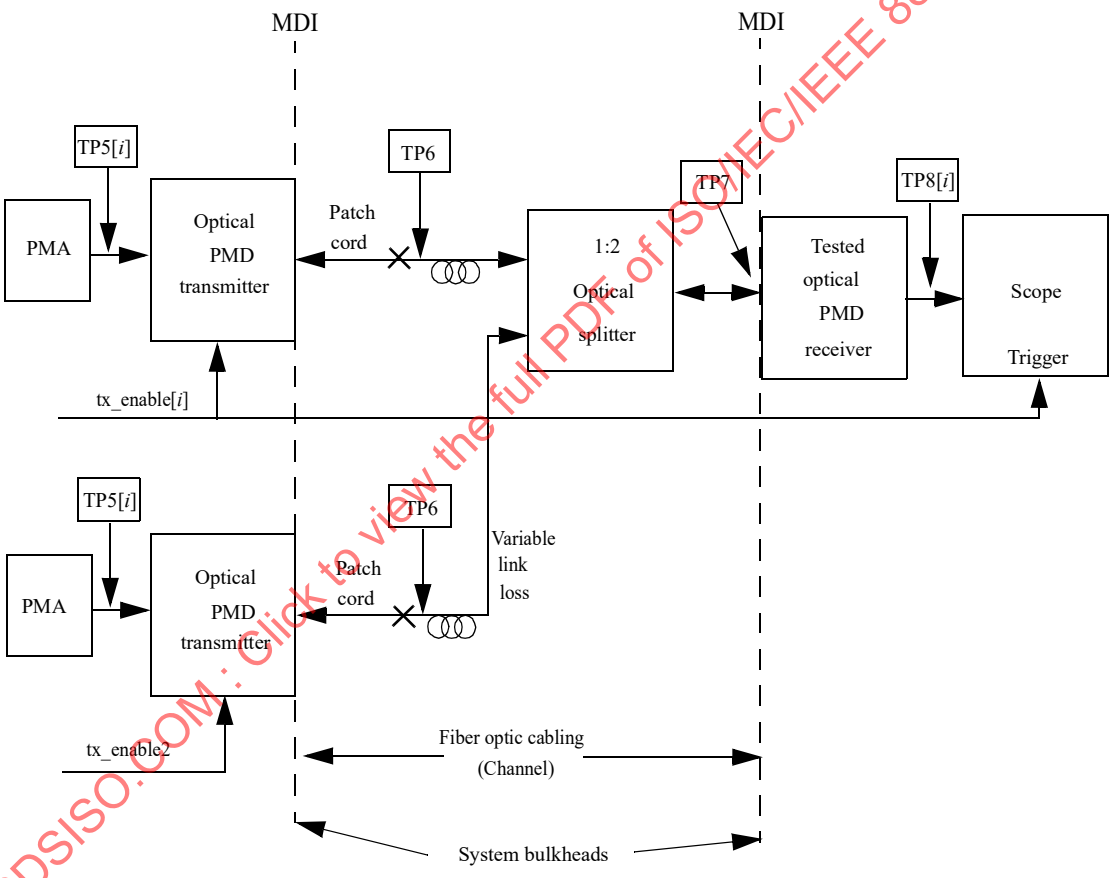


Figure 141–5—Receiver settling time measurement setup

Figure 141–5 illustrates the test setup for measuring the OLT PMD receiver (upstream) $T_{rx\_settling}$ time. The optical PMD transmitter has well–known parameters, with a fixed known T_{on} time. After T_{on} time the parameters of the reference transmitter, at TP6 and therefore at TP7, reach within 15% of their steady-state values as specified in Table 141–19 and Table 141–20.

Define $T_{rx\_settling}$ time as the time from the tx_enable assertion, minus the known T_{on} time, to the time the electrical signal at TP8 reaches within 15% of its steady-state conditions.

Conformance needs to be assured for an optical signal at TP7 with any level of its specified parameters before the tx_enable assertion. Especially, the $T_{rx\_settling}$ time is expected to be met in the following scenarios:

— Switching from a 'weak' (minimal received power at TP7) ONU to a 'strong' (maximal received power at TP7) ONU, with minimal guard band between.
— Switching from a 'strong' ONU to a 'weak' ONU, with minimal guard band between.
— Switching from noise level, with maximal duration interval, to 'strong' ONU power level.

For a tested PMD receiver with a declared $T_{rx\_settling}$ time, measure all PMD receiver electrical parameters at TP8[*i*] after $T_{rx\_settling}$ from the tx_enable trigger minus the reference transmitter T_{on}, assuring conformance to within 15% of their specified steady-state values.

141.8 Environmental, safety, and labeling

141.8.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

141.8.2 Laser safety

Nx25G-EPON optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.

141.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

141.8.4 Environment

The Nx25G-EPON operating environment specifications are as defined in 52.11, as defined in 52.11.1 for electromagnetic emission, and as defined in 52.11.2 for temperature, humidity, and handling.

See Annex 67A for additional environmental information. Two optional temperature ranges are defined in Table 60–18. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

141.8.5 PMD labeling

The Nx25G-EPON labeling recommendations and requirements are as defined in 52.12.

The list of all supported PMDs is shown in Table 141–7.

Each field-pluggable component shall be clearly labeled with its operating temperature range over which compliance is ensured.

141.9 Characteristics of the fiber optic cabling

The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 141–2.

141.9.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 141–2.

NOTE—The optical splitter presented in Figure 141–2 may be replaced by a number of smaller 1:n splitters such that a different topology may be implemented while preserving the link characteristics and power budget.

The maximum channel insertion losses shall meet the requirements specified in Table 141–1 through Table 141–5. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

141.9.2 Optical fiber and cable

The fiber optic cabling shall meet the dispersion specifications defined in ITU-T G.652, Section 6.10. Maximum and minimum dispersion levels at the maximum 20 km reach at the nominal transmission wavelengths bands are given in Table 141–23.

Table 141–23—Optical fiber and cable characteristics

Parameter	UW0	UW1	UW2	DW0	DW1	Unit
Nominal wavelength	1270	1300	1320	1358	1342	nm
Max Dispersion (at 20 km) [a,b]	–45.4	0	36	100.1	73.7	ps/nm
Min Dispersion (at 20 km) [a,b]	–105.9	–45.4	–7.4	47.8	25.8	ps/nm

[a] These dispersion values are informative and were calculated using inequalities specified in ITU-T G.652, section 6.10

[b] These dispersion requirements are satisfied by G.652.D fibers specified in ITU-T G.652 (low water peak, dispersion unshifted SMF) and G.657.A fibers specified in ITU-T G.657 (bend–insensitive SMF).

141.9.3 Optical fiber connection

An optical fiber connection consists of a mated pair of optical connectors or an optical splice point. The number of splices/connectors is not predefined; the number of individual fiber sections between the OLT MDI and the ONU MDI is not defined. The only requirements are that the resulting channel insertion loss at all specified transmission wavelengths is within the limits specified in Table 141–1 through Table 141–5. Other fiber arrangements (e.g., increasing the split ratio while decreasing the fiber length) are supported as long as the limits for the channel insertion loss specified in Table 141–1 through Table 141–5 are observed.

The maximum discrete reflectance for single-mode connections shall be less than –26 dB.

141.9.4 Medium Dependent Interface (MDI)

The Nx25G-EPON PMD is coupled to the fiber cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" as shown in Figure 141–2. Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a rateable connection, it shall meet the interface performance specifications of IEC 61753-1. The MDI carries the signal in both directions for Nx25G-EPON PMDs and couples to a single fiber.

NOTE—Compliance testing is performed at TP2 and TP3 as defined in 141.3.2, not at the MDI.

141.10 Protocol implementation conformance statement (PICS) proforma for Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks[4]

141.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

141.10.2 Identification

141.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

141.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ca-2020, Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ca-2020.)	

Date of Statement	

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

141.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HT	High temperature operation	141.8.4	–5 ºC to 85 ºC	O	Yes [ ] No [ ]
LT	Low temperature operation	141.8.4	–40 ºC to 60 ºC	O	Yes [ ] No [ ]
*PQG2510U2	25/10GBASE-PQG-U2 PHY or 25/10GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG2510D2	25/10GBASE-PQG-D2 PHY or 25/10GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG2510U3	25/10GBASE-PQG-U3 PHY or 25/10GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG2510D3	25/10GBASE-PQG-D3 PHY or 25/10GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX2510U2	25/10GBASE-PQX-U2 PHY or 25/10GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX2510D2	25/10GBASE-PQX-D2 PHY or 25/10GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX2510U3	25/10GBASE-PQX-U3 PHY or 25/10GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX2510D3	25/10GBASE-PQX-D3 PHY or 25/10GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG25U2	25GBASE-PQG-U2 PHY or 25GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG25D2	25GBASE-PQG-D2 PHY or 25GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG25U3	25GBASE-PQG-U3 PHY or 25GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG25D3	25GBASE-PQG-D3 PHY or 25GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
*PQX25U2	25GBASE-PQX-U2 PHY or 25GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX25D2	25GBASE-PQX-D2 PHY or 25GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX25U3	25GBASE-PQX-U3 PHY or 25GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX25D3	25GBASE-PQX-D3 PHY or 25GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG5010U2	50/10GBASE-PQG-U2 PHY or 50/10GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5010D2	50/10GBASE-PQG-D2 PHY or 50/10GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5010U3	50/10GBASE-PQG-U3 PHY or 50/10GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5010D3	50/10GBASE-PQG-D3 PHY or 50/10GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX5010U2	50/10GBASE-PQX-U2 PHY or 50/10GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5010D2	50/10GBASE-PQX-D2 PHY or 50/10GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5010U3	50/10GBASE-PQX-U3 PHY or 50/10GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5010D3	50/10GBASE-PQX-D3 PHY or 50/10GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG5025U2	50/25GBASE-PQG-U2 PHY or 50/25GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5025D2	50/25GBASE-PQG-D2 PHY or 50/25GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
*PQG5025U3	50/25GBASE-PQG-U3 PHY or 50/25GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5025D3	50/25GBASE-PQG-D3 PHY or 50/25GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX5025U2	50/25GBASE-PQX-U2 PHY or 50/25GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5025D2	50/25GBASE-PQX-D2 PHY or 50/25GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5025U3	50/25GBASE-PQX-U3 PHY or 50/25GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5025D3	50/25GBASE-PQX-D3 PHY or 50/25GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG50U2	50GBASE-PQG-U2 PHY or 50GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG50D2	50GBASE-PQG-D2 PHY or 50GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG50U3	50GBASE-PQG-U3 PHY or 50GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG50D3	50GBASE-PQG-D3 PHY or 50GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX50U2	50GBASE-PQX-U2 PHY or 50GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX50D2	50GBASE-PQX-D2 PHY or 50GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX50U3	50GBASE-PQX-U3 PHY or 50GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX50D3	50GBASE-PQX-D3 PHY or 50GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation/Cable	141.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

141.10.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 25/10GBASE-PQ, 25GBASE-PQ, 50/10GBASE-PQ, 50/25GBASE-PQ, and 50GBASE-PQ

141.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	141.3.3	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FN2	Transmitter optical signal	141.3.3	Highest optical power transmitted is a logic one	M	Yes [ ]
FN3	Receive function	141.3.4	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FN4	Receiver optical signal	141.3.4	Higher optical power received is a logic one	M	Yes [ ]
FN5	ONU signal detect function	141.3.5.1	Mapping to PMD service interface	M	Yes [ ]
FN6	ONU signal detect parameter	141.3.5.1	Generated according to Table 141–12	M	Yes [ ]
FN7	OLT signal detect function	141.3.5.2	Mapping to PMD service interface	O/2	Yes [ ] No [ ]
FN8	OLT signal detect function	141.3.5.2	Provided by higher layer	O/2	Yes [ ] No [ ]
FN9	OLT signal detect parameter	141.3.5.2	Generated according to Table 141–12	O	Yes [ ] No [ ]
FN10	Delay variation	141.3.1.2	Less than 0.25 EQT	M	Yes [ ]
FN11	Receiver sensitivity	141.7.10	The sensitivity is met for the bit error ratio defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
FN12	Stressed received sensitivity test	141.7.11	The receiver meets the specified bit error ratio at the power level and signal quality defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate, according to the measurement procedures of 52.9.9 for 10 Gb/s PHYs and 88.8.10 for 25 Gb/s PHYs.	M	Yes [ ]
FN13a	Channel-to-wavelength mapping, ONU	141.3.1.1	Channel-to-wavelength mapping for ONU	ONU:M	Yes [ ] N/A [ ]
FN13b	Channel-to-wavelength mapping, OLT	141.3.1.1	Channel-to-wavelength mapping for OLT	OLT:M	Yes [ ] N/A [ ]

141.10.4.2 PMD to MDI optical specifications for 25/10GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510D2F1	25/10GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG2510D2:M	Yes [ ] N/A [ ]
PQG2510D2F2	25/10GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG2510D2:M	Yes [ ] N/A [ ]

141.10.4.3 PMD to MDI optical specifications for 25/10GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510D3F1	25/10GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG2510D3:M	Yes [ ] N/A [ ]
PQG2510D3F2	25/10GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG2510D3:M	Yes [ ] N/A [ ]

141.10.4.4 PMD to MDI optical specifications for 25/10GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510D2F1	25/10GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX2510D2:M	Yes [ ] N/A [ ]
PQX2510D2F2	25/10GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX2510D2:M	Yes [ ] N/A [ ]

141.10.4.5 PMD to MDI optical specifications for 25/10GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510D3F1	25/10GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX2510D3:M	Yes [ ] N/A [ ]
PQX2510D3F2	25/10GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX2510D3:M	Yes [ ] N/A [ ]

141.10.4.6 PMD to MDI optical specifications for 25GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25D2F1	25GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG25D2:M	Yes [ ] N/A [ ]
PQG25D2F2	25GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG25D2:M	Yes [ ] N/A [ ]

141.10.4.7 PMD to MDI optical specifications for 25GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25D3F1	25GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG25D3:M	Yes [ ] N/A [ ]
PQG25D3F2	25GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG25D3:M	Yes [ ] N/A [ ]

141.10.4.8 PMD to MDI optical specifications for 25GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25D2F1	25GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX25D2:M	Yes [ ] N/A [ ]
PQX25D2F2	25GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX25D2:M	Yes [ ] N/A [ ]

141.10.4.9 PMD to MDI optical specifications for 25GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25D3F1	25GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX25D3:M	Yes [ ] N/A [ ]
PQX25D3F2	25GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX25D3:M	Yes [ ] N/A [ ]

141.10.4.10 PMD to MDI optical specifications for 50/10GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010D2F1	50/10GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG5010D2:M	Yes [ ] N/A [ ]
PQG5010D2F2	50/10GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG5010D2:M	Yes [ ] N/A [ ]

141.10.4.11 PMD to MDI optical specifications for 50/10GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010D3F1	50/10GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG5010D3:M	Yes [ ] N/A [ ]
PQG5010D3F2	50/10GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG5010D3:M	Yes [ ] N/A [ ]

141.10.4.12 PMD to MDI optical specifications for 50/10GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010D2F1	50/10GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX5010D2:M	Yes [ ] N/A [ ]
PQX5010D2F2	50/10GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX5010D2:M	Yes [ ] N/A [ ]

141.10.4.13 PMD to MDI optical specifications for 50/10GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010D3F1	50/10GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX5010D3:M	Yes [ ] N/A [ ]
PQX5010D3F2	50/10GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX5010D3:M	Yes [ ] N/A [ ]

141.10.4.14 PMD to MDI optical specifications for 50/25GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025D2F1	50/25GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG5025D2:M	Yes [ ] N/A [ ]
PQG5025D2F2	50/25GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG5025D2:M	Yes [ ] N/A [ ]

141.10.4.15 PMD to MDI optical specifications for 50/25GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025D3F1	50/25GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG5025D3:M	Yes [ ] N/A [ ]
PQG5025D3F2	50/25GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG5025D3:M	Yes [ ] N/A [ ]

141.10.4.16 PMD to MDI optical specifications for 50/25GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025D2F1	50/25GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX5025D2:M	Yes [ ] N/A [ ]
PQX5025D2F2	50/25GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX5025D2:M	Yes [ ] N/A [ ]

141.10.4.17 PMD to MDI optical specifications for 50/25GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025D3F1	50/25GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX5025D3:M	Yes [ ] N/A [ ]
PQX5025D3F2	50/25GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX5025D3:M	Yes [ ] N/A [ ]

141.10.4.18 PMD to MDI optical specifications for 50GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50D2F1	50GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG50D2:M	Yes [ ] N/A [ ]
PQG50D2F2	50GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG50D2:M	Yes [ ] N/A [ ]

141.10.4.19 PMD to MDI optical specifications for 50GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50D3F1	50GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG50D3:M	Yes [ ] N/A [ ]
PQG50D3F2	50GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG50D3:M	Yes [ ] N/A [ ]

141.10.4.20 PMD to MDI optical specifications for 50GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50D2F1	50GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX50D2:M	Yes [ ] N/A [ ]
PQX50D2F2	50GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX50D2:M	Yes [ ] N/A [ ]

141.10.4.21 PMD to MDI optical specifications for 50GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50D3F1	50GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX50D3:M	Yes [ ] N/A [ ]
PQX50D3F2	50GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX50D3:M	Yes [ ] N/A [ ]

141.10.4.22 PMD to MDI optical specifications for 25/10GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510U2F1	25/10GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG2510U2:M	Yes [ ] N/A [ ]
PQG2510U2F2	25/10GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG2510U2:M	Yes [ ] N/A [ ]

141.10.4.23 PMD to MDI optical specifications for 25/10GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510U3F1	25/10GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG2510U3:M	Yes [ ] N/A [ ]
PQG2510U3F2	25/10GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG2510U3:M	Yes [ ] N/A [ ]

141.10.4.24 PMD to MDI optical specifications for 25/10GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510U2F1	25/10GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX2510U2:M	Yes [ ] N/A [ ]
PQX2510U2F2	25/10GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX2510U2:M	Yes [ ] N/A [ ]

141.10.4.25 PMD to MDI optical specifications for 25/10GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510U3F1	25/10GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX2510U3:M	Yes [ ] N/A [ ]
PQX2510U3F2	25/10GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX2510U3:M	Yes [ ] N/A [ ]

141.10.4.26 PMD to MDI optical specifications for 25GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25U2F1	25GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG25U2:M	Yes [ ] N/A [ ]
PQG25U2F2	25GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG25U2:M	Yes [ ] N/A [ ]

141.10.4.27 PMD to MDI optical specifications for 25GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25U3F1	25GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG25U3:M	Yes [ ] N/A [ ]
PQG25U3F2	25GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG25U3:M	Yes [ ] N/A [ ]

141.10.4.28 PMD to MDI optical specifications for 25GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25U2F1	25GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX25U2:M	Yes [ ] N/A [ ]
PQX25U2F2	25GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX25U2:M	Yes [ ] N/A [ ]

141.10.4.29 PMD to MDI optical specifications for 25GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25U3F1	25GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX25U3:M	Yes [ ] N/A [ ]
PQX25U3F2	25GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX25U3:M	Yes [ ] N/A [ ]

141.10.4.30 PMD to MDI optical specifications for 50/10GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010U2F1	50/10GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG5010U2:M	Yes [ ] N/A [ ]
PQG5010U2F2	50/10GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG5010U2:M	Yes [ ] N/A [ ]

141.10.4.31 PMD to MDI optical specifications for 50/10GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010U3F1	50/10GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG5010U3:M	Yes [ ] N/A [ ]
PQG5010U3F2	50/10GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG5010U3:M	Yes [ ] N/A [ ]

141.10.4.32 PMD to MDI optical specifications for 50/10GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010U2F1	50/10GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX5010U2:M	Yes [ ] N/A [ ]
PQX5010U2F2	50/10GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX5010U2:M	Yes [ ] N/A [ ]

141.10.4.33 PMD to MDI optical specifications for 50/10GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010U3F1	50/10GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX5010U3:M	Yes [ ] N/A [ ]
PQX5010U3F2	50/10GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX5010U3:M	Yes [ ] N/A [ ]

141.10.4.34 PMD to MDI optical specifications for 50/25GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025U2F1	50/25GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG5025U2:M	Yes [ ] N/A [ ]
PQG5025U2F2	50/25GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG5025U2:M	Yes [ ] N/A [ ]

141.10.4.35 PMD to MDI optical specifications for 50/25GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025U3F1	50/25GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG5025U3:M	Yes [ ] N/A [ ]
PQG5025U3F2	50/25GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG5025U3:M	Yes [ ] N/A [ ]

141.10.4.36 PMD to MDI optical specifications for 50/25GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025U2F1	50/25GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX5025U2:M	Yes [ ] N/A [ ]
PQX5025U2F2	50/25GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX5025U2:M	Yes [ ] N/A [ ]

141.10.4.37 PMD to MDI optical specifications for 50/25GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025U3F1	50/25GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX5025U3:M	Yes [ ] N/A [ ]
PQX5025U3F2	50/25GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX5025U3:M	Yes [ ] N/A [ ]

141.10.4.38 PMD to MDI optical specifications for 50GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50U2F1	50GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG50U2:M	Yes [ ] N/A [ ]
PQG50U2F2	50GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG50U2:M	Yes [ ] N/A [ ]

141.10.4.39 PMD to MDI optical specifications for 50GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50U3F1	50GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG50U3:M	Yes [ ] N/A [ ]
PQG50U3F2	50GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG50U3:M	Yes [ ] N/A [ ]

141.10.4.40 PMD to MDI optical specifications for 50GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50U2F1	50GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX50U2:M	Yes [ ] N/A [ ]
PQX50U2F2	50GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX50U2:M	Yes [ ] N/A [ ]

141.10.4.41 PMD to MDI optical specifications for 50GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50U3F1	50GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX50U3:M	Yes [ ] N/A [ ]
PQX50U3F2	50GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX50U3:M	Yes [ ] N/A [ ]

141.10.4.42 Definitions of optical parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	141.7.1	2 m to 5 m in length	M	Yes [ ]
OM2	Wavelength and RMS spectral width	141.7.3	Per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	141.7.4	Per IEC 61280-1-1	M	Yes [ ]
OM4	Extinction ratio	141.7.5	Per IEC 61280-2-2 with minimal back reflections	M	Yes [ ]
OM5	Optical modulation amplitude (OMA) test procedure	141.7.6		M	Yes [ ]
OM6	RIN_xOMA	141.7.7		M	Yes [ ]
OM7	Transmit optical waveform (transmit eye)	141.7.8		M	Yes [ ]
OM8	Transmitter and dispersion penalty	141.7.9		M	Yes [ ]
OM9	Receiver sensitivity	141.7.10		M	Yes [ ]
OM10	Stressed receiver conformance test	141.7.11		O	Yes[ ] No[ ]
OM11	Jitter measurements	141.7.12		M	Yes [ ]
OM12	Laser On/Off timing measurement	141.7.13		M	Yes [ ]
OM13	Receiver settling timing measurement	141.7.14		O	Yes [ ] No [ ]

141.10.4.43 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	141.9	Specified in Table 141–23	INS:M	Yes [ ] N/A[ ]
F02	End–to–end channel loss	141.9	Meeting the requirements of Table 141–1 through Table 141–5	INS:M	Yes [ ] N/A[ ]
FO3	Maximum discrete reflectance – single-mode fiber	141.9.3	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO4	MDI requirements	141.9.4	Meet the interface performance specifications of IEC 61753-1, if remateable	INS:O	Yes [ ] No [ ] N/A [ ]

141.10.4.44 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	141.8.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	141.8.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Documentation	141.8.2	Explicitly defines requirements and usage restrictions to meet safety certifications	M	Yes [ ]
ES4	Operating temperature range	141.8.4	The operating temperature range is declared	M	Yes [ ]
ES5	Operating temperature range label	141.8.5	Provided for field-pluggable components	M	Yes [ ]

142. Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON

142.1 Overview

This clause describes the Physical Coding Sublayer (PCS) with forward error correction (FEC) and Physical Medium Attachment (PMA) used with Nx25G-EPON point-to-multipoint (P2MP) networks. P2MP networks are passive optical networks (PONs) that connect multiple DTEs using a single shared fiber. The architecture is asymmetric, based on a tree and branch topology utilizing passive optical splitters. This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in Clause 144 (see Figure 142–1).

In this clause the term xMII is used to refer to both the 25GMII and the XGMII interfaces.

Figure 142–2 illustrates the functional block diagram of the Nx25G-EPON PHY with emphasis placed on the PCS. The Nx25G-EPON PCS is specified to support Nx25G-EPON PMDs, where:

— Both the receive and transmit paths operate at 25.78125 GBd rate (25/25G-EPON, 50/25G-EPON, and 50/50G-EPON), or
— The receive path operates at 25.78125 GBd rate and the transmit path operates at 10.3125 GBd (25/10G-EPON and 50/10G-EPON ONU), or
— The transmit path operates at 25.78125 GBd rate and the receive path operates at 10.3125 GBd (25/10G-EPON and 50/10G-EPON OLT).

See 143.3.1.1 for definition of TXD, TXC, TX_CLK, RXD, RXD, and RX_CLK.

142.1.1 Conventions

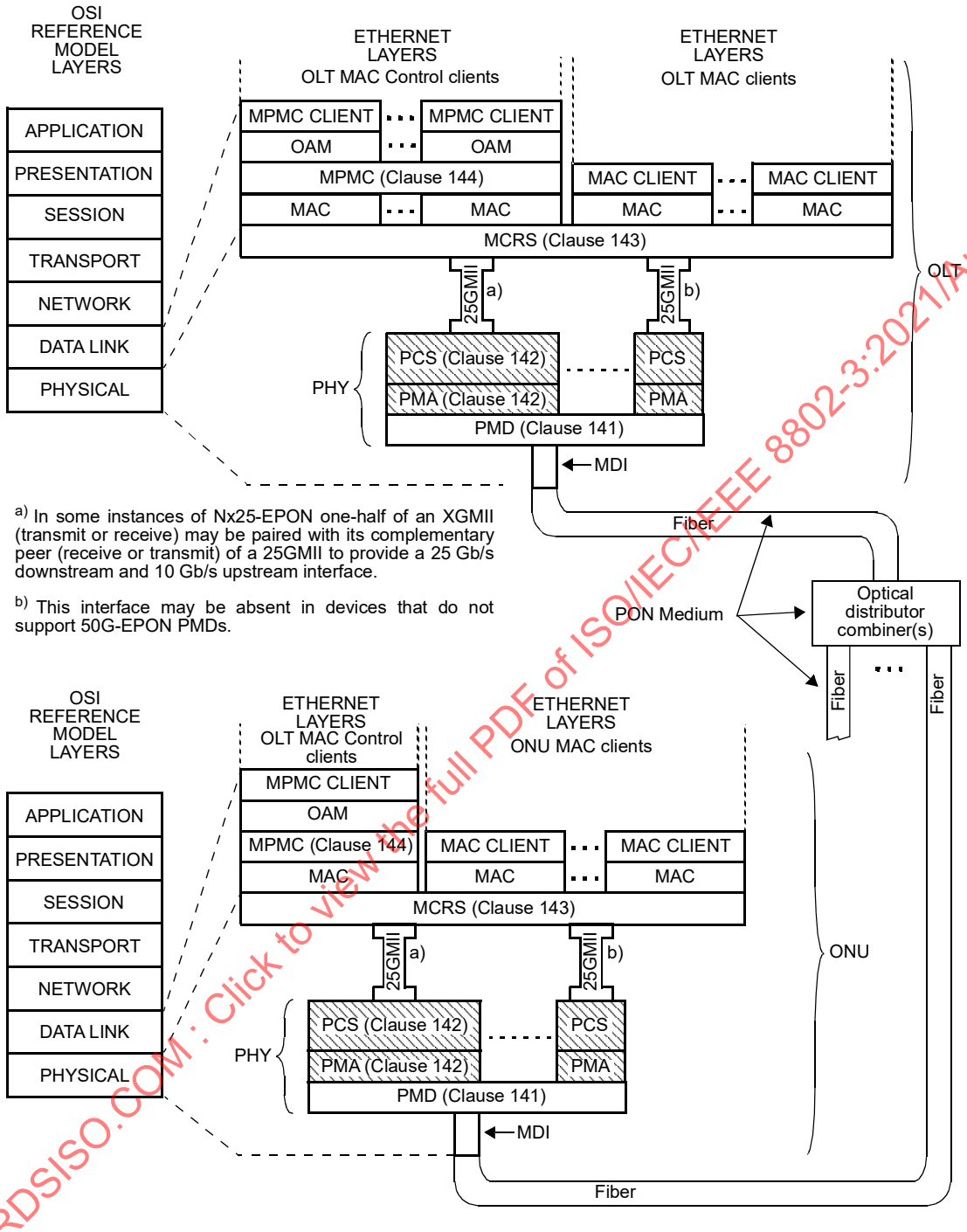
142.1.1.1 State diagrams

The body of this standard comprises state diagrams, including the associated definitions of variables, constants, and functions. The notation used in the state diagrams follows the conventions in 21.5, with extensions listed in the following subclauses. In case of any discrepancies between a state diagram and descriptive text, the state diagram prevails.

142.1.1.2 Hexadecimal notation

In addition to the rules for hexadecimal notation described in 1.2.5, the following conventions are used:

— Individual octets of a hexadecimal number are separated by hyphens, e.g., 0x1E-EE-80-23-CA.
— A part of a hexadecimal number enclosed in parenthesis followed by a subscripted decimal number n indicates that the parenthetical portion is to be repeated n times. For example, 0x12-34-56-$(AB\text{-}CD)_6$-EF is equivalent to the following expanded representation of a 128-bit number: 0x12-34-56-AB-CD-AB-CD-AB-CD-AB-CD-AB-CD-EF.



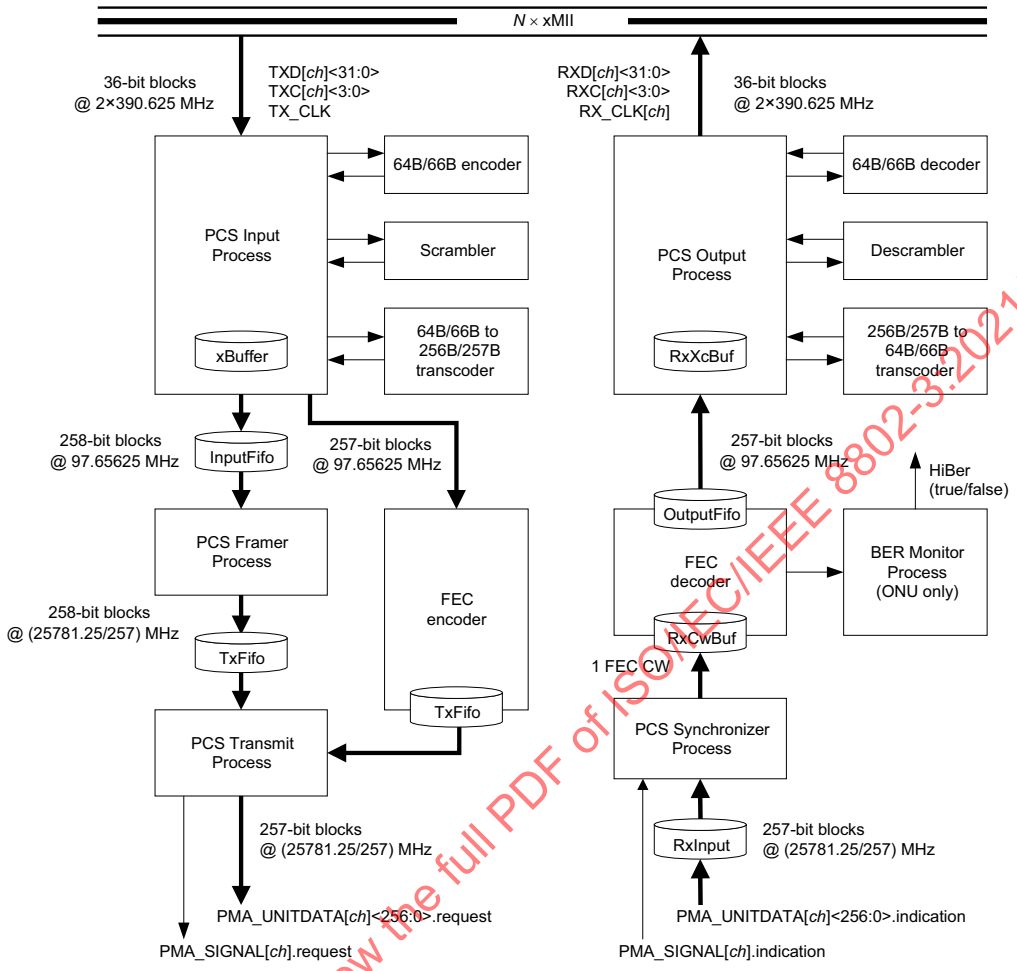
[a] In some instances of Nx25-EPON one-half of an XGMII (transmit or receive) may be paired with its complementary peer (receive or transmit) of a 25GMII to provide a 25 Gb/s downstream and 10 Gb/s upstream interface.

[b] This interface may be absent in devices that do not support 50G-EPON PMDs.

PCS and PMA described in this clause

25GMII= 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 142–1—Relationship of Nx25G-EPON P2MP PCS and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model



a) PCS transmit path **b) PCS receive path**

NOTE—All clock frequencies in this figure are shown for the nominal MAC data rate of 25 Gb/s. For PCS devices supporting the nominal MAC data rate of 10 Gb/s, all clock frequencies are scaled down by a multiplicative coefficient of 0.4.

Figure 142–2—PCS functional block diagram

142.1.1.3 Timers

Some state diagrams may utilize timers. Timers follow the conventions of 14.2.3.2 augmented as follows:

a) [start x_timer, *y*] sets expiration of *y* to timer x_timer.
b) Upon expiration of timer x_timer, a Boolean variable x_timer_done gets asserted automatically. Restarting the timer x_timer deasserts the value of x_timer_done.
c) [stop x_timer] aborts the timer operation for x_timer deasserting x_timer_done indefinitely.

142.1.1.4 Operations on variables

The operators used in state diagrams and in associated definitions of variables, constants, and functions are defined in Table 142–1. The operators are listed in decreasing order of precedence.

Table 142–1—Operators used in state diagrams and functions

Operator	Meaning
(…)	Indicates precedence or a set of function arguments
[…]	Array subscript
++	Unary operator placed after a variable; increments the variable by 1
– –	Unary operator placed after a variable; decrements the variable by 1
!	Boolean NOT
*	Multiplication
/	Division
+	Addition
–	Subtraction
<	Less than (see 142.1.1.5)
>	More than (see 142.1.1.5)
≤	Less than or equal to (see 142.1.1.5)
≥	More than or equal to (see 142.1.1.5)
==	Equals (a test of equality)
!=	Not equals
AND	Logical or bitwise AND. If one or both operands are defined as Boolean values, the operation is logical AND. Otherwise, the operation is considered the bitwise AND (each bit of the first operand is logically AND-ed with the corresponding bit of the second operand).
XOR	Logical or bitwise exclusive OR. If one or both operands are defined as Boolean values, the operation is logical XOR. Otherwise, the operation is considered the bitwise XOR (each bit of the first operand is logically XOR-ed with the corresponding bit of the second operand).

Table 142–1—Operators used in state diagrams and functions *(continued)*

Operator	Meaning
OR	Logical or bitwise OR. If one or both operands are defined as Boolean values, the operation is logical OR. Otherwise, the operation is considered the bitwise OR (each bit of the first operand is logically OR-ed with the corresponding bit of the second operand).
|	Concatenation operation that combines several subfields or parameters into a single aggregated field or parameter
∈	Is a member of
∉	Is not a member of
⇐ =	Assignment operator (in state diagrams) Assignment operator (in function code)
+=	Increments left operand value by the value of the operand on the right (x += y is equivalent to x ⇐ x + y)
–=	Decrements left operand value by the value of the operand on the right (x –= y is equivalent to x ⇐ x – y)

Variables that allow access to individual bits are called vectors. The vector notations use 0 to mark the first received bit. Individual bits are accessed using the following notation:

a) data_vector<*k*> accesses the *k*th bit of the vector.
b) data_vector<*m*:*n*> accesses bits *n* through *m* inclusively. The *n*th bit is received earlier than the *m*th bit. Refer to 3.1.1 for the conventions on bit ordering.

142.1.1.5 Operations on wrap-around variables

Various integer variables/counters defined in this clause wrap around on overflow, i.e., reset to zero when incremented by one after reaching the maximum value. A subtraction operation ($a - b$) on such variables is straightforward and may be replaced by addition of the first operand a and two's complement of the second operand b. Unless explicitly stated, the result of such subtraction is a signed integer of the same size (bit width) as the largest of the two operands. In other words, the subtraction operation assumes that the maximum absolute difference between the two operands does not exceed half of their maximum range.

A function $a < b$ is used to compare two wrap-around values. Returned value is true when b is larger than a allowing for wrap-around of a and b. The comparison is made by subtracting b from a and testing the MSB. If MSB($a - b$) = 1 (i.e., if the result of $a - b$ is negative) the value true is returned, else false is returned. In addition, the following functions are defined in terms of $a < b$:

a) $a > b$ is equivalent to $!(a < b \text{ or } a = b)$
b) $a \geq b$ is equivalent to $!(a < b)$
c) $a \leq b$ is equivalent to $!(a > b)$

142.1.1.6 FIFO access operations

State diagrams make extensive use of first-in, first-out (FIFO) buffers. These buffers support a common set of operations, defined as follows:

a) Buf.Append(*e*) adds the element *e* to the input of FIFO buffer Buf.
b) Buf.Clear() removes all elements from the FIFO buffer Buf.
c) Buf.Fill(*e*) writes element/value *e* into each position of FIFO buffer Buf.
d) Buf.GetHead() returns the oldest (head) element in the FIFO buffer Buf, and removes that element from the FIFO, decreasing its length by one.
e) Buf.IsEmpty() returns true if the FIFO buffer is empty (has no elements), otherwise the function returns false.
f) Buf.IsFull() returns true if the FIFO buffer Buf is full (i.e., Buf has no unoccupied positions), otherwise the function returns false.
g) Buf.PeekHead() returns the oldest (head) element in the FIFO buffer Buf without removing that element from the FIFO.

All of the FIFO access operations are assumed to be non-blocking and to take zero time to complete the execution.

142.1.2 Delay constraints

The combined delay variation through the transmit path of the Nx25G-EPON PCS and PMA is expected to be less than 6 EQTs (see 1.4.245c) for channels operating at 25.78125 GBd and less than 15 EQTs for channels operating at 10.3125 GBd.

The combined delay variation through the receive path of the Nx25G-EPON PCS and PMA is expected to be less than 2 EQTs for channels operating at 25.78125 GBd and less than 5 EQTs for channels operating at 10.3125 GBd.

The aforementioned delay variation limits are applicable only for the data units (either EQ or the corresponding 257-bit block) located at the fixed offset within the FEC codeword.

142.1.3 Burst transmission

Figure 142–3 presents the details of the ONU burst transmission, in particular, details of the FEC-unprotected and the FEC-protected areas of the upstream burst with three distinct synchronization pattern zones.

The upstream burst begins with a synchronization pattern, which is not FEC protected. The synchronization pattern comprises: SP1 zone, optimized for laser on (T_{on}) and automatic gain control (AGC, $T_{rx\_settling}$); SP2 zone, optimized for clock and data recovery (CDR, T_{CDR}); and SP3 zone, optimized for the start-of-burst delimiter (SBD) pattern. Each SP zone is a multiple of 257 bits, aligning with the PCS (defined in 142.2 and 142.3) line code of 256B/257B.

Bit patterns transmitted within each SP zone are configured by the OLT using three SYNC_PATTERN MPCPDUs (see 144.3.6.7).

In the bursts transmitted during the discovery operation, the SBD is followed by a single (shortened) FEC codeword carrying a single REGISTER_REQ MPCPDU. In normal operation the SBD is followed by a number of FEC codewords, where the last codeword may be shortened to reduce the unused QC-LDPC codeword payload at the end of the burst (see 142.2.4). Each FEC codeword comprises a series of 256B/257B encoded and scrambled data blocks, followed by a series of 257-bit long parity blocks. Within a non-shortened FEC codeword, the FEC payload portion includes 56 of these 257-bit data blocks and 10 257-bit blocks carrying QC-LDPC parity and codeword delimiter. Within a shortened FEC codeword, the FEC payload portion may be truncated to a number of data blocks smaller than 56, while the size of the FEC parity portion remains unchanged.

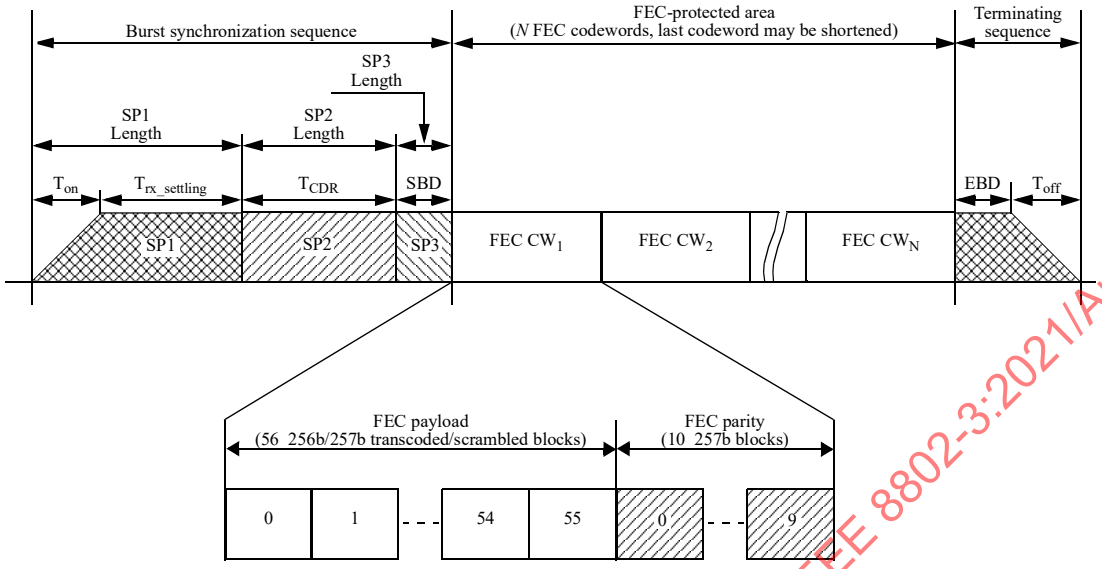


Figure 142–3—ONU burst structure, 3 zones

The upstream burst ends with an end-of-burst delimiter (EBD). When received at the OLT, the EBD pattern allows for the rapid reset of the OLT FEC synchronizer, preparing the OLT for the next incoming upstream burst. The EBD pattern is not part of the last FEC codeword.

142.1.3.1 Default synchronization pattern parameters

To assist the device development, testing/verification, and interoperability efforts, this subclause provides a set of default synchronization pattern parameters.

SP1 and SP2 synchronization patterns have the value of 0x1-$(AA)_{32}$ and are transmitted in a balanced form, i.e., every 257-bit block starting with the second one is an inversion of the previous block. The transmission bit sequence consists of 257 bits of alternating 1s and 0s, starting with 1.

The SP3 synchronization pattern zone represents the start-of-burst delimiter (SBD). It has the length of one block (257 bits) and the value of 0x1-BF-40-18-E5-C5-49-BB-59-6B-F8-D8-12-D8-58-E4-AB-40-BF-E7 -1A-3A-B6-44-A6-94-07-27-ED-27-A7-1B-54. The transmission bit sequence is:

(first bit) 1 1111 1101 0000 0010 0001 1000 1010 0111
1010 0011 1001 0010 1101 1101 1001 1010
1101 0110 0001 1111 0001 1011 0100 1000
0001 1011 0001 1010 0010 0111 1101 0101
0000 0010 1111 1101 1110 0111 0101 1000
0101 1100 0110 1101 0010 0010 0110 0101
0010 1001 1110 0000 1110 0100 1011 0111
1110 0100 1110 0101 1101 1000 0010 1010 (last bit)

This combination of SP2 and SP3 synchronization pattern values is characterized by the Hamming distance of 110 or higher between the SP3 and any preceding 257-bit long pattern, i.e., concatenation of x bits of SP2 and y bits of SP3, where x is between 1 and 257, and $x + y = 257$.

142.2 PCS transmit data path

This subclause defines the transmit direction of the Nx25G-EPON PCS. In the OLT, the PCS transmit function operates in a continuous mode at 25.78125 GBd rate.

In the ONU, the PCS transmit function operates in burst mode at 25.78125 GBd rate (25/25G-EPON, 50/25G-EPON, and 50/50G-EPON) or at 10.3125 GBd rate (25/10G-EPON and 50/10G-EPON).

The PCS transmit function includes a mandatory QC-LDPC FEC encoder. The functional block diagram for the PCS transmit function is shown in Figure 142–2. The PCS transmit function consists of the following functional blocks:

— PCS Input process (see 142.2.5.4.1),
— PCS Framer process (see 142.2.5.4.2), and
— PCS Transmit process (see 142.2.5.4.3).

As shown in Figure 142–4, the PCS transmitter first inputs two transfers from the xMII and consolidates these into a single 72-bit block that is then encoded into a 66-bit block. Four 66-bit blocks are accumulated, scrambled, and transcoded into a 257-bit block that is transferred to the InputFifo and also copied to the FEC encoder. Data is transferred to the TxFifo, along with framing information (see 142.2.5.4.2) by the PCS Framer process. The PCS Transmit process transfers 257-bit blocks containing framing, information, and parity bits to the PMA. The PCS shall transmit bits in the order shown in Figure 142–4.

NOTE—Figure 142–4 only shows the bits that are being transmitted and does not show the bit that is added and removed within PCS for control purposes.

142.2.1 64B/66B line encoder

The Nx25G PCS encodes a 72-bit block into a 64B/66B block structure as defined in 49.2.4, using all the block type fields in Figure 49–7 except block type field values of: 0x2D, 0x33, 0x66, 0x55, and 0x4B.

The control characters and their mappings to Nx25G-EPON control codes are specified in Table 142–2. The representations of the control characters are the control codes. Control characters are transferred over the xMII as 7-bit values. The Nx25G-EPON PCS encodes the start and terminate control characters implicitly using the block type field. The Nx25G-EPON PCS does not support ordered set control codes. All control code values that do not appear in Table 142–2 shall not be transmitted and are treated as an error if received.

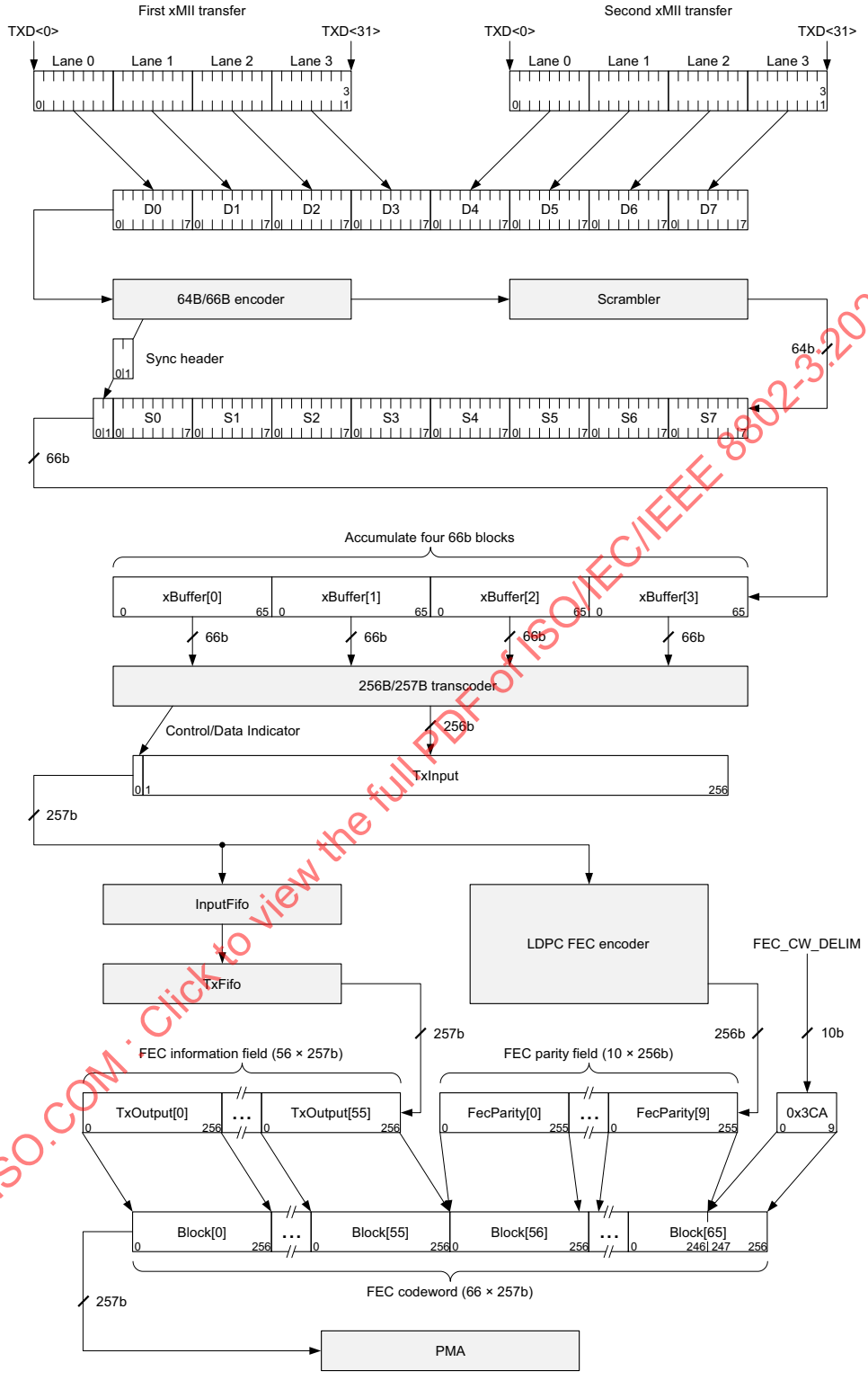


Figure 142–4—Transmit bit ordering

Table 142–2—Control codes

Control character	Notation	xMII control code	Nx25GBASE-PQ control code
Idle	/I/	0x07	0x00
Inter-envelope idle	/IEI/	0x08	0x08
Rate adjust	/RA/	0x09	0x09
Inter-burst idle	/IBI/	0x0A	0x0A
Start	/S/	0xFB	Encoded by block type field
Terminate	/T/	0xFD	Encoded by block type field
Error	/E/	0xFE	0x1E

142.2.2 Scrambler

The Nx25G PCS scrambles the payload of each 66-bit block. It then accumulates 66-bit blocks into groups of four and transcodes each group into a single 257-bit block. The payload of each 66-bit block is scrambled using the scrambling function defined in 49.2.6.

In the ONU, at the beginning of each burst, the scrambler is reset to a known initialization value (see the definition of ResetScrambler() function in 142.2.5.3).

142.2.3 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder converts four consecutive scrambled 64B/66B blocks into one scrambled 256B/257B block as described in 91.5.2.5.

142.2.4 FEC encoder

The Nx25G-EPON PCS shall encode the transmitted data stream using a quasi-cyclic QC-LDPC FEC, defined in 142.2.4.1. FEC encoder test vectors are provided in Annex 142A.

142.2.4.1 Low-density parity-check coding

The full QC-LDPC code is defined by a $(M + P) \times (K + S + M + P) = 3\,072 \times 17\,664$ size parity-check matrix H composed of a 12×69 array of 256×256 sub-matrices $A_{i,j}$:

$$H = \begin{bmatrix} A_{1,1} & \cdots & A_{1,69} \\ \cdots & & \cdots \\ A_{12,1} & \cdots & A_{12,69} \end{bmatrix}$$

The sub-matrices $A_{i,j}$ are either a cyclic shifted version of identity matrix or a zero matrix, and have a size of 256×256. The parity-check matrix is described in its compact form:

$$H_C = \begin{bmatrix} a_{1,1} & \cdots & a_{1,69} \\ \cdots & & \cdots \\ a_{12,1} & \cdots & a_{12,69} \end{bmatrix}$$

where $a_{i,j} = -1$ for a zero sub-matrix in position (i, j), and a positive integer number $a_{i,j}$ defines the number of right column shifts of the identity matrix.

The compact form of parity-check matrix H_c is shown in Table 142–3.

Table 142–3—Compact form of parity-check matrix H_c

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
80	–1	–1	105	–1	–1	137	–1	–1	0	209	53
–1	0	91	–1	170	46	–1	118	208	–1	–1	–1
–1	–1	–1	–1	250	–1	104	15	0	–1	252	93
60	0	74	87	–1	37	–1	–1	–1	123	–1	–1
169	–1	–1	–1	–1	–1	238	93	0	–1	39	216
–1	0	237	43	195	49	–1	–1	–1	41	–1	–1
11	–1	202	–1	139	150	–1	–1	0	191	–1	–1
–1	0	–1	165	–1	–1	228	228	–1	–1	159	57
143	–1	–1	–1	–1	65	–1	–1	0	211	69	9
–1	0	201	180	135	–1	225	78	–1	–1	–1	–1
–1	–1	136	–1	–1	–1	247	–1	0	217	37	130
222	0	–1	80	92	177	–1	16	–1	–1	–1	–1
–1	–1	178	227	–1	144	–1	0	–1	243	134	–1
59	0	–1	–1	147	–1	191	–1	251	–1	–1	130
–1	–1	239	221	–1	70	–1	48	0	97	–1	–1
218	0	–1	–1	–1	–1	177	–1	–1	–1	201	238
–1	–1	183	77	–1	95	–1	0	–1	252	49	–1
–1	0	–1	–1	–1	–1	255	–1	44	–1	–1	–1
178	0	–1	–1	–1	–1	–1	–1	123	–1	–1	–1
–1	–1	217	0	–1	221	–1	–1	–1	–1	–1	–1
–1	0	–1	–1	13	–1	–1	62	–1	–1	–1	–1
–1	–1	232	–1	–1	–1	–1	–1	–1	0	104	–1
–1	–1	–1	–1	–1	–1	192	0	–1	–1	–1	144
–1	–1	–1	–1	98	192	–1	–1	0	–1	–1	–1
105	0	–1	16	–1	–1	–1	–1	–1	–1	–1	–1
–1	–1	169	–1	–1	128	–1	0	–1	–1	–1	–1
–1	–1	–1	–1	142	–1	–1	–1	0	–1	129	–1
19	0	–1	–1	–1	–1	51	–1	–1	–1	–1	–1
–1	–1	–1	–1	–1	214	–1	–1	–1	0	–1	162

Table 142–3—Compact form of parity-check matrix H_c *(continued)*

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
–1	–1	–1	252	–1	–1	–1	–1	–1	–1	157	0
126	–1	–1	–1	225	–1	–1	0	–1	–1	–1	–1
–1	–1	–1	96	–1	–1	–1	–1	0	41	–1	–1
–1	0	129	–1	–1	–1	195	–1	–1	–1	–1	–1
–1	–1	60	0	–1	–1	–1	–1	–1	–1	222	–1
211	–1	–1	–1	–1	51	0	–1	–1	–1	–1	–1
–1	–1	–1	–1	–1	–1	–1	–1	0	29	–1	175
–1	0	–1	–1	23	–1	–1	112	–1	–1	–1	–1
–1	–1	–1	–1	108	–1	172	–1	–1	0	–1	–1
–1	–1	–1	17	–1	100	–1	0	–1	–1	–1	–1
–1	0	19	–1	–1	–1	–1	–1	–1	–1	–1	145
247	–1	76	–1	–1	–1	–1	–1	0	–1	–1	–1
–1	–1	–1	–1	–1	19	–1	–1	–1	–1	139	0
255	–1	–1	–1	–1	–1	–1	–1	–1	0	39	–1
–1	0	–1	–1	–1	–1	219	–1	153	–1	–1	–1
–1	–1	–1	219	0	235	–1	–1	–1	–1	–1	–1
85	–1	–1	–1	–1	–1	–1	0	–1	–1	–1	36
–1	–1	77	–1	0	–1	236	–1	–1	–1	–1	–1
–1	0	–1	198	–1	–1	–1	–1	–1	193	–1	–1
–1	–1	–1	165	–1	–1	–1	–1	0	–1	203	–1
–1	–1	–1	–1	–1	–1	136	0	–1	145	–1	–1
–1	–1	2	–1	–1	–1	–1	0	–1	–1	94	–1
–1	–1	–1	–1	135	–1	–1	–1	0	–1	–1	91
246	0	–1	–1	–1	4	–1	–1	–1	–1	–1	–1
94	–1	–1	36	–1	–1	0	–1	–1	–1	–1	–1
–1	–1	101	–1	–1	–1	–1	–1	–1	0	–1	22
–1	–1	–1	–1	–1	251	–1	22	0	–1	–1	–1
–1	0	–1	–1	121	–1	–1	–1	–1	–1	194	–1
–1	–1	217	–1	0	–1	159	–1	–1	–1	–1	–1
–1	–1	–1	171	–1	109	–1	–1	–1	–1	–1	0
242	–1	–1	–1	–1	–1	–1	–1	–1	–1	3	0
–1	0	–1	–1	–1	–1	10	–1	–1	–1	–1	212
–1	–1	48	–1	–1	–1	–1	0	–1	140	–1	–1

Table 142–3—Compact form of parity-check matrix H_c *(continued)*

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
–1	–1	–1	–1	–1	–1	–1	0	–1	46	43	–1
–1	–1	–1	228	0	–1	–1	–1	–1	–1	153	–1
129	–1	–1	–1	–1	140	–1	–1	–1	–1	–1	0
–1	–1	–1	–1	–1	–1	5	–1	0	58	–1	–1
19	–1	–1	–1	46	–1	–1	–1	0	–1	–1	–1
58	0	172	39	242	193	25	120	16	202	207	69
27	–1	42	234	228	241	94	192	0	215	109	88

NOTE—A CSV file containing the entire parity-check matrix H_c shown in Table 142–3 is available at: http://standards.ieee.org/downloads/802.3/.

142.2.4.2 FEC encoder processing

The FEC encoder is shown in Figure 142–5. The encoder consists of a systematic QC–LDPC encoding engine followed by a shortening and puncturing mechanism and the addition of a 10-bit delimiter. The parameters of the FEC encoder are as follows:

- The QC-LDPC parity-check matrix is a 12 × 69 array of circulant sub-matrices (see 142.2.4.1) with circulant size $Z = 256$; QC-LDPC user bit length before shortening is $57 \times 256 = 14\,592$, the parity bit length before puncturing is $12 \times 256 = 3072$; the codeword length before any shortening and puncturing is 17 664.
- The number of transmitted information bits, K (with maximum user length $K_{max} = 14\,392$).
- The number of shortened information bits, S ($S = 14\,592 - K$).
- The number of punctured parity-check bits, P ($P = 512$).
- The number of parity-check bits after puncturing, M ($M = 3072 - P = 2560$).
- The length of the FEC encoder output + delimiter is N where $N = K + M + 10$ bits and $N_{max} = K_{max} + M + 10$ bits = 16 962.
- The code rate, $R = K / N$, defined as the code rate after puncturing and after shortening.

The encoder supports a highest code rate $R_{max} = K_{max} / N_{max} = 0.848$. Codes with lower code rates/shorter block length shall be obtained through shortening. The puncturing length and location are fixed for all scenarios.

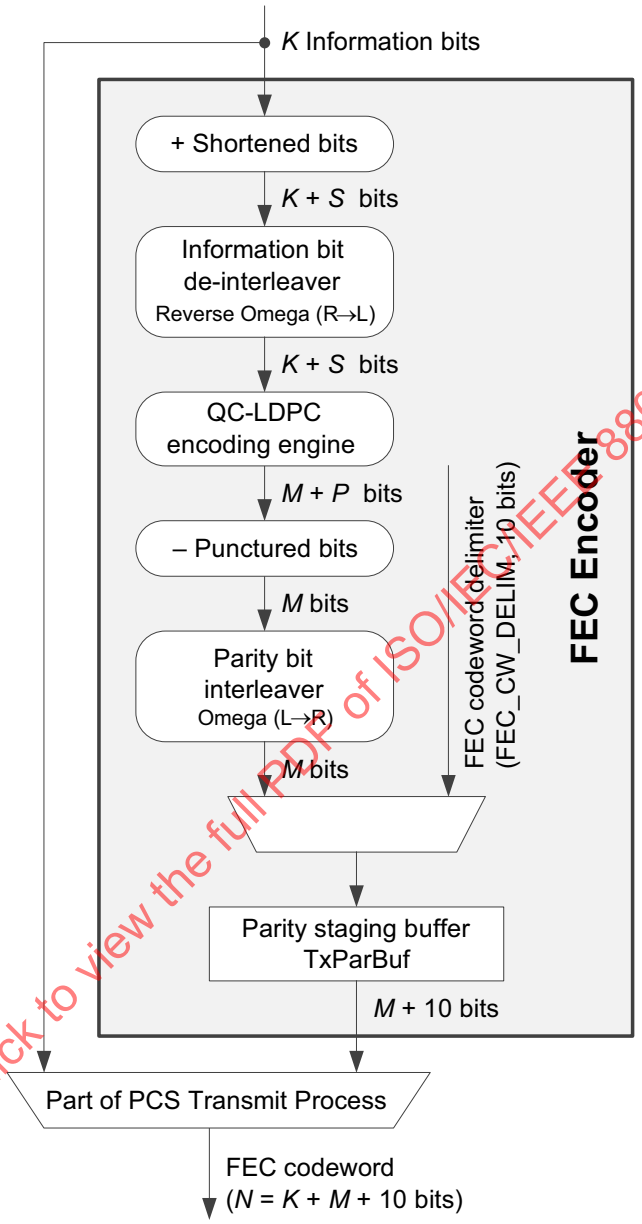


Figure 142–5—FEC encoder

The encoding process therefore shall be as follows:

- A group of K information bits $u = [u_1, u_2, \ldots, u_K]$ are collected and copied to the output of the encoder to form a block of systematic code bits. They are also the input to the zero-padding block.
- A total of S zero padding bits are appended at the end of u to form the full-length information bit block $u^* = [u \mid 0, \ldots, 0]$, which is then sent to the information bit de-interleaver module, which in turn produces the bit-de-interleaved sequence $u'' = \pi^{-1}_{\text{info}}(u^*)$. π^{-1}_{info} represents the de-interleaver mapping of information bits that permutes u^* to u''.
- The de-interleaved QC-LDPC information bits u'' are sent to the QC-LDPC encoding engine, and used to compute parity-check bits p'' with the parity-check matrix H, and p'' is then interleaved to get $p^* = \pi_{\text{parity}}(p'')$. π_{parity} represents the interleaver mapping of parity bits that permutes p'' to p^*.
- $M + P$ parity bits $p^* = [p_1, p_2, \ldots, p_M \mid p_{M+1}, \ldots, p_{M+P}]$ are sent to the puncturing block.
- The last P bits of p^* are truncated, and M parity bits $p = [p_1, p_2, \ldots, p_M]$ are copied to the output of the encoder to form the parity-check bits.
- The FEC codeword without delimiter is $c = [u \mid p] = [u_1, u_2, \ldots, u_K \mid p_1, p_2, \ldots, p_M]$, such that $[u'' \mid p'']\, H^T = 0$.

The QC-LDPC encoder in Figure 142–5 places M bits of FEC parity into the parity staging buffer (TxParBuf) for use by the PCS Transmit process (see 142.2.5.4.3) and the FecParity() function. The buffer comprises 2560 bits of calculated parity along with the 10-bit codeword delimiter (FEC_CW_DELIM). This results in the parity bits assigned to TxParBuf<2559:0> and the 10-bit FEC_CW_DELIM value to TxParBuf<2569:2560>. The transmission order starts with bit 0 and ends with bit 2569.

142.2.4.3 Interleaver

The interleaver and de-interleaver are realized by using Omega networks and reverse Omega networks. An Omega network is a multi-stage interconnection network that uses multiple stages of switches. At each stage, the switches may be controlled independently to “pass-through” or “cross”.

The outputs from each stage are connected to the inputs of the next stage using an interconnection system. The details of interconnection and switch programming are shown in Figure 142–8.

“De-interleaver” refers to the mapping from transmitted sequence to encoding/decoding sequence (including user and parity). This is implemented using “reverse Omega (R→L)” (i.e., data input from the right side and output from the left). “Interleaver” refers to the mapping from encoding/decoding sequence to transmitted sequence. This is implemented as “Omega (L→R)” (i.e., data input from the left side and output from the right). Note that the interleaver and de-interleaver area reverse mapping (permutation) of each other. That is, the Omega and reverse Omega networks are just the reverse of the data flow of each other.

The information bit de-interleaver consists of 57 independent reverse Omega (R→L) networks of size 256 × 256 as illustrated in Figure 142–6. The information bits after zero padding are divided into 57 data chunks, and each data chunk has 256 bits, which is sent to one of the 256 × 256 reverse Omega (R→L) networks.

The parity bit interleaver consists of 10 independent Omega (L→R) networks (see Figure 142–7). Each 256-bit parity-check bit segment is sent to one of the 256 × 256 Omega (L→R) networks. Because the puncturing length is fixed (512) and 512 bits make up two whole data chunks, the last two parity Omega networks [B49a] are bypassed. In implementation, the parity bit interleaver consists of 10 Omega networks.

Note that the interleaver (Omega L→R) and de-interleaver (reverse Omega R→L) are just reverse permutations of each other. To clarify, with the Omega (L→R) network architecture data is input from the left side and output from the right; while the reverse Omega (R→L) network are obtained just by feeding the

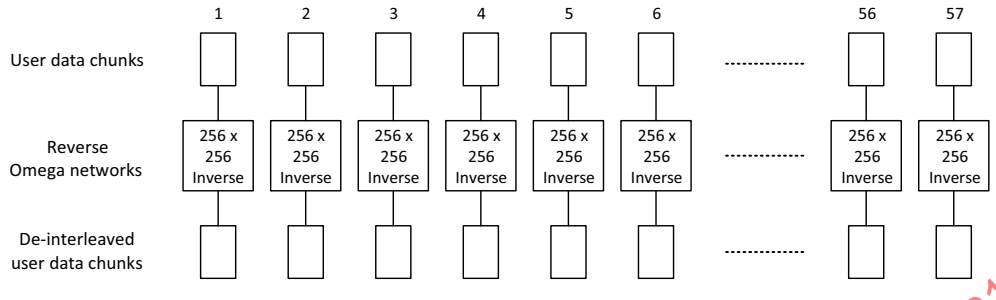


Figure 142–6—Information bit de-interleaver

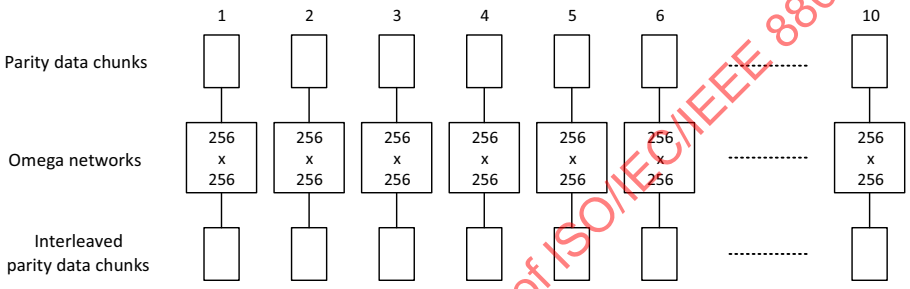


Figure 142–7—Parity bit interleaver

data to the right side and output from the left side. This is illustrated in Figure 142–8 where each Omega network is made of an interconnection network with 8 stages of switches, each stage has 128 switches, and each switch has two inputs and two outputs as shown.

Each switch is individually programmed. If the switch is programmed to be 1, then this switch performs a swap of the input bits, otherwise, the input will be pass-through.

The interconnection between each stage of switches is deterministic and is described as follows. Denote the two output ports of switch i in stage k as $S^k_{i,0}$ and $S^k_{i,1}$, $k = 0, \ldots, 7$ and $i = 0, \ldots, 127$:

— Switch output port at stage k, $S^k_{i,0}$ is connected to switch input port at stage $k + 1$:

$$S^{k+1}_{\left\lfloor \frac{i}{2} \right\rfloor, \mathrm{mod}(i,2)}$$

NOTE—The notation $\lfloor x \rfloor$ represents a floor function, which returns the value of its argument x rounded down to the nearest integer.

— Switch output port at stage k, $S^k_{i,1}$ is connected to switch input port at stage $k + 1$:

$$S^{k+1}_{\left\lfloor \frac{i}{2} \right\rfloor + 64, \mathrm{mod}(i,2)}$$

In implementation one 256 × 256 Omega network of 8 × 128 switches is programmed based on a 128-bit control seed (see Table 142–5 and Table 142–6). The 128-bit switch programming sequence is derived by a circular bit shift of the control seed by x positions where x is given in Table 142–4 for each of the 8 stages.

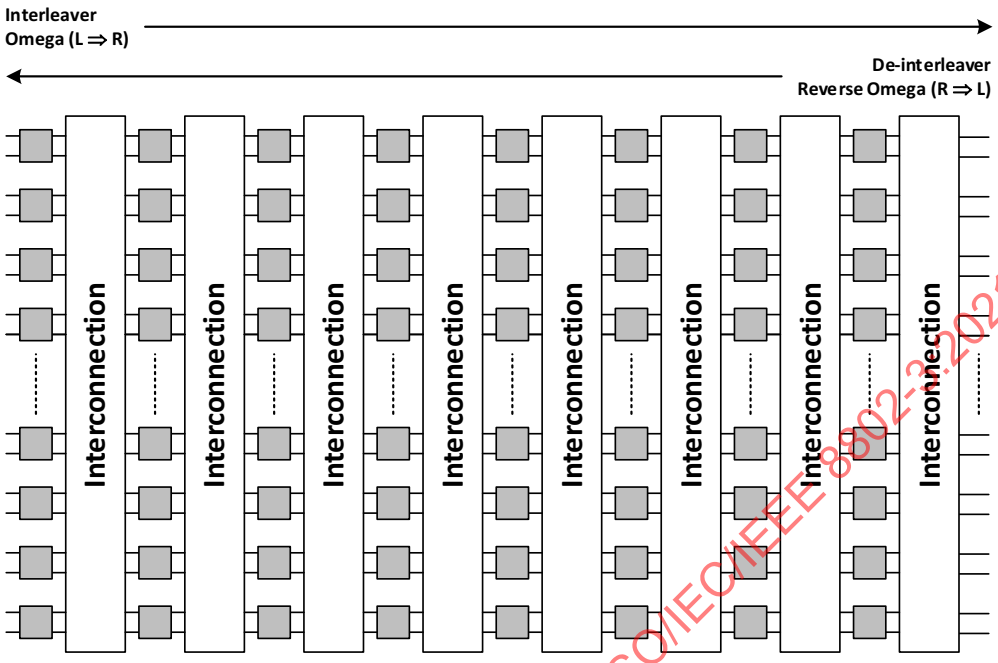


Figure 142–8—Omega network 256 interconnection network

Table 142–4—Control seed circular bit shift for stage 1 through 8

Stage	Circular shift *x* (bits)
1	17
2	34
3	51
4	68
5	85
6	102
7	119
8	8

The control seeds for the 57 independent user Omega networks are shown in Table 142–5 where each row is a 128-bit seed sequence.

The control seeds for the 10 independent parity Omega networks are in Table 142–6 where each row is a 128-bit seed sequence.

NOTE—A file containing the interleaver seeds shown in Table 142–5 and Table 142–6 is available at: http://standards.ieee.org/downloads/802.3/.

Table 142–5—User interleaver control seed values

User interleaver	128-bit control seed sequence (represented by a 32-character hex value)
1	0xE3-88-B0-9A-74-F4-94-8E-5D-C0-CC-8A-18-9A-B9-B2
2	0xC3-0A-B4-F4-92-08-FF-EA-24-FF-17-5D-94-96-70-72
3	0x88-31-C5-46-D3-EC-8B-9F-FF-48-44-9F-A9-4E-8F-20
4	0x92-43-32-87-0C-22-37-A3-E1-06-6A-9F-F8-F2-CC-1E
5	0x90-F6-C1-30-A0-3E-70-CF-60-81-79-53-6C-35-3F-7E
6	0x03-77-AA-71-8A-AC-D3-6D-1B-30-CA-20-D1-56-31-A9
7	0x97-28-EB-4E-AE-3B-93-6C-32-EA-07-9D-F8-18-47-EF
8	0xC1-E5-23-3A-D2-1A-92-00-B7-8B-34-65-90-E1-BD-40
9	0x8F-DC-FC-E6-E3-B0-EA-DF-96-42-7F-93-98-CE-3F-0C
10	0x3F-C4-29-23-C9-01-DE-E0-0B-BB-DD-19-40-B4-13-DA
11	0x42-95-0A-45-CF-AB-F1-6E-86-8D-96-F0-5E-F1-8F-7B
12	0x87-36-32-E9-5D-0D-99-BB-1F-57-46-5C-55-5E-E9-D2
13	0x05-11-38-7F-A6-EB-93-A2-43-91-96-F1-9C-EE-67-3A
14	0x4C-EF-11-A0-1D-FB-A0-5E-C0-01-9E-80-78-C1-B5-88
15	0x40-7C-C3-9F-D5-DE-6C-9A-C2-C0-1E-3B-45-FB-EE-B2
16	0xAE-FC-16-6F-9D-15-ED-E0-8C-7F-2B-14-74-85-36-14
17	0x8E-6D-B3-3B-C7-C8-9A-F9-08-AD-1D-C3-63-37-9B-43
18	0xE7-E0-B9-86-90-29-7B-7C-68-D8-6B-0E-52-79-8F-4F
19	0xA1-F1-78-71-4B-B7-D3-6B-13-41-90-A4-68-1C-88-8A
20	0x51-BD-15-AB-A9-88-5B-F8-11-C0-97-5C-FC-1B-65-E1
21	0xDA-5C-9A-8E-A2-F8-93-53-D9-F0-68-A5-F8-7F-2D-8E
22	0x31-69-A5-9D-01-B3-CD-B1-27-0C-8C-B5-E8-F7-A2-D2
23	0x04-E2-36-BE-89-46-7E-08-D5-63-DA-41-67-A2-DC-A5
24	0x4E-BB-16-BF-E6-19-C8-E3-44-98-AF-C4-88-18-53-B0
25	0xEF-BB-12-28-66-47-EC-22-C7-1D-F6-49-6F-BE-A0-3A
26	0x63-0F-7E-0F-AF-3C-47-15-2D-A7-20-E0-D2-EC-69-61
27	0x7C-3D-14-A5-BE-9E-E4-A4-71-64-BF-1B-71-C5-3E-D6
28	0xA4-66-0B-F8-27-EB-63-A4-C1-29-69-EC-81-D4-C0-89
29	0xF6-30-95-91-A5-F5-ED-B0-33-39-B6-72-75-CC-B1-93
30	0x13-93-BD-21-44-16-85-C3-5F-A1-A3-DE-89-A7-5B-A2
31	0xE2-32-7B-D2-31-11-CB-0E-D1-54-CC-59-E0-A4-55-4B
32	0x54-AC-4C-7E-58-74-32-DF-CE-54-F6-AE-65-F7-54-F8
33	0x7E-D1-D3-B8-7D-3A-1D-EF-DF-13-70-FB-6D-AF-79-49

Table 142–5—User interleaver control seed values *(continued)*

User interleaver	128-bit control seed sequence (represented by a 32-character hex value)
34	0x27-CC-FF-46-F2-C9-4A-45-A9-35-80-D2-44-69-A4-CE
35	0x99-27-52-B8-96-3F-C0-90-98-9F-6D-A0-7C-FC-D3-B3
36	0x13-D3-9E-3C-5A-B4-AD-76-CF-8B-82-5F-E9-02-A5-EA
37	0xB3-AD-1C-D1-ED-F5-17-4B-AF-4B-07-54-F6-30-5E-81
38	0x22-76-62-36-B9-92-4F-83-AB-04-E7-37-B6-4C-D2-7D
39	0x5F-3C-DE-A1-05-AE-02-99-24-CC-A2-89-8D-57-C3-E7
40	0xAF-E4-7D-A0-B9-F6-CC-51-2D-B8-C9-FD-B6-8A-E9-B2
41	0x94-E7-58-DF-61-7B-DA-BF-C0-C4-72-15-C7-76-99-5C
42	0x34-64-0A-89-2E-46-63-46-C0-A8-26-FD-46-60-F3-C7
43	0x89-54-48-83-50-C6-B4-72-35-F4-C8-47-6C-2B-D2-50
44	0xFB-68-B2-9B-CA-E6-F1-50-4B-ED-AA-C9-9F-DC-77-66
45	0x08-34-F8-F3-5F-4A-B4-E5-49-85-F1-C7-91-BF-A7-6A
46	0x9D-C7-37-D5-C6-91-7C-D0-60-CC-66-3A-AF-A6-A7-91
47	0x01-89-6B-6C-8C-6E-35-B5-12-B4-BB-BC-41-AA-DF-EC
48	0xF0-73-F8-02-02-9B-8B-38-1B-78-F2-70-51-96-2A-5C
49	0x67-AE-64-C5-1B-B3-B0-CE-E6-89-B1-6F-B3-57-8C-80
50	0x84-C3-F1-40-85-82-DE-32-FB-43-EF-1C-A0-02-15-D4
51	0x6E-73-3D-34-85-62-EF-E1-F1-8F-C6-09-6D-19-B9-5A
52	0x57-89-78-DB-42-D9-19-C5-11-2A-79-B4-77-F7-E4-28
53	0x87-03-83-E6-F6-C6-A0-F3-D5-65-84-63-83-07-42-4A
54	0x4F-B7-69-FC-30-0E-5A-5B-0E-E8-D8-97-68-43-F0-74
55	0xCF-AF-92-E6-AA-BF-CE-5C-B3-F2-2E-03-02-F1-C8-EC
56	0x43-29-FB-56-A6-57-01-9F-91-3F-BA-7A-B0-A5-7F-B3
57	0x1C-61-92-BE-C8-C3-FA-E3-B5-8B-B8-D0-7A-9B-B1-D7

Table 142–6—Parity interleaver control seed values

Parity interleaver	128-bit control seed sequence (represented by a 32-character hex value)
1	0x11-C7-DC-59-9A-61-76-D9-E3-44-BF-75-2E-AA-34-AF
2	0x5F-5C-F0-20-9A-E9-B4-4B-CD-F9-52-C8-22-8D-F0-89
3	0x89-34-9C-4B-F1-90-13-0B-F8-BE-47-6B-29-BB-96-3C
4	0xA2-6D-3B-8D-CC-B1-D9-C4-5E-FC-11-9F-AE-07-A6-C6
5	0xAC-45-29-CC-E5-2C-C7-D0-60-47-ED-32-76-4F-84-7B
6	0x92-3A-DC-97-5B-23-62-9A-FB-81-BE-93-EC-AB-25-BF
7	0x2C-4D-73-01-D3-01-D8-B8-9A-73-4A-3F-0A-E4-B6-F5
8	0xEF-CA-A9-2F-10-18-34-42-46-D4-BD-83-48-59-6A-BE
9	0x72-18-53-70-16-E0-84-4B-8E-D7-96-F8-07-AA-A5-8D
10	0x4D-F0-5D-35-75-9E-07-C9-56-6E-B1-4F-2B-22-43-90

142.2.5 Transmit data path state diagrams

Various variables and buffers in the PCS are structured as 258-bit wide blocks. Bits 0 through 256 of each 258-bit block hold one line-coding unit (a 257-bit block) and bit 257 indicates the 257-bit block has been scrambled and transcoded (bit 257 is equal to 1) or that the block has not been scrambled and transcoded (bit 257 is equal to 0). The value of bit 257 also implies the origin of the block as being either the PCS Input process (bit 257 is equal to 1) or the PCS Framer process (bit 257 is equal to 0).

142.2.5.1 Constants

EBD258
: Type: 258-bit block
Description: The EBD258 constant holds the value of the end-of-burst delimiter.
Value: EBD257 (see 142.3.5.1) with a bit having value 0 appended as MSB

FEC_CW_DELIM
: Type: 10-bit block
Description: The codeword delimiter bit pattern found at the end of each FEC parity block.
Value: 0x3-CA

FEC_PARITY_SIZE
: Type: Integer
Description: The FEC_PARITY_SIZE constant indicates the size of the parity portion of a FEC codeword.
Value: 10
Unit: 257-bit block

FEC_PAYLOAD_SIZE
Type: Integer
Description: The FEC_PAYLOAD_SIZE constant indicates the size of the payload portion of a FEC codeword.
Value: 56
Unit: 257-bit block

IBI258
Type: 258-bit block
Description: The IBI258 constant represents an inter-burst idle block that is generated by the PCS Framer process in the absence of any burst framing blocks, data blocks, or FEC parity blocks.
Value: $0x0\text{-}(0A)_{32}$

IBI_EQ
See 143.3.3.3

PAR_PLACEHLDR
Type: 258-bit block
Description: The PAR_PLACEHLDR constant represents the value of a 258-bit block inserted into the data stream by the PCS Framer process in order to reserve the location where FEC parity and the 10-bit FEC codeword delimiter is to be inserted into the data stream by the PCS Transmit process.
Value: $0x0\text{-}(09)_{32}$

RATE_ADJ_EQ
See 143.3.3.3

SCRAMBLED
Type: binary
Description: This constant indicates that the contents of the 257-bit block are scrambled. When the bit TxInput<257> or TxOutput<257> is set to 1, then bits TxInput<256:0> or TxOutput<256:0> in the same block carry scrambled data.
Value: 1

142.2.5.2 Variables

BEGIN
TYPE: Boolean
Description: This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset, and it is reset to false on read.

ClkIn
Type: Boolean
Description: The clear-on-read variable ClkIn is set to true on each rising edge of the xMII clock.

ClkOut
Type: Boolean
Description: The clear-on-read variable ClkOut is set to true once for each 257-bit block output by the PMA, i.e., the ClkOut tracks the transmit clock of the corresponding PMA channel (see 142.4.4).

ClkXfr

Type: Boolean

Description: The clear-on-read variable ClkXfr is set to true once for each 257-bit block output by the PMA, i.e., the ClkXfr tracks the transmit clock of the corresponding PMA channel (see 142.4.4).

InputFifo[]

Type: array of 258-bit blocks

Description: The InputFifo receives data from the PCS Input process and hands it off to the PCS Framer process. Its primary function is to absorb data while the PCS is transmitting burst overhead or FEC parity. This FIFO holds SpLength elements and supports FIFO access operations as defined in 142.1.1.6.

TxParBuf

Type: 2570-bit block

Description: This variable holds the 2560-bit calculated parity value along with the 10-bit FEC_CW_DELIM value (see 142.2.5.1). The total size of 2570 bits represents the same size as ten 257-bit line encoding blocks.

TxFifo[]

Type: array of 258-bit blocks

Description: The TxFifo holds information queued by the Framer process for output by the PCS and enforces a fixed delay that is implementation dependent. The fixed delay ensures the PHY has sufficient time to generate FEC parity given that the Framer process inserts SpLength 257-bit blocks at the beginning of the burst. This FIFO holds either (FEC_DELAY – SpLength) or two elements, whichever is greater. The TxFifo supports FIFO access operations as defined in 142.1.1.6.

ParityLeft

Type: Integer

Description: The ParityLeft variable indicates the number of 257-bit parity blocks needed to complete the current FEC codeword being processed by the PCS Framer process.

PayloadLeft

Type: Integer

Description: The PayloadLeft variable indicates the number of 257-bit payload blocks needed to complete the current FEC codeword being processed by the PCS Framer process.

SyncPattern[]

Type: array of 258-bit blocks

Description: The SyncPattern array is set to the provisioned value of the synchronization pattern as determined by the most recent settings of SP1, SP2, SP3, and their corresponding length parameters by the MPCP. The MSB of each cell is set to zero, indicating the 257-bit block has not been scrambled and transcoded.

SpLength

Type: unsigned integer

Description: The SpLength variable represents the length of the synchronization pattern as determined by the sum of the most recent settings of SP1Length, SP2Length, and SP3Length provisioned in an ONU (see 144.3.6.4 and 144.3.6.6).

SpIndex
Type: integer
Description: The SpIndex variable is a pointer into the SyncPattern array that indicates which 258-bit block from the array is sent to the TxFifo.

Transmitting
Type: Boolean
Description: The Transmitting variable indicates whether the device is transmitting or not.

TxInput
Type: 258-bit block
Description: This variable holds one transcoded 257-bit block prepended with a binary 1 indicating the 257-bit block has been scrambled and transcoded.

TxNext
Type: 72-bit block
Description: The next 72-bit block to be processed by the PCS Input process.

TxLast
Type: 258-bit block
Description: This variable holds the 258-bit that was read from TxFifo in the previous ClkOut cycle.

TxOutput
Type: 258-bit block
Description: This variable holds one 258-bit block retrieved from the TxFifo.

TxPrev
Type: 72-bit block
Description: This variable holds one 72-bit block received by the PCS Input process from the xMII in the previous ClkIn cycle.

xBuffer[]
Type: array of 66-bit blocks
Description: This buffer holds four 66-bit blocks of 64B/66B encoded data to be transcoded into one 257-bit block.

xIndex
Type: Integer
Description: An index into the xBuffer indicating the number of encoded blocks contained in the buffer that are ready to be transcoded.

142.2.5.3 Functions

FecParity()
Upon initiation, the first call to this function returns a block containing the first 257 bits from the TxParBuf, i.e., TxParBuf<256:0>. Each subsequent call returns the subsequent 257 bits from the buffer. On the 10th call, the last 257 bits are returned, i.e., TxParBuf<2569:2312>, and the function resets to return TxParBuf<256:0> on the next call. This emulates a circular buffer of size 10 × 257 bits.

Encode(v)
This function performs 64B/66B encoding of a 72-bit block v per 49.2.13.2.3 and returns the result.

PassToFecEncoder(v)
: This function passes a 257-bit block v to the FEC engine for calculating the LDPC code parity.

NextTxVector()
: This function returns a 72-bit block carrying a single EQ as shown in Figure 142–2. The block is constructed from the data received from the xMII over two subsequent 36-bit transfers: the first transfer is on rising TX_CLK edge and the second transfer is on the falling TX_CLK edge.

PassToPMA(v)
: This function passes a 257-bit block v to the PMA using PMA_UNITDATA[*i*].request(v) (see 142.4.1.1).

ResetScrambler()
: Description: This function resets the scrambler to the value of $0x3\text{-}(FF)_7$, i.e., each of the bits S0 through S57 of the scrambler shift register is set to 1 (see Figure 49–8).

Scramble(blk)
: This function accepts one 66-bit block blk and performs the scrambling operation on the 64-bit payload of the block, as described in 49.2.6. The returned value is a scrambled 66-bit block.

Transcode(a[4])
: This function transcodes four 64B/66B-encoded blocks into a single 256B/257B encoded block per 91.5.2.5 and returns the result. It takes four 64B/66B encoded blocks a[4] as an argument and returns a 257-bit block.

142.2.5.4 State diagrams

142.2.5.4.1 PCS Input process

The PCS Input process accepts two consecutive 36-bit transfers from the xMII interface and converts them into a single 72-bit block. The Input process discards all RATE_ADJ_EQs to allow for insertion of FEC parity blocks by the PCS Transmit process (see 142.2.5.4.3). IBI_EQs not required to complete a 256B/257B block at the end of an upstream burst are also discarded by the Input process. All other 72-bit blocks are encoded into 64B/66B blocks. Four 64B/66B blocks are accumulated, scrambled, and transcoded into a single 256B/257B block and copied to the FEC encoder. A single bit indicating the accompanying 256B/257B block has been scrambled and transcoded is appended to the block that is then stored in the InputFifo.

The PCS Input process shall implement the state diagram as depicted in Figure 142–9.

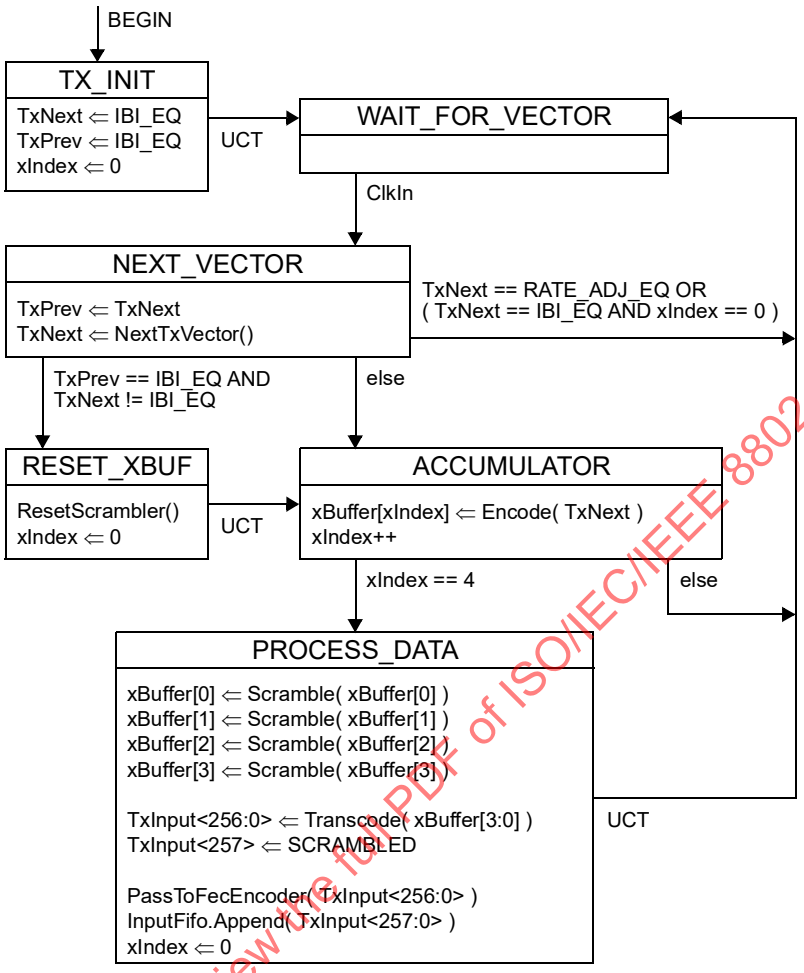


Figure 142–9—PCS Input process state diagram

142.2.5.4.2 PCS Framer process

The PCS Framer process monitors data from the InputFifo and transfers it to the TxFifo, inserting inter-burst idle blocks (IBI258), SyncPattern, parity placeholders (PAR_PLACEHLDR), and EBD258 as appropriate. While the InputFifo is empty, the PCS Framer process appends IBI258 to the TxFifo. When the InputFifo first becomes not empty, indicating the beginning of a burst, the SyncPattern is appended to the TxFifo. Once the complete SyncPattern is appended to the TxFifo, the Framer process begins transferring data from the InputFifo to the TxFifo. When sufficient data for a full FEC payload has been transferred to the TxFifo, or the end of the burst is detected as indicated by an empty InputFifo, the PCS Framer process appends sufficient PAR_PLACEHLDR blocks to the TxFifo to allow insertion of the contents of TxParBuf (FEC codeword parity and FEC codeword delimiter) into the data stream by the PCS Transmit process. Additional FEC codewords are allowed for until the end of the transmission is indicated by an empty InputFifo, at which point the Framer process appends the EBD258 to the TxFifo followed by IBI258.

The PCS Framer process shall implement the state diagram as depicted in Figure 142–10.

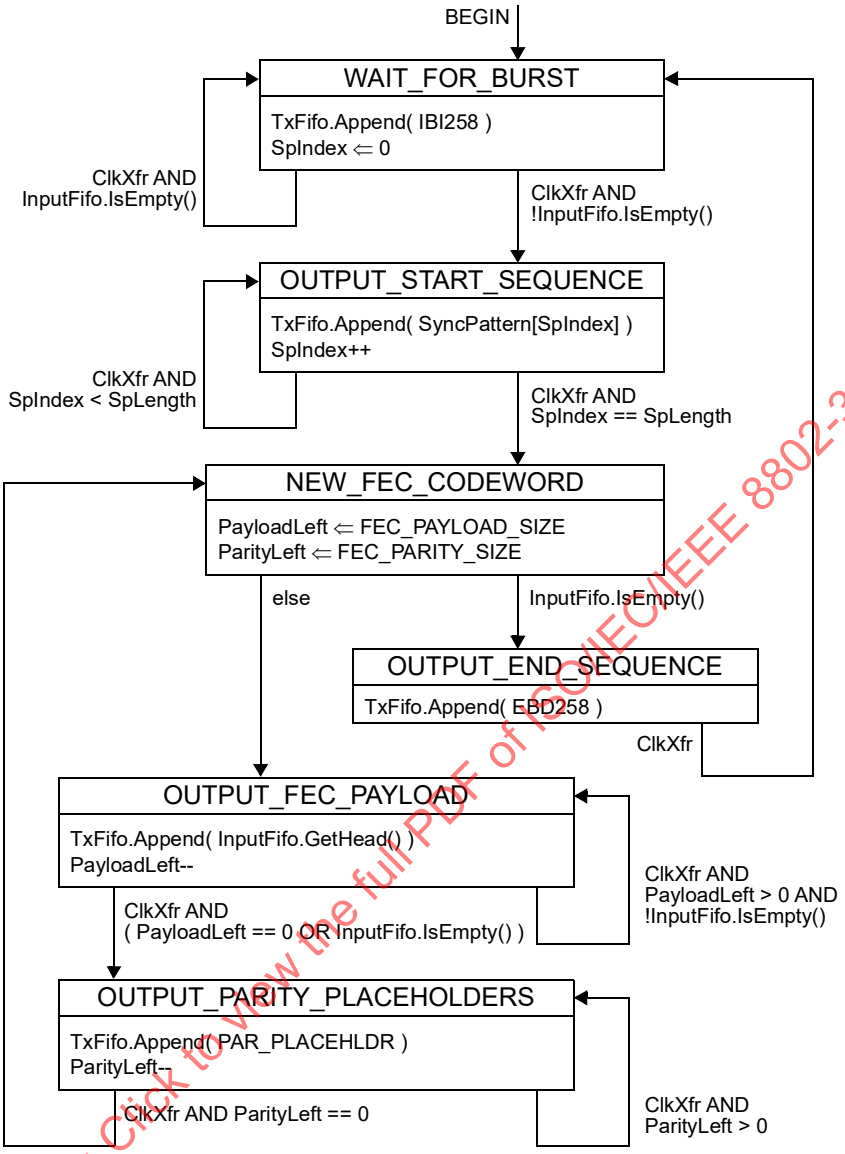


Figure 142–10—PCS Framer process state diagram

142.2.5.4.3 PCS Transmit process

The PCS Transmit process transfers data from the TxFifo or FEC encoder to the PMA. On each transition of the ClkOut to true the Transmit process retrieves one 258-bit block of data from the TxFifo. If the retrieved 258-bit block indicates the start of the burst and the ONU is currently not transmitting, the laser is turned on and data is sent towards the PMA for transmission. If the retrieved 258-bit block indicates the end of the burst and the ONU is currently transmitting, the laser is turned off and end of the burst delimiter is sent towards the PMA for transmission. If the retrieved 258-bit block indicates the FEC parity placeholder, the calculated FEC parity and 10 bits of FEC codeword delimiter are sent towards the PMA for transmission. Otherwise, data from the TxFifo is sent towards the PMA for transmission.

The PCS Transmit process shall implement the state diagram as depicted in Figure 142–11.

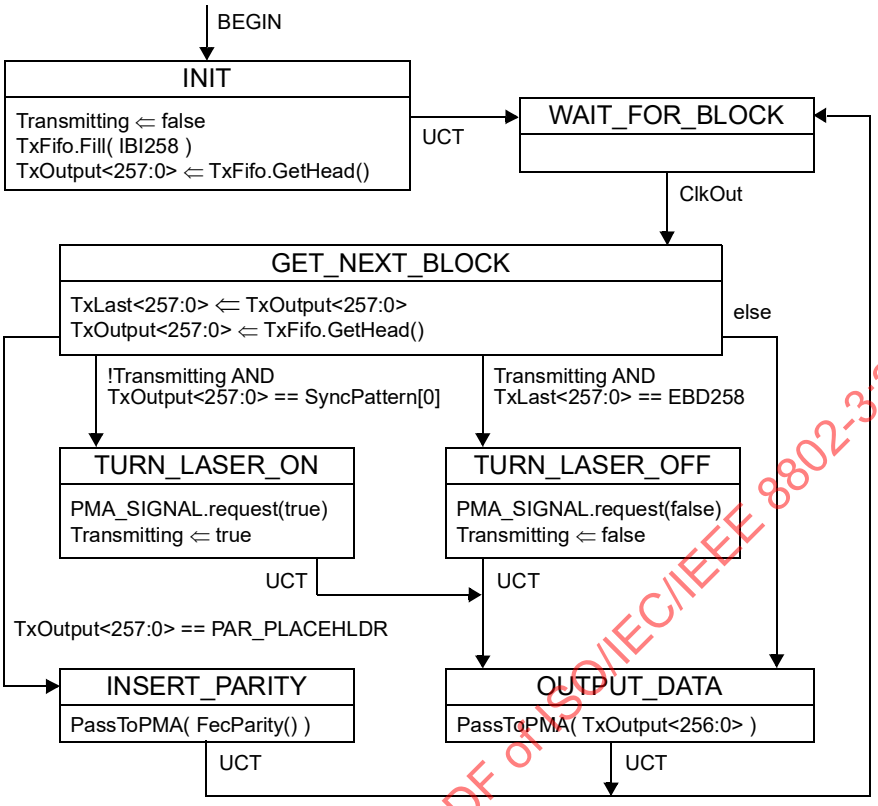


Figure 142–11—PCS Transmit state diagram

142.3 PCS receive data path

This subclause defines the PCS receive data path. In the ONU, the PCS receive data path operates in a continuous mode at a 25.78125 GBd rate. In the OLT, the PCS receive data path operates in burst mode at a 25.78125 GBd rate (25/25G-EPON, 50/25G-EPON, and 50/50G-EPON) or at a 10.3125 GBd rate (25/10G-EPON and 50/10G-EPON). The PCS receive data path includes a mandatory QC-LDPC FEC decoder (see 142.3.1.1).

The functional block diagram for the PCS receive data path is shown in Figure 142–2 and consists of the following processes:

— PCS Synchronizer process (see 142.3.5.4 and 142.3.5.5)
— PCS BER Monitor process (see 142.3.5.6)
— PCS Output process (see 142.3.5.7)

142.3.1 FEC decoder

Figure 142–12 illustrates the receiver QC-LDPC decoder with shortening/puncturing, interleaver/de-interleaver data path.

142.3.1.1 Receive interleaving

See 142.2.4.3.

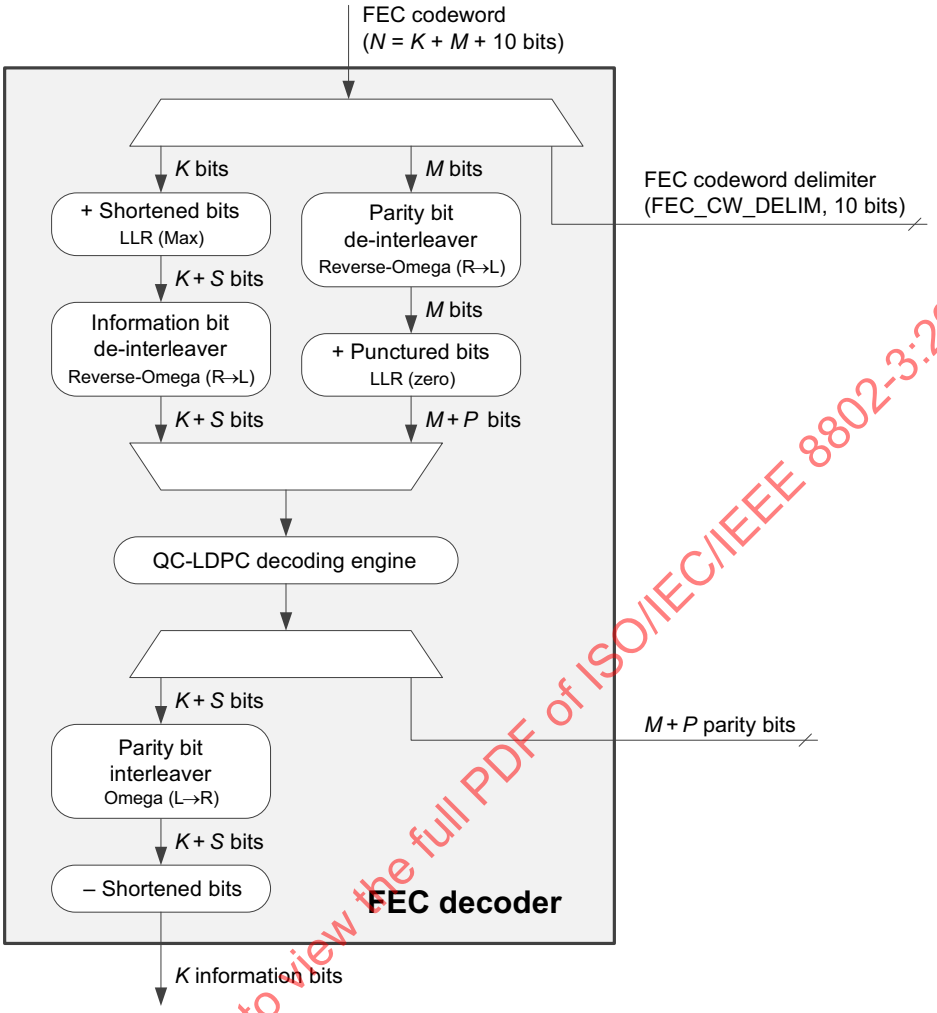


Figure 142–12—FEC decoder

142.3.2 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder converts one scrambled 257-bit block received from the FEC decoder into four consecutive scrambled 66-bit blocks as described in 91.5.3.5 and returns the result to the PCS Output process.

142.3.3 Descrambler

The PCS uses the descrambler specified in 49.2.10.

In the OLT, at the beginning of each burst, the descrambler is reset to a known initialization value (see the definition of ResetDescrambler() function in 142.3.5.3).

142.3.4 64B/66B decoder

See 49.2.11. The 64B/66B decoder shall perform functions specified in the state diagram shown in Figure 49–17. The PCS bit reception order is illustrated in Figure 142–13.

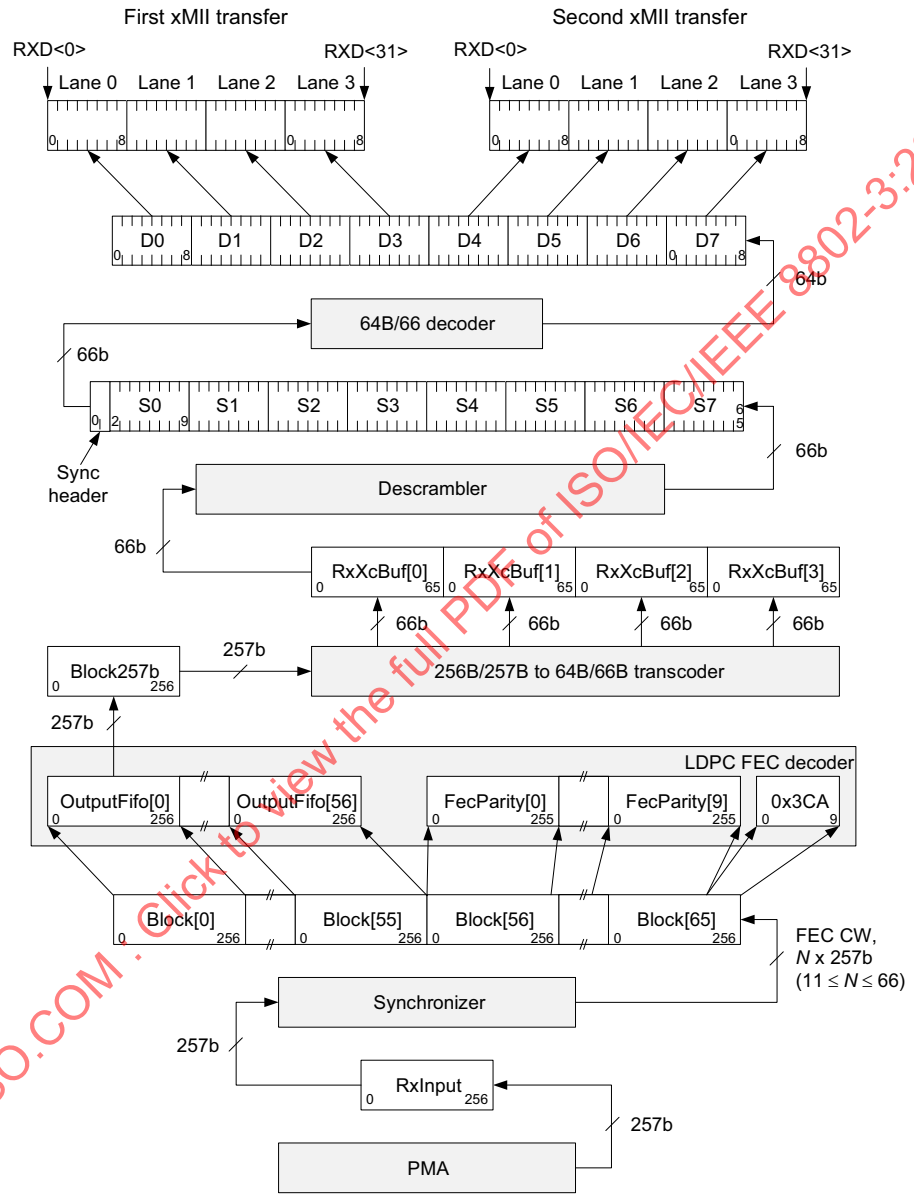


Figure 142–13—PCS receive bit ordering

142.3.5 Receive data path state diagrams

142.3.5.1 Constants

EBD257
Type: 257-bit block
Description: The EBD257 constant holds the value of the end-of-burst delimiter.
Value: 0x00

EBD_TH
Type: Integer
Description: The EBD_TH constant holds the value of the Hamming threshold required to match the end-of-burst delimiter.
Value: 36

FEC_CW_DELIM
See 142.2.5.1

FEC_PAYLOAD_SIZE
See 142.2.5.1

FEC_CW_BIT_SZ
Type: Integer
Description: This constant represents the size of a full-length FEC codeword in bits.
Value: 16 962 (i.e., 257 × 66)

IBI_EQ
See 143.3.3.3.

MATCH_TARGET
Type: Integer
Description: The number of FEC codeword delimiters required to match in order to declare the block alignment in the ONU (i.e., in the continuous reception mode).
Value: 4

PCS_BLK_SZ
Type: Unsigned integer
Description: The PCS_BLK_SZ constant holds the size of the PCS data block.
Value: 257
Unit: bits

RATE_ADJ_EQ
See 143.3.3.3

RATE_ADJ_SIZE
See 143.3.3.3

SBD_TH
Type: Integer
Description: The SBD_TH constant holds the value of the Hamming threshold required to match the start-of-burst delimiter.
Value: 60

142.3.5.2 Variables

All variable definitions in this section assume an independent instance of the variable per each enabled receive channel.

BadCwCount
: Counts the number of invalid QC-LDPC codewords within the current BER monitoring interval period.

BEGIN
: See 142.2.5.2

BerMonitorInterval
: Indicates the length of the interval window period associated with the QC-LDPC BER Monitor in units of QC-LDPC codewords (see 45.2.3.43). This value is reflected in MDIO register 3.80.

BerThreshold
: Indicates the threshold value of invalid QC-LDPC codeword errors within the QC-LDPC BER Monitor function. At the end of each monitor interval period, HiBer is updated. The value of BerThreshold is reflected in MDIO register 3.82

Block257b
: Type: 257-bit block
Description: The Block257b variable temporarily holds one 257-bit block removed from the head of OutputFifo.

Block66b
: Type: 66-bit block
Description: The Block66b variable temporarily holds one descrambled 66-bit block.

Block72b
: Type: 72-bit block
Description: The Block72b variable temporarily holds the value being passed to the xMII.

CwAvailable
: Boolean variable that is set true when a new QC-LDPC codeword is available for testing by the BER Monitor process and set to false when the WAIT_FOR_CODEWORD state is entered. A new QC-LDPC codeword is available for testing by the BER Monitor process when the ONU Synchronizer process has accumulated enough blocks from the PMA to evaluate the next QC-LDPC codeword (see Figure 142–15).

CwLeft
: Counts the remaining number of QC-LDPC codewords within the current BER monitoring interval.

CwValid
: Boolean indication that is set true if a received QC-LDPC codeword is valid. As an example, a QC-LDPC codeword is valid if and only if all parity checks of the QC-LDPC code are satisfied thereby terminating iterations without exceeding the maximum count (e.g., 15). The specific method for evaluating codeword validity is implementation dependent within the QC-LDPC decoder and outside the scope of this standard.

HiBer

Boolean variable that is asserted true if BadCwCount reaches or exceeds BerThreshold QC-LDPC codeword errors within one BER monitor interval period, otherwise set to false. The value of HiBer is reflected in MDIO register 3.81.

MatchCount

Type: Integer
Description: This counter tracks the number of consecutive successful detections of FEC codeword delimiters (FEC_CW_DELIM) while the ONU is not synchronized to the proper 257-bit block boundary.

OutputFifo[]

Type: Array of 257-bit blocks
Description: The OutputFifo buffer holds one FEC codeword payload after it has been processed by the FEC decoder. The OutputFifo supports FIFO access operations as defined in 142.1.1.6.

PayloadLeft

Type: Integer
Description: This variable holds the number of EQs remaining until one maximum-length FEC codeword payload has been sent to the xMII.

PersistentFecFail

Type: Boolean
Description: This variable is set to true if the FEC decoder is unable to correct all errors in the three FEC codewords most recently received on a given channel. Otherwise, this variable is set to false. In the OLT, the PersistentFecFail value is reset when SignalFail becomes true, or the EBD is detected, i.e., the uncorrectable FEC codewords from the previous burst do not result in PersistentFecFail becoming true during the next burst.

RateAdjLeft

Type: Integer
Description: This variable holds the number of EQs remaining to be generated in the PCS Output process to fill the gap left by the removal of FEC codeword parity data from the current FEC codeword.

RxCwBuf[]

Type: An array of 257-bit blocks
Description: The RxCwBuf is a buffer capable of storing one full FEC codeword. The RxCwBuf supports FIFO access operations as defined in 142.1.1.6.

RxInput

Type: 257-bit block
Description: The RxInput is a buffer containing the 257 bits most recently received from the PMA sublayer on a given channel.

RxXcBuf[3:0]

Type: Array of four 66-bit blocks
Description: This buffer holds four 66-bit blocks resulting from the decoding of a 257-bit block.

SBD257

Type: 257-bit block
Description: The SBD257 variable represents the start-of-burst delimiter, and its value is equal to SP3 for the most recently provisioned synchronization pattern (see 142.1.3.1).
Value: see 142.1.3.1

SignalFail
Type: Boolean
Description: This Boolean variable is set based on the most recently received value of PMA_SIGNAL.indication(SIGNAL_OK) received on a given channel. It is true if the value of SIGNAL_OK was FAIL and false if the value was OK.

XcIndex
Type: Integer
Description: The XcIndex variable is an index to the RxXcBuf array and has a value ranging between 0 and 3, inclusive.

142.3.5.3 Functions

Decode257b(blk)
Description: This function accepts one 256B/257B encoded block blk and transcodes it into four 64B/66B encoded blocks. The result is returned as an array of four 66-bit blocks.

Decode66b(blk)
Description: This function accepts one 64B/66B encoded block blk and performs the decoding operation as described in 49.2.11 and Figure 49–17. The returned value is a 72-bit block.

Descramble(blk)
Description: This function accepts one 66-bit block blk and performs the descrambling operation on the 64-bit payload of the block, as described in 49.2.10. The returned value is a descrambled 66-bit block.

PassToFecDecoder(cw)
Description: The PassToFecDecoder function passes one complete FEC codeword cw to the FEC decoder. The FEC codeword may be full-length or shortened. The codeword length is intrinsic to the parameter cw.

MatchFound(value1, value2, threshold)
Description: This function compares bit by bit its arguments value1 and value2 and returns a Boolean true if the number of bits that are different is less or equal to the threshold, otherwise the function returns false.

OutputBlock(eq)
Description: This function accepts one 72-bit block eq and outputs two 36-bit blocks over the xMII. This is a blocking function and the control is not returned to the calling state until after the second 36-bit block is sent.

ResetDescrambler()
Description: This function resets the descrambler to the value of $0x3\text{-}(FF)_7$, i.e., each of the bits S0 through S57 of the descrambler shift register is set to 1 (see Figure 49–10).

Shift(buffer, *n*)
Description: This function receives 257-bit blocks from the PMA via the PMA_UNITDATA.indication(rx_code_group<256:0>) primitive and inserts *n* new bits at the end of the FIFO buffer, while removing the same number of old bits at the head of the buffer. The Shift() function is blocking and its execution takes exactly *n* bit times at the given receiving line rate.

142.3.5.4 OLT Synchronizer process state diagram

The OLT Synchronizer process is responsible for receiving unaligned 257-bit blocks from the PMA sublayer and aligning these blocks to the correct 257-bit block boundary. This process hunts for SBD257 and EBD257 values, allowing for a certain Hamming distance (see SBD_TH and EBD_TH). The 257-bit blocks that are received between the SBD and the EBD are accumulated in the RxCwBuf buffer. When a complete full-length or shortened FEC codeword is stored in the RxCwBuf, the buffer content is passed to the FEC decoder function (see 142.3.1).

The OLT shall implement an instance of the Synchronizer process as depicted in Figure 142–14 for every enabled receive channel.

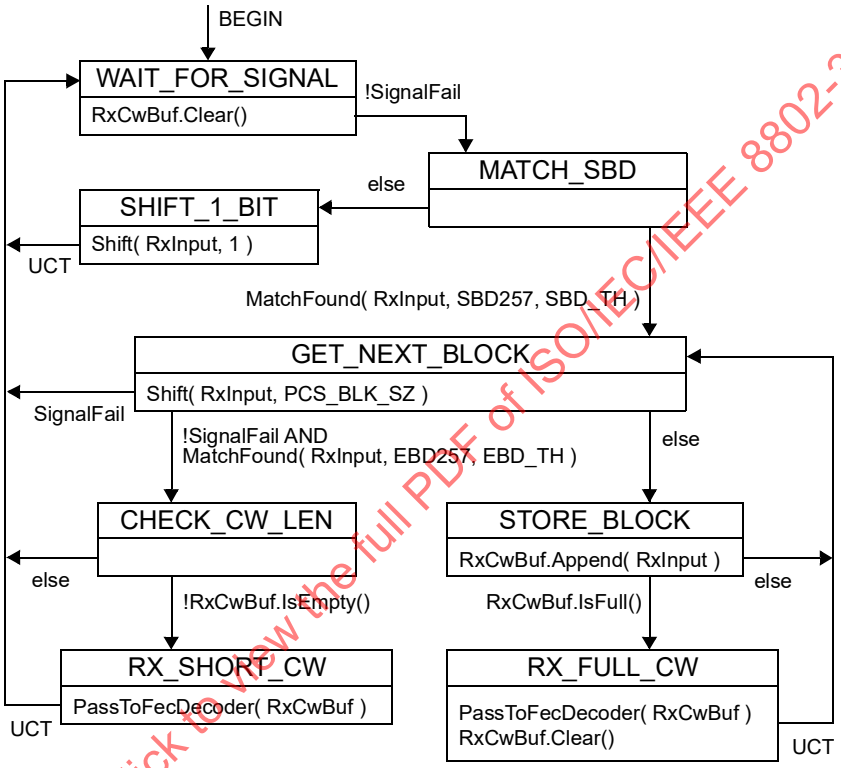


Figure 142–14—OLT Synchronizer process state diagram

142.3.5.5 ONU Synchronizer process state diagram

The ONU Synchronizer process is responsible for receiving unaligned 257-bit blocks from the PMA sublayer and aligning these blocks to the correct 257-bit block boundary. This process hunts for 10-bit FEC codeword delimiters FEC_CW_DELIM. The delimiter is expected to have the exact match and the block alignment is declared when the FEC_CW_DELIM values are matched MATCH_TARGET times and are exactly one FEC codeword size apart.

The received blocks are accumulated in the RxCwBuf buffer. When a complete full-length FEC codeword is stored in the RxCwBuf, the buffer content is passed to the FEC decoder function (see 142.3.1). In the ONU receive path, shortened FEC codewords are disallowed.

The ONU shall implement an instance of the Synchronizer process as depicted in Figure 142–15 for every enabled receive channel.

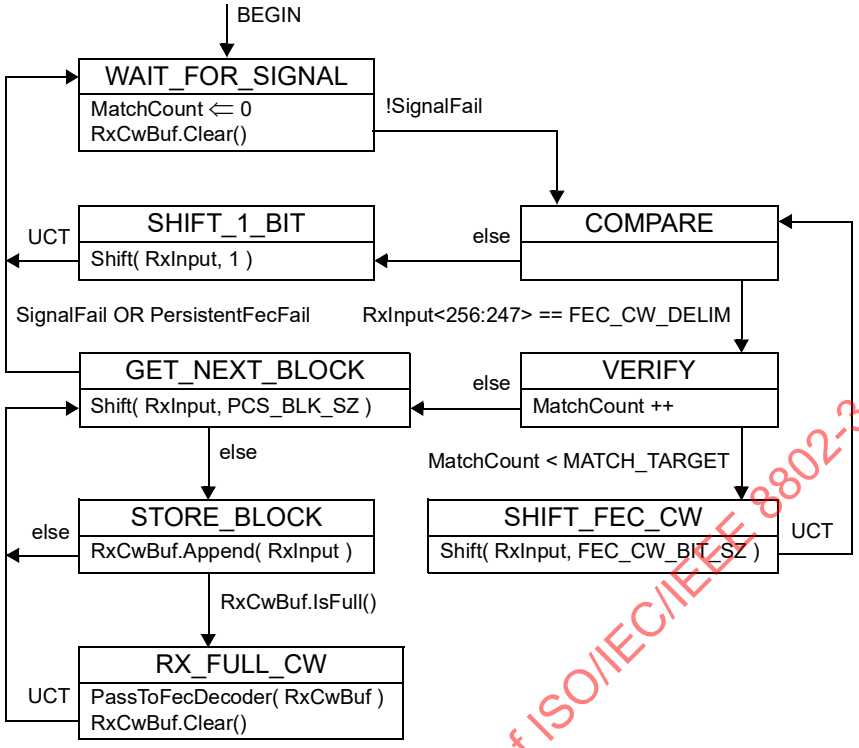


Figure 142–15—ONU Synchronizer process state diagram

142.3.5.6 PCS ONU BER Monitor process

When the ONU Synchronizer process has obtained block synchronization, the QC-LDPC BER Monitor process monitors the signal quality, asserting HiBer if a count of QC-LDPC parity errors reaches BerThreshold within the timer interval. The ONU shall implement an instance of the QC-LDPC BER Monitor shown in Figure 142–16 for each active downstream channel.

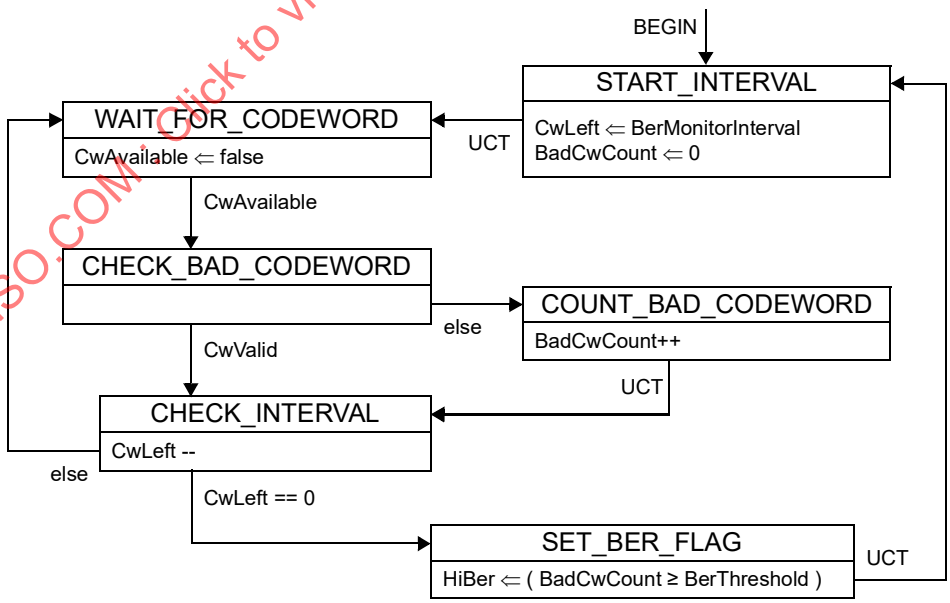


Figure 142–16—QC-LDPC BER Monitor state diagram (ONU only)

142.3.5.7 PCS Output process

The PCS Output process receives corrected information bits from the FEC decoder. The FEC decoder outputs an entire payload of a FEC codeword into the OutputFifo buffer. The FEC codeword payload consists of 56 257-bit blocks, however, in the OLT, the payload of a last codeword in a burst may contain fewer than 56 blocks.

The PCS Output process converts the 257-bit blocks into EQs by first transcoding each 257-bit block into four 66-bit blocks, then descrambling each block, and finally, decoding each 66-bit block into a 72-bit block. The 72-bit blocks are passed to xMII for transfer to the MCRS.

The PCS shall implement an instance of the Output process as depicted in Figure 142–17 for every enabled receive channel.

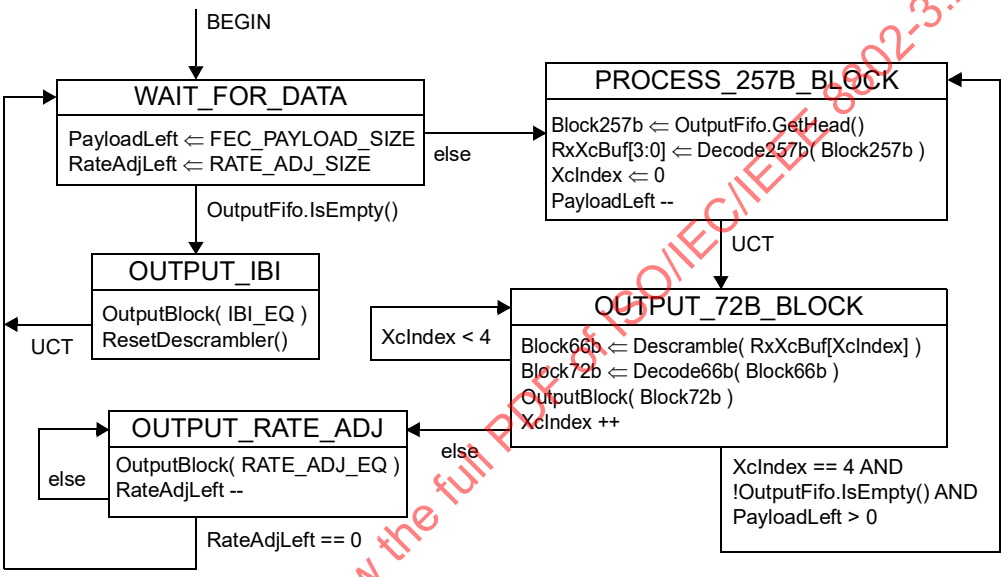


Figure 142–17—PCS Output process state diagram

142.4 Nx25G-EPON PMA

The PMA adapts the serial PMD service interface (PMD_UNITDATA, see 141.3.3 and 141.3.4) to the 257-bit wide interface of the PCS (PMA_UNITDATA, see 142.4.1). Where Nx25G-EPON operates over multiple channels, the PMA sublayer includes multiple identical instances of the transmit data path and/or the receive data path.

In the downstream direction (from the OLT to the ONUs), the PMA includes a differential encoding option (see 142.4.2 and 142.4.3). This encoding technique facilitates the use of lower bandwidth receivers at the ONUs.

142.4.1 Service Interface

The PMA provides a service interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA service interface supports the exchange of 257-bit single data-unit vectors between PCS entities. The PMA converts 257-bit single data-unit vectors into bits and passes these to the PMD, and vice versa.

The following primitives are defined:

— PMA_UNITDATA[*i*].request(tx_code_group<256:0>)
— PMA_UNITDATA[*i*].indication(rx_code_group<256:0>)
— PMA_SIGNAL[*i*].request(tx_enable)
— PMA_SIGNAL[*i*].indication(SIGNAL_OK)

where "[*i*]" represents the PMA Channel: 0 or 1.

142.4.1.1 PMA_UNITDATA[*i*].request

This primitive defines the transfer of data (in the form of 257-bit single data-unit vectors) from the PCS to the PMA by the PCS Transmit process, see 142.2.

142.4.1.1.1 Semantics of the service primitive

PMA_UNITDATA[*i*].request(tx_code_group<256:0>)

Data is conveyed to PMA_UNITDATA[*i*].request() as described in the PCS Transmit state diagram via the PassToPMA function, see Figure 142–11.

142.4.1.1.2 When generated

The PCS continuously sends tx_code_group<256:0> single data-unit vectors to the PMA according to the PMA transmit clock at either (25.78125 / 257) GHz or (10.3125 / 257) GHz as defined in 142.4.4.

142.4.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a serial bit stream for conveying data to the PMD using PMD_UNITDATA[*i*].request(tx_bit), see 141.3.1.2.

142.4.1.2 PMA_UNITDATA[*i*].indication

This primitive defines the transfer of data (in the form of 257-bit single data-unit vectors) from the PMA to the PCS. PMA_UNITDATA[*i*].indication is used by the PCS receive path processes, see 142.3.5.

142.4.1.2.1 Semantics of the service primitive

PMA_UNITDATA[*i*].indication(rx_code_group<256:0>)

The data conveyed by PMA_UNITDATA[*i*].indication is the rx_code_group<256:0> parameter that is used in the Shift() function (see 142.3.5.3). Shift() is used in the OLT Synchronizer process, see Figure 142–14, and in the ONU Synchronizer process, see Figure 142–15.

142.4.1.2.2 When generated

The PMA continuously sends rx_code_group<256:0> single data-unit vectors to the PCS according to the PMA transmit clock at either (25.78125 / 257) GHz or (10.3125 / 257) GHz as defined in 142.4.4.

142.4.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

142.4.1.3 PMA_SIGNAL[*i*].request

This primitive is used to turn the laser on and off at the PMD sublayer. In the OLT, this primitive shall always take the value ON. In the ONU, the value of this variable is controlled by the PCS Transmit function, see Figure 142–11.

142.4.1.4 PMA_SIGNAL[*i*].indication

PMA_SIGNAL[*i*].indication is generated by the PMA receive process to propagate the loss of optical signal from the PMD sublayer to the PMA client.

142.4.1.4.1 Semantics of the service primitive

PMA_SIGNAL[*i*].indication (SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented to the PMA client. A value of OK does not guarantee valid data is being presented to the PMA client.

142.4.1.4.2 When generated

The PMA generates a PMA_SIGNAL[*i*].indication primitive to the PMA client whenever there is change in the value of the SIGNAL_OK parameter.

142.4.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

142.4.2 Differential encoder

Differential encoding as shown in Figure 142–18 shall be implemented in the transmit path of the OLT PMA. The use of differential encoding is optional. Setting the MDIO control bit 1.29.15 (see 45.2.1.23a.1) to a one enables the differential encoding.

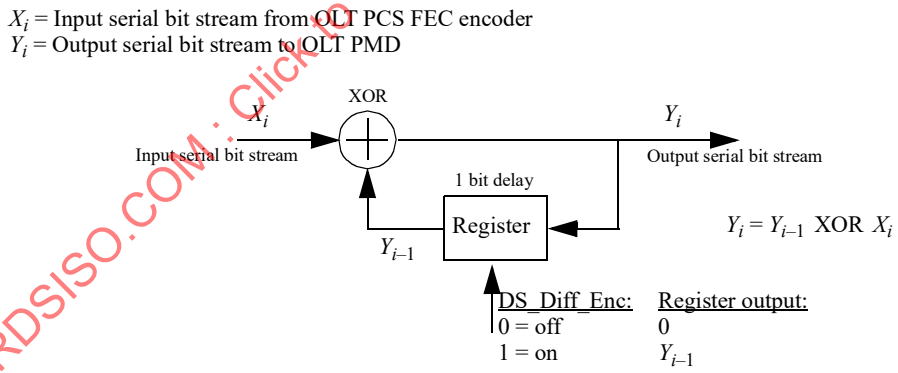


Figure 142–18—Differential encoding

142.4.3 Differential decoder

Differential decoding shall be implemented in the receive path of the ONU PMA as shown in Figure 142–19. The ONU shall implement automatic detection of receive path differential encoding, and switch in the decoder as appropriate. The DS_Diff_Enc bit is mapped to Clause 45 bit 1.29.15 (see 45.2.1.23a.1). This bit is controlled by a local differential encoding detection function (outside the scope of this standard).

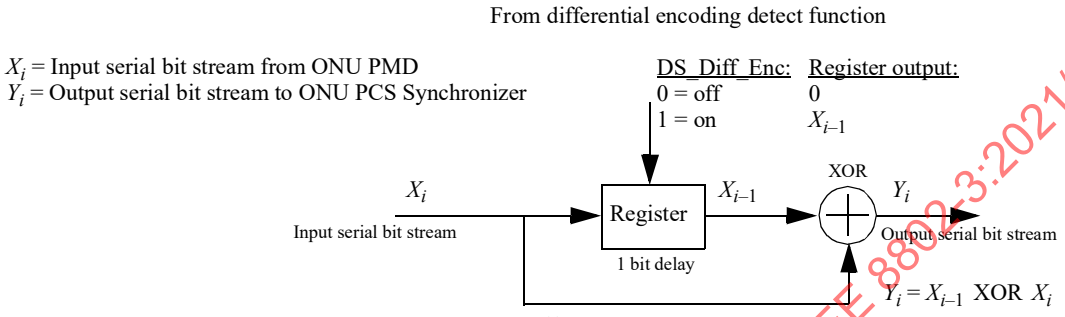


Figure 142–19—Differential decoding

142.4.4 PMA transmit clock

The data conveyed by PMA_UNITDATA.request() is a 257-bit vector representing a single data unit, which has been prepared for transmission by the PMA client. For the PMA devices transmitting at 25.78125 GBd, the PMA transmit clock is equal to (25.78125 / 257) GHz. For the PMA devices transmitting at 10.3125 GBd, the PMA transmit clock is equal to (10.3125 / 257) GHz. In PMA devices supporting multiple transmit channels, the transmit clocks for all channels are phase aligned.

142.4.4.1 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU PMA transmit clock tracks the ONU PMA receive clock. Jitter transfer masks are defined in 141.6.2. For the ONUs supporting 10G transmission (i.e., 25/10G-EPON and 50/10G-EPON ONUs), the PMA transmit clock is derived from the PMA receive clock by dividing the latter by 2.5. In the ONUs supporting multiple receive channels, the PMA transmit clock tracks the received clock of the active (enabled) receive channel with the lowest index.

142.4.5 T_{CDR} measurement

142.4.5.1 Definitions

Clock and data recovery (CDR) lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when the electrical signal after the PMD at TP8, as illustrated in Figure 141–3, reaches the conditions specified in 141.7.14 for receiver settling time to the moment when the signal phase is recovered and jitter is maintained for an input signal with BER of no worse than 10^{-2}.

A PMA instantiated in an OLT shall become synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8.

142.4.5.2 Test specification

The test of the OLT PMA receiver T_{CDR} time assumes that there is an optical PMD transmitter at the ONU with a well-known T_{on} time as defined in 141.7.13, and an optical PMD receiver at the OLT with a

well-known $T_{rx\_settling}$ time as defined in 141.7.14. After the T_{on} + $T_{rx\_settling}$ time, the parameters at TP8 reach within 15 % of their steady-state values.

Set up the test ONU/OLT test system for 10^{-2} BER. Assuming a 3-zone SP1, SP2, and SP3 upstream ONU burst structure as shown in Figure 142–3, program the ONU SP1 TX pattern length so that the SP1 pattern ends at the precise end of the well-known OLT receiver settling time (within one 257-bit block of SP1, or ~10 ns granularity). Starting with the SP2 pattern of zero length (zero 257-bit blocks), test for SP3 detection. If the detection fails, increase the SP2 length by one and repeat the test until SP3 pattern is detected reliably. The number of 257-bit SP2 blocks times the length of each block is the T_{CDR} time, with a margin of error of one 257-bit block time. To reduce hysteresis, increase the number of 257-bit SP2 blocks several hundred nanoseconds beyond this point (20 to 30 additional 257-bit SP2 blocks), and then start decrementing the number of 257-bit SP2 blocks, testing for the SP3 detection at each decrement, until the SP3 SBD is not detected at the OLT. If the SP2 block time counting both forward and backward is less than the specified T_{CDR} maximum time of 400 ns, then the CDR performance meets the requirement.

142.5 Protocol implementation conformance statement (PICS) proforma for Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON[5]

142.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

142.5.2 Identification

142.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

142.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ca-2020, Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ca-2020.)	

Date of Statement	

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

142.5.3 PCS capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	Transmission bit order	142.2	Per Figure 142–4	M	Yes [ ]
PCS2	Control code values treated as errors	142.2.1	All control code values that do not appear in Table 142–2 are not to be transmitted and are treated as an error if received	M	Yes [ ]
*OLT	OLT functionality		Device supports functionality required for OLT	O/1	Yes [ ] No [ ]
*ONU	ONU functionality		Device supports functionality required for ONU	O/1	Yes [ ] No [ ]

142.5.4 PCS processes

Item	Feature	Subclause	Value/Comment	Status	Support
PSD1	FEC encoder	142.2.4	Encodes the transmitted data stream using a quasi-cyclic QC-LDPC FEC, defined in 142.2.4.1	M	Yes [ ]
PSD1a	FEC codeword shortening	142.2.4.2	Supports FEC shortening	M	Yes [ ]
PSD1b	FEC encoding process	142.2.4.2	Per 142.2.4.2	M	Yes [ ]
PSD2	Input process	142.2.5.4.1	As depicted in Figure 142–9	M	Yes [ ]
PSD3	Framer process	142.2.5.4.2	As depicted in Figure 142–10	M	Yes [ ]
PSD4	Transmit process	142.2.5.4.3	As depicted in Figure 142–11	M	Yes [ ]
PSD5	64B/66B decoder	142.3.4	As depicted in Figure 49–17	M	Yes [ ]
PSD6a	Synchronizer process in OLT	142.3.5.4	As depicted in Figure 142–14, for every enabled receive channel	OLT:M	Yes [ ] N/A [ ]
PSD6b	Synchronizer process in ONU	142.3.5.5	As depicted in Figure 142–15, for every enabled receive channel	ONU:M	Yes [ ] N/A [ ]
PSD7	Output process	142.3.5.7	As depicted in Figure 142–17, for every enabled receive channel	M	Yes [ ]
PSD8	PCS ONU BER Monitor process	142.3.5.6	As depicted in Figure 142–16 for every enabled receive channel	ONU:M	Yes [ ] N/A [ ]

142.5.5 PMA processes

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Differential encoder in OLT	142.4.2	As depicted in Figure 142–18	OLT:M	Yes [ ] N/A [ ]
PMA2a	Differential decoder in ONU	142.4.3	As depicted in Figure 142–19	ONU:M	Yes [ ] N/A [ ]
PMA2b	Automatic detection of differential encoding	142.4.3	ONU implements automatic detection of Rx path differential encoding and enables decoder as appropriate	ONU:M	Yes [ ] N/A [ ]
PMA3	ONU loop-timing	142.5	ONU PMA transmit clock tracks the ONU PMA receive clock	ONU:M	Yes [ ] N/A [ ]
PMA4	OLT PMA CDR synchronization time	142.4.5.1	OLT PMA becomes synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8	OLT:M	Yes [ ] N/A [ ]
PMA5	PMA_SIGNAL[*i*].request, value in OLT	142.4.1.3	In OLT, this primitive always takes on the value of ON	OLT:M	Yes [ ] N/A [ ]

143. Multi-Channel Reconciliation Sublayer

143.1 Overview

This clause describes the Multi-Channel Reconciliation Sublayer (MCRS) which enables multiple MACs to interface with multiple xMIIs. Figure 143–1 shows the relationship between this MCRS and the ISO/IEC OSI reference model. Generally, single-channel RS specifications enabled a single MAC to interface to a single PHY in point-to-point (P2P) links, or multiple MACs to interface to a single PHY in P2MP links (e.g., EPON architectures). This concept is expanded in this clause to allow single or multiple MACs to interface with multiple PHYs in either P2P or P2MP applications.

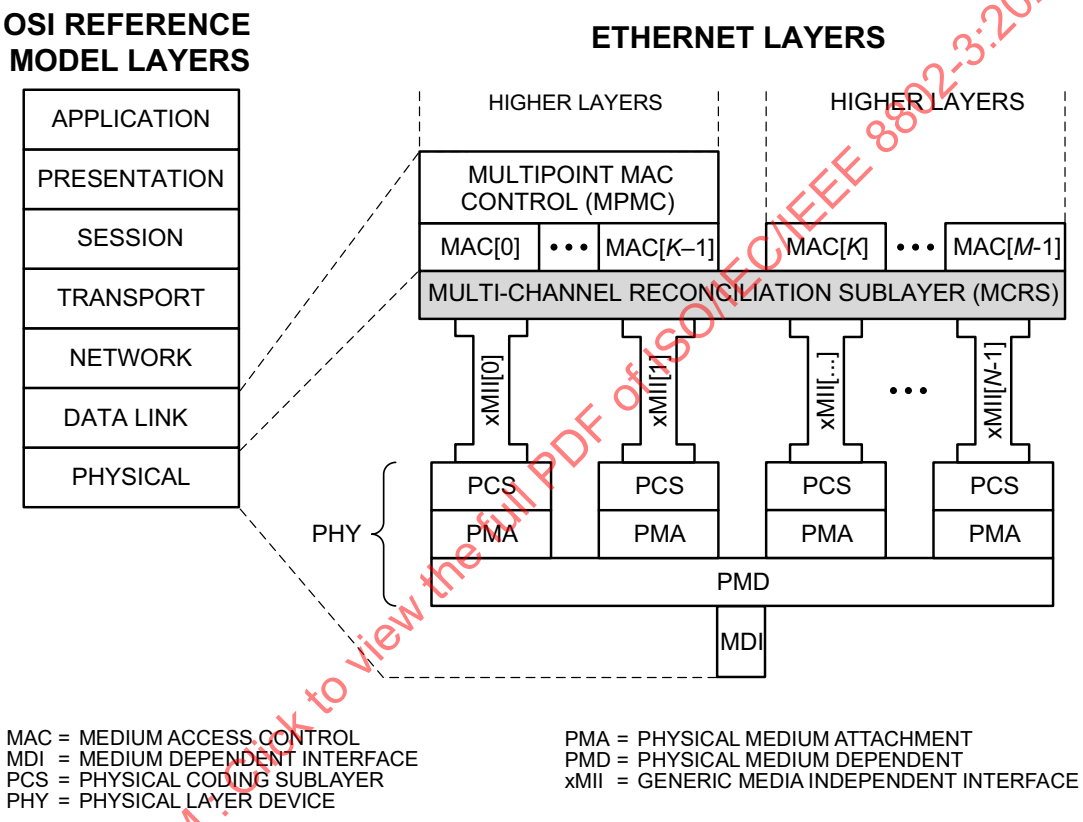


Figure 143–1—Relationship of MCRS to the OSI reference model

The MCRS adapts the bit-serial protocols of the MAC to the parallel format of the Physical Coding Sublayer (PCS) service interface. This clause defines an MCRS as an interface between the MAC sublayer and one or more xMIIs. In this clause, xMII is used as a generic term for the Media Independent Interfaces for implementations of 10 Gb/s and above. For example: for 10 Gb/s implementations, it is called XGMII; for 25 Gb/s implementations, it is called 25GMII. Though the xMII is an optional logical interface between the MAC sublayers and the Physical Layers, it is used extensively in this clause as a basis for specification.

143.2 Summary of major concepts

The following are the major concepts of the MCRS:

a) The MCRS transmission is controlled by a higher layer (e.g., Multipoint MAC Control sublayer defined in Clause 144) via the use of MCRS_CTRL primitives, which indicate envelope start time, durations, and transmission channels.
b) The MCRS establishes a temporary binding of a single MAC instance to one or more xMII instances with all xMIIs operating at the same rate.
c) In the transmit direction, the MCRS converts the MAC serial data stream into the parallel data paths of multiple xMIIs servicing separate PHYs.
d) In the receive direction, the MCRS maps the signal sets provided by the xMIIs to the PLS service primitives of individual MACs.
e) Each direction of data transfer is independent and serviced by data, control, and clock signals.
f) The MCRS generates continuous data or control characters in the transmit path and expects continuous data or control characters in the receive path.

143.2.1 Concept of a logical link and LLID

In point-to-multipoint architectures, such as EPON, the transmitting and receiving stations may include multiple MAC instances. Such architectures are best viewed as a collection of logical point-to-point and/or point-to-multipoint links. A point-to-point logical link connects a single MAC instance at the transmitting station to a single MAC instance at the receiving station. A point-to-multipoint logical link takes advantage of the P2MP topology and connects a single MAC instance at the transmitting station to multiple MAC instances at multiple receiving stations. The transmitting and receiving stations may be logically connected with each other via multiple logical links.

A logical link is created in the MCRS (below the MAC) by tagging each frame (or frame fragment) with a logical link identifier (LLID) value. The MCRS transmit function inserts a specific LLID value depending on which instance of MAC has sourced the frame. The MCRS receive function directs the received frame (or frame fragment) to the specific MAC instance mapped to this LLID value, or to multiple MAC instances, in case of a point-to-multipoint logical link. The concept of a logical link is further defined in 144.3.4.

143.2.2 Concept of an MCRS channel

An MCRS channel is a single unidirectional transmission path through the MCRS. The number of channels contained within an MCRS generally corresponds to the number of xMII instances connected to the MCRS. Thus, an MCRS implementation that connects to *N* xMII instances contains *N* transmit MCRS channels and *N* receive MCRS channels. Some architectures (e.g., EPON) allow an xMII interface to only implement either receive or a transmit data path. In such architectures, the number of receive and transmit MCRS channels may be different. For example, in a 50/10G-EPON OLT, there are two transmit MCRS channels attached to two 25GMIIs and one receive MCRS channel attached to one XGMII.

143.2.3 Binding of multiple MACs to multiple xMII instances

The key function of the MCRS is the dynamic binding of a PLS_DATA[*m*] interface to one or more MCRS channels (*m* represents the index of the MAC instance). The dynamic nature of the binding means that such a binding exists only for a predetermined interval of time during which a given MAC instance is expected to transmit or receive data. After that time, the binding no longer exists, and a different MAC instance may bind to the same MCRS channels.

The dynamic binding of MAC instances to MCRS transmit channels is controlled by the MCRS_CTRL.request() primitive described in 143.3.1.2.1. The dynamic binding of MAC instances to receive MCRS channels is determined by the LLID value of the incoming data.

143.2.4 Transmission and reception over multiple MCRS channels

143.2.4.1 Transmission unit

Within the MCRS, the basic unit of transmission is the envelope quantum (EQ). One EQ is represented by a 72-bit block consisting of 64 data bits and eight control bits. For 36-bit wide xMIIs, such as 25GMII, an EQ is mapped to two successive xMII transfers as shown in Figure 143–2.

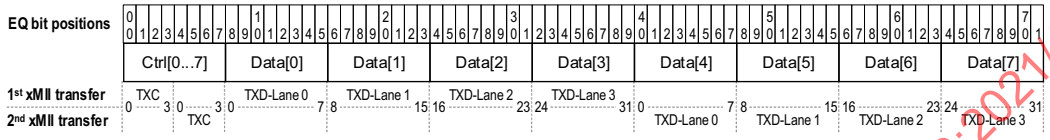


Figure 143–2—Envelope quantum (EQ) format

143.2.4.2 Transmission envelopes

The MCRS encapsulates data transmitted by a MAC instance in transmission envelopes. A transmission envelope represents a continuous transmission by a specific MAC instance (LLID) on a specific MCRS channel. A transmission envelope is transmitted on a single MCRS channel. In a system with a single channel an envelope includes one or more data frames and may contain at most two partial frames (one at the beginning and one at the end of the envelope) and any number of non-fragmented frames. In systems with multiple channels, envelopes may overlap (see 143.2.5) and a frame may be striped over multiple channels with each channel transporting parts of this frame. However, at the conclusion of the overlapped transmission, only a single frame may remain fragmented.

143.2.4.3 Envelope headers

Each transmission envelope begins with an envelope header (see Figure 143–3). The envelope header consists of multiple fields, such as LLID, Envelope Length, EnvType flag, and other fields defined in 143.3.2.

The LLID field identifies a specific logical link.

The size of the envelope header is exactly one EQ. The envelope header includes the Envelope Length field that shows the length of the entire envelope in units of EQ. The envelope header itself is counted as part of the envelope, therefore the minimum value of the Envelope Length field is one.

There are two distinct types of envelope headers; an envelope start header (ESH) and an envelope continuation header (ECH).

The ESH is inserted into the transmission stream at the beginning of every envelope, while no data is being taken from the corresponding MAC instance. At the receiving end, the ESH is processed by the MCRS and then discarded and no bits are passed to the corresponding MAC instance.

The ECH is inserted into the transmission stream in place of a data frame preamble. The length field of the ECH shows the residual length of the envelope. At the receiving end, the ECH is replaced with a normal frame preamble, which is passed to the corresponding MAC instance.

To distinguish the ESH and ECH, the envelope header includes a field called the EnvType flag. In ESH, the EnvType flag carries the value of 1 and in ECH, the flag carries the value of 0. Figure 143–3 illustrates a

transmission sequence for a single LLID *L* transmitting three frames (the first and the last frames are fragments). The format of the envelope header and field definitions are specified in 143.3.2.

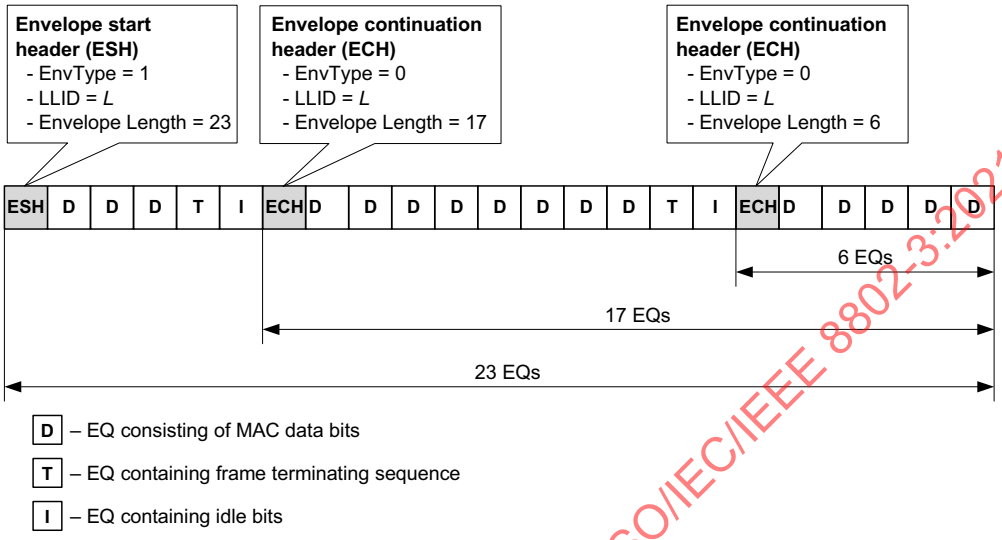


Figure 143–3—An illustration of transmission sequence consisting of three frames

143.2.4.4 Interpacket gap adjustment

Multi-lane xMIIs, such as 25GMII, require the alignment of the Start control character (first octet of preamble) to lane 0. Generally, a technique called Deficit Idle Count is used to accomplish this task (see 46.3.1.4).

However, because the MCRS replaces the frame preamble with an ECH, there is an additional requirement for the Start control character to be aligned to octet 0 of an EQ, such that the entire preamble occupies exactly one EQ and is not split across two consecutive EQs. To achieve such alignment, rather than maintaining a deficit idle count, the interpacket gap (IPG) is either unchanged or reduced, but is not expanded. The IPG may be reduced by up to seven octets from its default size of 96 bits. For back-to-back data frames, the minimum guaranteed IPG is five octets.

The exact size of the IPG depends on the length of the previous data frame (for the case of back-to-back frames). Figure 143–4 illustrates the IPG reduction for all possible positions of the end of frame character. The default IPG generated by the MAC and the reduced IPG are highlighted.

The minimum IPG of five octets is consistent with the requirements of 46.2.1 for XGMII (and hence applicable to 25GMII). Since the IPG either remains unchanged or is reduced, in order to prevent the MAC data rate from exceeding the specified maximum limit, the MCRS provides a rate adjustment mechanism, whereby a MAC is paused for a predefined duration of time at a predefined repeating interval.

Figure 143–4—An illustration of Start control character alignment to octet 0

143.2.5 Dynamic channel bonding

If the PLS_DATA[*m*] interface is bound to a single MCRS channel that is connected to an xMII instance, the corresponding MAC instance is able to transmit and receive at a data rate corresponding to that xMII data rate. For example, if the MCRS sublayer is connected to a 25GMII, that MAC instance is able to transmit and receive at 25 Gb/s.

However, in a system that supports multiple MCRS channels (i.e., MCRS is connected to multiple xMII instances), a single PLS_DATA[*m*] interface may be simultaneously bound to N_{TX} MCRS transmit channels and N_{RX} MCRS receive channels, where N_{TX} may not equal N_{RX}. In this case, again assuming the 25GMII, the corresponding MAC instance supports the transmit data rate of N_{TX} × 25 Gb/s and the receive data rate of N_{RX} × 25 Gb/s.

The channel bonding takes place when an LLID is assigned transmission envelopes on more than one channel. Such envelopes may happen to activate at the same time and to have the same duration, as illustrated in Figure 143–5 for LLID A. But most often the envelopes are not mutually aligned and just partially overlap as shown for LLID B.

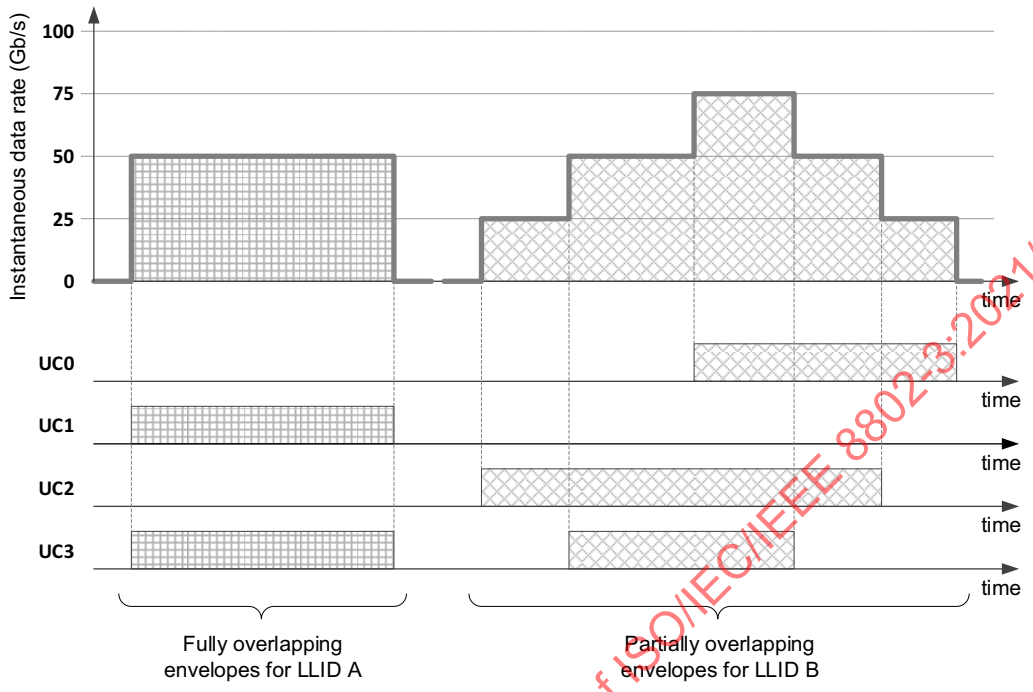


Figure 143–5—Full or partial envelope overlap and the resulting instantaneous data rate

An LLID (i.e., a MAC instance) that is given two or more overlapping envelopes on several MCRS channels is able to seamlessly increase its transmission data rate to the aggregated data rate of all the MCRS channels with the overlapping envelopes. This is referred to as dynamic channel bonding and it gives the system an ability to achieve a higher instantaneous transmission or reception rate than is available for any single MCRS channel. For example, a MAC instance connected to an MCRS with four channels of 25 Gb/s each can achieve an instantaneous transmission rate of 25 Gb/s, 50 Gb/s, 75 Gb/s, or 100 Gb/s by varying, in real time, the number of channels that are bonded to send data from a single LLID.

143.2.5.1 LLID transmission over multiple MCRS channels

The dynamic channel bonding is achieved by interleaving data belonging to a single LLID (i.e., data from a single MAC instance) over multiple envelopes on multiple MCRS channels. Figure 143–6 illustrates a dynamic channel bonding example based on the partially overlapping envelopes scenario in Figure 143–5. Each EQ is transmitted on the channel that has the earliest transmission availability. If there are multiple such channels, the one with the lowest channel index is selected. In other words, the overlapping envelopes are filled with EQs in the increasing order of MCRS channel index.

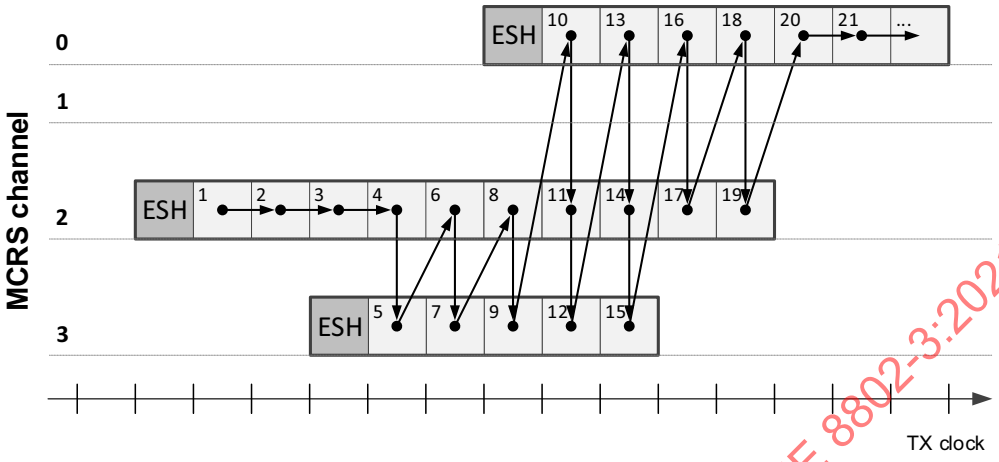


Figure 143–6—Fill order of overlapping envelopes

143.2.5.2 MCRS channel skew remediation mechanism

In a multi-channel system that uses multiple wavelengths to carry different MCRS channels, the channels have unequal propagation delays. This variable propagation delay results in a timing skew between signals received on separate MCRS channels. Other timing variability may accumulate in the sublayers below the MCRS, exacerbating this timing skew.

To properly restore the order of data transmitted over multiple bonded MCRS channels, the skew between the channels has to be eliminated at the receiver. The skew remediation mechanism is based on two buffers: an envelope transmission buffer (EnvTx) in the transmitting MCRS and an envelope reception buffer (EnvRx) in the receiving MCRS. As envelopes traverse the EnvTx buffer (before the skew has impacted any of the MCRS channels), their relative position in the EnvTx buffer is recorded and transmitted to the EnvRx buffer. At the receiving station, the envelopes received on multiple channels are aligned in the EnvRx buffer using the position information received from the transmitting device. The relative alignment of envelopes in EnvRx becomes identical to their relative alignment that existed in EnvTx. This envelope alignment method results in the complete elimination of any skew between the channels, as well as any timing variability that may accumulate in the sublayers below MCRS.

143.2.5.3 EnvTx and EnvRx buffers

The EnvTx and EnvRx buffers are two-dimensional buffers organized into rows and columns. The number of columns is equal to the number of channels supported by the device. If the number of rows is set to 32, this provides sufficient buffering to mitigate approximately 80 ns of skew between any two channels (assuming a 25GMII). If an application requires additional skew mitigation, up to ±81.92 ns of skew may be accommodated by increasing the number of buffer rows.

The EQs are written into the EnvTx and read from EnvRx buffers first by row, then by column, as shown in Figure 143–7.

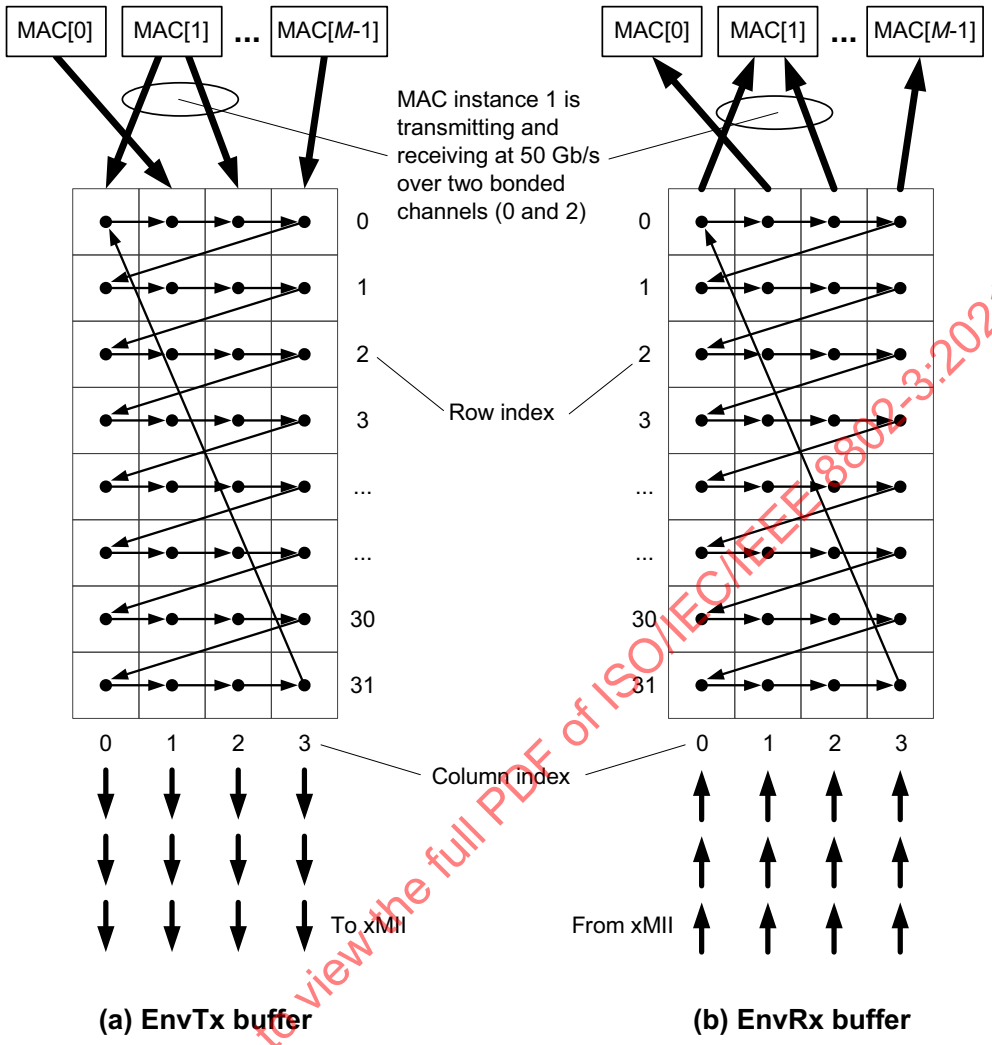


Figure 143–7—Internal structure of EnvTx and EnvRx buffers

In the EnvTx buffer all columns of a row are written before the write pointer shifts to the next row. The EQs written into each column may be sourced by different MAC instances, if the envelopes on different channels belonged to different LLIDs, or from the same MAC instance, in case of multiple channels bonded to serve the same LLID (see Figure 143–7).

Similarly, in the receiving device, the EQs read from different columns may be passed to different MAC instances, if the envelope headers on different channels carried different LLID values, or the EQs may be passed to the same MAC instance, if the envelope headers carried the same LLID value. In case of EQs from different columns being passed to the same MAC instance, the EQ from a column with the lower index is passed before an EQ from a column with the higher index.

EnvTx and EnvRx are circular buffers – after reading the last row, the read pointer shifts back to row 0. In EnvTx, the read and write pointers advance synchronously with the xMII transmit clock (TX_CLK). In

EnvRx, the read and write pointers advance synchronously with the xMII receive clock (RX_CLK). However, the value of the receive channel write pointer is updated whenever an envelope header is received.

143.2.5.4 Envelope position alignment marker

The relative envelope position recorded in an envelope header by the MCRS transmit function is simply the logical equivalent of the EnvTx buffer row index into which the given envelope header was written. This information is placed in an envelope header field called the envelope position alignment marker (EPAM). When an envelope header is received by the MCRS receive function, the EPAM field is extracted and its value is used to update the write pointer (row index) into which this envelope header is to be written. The remainder of the envelope is then written sequentially into the same column following the envelope header.

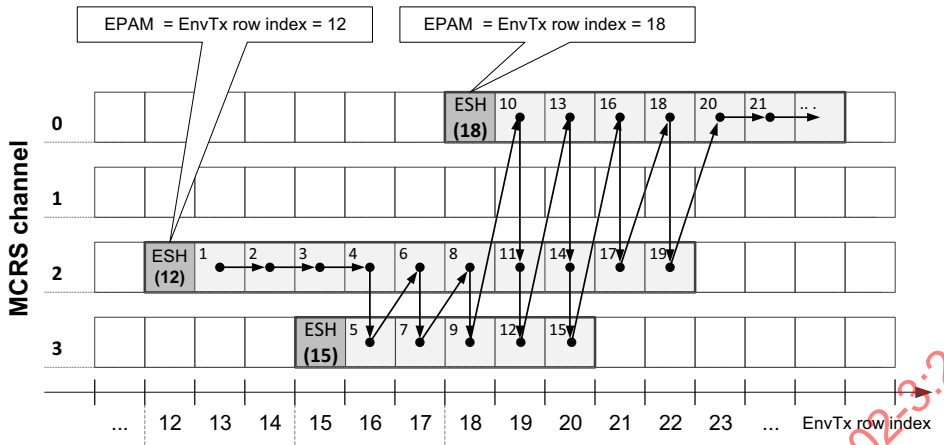
Figure 143–8 illustrates (a) the initial envelope positions in the EnvTx buffer, (b) the accumulated channel-dependent skew of the received channels at the EnvRx buffer, and (c) the restored alignment based on EPAM value carried in each envelope header. As the true relative positions of the envelopes are restored, reading the data in the same order as shown in Figure 143–8 properly serializes the data received over the multiple bonded channels.

At the receiving station, regardless of the amount of accumulated skew, EQs transmitted at the same time from the same MCRS are placed in the same row of the EnvRx. As the EnvRx is read out in a row-by-row order over all channels the receiver effectively realigns the EQs to the same order they were transmitted in.

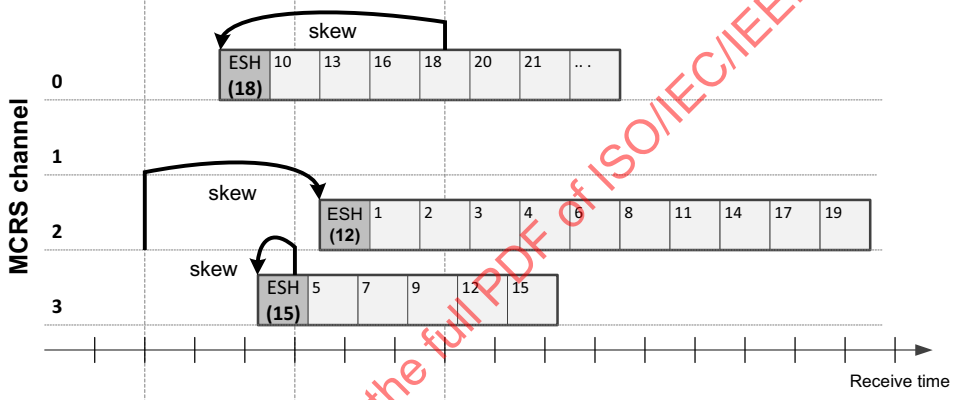
143.2.6 MDIO addressing model for multi-channel architecture

The MDIO addressing model for multi-channel architecture is defined as follows:

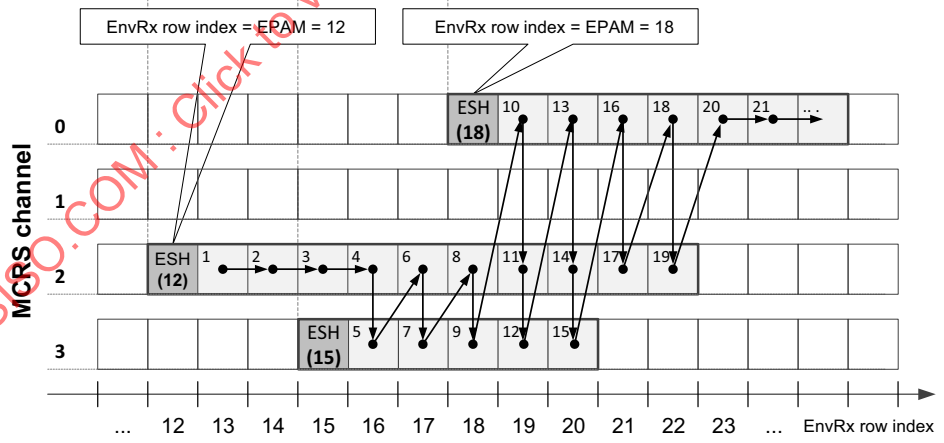
— Separate physical ports on the OLT are managed by separate Station Management entities (STAs, see 45.1.2).
— Within each physical port, separate channels are addressed via port address (PRTAD, see 45.3.5).
— Within each channel, separate layers (PMA, PCS, etc.) are addressed via device address (DEVAD, see 45.3.6) as shown in Table 45–1.
— A common PMD that spans multiple channels is addressed via the numerically-lowest PRTAD associated with that PMD.



(a) Envelope header records the row index of this header in the EnvTx buffer



(b) Data is received on multiple channels with different propagation delays (skew)



(c) Envelopes are positioned in the EnvRx buffer in a row index as recorded in the ESH

Figure 143–8—Illustration of skew elimination by envelope position alignment in the EnvRx buffer

143.3 MCRS functional specifications

143.3.1 MCRS interfaces

Interfaces to the MCRS are illustrated in Figure 143–9. In addition to the *M* instances of the PLS service interface (one per MAC) and *N* xMII instances, there is an MCRS_CTRL interface that connects to the higher layers (see Figure 143–1).

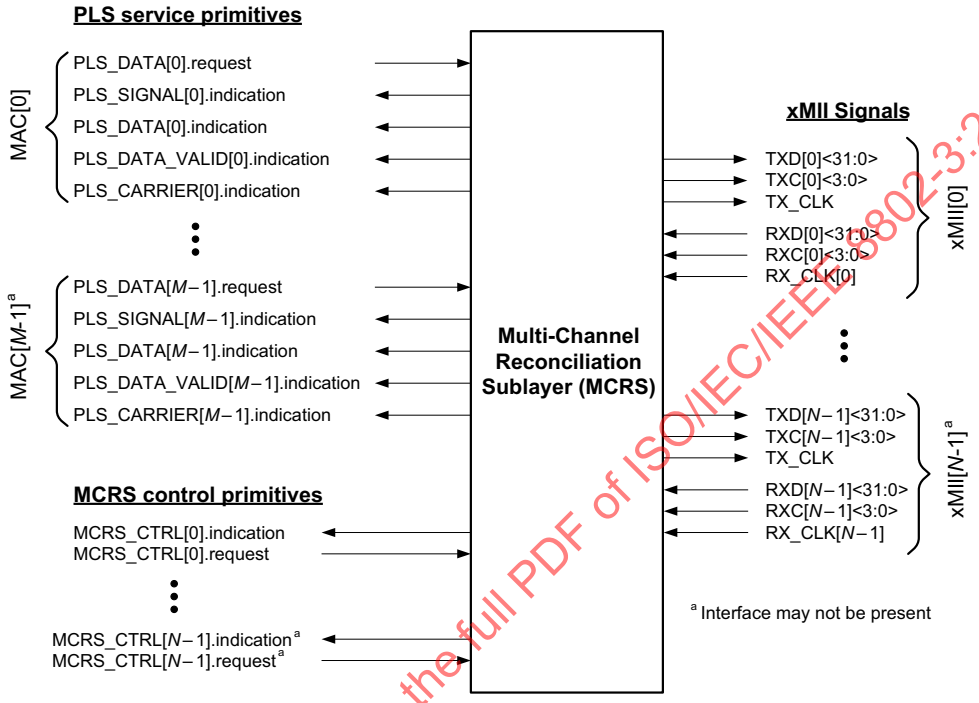


Figure 143–9—Multi-Channel Reconciliation Sublayer (MCRS) inputs and outputs

143.3.1.1 PLS service primitives

In all single-channel RS definitions, only one PLS service interface is active at any given moment; this is still true for systems with only one active MCRS channel. However, for systems with more than one MCRS channel there may be multiple PLS service interfaces active at any given time.

The mapping of the PLS service primitives to xMII signals are shown in 143.3.1.1.1 for PLS_DATA[].request primitives and in 143.3.1.1.3 for PLS_DATA[].indication primitives. These are similar to the mappings described in 46.1.7. However, in systems with multiple MCRS channels there are multiple xMIIs and therefore an index is added to the xMII signals to indicate which of the xMIIs to use.

Depending on the MAC operating speed, the PLS_DATA.request primitive maps to one or multiple xMII transmit interfaces (see Table 143–1).

Depending on the MAC operating speed, the PLS_DATA.indication primitive maps to one or multiple xMII receive interfaces (see Table 143–2).

Table 143–1—Mapping of PLS_DATA.request primitives

MAC operating speed	MCRS channels	Transmit interface	Signals
10 Gb/s	1	XGMII[0]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK
25 Gb/s	1	25GMII[0]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK
50 Gb/s	2	25GMII[0] 25GMII[1]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK[a] TXD[1]<31:0>, TXC[1]<3:0>
N × 25 Gb/s	*N*	25GMII[0] 25GMII[1] 25GMII[2] … 25GMII[*N* – 1]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK[a] TXD[1]<31:0>, TXC[1]<3:0> TXD[2]<31:0>, TXC[2]<3:0> … TXD[*N* – 1]<31:0>, TXC[*N* – 1]<3:0>

[a] All transmit 25GMII interfaces share a common clock.

Table 143–2—Mapping of PLS_DATA.indication primitives

MAC operating speed	MCRS channels	Receive interface	Signals
10 Gb/s	1	XGMII[0]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0]
25 Gb/s	1	25GMII[0]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0]
50 Gb/s	2	25GMII[0] 25GMII[1]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0] RXD[1]<31:0>, RXC[1]<3:0> and RX_CLK[1]
N × 25 Gb/s	*N*	25GMII[0] 25GMII[1] 25GMII[2] … 25GMII[*N* – 1]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0] RXD[1]<31:0>, RXC[1]<3:0> and RX_CLK[1] RXD[2]<31:0>, RXC[2]<3:0> and RX_CLK[2] … RXD[*N* – 1]<31:0>, RXC[*N* – 1]<3:0> and RX_CLK[*N* – 1]

143.3.1.1.1 Mapping of PLS_DATA[*ch*].request primitive

The MCRS maps the primitive PLS_DATA.request to the xMII signals TXD[*ch*]<31:0>, TXC[*ch*]<3:0>, and TX_CLK in the same way as for the XGMII as specified in 46.1.7.1.

143.3.1.1.2 Mapping of PLS_SIGNAL[*ch*].indication primitive

The MCRS support full duplex operation only and does not generate the PLS_SIGNAL.indication primitive.

143.3.1.1.3 Mapping of PLS_DATA[*ch*].indication primitive

The MCRS maps the primitive PLS_DATA.indication to the xMII signals RXD[*ch*]<31:0>, RXC[*ch*]<3:0> and RX_CLK[*ch*] in the same way as for the XGMII as specified in 46.1.7.2.

143.3.1.1.4 Mapping of PLS_DATA_VALID[*ch*].indication primitive

The MCRS maps the primitive PLS_DATA_VALID.indication to the xMII signals RXC[*ch*]<3:0> and RXD[*ch*]<31:0> in the same way as for the XGMII as specified in 46.1.7.5.

143.3.1.1.5 Mapping of PLS_CARRIER[*ch*].indication primitive

The MCRS supports full duplex operation only and does not generate the PLS_CARRIER.indication primitive.

143.3.1.2 MCRS control primitives

The MCRS inputs the MCRS_CTRL[*ch*].request primitives from the Multipoint Control Protocol (MPCP) and outputs to the MPCP the MCRS_CTRL[*ch*].indication primitives.

143.3.1.2.1 MCRS_CTRL[*ch*].request(link_id, epam, env_length) primitive

The MPCP requests the MCRS to transmit the next envelope using the MCRS_CTRL[*ch*].request(link_id, epam, env_length) primitive. This opens an envelope on channel *ch* for the LLID specified by link_id with a length (in EQs) of env_length. If all channels are idle, the EnvPam variable (see 143.3.3.4) is set to the value of epam (see EnvStartHeader() function definition in 143.3.3.5).

143.3.1.2.2 MCRS_CTRL[*ch*].indication() primitive

The Input process (see Figure 143–12) requests the next envelope from the MPCP after the completion of the previous envelope using the MCRS_CTRL[*ch*].indication() primitive. This primitive indicates to the MPCP that the MCRS is available for the next envelope in a given channel. In the absence of an active envelope, the MCRS_CTRL[*ch*].indication() primitive is generated continuously on every InClk transition (see 143.3.3.4). The MPCP may decide whether to issue a new envelope immediately adjacent to the previous envelope for envelopes that are expected to be packed in the same transmission burst. If the MPCP has determined that a transmission opportunity has ended, it signals that condition by issuing an envelope with link_id set to ESC_LLID (see Table 144–1).

143.3.1.2.3 MCRS_ECH[*ch*].indication(Llid) primitive

The Output process (see Figure 143–16) generates the MCRS_ECH[*ch*].indication(Llid) primitive every time an ESH EQ is read from the EnvRx buffer. This primitive causes the MPMC Control Parser process (see 144.2.1) to generate a local timestamp (i.e., to latch the local MPCP time) representing the arrival time of the ESH EQ.

143.3.1.3 XGMII interfaces

The XGMII is specified to support 10 Gb/s operation. The structure of each of the XGMII interfaces in an MCRS system is as specified in 46.1.6.

For mapping between the XGMII signals and the PLS service interface, see 143.3.1.1.1 and 143.3.1.1.3.

For multi-channel MCRS systems the transmit XGMIIs are synchronous and only one TX_CLK is required.

143.3.1.4 25GMII interfaces

The 25GMII is specified to support 25 Gb/s operation. The structure of each of the 25GMII interfaces in an MCRS system is identical to the XGMII structure specified in 46.1.6. The 25GMII data stream has the same

characteristics as the XGMII data stream described in 46.2 with the exception of the clock rate, which is 390.625 MHz for the 25GMII.

For mapping between the 25GMII signals and the PLS service interface, see 143.3.1.1.1 and 143.3.1.1.3.

For multi-channel MCRS systems the transmit 25GMIIs are synchronous and only one TX_CLK is required.

143.3.2 Envelope header format

Each envelope initiated by the MCRS begins with a 72-bit envelope header. The envelope header shall be as shown in Figure 143–10. The envelope header includes a Start control code, an EnvType flag bit, a 22-bit Envelope Length field, an envelope position alignment marker (EPAM) field, two bits (E and K) reserved for encryption purposes, an LLID field, and an 8-bit cyclic redundancy check (CRC8).

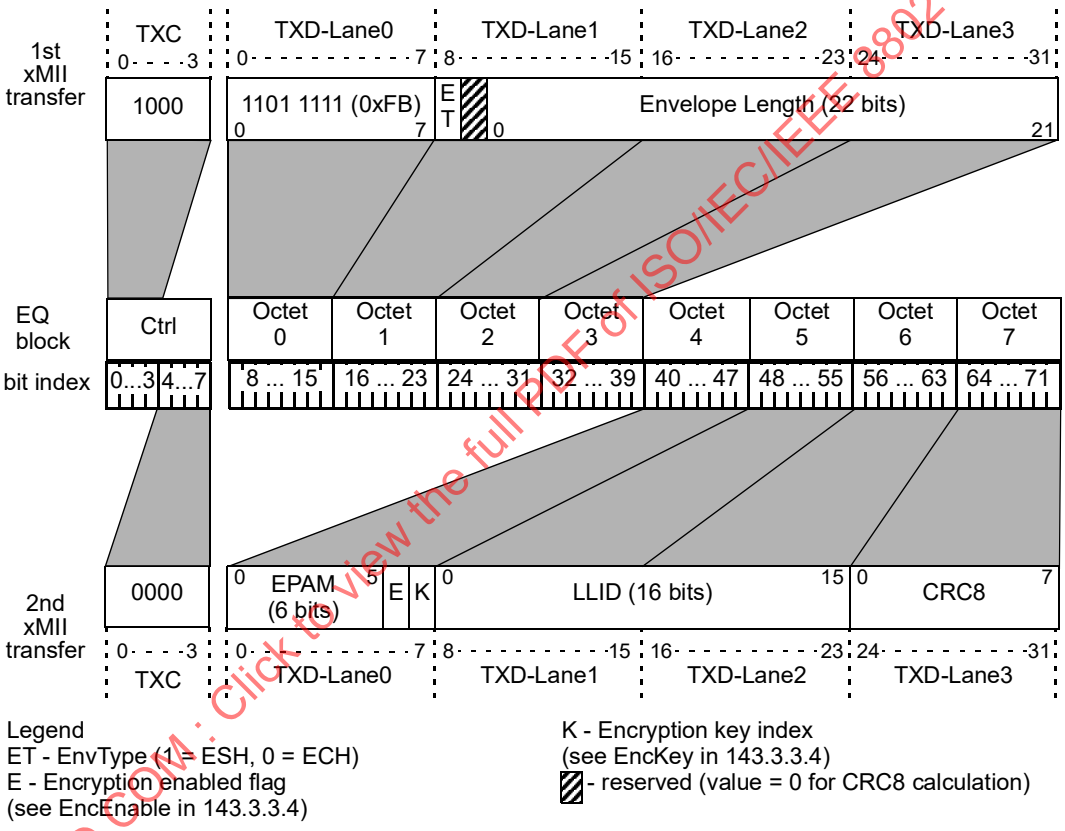


Figure 143–10—Mapping of envelope header fields into two xMII transfers

When the xMII is 36 bits wide, the transmission envelope header includes two successive transfers over the xMII, as illustrated in Figure 143–10. Each 36-bit transfer includes four control bits followed by 32 information bits. Octets within each envelope header field are transmitted from least significant to most significant. Bits within each octet are transmitted from LSB to MSB. An EQ contains eight octets of information so the length of the envelope header equals one EQ.

The envelope header is identified by a Start control code (Block type 0xFB, see Table 142–2).

The ESH has the EnvType flag set to one whereas the ECH has the EnvType flag set to zero. The ESH is used to indicate the beginning of a transmission from a specific LLID.

Following the EnvType flag, there is one reserved bit (EQ<17>) and it is set to zero at the transmitter and its value is ignored at the receiver except for the purposes of calculating the CRC8.

The Envelope Length field represents the number of EQs in the envelope, including the envelope header itself (1 EQ).

The EPAM is used by the receiving MCRS to remove any timing skew that may have occurred during the transmission of the envelope from the source MCRS to the destination MCRS.

The LLID field is set to the value of the LLID (MAC instance) associated with the data in the envelope.

The CRC8 field is used for error detection within the header. CRC8 uses the same generating polynomial as described in 65.1.3.2.3. The CRC8 checksum is calculated over EQ bits 8 through 63. The envelope header bits are processed by the CRC8 calculating function in the same order they are transmitted, i.e., for each field the bits are processed starting with the LSB and ending with the MSB.

143.3.2.1 CRC8 calculation test sequences

The test sequences in Table 143–3, Table 143–4, and Table 143–5 show several example envelope header field values and the resulting CRC8 value computed by a compliant implementation.

Table 143–3—CRC8 computation example #1[a]

Envelope header fields	Start control code	EnvType	Reserved	Envelope Length	EPAM	E	K	LLID
Envelope header fields	0xFB	1	0	64	15	0	0	0xAB-CD
Envelope header with CRC8 (hex)	E5-AB-CD-0F-00-01-01-FB (transmitted LSB first)							
Envelope header with CRC8 (bin)	(last bit) | 1110-0101-1010-1011-1100-1101-0000-1111-0000-0000-0000-0001-0000-0001-1111-1011 | (first bit)							

[a]Gray highlight indicates location and calculated value of CRC8 field

Table 143–4—CRC8 computation example #2[a]

Envelope header fields	Start control code	EnvType	Reserved	Envelope Length	EPAM	E	K	LLID
Envelope header fields	0xFB	0	0	960	5	1	0	0x00-01
Envelope header with CRC8 (hex)	23-00-01-45-00-0F-00-FB (transmitted LSB first)							
Envelope header with CRC8 (bin)	(last bit) | 0010-0011-0000-0000-0000-0001-0100-0101-0000-0000-0000-1111-0000-0000-1111-1011 | (first bit)							

[a]Gray highlight indicates location and calculated value of CRC8 field

Table 143–5—CRC8 computation example #3[a]

Envelope header fields	Start control code	EnvType	Reserved	Envelope Length	EPAM	E	K	LLID
Envelope header fields	0xFB	1	0	10 000	1	1	1	0x12-34
Envelope header with CRC8 (hex)	B6-12-34-C1-00-9C-41-FB (transmitted LSB first)							
Envelope header with CRC8 (bin)	(last bit) | 1011-0110-0001-0010-0011-0100-1100-0001-0000-0000-1001-1100-0100-0001-1111-1011 (first bit)							

[a]Gray highlight indicates location and calculated value of CRC8 field

143.3.3 Transmit functional specifications

A functional block diagram of the MCRS transmit path is illustrated in Figure 143–11. The MCRS interfaces are described in 143.3.1. The MCRS transmit path is composed of two processes and one buffer.

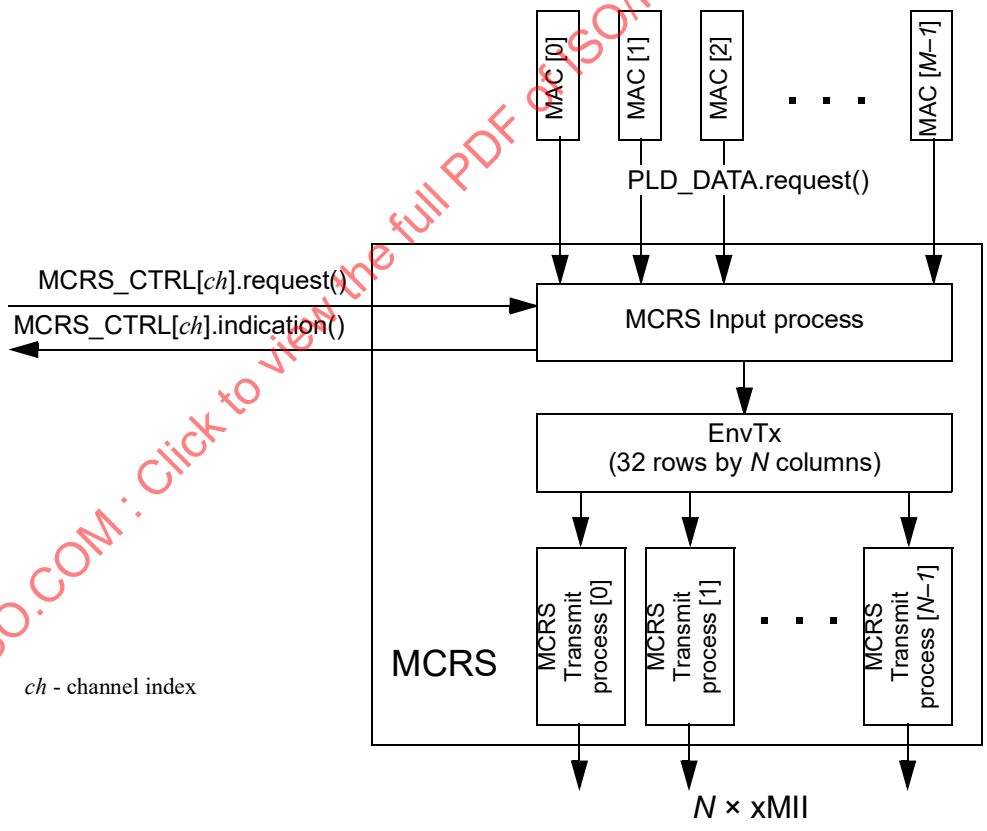


Figure 143–11—MCRS transmit functional block diagram

The Input process, described in 143.3.3.6.1, accepts MAC data, formats it into EQs and stores these EQs in the EnvTx buffer. The Transmit process, described in 143.3.3.6.2, pulls EQs from the EnvTx buffer and feeds them to two successive transfers on the appropriate xMII.

143.3.3.1 Conventions

See 142.1.1.

143.3.3.2 Application-specific parameter definitions

Some constants and variables in this sub-clause have characteristics that are application-specific. For Nx25G-EPON specific parameter definitions refer to 143.4.1.3.

NOTE—References to future application-specific parameters are to be added only to this subclause.

143.3.3.3 Constants

ADJ_BLOCK_SIZE
: Type: integer
Description: The ADJ_BLOCK_SIZE constant represents the block size (in EQs) that is used to adjust the rate between the MAC and the PHY in the MCRS-based device.
Value: application-specific (see 143.3.3.2)

ESC_LLID
: See Table 144–1

IBI_EQ
: Type: 72-bit block
Description: The IBI_EQ constant indicates to the PCS that the burst is terminated.
Value: 0x0A-0A-0A-0A-0A-0A-0A-0A-FF

IEI_EQ
: Type: 72-bit block
Description: The IEI_EQ represents an EQ value transmitted between envelopes.
Value: 0x08-08-08-08-08-08-08-08-FF

NUM_CH
: Type: unsigned integer
Description: The NUM_CH constant represents the number of channels supported by an MCRS-based device.
Value: application-specific (see 143.3.3.2)

PREAMBLE_EQ
: Type: 72-bit block
Description: The value of an EQ returned by the GetMacBlock() function that represents a preamble.
Value: 0x5D-55-55-55-55-55-55-FB-01

RATE_ADJ_EQ
: Type 72-bit block
Description: The value of an EQ that is used as a placeholder to allow for rate differences between the MAC and the PHY layers.
Value: 0x09-09-09-09-09-09-09-09-FF

RATE_ADJ_SIZE
Type: integer
Description: The RATE_ADJ_SIZE constant represents the number of EQs within the ADJ_BLOCK_SIZE block during which the MAC transmission is deferred. The effective MAC rate (per channel) is equal to (nominal MAC rate) × (1 – RATE_ADJ_SIZE / ADJ_BLOCK_SIZE).
Value: application-specific (see 143.3.3.2)

143.3.3.4 Variables

ch
Type: integer
Description: The ch variable represents the index of a specific xMII channel bound to an instance of the MCRS Transmit or MCRS Receive process. The values of ch range from 0 to (NUM_CH – 1). Within each instance of the MCRS Transmit or MCRS Receive process, the value of ch remains constant.

BEGIN
See 142.2.5.2

BlkLeft[ch]
Type: integer
Description: The BlkLeft variable represents the number of EQs remaining in the envelope currently being processed by the MCRS.

EncEnable
Type: Boolean
Description: Encryption enabled flag, not for use by IEEE Std 802.3.

EncKey
Type: one-bit integer
Description: Encryption key index, not for use by IEEE Std 802.3.

EnvTx
Type: array of 72-bit blocks
Description: The EnvTx buffer is used to transfer information between the MCRS Input process and the MCRS Transmit process. In this buffer, each cell, represented by the variables EnvTx[ch][r], stores one EQ (a 72-bit block) of information. The number of columns in the EnvTx buffer is NUM_CH (see 143.3.3.3). The number of rows is 64, as determined by the size of the EPAM field in the envelope header (see 143.3.3.2). The buffer is filled sequentially by the MCRS Input process and is emptied in parallel by NUM_CH instances of the MCRS Transmit process. For additional details, refer to 143.2.5.3.

EnvLeft[ch]
Type: 23-bit signed integer
Description: The EnvLeft variable represents the length remaining in the current envelope for channel ch.

EnvPam
Type: 6-bit integer
Description: The EnvPam variable is used to remove delay variability (including skew) accumulated during transport between two or more channels from a single transmitter. EnvPam is also used as the row index for the EnvRx buffer into which the received data is to be written (see 143.3.4).

InClk

Type: Boolean
Description: The InClk clear-on-read variable is set to true on each rising edge of the TX_CLK signal.

InEQ

Type: 72-bit binary array
Description: A temporary holding variable for one EQ used in the Input process.

LinkId[ch]

Type: 16-bit integer
Description: The LinkId[ch] variables represent the MAC (LLID) being transferred by the Input process or Output process for channel ch.

rCol

Type: integer
Description: The rCol variable represents the EnvTx buffer column currently being read by the MCRS Transmit process. Each column corresponds to a separate transmission channel, i.e., a separate xMII interface.

rRow

Type: 6-bit integer
Description: The rRow variable represents the row in the EnvTx buffer currently being read by the MCRS Transmit process. The value of this variable is synchronized to wRow and is equal to wRow – 1.

TxClk[ch]

Type: Boolean
Description: Description: The TxClk[ch] variable represents the MCRS transmit clock for channel ch. Each TxClk[ch] clear-on-read variable is set to true on each edge, rising and falling, of the TX_CLK signal (see Table 143–1).

TxActive[ch]

Type: Boolean
Description: When set to true, the TxActive[ch] variable indicates that channel ch is currently enabled for transmission. The channel transmits the envelopes or inter-envelope idle EQs (IEI_EQ values) in the absence of envelopes. When set to false, transmission on channel ch is prohibited and this channel generates only inter-burst idle EQs (IBI_EQ values) towards the xMII.

wCol

Type: integer
Description: The wCol variable represents the EnvTx buffer column currently being written by the MCRS Input process. Each column corresponds to a separate transmission channel, i.e., a separate xMII interface.

wRow

Type: 6-bit integer
Description: The variable wRow represents the EnvTx buffer row index currently being written by the MCRS Input process. The value of rRow is synchronized to this variable and is equal to wRow – 1.

143.3.3.5 Functions

EnvContHeader(wCol)

The EnvContHeader() function returns a new envelope header with the EnvType flag equal to 0, indicating that it is a continuation of the current envelope.

```
EQ EnvContHeader(int col)
{
    EQ hdr;
    hdr<7:0> = 0x01;                    // Control bits
    hdr<15:8> = 0xFB;                   // S character
    hdr<16> = 0;                        // EnvType identifies ECH
    hdr<17> = 0;                        // Reserved
    hdr<39:18> = EnvLeft[col];          // EnvLength
    hdr<45:40> = EnvPam;                // EPAM
    hdr<46> = EncEnable;                // Encryption enabled flag
    hdr<47> = EncKey;                   // Encryption key index
    hdr<63:48> = LinkId[col];           // LLID
    hdr<71:64> = CRC8(hdr<63:8>);       // Calculate CRC8
    return hdr;
}
```

EnvStartHeader(wCol, epam)

The EnvStartHeader() function returns a new envelope header with the EnvType flag equal to 1, indicating that it is a start of a new envelope. If this envelope starts a new burst (i.e., all channels are idle) it updates EnvPam to the value of the epam variable provided in the MCRS_CTRL[].request primitive.

```
EQ EnvStartHeader(int col, int6 epam)
{
    EQ hdr;

    // Use provided 'epam' value if this envelope starts a new burst
    if(!TxActive[0] AND !TxActive[1] AND … AND !TxActive[NUM_CH-1])
        EnvPam = epam;

    hdr<7:0> = 0x01;                    // Control bits
    hdr<15:8> = 0xFB;                   // S character
    hdr<16> = 1;                        // EnvType identifies ESH
    hdr<17> = 0;                        // Reserved
    hdr<39:18> = EnvLeft[col];          // EnvLength
    hdr<45:40> = EnvPam;                // EPAM
    hdr<46> = EncEnable;                // Encryption enabled flag
    hdr<47> = EncKey;                   // Encryption key index
    hdr<63:48> = LinkId[col];           // LLID
    hdr<71:64> = CRC8(hdr<63:8>);       // Calculate CRC8
    return hdr;
}
```

GetFillerEQ(int col)

The GetFillerEQ() function returns an EQ value used to fill the transmit channel when no active envelopes are available. If this function is called when the transmission channel is active, it returns an inter-envelope idle EQ (IEI_EQ). Otherwise, it returns an inter-burst idle EQ (IBI_EQ).

```
EQ GetFillerEQ( int col)
{
    if( TxActive[col] )
```

```
            return IEI_EQ; //Inter-Envelope Idle
        else
            return IBI_EQ; //Inter-Burst Idle
    }
```

GetMacBlock(link_id)

The GetMacBlock() function retrieves eight octets (64 bits) of data from a MAC identified by the link_id parameter and returns an EQ (72 bits) that contains both the data and the corresponding eight control bits. If the retrieved bits contain a partial frame preamble, the preamble is shifted forward such that the entire preamble is returned in one EQ in which case the function invokes the PLS_DATA.request() primitive up to 127 times. If no data is available from the MAC for a particular byte, the function returns an IDLE control code for that octet. This is a blocking function that returns control to the calling routine after 64 or more successive invocations of the PLS_DATA.request() primitive.

```
IdleFlag[.] = {true};
// Previous octet from a MAC (link_id)
// was an Idle. Global array of Booleans
// that retain their values between successive
// calls to GetMacBlock()
EQ GetMacBlock(int16 link_id)
{
    EQ eq; // Consists of 8 bits of control (Ctrl[0…7])
           // and 8 octets of data (Data[0…7]), as shown in Figure 143-2
    if( link_id == ESC_LLID )
        return IBI_EQ; // Inter-burst Idle
    for( octet_index = 0; octet_index < 8; octet_index++ )
    {
        tx_data = GetMacOctet( link_id ); // Get 8 bits from MAC
        if( IsIdle(tx_data) AND !IdleFlag[link_id] ) // 1st Idle after Data
        {
            IdleFlag[link_id] = true;
            eq.Ctrl[octet_index] = 1; // Store /T/ character
            eq.Data[octet_index] = 0xFD;
        }
        else if( IsIdle(tx_data) ) // Idle after Idle
        {
            eq.Ctrl[octet_index] = 1; // Store /I/ character
            eq.Data[octet_index] = 0x07;
        }
        else if( IdleFlag[link_id] ) // 1st Data after Idle
        {
            IdleFlag[link_id] = false;
            octet_index = 0; // Shift to octet 0
            eq.Ctrl[octet_index] = 1; // Store /S/ character
            eq.Data[octet_index] = 0xFB;
        }
        else // Data after Data
        {
            eq.Ctrl[octet_index] = 0; // Store Data octet
            eq.Data[octet_index] = tx_data;
        }
    }
    return eq;
}
```

GetMacOctet(link_id)

This function returns an eight-bit vector from a MAC identified by the link_id parameter. When the MAC sublayer has data available, the return value is composed of eight OUTPUT_UNIT values (see 46.1.7.1.2) delivered by eight consecutive invocations of the PLS_DATA[link_id].request(OUTPUT_UNIT) primitive (see Figure 143–9). When the MAC sublayer has no data available (i.e., if the last seen OUTPUT_UNIT value was equal to DATA_COMPLETE), the return value is composed of eight DATA_COMPLETE values.

IsIdle(octet)

This function returns a Boolean value indicating whether the parameter octet represents a data octet or an idle octet. This function returns true if any bit in octet has a value of DATA_COMPLETE (see 46.1.7.1.2), otherwise, false is returned. Note that since MAC data output is aligned to octet boundaries, all bits in the parameter octet are either equal to DATA_COMPLETE or all bits are not equal to DATA_COMPLETE.

143.3.3.6 State diagrams

143.3.3.6.1 Input process

The MCRS shall implement the Input process as depicted in Figure 143–12.

The Input process accepts data from a MAC interface and transfers that data to the EnvTx buffer one EQ at a time. The process prepends an ESH to each envelope and overwrites each preamble with an ECH. Only one instance of the process is needed. The Input process fills one full row (all columns) of the EnvTx buffer on each cycle of InClk (InClk is half the effective rate of TX_CLK). In case of overlapping envelopes, blocks in multiple columns are retrieved from the same MAC.

The process keeps track of the envelope sizes for each LLID and does not exceed the allowed number of EQs for a given envelope. The process adjusts the MAC rate to account for FEC parity insertion in the PCS.

143.3.3.6.2 Transmit process

The MCRS shall implement the Transmit process as depicted in Figure 143–13.

The Transmit process outputs one 36-bit block (TXD[*ch*]<31:0> + TXC[*ch*]<3:0>) to its associated xMII interface on each edge of the TX_CLK signal. There is one instantiation of the Transmit process for each channel implemented in the device. The main function of the process is to transmit a column of one row from the EnvTx buffer on an existing channel. The Transmit process is synchronized to TX_CLK.

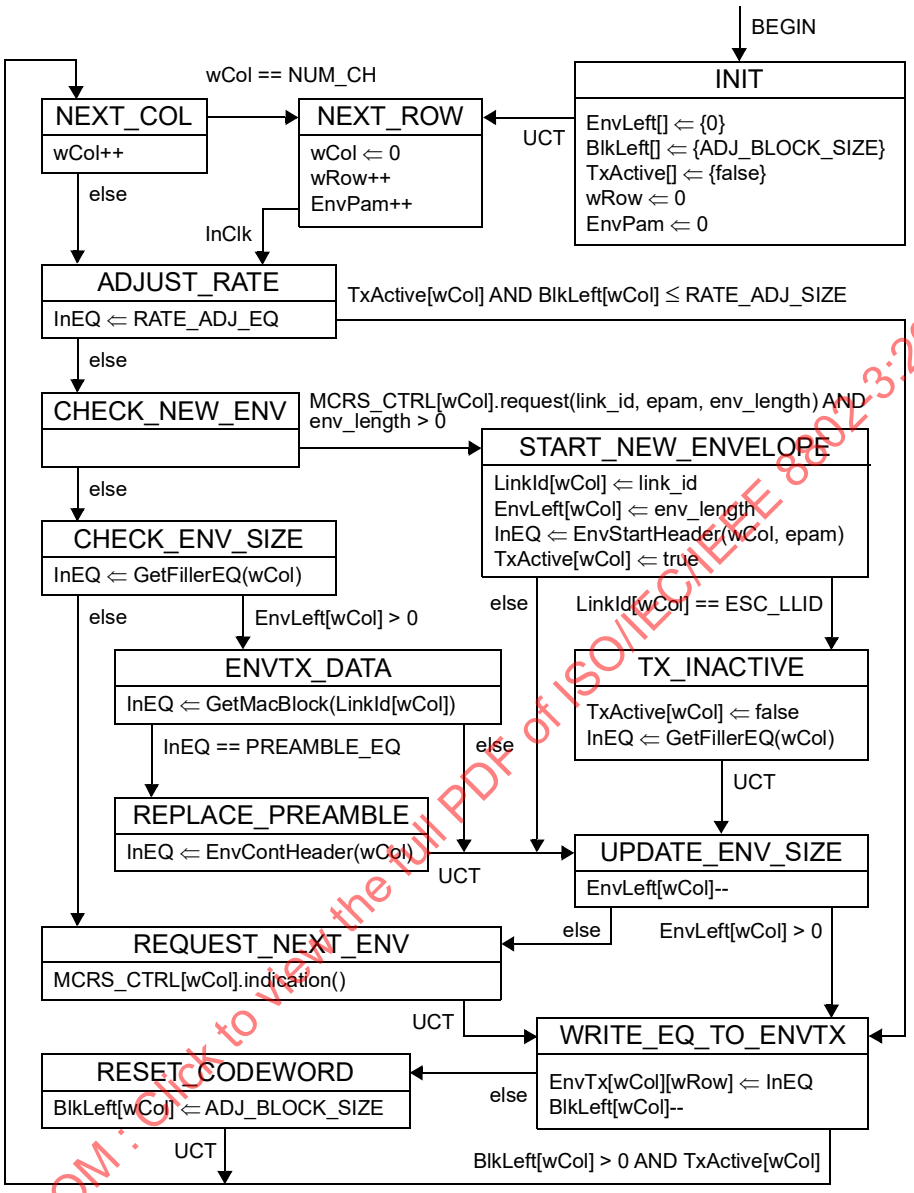


Figure 143–12—MCRS transmit function, Input process state diagram

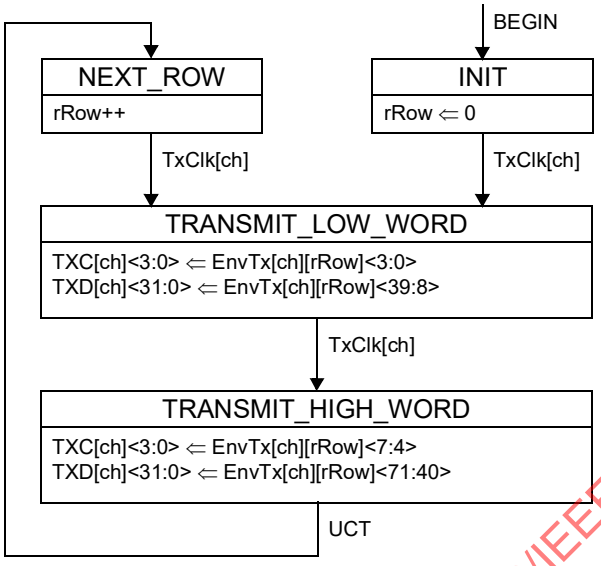


Figure 143–13—MCRS transmit function, Transmit process state diagram

143.3.4 Receive functional specifications

A functional block diagram of the MCRS receive path is illustrated in Figure 143–14. The MCRS interfaces are described in 143.3.1. The MCRS receive path is composed of two processes and one buffer. The Receive process, described in greater detail in 143.3.4.5.1, accepts two successive transfers from the associated xMII and consolidates them into an EQ, which is stored in the appropriate row of the EnvRx buffer. The Output process, described in greater detail in 143.3.4.5.2, pulls EQs from the EnvRx buffer and feeds them to the appropriate MAC as specified by the current LLID for that receive channel.

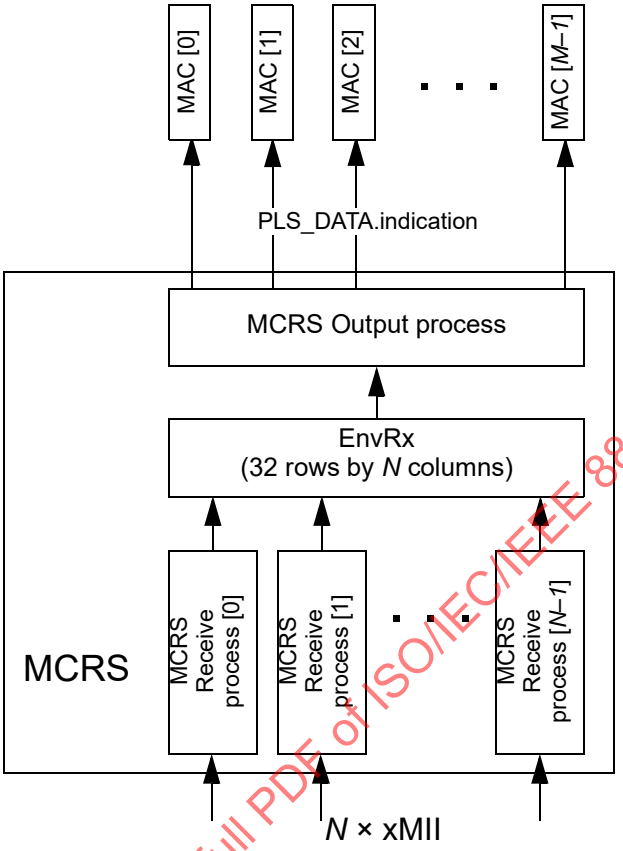


Figure 143–14—MCRS receive functional block diagram

143.3.4.1 Conventions

See 142.1.1

143.3.4.2 Constants

ES_HEADER
: Type: Integer
Description: The value of the envelope EnvType flag indicating the header is an envelope start header.
Value: 1

IEI_EQ
: See 143.3.3.3

RATE_ADJ_EQ
: See 143.3.3.3

PREAMBLE_EQ
: See 143.3.3.3

143.3.4.3 Variables

BEGIN
See 142.2.5.2

ch
See 143.3.3.4

EnvRx
Type: array of 72-bit blocks
Description: The EnvRx buffer is used to transfer information between the MCRS Receive process and the MCRS Output process. In this buffer, each cell, represented by the variable EnvRx stores one EQ (a 72-bit block) of information. The number of columns in EnvRx buffer is NUM_CH (see 143.3.3.3). The maximum number of rows is 64, as determined by the size of EPAM field in the envelope header (see 143.3.2). For some applications, fewer rows may be sufficient. The buffer is filled in parallel by NUM_CH instances of MCRS Receive process and is emptied sequentially by the MCRS Output process. For additional details, refer to 143.2.5.3.

EnvLeft[ch]
See 143.3.3.4

LinkId[ch]
See 143.3.3.4

OutClk
Type: Boolean
Description: The OutClk clear-on-read variable is set to true on each rising edge of TX_CLK.

OutEQ
Type: 72-bit binary array
Description: A temporary holding variable for one EQ used in the Output process.

rCol
Type: Integer
Description: The rCol variable represents the EnvRx buffer column currently being read by the MCRS Output process. Each column corresponds to a separate reception channel, i.e., a separate xMII interface.

rRow
Type: 6-bit integer
Description: The rRow variable represents the EnvRx buffer row index currently being read by the MCRS Output process.

RxClk[ch]
Type: Boolean
Description: The RxClk[ch] clear-on-read variables are set to true on each edge of the RX_CLK[ch] signals and represent the continuous clock that provides the timing reference for the transfer of the RXC[ch]<3:0> and RXD[ch]<31:0> signals received on the xMII channel ch.

RxEQ
Type: 72-bit binary
Description: The RxEQ variable represents the most recent EQ received from an xMII interface.

wCol

Type: Integer

Description: The wCol variable represents the EnvRx buffer column currently being written by the MCRS Receive process. Each column corresponds to a separate reception channel, i.e., a separate xMII interface.

wRow

Type: 6-bit integer

Description: The wRow variable represents the EnvRx buffer row index currently being written by the MCRS Receive process.

143.3.4.4 Functions

IsHeader(eq)

The IsHeader(eq) function returns true if the parameter eq represents an envelope header. An envelope header begins with a /S/ Start control character.

```
bool IsHeader(EQ eq)
{
    return(   eq<7:0> == 0x01 AND              // Control bits
              eq<15:8> == 0xFB AND             // Start Control Code /S/
              eq<71:64> == CRC8(eq<63:8>));    // Matching CRC8
}
```

IsMisaligned(eq)

The IsMisaligned(eq) function returns true if the parameter eq is misaligned, i.e., shifted by a half EQ.

```
bool IsMisaligned(EQ eq)
{
    return (  eq<7:0> == 0x1E AND           // Control bits
              eq<39:8> == IBI_EQ<71:40> AND // 1st Transfer: IBI_EQ
              eq<47:40> == 0xFB );          // 2nd Transfer: Env. Header
}
```

OutputToMac(LinkId[rCol], OutEQ)

The OutputToMac(LinkId[rCol], OutEQ) function transfers the eight information bytes in the OutEQ parameter to the MAC associated with the LLID value of LinkId[rCol] per the eight control bits in the OutEQ parameter.

```
OutputToMac(int16 link_id, EQ eq)
{
    for( octet_index = 0; octet_index < 8; octet_index++ )
    {
        if ( eq.Ctrl[octet_index] == 0 ) // Receive data octet
        {
            data_valid = true;
            rx_data = eq.Data[octet_index];
        }
        else if ( eq.Data[octet_index] == 0xFB ) // Rx /S/ character
        {
            data_valid = true;
            rx_data = 0x55; // Replace /S/ with preamble
        }
        else // Rx other ctrl. character, including /T/ (value 0xFD)
        {
```

```
                data_valid = false;
                rx_data = 0x07; // Replace with /I/
            }
            SetMacOctet( link_id, rx_data, data_valid ); // Set 8 bits to MAC
        }
    }
```

SetMacOctet(link_id, rx_data, data_valid)

This function passes eight bits of rx_data vector to the MAC instance identified by the link_id parameter. The rx_data value is passed to the MAC using eight consecutive invocations of the PLS_DATA[link_id].indication(INPUT_UNIT) primitive (see 46.1.7.2), along with eight invocations of the PLS_DATA_VALID[link_id].indication(DATA_VALID_STATUS) primitive (see 46.1.7.5). When the parameter data_valid is equal to true, the DATA_VALID_STATUS has the value of DATA_VALID. When the parameter data_valid is equal to false, the DATA_VALID_STATUS has the value of DATA_NOT_VALID.

143.3.4.5 State diagrams

143.3.4.5.1 Receive process

The ONU and OLT MCRS shall implement the Receive process as depicted in Figure 143–15.

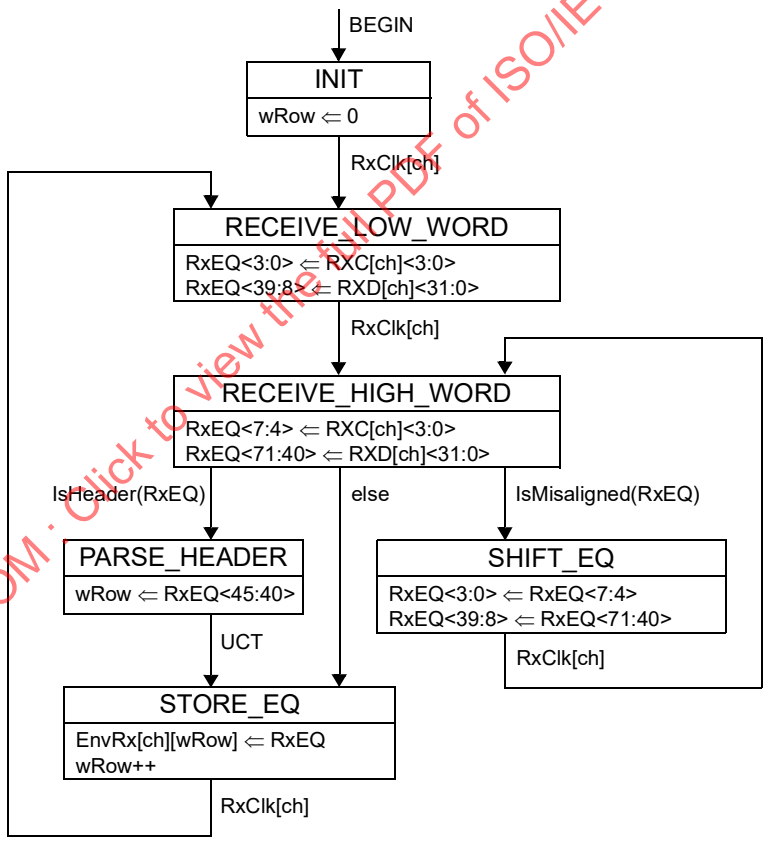


Figure 143–15—MCRS receive function, Receive process state diagram

This process forms an EQ from two successive xMII transfers. The process first verifies proper alignment of the EQ and, if misaligned, shifts the input by half of an EQ (four bytes). No other error checking is performed by this process. When an envelope header is received, the EPAM field is extracted and used as a

write position into the EnvRx buffer. Because the phase of the receive clock (RX_CLK[ch]) in every channel is different, due to different delay and transport skew, a separate instance of the Receive process is required for each channel implemented.

143.3.4.5.2 Output process

The ONU and OLT MCRS shall implement the MCRS Output process as depicted in Figure 143–16.

The Output process outputs EQs to the proper MAC. In the case of overlapping envelopes from the same LLID, data from multiple channels is properly serialized. A corrupted header may lead to loss of a frame, but no subsequent frames are lost due to the error since the next ECH resynchronizes the process for the following frame.

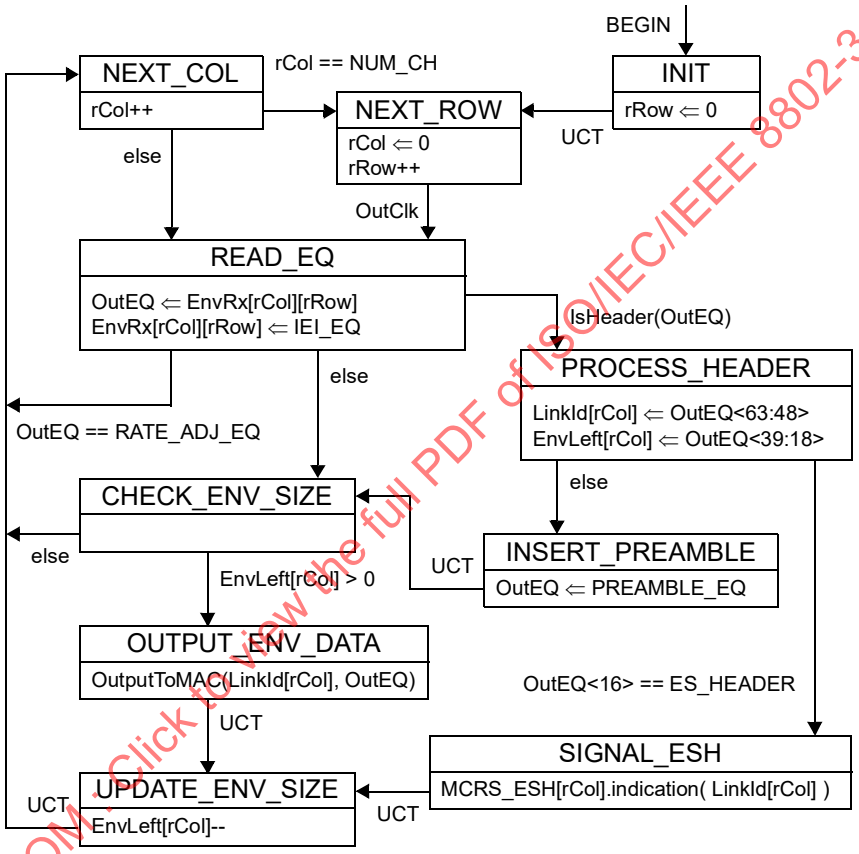


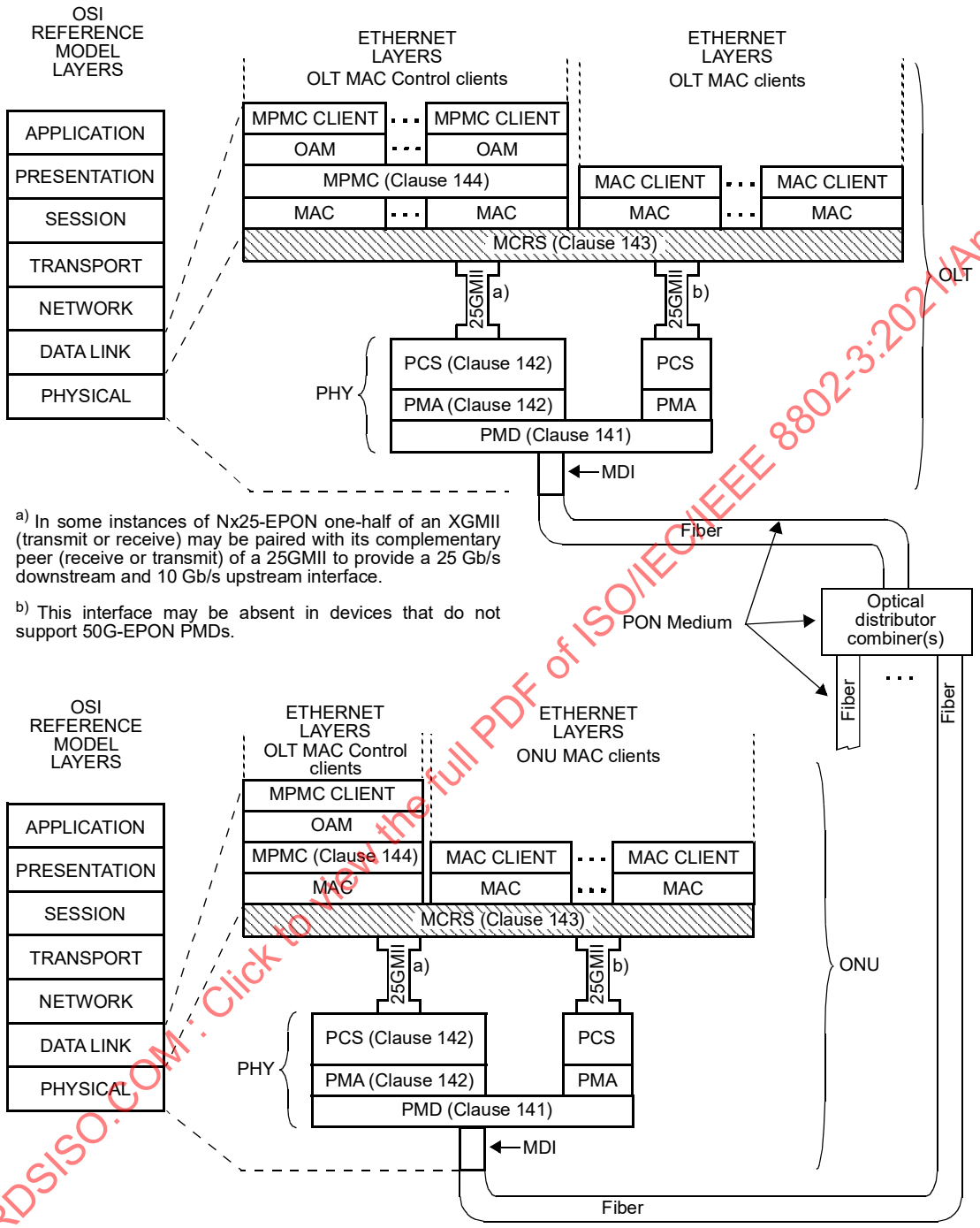
Figure 143–16—MCRS receive function, Output process state diagram

143.4 Nx25G-EPON MCRS requirements

143.4.1 Nx25G-EPON architecture

This subclause describes the MCRS requirements for Nx25G-EPON point-to-multipoint (P2MP) networks. P2MP networks are passive optical networks (PONs) that connect multiple optical network units (ONUs) to a single optical line terminal (OLT). The architecture is asymmetric, based on a tree and branch topology utilizing passive optical splitters.

A transmission direction from the OLT towards the ONUs is referred as the downstream direction and transmission direction from an ONU toward the OLT is referred as the upstream direction.



a) In some instances of Nx25-EPON one-half of an XGMII (transmit or receive) may be paired with its complementary peer (receive or transmit) of a 25GMII to provide a 25 Gb/s downstream and 10 Gb/s upstream interface.

b) This interface may be absent in devices that do not support 50G-EPON PMDs.

MCRS described in this clause

25GMII= 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 143–17—Relationship of Nx25G-EPON P2MP PMD to the ISO/IEC OSI reference model

The MCRS is used with Nx25G-EPON point-to-multipoint (P2MP) networks in order to interface multiple MAC instances with one or two 25GMII channels in each direction. Figure 143–17 illustrates the relationship of the MCRS and the OSI protocol stack for Nx25G–EPON.

Nx25G-EPON OLT and ONU PMDs are defined in Clause 141, with the respective Nx25G-EPON PCS defined in 142.2 and 142.3.

The MCRS in Nx25G-EPON architecture serves as an interfaces sublayer between the MAC sublayer and 25GMII. The 25GMII interface is defined in Clause 106.

143.4.1.1 MCRS channels

An MCRS channel that carries information from the OLT to the ONU is referred to as the downstream channel, and the channel that carries information from an ONU to the OLT is referred to as the upstream channel.

The 25/10G-EPON and 25G/25G-EPON architectures shall implement a single MCRS channel in each direction.

The 50/10G-EPON and 50/25G-EPON architectures shall implement two MCRS channels in the downstream direction and a single channel in the upstream direction.

The 50/50G-EPON architecture shall implement two channels in each direction.

When two channels are implemented in the same direction, channel bonding of these two channels shall be supported. Table 143–6 summarizes MCRS channels for Nx25G-EPON.

Each MCRS channel is bound to a separate PCS instance via a separate xMII instance. Channels operating at 25 Gb/s are bound to 25GMII, whereas the channel operating at 10 Gb/s is bound to an XGMII instance. Thus, for any given system, there is a one-to-one correspondence between the MCRS channel count and the number of xMII instances supported.

Table 143–6—MCRS channel designation and capabilities

Designation	MCRS channel	MCRS channel function
DC0	Downstream channel 0	All ONUs receive this MCRS channel, broadcast.
DC1	Downstream channel 1	Only ONUs capable of receiving at 50 Gb/s support this MCRS channel.
UC0	Upstream channel 0	All ONUs transmit on this MCRS channel.
UC1	Upstream channel 1	Only ONUs capable of transmitting at 50 Gb/s support this MCRS channel.

143.4.1.2 Symmetric and asymmetric data rates

The Nx25G-EPON architecture supports symmetric and asymmetric data rates. The symmetric data rate systems include 25/25G-EPON or 50/50G-EPON. The asymmetric rate systems include 25/10G-EPON, 50/10G-EPON, and 50/25G-EPON.

A distinction is made regarding the underlying mechanisms of achieving the asymmetric data rates. In 25/10G-EPON systems, the asymmetric data rate is achieved via the MCRS channel rate asymmetry, where a single downstream MCRS channel DC0 operates at 25 Gb/s and a single upstream MCRS channel UC0 operates at 10 Gb/s. Additional details for MCRS implementations supporting the channel rate asymmetry are provided in 143.4.4. In 50/25G-EPON systems, the asymmetric data rate is achieved via the MCRS

channel number asymmetry, where two MCRS channels are active in the downstream direction (DC0 and DC1), but only a single MCRS channel UC0 is active in the upstream direction. In 50/25G-EPON systems, upstream and downstream MCRS channels operate at the data rate of 25 Gb/s.

Both the channel rate asymmetry and the channel number asymmetry mechanisms may be combined, as is the case in 50/10G-EPON systems, where there are two downstream MCRS channels operating at 25 Gb/s and a single upstream MCRS channel operating at 10 Gb/s.

An Nx25G-EPON system may serve ONUs that support different numbers of MCRS channels (see 143.4.1). Therefore, some ONUs are only able to receive and transmit data on MCRS channels DC0 and UC0, some are able to receive on DC0 and DC1 and transmit on UC0 and UC1 or just on UC0.

143.4.1.3 Nx25G-EPON application-specific parameters

For definitions of constants, variables, and functions, see 143.3.3 (transmit direction) and 143.3.4 (receive direction).

143.4.1.3.1 Constants

ADJ_BLOCK_SIZE
: Value: 257

NUM_CH
: Value: 1 for devices supporting only 10 Gb/s or 25 Gb/s operation over a single channel; 2 for devices supporting 50 Gb/s operation over two channels.

RATE_ADJ_SIZE
: Value: 33

143.4.1.3.2 Transmit variables

EnvTx
: Description: Since there is no timing jitter or channel skew to be removed at the transmitting device, the size of the EnvTx buffer may be reduced to only two rows. If this optimization is implemented, the variables rRow and wRow are represented by 1-bit unsigned integers.

143.4.2 MCRS time synchronization

For MCRS to provide the intended skew and jitter remediation capabilities, a sufficient delay margin has to be built into the MCRS buffering at the ONU and the OLT. Such delay margin is established at the ONU registration time by proper setting of MCRS EnvRx read and write pointers at the OLT and the ONU.

Upon power-up or reset, an unregistered ONU synchronizes to the received clock and aligns to 257-bit block and FEC codeword boundaries on each of its active (enabled) receive channels (see ONU Synchronizer process, 142.3.5.5). After that, the received data is passed to FEC decoder, which introduces a near-constant delay. Corrected data from the FEC decoder is passed to xMII and is received into the ONU MCRS EnvRx buffer.

The following are the ONU rules for setting the EnvRx write and read pointers:

a) Write pointer
   1) The ONU MCRS always sets the write pointer for the EnvRx buffer to equal the EPAM value in any envelope header it receives, regardless of the LLID value in that envelope header.

2) If multiple receive channels are active, the write pointers are set independently for each channel based on EPAM values in envelope headers received on each channel.

b) Read Pointer
   1) The read pointer increments synchronously with the LocalTime counter, which is locked to the xMII receive clock of the active (enabled) receive channel with the lowest index.
   2) In an unregistered ONU, upon every update of a write pointer associated with the receive channel with the lowest index, the read pointer is also updated according to the following equation:

$$ReadPointer = WritePointer \text{ XOR } 0x20 \quad (143–1)$$

In the OLT, the PCS receiver synchronizes on start-of-burst delimiter (see OLT Synchronizer process, 142.3.5.5) independently on each active (enabled) receive channel. After that, the received data is passed to the FEC decoder, which introduces a near-constant delay. Corrected data from the FEC decoder is passed to the xMII and is received into the OLT MCRS EnvRx buffer. The following are the OLT rules for setting the EnvRx write and read pointers:

a) Write pointer
   1) When receiving an envelope from a registered ONU, the OLT MCRS sets the write pointer for the EnvRx buffer to equal the EPAM value in the envelope header.
   2) When receiving an envelope from an unregistered ONU, the OLT MCRS sets the write pointer according to the following equation:

$$WritePointer = ReadPointer \text{ XOR } 0x20 \quad (143–2)$$

NOTE—The OLT MCRS determines that an envelope is from an unregistered ONU by either checking the LLID value in the envelope header (DISC_PLID) or by checking that an envelope header is received during the discovery window (see 144.1.1.3). Otherwise, the envelope is assumed to be received from a registered ONU.

b) Read Pointer
   1) The read pointer increments synchronously with the LocalTime counter, which is locked to the xMII transmit clock.
   2) If the OLT implements multiple transmit channels, all these channels share the same xMII transmit clock. Correspondingly, the read pointers for all channels increment synchronously and maintain equal values.

The above set of rules produces a delay of 32 EQT that is built into the ONU MCRS receive path and a similar delay of 32 EQT that is built into the OLT MCRS receive path. Therefore, the total round-trip delay measured by the MPCP (see 144.3.1.1) during an ONU discovery and registration includes a built-in margin of 64 EQT that is used to eliminate skew between different channels or the timing jitter within a channel.

143.4.3 Delay variability constraints

The MPCP relies on strict timing based on the distribution of timestamps. The MCRS is designed to allow a delay variability of up to 64 EQTs. During the normal operation of a registered ONU, the delay any EQ experiences in the EnvRx buffer is complementary to the accumulated skew and jitter that this EQ encounters after leaving the EnvTx buffer in the transmitting MCRS, such that the sum of the two delays remains constant.

143.4.4 Asymmetric rate operation

The 25/10G-EPON and 50/10G-EPON systems are characterized by channel rate asymmetry. In such systems, downstream transmission uses one or two channels operating at 25 Gb/s, while the upstream transmission uses a single channel operating at 10 Gb/s.

Figure 143–18 illustrates the layering diagram of a 25/10G-EPON OLT and ONU. In the OLT, the MCRS sublayer serves MAC entities supporting the transmit data rate of 25 Gb/s and the receive data rate of 10 Gb/s. In turn, the MCRS sublayer is connected to the transmit path of a 25GMII and the receive path of an XGMII. In the ONU, the MCRS sublayer serves MAC entities supporting the transmit data rate of 10 Gb/s and the receive data rate of 25 Gb/s. The MCRS sublayer is connected to the transmit path of an XGMII and the receive path of a 25GMII.

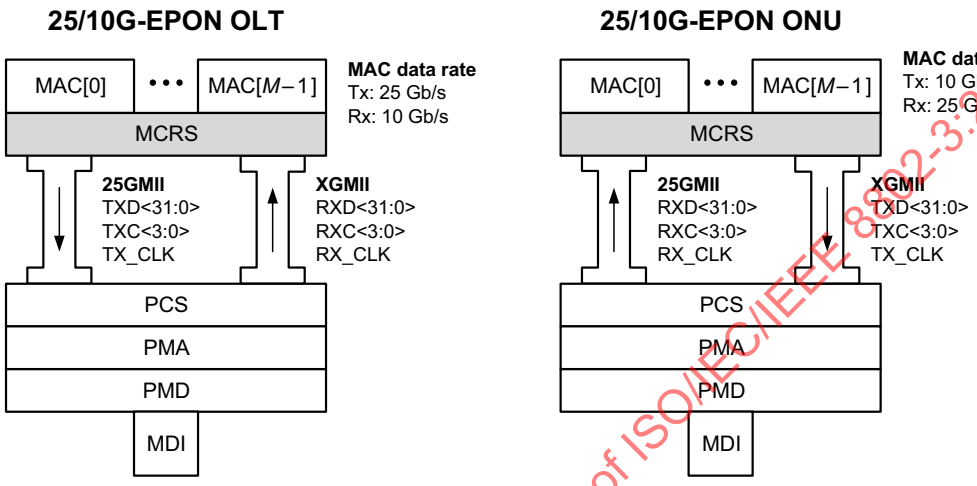


Figure 143–18—25G/10G-EPON OLT and ONU layering diagram

Because of the required close coupling between the MCRS clock (InClk, see 143.3.3.4 and OutClk, see 143.3.4.3) and MPCP clock (LocalTime, see 144.2.1.2), the MCRS buffer read pointers advance by one every EQT, i.e., both downstream and upstream channels within MCRS operate at a nominal data rate of 25 Gb/s. To adapt the MCRS channel rate to the MAC data rate of 10 Gb/s, the MCRS channel is throttled by inserting a padding EQ at the rate of 3 padding EQs per every 5 EQTs. The transfer of information through the 10 Gb/s MCRS channel is illustrated in Figure 143–19.

The padding EQs are interleaved with information EQs using the following pattern:

<information EQ> <padding EQ> <padding EQ> <information EQ> <padding EQ>

The usage of the padding EQs is entirely confined to the MCRS sublayer and does not affect the definition of interfaces to either of the adjacent sublayers. Therefore the definition of the padding EQ format and values are left to implementations.

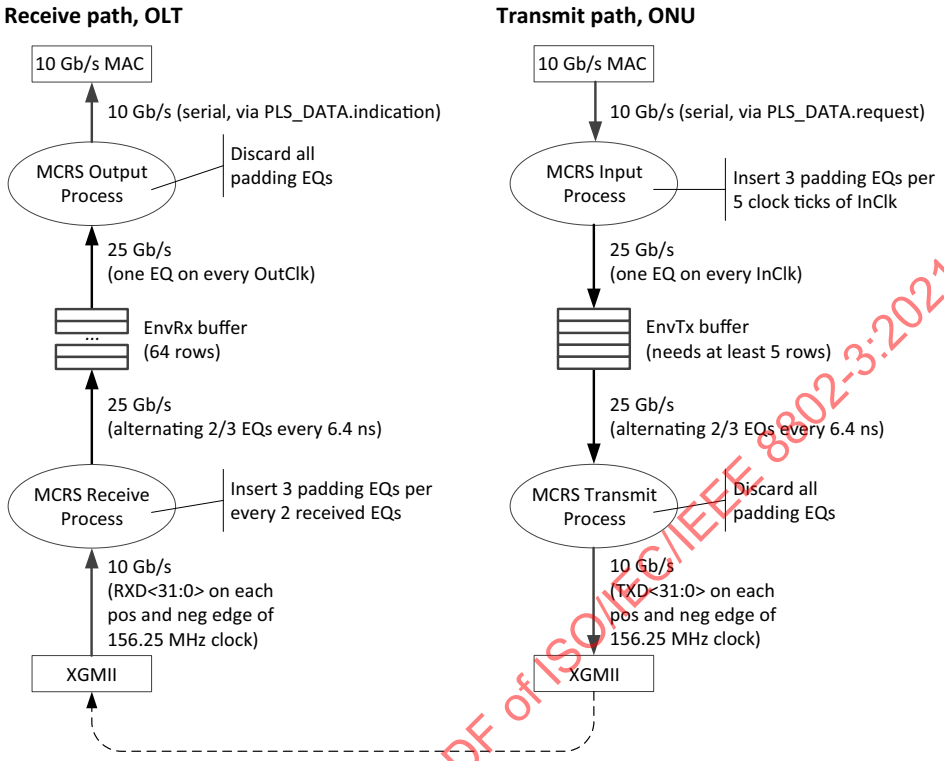


Figure 143–19—Upstream channel operating at 10 Gb/s

143.5 Protocol implementation conformance statement (PICS) proforma for Clause 143, Multi-Channel Reconciliation Sublayer[6]

143.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 143, Multi-Channel Reconciliation Sublayer, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

143.5.2 Identification

143.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

143.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ca-2020, Clause 143, Multi-Channel Reconciliation Sublayer
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ca-2020.)	

Date of Statement	

[6] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

143.5.3 Generic MCRS

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	Envelope header structure	143.3.2	Uses the format shown in Figure 143–10	M	Yes [ ]
MC2	Input process	143.3.3.6.1	Implements the state diagram as depicted in Figure 143–12	M	Yes [ ]
MC3	Transmit process	143.3.3.6.2	Implements the state diagram as depicted in Figure 143–13	M	Yes [ ]
MC4	Receive process	143.3.4.5.1	Implements the state diagram as depicted in Figure 143–15	M	Yes [ ]
MC5	Output process	143.3.4.5.2	Implements the state diagram as depicted in Figure 143–16	M	Yes [ ]

143.5.4 MCRS in Nx25G-EPON

143.5.4.1 Major capabilities/option

Item	Feature	Subclause	Value/Comment	Status	Support
*2510G	25/10G-EPON functionality	143.4.1.1	Device supports functionality required for 25/10G-EPON	O.1	Yes [ ] No [ ]
*2525G	25/25G-EPON functionality	143.4.1.1	Device supports functionality required for 25/25G-EPON	O.1	Yes [ ] No [ ]
*5010G	50/10G-EPON functionality	143.4.1.1	Device supports functionality required for 50/10G-EPON	O.1	Yes [ ] No [ ]
*5025G	50/25G-EPON functionality	143.4.1.1	Device supports functionality required for 50/25G-EPON	O.1	Yes [ ] No [ ]
*5050G	50/50G-EPON functionality	143.4.1.1	Device supports functionality required for 50/50G-EPON	O.1	Yes [ ] No [ ]

143.5.4.2 MCRS implementation in Nx25G-EPON

Item	Feature	Subclause	Value/Comment	Status	Support
EPON1	Number of MCRS channels	143.4.1.1	Implement a single channel in downstream direction and a single channel in upstream direction	2510G:M or 2525G:M	Yes [ ] N/A [ ]
EPON2	Number of MCRS channels	143.4.1.1	Implement two channels in downstream direction and a single channel in upstream direction	5010G:M or 5025G:M	Yes [ ] N/A [ ]
EPON3	Number of MCRS channels	143.4.1.1	Implement two channels in downstream direction and two channels in upstream direction	5050G:M	Yes [ ] N/A [ ]
EPON4	Channel bonding	143.4.1.1	Device supports channel bonding	50G10G:M or 50G25G:M or 50G50G:M	Yes [ ] N/A [ ]

144. Multipoint MAC Control for Nx25G-EPON

144.1 Overview

This clause defines the mechanisms and control protocols required in order to reconcile the 25 Gb/s or 50 Gb/s passive optical network (PON) into the Ethernet framework. A PON is an optical network with no active elements in the signal's path from source to destination. The only interior elements used in a PON are passive optical components, such as optical fiber, splices, and splitters. When combined with the Ethernet protocol, such a network is referred to as an Ethernet passive optical network (EPON).

Topics covered in this clause include allocation of transmission resources in EPON, discovery and registration of EPON devices, and reporting queue occupancy to higher layers to facilitate dynamic bandwidth allocation schemes and statistical multiplexing across the PON.

This clause does not address specific bandwidth allocation strategies, authentication of end devices, quality-of-service definitions, provisioning, or management.

The Multipoint MAC Control (MPMC) sublayer defined in this clause includes two protocols:

— Multipoint Control Protocol (MPCP) responsible for arbitration of TDM-based access to the P2MP medium
— Channel Control Protocol (CCP) responsible for querying and control of multiple channels within the Nx25G-EPON PHY

The MPMC functionality shall be implemented for subscriber access devices containing point-to-multipoint (P2MP) Physical Layer devices defined in Clause 141 and Clause 142.

144.1.1 Principles of point-to-multipoint operation

A P2MP medium is an asymmetric medium based on a tree (or trunk-and-branch) topology. The DTE connected to the trunk of the tree is called an optical line terminal (OLT) and the DTEs connected at the branches of the tree are called optical network units (ONUs). The OLT typically resides at the service provider's facility, while the ONUs are located at the subscriber premises. A simplified P2MP topology example is depicted in Figure 144–1. Clause 67 provides additional examples of P2MP topologies.

144.1.1.1 Transmission arbitration

In the downstream direction (from the OLT to an ONU), signals transmitted by the OLT pass through a 1:*N* passive splitter (or cascade of splitters) and reach each ONU.

In the upstream direction (from the ONUs to the OLT), the signal transmitted by an ONU would only reach the OLT but not other ONUs. To avoid upstream data collisions, transmission windows (grants) for all ONUs are controlled in such a way that only a single ONU's transmission reaches the OLT at any given time. The MPCP (see 144.3) is responsible for timing and arbitrating the ONU transmissions. This arbitration is achieved by allocating transmission windows (grants) to ONUs. An ONU defers its transmission until the start of its transmission window. When the transmission window starts, the ONU transmits its queued frames at full line rate for the duration of this transmission window.

Reporting of a queue occupancy state or congestion by different ONUs assists in optimal allocation of the transmission windows across the PON.

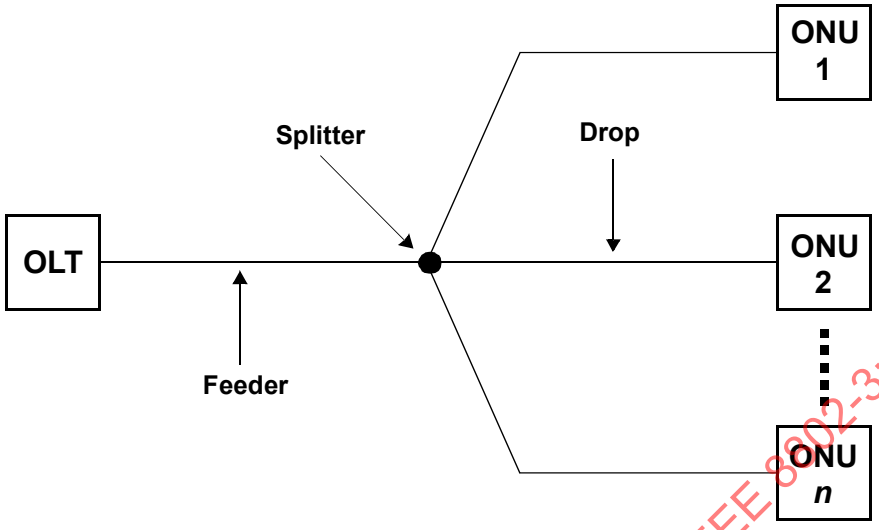


Figure 144–1—PON topology example

144.1.1.2 Concept of logical links

OLT and ONU devices instantiate multiple MAC instances (see Figure 144–2). P2MP architectures are best viewed as a collection of logical point-to-point and/or P2MP links. A logical link is created in the Multi-Channel Reconciliation Sublayer (MCRS), below the MAC by tagging each frame (or frame fragment) with a logical link identification (LLID) value and binding each instance of a MAC to a specific LLID value. See 143.2.1 for explanation of the mechanism of logical link operation.

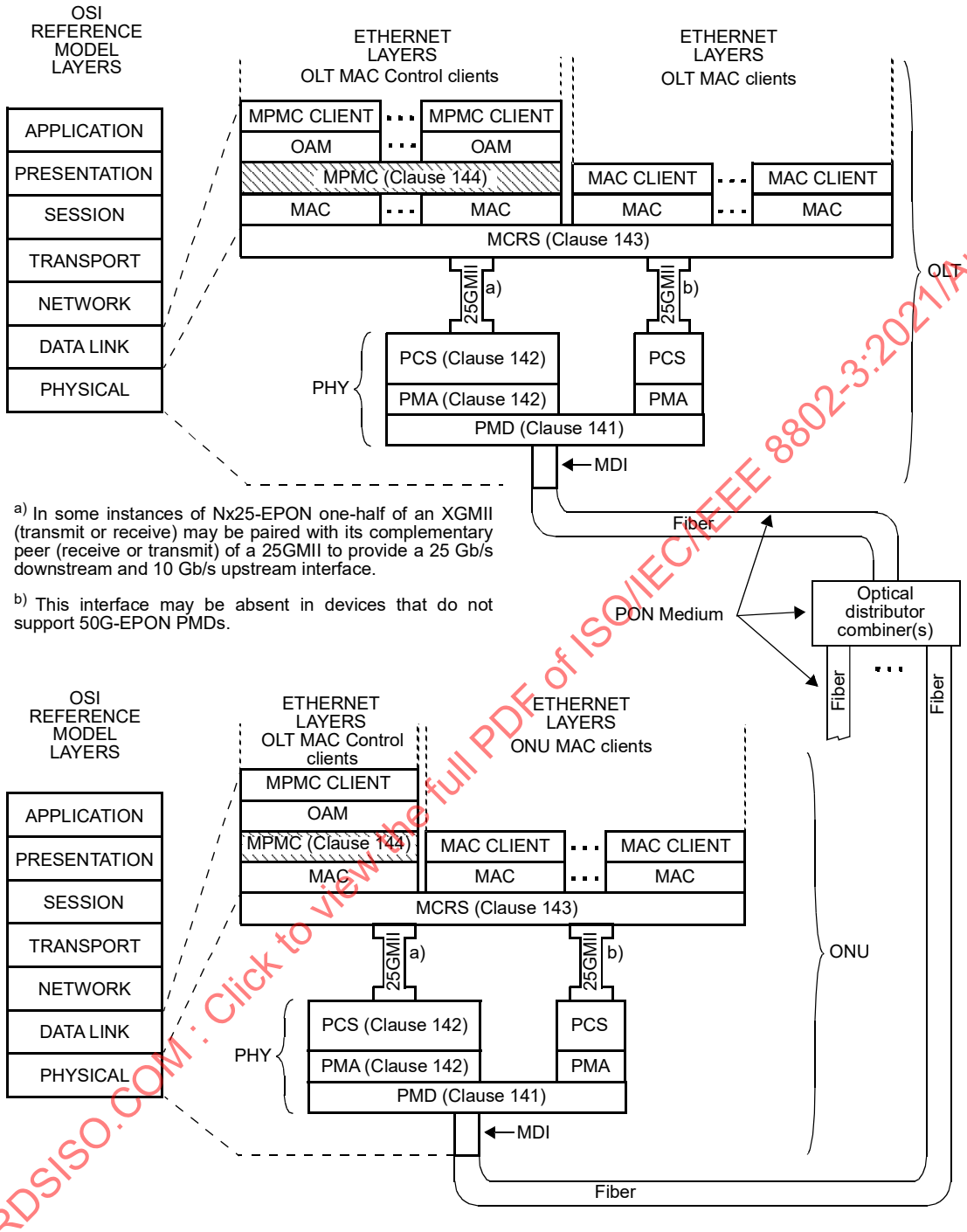
A logical connection is formed when a MAC instance at the OLT and a MAC instance at the ONU are bound to the same LLID value. A point-to-point logical link connects a single MAC instance at the OLT to a single MAC instance at the ONU. A P2MP logical link takes advantage of the broadcasting nature of the P2MP topology and connects a single MAC instance at the OLT to multiple MAC instances in different ONUs. In a P2MP logical link, MAC instances in multiple ONUs are bound to the same LLID value.

By default, the OLT is connected to each ONU via two point-to-point logical links: one link is used for MPMC traffic, such as MPCPDUs (see 144.3) and the other link is used for management traffic, such as OAMPDUs (see Clause 57). These two connections per each ONU are established during the Discovery process (see 144.3.5).

Several single-copy broadcast logical links are pre-defined for specific purposes (see Table 144–1).

Additional point-to-point and/or P2MP links between the OLT and ONUs may be provisioned by network management based on specific access network configuration and service requirements. Provisioning of such additional logical links is outside the scope of this standard. Different types of logical links are described in 144.3.4.

Although the OLT and ONUs instantiate multiple MAC entities, each device may use a single MAC address. Within the EPON Network, MAC instances are uniquely identified by their LLID.



[a] In some instances of Nx25-EPON one-half of an XGMII (transmit or receive) may be paired with its complementary peer (receive or transmit) of a 25GMII to provide a 25 Gb/s downstream and 10 Gb/s upstream interface.

[b] This interface may be absent in devices that do not support 50G-EPON PMDs.

MPMC described in this clause

25GMII= 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 144–2—Relationship of EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

144.1.1.3 ONU discovery and registration

As was explained in 144.1.1.1, the upstream transmissions in an EPON are arbitrated by the OLT. Before any newly connected ONU can be scheduled for the upstream transmission, it needs to be discovered by the OLT. The Discovery process is used to detect the newly-connected ONUs.

At a high level, the Discovery process schedules a periodic discovery window – a timeslot during which only the unregistered ONUs are allowed to transmit their registration request. These registration request messages allow the OLT to learn the MAC address and to measure the round-trip propagation time of each new ONU. As part of the Discovery process, the new ONU is assigned its initial LLID values (see 144.1.1.2) and that allows this ONU to receive downstream traffic and also be scheduled for the upstream transmission.

The Discovery process is described in more detail in 144.3.7.

144.1.2 Position of Multipoint MAC Control (MPMC) within the IEEE 802.3 hierarchy

Figure 144–2 depicts the architectural positioning of the MPMC sublayer with respect to the MAC and the MPMC client. The MPMC sublayer extends the MAC Control sublayer to support multiple clients and additional MAC control functionality.

144.1.3 Functional block diagram

Figure 144–3 and Figure 144–4 provide a functional block diagram of the MPMC architecture for the OLT and the ONU, respectively.

144.1.4 Service interfaces

The MAC clients communicate directly with dedicated MAC instances using the standard service interface specified in 2.3. The MPMC does not interface with any MAC Clients.

The MPMC clients communicate with MPMC instances using the service interface defined in this clause. Each MPMC instance communicates with the underlying MAC sublayer using the standard service interface specified in 4A.3.2. Similarly, MPMC communicates internally using primitives and interfaces consistent with definitions in Clause 31.

144.1.4.1 MAC Control service (MCS) interface

The MCS interface is an interface between the MAC Control sublayer and the MPMC client above it (see Figure 144–3 and Figure 144–4). The definition and behavior of the MPMC client is outside the scope of this standard.

The MAC Control sublayer and the MPMC client communicate via MCS:MA_CONTROL.indication and MCS:MA_CONTROL.request primitives. In the state diagrams used in this clause, the following abbreviations are used:

— MCSI(indication_operand_list) is equivalent to:
MCS:MA_CONTROL.indication(opcode, indication_operand_list), as defined in 31.3.2.
— MCSR(request_operand_list) is equivalent to:
MCS:MA_CONTROL.request(destination_address, opcode, request_operand_list), as defined in 31.3.1.

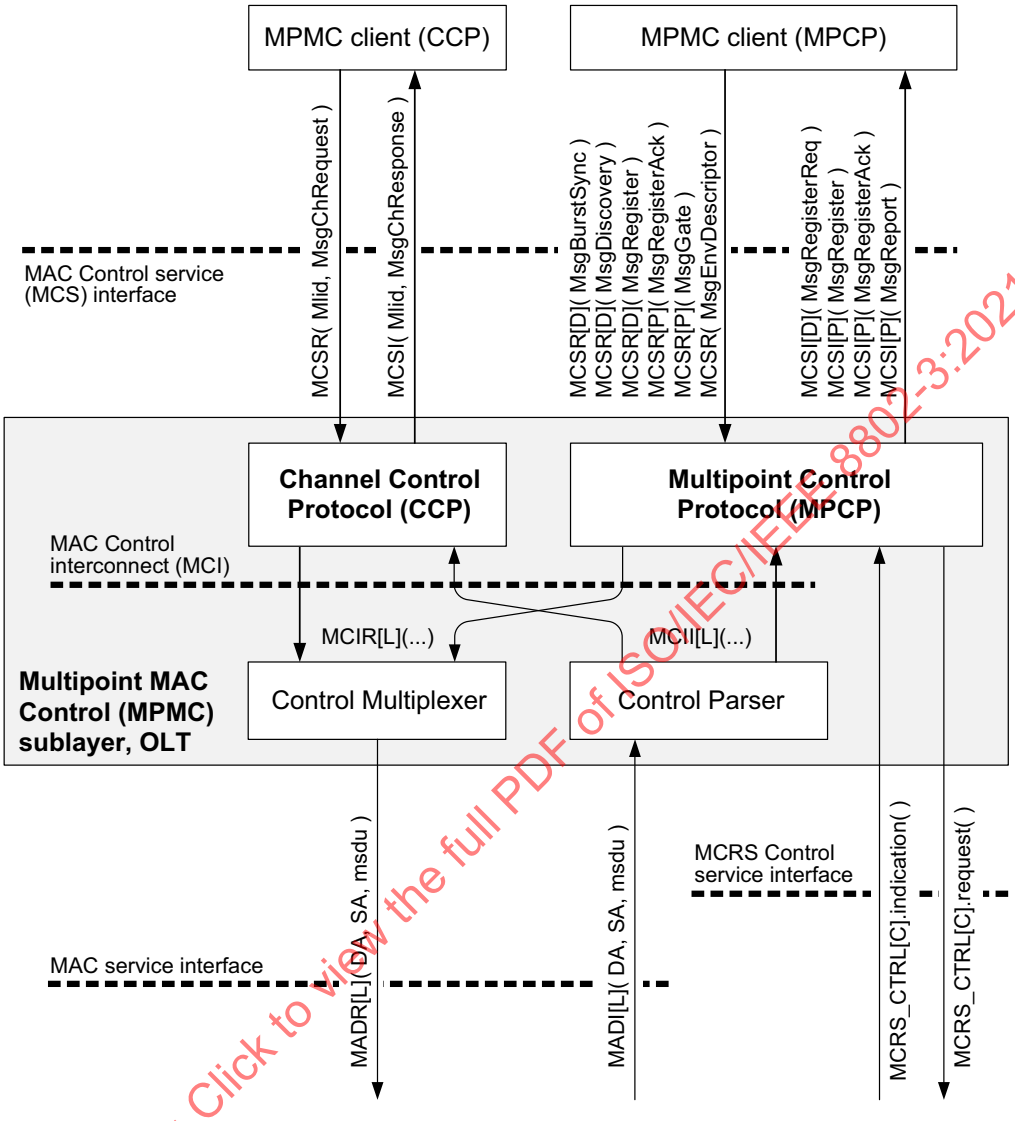


Figure 144–3—OLT Multipoint MAC Control (MPMC) sublayer functional block diagram

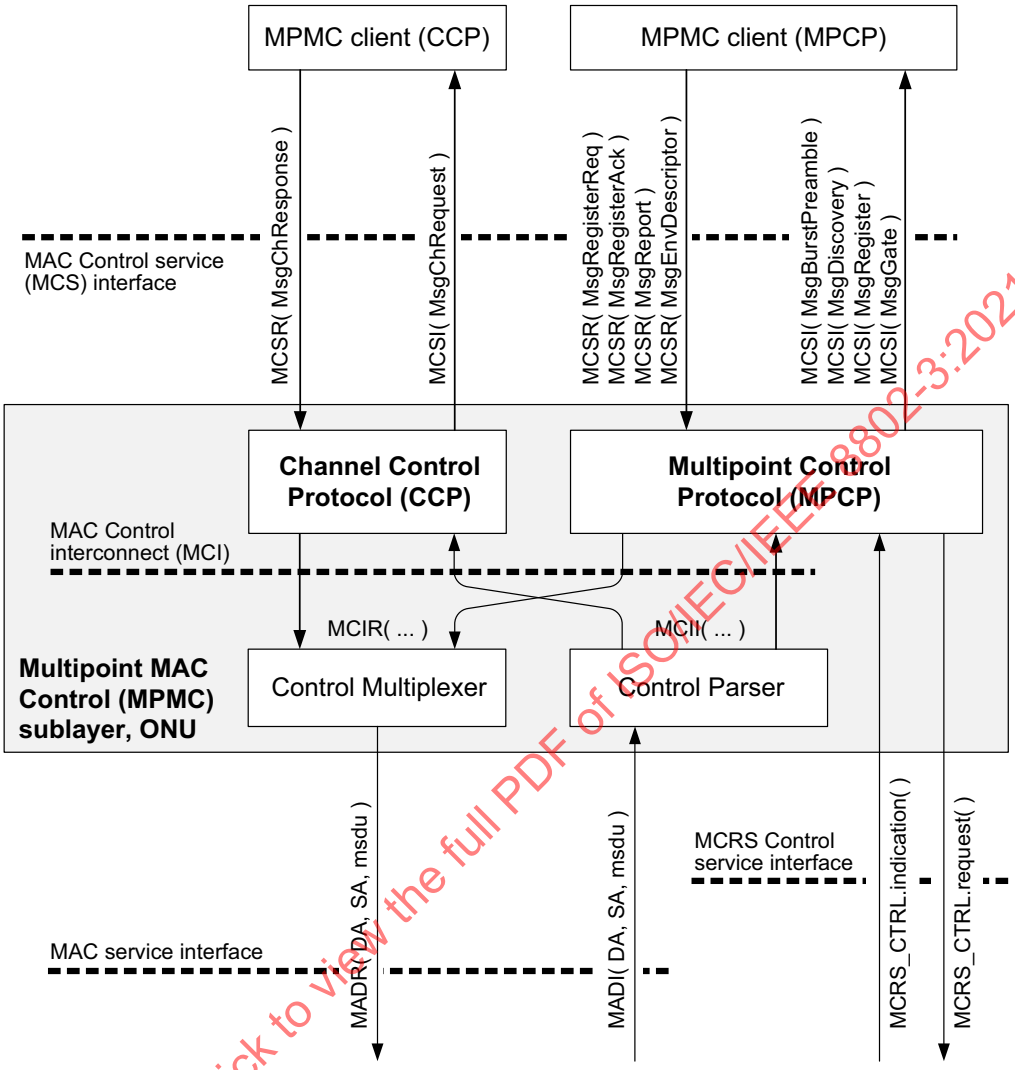


Figure 144–4—ONU Multipoint MAC Control (MPMC) sublayer functional block diagram

144.1.4.2 MAC Control interconnect (MCI)

MCI is an internal interface between the Control Parser/Control Multiplexer and other opcode-specific functions of the MAC Control sublayer (see Figure 144–3 and Figure 144–4).

The Control Parser and Control Multiplexer communicate with opcode-specific functions via MCI:MA_CONTROL.indication and MCI:MA_CONTROL.request primitives. In the state diagrams used in this clause, the following abbreviations are used:

— MCII(indication_operand_list) is equivalent to:
MCI:MA_CONTROL.indication(opcode, indication_operand_list), as defined in 31.3.2.
— MCIR(request_operand_list) is equivalent to:
MCI:MA_CONTROL.request(destination_address, opcode, request_operand_list), as defined in 31.3.1.

144.1.4.3 MAC service Interface

The MAC service interface is an interface between the MAC sublayer and the MAC Control sublayer above it (see Figure 144–3 and Figure 144–4).

The MAC sublayer and MAC Control sublayer communicate via MAC:MA_DATA.indication and MAC:MA_DATA.request primitives. The following abbreviations are used in this clause:

— MADI(destination_address, source_address, mac_service_data_unit) is equivalent to:
MAC:MA_DATA.indication(destination_address, source_address, mac_service_data_unit, frame_check_sequence, reception_status), as defined in 2.3.2.
— MADR(destination_address, source_address, mac_service_data_unit) is equivalent to:
MAC:MA_DATA.request(destination_address, source_address, mac_service_data_unit, frame_check_sequence), as defined in 2.3.1.

144.1.4.4 MCRS Control interface

The MCRS Control interface is an interface between the MAC Control sublayer and the Multi-Channel Reconciliation Sublayer (see Clause 143). The MCRS Control interface is used to control the timing of envelope transmission over a multi-channel P2MP media.

The MAC Control sublayer and the MCRS communicate via the MCRS_CTRL.indication and MCRS_CTRL.request primitives.

144.1.5 Conventions

See 142.1.1.

144.2 Protocol-independent operation

As depicted in Figure 144–3 and Figure 144–4, the MPMC comprises the following functional blocks:

a) Control Parser. This block is responsible for parsing MAC Control frames, as well as interfacing with Clause 31 entities, and opcode-specific blocks.
b) Control Multiplexer. This block is responsible for selecting the source of the frames to be transmitted.

144.2.1 Control Parser and Control Multiplexer

The Control Parser (see Figure 144–5) is responsible for opcode-independent parsing of MAC frames and forwarding these frames to other processes for opcode-specific operations. The Control Parser also extracts the value of the Timestamp field from all MPCPDUs that contain this field and checks whether the timestamp drift value is within the acceptable range. There are no interfaces connecting the Control Parser to MAC Clients.

The Control Multiplexer (see Figure 144–6) is responsible for forwarding frames received from multiple opcode-specific processes to the underlying MAC sublayer. The Control Multiplexer inserts the timestamp value into all MPCPDUs that carry the Timestamp field. There are no interfaces connecting the Control Multiplexer to MAC Clients.

144.2.1.1 Constants

DRIFT_THOLD
: Type: Integer
Description: This constant holds the maximum amount of drift allowed before a timestamp drift error is declared. Exceeding this drift causes ONU deregistration (either self-deregistration or deregistration by the OLT).
Value: 2 (for the receive channels operating at 25 Gb/s) or 3 (for the receive channels operating at 10 Gb/s)
Unit: EQT

144.2.1.2 Counters

LocalTime
: Type: 32-bit unsigned
Description: This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 390.625 MHz, and is equivalent to one EQT. At the OLT the counter shall track the 25GMII transmit clock, while at the ONU the counter shall track the 25GMII receive clock. For accuracy of the receive clock, see 142.4.4.1. In the ONU, this variable is updated with the received timestamp value by the Control Parser process (see 144.2.1.5).

144.2.1.3 Variables

BEGIN
: See 142.2.5.2

FirstTimestamp[Plid]
: Type: Boolean
Description: This variable indicates whether any MPCPDU with the given Physical Layer ID (PLID) value has been seen before or not. The FirstTimestamp[Plid] variable is initialized to true for any PLID value. After an MPCPDU is received from the MAC instance corresponding to the given PLID, the FirstTimestamp[Plid] is reset to false and does not change for the given PLID anymore.

msdu
: See the definition of mac_service_data_unit in 2.3.1.2.

opcode
: Type: 16-bit unsigned integer
Description: This variable represents the opcode value of the outgoing (in the Control Multiplexer) or incoming (in the Control Parser) MPCPDU.

LatchedTime[]
Type: An array of 32-bit unsigned integers
Description: Each element of this array represents the value of the LocalTime counter (see 144.2.1.2) latched at the moment when the MCRS_ESH.indication(Llid) primitive was generated. The elements of the array are indexed by the Llid values.

Rtt[Plid]
Type: 24-bit unsigned integer
Description: This variable holds the measured round-trip time to the ONU. At the OLT, Rtt[DISC_PLID] is zero. At the ONU, Rtt[PLID] is zero.
Unit: EQT

SupportedOpcodes
Type: list of 16-bit unsigned integers
Description: A list of all supported opcodes (see Table 31A–1).

Timestamp
Type: 32-bit unsigned integer
Description: In the Control Multiplexer state diagram, this variable holds the PLID-specific value of timestamp to be inserted into an outgoing MPCPDU. In the Control Parser state diagram this variable represents the value of the Timestamp field of the received MPCPDU.

TsDelta
Type: 32-bit signed integer
Description: This variable represents the difference between the time that ESH was read from the MCRS EnvRx buffer (i.e., the LatchedTime[Plid]) and the Timestamp value in an MPCPDU that followed that ESH. In the ONU, the TsDelta is used to adjust the LocalTime value, while in the OLT it is used as the measurement of the round-trip time to the ONU that sourced the given MPCPDU.

TimestampOpcodes
Type: list of 16-bit unsigned integers
Description: A list of all MPCPDU opcodes that contain the Timestamp field (see Table 31A–1).

TimestampDrift
Type: Boolean
Description: This variable is used to indicate whether an uncorrectable timestamp drift was detected (when set to true) or not (when set to false). An uncorrectable timestamp drift causes an immediate PLID deregistration (see DeregistrationTrigger in 144.3.7.3, Figure 144–21, and Figure 144–22).

144.2.1.4 Functions

ProcessTimestamp (Plid, TsDelta)
This function takes the PLID and a parameter TsDelta, which represents the difference between the local time and the timestamp value in a received MPCPDU. This function checks whether the timestamp drift has exceeded the predefined device-specific threshold DRIFT_THOLD. In the ONU, this function sets the LocalTime counter based on the value of the received Timestamp field (see 144.3.1.1). In the OLT, this function measures the RTT value when the first timestamped MPCPDU is received on a given PLID link. Note that in the ONU, the RTT value is always zero. The ProcessTimestamp function is defined as follows:

```
ProcessTimestamp( Plid, TsDelta )
{
   if( FirstTimestamp[Plid] )
   {
      // The following line is executed only in the ONU
      LocalTime -= TsDelta;

      // The following line is executed only in the OLT
      Rtt[Plid] = TsDelta;

      TimestampDrift[Plid] = false;
      FirstTimestamp[Plid] = false;
   }
   else
      TimestampDrift[Plid] = abs(TsDelta) > DRIFT_THOLD
}
```

144.2.1.5 Control Parser state diagram

The OLT and ONU shall implement the Control Parser state diagram shown in Figure 144–5.

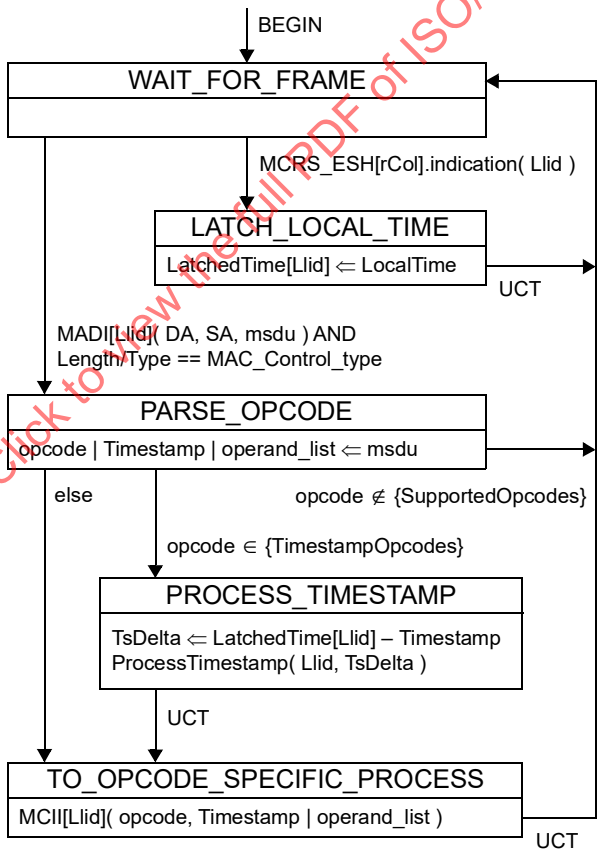


Figure 144–5—Control Parser state diagram

144.2.1.6 Control Multiplexer state diagram

The OLT and ONU shall implement the Control Multiplexer state diagram shown in Figure 144–6.

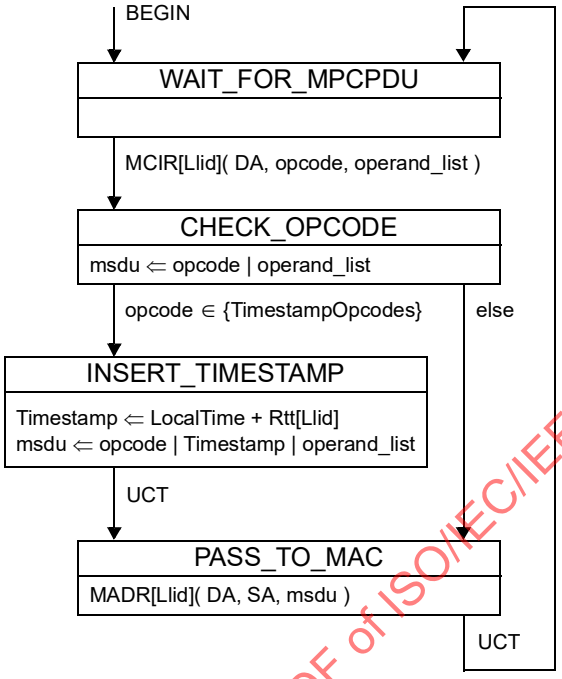


Figure 144–6—Control Multiplexer state diagram

144.3 Multipoint Control Protocol (MPCP)

144.3.1 Principles of Multipoint Control Protocol (MPCP)

In a TDM-based PON, the access to the shared physical medium needs to be arbitrated (see 144.1.1.1). The main purpose of the MPCP described in this subclause is to arbitrate transmissions in Nx25G-EPON. To achieve this goal, the MPCP includes processes that measure the range (i.e., round-trip propagation time) and maintain time synchronization between the OLT and ONUs (see 144.3.1.1) and processes that allow the OLT to assign transmission windows to individual logical links (see 144.3.3).

144.3.1.1 Ranging measurement and time synchronization

Both the OLT and the ONU have 32-bit counters (LocalTime) that increment by one every EQT. In the OLT, the LocalTime counter is synchronized with the OLT 25GMII transmit clock and increments synchronously with InClk (see 143.3.3.4). In the ONU, the LocalTime counter is synchronized with the 25GMII receive clock and increments synchronously with OutClk (see 143.3.3.4). In the ONUs supporting multiple downstream (receive) channels, the LocalTime counter is synchronized with the 25GMII receive clock of the active (enabled) channel with the lowest index.

The LocalTime counters supply the timestamp value for MPCPDUs transmitted by either device. The time reference point for the timestamp value is the transmission time of the envelope start header (ESH) of the envelope that includes the MPCPDU (see 143.3.2). In situations where multiple MPCPDUs are transmitted within a single envelope, all these MPCPDUs shall have the same timestamp value, referencing the transmission time of the ESH.

Note that the actual arrival times of MPCPDUs to the MAC Control sublayer do not affect the timing synchronization mechanism. MPCPDUs may get delayed in the transmitting MAC if, for example, the MAC is paused to allow for the MCRS rate adjustment or FEC parity insertion between the ESH and the MPCPDU.

The ONU ranging (i.e., round-trip propagation time) is measured during the ONU initial discovery and registration. The measured range value also includes the nominal delays of 32 EQT through the ONU MCRS receive data path and 32 EQT through the OLT MCRS receive data path (see 143.4.2).

The method of ranging measurement is illustrated in Figure 144–7. It consists of the following steps:

1) The OLT Discovery process transmits a DISCOVERY MPCPDU with a timestamp value equal to the LocalTime counter at the time when the MCRS_CTRL.request primitive is generated by the Envelope Activation process. This is also the time when the ESH is written into the EnvTx FIFO (see 143.3.1.2.1). Accordingly, the EPAM field of the ESH header matches the six least-significant bits of the LocalTime (LocalTime<5:0>).
2) When an unregistered ONU receives the DISCOVERY MPCPDUs, it sets its LocalTime counter based on the value in the Timestamp field in the received MPCPDU. From this moment, the LocalTime counter continues to increment synchronously with the 25GMII receive clock.
3) After the ONU's LocalTime counter reaches the value of GrantStartTime and an additional random delay, the ONU Registration process transmits the REGISTER_REQ MPCPDU with Timestamp field value equal to the LocalTime counter at the time when the MCRS_CTRL.request primitive is generated by the Envelope Activation process. This is also the time when the ESH is written into the EnvTx FIFO (see 143.3.1.2.1). Accordingly, the EPAM field of the ESH header matches the six least-significant bits of the LocalTime (LocalTime<5:0>).
4) When the OLT receives MPCPDUs, it uses the received Timestamp field value to calculate the round-trip time between the OLT and the ONU. The round-trip time (RTT) is equal to the difference between the OLT's LocalTime counter at the moment when the ESH is read from the MCRS EnvRx buffer and the Timestamp field value in the REGISTER_REQ MPCPDU.

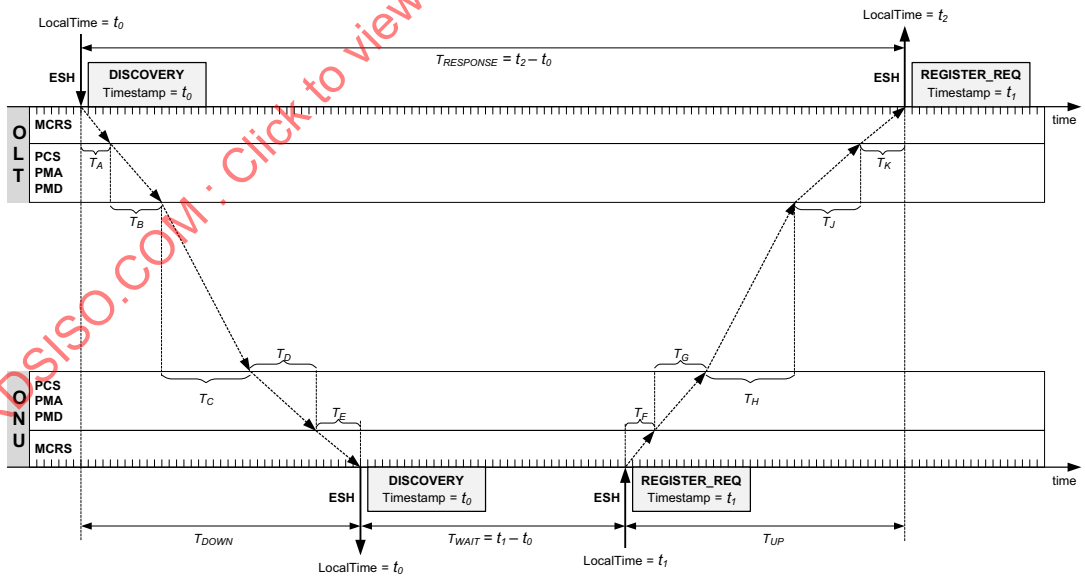


Figure 144–7—Ranging measurement

In the downstream direction, the combined delay T_{DOWN} includes the following delay components:

- T_A – delay through the transmit data path of the OLT MCRS sublayer.
- T_B – delay through the transmit data path of the OLT PCS, PMA, and PMD sublayers. This delay also includes FEC encoding delay.
- T_C – downstream optical signal propagation delay in fiber. In EPON systems supporting multiple downstream channels, this delay may be different on different channels.
- T_D – delay through the receive data path of the ONU PCS, PMA, and PMD sublayers. This delay also includes FEC decoding (correction) delay.
- T_E – delay through the receive data path of the ONU MCRS sublayer. During initial ranging, this delay is equal to 32 EQT (see 143.4.2). After the initial ranging, the delay T_E becomes inversely-correlated with the sum of delays T_A, T_B, T_C, and T_D, such that T_{DOWN} remains nearly-constant with only ± 1 EQT of variability.

In the upstream direction, the combined delay T_{UP} includes the following delay components:

- T_F – Delay through the transmit data path of the ONU MCRS sublayer.
- T_G – Delay through the transmit data path of the ONU PCS, PMA, and PMD sublayers. This delay also includes FEC encoding delay.
- T_H – Upstream optical signal propagation delay in fiber. In EPON systems supporting multiple upstream channels, this delay may be different on different channels.
- T_J – Delay through the receive data path of the OLT PCS, PMA, and PMD sublayers. This delay also includes FEC decoding (correction) delay.
- T_K – Delay through the receive data path of the OLT MCRS sublayer. During initial ranging, this delay is equal to 32 EQT (see 143.4.2). After the initial ranging, the delay T_K becomes inversely-correlated with the sum of delays T_F, T_G, T_H, and T_J, such that T_{UP} remains nearly-constant with only ± 1 EQT of variability.

As was stated above, the RTT value is equal to the difference between t_2 (the OLT's LocalTime counter at the moment when the ESH is received) and t_1 (the Timestamp field value in the REGISTER_REQ MPCPDU). Below is the derivation of this RTT value:

a) From the illustration in Figure 144–7, the total response time $T_{RESPONSE}$ (an interval of time from sending ESH with the DISCOVERY MPCPDU to the ONU and receiving ESH with the REGISTER_REQ MPCPDU from the ONU) is: $T_{RESPONSE} = t_2 - t_0$.
b) On the other hand, $T_{RESPONSE} = T_{DOWN} + T_{WAIT} + T_{UP}$, where $T_{WAIT} = t_1 - t_0$.
c) Thus, $t_2 - t_0 = T_{DOWN} + t_1 - t_0 + T_{UP}$.
d) RTT = $T_{DOWN} + T_{UP} = t_2 - t_1$.

Once the RTT is measured, the GATE Generation process for the new PLID is instantiated. That process is responsible for generating the GATE MPCPDUs to the registered ONU (PLID). All MPCPDUs sent by the OLT on unicast PLIDs have the Timestamp field value pre-compensated by the RTT associated with this PLID:

Timestamp[LLID] = LocalTime + RTT[LLID]

The effect of such pre-compensation is that the first ESH in any burst from an ONU arrives to the OLT MCRS EnvRx buffer approximately 32 EQT before their GrantStartTime values and this ESH is read from the EnvRx buffer into the associated MAC instance at the time when the OLT's LocalTime counter value is equal to GrantStartTime (see Figure 144–8).

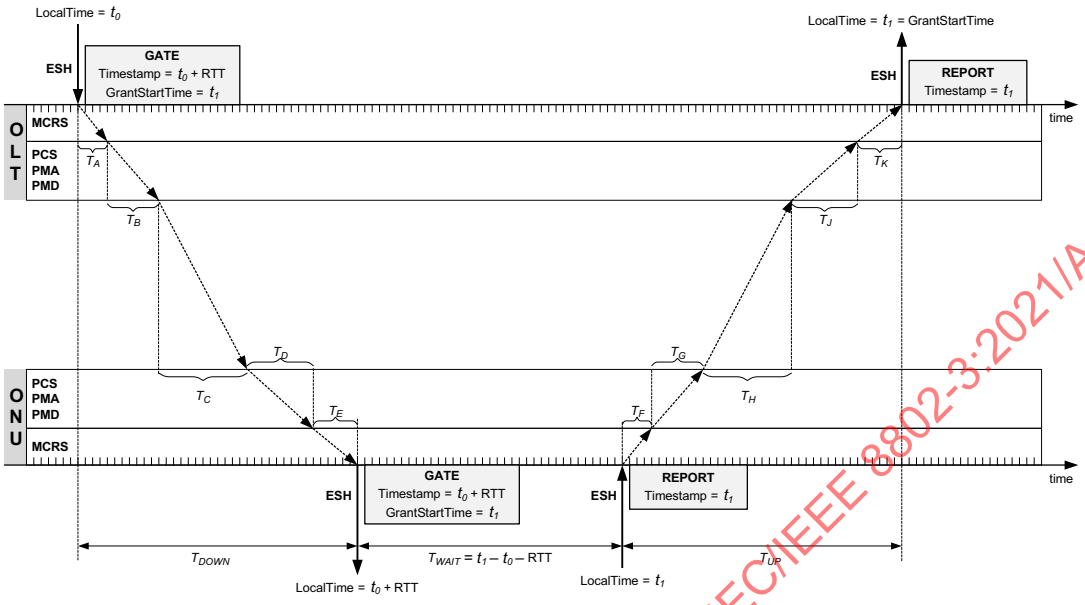


Figure 144–8—Illustration of GrantStartTime alignment

Another effect of the timestamp pre-compensation is that the Timestamp field value in a received MPCPDU is expected to match the LocalTime value at the time the MPCPDU is received. (As stated above, the timestamp reference point is the time the ESH is read from the EnvRx buffer).

A condition of timestamp drift error occurs if the OLT's and ONU's LocalTime counters lose their synchronization or mutual alignment. This condition can be independently detected by the OLT or an ONU. This condition is detected when an absolute difference between the Timestamp value received in an MPCPDU and the LocalTime counter exceeds the timestamp drift threshold limit DRIFT_THOLD (see 144.2.1.4). The timestamp drift error causes an immediate ONU deregistration.

After the ONU receives the REGISTER MPCPDU with its assigned PLID and management link ID (MLID), it stops processing any MPCPDUs received in envelopes with DISC_PLID. At this time, the ONU is ready to accept its first GATE received on the newly-assigned unicast PLID. The timestamp in this GATE MPCPDU is pre-compensated with ONU's RTT, and therefore, the ONU is expected to measure a large difference between the received Timestamp value and its LocalTime counter. This large difference that is detected immediately after registration is expected and the ONU does not recognize it as a timestamp drift error (see ProcessTimestamp in 144.2.1.4).

144.3.1.2 Granting access to the PON media by the OLT

To allow ONUs' access to the PON media, the OLT issues GATE MPCPDUs (see 144.3.6.1). A GATE MPCPDU contains a transmission start time (StartTime field) and transmission allocations (EnvAlloc[i] field) for up to seven LLIDs. The OLT may grant more than seven LLIDs by issuing multiple GATE MPCPDUs with the same StartTime value.

A GATE MPCPDU may be transmitted on any downstream channel and it may allocate upstream transmission windows on any or all upstream channels. An ONU ignores all the transmission allocations for the upstream channels that are not enabled in that ONU.

The ONU processes the GATE MPCPDUs in the order they are received and generates the upstream envelopes following the order of EnvAlloc[i] fields in each GATE MPCPDU. Therefore, it is possible for an LLID to be allocated multiple disjoint envelopes within the same grant.

As is explained in 143.3.1.2.3 and in 144.3.1.1, the value of the Timestamp field in MPCPDUs references the transmission (and reception) time of the ESH preceding these MPCPDUs. For that reason, the OLT shall never allocate overlapping envelopes to the PLID, except the fully-overlapping envelopes (see Figure 143–5).

In the case that the ONU is given partially overlapping PLID envelope allocations, it shall choose only one of these envelopes for MPCPDU transmission, and only if the envelope length is enough for at least one complete MPCPDU. The ONU ignores the rest of the overlapping PLID envelope allocations.

144.3.2 MPCP block diagram

Figure 144–9 illustrates a functional block diagram of the MPCP for the OLT. The MPCP in the OLT includes the following processes:

- GATE Generation process (see 144.3.8.7)
- Discovery Initiation process (see 144.3.7.6)
- Registration Completion process (see 144.3.7.7)
- Envelope Commitment process (see 144.3.8.9)
- Envelope Activation process (see 144.3.8.11)

In the OLT, a separate instance of the GATE Generation process and a separate instance of the Registration Completion process are created for each registered ONU (PLID, see 144.3.4).

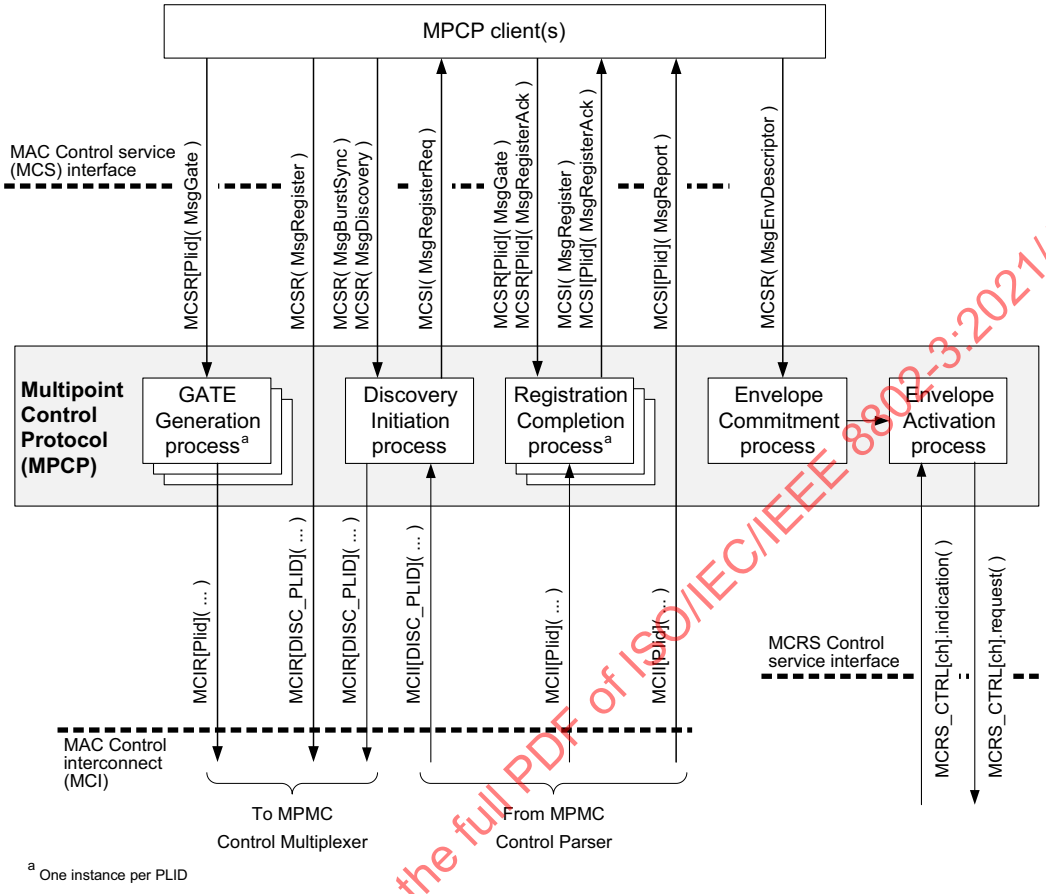


Figure 144–9—OLT Multipoint Control Protocol (MPCP) functional block diagram

Figure 144–10 illustrates a functional block diagram of the MPCP for the ONU. The MPCP in the ONU includes the following processes:

— ONU Registration process (see 144.3.7.8)
— GATE Reception process (see 144.3.8.8)
— Envelope Commitment process (see 144.3.8.10)
— Envelope Activation process (see 144.3.8.11)

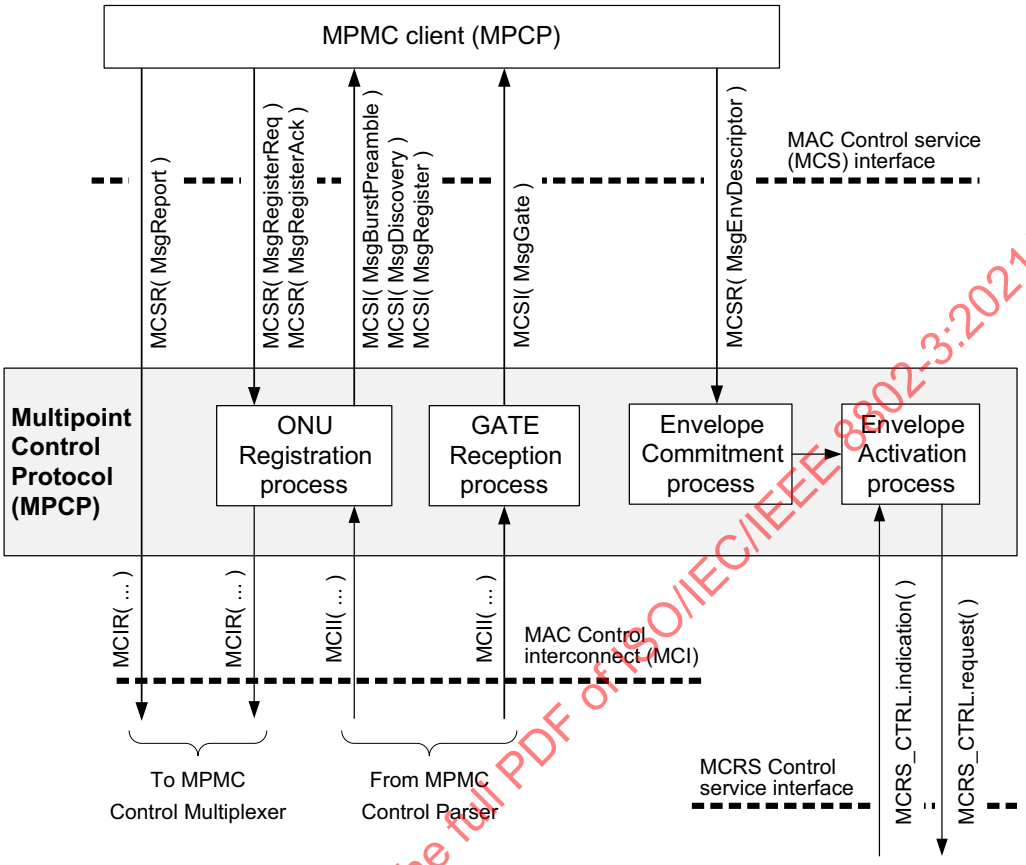


Figure 144–10—ONU Multipoint Control Protocol (MPCP) functional block diagram

144.3.3 Delay variability requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent; however, a complying implementation shall maintain the combined delay variation through the MAC and PHY of less than one EQT for channels operating at 25.78125 GBd and less than two EQTs for channels operating at 10.3125 GBd.

144.3.4 Logical link identifier (LLID) types

144.3.4.1 Physical Layer ID (PLID)

The PLID carries messages used to control critical Nx25G-EPON operations, such as ONU registrations and arbitration of ONUs' access to the PON medium. All Multipoint Control Protocol data units (MPCPDUs) are transported using the PLID. A successful ONU Discovery and Registration process, described in 144.3.7.8, results in the assignment of a single unique PLID value to the ONU.

144.3.4.2 Management link ID (MLID)

The MLID carries management traffic flows, such as OAMPDUs (see 57.4) and CCPDUs (see 144.4). Each ONU is assigned a single unique MLID value as part of the ONU Discovery and Registration process, described in 144.3.7.8.

144.3.4.3 User link ID (ULID)

User link IDs (ULIDs) carry subscriber traffic. It is expected that a single subscriber may be assigned one or more ULIDs to allow for separation of traffic classes and types. ULID values are assigned (provisioned) to an ONU using an appropriate management protocol outside the scope of this standard. ULID values need not have a one-to-one binding of an OLT MAC to an ONU MAC. A ULID that binds a single OLT MAC to multiple MACs in different ONUs represents a multicast ULID.

144.3.4.4 Group link ID (GLID)

To assist in traffic management the Nx25G-EPON system supports consolidation of several LLIDs into arbitrary groups using the group link ID (GLID). For example, all LLIDs for a specific subscriber hosted on an ONU servicing numerous subscribers could be grouped together into a single GLID; in another example all LLIDs supporting a specific traffic class (e.g., best-effort traffic) on a multi-subscriber ONU could be grouped together. GLID values are used only for the purposes of bandwidth granting by the OLT and reporting by the ONU. The GLID report contains the sum of all queue lengths of member LLIDs from that ONU. The bandwidth granted to a GLID is distributed among its member LLIDs. The method by which the granted bandwidth is distributed among the member LLIDs is outside the scope of this standard. The actual envelope transmission is identified by a PLID, an MLID, or a ULID value, associated with a specific MAC instance that sourced the data (i.e., the LLID field in the envelope headers may only contain a PLID, MLID, or ULID, but never a GLID).

144.3.5 Allocation of LLID values

Table 144–1 shows the allocation of LLID values.

Table 144–1—Allocation of LLID values

LLID value	Designation	Description
0x00-00	ESC_LLID	The ESC_LLID is used in the GATE MPCPDU to indicate an empty EnvAlloc[n] field or in the REPORT MPCPDU to indicate an empty LlidStatus field. The ESC_LLID is also used in the MCRS_CTRL.request primitive to mark the end of an upstream burst.
0x00-01	DISC_PLID	PLID value used for discovery of unregistered ONUs.
0x00-02	BCAST_PLID	PLID value reserved for MPCPDU broadcast.
0x00-03	BCAST_MLID	MLID value reserved for broadcast of management frames (OAMPDUs).
0x00-04 to 0x0F-FF	N/A	Reserved.
0x10-00 to 0xFF-FF	N/A	The range of LLID values available for allocation to PLID, MLID, ULID, or GLID. The values may be allocated to form unicast, multicast, or broadcast connections. LLID allocation policy is outside the scope of this standard.

The OLT and the ONUs shall not transmit envelopes with ESC_LLID or a reserved value in the LLID field, and they shall ignore the received envelopes with any of these LLID values.

An unregistered ONU shall accept only the envelopes containing the DISC_PLID value in the LLID field. The envelopes with other LLID values shall be ignored.

Upon successful registration, an ONU shall no longer accept envelopes with DISC_PLID. Instead, a registered ONU shall accept all envelopes containing any of the following LLID values:

- The specific PLID value assigned to this ONU during registration
- The specific MLID value assigned to this ONU during registration
- Broadcast PLID (BCAST_PLID)
- Broadcast MLID (BCAST_MLID)
- Any ULID or GLID assigned to this ONU by management[7]

144.3.6 MPCPDU structure and encoding

The MPCPDU structure is shown in Figure 144–11, and is further defined as follows:

- DestinationAddress:
  In MPCPDUs, the DestinationAddress is the MAC Control Multicast address as specified in the annexes to Clause 31, or the individual MAC address associated with the PLID to which the MPCPDU is destined.

- SourceAddress:
  In MPCPDUs, the SourceAddress is the individual MAC address associated with the PLID through which the MPCPDU is transmitted. For MPCPDUs originating at the OLT, this may be the address of any individual MAC. These MACs may all share a single unicast address, as explained in 144.1.1.2.

- Length/Type:
  In MPCPDUs this field carries the MAC_Control_type field value as specified in 31.4.1.3.

- Opcode:
  This field identifies the specific MPCPDU being encapsulated. Opcode field values are defined in Table 31A–1.

- OperandList:
  A set of opcode-specific fields as defined in 144.3.6.1 through 144.3.6.7.

- Pad:
  This field is present only when the total length of the OperandList is below 44 octets. The Pad field is added to bring the MPCPDU length up to the minimum frame size (see 4A.2.3.2.4). This field is filled with zeros on transmission, and is ignored on reception.

- FCS:
  This is the frame check sequence, typically generated by the MAC.

[7]After registration, an ONU may be configured to use multiple ULID or GLID values via management. The method of provisioning of these additional ULID or GLID values is outside the scope of this standard.

	Octets
DestinationAddress	6
SourceAddress	6
Length/Type = 0x88-08	2
Opcode	2
OperandList	*N*
Pad	44 – *N*
FCS	4

Figure 144–11—Generic MPCPDU

Fields within a frame are transmitted from top to bottom. When consecutive octets are used to represent a single numerical value, the most significant octet is transmitted first, followed by successively less significant octets. Bits within each octet are transmitted from LSB to MSB.

144.3.6.1 GATE description

The purpose of the GATE message is to grant transmission windows to ONUs for upstream transmission on the shared medium. A single grant to an ONU may consist of multiple GATE MPCPDUs, all having the same StartTime value. Up to seven envelope allocations can be carried in a single GATE MPCPDU. Only envelope allocations with a non-zero value for the LLID field are processed by the ONU. A GATE MPCPDU with no EnvAlloc (i.e., all LLID fields equal to zero) is valid and may be used as an MPCP keep alive from the OLT to the ONU.

The GATE MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–12.

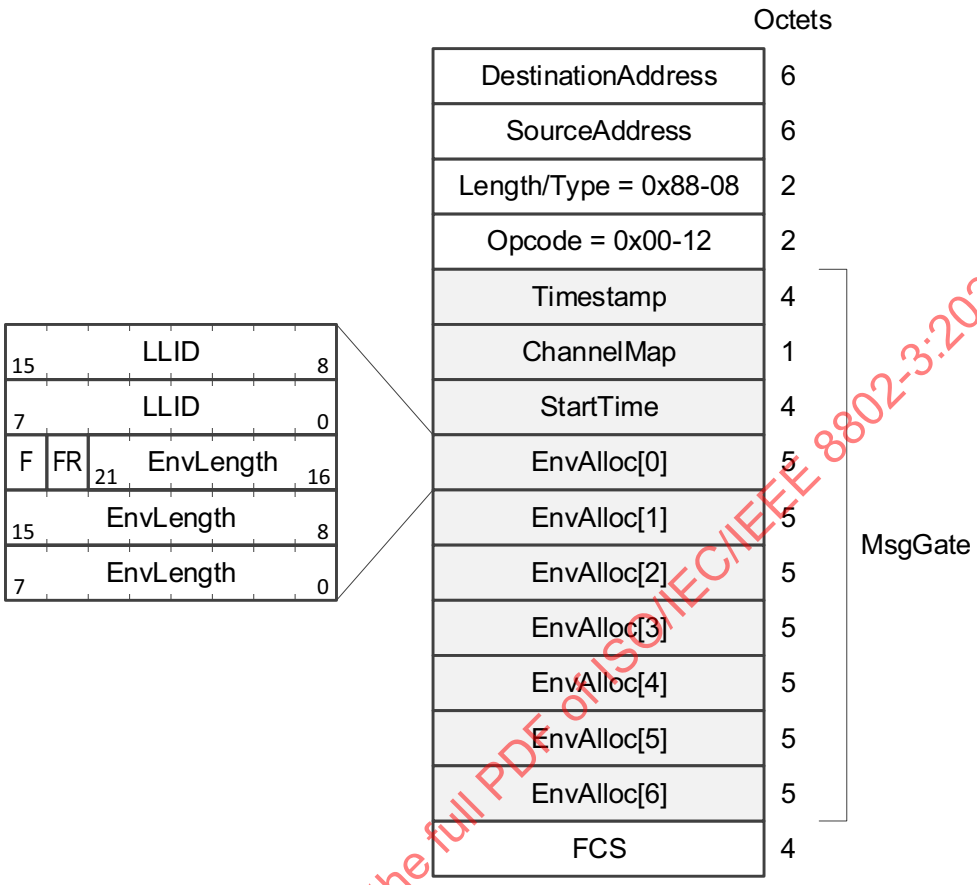


Figure 144–12—GATE MPCPDU

The GATE MPCPDU is identified by the Opcode field value of 0x00-12. The MsgGate structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the OLT's MPCP local time counter (see LocalTime counter in 144.2.1.2) compensated for the RTT of the PLID to which the GATE MPCPDU is sent. This field is used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

ChannelMap:
This 8-bit field identifies the upstream channel(s) granted to the ONU in a given GATE MPCPDU. Table 144–2 shows the mapping between individual bits and upstream channels. When multiple channels are allowed in a single GATE MPCPDU, the transmission on each channel shall start at the ONU's local time equal to the StartTime value and have the length as necessary to transmit all allocated envelopes (the sum of all EnvLength fields) together with the associated optical and FEC overhead.

Table 144–2—ChannelMap bit assignment

Bit	Channel field	Values
0	Upstream channel 0	0 – do not use upstream channel 0 for transmission 1 – use upstream channel 0 for transmission
1	Upstream channel 1	0 – do not use upstream channel 1 for transmission 1 – use upstream channel 1 for transmission
7:2	Reserved	set to 0

— StartTime:
This 32-bit unsigned integer value represents the start time of the transmission window (burst), expressed in the units of EQT. The start time is compared to the LocalTime to correlate the start of the grant.

— EnvAlloc:
This is a 40-bit structure that describes the transmission window assigned to a specific LLID. Up to seven EnvAlloc elements can be carried by a single GATE MPCPDU. The EnvAlloc structure consists of the following sub-fields:

  — LLID:
  This 16-bit unsigned integer value represents the logical link that is being allocated a transmission slot. When this field is set to the value of ESC_LLID (see Table 144–1) then it signifies an empty EnvAlloc structure.

  — EnvLength:
  This 22-bit unsigned value represents the length of the envelope assigned to this specific LLID. The length of the envelope is expressed in units of EQ. The EnvLength represents the number of EQs to be sourced from a corresponding (virtual) MAC, less one EQ reserved for the ESH. The EnvLength does not include any transmission overhead components (FEC overhead or optical burst-mode overhead).

  — Fragmentation (F):
  When set to 1, this flag informs the ONU that it is allowed to fragment new frames transmitted on the given LLID. When this flag set to 0, the ONU shall not fragment new frames. If a frame fragment remains queued in this LLID since the previous envelope transmission, this old fragment is transmitted first, regardless of the value of the Fragmentation flag. The ONU shall not fragment MPCPDU frames, regardless of the value of the Fragmentation flag in the EnvAlloc structure that allocates a PLID envelope.

  — ForceReport (FR):
  When this flag is set to 1, the ONU shall report the total length of the frames (including IPG and preamble), queued for transmission on this specific LLID. When the respective bit is set to 0, the ONU is not required to report the length of the given queue.

144.3.6.2 REPORT description

The purpose of the REPORT message is to report to the OLT the amount of data queued per individual LLID in an ONU. Up to seven LLIDs can be reported by a single REPORT MPCPDU. REPORT MPCPDUs also carry the Timestamp field. The value of this field is used by the OLT to check for the timestamp drift error (see 144.3.1.1).

The REPORT MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–13.

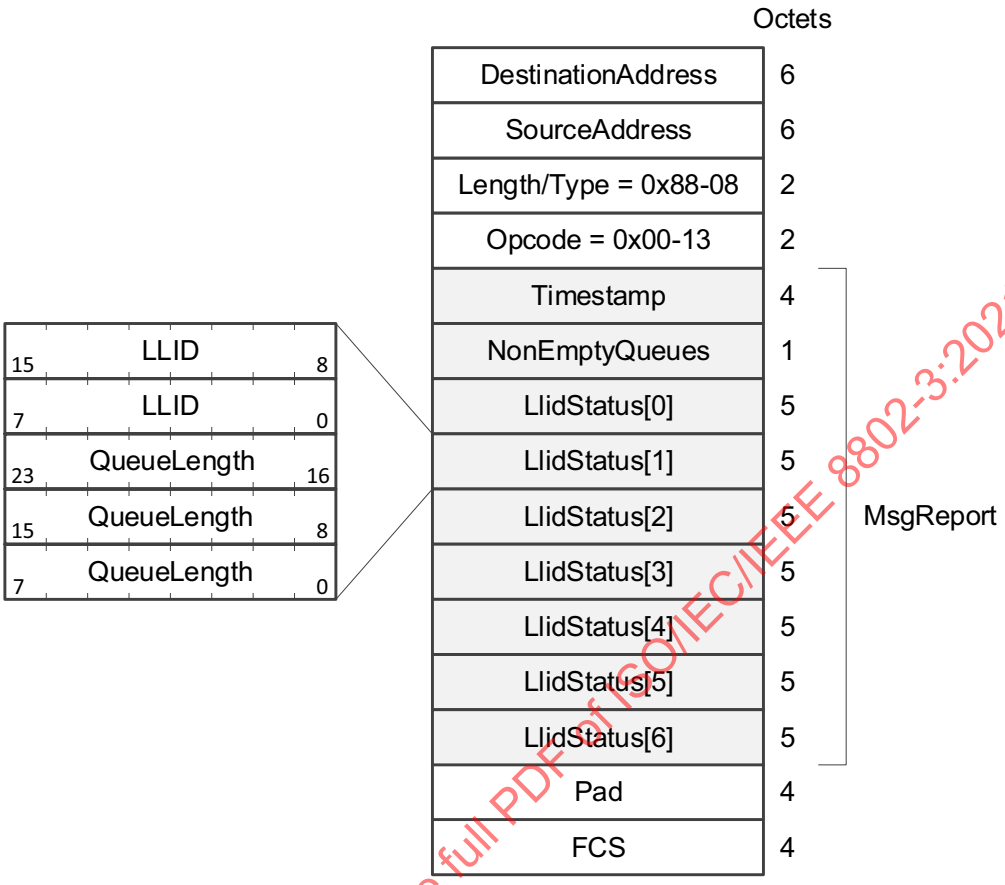


Figure 144–13—REPORT MPCPDU

The REPORT MPCPDU is identified by the Opcode field value of 0x00-13. The MsgReport structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the ONU's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— NonEmptyQueues:
The number of LLIDs in the ONU with queues that were non-empty at the time of the REPORT MPCPDU transmission.

— LlidStatus:
This is a 40-bit structure that describes the occupancy of the queue assigned to a specific LLID. The occupancy reports for up to seven queues may be included into a single REPORT MPCPDU. The LlidStatus structure consists of the following sub-fields:

  — LLID:
  This 16-bit unsigned integer value represents the logical link that is being reported. When this

field is set to the value of ESC_LLID (see Table 144–1) then it signifies an empty LlidStatus structure.

— QueueLength:
This 24-bit value represents the length of the queue assigned to the given logical link (as indicated by the value of LLID sub-field), including the associated framing overhead (IPG and preamble). The QueueLength value is expressed in the units of EQ.

144.3.6.3 REGISTER_REQ description

The purpose of the REGISTER_REQ message is to inform the OLT of an ONU's attempt to register or unregister. When multiple ONUs attempt registration, the REGISTER_REQ MPCPDUs are transmitted in the shared discovery window and may collide. The REGISTER_REQ MPCPDUs are transmitted in envelopes with the LLID equal to DISC_PLID (see 144.3.3). The REGISTER_REQ MPCPDUs carry the Timestamp field. The value of this field is used by the OLT to measure the round-trip time of that ONU (see 144.3.1.1).

The REGISTER_REQ MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–14.

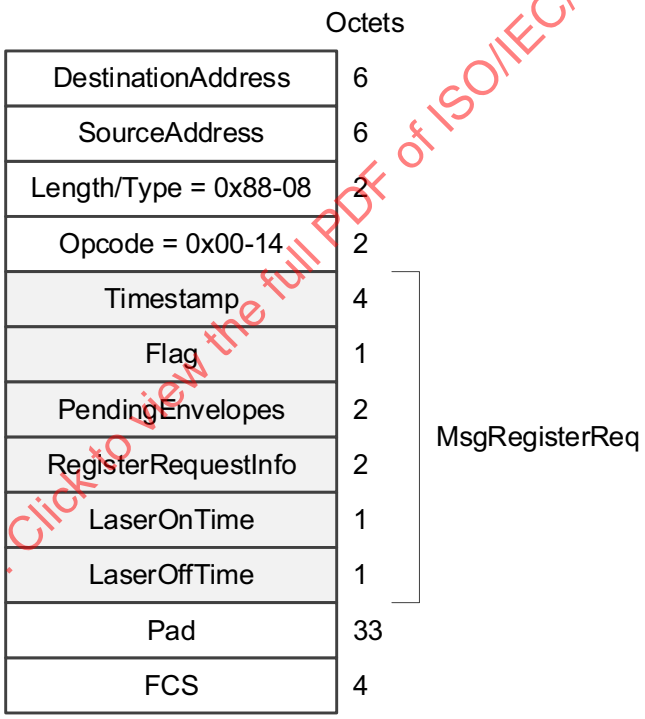


Figure 144–14—REGISTER_REQ MPCPDU

The REGISTER_REQ MPCPDU is identified by the Opcode field value of 0x00-14. The MsgRegisterReq structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the ONU's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— Flag:
This is an 8-bit field that indicates special requirements for the registration, as presented in Table 144–3.

Table 144–3—REGISTER_REQ MPCPDU Flag field

Value	Indication	Comment
0	ACK	ONU is requesting registration by the OLT
1	NACK	ONU is requesting deregistration by the OLT
2 to 255	Reserved	Ignored on reception

— PendingEnvelopes:
This is an unsigned 16-bit value signifying the maximum number of envelope allocations the ONU is capable of buffering. The OLT should not grant the ONU more than this maximum number of envelope allocations into the future.

— RegisterRequestInfo:
This is a 16-bit flag register that informs the OLT about the ONU's supported transmission rate on the channel on which this MPCPDU is transmitted. Table 144–4 presents the structure of the RegisterRequestInfo field.

Table 144–4—RegisterRequestInfo field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	ONU is 10G upstream capable	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
2	ONU is 25G upstream capable	0 – ONU transmitter is not capable of 25 Gb/s 1 – ONU transmitter is capable of 25 Gb/s
4:3	Reserved	Ignored on reception
5	10G registration attempt	0 – 10 Gb/s registration is not attempted 1 – 10 Gb/s registration is attempted
6	25G registration attempt	0 – 25 Gb/s registration is not attempted 1 – 25 Gb/s registration is attempted
15:7	Reserved	Ignored on reception

— LaserOnTime:
This field is one octet long and carries the time required to turn the ONU transmitter on. The value of LaserOnTime is expressed in the units of EQT.

— LaserOffTime:
This field is one octet long and carries the time required to turn the ONU transmitter off. The value of LaserOffTime is expressed in the units of EQT.

144.3.6.4 REGISTER description

The REGISTER message is used to convey to the registering ONU the assigned PLID and MLID values. As the ONU is not yet aware of its assigned PLID value, the REGISTER MPCPDUs are transmitted in envelopes with the LLID equal to DISC_PLID (see 144.3.5); however, they use the ONU's MAC address as the REGISTER MPCPDU DestinationAddress.