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AMENDMENT 3
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Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks —

Part 3: Standard for Ethernet

AMENDMENT 3: Media access control parameters for 50 Gb/s and physical layers and management parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s operation

Télécommunications et échange entre systèmes informatiques — Exigences pour les réseaux locaux et métropolitains —

Partie 3: Norme pour Ethernet

AMENDEMENT 3: Paramètres de commande d'accès media pour 50 Gb/s et couches physiques et paramètres de gestion pour fonctionnement à 50 Gb/s, 100 Gb/s et 200 Gb/s

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IEEE Std 802.3cd™-2018
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018
and IEEE Std 802.3bt™-2018)

IEEE Standard for Ethernet

Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

Sponsor

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 5 December 2018

IEEE-SA Standards Board

Abstract: Clause 131 through Clause 140 and Annex 135A through Annex 136D are added to IEEE Std 802.3-2018 by this amendment to specify IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

Keywords: 50GAUI-1, 50GAUI-2, 50GBASE-CR, 50GBASE-FR, 50GBASE-KR, 50GBASE-LR, 50GBASE-SR, 50 Gigabit Ethernet, 50GMII, 100GAUI-2, 100GAUI-4, 100GBASE-CR2, 100GBASE-DR, 100GBASE-KR2, 100GBASE-SR2, 100 Gigabit Ethernet, 200GBASE-CR4, 200GBASE-KR4, 200GBASE-SR4, 200 Gigabit Ethernet, amendment, EEE, Energy-Efficient Ethernet, Ethernet, FEC, forward error correction, IEEE 802.3™, IEEE 802.3cd™, LAUI-2, MME, SMF

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Introduction

This introduction is not part of IEEE Std 802.3cd-2018, IEEE Standard for Ethernet. Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of publication for IEEE Std 802.3cd-2018, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, Annex 128C, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

A companion document, IEEE Std 802.3.1, describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018 and IEEE Std 802.3bt™-2018.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[1]

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following new compatibility interfaces into 1.1.3.2 after m) "40 Gb/s Parallel Physical Interface (XLPPI)":

m1) *50 Gb/s Media Independent Interface (50GMII).* The 50GMII is designed to connect a 50 Gb/s capable MAC to a 50 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The 50GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 50GMII. The 50GMII is optional.

m2) *50 Gb/s Attachment Unit Interface (LAUI-2/50GAUI-n).* The LAUI-2/50GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The LAUI-2/50GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 50GAUI-n are defined: a two-lane version (50GAUI-2) in Annex 135D and Annex 135E, and a one-lane version (50GAUI-1) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the LAUI-2/50GAUI-n. The LAUI-2/50GAUI-n is optional.

Change the compatibility interface o) "100 Gb/s Attachment Unit Interface (CAUI-n)" in 1.1.3.2 as follows:

o) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n).* The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Three~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, ~~and~~ a four-lane version (CAUI-4/100GAUI-4) in Annex 83D, ~~and~~ Annex 83E, Annex 135D, and Annex 135E, and a two-lane version (100GAUI-2) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

1.3 Normative references

Change the following reference in 1.3 as shown:

IEC 61753-022-2:2012, Fibre optic interconnecting devices and passive components—Performance standard—Part 022-2: Fibre optic connectors terminated on multimode fibre for category C—Controlled environment~~, performance Class M~~.

1.4 Definitions

Insert the following new definition after 1.4.25 "100GBASE-CR10":

1.4.25a 100GBASE-CR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

Insert the following new definition after 1.4.26 "100GBASE-CR4":

1.4.26a 100GBASE-DR: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 140.)

Insert the following new definition after 1.4.28 "100GBASE-KP4":

1.4.28a 100GBASE-KR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.34 "100GBASE-SR10":

1.4.34a 100GBASE-SR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Change 1.4.36 as follows:

1.4.36 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Three~~Two~~ widths ~~of CAUI-n~~ are defined: a ten-lane version (CAUI-10), ~~and a~~two four-lane versions (CAUI-4, 100GAUI-4), and a two-lane version (100GAUI-2). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, ~~or~~ Annex 83D and Annex 83E for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, or Clause 135, Annex 135F, and Annex 135G for 100GAUI-2.)

Insert the following new definition after 1.4.82c "2.5GSEI" as inserted by IEEE Std 802.3cb-2018:

1.4.82d 200GBASE-CR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136)

Insert the following new definition after 1.4.84 "200GBASE-FR4":

1.4.84a 200GBASE-KR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.86 "200GBASE-R":

1.4.86a 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Insert the following new definitions before 1.4.128a "5GBASE-KR" as inserted by IEEE Std 802.3cb-2018:

1.4.128aa 50GBASE-CR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

1.4.128ab 50GBASE-FR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 139.)

1.4.128ac 50GBASE-KR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.128ad 50GBASE-LR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 139.)

1.4.128ae 50GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 50 Gb/s operation. (See IEEE Std 802.3, Clause 131.)

1.4.128af 50GBASE-SR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 138.)

1.4.128ag 50 Gb/s Attachment Unit Interface (50GAUI-n, LAUI-2): A physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs over one lane (50GAUI-1) or two lanes (50GAUI-2, LAUI-2), used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Clause 135 and Annex 135B through Annex 135G.)

1.4.128ah 50 Gb/s Media Independent Interface (50GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 50 Gb/s operation. (See IEEE Std 802.3, Clause 132.)

Insert the following new definition after 1.4.255 "fast wake":

1.4.255a FEC lane (FECL): In 50GBASE-R and 100GBASE-R, the FEC distributes encoded data to multiple logical lanes; these logical lanes are called FEC lanes. One or more FEC lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 135.)

Change 1.4.386 as follows:

1.4.386 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes; these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83, and Clause 120, and Clause 135.)

1.5 Abbreviations

Insert the following new abbreviations into 1.5 in alphanumeric order:

100GAUI	100 Gb/s Attachment Unit Interface
50GAUI	50 Gb/s Attachment Unit Interface
50GMII	50 Gb/s Media Independent Interface
ERL	effective return loss
FECL	FEC Lane
LAUI	50 Gb/s Attachment Unit Interface

4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	**1 Gb/s**	**2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s**	**10 Gb/s**
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap[a]	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

[a]References to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 7 in 4.4.2 as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry into "APPROPRIATE SYNTAX" in 30.3.2.1.2 after the entry for 40GBASE-T:

APPROPRIATE SYNTAX:

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry into "APPROPRIATE SYNTAX" in 30.3.2.1.3 after the entry for 40GBASE-T:

APPROPRIATE SYNTAX:

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph of "BEHAVIOUR DEFINED AS" in 30.3.2.1.5 (as modified by IEEE Std 802.3cb-2018) as follows:

BEHAVIOUR DEFINED AS:

For operation at 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate "Receive Error" on the media independent interface (see Table 46–4 and Table 81–4).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

APPROPRIATE SYNTAX:

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 40GBASE-T:

50GBASE-R	Multi-lane PCS as specified in Clause 133 with PMA as specified in Clause 135 over undefined PMD

50GBASE-CR	50GBASE-R PCS/PMA over shielded copper balanced cable PMD as specified in Clause 136
50GBASE-KR	50GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
50GBASE-SR	50GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 138
50GBASE-FR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-LR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 100GBASE-ER4:

100GBASE-CR2	100GBASE-R PCS/PMA over 2 lane shielded copper balanced cable PMD as specified in Clause 136
100GBASE-KR2	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
100GBASE-SR2	100GBASE-R PCS/PMA over 2 lane multimode fiber PMD as specified in Clause 138
100GBASE-DR	100GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 140

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 200GBASE-LR4:

200GBASE-CR4	200GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 136
200GBASE-KR4	200GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
200GBASE-SR4	200GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 138

Change the last paragraph of "BEHAVIOUR DEFINED AS" in 30.5.1.1.2 (as modified by IEEE Std 802.3cb-2018) as follows:

BEHAVIOUR DEFINED AS:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 2.5GBASE-X, 5GBASE-R, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of "BEHAVIOUR DEFINED AS" in 30.5.1.1.4 as follows:

BEHAVIOUR DEFINED AS:

For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, the enumerations map to value of the link_fault variable (see 81.3.4) within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration "available", the value Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault".

30.5.1.1.11 aBIPErrorCount

Change the text of "APPROPRIATE SYNTAX" and the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.11 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s and 50 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 40/50/100GBASE-R PHYs and 100GBASE-P PHYS, an array of BIP error counters.

30.5.1.1.12 aLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.12 as follows:

BEHAVIOUR DEFINED AS:

For 40/50/100/200/400GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.17 aFECCorrectedBlocks

Change the text of "APPROPRIATE SYNTAX" in 30.5.1.1.17 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.17 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters.

30.5.1.1.18 aFECUncorrectableBlocks

Change the text of "APPROPRIATE SYNTAX" in 30.5.1.1.18 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.18 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters.

30.5.1.1.26 aRSFECBIPErrorCount

Change the text of "APPROPRIATE SYNTAX" and the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.26 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of BIP error counters.

30.5.1.1.27 aRSFECLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.27 as follows:

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.29 aRSFECBypassIndicationAbility

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.29 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC error indication bypass ability ~~(see 91.5.3.3)~~.

30.5.1.1.31 aRSFECBypassIndicationEnable

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.31 as follows:

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function ~~(see 91.5.3.3)~~.

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

APPROPRIATE SYNTAX:

Insert the following new entry into "APPROPRIATE SYNTAX" in 30.6.1.1.5 after the entry for 40GBASE-T:

50GR	50GBASE-CR as specified in Clause 136 or 50GBASE-KR as specified in Clause 137

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.6.1.1.5 after the entry for 100GBASE-KP4:

100GR2	100GBASE-CR2 as specified in Clause 136 or 100GBASE-KR2 as specified in Clause 137
200GR4	200GBASE-CR4 as specified in Clause 136 or 200GBASE-KR4 as specified in Clause 137

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.20	~~Reserved~~ 50G PMA/PMD extended ability	45.2.1.17a
…		
1.25~~, 1.26~~	~~Reserved~~ PMA/PMD extended ability 2	45.2.1.21a
1.26	Reserved	
…		
1.500 through 1.515	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15	45.2.1.129, 45.2.1.130
1.516 through 1.531	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15	45.2.1.131, 45.2.1.132
~~1.532 through 1.699~~ 1.532 through 1.599	Reserved	
1.600	PMA precoder control Tx output	45.2.1.132a
1.601	PMA precoder control Rx input	45.2.1.132b
1.602	PMA precoder control Rx output	45.2.1.132c
1.603	PMA precoder control Tx input	45.2.1.132d
1.604	PMA precoder request flag	45.2.1.132e
1.605	PMA precoder request Rx input status	45.2.1.132f
1.606	PMA precoder request Tx input status	45.2.1.132g
1.607 through 1.649	Reserved	
1.650, 1.651	RS-FEC degraded SER activate threshold	45.2.1.132h
1.652, 1.653	RS-FEC degraded SER deactivate threshold	45.2.1.132i
1.654, 1.655	RS-FEC degraded SER interval	45.2.1.132j
1.656 through 1.699	Reserved	
…		

Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
~~1.1110 through 1.1199~~ 1.1110 through 1.1119	Reserved	
1.1120 through 1.1123	BASE-R PAM4 PMD training LP control, lane 0 through lane 3	45.2.1.135a
1.1124 through 1.1199	Reserved	
…		
~~1.1210 through 1.1299~~ 1.1210 through 1.1219	Reserved	
1.1220 through 1.1223	BASE-R PAM4 PMD training LP status, lane 0 through lane 3	45.2.1.136a
1.1224 through 1.1299	Reserved	
…		
~~1.1310 through 1.1399~~ 1.1310 through 1.1319	Reserved	
1.1320 through 1.1323	BASE-R PAM4 PMD training LD control, lane 0 through lane 3	45.2.1.137a
1.1324 through 1.1399	Reserved	
…		
~~1.1410 through 1.1449~~ 1.1410 through 1.1419	Reserved	
1.1420 through 1.1423	BASE-R PAM4 PMD training LD status, lane 0 through lane 3	45.2.1.138a
1.1424 through 1.1449	Reserved	
…		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the bits 1.0.5:2 row in Table 45–4 as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = ~~Reserved~~ 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6.3).

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

45.2.1.2.3 Fault (1.1.7)

Change the fourth sentence of 45.2.1.2.3 as follows:

For 10/25/40/50/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the bit 1.4.3 row in Table 45–6 as follows (unchanged rows not shown):

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.4.3	~~Reserved~~ 50G capable	~~Value always 0~~ 1 = PMA/PMD is capable of operating at 50 Gb/s 0 = PMA/PMD is not capable of operating at 50 Gb/s	RO
…			

[a]RO = Read only

Insert 45.2.1.4.12a after 45.2.1.4.12:

45.2.1.4.12a 50G capable (1.4.3)

When read as a one, bit 1.4.3 indicates that the PMA/PMD is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 1.4.3 indicates that the PMA/PMD is not able to operate at a data rate of 50 Gb/s.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the description for bits 1.7.6:0 in Table 45–7 as follows (unchanged table rows and bit description lines not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
...			
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 ... 1 0 1 0 0 1 0 = 200GBASE-SR4 PMA/PMD ~~reserved~~ 1 0 1 0 0 0 1 = 200GBASE-CR4 PMA/PMD 1 0 1 0 0 0 0 = 200GBASE-KR4 PMA/PMD ~~1 0 1 0 0 0 x = reserved~~ ~~1 0 0 x x x x = reserved~~ 1 0 0 1 1 x x = reserved 1 0 0 1 0 1 1 = 100GBASE-DR PMA/PMD 1 0 0 1 0 1 0 = 100GBASE-SR2 PMA/PMD 1 0 0 1 0 0 1 = 100GBASE-CR2 PMA/PMD 1 0 0 1 0 0 0 = 100GBASE-KR2 PMA/PMD 1 0 0 0 1 1 x = reserved 1 0 0 0 1 0 1 = reserved 1 0 0 0 1 0 0 = 50GBASE-LR PMA/PMD 1 0 0 0 0 1 1 = 50GBASE-FR PMA/PMD 1 0 0 0 0 1 0 = 50GBASE-SR PMA/PMD 1 0 0 0 0 0 1 = 50GBASE-CR PMA/PMD 1 0 0 0 0 0 0 = 50GBASE-KR PMA/PMD ...	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.6.3 PMA/PMD type selection (1.7.6:0)

Change 45.2.1.6.3 as follows:

The PMA/PMD type of the PMA/PMD shall be selected using bits 6 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in bits 9 and 7 through 0 of the PMA/PMD status 2 register; the PMA/PMD extended ability register; the 40G/100G PMA/PMD extended ability register; the 50G PMA/PMD extended ability register; the 200G PMA/PMD extended ability register; and the 400G PMA/PMD extended ability register. A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert the following rows into Table 45–9 after the 40GBASE-T row:

Table 45–9—Transmit fault description location

PMA/PMD	Description location
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.9
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.9
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	138.5.10
50GBASE-FR, 50GBASE-LR	139.5.8

Insert the following row into Table 45–9 after the 100GBASE-SR4 row:

Table 45–9—Transmit fault description location *(continued)*

PMA/PMD	Description location
100GBASE-DR	140.5.8

45.2.1.7.5 Receive fault (1.8.10)

Insert the following rows into Table 45–10 after the 40GBASE-T row:

Table 45–10—Receive fault description location

PMA/PMD	Description location
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.10
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.10
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	138.5.11
50GBASE-FR, 50GBASE-LR	139.5.9

Insert the following row into Table 45–10 after the 100GBASE-SR4 row:

Table 45–10—Receive fault description location *(continued)*

PMA/PMD	Description location
100GBASE-DR	140.5.9

45.2.1.8 PMD transmit disable register (Register 1.9)

Insert the following rows into Table 45–12 after the 40GBASE-T row:

Table 45–12—Transmit disable description location

PMA/PMD	Description location
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.6
50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	136.8.6
50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4	138.5.7
50GBASE-FR and 50GBASE-LR	139.5.6

Insert the following row into Table 45–12 after the 100GBASE-SR4 row:

Table 45–12—Transmit disable description location *(continued)*

PMA/PMD	Description location
100GBASE-DR	140.5.6

Insert 45.2.1.17a and its subclauses after 45.2.1.17.8:

45.2.1.17a 50G PMA/PMD extended ability (Register 1.20)

The assignment of bits in the 50G PMA/PMD extended ability register is shown in Table 45–20a.

Table 45–20a—50G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.20.15	50G PMA remote loopback ability	1 = 50G PMA has the ability to perform a remote loopback function 0 = 50G PMA does not have the ability to perform a remote loopback function	RO
1.20.14:5	Reserved	Value always 0	RO
1.20.4	50GBASE-LR ability	1 = PMA/PMD is able to perform 50GBASE-LR 0 = PMA/PMD is not able to perform 50GBASE-LR	RO
1.20.3	50GBASE-FR ability	1 = PMA/PMD is able to perform 50GBASE-FR 0 = PMA/PMD is not able to perform 50GBASE-FR	RO
1.20.2	50GBASE-SR ability	1 = PMA/PMD is able to perform 50GBASE-SR 0 = PMA/PMD is not able to perform 50GBASE-SR	RO
1.20.1	50GBASE-CR ability	1 = PMA/PMD is able to perform 50GBASE-CR 0 = PMA/PMD is not able to perform 50GBASE-CR	RO
1.20.0	50GBASE-KR ability	1 = PMA/PMD is able to perform 50GBASE-KR 0 = PMA/PMD is not able to perform 50GBASE-KR	RO

[a]RO = Read only

45.2.1.17a.1 50G PMA remote loopback ability (1.20.15)

When read as a one, bit 1.20.15 indicates that the 50G PMA is able to perform the remote loopback function. When read as a zero, bit 1.20.15 indicates that the 50G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.17a.2 50GBASE-LR ability (1.20.4)

When read as a one, bit 1.20.4 indicates that the PMA/PMD is able to operate as a 50GBASE-LR PMA/PMD type. When read as a zero, bit 1.20.4 indicates that the PMA/PMD is not able to operate as a 50GBASE-LR PMA/PMD type.

45.2.1.17a.3 50GBASE-FR ability (1.20.3)

When read as a one, bit 1.20.3 indicates that the PMA/PMD is able to operate as a 50GBASE-FR PMA/PMD type. When read as a zero, bit 1.20.3 indicates that the PMA/PMD is not able to operate as a 50GBASE-FR PMA/PMD type.

45.2.1.17a.4 50GBASE-SR ability (1.20.2)

When read as a one, bit 1.20.2 indicates that the PMA/PMD is able to operate as a 50GBASE-SR PMA/PMD type. When read as a zero, bit 1.20.2 indicates that the PMA/PMD is not able to operate as a 50GBASE-SR PMA/PMD type.

45.2.1.17a.5 50GBASE-CR ability (1.20.1)

When read as a one, bit 1.20.1 indicates that the PMA/PMD is able to operate as a 50GBASE-CR PMA/PMD type. When read as a zero, bit 1.20.1 indicates that the PMA/PMD is not able to operate as a 50GBASE-CR PMA/PMD type.

45.2.1.17a.6 50GBASE-KR ability (1.20.0)

When read as a one, bit 1.20.0 indicates that the PMA/PMD is able to operate as a 50GBASE-KR PMA/PMD type. When read as a zero, bit 1.20.0 indicates that the PMA/PMD is not able to operate as a 50GBASE-KR PMA/PMD type.

Insert 45.2.1.21a and 45.2.1.21a.1 after 45.2.1.21.5:

45.2.1.21a PMA/PMD extended ability 2 (Register 1.25)

The assignment of bits in the PMA/PMD extended ability 2 register is shown in Table 45–24a.

Table 45–24a—PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.25.15:1	Reserved	Value always 0	RO
1.25.0	50G extended abilities	1 = PMA/PMD has 50G extended abilities listed in register 1.20 0 = PMA/PMD does not have 50G extended abilities	RO

[a]RO = Read only

45.2.1.21a.1 50G extended abilities (1.25.0)

When read as a one, bit 1.25.0 indicates that the PMA/PMD has 50G extended abilities listed in register 1.20. When read as a zero, bit 1.25.0 indicates that the PMA/PMD does not have 50G extended abilities.

45.2.1.89 BASE-R PMD control register (Register 1.150)

Change the first sentence of 45.2.1.89 as follows:

The BASE-R PMD control register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, ~~or~~ Clause 111, Clause 136, or Clause 137.

45.2.1.90 BASE-R PMD status register (Register 1.151)

Change the first sentence of 45.2.1.90 as follows:

The BASE-R PMD status register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, ~~or~~ Clause 111, Clause 136, or Clause 137.

Change 45.2.1.90.1 through 45.2.1.90.4 as follows:

45.2.1.90.1 Receiver status 0 (1.151.0)

This bit maps to the state variable rx_trained as defined in 72.6.10.3.1 and local_trained in 136.8.11.7.1.

45.2.1.90.2 Frame lock 0 (1.151.1)

This bit maps to the state variable frame_lock as defined in 72.6.10.3.1 and local_tf_lock in 136.8.11.7.1.

45.2.1.90.3 Start-up protocol status 0 (1.151.2)

This bit maps to the state variable training as defined in 72.6.10.3.1 and 136.8.11.7.1.

45.2.1.90.4 Training failure 0 (1.151.3)

This bit maps to the state variable training_failure as defined in 72.6.10.3.1 and 136.8.11.7.1.

45.2.1.110 RS-FEC control register (Register 1.200)

Change Table 45–88 as follows:

Table 45–88—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.200.15:5 ~~1.200.15:3~~	Reserved	Value always 0	RO
1.200.4	FEC degraded SER enable	1 = FEC decoder indicates degraded SER 0 = FEC decoder does not indicate degraded SER	R/W
1.200.3	Four lane PMD indication	1 = FEC is not being used with a four-lane PMD (the four_lane_pmd variable defined in 91.6.2a is set to zero) 0 = FEC is being used with a four-lane PMD (the four_lane_pmd variable defined in 91.6.2a is set to one)	R/W
1.200.2	25G RS-FEC Enable	1 = The 25GBASE-R Reed-Solomon FEC is enabled 0 = The 25GBASE-R Reed-Solomon FEC is disabled	R/W
1.200.1	FEC bypass indication enable	1 = FEC decoder does not indicate errors to the PCS 0 = FEC decoder indicates errors to the PCS layer	R/W
1.200.0	FEC bypass correction enable	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.110.a and 45.2.1.110.b before 45.2.1.110.1:

45.2.1.110.a FEC degraded SER enable (1.200.4)

This bit enables the RS-FEC decoder to indicate the presence of a degraded SER (see 91.5.3.3.1 and 134.5.3.3.2). When set to a one, this bit enables degraded SER detection. When set to a zero, degraded SER detection is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER.

45.2.1.110.b Four-lane PMD (1.200.3)

This bit enables the alignment marker mapping function in the RS-FEC to substitute the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this bit is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of this bit is zero.

45.2.1.110.2 FEC bypass indication enable (1.200.1)

Change 45.2.1.110.2 as follows:

This bit enables the RS-FEC decoder to bypass error indication to the upper layers (PCS) through the sync bits for the BASE-R PHY in the Local Device. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the PCS through the sync bits. Writes to this bit are ignored and reads return a zero if the RS-FEC does not have the ability to bypass indicating decoding errors to the PCS layer (see 91.5.3.3, ~~and~~ 108.5.3.2, and 134.5.3.3.1).

45.2.1.111 RS-FEC status register (Register 1.201)

Change Table 45–89 as follows (unchanged rows not shown):

Table 45–89—RS-FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
...			
~~1.201.6:3~~ 1.201.6:5	Reserved	Value always 0	RO
1.201.4	FEC degraded SER	1 = SER is degraded 0 = SER is not degraded	RO
1.201.3	FEC degraded SER ability	1 = RS-FEC decoder has the ability to indicate the presence of a degraded SER 0 = RS-FEC decoder does not have the ability to indicate the presence of a degraded SER	RO
...			

[a]RO = Read only, LH = Latching high

Change 45.2.1.111.1 and 45.2.1.111.2 as follows:

45.2.1.111.1 PCS align status (1.201.15)

Bit 1.201.15 indicates the PCS alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PCS alignment is defined as block lock, alignment marker lock, and deskew of all 20 transmit PCS lanes. For the RS-FEC described in Clause 108, PCS alignment is defined as block lock of the transmit PCS signal. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not obtained PCS alignment. When read as a one, bit 1.201.15 indicates that the RS-FEC has obtained PCS alignment.

45.2.1.111.2 RS-FEC align status (1.201.14)

Bit 1.201.14 indicates the PMA alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PMA alignment is defined as alignment marker lock and deskew of all four lanes on the PMA service interface. For the RS-FEC described in Clause 108, PMA alignment is defined as codeword marker lock on the PMA service interface. When read as a zero, bit 1.201.14 indicates that the RS-FEC has not obtained PMA alignment. When read as a one, bit 1.201.14 indicates that the RS-FEC has obtained PMA alignment.

Change 45.2.1.111.5 and 45.2.1.111.6 as follows:

45.2.1.111.5 FEC AM lock 1 (1.201.9)

When read as a one, bit 1.201.9 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 1 of the PMA service interface. When read as a zero, bit 1.201.9 indicates that the RS-FEC has not locked and aligned lane 1 of the PMA service interface. This bit reflects the state of amps_lock[1] (see 91.5.3.1).

45.2.1.111.6 FEC AM lock 0 (1.201.8)

When read as a one, bit 1.201.8 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 0 of the PMA service interface. When read as a zero, bit 1.201.8 indicates that the RS-FEC has not locked and aligned lane 0 of the PMA service interface. This bit reflects the state of amps_lock[0] (see 91.5.3.1).

Insert 45.2.1.111.7a and 45.2.1.111.7b after 45.2.1.111.7:

45.2.1.111.7a FEC degraded SER (1.201.4)

This bit (1.201.4) reflects the state of the variable FEC_degraded_SER (see 91.6.5b and 134.6.9). When read as a one, bit 1.201.4 indicates the presence of a degraded received signal.

45.2.1.111.7b FEC degraded SER ability (1.201.3)

This bit is set to one to indicate that the decoder has the ability to indicate the presence of a degraded SER (see 91.5.3.3.1 and 134.5.3.3.2). This bit is set to zero if this ability is not supported.

Change 45.2.1.111.8 and 45.2.1.111.9 as follows:

45.2.1.111.8 RS-FEC high SER (1.201.2)

When FEC_bypass_indication_enable is set to one, bit 1.201.2 is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 91.5.3.3, ~~and~~ 108.5.3.2, and 134.5.3.3.1) and is set to zero otherwise. The bit is set to zero if FEC_bypass_indication_enable is set to zero. This bit shall be implemented with latching high behavior.

45.2.1.111.9 FEC bypass indication ability (1.201.1)

The Reed-Solomon decoder may have the option to perform error detection without error indication (see 91.5.3.3, ~~and~~ 108.5.3.2, and 134.5.3.3.1) to reduce the delay contributed by the RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

45.2.1.117 RS-FEC BIP error counter lane 0 (Register 1.230)

Change the second sentence of 45.2.1.117 as follows:

The RS-FEC described in Clause 91 or Clause 134 calculates a BIP value for each PCS lane (see 91.5.2.4, 91.6.3).

Change 45.2.1.129 to 45.2.1.132 as follows:

45.2.1.129 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–101. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

Table 45–101—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.500.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.500.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.500.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.500.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W

Table 45–101—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.500.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.129.1 Request flag (1.500.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.129.2 Post-cursor request (1.500.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.129.3 Pre-cursor request (1.500.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.129.4 Post-cursor remote setting (1.500.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and

120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.129.5 Pre-cursor remote setting (1.500.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(–1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.129.6 Post-cursor local setting (1.500.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.2 and 120D.3.2.3), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.129.7 Pre-cursor local setting (1.500.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization pre-cursor coefficient c(–1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.130 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers are defined similarly to register 1.500 (which is used for lane 0, see 45.2.1.129) but for lanes 1 through 15, respectively. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

45.2.1.131 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–102. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

Table 45–102—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.516.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.516.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.516.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.516.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W
1.516.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio–0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.131.1 Request flag (1.516.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.131.2 Post-cursor request (1.516.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.131.3 Pre-cursor request (1.516.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.131.4 Post-cursor remote setting (1.516.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.131.5 Pre-cursor remote setting (1.516.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(–1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.131.6 Post-cursor local setting (1.516.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n,

or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.131.7 Pre-cursor local setting (1.516.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.2), which controls the weight of the transmitter equalization pre-cursor coefficient c(–1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.132 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers are defined similarly to register 1.516 (which is used for lane 0, see 45.2.1.131) but for lanes 1 through 15, respectively. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

Insert 45.2.1.132a to 45.2.1.132j after 45.2.1.132:

45.2.1.132a PMA precoder control Tx output (Register 1.600)

The assignment of bits in the PMA precoder control Tx output register is shown in Table 45–102a.

Table 45–102a—PMA precoder control Tx output register bit definitions

Bit(s)	Name	Description	R/W[a]
1.600.15:4	Reserved	Value always 0	RO
1.600.3	Lane 3 Tx output precoder enable	1 = Lane 3 Tx output precoder enabled 0 = Lane 3 Tx output precoder disabled	R/W
1.600.2	Lane 2 Tx output precoder enable	1 = Lane 2 Tx output precoder enabled 0 = Lane 2 Tx output precoder disabled	R/W
1.600.1	Lane 1 Tx output precoder enable	1 = Lane 1 Tx output precoder enabled 0 = Lane 1 Tx output precoder disabled	R/W
1.600.0	Lane 0 Tx output precoder enable	1 = Lane 0 Tx output precoder enabled 0 = Lane 0 Tx output precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.132a.1 Lane 3 Tx output precoder enable (1.600.3)

This bit enables the lane 3 Tx output precoder.

45.2.1.132a.2 Lane 2 Tx output precoder enable (1.600.2)

This bit enables the lane 2 Tx output precoder.

45.2.1.132a.3 Lane 1 Tx output precoder enable (1.600.1)

This bit enables the lane 1 Tx output precoder.

45.2.1.132a.4 Lane 0 Tx output precoder enable (1.600.0)

This bit enables the lane 0 Tx output precoder.

45.2.1.132b PMA precoder control Rx input (Register 1.601)

The assignment of bits in the precoder control Rx input register is shown in Table 45–102b.

Table 45–102b—PMA precoder control Rx input register bit definitions

Bit(s)	Name	Description	R/W[a]
1.601.15:4	Reserved	Value always 0	RO
1.601.3	Lane 3 Rx input precoder enable	1 = Lane 3 Rx input precoder enabled 0 = Lane 3 Rx input precoder disabled	R/W
1.601.2	Lane 2 Rx input precoder enable	1 = Lane 2 Rx input precoder enabled 0 = Lane 2 Rx input precoder disabled	R/W
1.601.1	Lane 1 Rx input precoder enable	1 = Lane 1 Rx input precoder enabled 0 = Lane 1 Rx input precoder disabled	R/W
1.601.0	Lane 0 Rx input precoder enable	1 = Lane 0 Rx input precoder enabled 0 = Lane 0 Rx input precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.132b.1 Lane 3 Rx input precoder enable (1.601.3)

This bit enables the lane 3 Rx input precoder.

45.2.1.132b.2 Lane 2 Rx input precoder enable (1.601.2)

This bit enables the lane 2 Rx input precoder.

45.2.1.132b.3 Lane 1 Rx input precoder enable (1.601.1)

This bit enables the lane 1 Rx input precoder.

45.2.1.132b.4 Lane 0 Rx input precoder enable (1.601.0)

This bit enables the lane 0 Rx input precoder.

45.2.1.132c PMA precoder control Rx output (Register 1.602)

The assignment of bits in the precoder control Rx output register is shown in Table 45–102c.

Table 45–102c—PMA precoder control Rx output register bit definitions

Bit(s)	Name	Description	R/W[a]
1.602.15:2	Reserved	Value always 0	RO
1.602.1	Lane 1 Rx output precoder enable	1 = Lane 1 Rx output precoder enabled 0 = Lane 1 Rx output precoder disabled	R/W
1.602.0	Lane 0 Rx output precoder enable	1 = Lane 0 Rx output precoder enabled 0 = Lane 0 Rx output precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.132c.1 Lane 1 Rx output precoder enable (1.602.1)

This bit enables the lane 1 Rx output precoder.

45.2.1.132c.2 Lane 0 Rx output precoder enable (1.602.0)

This bit enables the lane 0 Rx output precoder.

45.2.1.132d PMA precoder control Tx input (Register 1.603)

The assignment of bits in the precoder control Tx input register is shown in Table 45–102d.

Table 45–102d—PMA precoder control Tx input register bit definitions

Bit(s)	Name	Description	R/W[a]
1.603.15:2	Reserved	Value always 0	RO
1.603.1	Lane 1 Tx input precoder enable	1 = Lane 1 Tx input precoder enabled 0 = Lane 1 Tx input precoder disabled	R/W
1.603.0	Lane 0 Tx input precoder enable	1 = Lane 0 Tx input precoder enabled 0 = Lane 0 Tx input precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.132d.1 Lane 1 Tx input precoder enable (1.603.1)

This bit enables the lane 1 Tx input precoder.

45.2.1.132d.2 Lane 0 Tx input precoder enable (1.603.0)

This bit enables the lane 0 Tx input precoder.

45.2.1.132e PMA precoder request flag (Register 1.604)

The assignment of bits in the precoder request flag register is shown in Table 45–102e.

Table 45–102e—PMA precoder request flag register bit definitions

Bit(s)	Name	Description	R/W[a]
1.604.15:2	Reserved	Value always 0	RO
1.604.1	Tx input precoder request flag	1 = Tx input precoding change requested 0 = Tx input precoding no change requested	RO
1.604.0	Rx input precoder request flag	1 = Rx input precoding change requested 0 = Rx input precoding no change requested	RO

[a]RO = Read only

45.2.1.132e.1 Tx input precoder request flag (1.604.1)

This bit indicates the Tx input precoder request flag.

45.2.1.132e.2 Rx input precoder request flag (1.604.0)

This bit indicates the Rx input precoder request flag.

45.2.1.132f PMA precoder request Rx input status (Register 1.605)

The assignment of bits in the precoder request Rx input status register is shown in Table 45–102f.

Table 45–102f—PMA precoder request Rx input status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.605.15:2	Reserved	Value always 0	RO
1.605.1	Lane 1 Rx input precoder request status	1 = Lane 1 precoder Rx input requested 0 = Lane 1 precoder Rx input not requested	RO
1.605.0	Lane 0 Rx input precoder request status	1 = Lane 0 precoder Rx input requested 0 = Lane 0 precoder Rx input not requested	RO

[a]RO = Read only

45.2.1.132f.1 Lane 1 Rx input precoder request status (1.605.1)

This bit indicates the Rx input precoder request status for lane 1.

45.2.1.132f.2 Lane 0 Rx input precoder request status (1.605.0)

This bit indicates the Rx input precoder request status for lane 0.

45.2.1.132g PMA precoder request Tx input status (Register 1.606)

The assignment of bits in the precoder request Tx input status register is shown in Table 45–102g.

Table 45–102g—PMA precoder request Tx input status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.606.15:2	Reserved	Value always 0	RO
1.606.1	Lane 1 Tx input precoder request status	1 = Lane 1 precoder Tx input requested 0 = Lane 1 precoder Tx input not requested	RO
1.606.0	Lane 0 Tx input precoder request status	1 = Lane 0 precoder Tx input requested 0 = Lane 0 precoder Tx input not requested	RO

[a]RO = Read only

45.2.1.132g.1 Lane 1 Tx input precoder request status(1.606.1)

This bit indicates the Tx input precoder request status for lane 1.

45.2.1.132g.2 Lane 0 Tx input precoder request status (1.606.0)

This bit indicates the Tx input precoder request status for lane 0.

45.2.1.132h RS-FEC degraded SER activate threshold register (Register 1.650, 1.651)

The assignment of bits in the RS-FEC degraded SER activate threshold register is shown in Table 45–102h. The value controls the threshold used to set the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1 and 134.5.3.3.2.

Table 45–102h—RS-FEC degraded SER activate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
1.650.15:0	FEC degraded SER activate threshold lower	FEC_degraded_SER_activate_threshold[15:0]	R/W
1.651.15:0	FEC degraded SER activate threshold upper	FEC_degraded_SER_activate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.1.132i RS-FEC degraded SER deactivate threshold register (Register 1.652, 1.653)

The assignment of bits in the RS-FEC degraded SER deactivate threshold register is shown in Table 45–102i. The value controls the threshold used to clear the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1 and 134.5.3.3.2.

Table 45–102i—RS-FEC degraded SER deactivate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
1.652.15:0	FEC degraded SER deactivate threshold lower	FEC_degraded_SER_deactivate_threshold[15:0]	R/W
1.653.15:0	FEC degraded SER deactivate threshold upper	FEC_degraded_SER_deactivate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.1.132j RS-FEC degraded SER interval register (Register 1.654, 1.655)

The assignment of bits in the RS-FEC degraded SER interval register is shown in Table 45–102j. The value controls the interval used to set and clear the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1 and 134.5.3.3.2.

Table 45–102j—RS-FEC degraded SER interval register bit definitions

Bit(s)	Name	Description	R/W[a]
1.654.15:0	FEC degraded SER interval lower	FEC_degraded_SER_interval[15:0]	R/W
1.655.15:0	FEC degraded SER interval upper	FEC_degraded_SER_interval[31:16]	R/W

[a]R/W = Read/Write

Insert 45.2.1.135a after 45.2.1.135:

45.2.1.135a BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers (Register 1.1120 through 1.1123)

The BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers reflect the contents of the first 16-bit word of the training frame most recently received for each lane. Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45-103a. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0. When training is not disabled, the bits in registers 1.1120 through 1.1123 are read only; however, when training is disabled the R/W bits become writeable.

Table 45–103a—BASE-R PAM4 PMD training LP control, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1120.15:14	Reserved	Value always 0	RO
1.1120.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	R/W
1.1120.11:10	Reserved	Value always 0	RO
1.1120.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	R/W
1.1120.7:5	Reserved	Value always 0	RO
1.1120.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	R/W
1.1120.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.136a after 45.2.1.136:

45.2.1.136a BASE-R PAM4 PMD training LP status, lane 0 through lane 3 registers (Register 1.1220 through 1.1223)

The BASE-R PAM4 PMD training LP status, lane 0 through lane 3 registers reflect the contents of the second 16-bit word of the training frame most recently received for each lane. Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223.

The assignment of bits in the BASE-R PAM4 PMD training LP status, lane 0 register is shown in Table 45–103b. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

Table 45–103b—BASE-R PAM4 PMD training LP status, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1220.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1220.14:12	Reserved	Value always 0	RO
1.1220.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1220.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1220.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1220.7	Parity	Even parity bit	RO
1.1220.6	Reserved	Value always 0	RO
1.1220.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1220.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]RO = Read only

Insert 45.2.1.137a after 45.2.1.137:

45.2.1.137a BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers (Register 1.1320 through 1.1323)

The BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers reflect the contents of the control field of the outgoing training frame for each lane. Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323.

The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45-103c. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

Table 45–103c—BASE-R PAM4 PMD training LD control, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1320.15:41	Reserved	Value always 0	RO
1.1320.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	R/W
1.1320.11:10	Reserved	Value always 0	RO
1.1320.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	R/W
1.1320.7:5	Reserved	Value always 0	RO
1.1320.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	R/W
1.1320.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	R/W

[a]R/W = Read/Write, RO = Read only

Insert 45.2.1.138a after 45.2.1.138 as follows:

45.2.1.138a BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers (Register 1.1420 through 1.1423)

The BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers reflect the contents of the status field of the outgoing training frame for each lane. Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423.

The assignment of bits in the BASE-R PAM4 PMD training LD status, lane 0 register is shown in Table 45–103d. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

Table 45–103d—BASE-R PAM4 PMD training LD status, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1420.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1420.14:12	Reserved	Value always 0	RO
1.1420.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1420.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1420.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1420.7	Parity	Even parity bit	RO
1.1420.6	Reserved	Value always 0	RO
1.1420.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1420.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]RO = Read only

45.2.1.139 PMD training pattern lanes 0 through 3 (Register 1.1450 through 1.1453)

Change Table 45–104 as follows:

Table 45–104—PMD training pattern lane 0 bit definitions

Bit(s)	Name	Description	R/W[a]
1.1450.15:14	Seed	Two most significant bits of PRBS13 seed	R/W
1.1450.~~15:~~13	Reserved	Value always 0	RO
1.1450.12:11	Polynomial identifier	Identifier (0, 1, 2, or 3) selecting polynomial for PRBS	R/W
1.1450.10:0	Seed	11 bit, binary seed for sequence	R/W

[a]R/W = Read/Write, RO = Read only

Change second paragraph of 45.2.1.139 by breaking it in two and changing text as follows:

Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training in the particular PMD lane according to the definition in 92.7.12. The polynomial identifier for each lane should be unique; two lanes having the same identifier could impair operation of the PMD control function. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11.

For PHYs that use a PRBS11 training pattern, register ~~Register~~ bits 10:0 contain the 11-bit seed for the sequence, where register bit 0 gives seed bit S0; register bit 1 gives seed bit S1; etc., through register bit 10 gives seed bit S10. The default seeds are (binary, S0 is left-most bit): for lane 0, 10101111110; for lane 1, 11001000101; for lane 2, 11100101101; for lane 3, 11110110110. This produces the following initial output (hexadecimal representation where the hex symbols are transmitted from left to right and the most significant bit of each hex symbol is transmitted first): for lane 0, 0xfbf1cb3e; for lane 1, 0xfbb1e665; for lane 2, 0xf3fdae46; for lane 3, 0xf2ffa46b.

Insert the following paragraph at end of 45.2.1.139:

For PHYs that use a PRBS13 training pattern, the 13-bit seed value is composed from register bits 15:14 and register bits 10:0, where register bit 0 gives seed bit S0; register bit 1 gives seed bit S1; etc., through register bit 10 gives seed bit S10, register bit 14 gives seed bit S11 and register bit 15 gives seed bit S12. The default PRBS13 seed values are given in Table 136–8.

45.2.1.141 PRBS pattern testing control (Register 1.1501)

Change the last four sentences of 45.2.1.141 as follows:

For the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 13 operates in conjunction with register 1.1501 bits 3 and 1. If neither bit is asserted, then register 1.1501 bit 13 has no effect. Also for the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 14 operates in conjunction with register 1.1501 bit 3. If bit 1.1501.3 is not asserted, then register 1.1501 bit 14 has no effect. For other PMA/PMD types register 1.1501 bits 13 and 14 have no effect.

45.2.3 PCS registers

45.2.3.1 PCS control 1 register (Register 3.0)

Change the bits 3.0.5:2 row in Table 45–177 as follows (unchanged rows not shown):

Table 45–177—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = Reserved 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s ~~Reserved~~ 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.2 PCS status 1 register (Register 3.1)

45.2.3.2.7 PCS receive link status (3.1.2)

Change the third sentence of 45.2.3.2.7 as follows:

When a 10/25/40/50/100/200/400GBASE-R, 10GBASE-W, or any MultiGBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), this bit is a latching low version of bit 3.32.12.

45.2.3.4 PCS speed ability (Register 3.4)

Change the bit 3.4.5 row in Table 45–179 as follows (unchanged rows not shown):

Table 45–179—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
3.4.5	~~Reserved~~ 50G capable	~~Value always 0~~ 1 = PCS is capable of operating at 50 Gb/s 0 = PCS is not capable of operating at 50 Gb/s	RO
…			

[a]RO = Read only

Insert 45.2.3.4.5a after 45.2.3.4.5:

45.2.3.4.5a 50G capable (3.4.5)

When read as a one, bit 3.4.5 indicates that the PCS is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 3.4.5 indicates that the PCS is not able to operate at a data rate of 50 Gb/s.

45.2.3.6 PCS control 2 register (Register 3.7)

Change Table 45–180 (as modified by IEEE Std 802.3cb-2018) as follows:

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:4	Reserved	Value always 0	RO
3.7.3:0	PCS type selection	3 2 1 0 1 1 1 1 = Select 5GBASE-R PCS type 1 1 1 0 = Select 2.5GBASE-X PCS type 1 1 0 1 = Select 400GBASE-R PCS type 1 1 0 0 = Select 200GBASE-R PCS type 1 0 1 1 = Select 5GBASE-T PCS type 1 0 1 0 = Select 2.5GBASE-T PCS type 1 0 0 1 = Select 25GBASE-T PCS type 1 0 0 0 = Select 50GBASE-R PCS type ~~reserved~~ 0 1 1 1 = Select 25GBASE-R PCS type 0 1 1 0 = Select 40GBASE-T PCS type 0 1 0 1 = Select 100GBASE-R PCS type 0 1 0 0 = Select 40GBASE-R PCS type 0 0 1 1 = Select 10GBASE-T PCS type 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.7 PCS status 2 register (Register 3.8)

Change the bit 3.8.8 row in Table 45–181 as follows (unchanged rows not shown):.

Table 45–181 —PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
...			
3.8.8	~~Reserved~~ 50GBASE-R capable	~~Value always 0~~ 1 = PCS is able to support 50GBASE-R PCS type 0 = PCS is not able to support 50GBASE-R PCS type	RO
...			

[a]RO = Read only, LH = Latching high

Insert 45.2.3.7.6a after 45.2.3.7.6:

45.2.3.7.6a 50GBASE-R capable (3.8.8)

When read as a one, bit 3.8.8 indicates that the PCS is able to support the 50GBASE-R PCS type. When read as a zero, bit 3.8.8 indicates that the PCS is not able to support the 50GBASE-R PCS type.

45.2.3.10 EEE control and capability 1 (Register 3.20)

Change Table 45–183 as follows (unchanged rows not shown):

Table 45–183—EEE control and capability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15~~:14~~	Reserved	Value always 0	RO
3.20.14	50GBASE-R fast wake	1 = EEE fast wake is supported for 50GBASE-R 0 = EEE fast wake is not supported for 50GBASE-R	RO
…			

[a]R/W = Read/Write, RO = Read only

Insert 45.2.3.10.a before 45.2.3.10.1:

45.2.3.10.a 50GBASE-R EEE fast wake supported (3.20.14)

If the PCS supports EEE fast wake operation for 50GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.15 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)

45.2.3.15.1 BASE-R and MultiGBASE-T receive link status (3.32.12)

Change the last sentence of 45.2.3.15.1 (as modified by IEEE Std 802.3cb-2018) as follows:

This bit is a reflection of the PCS_status variable defined in 49.2.14.1 for 5/10/25GBASE-R, in 126.3.7.1 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.1 for 10GBASE-T, in 113.3.7.1 for 25GBASE-T and 40GBASE-T, in 82.3.1 for 40/50/100GBASE-R, and in 119.3 for 200/400GBASE-R.

45.2.3.15.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)

Change the last sentence of the first paragraph of 45.2.3.15.4 (as modified by IEEE Std 802.3cb-2018) as follows:

This bit is a direct reflection of the state of the hi_ber variable in the BER monitor state diagrams as defined in 49.2.13.2.2 for 5/10/25GBASE-R and in 82.2.19.2.2 for 40/50/100GBASE-R.

45.2.3.15.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0)

Change the fourth sentence of 45.2.3.15.5 as follows:

For a 40/50/100GBASE-R PCS, this bit reflects the logical AND of the state of the block_lock<x> variables defined in 82.2.19.2.2.

45.2.3.16 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)

45.2.3.16.1 Latched block lock (3.33.15)

Change 45.2.3.16.1 (as modified by IEEE Std 802.3cb-2018) as follows:

When read as a one, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS block lock status bit (3.32.0).

45.2.3.16.2 Latched high BER (3.33.14)

Change 45.2.3.16.2 (as modified by IEEE Std 802.3cb-2018) as follows:

When read as a one, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS high BER status bit (3.32.1).

45.2.3.16.3 BER (3.33.13:8)

Change first sentence of 45.2.3.16.3 (as modified by IEEE Std 802.3cb-2018) as follows:

The BER counter is a six-bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.19.2.4 for 5/10/25/40/50/100GBASE-R and defined by counter lfer_count in 126.3.7.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.2 for 10GBASE-T, and in 113.3.7.2 for 25GBASE-T and 40GBASE-T.

45.2.3.16.4 Errored blocks (3.33.7:0)

Change first sentence of 45.2.3.16.4 (as modified by IEEE Std 802.3cb-2018) as follows:

The errored blocks counter is an eight-bit count defined by the counter errored_block_count specified in 49.2.14.2 for 5/10/25GBASE-R, in 82.3.1 for 40/50/100GBASE-R, in 126.3.7.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.2 for 10GBASE-T, and in 113.3.7.2 for 25GBASE-T and 40GBASE-T.

45.2.3.19 BASE-R PCS test-pattern control register (Register 3.42)

Change the fifth sentence of 45.2.3.19 as follows:

Scrambled idle test patterns are defined for 25/40/50/100/200/400GBASE-R PCS only.

45.2.7 Auto-Negotiation registers

Change Table 45–309 as follows (unchanged rows not shown):

Table 45–309—Auto-Negotiation MMD registers

Register address	Register name	Subclause
...		
7.49	Backplane Ethernet, BASE-R copper status 2	45.2.7.12a
7.4950 through 7.59	Reserved	
...		

45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

Change the title and first sentence of 45.2.7.12.3 (as modified by IEEE Std 802.3cb-2018) as follows:

45.2.7.12.3 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2)

When the AN process has been completed as indicated by the AN complete bit, these bits in register 7.48 and register 7.49 indicate the negotiated port type.

Insert 45.2.7.12a and 45.2.7.12a.1 after 45.2.7.12:

45.2.7.12a Backplane Ethernet, BASE-R copper status 2 (Register 7.49)

The assignment of bits in the Backplane Ethernet, BASE-R copper status 2 register is shown in Table 45–318a.

Table 45–318a—Backplane Ethernet, BASE-R copper status 2 register (Register 7.49) bit definitions

Bit(s)	Name	Description	RO[a]
7.49.15:3	Reserved	Value always 0	RO
7.49.2	200GBASE-KR4 or 200GBASE-CR4	1 = PMA/PMD is negotiated to perform 200GBASE-KR4 or 200GBASE-CR4 0 = PMA/PMD is not negotiated to perform 200GBASE-KR4 or 200GBASE-CR4	RO
7.49.1	100GBASE-KR2 or 100GBASE-CR2	1 = PMA/PMD is negotiated to perform 100GBASE-KR2 or 100GBASE-CR2 0 = PMA/PMD is not negotiated to perform 100GBASE-KR2 or 100GBASE-CR2	RO
7.49.0	50GBASE-KR or 50GBASE-CR	1 = PMA/PMD is negotiated to perform 50GBASE-KR or 50GBASE-CR 0 = PMA/PMD is not negotiated to perform 50GBASE-KR or 50GBASE-CR	RO

[a]RO = Read only

45.2.7.12a.1 Negotiated Port Type

See 45.2.7.12.3.

69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Change the second paragraph of 69.1.1 (as modified by IEEE Std 802.3cb-2018) as follows:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, or 100 Gb/s providing a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface or 200 Gb/s providing a BER better than or equal to 10^{-13} at the MAC/PLS service interface. The following Physical Layers are supported:

Change the list after the second paragraph of 69.1.1 (as modified by IEEE Std 802.3cb-2018) as follows:

- 1000BASE-KX for 1 Gb/s operation over a single lane
- 2.5GBASE-KX for 2.5 Gb/s operation over a single lane
- 5GBASE-KR for 5 Gb/s operation over a single lane
- 10GBASE-KX4 for 10 Gb/s operation over four lanes
- 10GBASE-KR for 10 Gb/s operation over a single lane
- 25GBASE-KR and 25GBASE-KR-S for 25 Gb/s operation over a single lane
- 40GBASE-KR4 for 40 Gb/s operation over four lanes
- 50GBASE-KR for 50 Gb/s operation over a single lane
- 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes
- 100GBASE-KR2 for 100 Gb/s operation over two lanes
- 200GBASE-KR4 for 200 Gb/s operation over four lanes

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change the first paragraph of 69.1.2 (as modified by IEEE Std 802.3cb-2018) as follows:

Backplane Ethernet couples the IEEE 802.3 MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1, Figure 69–2, Figure 69–3, ~~and~~ Figure 69–4, and Figure 69–5.

Insert Figure 69–5 after Figure 69–4 (as inserted by IEEE Std 802.3cb-2018):

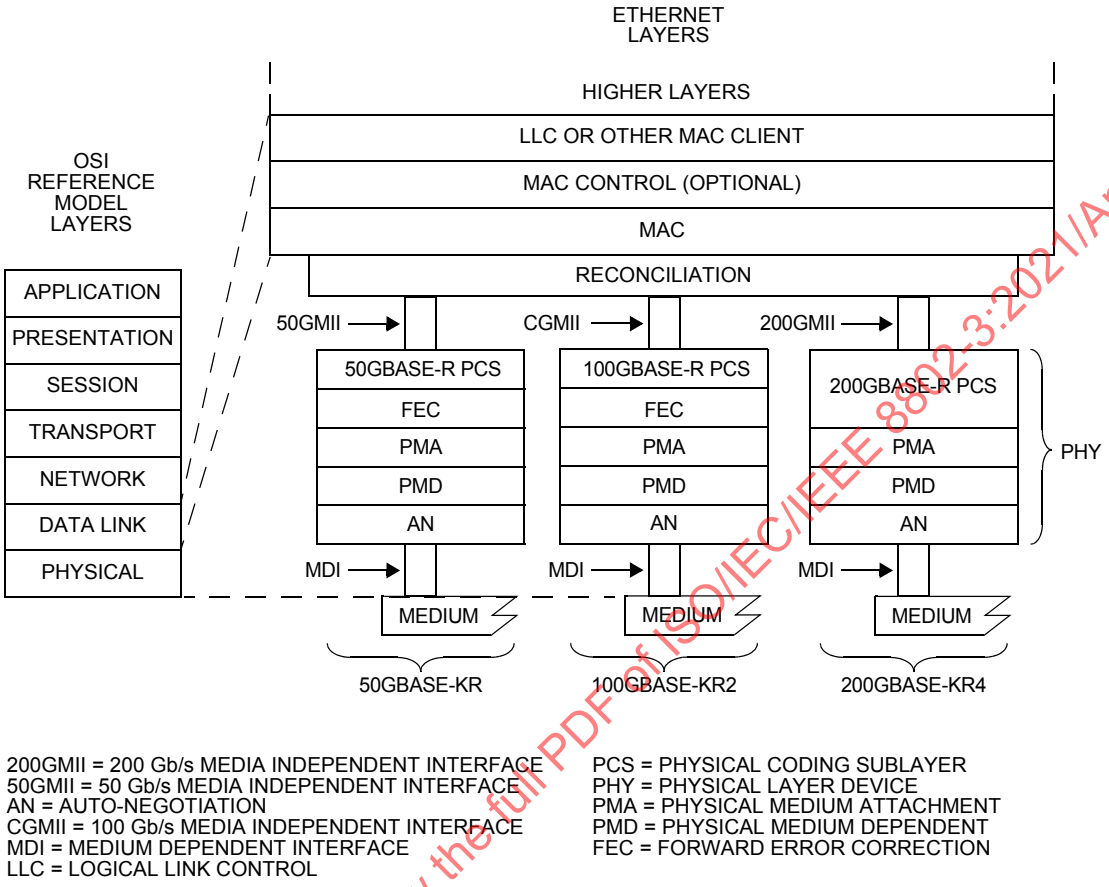


Figure 69–5—Architectural positioning of 50 Gb/s, 100 Gb/s, and 200 Gb/s PAM4 Backplane Ethernet

Change the lettered list in 69.1.2 (as modified by IEEE Std 802.3cb-2018) as follows (unchanged list items not shown):

f) The PMA service interface, which, when physically implemented as 25GAUI (25 Gigabit Attachment Unit Interface) or as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a serial data path as specified in Annex 109A or Annex 135F, respectively.

g) The PMA service interface, which, when physically implemented as LAUI-2/50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface) or as 100GAUI-2 (100 Gb/s two-lane Attachment Unit Interface) at an observable interconnection port, uses a serial two-lane path as specified in Annex 135B, Annex 135D, or Annex 135F, respectively.

h) ~~g)~~ The PMA service interface, which, when physically implemented as XLAUI (40 Gb/s Attachment Unit Interface), ~~or~~ as CAUI-4 (100 Gb/s four-lane Attachment Unit Interface), or as 200GAUI-4 (200 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a four-lane data path as specified in Annex 83A, ~~or~~ Annex 83D, or Annex 120D, respectively.

i) The PMA service interface, which, when physically implemented as 200GAUI-8 (200 Gb/s eight-lane Attachment Unit Interface) at an observable interconnection port, uses an eight-lane data path as specified in Annex 120B.

j) ~~h)~~ The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a ten-lane data path as specified in Annex 83A.

k) ~~i)~~ The MDIs for 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KR, 25GBASE-KR, ~~and~~ 25GBASE-KR-S, and 50GBASE-KR use a serial data path~~ while the MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, and 100GBASE-KP4 use a four-lane data path~~.

l) The MDI for 100GBASE-KR2 uses a two-lane data path.

m) The MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, 100GBASE-KP4, and 200GBASE-KR4 use a four-lane data path.

69.2 Summary of Backplane Ethernet Sublayers

69.2.1 Reconciliation sublayer and media independent interfaces

Change 69.2.1 as follows:

The Clause 35 RS and GMII, the Clause 46 RS and XGMII, the Clause 106 RS and 25GMII, ~~and~~ the Clause 81 RS, XLGMII, and CGMII, the Clause 132 RS and 50GMII, and the Clause 117 RS and 200GMII are employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.3 Physical Layer signaling systems

Insert the following new paragraph into 69.2.3 (as modified by IEEE Std 802.3cb-2018) after the now seventh paragraph ("Backplane Ethernet also specifies 40GBASE-KR4...."):

Backplane Ethernet also specifies 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4. The 50GBASE-KR embodiment employs the PCS defined in Clause 133, the RS-FEC defined in Clause 134, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 50 Gb/s operation using 4-level PAM over one differential path in each direction. The 100GBASE-KR2 embodiment employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 100 Gb/s operation using 4-level PAM over two differential paths in each direction. The 200GBASE-KR4 embodiment employs the PCS defined in Clause 119, the PMA defined in Clause 120, and the PMD defined in Clause 137, and specifies 200 Gb/s operation using 4-level PAM over four differential paths in each direction.

Change the last paragraph in 69.2.3 (as modified by IEEE Std 802.3cb-2018) as follows:

Table 69–1, Table 69–1a, Table 69–2, ~~and~~ Table 69–2a, Table 69–3, Table 69–3a, and Table 69–3b specify the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Insert Table 69–2a after Table 69–2:

Table 69–2a—Nomenclature and clause correlation for 50 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]									
	78	132		133	134	135	135A	135B	135C	137
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-KR PMD
50GBASE-KR	O	M	O	M	M	M	O	O	O	M

[a]O = Optional, M = Mandatory.

Change the title of Table 69–3 as follows:

Table 69–3—Nomenclature and clause correlation for 40 Gb/s and four-lane 100 Gb/s Backplane Ethernet Physical Layers

Insert Table 69–3a and Table 69–3b after Table 69–3:

Table 69–3a—Nomenclature and clause correlation for two-lane 100 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]											
	78	81		82	83	83A	83D	91	135	135D	135F	137
	EEE	RS	100GMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10 C2C	CAUI-4 C2C	100GBASE-R RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-KR2 PMD
100GBASE-KR2	O	M	O	M	O	O	O	M	M	O	O	M

[a]O = Optional, M = Mandatory.

Table 69–3b—Nomenclature and clause correlation for 200 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause[a]							
	78	117		119	120	120B	120D	137
	EEE	RS	200GMII	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	100GBASE-KR4 PMD
200GBASE-KR4	O	M	O	M	M	O	O	M

[a]O = Optional, M = Mandatory.

69.3 Delay constraints

Insert the following paragraph into 69.3 (as modified by IEEE Std 802.3cb-2018) after the now sixth paragraph ("For 40GBASE-KR4...."):

For 50GBASE-KR, normative delay specifications may be found in 132.1.4, 133.3, 135.5.4, and 137.5, and also referenced in 131.4.

Insert the following paragraphs into 69.3 (as modified by IEEE Std 802.3cb-2018) after the now ninth paragraph ("For 100GBASE-KP4...."):

For 100GBASE-KR2, normative delay specifications may be found in 81.1.4, 82.5, 135.5.4, and 137.5, and also referenced in 80.4.

For 200GBASE-KR4, normative delay specifications may be found in 117.1.4, 119.5, 120.5.4, and 137.5, and also referenced in 116.4.

69.5 Protocol implementation conformance statement (PICS) proforma

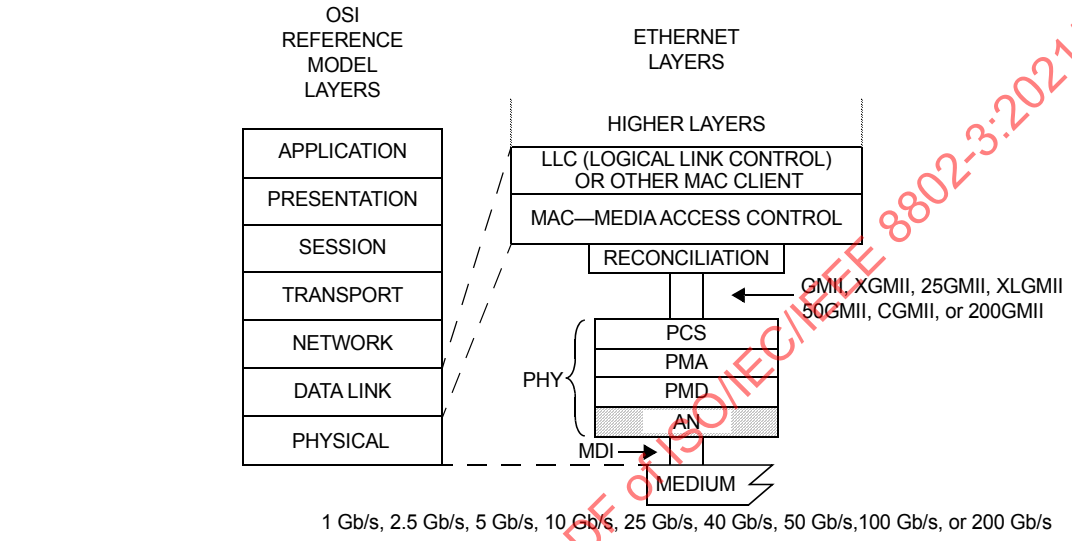
Change the first paragraph of 69.5 (as modified by IEEE Std 802.3cb-2018) as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 84, Clause 91, Clause 93, Clause 94, Clause 108, Clause 111, Clause 119, Clause 128, Clause 130, Clause 134, Clause 137, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

73. Auto-Negotiation for backplane and copper cable assembly

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Replace the Figure 73–1 from IEEE Std 802.3cb-2018 with the following figure:



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

73.5 DME transmission

73.5.1 DME electrical specifications

Change the second paragraph of 73.5.1 as follows:

For any multi-lane PHY, DME pages shall be transmitted only on lane 0. The transmitters on other lanes should be disabled as specified in 71.6.7, 84.7.7, 85.7.7, 92.7.7, 93.7.7, ~~or~~ 94.3.6.7, 136.8.7, or 137.8.7.

73.6 Link codeword encoding

73.6.4 Technology Ability Field

Change Table 73–4 (as modified by IEEE Std 802.3cb-2018) as follows:

Table 73–4—Technology Ability Field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3	40GBASE-KR4
A4	40GBASE-CR4
A5	100GBASE-CR10
A6	100GBASE-KP4
A7	100GBASE-KR4
A8	100GBASE-CR4
A9	25GBASE-KR-S or 25GBASE-CR-S
A10	25GBASE-KR or 25GBASE-CR
A11	2.5GBASE-KX
A12	5GBASE-KR
A13	50GBASE-KR or 50GBASE-CR
A14	100GBASE-KR2 or 100GBASE-CR2
A15	200GBASE-KR4 or 200GBASE-CR4
~~A13~~A16 through A22	Reserved ~~for future technology~~

Change the last paragraph of 73.6.4 (as modified by IEEE Std 802.3cb-2018) as follows:

The fields A[22:16~~13~~] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.7 Receive function requirements

73.7.6 Priority Resolution function

Change Table 73–5 (as modified by IEEE Std 802.3cb-2018) as follows:.

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	200GBASE-KR4 or 200GBASE-CR4	200 Gb/s 4 lane, highest priority
2	100GBASE-KR2 or 100GBASE-CR2	100 Gb/s 2 lane
3 ~~1~~	100GBASE-CR4	100 Gb/s 4 lane~~, highest priority~~
4 ~~2~~	100GBASE-KR4	100 Gb/s 4 lane
5 ~~3~~	100GBASE-KP4	100 Gb/s 4 lane
6 ~~4~~	100GBASE-CR10	100 Gb/s 10 lane
7	50GBASE-KR or 50GBASE-CR	50 Gb/s 1 lane
8 ~~5~~	40GBASE-CR4	40 Gb/s 4 lane
9 ~~6~~	40GBASE-KR4	40 Gb/s 4 lane
10 ~~7~~	25GBASE-KR or 25GBASE-CR	25 Gb/s 1 lane
11 ~~8~~	25GBASE-KR-S or 25GBASE-CR-S	25 Gb/s 1 lane, short reach
12 ~~9~~	10GBASE-KR	10 Gb/s 1 lane
13 ~~10~~	10GBASE-KX4	10 Gb/s 4 lane
14 ~~11~~	5GBASE-KR	5 Gb/s 1 lane
15 ~~12~~	2.5GBASE-KX	2.5 Gb/s 1 lane
16 ~~13~~	1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10 State diagrams and variable definitions

73.10.1 State diagram variables

Insert the following new entry into the first variable list in 73.10.1 (as modified by IEEE Std 802.3cb-2018) after the 40GCR4 entry:

50GR; represents the 50GBASE-KR or 50GBASE-CR PMD.

Insert the following new entries into the first variable list in 73.10.1 (as modified by IEEE Std 802.3cb-2018) after the 100GCR4 entry:

100GR2; represents the 100GBASE-KR2 or 100GBASE-CR2 PMD.

200GR4; represents the 200GBASE-KR4 or 200GBASE-CR4 PMD.

Change the single_link_ready entry in the list after the third paragraph ('Variables of the form "mr_x", ...') in 73.10.1 (as modified by IEEE Std 802.3cb-2018) as shown:

single_link_ready

Status indicating that an_receive_idle = true and only one of the following indications is being received:

1) link_status_[1GKX] = OK
2) link_status_[2.5GKX] = OK
3) link_status_[5GKR] = OK
4) link_status_[10GKX4] = OK
5) link_status_[10GKR] = OK
6) link_status_[25GR] = OK
7) link_status_[40GKR4] = OK
8) link_status_[40GCR4] = OK
9) link_status_[50GR] = OK
10~~9~~) link_status_[100GCR10] = OK
11~~10~~) link_status_[100GKP4] = OK
12~~11~~) link_status_[100GKR4] = OK
13~~12~~) link_status_[100GCR4] = OK
14) link_status_[100GR2] = OK
15) link_status_[200GR4] = OK

73.10.2 State diagram timers

Change Table 73–7 (as modified by IEEE Std 802.3cb-2018) as follows:

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
autoneg_wait_timer	25		50	ms
break_link_timer	60		75	ms
clock_detect_min_timer	4.8		6.2	ns
clock_detect_max_timer	6.6		8.0	ns
data_detect_min_timer	1.6		3.0	ns
data_detect_max_timer	3.4		4.8	ns
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is 50GBASE-KR, 50GBASE-CR, 100GBASE-KR2, 100GBASE-CR2, 200GBASE-KR4 or 200GBASE-CR4)	3.1		3.2	s
link_fail_inhibit_timer (when the link is 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-CR4, or 100GBASE-CR10 ~~not 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, or 10GBASE-KX4~~)	500		510	ms
link_fail_inhibit_timer (when the link is 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, or 10GBASE-KX4)	40		50	ms
page_test_min_timer	305		330	ns
page_test_max_timer	350		375	ns

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

Change the third paragraph of 78.1 as follows:

EEE supports operation over twisted-pair cabling systems, twinaxial cable, electrical backplanes, optical fiber, the XGXS for 10 Gb/s PHYs, the 25GAUI for 25 Gb/s PHYs, the XLAUI for 40 Gb/s PHYs, the LAUI-2 or 50GAUI-n for 50 Gb/s PHYs, the ~~CAUI-10 or CAUI-4~~ CAUI-n or 100GAUI-n for 100 Gb/s PHYs, the 200GAUI-n and 200GXS for 200 Gb/s PHYs, and the 400GAUI-n and 400GXS for 400 Gb/s PHYs. Table 78–1 lists the supported PHYs and interfaces and their associated clauses.

78.1.4 PHY types optionally supporting EEE

Change following group of rows in Table 78–1 as shown:

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
…	
40GBASE-ER4[b]	82, 83, 87
50GBASE-KR[b]	133, 134, 137
50GBASE-CR[b]	133, 134, 136
50GBASE-SR[b]	133, 134, 138
50GBASE-FR[b]	133, 134, 139
50GBASE-LR[b]	133, 134, 139
CAUI-10[a]	83A
CAUI-4[a]	83D
100GBASE-KR4	82, 83, 91, 93
100GBASE-KP4	82, 91, 94
100GBASE-CR2[b]	82, 135, 136
100GBASE-CR4	82, 83, 91, 92
100GBASE-CR10	82, 83, 85, 74
100GBASE-KR2[b]	82, 135, 137
100GBASE-SR4[b]	82, 83, 91, 95
100GBASE-SR2[b]	82, 135, 138
100GBASE-SR10[b]	82, 83, 86
100GBASE-DR[b]	82, 135, 140
100GBASE-LR4[b]	82, 83, 88
100GBASE-ER4[b]	82, 83, 88

Table 78–1—Clauses associated with each PHY or interface type *(continued)*

PHY or interface type	Clause
200GBASE-KR4[b]	119, 120, 137
200GBASE-CR4[b]	119, 120, 136
200GBASE-SR4[b]	119, 120, 138
200GBASE-DR4[b]	119, 120, 121
…	

[a]25GAUI/XLAUI/CAUI-n shutdown is supported only when deep sleep is enabled for the associated PHY.
[b]The deep sleep mode of EEE is not supported for this PHY.

78.5 Communication link access latency

Insert the following row into Table 78–4 after the "40GBASE-T" row:

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
50GBASE-R fast wake		0.34	0.3	0	0	0.25

80. Introduction to 40 Gb/s and 100 Gb/s networks

80.1 Overview

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

Change the second paragraph in 80.1.3 as follows:

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XLGMII and CGMII, which, when implemented as a logical interconnection port between the MAC sublayer and the Physical Layer (PHY), uses a 64-bit wide data path as specified in Clause 81. Physical instantiations of this interface may use other data-path widths.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as XLAUI (40 Gb/s Attachment Unit Interface) or CAUI-4 and 100GAUI-4 (100 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A, Annex 83B, Annex 83D, ~~or~~ Annex 83E, Annex 135D, or Annex 135E.

d) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 83A or Annex 83B.

e) The PMA service interface, which, when physically implemented as 100GAUI-2 (100 Gb/s 2 lane Attachment Unit Interface) at an observable interconnection port, uses a 2 lane data path as specified in Annex 135F or Annex 135G.

f) ~~e)~~ The PMD service interface, which, when physically implemented as XLPPI (40 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 86A.

g) ~~f)~~ The PMD service interface, which, when physically implemented as CPPI (100 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 86A.

h) ~~g)~~ The MDIs as specified in Clause 89 for 40GBASE-FR and Clause 140 for 100GBASE-DR use ~~uses~~ a single lane data path.

i) ~~h)~~ The MDIs as specified in Clause 85 for 40GBASE-CR4, in Clause 86 for 40GBASE-SR4, in Clause 87 for 40GBASE-LR4 and 40GBASE-ER4, in Clause 88 for 100GBASE-LR4 and 100GBASE-ER4, in Clause 92 for 100GBASE-CR4, and in Clause 95 for 100GBASE-SR4 all use a 4 lane data path.

j) ~~i)~~ The MDIs as specified in Clause 85 for 100GBASE-CR10, and in Clause 86 for 100GBASE-SR10 use a 10 lane data path.

k) ~~j)~~ Although there is no electrical or mechanical specification of the MDI for backplane Physical Layers, the PMDs as specified in Clause 84 for 40GBASE-KR4, in Clause 93 for 100GBASE-KR4, and in Clause 94 for 100GBASE-KP4 all use a 4 lane data path.

l) ~~k)~~ The MDI as specified in Clause 113 for 40GBASE-T uses a 4 lane data path.

m) The MDIs as specified in Clause 136 for 100GBASE-CR2, in Clause 137 for 100GBASE-KR2, and in Clause 138 for 100GBASE-SR2 all use a 2 lane data path.

80.1.4 Nomenclature

Change following group of rows in Table 80–1 as shown:

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
…	
40GBASE-T	40 Gb/s PHY using RS-FEC and LDPC encoding over balanced twisted-pair structured cabling systems (see Clause 113)
100GBASE-KR2	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of an electrical backplane, with a total insertion loss up to 30 dB at 13.28 GHz (see Clause 137)
100GBASE-KR4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz (see Clause 93)
100GBASE-KP4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz (see Clause 94)
100GBASE-CR2	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of shielded balanced copper cabling, with reach up to at least 3 m (see Clause 136)
100GBASE-CR4	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m (see Clause 92)
100GBASE-CR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of shielded balanced copper cabling, with reach up to at least 7 m (see Clause 85)
100GBASE-SR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of multimode fiber, with reach up to at least 100 m (see Clause 86)
100GBASE-SR2	100 Gb/s PHY using 100GBASE-R encoding over two lanes of multimode fiber, with reach up to at least 100 m (see Clause 138)
100GBASE-SR4	100 Gb/s PHY using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 95)
100GBASE-DR	100 Gb/s PHY using 100GBASE-R encoding over single-mode fiber, with reach up to at least 500 m (see Clause 140)
100GBASE-LR4	100 Gb/s PHY using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 88)
100GBASE-ER4	100 Gb/s PHY using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 88)

80.1.5 Physical Layer signaling systems

Change the first paragraph of 80.1.5 as follows:

This standard specifies a family of Physical Layer implementations. Table 80–2, Table 80–3, ~~and~~ Table 80–4, and Table 80–4a specify the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures must meet the requirements of the corresponding clauses.

Change Table 80–3 as follows:

Table 80–3—Nomenclature and clause correlation (100GBASE copper)

Nomenclature	Clause[a]																		
	73	74	78	81		82	83	83A	83D	85	91	92	93	94	135	135D	135F	136	137
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-4	100GBASE-CR10 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-CR2	100GBASE-KR2
100GBASE-KR2	M		O	M	O	M		O	O		M				M	O	O		M
100GBASE-KR4	M		O	M	O	M	M	O	O		M		M						
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M					
100GBASE-CR2	M		O	M	O	M		O	O		M				M	O	O	M	
100GBASE-CR4	M		O	M	O	M	M	O	O		M	M							
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M									

[a]O = Optional, M = Mandatory.

Change the title of Table 80–4 as follows:

Table 80–4—Nomenclature and clause correlation (100GBASE-R optical)

Insert Table 80–4a after Table 80–4 as follows:

Table 80–4a—Nomenclature and clause correlation (100GBASE-P optical)

Nomenclature	Clause[a]																
	78	81		82	83	83A	83B	83D	83E	91	135	135D	135E	135F	135G	138	140
	EEE	RS	CGMII	PCS	100GBASE-R PMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-4 C2M	100GAUI-2 C2C	100GAUI-2 C2M	100GBASE-SR2	100GBASE-DR
100GBASE-SR2	O	M	O	M	O	O	O	O	O	M	M	O	O	O	O	M	
100GBASE-DR	O	M	O	M	O	O	O	O	O	M	M	O	O	O	O		M

[a]O = Optional, M = Mandatory.

80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers

80.2.2 Physical Coding Sublayer (PCS)

Change 80.2.2 as follows:

The terms 40GBASE-R, 100GBASE-R, and 100GBASE-P refer to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 82 and the PMA specifications defined in Clause 83, ~~or~~ Clause 94, or Clause 135. Clause 82 PCSs perform encoding (decoding) of data from (to) the XLGMII/CGMII to 64B/66B code blocks, distribute the data to multiple lanes, and transfer the encoded data to the PMA.

80.2.3 Forward Error Correction (FEC) sublayers

Change the first paragraph in 80.2.3 as follows:

A Forward Error Correction sublayer ~~is available for all 40GBASE-R and 100GBASE-R copper and backplane PHYs as well as 100GBASE-SR4. It~~ is optional for 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR2, 100GBASE-CR4, 100GBASE-KR2, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-SR2, ~~and~~ 100GBASE-SR4, and 100GBASE-DR PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers.

80.2.4 Physical Medium Attachment (PMA) sublayer

Change the second paragraph of 80.2.4 as follows:

The 40GBASE-R and 100GBASE-R PMAs are specified in Clause 83. The PMA specific to the 100GBASE-KP4 PHY is specified in Clause 94. The PMA for other 100GBASE-P PHYs is specified in Clause 135.

80.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph of 80.2.5 as follows:

The 40GBASE-R, 100GBASE-R, and 100GBASE-P PMDs and their corresponding media are specified in Clause 84 through Clause 89, ~~and~~ Clause 92 through Clause 95, Clause 136 through Clause 138, and Clause 140.

80.2.6 Auto-Negotiation

Change the second paragraph of 80.2.6 as follows:

Clause 73 Auto-Negotiation is used by the 40 Gb/s and 100 Gb/s backplane PHYs (40GBASE-KR4, 100GBASE-KR2, 100GBASE-KP4, and 100GBASE-KR4) and the 40 Gb/s and 100 Gb/s copper PHYs (40GBASE-CR4, 100GBASE-CR2, 100GBASE-CR10, and 100GBASE-CR4).

80.4 Delay constraints

Change the following group of rows in Table 80–5 as follows:

Table 80–5—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
…				
100GBASE-R PMA	9 216	18	92.16	See 83.5.4.
100GBASE-P PMA	9 216	18	92.16	See 135.5.4.
100GBASE-KR2 PMD	4 096	8	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
100GBASE-KR4 PMD	2 048	4	20.48	Includes delay of one direction through backplane medium. See 93.4.
100GBASE-KP4 PMA/PMD	8 192	16	81.92	Includes delay of one direction through backplane medium. See 94.2.5.
100GBASE-CR2 PMD	4 096	8	40.96	Includes allocation for 20 ns for one direction through cable medium. See 136.5.
100GBASE-CR4 PMD	2 048	4	20.48	Does not include delay of cable medium. See 92.4.
100GBASE-CR10 PMD	9 728	19	97.28	Does not include delay of cable medium. See 85.4.
100GBASE-SR2 PMD	2 048	4	20.48	Includes 2 m of fiber. See 138.3.
100GBASE-SR4 PMD	2 048	4	20.48	Includes 2 m of fiber. See 95.3.1.
100GBASE-SR10 PMD	2 048	4	20.48	Includes 2 m of fiber. See 86.3.1.
100GBASE-DR PMD	2 048	4	20.48	Includes 2 m of fiber. See 140.3.
100GBASE-LR4 PMD	2 048	4	20.48	Includes 2 m of fiber. See 88.3.1.
100GBASE-ER4 PMD	2 048	4	20.48	Includes 2 m of fiber. See 88.3.1.

[a] For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.160 for the definition of bit time.)
[b] For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

80.5 Skew constraints

Replace Figure 80–8 with the following figure:

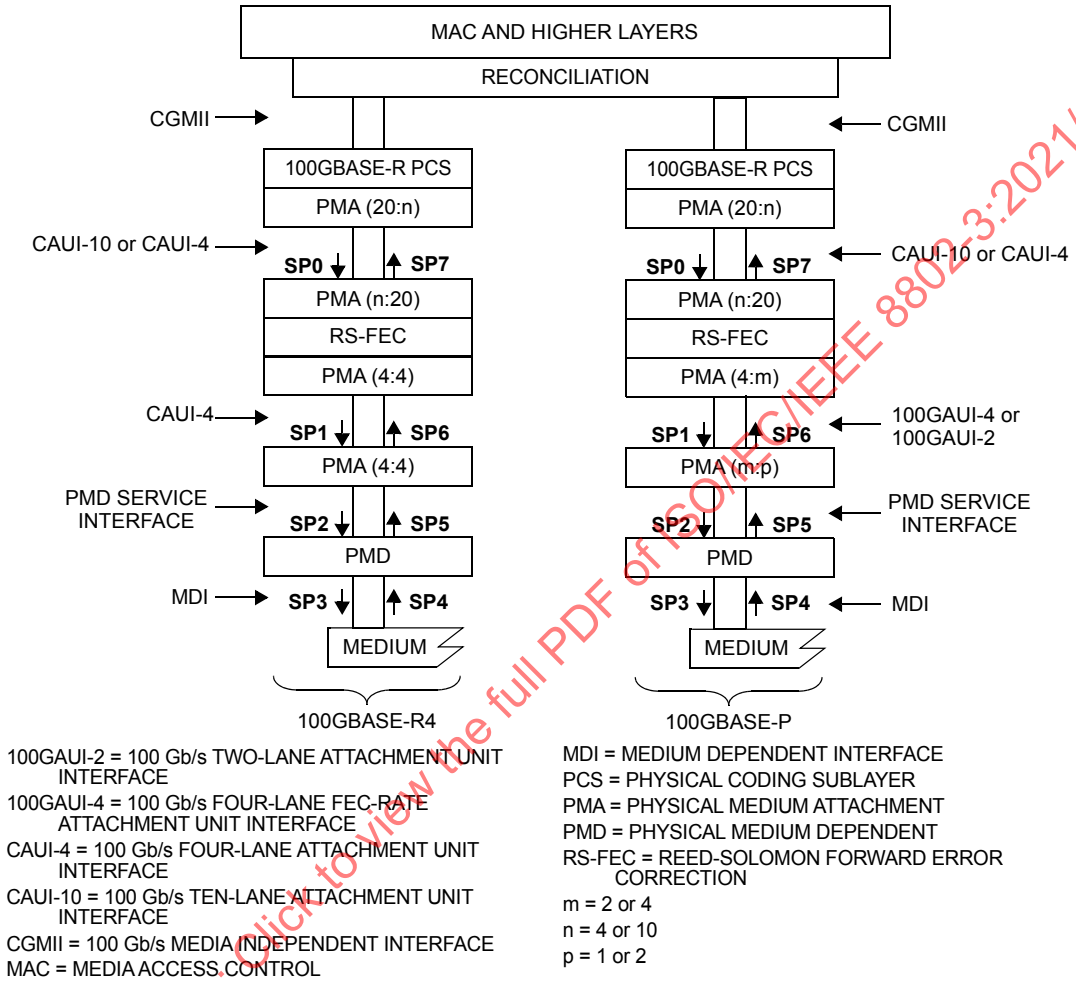


Figure 80–8—100GBASE-R Skew points with RS-FEC, CAUI-n, and 100GAUI-n

Change Table 80–6 as follows (table footnotes remain unchanged and are not shown):

Table 80–6—Summary of Skew constraints

Skew points	Maximum Skew (ns)	Maximum Skew for 40GBASE-R PCS lane (UI)	Maximum Skew for 100GBASE-R PCS lane (UI)	Notes
SP0	29	N/A	≈ 150	See 83.5.3.1 or 135.5.3
SP1	29	≈ 299	≈ 150	See 83.5.3.2 or 135.5.3
SP2	43	≈ 443	≈ 222	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.3
SP3	54	≈ 557	≈ 278	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.3
SP4	134	≈ 1382	≈ 691	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.3
SP5	145	≈ 1495	≈ 748	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3, or 140.3
SP6	160	≈ 1649	≈ 824	See 83.5.3.6 or 135.5.3
SP7	29	N/A	≈ 150	See 83.5.3.8 or 135.5.3
At PCS receive	180	≈ 1856	≈ 928	See 82.2.13
At RS-FEC transmit	49	N/A	≈ 253	See 91.5.2.2
At RS-FEC receive	180	N/A	≈ 4641	See 91.5.3.1
At PCS receive (with RS-FEC)	49	N/A	≈ 253	See 82.2.13

Change Table 80–7 as follows:

Table 80–7—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation				Notes[d]
	~~Maximum Skew Variation (ns)~~	~~Maximum Skew Variation~~ UI for 10.3125 GBd ~~PMD~~ lane ~~(UI)~~[a]	~~Maximum Skew Variation~~ UI for 25.78125 GBd ~~PMD~~ lane ~~(UI)~~[b]	UI for 26.5625 GBd lane[c]	
SP0	0.2	≈ 2	N/A	N/A	See 83.5.3.1 or 135.5.3
SP1	0.2	≈ 2	N/A	≈ 5	See 83.5.3.2 or 135.5.3
SP2	0.4	≈ 4	≈ 10	≈ 11	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, or 138.3
SP3	0.6	≈ 6	≈ 15	≈ 16	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 136.6, 137.6, or 138.3
SP4	3.4	≈ 35	≈ 88	≈ 90	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 136.6, 137.6, or 138.3
SP5	3.6	≈ 37	≈ 93	≈ 96	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, ~~or~~ 95.3.2, 135.5.3, 136.6, 137.6, 138.3
SP6	3.8	≈ 39	≈ 98	≈ 101	See 83.5.3.6 or 135.5.3
SP7	0.2	≈ 2	N/A	N/A	See 83.5.3.8 or 135.5.3
At PCS receive	4	≈ 41	N/A	N/A	See 82.2.13
At RS-FEC transmit	0.4	N/A	≈ 10	≈ 11	See 91.5.2.2
At RS-FEC receive[e]	4	N/A	≈ 103	≈ 106	See 91.5.3.1
At PCS receive (with RS-FEC)	0.4	N/A	≈ 10	N/A	See 82.2.13

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PMD lane signaling rate of 10.3125 GBd.

[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 100GBASE-R, based on 1 UI equals 38.787879 ps at PMD lane signaling rate of 25.78125 GBd.

[c]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 100GBASE-R, based on 1 UI equals 37.64706 ps at PMD lane signaling rate of 26.5625 GBd.

[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

[e]The skew at the RS-FEC receive is the skew between RS-FEC lanes.

80.7 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 80.7 as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, Clause 73, Clause 74, Clause 81 through Clause 89, Clause 91 through Clause 95, Clause 135 through Clause 138, Clause 140, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.6 Auto-Negotiation

Change 82.6 as follows:

The following requirements apply to a PCS used with a 40GBASE-KR4 PMD, 40GBASE-CR4 PMD, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, ~~or~~ 100GBASE-KP4, or 100GBASE-KR2 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R[2]

82.7.4 PICS proforma tables for PCS, type 40GBASE-R and 100GBASE-R

82.7.4.11 Auto-Negotiation for Backplane Ethernet functions

Change the table in 82.7.4.11 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*AN1	Support for use with a 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, ~~or~~ 100GBASE-KP4, or 100GBASE-KR2 PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN2	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status)~~, when the PCS is used with 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-KP4 PMD~~	AN1:M	Yes [ ] N/A [ ]
AN3	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN1:M	Yes [ ] N/A [ ]
AN4	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN1:M	Yes [ ] N/A [ ]

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90. Ethernet support for time synchronization protocols

90.1 Introduction

Change the second paragraph of 90.1 as follows:

The TSSI is defined for the full-duplex mode of operation only. It supports MAC operation at various data rates. The MII (Clause 22), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII (Clause 81), 50GMII (Clause 132), CGMII (Clause 81), 200GMII (Clause 117), and 400GMII (Clause 117) specifications are all compatible with the gRS sublayer defined in 90.5.

91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.3 PMA compatibility

Change the second sentence of the first paragraph of 91.3 as follows:

Therefore, the RS-FEC sublayer may be a client of the PMA sublayer defined in Clause 83 or Clause 135 when the PMA service interface width, *p*, is set to 4.

91.5 Functions within the RS-FEC sublayer

91.5.2 Transmit function

91.5.2.6 Alignment marker mapping and insertion

Change the third and fourth paragraphs of 91.5.2.6 as follows:

For *x*=0 to 19, amp_tx_*x*<63:0> is constructed as follows:

a) Set *y* = 0 when *x* ≤ 3, set *y* = 16 when *x* ≥ 16 and four_lane_pmd, otherwise set *y* = *x*.
b) amp_tx_*x*<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–2 for PCS lane number *y*. If am_tx_*x* corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–11).
c) amp_tx_*x*<31:24> = am_tx_*x*<33:26>
d) amp_tx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–2 for PCS lane number *y*. If am_tx_*x* corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–11).
e) amp_tx_*x*<63:56> = am_tx_*x*<65:58>

This process replaces the fixed bytes of the alignment markers received, possibly with errors, with the values from Table 82–2. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 1, 2, and 3 with the fixed bytes for the alignment marker corresponding to PCS lane 0. Similarly when used with a four-lane PMD, it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16. The variable bytes BIP or CD are unchanged. This process simplifies receiver synchronization since the receiver only needs to search for the fixed bytes corresponding to PCS lane 0 on each FEC lane. When the optional EEE deep sleep capability is supported, the receiver only needs to search for the fixed bytes corresponding to PCS lanes 0 and 16.

91.5.2.7 Reed-Solomon encoder

Change the second sentence of the second paragraph of 91.5.2.7 as follows:

When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the RS-FEC sublayer shall implement RS(544,514).

91.5.3 Receive function

91.5.3.3 Reed-Solomon decoder

Change the second sentence of the second paragraph of 91.5.3.3 as follows:

When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword.

Change the last sentence of the third paragraph of 91.5.3.3 as follows:

This option shall not be used when the RS-FEC sublayer is used to form part of a 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-SR4, or 100GBASE-DR PHY.

Change the last sentence of the last paragraph of 91.5.3.3 as follows:

When the RS-FEC sublayer used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY, the symbol error threshold shall be K=6380.

Insert 91.5.3.3.1 after 91.5.3.3:

91.5.3.3.1 FEC Degraded SER (optional)

For 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, and 100GBASE-DR PHYs an optional FEC degraded symbol error ratio function is available.

The Reed-Solomon decoder may optionally provide the ability to indicate a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 91.6.5a). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 91.6.2b).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the total number of symbol errors detected in consecutive non-overlapping blocks of FEC_degraded_SER_interval codewords (see 91.6.2e). If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 91.6.2c), the FEC_degraded_SER bit (see 91.6.5b) is set. At the end of each interval, if the number of symbol errors is less than the threshold set in FEC_degraded_SER_deactivate_threshold (see 91.6.2d), the FEC_degraded_SER bit is cleared. The value of the FEC_degraded_SER bit is unspecified if the value of FEC_degraded_SER_activate_threshold is less than the value of FEC_degraded_SER_deactivate_threshold.

If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is deasserted then the FEC_degraded_SER bit is cleared.

91.6 RS-FEC MDIO function mapping

Insert the following rows at end of Table 91–2:

Table 91–2—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
Four lane PMD	RS-FEC control register	1.200.3	four_lane_pmd
FEC degraded SER enable	RS-FEC control register	1.200.4	FEC_degraded_SER_enable
FEC degraded SER activate threshold	RS-FEC degraded SER activate threshold register	1.650, 1.651	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	RS-FEC degraded SER deactivate threshold register	1.652, 1.653	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	RS-FEC degraded SER interval register	1.654, 1.655	FEC_degraded_SER_interval

Insert the following rows in Table 91–3 after the "RS-FEC high SER" row:

Table 91–3—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC degraded SER ability	RS-FEC status register	1.201.3	FEC_degraded_SER_ability
FEC degraded SER	RS-FEC status register	1.201.4	FEC_degraded_SER

Insert 91.6.2a through 91.6.2e after 91.6.2:

91.6.2a four_lane_pmd

When this variable is set to one, the alignment marker mapping function substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this variable is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of the variable is one which is the value required by the 100GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, and 100GBASE-SR4 PMDs. This variable is set to zero for the 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, and 100GBASE-DR PMDs. This variable is mapped to the bit defined in 45.2.1.110 (1.200.3).

91.6.2b FEC_degraded_SER_enable

This variable enables the FEC decoder to indicate the presence of a degraded SER when the ability is supported (see 91.5.3.3.1). When set to a one, this variable enables degraded SER detection. When set to a zero, degraded SER detection is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER. This variable is mapped to the bit defined in 45.2.1.110 (1.200.4).

91.6.2c FEC_degraded_SER_activate_threshold

This variable controls the threshold used to set the FEC_degraded_SER bit as defined in 91.5.3.3.1. It is mapped to the registers defined in 45.2.1.132h (1.650, 1.651).

91.6.2d FEC_degraded_SER_deactivate_threshold

This variable controls the threshold used to clear the FEC_degraded_SER bit as defined in 91.5.3.3.1. It is mapped to the registers defined in 45.2.1.132i (1.652, 1.653).

91.6.2e FEC_degraded_SER_interval

This variable controls the interval used to set and clear the FEC_degraded_SER bit as defined in 91.5.3.3.1. It is mapped to the registers defined in 45.2.1.132j (1.654, 1.655).

Insert 91.6.5a and 91.6.5b after 91.6.5:

91.6.5a FEC_degraded_SER_ability

The FEC decoder may have the option to indicate the presence of a degraded SER (see 91.5.3.3.1). This variable is set to one to indicate that the FEC decoder has the ability to indicate the presence of a degraded SER. This variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.111 (1.201.3).

91.6.5b FEC_degraded_SER

When FEC_degraded_SER_enable is asserted, this variable indicates the presence of a degraded SER as defined in 91.5.3.3.1. This variable is mapped to the bit defined in 45.2.1.111 (1.201.4).

91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs[3]

91.7.3 Major capabilities/options

Change the PICS item *KP4 row in the table in 91.7.3 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…	…	…	…	…	…
*KP4	100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR		Used to form complete 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY	O	Yes [ ] No [ ]

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Insert the following rows for PICS items *FDDP and *FDD into the table in 91.7.3 after the *KP4 row:

Item	Feature	Subclause	Value/Comment	Status	Support
*FDDP	100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR	91.5.3.3.1	Used to form complete 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR PHY	O	Yes [ ] No [ ]
*FDD	Support for optional FEC degraded SER detection	91.5.3.3.1		FDDP:O	Yes [ ] No [ ] N/A [ ]

91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

91.7.4.1 Transmit function

Change the PICS item TF11 row in the table in 91.7.4.1 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…	…	…	…	…	…
TF11	Reed-Solomon encoder for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR	91.5.2.7	RS(544,514)	KP4:M	Yes [ ] N/A [ ]

91.7.4.2 Receive function

Change the table in 91.7.4.2 as follows (some unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…	…	…	…	…	…
RF4	Reed-Solomon decoder for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR	91.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword unless error correction bypassed	KP4:M	Yes [ ] N/A [ ]
…	…	…	…	…	…
RF6	Error correction bypass for 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-SR4, or 100GBASE-DR	91.5.3.3	Error correction is not bypassed	SR4:M or FDDP:M	Yes [ ] N/A [ ]
…	…	…	…	…	…

Item	Feature	Subclause	Value/Comment	Status	Support
RF12	Symbol error threshold for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, or 100GBASE-DR	91.5.3.3	*K*=6380	BEI* KP4:M	Yes [ ] N/A [ ]
…	…	…	…	…	…
RF19	Alignment marker insertion point	91.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-blocks immediately following am_rxmapped	M	Yes [ ]
RF20	FEC decoder detects FEC degraded SER at a programmable threshold	91.5.3.3.1		FDD:M	Yes [ ] N/A [ ]

116. Introduction to 200 Gb/s and 400 Gb/s networks

116.1 Overview

116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model

Change item h) in the lettered list in 116.1.2 as follows:

h) The MDIs as specified in Clause 121 for 200GBASE-DR4, in Clause 122 for 200GBASE-FR4 and 200GBASE-LR4, and in Clause 124 for 400GBASE-DR4, Clause 136 for 200GBASE-CR4, Clause 137 for 200GBASE-KR4, and Clause 138 for 200GBASE-SR4, all use a 4-lane data path.

116.1.3 Nomenclature

Insert the following rows at the beginning of Table 116-1:

Table 116–1—200 Gb/s PHYs

Name	Description
200GBASE-KR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of an electrical backplane (see Clause 137)
200GBASE-CR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of twinaxial copper cable (see 1.4.480 and Clause 136)
200GBASE-SR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of multimode fiber (see Clause 138)

116.1.4 Physical Layer signaling systems

Change the first paragraph in 116.1.4 as follows:

This standard specifies a family of Physical Layer implementations. Table 116–2a, Table 116–3, and Table 116–4 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types must meet the requirements of the corresponding clauses.

Insert Table 116-2a after Table 116-2:

Table 116–2a—PHY type and clause correlation (200GBASE copper)

PHY type	Clause[a]										
	73	78	117		118	119	120	120B	120D	136	137
	Auto-Negotiation	EEE	RS	200GMII	200GMII Extender	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	200GBASE-CR4 PMD	200GBASE-KR4 PMD
200GBASE-KR4	M	O	M	O	O	M	M	O	O		M
200GBASE-CR4	M	O	M	O	O	M	M	O	O	M	

[a]O = Optional, M = Mandatory.

Change Table 116-3 as shown:

Table 116–3—PHY type and clause correlation (200GBASE optical)

PHY type	Clause[a]													
	78	117		118	119	120	120B	120C	120D	120E	121	122	122	138
	EEE	RS	200GMII	200GMII Extender	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-8 C2M	200GAUI-4 C2C	200GAUI-4 C2M	200GBASE-DR4 PMD	200GBASE-FR4 PMD	200GBASE-LR4 PMD	200GBASE-SR4 PMD
200GBASE-SR4	O	M	O	O	M	M	O	O	O	O				M
200GBASE-DR4	O	M	O	O	M	M	O	O	O	O	M			
200GBASE-FR4	O	M	O	O	M	M	O	O	O	O		M		
200GBASE-LR4	O	M	O	O	M	M	O	O	O	O			M	

[a]O = Optional, M = Mandatory.

116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers

116.2.5 Physical Medium Dependent (PMD) sublayer

Change the second paragraph in 116.2.5 as shown:

The 200GBASE-R PMDs and their corresponding media are specified in Clause 121, ~~and~~ Clause 122, and Clause 136 through Clause 138. The 400GBASE-R PMDs and their corresponding media are specified in Clause 122 through Clause 124.

116.4 Delay constraints

Change Table 116-5 as shown (some unchanged rows not shown):

Table 116–5—Sublayer delay constraints (200GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
…				
200GBASE-R PMA	18 432	36	92.16	See 120.5.4.
200GBASE-KR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
200GBASE-CR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through cable medium. See 137.5.
200GBASE-SR4 PMD	4 096	8	20.48	See 138.3.
200GBASE-DR4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 121.3.1.
…				

[a] For 200GBASE-R, 1 bit time (BT) is equal to 5 ps. (See 1.4.160 for the definition of bit time.)
[b] For 200GBASE-R, 1 pause_quantum is equal to 2.56 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

119. Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R

Insert 119.5a after 119.5:

119.5a Auto-Negotiation

The following requirements apply to a PCS used with a 200GBASE-CR4 or 200GBASE-KR4 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the AN_LINK.indication(link_status) primitive (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

119.6 Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R[4]

119.6.4 PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R

Insert 119.6.4.12 after 119.6.4.11:

119.6.4.12 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 200GBASE-CR4 or 200GBASE-KR4 PMD	119.5a	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	119.5a	Support of the AN_LINK.indication(link_status) primitive	AN:M	Yes [ ] N/A [ ]
AN2	link_status parameter	119.5a	Takes the value OK or FAIL, as described in 119.5a	AN:M	Yes [ ] N/A [ ]
AN3	Generation of AN_LINK.indication primitive	119.5a	Generated when the value of link_status changes	AN:M	Yes [ ] N/A [ ]

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120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R

120.5 Functions within the PMA

Change the title for 120.5.7, and insert a new subclause number (120.5.7.1) immediately afterward as shown (note that the text of the former 120.5.7 is now in 120.5.7.1):

120.5.7 PAM4 Encoding ~~Gray mapping for PAM4 encoded lanes~~

120.5.7.1 Gray mapping for PAM4 encoded lanes

Insert 120.5.7.2 after 120.5.7.1:

120.5.7.2 Precoding for PAM4 encoded lanes

For PMA lanes connected to the PMD service interface of a 200GBASE-CR4 or 200GBASE-KR4 PMD, the PMA shall provide 1/(1+D) mod 4 precoding capability on each transmit lane and may optionally provide 1/(1+D) mod 4 decoding capability on each receive lane. Precoding is implemented as specified in 135.5.7.2.

The precoder is enabled independently on the Tx output (toward the PMD) and the Rx input (from the PMD) on each lane (0, 1, 2, and 3). Precoding is enabled and disabled using variables precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* (where *i* is 0, 1, 2, or 3).

If a Clause 45 MDIO is implemented, the variables precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* are accessible through register 1.600 and 1.601 (see 45.2.1.132a and 45.2.1.132b).

The variables precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* shall be set as determined by the PMD control function on lane *i* (see 136.8.11.7.5). The method by which the PMD control function affects these variables is implementation dependent.

120.6 PMA MDIO function mapping

Change Table 120–3 as shown (some unchanged rows not shown):

Table 120–3—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 0 Tx output precoder enable	PMA precoder control Tx output	1.600.0	precoder_tx_out_enable_0
Lane 1 Tx output precoder enable	PMA precoder control Tx output	1.600.1	precoder_tx_out_enable_1

Table 120–3—MDIO/PMA control variable mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
Lane 2 Tx output precoder enable	PMA precoder control Tx output	1.600.2	precoder_tx_out_enable_2
Lane 3 Tx output precoder enable	PMA precoder control Tx output	1.600.3	precoder_tx_out_enable_3
Lane 0 Rx input precoder enable	PMA precoder control Rx input	1.601.0	precoder_rx_in_enable_0
Lane 1 Rx input precoder enable	PMA precoder control Rx input	1.601.1	precoder_rx_in_enable_1
Lane 2 Rx input precoder enable	PMA precoder control Rx input	1.601.2	precoder_rx_in_enable_2
Lane 3 Rx input precoder enable	PMA precoder control Rx input	1.601.3	precoder_rx_in_enable_3
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
…			

120.7 Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R[5]

Insert 120.7.7 after 120.7.6:

120.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
*CKR4	PMA is adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD.	120.5.7.2		O	Yes [ ] No [ ]
E1	PMA supports Tx precoding	120.5.7.2		CKR4:M	Yes [ ] N/A [ ]
E2	PMA supports Rx precoding	120.5.7.2		CKR4:O	Yes [ ] No [ ] N/A [ ]

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Insert Clause 131 to Clause 140 in numeric order (see later in this amendment for the addition of corresponding annexes):

131. Introduction to 50 Gb/s networks

131.1 Overview

131.1.1 Scope

This clause describes the general requirements for 50 Gigabit Ethernet.

50 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 50 Gb/s, coupled with any IEEE 802.3 50GBASE Physical Layer implementation and is defined for full duplex operation only.

50 Gb/s Physical Layer entities, such as those specified in Table 131–1, provide a frame loss ratio (see 1.4.275) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

131.1.2 Relationship of 50 Gigabit Ethernet to the ISO OSI reference model

50 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 50 Gb/s Physical Layers. The relationships among 50 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 131–1.

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The 50GMII, which, when implemented as logical interconnection point between the MAC sublayer and the Physical Layer (PHY), uses a 64-bit-wide data path as specified in Clause 132. Physical instantiations of this interface may use other data-path widths.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as LAUI-2, as specified in Annex 135B and Annex 135C, or as 50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface), as specified in Annex 135D and Annex 135E, at an observable interconnection port, uses a two-lane data path.

d) The PMA service interface, which, when physically implemented as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a one-lane data path as specified in Annex 135F or Annex 135G.

e) The MDI as specified in Clause 136 for 50GBASE-CR, Clause 137 for 50GBASE-KR, Clause 138 for 50GBASE-SR, and Clause 139 for 50GBASE-FR and 50GBASE-LR uses a one-lane data path.

131.1.3 Nomenclature

The nomenclature employed by the 50 Gb/s Physical Layer is explained as follows.

The alpha-numeric prefix 50GBASE in the port type (e.g., 50GBASE-R) represents a family of Physical Layer devices operating at a speed of 50 Gb/s.

50GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) for 50 Gb/s operation over multiple PCS lanes (see Clause 133). Physical Layer devices listed in Table 131–1 are defined for operation at 50 Gb/s.

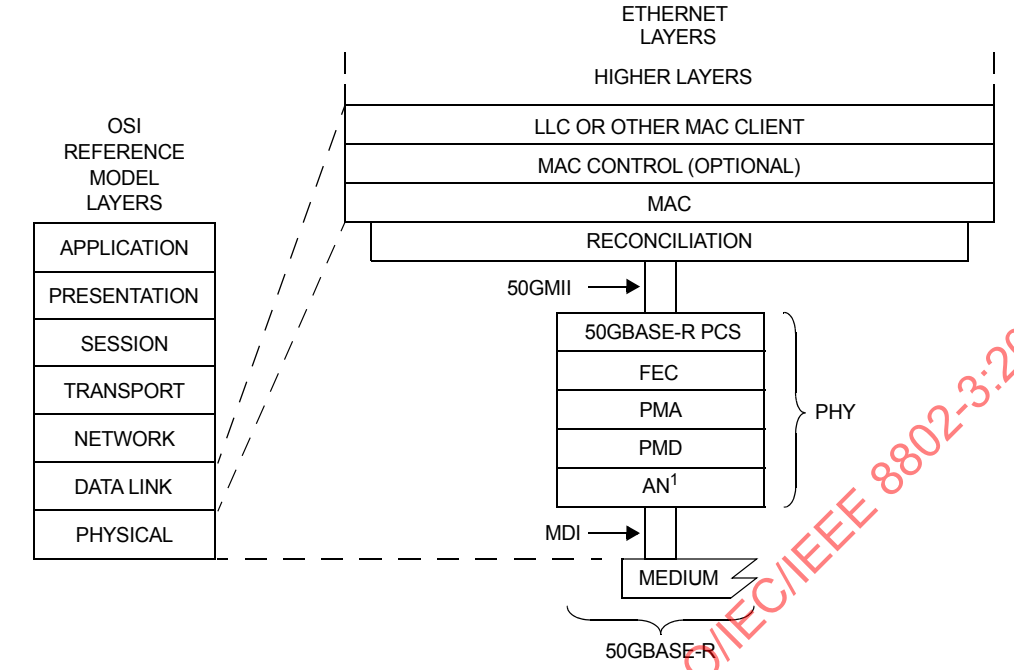


Figure 131–1—Architectural positioning of 50 Gigabit Ethernet

Table 131–1—50 Gb/s PHYs

Name	Description
50GBASE-KR	50 Gb/s PHY using 50GBASE-R encoding over an electrical backplane (see Clause 137).
50GBASE-CR	50 Gb/s PHY using 50GBASE-R encoding over twinaxial copper cable (see 1.4.480 and Clause 136).
50GBASE-SR	50 Gb/s PHY using 50GBASE-R encoding over multimode fiber (see Clause 138).
50GBASE-FR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 2 km (see Clause 139).
50GBASE-LR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 10 km (see Clause 139).

131.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 131–2 and Table 131–3 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types must meet the requirements of the corresponding clauses.

Table 131–2—PHY types and clause correlation (50GBASE copper)

PHY type	Clause[a]											
	73	78	132		133	134	135	135B	135D	135F	136	137
	Auto-Negotiation	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-CR PMD	50GBASE-KR PMD
50GBASE-KR	M	O	M	O	M	M	M	O	O	O		M
50GBASE-CR	M	O	M	O	M	M	M	O	O	O	M	

[a]O = Optional, M = Mandatory.

Table 131–3—PHY types and clause correlation (50GBASE optical)

PHY type	Clause[a]														
	78	132		133	134	135	135B	135C	135D	135E	135F	135G	138	139	
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	LAUI-2 C2M	50GAUI-2 C2C	50GAUI-2 C2M	50GAUI-1 C2C	50GAUI-1 C2M	50GBASE-SR PMD	50GBASE-FR PMD	50GBASE-LR PMD
50GBASE-SR	O	M	O	M	M	M	O	O	O	O	O	O	M		
50GBASE-FR	O	M	O	M	M	M	O	O	O	O	O	O		M	
50GBASE-LR	O	M	O	M	M	M	O	O	O	O	O	O			M

[a]O = Optional, M = Mandatory.

131.2 Summary of 50 Gigabit Ethernet sublayers

131.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (50GMII)

The Media Independent Interface specified in Clause 132 provides a logical interconnection between the MAC sublayer and Physical Layer entities (PHY). The Media Independent Interface is not intended to be physically instantiated, rather it can logically connect layers within a device.

The 50GMII supports 50 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the 50GMII and the MAC/PLS service definition.

While the 50GMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for the physical coding sublayer defined in Clause 133.

131.2.2 Physical Coding Sublayer (PCS)

50GBASE-R PHYs use the PCS specified in Clause 133. The 50GBASE-R PCS performs encoding of data from the 50GMII to 64B/66B code blocks and transfers the encoded data to the PMA (or FEC) and performs decoding of 64B/66B blocks from the PMA (or FEC) and transfers the decoded data to the 50GMII.

131.2.3 Forward Error Correction (FEC) sublayer

50GBASE-R PHYs use the FEC sublayer specified in Clause 134. The FEC sublayer can be placed between the PCS and PMA sublayers or between two PMA sublayers.

131.2.4 Physical Medium Attachment (PMA) sublayer

The 50GBASE-R PMA specified in Clause 135 provides a medium-independent means for the PCS to support the use of a range of physical media.

The 50GBASE-R PMA performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, the mapping of transmit and receive data streams between the FEC and the PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test-pattern generation and checking.

131.2.5 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

The 50GBASE-R PMDs and their corresponding media are specified in Clause 136 through Clause 139.

131.2.6 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

131.2.7 Management

Managed objects, attributes, and actions are defined for all 50 Gigabit Ethernet components. These items are defined in Clause 30.

131.3 Service interface specification method and notation

The service interface specification for the 50GBASE-R Physical Layers is as per the definition in 1.2.2. Note that the 50GBASE-R inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as defined in 131.3.1 through 131.3.3.

131.3.1 Inter-sublayer service interface

The inter-sublayer service interface is defined in 116.3.1.

131.3.2 Instances of the Inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.

b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS or the FEC sublayer called the PMA service interface.

c) FEC:—for primitives issued on the interface between the FEC sublayer and the PCS or the PMA sublayer called the FEC service interface.

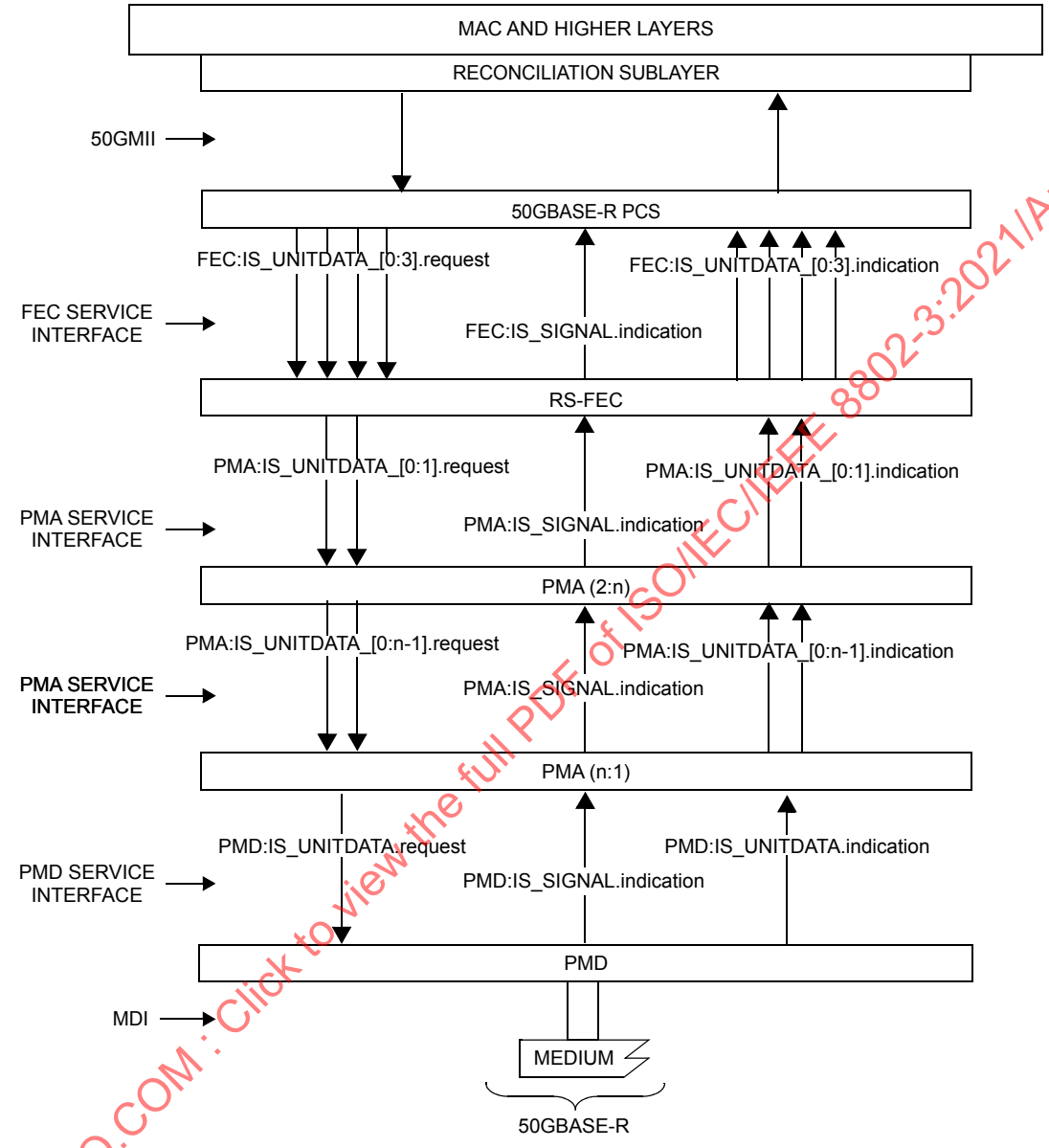
Examples of inter-sublayer service interfaces for 50GBASE-R with their corresponding instance names are illustrated in Figure 131–2. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication.

Primitives for other instances, of inter-sublayer interfaces, are represented in a similar manner as described above.

131.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 50GBASE-R sublayers are described in 116.3.3.1 through 116.3.3.3.



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS
n = 1 or 2

Figure 131–2—50GBASE-R inter-sublayer service interfaces

131.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 131–4 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2 for 50 Gigabit Ethernet. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Table 131–4—Sublayer delay constraints (50GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
50G MAC, RS, and MAC Control	16 384	32	327.68	See 132.1.4.
50GBASE-R PCS	11 264	22	225.28	See 135.3.
50GBASE-R RS-FEC	25 600	50	512	See 134.4.
50GBASE-R PMA	4 608	9	92.16	See 135.5.4.
50GBASE-KR PMD	2 048	4	40.96	See 137.5. Includes allocation of 20 ns for the medium.
50GBASE-CR PMD	2 048	4	40.96	See 136.5. Includes allocation of 20 ns for the medium.
50GBASE-SR PMD	1 024	2	20.48	Includes 2 m of fiber. See 138.3.1.
50GBASE-FR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.
50GBASE-LR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.

[a]For 50GBASE-R, 1 bit time is equal to 20 ps. (See 1.4.160 for the definition of bit time.)
[b]For 50GBASE-R, 1 pause_quantum is equal to 10.24 ns. (See 31B.2 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

See 80.4 for the calculation of bit time per meter of fiber or electrical cable.

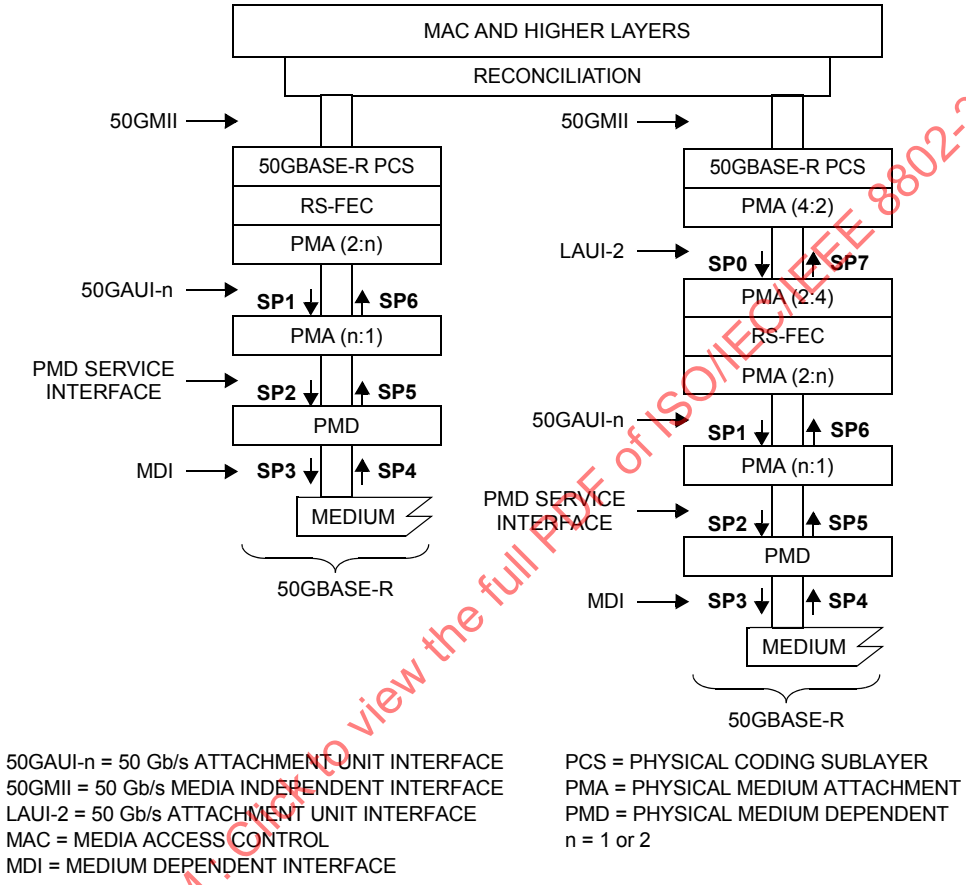
See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 50 Gb/s.

131.5 Skew constraints

Skew (or relative delay) can be introduced between lanes by both active and passive elements of a 50GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 133.2.3) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the lanes must be kept within limits as shown in Table 131–5 so that the transmitted information on the lanes can be reassembled by the receive PCS.

Skew Variation may be introduced due to variations in electrical, thermal or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation must be limited to ensure that each PCS lane always traverses the same lane between any pair of adjacent sublayers while the link remains in operation.

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP0, SP1, SP2, and SP3 for the transmit direction and SP4, SP5, SP6, and SP7 for the receive direction as illustrated in Figure 131–3.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
LAUI-2 = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 1 or 2

Figure 131–3—50GBASE-R Skew points

In the transmit direction, the Skew points are defined in the following locations:

— SP0 on the LAUI-2 interface, at the input of the PMA above the RS-FEC;
— SP1 on the 50GAUI-n interface, at the input of the PMA closest to the PMD;
— SP2 on the PMD service interface, at the input of the PMD;
— SP3 at the output of the PMD, at the MDI.

In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD;
— SP5 on the PMD service interface, at the output of the PMD;
— SP6 on the 50GAUI-n interface, at the output of the PMA below the RS-FEC;
— SP7 on the LAUI-2 interface, at the output of the PMA above the RS-FEC.

The allowable limits for Skew are shown in Table 131–5 and the allowable limits for Skew Variation are shown in Table 131–6.

The Skew requirements for the PCS, PMA and PMD sublayers are specified in the respective clauses as noted in Table 131–5 and Table 131–6.

Table 131–5—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 50GBASE-R PCS lane (UI)[b]	Maximum Skew for 50GBASE-R FEC lane (UI)[c]	Notes[d]
SP0	29	≈ 374	N/A	See 135.5.3.1
SP1	29	N/A	≈ 770	See 135.5.3.3
SP2	43	N/A	≈ 1142	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP3	54	N/A	≈ 1434	See 136.6, 137.6, 138.3.2, 139.3
SP4	134	N/A	≈ 3559	See 136.6, 137.6, 138.3.2, 139.3
SP5	145	N/A	≈ 3852	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP6	160	N/A	≈ 4250	See 135.5.3.7
SP7	29	≈ 374	N/A	See 135.5.3.8
At FEC transmit	49	N/A	≈ 1302	See 134.5.2.2
At FEC receive	180	N/A	≈ 4781	See 134.5.2.2
At PCS receive	49	≈ 632	N/A	See 133.2.3

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 77.5758 ps at PCS lane signaling rate of 12.890625 Gb/s.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.6471 ps at FEC lane signaling rate of 26.5625 Gb/s.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

Table 131–6—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 25.78125 GBd lane (UI)[a]	Maximum Skew Variation for 26.5625 GBd lane (UI)[b]	Notes[c]
SP0	0.2	≈ 5	N/A	See 135.5.3.1
SP1	0.2	N/A	≈ 5	See 135.5.3.3
SP2	0.4	N/A	≈ 11	See 135.5.3.5
SP3	0.6	N/A	≈ 16	
SP4	3.4	N/A	≈ 90	
SP5	3.6	N/A	≈ 96	See 135.5.3.6
SP6	3.8	N/A	≈ 101	See 135.5.3.7
SP7	0.2	≈ 6	N/A	See 135.5.3.8
At FEC transmit	0.4	N/A	≈ 11	See 134.5.2.2
At FEC receive	4	N/A	≈ 106	See 134.5.2.2
At PCS receive	0.4	≈ 10	N/A	See 133.2.3

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 38.7879 ps at LAUI-2 lane signaling rate of 25.78125 GBd.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 37.6471 ps at 50GAUI-2 lane signaling rate of 26.5625 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

131.6 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow must connect to the shared arrow, and the qualifier must be met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

131.7 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 132 through Clause 140, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 50 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

132. Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the Media Independent Interface between Ethernet media access controllers and various PHYs. Figure 132–1 shows the relationship of the RS and Media Independent Interface to the ISO/IEC OSI reference model. The 50 Gb/s RS has identical logical functionality to the 40 Gb/s RS defined in Clause 81.

The 50GMII is an optional logical interface between the MAC sublayer and the Physical Layer (PHY).

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 50GMII is an optional interface, it is used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the 50GMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and 50GMII were implemented.

The 50GMII has the following characteristics:

a) The 50GMII supports a speed of 50 Gb/s.
b) Data and delimiters are synchronous to a clock reference.
c) It provides independent 64-bit-wide transmit and receive data paths.
d) It supports full duplex operation only.

132.1.1 Summary of major concepts

The following are the major concepts of the 50GMII:

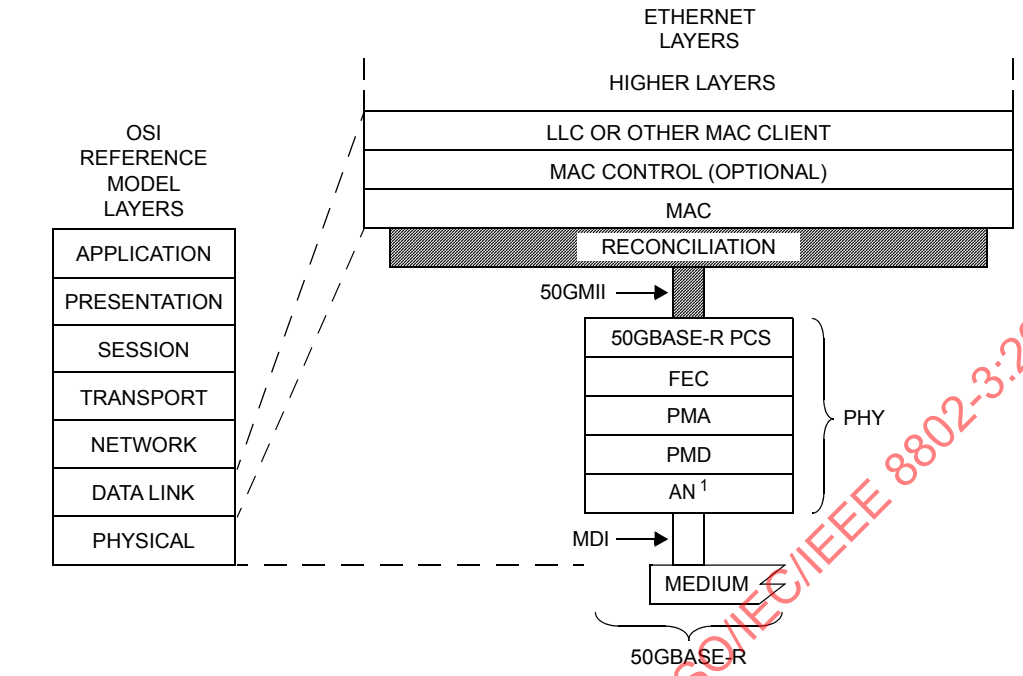
a) The 50GMII is functionally similar to other media independent interfaces that have been defined for other speeds, as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the 50GMII.
c) The RS maps the signal set provided at the 50GMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) The 50GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy-Efficient Ethernet (EEE) (see Clause 78).

132.1.2 Application

This clause applies to the interface between the MAC and PHY. This logical interface is used to provide media independence so that an identical media access controller may be used with all 50GBASE PHY types.

132.1.3 Rate of operation

The 50GMII is specified to support 50 Gb/s operation.



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 132–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

132.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 132–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

Table 132–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50 Gb/s MAC, RS, and MAC Control	16 384	32	327.68

132.1.5 Allocation of functions

The allocation of functions at the 50GMII balances the need for media independence with interface simplicity. The 50GMII maximizes media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

132.1.6 50GMII structure

The 50GMII structure is identical to the XLGMII/CGMII structure specified in 81.1.7.

132.1.7 Mapping of 50GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 50GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 50 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 50GMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 132.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 50 Gb/s:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

The RS maps all primitives in an identical manner as the XLGMII/CGMII does and as specified in 81.1.7.

132.2 50GMII data stream

The 50GMII data stream has the same characteristics as the XLGMII/CGMII data stream described in 81.2.

132.3 50GMII functional specifications

The 50GMII functions identically to the XLGMII/CGMII specified in 81.3.

132.4 LPI assertion and detection

LPI assertion and detection function identically to the XLGMII/CGMII specified in 81.4, with the single exception that the PMA stop signaling is not applicable.

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication in an identical manner to that defined in 81.4, with the single exception that the PMA stop signaling described in 81.4.4 is not applicable.

132.5 Protocol implementation conformance statement (PICS) proforma for Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation[6]

132.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

132.5.2 Identification

132.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

132.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

132.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of 50GMII	132.2		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of 50GMII	132.2		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	132.4		O	Yes [ ] No [ ]

132.5.3 PICS proforma tables for Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	132.1	Support MAC data rate of 50 Gb/s	PHY:M	Yes [ ] N/A [ ]
G2	Cumulative MAC Control, MAC, and RS round-trip delay	132.1.4	Per Table 132–1	RS:M	Yes [ ] N/A [ ]

132.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	132.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]

133. Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.1 Overview

133.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of 50 Gb/s Physical Layer implementations known as 50GBASE-R. The 50GBASE-R PCS is a sublayer of the 50 Gb/s PHYs listed in Table 131–1.

133.1.2 Relationship of 50GBASE-R to other standards

Figure 133–1 depicts the relationships among the 50GBASE-R sublayers, the Ethernet MAC and Reconciliation Sublayers, and the higher layers.

The 50GBASE-R PCS specifications are based on the 40GBASE-R PCS specifications in Clause 82, with the modifications listed in 133.2 and 133.3.

133.1.3 Summary of 50GBASE-R sublayers

Figure 133–1 shows the relationship of the 50GBASE-R PCS sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

133.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 50GMII, which is defined in Clause 132. The 50GMII provides a uniform interface to the Reconciliation Sublayer for all 50 Gb/s PHY implementations

The 50GBASE-R PCS provides all services required by the 50GMII.

133.1.4 Inter-sublayer interfaces

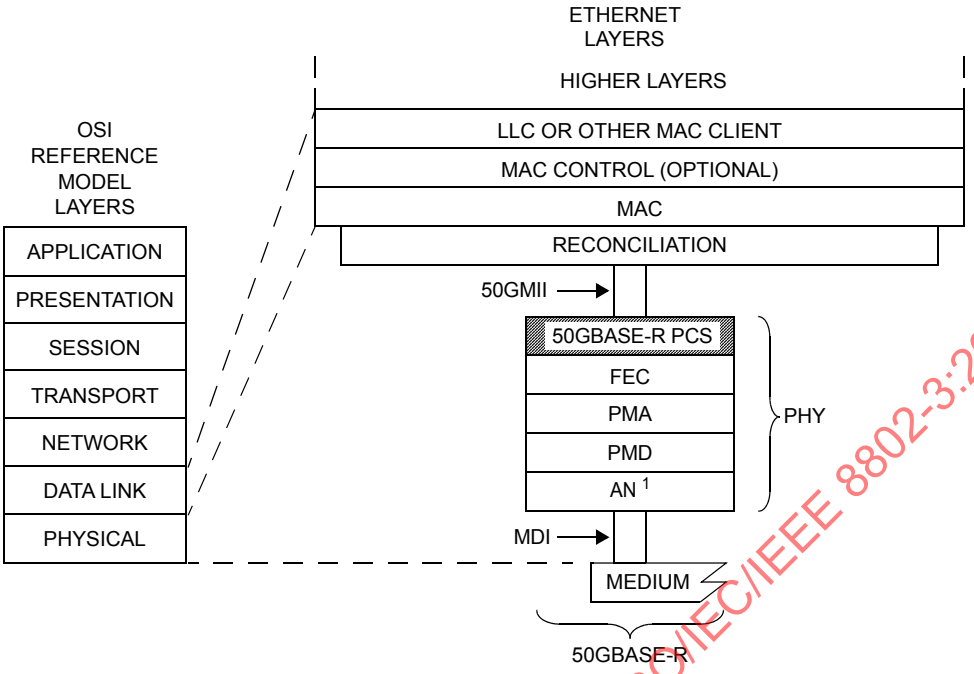
The upper interface of the PCS may connect to the Reconciliation Sublayer through the 50GMII.

The lower interface of the PCS connects to the FEC sublayer. If the optional LAUI-2 interface (see 135B.1 and 135C.1) is physically instantiated directly below the PCS sublayer, then the lower interface of the PCS instead connects to the PMA. The 50GBASE-R PCS is based on 4 PCS lanes and has a nominal rate at the FEC or PMA service interface of 12.890625 Gb/s per PCS lane, which provides capacity for the MAC data rate of 50 Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

133.1.4.1 PCS service interface (50GMII)

The PCS service interface allows the 50GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is defined as the 50GMII in Clause 132.



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
FEC = FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 133–1—50GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

133.1.4.2 Forward Error Correction (FEC) or Physical Medium Attachment (PMA) service interface

The FEC or PMA service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The FEC or PMA Service Interface supports the exchange of encoded data between the PCS and the FEC or PMA sublayer. The FEC service interface is defined in 134.2. The PMA service interface is defined in 135.3.

133.1.5 Functional block diagram

Figure 133–2 provides a functional block diagram of the 50GBASE-R PCS.

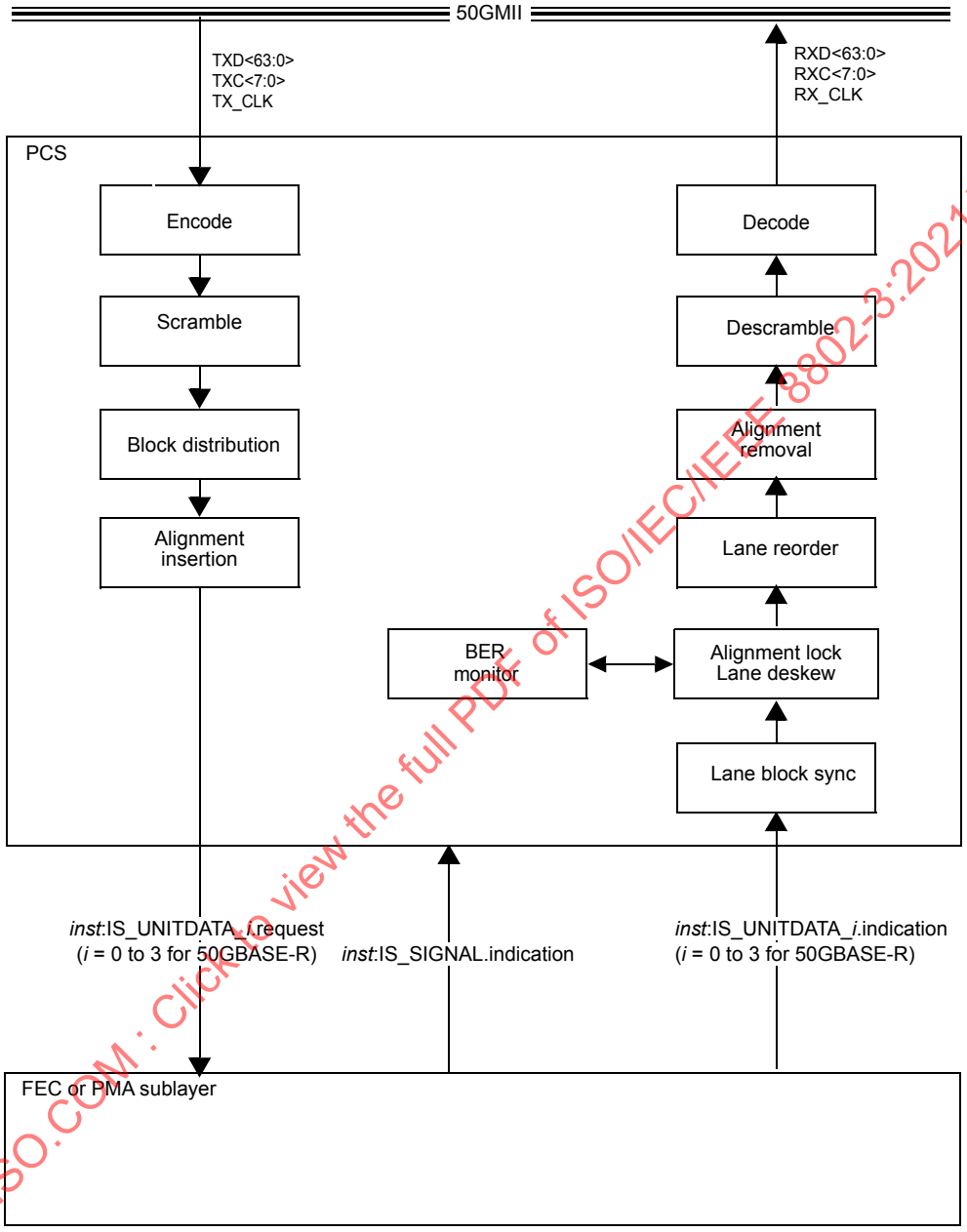


Figure 133–2—50GBASE-R PCS functional block diagram

133.2 Physical Coding Sublayer (PCS)

133.2.1 Functions within the PCS

The 50GBASE-R PCS shall have all of the functionality of the 40GBASE-R PCS specified in Clause 82 with the following exceptions:

a) The nominal rate at the FEC or PMA service interface is 12.890625 Gb/s per PCS lane, rather than 10.3125 Gb/s per PCS lane.

b) The alignment marker spacing is modified such that alignment markers are inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. (See 133.2.2.)

c) The definition of the variables current_am, am_counter, ber_cnt, and xus_timer in the state diagrams defined in 82.2.19 are modified to account for the different alignment marker spacing and the different data rate. (See 133.2.4.)

d) The optional deep sleep mode of EEE is not supported.

133.2.2 Alignment marker insertion

The alignment marker insertion for the 50GBASE-R PCS is identical to the alignment marker insertion for the 40GBASE-R PCS described in 82.2.7, with the exception that the alignment markers shall be inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. Alignment marker insertion is illustrated in Figure 133–3 and Figure 133–4.

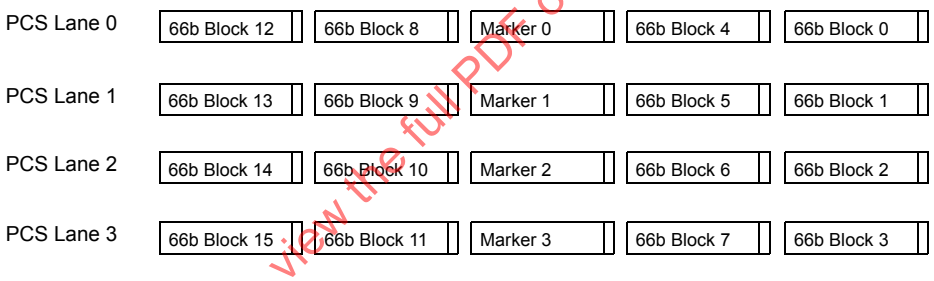


Figure 133–3—Alignment marker insertion

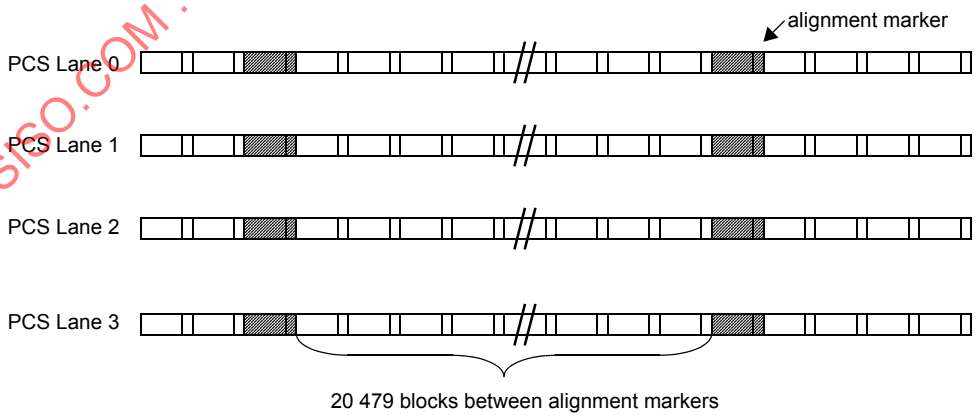


Figure 133–4—Alignment marker insertion period

The format of the 50GBASE-R PCS alignment markers is identical to the format of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Figure 82–9.

The content of the 50GBASE-R PCS alignment markers is identical to the content of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Table 82–3.

133.2.3 PCS lane deskew

The 50GBASE-R PCS receiver shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns.

Skew and Skew Variation are defined in 131.5.

133.2.4 Detailed functions and state diagrams

The state diagrams are identical to those for the 40GBASE-R PCS defined in 82.2.19 with the exception that some variables, counters and timers are redefined as follows:

current_am
: This variable holds the lane number of the current alignment marker. This is compared to the variable first_am to determine if we have alignment marker lock and is always n × 20 480 66-bit blocks away from the first_am.

am_counter
: This counter counts 66-bit blocks that separate two consecutive alignment markers. The terminal count is 20 479.

ber_cnt
: This counter counts up to a maximum of 97 of the number of invalid sync headers within the current 1 ms period.

xus_timer
: Timer that is triggered every 1 ms +1%, –25%.

133.3 Delay constraints

The maximum delay contributed by the 50GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 11 264 bit times (22 pause_quanta or 225.28 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

133.4 Auto-Negotiation

The following requirements apply to a PCS used with a 50GBASE-CR or 50GBASE-KR PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

133.5 Protocol implementation conformance statement (PICS) proforma for Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R[7]

133.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

133.5.2 Identification

133.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

133.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[7] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

133.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS	Supports 50GBASE-R PCS functionality	133.1.1		M	Yes [ ]
XGE50	50GMII logical interface	132, 133.1.4	Logical interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	45, 82.3	Registers and interface supported	O	Yes [ ] No [ ]
PMA	Supports operation directly connected to a PMA	133.1.4.2		O.1	Yes [ ] No [ ]
FEC	Supports operation directly connected to an FEC sublayer	133.1.4.2		O.1	Yes [ ] No [ ]
*JTM	Supports test-pattern mode	82.2.1		PMA:M	Yes [ ] N/A[ ]

133.5.4 PICS proforma tables for Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.5.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	82.2.3.3		M	Yes [ ]
C4	Invalid block types are treated as an error	82.2.3.3		M	Yes [ ]
C5	Only valid control characters are transmitted	82.2.3.4		M	Yes [ ]
C6	Invalid control characters are treated as an error	82.2.3.4		M	Yes [ ]
C7	Idles do not interrupt data	82.2.3.6		M	Yes [ ]
C8	IDLE control code insertion and deletion	82.2.3.6	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	82.2.3.9	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

133.5.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	82.2.5	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	82.2.16	Performs as shown in Figure 49–10	M	Yes [ ]

133.5.4.3 Deskew and Reordering

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Deskew	82.2.13, 133.2.3	Able to deskew up to the value in 133.2.3.	M	Yes [ ]
DR2	Reordering	82.2.14	Performs reordering.	M	Yes [ ]

133.5.4.4 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	133.2.2	Alignment markers are inserted periodically as described in section 133.2.2	M	Yes [ ]
AM2	Alignment marker format	133.2.2	Alignment markers are formed as described in Figure 82–9 and Table 82–3	M	Yes [ ]
AM3	Lane mapping	82.2.19.3	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]

133.5.4.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	82.2.11	Performs as in 82.2.11	JTM:M	Yes [ ] N/A[ ]
JT2	Scrambled idle receive test-pattern checker is implemented	82.2.18	Performs as in 82.2.18	JTM:M	Yes [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	82.2.1		JTM:M	Yes [ ] N/A[ ]

133.5.4.6 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	133.2.1, 82.2.3.2	Placement of bits into the PCS lanes as shown in Figure 82–3	M	Yes [ ]
B2	Receive bit order	133.2.1, 82.2.3.2	Placement of bits into the 50GMII as shown in Figure 82–4	M	Yes [ ]

133.5.4.7 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to PCS Management objects is provided	82.3		O	Yes [ ] No [ ]

133.5.4.8 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	50GBASE-R Block Lock	133.2.4	Implements 4 block lock processes as depicted in Figure 82–12	M	Yes [ ]
SM2	The SLIP function evaluates all possible bit positions	133.2.4		M	Yes [ ]
SM3	50GBASE-R Alignment Marker Lock	133.2.4	Implements 4 alignment marker lock processes as depicted in Figure 82–13	M	Yes [ ]
SM4	The AM_SLIP functions evaluates all possible blocks	133.2.4		M	Yes [ ]
SM5	50GBASE-R PCS deskew state diagram	133.2.4	Meets the requirements of Figure 82–14	M	Yes [ ]
SM6	50GBASE-R BER Monitor	133.2.4	Meets the requirements of Figure 82–15 with xus_timer_done set to 1 ms	M	Yes [ ]
SM7	50GBASE-R Transmit process	133.2.4	Meets the requirements of Figure 82–16	M	Yes [ ]
SM8	50GBASE-R Receive process	133.2.4	Meets the requirements of Figure 82–17	M	Yes [ ]

133.5.4.9 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	82.4	Performs as in 82.4	M	Yes [ ]
L2	When in loopback, transmits what it receives from the 50GMII	82.4	Performs as in 82.4	M	Yes [ ]

133.5.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	133.3	No more than 11 264 bit times for sum of transmit and receive path delays for 50GBASE-R	M	Yes [ ]

133.5.4.11 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 50GBASE-CR or 50GBASE-KR PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status)	AN:M	Yes [ ] N/A[ ]
AN2	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN:M	Yes [ ] N/A[ ]
AN2	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A[ ]

134. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.1 Overview

134.1.1 Scope

This clause specifies a Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs.

The RS-FEC sublayer for 50GBASE-R PHYs is identical to the RS-FEC sublayer for 100GBASE-R PHYs specified in Clause 91 with the following exceptions:

a) The service interface has four PCS lanes instead of 20 PCS lanes, and the nominal rate of each PCS lane is 12.890625 Gb/s rather than 5.15625 Gb/s. (See 134.2.)

b) It only implements the RS(544,514) Reed-Solomon encoder option defined in 91.5.2.7. (See 134.5.2.7.)

c) The output of the Reed-Solomon encoder is distributed to two FEC lanes, rather than the four FEC lanes described in 91.5.2.8.

d) The alignment marker processing is modified to account for the difference in the alignment marker format between the 50GBASE-R PCS (Clause 133) and the 100GBASE-R PCS (Clause 82), for the fact that the alignment markers are mapped to two FEC lanes rather than four FEC lanes, and the alignment marker mapping to the two FEC lanes needs to maintain a 10-bit alignment. (See 134.5.2.6.)

e) The definition of some of the variables and counters for the state diagrams in 91.5.4 are modified to support the different alignment marker spacing and the different number of FEC lanes. (See 134.5.4.)

f) The states identified as optional in the FEC synchronization state diagram in 91.5.4.3 (Figure 91–8) are mandatory for the 50GBASE-R RS-FEC.

g) The optional EEE deep sleep capability is not supported.

h) The optional FEC bypass correction feature (see 91.5.3.3) is not supported.

134.1.2 Position of RS-FEC in the 50GBASE-R sublayers

Figure 134–1 shows the relationship of the RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.

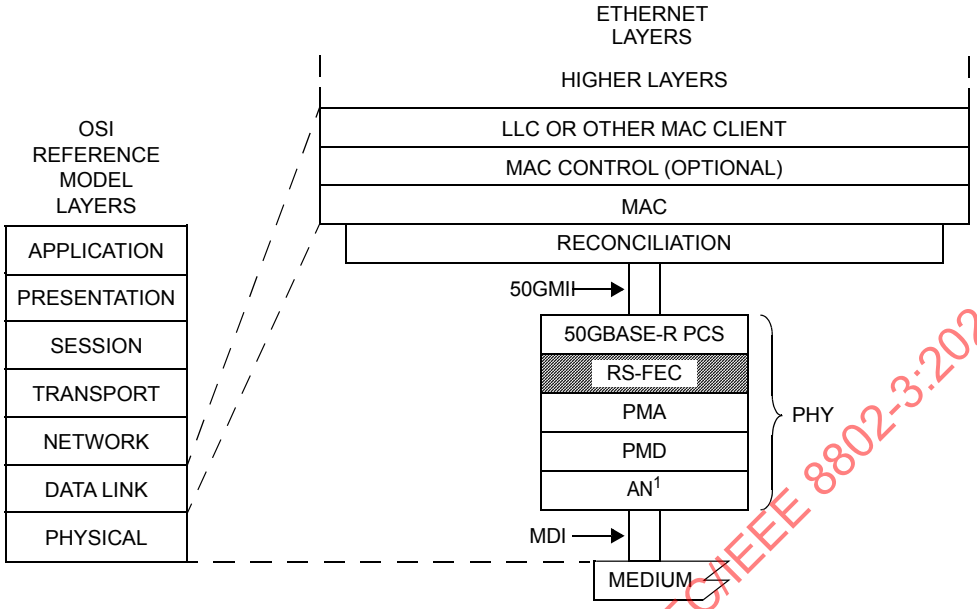
134.2 FEC service interface

This subclause specifies the services provided by the RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (see Annex 135B) in which case a PMA is the client of the FEC service interface.

The FEC service interface is an instance of the inter-sublayer service interface defined in 131.3. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
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LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 134–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The RS-FEC operates on four parallel bit streams, hence $i = 0$ to 3.

The PCS or PMA continuously sends four parallel bit streams to the RS-FEC, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s. The RS-FEC continuously sends four parallel bit streams to the PCS or PMA, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to false. When SIGNAL_OK is FAIL, the rx_symbol parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

134.3 PMA compatibility

The RS-FEC sublayer requires that the PMA service interface consist of exactly two upstream FEC lanes and exactly two downstream FEC lanes, with each lane running at a nominal signaling rate of 26.5625 Gb/s. Therefore, the RS-FEC sublayer may be a client of the 50GBASE-R PMA sublayer defined in Clause 135, when the PMA service interface width, *p*, is set to 2.

134.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 25 600 bit times (50 pause_quanta or 512 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

134.5 Functions within the RS-FEC sublayer

134.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 134–2.

134.5.2 Transmit function

134.5.2.1 PCS Lane block synchronization

The RS-FEC transmit function forms four bit streams by concatenating the bits from each of the four FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12, but using the variable definitions from 133.2.4.

134.5.2.2 PCS Alignment lock and deskew

Once the RS-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–13, but using the variable definitions from 133.2.4. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all four PCS lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14, but using the variable definitions from 133.2.4. The RS-FEC transmit function shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns. Skew and Skew Variation are defined in 131.5.

134.5.2.3 PCS Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The RS-FEC transmit function shall order the PCS lanes according to the PCS lane number.

134.5.2.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors result in am_lock being set to false for a given PCS lane, but until that happens it is sufficient to remove the block in the alignment marker position.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (see 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.233) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The bit error ratio in the data received from the local PCS can be estimated by dividing the BIP block error ratio by a factor of 1 351 680.

NOTE—The data received from the local PCS is processed by the RS-FEC transmit function without error correction.

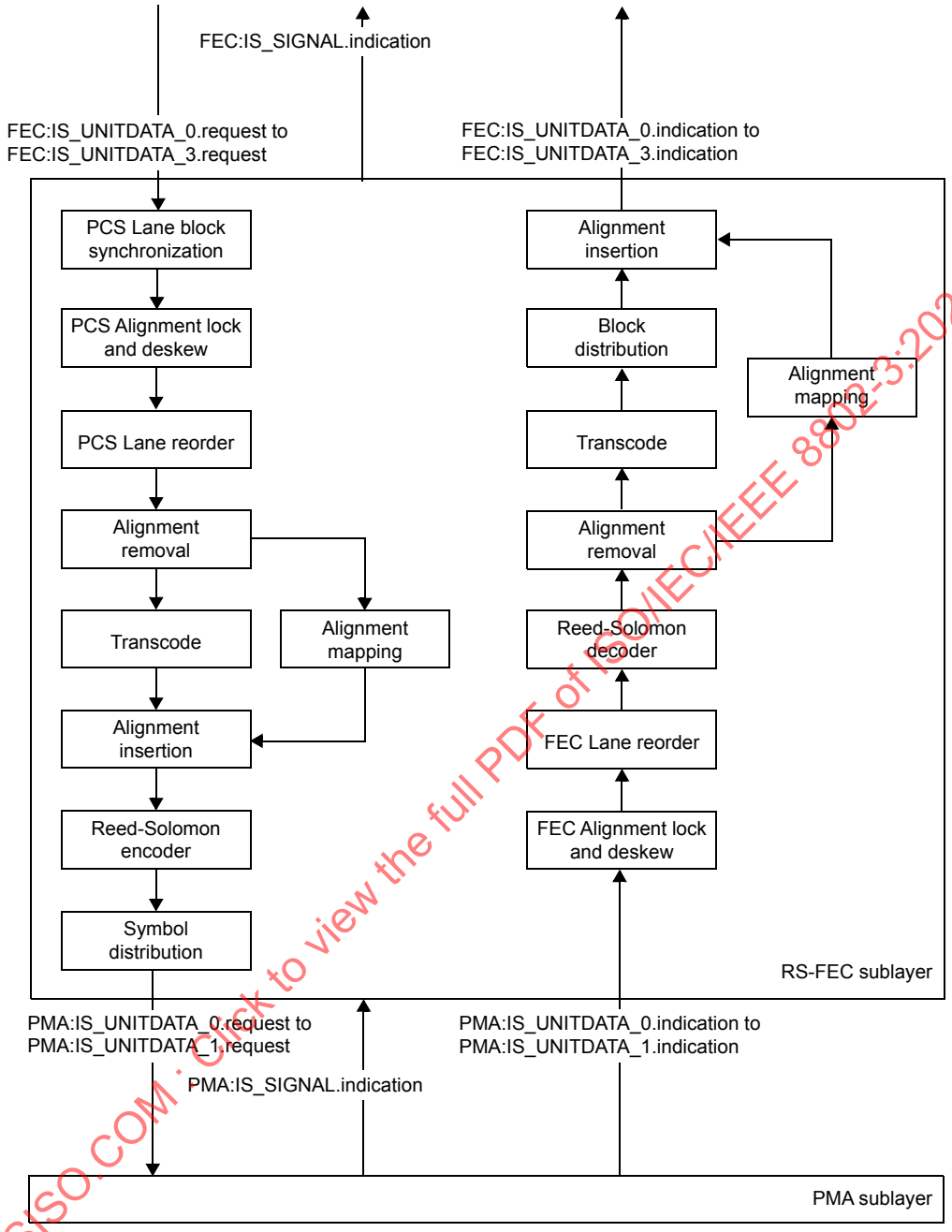


Figure 134–2—Functional block diagram

134.5.2.5 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.2.5.

134.5.2.6 Alignment marker mapping and insertion

The alignment markers that were removed per 134.5.2.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 134.5.2.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g., DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization at the receiver. The RS-FEC receive function uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface, to compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of four aligned and reordered alignment markers received from the PCS. Let am_tx_*x*<65:0> be the alignment marker for PCS lane *x*, *x*=0 to 3, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_txmapped<256:0> in a manner that yields the same result as the following process.

For *x*=0 to 3, amp_tx_*x*<63:0> is constructed as follows:

— Set $y = 0$ when $x \leq 1$, otherwise set $y = x$.
— amp_tx_*x*<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–3 for PCS lane number *y*.
— amp_tx_*x*<31:24> = am_tx_*x*<33:26>
— amp_tx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–3 for PCS lane number *y*.
— amp_tx_*x*<63:56> = am_tx_*x*<65:58>

This process replaces the fixed bytes of the alignment markers received from the PCS, possibly with errors, with the values from Table 82–3. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lane 1 with the fixed bytes for the alignment marker corresponding to PCS lane 0. The variable bytes of the alignment markers received from the PCS (BIP_3 and BIP_7) are unchanged. This simplifies the synchronization process at the RS-FEC receiver, as the receiver only needs to search for the fixed alignment marker bytes corresponding to PCS lane 0 on each FEC lane.

am_txpayloads<0,129:0> and am_txpayloads<1,125:0> are then constructed from amp_tx as follows:

— am_txpayloads<0, 63:0> = amp_tx_0<63:0>
— am_txpayloads<0, 127:64> = amp_tx_2<63:0>
— am_txpayloads<0, 129:128> = amp_tx_3<57:56>
— am_txpayloads<1, 63:0> = amp_tx_1<63:0>
— am_txpayloads<1, 119:64> = amp_tx_3<55:0>
— am_txpayloads<1, 125:120> = amp_tx_3<63:58>

This process is an intermediate step in the generation of am_txmapped<256:0>, and is illustrated in Figure 134–3.

Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_txmapped<255:0> is constructed from am_txpayloads as follows:

— If ($y < 25$) then am_txmapped<(10*y*+9):10*y*> = am_txpayloads<*i*, (10*k*+9):10*k*>
— am_txmapped<255:250> = am_txpayloads<1, 125:120>

A 1-bit pad is appended to the mapped alignment markers to yield the equivalent of one 257-bit block. The pad bit, am_txmapped<256>, shall be set to 0 or 1 in an alternating pattern.

am_txmapped<256:0> is inserted into the data path prior to the Reed-Solomon encoder (see Figure 134–4) every $4 \times 20\,480$ 66-bit blocks, corresponding to every 1024 Reed-Solomon codewords. The mapped alignment markers, am_txmapped<256:0> shall be inserted as the first 257 message bits to be transmitted every 1024th codeword. The first 257-bit block inserted after am_txmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective PCS lane.

The result of this alignment mapping process is that after Reed-Solomon encoding and symbol distribution (134.5.2.7 and 134.5.2.8 respectively), the alignment marker bit patterns shown in Figure 134–3 appear on the two FEC output lanes and aligned with the start of every 1024th FEC codeword. The FEC receiver uses this information to lock onto the two FEC lanes and to identify the FEC codeword boundaries.

An additional result of this alignment mapping process, is that the BIP_3 and BIP_7 fields from normal PCS alignment markers are carried across the link protected by FEC. These fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, i.e., following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

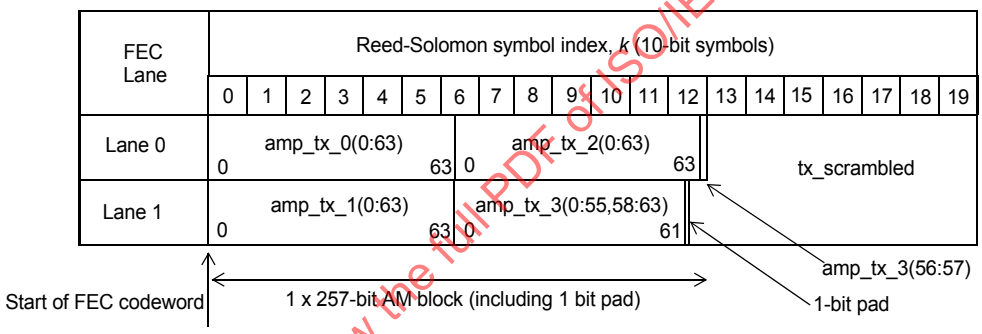


Figure 134–3—Alignment marker mapping to FEC lanes

134.5.2.7 Reed-Solomon encoder

The Reed-Solomon encoder is identical to the RS(544,514) Reed-Solomon encoder defined in 91.5.2.7.

134.5.2.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it is distributed to two FEC lanes, one 10-bit symbol at a time alternating between FEC lanes 0 and 1. The distribution process is shown in Figure 134–4.

134.5.2.9 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 134–4.

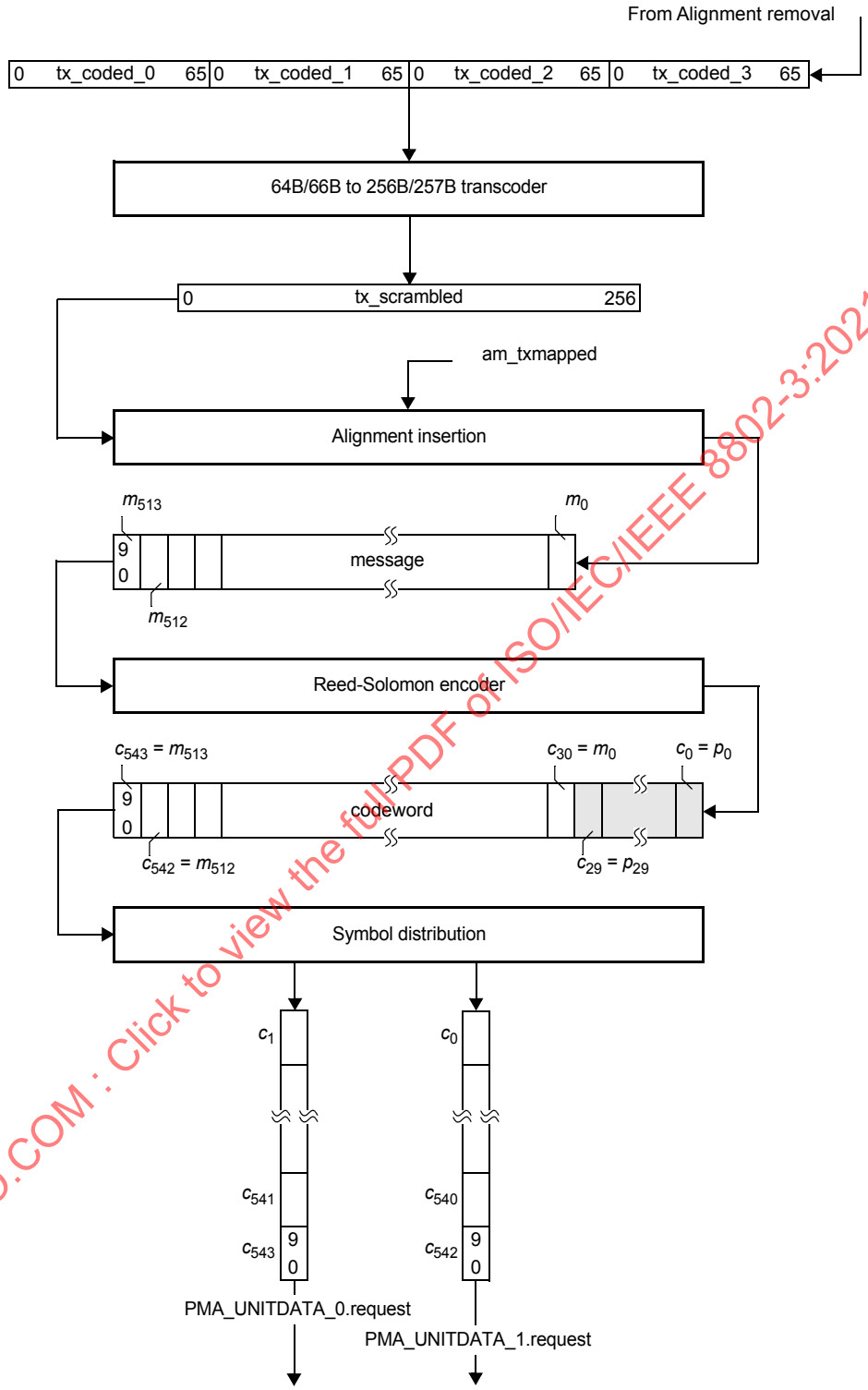


Figure 134–4—Transmit bit ordering

134.5.3 Receive function

134.5.3.1 Alignment lock and deskew

The RS-FEC receive function forms two bit streams by concatenating the bits from each of the two PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8, but using the variable definitions from 134.5.4.

After alignment marker lock is achieved on the two FEC lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

134.5.3.2 FEC Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 134.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After both FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

134.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-16}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors that were not corrected, it ensures that for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the 66-bit block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This causes the PCS to discard all frames 64 bytes and larger that are fully or partially contained within the codeword.

134.5.3.3.1 FEC Error indication bypass (optional)

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 134.6.6). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 134.6.1).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the

number of symbol errors in a block of 8192 codewords exceeds 6380, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber = true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

134.5.3.3.2 FEC Degraded SER (optional)

The Reed-Solomon decoder may optionally provide the ability to indicate a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 134.6.8). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 134.6.2).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the total number of symbol errors detected in consecutive non-overlapping blocks of FEC_degraded_SER_interval codewords (see 134.6.5). If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 134.6.3), the FEC_degraded_SER bit (see 134.6.9) is set. At the end of each interval, if the number of symbol errors is less than the threshold set in FEC_degraded_SER_deactivate_threshold (see 134.6.4), the FEC_degraded_SER bit is cleared. The value of the FEC_degraded_SER bit is unspecified if the value of FEC_degraded_SER_activate_threshold is less than the value of FEC_degraded_SER_deactivate_threshold.

If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is deasserted then the FEC_degraded_SER bit is cleared.

134.5.3.4 Alignment marker removal

The first 257 message bits in every 1024th codeword is the vector am_rxmapped<256:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (see 134.5.3.1).

The vector am_rxmapped shall be removed prior to transcoding.

134.5.3.5 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.3.5.

134.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to four PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

134.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of the lane reorder function (see 134.5.2.3) to derive the PCS lane alignment markers, am_rx_*x*<65:0> for *x*=0 to 3, from am_rxmapped<256:0> (see 134.5.3.4).

The alignment markers shall be derived from am_rxmapped<256:0> in a manner that yields the same result as the following process.

Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_rxpayloads is constructed from am_rxmapped as follows:

— If (*y* < 25) then am_rxpayloads<*i*, (10*k*+9):10*k*> = am_rxmapped<(10*y*+9):10*y*>

— am_rxpayloads<1, 125:120> = am_rxmapped<255:250>

The one bit pad am_rxmapped<256> is ignored by the receiver.

For *x*=0 to 3, amp_rx_*x*<63:0> is constructed from am_rxpayloads as follows:

— amp_rx_0<63:0> = am_rxpayloads<0, 63:0>

— amp_rx_1<63:0> = am_rxpayloads<1, 63:0>

— amp_rx_2<63:0> = am_rxpayloads<0, 127:64>

— amp_rx_3<55:0> = am_rxpayloads<1, 119:64>

— amp_rx_3<57:56> = am_rxpayloads<0, 129:128>

— amp_rx_3<63:58> = am_rxpayloads<1, 125:120>

For *x*=0 to 3, am_rx_*x*<65:0> is constructed as follows:

— am_rx_*x*<0>=1 and am_rx_*x*<1>=0.

— am_rx_*x*<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.

— am_rx_*x*<33:26> = amp_rx_*x*<31:24>.

— am_rx_*x*<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.

— am_rx_*x*<65:58> = amp_rx_*x*<63:56>

One vector is mapped to four alignment markers every 1024 Reed-Solomon codewords (see 134.5.3.4). The alignment markers are simultaneously transmitted on the four PCS lanes after every 20 479th column of four 66-bit blocks.

The alignment markers am_rx_0 to am_rx_3 shall be inserted so that they are immediately followed by rx_coded_0 to rx_coded_3, respectively, as derived from the first 257-bit block following am_rxmapped.

134.5.3.8 Receive bit ordering

The receive bit ordering is illustrated in Figure 134–5. This illustration shows the case where the FEC lanes appear across the PMA_IS_UNITDATA_*i*.indication primitives in the correct order.

134.5.4 Detailed functions and state diagrams

The state diagrams, including the associated definitions of variables, functions and counters, are identical to those for the 100GBASE-R RS-FEC sublayer defined in 91.5.4, with the exception that some of the variables and counters are redefined to account for the differences in alignment marker spacing and number of FEC lanes.

In addition, EEE optional deep sleep capability is not supported for 50GBASE-R PHYs and therefore any reference to the optional EEE deep sleep capability in 91.5.4 can be ignored.

134.5.4.1 State diagram conventions

The state diagram conventions are identical to those defined in 91.5.4.1.

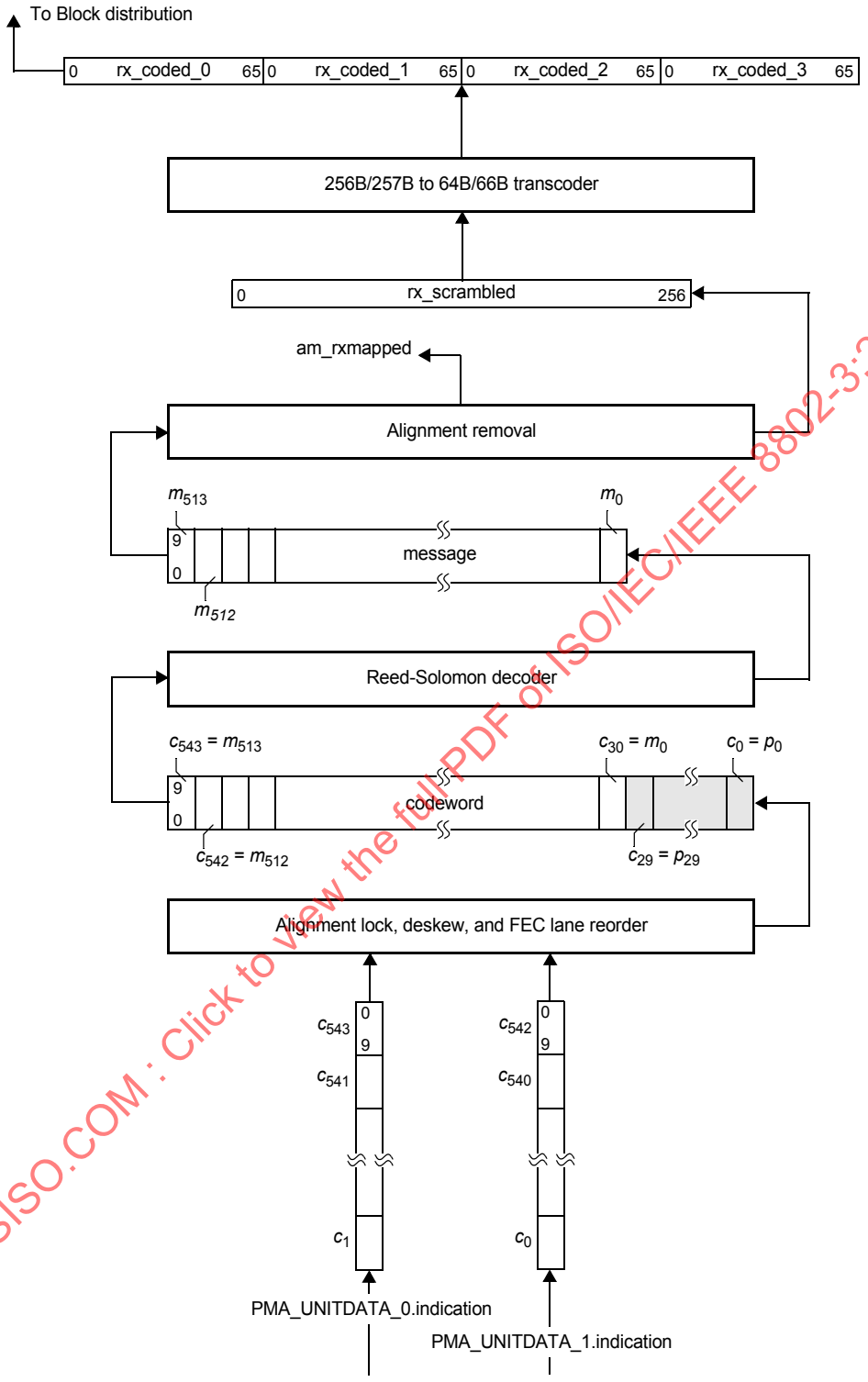


Figure 134–5—Receive bit ordering

134.5.4.2 State variables

134.5.4.2.1 Variables

This following variables are redefined from what is described in 91.5.4.2.1:

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 134.5.2.6, consists of 48 known bits and 16 variable bits (the BIP3 field and its complement BIP7 see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. Each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where *x* = 0:1.

fec_lane
: A variable that holds the FEC lane number (0 to 1) received on lane *x* of the PMA service interface when amps_lock<*x*> = true. The FEC lane number is determined by the alignment marker payloads in the 2nd position of the sequence based on the mapping defined in 134.5.2.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state diagrams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise. This variable shall always be set to true.

fec_optional_states
: Boolean variable that is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented.

134.5.4.2.2 Functions

The functions are identical to those defined in 91.5.4.2.2.

134.5.4.2.3 Counters

This following counters are redefined from what is described in 91.5.4.2.3:

amp_counter
: This counter counts the 1024 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. An FEC codeword is 2720 bits per FEC lane.

134.5.4.3 State diagrams

The state diagrams are identical to those defined in 91.5.4.3.

134.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 134–1, and MDIO status bits to RS-FEC status variables as shown in Table 134–2, and if a separated PMA (see 45.2.1) is connected to the FEC service interface (e.g., if the RS-FEC and PCS are separated via a LAUI-2 interface) it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 134–3.

Table 134–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
FEC degraded SER enable	RS-FEC control register	1.200.4	FEC_degraded_SER_enable
FEC degraded SER activate threshold	RS-FEC degraded SER activate threshold register	1.650, 1.651	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	RS-FEC degraded SER deactivate threshold register	1.652, 1.653	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	RS-FEC degraded SER interval register	1.654, 1.655	FEC_degraded_SER_interval

Table 134–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC degraded SER ability	RS-FEC status register	1.201.3	FEC_degraded_SER_ability
FEC degraded SER	RS-FEC status register	1.201.4	FEC_degraded_SER
FEC optional states supported	RS-FEC status register	1.201.7	fec_optional_states
FEC AM lock *x*, *x*=0 to 1	RS-FEC status register	1.201.8:9	amps_lock<*x*>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC symbol errors, FEC lanes 0 to 1	RS-FEC symbol error counter register, FEC lanes 0 to 1	1.210 to 1.213	FEC_symbol_error_counter_*i*

Table 134–3—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status
BIP errors, PCS lanes 0 to 3	RS-FEC BIP error counter register, PCS lanes 0 to 3	1.230 to 1.233	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.253	lane_mapping<*x*>
Block *x* lock	RS-FEC PCS alignment status 1 register	1.280	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status 3 register	1.282	am_lock<*x*>

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

134.6.1 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 134.5.3.3.1) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.110.2 (1.200.1).

134.6.2 FEC_degraded_SER_enable

This variable enables the FEC decoder to indicate the presence of a degraded SER when the ability is supported (see 134.5.3.3.2). When set to a one, this variable enables degraded SER detection. When set to a zero, degraded SER detection is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER. This variable is mapped to the bit defined in 45.2.1.110.a (1.200.4).

134.6.3 FEC_degraded_SER_activate_threshold

This variable controls the threshold used to set the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in 45.2.1.132h (1.650, 1.651).

134.6.4 FEC_degraded_SER_deactivate_threshold

This variable controls the threshold used to clear the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in 45.2.1.132i (1.652, 1.653).

134.6.5 FEC_degraded_SER_interval

This variable controls the interval used to set and clear the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in 45.2.1.132j (1.654, 1.655).

134.6.6 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 134.5.3.3.1) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.111.9 (1.201.1).

134.6.7 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 134.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.111.8 (1.201.2).

134.6.8 FEC_degraded_SER_ability

The FEC decoder may have the option to indicate the presence of a degraded SER (see 134.5.3.3.2). This variable is set to one to indicate that the FEC decoder has the ability to indicate the presence of a degraded SER. This variable is set to zero if this ability is not supported. It is mapped to the bit defined in 45.2.1.111.7b (1.201.3).

134.6.9 FEC_degraded_SER

When FEC_degraded_SER_enable is asserted, this variable indicates the presence of a degraded SER as defined in 134.5.3.3.2. This variable is mapped to the bit defined in 45.2.1.111.7a (1.201.4).

134.6.10 fec_optional_states

This variable is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented. This variable is mapped to the bit defined in 45.2.1.111.7a (1.201.7).

134.6.11 amps_lock<*x*>

These variables are assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3 and 134.5.4). They are mapped to the bits defined in 45.2.1.111 (1.201.8 to 1.201.9 for FEC lanes 0 to 1, respectively).

134.6.12 fec_align_status

This variable assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). It is mapped to the bit defined in 45.2.1.111.2 (1.201.14).

134.6.13 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.103 (1.202, 1.203).

134.6.14 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors that were not corrected.

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.104 (1.204, 1.205).

134.6.15 FEC_lane_mapping<*x*>

When the RS-FEC receive function detects and locks to an alignment marker payload on PMA service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable FEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.105 (1.206).

134.6.16 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i*, where *i*=0 to 1, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.106 and 45.2.1.107 (1.210 to 1.213).

134.6.17 align_status

This variable is assigned the value of rx_align_status as defined by the PCS deskew state diagram shown in Figure 82–14 (see 134.5.2.2). It is mapped to the bit defined in 45.2.1.111.1 (1.201.15).

134.6.18 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i*=0 to 3, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC transmit function (see 134.5.2.4). These variables are mapped to the registers defined in 45.2.1.117 and 45.2.1.109 (1.230 to 1.233).

134.6.19 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.110 and 45.2.1.111 (1.250 to 1.253).

134.6.20 block_lock<*x*>

These variables are assigned by the block lock state diagram shown in Figure 82–12 (see 134.5.2.1). They are mapped to the registers defined in 45.2.1.112 (1.280).

134.6.21 am_lock<*x*>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–13 (see 134.5.2.2). They are mapped to the registers defined in 45.2.1.114 (1.282).

134.7 Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs[8]

134.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

134.7.2 Identification

134.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

134.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[8] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

134.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RS-FEC	Supports 50GBASE-R RS-FEC functionality	134.1.1		M	Yes [ ]
*MD	MDIO capability	45, 134.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	134.5.3.3.1	Capability is supported	O	Yes [ ] No [ ]
*FDD	Support for optional FEC degraded SER detection	134.5.3.3.2		O	Yes [ ] No [ ]

134.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	134.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps.	M	Yes [ ]
TF2	Lane reorder	134.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	134.5.2.5	tx_xcoded<256:0> constructed per 134.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	134.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	134.5.2.6	Map to am_txmapped<256:0> per 134.5.2.6	M	Yes [ ]
TF6	Pad value	134.5.2.6	Set to 0 or 1 in an alternating pattern	M	Yes [ ]
TF7	Alignment marker insertion	134.5.2.6	First 257 message bits to be transmitted from every 1024th codeword	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TF8	First 257-bit block inserted after am_txmapped	134.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF9	Reed-Solomon encoder	134.5.2.7		M	Yes [ ]
TF10	Symbol distribution	134.5.2.8	Distributed to 2 FEC lanes, one 10-bit symbol at a time alternating between FEC lanes 0 and 1	M	Yes [ ]

134.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	134.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	134.5.2.3	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for RS(544,514)	134.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword.	M	Yes [ ]
RF4	Reed-Solomon decoder	134.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	134.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords.	M	Yes [ ]
RF6	Error monitoring while error indication is bypassed	134.5.3.3.1	When the number of symbols errors in a block of 8192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF7	Symbol error threshold for RS(544,514)	134.5.3.3.1	K=6380	BEI:M	Yes [ ] N/A [ ]
RF8	FEC decoder detects FEC degraded SER at a program-mable threshold	134.5.3.3.2		FDD:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	134.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF10	256B/257B to 64B/66B transcoder	134.5.3.5	rx_coded_j<65:0>, j=0 to 3 constructed per 134.5.3.5	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RF11	Block distribution	134.5.3.6	One 66-bit block at a time in a round robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
RF12	Alignment marker mapping	134.5.3.7	Map to am_rx_*x*, *x*=0 to 3 per 134.5.3.7	M	Yes [ ]
RF13	Alignment marker insertion point	134.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-bit blocks immediately following am_rxmapped	M	Yes [ ]

134.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	134.5.4.2.2	Ensure that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	134.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	134.5.4.3	Per Figure 91–9	M	Yes [ ]

134.7.4.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	RS-FEC Delay Constraint	134.4	No more than 25 600 bit times for sum of transmit and receive path delays	M	Yes [ ]

135. Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.1 Overview

135.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) for the families of 50 Gb/s and 100 Gb/s PAM4 Physical Layer implementations known as 50GBASE-R (see 131.1.3) and 100GBASE-P (see 80.1.4). The PMA allows the PCS (see Clause 133 and Clause 82) and FEC (see Clause 134 and Clause 91) to connect in a media-independent way with a range of physical media. The 50GBASE-R PMA can support any of the 50 Gb/s PMDs in Table 131–1 and the 100GBASE-P PMA can support any of the 100 Gb/s PAM4 PMDs according to Table 80–3 and Table 80–4a.

50GBASE-R and 100GBASE-P PHYs can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

The interfaces for the inputs of the 50GBASE-R and 100GBASE-P PMAs are defined in an abstract manner and do not imply any particular implementation. For 50GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as LAUI-2 and 50GAUI-n, are defined in Annex 135B through Annex 135G. For 100GBASE-P PMAs, electrical interfaces connecting PMA sublayers, known as 100GAUI-n, are defined in Annex 135D through Annex 135G.

135.1.2 Position of the PMA in the 50GBASE-R and 100GBASE-P sublayers

Figure 135–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

135.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Adapt the PCSL/FECL-formatted signal to the appropriate number of abstract or physical lanes.
b) Provide per-input-lane clock and data recovery.
c) Provide bit-level multiplexing.
d) Provide clock generation.
e) Provide signal drivers.
f) Optionally provide local loopback to/from the PMA service interface.
g) Optionally provide remote loopback to/from the PMD service interface.
h) Optionally provide test-pattern generation and checking.
i) Tolerate Skew Variation.
j) Perform PAM4 encoding and decoding, including Gray mapping and optional precoding, when required.

PAM4 encoding and decoding is required for 50GBASE-R PMAs where the number of physical lanes is 1 and for 100GBASE-P PMAs where the number of physical lanes is 1 or 2.

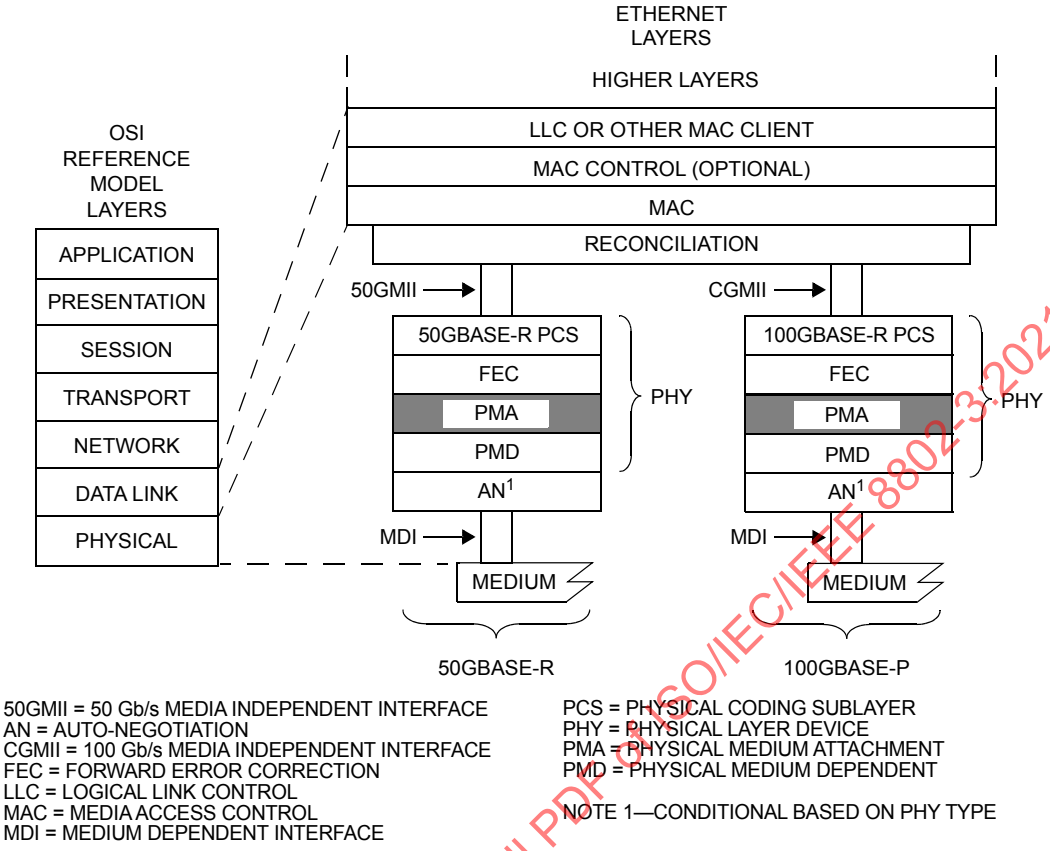
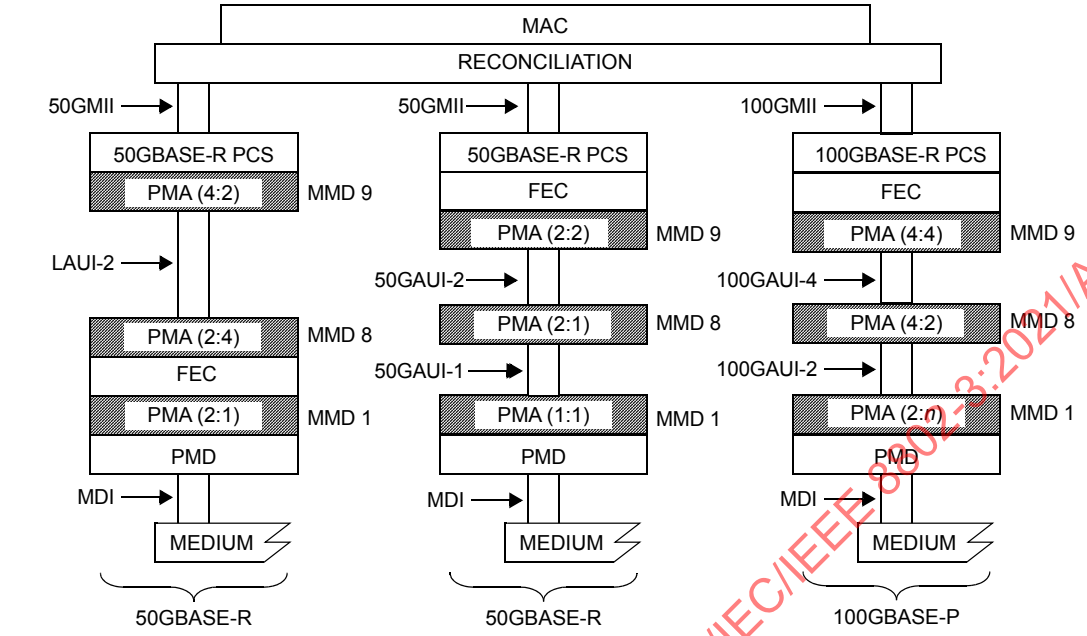


Figure 135–1—50GBASE-R and 100GBASE-P PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

135.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCS lanes to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation. An example is illustrated in Figure 135–2. Additional examples are illustrated in Annex 135A. Each PMA maps the PCSLs/FECLs from *p* PMA input lanes to *q* PMA output lanes in the Tx direction, and from *q* PMA input lanes to *p* PMA output lanes in the Rx direction.

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, and 10 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the MAC. The examples shown in Figure 135–2 could be implemented with three addressable instances: MMD 1 addressing the lowest PMA sublayer (co-packaged with the PMD), MMD 8 addressing the middle PMA sublayer, and MMD 9 addressing the highest PMA sublayer (immediately below the FEC).



100GAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 1 or 2

Figure 135–2—Example 50GBASE-R and 100GBASE-P PMA layering

The number of input lanes and the number of output lanes for a PMA are always divisors of the number of PCSLs/FECLs. For PMA sublayers supporting 50GBASE-R PMDs, the number of PCSLs (above the FEC) is 4 and the number of FECLs (below the FEC) is 2. For PMA sublayers supporting 100GBASE-P PMDs, the number of FECLs is 4.

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 131.3.1, is used for the PMA service interfaces supporting a flexible architecture with multiple PMA sublayers.
   1) An instance of this interface can only connect service interfaces with the same number of lanes, where the lanes operate at the same rate.

b) The abstract PMA service interface can be physically instantiated as a LAUI-2, 50GAUI-n, or 100GAUI-n, using associated PMAs to map to the appropriate number of lanes.

c) For physical instantiations of the PMA service interface, the PMA:IS_SIGNAL.indication is conveyed outside of this physically instantiated interface.

d) Physical instantiations of the PMA service interface define electrical and timing specification as well as requiring a receive re-timing function.

e) LAUI-2 is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers above the FEC.
   1) LAUI-2 provides bit-multiplexing of 4 PCSLs.
   2) LAUI-2 is a 25.78125 GBd by two-lane NRZ physical instantiation of the 50 Gb/s connection.

f) 50GAUI-n is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers below the FEC and contains 2 FECLs.
   1) 50GAUI-n provides bit-multiplexing of 2 FECLs.
   2) 50GAUI-2 is a 26.5625 GBd by two-lane NRZ physical instantiation of the 50 Gb/s connection.
   3) 50GAUI-1 is a 26.5625 GBd by one-lane PAM4 physical instantiation of the 50 Gb/s connection.

g) CAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-R PMA (see Clause 83) sublayers above the FEC for a 100GBASE-P PHY or between adjacent sublayers below the PCS for a 100GBASE-R PHY. CAUI-n is not specified in this clause, but is listed here for completeness.
   1) CAUI-n provides bit-multiplexing of 20 PCSLs.
   2) CAUI-4 is a 25.78125 GBd by four-lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-4 is specified in Clause 83 and associated annexes.
   3) CAUI-10 is a 10.3125 GBd by ten-lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-10 is specified in Clause 83 and associated annexes.

h) 100GAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-P PMA sublayers below the FEC for a 100GBASE-P PHY.
   1) 100GAUI-n provides bit-multiplexing of 4 FECLs.
   2) 100GAUI-4 is a 26.5625 GBd by four-lane NRZ physical instantiation of the 100 Gb/s connection.
   3) 100GAUI-2 is a 26.5625 GBd by two-lane PAM4 physical instantiation of the 100 Gb/s connection.

i) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 135–5.

j) A minimum of one PMA sublayer is required in a PHY.

k) A maximum of four PMA sublayers are addressable as MDIO MMDs.

135.2 PMA interfaces

All PMA variants for 50GBASE-R and 100GBASE-P are based on a generic specification of a bit mux function that applies to all input/output lane counts and each direction of transmission. Each direction of transmission may employ one or more such bit muxes to adapt from the appropriate number of input lanes to the appropriate number of output lanes as illustrated in Figure 135–3.

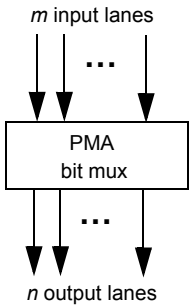


Figure 135–3—PMA bit mux used in both Tx and Rx directions

Conceptually, the PMA bit mux operates in one direction of transmission by demultiplexing PCSLs/FECLs from *m* PMA input lanes and remultiplexing them into *n* PMA output lanes. The mapping of PCSLs/FECLs from input to output lanes is not specified. See 135.5.2 and Figure 135–4 for details.

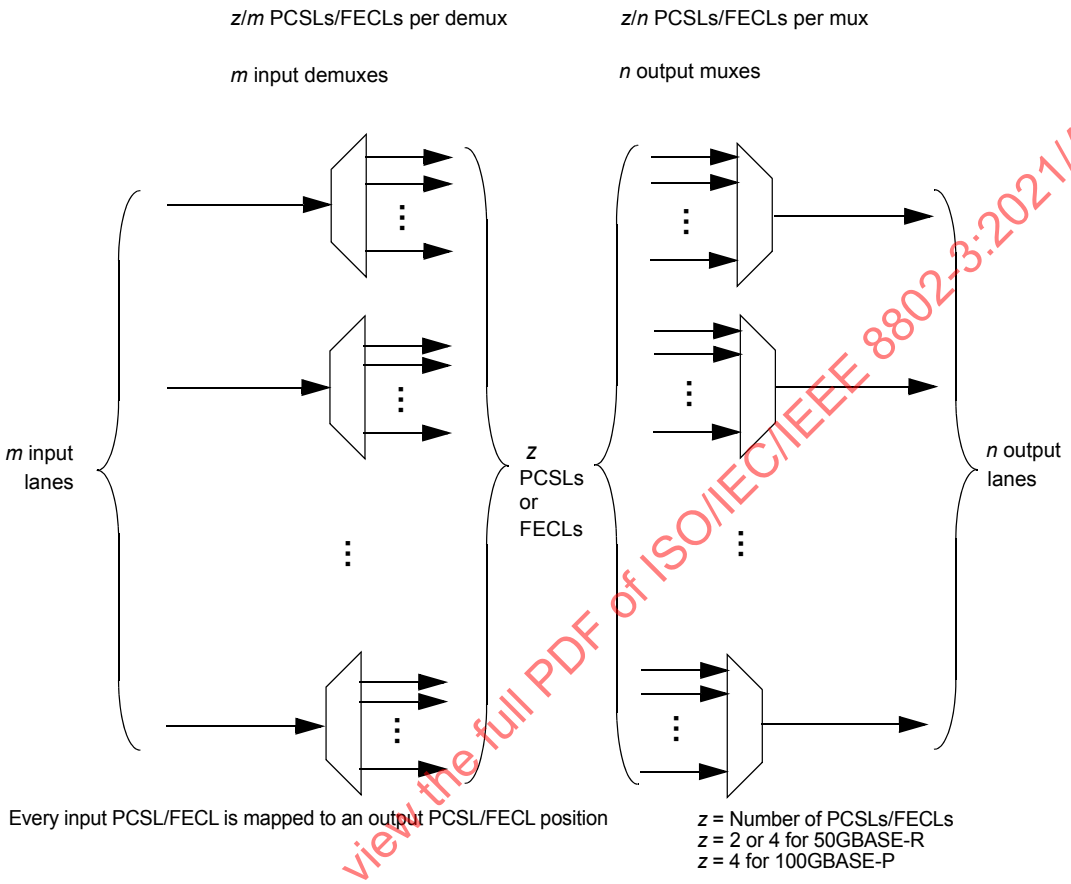


Figure 135–4—PMA bit mux operation used in both Tx and Rx directions

135.3 PMA service interface

The PMA service interface for 50GBASE-R and 100GBASE-P is an instance of the inter-sublayer service interface defined in 131.3.1. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication
PMA:IS_SIGNAL.indication

For a PMA service interface with *p* lanes, the primitives are defined for $i = 0$ to $p - 1$.

If the PMA client is the 50GBASE-R PCS, the PMA continuously sends four parallel bit streams to the PCS, each at the nominal signaling rate of the PCSL.

If a PMA client is another PMA, a 50GBASE-R PMA with p=2 physical input lanes receives NRZ symbols on each of its input lanes at the FECL rate or at 2 times the PCSL rate. A 50GBASE-R PMA with p=1

physical input lane receives PAM4 symbols on that input lane at the FECL rate, with each symbol formed from two bits.

If a PMA client is another PMA, 100GBASE-P PMA with p=4 physical input lanes receives NRZ symbols on each of its input lanes at the FECL rate. A 100GBASE-P PMA with p=1 or p=2 physical input lanes receives PAM4 symbols on each of its input lanes at 2 or 1 times, respectively, the FECL rate, with each symbol formed from two bits. The bit stream represented by the input symbols carries z/p bit-multiplexed FECLs on each physical input lane, where z=4 for 100GBASE-P.

Skew may exist between different PCSLs/FECLs received on the same physical input lane even though all PCSLs/FECLs originate from the same synchronous source, so there is independence of arrival of bits from each PCSL/FECL on each physical input lane.

In the Tx direction, if the symbol from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols are converted to pairs of bits. Bits are routed through the PMA to an output lane through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits on output lanes are converted to PAM4 symbols. The symbols are sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (k not necessarily equal to i) primitive (see 135.4).

In the Rx direction, the PMA passes the bits represented by the symbols from the input lane(s) received from the sublayer below the PMA into encoded symbols on the output lanes. If necessary, buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes. PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the PMA client via the PMA:IS_UNITDATA_i.indication primitive.

The PMA:IS_SIGNAL.indication primitive is generated by a Signal Indication Logic (SIL) function that reports signal health based on receipt of the *inst*:IS_SIGNAL.indication from the sublayer below, data being received on all of the input lanes from the sublayer below, buffers filled (if necessary) to accommodate Skew Variation, and symbols being sent to the PMA client on all of the output lanes. When these conditions are met, the SIGNAL_OK parameter sent to the PMA client via the PMA:IS_SIGNAL.indication primitive has the value OK. Otherwise, the SIGNAL_OK primitive has the value FAIL.

135.4 Service interface below PMA

Since the architecture supports multiple PMA sublayers for various PMD lane counts and device partitioning, there are several different sublayers that may appear below a PMA, including the FEC, PMD, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA, FEC, or PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 131.3. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA_*i*.request
inst:IS_UNITDATA_*i*.indication
inst:IS_SIGNAL.indication

The number of lanes q for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane $i = 0$ to $q - 1$ of the service interface below the PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., LAUI-2, 50GAUI-n, or 100GAUI-n), otherwise the service interface is

specified only abstractly. The interface between the PMA and the sublayer below consists of *q* lanes for data transfer and a status indicating a good signal from the sublayer below the PMA (see Figure 135–5).

In the Tx direction, the PMA passes the bits represented by the symbols from the input lane(s) received via the PMA:IS_UNITDATA_i.request primitive(s) into encoded symbols on the output lanes. If necessary, buffers are filled to provide the ability to tolerate the Skew Variation that may appear between the input lanes from the PMA client. PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the sublayer below the PMA.

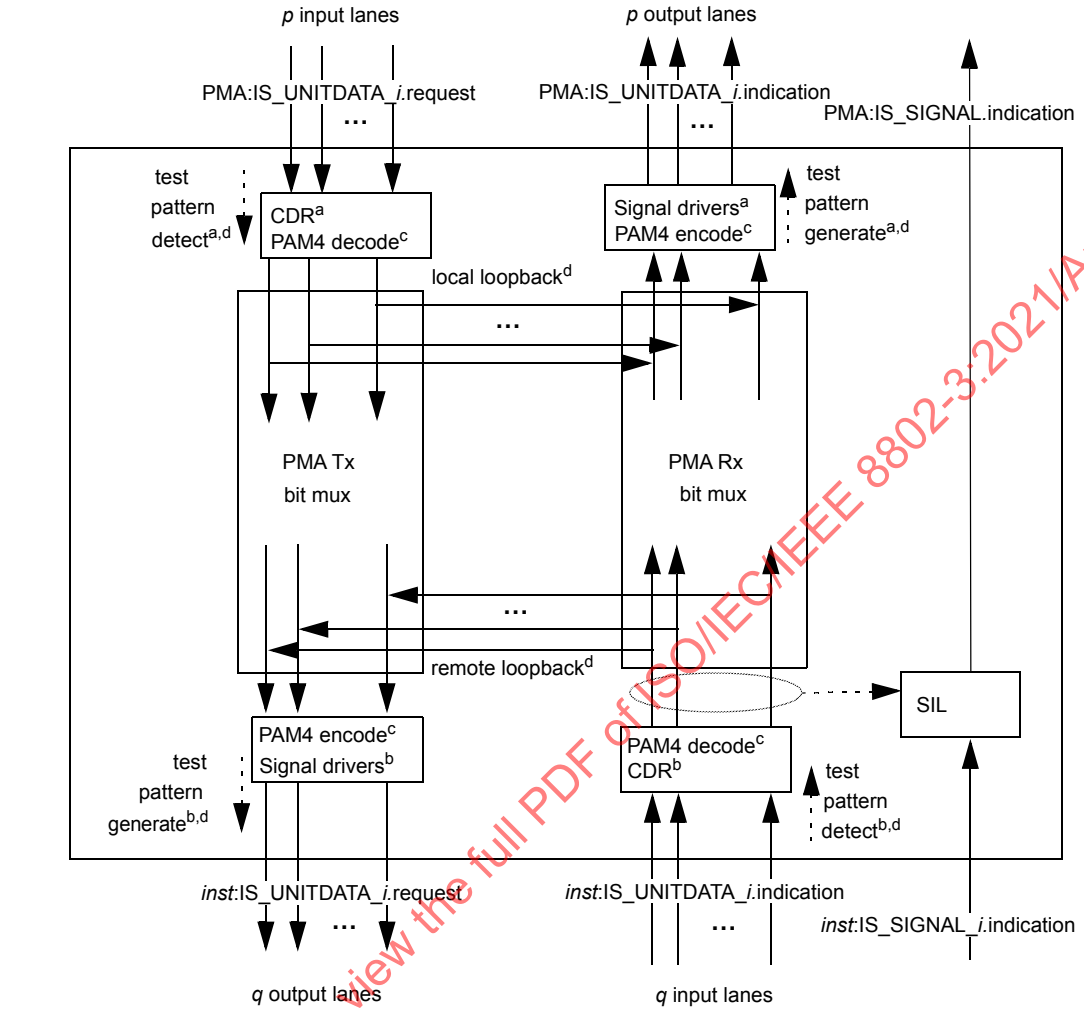
In the Rx direction, if the symbol is received over a physically instantiated interface (50GAUI-n, 100GAUI-n, or physically instantiated PMD service interface), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols received on the input lanes are converted to pairs of bits. The bits are routed through the PMA to an output lane toward the PMA client through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits are converted to PAM4 symbols on the output lanes. Each symbol is sent on an output lane to the PMA client using the PMA:IS_UNITDATA_*k*.indication (*k* not necessarily equal to *i*) primitive at the PMA service interface.

135.5 Functions within the PMA

The purpose of the PMA is to adapt the PCSL/FECL-formatted signal to an appropriate number of abstract or physical lanes, to recover clock from the received signal (if appropriate), and optionally to provide test signals and loopback. Each input (Tx direction) or output (Rx direction) lane between the PMA and the PMA client carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the PMA client carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. Likewise, each input (Rx direction) or output (Tx direction) lane between the PMA and the sublayer below the PMA carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the sublayer below the PMA carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. As described in 135.1.4, the number of input lanes and the number of output lanes for a given PMA are divisors of 2 (below the FEC) or 4 (above the FEC) for 50GBASE-R, or 4 for 100GBASE-P, which are the number of PCSLs/FECLs for the respective PHYs.

Figure 135–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

— The numbers of input and output lanes in each direction.
— Whether the PMA is adjacent to a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n above or below).
— Whether the PMA is adjacent to the PCS.
— Whether the PMA is adjacent to the PMD.
— Whether the PMA is adjacent to the FEC.



inst = PMD, PMA, depending on which sublayer is below this PMA
SIL = Signal Indication Logic

[a] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately above this PMA.
[b] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately below this PMA or if this is the closest PMA to the PMD.
[c] If number of input or output lanes is 1 for a 50GBASE-R PMA, or 1 or 2 for a 100GBASE-P PMA.
[d] Optional.

Figure 135–5—PMA Functional Block Diagram

135.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications above the PMA in Annex 135B through Annex 135G, as appropriate.

If the interface between the sublayer below the PMA and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications below the PMA at the service interface as specified in Annex 135B through Annex 135G, as appropriate.

135.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing in both the Tx and Rx directions. In the Tx direction, the function is performed among the bits received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to $p - 1$) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to $q - 1$), referencing the functional block diagram shown in Figure 135–5. The bit multiplexing behavior is illustrated in Figure 135–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs/FECLs. The number of PCSLs/FECLs z is 2 FECLs (below the FEC) and 4 PCSLs (above the FEC) for 50GBASE-R interfaces and 4 FECLs for 100GBASE-P interfaces. For 50GBASE-R, the nominal bit rate R_{lane} is 12.890625 Gb/s for each PCSL and 26.5625 Gb/s for each FECL. For 100GBASE-P, the nominal bit rate R_{lane} is 26.5625 Gb/s for each FECL.

For a PMA with m input lanes (Tx or Rx direction), each input lane carries, bit multiplexed, z/m PCSLs/FECLs. Each input lane has a nominal bit rate of $z/m \times R_{lane}$. Note that the signaling rate is equal to the bit rate when the signal modulation is NRZ. The signaling rate is equal to half of the bit rate when the signal modulation is PAM4. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes. If bit x received on an input lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is received on the same input lane at bit position $x+(z/m)$. The z/m PCSLs/FECLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (Tx or Rx direction), each output lane carries, bit multiplexed, z/n PCSLs/FECLs. Each output lane has a nominal signaling rate of $z/n \times R_{lane}$. Each PCSL/FECL is mapped from a position in the sequence on one of the m input lanes to a position in the sequence on one of the n output lanes. If bit x sent on an output lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is sent on the same output lane at bit position $x + (z/n)$. The PMA shall maintain the chosen sequence of PCSLs/FECLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

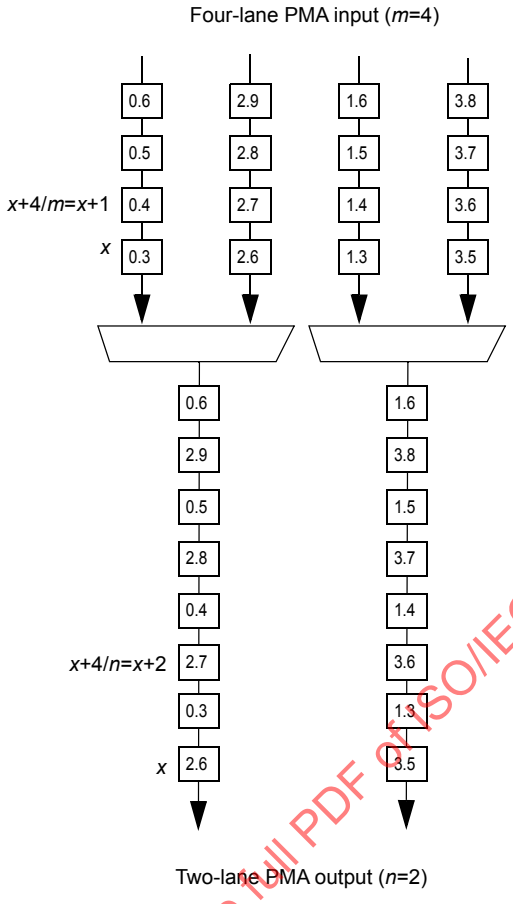
Each PCSL/FECL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 133 and Clause 82) and FEC (See Clause 91 and Clause 134) have fully flexible receive logic, an implementation is free to perform the mapping of PCSLs/FECLs from input lanes to output lanes without constraint. Figure 135–6 illustrates one possible bit ordering for a 100GBASE-P 4:2 PMA bit mux. Other bit orderings are also valid.

Note that since the number of input lanes and output lanes for a 50GBASE-R or 100GBASE-P PMA is always a power of two, many PMAs converting between different numbers of lanes normally simply multiplex two or four input lanes to one output lane, or demultiplex two or four output lanes from one input lane. However, any PMA implementation which produces an allowable order of bits from all PCSLs/FECLs on the output lanes is valid.

135.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs/FECLs must be kept within limits so that the information on the lanes can be reassembled by the PCS and FEC.

Any PMA that combines PCSLs/FECLs from different input lanes onto the same output lane must tolerate Skew Variation between the input lanes without changing the PCSL/FECL positions on the output. Skew and Skew Variation are defined in 131.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP0, SP1, and SP2 in the transmit direction and SP5, SP6, and SP7 in the receive direction as defined in 131.5 and illustrated in Figure 131–3 for 50GBASE-R and as defined in 80.5 and illustrated in Figure 80–8 for 100GBASE-P.



NOTE—*i.k* indicates bit *k* on FECL *i*. Skew may exist between FECLs.

Figure 135–6—Example 4:2 100GBASE-P PMA bit mux

135.5.3.1 Skew generation toward SP0

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the transmit direction toward the LAUI-2 (SP0 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.2 Skew tolerance at SP0

In an implementation with an instantiated LAUI-2 interface, the PMA service interface that receives data in the transmit direction from the LAUI-2 (SP0 in Figure 131–3) shall tolerate the maximum amount of Skew Variation allowed at SP0 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.3 Skew generation toward SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA that sends data in the transmit direction toward the 50GAUI-n or 100GAUI-n that is closest to the PMD (SP1 in Figure 131–3 and Figure 80–8) shall produce no more than 29 ns of Skew between FECLs toward the 50GAUI-n or 100GAUI-n and no more than 0.2 ns of Skew Variation.

135.5.3.4 Skew tolerance at SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the 50GAUI-n or 100GAUI-n (SP1 in Figure 131–3 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP1 (0.2 ns) between input lanes while maintaining the bit ordering and position of each FECL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.5 Skew generation toward SP2

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 0.4 ns of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 80–8 and Figure 131–3). If there is a physically instantiated 50GAUI-n or 100GAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 0.2 ns of Skew Variation.

135.5.3.6 Skew tolerance at SP5

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, the PMA adjacent to the PMD service interface (SP5 in Figure 131–3 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP5 (0.4 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each FECL on each PMA lane in the receive direction (toward the MAC).

135.5.3.7 Skew generation at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, at SP6 (the receive direction of the 50GAUI-n or 100GAUI-n closest to the FEC), the PMA or group of PMAs between the PMD and the 50GAUI-n or 100GAUI-n closest to the FEC shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the 50GAUI-n or 100GAUI-n in the Rx direction.

If there is a physically instantiated PMD service interface that allows the Skew to be measured, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

135.5.3.8 Skew tolerance at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA between the 50GAUI-n or 100GAUI-n closest to the FEC and the FEC shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of FECLs on lanes sent in the receive direction towards the MAC.

135.5.3.9 Skew generation at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the receive direction toward the LAUI-2 (SP7 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.10 Skew tolerance at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA service interface that receives data in the receive direction from the LAUI-2 (SP7 in Figure 131–3) shall tolerate the

maximum amount of Skew Variation allowed at SP7 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

135.5.4 Delay constraints

The maximum cumulative delay contributed by up to three PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 135–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

Table 135–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50GBASE-R PMA	4608	9	92.16
100GBASE-P PMA	9216	18	92.16

135.5.5 Clocking architecture

A PMA with *m* input lanes and *n* output lanes shall clock the output lanes such that the bit rate of the output lanes is *m*/*n* times the bit rate of the input lanes. For input or output lanes encoded as PAM4, the symbol rate is half of the bit rate. This applies in both the Tx and Rx directions of transmission. In the case where the interfaces between the PMA client and the PMA and/or the PMA and the sublayer below the PMA are physically instantiated, the PMA may derive its input clock(s) from the electrical interface on one or more of the input lanes, and generate the output clock(s) with an appropriate PLL multiplier/divider circuit.

NOTE—For a PMA where the signaling rate on each output lane is higher than the signaling rate on each input lane, any low-frequency jitter on the input lanes may result in more jitter relative to the UI on the output lanes.

There is no requirement that the PMA clock all output lanes in unison. Examples of independent clocking of output lanes include the following:

— The case where the number of input and output lanes are equal (the PMA is provided for retiming and regeneration of the signal). This may be implemented without any rearrangement of PCSLs/FECLs between input lanes and output lanes (although rearrangements are allowed). Such a PMA may be implemented by driving each output lane using the clock recovered from the corresponding input lane.

— Since the number of PCSLs/FECLs is a power of 2, whenever the number of input and output lanes are unequal, each input lane could be mapped to multiple output lanes (in the case where the number of output lanes is greater), or multiple input lanes could be mapped to a single output lane.

135.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

— Annex 135B for LAUI-2 C2C applications
— Annex 135C for LAUI-2 C2M applications
— Annex 135D for 50GAUI-2 and 100GAUI-4 C2C applications
— Annex 135E for 50GAUI-2 and 100GAUI-4 C2M applications
— Annex 135F for 50GAUI-1 and 100GAUI-2 C2C applications
— Annex 135G for 50GAUI-1 and 100GAUI-2 C2M applications

The modulation format is NRZ for LAUI-2, 50GAUI-2, and 100GAUI-4 and the modulation format is PAM4 for 50GAUI-1 and 100GAUI-2.

135.5.7 PAM4 encoding

135.5.7.1 Gray mapping for PAM4 encoded lanes

For output lanes encoded as PAM4, the PMA transmit process shall map consecutive pairs of bits to Gray-coded symbols G(*j*) with one of four levels as specified in 120.5.7.1.

For input lanes encoded as PAM4, the PMA receive process shall map Gray-coded symbols G(*j*) with one of four levels to pairs of bits as specified in 120.5.7.1.

135.5.7.2 Precoding for PAM4 encoded lanes

A PMA shall provide 1/(1+D) mod 4 precoding capability on each output lane that is part of a 50GAUI-1 C2C or 100GAUI-2 C2C link, or connected to the PMD service interface of a 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, or 100GBASE-KR2 PMD. A PMA may optionally provide 1/(1+D) mod 4 decoding capability on each input lane that is part of a 50GAUI-1 C2C or 100GAUI-2 C2C link, or connected to the PMD service interface of a 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, or 100GBASE-KR2 PMD.

On each output lane, for each Gray-coded symbol G(*j*), a precoded symbol P(*j*) shall be determined by the following algorithm, where *j* is an index indicating the symbol number:

$$P(j) = (G(j) - P(j\text{-}1)) \bmod 4, \text{ when precoding is enabled} \quad (135\text{–}1)$$

$$P(j) = G(j), \text{ when precoding is disabled} \quad (135\text{–}2)$$

On each input lane, for each precoded symbol P(*j*), a Gray-code symbol G(*j*) shall be determined by the following algorithm:

$$G(j) = (P(j) + P(j\text{-}1)) \bmod 4, \text{ when precoding is enabled} \quad (135\text{–}3)$$

$$G(j) = P(j), \text{ when precoding is disabled} \quad (135\text{–}4)$$

The precoder is enabled independently for the input and output in each direction (Tx direction toward the PMD and Rx direction toward the MAC) and on each lane. Precoding is enabled and disabled using variables precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i*, precoder_rx_out_enable_*i*, and precoder_tx_in_enable_*i*. If a Clause 45 MDIO is implemented, these variables are accessible through registers 1.600, 1.601, 1.602, and 1.603 (see 45.2.1.132a through 45.2.1.132d). An example relating the variables with input and outputs is provided in Figure 135–7.

For PMA input and output lanes connected to the PMD service interface of a 50GBASE-CR PMD, 50GBASE-KR PMD, 100GBASE-CR2 PMD, or 100GBASE-KR2 PMD, precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* shall be set as determined by the PMD control function on lane *i* (see 136.8.11.7.5). The method by which the PMD control function affects these variables is implementation dependent.

For PMA input and output lanes that are part of a 50GAUI-1 C2C or a 100GAUI-2 C2C link, precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i*, precoder_tx_in_enable_*i*, and precoder_rx_out_enable_*i* are set as required by the implementation. The implementation may use the method described in 135F.3.2.1.

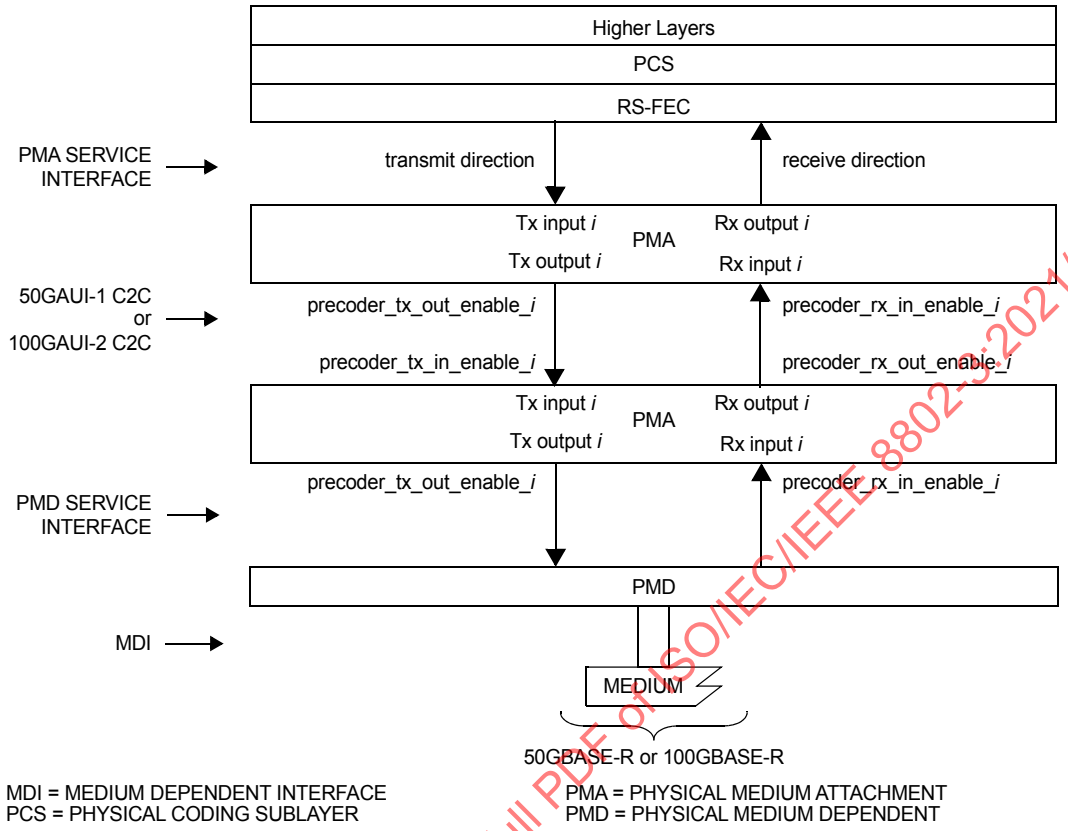


Figure 135–7—Example relating PMA precoder variables to inputs and outputs

135.5.8 PMA local loopback mode (optional)

PMA local loopback mode is optional. If it is implemented, it shall be as specified in this subclause.

The PMA sublayer may provide a local loopback function. The function involves looping back each input lane to the corresponding output lane. Each bit received from the PMA:IS_UNITDATA_*i*.request(tx_symbol) primitive is looped back toward the MAC using the PMA:IS_UNITDATA_*i*.indication(rx_symbol) primitive.

During local loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Tx direction toward the service interface below the PMA.

Ability to perform this function is indicated by the Local_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15).

A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

NOTE—Placing a network port into loopback mode can be disruptive to a network.

135.5.9 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

Remote loopback, if provided, should be implemented in a PMA sublayer close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each symbol received over a lane of the service interface below the PMA via *inst*:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via *inst*:IS_UNITDATA_*i*.request. Note that the service interface below the PMA can be provided by the PMD, FEC (LAUI-2 only), or another PMA sublayer.

During remote loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the 50G_Remote_loopback_ability status variable for 50GBASE-R 100G_Remote_loopback_ability status variable for 100GBASE-P.

A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one and removed from remote loopback mode when this variable is set to zero.

If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (45.2.1.12.1).

If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

135.5.10 PMA test patterns (optional)

Where the output lanes of the PMA appear on a physically instantiated interface LAUI-2, 50GAUI-n, 100GAUI-n or the PMD service interface (whether or not it is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent-layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external test equipment.

135.5.10.1 Test patterns for NRZ encoded signals

For a 50GBASE-R PMA with NRZ encoding, the test patterns in this subclause may be supported.

135.5.10.1.1 PRBS31 test pattern

A PMA may optionally include a PRBS31 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.1.

A PMA may optionally include a PRBS31 test-pattern checker on input lanes in either direction as specified in 120.5.11.1.1.

135.5.10.1.2 PRBS9 test pattern

A PMA may optionally include a PRBS9 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.2.

135.5.10.1.3 Square-wave test pattern

A PMA may optionally include a square-wave test-pattern generator on output lanes in either direction as specified in 120.5.11.1.3.

135.5.10.2 Test patterns for PAM4 encoded signals

For a 50GBASE-R PMA with PAM4 encoding, the test patterns described in this subclause may be supported.

The PRBS13Q and quaternary square wave test patterns are enabled on a lane-by-lane basis. The patterns PRBS31Q and SSPRQ are enabled on all lanes of an interface at once. If a per-lane pattern is enabled on one or more of the lanes and a per-interface pattern is also enabled, the per-lane patterns are generated only on the indicated lanes and the per-interface pattern is generated on the remaining lanes. The behavior if more than one per-lane pattern is enabled for the same lane or more than one per-interface pattern is enabled is not defined.

135.5.10.2.1 PRBS13Q test pattern

A PMA may optionally include a PRBS13Q test-pattern generator as specified in 120.5.11.2.1.

135.5.10.2.2 PRBS31Q test pattern

A PMA may optionally include a PRBS31Q test-pattern generator on output lanes in either direction as specified in 120.5.11.2.2.

A PMA may optionally include a PRBS31Q test-pattern checker on input lanes in either direction as specified in 120.5.11.2.2.

135.5.10.2.3 SSPRQ test pattern

A PMA may optionally include a short stress pattern random quaternary (SSPRQ) test-pattern generator as specified in 120.5.11.2.3.

135.5.10.2.4 Square wave (quaternary) test pattern

Transmit square wave (quaternary) test-pattern generator optionally applies to each lane of the Tx direction PMA towards a physically instantiated 50GAUI-1 or 100GAUI-1, or towards a PAM4 PMD service interface whether or not it is physically instantiated as specified in 120.11.5.2.4.

135.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 135.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, and 10 use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 135–2. Mapping of MDIO status variables to PMA status variables is shown in Table 135–3. Mapping of MDIO counter to PMA counters is shown in Table 135–4. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, and 10 as necessary.

Table 135–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 1 Tx output precoder enable	PMA precoder control Tx output	1.600.1	precoder_tx_out_enable_1
Lane 0 Tx output precoder enable	PMA precoder control Tx output	1.600.0	precoder_tx_out_enable_0
Lane 1 Rx input precoder enable	PMA precoder control Rx input	1.601.1	precoder_rx_in_enable_1
Lane 0 Rx input precoder enable	PMA precoder control Rx input	1.601.0	precoder_rx_in_enable_0
Lane 1 Rx output precoder enable	PMA precoder control Rx output	1.602.1	precoder_rx_out_enable_1
Lane 0 Rx output precoder enable	PMA precoder control Rx output	1.602.0	precoder_rx_out_enable_0
Lane 1 Tx input precoder enable	PMA precoder control Tx input	1.603.1	precoder_tx_in_enable_1
Lane 0 Tx input precoder enable	PMA precoder control Tx input	1.603.0	precoder_tx_in_enable_0
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
PRBS31Q pattern enable	PRBS pattern testing control	1.1501.13	PRBS31Q_pattern_enable
SSPRQ pattern enable	PRBS pattern testing control	1.1501.14	SSPRQ_pattern_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
Lane 1 SW enable	Square wave testing control	1.1510.1	Square_wave_enable_1
Lane 2 SW enable	Square wave testing control	1.1510.2	Square_wave_enable_2
Lane 3 SW enable	Square wave testing control	1.1510.3	Square_wave_enable_3
Lane 0 PRBS13Q enable	PRBS13Q testing control	1.1512.0	PRBS13Q_enable_0

Table 135–2—MDIO/PMA control variable mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
Lane 1 PRBS13Q enable	PRBS13Q testing control	1.1512.1	PRBS13Q_enable_1
Lane 2 PRBS13Q enable	PRBS13Q testing control	1.1512.2	PRBS13Q_enable_2
Lane 3 PRBS13Q enable	PRBS13Q testing control	1.1512.3	PRBS13Q_enable_3

Table 135–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PMA remote loopback ability	40G/100G PMA extended ability	1.13.15	100G_Remote_loopback_ ability
50G PMA remote loopback ability	50G PMA extended ability	1.22.15	50G_Remote_loopback_ ability
PRBS9 Tx generator ability	Test-pattern ability	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability	1.1500.4	PRBS9_Rx_generator_ability
PRBS31Tx generator ability	Test-pattern ability	1.1500.3	PRBS31_Tx_generator_ability
PRBS31Tx checker ability	Test-pattern ability	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability	1.1500.12	Square_wave_ability
PRBS13Q Tx generator ability	Test-pattern ability	1.1500.11	PRBS13Q_gen_Tx_ability
PRBS13Q Rx generator ability	Test-pattern ability	1.1500.10	PRBS13Q_gen_Rx_ability
PRBS31Q Tx generator ability	Test-pattern ability	1.1500.9	PRBS31Q_gen_Tx_ability
PRBS31Q Rx generator ability	Test-pattern ability	1.1500.7	PRBS31Q_gen_rx_ability
PRBS31Q Tx checker ability	Test-pattern ability	1.1500.8	PRBS31Q_Tx_checker_ability
PRBS31Q Rx checker ability	Test-pattern ability	1.1500.6	PRBS31Q_Rx_checker_ ability
SSPRQ Tx generator ability	Test-pattern ability	1.1500.13	SSPRQ_gen_Tx_ability

Table 135–4—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Tx, lane 1	PRBS Tx pattern testing error counter, lane 1	1.1601	Ln1_PRBS_Tx_test_err_counter
Error counter Tx, lane 2	PRBS Tx pattern testing error counter, lane 2	1.1602	Ln2_PRBS_Tx_test_err_counter
Error counter Tx, lane 3	PRBS Tx pattern testing error counter, lane 3	1.1603	Ln3_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter
Error counter Rx, lane 1	PRBS Rx pattern testing error counter, lane 1	1.1701	Ln1_PRBS_Rx_test_err_counter
Error counter Rx, lane 2	PRBS Rx pattern testing error counter, lane 2	1.1702	Ln2_PRBS_Rx_test_err_counter
Error counter Rx, lane 3	PRBS Rx pattern testing error counter, lane 3	1.1703	Ln3_PRBS_Rx_test_err_counter

135.7 Protocol implementation conformance statement (PICS) proforma for Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P[9]

135.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135.7.2 Identification

135.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[9] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

135.7.3 Major capabilities/options

Item	Feature	Subclause	Value/ Comment	Status	Support
*P50	PMA for 50GBASE-R	135.1.1		O.1	Yes [ ] No [ ]
*P100	PMA for 100GBASE-P	135.1.1		O.1	Yes [ ] No [ ]
*BPCS	PMA is immediately below PCS	135.1.4		O.2	Yes [ ] No [ ]
*AFEC	PMA is immediately above FEC	135.1.4		O.2	Yes [ ] No [ ]
*BFEC	PMA is below FEC and not immediately above PMD.	135.1.4		O.2	Yes [ ] No [ ]
*APMD	PMA is immediately above PMD	135.1.4		O.2	Yes [ ] No [ ]
*PSIA	PMA connected to a physically instantiated PMA service interface	135.1.4		O	Yes [ ] No [ ]
*PSID	PMA connected to a physically instantiated PMD service interface	135.1.4		APMD:O	Yes [ ] N/A [ ]
*NLA	Number of lanes on physically instantiated PMA service interface	135.1.4		50G*PSIA:M	1 [ ] 2 [ ] N/A [ ]
				100G*PSIA:M	2 [ ] 4 [ ] N/A [ ]
*NLD	Number of lanes on PMD service interface	135.1.4		50G*APMD:M	1 [ ] N/A [ ]
				100G*APMD:M	1 [ ] 2 [ ] N/A [ ]
*50GL	Physical instantiation of the PMA service interface is LAUI-2	135.1.4		50G*(BPCS+AFEC)* PSIA:M	Yes [ ] N/A [ ]
*50GA1	Physical instantiation of the PMA service interface is 50GAUI-1	135.1.4		50G*(BFEC+APMD)* PSIA*NLA=1:M	Yes [ ] N/A [ ]
*50GA2	Physical instantiation of the PMA service interface is 50GAUI-2	135.1.4		50G*(BFEC+APMD)* PSIA*NLA=2:M	Yes [ ] N/A [ ]
*100GA2	Physical instantiation of the PMA service interface is 100GAUI-2	135.1.4		100G*(BFEC+APMD) *PSIA*NLA=2:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/ Comment	Status	Support
*100GA4	Physical instantiation of the PMA service interface is 100GAUI-4	135.1.4		100G*(BFEC+APMD) *PSIA*NLA=4:M	Yes [ ] N/A [ ]
*AT	AUI type, C2C or C2M	135.5.6		PSIA:M	C2C [ ] C2M [ ] N/A [ ]
*NRZ	NRZ modulation	135.1.4		50GL+50GA2+ 100GA4:M	Yes [ ] N/A [ ]
*PAM4A	PAM4 modulation on physically instantiated PMA service interface	135.1.4		50GA1+100GA2:M	Yes [ ] N/A [ ]
*PAM4D	PAM4 modulation on PMD service interface	135.1.4		APMD:M	Yes [ ] N/A [ ]
*PMDE	PMD is 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, 100GBASE-KR2	135.5.7.2		APMD:O	Yes [ ] N/A [ ]
MD	MDIO	135.6	Registers and interface supported	O	Yes [ ] No [ ]

135.7.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.7.4.1 Functions

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Maintain lane mapping while link is in operation	135.5.2	Maintain sequence of PCSLs/FECLs on all output lanes	M	Yes [ ]

135.7.4.2 Timing

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP0 in Tx direction	135.5.3.1	≤ 29 ns	BPCS*PSIA:M	Yes [ ] N/A [ ]
S2	Skew Variation generation toward SP0 in Tx direction	135.5.3.1	≤ 200 ps	BPCS*PSIA:M	Yes [ ] N/A [ ]
S3	Skew Variation tolerance at SP0	135.5.3.2	Minimum 200 ps	AFEC*PSIA:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP1 in Tx direction	135.5.3.3	≤ 29 ns	BFEC*PSIA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
S5	Skew Variation generation toward SP1 in Tx direction	135.5.3.3	≤ 200 ps	BFEC*PSIA:M	Yes [ ] N/A [ ]
S6	Skew Variation tolerance at SP1	135.5.3.4	Minimum 200 ps	APMD*PSIA:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP2 in Tx direction	135.5.3.5	≤ 43 ns	APMD*PSID:M	Yes [ ] N/A [ ]
S8	Skew Variation generation toward SP2 in Tx direction	135.5.3.5	≤ 400 ps	APMD*PSID:M	Yes [ ] N/A [ ]
S9	Skew Variation tolerance at SP5	135.5.3.6	Minimum 3.6 ns	APMD*PSID:M	Yes [ ] N/A [ ]
S10	Skew generation toward SP6 in Rx direction	135.5.3.7	≤ 160 ns	(BFEC+APMD)* PSIA:M	Yes [ ] N/A [ ]
S11	Skew Variation generation toward SP6 in Rx direction	135.5.3.7	≤ 3.8 ns	(BFEC+APMD)* PSIA:M	Yes [ ] N/A [ ]
S12	Skew Variation tolerance at SP6	135.5.3.8	Minimum 3.8 ns	BFEC*PSIA:M	Yes [ ] N/A [ ]
S13	Skew generation toward SP7 in Rx direction	135.5.3.9	≤ 160 ns	AFEC*PSIA:M	Yes [ ] N/A [ ]
S14	Skew Variation generation toward SP7 in Rx direction	135.5.3.9	≤ 3.8 ns	AFEC*PSIA:M	Yes [ ] N/A [ ]
S15	Skew Variation tolerance at SP7	135.5.3.10	Minimum 3.8 ns	BPCS*PSIA:M	Yes [ ] N/A [ ]
S16	Round-trip delay limit for 50GBASE-R	135.5.4	No more than 18 432 bit times or 36 pause_quanta	P50:M	Yes [ ] N/A [ ]
S17	Round-trip delay limit for 100GBASE-P	135.5.4	No more than 36 864 bit times or 72 pause_quanta	P100:M	Yes [ ] N/A [ ]

135.7.4.3 Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Lane signaling rate for LAUI-2	135.1.4	25.78125 GBd	50GL:M	Yes [ ] N/A [ ]
E2	Lane signaling rate for 50GAUI-n, 100GAUI-n	135.1.4	26.5625 GBd	50GA1+50GA2+ 100GA2+ 100GA4:M	Yes [ ] N/A [ ]
E3	Lane signaling rate for one-lane 50 Gb/s PMD service interface	135.1.4	26.5625 GBd	APMD*50G:M	Yes [ ] N/A [ ]
E4	Lane signaling rate for two-lane 100 Gb/s PMD service interface	135.1.4	26.5625 GBd	APMD*100G* NLD=2:M	Yes [ ] N/A [ ]
E5	Lane signaling rate for one-lane 100 Gb/s PMD service interface	135.1.4	53.125 GBd	APMD*100G* NLD=1:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
E6	Electrical and timing requirements of Annex 135B met by LAUI-2	135.5.1, 135.5.5		50GL* (AT=C2C):M	Yes [ ] N/A [ ]
E7	Electrical and timing requirements of Annex 135D met by 50GAUI-2 or 100GAUI-4	135.5.1, 135.5.6		(50GA2+ 100GA4)* (AT=C2C):M	Yes [ ] N/A [ ]
E8	Electrical and timing requirements of Annex 135E met by 50GAUI-2 or 100GAUI-4	135.5.1, 135.5.6		(50GA2+ 100GA4)* (AT=C2M):M	Yes [ ] N/A [ ]
E9	Electrical and timing requirements of Annex 135F met by 50GAUI-1 or 100GAUI-2	135.5.1, 135.5.6		(50GA1+ 100GA2)* (AT=C2C):M	Yes [ ] N/A [ ]
E10	Electrical and timing requirements of Annex 135G met by 50GAUI-1 or 100GAUI-2	135.5.1, 135.5.6		(50GA1+ 100GA2)* (AT=C2M):M	Yes [ ] N/A [ ]

135.7.4.4 Diagnostics

Item	Feature	Subclause	Value/Comment	Status	Support
*LBL	PMA local loopback	135.5.8	Supports local loopback	O	Yes [ ] No [ ]
*LBR	PMA remote loopback	135.5.9	Supports remote loopback	O	Yes [ ] No [ ]
D1	PMA local loopback implemented	135.5.8	Meets the requirements of 135.5.8	LBL:M	Yes [ ] N/A [ ]
D2	PMA remote loopback implemented	135.5.9	Meets the requirements of 135.5.9	LBR:M	Yes [ ] N/A [ ]
D3	Send PRBS31 Tx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]
D4	Send PRBS31 Rx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]
D5	Check PRBS31 Tx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]
D6	Check PRBS31 Rx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]

Item	Feature	Subclause	Value/Comment	Status	Support
D7	Send PRBS9 Tx	135.5.10.1.2		NRZ:O	Yes [ ] No [ ] N/A[ ]
D8	Send PRBS9 Rx	135.5.10.1.2		NRZ:O	Yes [ ] No [ ] N/A[ ]
D9	Send NRZ square wave Tx	135.5.10.1.3		NRZ:O	Yes [ ] No [ ] N/A[ ]
D10	Send PRBS13Q Tx	135.5.10.2.1		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D11	Send PRBS13Q Rx	135.5.10.2.1		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D12	Send PRBS31Q Tx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D13	Send PRBS31Q Rx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D14	Check PRBS31Q Tx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D15	Check PRBS31Q Rx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D16	Send SSPRQ Tx	135.5.10.2.3		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D17	Send quaternary square wave Tx	135.5.10.2.4		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]

135.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
C1	PMA supports Gray coding	135.5.7.1		PAM4A+PAM4D:M	Yes [ ] N/A [ ]
C2	PMA supports output precoding for physically instantiated PMA service interface	135.5.7.2		(50GA1+100GA2)* (AT=C2C):M	Yes [ ] N/A [ ]
C3	PMA supports input precoding for physically instantiated PMA service interface	135.5.7.2		(50GA1+100GA2)* (AT=C2C):O	Yes [ ] No [ ] N/A [ ]
C4	PMA supports output precoding for PMD service interface	135.5.7.2		PMDE:M	Yes [ ] N/A [ ]
C4	PMA supports input precoding for PMD service interface	135.5.7.2		PMDE:O	Yes [ ] No [ ] N/A [ ]

136. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.1 Overview

This clause specifies the 50GBASE-CR PMD, the 100GBASE-CR2 PMD, the 200GBASE-CR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

There are four associated annexes. Annex 136A provides information on parameters with test points that may not be testable in an implemented system. Annex 136B specifies test fixtures. Annex 136C specifies MDIs. Annex 136D describes 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 host and cable assembly form factors.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 136–1, to the appropriate sublayers (as specified in Table 136–1, Table 136–2, and Table 136–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 136–1—Physical Layer clauses associated with the 50GBASE-CR PMD

Associated clause	50GBASE-CR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

Table 136–2—Physical Layer clauses associated with the 100GBASE-CR2 PMD

Associated clause	100GBASE-CR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 136–3—Physical Layer clauses associated with the 200GBASE-CR4 PMD

Associated clause	200GBASE-CR4
117—RS	Required
117—200GMII[a]	Optional
118—200GMII extender	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

For the 50GBASE-CR and 100GBASE-CR2 PHYs, in order to support the required frame loss ratio (see 1.4.275) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if

there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

For the 200GBASE-CR4 PHY, in order to support the required frame loss ratio (see 1.4.275) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant cable assembly.

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 136–1 shows the relationship of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD sublayers and MDIs to the ISO/IEC Open System Interconnection (OSI) reference model.

136.2 Conventions

Clause 136 describes three PMDs, 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-CR, n = 2 for 100GBASE-CR2, and n = 4 for 200GBASE-CR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term "PMD" refers to any of 50GBASE-CR PMD, 100GBASE-CR2 PMD, or 200GBASE-CR4 PMD.

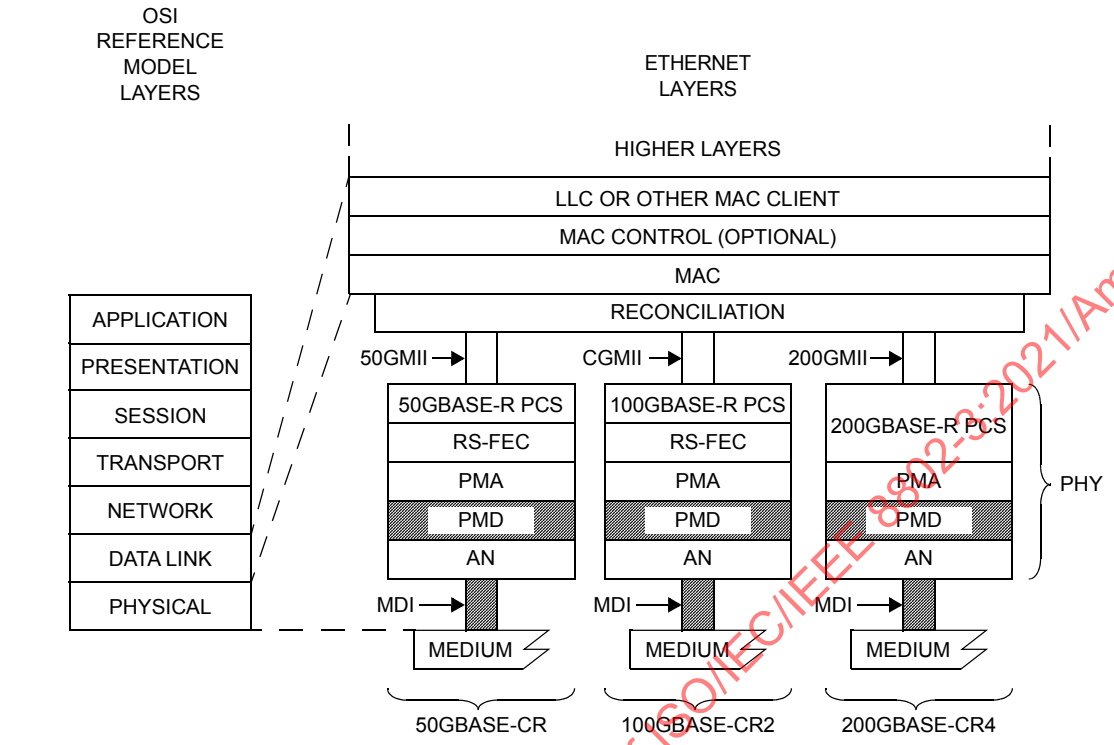
136.3 PMD service interface

This subclause specifies the services provided by the 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-CR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-CR2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with the exception that there are two parallel symbol streams (n = 2).

The 200GBASE-CR4 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with four parallel symbol streams (n = 4).



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 136–1—50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-CR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-CR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-CR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends *n* streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 136.8.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_*i*.indication parameter is undefined.

136.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCSs associated with the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs are required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 133.4, 82.6, and 119.5a.)

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR-4 PHYs may be extended using chip-to-chip (C2C) 50GAUI-n/LAUI-2, 100GAUI-n/CAUI-n, and 200GAUI-n, respectively, as physical instantiations of the inter-sublayer service interface between devices. If such extension is used, then the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

136.5 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 136–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 136–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-CR	2048	4	40.96
100GBASE-CR2	4096	8	40.96
200GBASE-CR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-CR, 10 ps for 100GBASE-CR2, and 5 ps for 200GBASE-CR4. (See 1.4.160 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-CR, 5.12 ns for 100GBASE-CR2, and 2.56 ns for 200GBASE-CR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-CR, in 80.4 for 100GBASE-CR2, and in 116.4 for 200GBASE-CR4.

136.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

136.6.1 Skew Constraints for 50GBASE-CR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

136.6.2 Skew Constraints for 100GBASE-CR2 and 200GBASE-CR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

136.7 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD

control variables as shown in Table 136–5, and MDIO status bits to PMD status variables as shown in Table 136–6.

Table 136–5—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 2[a]	PMD transmit disable	1.9.4:3	PMD_transmit_disable_3, PMD_transmit_disable_2
PMD transmit disable 1[b]	PMD transmit disable	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable	1.9.1	PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3[a]	PMD training pattern lane 3	1.1453.12:11	identifier_3
Seed 3[a]	PMD training pattern lane 3	1.1453.15:14 1.1453.10:0	seed_3
Polynomial identifier 2[a]	PMD training pattern lane 2	1.1452.12:11	identifier_2
Seed 2[a]	PMD training pattern lane 2	1.1452.15:14 1.1452.10:0	seed_2
Polynomial identifier 1[b]	PMD training pattern lane 1	1.1451.12:11	identifier_1
Seed 1[b]	PMD training pattern lane 1	1.1451.15:14 1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern lane 0	1.1450.12:11	identifier_0
Seed 0	PMD training pattern lane 0	1.1450.15:14 1.1450.10:0	seed_0
Initial condition request 3[a]	BASE-R PAM4 PMD training LP control, lane 3	1.1123.13:12	ic_req
Coefficient select 3[a]	BASE-R PAM4 PMD training LP control, lane 3	1.1123.4:2	coef_sel
Coefficient request 3[a]	BASE-R PAM4 PMD training LP control, lane 3	1.1123.1:0	coef_req
Initial condition request 2[a]	BASE-R PAM4 PMD training LP control, lane 2	1.1122.13:12	ic_req
Coefficient select 2[a]	BASE-R PAM4 PMD training LP control, lane 2	1.1122.4:2	coef_sel
Coefficient request 2[a]	BASE-R PAM4 PMD training LP control, lane 2	1.1122.1:0	coef_req
Initial condition request 1[b]	BASE-R PAM4 PMD training LP control, lane 1	1.1121.13:12	ic_req
Coefficient select 1[b]	BASE-R PAM4 PMD training LP control, lane 1	1.1121.4:2	coef_sel

Table 136–5—MDIO/PMD control variable mapping *(continued)*

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Coefficient request 1[b]	BASE-R PAM4 PMD training LP control, lane 1	1.1121.1:0	coef_req
Initial condition request 0	BASE-R PAM4 PMD training LP control, lane 0	1.1120.13:12	ic_req
Coefficient select 0	BASE-R PAM4 PMD training LP control, lane 0	1.1120.4:2	coef_sel
Coefficient request 0	BASE-R PAM4 PMD training LP control, lane 0	1.1120.1:0	coef_req

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

Table 136–6—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 2[a]	PMD receive signal detect	1.10.4:3	PMD_signal_detect_3 to PMD_signal_detect_2
PMD receive signal detect 1[b]	PMD receive signal detect	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect	1.10.1	PMD_signal_detect_0
Receiver status 3[a]	BASE-R PMD status	1.151.12	local_trained_3
Frame lock 3[a]	BASE-R PMD status	1.151.13	local_tf_lock_3
Start-up protocol status 3[a]	BASE-R PMD status	1.151.14	training_3
Training failure 3[a]	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2[a]	BASE-R PMD status	1.151.8	local_trained_2
Frame lock 2[a]	BASE-R PMD status	1.151.9	local_tf_lock_2
Start-up protocol status 2[a]	BASE-R PMD status	1.151.10	training_2
Training failure 2[a]	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1[b]	BASE-R PMD status	1.151.4	local_trained_1
Frame lock 1[b]	BASE-R PMD status	1.151.5	local_tf_lock_1
Start-up protocol status 1[b]	BASE-R PMD status	1.151.6	training_1
Training failure 1[b]	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	local_trained_0

Table 136–6—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Frame lock 0	BASE-R PMD status	1.151.1	local_tf_lock_0
Start-up protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0
Receiver ready[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.15	remote_rx_ready
Modulation and precoding status[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.11:10	remote_tp_mode
Receiver frame lock[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.9	remote_tf_lock
Initial condition status[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.8	ic_sts
Coefficient status[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.2:0	coef_sts
Receiver ready[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.15	remote_rx_ready
Modulation and precoding status[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.11:10	remote_tp_mode
Receiver frame lock[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.9	remote_tf_lock
Initial condition status[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.8	ic_sts
Coefficient status[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.2:0	coef_sts
Receiver ready[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.15	remote_rx_ready
Modulation and precoding status[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.11:10	remote_tp_mode
Receiver frame lock[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.9	remote_tf_lock
Initial condition status[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.8	ic_sts
Coefficient status[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.2:0	coef_sts
Receiver ready	BASE-R PAM4 PMD training LP status, lane 0	1.1220.15	remote_rx_ready
Modulation and precoding status	BASE-R PAM4 PMD training LP status, lane 0	1.1220.11:10	remote_tp_mode

Table 136–6—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Receiver frame lock	BASE-R PAM4 PMD training LP status, lane 0	1.1220.9	remote_tf_lock
Initial condition status	BASE-R PAM4 PMD training LP status, lane 0	1.1220.8	ic_sts
Coefficient status	BASE-R PAM4 PMD training LP status, lane 0	1.1220.2:0	coef_sts

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

136.8 PMD functional specifications

136.8.1 Link block diagram

One direction of a 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 link is shown in Figure 136–2.

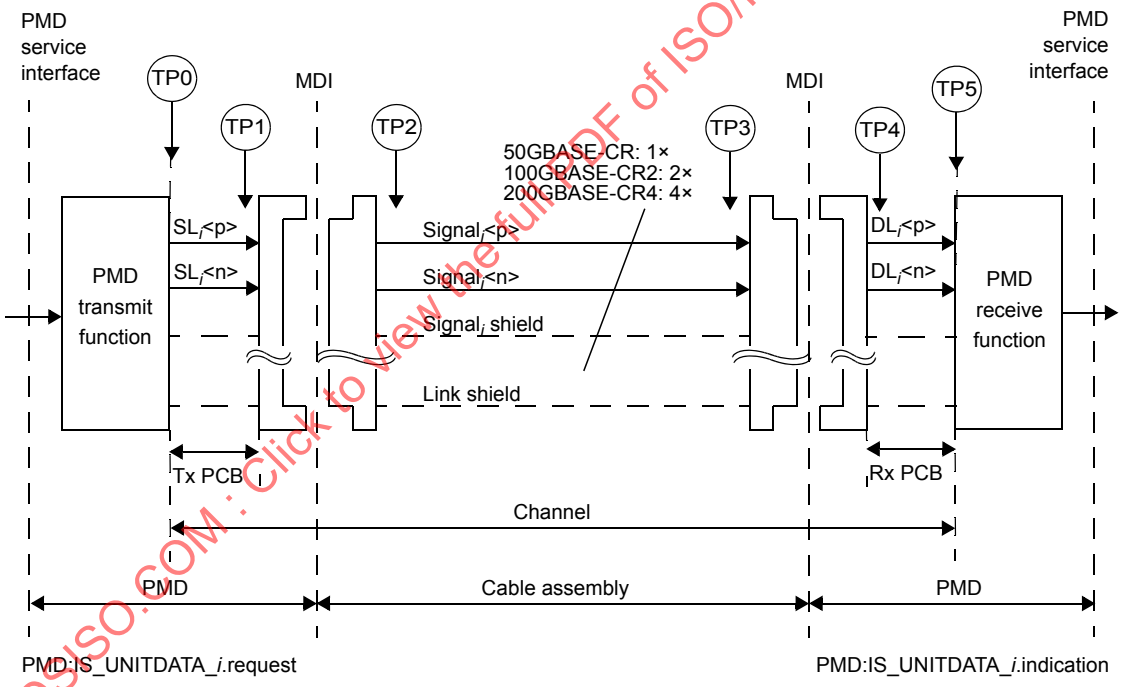


Figure 136–2—50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 link (one direction is illustrated)

Note that the source lane (SL) signals SL_i<p> and SL_i<n> are the positive and negative sides of the transmitter's differential signal pair on lane *i* and the destination lane (DL) signals DL_i<p> and DL_i<n> are the positive and negative sides of the receiver's differential signal pair on lane *i*.

For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause.

The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 136.9.3 are made at TP2 utilizing the test fixture specified in Annex 136B.

The electrical receive signal is defined at TP3. Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are performed at TP3 utilizing the test fixture specified in Annex 136B.

A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is provided in 136.9.3.2. Annex 136A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system.

The channel (see 136.10) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 136–2. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of 136B.1, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4. Two cable assembly test fixtures have been included in the cable assembly specifications defined in 136.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0 and the MDI and between the MDI and TP5, respectively, are provided informatively in 136A.4.

Table 136–7 describes the defined test points illustrated in Figure 136–2.

Table 136–7—Test points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of Annex 136B, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 136.9.3.2.
TP2	Unless specified otherwise, all transmitter measurements defined in 136.9.3 are made at TP2 utilizing the test fixture specified in Annex 136B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are made at TP3 utilizing the test fixture specified in Annex 136B.

136.8.2 PMD transmit function

The PMD transmit function has two operating modes, DATA and TRAINING. The operating mode is controlled by the PMD control state diagram (Figure 136–7).

When operating in DATA mode, the PMD transmit function shall convert the symbol stream requested by the PMD service interface message PMD:IS_UNITDATA_*i*.request(tx_symbol) of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical

specifications in 136.9.3. The differential output voltage (SL_i<p> minus SL_i<n>) meets the specifications in 136.9.3.1.1 where the PAM4 symbol values 0, 1, 2, and 3 correspond to the tx_symbol values zero, one, two, and three, respectively, with the highest differential output voltage corresponding to tx_symbol = three and the lowest differential output voltage corresponding to tx_symbol = zero.

When operating in TRAINING mode, the PMD transmit function shall convert the symbol stream generated by the PMD control function of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The differential output voltage (SL_i<p> minus SL_i<n>) meets the specifications in 136.9.3.1.1, with the highest differential output voltage corresponding to the PAM4 symbol 3 and the lowest differential output voltage corresponding to the PAM4 symbol 0.

136.8.3 PMD receive function

The PMD receive function shall convert the electrical signal from each of the lanes on the MDI into a symbol stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication(rx_symbol). The highest differential input voltage (DL_i<p> minus DL_i<n>) shall correspond to rx_symbol = three and the lowest differential input voltage shall correspond to rx_symbol = zero.

136.8.4 PMD global signal detect function

For the 50GBASE-CR PMD, the variable Global_PMD_signal_detect is set to PMD_signal_detect_0 (see 136.8.5). For the 100GBASE-CR2 and 200GBASE-CR4 PMDs, the variable Global_PMD_signal_detect is set to the logical AND of the values of PMD_signal_detect_*i* from each of the PMD lanes.

136.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the PMD to indicate the successful completion of the start-up protocol by the PMD control function (see 136.8.11). PMD_signal_detect_*i* shall be set to zero when signal_detect on lane *i* is set to false, and to one when signal_detect on lane *i* is set to true. The signal_detect variables are set independently on each lane by the PMD control state diagram (Figure 136–7).

If training is disabled by the management variable mr_training_enable (see 136.7), PMD_signal_detect_*i* shall be set to one for all lanes.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 136.7.

136.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. When implemented, it allows the transmitters on all lanes to be disabled with a single variable.

When Global_PMD_transmit_disable variable is set to one, this function shall turn off all the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

If a PMD fault (136.8.8) is detected, then the PMD may set Global_PMD_transmit_disable to one.

136.8.7 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

— When a PMD_transmit_disable_*i* variable is set to one, this function shall turn off the transmitter in lane *i* so that it drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

— If a PMD fault (136.8.8) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the transmitter in each lane.

136.8.8 PMD fault function

PMD_fault is the logical-OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO interface is implemented, then PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

136.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

136.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

136.8.11 PMD control function

The PMD control function performs the PMD start-up protocol. This protocol facilitates timing recovery and equalization while providing a mechanism through which the receiver can configure the transmitter to optimize performance. The protocol supports these functions through the continuous exchange of fixed-length training frames.

The PMD shall implement one instance of the PMD control function described in this subclause for each lane. The PMD control functions operate independently on each lane.

136.8.11.1 Training frame structure

The training frame is a sequence of PAM4 symbols whose values correspond to the possible values of the tx_symbol and rx_symbol variables (the PAM4 symbol values 0, 1, 2, and 3 correspond to tx_symbol or rx_symbol values zero, one, two, and three, respectively). The structure of a training frame is shown in Figure 136–3.

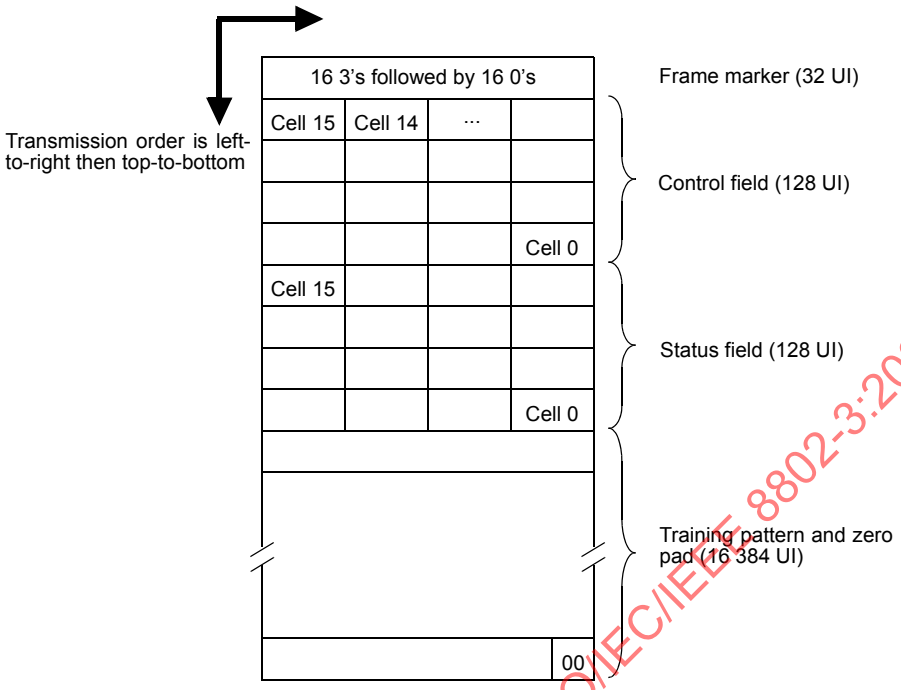


Figure 136–3—Training frame structure

136.8.11.1.1 Frame marker

Training frames are delimited by a specific sequence of PAM4 symbols. The training frame marker is a run of 16 consecutive "3" symbols followed by a run of 16 consecutive "0" symbols. This sequence is not found in the control field, status field, or training pattern and it uniquely identifies the beginning of a training frame.

136.8.11.1.2 Control and status fields

The control field comprises 16 bits with the structure defined in 136.8.11.2. The status field comprises 16 bits with the structure defined in 136.8.11.3.

Each bit of the control and status fields is sent as a differential Manchester encoded (DME) cell, where each cell is eight unit intervals in length. The specific rules for this encoding follow.

a) A transition from 0 to 3 or from 3 to 0 occurs at the start of each cell.
b) A transition from 0 to 3 or from 3 to 0 at the midpoint of a cell, i.e., four unit intervals from the transition at the beginning of the cell, corresponds to a logical one.
c) The absence of a transition at the midpoint of a cell corresponds to a logical zero.

The control field is transmitted immediately after the frame marker. The status field is transmitted immediately after the control field. Within each field, the order of transmission is from bit 15 to bit 0.

When a training frame is received, if a violation of the DME encoding rules is detected within the control field or the status field, the contents of both fields in that frame are ignored.

136.8.11.1.3 Training pattern

The training pattern is the result of a training pattern generator equivalent to the structure shown in Figure 136–4.

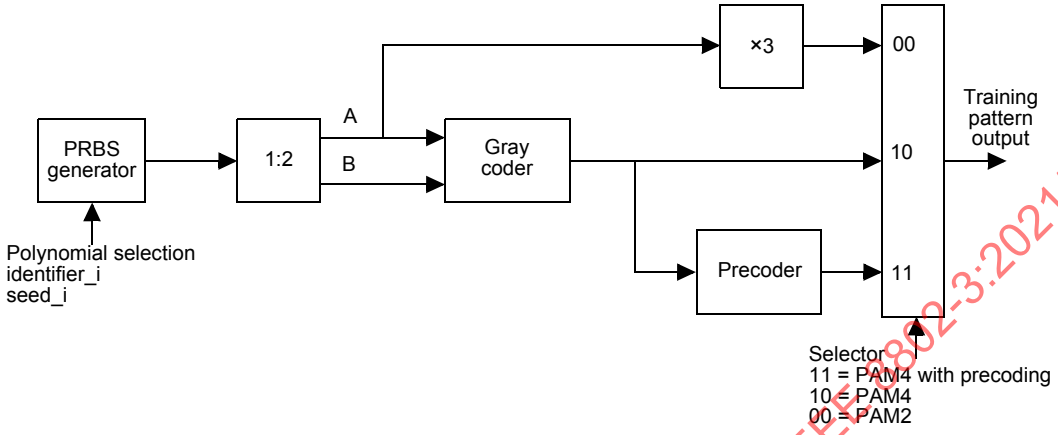


Figure 136–4—Training pattern generator

A set of four PRBS generator polynomials are defined to minimize correlated interference between PMDs, or physical lanes within a PMD, during the start-up protocol. The PRBS generator for each lane shall implement each of four generator polynomials defined in Table 136–8. The polynomial used in each lane *i* is selectable by identifier_*i*. The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0). A sample implementation of the PRBS generator for identifier_*i* = 0 is shown in Figure 136–5.

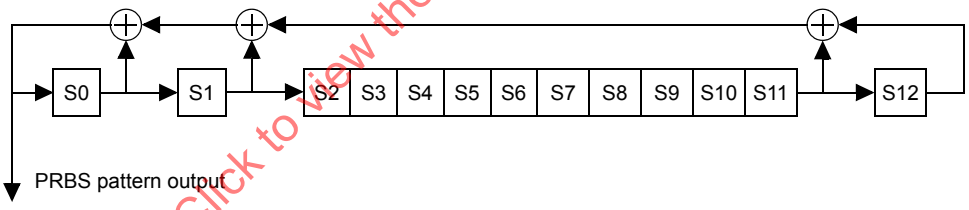


Figure 136–5—Training pattern PRBS generator (identifier_*i* = 0)

At the start of the training pattern, the state of the PRBS generator shall be set to the value seed_*i*. The default value of seed_*i* shall be the value given in Table 136–8 for $p = i$. A seed of all zeros is not valid.

The polynomials for each identifier value *p* and the default seeds, as well as the first 13 symbols of the training pattern for each modulation and precoding mode, using the default seed, are provided in Table 136–8.

Table 136–8—Training patterns

p	Polynomial_*p*, *G*(*x*)	Default seed bits[a]	Initial output, PAM2	Initial output, PAM4	Initial output, PAM4 with precoding
0	$1+x+x^2+x^{12}+x^{13}$	0000010101011	0030330330000	1031320220111[b]	1301200200101
1	$1+x^2+x^3+x^7+x^{13}$	0011101000001	3030303030333	3030213021333	3122012201212
2	$1+x^2+x^4+x^8+x^{13}$	1001000101100	0303333033030	1212332133031	1102120121301
3	$1+x^2+x^5+x^9+x^{13}$	0100010000010	3330300030330	2231210121221	2032013201110

[a]The leftmost bit in the sequence corresponds to the initial value of S0 and the rightmost bit corresponds to the initial value of S12.
[b]This is equivalent to the PRBS13Q test pattern defined in 120.5.11.2.1.

For a given configuration of the PRBS generator, there are three possible training patterns. The construction of each training pattern begins by demultiplexing the PRBS generator output into pairs of bits {A, B} where A corresponds to the 1st, 3rd, 5th, etc. bits output by the PRBS generator and B corresponds to the 2nd, 4th, 6th, etc. bits output by the PRBS generator. There is a new pair of bits each unit interval which implies that the PRBS generator is required to generate bits at twice the signaling rate. Given these pairs of bits, the three different training patterns correspond to three modulation and precoding modes: PAM2, PAM4, PAM4 with precoding.

When the modulation and precoding mode is set to PAM2, the training pattern is the sequence of 16 382 PAM4 symbols derived by mapping only the A bits such that logical 0 is transmitted as 0 and logical 1 is transmitted as 3.

When the modulation and precoding mode is set to PAM4, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1.

When the modulation and precoding mode is set to PAM4 with precoding, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1 and precoding the result as specified in 135.5.7.2. The precoder state is initialized to 0 at the beginning of each training pattern, so that P(j–1)=0 in Equation (135–1) for the first PAM4 symbol of the training pattern.

The modulation and precoding mode is set to PAM2 upon entry to the INITIALIZE state of the PMD control state diagram (see Figure 136–7).

NOTE—Exiting TRAINING mode requires both sides to use PAM4 modulation, thus the request and the status of the modulation and precoding are both required to have values other than PAM2 (either “PAM4” or “PAM4 with precoding”).

136.8.11.1.4 Zero pad

Two “0” symbols are transmitted immediately after the training pattern. This zero pad ensures the training frame is DC balanced and helps to delineate the start of the frame marker for the next training frame.

136.8.11.2 Control field structure

The structure of the control field shall be as shown in Table 136–9.

Table 136–9—Control field structure

Bit(s)	Name	Description
15:14	Reserved	Transmit as 0, ignore on receipt
13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control
11:10	Reserved	Transmit as 0, ignore on receipt
9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
7:5	Reserved	Transmit as 0, ignore on receipt
4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold

136.8.11.2.1 Initial condition request

The initial condition request bits are used to select one of the three predefined transmitter equalizer configurations (presets) specified in 136.9.3.1.3. When the initial condition request bits are 00, the coefficient select and coefficient request bits are used to update the transmitter equalizer configuration.

136.8.11.2.2 Modulation and precoding request

The modulation and precoding request bits are used to request that the link partner transmitter transmit one of the three training pattern formats defined in 136.8.11.1.3.

136.8.11.2.3 Coefficient select

The coefficient select bits are used to identify the coefficient that is the target of a coefficient request. The value of the field is the two's complement encoding of the coefficient index. For example, binary value 111 corresponds to a coefficient index of –1.

136.8.11.2.4 Coefficient request

The coefficient request bits are used to change the value of the coefficient specified by the coefficient select bits. A coefficient may be changed by incrementing or decrementing its value or by setting it to "No equalization". The "No equalization" value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.

136.8.11.3 Status field structure

The structure of the status field is shown in Table 136–10.

Table 136–10—Status field structure

Bit(s)	Name	Description
15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue
14:12	Reserved	Transmit as 0, ignore on receipt
11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified
8	Initial condition status	1 = Updated 0 = Not updated
7	Parity	Even parity bit
6	Reserved	Transmit as 0, ignore on receipt
5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated

136.8.11.3.1 Receiver ready

The receiver ready bit is used to signal the local receiver state to the link partner. When this bit is 1, it indicates that the local receiver has completed training and is prepared to receive data (local_rx_ready = true). When this bit is 0, it indicates that the local receiver is requesting that training continue (local_rx_ready = false).

136.8.11.3.2 Modulation and precoding status

The modulation and precoding status bits encode the value of local_tp_mode.

136.8.11.3.3 Receiver frame lock

When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 136.8.11.6 are met.

Receiver frame lock shall be set to 0 when the variable training is false, and shall not be set to 1 until training and local_tf_lock are both true.

136.8.11.3.4 Initial condition status

The initial condition status bit acknowledges the initial condition request bits received from the link partner. The acknowledgment reflects the value of ic_sts resulting from the procedure described in 136.8.11.4.1.

136.8.11.3.5 Parity bit

The parity bit is calculated based on the other bits in the control field and status field to create even parity for these fields. Even parity ensures that the transmitted control and status fields (see 136.8.11.1.2) are DC balanced. This field is ignored on receipt.

136.8.11.3.6 Coefficient select echo

The coefficient select echo bits acknowledge the coefficient select bits received from the link partner. When a change to the coefficient select bits is detected, the coefficient select echo bits are updated to represent the same coefficient index. This serves as a confirmation to the link partner that subsequent coefficient requests will act on the targeted coefficient.

136.8.11.3.7 Coefficient status

The coefficient status bits acknowledge the coefficient request bits received from the link partner. The acknowledge reflects the value of coef_sts resulting from the procedure described in 136.8.11.4.3.

136.8.11.4 Equalization control

When the PMD control state diagram (Figure 136–7) is in the TRAIN_LOCAL state, a PMD may request its link partner to change the transmitter equalization coefficients, either to predefined initial conditions or by individual coefficient control. The criteria for initiating such requests are implementation dependent.

A new individual coefficient update request or initial condition update request is not initiated until after the prior request has completed.

136.8.11.4.1 Initial condition setting request process

A request to change the initial condition of the link partner's transmitter is made by using the following procedure:

a) Set the initial condition request bits (136.8.11.2.1) to the desired predefined transmitter equalizer configuration (preset) and the coefficient request bits (136.8.11.2.4) to "hold".
b) Wait until the initial condition status bits (136.8.11.3.4) indicate "updated" and the coefficient status bits (136.8.11.3.7) indicate "not updated".
c) Set the initial condition request bits (136.8.11.2.1) to individual coefficient control and the coefficient request bits (136.8.11.2.4) to "hold".
d) Wait until both the initial condition status bits (136.8.11.3.4) and the coefficient status bits (136.8.11.3.7) indicate "not updated".

136.8.11.4.2 Initial condition setting response process

The handling of incoming requests is specified by the coefficient update state diagram (Figure 136–9). The behavior of the UPDATE_IC function is consistent with the following algorithm.

```
if ic_req = ind_ctl
   ic_sts = not_upd
else
   if ic_req = preset 1
      Set coefficients to preset 1
   else if ic_req = preset 2
      Set coefficients to preset 2
   else if ic_req = preset 3
      Set coefficients to preset 3
   end if
   ic_sts = updated
end if
```

The variables ic_req and ic_sts are defined in 136.8.11.7.1. The transmitter equalizer coefficients corresponding to each of the three presets shall be within the ranges specified in Table 136–12.

The transmitter equalizer is set to preset 1 upon entry to the INITIALIZE state of the PMD control state diagram.

136.8.11.4.3 Coefficient update request process

A request to change an individual equalizer coefficient of the link partner's transmitter is made by using the following procedure:

a) In the transmitted control field, set the initial condition request bits (136.8.11.2.1) to individual control, and set the coefficient select bits (136.8.11.2.3) and coefficient request bits (136.8.11.2.4) to the desired values. This may be done in one step (all fields updated in the same training frame) or sequentially.

b) Wait until the received coefficient status bits (136.8.11.3.7) do not indicate "not updated" and the coefficient select echo bits (136.8.11.3.6) indicate the requested coefficient select value.

c) If the subsequent request is to change the same coefficient or request a new initial condition, set the coefficient request bits (136.8.11.2.4) to "hold" and wait until the received coefficient status bits (136.8.11.3.7) indicate "not updated".

136.8.11.4.4 Coefficient update response process

The handling of incoming requests is specified by the coefficient update state diagram (Figure 136–9). The behavior of the UPDATE_C(k) function is consistent with the following algorithm.

```
if k in k_list

   if coef_req = INCREMENT
      ck_ask = c(k) + ck_stp
   else if coef_req = DECREMENT
      ck_ask = c(k) - ck_stp
   else if coef_req = NO EQUALIZATION
      if k = 0
         ck_ask = 1
      else
         ck_ask = 0
      end if
   else
      ck_ask = c(k)
   end if

   if ck_ask > ck_max
      c(k) = ck_max
```

```
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICIENT AT LIMIT
      end if
   else if ck_ask < ck_min
      c(k) = ck_min
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICENT AT LIMIT
      end if
   else if CHECK_EQ(ck_ask,k)
      coef_sts = EQUALIZATION LIMIT
   else
      c(k) = ck_ask
      coef_sts = UPDATED
   end if
else
   coef_sts = COEFFICIENT NOT SUPPORTED
end if
```

The variables coef_req, coef_sts, and k are defined in 136.8.11.7.1. The following additional variables and functions are used.

c(k)
: Variable that contains the current value of the coefficient *c*(k).

ck_ask
: Variable that contains the value of *c*(k) that would result from the requested update.

ck_min
: Variable that contains the minimum supported value of *c*(k).

ck_max
: Variable that contains the maximum supported value of *c*(k).

ck_stp
: Variable that contains the magnitude of the change in *c*(k) for one step up or one step down from its current value.

k_list
: The set of valid transmitter equalizer coefficient indices {–2, –1, 0, 1}.

CHECK_EQ(ck_ask,k)
: Compares the transmitter's steady-state voltage that would result from setting transmit equalization coefficient *c*(k) value to ck_ask, while keeping all other coefficients unchanged, against the transmitter's steady-state voltage (see 136.9.3.1.2) and equalization capability. Returns true if the resulting combination of coefficients would exceed the maximum steady-state voltage or the transmitter's equalization capability. Otherwise returns false.

136.8.11.5 Modulation and precoding setting

When a change to the modulation and precoding request bits is detected, the modulation and precoding mode of the transmitted training pattern (see 136.8.11.1.3) is set accordingly, and the local_tp_mode variable is then set to the value of the modulation and precoding request bits to confirm that the change to the format of the training pattern was completed. local_tp_mode is encoded in the status field (see 136.8.11.3.2).

136.8.11.6 Handshake timing

Changes to the configuration of the transmitter equalizer or the transmitted training pattern may occur at any point between the time the request for the new configuration is received and the time that the request is acknowledged.

When the receiver frame lock bit in the status field of transmitted training frames is set to 1, the time from the receipt of a new request to the acknowledgment of that request shall be less than 2 ms. A new request is defined to be a received training frame whose control field differs from the control field of the preceding training frame. An acknowledgment is defined as the first transmitted training frame that contains a status field encoding that is an appropriate response for the requested action. For example, a change in the coefficient select bits in the control field would be acknowledged by a change in the coefficient select echo bits of the status field. Similarly, a change in the modulation and precoding request bits in the control field would be acknowledged by a change in the modulation and precoding status bits in the status field. All timing measurements are referred to a common reference point within the training frame (e.g., the 3 to 0 transition in the training frame marker).

The timing of requests and acknowledgment is illustrated in Figure 136–6.

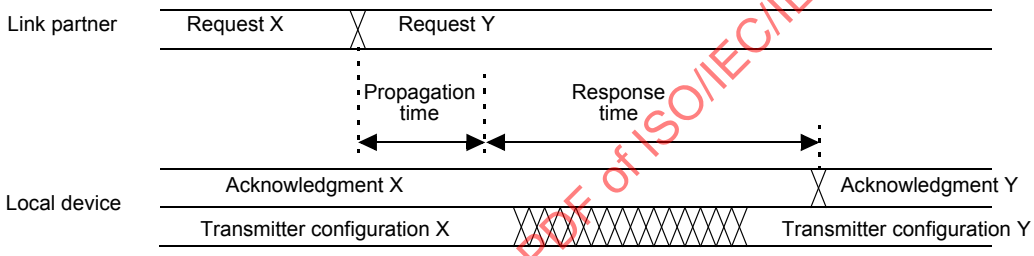


Figure 136–6—Transmitter update timing

136.8.11.7 Variables, functions, timers, counters, and state diagrams

The PMD implements one instance of each of the PMD control state diagrams, and the set of associated variables, functions, counters and timers defined in this subclause, independently for each of the n physical lanes.

136.8.11.7.1 Variables

coef_req

Enumerated variable derived from the “coefficient request” bits from the control field of the received training frames (see 136.8.11.2). This variable may be one of the following values: hold, decrement, increment, no equalization.

coef_sel

Variable derived from the “coefficient select” bits from the control field of the received training frames (see 136.8.11.2). It is assigned a signed integer value that is the two’s complement interpretation of the bits.

coef_sts

Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated, coefficient at limit, coefficient not supported, equalization limit, coefficient at limit and equalization limit. The value is assigned by the UPDATE_C(k) function and Coefficient update state diagram

(Figure 136–9), and then encoded in the status field of transmitted training frames via the ENCODE_STS function.

ic_req

Enumerated variable derived from the "initial condition request" bits from the control field of the received training frames (see 136.8.11.2). This variable may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): individual control (ind_ctl), preset 1, preset 2, preset 3.

ic_sts

Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated.

k

Variable that stores the most recent value of coef_sel.

local_rx_ready

Boolean variable that is set to true by the training state diagram when local_trained is asserted and is set to false otherwise. This value is encoded as the "receiver ready" bit in the status field of transmitted training frames.

local_tf_lock

Boolean variable that is true when the training frame marker positions have been identified and is false otherwise.

local_tp_mode

Enumerated variable that controls the modulation and precoding mode in the transmitted training pattern (see 136.8.11.1.3) and may be assigned one of the following values: pam2, pam4, pam4 with precoding.

local_trained

Boolean variable that is set to true when the local receiver has determined that the remote transmit and local receive equalizers have been optimized and normal data transmission may commence. It is set to false otherwise. The exact criteria for setting this variable to true are implementation specific.

marker_valid

Boolean variable that is set to true when the candidate frame marker matches the frame marker pattern defined in 136.8.11.1.1 and is set to false otherwise.

mr_restart_training

Boolean variable used by system management to restart the start-up protocol. When set to true, it forces the PMD control state diagram to the INITIALIZE state.

mr_training_enable

Boolean variable used by system management to enable or disable the start-up protocol. When set to true it enables the start-up protocol, and when set to false it disables the start-up protocol.

new_marker

Boolean variable that is set to true when a new candidate frame marker is available for testing and is set to false when the TEST_MARKER state is entered. A new frame marker is available for testing when the training frame lock process has accumulated 32 consecutive symbols starting at the candidate frame start position.

remote_rx_ready

Boolean variable derived from the "receiver ready" bit of the status field of received training frames. The value of remote_rx_ready shall not be set to TRUE until no fewer than three consecutive training frames have been received with the "receiver ready" bit asserted.

remote_tf_lock
: Boolean variable derived from the "receiver frame lock" bit of the status field of received training frames. The value of remote_tf_lock shall not be set to TRUE until no fewer than three consecutive training frames have been received with the "receiver frame lock" bit asserted.

remote_tp_mode
: Enumerated variable that corresponds to the "modulation and precoding status" bits in the status field of received training frames. It may be assigned one of the following values: pam2, pam4, pam4 with precoding.

reset
: Boolean variable that resets the PMD. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMD into low-power mode. It is false otherwise.

signal_detect
: Boolean variable that is set to true when the training process is complete and is set to false otherwise. The value of signal_detect is used by the PMD lane-by-lane signal detect function (136.8.5).

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the Training frame lock state diagram (Figure 136–8) is completed indicating that the next candidate frame sync position can be tested.

tf_offset
: Boolean variable that is set to true when receiving one full training frame (16 672 symbols, see 136.8.11.1) following the recent frame start position, such that a new frame marker is expected. Otherwise it is set to false

training
: Boolean variable that is set to true when the start-up protocol is in progress and is set to false otherwise.

training_failure
: Boolean variable that is set to true when training failed to complete successfully within the allotted time limit. Otherwise it is set to false.

136.8.11.7.2 Functions

ENCODE_STS
: Encodes portions of the status field of transmitted training frames. k is mapped to the coefficient select echo bits, coef_sts is mapped to the coefficient status bits, and ic_sts is mapped to the initial condition status bit.

SLIP
: Causes the next candidate frame marker position to be tested. Repeated invocations of SLIP cause all possible positions to be evaluated. The precise method for determining the next candidate frame marker position is implementation dependent and beyond the scope of this standard.

TRANSMIT(tx_mode)
: Controls the output of the PMD transmit function on the current lane. When tx_mode = DATA, the PMD transmit function output is the parameter of the PMD:IS_UNITDATA_*i*.request primitive (see 136.3). When tx_mode = TRAINING, the PMD transmit function output is the stream of symbols generated by the PMD control function.

UPDATE_C(k)
: Updates the value of *c*(k) based on the current values of the variables k and coef_req. The result of the update is stored in the variable coef_sts. This function implements the algorithm specified in 136.8.11.4.4.

UPDATE_IC
: Updates all transmit equalizer coefficients based on the current value of the variable ic_req. The result is stored in the variable ic_sts. This function implements the algorithm specified in 136.8.11.4.2.

136.8.11.7.3 Timers

holdoff_timer
: This timer is started when the PMD control state diagram enters the TIMEOUT state. The terminal count of holdoff_timer is 80 ms ± 2%.

max_wait_timer
: This timer sets the limit for how long the PMD start-up protocol is allowed to operate. It is started upon entry to the INITIALIZE state of the PMD control state diagram. If the timer expires before the LINK_READY state is reached, then a failure to train is indicated. The terminal count of max_wait_timer is 3 s ± 2%.

wait_timer
: This timer is started when the local receiver has completed training and detects that the remote receiver is ready to receive data. The local transmitter sends additional training frames until the timer expires to ensure that the link partner correctly detects the local receiver state. The terminal count of wait_timer is between 25 µs and 125 µs, equivalent to approximately 40 to 200 training frames.

136.8.11.7.4 Counters

bad_markers
: Count of the number of consecutive frame marker mismatches.

good_markers
: Count of the number of consecutive frame marker matches.

136.8.11.7.5 State diagrams

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter indicates that its value is to be incremented.

The PMD control state diagram (Figure 136–7) defines the operation of the start-up protocol.

If the LINK_READY state is entered with local_tp_mode set to “PAM4 with precoding”, then the PMD shall cause the adjacent PMA to transmit all subsequent data on the corresponding lane with precoding (see 135.5.7.2 and 120.5.7.2).

If the LINK_READY state is entered with remote_tp_mode set to “PAM4 with precoding”, then the PMD shall inform the adjacent PMA that all subsequently received data on the corresponding lane includes precoding (see 135.5.7.2 and 120.5.7.2).

The PMD control state diagram is supported by the training frame lock and coefficient update state diagrams. The training frame lock state diagram (Figure 136–8) determines when the PMD control function has detected training frame boundaries. The coefficient update state diagram (Figure 136–9) defines the process for updating the local transmitter equalizer coefficients in response to requests from the link partner.

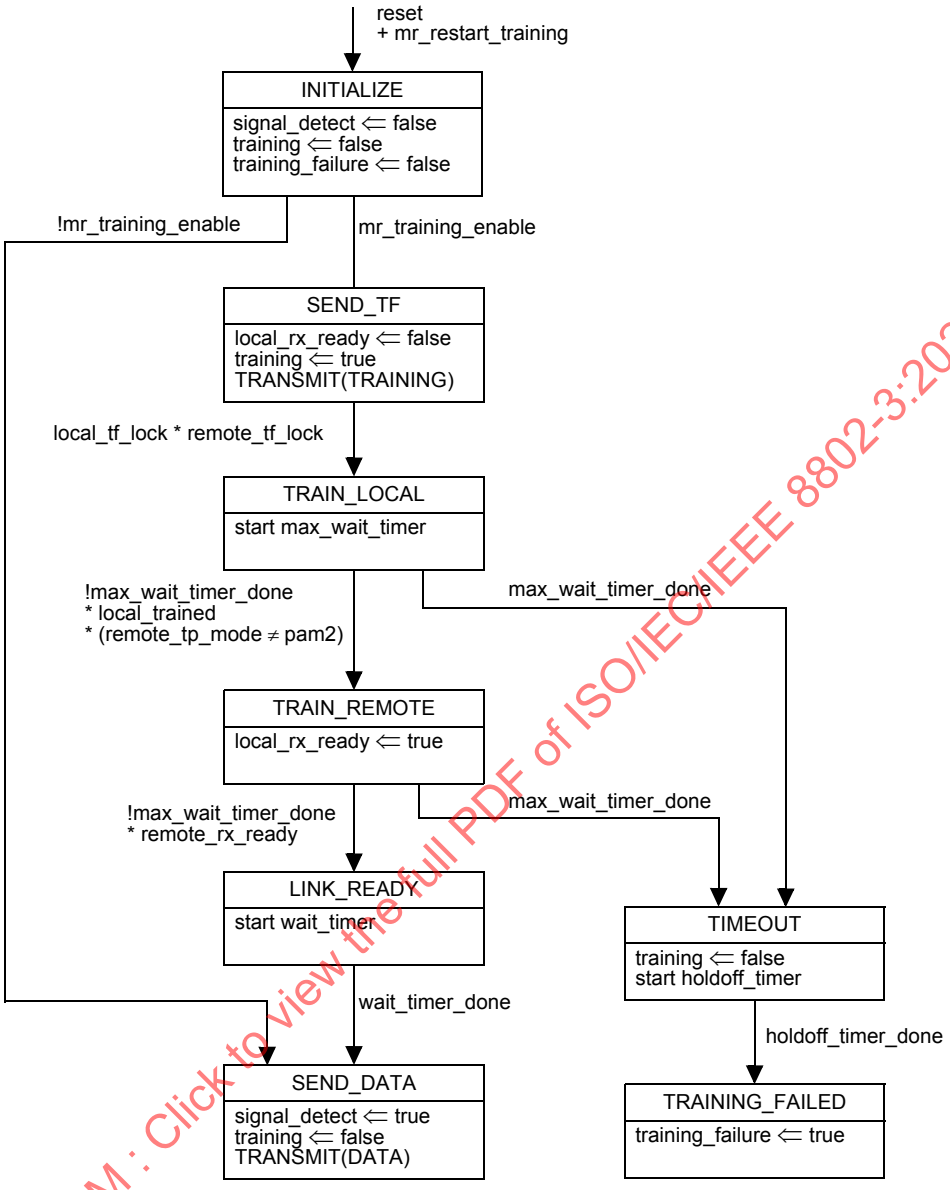


Figure 136–7—PMD control state diagram

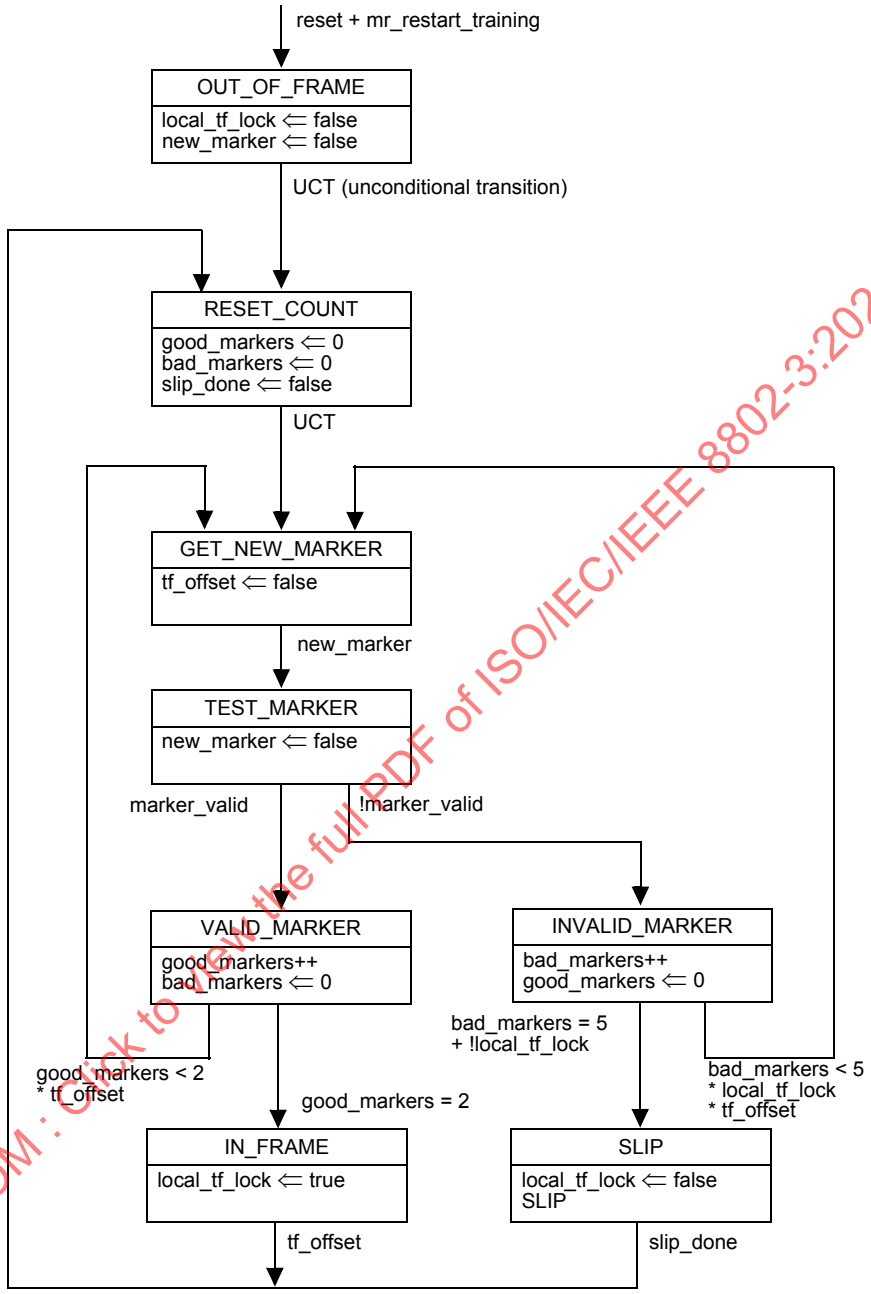


Figure 136–8—Training frame lock state diagram

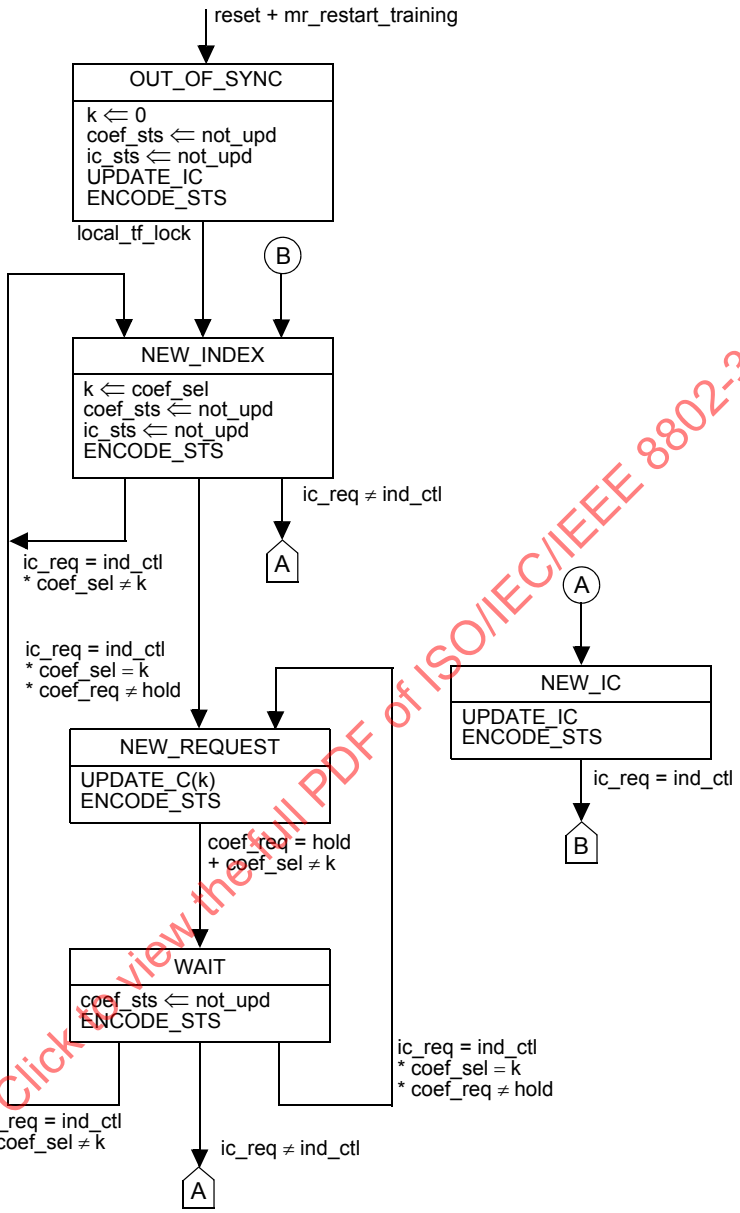


Figure 136–9—Coefficient update state diagram

136.9 PMD electrical characteristics

136.9.1 AC-coupling

Interoperability between PMD components operating from different supply voltages is facilitated by AC-coupling within the cable assembly (as specified in 136.11).

136.9.2 Signal paths

The MDI transmit and receive paths are point-to-point connections. Each path corresponds to one MDI lane and comprises two complementary signals, which form a balanced differential pair.

For 50GBASE-CR, there is one differential path in each direction for a total of two pairs, or four connections. For 100GBASE-CR2, there are two differential paths in each direction for a total of four pairs, or eight connections. For 200GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections.

136.9.3 Transmitter characteristics

The transmitter on each lane shall meet the specifications given in Table 136–11 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in Annex 136B, using a test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth. The connection from TP2 to the test equipment is AC-coupled.

Measurement of the DC common-mode voltage is made with a high-impedance connection to TP2 where each conductor of the differential pair is AC-coupled to a 50 Ω termination.

The transmitter characteristics at TP0 are provided informatively in 136A.2.

Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Differential pk-pk output voltage (max.) with Tx disabled[a]	93.8.1.3	30	mV
DC common-mode voltage (max.)[a]	93.8.1.3	1.9	V
AC common-mode RMS output voltage, v_{cmi} (max.)[a]	93.8.1.3	30	mV
Differential pk-pk voltage, v_{di} (max.)[a]	93.8.1.3	1200	mV
Effective return loss (ERL) (min.)	136.9.3.4	See Equation (136–6)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	136.9.3.1.2	0.354 0.6	V
Linear fit pulse peak (min.)	136.9.3.1.2	$0.49 \times v_f$	V
Level separation mismatch ratio R_{LM} (min.)	120D.3.1.2	0.95	—

Table 136–11—Summary of transmitter specifications at TP2 *(continued)*

Parameter	Subclause reference	Value	Units
Transmitter output waveform			
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (max.)	136.9.3.1.4	0.05	—
abs step size for $c(-2)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-2)$ (max.)	136.9.3.1.4	0.025	—
value at minimum state for $c(-1)$ and $c(1)$ (max.)	136.9.3.1.5	−0.25	—
value at maximum state for $c(-2)$ (min.)	136.9.3.1.5	0.1	—
Signal-to-noise-and-distortion ratio SNDR (min.)	120D.3.1.6	32.2	dB
Output jitter (max.)[b]			
J_{RMS}	120D.3.1.8	0.023	UI
J3u	136.9.3.3	0.115	UI
Even-odd jitter, pk-pk[c]	120D.3.1.8	0.019	UI
Signaling rate		26.5625 ± 100 ppm	GBd
Unit interval nominal		37.64706	ps

[a]Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.
[b]J3u, J_{RMS}, and even-odd jitter measurements are made with a single transmit equalizer setting selected to compensate for the loss of the host channel.
[c]If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

136.9.3.1 Transmitter output waveform

The transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer on each lane is the four-tap transversal filter shown in Figure 136–10.

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 136.8.11 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path. This command set includes instructions to increment, decrement, hold, or set to zero a selected coefficient $c(k)$, where $k = -2$ to 1. In addition, it includes commands to set all coefficients to one of three initial conditions.

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate the selected coefficient index k, the status of the coefficient $c(k)$ (updated, not updated, or at limit), and the status of the initial condition (updated or not updated).

136.9.3.1.1 Linear fit to the measured waveform

The following procedure is used to determine the linear fit pulse response, linear fit error, and normalized transmitter coefficient values.

Set the transmitter under test to transmit the PRBS13Q test pattern (defined in 120.5.11.2.1). For each configuration of the transmit equalizer, capture at least one complete cycle of the test pattern at TP2, as specified in 85.8.3.3.4. The clock recovery unit (CRU) used in the measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade.

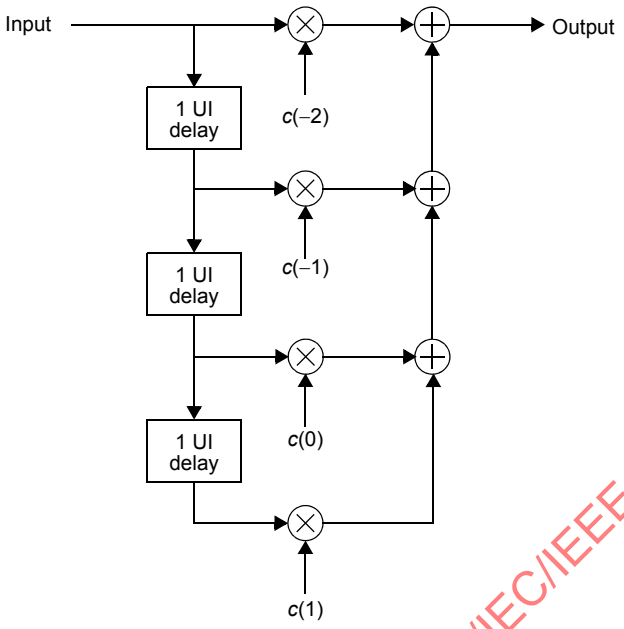


Figure 136–10—Transmit equalizer functional model

In the following calculations, M should be an integer not less than 32. Interpolation of the captured waveform may be used to achieve this.

Compute the linear fit pulse response $p(k)$, k=1 to $M \times N_p$, from the captured waveform, as specified in 85.8.3.3.5, with $N_p = 200$ and $D_p = 3$, where the aligned symbols $x(n)$ are assigned normalized amplitudes −1, $-ES$, ES, and 1 to represent the PAM4 symbol values 0, 1, 2, and 3 respectively. ES is defined as $(|ES1| + |ES2|)/2$ where $ES1$ and $ES2$ are calculated according to 120D.3.1.2.

Define $r(k)$ to be the linear fit pulse response when transmit equalizer coefficients have been set to the "pre-set 1" values. The normalized coefficients for any configuration of the transmit equalizer are computed using the following method.

For each value of m in the range $-M/2$ to $M/2-1$ when M is even and $-(M-1)/2$ to $(M-1)/2$ when M is odd:

a) Define an $M \times N_p$-by-4 matrix R_m. The elements of R_m are assigned values per Equation (136–1) where $i = -2$ to 1 and $j = 1$ to $M \times N_p$.

$$R_m(j, i+3) = \begin{cases} r(m+j-M\times i) & \text{if } 1 \le m+j-M\times i \le M\times N_p \\ 0 & \text{otherwise} \end{cases} \quad (136\text{–}1)$$

b) The normalized coefficients of the transmit equalizer are computed using Equation (136–2).

$$\begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} = (R_m^T R_m)^{-1} R_m^T \begin{bmatrix} p(1) \\ \dots \\ p(M\times N_p) \end{bmatrix} \quad (136\text{–}2)$$

c) The linear fit pulse response is reconstructed from the matrix R_m and the normalized coefficients using Equation (136–3).

$$\begin{bmatrix} p_m(1) \\ \dots \\ p_m(M \times N_p) \end{bmatrix} = R_m \begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} \quad (136\text{–}3)$$

d) $\varepsilon^2(m)$ is computed using Equation (136–4).

$$\varepsilon^2(m) = \sum_{k=1}^{M \times N_p} (p(k) - p_m(k))^2 \quad (136\text{–}4)$$

The normalized transmit equalizer coefficients $c(i)$ for a given linear fit pulse $p(k)$ are the values $c_m(i)$ for the value of m that minimizes $\varepsilon^2(m)$.

136.9.3.1.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(1)$ through $p(M \times N_v)$ divided by M (refer to 85.8.3.3 step 3), where N_v represents the number of symbols to take into account and has a value of 13. The steady-state voltage shall be greater than or equal to 0.354 V and less than or equal to 0.6 V after the transmit equalizer initial condition has been set to preset 1 (no equalization).

The peak value of $p(k)$ shall be greater than $0.49 \times v_f$ after the transmit equalizer initial condition has been set to preset 1 (no equalization).

136.9.3.1.3 Coefficient initialization

When the Coefficient update state diagram (Figure 136–9) is in either the OUT_OF_SYNC state or the NEW_IC state, the coefficients of the transmit equalizer shall be configured to values within the ranges specified in Table 136–12 (according to the value of the variable ic_req). These requirements apply upon the assertion of Initial condition status of "Updated".

Table 136–12—Coefficient initial conditions

Coefficient update state	ic_req	$c(-2)$	$c(-1)$	$c(0)$	$c(1)$
OUT_OF_SYNC	N/A	0 ± 0.025	0 ± 0.05	1 ± 0.05	0 ± 0.05
NEW_IC	preset 1	0 ± 0.025	0 ± 0.05	1 ± 0.05	0 ± 0.05
	preset 2	0 ± 0.025	–0.15 ± 0.05	0.75 ± 0.05	–0.1 ± 0.05
	preset 3	0 ± 0.025	–0.25 ± 0.05	0.75 ± 0.05	0 ± 0.05

136.9.3.1.4 Coefficient step size

When coef_sel is –1, 0, or 1, the change in the normalized transmit equalizer coefficient c(coef_sel) corresponding to a request to "increment" shall be between 0.005 and 0.05, and the change in the normalized

transmit equalizer coefficient *c*(coef_sel) corresponding to a request to "decrement" shall be between –0.05 and –0.005.

When coef_sel is –2, the change in the normalized transmit equalizer coefficient *c*(–2) corresponding to a request to "increment" shall be between 0.005 and 0.025, and the change in the normalized transmit equalizer coefficient *c*(coef_sel) corresponding to a request to "decrement" shall be between –0.025 and –0.005.

The coefficients other than *c*(coef_sel) are not expected to change. The absolute change in any coefficient other than *c*(coef_sel) shall be less than 0.005.

The change in the normalized transmit equalizer coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (i.e., coef_req is "Hold") and the value upon the assertion of a coefficient status of "updated".

136.9.3.1.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient reaches a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With *c*(−2) and *c*(−1) both set to zero and both *c*(0) and *c*(1) having received sufficient "decrement" requests so that they are at their respective minimum values, *c*(1) shall be less than or equal to −0.25.

With *c*(−2) and *c*(1) set to zero and both *c*(−1) and *c*(0) having received sufficient "decrement" requests so that they are at their respective minimum values, *c*(−1) shall be less than or equal to −0.25.

With *c*(−1) and *c*(1) set to zero, *c*(0) having received sufficient "decrement" requests so that it is at its minimum value, and *c*(−2) having received sufficient "increment" requests so that it is at its maximum value, *c*(−2) shall be greater than or equal to 0.1.

NOTE—A coefficient may be set to zero by asserting a coefficient request of "no equalization" for that coefficient, using the control function specified in 136.8.11, or by implementation specific means.

136.9.3.2 Insertion loss, TP0 to TP2 or TP3 to TP5

The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is given by Equation (136–5). Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.07 dB at 13.28 GHz.

$$Insertion\_loss(f) \le \begin{cases} 0.08 + 0.57\sqrt{f} + 0.596f & 0.01 \le f < 14 \\ -19.109 + 2.119f & 14 \le f \le 19 \end{cases} \text{ (dB)} \qquad (136\text{–}5)$$

136.9.3.3 J3u jitter

J3u is calculated from a jitter measurement specified in 120D.3.1.8.1. J3u is defined as the time interval that includes all but 10^{-3} of $f_J(t)$, from the 0.05th to the 99.95th percentile of $f_J(t)$.

136.9.3.4 Transmitter effective return loss (ERL)

ERL of the transmitter at TP2 is computed using the procedure in 93A.5 with the values in Table 136–13. Parameters that do not appear in Table 136–13 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the TP2 test fixture being used. N_{bx} is set to the value of N_b in Table 136–18.

Table 136–13—Transmitter and receiver ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.3	—
Length of the reflection signal	N	300	UI

Transmitter ERL at TP2 shall meet Equation (136–6).

$$ERL \geq 40\log_{10}\left(\frac{v_f}{\max\limits_{k}(p(k))}\right) \quad \text{(dB)} \qquad (136\text{–}6)$$

where

v_f is the steady-state voltage, defined in 136.9.3.1.2

$p(k)$ is the linear fit pulse at preset 1 (no equalization) (see 136.9.3.1.2)

136.9.4 Receiver characteristics

The receiver on each lane shall meet the specifications given in Table 136–14 and detailed in the referenced subclauses. Unless specified otherwise, all receiver measurements are made for each lane separately, at TP3, utilizing the test fixtures specified in Annex 136B.

The receiver specifications at TP5 are provided informatively in 136A.3.

Table 136–14—Summary of receiver specifications at TP3

Parameter	Subclause reference	Value	Units
Input amplitude tolerance	136.9.4.1	1200[a]	mV
Interference tolerance	136.9.4.2	Table 136–15	—
Jitter tolerance	136.9.4.3	Table 120D–7	—
Signaling rate	136.9.4.4	26.5625 ± 100 ppm	GBd
ERL (min.)	136.9.4.5	10	dB
Differential to common-mode input return loss	92.8.4.3	Equation (92–21)	dB

[a]Amplitude is measured at TP2.

136.9.4.1 Receiver input amplitude tolerance

When a PMD receiver is connected to a compliant transmitter whose peak-to-peak differential output voltage (see Table 136–11 footnote a) measured at the preset 1 equalizer setting is 1200 mV, using a compliant cable assembly with the minimum insertion loss specified in 136.11.2, the PMD receiver operation shall enable an FEC symbol error ratio better than 10^{-3} assuming errors are sufficiently

uncorrelated to support the required frame loss ratio (see 136.1). If errors are not sufficiently uncorrelated, the FEC symbol error ratio shall be lower as appropriate to support the required frame loss ratio.

The receiver is allowed to control the transmitter equalizer coefficients, using the PMD control function defined in 136.8.11 or an equivalent process, to meet these requirements.

136.9.4.2 Receiver interference tolerance

Receiver interference tolerance is measured according to the procedure described in 136.9.4.2.1 through 136.9.4.2.5. Receiver interference tolerance test requirements are specified in Table 136–15.

Two tests are defined. Test 1 includes a low-loss channel. Test 2 includes a high-loss channel. The cable assembly used in the test channel (see 110.8.4.2.2) shall meet the cable assembly Channel Operating Margin (COM) as specified in 136.11.7.

Table 136–15—Interference tolerance test parameters

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle encoded by RS-FEC				
FEC symbol error ratio required[a]	$< 10^{-3}$				
Test channel insertion loss at 13.28 GHz[b]	14.3	14.8	24.34	24.84	dB
Cable assembly insertion loss at 13.28 GHz	8	10	15.16	17.16	dB
COM[c]	3		3		dB

[a]See 136.9.4.2.5 for definition of FEC symbol error ratio.
[b]Insertion loss between the two test references (see Figure 110–3b).
[c]The COM value is the target value for the SNR_{TX} calibration defined in 136.9.4.2.3 item f. The SNR_{TX} value measured at the Tx test reference should be as close as practical to the value needed to produce the target COM. If lower SNR_{TX} values are used, this would demonstrate margin to the specification but this is not required for compliance.

136.9.4.2.1 Test setup

The interference tolerance test is performed with the setup similar to the one described in 110.8.4.2.1. The test setup includes noise injection for all lanes of the pattern generator.

136.9.4.2.2 Test channel

The test channel is the same as the one defined in 110.8.4.2.2, except that the cable assembly meets the requirements of 136.11 and the cable assembly test fixture meets the requirements of Annex 136B.

136.9.4.2.3 Test channel calibration

The scattering parameters of the test channel are measured at the test references as illustrated in Figure 110–3b using the cable assembly test fixtures specified in Annex 136B.

The insertion loss at 13.28 GHz of the signal path between the test references in Figure 110–3b is within the limits in Table 136–15.

The COM is calculated using the method and parameters of 136.11.7 with the following considerations:

a) The channel signal path is $SCHS_p$ = cascade($S^{(CTSP)}$, $S^{(HOSP)}$), where cascade() is defined in 93A.1.2.1, $S^{(HOSP)}$ is defined in 136.11.7.1.1, and $S^{(CTSP)}$ is the measured channel between the test references in Figure 110–3b.

b) The COM parameters are as modified by Table 136–15.

c) COM is calculated using both Test 1 and Test 2 device package model transmission line lengths listed in Table 136–18 on the receiver side. The value of COM is taken as the lower of the two calculated values.

d) The augmented signal path in 93A.1.2 is replaced by S_p determined from Equation (136–7) (effectively omitting the transmitter device package model $S^{(tp)}$). The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses T_r equal to the 20% to 80% transition time at the Tx test reference. T_r is measured using the method in 120E.3.1.5 with the transmit equalizer turned off (i.e., coefficients set to the preset 1 values, see 136.9.3.1.3).

e) Even-odd jitter, J3u, and J_{RMS} without noise injection (see 136.9.4.2.4) are measured at the Tx test reference and comply with the specification in Table 136–11. In the calculation of COM, A_{DD} and σ_{RJ} are calculated from the measured values of J3u and J_{RMS} using Equation (136–8) and Equation (136–9), replacing the values in Table 136–18. It is recommended to adjust the pattern generator jitter such that J3u and J_{RMS} are as close as practical to their limits in Table 136–11.

f) The SNR_{TX} value that results in the required COM value for the test is calculated. The injected noise (see 136.9.4.2.4) is set such that the SNDR matches the calculated SNR_{TX} value. SNDR is measured at the Tx test reference using the procedure in 120D.3.1.6, with the exception that the linear fit in 120D.3.1.3 is performed with a pulse length (N_p) of 15 UI.

$$S_p = \text{cascade}(SCHS_p, S^{(rp)}) \tag{136–7}$$

where

cascade()	is defined in 93A.1.2.1
$SCHS_p$	is defined in item a) above
$S^{(rp)}$	is defined in 93A.1.2.4

$$A_{DD} = \frac{\frac{J3u}{2} + Q3\sqrt{(Q3^2+1)\times J_{RMS}^2 - \left(\frac{J3u}{2}\right)^2}}{Q3^2+1} \tag{136–8}$$

$$\sigma_{RJ} = \frac{\frac{J3u}{2} - A_{DD}}{Q3} \tag{136–9}$$

where $Q3 = 3.2905$

NOTE 1—Q3 is an approximated solution of $Q(Q3) = 5\times10^{-4}$, where the Q function is defined in Equation (95–1).

NOTE 2—Calculation of A_{DD} requires that $(Q3^2+1)\times J_{RMS}^2 \geq \left(\frac{J3u}{2}\right)^2$. If this does not hold, a different transmitter should be used in the test setup.

136.9.4.2.4 Pattern generator and noise injection

The pattern generator transmits data to all lanes of the device under test. At the start of transmitter training, the pattern generator output amplitude on all lanes shall be 800 mV peak-to-peak differential when measured on an alternating zero-three pattern. The output amplitude, measured on an alternating zero-three pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The output waveform and the ERL of the pattern generator shall comply with 136.9.3.

Broadband noise is added to the signal before the Tx test reference, with noise level set according to step f in 136.9.4.2.3.

The broadband noise required for each lane is calibrated. The noise may be added either to one lane at a time or using multiple noise sources to all lanes at the same time.

136.9.4.2.5 Test procedure

The pattern generator is first configured to transmit the training pattern defined in 136.8.11. During this initialization period, the device under test (DUT) configures the pattern generator transmit equalizer to the coefficient settings it would select using the protocol described in 136.8.11 and the receiver is tuned using its optimization method. The coefficient settings may be communicated via the start-up protocol or by other means.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to generate the test pattern specified in Table 136–15. During the test, the transmitters in the device under test transmit the same pattern type specified for the test, with equalization turned off (preset 1 condition).

Symbol error ratio is measured using the per-lane RS-FEC symbol error counters (see 91.6) in the adjacent RS-FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate.

The FEC symbol error ratio is defined as the sum of the symbol error counters on all lanes divided by the number of symbols transmitted on all lanes, which may be estimated from the test time.

A PHY shall meet the FEC symbol error ratio requirement in all tests defined in Table 136–15 with broadband noise added to all lanes (see 136.9.4.2.4). The FEC symbol error ratio requirement assumes errors are sufficiently uncorrelated to support the required frame loss ratio (see 136.1). If errors are not sufficiently uncorrelated, the FEC symbol error ratio shall be lower as appropriate to support the required frame loss ratio.

NOTE—If noise is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no noise added on any lane.

136.9.4.3 Receiver jitter tolerance

136.9.4.3.1 Test setup

Jitter tolerance is measured with a channel meeting the insertion loss of Test 2 as specified in Table 136–15. The pattern generator includes sinusoidal jitter injection.

136.9.4.3.2 Test procedure

The jitter tolerance test procedure is similar to that of 136.9.4.2, with the exception that no noise is injected (i.e., step f in 136.9.4.2.3 is not performed). Instead, jitter with the specified frequency and amplitude is applied to the pattern generator and the jitter amplitude is adjusted to obtain the peak-to-peak jitter specified for that frequency in Table 120D–7 at the Tx test reference (see Figure 110–3a). The test channel COM, calculated per 136.9.4.2.3 with the jitter-stressed transmitter output, shall not be lower than the value in Table 136–15.

A PHY shall meet the FEC symbol error ratio requirement defined in Table 136–15 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–7 with jitter added to all lanes (see 136.9.4.2.4).

NOTE 1—If jitter is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no jitter applied on any lane.

NOTE 2—The A_{DD} (Equation (136–8)) and σ_{RJ} (Equation (136–9)) calculated from transmitter measurements in this test may be higher than the values in Table 136–18. A suitable channel should be chosen in order to meet the COM requirement with these values.

136.9.4.4 Signaling rate range

A PHY shall comply with the receiver requirements of 136.9.4.2 and 136.9.4.3 for any signaling rate in the range 26.5625 GBd ± 100 ppm. This translates to a nominal unit interval of 37.64706 ps.

136.9.4.5 Receiver ERL

ERL of the receiver at TP3 is computed using the procedure in 93A.5 with the values in Table 136–13. Parameters that do not appear in Table 136–13 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the TP3 test fixture being used. N_{bx} is set to the value of N_b in Table 136–18.

Receiver ERL at TP3 shall be greater than or equal to 10 dB.

136.10 Channel characteristics

The channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 136–2. The channel insertion loss, return loss, COM, and the transmitter and receiver differential controlled impedance printed circuit board parameters are provided informatively in 136A.4 through 136A.7.

Channel definitions apply for links between two PHYs of the same type, 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4.

136.11 Cable assembly characteristics

Cable assemblies defined in this subclause contain insulated conductors terminated in a connector at each end for use as link segments between MDIs. Cable assemblies are primarily intended as point-to-point links between 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 PHYs using controlled impedance cables.

Three cable assembly types are specified:

a) 50GBASE-CR: Cable assembly that supports single-lane links between two 50GBASE-CR PHYs with achievable cable length of at least 3 m.
b) 100GBASE-CR2: Cable assembly that supports two-lane links between two 100GBASE-CR2 PHYs with achievable cable length of at least 3 m.
c) 200GBASE-CR4: Cable assembly that supports four-lane links between two 200GBASE-CR4 PHYs with achievable cable length of at least 3 m.

NOTE—It may be possible to construct compliant cable assemblies longer than indicated. Length of a cable assembly does not imply compliance to specifications.

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 cable assembly form factors are described in Annex 136D. There are five possible MDIs which are defined in Annex 136C.

For 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, the lanes are AC-coupled. The AC-coupling shall be within the cable assembly. It is recommended that it is within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low-frequency 3 dB

cutoff of the AC-coupling shall be less than 50 kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor limits the inrush charge and baseline wander.

All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in Annex 136B. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of this subclause are met.

Table 136–16 provides a summary of the cable assembly characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, and references to the subclauses addressing each parameter.

The specifications for the three cable assembly types are identical except the number of lanes.

Table 136–16—Cable assembly characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 13.28 GHz	136.11.2	17.16	dB
Minimum insertion loss at 13.28 GHz	136.11.2	8	dB
Minimum cable assembly ERL[a]	136.11.3	11	dB
Differential to common-mode return loss	136.11.4	Equation (92–28)	dB
Differential to common-mode conversion loss	136.11.5	Equation (92–29)	dB
Common-mode to common-mode return loss	136.11.6	Equation (92–30)	dB
Minimum COM	136.11.7	3	dB

[a]Cable assemblies with a COM greater than 4 dB are not required to meet minimum ERL.

136.11.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

136.11.2 Cable assembly insertion loss

The measured insertion loss of a cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in Equation (92–26) and illustrated in Figure 92–12.

The measured insertion loss at 13.28 GHz of a cable assembly shall be less than or equal to 17.16 dB.

136.11.3 Cable assembly ERL

ERL of the cable assembly at TP1 and at TP4 are computed using the procedure in 93A.5 with the values in Table 136–17. Parameters that do not appear in Table 136–17 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the specific cable assembly test fixture being used. Note that test fixtures are specified in 136B.1. N_{bx} is set to the value of N_b in Table 136–18.

Cable assembly ERL at TP1 and at TP4 shall be greater than or equal to 11 dB for cable assemblies that have a COM less than 4 dB.

Table 136–17—Cable assembly ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.25	—
Length of the reflection signal	N	1000	UI

136.11.4 Differential to common-mode return loss

The cable assembly differential to common-mode return loss shall meet the requirements of 92.10.4.

136.11.5 Differential to common-mode conversion loss

The cable assembly differential to common-mode conversion loss shall meet the requirements of 92.10.5.

136.11.6 Common-mode to common-mode return loss

The cable assembly common-mode to common-mode return loss shall meet the requirements of 92.10.6.

136.11.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each lane is derived from measurements of the cable assembly signal, near-end crosstalk and far-end crosstalk paths. COM is computed using the path calculations defined in 136.11.7.1 and the procedure in 93A.1, where T_r is 12 ps for $H_t(f)$ as used in Equation (93A–19). The specific paths used depend on cable assembly form factor (see Annex 136D), as described in 136.11.7.2.

COM parameter values for the three cable assembly types are provided in Table 136–18.

Test 1 and Test 2 differ in the value of the device package model transmission line length z_p. COM for any channel within the cable assembly shall be greater than or equal to 3 dB for both Test 1 and Test 2.

Table 136–18—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step[a]	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_d	1.8×10^{-4}	nF
Transmission line length, Test 1	z_p	12	mm
Transmission line length, Test 2	z_p	30	mm
Single-ended package capacitance at package-to-board interface	C_p	1.1×10^{-4}	nF
Package transmission line characteristic impedance	Z_c	95	Ω
Single-ended reference resistance	R_0	50	Ω

Table 136–18—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.25 0 0.05	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	f_b / 2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 2.5 $2 \times f_b$	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	f_b / 40	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.415 0.415 0.604	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit for $n = 1$ for $n = 2$ to N_b	$b_{max}(n)$	 0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI

Table 136–18—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—

[a]For cable lengths greater than 4 m, a frequency step (Δf) no larger than 5 MHz is recommended.

136.11.7.1 Channel signal and crosstalk path calculations

The channel paths between TP0 and TP5 used for calculation of the cable assembly COM consist of measured cable assembly signal and crosstalk paths, representative transmitter PCB signal paths, and representative receiver PCB signal paths.

The transmitter and receiver PCB signal paths are calculated using the method defined in 93A.1.2.3. The scattering parameters for a PCB are defined by Equation (93A–13), Equation (93A–14), and the parameter values given in Table 92–12, with the exception that Z_c is 100 Ω. The PCB trace length parameter z_p has different value for each specific signal path, as specified in 136.11.7.1.1 and 136.11.7.1.2.

The channel path calculations use the function cascade() defined in 93A.1.2.1.

136.11.7.1.1 Channel signal path

The scattering parameters of the channel signal path from TP0 to TP5 are calculated using Equation (136–10). The transmitter and receiver PCB signal paths are both denoted as $S^{(HOSP)}$ and are calculated from Equation (93A–13) and Equation (93A–14) using z_p = 151 mm in length and the parameter values given in Table 92–12, with the exception that Z_c is 100 Ω, representing an insertion loss of 6.42 dB at 13.28 GHz on each PCB.

$$SCHS_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOSP)}, S^{(CASP)}), S^{(HOSP)}) \quad (136\text{–}10)$$

where

$SCHS_p^{(k)}$ is the channel signal path

$S^{(HOSP)}$ is the host (transmitter or receiver) PCB signal path

$S^{(CASP)}$ is the cable assembly signal path (TP1 to TP4)

k is equal to zero

136.11.7.1.2 Channel crosstalk paths

The MDI is the significant contributor to crosstalk and is included in and characterized by the cable assembly crosstalk measurements. Crosstalk includes a near-end path where the aggressor is the PMD transmitter, and in some cases, additional near-end, far-end, and alien far-end crosstalk paths where the aggressors are other PMD transmitters that are connected to the same cable assembly.

For the channel crosstalk paths, the receiver PCB model is $S^{(HOSP)}$ as defined in 136.11.7.1.1. The aggressor transmitter host PCB model is denoted as $S^{(HOTxSP)}$ and is calculated from Equation (93A–13) and Equation (93A–14) using z_p = 110 mm in length and the parameter values given in Table 92–12, with the exception that Z_c is 100 Ω, representing an insertion loss of 4.68 dB at 13.28 GHz. The transmitter host PCB

insertion loss is lower than that used for the signal path, to allow for a reasonable worst-case crosstalk in the COM calculation.

The scattering parameters of the channel near-end crosstalk paths are calculated using Equation (136–11). The scattering parameters of the channel alien far-end crosstalk paths are calculated using Equation (136–12).

$$SCHNXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CANXTk)}), S^{(HOSP)}) \quad (136\text{–}11)$$

where

$SCHNXT_p^{(k)}$ is the near-end crosstalk path

$S^{(HOSP)}$ is the host receiver PCB signal path defined in 136.11.7.1.1

$S^{(HOTxSP)}$ is the aggressor transmitter PCB signal path

$S^{(CANXTk)}$ is the cable assembly near-end crosstalk path k (TP1 to TP4)

k is the index of the near-end crosstalk path

$$SCHAFXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CAFXTk)}), S^{(HOSP)}) \quad (136\text{–}12)$$

where

$SCHAFXT_p^{(k)}$ is the alien far-end crosstalk path

$S^{(HOSP)}$ is the host receiver PCB signal path defined in 136.11.7.1.1

$S^{(HOTxSP)}$ is the aggressor transmitter PCB signal path

$S^{(CAFXTk)}$ is the cable assembly far-end crosstalk path k (TP1 to TP4)

k is the index of the alien far-end crosstalk path

136.11.7.2 Signal and crosstalk paths used in calculation of COM

Cable assemblies have several form factors, as described in Annex 136D. The choice of signal and crosstalk paths for calculation of COM is specific to each cable assembly form factor, as specified in Table 136–19.

The signal path is calculated using Equation (136–10).

The near-end crosstalk paths are calculated using Equation (136–11), with k values from 1 to n; where n is the number of near-end crosstalk paths given in Table 136–19 for the cable assembly form factor considered.

The far-end crosstalk paths are calculated using Equation (136–12), with k values from 1 to n; where n is the number of far-end crosstalk paths given in Table 136–19 for the cable assembly form factor considered.

Annex 136C specifies the MDIs for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4.

The specifications for the cable assembly types are identical except the number of lanes.

The crosstalk paths for each MDI type are given in Table 136–19; the crosstalk paths are from the aggressors given in columns two through four to the victim given in the first column.

Table 136–19—Number of crosstalk paths used in COM

	SFP28		QSFP28 or microQSFP		QSFP-DD or OSFP	
	NEXT	FEXT	NEXT	FEXT	NEXT	FEXT
SFP28	1	0	1	3	1	7
QSFP28 or microQSFP	4	3	4	3	4	7
QSFP-DD or OSFP	8	7	8	7	8	7

136.12 MDI specifications

The MDI couples the PMD (specified in 136.8 and 136.9) to the cable assembly (specified in 136.11).

50GBASE-CR has five specified MDI connectors: SFP28, QSFP28, microQSFP, QSFP-DD, and OSFP.

100GBASE-CR2 and 200GBASE-CR4 have four specified MDI connectors: QSFP28, microQSFP, QSFP-DD, and OSFP.

Annex 136C specifies the MDIs for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4.

136.13 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

136.14 Protocol implementation conformance statement (PICS) proforma for Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4[10]

136.14.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

136.14.2 Identification

136.14.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

136.14.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[10] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

136.14.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*CR	50GBASE-CR PMD	136.1	Can operate as a 50GBASE-CR PMD	O.1	Yes [ ] No [ ]
*CR2	100GBASE-CR2 PMD	136.1	Can operate as a 100GBASE-CR2 PMD	O.1	Yes [ ] No [ ]
*CR4	200GBASE-CR4 PMD	136.1	Can operate as a 200GBASE-CR4 PMD	O.1	Yes [ ] No [ ]
PMA50	50GBASE-R PMA	136.1	Device implements Clause 135 PMA for 50GBASE-R	CR:M	Yes [ ] N/A [ ]
PMA100	100GBASE-P PMA	136.1	Device implements Clause 135 PMA for 100GBASE-P	CR2:M	Yes [ ] N/A [ ]
PMA200	200GBASE-R PMA	136.1	Device implements Clause 120 PMA for 200GBASE-R	CR4:M	Yes [ ] N/A [ ]
*AUIPMD	50GAUI-n C2C, 100GAUI-n C2C, or 200GAUI-n C2C	136.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
AUIFEC	LAUI-2 C2C or CAUI-n C2C	136.1	Service interface of PMA between PCS and RS-FEC is physically instantiated	!CR4:O.2	Yes [ ] No [ ] N/A [ ]
*nGMII	50GMII, CGMII or 200GMII and RS	136.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
AN	Auto-negotiation	136.1	Device implements auto-negotiation	M	Yes [ ]
FEC50	50GBASE-R RS-FEC	136.1	Device implements Clause 134 RS-FEC	CR* !AUIPMD :M	Yes [ ] N/A [ ]
PCS50	50GBASE-R PCS	136.1	Device implements Clause 133 PCS	CR* nGMII:M	Yes [ ] N/A [ ]
FEC100	100GBASE-R RS-FEC	136.1	Device implements Clause 91 RS-FEC with RS(544,514)	CR2* !AUIPMD :M	Yes [ ] N/A [ ]
PCS100	100GBASE-R PCS	136.1	Device implements Clause 82 100GBASE-R PCS	CR2* nGMII:M	Yes [ ] N/A [ ]
PCS200	200GBASE-R PCS	136.1	Device implements Clause 119 200GBASE-R PCS	CR4* nGMII:M	Yes [ ] N/A [ ]
*EEE	EEE fast wake capability	136.1	Capability is supported	nGMII:O	Yes [ ] No [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	136.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
DC	Delay constraints	136.5	Conforms to constraints	M	Yes [ ]

Item[a]	Feature	Subclause	Value/Comment	Status	Support
SC	Skew and Skew Variation constraints	136.6	Conforms to constraints	M	Yes [ ]
*MD	MDIO capability	136.7	Device implements Clause 45 MDIO	O	Yes [ ] No [ ]
*CBL	Cable assembly	136.11	Item marked with CBL are cable assembly specifications, these items are the only ones applicable to cable assemblies and are not applicable to PHYs.	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

136.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.14.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function in DATA mode	136.8.2	Converts each symbol stream from the PMD service interface into an electrical signal as specified, and delivers it to the MDI	M	Yes [ ]
PF2	Transmit function in TRAINING mode	136.8.2	Converts each symbol stream generated by the PMD control function into an electrical signal as specified, and delivers it to the MDI	M	Yes [ ]
PF4	Receive function	136.8.3	Converts each electrical signal from the MDI into a symbol stream as specified, and delivers it to the PMD service interface	M	Yes [ ]
PF5	Lane-by-lane signal detect	136.8.5	Set to one if training is disabled, otherwise set according to signal_detect	M	Yes [ ]
PF6	Global PMD transmit disable	136.8.6	Function is implemented as specified	O	Yes [ ] No [ ]
PF7	Lane-by-lane PMD transmit disable	136.8.7	Function is implemented as specified	O	Yes [ ] No [ ]
PF8	PMD fault	136.8.8	PMD_fault variable mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
PF9	PMD transmit fault	136.8.9	Implemented, PMD_transmit_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
PF10	PMD receive fault	136.8.10	Implemented, PMD_receive_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]

136.14.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	136.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	136.8.11.2	As shown in Table 136–9	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_tf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4.1	When requested, set according to the request, with values per Table 136–12	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

136.14.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Output voltage specifications	93.8.1.3	Per Table 136–11	M	Yes [ ]
TC2	ERL	136.9.3.4	Meets equation constraints	M	Yes [ ]
TC3	Common-mode to differential mode output return loss	92.8.3.3	Meets equation constraints	M	Yes [ ]
TC4	Common-mode to common-mode output return loss	92.8.3.4	Meets equation constraints	M	Yes [ ]
TC5	Steady-state voltage, v_f	136.9.3.1.2	Per Table 136–11	M	Yes [ ]
TC6	Linear fit pulse peak (min.)	136.9.3.1.2	Per Table 136–11	M	Yes [ ]
TC7	Level separation mismatch ratio	120D.3.1.2	Per Table 136–11	M	Yes [ ]
TC8	Absolute coefficient step size	136.9.3.1.4	Per Table 136–11	M	Yes [ ]
TC9	Absolute change in coefficients other than *c*(coef_sel)	136.9.3.1.4	Less than 0.005	M	Yes [ ]
TC10	Coefficient range	136.9.3.1.5	Per Table 136–11	M	Yes [ ]
TC11	Signal-to-noise-and-distortion ratio	120D.3.1.6	Per Table 136–11	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC12	Output jitter	120D.3.1.8	Per Table 136–11	M	Yes [ ]
TC13	Transmitter signaling rate	136.9.3	26.5625 GBd ± 100 ppm	M	Yes [ ]

136.14.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	ERL	136.9.4.5	Greater than or equal to 10 dB	M	Yes [ ]
RC2	Differential to common-mode return loss at TP3	92.8.4.3	Meets equation constrains	M	Yes [ ]
RC3	Input amplitude tolerance	136.9.4.1	Meets FEC symbol error ratio requirement under described conditions	M	Yes [ ]
RC4	Interference tolerance	136.9.4.2	PHY meets FEC symbol error ratio requirement in all tests defined in Table 136–15 with the specified test setup and procedure	M	Yes [ ]
RC5	Jitter tolerance	136.9.4.3	PHY meets FEC symbol error ratio requirement with the specified test setup and procedure	M	Yes [ ]
RC6	Signaling rate range	136.9.4.4	PHY complies with receiver requirements for signaling rate of 26.5625 GBd ± 100 ppm	M	Yes [ ]

136.14.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	136.11.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Minimum insertion loss	136.11.2	Per Equation (92–26)	CBL:M	Yes [ ] N/A [ ]
CA3	Maximum insertion loss at 13.28 GHz	136.11.2	17.16 dB	CBL:M	Yes [ ] N/A [ ]
CA4	ERL	136.11.3	Greater than or equal to 11 dB for cable assemblies that have a COM less than 4 dB	CBL:M	Yes [ ] N/A [ ]
CA5	Differential to common-mode input and output return loss	92.10.4	Per Equation (92–28)	CBL:M	Yes [ ] N/A [ ]
CA6	Differential to common-mode conversion loss	92.10.5	Per Equation (92–29)	CBL:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CA7	Common-mode to common-mode return loss	92.10.6	Per Equation (92–30)	CBL:M	Yes [ ] N/A [ ]
CA8	Cable assembly Channel Operating Margin (COM)	136.11.7	Greater than or equal to 3 dB for both Test 1 and Test 2, for all channels within the cable assembly	CBL:M	Yes [ ] N/A [ ]
CA9	AC-coupling	136.11	3 dB cutoff frequency less than 50 kHz	CBL:M	Yes [ ] N/A [ ]

136.14.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	136.13	Conform to applicable requirements of 14.7	M	Yes [ ]

137. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4

137.1 Overview

This clause specifies the 50GBASE-KR PMD, the 100GBASE-KR2 PMD, the 200GBASE-KR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 137–1, to the appropriate sublayers (as specified in Table 137–1, Table 137–2, and Table 137–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 137–1—Physical Layer clauses associated with the 50GBASE-KR PMD

Associated clause	50GBASE-KR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

For the 50GBASE-KR and 100GBASE-KR2 PHYs, in order to support the required frame loss ratio (see 1.4.275) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

Table 137–2—Physical Layer clauses associated with the 100GBASE-KR2 PMD

Associated clause	100GBASE-KR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 137–3—Physical Layer clauses associated with the 200GBASE-KR4 PMD

Associated clause	200GBASE-KR4
117—RS	Required
117—200GMII[a]	Optional
118—200GMII extender	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

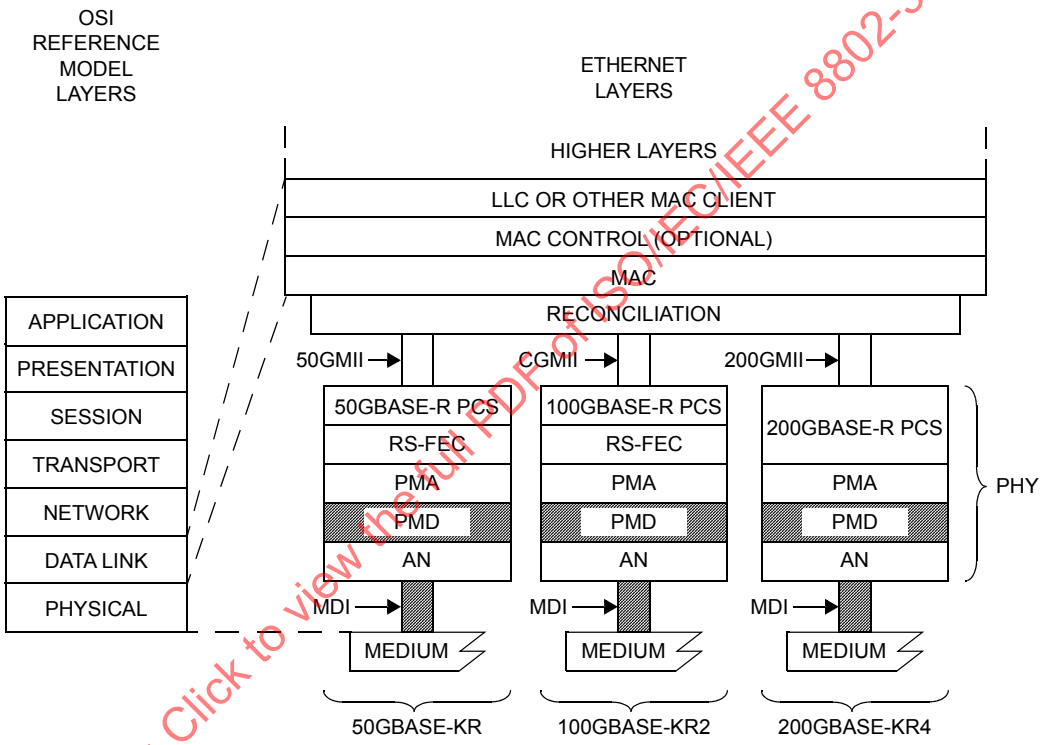
For the 200GBASE-KR4 PHY, in order to support the required frame loss ratio (see 1.4.275) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD

and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant channel.

50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 137–1 shows the relationship of the PMD and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE

MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 137–1—50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

137.2 Conventions

Clause 137 describes three PMDs, 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-KR, n = 2 for 100GBASE-KR2, and n = 4 for 200GBASE-KR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term "PMD" refers to any of 50GBASE-KR PMD, 100GBASE-KR2 PMD, or 200GBASE-KR4 PMD.

137.3 PMD service interfaces

The service interfaces of the 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 PMDs are identical to those of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs, respectively (see 136.3).

137.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with the PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. The requirements are the same as those specified in 136.4.

137.5 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 137–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 137–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-KR	2048	4	40.96
100GBASE-KR2	4096	8	40.96
200GBASE-KR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-KR, 10 ps for 100GBASE-KR2, and 5 ps for 200GBASE-KR4. (See 1.4.160 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-KR, 5.12 ns for 100GBASE-KR2, and 2.56 ns for 200GBASE-KR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-KR, in 80.4 for 100GBASE-KR2, and in 116.4 for 200GBASE-KR4.

137.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

137.6.1 Skew Constraints for 50GBASE-KR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

137.6.2 Skew Constraints for 100GBASE-KR2 and 200GBASE-KR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

137.7 PMD MDIO function mapping

The PMD MDIO function mapping requirements for the PMDs defined in this clause are identical to those of 136.7.

137.8 PMD functional specifications

137.8.1 Link block diagram

One direction of a 50GBASE-KR, 100GBASE-KR2, or 200GBASE-KR4 link is shown in Figure 137–2.

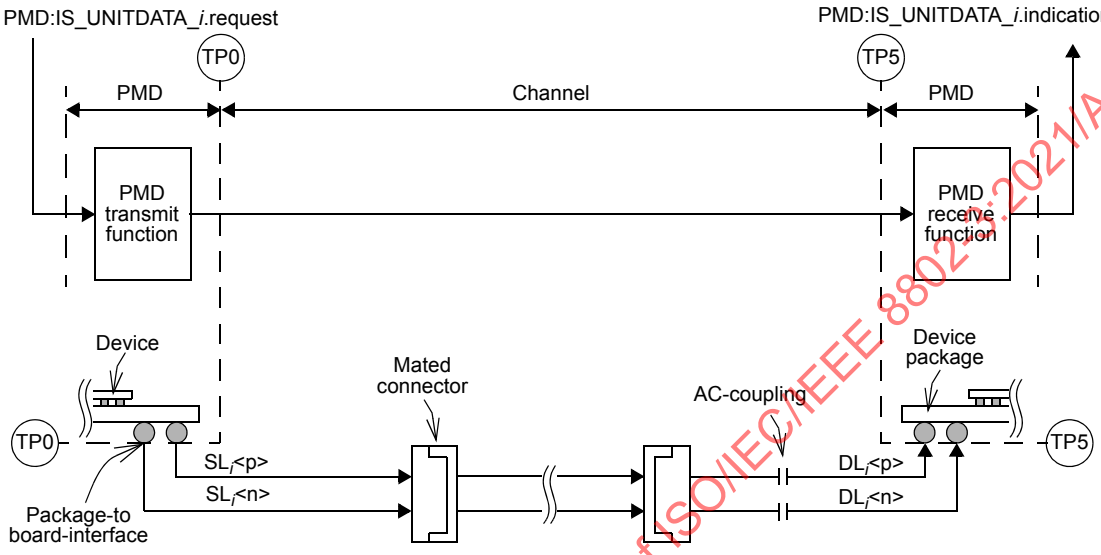


Figure 137–2—50GBASE-KR, 100GBASE-KR2 or 200GBASE-KR4 link (one direction for one lane is illustrated)

137.8.2 PMD transmit function

The PMD transmit function specification is identical to that of 136.8.2 with the exception that electrical signals are delivered to the MDI, according to the transmit electrical specifications in 137.9.2.

137.8.3 PMD receive function

The PMD receive function specification is identical to that of 136.8.3 with the exception that electrical signals are received from the MDI, according to the receive electrical specifications in 137.9.3.

137.8.4 PMD global signal detect function

The PMD global signal detect function specification is identical to that of 136.8.4.

137.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function specification is identical to that of 136.8.5.

137.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. Its specification is identical to that of 136.8.6.

137.8.7 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional. Its specification is identical to that of 136.8.7.

137.8.8 PMD fault function

The PMD fault function specification is identical to that of 136.8.8.

137.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. Its specification is identical to that of 136.8.9.

137.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. Its specification is identical to that of 136.8.10.

137.8.11 PMD control function

The PMD control function specification is identical to that of 136.8.11.

137.9 Electrical characteristics

137.9.1 MDI

The MDI for the 50GBASE-KR, 100GBASE-KR2 and 200GBASE-KR4 PHYs is an implementation-dependent direct electrical connection between the PMD and the medium. The MDI comprises 2 × n differential pairs, one pair for the transmit function and one pair for the receive function on each lane, marked by TP0 and TP5 in Figure 137–2.

Transmitter and receiver characteristics are defined at TP0a and TP5a.

The location of TP0a and the electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93–5 and 93.8.1.1, respectively, with the exception that the upper frequency for Equation 93–1 and Equation 93–2 is 26.5625 GHz.

The location of TP5a and the electrical characteristics of the test fixture used to measure receiver characteristics are defined in Figure 93–10 and 93.8.2.1, respectively, with the exception that the upper frequency for Equation 93–1 and Equation 93–2 is 26.5625 GHz.

137.9.2 Transmitter characteristics

The transmitter shall meet the specifications given in Table 120D–1, with the following exceptions:

a) The value of linear fit pulse peak (min) is $0.75 \times v_f$.
b) The output waveform Pre-cursor equalization and Post-cursor equalization parameters are replaced by the "Transmitter output waveform" specifications summarized in Table 136–11 and detailed in 136.9.3.1.
c) The differential output return loss (min) and SNR_{ISI} (min) requirements are replaced by the transmitter effective return loss (ERL) specification in 137.9.2.1.
d) The value of SNDR (min) is 32.5 dB.
e) The J4u limit in Table 120D–1 does not apply. The maximum J3u (see 136.9.3.3) is 0.106 UI.

137.9.2.1 Transmitter ERL

ERL of the transmitter at TP0a is computed using the procedure in 93A.5 with the values in Table 137–5. Parameters that do not appear in Table 137–5 take values from Table 137–6. The value of T_{fx} is twice the delay from TP0 to TP0a. N_{bx} is set to the value of N_b in Table 137–6.

Table 137–5—Transmitter and receiver ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.32	—
Length of the reflection signal	N	100	UI

Transmitter ERL at TP0a shall be greater than or equal to 15 dB.

137.9.3 Receiver characteristics

Receiver electrical characteristics are specified at TP5a. The receiver shall meet the specifications given in Table 120D–5 with the following exceptions:

a) PCS FEC symbol error ratio (max) values in Table 120D–6 and Table 120D–7 are all 10^{-3}. For 50GBASE-KR and 100GBASE-KR2, RS-FEC symbol error ratio is used instead of PCS FEC symbol error ratio.

b) Insertion loss at 13.2813 GHz values for Test 1 are 14.5 (min) and 15.5 (max).

c) Insertion loss at 13.2813 GHz values for Test 2 are 29.5 (min) and 30.5 (max).

d) RSS_DFE4 value for Test 1 is 0.05.

e) Receiver jitter tolerance (see 120D.3.2.2) is tested using the test channel used for receiver interference tolerance Test 2 (see item c).

f) The differential input return loss (min) requirements are replaced by the receiver ERL specification in 137.9.3.1.

137.9.3.1 Receiver ERL

ERL of the receiver at TP5a is computed using the procedure in 93A.5 with the values in Table 137–5. Parameters that do not appear in Table 137–5 take values from Table 137–6. The value of T_{fx} is twice the delay from TP5a to TP5. N_{bx} is set to the value of N_b in Table 137–6.

Receiver ERL at TP5a shall be greater than or equal to 15 dB.

137.10 Channel characteristics

The Channel Operating Margin (COM) is computed using the procedure in 93A.1 with the values in Table 137–6, where T_r is 12 ps for $H_t(f)$ as used in Equation (93A–19). COM shall be greater than or equal to 3 dB.

Channels shall have AC-coupling as specified in 93.9.4.

Channels are recommended to meet the insertion loss limits in 137.10.1. Channels shall meet the ERL requirement in 137.10.2. The reference differential impedance for channel specifications is 100 Ω.

Table 137–6—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Package transmission line nominal characteristic impedance	 C_d z_p z_p C_p Z_c	 1.8×10^{-4} 12 30 1.1×10^{-4} 95	 nF mm mm nF Ω
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.25 0 0.05	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 2.5$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 2.5$ $2 \times f_b$	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	$f_b / 40$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.415 0.415 0.604	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB

Table 137–6—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit $n = 1$ $n = 2$ to N_b	$b_{max}(n)$	 0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—

137.10.1 Channel insertion loss

The maximum recommended insertion loss of the channel is given by Equation (137–1).

$$IL(f) \leq \begin{cases} 1.25 + 3.9\sqrt{f} + 1.095f & 0.01 \leq f \leq f_b/2 \\ -12.5 + 3.2f & f_b/2 < f \leq f_b \end{cases} \text{ (dB)} \qquad (137\text{–}1)$$

where

f is the frequency in GHz
f_b is the signaling rate (26.5625) in GHz
$IL(f)$ is the insertion loss at frequency f

The insertion loss limit is illustrated by Figure 137–3.

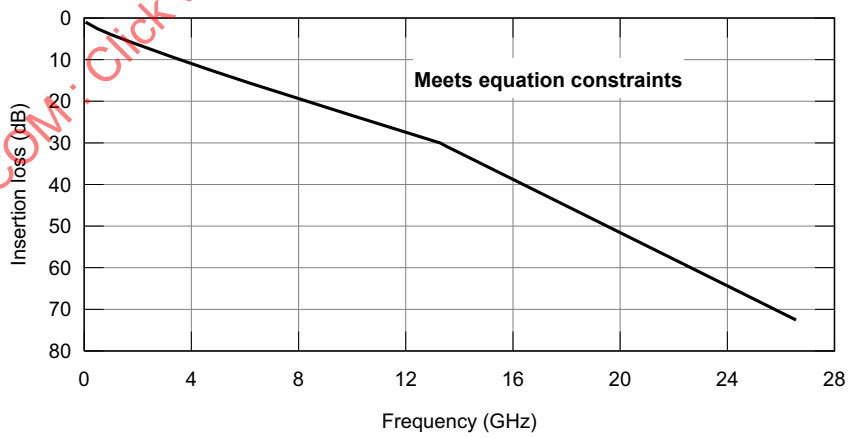


Figure 137–3—Channel insertion loss limit

137.10.2 Channel ERL

ERL of the channel at TP0 and at TP5 are computed using the procedure in 93A.5 with the values in Table 137–7. Parameters that do not appear in Table 137–7 take values from Table 137–6. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 137–6.

Table 137–7—Channel ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.18	—
Length of the reflection signal	N	1000	UI

Channel ERL at TP0 and at TP5 shall be greater than or equal to 10 dB.

137.11 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 93.10.

137.12 Protocol implementation conformance statement (PICS) proforma for Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4[11]

137.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

137.12.2 Identification

137.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

137.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[11] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

137.12.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*KR	50GBASE-KR PMD	137.1	Can operate as a 50GBASE-KR PMD	O.1	Yes [ ] No [ ]
*KR2	100GBASE-KR2 PMD	137.1	Can operate as a 100GBASE-KR2 PMD	O.1	Yes [ ] No [ ]
*KR4	200GBASE-KR4 PMD	137.1	Can operate as a 200GBASE-KR4 PMD	O.1	Yes [ ] No [ ]
PMA50	50GBASE-R PMA	137.1	Device implements Clause 135 PMA for 50GBASE-R	KR:M	Yes [ ] N/A [ ]
PMA100	100GBASE-P PMA	137.1	Device implements Clause 135 PMA for 100GBASE-P	KR2:M	Yes [ ] N/A [ ]
PMA200	200GBASE-R PMA	137.1	Device implements Clause 120 PMA for 200GBASE-R	KR4:M	Yes [ ] N/A [ ]
*AUIPMD	50GAUI-n C2C, 100GAUI-n C2C, or 200GAUI-n C2C	137.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
AUIFEC	LAUI-2 C2C or CAUI-n C2C	137.1	Service interface of PMA between PCS and RS-FEC is physically instantiated	!KR4:O.2	Yes [ ] No [ ] N/A [ ]
*nGMII	50GMII, CGMII or 200GMII and RS	137.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
AN	Auto-negotiation	137.1	Device implements auto-negotiation	M	Yes [ ]
FEC50	50GBASE-R RS-FEC	137.1	Device implements Clause 134 RS-FEC	KR* !AUIPMD :M	Yes [ ] N/A [ ]
PCS50	50GBASE-R PCS	137.1	Device implements Clause 133 PCS	KR* nGMII:M	Yes [ ] N/A [ ]
FEC100	100GBASE-R RS-FEC	137.1	Device implements Clause 91 RS-FEC with RS(544,514)	KR2* !AUIPMD :M	Yes [ ] N/A [ ]
PCS100	100GBASE-R PCS	137.1	Device implements Clause 82 100GBASE-R PCS	KR2* nGMII:M	Yes [ ] N/A [ ]
PCS200	200GBASE-R PCS	137.1	Device implements Clause 119 200GBASE-R PCS	KR4* nGMII:M	Yes [ ] N/A [ ]
*EEE	EEE fast wake capability	137.1	Capability is supported	nGMII:O	Yes [ ] No [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	137.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
DC	Delay constraints	137.5	Conforms to constraints	M	Yes [ ]
SC	Skew and Skew Variation constraints	137.6	Conforms to constraints	M	Yes [ ]

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	137.7	Device implements Clause 45 MDIO	O	Yes [ ] No [ ]
*CHNL	Channel	137.10	Item marked with CHNL are channel specifications, these items are the only ones applicable to channels and are not applicable to PHYs.	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

137.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4

137.12.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function in DATA mode	136.8.2	Converts each symbol stream from the PMD service interface into an electrical signal as specified, and delivers it to the MDI, with the electrical specifications in 137.9.2	M	Yes [ ]
PF2	Transmit function in TRAINING mode	136.8.2	Converts each symbol stream generated by the PMD control function into an electrical signal as specified, and delivers it to the MDI, with the electrical specifications in 137.9.2	M	Yes [ ]
PF4	Receive function	136.8.3	Converts each electrical signal from the MDI into a symbol stream as specified, and delivers it to the PMD service interface	M	Yes [ ]
PF5	Lane-by-lane signal detect	136.8.5	Set to one if training is disabled, otherwise set according to signal_detect	M	Yes [ ]
PF6	Global PMD transmit disable	136.8.6	Function is implemented as specified	O	Yes [ ] No [ ]
PF7	Lane-by-lane PMD transmit disable	136.8.7	Function is implemented as specified	O	Yes [ ] No [ ]
PF8	PMD fault	136.8.8	PMD_fault variable mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
PF9	PMD transmit fault	136.8.9	Implemented, PMD_transmit_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
PF10	PMD receive fault	136.8.10	Implemented, PMD_receive_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]

137.12.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	136.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	136.8.11.2	As shown in Table 136–9	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_tf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4.1	When requested, set according to the request, with values per Table 136–12	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

137.12.4.3 Transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	TP0-TP0a test fixture	137.9.1	Meets specifications	M	Yes [ ]
TC2	Output voltage specifications	93.8.1.3	Per Table 120D–1	M	Yes [ ]
TC3	ERL at TP0a	137.9.2.1	Greater than or equal to 15 dB	M	Yes [ ]
TC4	Common-mode to common-mode output return loss	93.8.1.4	Per Table 120D–1	M	Yes [ ]
TC5	Steady-state voltage, v_f	120D.3.1.4	Per Table 120D–1	M	Yes [ ]
TC6	Linear fit pulse peak (min)	137.9.2	$0.75 \times v_f$	M	Yes [ ]
TC7	Level separation mismatch ratio	120D.3.1.2	Per Table 120D–1	M	Yes [ ]
TC8	Absolute coefficient step size	136.9.3.1.4	Per Table 136–11	M	Yes [ ]
TC9	Coefficient range	136.9.3.1.5	Per Table 136–11	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC10	Signal-to-noise-and-distortion ratio	137.9.2	Greater than specified minimum	M	Yes [ ]
TC11	Output jitter	120D.3.1.8	Per Table 136–11	M	Yes [ ]
TC12	Transmitter signaling rate	120D.3.1	26.5625 GBd ± 100 ppm	M	Yes [ ]

137.12.4.4 Receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	TP5-TP5a test fixture	137.9.1	Meets specifications	M	Yes [ ]
RC2	ERL at TP5a	137.9.3.1	Greater than or equal to 15 dB	M	Yes [ ]
RC3	Input differential to common-mode return loss	137.9.3	Meets constraints of Equation (93–5)	M	Yes [ ]
RC4	Interference tolerance	137.9.3	PHY meets FEC symbol error ratio requirement in all tests defined in Table 120D–6 with the specified test setup and procedure, and the exceptions listed in 137.9.3	M	Yes [ ]
RC5	Jitter tolerance	137.9.3	PHY meets FEC symbol error ratio requirement in all cases defined in Table 120D–7 with the specified test setup and procedure, and the exceptions listed in 137.9.3	M	Yes [ ]

137.12.4.5 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	ERL	137.10.2	Greater than or equal to 10 dB	CHNL:M	Yes [ ] N/A [ ]
CC2	Channel Operating Margin (COM)	137.10	Greater than or equal to 3 dB	CHNL:M	Yes [ ] N/A [ ]
CC3	AC-coupling	93.9.4	Between TP0 and TP5, 3 dB cutoff frequency less than 50 kHz	CHNL:M	Yes [ ] N/A [ ]

137.12.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Environmental specifications	137.11	Conform to applicable requirements of 93.10	M	Yes [ ]

138. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4

138.1 Overview

This clause specifies the 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PMDs together with the multimode fiber medium. The optical signals generated by these three PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. The PMD sublayers provide point-to-point 50, 100, and 200 Gigabit Ethernet links over one, two, or four pairs of multimode fiber, with a reach of up to at least 100 m.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA, as shown in Table 138–1, Table 138–2, or Table 138–3, to the medium through the MDI and optionally, with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 138–1—Physical Layer clauses associated with the 50GBASE-SR PMD

Associated clause	50GBASE-SR
132—RS	Required
132—50GMII[a]	Optional
133—PCS	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

Table 138–2—Physical Layer clauses associated with the 100GBASE-SR2 PMD

Associated clause	100GBASE-SR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC[b]	Required
83—PMA for 100GBASE-R	Optional
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4 C2M	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.
[b]The option to bypass the Clause 91 RS-FEC correction function is not supported.

Table 138–3—Physical Layer clauses associated with the 200GBASE-SR4 PMD

Associated clause	200GBASE-SR4
117—RS	Required
117—200GMII[a]	Optional
118—200GMII Extender	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120C—200GAUI-8 C2M	Optional
120D—200GAUI-4 C2C	Optional
120E—200GAUI-4 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

Figure 138–1 shows the relationship of the PMDs and MDIs (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 131.2. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2. 200 Gigabit Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.). The 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 sublayers provide point-to-point 50, 100, and 200 Gigabit Ethernet links over one, two, or four, pairs of multimode fiber, up to at least 100 m.

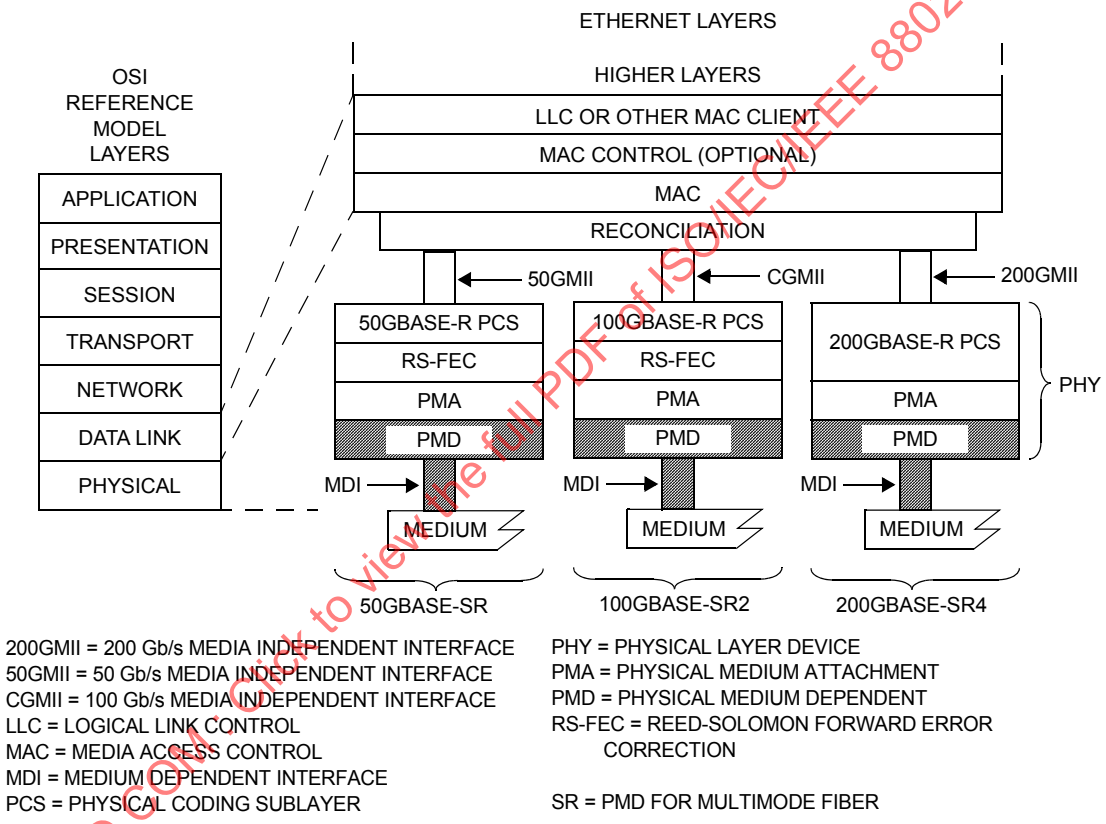


Figure 138–1—50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

138.1.1 Bit error ratio

For the 50GBASE-SR and 100GBASE-SR2 PMDs, the bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.275) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134 or Clause 91) and PCS (Clause 133 or Clause 82). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet

frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

For the 200GBASE-SR4 PMD, the bit error ratio (BER) when processed by the PMA (Clause 120) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.275) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when additionally processed by the PCS (Clause 119). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

138.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-SR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-SR2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with two parallel symbol streams (n = 2).

The 200GBASE-SR4 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with four parallel symbol streams (n = 4).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-SR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends n streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 138.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 138.1.1.

138.3 Delay and Skew

138.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation.

The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-SR PMD including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-SR2 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 200GBASE-SR4 PMD including 2 m of fiber in one direction shall be no more than 4096 bit times (8 pause_quanta or 20.48 ns).

Descriptions of overall system delay constraints and the definitions for bit times and pause_quanta, can be found in 131.4 for 50GBASE-SR, in 80.4 for 100GBASE-SR2, and in 116.4 and its references for 200GBASE-SR4.

138.3.2 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes must be kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation must also be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

138.3.2.1 Skew Constraints for 50GBASE-SR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

138.3.2.2 Skew Constraints for 100GBASE-SR2 and 200GBASE-SR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

138.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 138–4, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 138–5.

Table 138–4—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0

Table 138–5—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0

138.5 PMD functional specifications

The 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

138.5.1 PMD block diagram

The PMD block diagram for 200GBASE-SR4 is shown in Figure 138–2. The block diagrams for 100GBASE-SR2 and 50GBASE-SR are equivalent to Figure 138–2, but for two lanes and one lane per direction, respectively.

For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 138.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 138.10.3). Unless specified otherwise, all receiver measurements and tests defined in 138.8 are made at TP3.

TP1<0:3> and TP4<0:3> are informative reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

138.5.2 PMD transmit function

The PMD Transmit function shall convert the one, two, or four signal streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request into one, two, or four separate optical signal streams. The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$. The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1. The 200GBASE-SR4 has four parallel symbol streams, hence $i = 0$ to 3. Each optical signal stream shall then be delivered to the MDI, which contains one, two, or four parallel light paths for transmit, according to the transmit optical specifications in this clause. The four optical power levels in the signal stream in order from lowest to highest shall correspond to tx_symbols zero, one, two, and three, respectively.

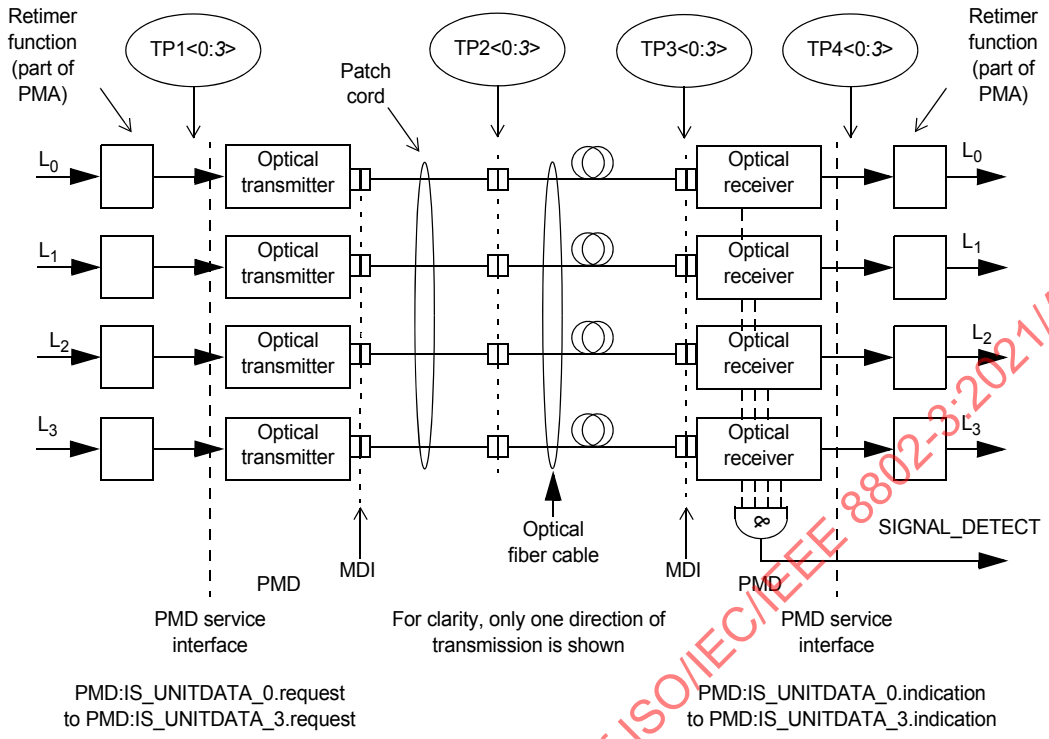


Figure 138–2—Block diagram for 200GBASE-SR4 transmit/receive paths

138.5.3 PMD receive function

The PMD Receive function shall convert the one, two, or four parallel optical signal streams received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbols zero, one, two, and three, respectively.

138.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 138–6. The PMD receiver is not required to verify whether a compliant 50GBASE-SR, 100GBSE-SR2, or 200GBASE-SR4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Table 138–6—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 138–8) AND (compliant 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

138.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 138–6.

138.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

138.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 138–8.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

138.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 138–8.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

138.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

138.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4

138.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

138.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 100GBASE-SR2 or 200GBASE-SR4. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the RS-FEC sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 138.10.3.1.

138.7 PMD to MDI optical specifications for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4

The operating range for the 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 PMDs is defined in Table 138–7. A compliant PMD operates on 50/125 µm multimode fibers, type A1a.2 (OM3), type A1a.3 (OM4), or type A1a.4 (OM5), according to the specifications defined in Table 138–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-SR PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m).

Table 138–7—Operating range

PMD type	Required operating range[a]
50GBASE-SR 100GBASE-SR2 200GBASE-SR4	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4
	0.5 m to 100 m for OM5

[a]The PCS FEC correction function may not be bypassed for any operating distance.

138.7.1 Transmitter optical specifications

Each lane of a 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 transmitter shall meet the specifications in Table 138–8 per the definitions in 138.8.

Table 138–8—Transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	
Center wavelength (range)	840 to 860	nm
RMS spectral width[a] (max)	0.6	nm
Average launch power, each lane (max)	4	dBm
Average launch power, each lane (min)	–6.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	3	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	–4.5	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–5.9	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	4.5	dB
TDECQ – $10\log_{10}(C_{eq})$[c], each lane (max)	4.5	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio, each lane (min)	3	dB
Transmitter transition time, each lane (max)	34	ps
$RIN_{12}OMA$ (max)	–128	dB/Hz
Optical return loss tolerance (max)	12	dB
Encircled flux[d]	≥ 86% at 19 µm ≤ 30% at 4.5 µm	

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDECQ < 1.4 dB, the OMA (min) must exceed this value.
[c]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d]If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.

138.7.2 Receiver optical specifications

Each lane of a 50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 receiver shall meet the specifications in Table 138–9 per the definitions in 138.8.

Table 138–9—Receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	
Center wavelength (range)	840 to 860	nm

Table 138–9—Receive characteristics *(continued)*

Description	Value	Unit
Damage threshold[a] (min)	5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[b] (min)	–8.4	dBm
Receive power, each lane (OMA_{outer}) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA_{outer}), each lane[c] (max)	–3.4	dBm
Receiver sensitivity (OMA_{outer}), each lane[d] (max)	Equation (138–1)	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ), lane under test	4.5	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	4.5	dB
OMA_{outer} of each aggressor lane[g]	3	dBm

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 138.8.10) for the BER specified in 138.1.1.
[d]Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[g]Only applies to 100GBASE-SR2 and 200GBASE-SR4.

138.7.3 Illustrative link power budget

An illustrative power budget and penalties for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 channels are shown in Table 138–10.

Table 138–10—Illustrative link power budget

Parameter	OM3	OM4	OM5	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700		MHz.km
Power budget (for max TDECQ)	6.5			dB
Operating distance	0.5 to 70	0.5 to 100		m
Channel insertion loss[b]	1.8	1.9		dB
Allocation for penalties[c] (for max TDECQ)	4.6			dB
Additional insertion loss allowed	0.1	0		dB

[a]Per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 138–7 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 138.10.2.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

138.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

138.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 138–12 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 138–12 may be used to perform that test. The test patterns used in this clause are shown in Table 138–11.

Table 138–11—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 138–12—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 4, 5, 6, or valid 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal	138.8.2
Average optical power	3, 4, 5, 6, or valid 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal	138.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	138.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	138.8.5
Extinction ratio	4 or 6	138.8.6
Transmitter transition time	Square wave or 6	138.8.7
$RIN_{12}OMA$	Square wave	138.8.8
Stressed receiver sensitivity	3, 5, or valid 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 signal	138.8.10
Stressed eye closure (SEC), calibration	6	138.8.10

138.8.1.1 Multi-lane testing considerations

Stressed receiver sensitivity is defined for each lane at the BER specified in 138.1.1. Measurements with Pattern 3 (PRBS31Q) allow lane-by-lane BER measurements. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA_{outer}) for a particular situation is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31Q patterns on one lane and any other lane so that the symbols on each lane are not correlated within the PMD.

138.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 138–8 if measured per IEC 61280-1-3. The lane under test is modulated using one of the test patterns specified in Table 138–12.

138.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 138–8 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using one of the test patterns defined in Table 138–12, per the set up shown in Figure 53–6.

138.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 138–8 if measured as defined in 121.8.4.

138.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

TDECQ is a measure of each optical transmitter's vertical eye closure as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a combined reference receiver and worst case optical channel, and equalized with the reference equalizer specified in 138.8.5.1. Table 138–9 specifies the test pattern to be used for measurement of TDECQ.

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 138–8 if measured using the methods specified in 121.8.5, with the following exceptions:

- The polarization rotator and test fiber shown in Figure 121–4 are not used.
- The optical channel requirements in 121.8.5.2 do not apply.
- The combination of the O/E converter and the oscilloscope used to measure the optical waveform has a 3 dB bandwidth of approximately 11.2 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 22.4 GHz and at frequencies above 1.5 × 22.4 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.
- The reference equalizer to be used for TDECQ for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 is specified in 138.8.5.1.
- P_{th1}, P_{th2}, and P_{th3} are varied from their nominal values by up to ±1% of OMA_{outer} in order to optimize TDECQ. The same three thresholds are used for both the left and the right histogram.

138.8.5.1 TDECQ reference equalizer

The reference equalizer for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4 is a 5 tap, T spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 138–3. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

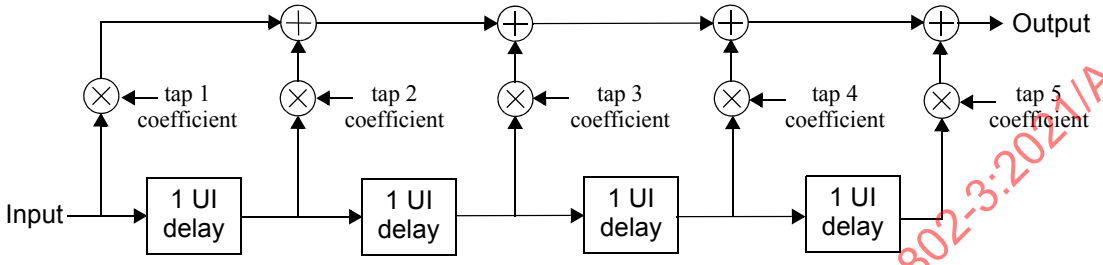


Figure 138–3—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver implementation.

138.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 138–8 if measured using the methods specified in 121.8.6.

138.8.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 138–8 if measured using a test pattern specified for transmitter transition time in Table 138–12.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 138.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

138.8.8 Relative intensity noise ($RIN_{12}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 12 dB.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).
c) The test pattern is according to Table 138–12.

138.8.9 Receiver sensitivity

Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB. Receiver sensitivity should meet Equation (138–1), which is illustrated in Figure 138–4.

$$RS = \max(-6.5, SECQ - 7.9) \quad \text{(dBm)} \qquad (138\text{–}1)$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

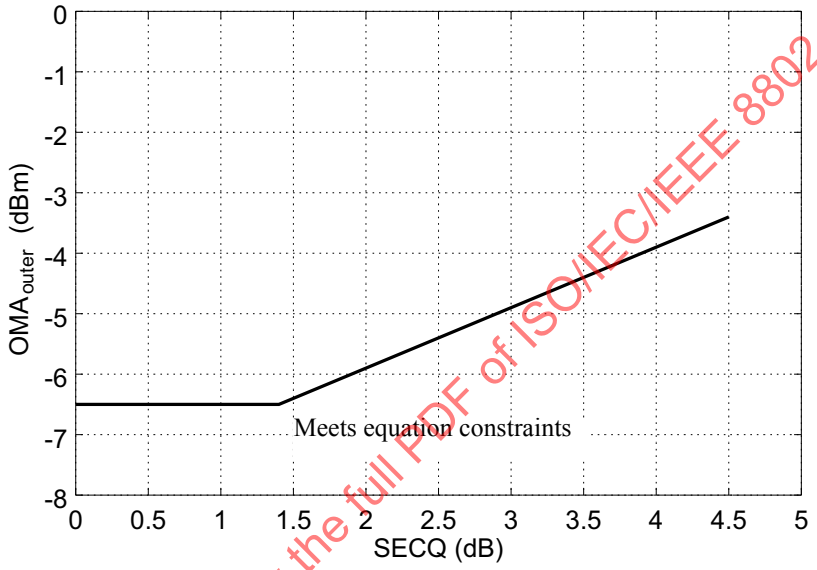


Figure 138–4—Illustration of receiver sensitivity

138.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 138–9 if measured using the methodology defined in 121.8.9.1 and 121.8.9.3, with the conformance test signal at TP3 as described in 121.8.9.2, with the following exceptions:

— The SECQ of the stressed receiver conformance test signal is measured according to 138.8.5, except that the combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response. The optical splitter and variable reflector shown in Figure 121–4 are not used, and the transition time is no greater than the value specified in Table 138–8.

— With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{12}OMA$ of the SRS test source should be no greater than the $RIN_{12}OMA$ (max) specified for the transmit characteristics in Table 138–8.

— The test patterns used for stressed receiver sensitivity are specified in Table 138–12.

— The signaling rate, the required stressed eye closure (SECQ), and the maximum $SECQ - 10\log_{10}(C_{eq})$ of the stressed receiver conformance test signal is as specified in Table 138–9.

— The restriction that at least half of the dB value of the SECQ is due to the frequency response of the combination of the low-pass filter and the E/O converter in 121.8.9.1 and 121.8.9.2 does not apply.
— The applied sinusoidal jitter is specified in 138.8.10.1.
— For 100GBASE-SR2 and 200GBASE-SR4, the OMA_{outer} of the aggressor lanes is specified in Table 138–9.

The BER is required to be met for each lane under test on its own. Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Any of the patterns specified for stressed receiver sensitivity in Table 138–12 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

138.8.10.1 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 138–13.

Table 138–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	$2 \times 10^5 / f$
4 MHz $< f \leq 10$ LB[a]	0.05

[a] *LB* = loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.

138.9 Safety, installation, environment, and labeling

138.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

138.9.2 Laser safety

50GBASE-SR, 100GBASE-SR2 and 200GBASE-SR4 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[12]

[12] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

138.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

138.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

138.9.5 Electromagnetic emission

A system integrating a 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

138.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

138.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4).

Labeling requirements for Hazard Level 1M lasers are given in the laser safety standards referenced in 138.9.2.

138.10 Fiber optic cabling model

The fiber optic cabling (channel) contains 1, 2, or 4 optical fibers for each direction to support 50GBASE-SR, 100GBASE-SR2, or 200GBASE-SR4, respectively. The fiber optic cabling interconnects the transmitters at the MDI on one end of the channel to the receivers at the MDI on the other end of the channel. As defined in 138.10.3, the optical lanes appear in defined locations at the MDI but the locations are not assigned specific lane numbers within this standard because any transmitter lane may be connected to any receiver lane.

138.10.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 138–5.

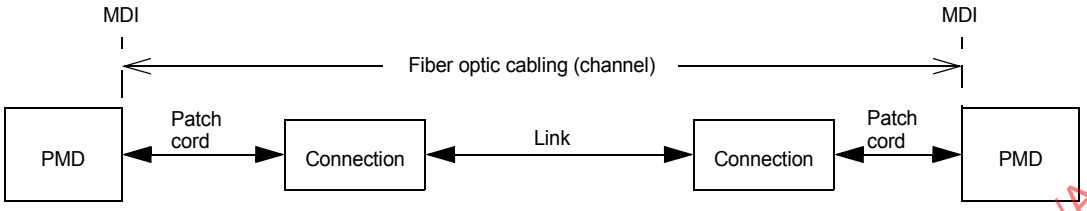


Figure 138–5—Fiber optic cabling model

The channel insertion loss is given in Table 138–14. A channel may contain additional connectors as long as the optical characteristics of the channel (such as attenuation, modal dispersion, reflections and losses of all connectors and splices) meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1:2009. As OM4 and OM5 optical fiber meet the requirements for OM3, a channel compliant to the "OM3" column may use OM4 or OM5 optical fiber, or a combination of OM3, OM4, and OM5. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 138–14—Fiber optic cabling (channel) characteristics

Description	OM3	OM4	OM5	Unit
Operating distance (max)	70	100		m
Cabling Skew (max)[a]	79			ns
Cabling Skew Variation[ab] (max)	2.4			ns
Channel insertion loss[c] (max)	1.8	1.9		dB
Channel insertion loss (min)	0			dB

[a]Only applies to 100GBASE-SR2 and 200GBASE-SR4.
[b]An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.
[c]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

138.10.2 Characteristics of the fiber optic cabling (channel)

The fiber optic cabling shall meet the specifications defined in Table 138–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

138.10.2.1 Optical fiber cable

The fiber contained within the fiber optic cabling shall comply with the specifications and parameters of Table 138–15. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 138–14.

Table 138–15—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	OM5[c]	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850			nm
Effective modal bandwidth (min)[d]	2000	4700		MHz.km
Cabled optical fiber attenuation (max)	3.5			dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		$1297 \le \lambda_0 \le 1328$	nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		$-412/(840(1-(\lambda_0/840)^4))$	ps/nm^2 km

[a]IEC 60793-2-10 type A1a.2
[b]IEC 60793-2-10 type A1a.3
[c]IEC 60793-2-10 type A1a.4
[d]When measured with the launch conditions specified in Table 138–8

138.10.2.2 Optical fiber connection

An optical fiber connection, as shown in Figure 138–5, consists of a mated pair of optical connectors.

138.10.2.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 138–14 are met. However, the loss of a single connection shall not exceed 0.75 dB.

138.10.2.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

138.10.3 Medium Dependent Interface (MDI)

The 50GBASE-SR, 100GBASE-SR2 or 200GBASE-SR4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 138–5). Examples of an MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;

b) PMD receptacle.

NOTE—Compliance testing is performed at TP2 and TP3 as defined in 138.5.1, not at the MDI.

138.10.3.1 Optical lane assignments for 100GBASE-SR2 and 200GBASE-SR4

The two transmit and two receive optical lanes of 100GBASE-SR2 shall occupy the positions depicted in Figure 138–6 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains four active lanes within 12 total positions. The eight center positions are unused. The transmit optical lanes occupy the leftmost two positions. The receive optical lanes occupy the rightmost two positions.

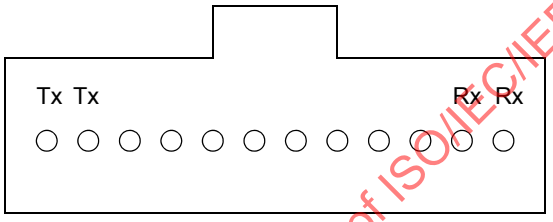


Figure 138–6—Optical lane assignments for 100GBASE-SR2

The four transmit and four receive optical lanes of 200GBASE-SR4 shall occupy the positions depicted in Figure 138–7 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within 12 total positions. The four center positions are unused. The transmit optical lanes occupy the leftmost four positions. The receive optical lanes occupy the rightmost four positions.

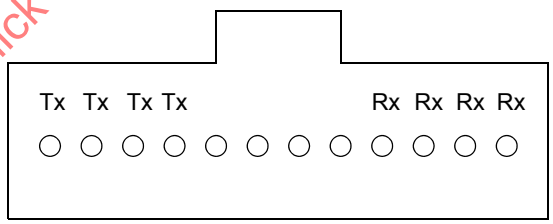


Figure 138–7—Optical lane assignments for 200GBASE-SR4

138.10.3.2 MDI requirements for 50GBASE-SR

The MDI shall optically mate with the compatible plug on the optical fiber cabling. For 50GBASE-SR, when the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

138.10.3.3 MDI requirements for 100GBASE-SR2 and 200GBASE-SR4

The MDI shall optically mate with the compatible plug on the optical fiber cabling. For 100GBASE-SR2 and 200GBASE-SR4 the MDI adapter or receptacle shall meet the dimensional specifications for interface 7-1-3: *MPO adapter interface - opposed keyway configuration*, or interface 7-1-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4: *MPO female plug connector, flat interface for 2 to 12 fibers*, as defined in IEC 61754-7-1. Figure 138–8 shows an MPO female plug connector with flat interface, and an MDI. The MDI connection shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

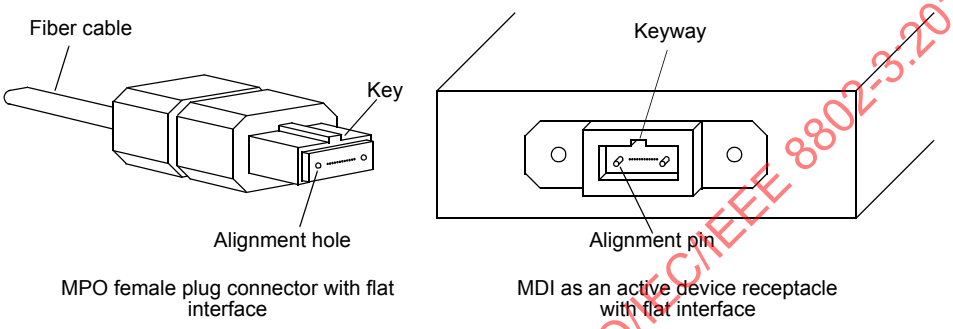


Figure 138–8—MPO female plug with flat interface and MDI active device receptacle with flat interface

138.11 Protocol implementation conformance statement (PICS) proforma for Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4[13]

138.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

138.11.2 Identification

138.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

138.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[13] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

138.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*SR	50GBASE-SR PMD	138.7	Device supports requirements for 50GBASE-SR PHY	O	Yes [ ] No [ ]
*SR2	100GBASE-SR2 PMD	138.7	Device supports requirements for 100GBASE-SR2 PHY	O	Yes [ ] No [ ]
*SR4	200GBASE-SR4 PMD	138.7	Device supports requirements for 200GBASE-SR4 PHY	O	Yes [ ] No [ ]
*INS	Installation / cable	138.10.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	138.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	138.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	138.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	138.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	138.4	Registers and interface supported	O	Yes [ ] No [ ]

138.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4

138.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R or 100GBASE-R or 200GBASE-R PCS and PMA	138.1		M	Yes [ ]
F2	Integration with management functions	138.1		O	Yes [ ] No [ ]
F3	Bit error ratio	138.1.1	Meets the BER specified in 138.1.1	M	Yes [ ]
F4	Transmit function	138.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
F5	Mapping between optical signal and logical signal for transmitter	138.5.2	Optical power levels from lowest to highest correspond to tx_symbols zero, one, two, and three, respectively	M	Yes [ ]
F6	Receive function	138.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of n optical signals to n electrical signals	138.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	138.5.3	Optical power levels from lowest to highest correspond to rx_symbols zero, one, two, and three, respectively	M	Yes [ ]
F9	Global Signal Detect function	138.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	138.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all n lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	138.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 138–6	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	138.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

138.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	138.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	138.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_lane_by_lane_transmit_ disable function	138.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD lane-by-lane transmit disable	138.5.8	Disables each optical transmitter independently if M3 = No	!MD:O	Yes [ ] No [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
M5	PMD_fault function	138.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_transmit_fault function	138.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M7	PMD_receive_fault function	138.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

138.11.4.3 PMD to MDI optical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Transmitter meets specifications in Table 138–8	138.7.1	Per definitions in 138.8	M	Yes [ ]
S2	Receiver meets specifications in Table 138–9	138.7.2	Per definitions in 138.8	M	Yes [ ]

138.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	138.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and spectral width	138.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	138.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA_{outer} measurements	138.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	138.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	138.8.6	Per IEC 61280-2-2	M	Yes [ ]
OM7	Transmitter transition time	138.8.7	Each lane	M	Yes [ ]
OM8	$RIN_{12}OMA$ measurement procedure	138.8.8	Each lane	M	Yes [ ]
OM9	Stressed receiver sensitivity	138.8.10	See 138.8.10	M	Yes [ ]

138.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	138.9.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1M	138.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	138.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

138.11.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	138.10	Meets requirements specified in Table 138–14	INS:M	Yes [ ] N/A [ ]
OC2	Optical fiber characteristics	138.10.1	Per Table 138–15	INS:M	Yes [ ] N/A [ ]
OC3	Maximum discrete reflectance	138.10.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
OC4	MDI layout for 100GBASE-SR2	138.10.3.1	Optical lane assignments per Figure 138–6	SR2:M	Yes [ ] N/A [ ]
OC5	MDI layout for 200GBASE-SR4	138.10.3.1	Optical lane assignments per Figure 138–7	SR4:M	Yes [ ] N/A [ ]
OC6	MDI mating, 50GBASE-SR	138.10.3.2	MDI optically mates with plug on the cabling, performance grade Bm/2m	SR:M	Yes [ ] N/A [ ]
OC7	MDI requirements for 50GBASE-SR	138.10.3.2	Per IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]
OC8	MDI mating, 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	MDI optically mates with plug on the cabling	(SR2 or SR4):M	Yes [ ] N/A [ ]
OC9	MDI dimensions	138.10.3.3	Per IEC 61754-7-1 interface 7-1-1	M	Yes [ ]
OC10	Cabling connector dimensions	138.10.3.3	Per IEC 61754-7-1 interface 7-1-1	INS:M	Yes [ ] N/A [ ]
OC11	MDI requirements for 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m	INS*(SR2 or SR4):M	Yes [ ] N/A [ ]

139. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR

139.1 Overview

This clause specifies the 50GBASE-FR and the 50GBASE-LR PMDs together with the single-mode fiber medium. The optical signals generated by these two PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 139–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 139–1—Physical Layer clauses associated with the 50GBASE-FR and 50GBASE-LR PMDs

Associated clause	50GBASE-FR, 50GBASE-LR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC for 50GBASE-R	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]50GMII is an optional interface. However, if the appropriate interface is not implemented, a conforming implementation must behave functionally as though the RS and 50GMII were present.

Figure 139–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 131.2.

50GBASE-FR and 50GBASE-LR PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

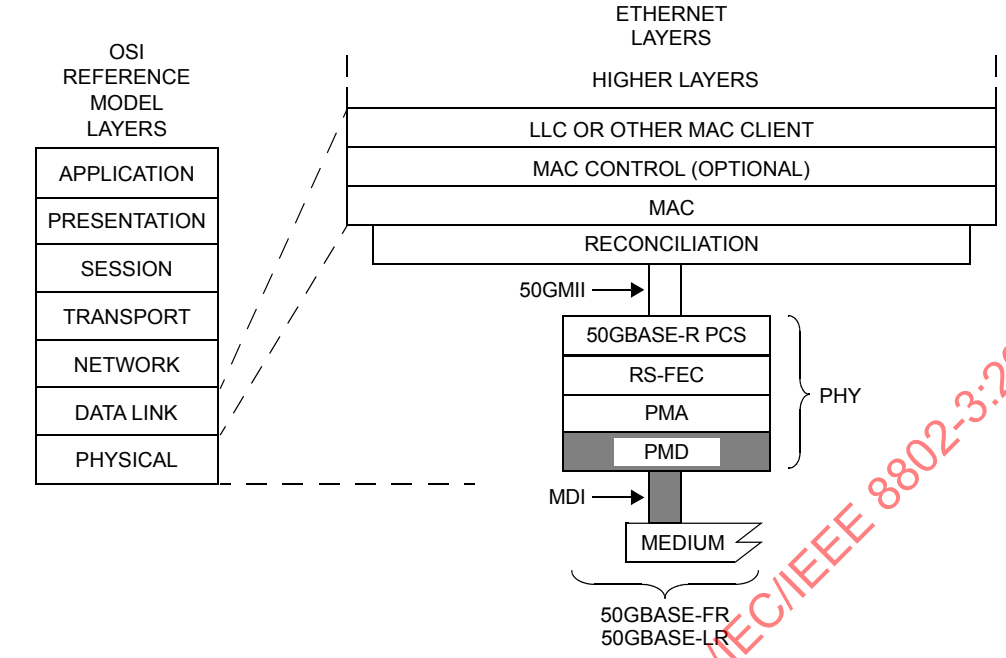


Figure 139–1—50GBASE-FR and 50GBASE-LR PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

139.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.275) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134) and PCS (Clause 133). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

139.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-FR and 50GBASE-LR PMDs. The service interface for these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-FR and 50GBASE-LR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 139.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 139.1.1.

139.3 Delay and Skew

139.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-FR and 50GBASE-LR PMDs including 2 m of fiber in one direction shall be no more than 512 bit times (2 pause_quantum or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 131.4 and its references.

139.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes must be kept within limits so that the information on the lanes can be reassembled by the FEC. The Skew Variation must also be limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

139.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 139–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 139–3.

Table 139–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 139–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

139.5 PMD functional specifications

The 50GBASE-FR and 50GBASE-LR PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

139.5.1 PMD block diagram

The PMD block diagram is shown in Figure 139–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 139.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 139.10.3). Unless specified otherwise, all receiver measurements and tests defined in 139.7 are made at TP3.

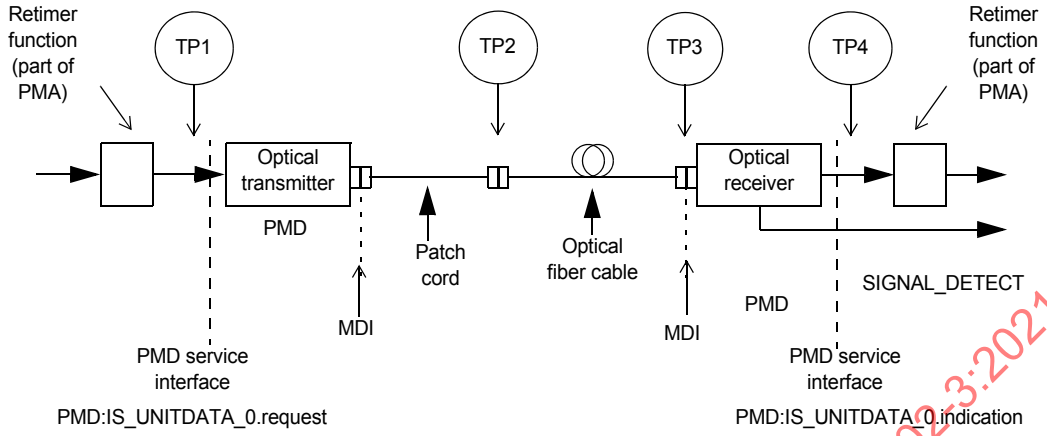


Figure 139–2—Block diagram for 50GBASE-FR and 50GBASE-LR transmit/receive paths

139.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal stream. The optical signal stream shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The four optical power levels in the signal stream in order from lowest to highest shall correspond to tx_symbols zero, one, two, and three, respectively.

139.5.3 PMD receive function

The PMD receive function shall convert the optical signal stream received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbols zero, one, two, and three, respectively.

139.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 139–4. The PMD receiver is not required to verify whether a compliant 50GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Table 139–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –16 dBm	FAIL
[(Optical power at TP3 ≥ average receive power in Table 139–7) AND (compliant 50GBASE-R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

139.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

139.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 139–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

139.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

139.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

139.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

139.6 PMD to MDI optical specifications for 50GBASE-FR and 50GBASE-LR

The operating ranges for the 50GBASE-FR and 50GBASE-LR PMDs are defined in Table 139–5. A 50GBASE-FR or 50GBASE-LR compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 139–13. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-FR PMD operating at 2.5 km meets the operating range requirement of 2 m to 2 km). The 50GBASE-LR PMD interoperates with the 50GBASE-FR PMD provided that the channel requirements for 50GBASE-FR are met.

Table 139–5—50GBASE-FR and 50GBASE-LR operating ranges

PMD type	Required operating range
50GBASE-FR	2 m to 2 km
50GBASE-LR	2 m to 10 km

139.6.1 50GBASE-FR and 50GBASE-LR transmitter optical specifications

The 50GBASE-FR transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7. The 50GBASE-LR transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7.

Table 139–6—50GBASE-FR and 50GBASE-LR transmit characteristics

Description	50GBASE-FR	50GBASE-LR	Unit
Signaling rate (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Wavelengths (range)	1304.5 to 1317.5		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Average launch power (max)	3	4.2	dBm
Average launch power[a] (min)	–4.1	–4.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	2.8	4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	–2.5	–1.5	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–3.9	–2.9	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	3	3.2	dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3	3.2	dB
Average launch power of OFF transmitter (max)	–16		dBm
Extinction ratio (min)	3.5		dB
Transmitter transition time (max)	34		ps

Table 139–6—50GBASE-FR and 50GBASE-LR transmit characteristics *(continued)*

Description	50GBASE-FR	50GBASE-LR	Unit
$RIN_{17.1}OMA$ (max)	–132	—	dB/Hz
$RIN_{15.6}OMA$ (max)	—	–132	dB/Hz
Optical return loss tolerance (max)	17.1	15.6	dB
Transmitter reflectance[d] (max)	–26		dB

[a]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed this value.
[c]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d]Transmitter reflectance is defined looking into the transmitter.

139.6.2 50GBASE-FR and 50GBASE-LR receive optical specifications

The 50GBASE-FR receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.
The 50GBASE-LR receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.

Table 139–7—50GBASE-FR and 50GBASE-LR receive characteristics

Description	50GBASE-FR	50GBASE-LR	Unit
Signaling rate (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Wavelengths (range)	1304.5 to 1317.5		nm
Damage threshold[a]	5.2	5.2	dBm
Average receive power (max)	3	4.2	dBm
Average receive power[b] (min)	–8.1	–10.8	dBm
Receive power (OMA_{outer}) (max)	2.8	4	dBm
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA_{outer})[c] (max)	Equation (139–1)	Equation (139–2)	dBm
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–5.3	–6.6	dBm
Conditions of stressed receiver sensitivity test:[e]			
Stressed eye closure for PAM4 (SECQ)	3	3.2	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max)	3	3.2	dB

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA_{outer}) (max) is informative and is defined for a transmitter with a value of SECQ up to 3 dB for 50GBASE-FR and 3.2 dB for 50GBASE-LR.
[d]Measured with conformance test signal at TP3 (see 139.7.10) for the BER specified in 139.1.1.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

139.6.3 50GBASE-FR and 50GBASE-LR illustrative link power budgets

Illustrative power budgets and penalties for 50GBASE-FR and 50GBASE-LR channels are shown in Table 139–8.

Table 139–8—50GBASE-FR and 50GBASE-LR illustrative link power budgets

Parameter	50GBASE-FR	50GBASE-LR	Unit
Power budget (for maximum TDECQ)	7.4	10.1	dB
Operating distance	2	10	km
Channel insertion loss	4[a]	6.3[b]	dB
Maximum discrete reflectance	See 139.10.2.2	See 139.10.2.2	dB
Allocation for penalties[c] (for maximum TDECQ)	3.4	3.8	dB
Additional insertion loss allowed	0	0	dB

[a]The channel insertion loss is calculated using the maximum distance specified in Table 139–5 for 50GBASE-FR and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 139.10.2.1.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 139–5 for 50GBASE-LR and fiber attenuation of 0.43 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 139.10.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

139.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

139.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 139–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 139–10 may be used to perform that test. The test patterns used in this clause are shown in Table 139–9.

Table 139–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle encoded by RS-FEC	82.2.11[a], 134
6	SSPRQ	120.5.11.2.3

[a]As modified by Clause 133.

Table 139–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 50GBASE-R signal	139.7.2
Side-mode suppression ratio	3, 5, 6 or valid 50GBASE-R signal	139.7.2
Average optical power	3, 5, 6 or valid 50GBASE-R signal	139.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	139.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	139.7.5
Extinction ratio	4 or 6	139.7.6
Transmitter transition time	Square wave or 6	139.7.7
$RIN_{15.1}OMA$ and $RIN_{16.5}OMA$	Square wave	139.7.8
Stressed receiver conformance test signal calibration	6	139.7.10.2
Stressed receiver sensitivity	3 or 5	139.7.10

139.7.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the ranges given in Table 139–6 for 50GBASE-FR and 50GBASE-LR, if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 139–10.

139.7.3 Average optical power

The average optical power shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using the methods given in IEC 61280-1-1.

139.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 139–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 139–3.

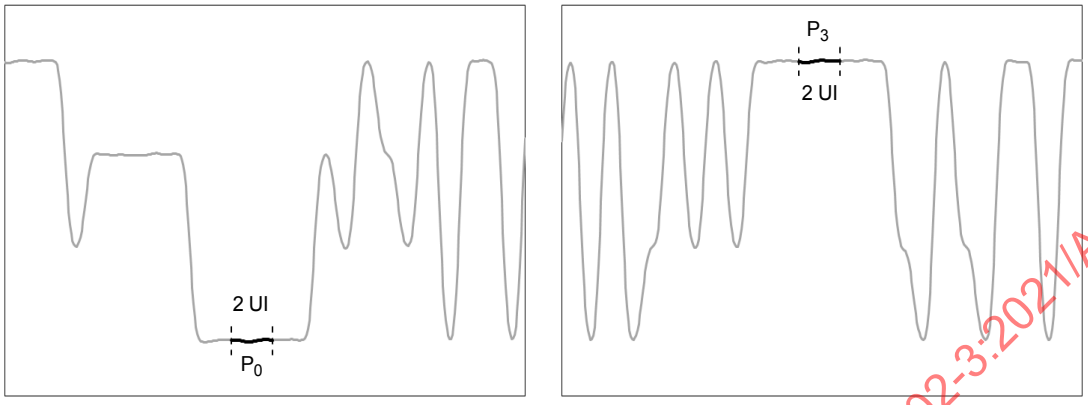


Figure 139–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

139.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using the methods specified in 139.7.5.1, 139.7.5.2, and 139.7.5.3.

TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in 139.7.5.2), as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a reference receiver, and equalized with the reference equalizer (as described in 139.7.5.4). The reference receiver and equalizer may be implemented in software or may be part of the oscilloscope.

Table 139–10 specifies the test patterns to be used for measurement of TDECQ.

139.7.5.1 TDECQ conformance test setup

A block diagram for the TDECQ conformance test is shown in Figure 139–4. Other equivalent measurement implementations may be used with suitable calibration.

The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 139–11. The state of polarization of the back reflection is adjusted to create the greatest RIN. The signal is tested with the optical channel described in 139.7.5.2. The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The test pattern (specified in Table 139–11) is transmitted repetitively and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 139.7.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

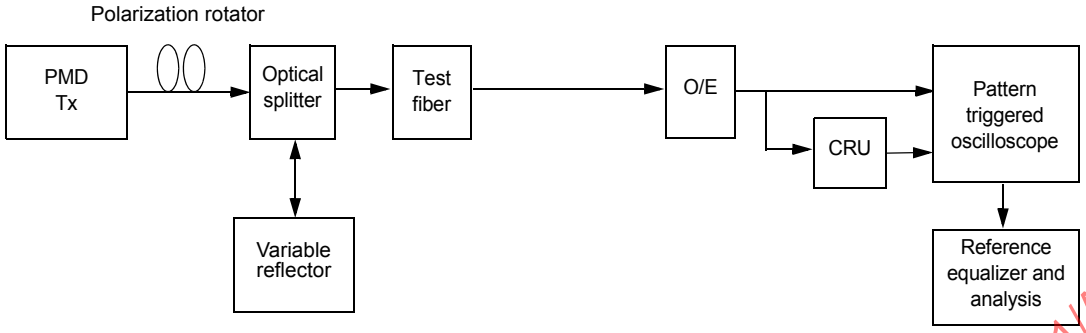


Figure 139–4—TDECQ conformance test block diagram

139.7.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 139–11.

Table 139–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
50GBASE-FR	$0.0465 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.0465 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	17.1 dB	0.8 ps
50GBASE-LR	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	15.6 dB	0.8 ps

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 2 km for 50GBASE-FR and 10 km for 50GBASE-LR.
[b]There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c]The optical return loss is applied at TP2.

A 50GBASE-FR or 50GBASE-LR transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 139–11 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 139–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 139–11.

139.7.5.3 TDECQ measurement method

TDECQ for 50GBASE-FR and 50GBASE-LR is measured as described in 121.8.5.3 with the following exceptions:

— The reference equalizer is as specified in 139.7.5.4.

— P_{th1}, P_{th2}, and P_{th3} are varied from their nominal values by up to ±1% of OMA_{outer} in order to optimize TDECQ. The same three thresholds are used for both the left and the right histogram.

139.7.5.4 TDECQ reference equalizer

The reference equalizer for 50GBASE-FR and 50GBASE-LR is a 5 tap, T spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 139–5. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

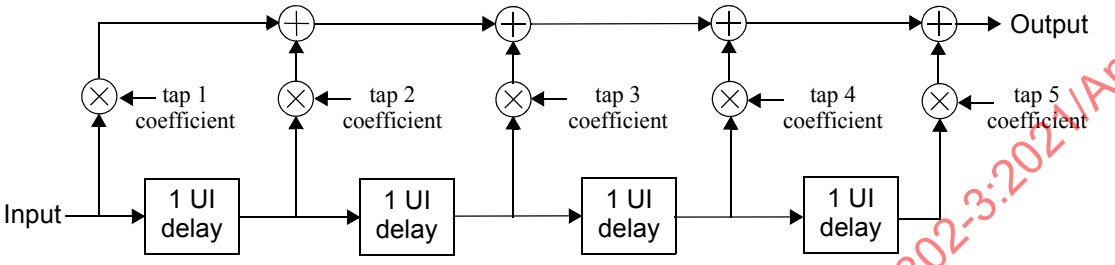


Figure 139–5—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver equalizer implementation.

139.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 139–6 for 50GBASE-FR and 50GBASE-LR if measured using a test pattern specified for extinction ratio in Table 139–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 139–3.

139.7.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 139–6 if measured using a test pattern specified for transmitter transition time in Table 139–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 139.7.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

139.7.8 Relative intensity noise ($RIN_{17.1}OMA$ and $RIN_{15.6}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 17.1 dB for 50GBASE-FR and 15.6 dB for 50GBASE-LR.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).
c) The test pattern is according to Table 139–10.

139.7.9 Receiver sensitivity

For 50GBASE-FR, receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 3 dB. Receiver sensitivity should meet Equation (139–1), which is illustrated in Figure 139–6.

For 50GBASE-LR, receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (139–2), which is illustrated in Figure 139–6.

$$RS = \max(-6.9, SECQ - 8.3) \quad \text{(dBm)} \tag{139–1}$$

$$RS = \max(-8.4, SECQ - 9.8) \quad \text{(dBm)} \tag{139–2}$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

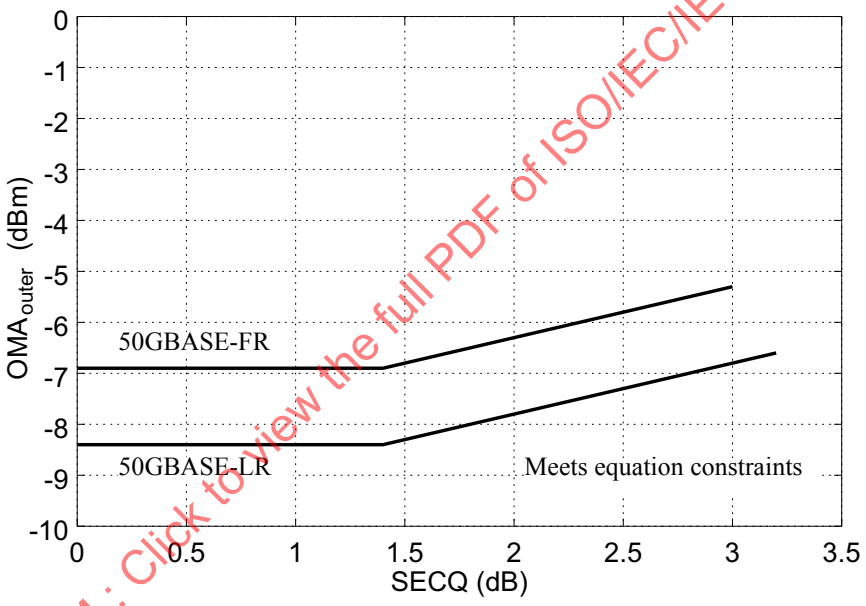


Figure 139–6—Illustration of receiver sensitivity

139.7.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 139–7 for 50GBASE-FR and 50GBASE-LR if measured using the method defined in 139.7.10.1 and 139.7.10.3, with the conformance test signal at TP3 as described in 139.7.10.2, using the test pattern specified for SRS in Table 139–10.

Any of the patterns specified for SRS in Table 139–10 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

139.7.10.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 139–7. The patterns used for the received conformance signal are specified in Table 139–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 139.7.10.2 and has sinusoidal jitter applied as specified in 121.8.9.4. A suitable test set is needed to characterize the signal used to test the receiver. Stressed receiver conformance test signal verification is described in 139.7.10.3.

The low-pass filter is used to create ISI. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the finite edge rates, also causes some jitter.

The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferer, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferer, and the low-pass filter are adjusted so that the SECQ specified in Table 139–7 is met, according to the methods specified in 139.7.10.2.

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be negligible.

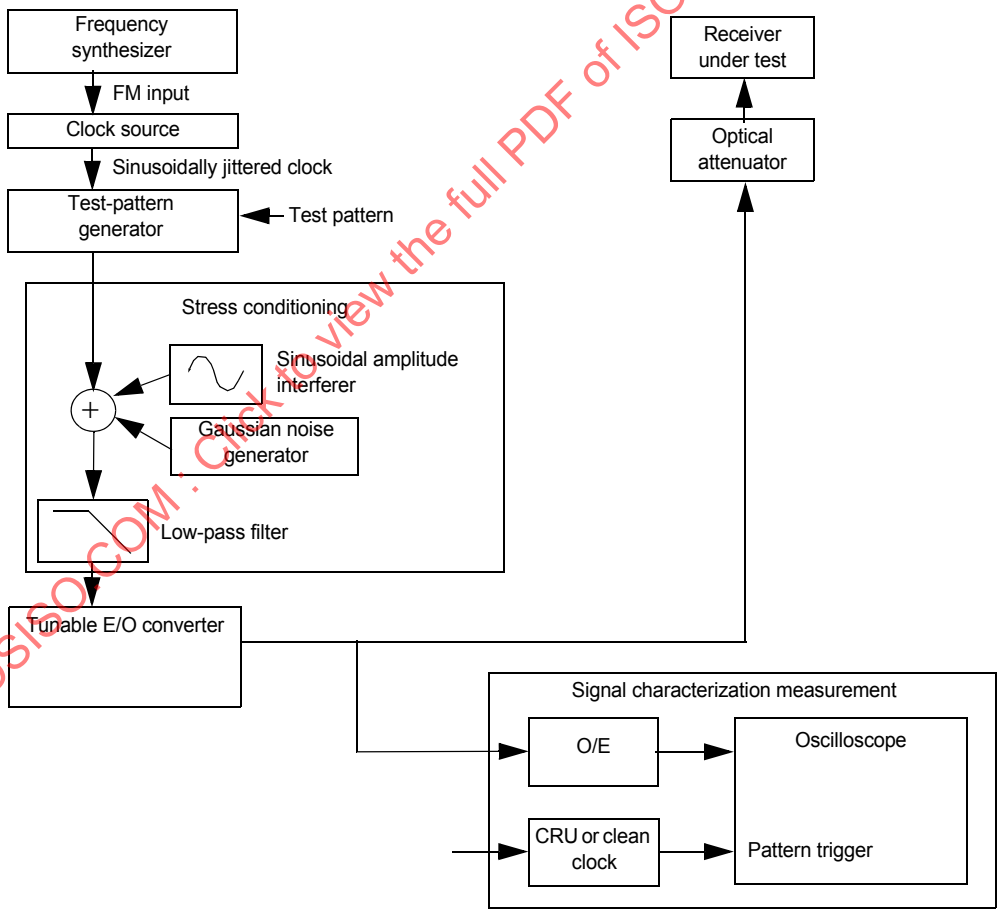


Figure 139–7—Stressed receiver conformance test block diagram

139.7.10.2 Stressed receiver conformance test signal characteristics and calibration

The stressed receiver conformance test signal characteristics and calibration methods are as described in 121.8.9.2 with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 139.7.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 139–6.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{17.1}OMA$ and $RIN_{15.6}OMA$ of the SRS test source for 50GBASE-FR and 50GBASE-LR, respectively, should be no greater than the values specified in Table 139–6.
- An example stressed receiver conformance test setup is shown in Figure 139–7; however, alternative test setups that generate equivalent stress conditions may be used.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 139–6 for 50GBASE-FR and 50GBASE-LR.
- The required values of the "Stressed receiver sensitivity (OMA_{outer}) (max)", "Stressed eye closure for PAM4 (SECQ)", and "SECQ – $10\log_{10}(C_{eq})$ (max)" are as given in Table 139–7 for 50GBASE-FR and 50GBASE-LR.
- The restriction that at least half of the dB value of the SECQ is due to the frequency response of the combination of the low-pass filter and the E/O converter does not apply.

139.7.10.3 Stressed receiver conformance test signal verification

The SECQ of the stressed receiver conformance test signal is measured according to 139.7.5, except that the test fiber is not used. The clock output from the clock source in Figure 139–7 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 139–7) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is understressed may result in the deployment of non-compliant receivers. The noise/jitter introduced by the O/E, filters, and oscilloscope should be negligible or the results should be corrected for its effects. While the details of test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 139.7.10.2 and 121.8.9.4.

139.8 Safety, installation, environment, and labeling

139.8.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

139.8.2 Laser safety

50GBASE-FR and 50GBASE-LR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[14]

139.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

139.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-FR or 50GBASE-LR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

139.8.5 Electromagnetic emission

A system integrating a 50GBASE-FR or 50GBASE-LR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

139.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

139.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-FR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 139.8.2.

[14] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

139.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 139–8.

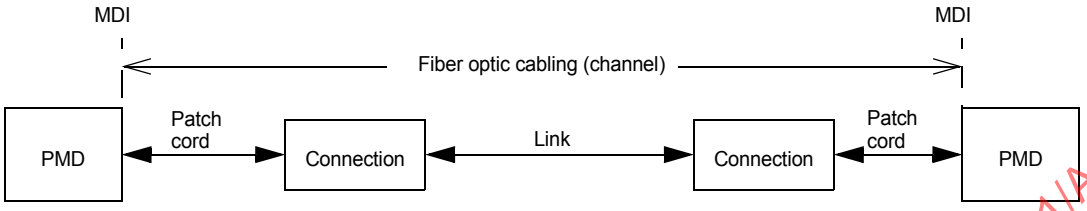


Figure 139–8—Fiber optic cabling model

The channel insertion loss is given in Table 139–12. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-7/method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 139–12—Fiber optic cabling (channel) characteristics

Description	50GBASE-FR	50GBASE-LR	Unit
Operating distance (max)	2	10	km
Channel insertion loss[a, b] (max)	4	6.3	dB
Channel insertion loss (min)	0	0	dB
Positive dispersion[b] (max)	3.2	16	ps/nm
Negative dispersion[b] (min)	–3.7	–18.6	ps/nm
DGD_max[c]	3	8	ps
Optical return loss (min)	25	22	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1304.5 nm to 1317.5 nm for 50GBASE-FR and 50GBASE-LR.
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system must tolerate.

139.10 Characteristics of the fiber optic cabling (channel)

The 50GBASE-FR and 50GBASE-LR fiber optic cabling shall meet the specifications defined in Table 139–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

139.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion unshifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 139–13 where they differ.

Table 139–13—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.43[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \le \lambda_0 \le 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.43 dB/km at 1304.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation 10 km for 50GBASE-LR.

139.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 139–8, consists of a mated pair of optical connectors.

139.10.2.1 Connection insertion loss

The maximum link distance for 50GBASE-LR is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. The maximum link distance for 50GBASE-FR is based on an allocation of 3 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 139–12 are met.

139.10.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 139–14 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 139–14—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance	
	50GBASE-FR	50GBASE-LR
1	–25 dB	–22 dB
2	–31 dB	–29 dB
4	–35 dB	–33 dB
6	–38 dB	–35 dB
8	–40 dB	–37 dB
10	–41 dB	–39 dB

139.10.3 Medium Dependent Interface (MDI) requirements

The 50GBASE-FR or 50GBASE-LR PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 139–8). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 139.5.1, not at the MDI.

139.11 Protocol implementation conformance statement (PICS) proforma for Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR[15]

139.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

139.11.2 Identification

139.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

139.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-2018, Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-2018.)	

Date of Statement	

[15] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

139.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*FR	50GBASE-FR PMD	139.6	Device supports requirements for 50GBASE-FR PHY	O.1	Yes [ ] No [ ]
*LR	50GBASE-LR PMD	139.6	Device supports requirements for 50GBASE-LR PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	139.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	139.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	139.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	139.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	139.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	139.4	Registers and interface supported	O	Yes [ ] No [ ]

139.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR

139.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R PCS and PMA	139.1		M	Yes [ ]
F2	Integration with management functions	139.1		O	Yes [ ] No [ ]
F3	Bit error ratio	139.1.1	Meets the BER specified in 139.1.1	M	Yes [ ]
F4	Transmit function	139.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F6	Mapping between optical signal and logical signal for transmitter	139.5.2	Optical power levels from lowest to highest correspond to tx_symbols zero, one, two, and three, respectively	M	Yes [ ]
F7	Receive function	139.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
F8	Conversion of optical signal to electrical signal	139.5.3	For delivery to the PMD service interface	M	Yes [ ]
F9	Mapping between optical signal and logical signal for receiver	139.5.3	Optical power levels from lowest to highest correspond to rx_symbols zero, one, two, and three, respectively	M	Yes [ ]
F10	Global Signal Detect function	139.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F11	Global Signal Detect behavior	139.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F12	PMD reset function	139.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

139.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	139.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	139.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_fault function	139.5.7	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	139.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	139.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

139.11.4.3 PMD to MDI optical specifications for 50GBASE-FR

Item	Feature	Subclause	Value/Comment	Status	Support
FRF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	FR:M	Yes [ ] N/A [ ]
FRF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	FR:M	Yes [ ] N/A [ ]

139.11.4.4 PMD to MDI optical specifications for 50GBASE-LR

Item	Feature	Subclause	Value/Comment	Status	Support
LRF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	LR:M	Yes [ ] N/A [ ]
LRF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	LR:M	Yes [ ] N/A [ ]

139.11.4.5 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	139.7	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	139.7.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	139.7.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	139.7.4		M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	139.7.5		M	Yes [ ]
OM6	Extinction ratio	139.7.6		M	Yes [ ]
OM7	Transmitter transition time	139.7.7		M	Yes [ ]
OM8	RIN_{xx}OMA measurement procedure	139.7.8		M	Yes [ ]
OM9	Stressed receiver sensitivity	139.7.10		M	Yes [ ]

139.11.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	139.8.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	139.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	139.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

139.11.4.7 Characteristics of the fiber optic cabling and MD

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	139.10	Meets requirements specified in Table 139–12	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	139.10.2.2	Meets requirements specified in Table 139–14	INS:M	Yes [ ] N/A [ ]
OC3	MDI requirements	139.10.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

140. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR

140.1 Overview

This clause specifies the 100GBASE-DR PMD together with the single-mode fiber medium. The optical signal generated by this PMD type is modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 140–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 140–1—Physical Layer clauses associated with the 100GBASE-DR PMD

Associated clause	100GBASE-DR
81—RS	Required
81—100GMII[a]	Optional
82—PCS	Required
83—100GBASE-R PMA	Optional
91—RS-FEC	Required
83A—CAUI-10 C2C	Optional
83B—CAUI-10 C2M	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4 C2M	Optional
135—100GBASE-P PMA	Required
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The 100GMII is an optional interface. However, if the 100GMII is not implemented, a conforming implementation must behave functionally as though the RS and 100GMII were present.

Figure 140–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

100GBASE-DR PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

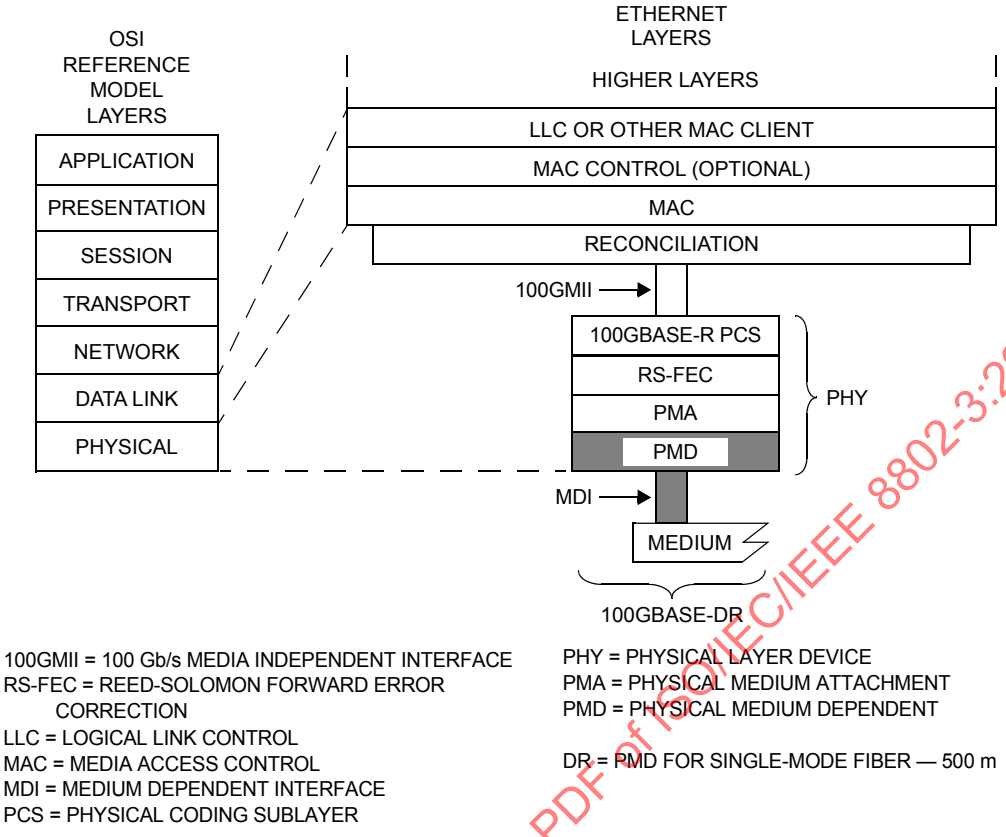


Figure 140–1—100GBASE-DR PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

140.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.275) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 91) and PCS (Clause 82). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

140.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-DR PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 100GBASE-DR PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 53.125 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 53.125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 140.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 140.1.1.

140.3 Delay and Skew

140.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-DR PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

140.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes must be kept within limits so that the information on the FEC lanes can be reassembled by the FEC. The Skew Variation must also be limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP0 to SP7 shown in Figure 80–8.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 83.5.3.4. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 80.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

140.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 140–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 140–3.

Table 140–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 140–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

140.5 PMD functional specifications

The 100GBASE-DR PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

140.5.1 PMD block diagram

The PMD block diagram is shown in Figure 140–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 140.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 140.10.3). Unless specified otherwise, all receiver measurements and tests defined in 140.7 are made at TP3.

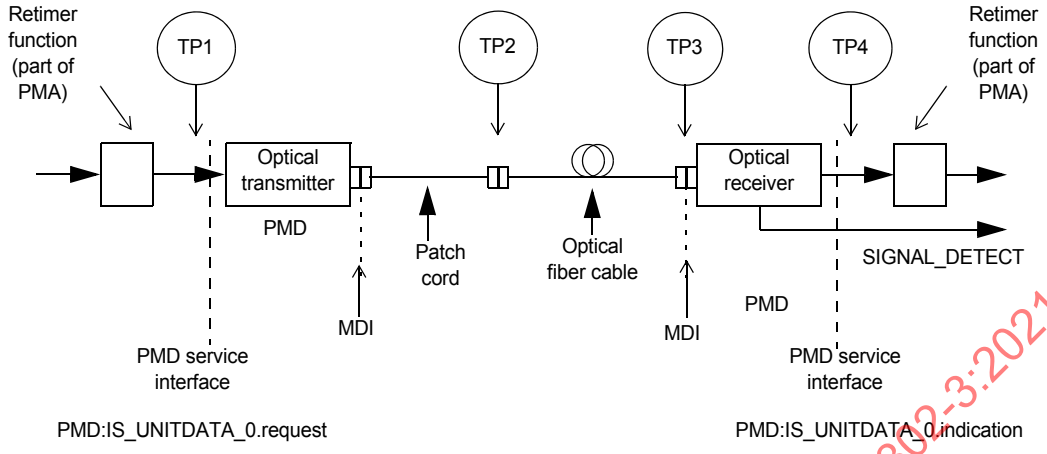


Figure 140–2—Block diagram for 100GBASE-DR transmit/receive paths

140.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal stream. The optical signal stream shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The four optical power levels in the signal stream in order from lowest to highest shall correspond to tx_symbols zero, one, two, and three, respectively.

140.5.3 PMD receive function

The PMD receive function shall convert the optical signal stream received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbols zero, one, two, and three, respectively.

140.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 140–4. The PMD receiver is not required to verify whether a compliant 100GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Table 140–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –15 dBm	FAIL
[(Optical power at TP3 ≥ average receive power (min) Table 140–7) AND (compliant 100GBASE–R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

140.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

140.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 140–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

140.5.7 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

140.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

140.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

140.6 PMD to MDI optical specifications for 100GBASE-DR

The operating range for the 100GBASE-DR PMD is defined in Table 140–5. A 100GBASE-DR compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 140–13. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-DR PMD operating at 600 m meets the operating range requirement of 2 m to 500 m).

Table 140–5—100GBASE-DR operating range

PMD type	Required operating range
100GBASE-DR	2 m to 500 m

140.6.1 100GBASE-DR transmitter optical specifications

The 100GBASE-DR transmitter shall meet the specifications defined in Table 140–6 per the definitions in 140.7.

Table 140–6—100GBASE-DR transmit characteristics

Description	Value	Unit
Signaling rate (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Wavelength (range)	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Average launch power (max)	4	dBm
Average launch power[a] (min)	–2.9	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	–0.8	dBm
Launch power in OMA_{outer} minus TDECQ (min): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB	 –2.2 –1.9	 dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	3.4	dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3.4	dB
Average launch power of OFF transmitter (max)	–15	dBm
Extinction ratio (min)	3.5	dB
Transmitter transition time (max)	17	ps

Table 140–6—100GBASE-DR transmit characteristics *(continued)*

Description	Value	Unit
$RIN_{15.5}OMA$ (max)	–136	dB/Hz
Optical return loss tolerance (max)	15.5	dB
Transmitter reflectance[d] (max)	–26	dB

[a]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 5 dB or TDECQ < 1.1 dB for an extinction ratio of < 5 dB, the OMA_{outer} (min) must exceed this value.
[c]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d]Transmitter reflectance is defined looking into the transmitter.

140.6.2 100GBASE-DR receive optical specifications

The 100GBASE-DR receiver shall meet the specifications defined in Table 140–7 per the definitions in 140.7.

Table 140–7—100GBASE-DR receive characteristics

Description	Value	Unit
Signaling rate (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Wavelengths (range)	1304.5 to 1317.5	nm
Damage threshold[a]	5	dBm
Average receive power (max)	4	dBm
Average receive power[b] (min)	–5.9	dBm
Receive power (OMA_{outer}) (max)	4.2	dBm
Receiver reflectance (max)	–26	dB
Receiver sensitivity (OMA_{outer})[c] (max)	Equation (140–1)	dBm
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–1.9	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ)	3.4	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max)	3.4	dB

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA_{outer}) (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
[d]Measured with conformance test signal at TP3 (see 140.7.10) for the BER specified in 140.1.1.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

140.6.3 100GBASE-DR illustrative link power budget

An illustrative power budget and penalties for 100GBASE-DR channels are shown in Table 140–8.

Table 140–8—100GBASE-DR illustrative link power budget

Parameter	Value	Unit
Power budget (for max TDECQ): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB	 6.5 6.8	 dB dB
Operating distance	500	m
Channel insertion loss[a]	See 140.9	dB
Maximum discrete reflectance	–35	dB
Allocation for penalties[b] (for max TDECQ): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB	 6.5 minus max channel insertion loss per Table 140–12 6.8 minus max channel insertion loss per Table 140–12	 dB dB
Additional insertion loss allowed	0	dB

[a]The channel insertion loss is calculated using the maximum distance specified in Table 140–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 140.10.2.1.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

140.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

140.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 140–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 140–10 may be used to perform that test. The test patterns used in this clause are shown in Table 140–9.

Table 140–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle encoded by RS-FEC	82.2.11, 91
6	SSPRQ	120.5.11.2.3

Table 140–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 100GBASE-R signal	140.7.2
Side-mode suppression ratio	3, 5, 6 or valid 100GBASE-R signal	140.7.2
Average optical power	3, 5, 6 or valid 100GBASE-R signal	140.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	140.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	140.7.5
Extinction ratio	4 or 6	140.7.6
Transmitter transition time	Square wave or 6	140.7.7
$RIN_{15.5}OMA$	Square wave	140.7.8
Stressed receiver conformance test signal calibration	6	140.7.10
Stressed receiver sensitivity	3 or 5	140.7.10

140.7.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the range given in Table 140–6 if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 140–10.

140.7.3 Average optical power

The average optical power shall be within the limits given in Table 140–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 140–10, per the test setup in Figure 53–6.

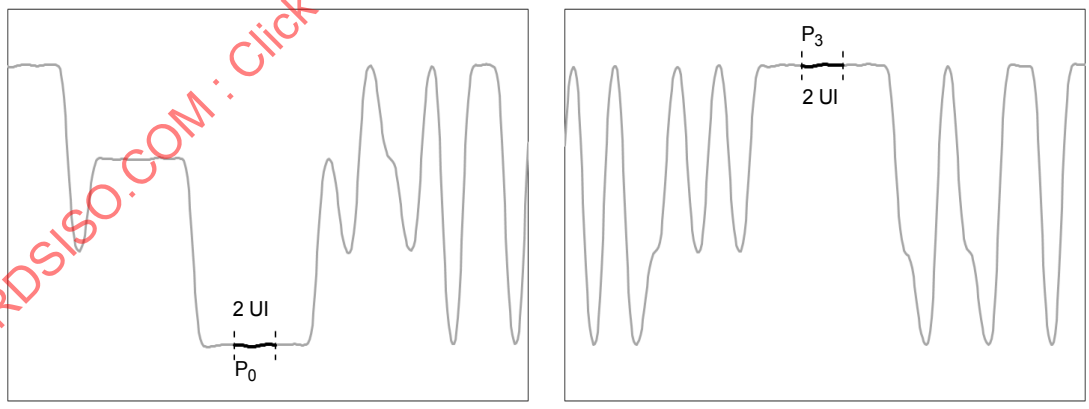


Figure 140–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

140.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 140–6. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 140–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 140–3.

140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ shall be within the limits given in Table 140–6 if measured using the methods specified in 121.8.5.1, 121.8.5.2, and 121.8.5.3 using a reference equalizer as described in 140.7.5.1, with the following exceptions:

— The optical return loss of the transmitter compliance channel is 15.5 dB.

— The signaling rate of the test pattern generator is as given in Table 140–6 and uses a test pattern specified for TDECQ in Table 140–10.

— There are no interfering optical lanes and therefore the delay requirement of at least 31 UI between test pattern on one lane and any other lane, as specified in 121.8.5.1, is redundant.

— The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz and at frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

— The normalized noise power density spectrum, $N(f)$ in Equation (121–9), is equivalent to white noise filtered by a fourth-order Bessel-Thomson response filter with a bandwidth of 26.5625 GHz.

— P_{th1}, P_{th2}, and P_{th3} are varied from their nominal values by up to ±1% of OMA_{outer} in order to optimize TDECQ. The same three thresholds are used for both the left and the right histogram.

140.7.5.1 TDECQ reference equalizer

The reference equalizer for 100GBASE-DR is a 5 tap, T spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 140–4. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3 has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

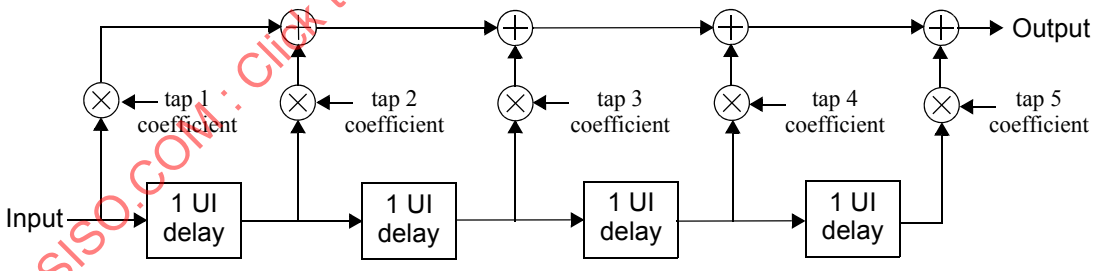


Figure 140–4—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver implementation.

140.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 140–6 if measured using a test pattern specified for extinction ratio in Table 140–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 140–3.

140.7.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 140–6 if measured using a test pattern specified for transmitter transition time in Table 140–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz and at frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 140.7.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

140.7.8 Relative intensity noise ($RIN_{15.5}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 15.5 dB.

b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 53.2 GHz).

140.7.9 Receiver sensitivity

Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (140–1), which is illustrated in Figure 140–5.

$$RS = \max(-3.9, SECQ - 5.3) \quad \text{(dBm)} \tag{140–1}$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

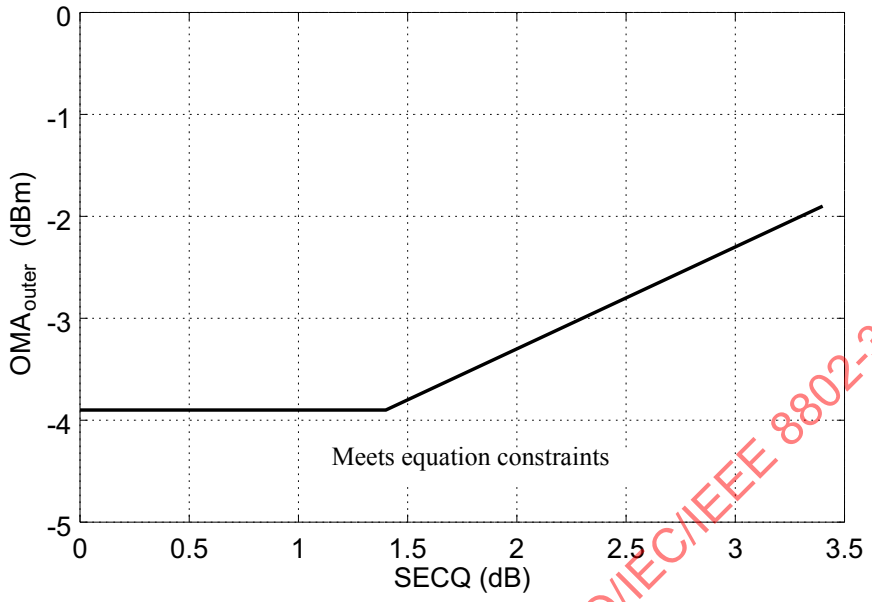


Figure 140–5—Illustration of receiver sensitivity

140.7.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 140–7 if measured using the method defined in 121.8.9, using the test pattern specified for SRS in Table 140–10, with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 140.7.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 140–6.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{15.5}OMA$ of the SRS test source should be no greater than the value specified in Table 140–6.
- An example stressed receiver conformance test setup is shown in Figure 139–7; however, alternative test setups that generate equivalent stress conditions may be used.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 140–6 using test patterns specified in Table 140–10.
- The required values of the “Stressed receiver sensitivity (OMA_{outer}) (max)”, “Stressed eye closure for PAM4 (SECQ)”, and “SECQ – $10\log_{10}(C_{eq})$ (max)” are as given in Table 140–7.
- The restriction that at least half of the dB value of the SECQ is due to the frequency response of the combination of the low-pass filter and the E/O converter in 121.8.9.1 and 121.8.9.2 does not apply.

140.8 Safety, installation, environment, and labeling

140.8.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

140.8.2 Laser safety

100GBASE-DR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[16]

140.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

140.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-DR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

140.8.5 Electromagnetic emission

A system integrating a 100GBASE-DR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

140.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

140.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-DR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 140.8.2.

[16] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

140.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 140–6.

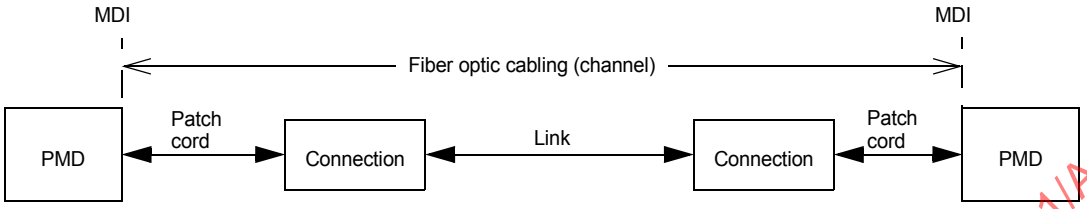


Figure 140–6—Fiber optic cabling model

The channel insertion loss is given in Table 140–11. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. The maximum value of channel insertion loss is dependent on the number and maximum value of the discrete reflectances within the channel as given in Table 140–12. Discrete reflectances below –55 dB may be ignored when determining the supported channel insertion loss. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-7/method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 140–11—Fiber optic cabling (channel) characteristics

Description	100GBASE-DR	Unit
Operating distance (max)	500	m
Channel insertion loss[a, b] (max)	See Table 140–12	dB
Channel insertion loss (min)	0	dB
Positive dispersion[b] (max)	0.8	ps/nm
Negative dispersion[b] (min)	–0.93	ps/nm
DGD_max[c]	2.24	ps
Optical return loss (min)	27	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1304.5 nm to 1317.5 nm
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system must tolerate.

Table 140–12—Maximum channel insertion loss versus number of discrete reflectances

Maximum channel insertion loss (dB)		Number of discrete reflectances > –55 dB and ≤ –45 dB								
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Number of discrete reflectances > –45 dB and ≤ –35 dB	**0**	3	3	3	3	3	3	3	3	3
	1	3	3	3	3	3	3	3	3	3
	2	3	3	3	2.9	2.9	2.9	2.9	2.9	2.9
	3	2.9	2.9	2.9	2.9	2.9	2.8	2.8	2.8	—[a]
	4	2.8	2.8	2.8	2.8	2.7	2.7	2.7	—[a]	—[a]
	5	2.8	2.8	2.7	2.7	2.7	2.6	—[a]	—[a]	—[a]
	6	2.6	2.6	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]

[a]The indicated combination of reflectances does not provide a supported maximum channel insertion loss.

140.10 Characteristics of the fiber optic cabling (channel)

The 100GBASE-DR fiber optic cabling shall meet the specifications defined in Table 140–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

140.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion unshifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 140–13 where they differ.

Table 140–13—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.5[a]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3.

140.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 140–6, consists of a mated pair of optical connectors.

140.10.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 2.75 dB total connection and splice loss. For example, this allocation supports five connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 140–11 are met.

140.10.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less or equal than –35 dB. The number of maximum discrete reflectances in the ranges, > –45 dB and ≤ –35 dB, and, > –55 dB and ≤ –45 dB, is limited to the numbers given in Table 140–12 in relation to the maximum channel insertion loss.

140.10.3 Medium Dependent Interface (MDI)

The 100GBASE-DR PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 140–6). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 140.5.1, not at the MDI.