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AMENDMENT 8
2021-10

Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks —

Part 3: Standard for Ethernet

AMENDMENT 8: Physical layer specifications and management parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s automotive electrical ethernet

Télécommunications et échange entre systèmes informatiques — Exigences pour les réseaux locaux et métropolitains —

Partie 3: Norme pour Ethernet

AMENDEMENT 8: Spécifications des couches physiques et paramètres de gestion pour l'ethernet électrique automobile à 2,5 Gb/s, 5Gb/s et 10 Gb/s

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IEEE Std 802.3ch™-2020
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018,
IEEE Std 802.3bt™-2018,
IEEE Std 802.3cd™-2018,
IEEE Std 802.3cn™-2019,
IEEE Std 802.3cg™-2019,
IEEE Std 802.3cq™-2020,
and IEEE Std 802.3cm™-2020)

IEEE Standard for Ethernet

Amendment 8: Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet

Developed by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 4 June 2020

IEEE SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2018 adds physical layer specifications and management parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation on a single balanced pair of conductors suitable for automotive applications.

Keywords: 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1, Ethernet, IEEE 802.3ch™, MASTER-SLAVE, Medium Dependent Interface, Physical Coding Sublayer, Physical Layer, Physical Medium Attachment

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Introduction

This introduction is not part of IEEE Std 802.3ch-2020, IEEE Standard for Ethernet. Amendment 8: Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of IEEE Std 802.3ch-2020 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines

services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb™-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt™-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

IEEE Std 802.3cn™-2019

Amendment 4—This amendment includes changes to IEEE Std 802.3-2018 and adds 50 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications and management parameters for operation over single-mode fiber with reaches of at least 40 km.

IEEE Std 802.3cg™-2019

Amendment 5—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 146 through Clause 148 and Annex 146A and Annex 146B. This amendment adds 10 Mb/s Physical Layer specifications and management parameters for operation on a single balanced pair of conductors.

IEEE Std 802.3cq™-2020

Amendment 6—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 33 and related portions of the standard.

IEEE Std 802.3cm™-2020

Amendment 7—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 150. This amendment adds Physical Layer (PHY) specifications and management parameters for 400 Gb/s operation on four pairs (400GBASE-SR4.2) and eight pairs (400GBASE-SR8) of multimode fiber, over reaches of at least 100 m.

IEEE Std 802.3ch™-2020

Amendment 8—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 149, Annex 149A, Annex 149B, and Annex 149C. This amendment adds physical layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s over a single balanced pair of conductors.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 8: Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018, IEEE Std 802.3bt™-2018, IEEE Std 802.3cd™-2018, IEEE Std 802.3cn™-2019, IEEE Std 802.3cg™-2019, IEEE Std 802.3cq™-2020, and IEEE Std 802.3cm™-2020.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

[1] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Insert the following references in 1.3 in alphanumeric order as follows:

IEC 62153-4-7, Metallic communication cable test methods—Part 4-7: Electromagnetic compatibility (EMC)—Test method for measuring of transfer impedance Z_T and screening attenuation a_S or coupling attenuation a_C of connectors and assemblies up to and above 3 GHz—Triaxial tube in tube method.[2]

1.4 Definitions

Insert a new definition for 10GBASE-T1 after 1.4.69 10GBASE-T as follows:

1.4.69a 10GBASE-T1: IEEE 802.3 Physical Layer specification for a 10 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

Insert a new definition for 2.5GBASE-T1 after 1.4.82 2.5GBASE-T and before 1.4.82a 2.5GBASE-X (as inserted by IEEE Std 802.3cb-2018) as follows:

1.4.82aa 2.5GBASE-T1: IEEE 802.3 Physical Layer specification for a 2.5 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

Insert a new definition for 5GBASE-T1 after 1.4.129 5GBASE-T and before 1.4.129a 5GSEI (as inserted by IEEE Std 802.3cb-2018) as follows:

1.4.129aa 5GBASE-T1: IEEE 802.3 Physical Layer specification for a 5 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

Change the definition of Infofield in 1.4.289 as follows:

1.4.289 Infofield: A 16 octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 55, Clause 113, and Clause 126.) Also a 12-octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 97 and Clause 149.)

Insert a new definition for MultiGBASE-T1 after 1.4.333 MultiGBASE-T (re-numbered from 1.4.334 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018) as follows:

1.4.333a MultiGBASE-T1: PHYs that belong to the set of specific BASE-T1 PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1. (See IEEE Std 802.3, Clause 149.)

Insert a new definition for Type F PoDL System after 1.4.494a Type E PoDL System (as inserted by IEEE Std 802.3cg-2019) as follows:

1.4.494b Type F PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1.

[2]IEC publications are available from the International Electrotechnical Commission (https://www.iec.ch/) and the American National Standards Institute (https://www.ansi.org).

1.5 Abbreviations

Insert the following new abbreviation into the list, in alphanumeric order:

RFER	RS-FEC frame error ratio

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "2.5GBASE-T" (and before the entry for "2.5GBASE-X" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 Clause 149 2.5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "5GBASE-T" (and before the entry for "5GBASE-R" inserted by IEEE Std 802.3cb-2018) as follows:

5GBASE-T1 Clause 149 5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "10GBASE-T" as follows:

10GBASE-T1 Clause 149 10 Gb/s PAM4

30.3.2.1.3 aPhyTypeList

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "2.5GBASE-T" (and before the entry for "2.5GBASE-X" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 Clause 149 2.5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "5GBASE-T" (and before the entry for "5GBASE-R" inserted by IEEE Std 802.3cb-2018) as follows:

5GBASE-T1 Clause 149 5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "10GBASE-T" as follows:

10GBASE-T1 Clause 149 10 Gb/s PAM4

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "2.5GBASE-T" (and before the entry for "2.5GBASE-X" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "5GBASE-T" as follows:

5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "10GBASE-T" as follows:

10GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149

30.5.1.1.4 aMediaAvailable

Change the fifth sentence of the eighth paragraph of the BEHAVIOUR DEFINED AS section of 30.5.1.1.4 as follows:

> Where a Clause 45 MDIO interface is present a zero in the PMA/PMD Receive link status bit (45.2.1.2.4) maps to the enumeration "PMD link fault", a one in the LOF status bit (45.2.2.10.4) maps to the enumeration "WIS frame loss", a one in the LOS status bit (45.2.2.10.5) maps to the enumeration "WIS signal loss", a zero in the PCS Receive link status bit (45.2.3.2.7 or 45.2.3.80.1) maps to the enumeration "PCS link fault", a one in the 10/40/100GBASE-R PCS Latched high BER status bit (45.2.3.16.2) or a one in the MultiGBASE-T1 PCS status 2 Latched high BER status bit (45.2.3.80.4) maps to the enumeration "excessive BER", a zero in the DTE XS receive link status bit (45.2.5.2.7) maps to the enumeration "DXS link fault" and a zero in the PHY XS transmit link status bit (45.2.4.2.7) maps to the enumeration "PXS link fault".;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "2.5GBASE-T" (and before the entry for "2.5GKX" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1	2.5GBASE-T1 as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "5GBASE-T" (and before the entry for "5GKR" inserted by IEEE Std 802.3cb-2018) as follows:

5GBASE-T1	5GBASE-T1 as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "10GBASE-T" as follows:

10GBASE-T1 10GBASE-T1 as specified in Clause 149

30.15 Layer management for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

30.15.1 PoDL PSE managed object class

30.15.1.1 PoDL PSE attributes

30.15.1.1.4 aPoDLPSEType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.15.1.1.4 after the entry for "typeE" (inserted by IEEE Std 802.3cg-2019) as follows:

typeF Type F PoDL PSE

30.15.1.1.5 aPoDLPSEDetectedPDType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.15.1.1.5 after the entry for "typeE" (inserted by IEEE Std 802.3cg-2019) as follows:

typeF Type F PoDL PD

44. Introduction to 10 Gb/s baseband network

44.1 Overview

44.1.1 Scope

Change the first paragraph of 44.1.1 as follows:

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LRM, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, 10GBASE-EW, ~~and~~10GBASE-T, and 10GBASE-T1.

44.1.2 Objectives

Insert the following text as new item h) and renumber existing item h) to item i) of 44.1.2 as follows:

h) Support operation over a single balanced pair of conductors.

44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

Replace Figure 44-1 with the following figure, which adds 10GBASE-T1:

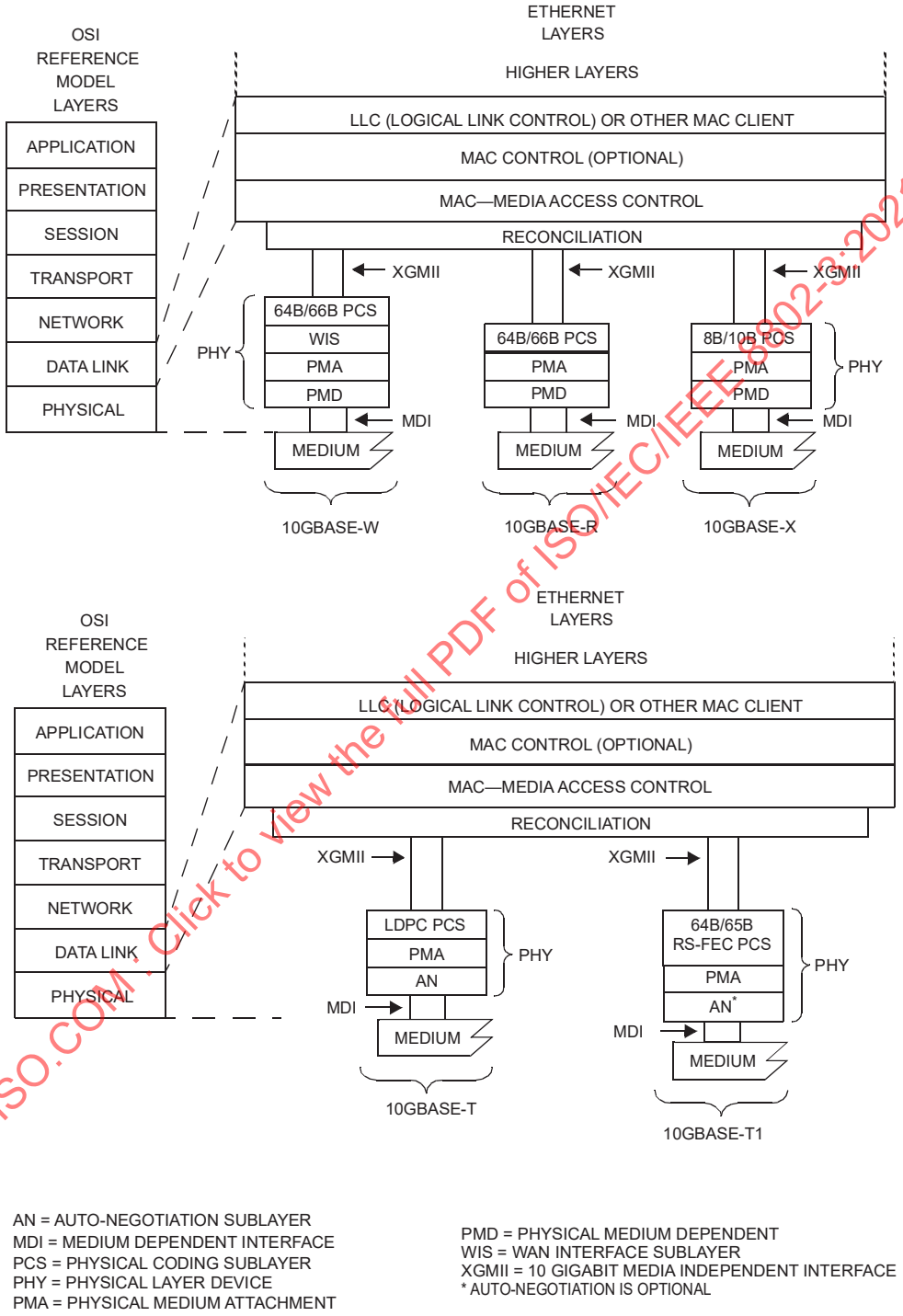


Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

Change item d) of 44.1.3 as follows:

d) The MDI as specified in Clause 53 for 10GBASE-LX4, in Clause 54 for 10GBASE-CX4, in Clause 55 for 10GBASE-T, in Clause 68 for 10GBASE-LRM, in Clause 149 for 10GBASE-T1, and in Clause 52 for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

Change the second paragraph of 44.1.4.1 as follows:

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clause 47, Clause 48, Clause 49, ~~and~~ Clause 55, and Clause 149.

44.1.4.4 Physical Layer signaling systems

Change Table 44–1 as follows:

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause[a]										
	48	49	50	51	52		53	54	55	68	149
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane electrical PMD	~~Twisted pair~~ LDPC PCS & 4-pair PMA	1310 nm Serial MMF PMD	RS–FEC PCS & 1-pair PMA
10GBASE-SR		M[a]		M	M							
10GBASE-SW		M	M	M	M							
10GBASE-LX4	M							M				
10GBASE-CX4	M								M			
10GBASE-LR		M		M		M						
10GBASE-LW		M	M	M		M						
10GBASE-ER		M		M			M					
10GBASE-EW		M	M	M			M					
10GBASE-T										M		
10GBASE-LRM		M		M							M	
10GBASE-T1												M

[a] M = Mandatory

Insert the following paragraph between paragraphs 6 and 7 in 44.1.4.4 as follows:

The term 10GBASE-T1, specified in Clause 149, refers to a specific Physical Layer implementation based upon 64B/65B data coding method placed in an RS-FEC frame that is Gray-code mapped to PAM4 for transmission over a single balanced pair of conductors.

Change former paragraph 7 (now paragraph 8 due to the above insertion) in 44.1.4.4 as follows:

Physical Layer device specifications are contained in Clause 52, Clause 53, Clause 54, Clause 55, ~~and~~ Clause 68, and Clause 149.

44.3 Delay constraints

Insert new rows at the end of Table 44–2 as follows (unchanged rows not shown):

Table 44–2—Round-trip delay constraints (informative)

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
…			
10GBASE-T1 no interleave	10 240	20	See 149.10.
10GBASE-T1 2x interleave	13 824	27	See 149.10.
10GBASE-T1 4x interleave	20 480	40	See 149.10.

44.4 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 44.4 as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45 through Clause 55, ~~and~~ Clause 68, and Clause 149, demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Insert new rows in Table 45–3 for registers 1.2309 to 1.2315 after row for register 1.2308, and change the appropriate reserved row as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.2309	MultiGBASE-T1 PMA control	45.2.1.192
1.2310	MultiGBASE-T1 PMA status	45.2.1.193
1.2311	MultiGBASE-T1 training	45.2.1.194
1.2312	MultiGBASE-T1 link partner training	45.2.1.195
1.2313	MultiGBASE-T1 test mode control	45.2.1.196
1.2314	MultiGBASE-T1 SNR operating margin	45.2.1.197
1.2315	MultiGBASE-T1 minimum SNR margin	45.2.1.198
1.2316	MultiGBASE-T1 user defined data	45.2.1.199
1.2317	MultiGBASE-T1 link partner user defined data	45.2.1.200
1.~~2309~~2318 through 1.32767	Reserved	
…		

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert a new row in Table 45–9 immediately after the row for "2.5GBASE-T, 5GBASE-T" as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1	149.4.2.2
…	

45.2.1.7.5 Receive fault (1.8.10)

Insert a new row in Table 45–10 immediately after row for "2.5GBASE-T, 5GBASE-T" as follows (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1	149.4.2.3
…	

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

Change the identified reserved row in Table 45–19 (as modified by IEEE Std 802.3cg-2019) and insert new rows immediately below the changed row as follows (unchanged rows not shown):

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:~~4~~7	Reserved	Value always 0	RO
1.18.6	10GBASE-T1 ability	1 = PMA/PMD is able to perform 10GBASE-T1 0 = PMA/PMD is not able to perform 10GBASE-T1	RO
1.18.5	5GBASE-T1 ability	1 = PMA/PMD is able to perform 5GBASE-T1 0 = PMA/PMD is not able to perform 5GBASE-T1	RO
1.18.4	2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 2.5GBASE-T1 0 = PMA/PMD is not able to perform 2.5GBASE-T1	RO
…			

[a]RO = Read only

Insert 45.2.1.16.1, 45.2.1.16.2, and 45.2.1.16.3 at the end of 45.2.1.16 as follows:

45.2.1.16.1 10GBASE-T1 ability (1.18.6)

When read as a one, bit 1.18.6 indicates that the PMA/PMD is able to operate as a 10GBASE-T1 PMA type. When read as a zero, bit 1.18.6 indicates that the PMA/PMD is not able to operate as a 10GBASE-T1 PMA type.

45.2.1.16.2 5GBASE-T1 ability (1.18.5)

When read as a one, bit 1.18.5 indicates that the PMA/PMD is able to operate as a 5GBASE-T1 PMA type. When read as a zero, bit 1.18.5 indicates that the PMA/PMD is not able to operate as a 5GBASE-T1 PMA type.

45.2.1.16.3 2.5GBASE-T1 ability (1.18.4)

When read as a one, bit 1.18.4 indicates that the PMA/PMD is able to operate as a 2.5GBASE-T1 PMA type. When read as a zero, bit 1.18.4 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-T1 PMA type.

45.2.1.18 2.5G/5G PMA/PMD extended ability register (Register 1.21)

Insert the following note at the end of 45.2.1.18 (below Table 45–21):

NOTE—2.5GBASE-T1 and 5GBASE-T1 PMA/PMD extended abilities can be found in Register 1.18, see Table 45–19.

45.2.1.185 BASE-T1 PMA/PMD control register (1.2100)

Change the row for bits 1.2100.3:0 in Table 45–149 (as modified by IEEE Std 802.3cg-2019) (unchanged rows not shown) as follows:

Table 45–149—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved ~~0 1 x x = Reserved~~ 0 1 1 1 = Reserved 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.185.2 Type selection (1.2100.3:0)

Insert the following text after the fifth sentence of 45.2.1.185.2 (as modified by IEEE Std 802.3cg-2019) as follows:

When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is 10GBASE-T1.

Insert 45.2.1.192 through 45.2.1.196 after 45.2.1.191 as follows:

45.2.1.192 MultiGBASE-T1 PMA control register (Register 1.2309)

The assignment of bits in the MultiGBASE-T1 PMA control register is shown in Table 45–155a.

Table 45–155a—MultiGBASE-T1 PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2309.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2309.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2309.13:12	Reserved	Value always 0	RO
1.2309.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2309.10:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.1.192.1 PMA/PMD reset (1.2309.15)

Resetting the MultiGBASE-T1 PMA/PMD is accomplished by setting bit 1.2309.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of a MultiGBASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. Bit 1.2309.15 is self-clearing, and the MultiGBASE-T1 PMA/PMD shall return a value of one in bit 1.2309.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation as defined in 149.4.2.1, starting when bit 1.2309.15 is set.

During a reset, the MultiGBASE-T1 PMA/PMD shall respond to reads from register bits 1.2309.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 1.2309.15 is a copy of bit 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PMA/PMD.

45.2.1.192.2 Transmit disable (1.2309.14)

When bit 1.2309.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2309.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2309.14 is a copy of bit 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.192.3 Low power (1.2309.11)

When the low-power ability is supported, the MultiGBASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2309.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the MultiGBASE-T1 PMA/PMD. The behavior of the MultiGBASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power

mode, the device shall, at a minimum, respond to management transactions necessary to exit the low-power mode.

The default value of bit 1.2309.11 is zero.

This operation interrupts data communication.

Bit 1.2309.11 is a copy of bit 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the MultiGBASE-T1 PMA/PMD in low-power mode.

45.2.1.193 MultiGBASE-T1 PMA status register (1.2310)

The assignment of bits in the MultiGBASE-T1 PMA status register is shown in Table 45–155b.

Table 45–155b—MultiGBASE-T1 PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2310.15:12	Reserved	Value always 0	RO
1.2310.11	MultiGBASE-T1 OAM ability	1 = PHY has MultiGBASE-T1 OAM ability 0 = PHY does not have MultiGBASE-T1 OAM ability	RO
1.2310.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2310.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2310.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2310.7:5	Reserved	Value always 0	RO
1.2310.4:3	PrecodeSel	4 3 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	RO
1.2310.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2310.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2310.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LH = Latching High, LL = Latching Low

45.2.1.193.1 MultiGBASE-T1 OAM ability (1.2310.11)

When read as a one, bit 1.2310.11 indicates that the MultiGBASE-T1 PHY supports MultiGBASE-T1 OAM (see 149.3.9). When read as a zero, bit 1.2310.11 indicates that the MultiGBASE-T1 PHY does not support MultiGBASE-T1 OAM.

45.2.1.193.2 EEE ability (1.2310.10)

When read as a one, bit 1.2310.10 indicates that the MultiGBASE-T1 PHY supports EEE. When read as a zero, bit 1.2310.10 indicates that the MultiGBASE-T1 PHY does not support EEE.

45.2.1.193.3 Receive fault ability (1.2310.9)

When read as a one, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.193.4 Low-power ability (1.2310.8)

When read as a one, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD supports the low-power feature. When read as a zero, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD does not support the low-power feature. If the MultiGBASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2309.11 or bit 1.0.11.

45.2.1.193.5 PrecodeSel (1.2310.4:3)

Bits 1.2310.4:3 contain the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see 149.4.2.4.5).

45.2.1.193.6 Receive polarity (1.2310.2)

When read as zero, bit 1.2310.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2310.2 indicates that the polarity of the receiver is reversed.

45.2.1.193.7 Receive fault (1.2310.1)

When read as a one, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2310.9. A MultiGBASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for bit 1.2310.1. The receive fault bit shall be implemented with latching high behavior.

45.2.1.193.8 Receive link status (1.2310.0)

When read as a one, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.194 MultiGBASE-T1 training register (1.2311)

The assignment of bits in the MultiGBASE-T1 training register is shown in Table 45–155c.

Table 45–155c—MultiGBASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2311.15:13	Reserved	Value always 0	RO
1.2311.12:11	Interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, undefined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, undefined for 2.5GBASE-T1 and 5GBASE-T1 1 1: Reserved	R/W
1.2311.10:6	Reserved	Value always 0	RO
1.2311.5	Precoder selection	Controls requested precoder setting 0 = PHY 1 = User	R/W
1.2311.4	Slow Wake request	1 = Alert window start is only immediate frame after refresh 0 = Alert window start is every 8th RS frame after refresh	R/W
1.2311.3:2	User precoder selection	3 2 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	R/W
1.2311.1	MultiGBASE-T1 OAM advertisement	1 = MultiGBASE-T1 OAM ability advertised to link partner 0 = MultiGBASE-T1 OAM ability not advertised to link partner	R/W
1.2311.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.194.1 Interleave request (1.2311.12:11)

Bits 1.2311.12:11 control the Reed-Solomon interleave setting of this PHY. Reed-Solomon interleaving is described in 149.3.2.2.15. This is communicated to the link partner via Infofields as specified in 149.4.2.4.5.

The values of L = 2 and L = 4 are not defined for 2.5GBASE-T1 PHYs, and the value of L = 4 is not defined for 5GBASE-T1 PHYs. If bits 1.2311.12:11 are set to these undefined values, the PHY will communicate these values to the link partner, but the requested interleaver depth is out of scope of this standard and may not be supported by the link partner.

45.2.1.194.2 Precoder selection (1.2311.5)

When bit 1.2311.5 is set to a one, the PHY shall use bits 1.2311.3:2 for the value of PrecodeSel, and when set to a zero the PHY controls the value of PrecodeSel. PrecodeSel is the desired precoder setting communicated to the link partner via the Infofield specified in 149.4.2.4.5.

45.2.1.194.3 Slow Wake request (1.2311.4)

When set as a one, bit 1.2311.4 indicates to the link partner that the local MultiGBASE-T1 PHY may only transmit alert immediately following refresh. When set as a zero, bit 1.2311.4 indicates to the link partner that the local MultiGBASE-T1 PHY may transmit an alert at any eighth RS-FEC frame after a refresh.

45.2.1.194.4 User precoder selection (1.2311.3:2)

When bit 1.2311.5 is a one, bits 1.2311.3:2 are the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see 149.4.2.4.5).

45.2.1.194.5 MultiGBASE-T1 OAM advertisement (1.2311.1)

Support for MultiGBASE-T1 OAM capability shall be advertised if bit 1.2311.1 is set to one. Support for MultiGBASE-T1 OAM capability shall not be advertised if bit 1.2311.1 is set to zero. Support for MultGBASE-T1 OAM capability should only be advertised if it is supported by the PHY.

45.2.1.194.6 EEE advertisement (1.2311.0)

Support for EEE capability shall be advertised if bit 1.2311.0 is set to one. Support for EEE capability shall not be advertised if bit 1.2311.0 is set to zero. Support for EEE operation should only be advertised if it is supported by the PHY.

45.2.1.195 MultiGBASE-T1 link partner training register (1.2312)

The assignment of bits in the MultiGBASE-T1 link partner training register is shown in Table 45–155d. The values in this register are not valid when the link is down.

Table 45–155d—MultiGBASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2312.15:13	Reserved	Value always 0	RO
1.2312.12:11	Link partner interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, undefined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, undefined for 2.5GBASE-T1 and 5GBASE-T1 1 1: Reserved	RO
1.2312.10:5	Reserved	Value always 0	RO
1.2312.4	Link partner Slow Wake requested	1 = Alert window start is only immediate frame after refresh 0 = Alert window start is every 8th RS frame after refresh	RO
1.2312.3:2	Link partner precoder requested	3 2 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	RO

Table 45–155d—MultiGBASE-T1 link partner training register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.2312.1	Link partner MultiGBASE-T1 OAM advertisement	1 = Link partner has MultiGBASE-T1 OAM ability 0 = Link partner does not have MultiGBASE-T1 OAM ability	RO
1.2312.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.195.1 Link partner interleave request (1.2312.12:11)

Bits 1.2312.12:11 contain the Reed-Solomon interleave setting requested by the link partner. Reed-Solomon interleaving is described in 149.3.2.2.15. This is communicated by the link partner via Infofields as specified in 149.4.2.4.5.

The values of L = 2 and L = 4 are not defined for 2.5GBASE-T1 PHYs, and the value of L = 4 is not defined for 5GBASE-T1 PHYs. Bits 1.2312.12:11 will indicate whatever value is received from the link partner, but if the undefined values are received, the requested interleaver depth is out of scope of this standard and may not be supported by the local PHY.

45.2.1.195.2 Link partner Slow Wake requested (1.2312.4)

Bit 1.2312.4 contains the Slow Wake setting received from the link partner. When set as a one, the link partner may only transmit alert immediately following refresh. When set as a zero, the link partner may only transmit an alert at any eighth RS-FEC frame after a refresh.

45.2.1.195.3 Link partner precoder requested (1.2312.3:2)

Bits 1.2312.3:2 contain the precoder setting requested by the link partner. The precoder requested is encoded as the value of precoder_type defined in 149.3.2.2.20.

45.2.1.195.4 Link partner MultiGBASE-T1 OAM advertisement (1.2312.1)

When read as a one, bit 1.2312.1 indicates the link partner is advertising MultiGBASE-T1 OAM capability. When read as a zero, bit 1.2312.1 indicates the link partner is not advertising MultiGBASE-T1 OAM capability. MultiGBASE-T1 OAM capability shall be enabled only when both the local PHY and its link partner are advertising MultiGBASE-T1 OAM capability.

45.2.1.195.5 Link partner EEE advertisement (1.2312.0)

When read as a one, bit 1.2312.0 indicates the link partner is advertising EEE capability. When read as a zero, bit 1.2312.0 indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local PHY and its link partner are advertising EEE capability.

45.2.1.196 MultiGBASE-T1 test mode control register (1.2313)

The assignment of bits in the MultiGBASE-T1 test mode control register is shown in Table 45–155e. The default values for each bit are chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–155e—MultiGBASE-T1 test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2313.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2313.12	Reserved	Value always 0	RO
1.2313.11	Local transmitter precoder override	0 = Normal operation 1 = User override	R/W
1.2313.10:9	Local transmit precoder setting	10 9 0 0 = transmit with no precoder 0 1 = transmit with 1–D precoder 1 0 = transmit with 1+D precoder 1 1 = transmit with $1-D^2$ precoder	R/W
1.2313.8:2	Reserved	Value always 0	RO
1.2313.1:0	Jitter test control	1 0 0 0 = Square wave 0 1 = JP03A Pattern 1 0 = JP03B Pattern 1 1 = Reserved	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.196.1 Test mode control (1.2313.15:13)

Transmitter test mode operations defined by bits 1.2313.15:13, are described in 149.5.1 and Table 149–17. The default value for bits 1.2313.15:13 is zero.

45.2.1.196.2 Local transmitter precoder override (1.2313.11)

When bit 1.2313.11 is set to one, the local transmitter's precoder shall be controlled by the value of bits 1.2313.10:9, and the precoder requested by the link partner in PrecodeSel shall be ignored. When bit 1.2313.11 is set to zero, the transmitter shall ignore bits 1.2313.10:9, and the precoder is set according to the value of PrecodeSel received from the link partner as specified in 149.3.2.2.20. The default value of 1.2313.11 is zero.

45.2.1.196.3 Local transmit precoder setting (1.2313.10:9)

When bit 1.2313.11 is set to one, bits 1.2313.10:9 control the precoder setting of the local transmitter, as defined in 149.3.2.2.20 in the variable precoder_type.

45.2.1.196.4 Jitter test control (1.2313.1:0)

When the transmitter is in test mode 2, bits 1.2313.1:0 control the pattern of the jitter test signal. When the transmitter is not in test mode 2, the setting of bits 1.2313.1:0 has no effect. A value of 00 transmits a square

wave from the transmitter, a value of 01 transmits the JP03A pattern, and a value of 10 transmits the JP03B pattern. See 149.5.2.3.1 and 149.5.2.3.2 for more information.

45.2.1.197 MultiGBASE-T1 SNR operating margin register (Register 1.2314)

Register 1.2314 contains the current SNR operating margin measured at the slicer input for the PMAs in the MultiGBASE-T1 set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x80, 12.7 dB represented by 0xFF, and –12.7 dB represented by 0x01. Implementation of this register is optional.

The assignment of bits in the MultiGBASE-T1 SNR operating margin register is shown in Table 45–155f.

Table 45–155f—MultiGBASE-T1 SNR operating margin register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2314.15:8	MultiGBASE-T1 SNR operating margin	Value of current SNR operating margin in dB	RO
1.2314.7:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.198 MultiGBASE-T1 minimum SNR margin register (Register 1.2315)

Register 1.2315 contains a latched copy of the lowest value observed in the MultiGBASE-T1 SNR operating margin register (1.2314) since the last read. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x80, 12.7 dB represented by 0xFF, and –12.7 dB represented by 0x01. Implementation of this register is optional.

The assignment of bits in the MultiGBASE-T1 minimum SNR margin register is shown in Table 45–155g.

Table 45–155g—MultiGBASE-T1 minimum SNR margin register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2315.15:8	MultiGBASE-T1 minimum SNR margin	Value of minimum observed SNR margin in dB	RO
1.2315.7:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.199 MultiGBASE-T1 user defined data (Register 1.2316)

The assignment of bits for the MultiGBASE-T1 user defined data register is shown in Table 45–155h. The values of the bits in this register are outside the scope of this standard.

Table 45–155h—MultiGBASE-T1 user defined data register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2316.15:0	MultiGBASE-T1 user defined data	16 bits of vendor specific data that the PHY sends to its link partner	R/W

[a]R/W = Read/Write

45.2.1.199.1 MultiGBASE-T1 user defined data (1.2316.15:0)

Bits 1.2316.15:0 contain vendor specific data that the PHY may communicate to its link partner during training.

45.2.1.200 MultiGBASE-T1 link partner user defined data register (Register 1.2317)

The assignment of bits for the MultiGBASE-T1 link partner user defined data register is shown in 45–155i. The values of the bits in this register are outside the scope of this standard.

Table 45–155i—MultiGBASE-T1 link partner user defined data register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2317.15:0	MultiGBASE-T1 link partner user defined data	16 bits of vendor specific data that the PHY may receive from its link partner	RO

[a]RO = Read only

45.2.1.200.1 MultiGBASE-T1 link partner user defined data register (1.2317.15:0)

Bits 1.2317.15:0 contain vendor specific data that the PHY may receive from its link partner during training.

45.2.3 PCS registers

Change the rows for registers 3.2308 through 3.2317, insert new rows for registers 1.2318 to 1.2324 after row for register 1.2317 and change the appropriate reserved row in Table 45–176 as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
…		
3.~~32~~2308	~~1000~~BASE-T1 OAM transmit	45.2.3.72
3.2309 through 3.2312	~~1000~~BASE-T1 OAM message	45.2.3.73
3.2313	~~1000~~BASE-T1 OAM receive	45.2.3.74
3.2314 through 3.2317	Link partner ~~1000~~BASE-T1 OAM message	45.2.3.75
3.2318 through 3.2319	MultiGBASE-T1 OAM status message	45.2.3.76
3.2320 through 3.2321	Link partner MultiGBASE-T1 OAM status message	45.2.3.77
3.2322	MultiGBASE-T1 PCS control	45.2.3.78
3.2323	MultiGBASE-T1 PCS status 1	45.2.3.79
3.2324	MultiGBASE-T1 PCS status 2	45.2.3.80
3.23~~18~~25 through 3.32767	Reserved	
…		

Change the titles, text, and tables in 45.2.3.72 through 45.2.3.75 as follows:

45.2.3.72 ~~1000~~BASE-T1 OAM transmit register (Register 3.2308)

The assignment of bits in the ~~1000~~BASE-T1 OAM transmit register is shown in Table 45–241.

Table 45–241—~~1000~~BASE-T1 OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2308.15	~~1000~~BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit ~~shall~~ self-clears when registers are loaded by the OAM transmit state diagram. ~~machine.~~ 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2308.13	~~1000~~BASE-T1 OAM message received	This bit shall self clear on read. 1 = ~~1000~~BASE-T1 OAM message received by link partner 0 = ~~1000~~BASE-T1 OAM message not received by link partner	RO, LH

Table 45–241—~~1000~~BASE-T1 OAM transmit register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.2308.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO
3.2308.11:8	Message number	User-defined message number to send	R/W
3.2308.7:4	Reserved	Value always 0	RO
3.2308.3	Ping received	Received PingTx value from latest good ~~1000~~BASE-T1 OAM frame received	RO
3.2308.2	Ping transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current ~~1000~~BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.72.1 ~~1000~~BASE-T1 OAM message valid (3.2308.15)

Bit 3.2308.15 shall be set to one when the ~~1000~~BASE-T1 OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted. ~~This register shall be cleared by the state machine~~ Bit 3.2308.15 self-clears to indicate whether the next ~~1000~~BASE-T1 OAM message can be written into the registers.

45.2.3.72.2 Toggle value (3.2308.14)

The state machine shall assign a value alternating between zero and one to associate with the ~~8 octet~~ 8-octet ~~1000~~BASE-T1 OAM message transmitted by the ~~1000BASE-T1~~ PHY. Bit 3.2308.14 should be read and recorded prior to setting 3.2308.15 to one. The recorded value can be correlated with 3.2308.12 as a confirmation that the ~~1000~~BASE-T1 OAM message is received by the link partner.

45.2.3.72.3 ~~1000~~BASE-T1 OAM message received (3.2308.13)

Bit 3.2308.13 shall indicate whether the most recently transmitted ~~1000~~BASE-T1 OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.72.4 Received message toggle value (3.2308.12)

Bit 3.2308.12 indicates the toggle bit value of the ~~1000~~BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2308.13 is one.

45.2.3.72.5 Message number (3.2308.11:8)

Bits 3.2308.11:8 contain the ~~1000~~BASE-T1 OAM message number to be transmitted. This field is user defined but it is recommended that it be used to indicate the meaning of the ~~8 octet~~ 8-octet ~~1000~~BASE-T1

OAM message. If used this way, up to 16 different 8-octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.72.6 Ping received (3.2308.3)

Bit 3.2308.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.72.7 Ping transmit (3.2308.2)

Bit 3.2308.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.72.8 Local SNR (3.2308.1:0)

Bits 3.2308.1:0 are set by the ~~1000~~BASE-T1 PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.73 ~~1000~~BASE-T1 OAM message register (Registers 3.2309 to 3.2312)

The ~~1000~~BASE-T1 OAM message register contains the 8-octet ~~1000~~BASE-T1 OAM message data to be transmitted. The 8-octet message data is user defined and its definition is outside the scope of this standard. See Table 45–242.

Table 45–242—~~1000~~BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2309.15:8	~~1000~~BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2309.7:0	~~1000~~BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2310.15:8	~~1000~~BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2310.7:0	~~1000~~BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2311.15:8	~~1000~~BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2311.7:0	~~1000~~BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2312.15:8	~~1000~~BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2312.7:0	~~1000~~BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

45.2.3.74 ~~1000~~BASE-T1 OAM receive register (Register 3.2313)

The assignment of bits in the ~~1000~~BASE-T1 OAM receive register is shown in Table 45–243.

Table 45–243—~~1000~~BASE-T1 OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2313.15	Link partner ~~1000~~BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. ~~This bit shall self clear when register 3.2317 is read.~~ See 45.2.3.74.1 for self-clearing behavior. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2313.14	Link partner toggle value	Toggle value received with message.	RO
3.2313.13:12	Reserved	Value always 0	RO
3.2313.11:8	Link partner message number	Message number from link partner	RO
3.2313.7:2	Reserved	Value always 0	RO
3.2313.1:0	Link partner SNR	00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current ~~1000~~BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local ~~device~~ PHY to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.74.1 Link partner ~~1000~~BASE-T1 OAM message valid (3.2313.15)

Bit 3.2313.15 shall be set to one when the ~~1000~~BASE-T1 OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8. ~~This register shall be cleared~~ Bit 3.2313.15 shall self-clear when register 3.2317 is read.

45.2.3.74.2 Link partner toggle value (3.2313.14)

Bit 3.2313.14 indicates the toggle value associated with the ~~8 octet~~ 8-octet ~~1000~~BASE-T1 OAM message from the link partner.

45.2.3.74.3 Link partner message number (3.2313.11:8)

Bits 3.2313.11:8 contain the ~~1000~~BASE-T1 OAM message number from the link partner.

45.2.3.74.4 Link partner SNR (3.2313.1:0)

Bits 3.2313.1:0 indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.75 Link partner ~~1000~~BASE-T1 OAM message register (Registers 3.2314 to 3.2317)

The link partner ~~1000~~BASE-T1 OAM message register contains the ~~8 octet~~ 8-octet ~~1000~~BASE-T1 OAM message data from the link partner. ~~Register 3.2313.15 shall be cleared when register 3.2317 is read.~~ See Table 45–244.

Table 45–244—Link partner ~~1000~~BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2314.15:8	Link partner ~~1000~~BASE-T1 OAM message 1	Message octet 1. LSB ~~transmitted~~ received first.	RO
3.2314.7:0	Link partner ~~1000~~BASE-T1 OAM message 0	Message octet 0. LSB ~~transmitted~~ received first.	RO
3.2315.15:8	Link partner ~~1000~~BASE-T1 OAM message 3	Message octet 3. LSB ~~transmitted~~ received first.	RO
3.2315.7:0	Link partner ~~1000~~BASE-T1 OAM message 2	Message octet 2. LSB ~~transmitted~~ received first.	RO
3.2316.15:8	Link partner ~~1000~~BASE-T1 OAM message 5	Message octet 5. LSB ~~transmitted~~ received first.	RO
3.2316.7:0	Link partner ~~1000~~BASE-T1 OAM message 4	Message octet 4. LSB ~~transmitted~~ received first.	RO
3.2317.15:8	Link partner ~~1000~~BASE-T1 OAM message 7	Message octet 7. LSB ~~transmitted~~ received first.	RO
3.2317.7:0	Link partner ~~1000~~BASE-T1 OAM message 6	Message octet 6. LSB ~~transmitted~~ received first.	RO

[a]RO = Read only

Insert 45.2.3.76 through 45.2.3.80 after 45.2.3.75 as follows:

45.2.3.76 MultiGBASE-T1 OAM status message register (Register 3.2318 and 3.2319)

The MultiGBASE-T1 OAM status message register contains octets 8 through 11 of the MultiGBASE-T1 OAM message data to be transmitted. See 149.3.9.2.12 for details on the OAM status message definition. See Table 45–244a.

Table 45–244a—MultiGBASE-T1 OAM status message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2318.15:8	MultiGBASE-T1 OAM status message 9	Message octet 9. LSB transmitted first.	R/W
3.2318.7:0	MultiGBASE-T1 OAM status message 8	Message octet 8. LSB transmitted first.	R/W
3.2319.15:8	MultiGBASE-T1 OAM status message 11	Message octet 11. LSB transmitted first.	R/W
3.2319.7:0	MultiGBASE-T1 OAM status message 10	Message octet 10. LSB transmitted first.	R/W

[a]R/W = Read/Write

45.2.3.77 Link partner MultiGBASE-T1 OAM status message register (Register 3.2320 and 3.2321)

The link partner MultiGBASE-T1 OAM status message register contains octets 8 through 11 of the MultiGBASE-T1 OAM message data from the link partner. See 149.3.9.2.12 for details on the OAM status message definition. See Table 45–244b.

Table 45–244b—Link partner MultiGBASE-T1 OAM status message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2320.15:8	Link partner MultiGBASE-T1 OAM status message 9	Message octet 9. LSB received first.	RO
3.2320.7:0	Link partner MultiGBASE-T1 OAM status message 8	Message octet 8. LSB received first.	RO
3.2321.15:8	Link partner MultiGBASE-T1 OAM status message 11	Message octet 11. LSB received first.	RO
3.2321.7:0	Link partner MultiGBASE-T1 OAM status message 10	Message octet 10. LSB received first.	RO

[a]RO = Read only

45.2.3.78 MultiGBASE-T1 PCS control register (Register 3.2322)

The assignment of bits in the MultiGBASE-T1 PCS control register is shown in Table 45–244c. The default value for each bit of the MultiGBASE-T1 PCS control register is chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–244c—MultiGBASE-T1 PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2322.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2322.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2322.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.78.1 PCS reset (3.2322.15)

Resetting the MultiGBASE-T1 PCS is accomplished by setting bit 3.2322.15 to a one. This action shall set all MultiGBASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the MultiGBASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. Bit 3.2322.15 is self-clearing, and the MultiGBASE-T1 PCS shall return a value of one in bit 3.2322.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to

operation as defined in 149.3.2.1 starting when bit 3.2322.15 is set. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2322.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2322.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PCS.

45.2.3.78.2 Loopback (3.2322.14)

The MultiGBASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2322.14 is set to a one. When bit 3.2322.14 is set to a one, the MultiGBASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2322.14 is zero.

Bit 3.2322.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.79 MultiGBASE-T1 PCS status 1 register (Register 3.2323)

The assignment of bits in the MultiGBASE-T1 PCS status 1 register is shown in Table 45–244d. All the bits in the MultiGBASE-T1 PCS status 1 register are read only; a write to the MultiGBASE-T1 PCS status 1 register shall have no effect.

Table 45–244d—MultiGBASE-T1 PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2323.15:12	Reserved	Value always 0	RO
3.2323.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2323.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2323.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2323.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2323.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2323.6:3	Reserved	Value always 0	RO
3.2323.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2323.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.79.1 Tx LPI received (3.2323.11)

When read as a one, bit 3.2323.11 indicates that the transmit MultiGBASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2323.11 indicates that the transmit MultiGBASE-T1 PCS has not received LPI signaling. Bit 3.2323.11 shall be implemented with latching high behavior.

45.2.3.79.2 Rx LPI received (3.2323.10)

When read as a one, bit 3.2323.10 indicates that the receive MultiGBASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2323.10 indicates that the receive MultiGBASE-T1 PCS has not received LPI signaling. Bit 3.2323.10 shall be implemented with latching high behavior.

45.2.3.79.3 Tx LPI indication (3.2323.9)

When read as a one, bit 3.2323.9 indicates that the transmit MultiGBASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2323.9 indicates that the transmit MultiGBASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.79.4 Rx LPI indication (3.2323.8)

When read as a one, bit 3.2323.8 indicates that the receive MultiGBASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2323.8 indicates that the receive MultiGBASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.79.5 Fault (3.2323.7)

When read as a one, bit 3.2323.7 indicates that the MultiGBASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2323.7 indicates that the MultiGBASE-T1 PCS has not detected a fault condition.

45.2.3.79.6 PCS receive link status (3.2323.2)

When read as a one, bit 3.2323.2 indicates that the MultiGBASE-T1 PCS receive link is up. When read as a zero, bit 3.2323.2 indicates that the MultiGBASE-T1 PCS receive link was down since the last read from this register. Bit 3.2323.2 is a latching low version of bit 3.2324.10. The PCS receive link status bit shall be implemented with latching low behavior.

45.2.3.80 MultiGBASE-T1 PCS status 2 register (Register 3.2324)

The assignment of bits in the MultiGBASE-T1 PCS status 2 register is shown in Table 45–244e. All the bits in the MultiGBASE-T1 PCS status 2 register are read only; a write to the MultiGBASE-T1 PCS status 2 register shall have no effect.

45.2.3.80.1 Receive link status (3.2324.10)

When read as a one, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is not fully operational. Bit 3.2324.10 is a reflection of the pcs_status variable defined in 149.3.8.1.

Table 45–244e—MultiGBASE-T1 PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2324.15:11	Reserved	Value always 0	RO
3.2324.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2324.9	PCS high RFER	1 = PCS reporting a high RFER 0 = PCS not reporting a high RFER	RO
3.2324.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2324.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2324.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2324.5:0	BER count	Count of RS-FEC frame errors since last read	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.80.2 PCS high RFER (3.2324.9)

When read as a one, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS receiver is detecting 16 or more RS-FEC errored blocks in 312 500 bit times (one rfer_timer interval). When read as a zero, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS is detecting fewer than 16 RS-FEC errored blocks in 312 500 bit times. Bit 3.2324.9 is a reflection of the state of the hi_rfer variable defined in 149.3.8.1.

45.2.3.80.3 PCS block lock (3.2324.8)

When read as a one, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has not achieved block lock. Bit 3.2324.8 is a reflection of the state of the block_lock variable defined in 149.3.8.1.

45.2.3.80.4 Latched high BER (3.2324.7)

When read as a one, bit 3.2324.7 indicates that the MultiGBASE-T1 PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2324.7 indicates that the MultiGBASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. Bit 3.2324.7 is a latching high version of the MultiGBASE-T1 PCS high RFER status bit (3.2324.9).

45.2.3.80.5 Latched block lock (3.2324.6)

When read as a one, bit 3.2324.6 indicates that the MultiGBASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2324.6 indicates that the MultiGBASE-T1 PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

Bit 3.2324.6 is a latching low version of the MultiGBASE-T1 PCS block lock status bit (3.2324.8).

45.2.3.80.6 BER count (3.2324.5:0)

The BER counter formed by bits 3.2324.5:0 is a six bit counter as defined by RFER_count in 149.3.8.2. These bits shall be reset to all zeros when the MultiGBASE-T1 PCS status 2 register is read by the management function or upon execution of the MultiGBASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.9 Power Unit Registers

45.2.9.2 PoDL PSE Status 1 register (Register 13.1)

Change the row for bits 13.1.9:7 in Table 45–340 (as modified by IEEE Std 802.3cg-2019) as follows (unchanged rows not shown):

Table 45–340—PoDL PSE Status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
13.1.9:7	PSE Type	9 8 7 1 1 x = Reserved 1 0 1 = Type F PSE~~Reserved~~ 1 0 0 = Type E PSE 0 1 1 = Type D PSE 0 1 0 = Type C PSE 0 0 1 = Type B PSE 0 0 0 = Type A PSE	RO
…			

[a]RO = Read Only, LH = Latching High

45.2.9.2.7 PSE Type (13.1.9:7)

Change 45.2.9.2.7 (as modified by IEEE Std 802.3cg-2019) as follows:

Bits 13.1.9:7 report the PSE Type of the PSE as specified in 104.4.1. When read as 000, bits 13.1.9:7 indicate a Type A PSE; when read as 001, a Type B PSE is indicated; when read as 010, a Type C PSE is indicated; when read as 011, a Type D PSE is indicated; ~~and~~ when read as 100, a Type E PSE is indicated; and when read as 101, a Type F PSE is indicated. Values of ~~101 and~~ 11x are reserved.

45.2.9.3 PoDL PSE Status 2 register (Register 13.2)

Change the row for bits 13.2.2:0 in Table 45–341 (as modified by IEEE Std 802.3cg-2019) as follows (unchanged rows not shown):

Table 45–341—PoDL PSE Status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
13.2.2:0	PD Type	2 1 0 1 1 1 = Unknown 1 1 0 = Reserved 1 0 1 = Type F PD~~Reserved~~ 1 0 0 = Type E PD 0 1 1 = Type D PD 0 1 0 = Type C PD 0 0 1 = Type B PD 0 0 0 = Type A PD	RO

[a]RO = Read Only, LH = Latching High

45.2.9.3.2 PD Type (13.2.2:0)

Change 45.2.9.3.2 (as modified by IEEE Std 802.3cg-2019) as follows:

Bits 13.2.2:0 report a value of 111 until a valid classification has taken place, or if no PD is present. A value of 111 indicates that the PSE has not performed classification and therefore cannot indicate the proper value for the PD Type. Once a valid classification has occurred, the value of these bits reflect the PD Type of an attached PD as specified in 104.5.1. When read as 000, bits 13.2.2:0 indicate a Type A PD; when read as 001, a Type B PD is indicated; when read as 010, a Type C PD is indicated; when read as 011, a Type D PD is indicated; ~~and~~ when read as 100, a Type E PD is indicated; and when read as 101, a Type F PD is indicated. A v~~V~~alue~~s~~ of ~~101 and~~ 110 is~~are~~ reserved.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[3]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface.

45.5.3.3 PMA/PMD management functions

Insert PICS items MM204 through MM229 after MM203 (as inserted by IEEE Std 802.3cg-2019) in the table in 45.5.3.3 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MM204	Setting bit 1.2309.15 sets all MultiGBASE-T1 PMA/PMD registers to their default states.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM205	The MultiGBASE-T1 PMA/PMD returns a value of one in bit 1.2309.15 when a reset is in progress.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM206	The MultiGBASE-T1 PMA/PMD returns a value of zero in bit 1.2309.15 when a reset is complete.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM207	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2309.15.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM208	During a reset, the MultiGBASE-T1 PMA/PMD responds to reads from register bits 1.2309.15, 1.8.15:14, and 1.0.15.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM209	During a reset, all MultiGBASE-T1 PMA/PMD register bits are ignored.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM210	Setting or clearing either bit 1.2309.15 or 1.0.15 sets or clears the other bit.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM211	Setting either bit 1.2309.15 or 1.0.15 resets the MultiGBASE-T1 PMA/PMD.	45.2.1.192.1		PMA:M	Yes [ ] N/A [ ]
MM212	When bit 1.2309.14 is set to a one, the PMA disables output on the transmit path.	45.2.1.192.2		PMA:M	Yes [ ] N/A [ ]
MM213	When bit 1.2309.14 is zero, the PMA enables output on the transmit path.	45.2.1.192.2		PMA:M	Yes [ ] N/A [ ]
MM214	Setting or clearing either bit 1.2309.14 or 1.0.14 sets or clears the other bit.	45.2.1.192.2		PMA:M	Yes [ ] N/A [ ]
MM215	Setting either bit 1.2309.14 or 1.0.14 disables the MultiGBASE-T1 transmit path.	45.2.1.192.2		PMA:M	Yes [ ] N/A [ ]

[3] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
MM216	While in low-power mode, the device, at a minimum, responds to management transactions necessary to exit the low-power mode.	45.2.1.192.3		PMA:M	Yes [ ] N/A [ ]
MM217	Setting or clearing either bit 1.2309.11 or 1.0.11 sets or clears the other bit.	45.2.1.192.3		PMA:M	Yes [ ] N/A [ ]
MM218	Setting either bit 1.2309.11 or 1.0.11 puts the MultiGBASE-T1 PMA/PMD in low-power mode.	45.2.1.192.3		PMA:M	Yes [ ] N/A [ ]
MM219	A MultiGBASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2310.1.	45.2.1.193.7		PMA:M	Yes [ ] N/A [ ]
MM220	The receive fault bit (1.2310.1) is implemented with latching high behavior.	45.2.1.193.7		PMA:M	Yes [ ] N/A [ ]
MM221	The link status bit (1.2310.0) is implemented with latching low behavior.	45.2.1.193.8		PMA:M	Yes [ ] N/A [ ]
MM222	When bit 1.2311.5 is set to a one, the PHY uses 1.23.11.3:2 for the value of PrecodeSel.	45.2.1.194.2		PMA:M	Yes [ ] N/A [ ]
MM223	When bit 1.2311.5 is set to a zero, the PHY controls the value of PrecodeSel.	45.2.1.194.2		PMA:M	Yes [ ] N/A [ ]
MM224	Advertisement of support for MultiGBASE-T1 OAM.	45.2.1.194.5	Support is advertised if bit 1.2311.1 is set to one, and not advertised if bit 1.2311.1 is set to zero.	PMA:M	Yes [ ] N/A [ ]
MM225	Advertisement of support for MultiGBASE-T1 EEE.	45.2.1.194.6	Support is advertised if bit 1.2311.0 is set to one, and not advertised if bit 1.2311.0 is set to zero.	PMA:M	Yes [ ] N/A [ ]
MM226	OAM capability is enabled only when both the local PHY and its link partner are advertising OAM capability.	45.2.1.195.4		PMA:M	Yes [ ] N/A [ ]
MM227	EEE capability is enabled only when both the local PHY and its link partner are advertising EEE capability.	45.2.1.195.5		PMA:M	Yes [ ] N/A [ ]
MM228	When bit 1.2313.11 is set to one, the local transmitter's precoder shall be controlled by the value of bits 1.2313.10:9, and the precoder requested by the link partner in PrecodeSel shall be ignored.	45.2.1.196.2		PMA:M	Yes [ ] N/A [ ]
MM229	When bit 1.2313.11 is set to zero, the transmitter shall ignore bits 1.2313.10:9, and the precoder is set according to the value of PrecodeSel.	45.2.1.196.2		PMA:M	Yes [ ] N/A [ ]

45.5.3.7 PCS management functions

Change the rows for items RM127 and RM134 in the table in 45.5.3.7 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
RM127	The state machine assigns a value alternating between 0 and 1 to associate with the 8 octet OAM message transmitted by the ~~1000~~BASE-T1 PHY.	45.2.3.72.2		PCS:M	Yes [ ] N/A [ ]
…					
RM134	~~Register 3.2313 is cleared~~ Bit 3.2313.15 self-clears when register 3.2317 is read.	45.2.3.74.1		PCS:M	Yes [ ] N/A [ ]
…					

Insert PICS items RM193 through RM213 after item RM192 (inserted by IEEE Std 802.3cg-2019) in the table in 45.5.3.7 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
RM193	Setting bit 3.2322.15 sets all MultiGBASE-T1 PCS registers to their default states.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM194	Bit 3.2322.15 is self-clearing, and the MultiGBASE-T1 PCS returns a value of one in bit 3.2322.15 when a reset is in progress.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM195	Otherwise, bit 3.2322.15 returns a value of zero.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM196	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2322.15.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM197	During a reset, the MultiGBASE-T1 PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2322.15.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM198	All other register bits are ignored during a reset.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM199	Setting or clearing either bit 3.2322.15 or 3.0.15 sets or clears the other bit.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM200	Setting either bit 3.2322.15 or 3.0.15 resets the MultiGBASE-T1 PCS.	45.2.3.78.1		PCS:M	Yes [ ] N/A [ ]
RM201	The MultiGBASE-T1 PCS is placed in a loopback mode of operation when bit 3.2322.14 is set to a one.	45.2.3.78.2		PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM202	When bit 3.2322.14 is set to a one, the MultiGBASE-T1 PCS accepts data on the transmit path and returns it on the receive path.	45.2.3.78.2		PCS:M	Yes [ ] N/A [ ]
RM203	Setting or clearing either bit 3.2322.14 or 3.0.14 sets or clears the other bit.	45.2.3.78.2		PCS:M	Yes [ ] N/A [ ]
RM204	Setting either bit 3.2322.14 or 3.0.14 enables loopback.	45.2.3.78.2		PCS:M	Yes [ ] N/A [ ]
RM205	All bits in the MultiGBASE_T1 PCS status 1 register are read only; a write to the MultiGBASE-T1 PCS status 1 register has no effect.	45.2.3.79		PCS:M	Yes [ ] N/A [ ]
RM206	Bit 3.2323.11 is implemented with latching high behavior.	45.2.3.79.1		PCS:M	Yes [ ] N/A [ ]
RM207	Bit 3.2323.10 is implemented with latching high behavior.	45.2.3.79.2		PCS:M	Yes [ ] N/A [ ]
RM208	Bit 3.2323.2 is implemented with latching low behavior.	45.2.3.79.6		PCS:M	Yes [ ] N/A [ ]
RM209	All bits in the MultiGBASE_T1 PCS status 2 register are read only; a write to the the MultiGBASE-T1 PCS status 2 register has no effect.	45.2.3.80		PCS:M	Yes [ ] N/A [ ]
RM210	Bit 3.2324.7 is implemented with latching high behavior.	45.2.3.80.4		PCS:M	Yes [ ] N/A [ ]
RM211	Bit 3.2324.6 is implemented with latching low behavior.	45.2.3.80.5		PCS:M	Yes [ ] N/A [ ]
RM212	Bits 3.2324.5:0 are reset to all zeros when the MultiGBASE-T1 PCS 2 register is read by management function or upon execution of the MultiGBASE-T1 reset.	45.2.3.80.6		PCS:M	Yes [ ] N/A [ ]
RM213	Bits 3.2324.5:0 are held at all ones in case of overflow.	45.2.3.80.6		PCS:M	Yes [ ] N/A [ ]

Delete the rows for RM125, RM126, RM129, RM135, and RM136 in the table in 45.5.3.7 and renumber all of the items in the table accordingly (RM1 through RM208).

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.4 PHY types optionally supporting EEE

Insert a row for 2.5GBASE-T1 after 2.5GBASE-KX (as inserted by IEEE Std 802.3cb-2018), insert a row for 5GBASE-T1 after 5GBASE-KR (as inserted by IEEE Std 802.3cb-2018), and insert a row for 10GBASE-T1 after 10GBASE-KR in Table 78–1 as follows (unchanged rows not shown):

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
…	
2.5GBASE-T1	149
…	
5GBASE-T1	149
…	
10GBASE-T1	149
…	

78.2 LPI mode timing parameters description

Insert a row for 2.5GBASE-T1 after 2.5GBASE-KX (as inserted by IEEE Std 802.3cb-2018), insert a row for 5GBASE-T1 after 5GBASE-KR (as inserted by IEEE Std 802.3cb-2018), and insert a row for 10GBASE-T1 after 10GBASE-KR in Table 78–2 as follows (unchanged rows not shown):

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY or interface type	T_s (μs)		T_q (μs)		T_r (μs)	
	Min	Max	Min	Max	Min	Max
…						
2.5GBASE-T1	10.24	10.24	121.6	121.6	1.28	1.28
…						
5GBASE-T1	5.12	5.12	60.8	60.8	0.64	0.64
…						
10GBASE-T1	2.56	2.56	30.4	30.4	0.32	0.32
…						

78.3 Capabilities Negotiation

Insert the following sentence between sentences 5 and 6 of the first paragraph of 78.3 as follows:

The EEE capability for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 shall be advertised during link training according to 149.4.2.4.10.

Change the last sentence of the second paragraph of 78.3 as follows:

The same applies to 2.5GBASE-T, 2.5GBASE-T1, 5GBASE-T, 5GBASE-T1, 10GBASE-T1, 25GBASE-T, and 40GBASE-T except the EEE capabilities are exchanged and resolved during link training instead of during Auto-Negotiation.

78.5 Communication link access latency

Insert a 10th paragraph in 78.5 as follows:

Case-1 of the PHY in the MultiGBASE-T1 set applies when the PHY is requested to transmit the alert signal before transmission of the sleep signal to the link partner is complete. Case-2 of the PHY in the MultiGBASE-T1 set applies when the PHY is requested to transmit the wake signal after transmission of the sleep signal to the link partner is complete and if the PHY has not indicated LOCAL FAULT at any time during the previous 10 ms. Case-3 of the PHY in the MultiGBASE-T1 set is the same as Case-1 when Slow Wake is active. Case-4 of the PHY in the MultiGBASE-T1 set is the same as Case-2 when Slow Wake is active.

Insert a row for 2.5GBASE-T1 after 2.5GBASE-KX (as inserted by IEEE Std 802.3cb-2018), insert a row for 5GBASE-T1 after 5GBASE-KR (as inserted by IEEE Std 802.3cb-2018), and insert a row for 10GBASE-T1 after 10GBASE-KR in Table 78–4 as follows (unchanged rows not shown):

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
…						
2.5GBASE-T1	Case-1	35.84	35.84	25.6	0	10.24
	Case-2	25.6	25.6	15.36	0	10.24
	Case-3	148.48	148.48	138.24	0	10.24
	Case-4	138.24	138.24	128	0	10.24
…						
5GBASE-T1	Case-1	17.92	17.92	12.8	0	5.12
	Case-2	12.8	12.8	7.68	0	5.12
	Case-3	74.24	74.24	69.12	0	5.12
	Case-4	69.12	69.12	64	0	5.12
…						

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces *(continued)*

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
10GBASE-T1	Case-1	8.96	8.96	6.4	0	2.56
	Case-2	6.4	6.4	3.84	0	2.56
	Case-3	37.12	37.12	34.56	0	2.56
	Case-4	34.56	34.56	32	0	2.56
…						

97. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1

97.3 Physical Coding Sublayer (PCS)

Change the titles of 97.3.8 and 97.3.8.3 as follows:

97.3.8 ~~1000~~BASE-T1 Operations, Administration, and Maintenance (OAM)

97.3.8.3 State diagram variable to ~~1000~~BASE-T1 OAM register mapping

Change Table 97–6 in 97.3.8.3 as follows:

Table 97–6—State Variables to ~~1000~~BASE-T1 OAM Register Mapping

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
~~1000~~BASE-T1 OAM Message Valid	~~1000~~BASE-T1 OAM transmit register	3.2308.15	mr_tx_valid
Toggle Value	~~1000~~BASE-T1 OAM transmit register	3.2308.14	mr_tx_toggle
~~1000~~BASE-T1 OAM Message Received	~~1000~~BASE-T1 OAM transmit register	3.2308.13	mr_tx_received
Received Message Toggle Value	~~1000~~BASE-T1 OAM transmit register	3.2308.12	mr_tx_received_toggle
Message Number	~~1000~~BASE-T1 OAM transmit register	3.2308.11:8	mr_tx_message_num[3:0]
Ping Received	~~1000~~BASE-T1 OAM transmit register	3.2308.3	mr_rx_ping
Ping Transmit	~~1000~~BASE-T1 OAM transmit register	3.2308.2	mr_tx_ping
Local SNR	~~1000~~BASE-T1 OAM transmit register	3.2308.1:0	mr_tx_SNR[1:0]
~~1000~~BASE-T1 OAM Message 0	~~1000~~BASE-T1 OAM message register	3.2309.7:0	mr_tx_message[7:0]
~~1000~~BASE-T1 OAM Message 1	~~1000~~BASE-T1 OAM message register	3.2309.15:8	mr_tx_message[15:8]
~~1000~~BASE-T1 OAM Message 2	~~1000~~BASE-T1 OAM message register	3.2310.7:0	mr_tx_message[23:16]
~~1000~~BASE-T1 OAM Message 3	~~1000~~BASE-T1 OAM message register	3.2310.15:8	mr_tx_message[31:24]
~~1000~~BASE-T1 OAM Message 4	~~1000~~BASE-T1 OAM message register	3.2311.7:0	mr_tx_message[39:32]
~~1000~~BASE-T1 OAM Message 5	~~1000~~BASE-T1 OAM message register	3.2311.15:8	mr_tx_message[47:40]

Table 97–6—State Variables to ~~1000~~BASE-T1 OAM Register Mapping *(continued)*

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
~~1000~~BASE-T1 OAM Message 6	~~1000~~BASE-T1 OAM message register	3.2312.7:0	mr_tx_message[55:48]
~~1000~~BASE-T1 OAM Message 7	~~1000~~BASE-T1 OAM message register	3.2312.15:8	mr_tx_message[63:56]
Link Partner ~~1000~~BASE-T1 OAM Message Valid	~~1000~~BASE-T1 OAM receive register	3.2313.15	mr_rx_lp_valid
Link Partner Toggle Value	~~1000~~BASE-T1 OAM receive register	3.2313.14	mr_rx_lp_toggle
Link Partner Message Number	~~1000~~BASE-T1 OAM receive register	3.2313.11:8	mr_rx_lp_message_-num[3:0]
Link Partner SNR	~~1000~~BASE-T1 OAM receive register	3.2313.1:0	mr_rx_lp_SNR[1:0]
Link Partner ~~1000~~BASE-T1 OAM Message 0	Link partner ~~1000~~BASE-T1 OAM message register	3.2314.7:0	mr_rx_lp_message[7:0]
Link Partner ~~1000~~BASE-T1 OAM Message 1	Link partner ~~1000~~BASE-T1 OAM message register	3.2314.15:8	mr_rx_lp_message[15:8]
Link Partner ~~1000~~BASE-T1 OAM Message 2	Link partner ~~1000~~BASE-T1 OAM message register	3.2315.7:0	mr_rx_lp_message[23:16]
Link Partner ~~1000~~BASE-T1 OAM Message 3	Link partner ~~1000~~BASE-T1 OAM message register	3.2315.15:8	mr_rx_lp_message[31:24]
Link Partner ~~1000~~BASE-T1 OAM Message 4	Link partner ~~1000~~BASE-T1 OAM message register	3.2316.7:0	mr_rx_lp_message[39:32]
Link Partner ~~1000~~BASE-T1 OAM Message 5	Link partner ~~1000~~BASE-T1 OAM message register	3.2316.15:8	mr_rx_lp_message[47:40]
Link Partner ~~1000~~BASE-T1 OAM Message 6	Link partner ~~1000~~BASE-T1 OAM message register	3.2317.7:0	mr_rx_lp_message[55:48]
Link Partner ~~1000~~BASE-T1 OAM Message 7	Link partner ~~1000~~BASE-T1 OAM message register	3.2317.15:8	mr_rx_lp_message[63:56]

98. Auto-Negotiation for single differential-pair media

98.5 Detailed functions and state diagrams

98.5.1 State diagram variables

Insert the following new entries at the end of the dashed list in 98.5.1 after the entry for 1GigT1 as follows:

— 2.5GigT1; represents that the 2.5GBASE-T1 PMA is the signal source.
— 5GigT1; represents that the 5GBASE-T1 PMA is the signal source.
— 10GigT1; represents that the 10GBASE-T1 PMA is the signal source.

104. Power over Data Lines (PoDL) of Single-Pair Ethernet

104.1 Overview

104.1.3 PoDL system types

Insert the following sentence at the end of the second paragraph of 104.1.3 (as modified by IEEE Std 802.3cg-2019) as follows:

A Type F PSE and Type F PD are compatible with 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs.

104.4 Power Sourcing Equipment (PSE)

104.4.1 PSE types

Change 104.4.1 (as modified by IEEE Std 802.3cg-2019) as follows:

For PoDL systems there are multiple types of PSEs—Type A, Type B, Type C, Type D, ~~and~~ Type E, and Type F consistent with 104.1.3.

104.4.6 PSE output requirements

Change item 3, item 4a, and item 4b in Table 104–4 (as modified by IEEE Std 802.3cg-2019) as follows (unchanged rows not shown):

Table 104–4—PSE output requirements

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
…								
3	Output slew rate dV/dt		V/ms	—	22	All	A, C	See 104.4.6.3
				—	2	All	E	See 104.4.6.3
				—	40	All	A, C, E	During inrush only
				—	200	All	B, F	See 104.4.6.3
…								
4a	1 kHz < *f* < 10 MHz		V_{p-p}	—	0.1	All	~~All~~ A, B, C, D, E	See 104.4.6.3
					0.066		F	
4b	1 kHz < *f* < 10 MHz			—	0.01	All	~~All~~ A, B, C, D, E	
					0.0066		F	
…								

104.4.6.3 Power feeding ripple and transients

Change the fourth sentence of the second paragraph of 104.4.1 (as modified by IEEE Std 802.3cg-2019) as follows:

When measuring the ripple voltage for a Type B or Type F PSE as specified in Table 104–4 item (4a), f_1 = 318 kHz ± 1%.

Change the fourth paragraph of 104.4.1 (as modified by IEEE Std 802.3cg-2019) as follows.

When measuring the ripple voltages for a Type B or Type F PSE as specified by Table 104–4 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 318 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%.

104.5 Powered Device (PD)

104.5.1 PD types

Change 104.5.1 (as modified by IEEE Std 802.3cg-2019) as follows:

For PoDL systems there are ~~five~~six types of PDs—Type A, Type B, Type C, Type D, ~~and~~ Type E, and Type F consistent with 104.1.3.

104.5.6 PD power

Change item 3a and item 3b in Table 104–7 as follows (unchanged rows not shown):

Table 104–7—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD type	Additional information
…							
3a	1 kHz < f < 10 MHz		V_{p-p}	—	0.1	~~All~~ A, B, C, D, E	See 104.5.6.4
					0.066	F	
3b	1 kHz < f < 10 MHz			—	0.01	~~All~~ A, B, C, D, E	
					0.0066	F	
…							

104.5.6.4 PD ripple and transients

Change 104.5.6.4 (as modified by IEEE Std 802.3cg-2019) as follows (make no change to Figure 104–9):

The specifications for ripple and transients in Table 104–7 apply to the voltage or current at the PD PI generated by the PD circuitry. Ripple and transient limits are provided to preserve data integrity.

The PD DUT is connected to a power supply through a dc bias coupling network as shown in Figure 104-9. The ripple and transient specifications for a Type A or Type C PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Equation (96–12), and over the range of P_{PD}. The ripple and transient specifications for a Type B PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 97, and over the range of P_{PD}. The ripple and transient specifications for a Type E PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 146, and over the range of P_{PD}. The ripple and transient specifications for a Type F PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 149, and over the range of P_{PD}.

A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PD as specified by Table 104–7 item (3a), $f_1 = 31.8$ kHz ± 1%. When measuring the ripple voltage for a Type B or Type F PD as specified by Table 104–7 item (3a), $f_1 = 318$ kHz ± 1%. When measuring the ripple voltage for a Type E PD as specified by Table 104–7 item (3a), $f_1 = 3.18$ kHz ± 1%.

When measuring the ripple voltages for a Type A or Type C PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where $f_1 = 31.8$ kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where $f_2 = 1$ MHz ± 1%. When measuring the ripple voltages for a Type B or Type F PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where $f_1 = 318$ kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where $f_2 = 10$ MHz ± 1%. When measuring the ripple voltages for a Type E PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where $f_1 = 3.18$ kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where $f_2 = 0.1$ MHz ± 1%.

104.6 Additional electrical specifications

104.6.2 Fault tolerance

Change the first sentence of the first paragraph of 104.6.2 (as modified by IEEE Std 802.3cg-2019) as follows:

The PI for Type A, Type B, ~~and~~ Type C, and Type F PSEs and PDs shall meet the fault tolerance requirements as specified in 96.8.3.

104.7 Serial communication classification protocol (SCCP)

104.7.2 Serial communication classification protocols

104.7.2.4 Read_Scratchpad function command [0xAA]

Change the row for b[15:12] in Table 104–9 (as modified by IEEE Std 802.3cg-2019) as follows (unchanged rows not shown):

Table 104–9—CLASS_TYPE_INFO Register Table

Bit(s)	Name	Description	R/W
b[15:12]	Type	15 14 13 12 1 1 1 0 = Type A 1 1 0 1 = Type B 1 0 1 1 = Type C 0 1 1 1 = Type D 1 1 0 0 = Type E 0 0 1 1 = Type F	RO
…			

104.9 Protocol implementation conformance statement (PICS) proforma for Clause 104, Power over Data Lines (PoDL) of Single-Pair Ethernet[4]

104.9.3 Major capabilities/options

Insert a row for new item *PSETF after item *PSETE and insert a row for new item *PDTF after item *PDTE in the table in 104.9.3 (as modified by IEEE Std 802.3cg-2019) as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
...					
*PSETF	Implements PSE Type F functionality	104.1.3	Provides support for requirements of Type F Power Sourcing Equipment	O	Yes [ ] No [ ]
...					
*PDTF	Implements PD Type F functionality	104.1.3	Provides support for requirements of Type F Powered Device Equipment	O	Yes [ ] No [ ]
...					

104.9.4 PICS proforma tables for Clause 104, Power over Data Lines (PoDL) of Single-Pair Ethernet

104.9.4.3 Powered Device (PD)

Insert new item PD20a after item PD20, and new item PD22a after item PD22 in the table in 104.9.4.3 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
...					
PD20a	Type F PD ripple and transients	104.5.6.4	In accordance with specifications shown in Table 104–7 for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 149, and over the range of P_{PD}	PDTF:M	Yes [ ] N/A [ ]
...					

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
PD22a	Type F PD measured ripple voltage post-processing	104.5.6.4	With transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%	PDTF:M	Yes [ ] N/A [ ]
...					

104.9.4.4 Common Electrical

Change the table in 104.9.4.4 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
COMEL1	Type A, Type B, ~~and~~ Type C, and Type F PSE and PD fault tolerance	104.6.2	The PI shall meet the fault tolerance requirements as specified in 96.8.3	~~*~~PSETA:M ~~*~~PSETB:M ~~*~~PSETC:M PSETF:M ~~*~~PDTA:M ~~*~~PDTB:M ~~*~~PDTC:M PDTF:M	Yes [ ] N/A [ ]

125. Introduction to 2.5 Gb/s and 5 Gb/s networks

125.1 Overview

125.1.2 Relationship of 2.5 Gigabit and 5 Gigabit Ethernet to the ISO OSI reference model

Insert the following text at the end of the list after d) of 125.1.2 (as modified by IEEE Std 802.3cb-2018) as follows:

e) The MDI as specified in Clause 149 for 2.5GBASE-T1 and 5GBASE-T1 uses a single-lane data path.

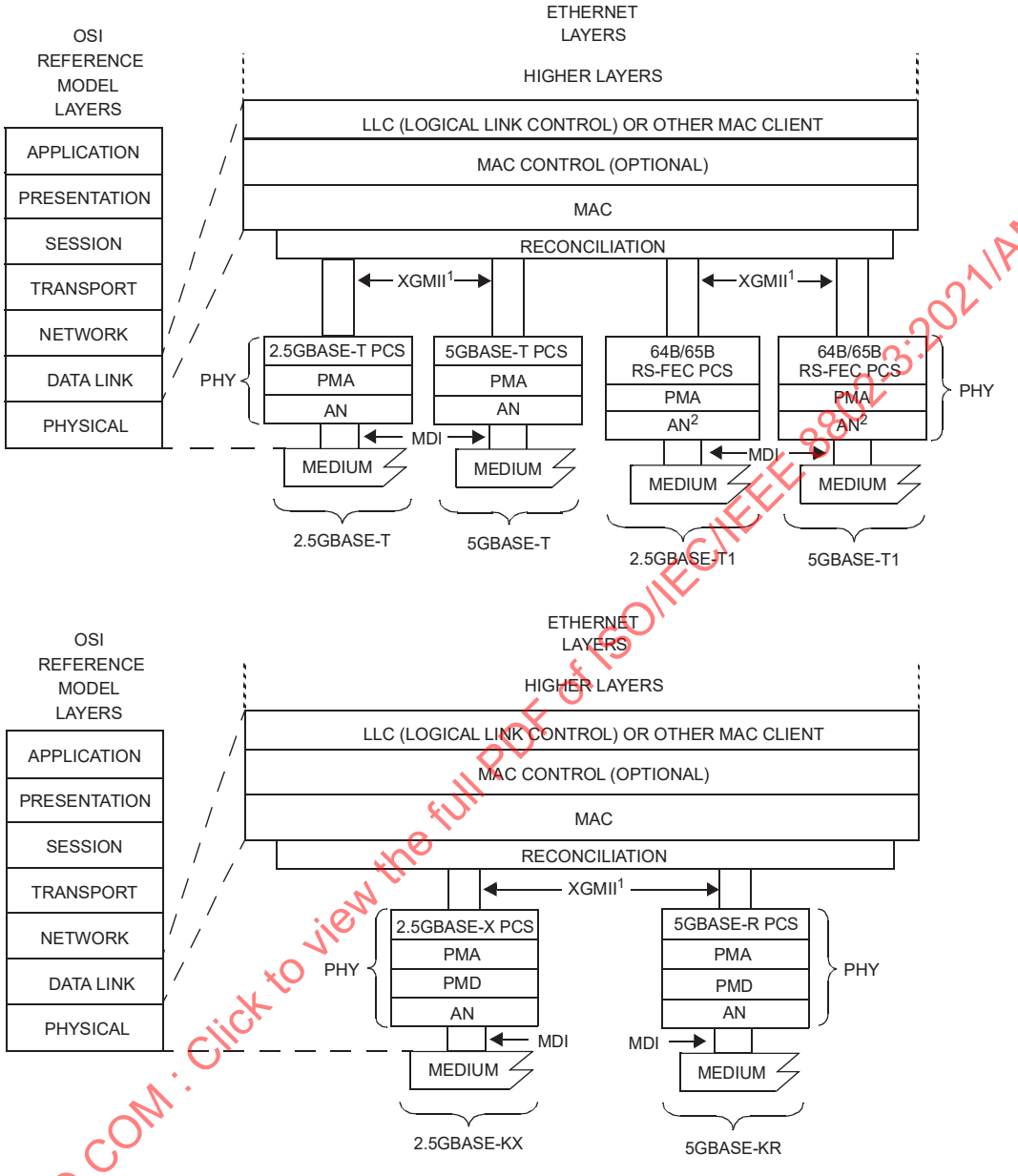
125.1.3 Nomenclature

Insert two new paragraphs at the end of 125.1.3 (as modified by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 represents Physical Layer devices using Clause 149 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for transmitting 2.5 Gb/s Ethernet over a point-to-point single balanced pair of conductors. 2.5GBASE-T1 uses Reed-Solomon FEC in its Physical Coding Sublayers mapped to PAM4 for transmission on a single balanced pair of conductors.

5GBASE-T1 represents Physical Layer devices using Clause 149 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for transmitting 5 Gb/s Ethernet over a point-to-point single balanced pair of conductors. 5GBASE-T1 uses Reed-Solomon FEC in its Physical Coding Sublayers mapped to PAM4 for transmission on a single balanced pair of conductors.

Replace Figure 125–1 (as modified by IEEE Std 802.3cb-2018) with the following figure, which adds 2.5GBASE-T1 and 5GBASE-T1.



AN = AUTO-NEGOTIATION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
NOTE 1 – XGMII IS OPTIONAL
NOTE 2 – AUTO-NEGOTIATION IS OPTIONAL

Figure 125–1—Architectural positioning of 2.5 Gigabit and 5 Gigabit Ethernet

125.1.4 Physical Layer signaling systems

Change Table 125–1 (as modified by IEEE Std 802.3cb-2018), as follows:

Table 125–1—2.5 Gb/s and 5 Gb/s PHYs

Name	Description
2.5GBASE-KX	2.5 Gb/s PHY using 2.5GBASE-X encoding over one lane of an electrical backplane (see Clause 128)
2.5GBASE-T	2.5 Gb/s PHY using LDPC encoding and PAM16 modulation over balanced twisted-pair structured cabling systems (see Clause 126)
2.5GBASE-T1	2.5 Gb/s PHY using Reed–Solomon encoding and PAM4 modulation over a single balanced pair of conductors (see Clause 149)
5GBASE-KR	5 Gb/s PHY using 2.5GBASE-X encoding over one lane of an electrical backplane (see Clause 130)
5GBASE-T	5 Gb/s PHY using LDPC encoding and PAM16 modulation over balanced twisted-pair structured cabling systems (see Clause 126)
5GBASE-T1	5 Gb/s PHY using Reed–Solomon encoding and PAM4 modulation over a single balanced pair of conductors (see Clause 149)

Change Table 125–2 (as modified by IEEE Std 802.3cb-2018) as follows:

Table 125–2—Nomenclature and clause correlation

Nomenclature	Clause[a]															
	28	46		73	78	98	126	126	127	128	128A	129	130	130A	149	
	Auto-Negotiation	RS	XGMII	Auto-Negotiation	EEE	Auto-Negotiation	2.5GBASE-T PCS/PMA	5GBASE-T PCS/PMA	2.5GBASE-X PCS/PMA	2.5GBASE-KX PMD	2.5GSEI	5GBASE-R PCS/PMA	5GBASE-KR PMD	5GSEI	2.5GBASE-T1 PCS/PMA	5GBASE-T1 PCS/PMA
2.5GBASE-KX		M	O	M	O				M	M	O					
2.5GBASE-T	M	M	O		O		M									
2.5GBASE-T1		M	O		O	O									M	
5GBASE-KR		M	O	M	O							M	M	O		
5GBASE-T	M	M	O		O			M								
5GBASE-T1		M	O		O	O										M

[a]O = Optional, M = Mandatory.

125.2 Summary of 2.5 Gigabit and 5 Gigabit Ethernet sublayers

125.2.2 Physical coding sublayer (PCS)

Insert a new paragraph at the end of 125.2.2 (as modified by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 and 5GBASE-T1 use the PCS specified in Clause 149.

125.2.3 Physical Medium Attachment sublayer (PMA)

Insert a new paragraph at the end of 125.5.3 (as modified by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 and 5GBASE-T1 use the PMA specified in Clause 149.

125.2.4 Auto-Negotiation

Insert new subclause 125.2.4.3 after 125.2.4.2 (as inserted by IEEE Std 802.3cb-2018) as follows:

125.2.4.3 Auto-Negotiation, type single differential-pair media

Auto-Negotiation (Clause 98) may be used by 2.5GBASE-T1 and 5GBASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding.

The use of Clause 98 Auto-Negotiation is optional for 2.5GBASE-T1 and 5GBASE-T1 PHYs.

125.3 Delay Constraints

Change Table 125–3 (as modified by IEEE Std 802.3cb-2018) as follows:

Table 125–3—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
2.5GBASE-KX PHY	1 024	2	409.6	See 127.5 and 128.4.
2.5GBASE-T PHY	12 800	25	~~5 120~~ 5120	Does not include delay of cable medium. See 126.11.
2.5GBASE-T1 PHY	10 240	20	4096	See 149.10.
5GBASE-KR PMD	1 024	1	102.4	See 130.4.
5GBASE-R PCS PMA	3 584	7	716.8	See 129.5.
5GBASE-T PHY	14 336	28	~~2 867.2~~ 2867.2	Does not include delay of cable medium. See 126.11.

Table 125–3—Sublayer delay constraints *(continued)*

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
5GBASE-T1 PHY no interleave	10 240	20	2048	See 149.10.
5GBASE-T1 PHY 2x interleave	13 824	27	2764.8	See 149.10.

[a] For 2.5GBASE-T, ~~and~~ 2.5GBASE-X, and 2.5GBASE-T1, 1 bit time (BT) is equal to 400 ps and for 5GBASE-T, ~~and~~ 5GBASE-R, and 5GBASE-T1, 1 bit time (BT) is equal to 200 ps. (See 1.4.160 for the definition of bit time.)

[b] For 2.5GBASE-T, ~~and~~ 2.5GBASE-X, and 2.5GBASE-T1, 1 pause_quantum is equal to 204.8 ns and for 5GBASE-T, ~~and~~ 5GBASE-R, and 5GBASE-T1, 1 pause_quantum is equal to 102.4 ns. (See 31B.2 for the definition of pause_quanta.)

[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

Insert new Clause 149 as follows:

149. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1

149.1 Overview

This clause defines the type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 Physical Coding Sublayer (PCS) as well as the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 Physical Medium Attachment (PMA) sublayers. Together, the corresponding PCS and PMA sublayers comprise a 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 Physical Layer (PHY). Provided in this clause are functional and electrical specifications for the type 2.5GBASE-T1 PCS and PMA, 5GBASE-T1 PCS and PMA, and 10GBASE-T1 PCS and PMA.

The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs are intended to be operated over a single balanced pair of conductors. The link segment specifications defined in 149.7 were derived from automotive requirements, but may also be used for non-automotive applications. The conductors supporting the operation of the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) allowing implementers to provide their own conductors to operate the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs as long as the normative requirements included in 149.7 are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

149.1.1 Nomenclature

The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs described in this clause represent three distinct PHY types that share the same PCS, PMA, and MDI specifications subject to frequency scaling. In order to efficiently describe the three PHYs, the nomenclature MultiGBASE-T1 is used to describe specifications that apply to the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs. Additionally, for parameters that scale with the PHY's data rate, the parameter *S* is used for scaling, see Table 149–1.

Table 149–1—Scaling parameter

PHY type	*S*
10GBASE-T1	1
5GBASE-T1	0.5
2.5GBASE-T1	0.25

149.1.2 Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 to other standards

The relationship between the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure 149–1. The PHY sublayers (shown shaded) in Figure 149–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs is defined in Clause 98. The XGMII is defined in Clause 46.

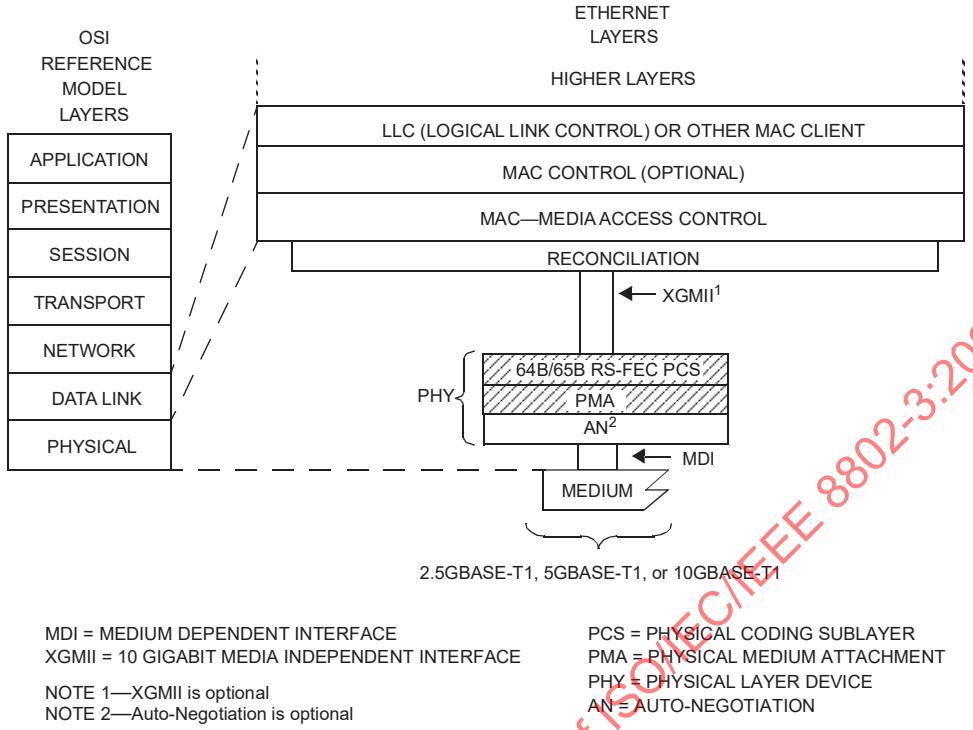


Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

149.1.3 Operation of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1

The 2.5GBASE-T1 PHY, 5GBASE-T1 PHY, and 10GBASE-T1 PHY each operate using full-duplex communications over a single balanced pair of conductors with an effective rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive environments. The PHY supports operation on an automotive link segment supporting up to four in-line connectors using a single balanced pair of conductors for up to at least 15 m. The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs utilize 4-level pulse amplitude modulation (PAM4) transmitted at 1406.25 MBd, 2812.5 MBd, and 5625 MBd rates, respectively. A 33-bit scrambler is used to improve the EMC performance. XGMII TX_D, TX_EN, and TX_ER are encoded together using 64B/65B encoding. To maintain a bit error ratio (BER) of less than or equal to 10^{-12}, the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs add 340 bits of Reed-Solomon forward error correction (RS-FEC) parity to each group of 50 64B/65B blocks. The PAM4 mapping, scrambler, RS-FEC, interleaver, and PAM4 encoder/decoder are all contained in the PCS (see 149.3).

Auto-Negotiation (Clause 98) may optionally be used by 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

A 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY shall be capable of operating as MASTER or SLAVE, per runtime configuration. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If

Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs, and the MASTER and SLAVE are synchronized by the PHY Link Synchronization function in the PHY (see 149.4.2.6).

A 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY may optionally support Energy-Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 149.4.2.4.5. The EEE capability is a mechanism by which 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHYs are able to reduce power consumption during periods of low link utilization.

The 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY may optionally support the MultiGBASE-T1 PCS-based operations, administration, and maintenance (OAM). The MultiGBASE-T1 OAM is useful for monitoring link operation by exchanging PHY link health status and messages. The MultiGBASE-T1 OAM information is exchanged between two 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHYs out of band, that is, outside of the specified 2.5 Gb/s, 5 Gb/s, or 10 Gb/s Ethernet data stream. The MultiGBASE-T1 OAM is specified in 149.3.9, and the 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY advertises its MultiGBASE-T1 OAM capability as described in 149.4.2.4.5.

The 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 1406.25 MBd for 2.5GBASE-T1, 2812.5 MBd for 5GBASE-T1, and 5625 MBd for 10GBASE-T1 over the single balanced pair of conductors. PMA functionality is described in 149.4. The MDI is specified in 149.8. Figure 149–2 shows the functional block diagram.

149.1.3.1 Physical Coding Sublayer (PCS)

The MultiGBASE-T1 PCS couples a 10 Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 50 blocks. The contents of each group are contained in a vector tx_group50x65B. Next, a 10-bit OAM field is appended to form a 3260-bit block. A number, L, of these 3260-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC (360, 326, 2^{10}) and the round–robin interleaving as described in 149.3.2.2.16. The RS-FEC output superframe consists of L × 3600 bits. The duration of the superframe is L × 320 / S ns. Finally these bits are exclusive OR'd with a degree 33 scrambler to create the MultiGBASE-T1 payload. PCS transmit functions are described in 149.3.2.2.

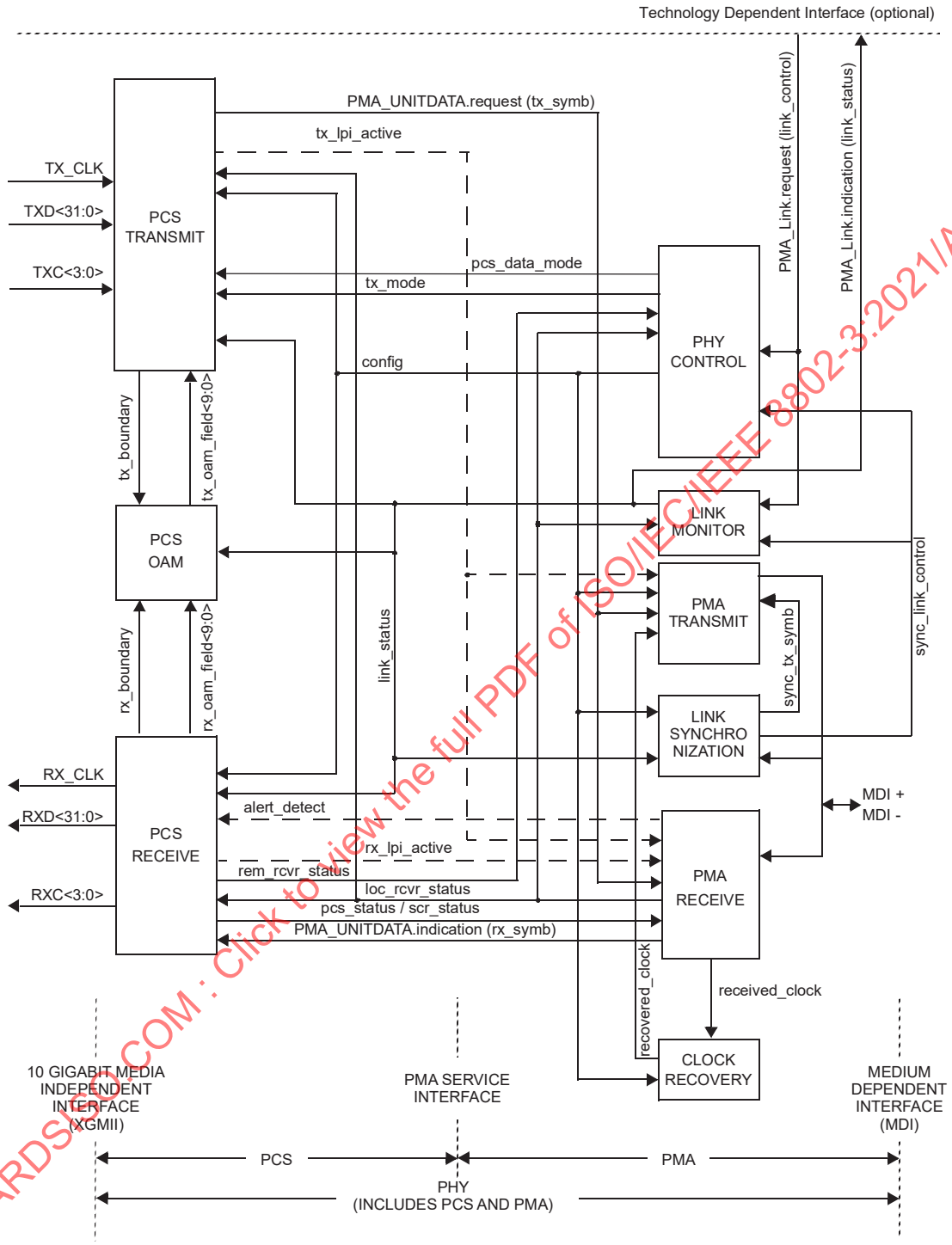
tx_group50x65B<3249:0> is defined as:

$$\text{tx\_group50x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where i = 0 to 49, j = 0 to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded_0<64:0> is the first block transmitted.

In the training mode (see 149.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges EEE and MultiGBASE-T1 OAM capabilities.

Details of the PCS functions and state diagrams are covered in 149.3. The interface to the PMA is an abstract message-passing interface specified in 149.4.



NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 149–2—Functional block diagram

149.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the single balanced pair of conductors via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at 5625 × *S* MBd. See Table 149–1 for the definition of *S*.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the startup functions required for successful MultiGBASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

PMA functions and state diagrams are specified in 149.4. The electrical parameters of the PMA, i.e., test modes and electrical specifications for the transmitter and receiver, are specified in 149.5.

149.1.3.3 EEE Capability

A MultiGBASE-T1 PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which MultiGBASE-T1 PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter the LPI mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode is not expected to cause any MAC frames to be lost or corrupted.

Support for the EEE capability is advertised in the Infofield (Octet 10 bit 6) during link startup. Transitions to and from the LPI transmit mode are controlled via XGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

When the PHY Health status received from the link partner indicates that LPI is insufficient to maintain PHY SNR, the PHY may temporarily exit LPI mode and send idles.

The PCS 64B/65B Transmit state diagram in Figure 149–16 and Figure 149–17 includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 149–18 and Figure 149–19 includes additional states for EEE. The EEE transmit state diagram is contained in the PCS Transmit function and is specified in Figure 149–20.

149.1.3.4 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled or not implemented to detect the presence of the link partner, time and control link failure, and act as the data source for the PHY control state diagram. Link Synchronization operates in a half-duplex fashion. Link Synchronization is defined in 149.4.2.6.

149.1.4 Signaling

MultiGBASE-T1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over the single balanced pair of conductors. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM4 symbols in the transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection.
i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In normal mode, the PCS generates a continuous stream of PAM4 symbols that are transmitted via the PMA at one of four voltage levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA. (See Figure 149–32.)

PHYs may also support the EEE capability as described in 149.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

149.1.5 Interfaces

All 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

149.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

149.2 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 service primitives and interfaces

MultiGBASE-T1 transfers data and control information across the following four service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in 149.2.2 and the MDI is defined in 149.8.

149.2.1 Technology Dependent Interface

MultiGBASE-T1 uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface, required in PHYs that implement Auto-Negotiation, as specified in 98.4:

PMA_LINK.request(link_control)
PMA_LINK.indication(link_status)

149.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation to enable and disable operation of the PMA, as specified in 98.4.2.

149.2.1.1.1 Semantics of the primitive

PMA_LINK.request(link_control)

The link_control parameter can take on one of two values: DISABLE, or ENABLE.

DISABLE Used by the Auto-Negotiation function to disable the PHY.

ENABLE Used by the Auto-Negotiation function to enable the PHY.

149.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

149.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 149.4.2.5, the PMA PHY Control function as defined in 149.4.2.4, and the PMA Receive function defined in 149.4.2.3.

149.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

149.2.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL No valid link established.

OK The Link Monitor function indicates that a valid MultiGBASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

149.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 149–33.

149.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

149.2.2 PMA service interface

MultiGBASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication (pcs_data_mode)

The use of these primitives is illustrated in Figure 149–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 149–3.

EEE-capable PHYs additionally support the following service primitives:

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)
PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)
PMA_ALERTDETECT.indication (alert_detect)

149.2.2.1 PMA_TXMODE.indication

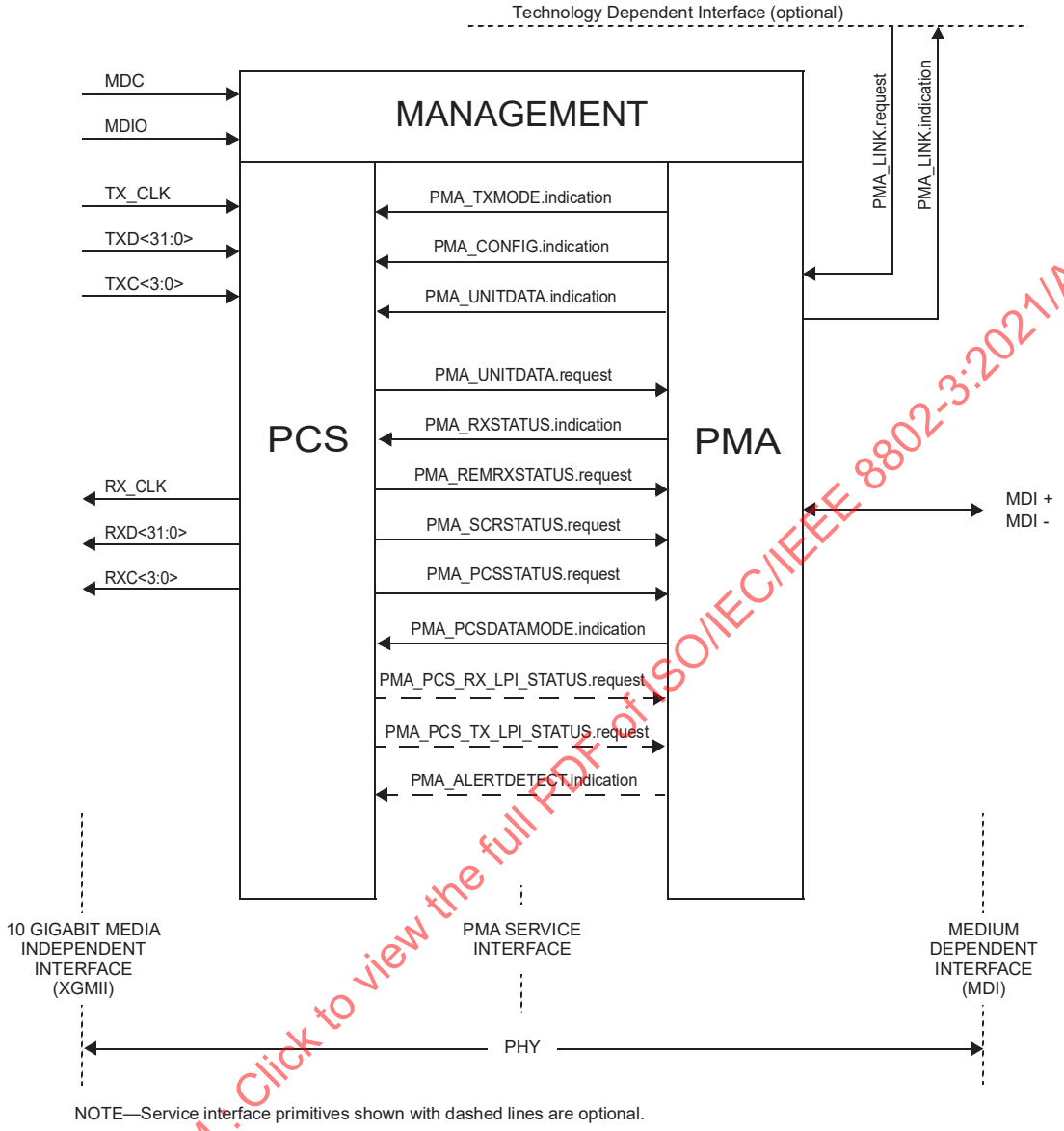
The transmitter in a MultiGBASE-T1 link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

149.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.
SEND_T	This value is continuously asserted in case transmission of sequences of symbols representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.



NOTE—Service interface primitives shown with dashed lines are optional.

Figure 149–3—2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 service interfaces

149.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

149.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 149.3.2.2.

149.2.2.2 PMA_CONFIG.indication

Each PHY in a MultiGBASE-T1 link is capable of operating as a MASTER PHY and as a SLAVE PHY. If the Auto-Negotiation process is enabled, PMA_CONFIG MASTER-SLAVE configuration is determined during Auto-Negotiation (see Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

149.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY.

149.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

149.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

149.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 149.3.2.2 to represent XGMII data and control streams or other sequences.

149.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the following values:

{–1, –1/3, +1/3, +1}	in normal operation.
0	when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the LPI transmit mode, and lpi_tx_mode is QUIET.

149.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

149.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 149.5.2.

149.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

149.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

149.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 1406.25 MHz for 2.5GBASE-T1, 2812.5 MHz for 5GBASE-T1, and 5625 MHz for 10GBASE-T1; as governed by the recovered clock.

149.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

149.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

149.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

OK The training mode descrambler has achieved synchronization.
NOT_OK The training mode descrambler is not synchronized.

149.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

149.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.4.2.3 and 149.4.2.4.

149.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

149.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in the data mode.
NOT_OK	The PCS is not operating reliably in the data mode.

149.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

149.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.4.4.1.

149.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

149.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

149.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

149.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 149–33, 149.3.2.3, 149.4.2.4, and 149.4.5.

149.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

149.2.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

149.2.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infofield messages received from the remote PHY during training.

149.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 149–32.

149.2.2.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

149.2.2.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

149.2.2.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

149.2.2.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 149.3.2.2.

149.2.2.10 PMA_PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS Receive function to indicate the status of the receive link at the local PHY. The parameter PMA_PCS_RX_LPI_STATUS.request conveys to the PCS Transmit and PMA Receive functions information regarding whether the receive function is in the LPI receive mode.

149.2.2.10.1 Semantics of the primitive

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

TRUE	The receive function is in the LPI receive mode.
FALSE	The receive function is not in the LPI receive mode.

149.2.2.10.2 When generated

The PCS generates PMA_PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in 149.3.2.3 and 149.3.7.2.2.

149.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.3.7.3.

149.2.2.11 PMA_PCS_TX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS Transmit function to indicate the status of the transmit link at the local PHY. The parameter PMA_PCS_TX_LPI_STATUS.request conveys to the PCS Transmit and PMA Receive functions information regarding whether the transmit function is in the LPI transmit mode.

149.2.2.11.1 Semantics of the primitive

PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the form:

TRUE	The transmit function is in the LPI transmit mode.
FALSE	The transmit function is not in the LPI transmit mode.

149.2.2.11.2 When generated

The PCS generates PMA_PCS_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable as described in 149.3.6 and 149.3.7.2.2.

149.2.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.3.7.3.

149.2.2.12 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is TRUE. The parameter alert_detect conveys to the PCS Receive function information regarding the detection of the LPI alert signal by the PMA Receive function. The criterion for setting the parameter alert_detect is left to the implementer.

149.2.2.12.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of two values of the form:

TRUE	The alert signal has been reliably detected at the local receiver.
FALSE	The alert signal at the local receiver has not been detected.

149.2.2.12.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

149.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.3.2.3, Figure 149–17.

149.3 Physical Coding Sublayer (PCS) functions

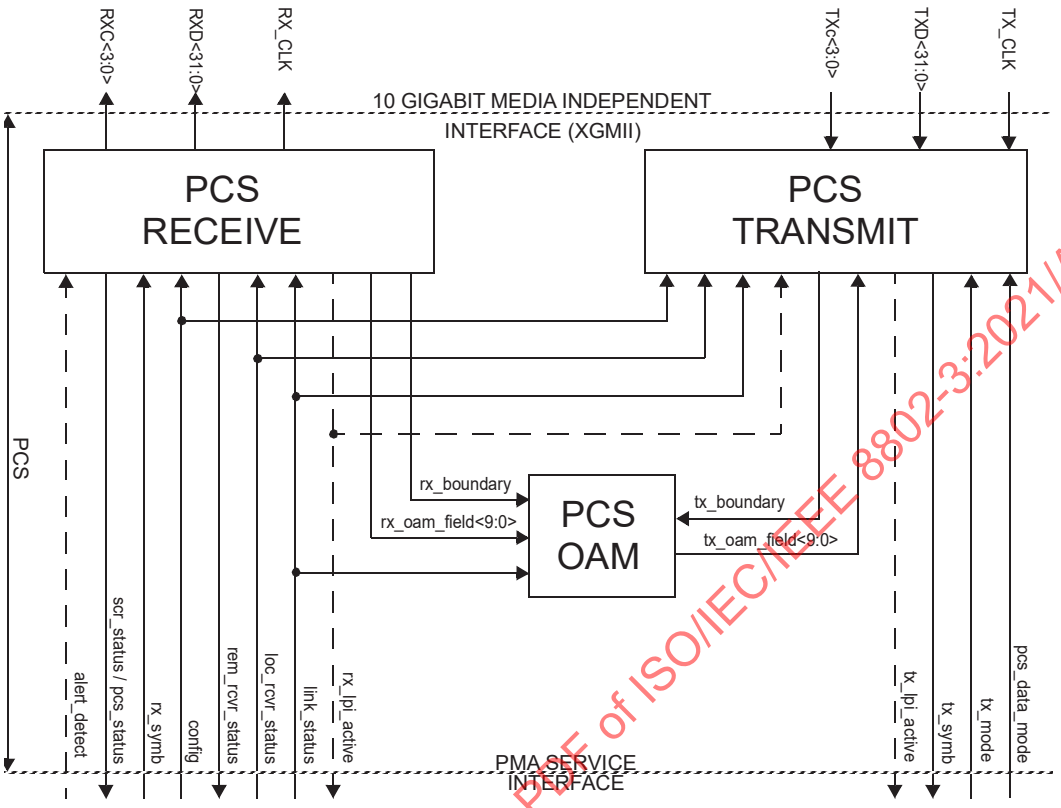
149.3.1 PCS service interface (XGMII)

The PCS service interface allows the MultiGBASE-T1 PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

149.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 149–4, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 149–4.



NOTE—rx_lpi_active and tx_lpi_active are only required for the EEE capability.

Figure 149–4—PCS reference diagram

149.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 149.3.7.2.2).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

149.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 149–16 and Figure 149–17, and to the PCS Transmit bit ordering in Figure 149–6.

Dashed rectangles in Figure 149–16 and Figure 149–17 are used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these states or transitions.

When communicating with the XGMII, the MultiGBASE-T1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take L groups of 50 65B blocks and append a 10-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC which adds L × 340 parity bits. The resulting L × 3600 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T, is 1000 / (5.625 × S) ps. See Table 149–1 for the definition of S.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 149.3.5.1 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–1, +1}.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 149.4.2.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the 50 blocks of 65B encoded bits are appended with a 10-bit OAM field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes L-interleaved (L = 1, 2, or 4) Reed-Solomon encoders to generate and append 340 parity check bits to form 3600-bit (360,326) RS-FEC frames that are interleaved into an L-interleaved RS-FEC superframe.

Each RS-FEC input superframe consists of 3260 × L bits, or 326 × L Reed-Solomon message symbols. The interleaving function is integrated with the RS-FEC encoding, applying a round-robin interleaving scheme and distributing the 10-bit Reed-Solomon message symbols into L RS-FEC encoders. After encoding, the RS-FEC frames from each encoder are recombined into one single interleaved RS-FEC superframe, which consists of 360 × L symbols, or 3600 × L bits. The bits of the RS-FEC superframe are then scrambled by the PCS using an additive scrambler, encoded in PAM4 symbols, and transferred to the PMA.

L is called the interleaving depth, and the possible choices of L are 1, 2, and 4. The interleaver settings requested in each direction of transmission may be different, and the value of L used by the transmitter is determined by the link partner and signaled during the PAM2 training mode Infofield exchange.

After reaching the normal mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the RS via the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 149.3.2.2.22.

A block diagram of the PCS Transmit functions is shown in Figure 149–5.

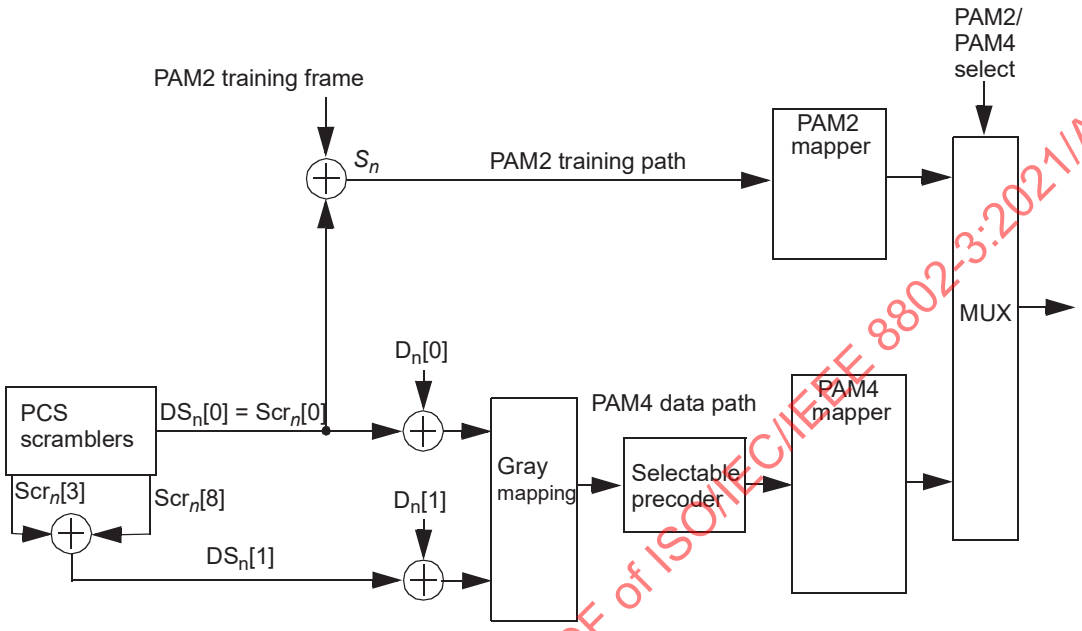


Figure 149–5—PCS Transmit function block diagram

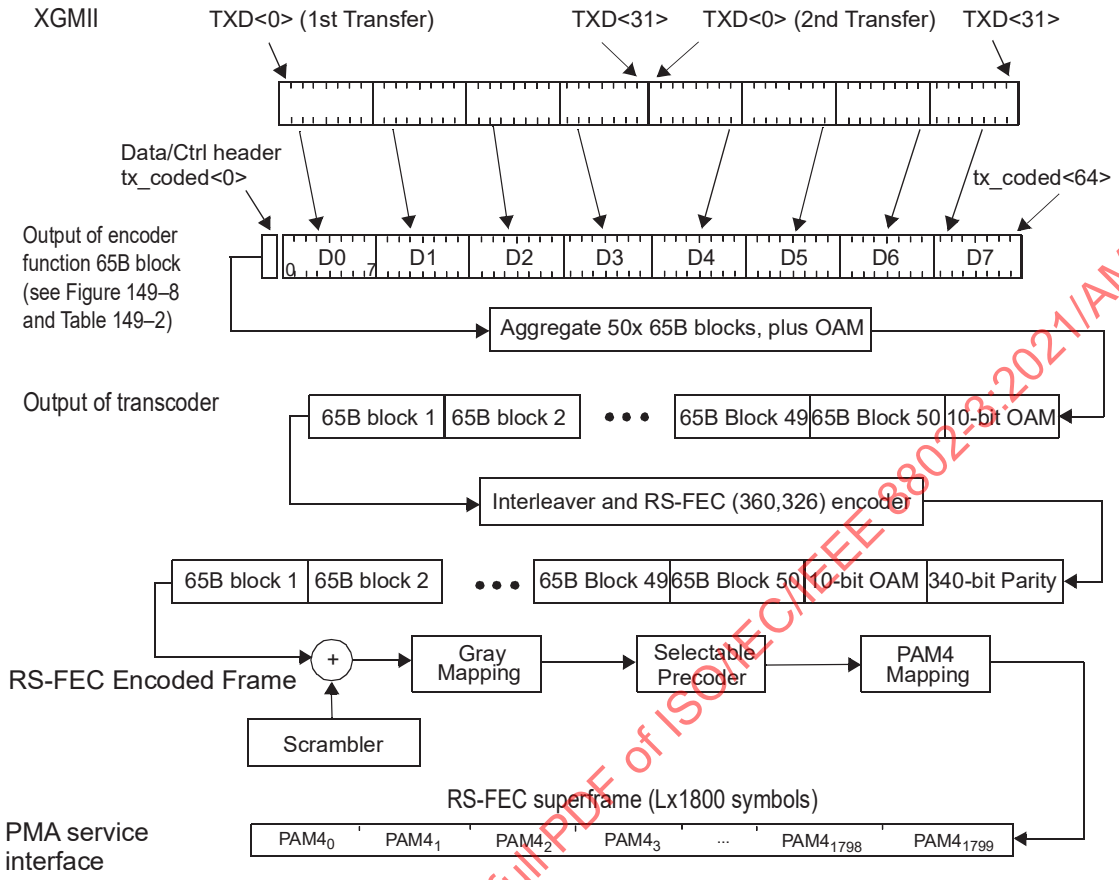
149.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. During the LPI mode, RS-FEC frame boundaries delimit sleep, wake, refresh, quiet, and alert cycles. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 149.3.2.2.2.

149.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 149–6 for transmit and Figure 149–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

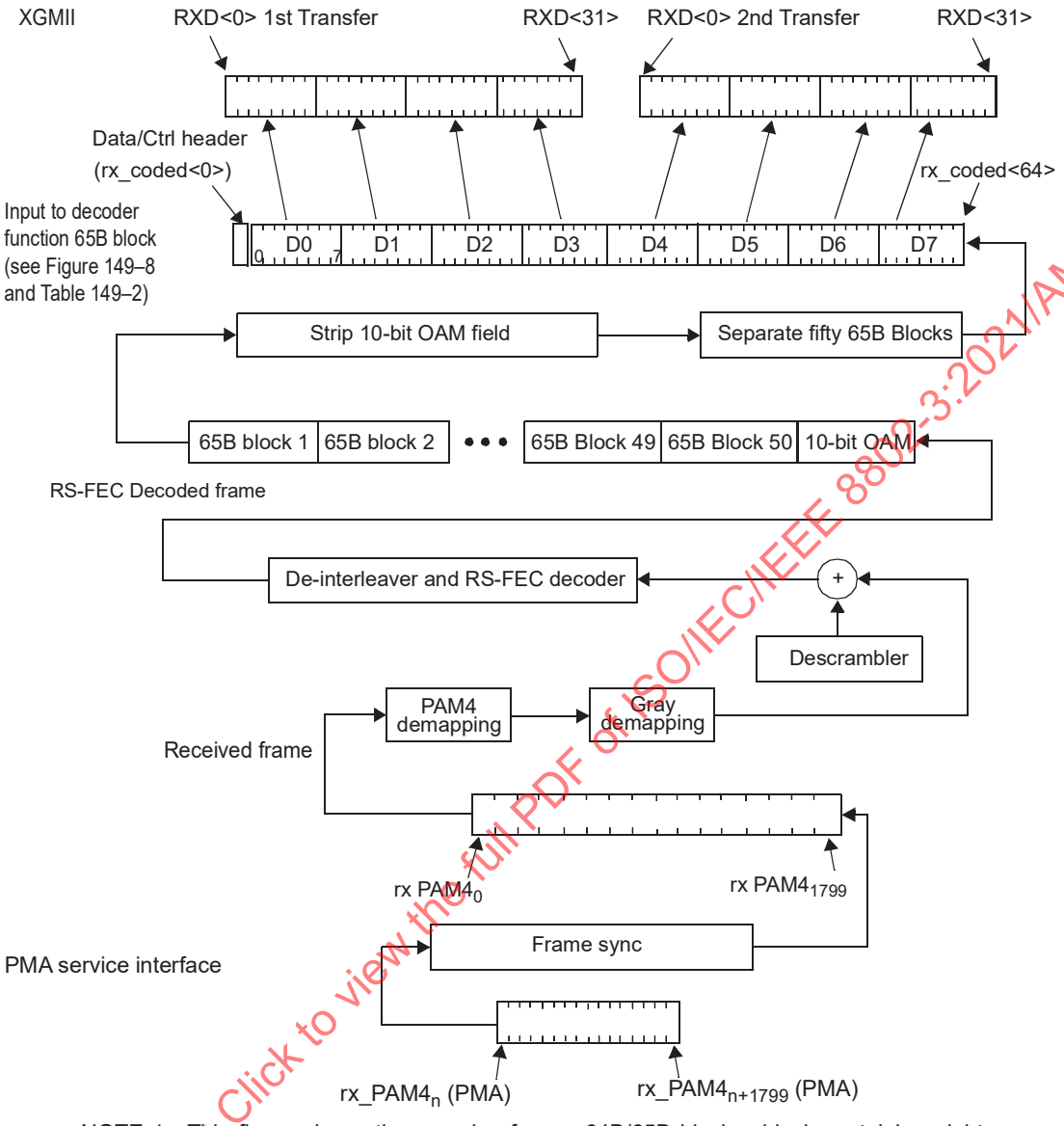
Figure 149–6—PCS Transmit bit ordering

149.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/, and /T/ are labeled C_0 to C_7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

For MultiGBASE-T1, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).



NOTE 1—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the XGMII.

NOTE 2—Figure shown for L = 1.

Figure 149–7—PCS Receive bit ordering

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<31:0> and rx_coded<31:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

149.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks for MultiGBASE-T1 is as shown in Figure 149–8. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Input Data	data ctrl header	**Block Payload**							
Bit Position: / **Data Block Format:**	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 149–8—64B/65B block formats for MultiGBASE-T1

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown prepended with '0x', and with the least significant digit on the right. For example the block type field 0x1E

is sent as 01111000 representing bits 1 through 8 of the 65-bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[5] are reserved.

149.3.2.2.5 Control codes

The same set of control characters are supported by the XGMII and the 2.5G/5G/10GBASE-T1 PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The 2.5G/5G/10GBASE-T1 PCS encodes the start and terminate control characters implicitly by the block type field. The 2.5G/5G/10GBASE-T1 PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The 2.5G/5G/10GBASE-T1 PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to 2.5G/5G/10GBASE-T1 control codes and XGMII control codes are specified in Table 149–2. All XGMII control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

149.3.2.2.6 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 149–2 for the mappings.

149.3.2.2.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

149.3.2.2.8 LPI (/LI/)

Low Power Idle (LPI) control characters (/LI/) on the XGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. PHYs that support EEE respond to the LPI XGMII control characters using the procedure outlined in 149.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of four. /LI/s may be added following Low Power Idle characters. They shall not be added while data is being received.

If EEE is not supported, then /LI/ is not a valid control character.

149.3.2.2.9 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error.

[5]The block type field values have been chosen to have a four-bit Hamming distance between them. The only unused value that maintains this Hamming distance is 0x00.

Table 149–2—Control codes for MultiGBASE-T1

Control character	Notation	XGMII control code	2.5G/5G/10G BASE-T1 control code	2.5G/5G/10G BASE-T1 O code
idle	/I/	0x07	0x00	
LPI	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5
Signal ordered set[1]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[1]Reserved for INCITS T11 Fibre Channel use.

Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

149.3.2.2.10 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

149.3.2.2.11 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered sets are not deleted for clock compensation.

149.3.2.2.12 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 149.3.7.2.4 for further information.

149.3.2.2.13 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 100 XGMII data transfers are encoded into an RS-FEC frame. It takes 1800 PMA_UNITDATA transfers to send an RS-FEC frame of data. Therefore, for MultiGBASE-T1, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 1:18, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 149–16 and Figure 149–17). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

149.3.2.2.14 RS-FEC framing and RS-FEC encoder

The resulting RS-FEC frame of 50 65B blocks, followed by the 10-bit OAM field and 340 parity bits is 3600 bits. See Figure 149–6 and 149.3.2.2.17 for details on PCS bit ordering and RS-FEC encoding.

The RS-FEC encoding takes the 3260-bit vector, consisting of tx_group50x65B, and the 10-bit OAM_field, and shall generate the 34 10-bit parity symbols (340 bits total).

149.3.2.2.15 RS-FEC superframe and round-robin interleaving

The interleaver depth L of the transmitter shall be set to the InterleaverDepth requested by the link partner during Infofield exchange, as specified in 149.4.2.4.5.

When the selected interleaving depth L = 1, there is no interleaving, and the RS-FEC superframe is the same as the RS-FEC frame.

When the selected interleaving depth L > 1, the round-robin interleaving scheme as shown in Figure 149–9 shall be applied.

2.5GBASE-T1 only supports L = 1.

5GBASE-T1 supports L = 1 and L = 2.

10GBASE-T1 supports L = 1, L = 2, and L = 4.

The PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 3260 × L bits, or 326 × L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are $m_{326 \times L-1}$, $m_{326 \times L-2}$,…,m_1, m_0. These message symbols are

distributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message symbols from the superframe; otherwise, the RS-FEC encoder operates exactly the same as specified in 149.3.2.2.17.

149.3.2.2.16 RS-FEC recombine

The L encoded RS-FEC frames are recombined into an interleaved RS-FEC superframe. The output symbols are as follows:

$m_{326 \times L-1}, m_{326 \times L-2}, \ldots, m_1, m_0, p_{1,33}, \ldots, p_{L,33}, \ldots, p_{1,0}, \ldots, p_{L,0}$, where $p_{i,r}$ is the r^{th} parity symbol of the i^{th} encoder.

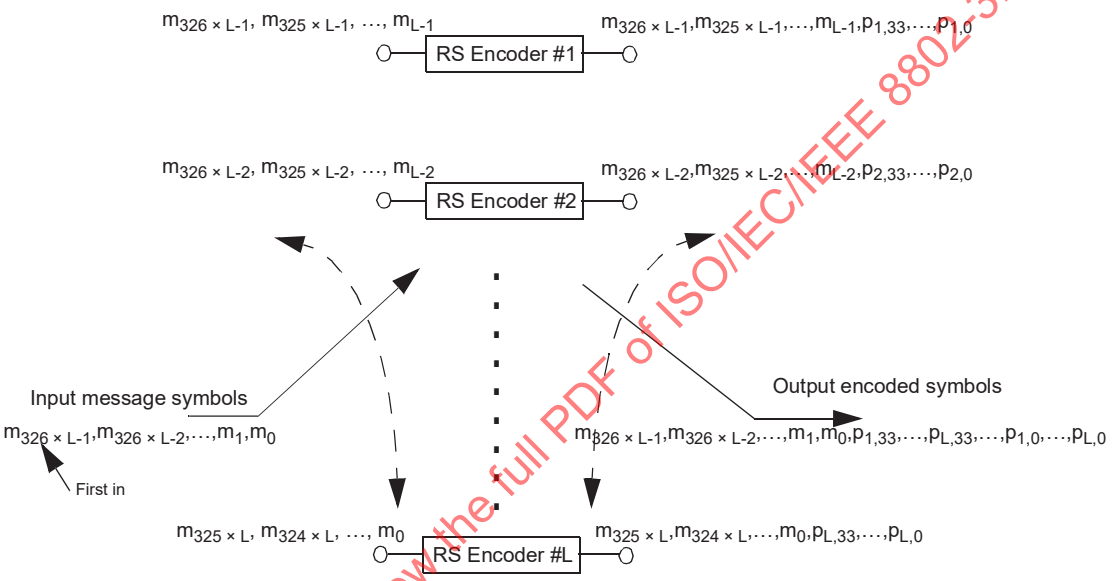


Figure 149–9—Interleaving block diagram with interleaving depth L

149.3.2.2.17 Reed-Solomon encoder

The group of 3260 bits are encoded using a Reed-Solomon encoder operating over the Galois Field GF(2^{10}) where the symbol size is 10 bits. The encoder processes 326 ten-bit RS-FEC message symbols to generate 34 ten-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 360 ten-bit RS-FEC symbols. For the purposes of this clause, the particular Reed-Solomon code is denoted as RS-FEC(360,326).

The code is based on the generating polynomial given by Equation (149–1).

$$g(x) = \prod_{j=0}^{33}(x - \alpha^j) = g_{34}x^{34} + g_{33}x^{33} + \ldots + g_4x^4 + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (149\text{–}1)$$

In Equation (149–1), α, is a primitive element of the finite field defined by the primitive polynomial $0x409 = x^{10} + x^3 + 1$.

Equation (149–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{325} to $m_{0.}$

$$m(x) = m_{325}x^{359} + m_{324}x^{358} + \ldots + m_1x^{35} + m_0x^{34} \quad (149\text{–}2)$$

Each message symbol m_i is the bit vector ($m_{i,9}$, $m_{i,8}$, ... $m_{i,1}$,$m_{i,0}$), which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<3259:0> where
$m_{i,j}$ = tx_RSmessage <(325 – i) × 10 + j>, for i = 0 to 325, and j = 0 to 9.

tx_RSmessage<3259:0> prior to RS-FEC (360,326) encoder is formed as follows:

tx_RSmessage<3249:0> = tx_group50x65B<3249:0>.
tx_RSmessage<3259:3250> = OAM_field<9:0>.

The first symbol input to the encoder is m_{325}.

Equation (149–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_{33} to $p_{0.}$

$$p(x) = p_{33}x^{33} + p_{32}x^{32} + \ldots + p_2x^2 + p_1x + p_0 \quad (149\text{–}3)$$

Each parity symbol p_i is the bit vector ($p_{i,9}$, $p_{i,8}$, ... $p_{i,1}$,$p_{i,0}$), which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 149–10. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{359} = m_{325}$ is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

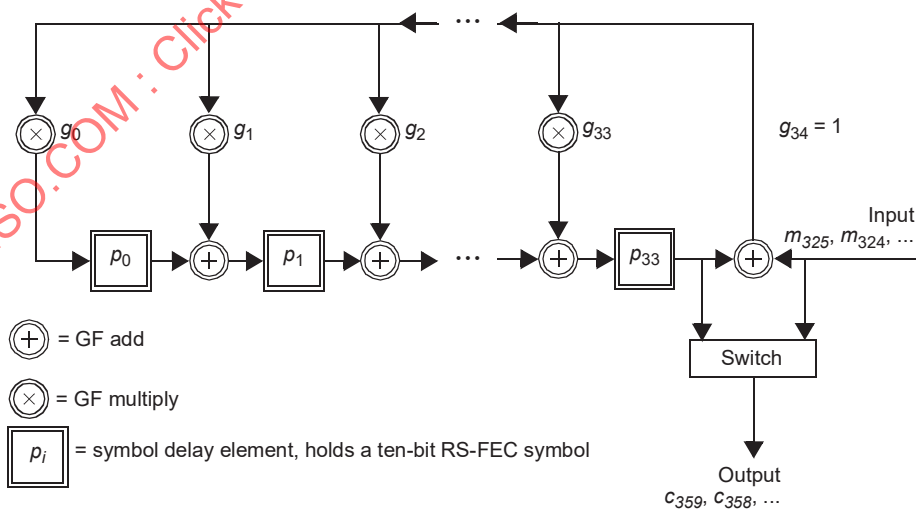


Figure 149–10—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 149–3.

Table 149–3—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(360, 326)	*i*	RS-FEC(360, 326)
0	315	18	615
1	269	19	952
2	594	20	672
3	756	21	636
4	732	22	765
5	709	23	929
6	198	24	173
7	560	25	242
8	444	26	197
9	323	27	886
10	546	28	902
11	161	29	736
12	930	30	168
13	914	31	248
14	412	32	800
15	68	33	951
16	150	34	1
17	878	—	—

149.3.2.2.18 PCS scrambler

The bits of the interleaved RS-FEC superframe are grouped into pairs, and each pair of bits, $D_n[0]$ and $D_n[1]$, where n is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the side-stream scrambler. The first (LSB) bit is $DS_n[0]$ equal to $Scr_n[0]$ defined in 149.3.4. The second (MSB) bit is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$.

$DS_n[0]$ and $DS_n[1]$ are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$ as shown in Equation (149–4).

$$A_n = DS_n[0] \oplus D_n[0]$$
$$B_n = DS_n[1] \oplus D_n[1] \quad (149–4)$$

149.3.2.2.19 Gray mapping for PAM4 encoding

For output symbols, the PCS transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where A_n is the bit arriving first, and n is an index indicating the symbol number, to Gray-coded symbols $G(n)$ with one of

four levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

For input symbols, the PCS receive process shall map Gray-coded PAM4 symbols G(n), with one of four levels, to pairs of bits, {A_n, B_n}, where A_n is considered to be the first bit as follows:

0 maps to {0, 0},
1 maps to {0, 1},
2 maps to {1, 1}, and
3 maps to {1, 0}.

149.3.2.2.20 Selectable precoder

The PCS transmit process shall precode the Gray-coded symbols as specified in this subclause.

In normal operation the value of precoder_type (see 45.2.1.196.3) shall be set to the value of PrecodeSel received from the link partner in the Infofield messages (see 149.4.2.4.5):

0 0: No precoder,
0 1: Precoder for 1 – D channel,
1 0: Precoder for 1 + D channel, and
1 1: Precoder for 1 – D^2 channel.

For each Gray-coded symbol G(n), a precoded symbol P(n) shall be determined by the following algorithm, where n is an index indicating the symbol number:

P(n) = G(n), when precoder_type = No precoder,
P(n) = (G(n) + P(n–1)) mod 4, when precoder_type = Precoder for 1 – D channel,
P(n) = (G(n) – P(n–1)) mod 4, when precoder_type = Precoder for 1 + D channel, and
P(n) = (G(n) + P(n–2)) mod 4, when precoder_type = Precoder for 1 – D^2 channel.

In normal data mode, the precoder should be initialized to the zero state when entering TX_SWITCH state of the startup sequence. In EEE mode, the precoder should be initialized to the zero state when transitioning to PAM4 encoding. When the precoder is not initialized to the zero state as described, there may be a short period of errors when entering the associated state.

149.3.2.2.21 PAM4 encoding

The PCS transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this subclause.

The PAM4 encoded symbols are denoted M(n), where:

n is an index indicating the symbol number.

Each consecutive precoder output symbol, P(n), is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output M(n).

Mapping from the precoder output symbol P(n) to a PAM4 encoded symbol M(n) is as follows:

0 maps to –1,
1 maps to –1/3,
2 maps to +1/3, and
3 maps to +1.

149.3.2.2.22 EEE capability

The optional 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low in either direction of transmission.

PHYs that support EEE shall conform to the EEE transmit state diagram, shown in Figure 149–20, within the PCS.

In the transmit direction, the transition to the LPI transmit mode begins when the PCS Transmit function detects an LPI control character in the last 64B/65B block of a Reed-Solomon frame. Following this event, the PMA transmits the sleep signal to indicate to the link partner that it is transitioning to the LPI transmit mode. The sleep signal is composed of eight Reed-Solomon frames that contain only LP_IDLE 64B/65B blocks. Once initiated, the complete sleep signal consisting of eight RS-FEC frames of LP_IDLE shall be transmitted.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 149.3.6.

After the sleep signal is transmitted, LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit function exits the LPI transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

When the PHY is not in the PCS_DATA state, the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value NORMAL and the PMA asserts SEND_N, the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive as described in 149.3.2.2.

When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N, the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH and the PMA asserts SEND_N, the PCS passes the PMA training signal to the PMA, to allow both the local and remote PHY to refresh adaptive filters and timing loops.

When the lpi_tx_mode variable takes the value ALERT, the PMA transmits the link synchronization sequence onto the MDI as provided by the link synchronization block via sync_tx_symb.

The quiet-refresh cycle is repeated until codewords other than LP_IDLE are detected at the XGMII. These codewords indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request parameter tx_symb_vector is set to the value ALERT.

After transmitting the alert signal, the PCS completes the transition from LPI mode to normal mode by sending a wake signal containing lpi_wake_time RS-FEC frames composed of IDLE 64B/65B blocks.

lpi_wake_time is a fixed parameter that is defined in Table 149–4. See Table 149–1 for the definition of *S*.

Table 149–4—LPI wake time

lpi_wake_time	*lpi_tx_wake_time when wake starts before sleep signal is complete*		*lpi_tx_wake_time when wake starts after sleep signal is complete*	
(frames)	(frames)	(μs)	(frames)	(μs)
8	28	8.96/*S*	20	6.4/*S*

149.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 149–18 and Figure 149–19, and the PCS Receive bit ordering in Figure 149–7 including compliance with the associated state variables as specified in 149.3.7.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM4 symbols are demapped and descrambling is performed.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into a 10-bit OAM field and 50 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 149–18 and Figure 149–19). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment bit every 450 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an Infofield, which is inserted in the 16th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE and subject to the timing requirements of 46.1.7. Transitions to and

from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS Receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 149.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting eight RS-FEC frames composed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS Receive function and the /LI/ character is continuously asserted at the receive XGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames, the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses RS-FEC frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 149.3.6. The quiet-refresh cycle continues until the link synchronization detect asserts alert_detect to indicate that the alert (link synchronization) sequence has been reliably detected. After the alert sequence, the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the XGMII for eight RS-Frame periods (wake duration) and then resumes normal operation.

149.3.2.3.1 Frame and block synchronization

When operating in the data mode, the receiving PCS shall form a PAM4 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM4_0 to rx_PAM4_1799 (see Figure 149–7). It obtains block lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

149.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial per Equation (149–6) and the SLAVE PHY shall employ the receiver descrambler generator polynomial per Equation (149–5).

149.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 149–2.
c) Any O code contains a value not in Table 149–2.
d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 149.3.2.2.14. If the check fails the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

149.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 149–6, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero.

When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 149–7. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 in 149.5.1.

149.3.4 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation (149–5) as transmitter side-stream scrambler generator polynomial.

$$g_M(x) = 1 + x^{13} + x^{33} \tag{149–5}$$

If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation (149–6) as transmitter side-stream scrambler generator polynomial.

$$g_S(x) = 1 + x^{20} + x^{33} \tag{149–6}$$

An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 149–11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the transition from PAM2 to PAM4.

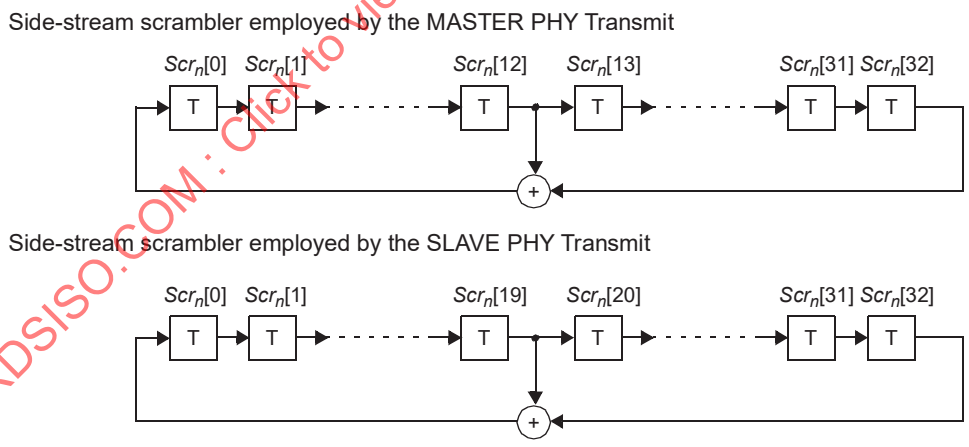


Figure 149–11—Realization of side-stream scramblers by linear feedback shift registers

149.3.5 PMA training frame

During PMA training, the training frames are embedded with indicators to establish alignment to the RS-FEC superframe comprised of 16 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners. The timing relationship among training frame, partial frame, RS-FEC frame, superframe, and partial PHY frame count (PFC24) are shown in Figure 149–12.

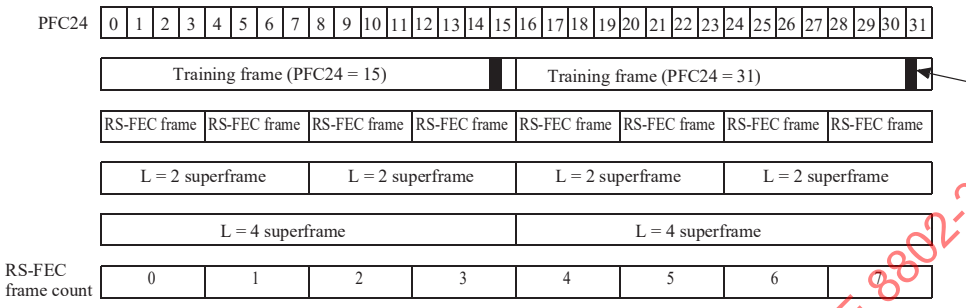


Figure 149–12—Timing relationship to PFC24

PMA training frame encoding is based on the generation, at time n, of the bit S_n. The first bit is inverted in the first 15 partial PHY frames of each RS-FEC block. The first 96 bits of the 16th partial PHY frame are XORed with the contents of the Infofield. Each partial PHY frame is 450 bits long, beginning at S_n where (n mod 450) = 0. See Equation (149–7).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 450)} & 6750 \le (n \bmod 7200) \le 6845 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 450) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad (149\text{–}7)$$

149.3.5.1 Generation of symbol T_n

The bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$.

149.3.5.2 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation (149–6) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation (149–5).

149.3.6 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode by generating the sleep signal comprised of eight RS-FEC frames composed entirely of LPI control characters, as described in 149.3.2.2.22. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode, PHYs use a repeating quiet-refresh cycle (see Figure 149–13 and Figure 149–14). The LPI timing parameters are shown in Table 149–5. The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time. The quiet period is defined in 149.3.6.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time. The refresh period is defined in 149.3.6.3. A cycle composed of one quiet period and one refresh period is known as an LPI cycle and lasts for a time lpi_qr_time.

The parameters lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the RS-FEC frame period. lpi_offset is a fixed value equal to lpi_qr_time / 2 + 4 (52 RS-FEC frame periods).

The end of LPI mode occurs at the transmission of the alert signal indicating the end of quiet-refresh cycle.

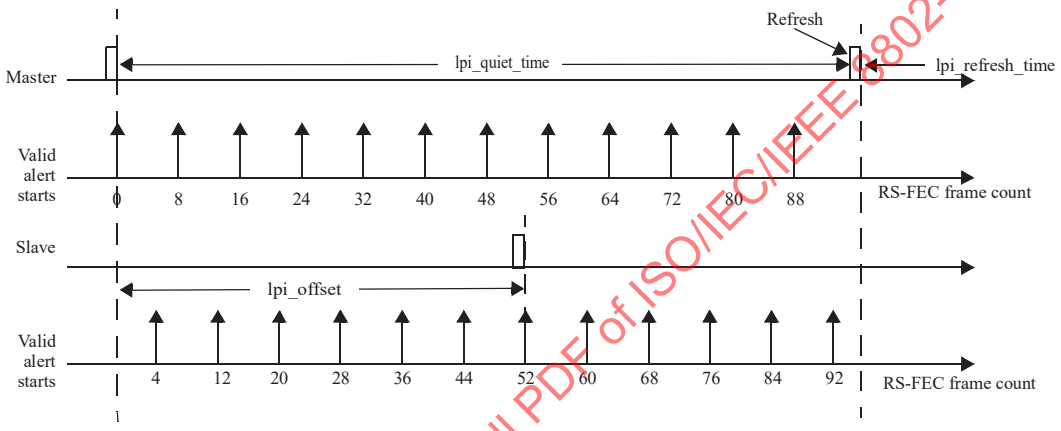


Figure 149–13—Timing periods for LPI signals when Slow Wake not active

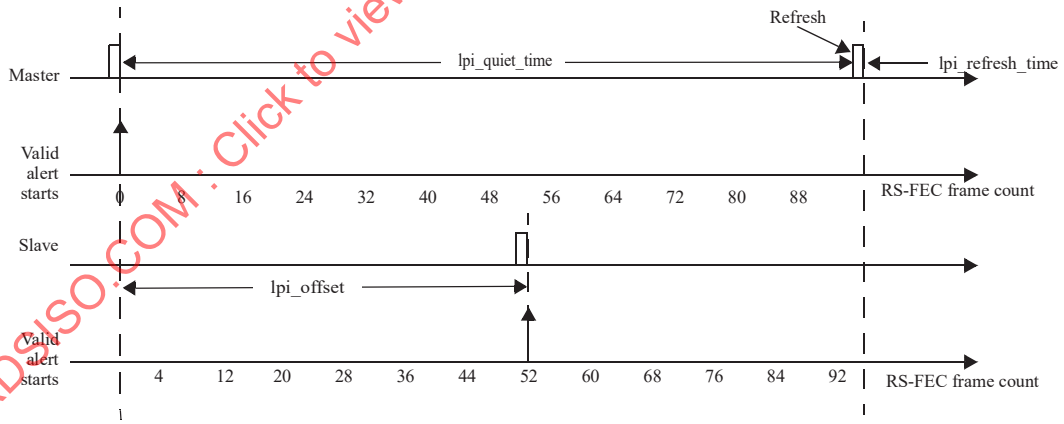


Figure 149–14—Timing periods for LPI signals when Slow Wake is active

149.3.6.1 LPI synchronization

EEE-capable PHYs shall synchronize refresh intervals during the LPI mode. A PHY in SLAVE mode is responsible for synchronizing its partial PHY frame count (PFC24) to the MASTER's PFC24 during PAM2 training. For the requirements on the SLAVE and the MASTER frame alignment, see 149.4.2.4.10.

Table 149–5—LPI timing parameters

Parameter	Number of RS-FEC frame periods
alert_length	4
alert_period	8
lpi_offset	52
lpi_qr_time	96
lpi_quiet_time	95
lpi_refresh_time	1

Refresh signaling is derived by tracking the RS-FEC frame count as shown in Figure 149–13, where:

RS-FEC frame count = floor (PFC24 / 4) mod 96.

The start of the SLAVE quiet-refresh cycle is delayed from the MASTER by lpi_offset. The MASTER and SLAVE alert windows are offset from each other and the refresh periods are close to half a cycle offset.

Following the transition to PAM4, the PCS continues with the RS-FEC frame count and uses the count to generate refresh, alert, and wake control signals for the transmit functions.

Alert, a four RS-FEC frame long sequence (alert_length), shall start at the beginning of any eighth PHY frame boundary starting at the beginning of the frame following a refresh PHY frame. This offsets the MASTER and SLAVE alert start times by alert_period/2 and provides two benefits. The first benefit is that alert transmissions do not overlap with the device's own refresh. The second benefit is that the MASTER and SLAVE alert transmissions generally do not overlap, and only overlap at the limits of tolerances. The MASTER and SLAVE shall derive the tx_refresh_active and tx_alert_start_next signals from the transmitted PHY frames as shown in Table 149–6 and Table 149–7. When Slow Wake is active, alert can be transmitted in only a single QR cycle location.

Table 149–6—Synchronization logic derived from slave signal RS-FEC frame count

Slave-side variable	Condition (where u = RS-FEC frame count)	Slow Wake
tx_refresh_active = TRUE	lpi_offset – lpi_refresh_time ≤mod(u, lpi_qr_time) < lpi_offset	0 or 1
tx_alert_start_next = TRUE	mod(u, alert_period) = alert_period/2 –1	0
tx_alert_start_next = TRUE	mod(u, lpi_qr_time) = lpi_qr_time/2 + alert_period/2 –1	1

149.3.6.2 Quiet period signaling

During the quiet period the PCS transmitter shall pass zeros to the PMA via the PMA_UNITDATA.request primitive.

Table 149–7—Synchronization logic derived from master signal RS-FEC frame count

Master-side variable	Condition (where v = RS-FEC frame count)	Slow Wake
tx_refresh_active = TRUE	mod(v, lpi_qr_time) ≥ lpi_quiet_time	0 or 1
tx_alert_start_next = TRUE	mod(v, alert_period) = alert_period –1	0
tx_alert_start_next = TRUE	mod(v, lpi_qr_time) = lpi_qr_time –1	1

149.3.6.3 Refresh period signaling

During the LPI mode the MultiGBASE-T1 PHY uses staggered, out-of-phase refresh signaling. Two-level PAM refresh symbols are generated from the T_n mapping defined in 149.3.5.1 of S_n defined in 149.3.5, with the exception that the Infofield consists of zeros. The 10-bit OAM symbol to be transmitted is XORed with the last 10 bits of the PAM2 refresh transmission.

149.3.7 Detailed functions and state diagrams

149.3.7.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

149.3.7.2 State diagram parameters

149.3.7.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

LPBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing /LI/ in all the eight character locations.

LPBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /LI/ in all the eight character locations.

IBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.

RFER_CNT_LIMIT
TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>
72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.
The Link Interruption ordered set is defined in 46.3.4.

149.3.7.2.2 Variables

rfer_test_lf
Boolean variable that is set TRUE when a new Reed-Solomon frame is available for testing and FALSE when RFER_TEST_LF state is entered. A new Reed-Solomon frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next Reed-Solomon frame.

block_lock
Boolean variable that is set TRUE when receiver acquires block delineation.

hi_rfer
Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one rfer_timer interval.

lp_low_snr
Boolean variable that is set TRUE when the link partner indicates LPI refresh is insufficient to maintain PHY SNR. It is set FALSE otherwise.

pcs_data_mode
Variable set by the PMA PHY Control function. See 149.4.4.1.

pcs_reset
Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

rf_valid
: Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

tx_coded<64:0>
: Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

The following variables are required for PHYs that support the EEE capability:

alert_detect
: Indicates that an alert signal from the link partner has been received at the MDI as indicated by PMA_ALERTDETECT.indication(alert_detect).

lpi_refresh_detect
: Set TRUE when the receiver has reliably detected refresh signaling. It is set FALSE otherwise.

lpi_tx_mode
: A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb) interface.
lpi_tx_mode controls tx_symb only when tx_mode is set to SEND_N.
The variable is set to NORMAL when (!tx_lpi_qr_active * !tx_lpi_alert_active), indicating that the PCS is in the normal mode of operation and will encode code-groups as described in Figure 149–16 and Figure 149–17.
The variable is set to REFRESH when (tx_lpi_qr_active * tx_refresh active).
The variable is set to QUIET when (tx_lpi_qr_active * !tx_refresh_active).
The variable is set to ALERT when (tx_lpi_alert_active).

rs_fec_frame_done
: A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. It is set FALSE otherwise.

rx_lpi_active
: A Boolean variable that is set TRUE when the PHY receive function is operating in the LPI receive mode and set FALSE otherwise. The LPI receive mode begins when the sleep signal is detected and lasts until the alert signal is detected. When the EEE capability is not supported, rx_lpi_active is set FALSE.

rx_lpi_wake
: A Boolean variable that is set TRUE when the PHY receiver is in the WAKE state and sending IDLE to the XGMII. Set FALSE otherwise. When the EEE capability is not supported, rx_lpi_wake is set FALSE.

tx_alert_start_next
: A Boolean variable that is set TRUE on the frame prior to the one on which the alert transmission can start. It is set FALSE otherwise.

tx_lpi_active
: A Boolean variable that is set TRUE when the PHY transmit function is operating in the LPI transmit mode and during transitions to and from the LPI transmit mode (i.e., at any time when the PHY is transmitting sleep, alert, wake, or quiet-refresh signaling). It is set FALSE otherwise.

tx_lpi_qr_active
: A Boolean variable that is set TRUE during the LPI transmit mode, when the PHY is transmitting quiet-refresh signaling. It is set FALSE otherwise.

tx_refresh_active
: A Boolean value. This variable is set TRUE following the logic described in 149.3.6.1.

tx_sleep_start_next
: A Boolean value. This variable is set TRUE during the seventh RS-FEC frame in every group of eight RS-FEC frames, where the group of eight RS-FEC frames start with the RS-FEC frame after refresh.

tx_lpi_req
: A Boolean variable that is set TRUE when the LPI client indicates that it is requesting operation in the LPI transmit mode via the XGMII. It is set FALSE otherwise.

149.3.7.2.3 Timers

rfer_timer
: Timer that is triggered every $125/(4 \times S)$ µs +1%, –25%. When the timer reaches its terminal count, rfer_timer_done = TRUE. See Table 149–1 for the definition of *S*.

The following timers are required for PHYs that support the EEE capability:

lpi_tx_sleep_timer
: This timer defines the time the local transmitter sends the sleep signal to the link partner.
Values: The condition lpi_tx_sleep_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to eight RS-FEC frame periods.

lpi_tx_alert_timer
: This timer defines the time the local transmitter transmits the alert signal.
Values: The condition lpi_tx_alert_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to four RS-FEC frame periods.

lpi_tx_wake_timer
: This timer defines the time the local transmitter transmits the wake signal.
Values: The condition lpi_tx_wake_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time RS-FEC frame periods.

lpi_rx_wake_timer
: This timer defines the time the receiver sends IDLE blocks to the XGMII after the alert signal is detected.
Values: The condition lpi_rx_wake_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time RS-FEC frame periods.

149.3.7.2.4 Functions

DECODE(rx_coded<64:0>)
: In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the

RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 149.3.2.2.2.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 149.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 65-bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 65-bit rx_coded vector as belonging to one or more of the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and eight valid control characters other than /E/ and /LI/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /LI/.

LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:

a) Four control characters of /LI/ followed by four control characters of /I/;
b) Four control characters of /I/ followed by four control characters of /LI/

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a MultiGBASE-T1 control code specified in Table 149–2. A valid O code is one containing an O code specified in Table 149–2.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to one or more of the eight types depending on its contents. A vector may

simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) Eight valid control characters other than /O/, /S/, /T/, /E/, and /LI/;
b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains eight control characters of /I/.

LI; If the optional EEE capability is supported, then the LI type occurs when the vector contains eight control characters of /LI/.

LII; If the optional EEE capability is supported, then the LII type occurs when the vector contains one of the following:

a) Four control characters of /LI/ followed by four control characters of /I/;
b) Four control characters of /I/ followed by four control characters of /LI/.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 149–2. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 149–2.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT
Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

149.3.7.2.5 Counters

lpi_rxw_err_cnt
An integer value that counts the number of receive wake time faults. lpi_rxw_err_cnt is reset to zero during PCS_TEST. The counter is reflected in register 3.22 (see 45.2.3.12).

rfer_cnt
Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt
Count number Reed-Solomon frames received during current period.

149.3.7.2.6 Messages

RX_FRAME
A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

149.3.7.3 State diagrams

The RFER monitor state diagram shown in Figure 149–15 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 149–16 and Figure 149–17 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

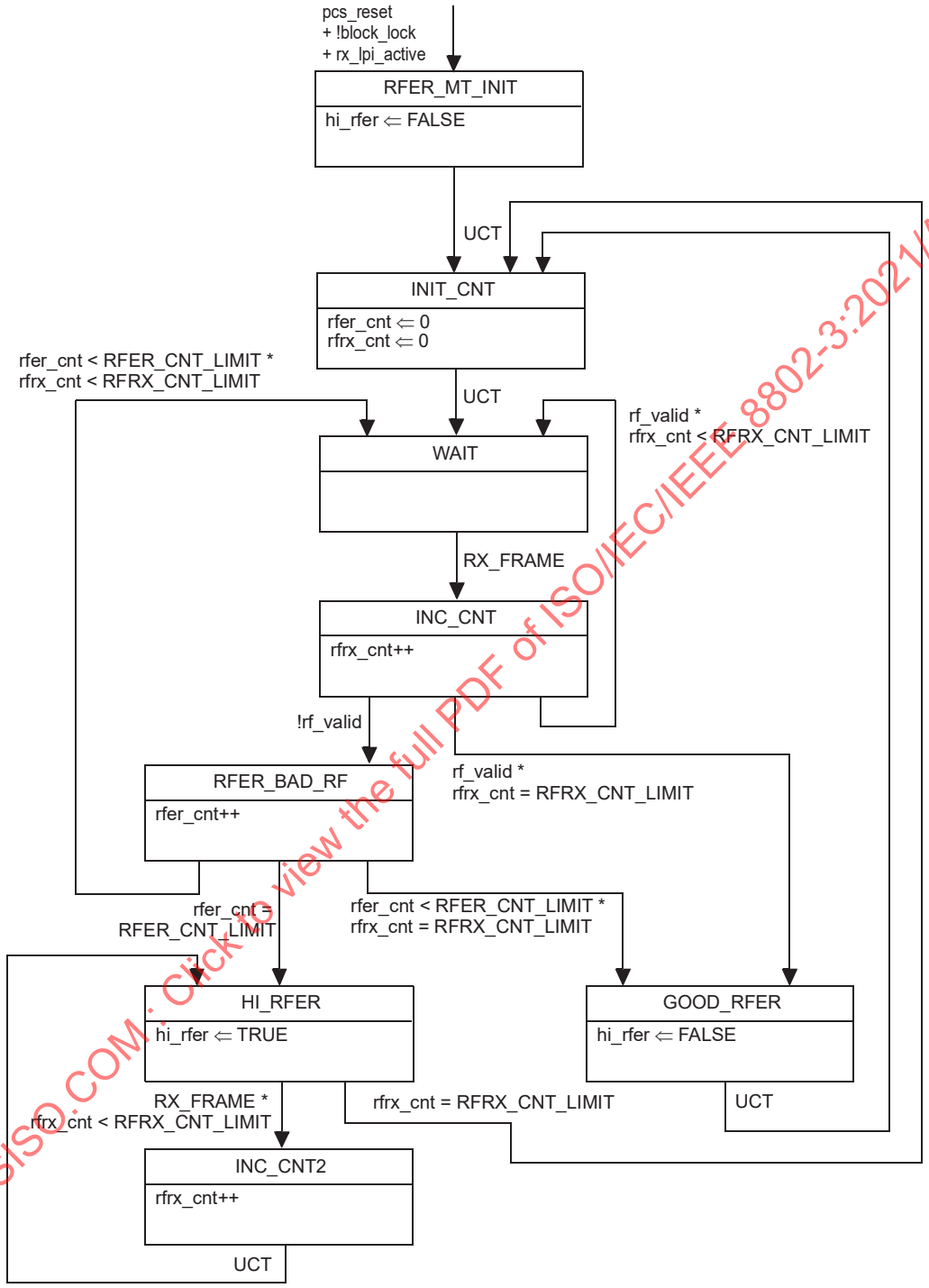
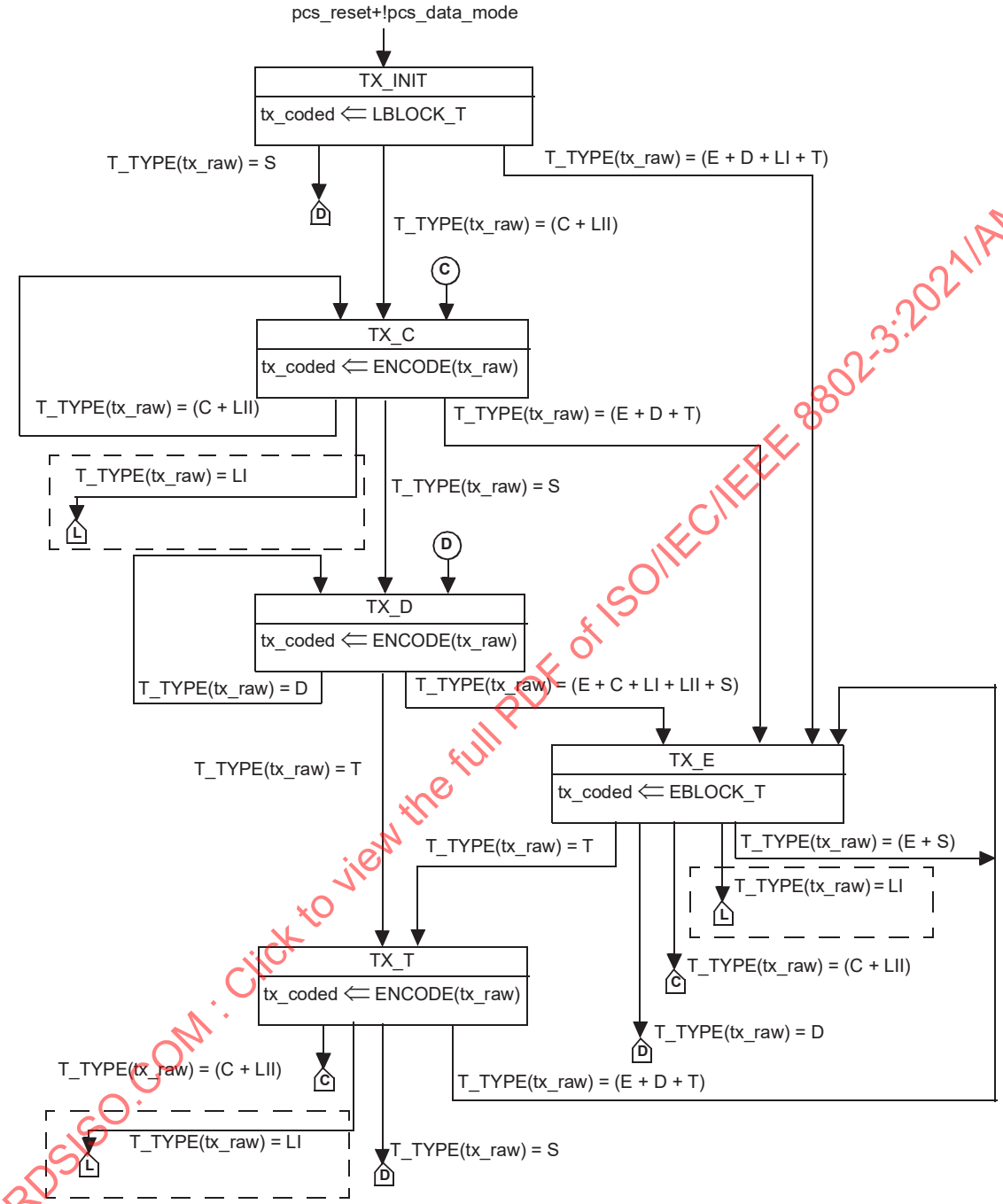
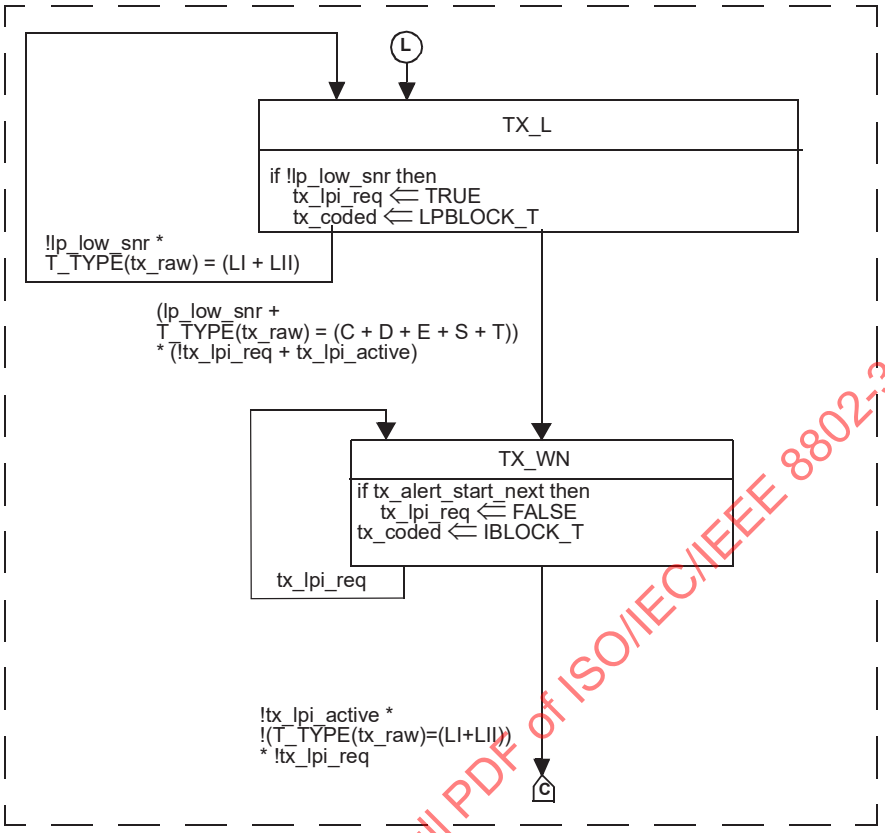


Figure 149–15—RFER monitor state diagram



NOTE—Transitions inside dashed boxes are only required for the EEE capability.

Figure 149–16—PCS 64B/65B Transmit state diagram, part a



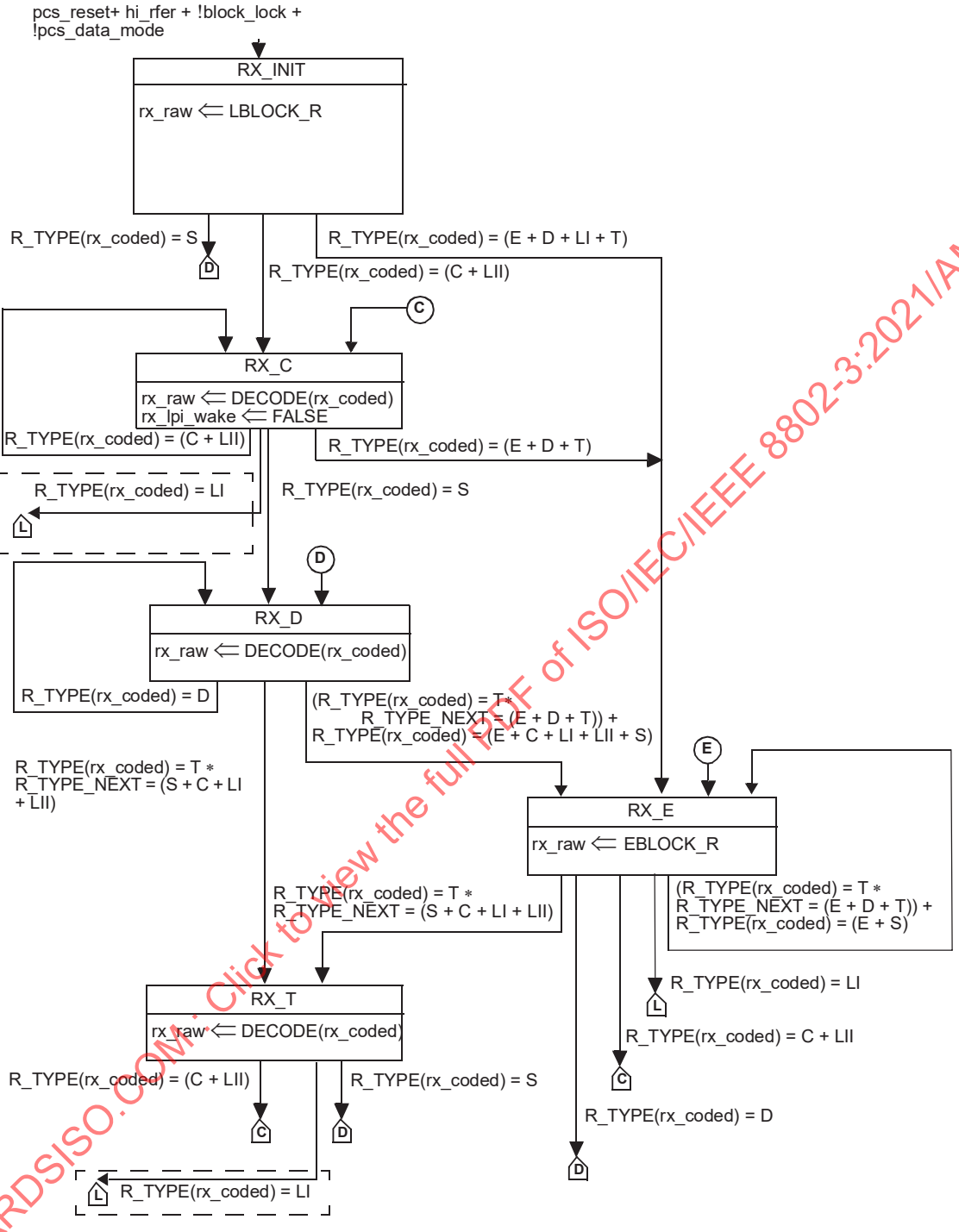
NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 149–17—PCS 64B/65B Transmit state diagram, part b

The PCS 64B/65B Receive state diagram is shown in Figure 149–18 and Figure 149–19 and controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

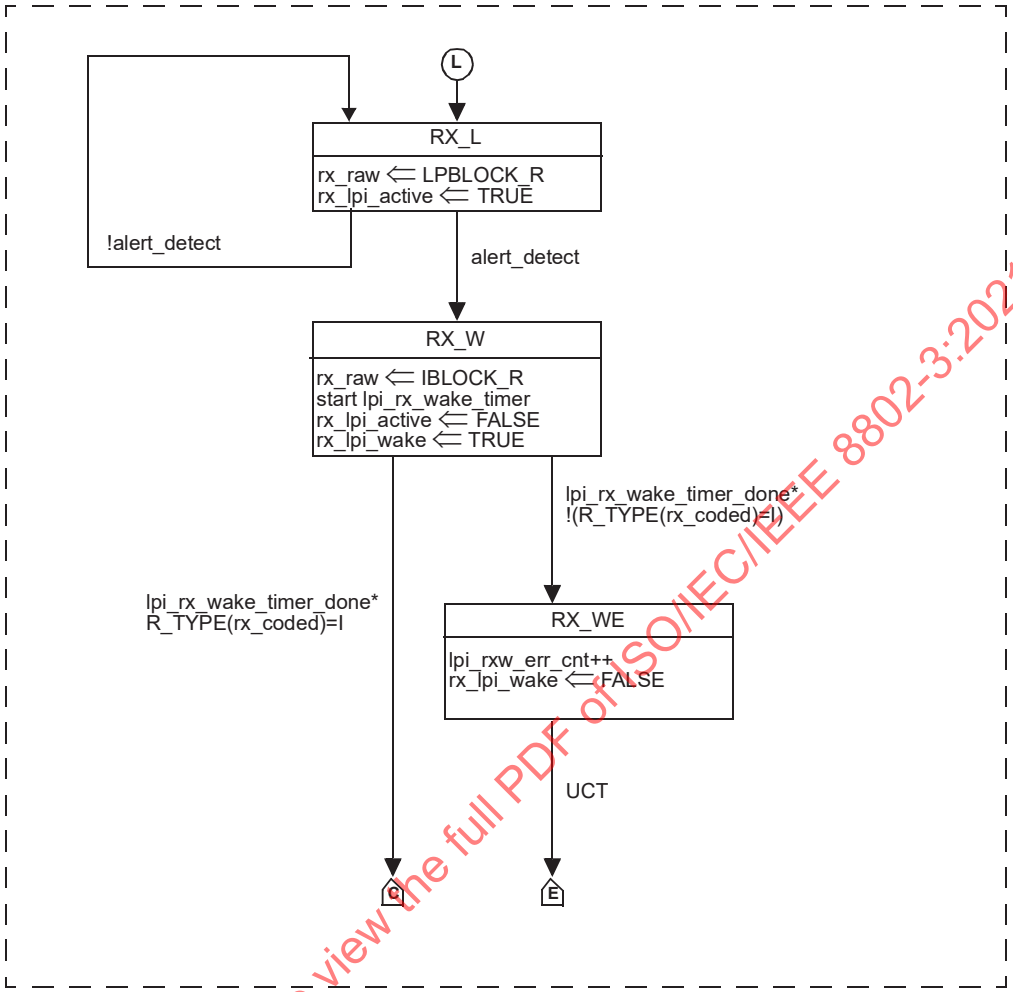
The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams. The PCS shall not perform the RFER monitor function during LPI receive operation from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.

Transitions surrounded by dashed rectangles indicate requirements for MultiGBASE-T1 EEE-capable implementations.



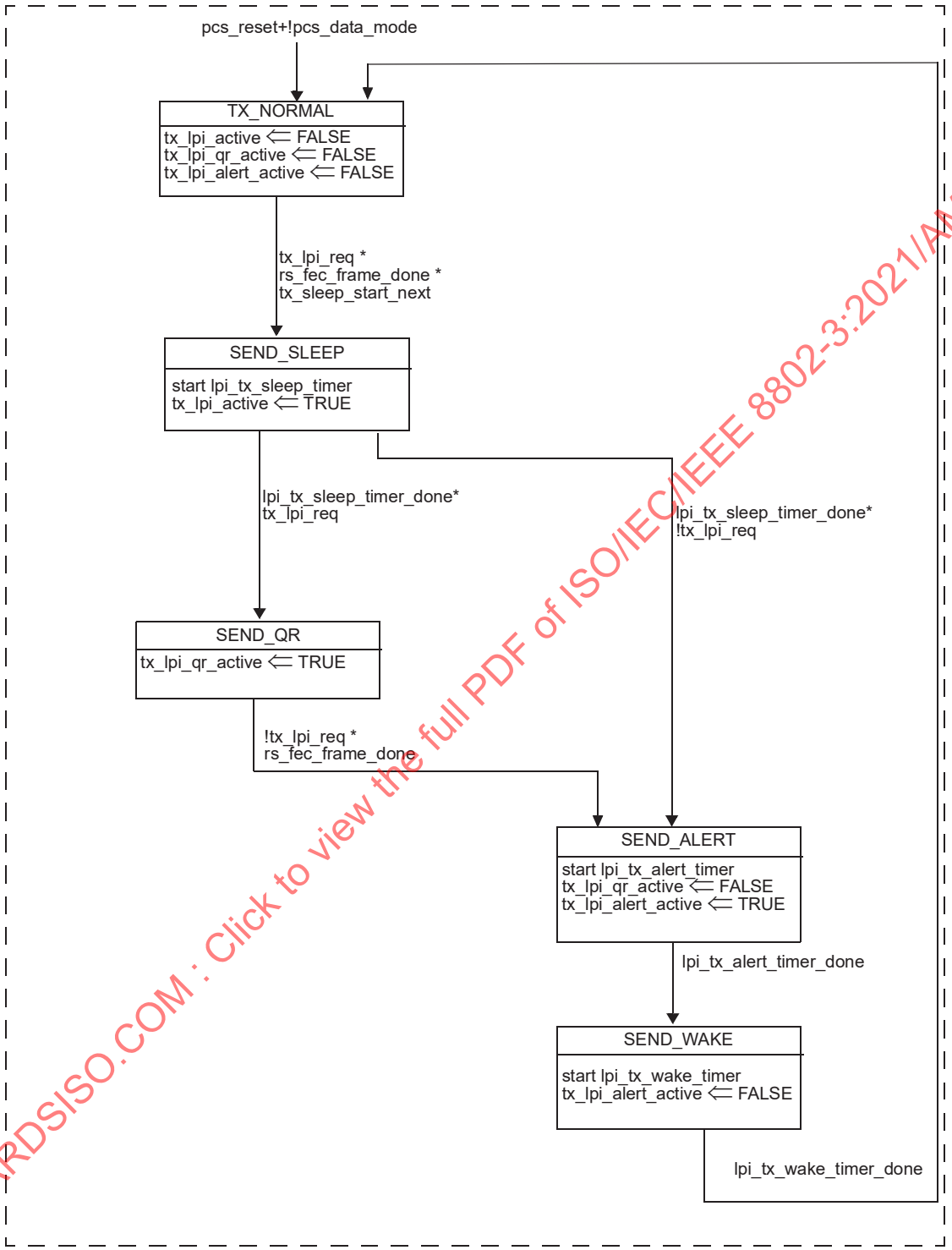
NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 149–18—PCS 64B/65B Receive state diagram, part a



NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 149–19—PCS 64B/65B Receive state diagram, part b



NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 149–20—EEE transmit state diagram

149.3.8 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

149.3.8.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO bit 3.2323.2 and the inverse of this status is reflected in MDIO bit 3.2323.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

Rx LPI indication:
: For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS Receive state diagram (Figure 149–19) is in the RX_L or RX_W states. This status is reflected in MDIO bit 3.2323.8. A latching high version of this status is reflected in MDIO bit 3.2323.10 (Rx LPI received).

Tx LPI indication:
: For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS Transmit state diagram (Figure 149–17) is in the TX_L or TX_WN states. This status is reflected in MDIO bit 3.2323.9. A latching high version of this status is reflected in MDIO bit 3.2323.11 (Tx LPI received).

149.3.8.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 149–15) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

149.3.8.3 Loopback

The PCS shall be placed in loopback mode when the loopback bit (MDIO bit 3.2322.14) is set to a one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of 65B RS-FEC encoded PAM4 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

149.3.9 MultiGBASE-T1 operations, administration, and maintenance (OAM)

The MultiGBASE-T1 PCS level operations, administration, and maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. When OAM is implemented, behavior shall conform to the state diagrams in Figure 149–24 and Figure 149–25. OAM information is exchanged out of band between two PHYs using excess bandwidth available on the link. The OAM is strictly between two PHYs on the Physical Layer and their associated management entities if present. Passing OAM information to other layers is outside the scope of this standard.

OAM is operational as long as both PHYs implement this mechanism and the link is up. It continues to be operational during Low Power Idle, albeit the information is transferred at a slower rate during the refresh cycle.

The OAM frame data is carried in the OAM 10-bit field described in 149.3.2.2.14 for the normal power data mode and 149.3.6.3 for low power mode. This 10-bit field is used to exchange OAM frames. The implementation of the OAM frame exchange function is optional. However, if EEE is implemented, then the OAM frame exchange function is implemented to exchange, at a minimum, the link partner OAM status.

For the remainder of this subclause, the term OAM is specific to the MultiGBASE-T1 PCS level OAM.

149.3.9.1 Definitions

OAM frame: A frame consisting of 14 octets of data, 14 framing bits, 14 reserved bits and two 10-bit Reed-Solomon parity symbols.

OAM symbol: A 10-bit symbol consisting of either one data octet plus a framing bit and a reserved bit, or a 10-bit Reed-Solomon parity symbol. Sixteen OAM symbols make up an OAM frame.

OAM field: A 10-bit field in each PHY frame reserved for the OAM symbol as described in 149.3.2.2.14 or in each refresh cycle as described in 149.3.6.3.

OAM message: A message contains a 4-bit message number plus 8 octets of message data (Message<7:0><7:0>) embedded in an OAM frame. The same OAM message can be repeated on multiple OAM frames.

OAM status: The 4 octets of status data (Message<11:8><7:0>) that is embedded in each OAM frame.

149.3.9.2 Functional specifications

149.3.9.2.1 MultiGBASE-T1 OAM frame structure

Each OAM frame is made up of 16 OAM symbols. Each of the first 14 symbols is made up of one octet of data, one framing bit, and one reserved bit. The last 2 symbols are the Reed-Solomon (16,14) parity symbols.

One OAM symbol is placed in the 10-bit OAM field in each PHY frame during normal power operation in the data mode. One OAM symbol is placed in the 10-bit OAM field in each refresh cycle during Low Power Idle. The sixteen OAM symbols are consecutively inserted into sixteen consecutive PHY frames and/or refresh cycles. Once the sixteen symbols of the current OAM frame are inserted, the sixteen symbols of the next OAM frame are inserted. This process is continuous without any break in the insertion of OAM symbols with the exception noted below.

When the PCS frame is operating in interleaved mode of 2x or 4x, the first symbol (OAM<0>) shall be inserted in the first RS frame in the superframe so that the full OAM frame can be packed into eight superframes in the 2x interleaved mode, and into four superframes in the 4x interleaved mode.

When transitioning from normal operation to Low Power Idle, it is possible that part of the OAM frame is packed in RS frames and the remainder of the OAM frame is sent over the LPI refreshes.

When transitioning from Low Power Idle to normal operation, it is possible that part of the OAM frame is sent over the LPI refreshes and the remainder of the OAM frame is packed in RS frames. In some instances, it is possible that the remainder of the OAM frame cannot be aligned where the next OAM frame will have its first symbol (OAM<0>) inserted in the first RS frame of the superframe. In such cases, the partially transmitted OAM frame shall be interrupted according to the following rules:

1x interleaving — no interruption is required.

2x interleaving — insert 0 or 1 dummy OAM symbol into the superframe for alignment before continuing.

4x interleaving — insert 0 to 3 dummy OAM symbols into the superframe for alignment before continuing.

The receiver can anticipate when the dummy OAM symbols will be inserted based on the sequence of refresh and wake events.

The dummy OAM symbol is all 0's and its value is ignored at the receiver.

An example in Figure 149–21 shows two dummy OAM symbols inserted to realign OAM<0> to the 4x interleaved superframe boundary.

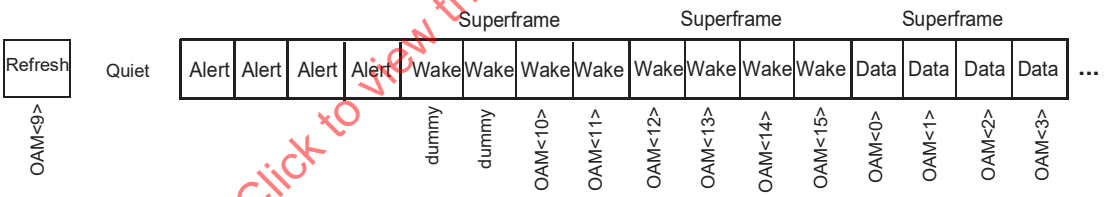


Figure 149–21—Example of 4x interleave dummy data insertion

Bit 0 of each OAM symbol is the first bit transmitted in the 10-bit OAM field. Symbol 0 is the first symbol transmitted in each OAM frame.

The OAM frame boundary can be found at the receiver by looking at bit D8. The boundary is a 0 followed by thirteen 1's followed by two don't care.

If OAM is not implemented then the 10-bit OAM field shall be set to all 0's. If the link partner does not implement OAM, the 10-bit OAM field will remain static.

149.3.9.2.2 OAM frame data

The OAM frame data is shown in Figure 149–22. OAM<*x*><*y*> refers to symbol *x*, bit *y* of the OAM frame. Reserved fields shall be set to 0.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Reserved	0	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Reserved	1	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Reserved	1	Message<0><7:0>							
Symbol 3	Reserved	1	Message<1><7:0>							
Symbol 4	Reserved	1	Message<2><7:0>							
Symbol 5	Reserved	1	Message<3><7:0>							
Symbol 6	Reserved	1	Message<4><7:0>							
Symbol 7	Reserved	1	Message<5><7:0>							
Symbol 8	Reserved	1	Message<6><7:0>							
Symbol 9	Reserved	1	Message<7><7:0>							
Symbol 10	Reserved	1	Message<8><7:0>							
Symbol 11	Reserved	1	Message<9><7:0>							
Symbol 12	Reserved	1	Message<10><7:0>							
Symbol 13	Reserved	1	Message<11><7:0>							
Symbol 14	RS(16,14) parity									
Symbol 15	RS(16,14) parity									

Figure 149–22—OAM frame

149.3.9.2.3 Ping RX

The Ping RX is indicated in OAM<0><3>.

This bit is set by the PHY to the same value as the Ping TX bit received from the link partner.

149.3.9.2.4 Ping TX

The Ping TX is indicated in OAM<0><2>.

This bit is set by the PHY for the link partner to echo on Ping RX.

149.3.9.2.5 PHY health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame
- 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)
- 10: PHY SNR is marginal
- 11: PHY SNR is good

149.3.9.2.6 OAM message valid

The OAM message valid (Valid) is indicated in OAM<1><7>.

— 0: Current OAM frame does not contain a valid OAM message
— 1: Current OAM frame contains a valid OAM message

149.3.9.2.7 OAM message toggle

The OAM message toggle (Toggle) is indicated in OAM<1><6>.

The toggle bit lets the management entity determine which OAM message is being referenced. The toggle bit in the current OAM message is set to the opposite value of the toggle bit in the previous OAM message only if link partner acknowledges the OAM message is received. This allows one OAM message to be delineated from a second OAM message since the same OAM message may be repeated over multiple OAM frames. This bit is valid only if Valid is set to 1.

149.3.9.2.8 OAM message acknowledge

The OAM message acknowledge (Ack) is indicated in OAM<1><5>.

Ack is set by the PHY to let the link partner know that the OAM message sent by the link partner was successfully received as defined in 149.3.9.2.14 and the PHY is ready to accept a new OAM message. An OAM message is defined to be Message_Number<3:0> and Message<7:0><7:0>.

— 0: No acknowledge
— 1: Acknowledge

149.3.9.2.9 OAM message toggle acknowledge

The OAM message toggle acknowledge (TogAck) is indicated in OAM<1><4>.

TogAck is set by the PHY to let the link partner know that the OAM message is being acknowledged. TogAck takes the value of Toggle bit of the OAM message being acknowledged. This bit is valid only if Ack is set to 1.

149.3.9.2.10 OAM message number

The OAM message number is indicated in OAM<1><3:0>.

This field is user-defined but it is recommended that it be used to indicate the meaning of the 8-octet message that follows. If used this way, up to 16 different 8-octet messages can be exchanged.

The message number is user-defined and its definition is outside the scope of this standard.

149.3.9.2.11 OAM message data

The OAM message data is indicated in OAM<9:2><7:0>.

The 8-octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the OAM frame sent by the link partner is successfully received as defined. The OAM frame octet is the lower 8 bits of the 10-bit OAM symbol.

149.3.9.2.12 OAM status

The OAM status data is indicated in OAM<13:10><7:0>.

These 32 bits are set by the PHY to convey its status in the mr_tx_message[95:64] to the link partner.

For additional information on the usage of these bits see Annex 149B.

149.3.9.2.13 OAM Reed-Solomon

The RS(16, 14) parity symbols are indicated in OAM<15:14><9:0>.

The OAM frame shall encode the 14 data symbols using Reed-Solomon code (16,14). The FEC code used is a shortened Reed-Solomon (16,14) code over the Galois Field of GF(2^{10}) — a code operating on 10-bit symbols. The code encodes 14 information symbols and adds 2 parity symbols, enabling correction of up to 1 symbol error. The code is systematic, meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block, and is based on the generating polynomial shown in Equation (149–8).

$$G(Z) = (Z-\alpha)(Z-1) = A_2Z^2 + A_1Z^1 + A_0Z^0 \quad (149\text{–}8)$$

where

α is a root of the binary primitive polynomial $x^{10} + x^3 + 1$ and is represented as 0x002.
A is a series representing the resulting polynomial coefficients of $G(Z)$, (A_2 is equal to 0x001).
Z corresponds to a 10-bit GF(2^{10}) symbol.

The parity calculation shall produce the same result as the shift register implementation shown in Figure 149–23. Before calculation begins, the shift register shall be initialized to zero. The contents of the shift register are transmitted without inversion.

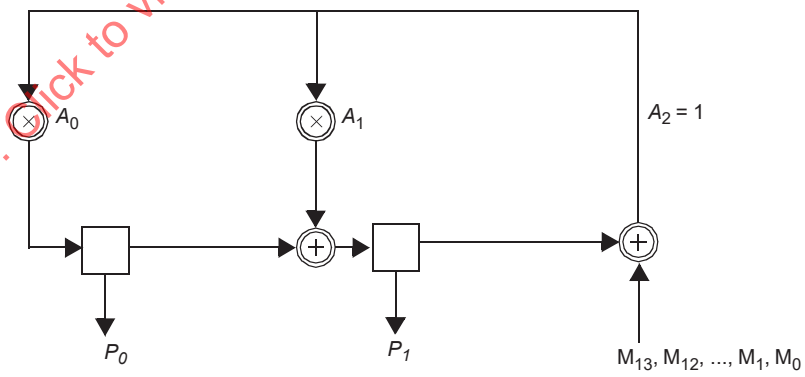


Figure 149–23—OAM FEC parity vector model

A FEC parity vector is represented by Equation (149–9).

$$P(Z) = M(Z) \bmod G(Z) \quad (149\text{–}9)$$

where

$M(Z)$	is the data vector $M(Z) = M_{13}Z^{15} + M_{12}Z^{14} + \ldots + M_0Z^2$. M_{13} is the first 10-bit data symbol and M_0 is the last. (M_{13} corresponds to OAM<0><9:0>, M_{12} corresponds to OAM<1><9:0>, etc.)
$P(Z)$	is the parity vector $P(Z) = P_1Z^1 + P_0Z^0$. P_1 (OAM<14><9:0>) is the first 10-bit parity symbol and P_0 (OAM<15><9:0>) is the last.
A data/parity symbol	(d_9, d_8, …, d_0) is identified with the element: $d_9\alpha^9 + d_8\alpha^8 + \ldots + d_0\alpha^0$ in GF(2^{10}), the finite field with 2^{10} elements.
d_0	is identified as the LSB (OAM<*><0>).
d_9	is identified as the MSB (OAM<*><9>) for all symbols.

The OAM Reed-Solomon parity symbol generation/correction is required only when EEE is implemented. When all 16 symbols of the OAM are embedded in tx_RSmessage<9:0> as described in 149.3.2.2.17 then OAM<15:14><9:0> are dummy symbols and are ignored at the receiver.

149.3.9.2.14 MultiGBASE-T1 OAM frame acceptance criteria

All fields of the OAM frame shall be accepted and updated, unless any of the following occurs:

a) RS(16, 14) contains an uncorrectable error, or
b) there is an uncorrectable PHY frame on any of the 16 symbols.

149.3.9.2.15 PHY health indicator

The PHY current health is sent to the link partner on a per OAM frame basis using the SNR<1:0> bits as described in 149.3.9.2.5. It lets the link partner have an early indication of potential problems that can cause the PHY to drop link or have high error rates.

If EEE is implemented, there can be a case where a PHY's receiver can no longer maintain good SNR based on quiet/refresh cycles. Instead of dropping the link, the PHY can attempt to recover the link by forcing the link partner to exit LPI in its egress direction so that the PHY can use normal power mode to recover. This is done by transmitting SNR<1:0> with a value of 01.

If a PHY receives SNR<1:0> set to 01 by its link partner, then it cannot enter into LPI in the egress direction. If the PHY is already in LPI then the PHY shall immediately exit LPI.

149.3.9.2.16 Ping

The PingTx bit is set based on the value in mr_tx_ping. The PingRx bit is set based on the latest PingTx received from the link partner. The value in mr_rx_ping is set based on the received PingRx from the link partner. The user can determine that the link partner OAM is operating properly by toggling mr_tx_ping and observing mr_rx_ping matches after a short delay.

The Ping bits are updated on a per OAM frame basis.

149.3.9.2.17 OAM message exchange

Unlike the PHY health indicator, the ping function, and the OAM status that operate on a per OAM frame basis, the OAM message exchange operates on a per OAM message basis that may occur over many OAM frames. The OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass OAM messages and verify their delivery.

The OAM message is first written into the OAM transmit registers in the PHY. The OAM message is then read out of the OAM transmit registers and transmitted to the link partner. After the link partner receives the OAM message, it transfers it into the link partner's OAM receive registers and also sends an acknowledge back to the PHY indicating that the next OAM message can be transmitted. One OAM message can be loaded into the OAM transmit registers while another OAM message is being transmitted by the PHY to the link partner, while yet another OAM message is being read out at the link partner's OAM receive registers. The exchange of OAM messages is occurring concurrently and bi-directionally. The transfers between the management entities can be done asynchronously. On the transmit side, mr_tx_valid = 0 indicates that the next OAM message can be written into the OAM transmit registers. Once the registers are written, the management entity sets mr_tx_valid to 1 to indicate that the OAM transmit registers contain a valid OAM message. Once the message is read out atomically, the state diagram clears the mr_tx_valid to 0 to indicate that the registers are ready to accept the next OAM message.

On the receive side, mr_rx_lp_valid indicates that valid OAM message can be read from the OAM receive registers. Once these registers are read, the mr_rx_lp_valid should be cleared to 0 to indicate that the registers are ready to receive the next OAM message. If mr_rx_lp_valid is not cleared, then the OAM message transfer will eventually stall since the sender cannot send new OAM messages if the receiver does not acknowledge that an OAM message has been transferred into the OAM receive registers.

The management entities can asynchronously read mr_tx_valid and mr_rx_lp_valid to know when OAM messages can be transferred in and out of the OAM registers.

The toggle bit alternates between 0 and 1, which lets the management entity determine which OAM message is being referred to. The toggle bit transitioning rules between one OAM frame and the next OAM frame are shown in Table 149–8.

Table 149–8—Toggle bit transition rules

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
0	0	0	0	No valid OAM message
0	0	0	1	Illegal transition (Error)
0	0	1	0	New OAM message starting
0	0	1	1	Illegal transition (Error)
0	1	0	0	Illegal transition (Error)
0	1	0	1	No valid OAM message
0	1	1	0	Illegal transition (Error)
0	1	1	1	New OAM message starting
1	0	0	0	Illegal transition (Error)
1	0	0	1	Received acknowledge, no new OAM message to send
1	0	1	0	Repeating current OAM message, waiting for link partner's acknowledge
1	0	1	1	Previous OAM message ending, new OAM message starting
1	1	0	0	Received acknowledge, no new OAM message to send

Table 149–8—Toggle bit transition rules *(continued)*

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
1	1	0	1	Illegal transition (Error)
1	1	1	0	Previous OAM message ending, new OAM message starting
1	1	1	1	Repeating current OAM message, waiting for link partner's acknowledge

149.3.9.3 State diagram variable to OAM register mapping

The state diagrams of Figure 149–24 and Figure 149–25 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface to communicate the OAM information to and from the management entity. Clause 45 MDIO registers are defined in MMD3 to support the OAM. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended. Table 97–6 and Table 149–9 describe the MDIO register to the state diagrams variable mapping.

Table 149–9—State variables to OAM register mapping

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
MultiGBASE-T1 OAM status Message 8	MultiGBASE-T1 OAM status message register	3.2318.7:0	mr_tx_message[71:64]
MultiGBASE-T1 OAM status Message 9	MultiGBASE-T1 OAM status message register	3.2318.15:8	mr_tx_message[79:72]
MultiGBASE-T1 OAM status Message 10	MultiGBASE-T1 OAM status message register	3.2319.7:0	mr_tx_message[87:80]
MultiGBASE-T1 OAM status Message 11	MultiGBASE-T1 OAM status message register	3.2319.15:8	mr_tx_message[95:88]
Link partner MultiGBASE-T1 OAM status Message 8	Link partner MultiGBASE-T1 OAM status message register	3.2320.7:0	mr_rx_lp_message[71:64]
Link partner MultiGBASE-T1 OAM status Message 9	Link partner MultiGBASE-T1 OAM status message register	3.2320.15:8	mr_rx_lp_message[79:72]
Link partner MultiGBASE-T1 OAM status Message 10	Link partner MultiGBASE-T1 OAM status message register	3.2321.7:0	mr_rx_lp_message[87:80]
Link partner MultiGBASE-T1 OAM status Message 11	Link partner MultiGBASE-T1 OAM status message register	3.2321.15:8	mr_rx_lp_message[95:88]

149.3.9.4 Detailed functions and state diagrams

149.3.9.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

149.3.9.4.2 State diagram parameters

149.3.9.4.3 Variables

frame_boundary
: Frame boundary detection based on the latest 16 rx_oam_field<8> received. The leftmost bit is the earliest received bit.
Values:
TRUE: latest 16 rx_oam_field<8> = 01111111111111xx
FALSE: latest 16 rx_oam_field<8> ≠ 01111111111111xx

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_rx_lp_message[95:0]
: Twelve octet OAM message from the link partner. mr_rx_lp_message[63:0] in this variable is valid only when mr_rx_lp_valid is 1. mr_rx_lp_message[95:64] is always valid and continuously updated.

mr_rx_lp_message_num[3:0]
: Four bit message number from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1.

mr_rx_lp_SNR[1:0]
: Link partner health status.
Values:
00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.
01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).
10: PHY SNR is marginal.
11: PHY SNR is good.
The threshold for the status is implementation dependent.

mr_rx_lp_toggle
: The toggle bit value associated with the eight octet BASE-T1 OAM message from the link partner.
Values:
The toggle bit alternates between 0 and 1.

mr_rx_lp_valid
: Indicates whether the OAM message in mr_rx_lp_message[63:0], mr_rx_lp_message_num[3:0] and the toggle bit in mr_rx_lp_toggle is valid or not. This variable should be cleared when mr_rx_lp_message[63:48] is read and is not explicitly shown in the state diagram. The clearing of this variable indicates to the state diagram that the BASE-T1 OAM message is read by the user and the state diagram can proceed to load in the next BASE-T1 OAM message.
Values:
0: invalid
1: valid

mr_rx_ping
: Echoed ping value from the link partner.
Values:
The value can be 0 or 1.

mr_tx_message[95:0]
: Eight-octet BASE-T1 OAM message and four-octet MultiGBASE-T1 status transmitted by the local PHY. mr_tx_message[63:0] in this variable is valid only when mr_tx_valid is 1. mr_tx_message[95:64] in this variable is always valid.

mr_tx_message_num[3:0]
: Four-bit message number transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is 1.

mr_tx_ping
: Ping value transmitted by the local PHY.
Values:
The value can be 0 or 1.

mr_tx_received
: Indicates whether the most recently transmitted BASE-T1 OAM message with a toggle bit value of mr_tx_received_toggle was received, read, and acknowledged by the link partner. This variable shall clear on read.
Values:
0: BASE-T1 OAM message was not received and read by the link partner.
1: BASE-T1 OAM message was received by the link partner.

mr_tx_received_toggle
: Toggle bit value of the BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if mr_tx_received is 1.
Values:
The value can be 0 or 1.

mr_tx_SNR[1:0]
: Status register indicating PHY health status.
Values:
00: PHY link is failing and will drop link and relink within 2 to 4 ms after the end of the current OAM frame.
01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).
10: PHY SNR is marginal.
11: PHY SNR is good.
The threshold for the status is implementation dependent.

mr_tx_toggle
: The toggle bit value associated with the eight-octet BASE-T1 OAM message transmitted by the PHY. The value is automatically set by the state diagram and cannot be set by the user. This bit should be read and recorded prior to setting mr_tx_valid to 1.
Values:
The toggle bit alternates between 0 and 1.

mr_tx_valid
: Indicates whether BASE-T1 OAM message in mr_tx_message[63:0] and mr_rx_lp_message_num[3:0] is valid or not. This register will be cleared by the state diagram to indicate whether the next BASE-T1 OAM message can be written into the registers.
Values:
0: invalid
1: valid

reset
Reset
Values:
FALSE: OAM circuit is not in reset.
TRUE: OAM circuit is in reset.

rs_check
Status of the latest rs_correct() operation
Values:
GOOD: no errors or correctable error
BAD: uncorrectable error

rx_ack
Acknowledge from link partner in response to PHY's BASE-T1 OAM message.
Values:
0: no acknowledge
1: acknowledge

rx_ack_toggle
The toggle value corresponding to the PHY's BASE-T1 OAM message that the link partner is acknowledging. This value is valid only if the rx_ack is set to 1.
Values:
The toggle bit can take on values of 0 or 1.

rx_boundary
This variable is set to TRUE whenever the receive data stream reaches the end of a Reed-Solomon frame and a dummy OAM symbol is not expected per 149.3.9.2.1 during normal power operation in the data mode, or at the end of a received refresh cycle during Low Power Idle operation. This variable is set to FALSE at other times.
Values:
FALSE: Receive stream is not at a boundary end.
TRUE: Receive stream is at a boundary end.

rx_exp_toggle
This variable holds the expected toggle value of the next BASE-T1 OAM message. This is normally the opposite value of the current toggle value, but shall reset on error conditions where two back-to-back BASE-T1 OAM messages separated by BASE-T1 OAM frames without a valid message have the same toggle value.
Values:
The toggle bit can take on values of 0 or 1.

rx_lp_ack
Acknowledge from PHY in response to link partner's BASE-T1 OAM message. Indicates whether valid BASE-T1 OAM message from the link partner has been sampled into the PHY's registers.
Values:
0: no acknowledge / not sampled
1: acknowledge / sampled

rx_lp_ping
Ping value received from the link partner that is looped back.
Values:
The value can be 0 or 1.

rx_lp_toggle
: The toggle bit value in the previous BASE-T1 OAM frame received from the link partner.
Values:
: The toggle bit alternates between 0 and 1.

rx_lp_valid
: Indicates whether BASE-T1 OAM message in previous BASE-T1 OAM frame received from the link partner is valid or not.
Values:
: 0: invalid
1: valid

rx_oam_field<9:0>
: Ten-bit BASE-T1 OAM symbol extracted from a received Reed-Solomon frame during normal power operation in the data mode, or from a received refresh cycle during Low Power Idle operation.

rx_oam<15 to 0><9:0>
: Raw 16-symbol OAM frame received from the link partner.

SNR[1:0]
: PHY health status.
Values:
: 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.
01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).
10: PHY SNR is marginal.
11: PHY SNR is good.
Both the status threshold and condition for generating this status are implementation dependent.

tx_boundary
: This variable is set to TRUE whenever the transmit data stream reaches the start of a PHY frame and a dummy OAM symbol is not transmitted per 149.3.9.2.1 during normal power operation in the data mode, or at the start of a transmit refresh cycle during Low Power Idle operation. This variable is set to FALSE at other times.
Values:
: FALSE: Transmit stream is not at a boundary end.
TRUE: Transmit stream is at a boundary end.

tx_oam_field<9:0>
: Ten-bit BASE-T1 OAM symbol inserted into a transmitted Reed-Solomon frame during normal power operation in the data mode, or into a transmitted refresh cycle during Low Power Idle operation.

tx_oam<15 to 0><9:0>
: Raw 16-symbol OAM frame transmitted from the PHY.

tx_lp_ready
: Indicates whether the link partner is ready to receive the next BASE-T1 OAM message from the PHY. If ready, then the PHY will load the next BASE-T1 OAM message from the registers and begin transmitting them.
Values:
0: not ready
1: ready

tx_toggle
: The toggle bit value being sent in the current BASE-T1 OAM frame transmitted by the PHY.
Values:
The value can be 0 or 1.

149.3.9.4.4 Counters

rx_cnt
: A count of received OAM frame symbols.
Values:
The value can be any integer from 0 to 16, inclusive.

tx_cnt
: OAM frame transmit symbol count.
Values:
The value can be any integer from 0 to 16, inclusive.

tx_rec
: A count of received RS-FEC block errors, both correctable and uncorrectable.
Values:
The value can be any integer from 0 to 65 535, inclusive.

149.3.9.4.5 Functions

rs (14 OAM symbols)
: This function outputs the 2 parity symbols as defined in 149.3.9.2.13.
If all 16 symbols of the OAM frame are embedded in tx_RSmessage<9:0> as described in 149.3.2.2.15 then this function can return any arbitrary value.

rs_correct (16 OAM symbols)
: This function outputs the 14 corrected data symbols as defined in 149.3.9.2.13 and sets/clears the rs_check variable when at least one of the 16 symbols of the OAM frame is embedded in a LPI refresh.
Otherwise, this function returns the 14 data symbols unmodified and sets rs_check to GOOD if none of the 16 RS(360, 326) frames are uncorrectable.

149.3.9.4.6 State diagrams

The receive state diagram is shown in Figure 149–24 and the transmit state diagram is shown in Figure 149–25.

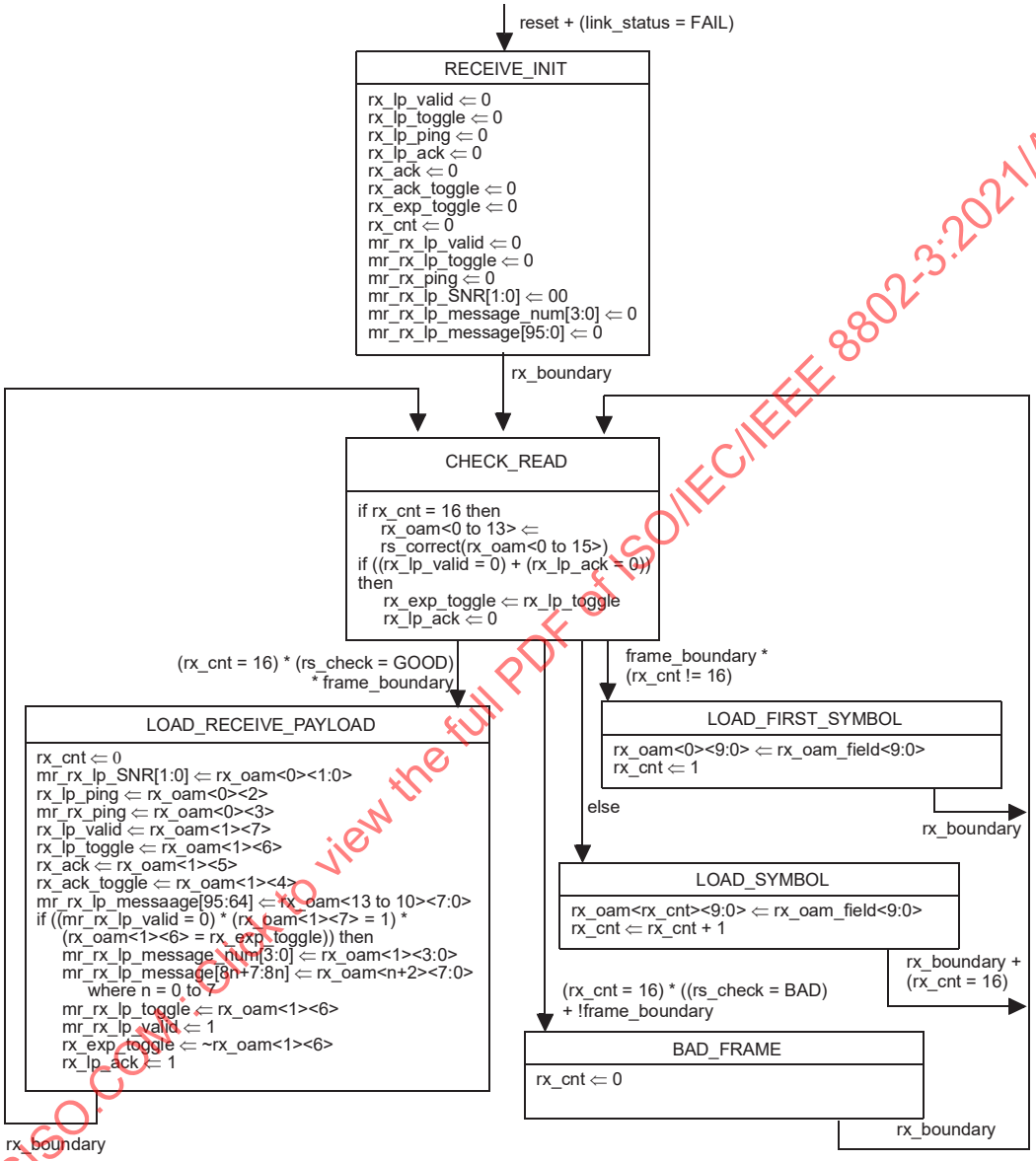


Figure 149–24—Receive state diagram

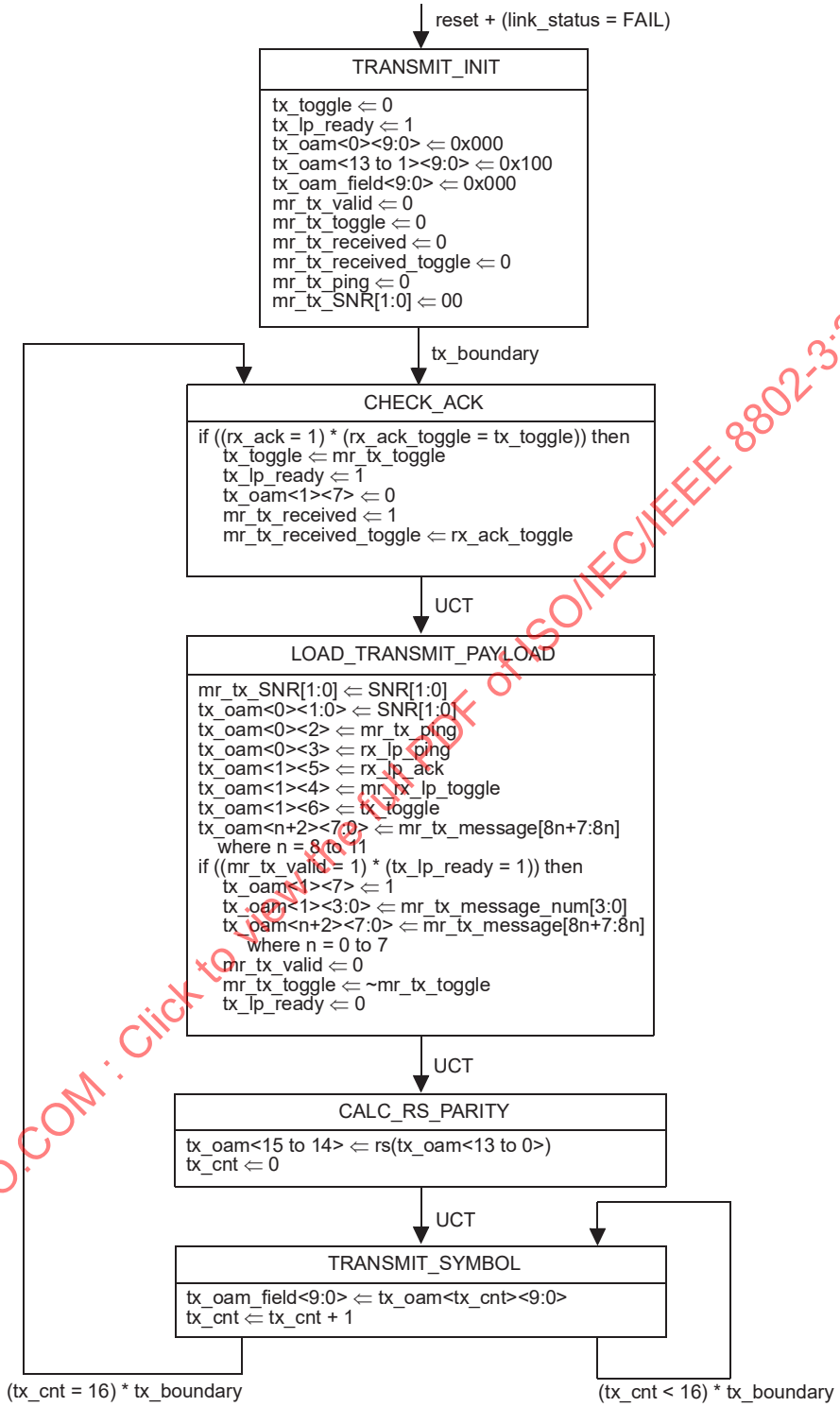


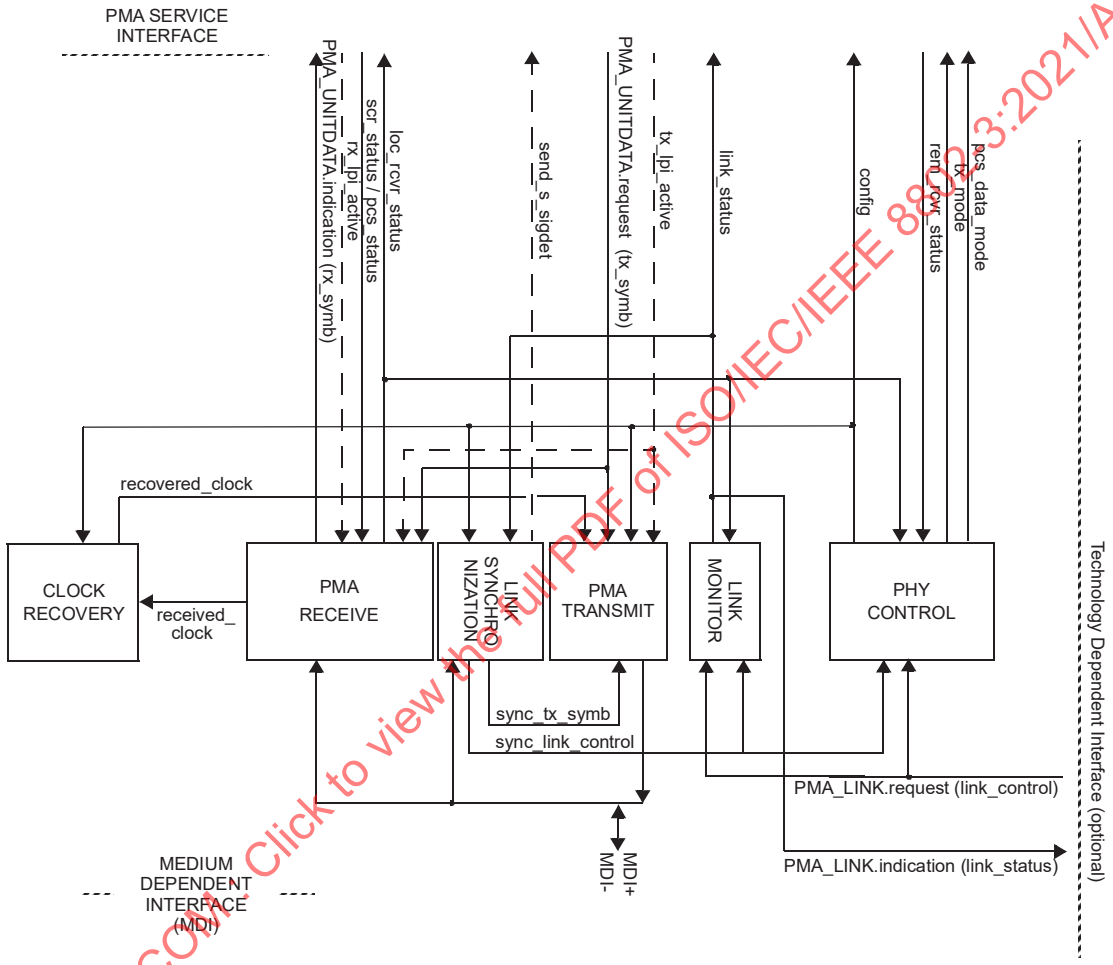
Figure 149–25—Transmit state diagram

149.4 Physical Medium Attachment (PMA) sublayer

149.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 149.2.2 to the MultiGBASE-T1 baseband medium, specified in 149.7.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 149.8.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 149–26—PMA reference diagram

149.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 149–26, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 149–26.

149.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The MultiGBASE-T1 PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 149–32).

149.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a four-level modulated signal on the single balanced pair of conductors. When the PHY Control state diagram (Figure 149–32) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit. When lpi_tx_mode = ALERT, the PN sequence defined in 149.4.2.6 shall be used in place of tx_symb as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 149.5.2.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 149.5.2.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 149.4.2.8 while meeting the jitter requirements of 149.5.2.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

149.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

149.4.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM4 signals on the balanced pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over the receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 149.7.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb is needed to perform echo cancellation.

The PMA Receive function uses the parameters pcs_status and scr_status, and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 149–32). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.193.7.

149.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 149–32.

During PMA training (TRAINING and COUNTDOWN states in Figure 149–32), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the first 96 bits of the 16th partial PHY frame (bits 6750 to 6845). The Infofield is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM4 transition.

The 12-octet Infofield shall include the fields in 149.4.2.4.2 through 149.4.2.4.8, also shown in Figure 149–27 and Figure 149–28. Infofield shall be transmitted at least 256 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 149–27—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149–28—Infofield COUNTDOWN format

149.4.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

149.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0> and so forth.

149.4.2.4.3 Partial PHY frame count (PFC24)

The partial PHY frame count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 16 partial PHY frames per PHY frame and the Infofield is embedded within the 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 15.

PFC24 continues to run uninterrupted for the duration of the link. The resolution of PFC24 is large enough that it does not rollover during the allotted training time. However, it will rollover if allowed to run indefinitely. PFC24 is defined to rollover to 0 after it reaches 16 776 959 to align with the EEE QR cycle.

149.4.2.4.4 Message Field

The Message Field is one octet. For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 149–10 for the MASTER and Table 149–11 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 149–10 for the MASTER and the first or second row of Table 149–11 for the SLAVE. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 149–10—Infofield message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149–11—Infofield message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

149.4.2.4.5 PHY capability bits

When PMA_state<7:6> = 00, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 149–12 for the details.

Table 149–12—PHY capability bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	InterleaverDepth		PrecodeSel		SlowWakeRequest	EEEen	OAMen

The format of PHY capability bits is Oct10<2:1> = InterleaverDepth[1:0], Oct10<4:3> = PrecodeSel[1:0], Oct10<5> = SlowWakeRequest, Oct10<6> = EEEen, Oct10<7> = OAMen, Oct8<7:0> = VendorSpecificData[7:0], and Oct9<7:0> = VendorSpecificData[15:8].

EEEen and OAMen indicate EEE and MultiGBASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of these two optional capabilities by setting the corresponding capability bits.

The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen = 1. The optional BASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1. InterleaverDepth indicates the requested data mode interleaving depth. PrecodeSel indicates the requested precoder. SlowWakeRequest is set to indicate to the link partner that the PHY will transmit alert only immediately following a refresh.

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining bits shall be reserved and set to 0.

149.4.2.4.6 Data switch partial PHY frame count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count

when the transmitter switches from PAM2 to PAM4, which occurs at the start of an RS-FEC superframe. The last value of PFC24 prior to the transition is DataSwPFC24 – 1. DataSwPFC24 shall be set to an integer multiple of 16. When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary. DataSwPFC24 shall be a minimum of 4081 and a maximum of 4785 from the current PFC24 value.

149.4.2.4.7 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

149.4.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 149–29. In Figure 149–29 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 149–29, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

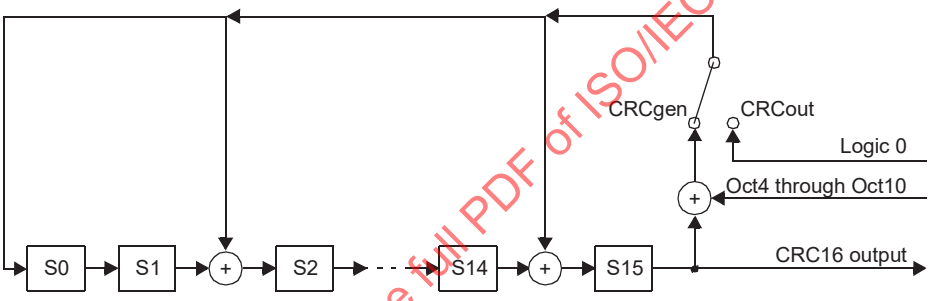


Figure 149–29—CRC16

149.4.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 149–13. Mapping of MDIO status variables to PMA status variables is shown in Table 149–14.

Table 149–13—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1 PMA control register	1.2309.14	PMA_transmit_disable

Table 149–14—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1 PMA status register	1.2310.1	PMA_receive_fault

149.4.2.4.10 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 149–32. If the Auto-Negotiation function is not implemented, or disabled (mr_autoneg_en = FALSE), PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup. The Auto-Negotiation function is optional for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs. If the Auto-Negotiation function is implemented and enabled, Auto-Negotiation is the source of control (via link_control) and MASTER/SLAVE configuration; however, if Auto-Negotiation is either not enabled or is not implemented, the Link Synchronization function is the source of control (via sync_link_control) and MASTER/SLAVE configuration.

During startup, prior to entering the TRAINING state, the SLAVE shall align its transmit 65B RS-FEC frame to within +0/–4 × *S* (See Table 149–1 for the definition of *S*.) partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE Infofield partial PHY frame count shall match the MASTER Infofield partial PHY frame count for the aligned frame.

In the TRAINING state, PAM 2 transmission is used and PHY capabilities are exchanged with Infofields as specified in 149.4.2.4.5.

At any time following the TRAINING state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT state and attempts a retrain.

The startup timing shall comply with Table 149–15 for MASTER and Table 149–16 for SLAVE.

NOTE—See Table 149–1 for the definition of *S*.

Table 149–15—Startup timing maximums for MASTER

Timing interval	Maximum time (ms)
From entry to SILENT state until en_slave_tx = 1 is transmitted	40 – 0.384 / *S*
From entry of SILENT state until entry to COUNTDOWN state	95.975 – 0.384 / *S*
Entry to COUNTDOWN until entry of TX_SWITCH	0.384 / *S*
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

149.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the Auto-Negotiation (if enabled) or Link Synchronization (if Auto-Negotiation is not enabled) process.

Table 149–16—Startup timing maximums for SLAVE

Timing interval	Maximum time (ms)
Entry to exit of SILENT state	40
Entry of SILENT state to exit of TRAINING state	95.975 – 0.384 / *S*
Entry to COUNTDOWN until entry of TX_SWITCH	0.384 / *S*
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

The Link Monitor function shall comply with the state diagram of Figure 149–33.

Upon power on, reset, or release from power down, the Auto-Negotiation function sets link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. During this period, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote MultiGBASE-T1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state diagram begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, the variable link_status = OK is asserted, upon which further PHY operations can take place.

149.4.2.6 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function shall establish the start of PHY PMA training as defined in 149.4.2.4.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 149.4.2.2), and uses a signal, SEND_S. This signal is used by the MASTER and SLAVE to discover the link partner and synchronize the start of PMA training.

The frequency of the SEND_S signal shall be 703.125 MHz.

Link Synchronization employs the SEND_S signal to achieve synchronization prior to link training. If the PHY is configured as MASTER, Link Synchronization shall employ Equation (149–10) as the PN sequence generator.

$$p_M(x) = x^8 + x^4 + x^3 + x^2 + 1 \quad (149–10)$$

If the PHY is configured as SLAVE, Link Synchronization shall employ Equation (149–11) as PN sequence generator.

$$p_{MS}(x) = x^8 + x^6 + x^5 + x^4 + 1 \quad (149–11)$$

The period of both PN sequences is 255.

An implementation of MASTER and SLAVE PHY SEND_S PN sequence generators by linear-feedback shift registers is shown in Figure 149–30. The bits stored in the shift register delay line at time *n* are denoted by $S_n[7:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $S_n[0]$ is generated. The PN sequence generator shift registers shall be reset to a value of $S_n[7:0]$ = 0000 0001 upon entering into the TRANSMIT_DISABLE state (see Figure 149–30) or on the transmission of the first

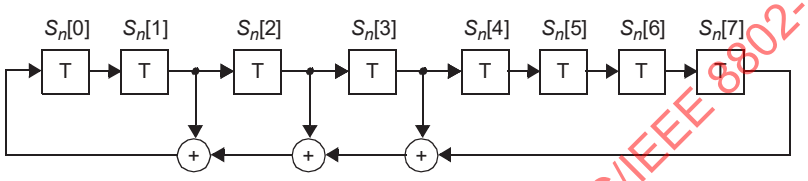
symbol of the alert sequence. The receiver may not necessarily receive a continuous PN sequence between separate periods of the SEND_S signal.

For 10GBASE-T1, the bit $S_n[0]$ shall be mapped to the transmit symbol T_n as follows: if $S_n[0] = 0$ then $T_n = +1\ +1\ +1\ +1\ +1\ +1\ +1\ +1$, if $S_n[0] = 1$ then $T_n = -1\ -1\ -1\ -1\ -1\ -1\ -1\ -1$.

For 5GBASE-T1, the bit $S_n[0]$ shall be mapped to the transmit symbol T_n as follows: if $S_n[0] = 0$ then $T_n = +1\ +1\ +1\ +1$, if $S_n[0] = 1$ then $T_n = -1\ -1\ -1\ -1$.

For 2.5GBASE-T1, the bit $S_n[0]$ shall be mapped to the transmit symbol T_n as follows: if $S_n[0] = 0$ then $T_n = +1\ +1$, if $S_n[0] = 1$ then $T_n = -1\ -1$.

MASTER PHY SEND_S PN sequence generator



SLAVE PHY SEND_S PN sequence generator

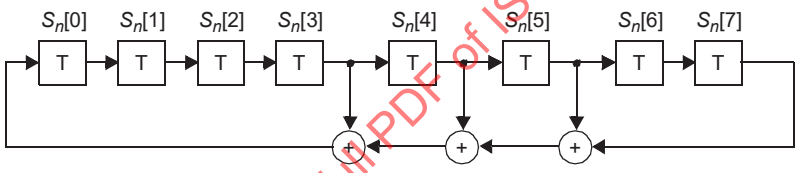


Figure 149–30—SEND_S PN sequence generator by linear feedback shift registers S_n

The PHY Link Synchronization state diagram in Figure 149–31 shall be used to synchronize 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHYs prior to the MultiGBASE-T1 link training. If the Clause 98 Auto-Negotiation function is enabled, then the Auto-Negotiation function shall be used as the mechanism for PHY synchronization and the PHY Link Synchronization state diagram in Figure 149–31 remains in the SYNC_DISABLE state.

149.4.2.6.1 State diagram variables

force_config

This variable indicates whether the PHY operates as a MASTER or as a SLAVE. The variable takes on one of the following values:

MASTER: This value is continuously asserted when the PHY operates as a MASTER.
SLAVE: This value is continuously asserted when the PHY operates as a SLAVE.

force_phy_type

This variable indicates what speed the PHY is to operate when Auto-Negotiation is disabled or not implemented. The variable takes on one of the following values:

10G-T1: If Auto-Negotiation is disabled or not implemented and 10GBASE-T1 is selected.
5G-T1: If Auto-Negotiation is disabled or not implemented and 5GBASE-T1 is selected.
2.5G-T1: If Auto-Negotiation is disabled or not implemented and 2.5GBASE-T1 is selected.

Other values are implementation-dependent and beyond the scope of this clause.

link_status
: The link_status parameter is set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_enable:
: see 98.5.1.

mr_main_reset
: see 98.5.1.

power_on
: see 98.5.1.

send_s_sigdet
: This variable indicates whether the SEND_S signal was detected. This variable shall be set FALSE no later than 1 µs after the signal goes quiet on the MDI.
Values:
TRUE: SEND_S signal detected.
FALSE: SEND_S signal not detected.

sync_link_control
: This variable indicates the data source for the PMA Transmit function.
Values:
DISABLE: The data source is the PHY Link Synchronization function (sync_tx_symb).
ENABLE: The data source is PMA_UNITDATA.request (tx_symb).

149.4.2.6.2 State diagram timers

break_link_timer
: see 98.5.2.

link_fail_inhibit_timer
: see 98.5.2.

send_s_timer
: This timer is used to control the duration SEND_S is transmitted. The timer shall expire 1.25 µs ± 0.05 µs after being started.

sigdet_wait_timer
: This timer is used to control the wait time after transmitting or detecting the end of SEND_S. The timer shall expire 5 µs ± 0.15 µs after being started.

149.4.2.6.3 Messages

sync_tx_symb
: The value of sync_tx_symb is set by the Link Synchronization state diagram and indicates the symbols sent from the PHY Link Synchronization block to PMA Transmit. The Link Synchronization block generates sync_tx_symb synchronously with every transmit clock cycle.
Values:
SEND_S: Transmit the SEND_S signal defined in 149.4.2.6.
SEND_Z: Transmit a zero value.

149.4.2.6.4 State diagrams

The PHY Link Synchronization state diagram is shown in Figure 149–31.

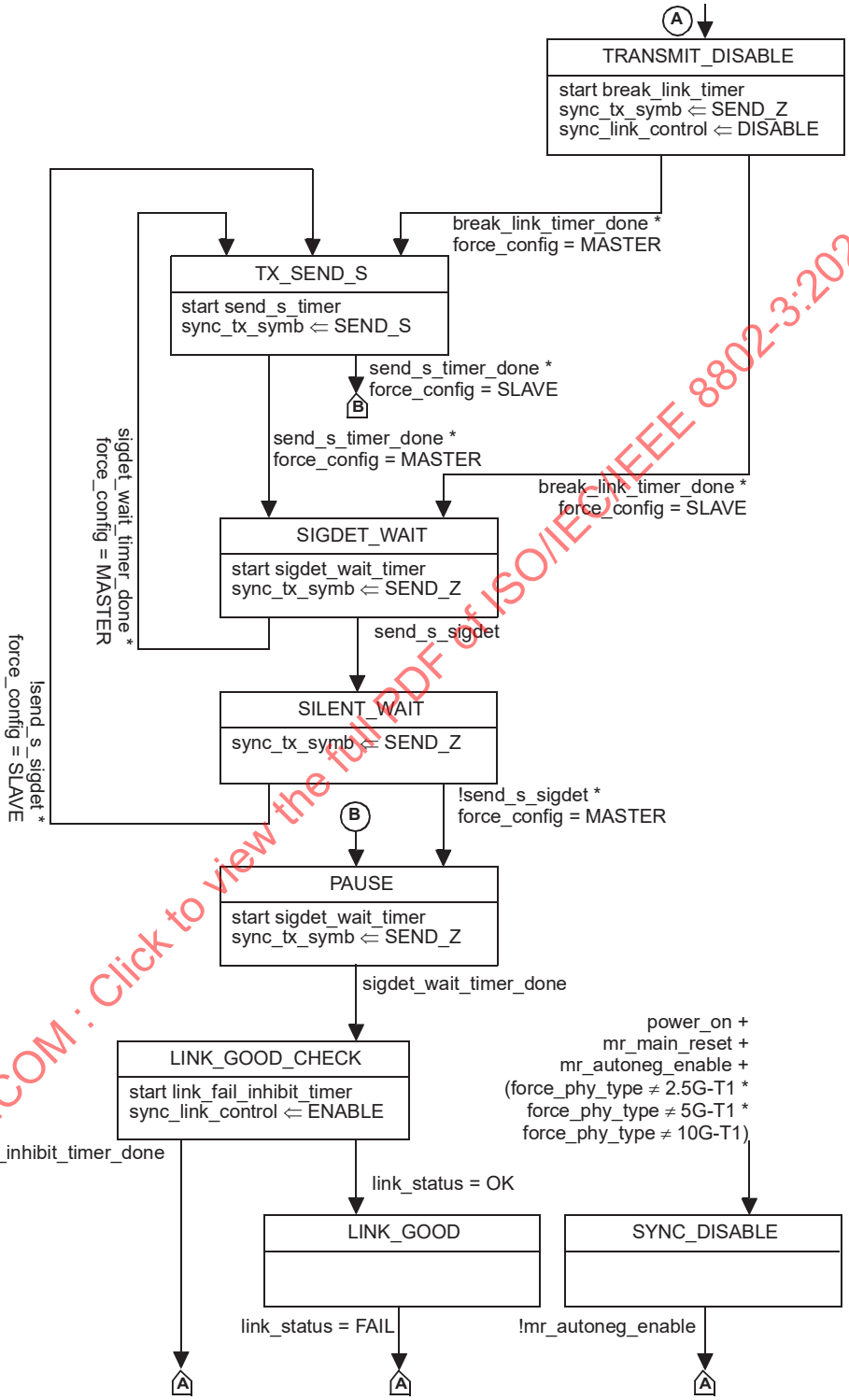


Figure 149–31—PHY Link Synchronization state diagram

149.4.2.7 Refresh monitor function

The Refresh monitor is required for PHYs that support the EEE capability. The Refresh monitor operates when the PHY is in the LPI receive mode. The Refresh monitor shall comply with the state diagram of Figure 149–34. The Refresh monitor sets the PMA_refresh_status variable, which forces a link retrain if a refresh signal is not reliably detected within a moving time window equivalent to 50 complete quiet-refresh cycles (nominally equal to 1.536/S ms), when the PHY is in the lower power receive mode. See Table 149–1 for the definition of S.

149.4.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 149.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

149.4.3 MDI

Communication through the MDI is summarized in 149.4.3.1 and 149.4.3.2.

149.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \quad (149–12)$$

In Equation (149–12), a_n is the PAM4 modulation symbol from the set {–1, –1/3, +1/3, +1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 149.5.2.

149.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \quad (149–13)$$

In Equation (149–13) $h_R(t)$ denotes the symbol response of the overall channel impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources including uncancelled echo. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

149.4.4 State variables

149.4.4.1 State diagram variables

auto_neg_imp
: This variable indicates if an optional Auto-Negotiation sublayer is associated with the PMA.
Values:
TRUE: An optional Auto-Negotiation sublayer is associated with the PMA.
FALSE: An optional Auto-Negotiation sublayer is not associated with the PMA.

config
: The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.
Values: MASTER or SLAVE.

en_slave_tx
: The en_slave_tx variable in the Infofield received by the SLAVE.
Values:
0: MASTER is not ready for the SLAVE to transmit.
1: MASTER is ready for the SLAVE to transmit.

infofield_complete
: This variable indicates that a complete set of Infofield messages has been sent (see 149.4.2.4).
Values:
FALSE: A complete set of Infofield messages has not been sent.
TRUE: A complete set of Infofield messages has been sent.

link_control
: This variable is defined in 149.2.1.1.1.

link_status
: The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.
Values: OK or FAIL.

loc_countdown_done
: This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to TRUE immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.
Values:
OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin
: This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.
Values:
OK: The local device has sufficient SNR margin.
NOT_OK: The local device does not have sufficient SNR margin.

pcs_data_mode
: Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

PMA_refresh_status
: This variable indicates the status of the Refresh monitor as described in 149.4.2.7.
Values: OK or FAIL.

pma_reset
: Allows reset of the PHY Control and Link Monitor state diagrams.
Values: ON or OFF.

PMA_state
: Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.
Values:
00: TRAINING state
01: COUNTDOWN state

rem_countdown_done
: This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state and is set to TRUE once the receiver has transitioned from PAM2 to PAM4.

rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.
Values:
OK: The receive link for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

sync_link_control
: This variable is defined in 149.4.2.6.1.

tx_mode
: The PMA generates this variable continuously and passes it to the PCS via the PMA_TXMODE.indication primitive.
Values:
SEND_N: This value is continuously asserted when transmission of sequences of symbols representing a XGMII data stream take place.
SEND_T: This value is continuously asserted when transmission of sequences of symbols representing the training sequences of symbols is to take place.
SEND_Z: This value is asserted when transmission of zero symbols is to take place.

149.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING, PCS_TEST, and PCS_DATA states. The timer shall expire 975 μs ± 50 μs after being started.

The following timer is required only for PHYs that support the EEE capability:

lpi_refresh_rx_timer
: This timer is used to monitor link quality during the LPI receive mode. If the PHY does not detect reliable refresh signaling before this timer expires then a full retrain is performed.
Values: The condition lpi_refresh_rx_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to 50 complete quiet-refresh signal periods, equivalent to 1.536/*S* ms. See Table 149–1 for the definition of *S*.

149.4.5 State diagrams

The PHY Control state diagram is shown in Figure 149–32, the Link Monitor state diagram is shown in Figure 149–33, and the EEE Refresh monitor state diagram is shown in Figure 149–34.

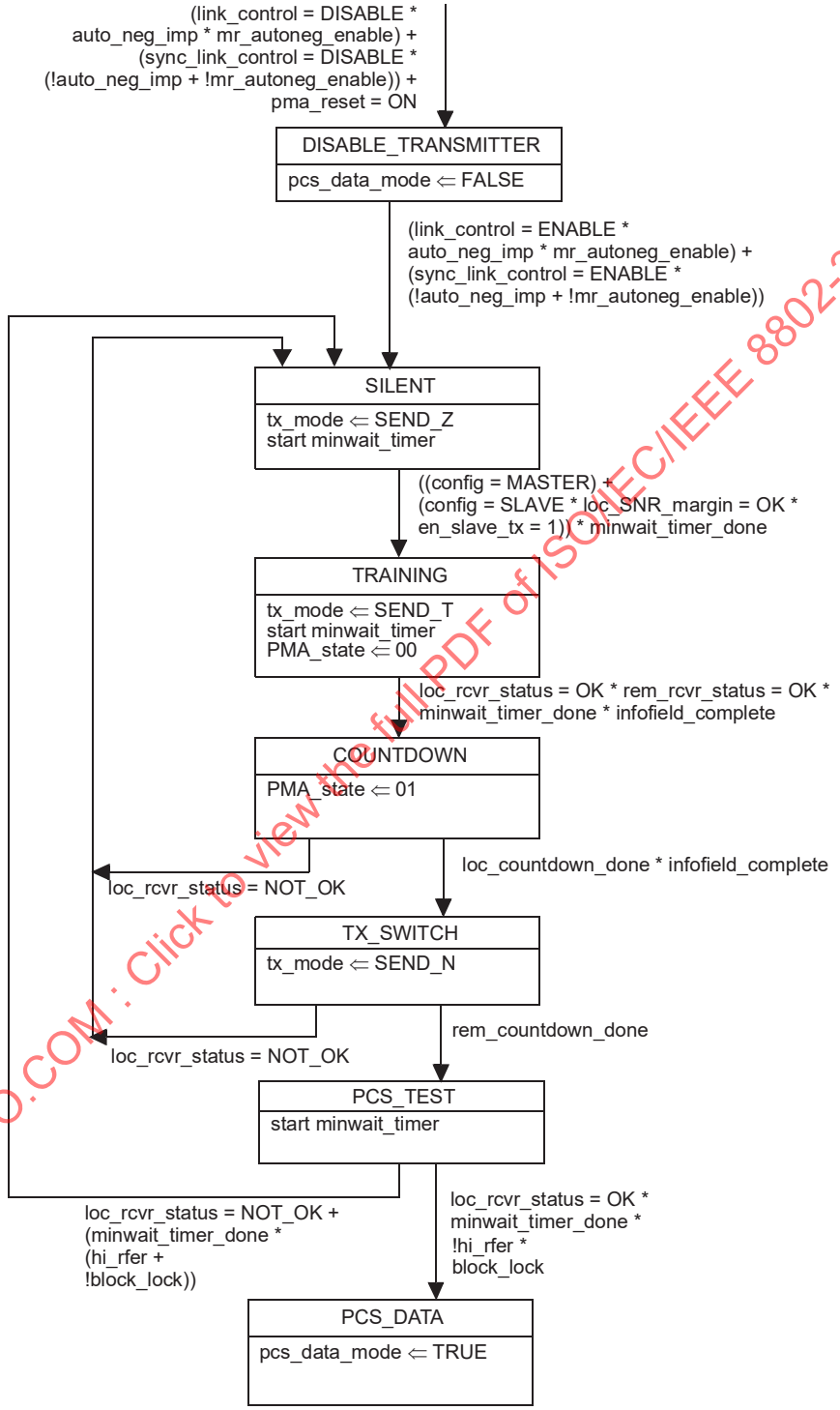
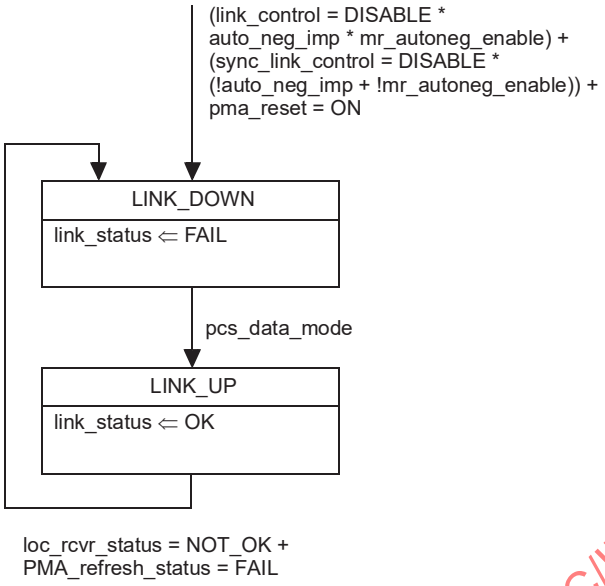
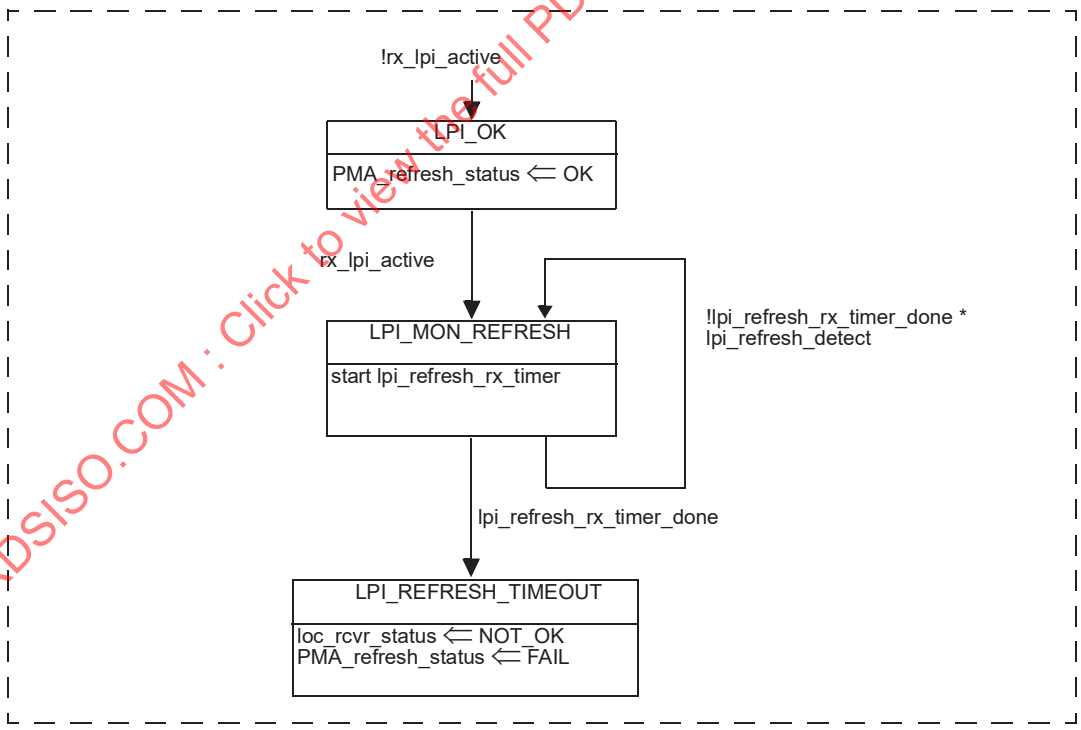


Figure 149–32—PHY Control state diagram



NOTE—The variables link_control and link_status are designated as link_control_mGigT1 and link_status_mGigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–7) if the optional Auto-Negotiation function is implemented.

Figure 149–33—Link Monitor state diagram



NOTE—This state diagram is only required when the PHY supports the EEE capability.

Figure 149–34—EEE Refresh monitor state diagram

149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 149–17. If MDIO is not implemented then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Table 149–17—MDIO management registers settings for test modes

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in MASTER mode.
011	Test mode 3—Precoder test mode.
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE PHYs are connected over a link segment defined in 149.7. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 175.78125 MHz.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous pattern of JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source.

Test mode 3 is for testing the precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the transmit precoder specified in 149.3.2.2.20, to be precoded according to the transmit precoder settings as determined by the value set in register 1.2313:10:9, or equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, the PHY shall transmit a continuous pattern of PRBS13Q (as specified in 120.5.11.2.1).

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 128 × *S* {+1} symbols followed by 128 × *S* {–1} symbols with the transmitted symbols timed from its local clock source. See Table 149–1 for the definition of *S*.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

149.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 149–35, Figure 149–36, Figure 149–37, and Figure 149–38, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

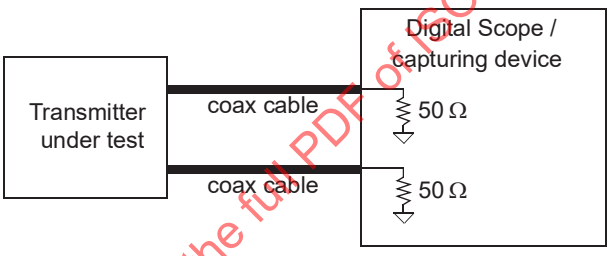


Figure 149–35—Transmitter test fixture 1 for transmitter droop measurement and transmitter linearity measurement

Figure 149–36—Transmitter test fixture 2 for MASTER and SLAVE clock jitter measurement

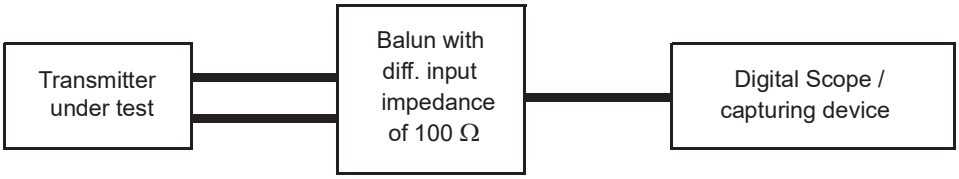


Figure 149–37—Transmitter test fixture 3 for MDI jitter measurement

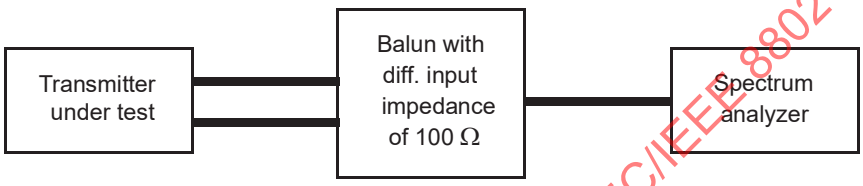


Figure 149–38—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement

149.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 149.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high DC common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

149.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 149–35, the magnitude of both the positive and negative droop shall be less than 15%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).

149.5.2.2 Transmitter linearity

With the transmitter in test mode 4 and using the transmitter test fixture 1 shown in Figure 149–35, the test defined in 120D.3.1.2 shall be performed. The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2. The transmitter SNDR distortion, as specified in 120D.3.1.6, shall exceed 38 dB in 10GBASE-T1, 36 dB in 5GBASE-T1, and 35 dB in 2.5G modes.

149.5.2.3 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 149–36.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 1/*S* ps. The peak-to-peak value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10/*S* ps. See Table 149–1 for the definition of *S*.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 2/*S* ps. The peak-to-peak value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 20/*S* ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

149.5.2.3.1 Transmit MDI random jitter in MASTER mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 149–18) and using test fixture 3 as shown in Figure 149–37. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than 1/*S* ps. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 10/*S* ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

Table 149–18—Jitter test modes

Bit 1.2313.1	Bit 1.2313.0	Test pattern
0	0	Square wave: TX_TCLK_175
0	1	JP03A (as specified in 94.2.9.1)
1	0	JP03B (as specified in 94.2.9.2)
1	1	Reserved

149.5.2.3.2 Transmit MDI deterministic jitter in MASTER mode

Jitter measurements in this subclause are performed with the transmitter enabled in MASTER timing mode in test mode 2, with the patterns as defined by Table 149–18, and timed with a local clock.

To measure the peak-to-peak deterministic jitter ($DJ_{pk\text{-}pk}$) follow the steps as specified in 94.3.12.6.1, with the following modifications to step 5:

$f_n = 1 \times S$ MHz, $T = 68 / S$ ns.

Using this method, $DJ_{pk\text{-}pk}$ shall be less than 9 / *S* ps.

To measure peak-to-peak even-odd jitter ($EOJ_{pk\text{-}pk}$) follow the steps as specified in 94.3.12.6.2.

Using this method, $EOJ_{pk\text{-}pk}$ shall be less than 4 / *S* ps. See Table 149–1 for the definition of *S*.

149.5.2.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power shall be in the range of –1 dBm to 2 dBm and the power spectral density of the transmitter, measured into a 100 Ω load using test fixture 4 shown in Figure 149–38 shall be between the upper and lower masks specified in Equation (149–14) and Equation (149–15). The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 149–39. See Table 149–1 for the definition of *S*.

$$UPSD(f) = \begin{cases} -90 - K & \text{dBm/Hz} \quad 0 < f \le 600 \times S \\ -89 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 600 \times S < f \le 3000 \times S \\ -82 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 3000 \times S < f \le 5500 \times S \end{cases} \tag{149–14}$$

$$LPSD(f) = \begin{cases} -96 - K & \text{dBm/Hz} \quad 5 < f \le 400 \times S \\ -95 - K - \dfrac{f}{400 \times S} & \text{dBm/Hz} \quad 400 \times S < f \le 2000 \times S \\ -90 - K - \dfrac{f}{200 \times S} & \text{dBm/Hz} \quad 2000 \times S < f \le 3000 \times S \end{cases} \tag{149–15}$$

where

f is the frequency in MHz

$$K = 10\log_{10}(S) \tag{149–16}$$

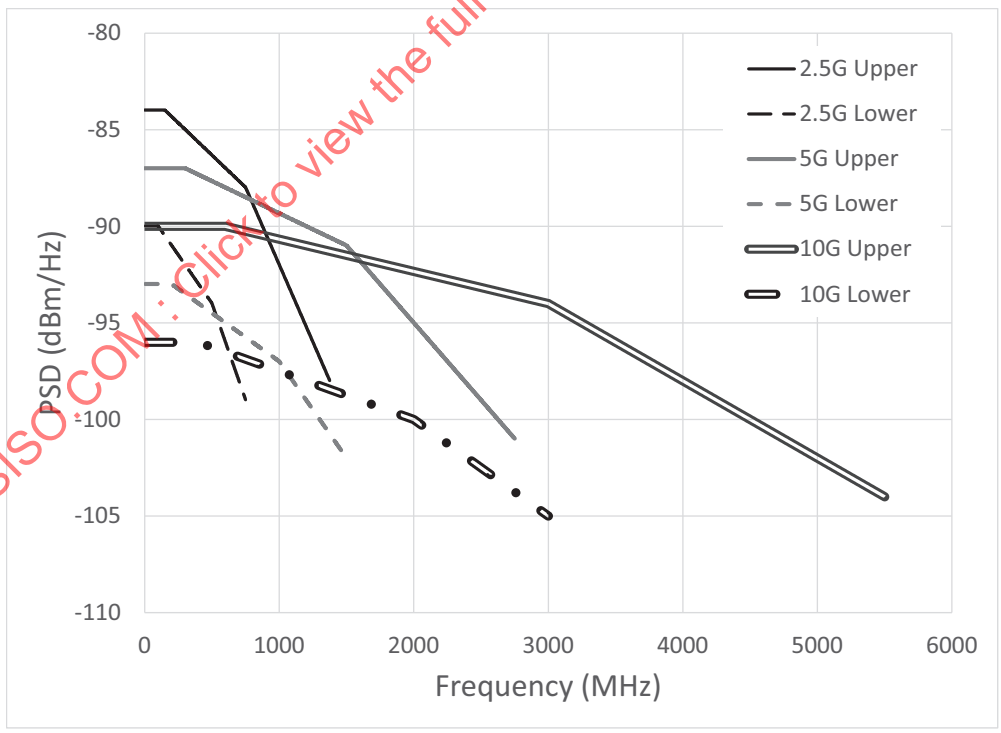


Figure 149–39—Transmitter power spectral density, upper and lower masks

149.5.2.5 Transmitter peak differential output

When measured with 100 Ω termination, the transmit differential signal at the MDI shall be less than 1.3 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

149.5.2.6 Transmitter clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 5625 × *S* MHz ± 50 ppm. See Table 149–1 for the definition of *S*.

For a MASTER PHY, when the transmitter is in the LPI transmit mode, the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

149.5.3 Receiver electrical specifications

The PMA provides the Receive function specified in 149.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 149.7.

149.5.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 149.5.2 and have passed through a link specified in 149.7 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

149.5.3.2 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 149–19. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 149–40, with a link segment as defined in 149.7. The BER is expected to be less than 10^{-12}, and to satisfy this specification the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

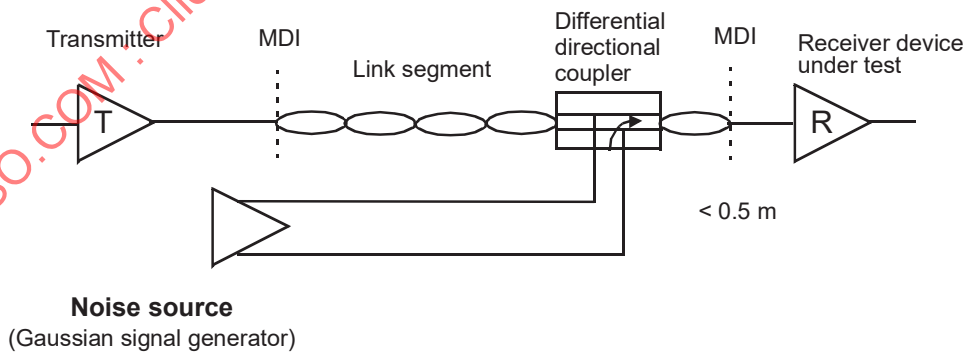


Figure 149–40—Alien crosstalk noise rejection test setup

Table 149–19—Alien crosstalk noise source

PHY type	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)
10GBASE-T1	3500	–152
5GBASE-T1	1750	–149
2.5GBASE-T1	875	–146

149.6 Management interface

2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 make extensive use of the management functions that may be provided by the optional MDIO (Clause 45), and the communication and self-configuration functions provided by the optional Auto-Negotiation (Clause 98).

149.6.1 Optional Support for Auto-Negotiation

If Auto-Negotiation is supported and enabled the mechanism described in Clause 98 shall be used.

Auto-Negotiation is performed as part of the initial setup of the link, and allows the PHYs at each end to advertise their capabilities and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1:

a) To negotiate that the PHY is capable of supporting 2.5GBASE-T1 transmission.
b) To negotiate that the PHY is capable of supporting 5GBASE-T1 transmission.
c) To negotiate that the PHY is capable of supporting 10GBASE-T1 transmission.
d) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

149.7 Link segment characteristics

2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 are designed to operate over a single shielded balanced pair of conductors that meet the requirements specified in this subclause. The single shielded balanced pair of conductors supports an effective data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in each direction simultaneously. The term *link segment* used in this clause refers to a single balanced pair of conductors (cable or backplane) operating in full duplex.

For the three different PHY types, link segment parameters are specified to different upper frequencies, given by the parameter F_{max} shown in Equation (149–17).

$$F_{max} = 4000 \times S \quad (149–17)$$

See Table 149–1 for the definition of *S*.

149.7.1 Link transmission parameters

The transmission characteristics for the MultiGBASE-T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

149.7.1.1 Insertion loss

The insertion loss of each MultiGBASE-T1 link segment shall meet the values determined using Equation (149–18).

$$Insertion\ loss(f) \le 0.002\,f + 0.68\sqrt{f} \quad \text{(dB)} \tag{149–18}$$

where

f is the frequency in MHz; $1 \le f \le F_{max}$

The insertion loss is illustrated in Figure 149–41.

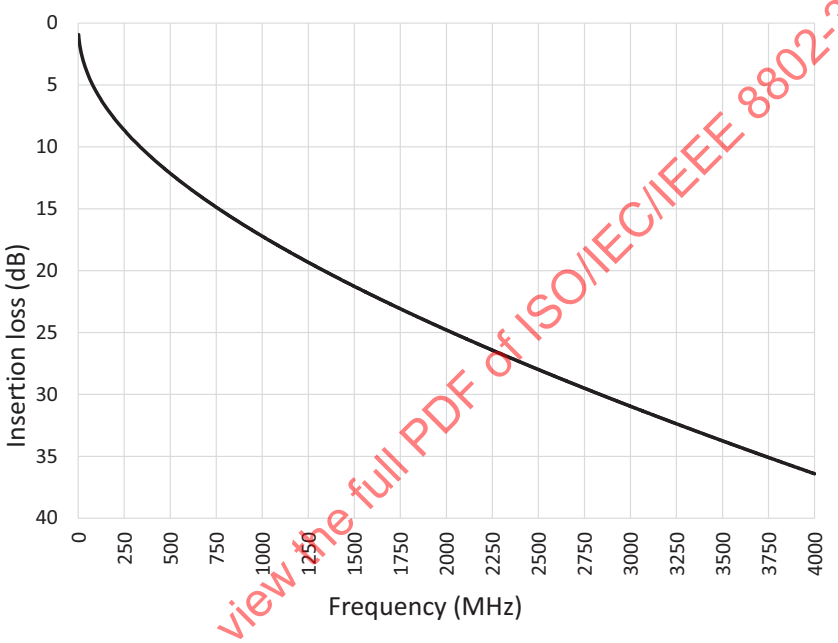


Figure 149–41—Insertion loss calculated using Equation (149–18)

149.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of the link segment is 100 Ω.

149.7.1.3 Return loss

149.7.1.3.1 2.5GBASE-T1 link segment return loss

In order to limit the noise at the receiver due to impedance mismatches each 2.5GBASE-T1 link segment shall meet the values determined by using Equation (149–19) at all frequencies from 1 MHz to 1000 MHz. The reference impedance for the return loss specification is 100 Ω.

$$2.5G\_Return\_Loss \ge \begin{cases} 20 & 1 \le f < 240 \\ 20 - 10\log_{10}(f/240) & 240 \le f \le 1000 \end{cases} \text{(dB)} \tag{149–19}$$

where

f is the frequency in MHz; $1 \le f \le 1000$

The 2.5GBASE-T1 return loss is illustrated in Figure 149–42.

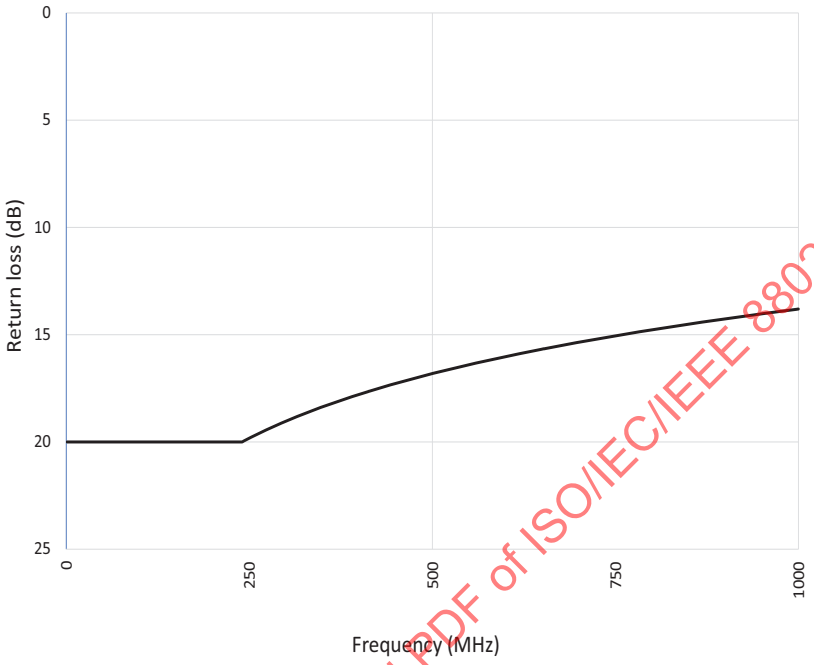


Figure 149–42—Return loss calculated using Equation (149–19)

149.7.1.3.2 5GBASE-T1 link segment return loss

In order to limit the noise at the receiver due to impedance mismatches each 5GBASE-T1 link segment shall meet the values determined by using Equation (149–20) at all frequencies from 1 MHz to 2000 MHz. The reference impedance for the return loss specification is 100 Ω. The return loss is dependent on the insertion loss at 1.5 GHz as determined by using Equation (149–21) to calculate N.

$$5G\_Return\_Loss \ge \begin{cases} 20 & 1 \le f < 480/2^N \\ 20 - 10\log_{10}((2^N \times f)/480) & 480/2^N \le f \le 2000 \end{cases} \text{(dB)} \qquad (149\text{–}20)$$

where

f is the frequency in MHz; $1 \le f \le 2000$

$$N = \begin{cases} 0 & 15 \text{ dB} < IL\ (1.5\ GHz) \\ 1 & IL\ (1.5\ GHz) \le 15 \text{ dB} \end{cases} \qquad (149\text{–}21)$$