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Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements —

Part 3: Standard for Ethernet

AMENDMENT 4: Physical layer specifications and management parameters for 1 Gb/s operation over a single twisted-pair copper cable

Technologies de l'information — Télécommunications et échange d'information entre systèmes — Réseaux locaux et métropolitains — Prescriptions spécifiques —

Partie 3: Norme pour Ethernet

AMENDEMENT 4: Spécifications des couches physiques et paramètres de gestion pour l'exploitation des interfaces à 1 Go/s sur un seul câble de cuivre à paires torsadées

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IEEE Std 802.3bp™-2016
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016, and
IEEE Std 802.3bq™-2016)

IEEE Standard for Ethernet

Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable

Sponsor

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 30 June 2016

IEEE-SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2015 adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single twisted-pair copper cable in an automotive application.

Keywords: 1000BASE-T1, Ethernet, IEEE 802®, IEEE 802.3™, IEEE 802.3bp™

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Introduction

This introduction is not part of IEEE Std 802.3bp™-2016, IEEE Standard for Ethernet—Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half-duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel, and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile), and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bp-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats, and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted-pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 109C, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable

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NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and <u>underscore</u> (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.[1]

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

[1]Notes in text, tables, and figures are given for information only, and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Insert the following references in alphanumeric order:

IEC 62153-4-14:2012, Metallic communication cable test methods—Part 4-14: Electromagnetic compatibility (EMC)—Coupling attenuation of cable assemblies (Field conditions) absorbing clamp method.

SAE J1292, Automobile and Motor Coach Wiring.

Change CISPR 25 reference, added in IEEE Std 802.3bw-2015, as follows:

IEC CISPR 25 ~~Edition 3.0 2008-03~~: Vehicles, boats and internal combustion engines—Radio disturbance characteristics—Limits and methods of measurement for the protection of on-board receivers.

1.4 Definitions

Insert the following new definition after 1.4.28 1000BASE-T:

1.4.28a 1000BASE-T1: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using a single twisted-pair copper cable. (See IEEE Std 802.3, Clause 97.)

Insert the following new definition after 1.4.99 anomaly:

1.4.99a AN half-duplex function: The ability to exchange Auto-Negotiation DME pages over a single differential-pair medium. (See IEEE Std 802.3, Clause 98.)

Insert the following new definition after 1.4.107 BASE-R:

1.4.107a BASE-T1: PHYs that belong to the set of specific Ethernet PCS/PMA/PMDs that operate on a single twisted-pair copper cable, including 100BASE-T1 and 1000BASE-T1. (See IEEE Std 802.3, Clause 96 and Clause 97.)

Insert the following new definition after 1.4.381 single-port device:

1.4.381a single twisted-pair copper cable: Two insulated conductors twisted together in a regular fashion to form a balanced transmission line.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

MDAFEXT	multiple disturber alien far-end crosstalk
MDANEXT	multiple disturber alien near-end crosstalk

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) after the entry for 1000BASE-T:

1000BASE-T1 Clause 97 1000 Mb/s PAM3

30.3.2.1.3 aPhyTypeList

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) after the entry for 1000BASE-T:

1000BASE-T1 Clause 97 1000 Mb/s PAM3

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016. and IEEE Std 802.3bq-2016) after the entry for 1000BASE-TFD:

1000BASE-T1 single twisted-pair copper cable PHY as specified in Clause 97

30.5.1.1.4 aMediaAvailable

Insert the following new text into the third paragraph of BEHAVIOUR DEFINED AS (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) after the third sentence inserted by IEEE Std 802.3bw:

For 1000BASE-T1, a link_status of OK maps to the enumeration "available". All other states of link_status map to the enumeration "not available".;

Change the fourth sentence of the third paragraph of BEHAVIOUR DEFINED AS (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) as follows:

Any MAU that implements management of Clause 28, ~~or~~ Clause 73, or Clause 98 Auto-Negotiation will map remote fault indication to MediaAvailable "remote fault."

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.3 aAutoNegRemoteSignaling

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, /C/ ordered sets (see 36.2.4.10) or DME signals (see 73.5 and 98.2.1.1) were received from the remote end.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) after the entry for 1000BASE-TFD:

1000BASE-T1 1000BASE-T1 as specified in Clause 97

Change the following entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) as follows:

Rem Fault Remote fault bit (RF) as specified in Clause 73 and Clause 98

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) after the entry for BASE-RFEC25G Req inserted by IEEE Std 802.3by-2016:

Force MS Force MASTER-SLAVE as specified in Clause 98 (see 98.2.1.2.5)

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

This indicates the technology ability of the local device, as defined in Clause 28, Clause 37, ~~and~~ Clause 73, and Clause 98.;

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

This GET-SET attribute maps to the technology ability of the local device, as defined in Clause 28, ~~and~~ Clause 37, and Clause 98.

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability Field of the last received

Auto- Negotiation link codeword(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0-D13 of the received Config_Reg Base Page (see 37.2.1). For Clause 73 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 73.6). For Clause 98 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 98.2.1.2).;

30.6.1.1.8 aAutoNegLocalSelectorAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

This indicates the value of the selector field of the local hardware. The Selector Field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation, in ~~and~~ 73.6.1 for Clause 73 Auto-Negotiation, and in 98.2.1.2.1 for Clause 98 Auto-Negotiation. The enumeration of the Selector Field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector Field of the Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".

30.6.1.1.10 aAutoNegReceivedSelectorAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. It maps to the Message Selector Field of the last received Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). For Clause 37 Auto- Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".;

34. Introduction to 1000 Mb/s baseband network

34.1 Overview

Insert a new subclause 34.1.5a after 34.1.5, with text on the support of Auto-Negotiation capability in 1000BASE-T1 PHY:

34.1.5a Auto-Negotiation, type 1000BASE-T1

Auto-Negotiation (Clause 98) may be used by 1000BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link start-up through the use of half-duplex differential Manchester encoding.

The use of Clause 98 Auto-Negotiation is optional for a 1000BASE-T1 PHY.

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the row for 1.2103 through 1.32767 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bw-2015) in Table 45-3 as follows (unchanged rows not shown)

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.2103 through 1.~~32767~~2303	Reserved	
1.2304	1000BASE-T1 PMA control	45.2.1.133
1.2305	1000BASE-T1 PMA status	45.2.1.134
1.2306	1000BASE-T1 training	45.2.1.135
1.2307	1000BASE-T1 link partner training	45.2.1.136
1.2308	1000BASE-T1 test mode control	45.2.1.137
1.2309 through 32767	Reserved	

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

45.2.1.6.3 PMA/PMD type selection (1.7.5:0)

Change definition of value 1 1 1 1 0 1 for bits 1.7.5:0 in Table 45–7 (as added by IEEE Std 802.3bw-2015) as follows (unchanged rows not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 1 1 0 1 = ~~100~~BASE-T1 PMA/PMD[b]	R/W

[a]R/W = Read/Write, RO = Read only
[b]If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.

45.2.1.14a BASE-T1 PMA/PMD extended ability register (1.18)

Change Table 45–17a (as added by IEEE Std 802.3bw-2015) as follows:

Table 45–17a—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:~~1~~2	Reserved	Value always 0	RO
1.18.1	1000BASE-T1 ability	1 = PMA/PMD is able to perform 1000BASE-T1 0 = PMA/PMD is not able to perform 1000BASE-T1	RO
1.18.0	100BASE-T1 ability	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1	RO

[a]RO = Read only

45.2.1.131 BASE-T1 PMA/PMD control register (Register 1.2100)

Change 45.2.1.131 (added by IEEE Std 802.3bw-2015) as follows:

The assignment of bits in the BASE-T1 PMA/PMD control register is shown in Table 45–98a.

Table 45–98a—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2100.15	~~MASTER-SLAVE manual config enable~~Reserved	Value always 1	RO
1.2100.14	MASTER-SLAVE config value	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE	R/W
1.2100.13:4	Reserved	Value always 0	RO
1.2100.3:0	Type ~~s~~Selection	3 2 1 0 1 x x x = Reserved~~ for future use~~ 0 1 x x = Reserved~~ for future use~~ 0 0 1 x = Reserved~~ for future use~~ 0 0 0 1 = ~~Reserved for future use~~1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

Delete 45.2.1.131.1 and renumber 45.2.1.131.2 and 45.2.1.131.3 to 45.2.1.131.1 and 45.2.1.131.2. Change renumbered 45.2.1.131.1 and 45.2.1.131.2 (as added by IEEE Std 802.3bw-2015) as follows:

~~45.2.1.131.1 BASE-T1 MASTER-SLAVE manual config enable (1.2100.15)~~

~~Bit 1.2100.15 returns a one to indicate that MASTER or SLAVE configuration is set manually.~~

45.2.1.131.1 ~~BASE-T1~~ MASTER-SLAVE config value (1.2100.14)

Bit 1.2100.14 is used to select MASTER or SLAVE operation when ~~MASTER-SLAVE manual config enable bit 1.2100.15 is set to one~~Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. If bit 1.2100.14 is set to one the PHY shall operate as MASTER. If bit 1.2100.14 is set to zero the PHY shall operate as SLAVE. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.131.2 ~~BASE-T1 t~~Type selection (1.2100.3:0)

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

Insert 45.2.1.133 through 45.2.1.137 after 45.2.1.132 (as inserted by IEEE Std 802.3bw-2015) as follows:

45.2.1.133 1000BASE-T1 PMA control register (Register 1.2304)

The assignment of bits in the 1000BASE-T1 PMA control register is shown in Table 45–98c.

Table 45–98c—1000BASE-T1 PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2304.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2304.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2304.13:12	Reserved	Value always 0	RO
1.2304.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2304.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.133.1 PMA/PMD reset (1.2304.15)

Resetting the 1000BASE-T1 PMA/PMD is accomplished by setting bit 1.2304.15 to a one. This action shall set all 1000BASE-T1 PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the 1000BASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 1000BASE-T1 PMA/PMD shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. The 1000BASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2304.15.

During a reset, the 1000BASE-T1 PMD/PMA shall respond to reads from register bits 1.2304.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 1.2304.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 1000BASE-T1 PMA/PMD.

45.2.1.133.2 Transmit disable (1.2304.14)

When bit 1.2304.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2304.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2304.14 is a copy of 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.133.3 Low power (1.2304.11)

When the low-power ability is supported, the 1000BASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2304.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 1000BASE-T1 PMA/PMD. The behavior of the 1000BASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2304.11 is zero.

This operation interrupts data communication. The data path of the 1000BASE-T1 PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2304.11 is a copy of 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 1000BASE-T1 PMA/PMD in low-power mode.

45.2.1.134 1000BASE-T1 PMA status register (Register 1.2305)

The assignment of bits in the 1000BASE-T1 PMA status register is shown in Table 45–98d.

45.2.1.134.1 1000BASE-T1 OAM ability (1.2305.11)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports 1000BASE-T1 OAM (see 97.3.8). When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support 1000BASE-T1 OAM.

45.2.1.134.2 EEE ability (1.2305.10)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports EEE. When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support EEE.

45.2.1.134.3 Receive fault ability (1.2305.9)

When read as a one, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

Table 45–98d—1000BASE-T1 PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2305.15:12	Reserved	Value always 0	RO
1.2305.11	1000BASE-T1 OAM Ability	1 = PHY has 1000BASE-T1 OAM ability 0 = PHY does not have 1000BASE-T1 OAM ability	RO
1.2305.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2305.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2305.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2305.7:3	Reserved	Value always 0	RO
1.2305.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2305.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2305.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching Low

45.2.1.134.4 Low-power ability (1.2305.8)

When read as a one, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD supports the low-power ability. When read as a zero, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD does not support the low-power feature. If the 1000BASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2304.11 or bit 1.0.11.

45.2.1.134.5 Receive polarity (1.2305.2)

When read as zero, bit 1.2305.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2305.2 indicates that the polarity of receiver is reversed.

45.2.1.134.6 Receive fault (1.2305.1)

When read as a one, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2305.9. The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.134.7 Receive link status (1.2305.0)

When read as a one, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.135 1000BASE-T1 training register (Register 1.2306)

The assignment of bits in the 1000BASE-T1 training register is shown in Table 45–98e.

Table 45–98e—1000BASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2306.15:11	Reserved	Value always 0	RO
1.2306.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2306.3:2	Reserved	Value always 0	RO
1.2306.1	1000BASE-T1 OAM advertisement	1 = 1000BASE-T1 OAM ability advertised to link partner 0 = 1000BASE-T1 OAM ability not advertised to link partner	R/W
1.2306.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.135.1 User field (1.2306.10:4)

This register is a user defined 7-bit field that is transmitted to the link partner during training.

45.2.1.135.2 1000BASE-T1 OAM advertisement (1.2306.1)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising 1000BASE-T1 OAM capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising 1000BASE-T1 OAM capability. This bit shall be set to 0 if the 1000BASE-T1 PHY does not support 1000BASE-T1 OAM.

45.2.1.135.3 EEE advertisement (1.2306.0)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising EEE capability. This bit shall be set to 0 if the 1000BASE-T1 PHY does not support EEE.

45.2.1.136 1000BASE-T1 link partner training register (Register 1.2307)

The assignment of bits in the 1000BASE-T1 link partner training register is shown in Table 45–98f. The values in this register are not valid until link is up.

Table 45–98f—1000BASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2307.15:11	Reserved	Value always 0	RO
1.2307.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2307.3:2	Reserved	Value always 0	RO
1.2307.1	Link partner 1000BASE-T1 OAM advertisement	1 = Link partner has 1000BASE-T1 OAM ability 0 = Link partner does not have 1000BASE-T1 OAM ability	RO
1.2307.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.136.1 Link partner user field (1.2307.10:4)

This register is a user defined 7-bit field that is received from the link partner during training.

45.2.1.136.2 Link partner 1000BASE-T1 OAM advertisement (1.2307.1)

When read as a one, this bit indicates the link partner is advertising 1000BASE-T1 OAM capability. When read as a zero, this bit indicates the link partner is not advertising 1000BASE-T1 OAM capability. 1000BASE-T1 OAM capability shall be enabled only when both the local device and its link partner are advertising 1000BASE-T1 OAM capability.

45.2.1.136.3 Link partner EEE advertisement (1.2307.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local device and its link partner are advertising EEE capability.

45.2.1.137 1000BASE-T1 test mode control register (Register 1.2308)

The assignment of bits in the 1000BASE-T1 test mode control register is shown in Table 45–98g. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.1.137.1 Test mode control (1.2308.15:13)

Transmitter test mode operations defined by bits 1.2307.15:13, are described in 97.5.2 and Table 97–12. The default value for bits 1.2308.15:13 is zero.

Table 45–98g—1000BASE-T1 test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2308.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	RO
1.2308.12:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.3 PCS Registers

Change reserved register space (3.1809 through 3.32767) in Table 45–119 as follows:

Table 45–119—PCS registers

Register address	Register name	Subclause
3.1809 through 3.~~32767~~2303	Reserved	
3.2304	1000BASE-T1 PCS control	45.2.3.51
3.2305	1000BASE-T1 PCS status 1	45.2.3.52
3.2306	1000BASE-T1 PCS status 2	45.2.3.53
3.2307	Reserved	
3.3208	1000BASE-T1 OAM transmit	45.2.3.54
3.2309 through 3.2312	1000BASE-T1 OAM message	45.2.3.55
3.2313	1000BASE-T1 OAM receive	45.2.3.56
3.2314 through 3.2317	Link partner 1000BASE-T1 OAM message	45.2.3.57
3.2318 through 3.32767	Reserved	

Insert new subclauses 45.2.3.51 through 45.2.3.57 after 45.2.3.50 as follows:

45.2.3.51 1000BASE-T1 PCS control register (Register 3.2304)

The assignment of bits in the 1000BASE-T1 PCS control register is shown in Table 45–163a. The default value for each bit of the 1000BASE-T1 PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–163a—1000BASE-T1 PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2304.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2304.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2304.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.51.1 PCS reset (3.2304.15)

Resetting the 1000BASE-T1 PCS is accomplished by setting bit 3.2304.15 to a one. This action shall set all 1000BASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the 1000BASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 1000BASE-T1 PCS shall return a value of one in bit 3.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. The 1000BASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2304.15. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2304.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2304.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 1000BASE-T1 PCS.

45.2.3.51.2 Loopback (3.2304.14)

The 1000BASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2304.14 is set to a one. When bit 3. 2304.14 is set to a one, the 1000BASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2304.14 is zero.

Bit 3.2304.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.52 1000BASE-T1 PCS status 1 register (Register 3.2305)

The assignment of bits in the 1000BASE-T1 PCS status 1 register is shown in Table 45–163b. All the bits in the 1000BASE-T1 PCS status 1 register are read only; a write to the 1000BASE-T1 PCS status 1 register shall have no effect.

Table 45–163b—1000BASE-T1 PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2305.15:12	Reserved	Value always 0	RO
3.2305.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2305.6:3	Reserved	Value always 0	RO
3.2305.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2305.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.52.1 Tx LPI received (3.2305.11)

When read as a one, bit 3.2305.11 indicates that the transmit 1000BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.11 indicates that the 1000BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.52.2 Rx LPI received (3.2305.10)

When read as a one, bit 3.2305.10 indicates that the receive 1000BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.10 indicates that the 1000BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.52.3 Tx LPI indication (3.2305.9)

When read as a one, bit 3.2305.9 indicates that the transmit 1000BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.9 indicates that the 1000BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.52.4 Rx LPI indication (3.2305.8)

When read as a one, bit 3.2305.8 indicates that the receive 1000BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.8 indicates that the 1000BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.52.5 Fault (3.2305.7)

When read as a one, bit 3.2305.7 indicates that the 1000BASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2305.7 indicates that the 1000BASE-T1 PCS has not detected a fault condition.

45.2.3.52.6 PCS receive link status (3.2305.2)

When read as a one, bit 3.2305.2 indicates that the 1000BASE-T1 PCS receive link is up. When read as a zero, bit 3.2305.2 indicates that the 1000BASE-T1 PCS receive link was down since the last read from this register. This bit is a latching low version of bit 3.2306.10. The PCS receive link status bit shall be implemented with latching low behavior.

45.2.3.53 1000BASE-T1 PCS status 2 register (Register 3.2306)

The assignment of bits in the 1000BASE-T1 PCS status 2 register is shown in Table 45–163c. All the bits in the 1000BASE-T1 PCS status 2 register are read only; a write to the 1000BASE-T1 PCS status 2 register shall have no effect.

Table 45–163c—1000BASE-T1 PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2306.15:11	Reserved	Value always 0	RO
3.2306.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2306.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2306.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2306.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2306.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2306.5:0	BER count	BER counter	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.53.1 Receive link status (3.2306.10)

When read as a one, bit 3.2306.10 indicates that the 1000BASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2306.10 indicates that the 1000BASE-T1 PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1.

45.2.3.53.2 PCS high BER (3.2306.9)

When read as a one, bit 3.2306.9 indicates that the 1000BASE-T1 PCS receiver is detecting a BER of $> 4 \times 10^{-4}$. When read as a zero, bit 3.2306.9 indicates that the 1000BASE-T1 PCS is not detecting a BER of $> 4 \times 10^{-4}$. This bit is a reflection of the state of the hi_rfer variable defined in 97.3.7.1.

45.2.3.53.3 PCS block lock (3.2306.8)

When read as a one, bit 3.2306.8 indicates that the 1000BASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2306.8 indicates that the 1000BASE-T1 PCS receiver has not achieved block lock. This bit is a reflection of the state of the block_lock variable defined in 97.3.7.1.

45.2.3.53.4 Latched high BER (3.2306.7)

When read as a one, bit 3.2306.7 indicates that the 1000BASE-T1 PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2306.7 indicates that the 1000BASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the 1000BASE-T1 PCS high BER status bit (3.2306.9).

45.2.3.53.5 Latched block lock (3.2306.6)

When read as a one, bit 3.2306.6 indicates that the 1000BASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2306.6 indicates that the 1000BASE-T1 PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 1000BASE-T1 PCS block lock status bit (3.2306.8).

45.2.3.53.6 BER count (3.2306.5:0)

The BER counter formed by bits 3.2306.5:0 is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the 1000BASE-T1 PCS status 2 register is read by the management function or upon execution of the 1000BASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.54 1000BASE-T1 OAM transmit register (Register 3.2308)

The assignment of bits in the 1000BASE-T1 OAM transmit register is shown in Table 45–163d.

Table 45–163d—1000BASE-T1 OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2308.15	1000BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self-clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2308.13	1000BASE-T1 OAM message received	This bit shall self clear on read. 1 = 1000BASE-T1 OAM message received by link partner 0 = 1000BASE-T1 OAM message not received by link partner	RO, LH
3.2308.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO

Table 45–163d—1000BASE-T1 OAM transmit register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.2308.11:8	Message number	User-defined message number to send	R/W
3.2308.7:4	Reserved	Value always 0	RO
3.2308.3	Ping received	Received PingTx value from latest good 1000BASE-T1 OAM frame received	RO
3.2308.2	Ping transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.54.1 1000BASE-T1 OAM message valid (3.2308.15)

Bit 3.2308.15 shall be set to 1 when the 1000BASE-T1 OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted. This register shall be cleared by the state machine to indicate whether the next 1000BASE-T1 OAM message can be written into the registers.

45.2.3.54.2 Toggle value (3.2308.14)

The state machine shall assign a value alternating between 0 and 1 to associate with the 8 octet 1000BASE-T1 OAM message transmit by the 1000BASE-T1 PHY. Bit 3.2308.14 should be read and recorded prior to setting 3.2308.15 to 1. The recorded value can be correlated with 3.2308.12 as a confirmation that the 1000BASE-T1 OAM message is received by the link partner.

45.2.3.54.3 1000BASE-T1 OAM message received (3.2308.13)

Bit 3.2308.13 shall indicate whether the most recently transmitted 1000BASE-T1 OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.54.4 Received message toggle value (3.2308.12)

Bit 3.2308.12 indicates the toggle bit value of the 1000BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2308.13 is 1.

45.2.3.54.5 Message number (3.2308.11:8)

The 1000BASE-T1 OAM message number to be transmitted. This field is user defined but is recommended that it be used to indicate the meaning of the 8 octet 1000BASE-T1 OAM message. If used this way, up to 16 different 8-octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.54.6 Ping received (3.2308.3)

Bit 3.2308.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.54.7 Ping transmit (3.2308.2)

Bit 3.2308.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.54.8 Local SNR (3.2308.1:0)

Bits 3.2308.1:0 are set by the 1000BASE-T1 PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.55 1000BASE-T1 OAM message register (Registers 3.2309 to 3.2312)

The 8-octet 1000BASE-T1 OAM message data to be transmitted. The 8-octet message data is user defined and its definition is outside the scope of this standard. See Table 45–163e.

Table 45–163e—1000BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2309.15:8	1000BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2309.7:0	1000BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2310.15:8	1000BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2310.7:0	1000BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2311.15:8	1000BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2311.7:0	1000BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2312.15:8	1000BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2312.7:0	1000BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

45.2.3.56 1000BASE-T1 OAM receive register (Register 3.2313)

The assignment of bits in the 1000BASE-T1 OAM receive register is shown in Table 45–163f.

45.2.3.56.1 Link partner 1000BASE-T1 OAM message valid (3.2313.15)

Bit 3.2313.15 shall be set to 1 when the 1000BASE-T1 OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8. This register shall be cleared when register 3.2317 is read.

45.2.3.56.2 Link partner toggle value (3.2313.14)

Bit 3.2313.14 indicates the toggle value associate with the 8 octet 1000BASE-T1 OAM message from the link partner.

Table 45–163f—1000BASE-T1 OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2313.15	Link partner 1000BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2313.14	Link partner toggle value	Toggle value received with message.	RO
3.2313.13:12	Reserved	Value always 0	RO
3.2313.11:8	Link partner message number	Message number from link partner	RO
3.2313.7:2	Reserved	Value always 0	RO
3.2313.1:0	Link partner SNR	00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.56.3 Link partner message number (3.2313.11:8)

The 1000BASE-T1 OAM message number from the link partner.

45.2.3.56.4 Link partner SNR (3.2313.1:0)

Bits 3.2313.1:0 indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.57 Link partner 1000BASE-T1 OAM message register (Registers 3.2314 to 3.2317)

The 8 octet 1000BASE-T1 OAM message data from the link partner. Register 3.2313.15 shall be cleared when register 3.2317 is read. See Table 45–163g.

Table 45–163g—Link partner 1000BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2314.15:8	Link partner 1000BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	RO
3.2314.7:0	Link partner 1000BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	RO
3.2315.15:8	Link partner 1000BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	RO
3.2315.7:0	Link partner 1000BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	RO
3.2316.15:8	Link partner 1000BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	RO
3.2316.7:0	Link partner 1000BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	RO
3.2317.15:8	Link partner 1000BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	RO
3.2317.7:0	Link partner 1000BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	RO

[a]RO = Read only

45.2.7 Auto-Negotiation registers

Change reserved register space (7.62 through 7.32767) in Table 45-200 as follows:

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.62 through 7.~~32 767~~511	Reserved	
7.512	BASE-T1 AN control	45.2.7.14c
7.513	BASE-T1 AN status	45.2.7.14d
7.514 through 7.516	BASE-T1 AN advertisement	45.2.7.14e
7.517 through 7.519	BASE-T1 AN LP Base Page ability	45.2.7.14f
7.520 through 7.522	BASE-T1 AN Next Page transmit	45.2.7.14g
7.523 through 7.525	BASE-T1 AN LP Next Page ability	45.2.7.14h
7.526 through 7.32767	Reserved	

Insert subclauses 45.2.7.14c through 45.2.7.14h (after 45.2.7.14b inserted by IEEE Std 802.3bq-2016) as follows:

45.2.7.14c BASE-T1 AN control register (Register 7.512)

The assignment of bits in the BASE-T1 AN control register is shown in Table 45–211c. The default value for each bit of the BASE-T1 AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–211c—BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.512.15	AN reset	1 = AN reset 0 = AN normal operation	R/W, SC
7.512.14:13	Reserved	Value always 0	RO
7.512.12	Auto-Negotiation enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
7.512.11:10	Reserved	Value always 0	RO
7.512.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported	R/W, SC
7.512.8:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.7.14c.1 AN reset (7.512.15)

Resetting AN is accomplished by setting bit 7.512.15 to a one. This action shall set all BASE-T1 AN registers to their default states. As a consequence, this action may change the internal state of AN and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise. AN is not required to accept a write transaction to any of its registers until the reset process is complete. The reset process shall be completed within 0.5 s from the setting of bit 7.512.15. During an AN reset, AN shall respond to reads from register bit 7.512.15. All other register bits shall be ignored.

The default value for bit 7.512.15 is zero.

NOTE—This operation may interrupt data communication.

45.2.7.14c.2 Auto-Negotiation enable (7.512.12)

The Auto-Negotiation function shall be enabled by setting bit 7.512.12 to a one. If bit 7.512.12 is set to one, then type selection bits 1.2100.3:0 and MASTER-SLAVE bits 1.2100.14 shall have no effect on the link configuration, and the Auto-Negotiation process determines the link configuration. If bit 7.512.12 is cleared to zero, then bits 1.2100.3:0 and bit 1.2100.14 determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

If the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, then the value of bit 7.512.12 shall be zero.

45.2.7.14c.3 Restart Auto-Negotiation (7.512.9)

If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD shall return a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 7.512.9 to one. This bit is self-clearing, and the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitialized. The Auto-Negotiation process shall not be affected by clearing this bit to zero.

The default value for 7.512.9 is zero.

45.2.7.14d BASE-T1 AN status (Register 7.513)

The assignment of bits in the BASE-T1 AN status register is shown in Table 45–211d. All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register shall have no effect.

Table 45–211d—BASE-T1 AN status register bit definitions

Bit(s)	Name	Description	R/W[a]
7.513.15:7	Reserved	Value always 0	RO
7.513.6	Page received	1 = A page has been received 0 = A page has not been received	RO, LH
7.513.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.513.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO, LH
7.513.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.513.2	Link status	1 = Link is up 0 = Link is down	RO, LL
7.513.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching High, LL = Latching Low

45.2.7.14d.1 Page received (7.513.6)

The Page received bit (7.513.6) shall be set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP Next Page ability registers 7.523 to 7.525. The contents of the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 are valid when bit 7.513.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the BASE-T1 AN status register (Register 7.513).

45.2.7.14d.2 Auto-Negotiation complete (7.513.5)

When read as a one, bit 7.513.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the Auto-Negotiation registers 7.514 to 7.516 and 7.517 to 7.519 are valid. When read as a zero, bit 7.513.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of 7.517 through 7.525 registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. The BASE-T1 PMA/PMD shall return a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12. The BASE-T1 PMA/PMD shall also return a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.

45.2.7.14d.3 Remote fault (7.513.4)

When read as one, bit 7.513.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is AN specific. The remote fault bit shall be implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and remain set until it is cleared. Bit 7.513.4 shall be cleared each time register 7.513 is read via the management interface, and shall also be cleared by a AN reset.

45.2.7.14d.4 Auto-Negotiation ability (7.513.3)

When read as a one, bit 7.513.3 indicates that the BASE-T1 PMA/PMD has the ability to perform BASE-T1 Auto-Negotiation. When read as a zero, bit 7.513.3 indicates that the BASE-T1 PMA/PMD lacks the ability to perform BASE-T1 Auto-Negotiation.

45.2.7.14d.5 Link status (7.513.2)

When read as a one, bit 7.513.2 indicates that the BASE-T1 PMA/PMD has determined that a valid link has been established. When read as a zero, bit 7.513.2 indicates that the link has been invalid after this bit was last read. Bit 7.513.2 is set to one when the variable link_status equals OK and is cleared to zero when the variable link_status equals FAIL. The link status bit shall be implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface. Bit 7.513.2 shall be cleared upon AN reset. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

45.2.7.14e BASE-T1 AN advertisement register (Registers 7.514, 7.515, and 7.516)

The assignment of bits in the BASE-T1 AN advertisement register is shown in Table 45–211e.

The Selector field (7.514.4:0) shall be set to the IEEE 802.3 code as specified in Annex 98A. The Acknowledge bit (7.514.14) is set to zero.

The technology ability field, as defined in 98.2.1.2, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.512.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.513.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP Base Page ability register to determine the highest common denominator technology.

The Base Page value is transferred to mr_adv_ability when register 7.514 is written. Therefore, registers 7.515 and 7.516 should be written before 7.514.

Table 45–211e—BASE-T1 AN advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
7.514.15	Next Page	See 98.2.1.2.9	R/W
7.514.14	Acknowledge	Value always 0	RO
7.514.13	Remote fault	See 98.2.1.2.7	R/W
7.514.12:5	D12:D5	See 98.2.1.2	R/W
7.514.4:0	Selector field	See Annex 98A	R/W
7.515.15:0	D31:D16	See 98.2.1.2	R/W
7.516.15:0	D47:D32	See 98.2.1.2	R/W

[a]RO = Read only, R/W = Read/Write

45.2.7.14f BASE-T1 AN LP Base Page ability register (Registers 7.517, 7.518, and 7.519)

The assignment of bits in the BASE-T1 AN LP Base Page ability register is shown in Table 45–211f.

All of the bits in the BASE-T1 AN LP Base Page ability register are read only. A write to the BASE-T1 AN LP Base Page ability register shall have no effect.

The value of the registers 7.518 and 7.519 is latched when register 7.517 is read and reads of registers 7.518 and 7.519 return the latched value rather than the current value.

Table 45–211f—BASE-T1 AN LP Base Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.517.15:0	D15:D0	See 98.2.1.2	RO
7.518.15:0	D31:D16	See 98.2.1.2	RO
7.519.15:0	D47:D32	See 98.2.1.2	RO

[a]RO = Read only

45.2.7.14g BASE-T1 AN Next Page transmit register (Registers 7.520, 7.521, and 7.522)

The assignment of bits in the BASE-T1 AN Next Page transmit register is shown in Table 45–211g.

The register contains the BASE-T1 AN Next Page link codeword as defined in 98.2.4.3.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Next Page Message Code that the device intends to transmit. The BASE-T1 AN shall use Next Page Message Codes as defined in Annex 98C.

A write to register 7.521 or 7.522 does not set mr_next_page_loaded. Only a write to register 7.520 sets mr_next_page_loaded true as described in 98.5.1. Therefore registers 7.521 and 7.522 should be written before register 7.520.

Table 45–211g—BASE-T1 AN Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.520.15	Next page	See 98.2.4.3	R/W
7.520.14	Reserved	Value always 0	RO
7.520.13	Message page	See 98.2.4.3	R/W
7.520.12	Acknowledge 2	See 98.2.4.3	R/W
7.520.11	Toggle	See 98.2.4.3	RO
7.520.10:0	Message/Unformatted code field	See 98.2.4.3	R/W
7.521.15:0	Unformatted code field 1	See 98.2.4.3	R/W
7.522.15:0	Unformatted code field 2	See 98.2.4.3	R/W

[a]RO = Read only, R/W = Read/Write

45.2.7.14h BASE-T1 AN LP Next Page ability register (Registers 7.523, 7.524, and 7.525)

BASE-T1 AN LP Next Page ability register (registers 7.523, 7.524, and 7.525) store BASE-T1 link partner Next Pages as shown in Table 45–211h. All of the bits in the BASE-T1 AN LP Next Page ability register are read only. A write to the BASE-T1 AN LP Next Page ability register shall have no effect.

Table 45–211h—BASE-T1 AN LP Next Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.523.15	Next Page	See 98.2.4.3	RO
7.523.14	Acknowledge	See 98.2.4.3	RO
7.523.13	Message page	See 98.2.4.3	RO
7.523.12	Acknowledge 2	See 98.2.4.3	RO
7.523.11	Toggle	See 98.2.4.3	RO
7.523.10:0	Message/Unformatted code field	See 98.2.4.3	RO
7.524.15:0	Unformatted code field 1	See 98.2.4.3	RO
7.525.15:0	Unformatted code field 2	See 98.2.4.3	RO

[a]RO = Read only

The value of registers 7.524 and 7.525 is latched when register 7.523 is read and reads of registers 7.524 and 7.525 return the latched value rather than the current value.

NOTE—If this register is used to store multiple link partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Next Pages.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[2]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.3 PMA/PMD management functions

Insert PICS items MM130 through MM149 at the bottom of the table in 45.5.3.3 (as modified by IEEE Std 802.3bw-2015 and IEEE Std 802.3by-2016) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MM130	A reset sets all 1000BASE-T1 PMA/PMD registers to their default states	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM131	1000BASE-T1 PMA/PMD returns a one in bit 1.2304.15 when a reset is in progress	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM132	1000BASE-T1 PMA/PMD returns a zero in bit 1.2304.15 when a reset is complete	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM133	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2304.15	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM134	During a reset, the 1000BASE-T1 PMD/PMA responds to reads from register bits 1.2304.15, 1.8.15:14, and 1.0.15.	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM135	During a reset, the 1000BASE-T1 PMD/PMA register bits are ignored.	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM136	Setting either 1.2304.15 or 1.0.15 resets the 1000BASE-T1 PMA/PMD.	45.2.1.133.1		PMA:M	Yes [ ] N/A [ ]
MM137	When bit 1.2304.14 is set to a one, the PMA disables output on the transmit path.	45.2.1.133.2		PMA:M	Yes [ ] N/A [ ]
MM138	When bit 1.2304.14 is set to a zero, the PMA enables output on the transmit path.	45.2.1.133.2		PMA:M	Yes [ ] N/A [ ]
MM139	Setting either bit 1.2304.14 or 1.9.0 disables the 1000BASE-T1 PMA transmit path.	45.2.1.133.2		PMA:M	Yes [ ] N/A [ ]

[2] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Value/Comment	Status	Support
MM140	While in the low-power mode, the device, as a minimum, responds to management transactions necessary to exit the low-power mode.	45.2.1.133.3		PMA:M	Yes [ ] N/A [ ]
MM141	Setting either 1.2304.11 or 1.0.11 puts the 1000BASE-T1 PMA/PMD in low-power mode.	45.2.1.133.3		PMA:M	Yes [ ] N/A [ ]
MM142	The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2305.1.	45.2.1.134.6		PMA:M	Yes [ ] N/A [ ]
MM143	Bit 1.2305.0 is implemented with latching low behavior.	45.2.1.134.6		PMA:M	Yes [ ] N/A [ ]
MM144	Bit 1.2306.1 is set to 0 if the 1000BASE-T1 PHY does not support OAM.	45.2.1.135.2		PMA:M	Yes [ ] N/A [ ]
MM145	Bit 1.2306.0 is set to 0 if the 1000BASE-T1 PHY does not support EEE.	45.2.1.135.3		PMA:M	Yes [ ] N/A [ ]
MM146	OAM capability is enabled only when both the 1000BASE-T1 PHY and link partner are advertising OAM capability.	45.2.1.136.2		PMA:M	Yes [ ] N/A [ ]
MM147	EEE capability is enabled only when both the 1000BASE-T1 PHY and link partner are advertising EEE capability	45.2.1.136.3		PMA:M	Yes [ ] N/A [ ]
MM148	Bit 1.2100.14 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.	45.2.1.131.1		PMA:M	Yes [ ] N/A [ ]
MM149	Bits 1.2100.3:0 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.	45.2.1.131.2		PMA:M	Yes [ ] N/A [ ]

45.5.3.7 PCS management functions

Insert PICS items RM107 through RM136, as follows, at the bottom of the table:

Item	Feature	Subclause	Value/Comment	Status	Support
RM107	This action sets all 1000BASE-T1 PCS registers to their default states.	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM108	Bit 3.2304.15 is self-clearing, and the 1000BASE-T1 PCS returns a value of one in bit 3.2304.15 when a reset is in progress.	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM109	Otherwise, bit 3.2304.15 returns a value of zero	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM110	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2304.15.	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM111	During a reset, the 1000BASE-T1 PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2304.15.	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM112	All other register bits are ignored during a reset.	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM113	Setting either bit 3.2304.15 or 3.0.15 resets the 1000BASE-T1 PCS.	45.2.3.51.1		PCS:M	Yes [ ] N/A [ ]
RM114	The 1000BASE-T1 PCS is placed in a loopback mode of operation when bit 3.2304.14 is set to a one.	45.2.3.51.2		PCS:M	Yes [ ] N/A [ ]
RM115	When bit 3. 2304.14 is set to a one, the 1000BASE-T1 PCS accepts data on the transmit path and return it on the receive path.	45.2.3.51.2		PCS:M	Yes [ ] N/A [ ]
RM116	Setting either bit 3.2304.14 or 3.0.14 enables loopback.	45.2.3.51.2		PCS:M	Yes [ ] N/A [ ]
RM117	All the bits in the 1000BASE-T1 PCS status 1 register are read only; a write to the 1000BASE-T1 PCS status 1 register has no effect.	45.2.3.52		PCS:M	Yes [ ] N/A [ ]
RM118	Bit 3.2305.11 is implemented with latching high behavior.	45.2.3.52.1		PCS:M	Yes [ ] N/A [ ]
RM119	Bit 3.2305.10 is implemented with latching high behavior.	45.2.3.52.2		PCS:M	Yes [ ] N/A [ ]
RM120	All the bits in the 1000BASE-T1 PCS status 2 register are read only; a write to the 1000BASE-T1 PCS status 2 register has no effect.	45.2.3.53		PCS:M	Yes [ ] N/A [ ]
RM121	Bit 3.2306.7 is implemented with latching high behavior.	45.2.3.53.4		PCS:M	Yes [ ] N/A [ ]
RM122	Bit 3.2306.6 is implemented with latching low behavior.	45.2.3.53.5		PCS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM123	Bits 3.2306.5:0 are reset to all zeros when the 1000BASE-T1 PCS status 2 register is read by the management function or upon execution of the 1000BASE-T1 PCS reset.	45.2.3.53.6		PCS:M	Yes [ ] N/A [ ]
RM124	Bits 3.2306.5:0 are held at all ones in the case of overflow.	45.2.3.53.6		PCS:M	Yes [ ] N/A [ ]
RM125	Bit 3.2308.15 is set to 1 when the OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted.	45.2.3.54.1		PCS:M	Yes [ ] N/A [ ]
RM126	Register 3.2308 is cleared by the state machine to indicate whether the next OAM message can be written into the registers.	45.2.3.54.1		PCS:M	Yes [ ] N/A [ ]
RM127	The state machine assigns a value alternating between 0 and 1 to associate with the 8 octet OAM message transmit by the 1000BASE-T1 PHY.	45.2.3.54.2		PCS:M	Yes [ ] N/A [ ]
RM128	Bit 3.2308.14 is read and recorded prior to setting 3.2308.15 to 1.	45.2.3.54.2		PCS:O	Yes [ ] No [ ]
RM129	Bit 3.2308.15 self clears when registers are loaded by the state machine.	45.2.3.54		PCS:M	Yes [ ] N/A [ ]
RM130	Bit 3.2308.14 self clears on read.	45.2.3.54		PCS:M	Yes [ ] N/A [ ]
RM131	Bit 3.2308.13 indicates whether the most recently transmitted OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner.	45.2.3.54.3		PCS:M	Yes [ ] N/A [ ]
RM132	Bit 3.2308.13 clears on read.	45.2.3.54.3		PCS:M	Yes [ ] N/A [ ]
RM133	Bit 3.2313.15 is set to 1 when the OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8.	45.2.3.56.1		PCS:M	Yes [ ] N/A [ ]
RM134	Register 3.2313 is cleared when register 3.2317 is read.	45.2.3.56.1		PCS:M	Yes [ ] N/A [ ]
RM135	Bit 3.2313.15 self clears when register 3.2317 is read.	45.2.3.56		PCS:M	Yes [ ] N/A [ ]
RM136	Register 3.2313.15 is cleared when register 3.2317 is read.	45.2.3.57		PCS:M	Yes [ ] N/A [ ]

45.5.3.9 Auto-Negotiation management functions

Insert PICS items AM65 through AM89 at the bottom of the table in 45.5.3.9 (as modified by IEEE Std 802.3bq-2016) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
AM65	Setting bit 7.512.15 to a one sets all BASE-T1 AN registers to their default states.	45.2.7.14c.1		AN:M	Yes [ ] N/A [ ]
AM66	Bit 7.512.15 is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise.	45.2.7.14c.1		AN:M	Yes [ ] N/A [ ]
AM67	The reset process is completed within 0.5 s from the setting of bit 7.512.15.	45.2.7.14c.1		AN:M	Yes [ ] N/A [ ]
AM68	During an AN reset, AN responds to reads from register bit 7.512.15.	45.2.7.14c.1		AN:M	Yes [ ] N/A [ ]
AM69	All other register bits are ignored.	45.2.7.14c.1		AN:M	Yes [ ] N/A [ ]
AM70	The Auto-Negotiation function is enabled by setting bit 7.512.12 to a one.	45.2.7.14c.2		AN:M	Yes [ ] N/A [ ]
AM71	If bit 7.512.12 is set to one, then PHY type bits 1.2100.3:0 and MASTER-SLAVE bits 1.2100.14 has no effect on the link configuration, and the Auto-Negotiation process determines the link configuration.	45.2.7.14c.2		AN:M	Yes [ ] N/A [ ]
AM72	If the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, then the value of bit 7.512.12 is zero.	45.2.7.14c.2		AN:M	Yes [ ] N/A [ ]
AM73	If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD returns a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 are ignored.	45.2.7.14c.3		AN:M	Yes [ ] N/A [ ]
AM74	Otherwise, the Auto-Negotiation process is restarted by setting bit 7.512.9 to one.	45.2.7.14c.3		AN:M	Yes [ ] N/A [ ]
AM75	Bit 7.512.9 is self-clearing, and the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated.	45.2.7.14c.3		AN:M	Yes [ ] N/A [ ]
AM76	If Auto-Negotiation was completed prior to this bit being set, the process is reinitialized.	45.2.7.14c.3		AN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
AM77	The Auto-Negotiation process is affected by clearing this bit to zero.	45.2.7.14c.3		AN:M	Yes [ ] N/A [ ]
AM78	All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register has no effect.	45.2.7.14d		AN:M	Yes [ ] N/A [ ]
AM79	The Page received bit (7.513.6) is set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP Next Page ability registers 7.523 to 7.525.	45.2.7.14d.1		AN:M	Yes [ ] N/A [ ]
AM80	The Page received bit is reset to zero on a read of the BASE-T1 AN status register (Register 7.513).	45.2.7.14d.1		AN:M	Yes [ ] N/A [ ]
AM81	The BASE-T1 PMA/PMD returns a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12.	45.2.7.14d.2		AN:M	Yes [ ] N/A [ ]
AM82	The BASE-T1 PMA/PMD also returns a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.	45.2.7.14d.2		AN:M	Yes [ ] N/A [ ]
AM83	The remote fault bit is implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and remain set until it is cleared.	45.2.7.14d.3		AN:M	Yes [ ] N/A [ ]
AM84	Bit 7.513.4 is cleared each time register 7.513 is read via the management interface, and is also cleared by a AN reset.	45.2.7.14d.3		AN:M	Yes [ ] N/A [ ]
AM85	The link status bit is implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface.	45.2.7.14d.5		AN:M	Yes [ ] N/A [ ]
AM86	Bit 7.513.2 is cleared upon AN reset.	45.2.7.14d.5		AN:M	Yes [ ] N/A [ ]
AM87	A write to the BASE-T1 AN LP Base Page ability register has no effect.	45.2.7.14f		AN:M	Yes [ ] N/A [ ]
AM88	On power-up or AN reset, registers 7.520, 7.521, and 7.522 contain the default value, which represents a Message Page with the message code set to Null Message.	45.2.7.14g		AN:M	Yes [ ] N/A [ ]
AM89	A write to the BASE-T1 AN LP Next Page ability register has no effect.	45.2.7.14h		AN:M	Yes [ ] N/A [ ]

78. Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.3 Reconciliation sublayer operation

78.1.3.3 PHY LPI operation

78.1.3.3.1 PHY LPI transmit operation

Change the second paragraph of 78.1.3.3.1, adding references to 1000BASE-T1 PHY, as follows:

The EEE capability in most PHYs ~~(for example, 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KR, and 10GBASE-KX4)~~ requires the local PHY transmitter to go quiet after sleep is signal~~l~~ed.

Insert a row for 1000BASE-T1 between 1000BASE-T and XGXS (XAUI) in Table 78–1 as follows (unchanged rows not shown):

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
...	...
1000BASE-T1	97
...	...

78.2 LPI mode timing parameters description

Insert a row for 1000BASE-T1 between 1000BASE-T and XGXS (XAUI) in Table 78–2 as follows (unchanged rows not shown):

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY or interface type	T_s (μs)		T_q (μs)		T_r (μs)	
	Min	Max	Min	Max	Min	Max
...	...	...	...	...	...	...
1000BASE-T1	3.6	3.6	84.95	84.97	1.44	1.44
...	...	...	...	...	...	...

78.5 Communication link access latency

Insert a row (and footnote) for 1000BASE-T1 after 1000BASE-T in Table 78–4 (as modified by IEEE Std 802.3by-2016) as follows (unchanged rows not shown):

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (µs)	T_{w_phy} (min) (µs)	$T_{phy\_shrink\_tx}$ (max) (µs)	$T_{phy\_shrink\_rx}$ (max) (µs)	$T_{w\_sys\_rx}$ (min) (µs)
...	...	...	...	...	...	...
1000BASE-T1		10.8	10.8	10.8	0[a]	0[a]
...	...	...	...	...	...	...

[a]All data transmission in 1000BASE-T1 PHY is synchronized to the PHY frame boundary. As such, the EEE function in the 1000BASE-T1 PHY is expected to assert the wake signal only at specific moments of time, aligned to PHY frame boundaries, and no shrinkage or delay at the RX side is expected.

Insert new clauses, Clause 97 and Clause 98, and corresponding Annexes 97A to 97B and 98A, 98B, and 98C, as follows:

97. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1

97.1 Overview

This clause defines the type 1000BASE-T1 Physical Coding Sublayer (PCS) and type 1000BASE-T1 Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 1000BASE-T1 Physical Layer (PHY). Provided in this clause are fully functional and electrical specifications for the type 1000BASE-T1 PCS and PMA.

The 1000BASE-T1 PHY is one of the Gigabit Ethernet family of high-speed full-duplex PHY specifications, capable of operating at 1000 Mb/s. The 1000BASE-T1 PHY is intended to be operated over a single twisted-pair copper cable, referred to as an *automotive link segment* (Type A) or *optional link segment* (Type B), defined in 97.6. The automotive link segment specifications defined in 97.6 may also be used for other applications that have similar link segment requirements. The cabling supporting the operation of the 1000BASE-T1 PHY is defined in terms of performance requirements between the attachment points [Medium Dependent Interface (MDI)], allowing implementers to provide their own cabling to operate the 1000BASE-T1 PHY as long as the normative requirements included in this clause are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 1000BASE-T1 that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

97.1.1 Relationship of 1000BASE-T1 to other standards

The relationship between the 1000BASE-T1 PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure 97–1. The PHY sublayers (shown shaded) in Figure 97–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 1000BASE-T1 is defined in Clause 98. GMII is defined in Clause 35.

97.1.2 Operation of 1000BASE-T1

The 1000BASE-T1 PHY operates using full-duplex communications over a single twisted-pair copper cable with an effective rate of 1 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive and industrial environments. The PHY supports operation on two types of link segments:

a) An automotive link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 15 m (referred to as *link segment type A*)
b) An optional link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 40 m to support applications requiring extended physical reach, such as industrial and automation controls and transportation (aircraft, railway, bus and heavy trucks). This link segment is referred to as *link segment type B*.

The 1000BASE-T1 PHY utilizes 3 level Pulse Amplitude Modulation (PAM3) transmitted at a 750 MBd rate. A 15-bit scrambler is used to improve the EMC performance. GMII TX_D, TX_EN, and TX_ER are encoded together using 80B/81B encoding, where 10 cycles of GMII data and control are encoded together in 81 bits to reduce the overhead. To maintain a bit error ratio (BER) of less than or equal to 10^{-10}, the 1000BASE-T1 PHY adds 396 bits of Reed-Solomon Forward Error Correction (RS-FEC) parity to each group of 45 80B/81B blocks (containing 450 octets of GMII data). The PAM3 mapping, scrambler, RS-FEC, and 80B/81B encoder/decoder are all contained in the PCS (see 97.3).

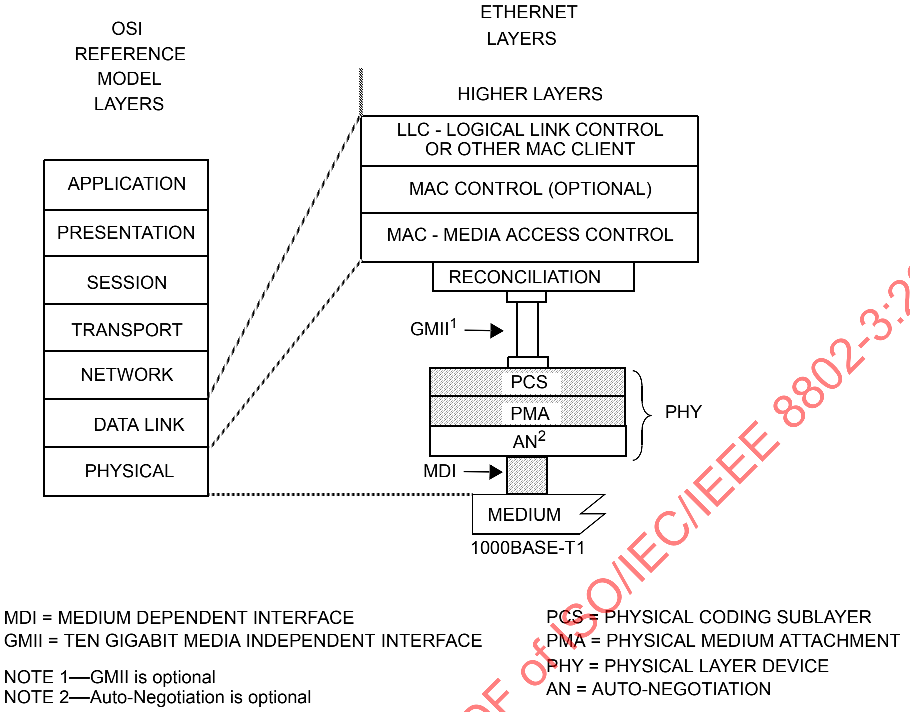


Figure 97–1—Relationship of 1000BASE-T1 PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

Auto-Negotiation (Clause 98) may optionally be used by 1000BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link start-up through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

A 1000BASE-T1 PHY shall be capable of operating as MASTER or SLAVE, per runtime configuration. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs. The MASTER and SLAVE are synchronized by a PHY Link Synchronization function in the PHY (see 97.4.2.6).

A 1000BASE-T1 PHY may optionally support Energy-Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 97.4.2.4.5. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization.

The 1000BASE-T1 PHY may optionally support the 1000BASE-T1 PCS-based Operations, Administration, and Maintenance (OAM). The 1000BASE-T1 OAM is useful for monitoring link operation by exchanging PHY link health status and messages. The 1000BASE-T1 OAM information is exchanged between two 1000BASE-T1 PHYs out-of-band. The 1000BASE-T1 OAM is specified in 97.3.8, and the 1000BASE-T1 PHY advertises its 1000BASE-T1 OAM capability as described in 97.4.2.4.5.

The 1000BASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 750 MBd over the single twisted-pair copper cable. PMA functionality is described in 97.4. The MDI is specified in 97.7.

97.1.2.1 Physical Coding Sublayer (PCS)

The 1000BASE-T1 PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to a Physical Medium Attachment (PMA) sublayer, described in 97.4, which supports communication over a single twisted-pair copper cable.

The PCS comprises the PCS Reset function, PCS Transmit, and PCS Receive. After completion of the Reset function, the Transmit and Receive functions start immediately and run simultaneously.

The PCS operates in two modes: the data mode and the training mode. In the data mode, the PCS Transmit function data path starts with the GMII interface, where TXD, TX_EN, and TX_ER input data to the PCS every 8 ns (as clocked by GTX_CLK). Data and control from ten GTX_CLK cycles are 80B/81B encoded into an 81-bit “81B block” that encodes every possible combination of data and control (control signals include transmit error propagation, receive error, assert low power idle, and inter-frame signaling, as defined in 35.2.1.6). Each set of 45 80B/81B blocks along with 9 bits of 1000BASE-T1 OAM data (see 97.3.8) is processed by an RS-FEC encoder. The RS-FEC encoder adds 396 RS-FEC parity bits and the resulting 4050 bits (45 80B/81B blocks = 3645 bits, 9 bits of 1000BASE-T1 OAM, and 396 bits of FEC parity bits) are scrambled using a 15-bit side-stream scrambler. The 4050 bits are referred to interchangeably as a *PHY frame* or as a *Reed-Solomon frame*. Each group of 3 bits of the scrambled data is converted to 2 PAM3 symbols by the 3B2T mapper (the 4050 bits in the PHY frame become 2700 PAM3 symbols) and passed to the PMA. PCS transmit functions are described in 97.3.2.2.

In the data mode, the PCS Receive function data path operates in the opposite order as the transmit path. The incoming PAM3 symbols are synchronized to PHY frame boundaries. Within each PHY frame, each two PAM3 symbols are demapped to 3 bits by the 3B2T demapper (the 2700 PAM3 symbols are converted to 4050 bits). The data is then descrambled and passed to the RS-FEC decoder for data validation and correction. Finally, each of the 45 80B/81B blocks is 80B/81B decoded into GMII data or control. The PCS data mode receive is described in 97.3.2.3.

In the training mode (see 97.4.2.4), the PCS transmits and receives PAM2 training sequences to synchronize to the PHY frame, learns the data mode scrambler seed, and exchanges EEE and 1000BASE-T1 OAM capabilities. The training mode uses PAM2 encoding.

97.1.2.2 Physical Medium Attachment (PMA) sublayer

The 1000BASE-T1 PMA transmits/receives symbol streams to/from the PCS onto the single balanced twisted-pair and provides the clock recovery, link monitor, and the 1000BASE-T1 PHY Control function. The PMA provides full duplex communications at 750 MBd.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the start-up functions required for successful 1000BASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

The minimum link segment characteristics, EMC requirements, and test modes are specified in 97.5.

97.1.2.3 EEE capability

A 1000BASE-T1 PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter the LPI mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode shall not cause any MAC frames to be lost or corrupted.

In the transmit direction the transition to the LPI transmit mode begins when the PCS transmit function detects an "Assert Low Power Idle" condition on the GMII in the last 80B/81B block of a PHY frame. At the next PHY frame aligned to the wake window the PCS transmits a sleep signal composed of an entire PHY frame containing only LP_IDLE. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep frame, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that may be used by the link partner to update adaptive filters and timing circuits. LPI mode may begin with quiet signaling, a full refresh period, or a wake frame. The quiet-refresh cycle continues until the PCS function detects a condition that is not Assert Low Power Idle on the GMII. This condition signals to the PHY that the LPI transmit mode should end. At the next PHY frame the PCS transmits a wake frame composed of an entire PHY frame containing only Idle. On the next PHY frame normal power mode shall resume.

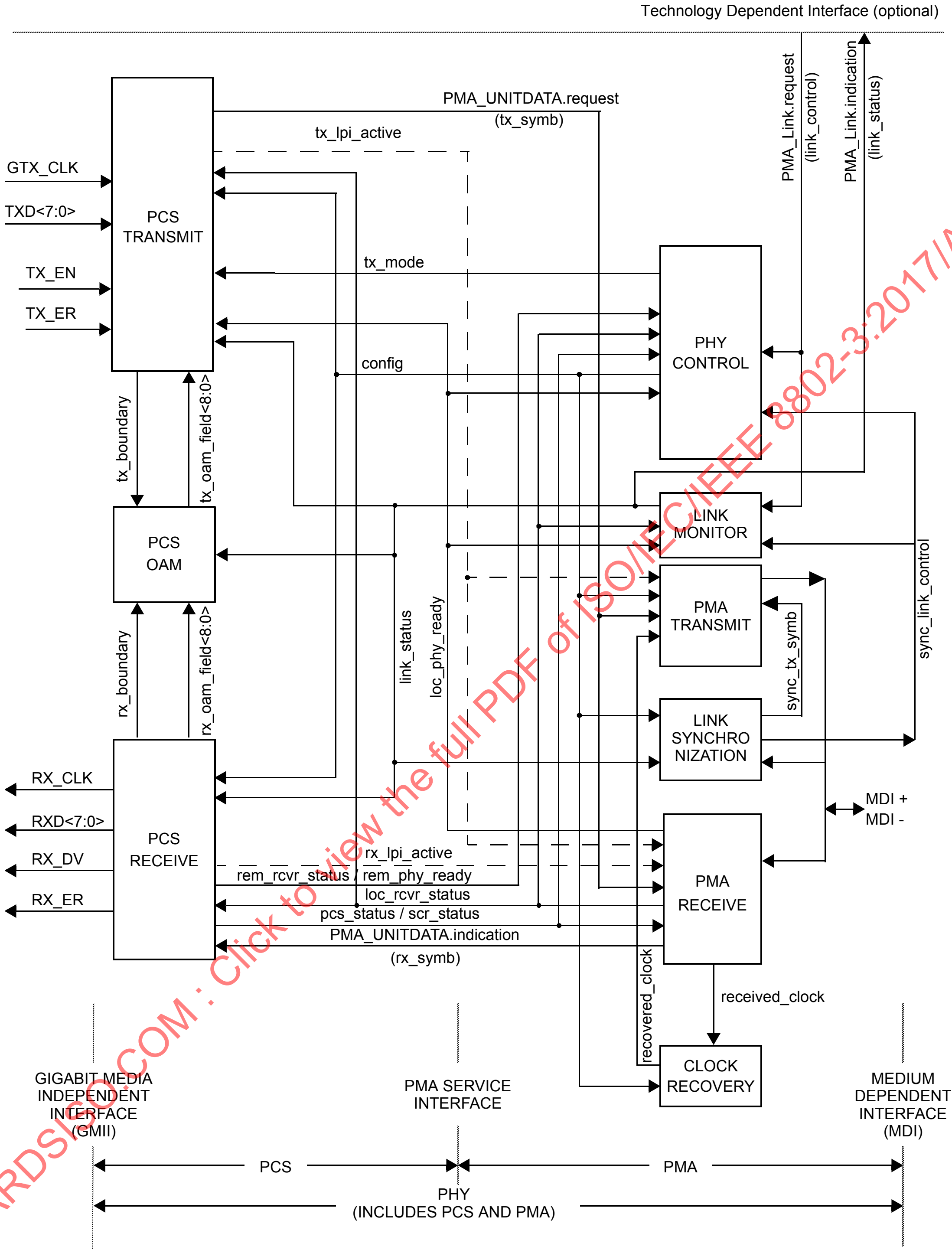
Support for EEE capability is advertised during Training. See 97.4.2.4.5 for details. Transitions to and from the LPI transmit mode are controlled via GMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

When the 1000BASE-T1 OAM SNR settings indicate that LPI is insufficient to maintain PHY SNR, the PHY may temporarily be forced to exit LPI mode and send idles.

The PCS 80B/81B Transmit state diagram in Figure 97–14 includes additional states for EEE. The PCS 80B/81B Receive state diagram in Figure 97–12 includes additional states for EEE.

97.1.2.4 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled to synchronize between the MASTER PHY and SLAVE PHY before training starts. Link Synchronization provides a fast and reliable mechanism for the link partner to detect the presence of the other, validate link, and start the timers used by the link monitor. Link Synchronization operates in a half-duplex fashion. Based on timers, the MASTER PHY sends a synchronization sequence for 1 µs. If there is no response from the SLAVE, the MASTER repeats by sending a synchronization sequence every 5 µs. If the slave detects the sequence, it responds with a synchronization sequence for 1 µs (after the MASTER has stopped transmitting). If no other detection happens after the SLAVE response for 4 µs then Link Synchronization is successfully complete, link monitor timers are started, and the PHY Control state machine starts Training. Link synchronization is defined in 97.4.2.6.



NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 97–2—Functional block diagram

97.1.3 Signaling

1000BASE-T1 signaling is performed by the PCS generating continuous symbol sequences that the PMA transmits over the single twisted-pair copper cable. The signaling scheme achieves a number of objectives including the following:

a) Algorithmic mapping from TXD<7:0> to PAM3 symbols in the transmit path
b) Algorithmic mapping from PAM3 symbols to RXD<7:0> in the receive path
c) Adding FEC coded data to transmit and validating data using FEC on receive
d) Uncorrelated symbols in the transmitted symbol stream
e) No correlation between symbol streams traveling both directions
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining
g) Optionally, ability to signal to the remote PHY that the transmitting PHY is entering the LPI mode or exiting the LPI mode and returning to normal power operation

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In the normal data mode, PCS generates symbols that represent data, control, or idles for transmission by the PMA.

In the training mode, the PCS generates only a PAM2 pattern with periodic embedded data that enables the receiver at the other end to train and synchronize timing, scrambler seeds, and capabilities. The LPI mode is enabled separately in each direction (see LPI signaling in 97.3.5). When transmitting in LPI mode, the PCS generates zero symbols and periodically send a REFRESH pattern to keep the two PHYs synchronized (see 97.3.2.2.15).

97.1.4 Interfaces

All 1000BASE-T1 PHY implementations are compatible at the MDI and at a physically exposed GMII, if made available. Physical implementation of the GMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

97.1.5 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ± 1% unless otherwise stated.

Default initializations, unless specified, are left to the implementer.

97.2 1000BASE-T1 Service Primitives and Interfaces

1000BASE-T1 transfers data and control information across the following four service interfaces:

a) Gigabit Media Independent Interface (GMII)
b) Technology Dependent Interface

c) PMA service interface
d) Medium dependent interface (MDI)

The GMII is specified in Clause 35; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in 97.2.2, and the MDI is defined in 97.7.3.

97.2.1 Technology Dependent Interface

1000BASE-T1 uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface as specified in 98.4:

PMA_LINK.request(link_control)

PMA_LINK.indication(link_status)

97.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation or the PHY Link Synchronization algorithm to enable and disable operation of the PMA, as specified in 98.4.2, respectively.

97.2.1.1.1 Semantics of the primitive

PMA_LINK.request(link_control)

The link_control parameter can take on one of two values: DISABLE, or ENABLE.

DISABLE	Used by the Auto-Negotiation function to disable the PHY
ENABLE	Used by the Auto-Negotiation to enable the PHY

97.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

97.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 97.4.2.5, the PMA PHY Control function as defined in 97.4.2.4, and the PMA Receive function defined in 97.4.2.3.

97.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

97.2.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL	No valid link established
OK	The Link Monitor function indicates that a valid 1000BASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

97.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 97–27.

97.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

97.2.2 PMA service interface

1000BASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_PHYREADY.indication(loc_phy_ready)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_REMPHYREADY.request(rem_phy_ready)

The use of these primitives is illustrated in Figure 97–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 97–3.

EEE-capable PHYs additionally support the following service primitives:

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)
PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)

97.2.2.1 PMA_TXMODE.indication

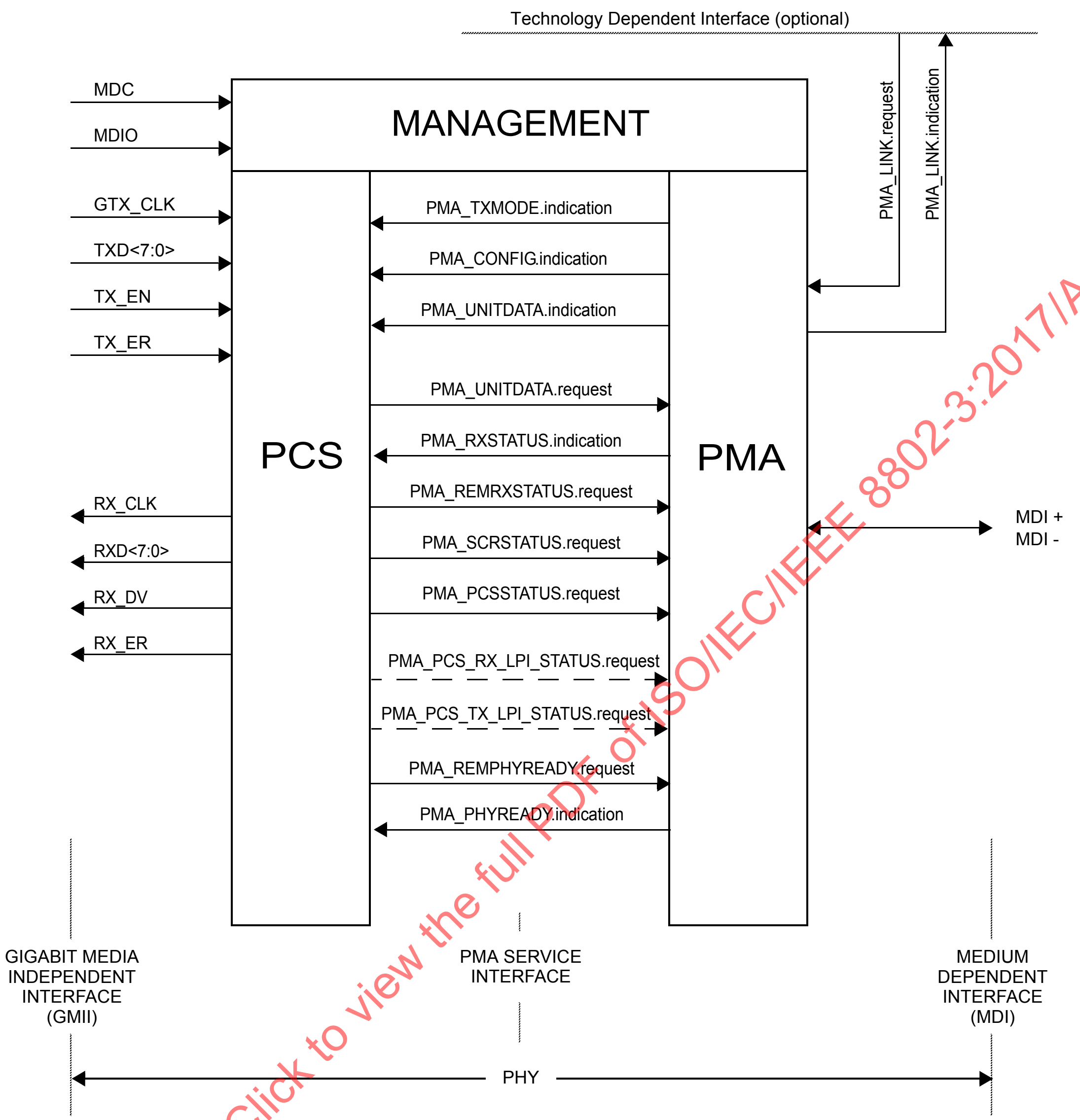
The transmitter in a 1000BASE-T1 link normally sends over the MDI symbols that represent a GMII data stream with framing, scrambling and encoding of data, control information, or idles.

97.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following four values of the form:

SEND_NThis value is continuously asserted during transmission of sequences of symbols representing a GMII data stream in the data mode
SEND_IThis value is continuously asserted when transmission of sequences of idle symbols is to take place
SEND_TThis value is continuously asserted in case transmission of sequences of symbols representing the training mode is to take place
SEND_ZThis value is continuously asserted in case transmission of zeros is required



NOTE—Service interface primitives shown with dashed lines are optional.

Figure 97–3—1000BASE-T1 service interfaces

97.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

97.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 97.3.2.2.

97.2.2.2 PMA_CONFIG.indication

Each PHY in a 1000BASE-T1 link is capable of operating as a MASTER PHY and as a SLAVE PHY. If the Auto-Negotiation process is enabled, PMA_CONFIG MASTER-SLAVE configuration is determined during Auto-Negotiation (Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

97.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY

97.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

97.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter configuration.

97.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 97.3.2.2 to represent GMII data and control streams or other sequences.

97.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the values in the set { –1, 0, 1 }

97.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

97.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with optional transmit filtering and other specified PMA Transmit processing.

97.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

97.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

97.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 750 MHz, as governed by the recovered clock.

97.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

97.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

97.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The training mode descrambler has achieved synchronization
NOT_OK	The training mode descrambler is not synchronized

97.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

97.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.2.3 and 97.4.2.4.

97.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

97.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in the data mode
NOT_OK	The PCS is not operating reliably in the data mode

97.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

97.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.4.1.

97.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

97.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable

97.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

97.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26, 97.3.2.3, 97.4.2.4, and 97.4.597.4.5.

97.2.2.8 PMA_PHYREADY.indication

This primitive is generated by PMA Receive to indicate the local PHY is ready or not ready to receive data. The parameter loc_phy_ready is conveyed to the link partner by the PCS as defined in Table 97–1.

97.2.2.8.1 Semantics of the primitive

PMA_PHYREADY.indication(loc_phy_ready)

The loc_phy_ready parameter can take on one of two values of the form:

OK	The local PHY is ready to receive data
NOT_OK	The local PHY is not ready to receive data

97.2.2.8.2 When generated

PMA Receive generates PMA_PHYREADY.indication messages to indicate a change in loc_phy_ready based on loc_rcvr_status and pcs_status values.

97.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26 and Figure 97–27.

97.2.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the InfoField from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY.

97.2.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected

97.2.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in InfoField messages received from the remote PHY during training.

97.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26.

97.2.2.10 PMA_REMPHYREADY.request

This primitive is generated by PCS Receive to indicate whether the remote PHY is ready or not ready to receive data. Its value is received from the link partner by the PCS as defined in Table 97–1.

97.2.2.10.1 Semantics of the primitive

PMA_REMPHYREADY.request(rem_phy_ready)

The rem_phy_ready parameter can take on one of two values of the form:

OK	The remote PHY is ready to receive data
NOT_OK	The remote PHY is not ready to receive data

97.2.2.10.2 When generated

The PCS generates PMA_REMPHYREADY.request messages to indicate a change in rem_phy_ready based on the PCS decoding the control words in Table 97–1 received from the remote PHY.

97.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26.

97.2.2.11 PMA_PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PMA_PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode.

97.2.2.11.1 Semantics of the primitive

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

true	The receive function is in the LPI receive mode
false	The receive function is not in the LPI receive mode

97.2.2.11.2 When generated

The PCS generates PMA_PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in 97.3.2.3 and 97.3.6.2.2.

97.2.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.3.6.4.

97.2.2.12 PMA_PCS_TX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS transmit function to indicate the status of the transmit link at the local PHY. The parameter PMA_PCS_TX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the transmit function is in the LPI transmit mode.

97.2.2.12.1 Semantics of the primitive

PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the form:

true	The transmit function is in the LPI transmit mode
false	The transmit function is not in the LPI transmit mode

97.2.2.12.2 When generated

The PCS generates PMA_PCS_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable as described in 97.3.5 and 97.3.6.2.2.

97.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.3.6.4.

97.3 Physical Coding Sublayer (PCS)

97.3.1 PCS service interface (GMII)

The PCS service interface allows the 1000BASE-T1 PCS to transfer information to and from a PCS client. The PCS Interface is defined as the Gigabit Media Independent Interface (GMII) in Clause 35.

97.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 97–4, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 97–4.

97.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power for the device containing the PMA has not reached the operating state
b) The receipt of a request for reset from the management entity

PCS Reset sets pcs_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

97.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 80B/81B Transmit state diagram in Figure 97–14 and the PCS Transmit bit ordering in Figure 97–5 and Figure 97–7.

When communicating with the GMII, the PCS uses an octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 80B/81B blocks is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the GMII format and the PMA service interface format.

When the transmit channel is in the data mode, the PCS Transmit process continuously generates 80B/81B blocks based upon the TXD <7:0>, TX_EN and TX_ER signals on the GMII. The subsequent functions of the PCS Transmit process then pack the resulting blocks plus one 1000BASE-T1 OAM symbol, both of which are then processed by a Reed-Solomon (RS-FEC) encoder and subsequently 3B2T mapped into a transmit PHY frame of PAM3 symbols. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive. A symbol period, T, is 4/3 ns.

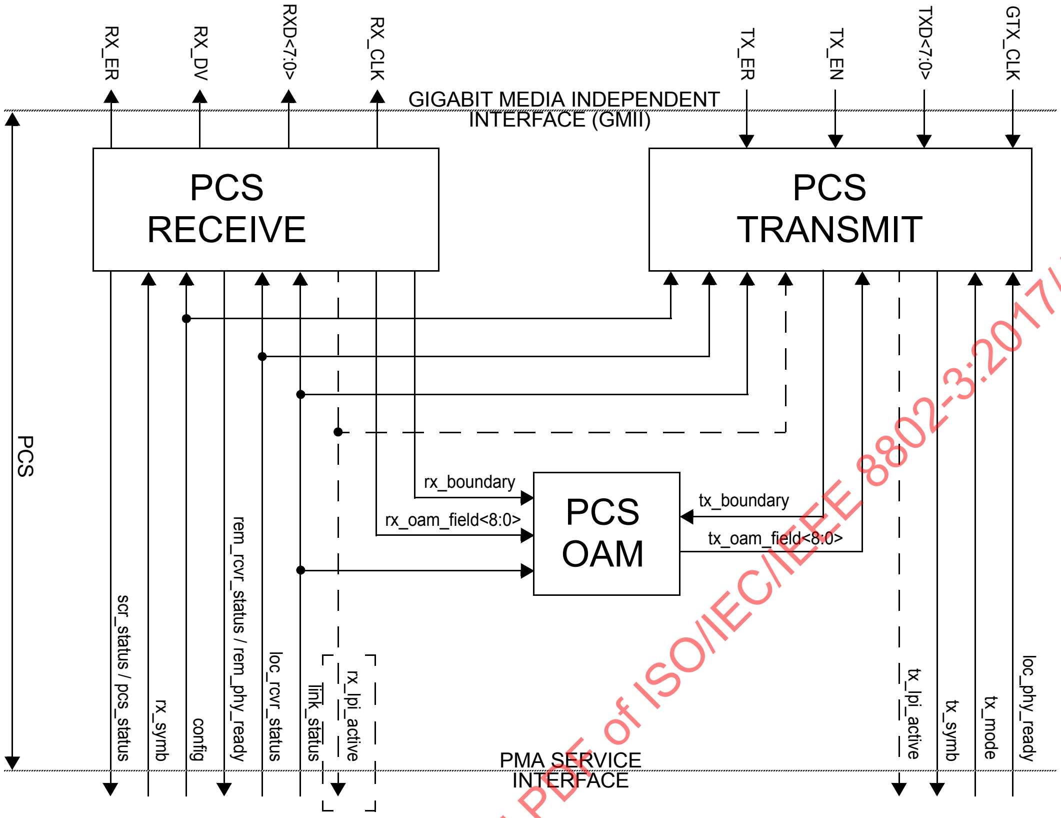


Figure 97–4—PCS reference diagram

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit generates sequences of codes defined in 97.3.4.2 to the PMA via the PMA_UNITDATA.request primitive. These codes are used for training mode and only transmit the values {–1, +1}.

During training mode an InfoField is transmitted at regular intervals containing messages for start-up operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner. (See 97.4.2.4.)

In the data mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses an 81B-RS coding technique to generate at each symbol period symbols that represent data or control. During transmission, 45 80B/81B blocks shall be aggregated, encoded by a PHY frame encoder, and then scrambled by a PCS scrambler. During data encoding PCS Transmit frames shall be encoded into a sequence of PAM3 symbols and transferred to the PMA.

Dashed rectangles in Figure 97–14 indicate states and state transitions in the transmit process state diagram that are supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

After reaching the data mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the GMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 97.3.2.2.15.

97.3.2.2.1 Use of blocks

The PCS maps GMII signals into 81-bit blocks inserted into a PHY frame, and vice versa, using an 81B-RS coding scheme. The PAM2 PMA training frame synchronization allows establishment of PHY frame and 81B boundaries by the PCS Synchronization process. Blocks and PHY frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and PHY frames as provided by the rules in 97.3.2.2.2.

97.3.2.2.2 81B-RS transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encoding defined by the transmission code ensures that sufficient information is present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any PHY frame errors that may occur during transmission and reception of information. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to GMII, PMA, and other PCS constructs is illustrated in Figure 97–5 for transmit and Figure 97–6 for receive. These figures illustrate the processing of a multiplicity of blocks containing 10 data octets. See 97.3.2.2.5 for information on how blocks containing control characters are mapped.

97.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

97.3.2.2.4 Transmission order

The PCS Transmit bit ordering shall conform to Figure 97–5 and Figure 97–7. Note that these figures show the mapping from GMII to 80B/81B block for a block containing ten data characters. The LSB of the 1000BASE-T1 OAM symbol is transmitted first.

97.3.2.2.5 Block structure

Blocks consist of 81 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain 10 data octets. Control blocks begin with a 5-bit pointer field that indicates the location of the first control code within the block. Bits 0 to 3 of the pointer field points to the next octet that is a control symbol. Bit 4 of the pointer field indicates whether the next control symbol is the final control symbol of the block: 0 = final, 1 = more control symbols. If the first octet in the block is a control character, the pointer field is followed by a 3-bit control code. Otherwise the pointer field is followed by one or more data octets until the position of the first control code. Then the 3-bit control code indicates type of control character. The control code is followed by a 5-bit pointer field to the next control character if the prior pointer field value was greater than 15 (i.e., bit 4 = 1). The pointer field may be followed by a data octet or control code depending on the value of the pointer field. In this way any combination of ten data octets and control characters may be encapsulated within an 80B/81B block.

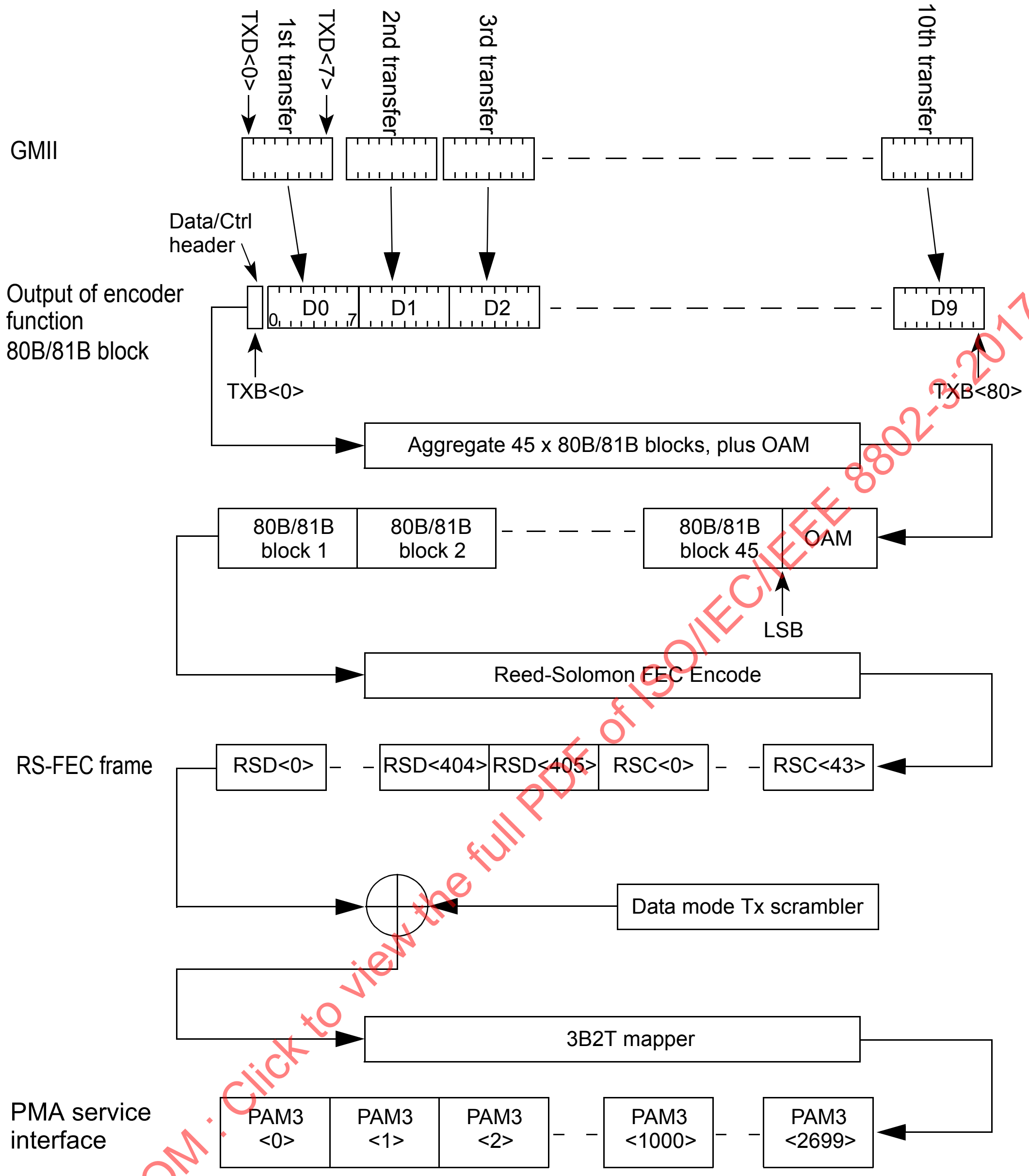


Figure 97–5—PCS Transmit bit ordering

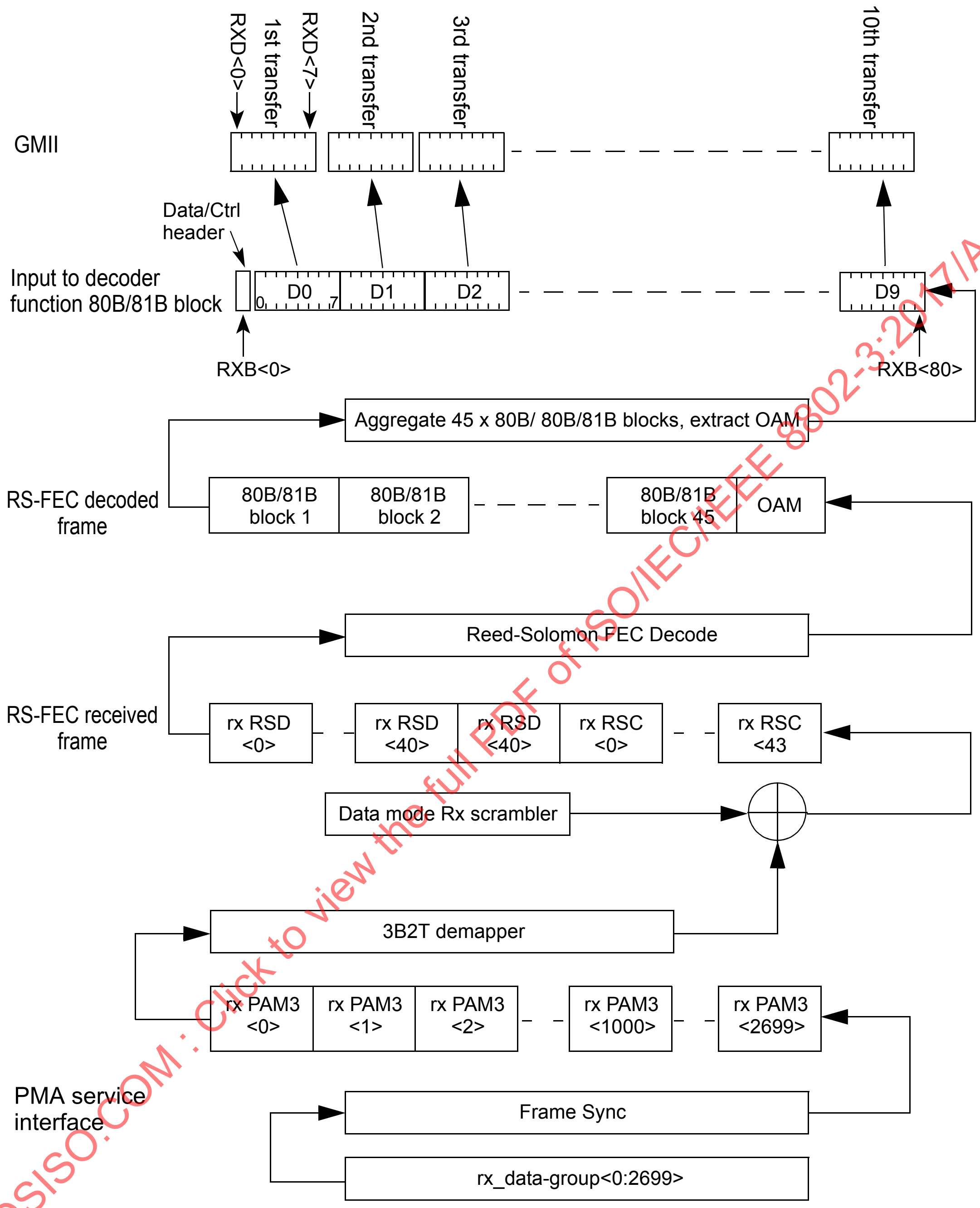


Figure 97–6—PCS Receive bit ordering

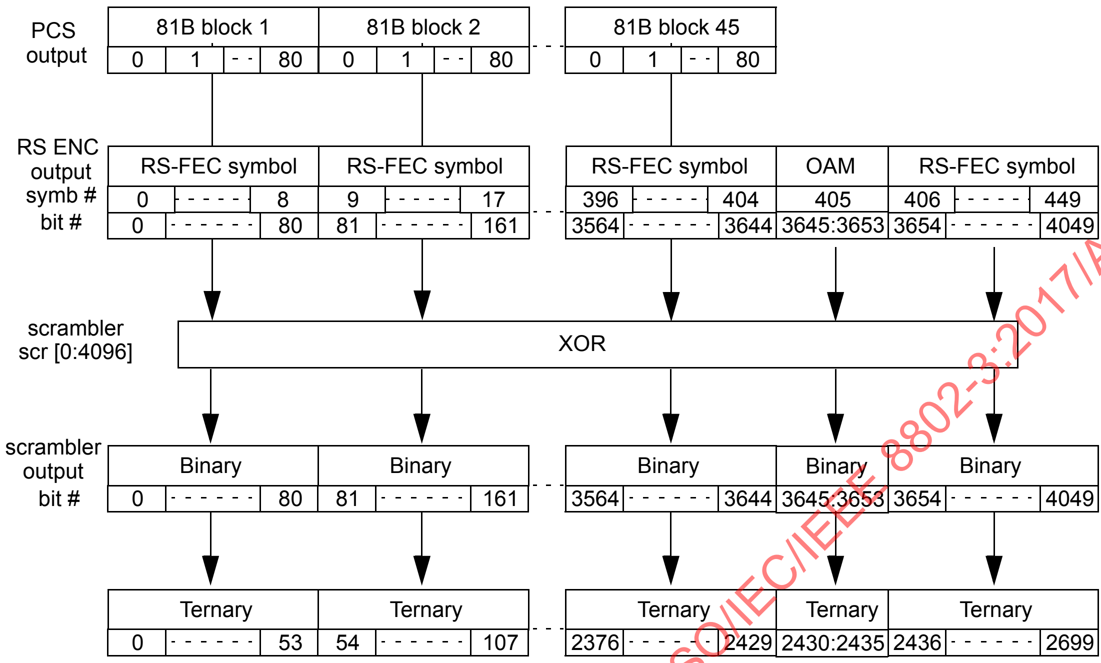


Figure 97–7—PCS detailed transmit bit ordering

The 80B/81B block encoding is defined by the following pseudo-code, where N = 10.

```
N = number of GMII octets encoded into block. Octets numbered n = 0,1,2,…,N-1.
octet 0 is the first one presented on GMII.
TC[n] = 0 if octet n is data octet on GMII, 1 if octet n is control octet on GMII
TC[-1] = 1 by definition
TD[n][0:7] = GMII octet n TXD[0:7] if TC[n] = 0
TD[n][5:7] = 010 – IPG (loc_phy_ready = OK), 101 – LPI, 001 – TX Error, 000 – IPG
(loc_phy_ready = NOT_OK) if TC[n] = 1. TD[n][0:4] is undefined.
B[0:8N] is the 8N+1 block. Bit 0 transmitted first.
OR(n) = Bitwise OR of TC[n:N-1]
NEXT(n)[0:3] = bit position of lowest bit in TC[n:N-1] that is a 1. Bit 3 is MSB.
NEXT(n)[4] = 0 if Bitwise SUM of TC[n:N-1] = 1, else 1

B[0] =              OR(0)
B[8n+1:8n+4] =      TD[n][0:3] – if OR(n) = 0
                    NEXT(n)[0:3] – if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][3:6] – if OR(n) = 1 AND TC[n-1] = 0
B[8n+5] =           TD[n][4] – if OR(n) = 0
                    NEXT(n)[4] – if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][7] – if OR(n) = 1 AND TC[n-1] = 0
B[8n+6:8n+8] =      TD[n][5:7] – if OR(n) = 0
                    TD[n][5:7] – if OR(n) = 1 AND TC[n] = 1
                    TD[n][0:2] – if OR(n) = 1 AND TC[n] = 0
```

97.3.2.2.6 Control codes

A subset of control characters defined at the GMII are supported by the 1000BASE-T1 PCS. When TX_ER and TX_EN are both asserted, the 1000BASE-T1 PCS conveys an Error symbol in the 80B/81B block code. When TX_EN is not asserted and no other supported control code is present at the GMII, the 1000BASE-T1 PCS conveys a Normal Inter-Frame control code in the 80B/81B block code.

The control characters and their mappings to 1000BASE-T1 control code and GMII control code are specified in Table 97–1. All GMII and 1000BASE-T1 control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

Table 97–1—GMII control code mapping

Control Code[0:2]	GMII Transmit	GMII Receive
000	Normal Inter-Frame with loc_phy_ready = NOT_OK	Normal Inter-Frame with rem_phy_ready = NOT_OK
001	Transmit Error Propagation	Data Reception Error
010	Normal Inter-Frame with loc_phy_ready = OK	Normal Inter-Frame with rem_phy_ready = OK
101	Assert Low Power Idle	Assert Low Power Idle

The Carrier Extend and Carrier Extend Error, and Reserved transactions, if any occurred, are assigned to Normal inter-frame in the PCS 80B/81B Encoder.

97.3.2.2.7 Idle

Idle (Normal Inter-frame) control characters are transmitted when TX_EN is not asserted and no other supported control code is present at the GMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. Idle characters shall not be added within a MAC frame.

97.3.2.2.8 LP_IDLE

The low power idle control characters (LP_IDLEs) are transmitted when TX_EN is not asserted, TX_ER is asserted, and TXD<7:0> = 0x1. A continuous stream of LPI control characters is used to maintain a link in the LPI transmit mode. Idle control characters are used to transition from the LPI transmit mode to the normal power mode. EEE compliant PHYs respond to the Assert Low Power Idle condition on the GMII using the procedure outlined in 97.1.2.3. LP_IDLE characters may be added or deleted by the PCS to adapt between clock rates. LP_IDLE characters shall not be added within a MAC frame.

Where the GMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert LPI_IDLEs, or delete LPI_IDLEs to adapt between the rates.

If EEE is not supported, then LP_IDLE shall be converted to IDLE.

97.3.2.2.9 Error

The Error control code is sent when TX_ER and TX_EN are both asserted. Error allows physical sublayers such as the PCS to propagate received errors.

97.3.2.2.10 Transmit process

The transmit process generates blocks based upon the TXD<7:0>, TX_EN, and TX_ER signals received from the GMII. Ten GMII data transfers are encoded into each block. It takes 2700 PMA_UNITDATA transfers to send a PHY frame of data. Where the GMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, or delete idles to adapt between the rates.

The transmit process generates blocks as specified in the transmit process state diagram. The contents of each block are contained in a vector tx_coded<80:0>, which is aggregated with 45 80B/81B blocks and 1000BASE-T1 OAM, then passed to the RS-FEC Encoder and then finally passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

97.3.2.2.11 RS-FEC encoder

The 1000BASE-T1 PCS shall encode the transmitted data stream using Reed-Solomon code (450,406). The RS-FEC encoder shall follow the bit order described in 97.3.2.2.3 where the LSB is the first bit into the RS-FEC encoder and the first transmitted bit.

The FEC code used for 1000BASE-T1 links is a shortened Reed-Solomon (450,406) code over the Galois Field of GF(2^9)—a code operating on 9-bit symbols, as shown in Figure 97–8. The code encodes 406 information symbols and adds 44 parity symbols, enabling correction of up to 22 symbol errors. The code is systematic, meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block.

The code is based on the generating polynomial shown in Equation (97–1).

$$G(Z) = \prod_{i=0}^{43}(Z - \alpha^i) = A_{44}Z^{44} + A_{43}Z^{43} + \ldots + A_0Z^0 \qquad (97\text{–}1)$$

where

α is a root of the binary primitive polynomial $x^9 + x^4 + 1$ and is represented as 0x002
A is a series representing the resulting polynomial coefficients of $G(Z)$, (A_{44} is equal to 0x001)
Z corresponds to an 9-bit GF(2^9) symbol
x corresponds to a bit position in a GF(2^9) symbol

The parity calculation shall produce the same result as the shift register implementation shown in Figure 97–8. Before calculation begins, the shift register shall be initialized to zero. The contents of the shift register are transmitted without inversion.

A FEC parity vector is represented by Equation (97–2).

$$P(Z) = D(Z) \bmod G(Z) \qquad (97\text{–}2)$$

where

$D(Z)$ is the data vector $D(Z) = D_{405}Z^{449} + D_{404}Z^{448} + \ldots + D_0Z^{44}$. D_{405} is the first 9-bit data symbol and D_0 is the last
$P(Z)$ is the parity vector $P(Z) = P_{43}Z^{43} + P_{42}Z^{42} \ldots + P_0Z^0$. P_{43} is the first 9-bit parity symbol and P_0 is the last

A data symbol ($d_8, d_7, \ldots, d_1, d_0$) is identified with the element: $d_8\alpha^8 + d_7\alpha^7 + \ldots + d_1\alpha^1 + d_0$ in GF(2^9), the finite field with 2^9 elements.

The d_0 is identified as the LSB and d_8 is identified as the MSB for all symbols.

The resulting payload of scrambled 45 80B/81B blocks, followed by the 1000BASE-T1 OAM symbol results in a total payload of 3654 bits. The resulting PHY frame size is 450 9-bit symbols, a total of 4050 bits. Figure 97–7 shows the bit mapping between PCS and FEC.

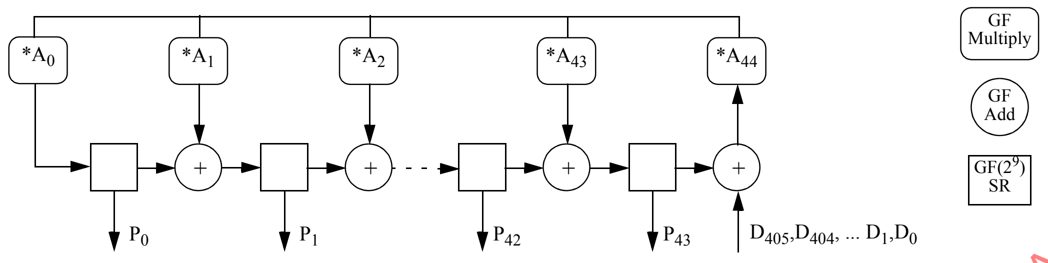


Figure 97–8—Circuit for generating FEC parity vector

97.3.2.2.12 PCS scrambler

The PCS Transmit function employs side-stream scrambling. The scrambler for the MASTER shall produce the same result as the implementation shown in Figure 97–9. This implements the scrambler polynomial as shown in Equation (97–3):[3]

$$G(x) = 1 + x^4 + x^{15} \quad (97\text{–}3)$$

The scrambler for the SLAVE shall produce the same result as the implementation shown in Figure 97–9. This implements the scrambler polynomial as shown in Equation (97–4):

$$G(x) = 1 + x^{11} + x^{15} \quad (97\text{–}4)$$

The initial seed values for the MASTER and SLAVE scramblers are left to the implementer. The seed values shall be non-zero and transmitted during the InfoField exchange. (See 97.4.2.4.5). The scrambler is run continuously on all PHY frame output bits.

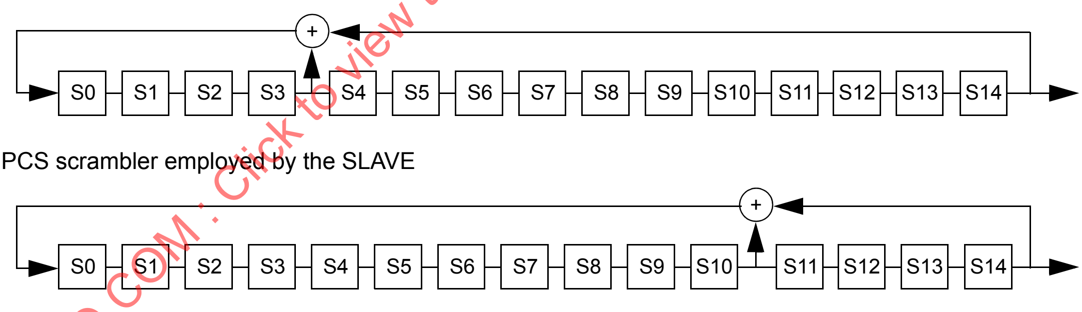


Figure 97–9—MASTER and SLAVE PCS scramblers

97.3.2.2.13 3B2T to PAM3

The 3B2T mapper generates 2700 PAM3 symbols per PHY frame that are sent to the PMA via PMA_UNITDATA.request. Every 9-bit symbol is divided into three 3-bit groups with the LSB bits as the first group. Each 3-bit group is then mapped by the 3B2T into 2 PAM3 symbols. The mapping of 3B2T to PAM3 is illustrated in Table 97–2. B[0] is the LSB and T[0] is the first PAM3 symbol transmitted..

[3]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (97–3). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

Table 97–2—3B2T Mapping to PAM3

B[2], B[1], B[0]	T[1], T[0]
000	–1,–1
001	0,–1
010	–1,0
011	–1,+1
100	+1,0
101	+1,–1
110	+1,+1
111	0,+1

97.3.2.2.14 81B-RS framer

The 81B-RS framer adapts between the 81-bit width of the 80B/81B blocks and the PAM3 input to the PMA. When the transmit channel is operating in the data mode, the 81B-RS sends one PAM3 symbol of transmit data at a time via PMA_UNITDATA.request primitives. The PMA_UNITDATA.request primitives are fully packed with bits.

97.3.2.2.15 EEE capability

The optional 1000BASE-T1 EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low. EEE compliant PHYs shall implement the transmit state diagram including the EEE portion, noted by dotted lines in Figure 97–14, within the PCS.

When there is an Assert Low Power Idle while in the SEND_DATA state the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the SEND_LPI state. The sleep signal is one PHY frame composed entirely of LP_IDLE characters. If the LP_IDLE character fills the entire last 80B/81B block then the sleep signal is the next PHY frame. The PHY shall transmit no PHY frames partially filled with LP_IDLES.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 97.3.5.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

— When the PMA_TXMODE.indication message does not have the value of SEND_N, the lpi_tx_mode variable is ignored
— When the lpi_tx_mode variable takes the value NORMAL the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive
— When the lpi_tx_mode variable takes the value QUIET the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive
— When the lpi_tx_mode variable takes the value REFRESH, the PCS passes zero data encoded through PCS data path to the PMA via the PMA_UNITDATA.request primitive

The quiet-refresh cycle is repeated until Assert Low Power Idle is not detected at the GMII (indicating that the local system is requesting a transition back to the normal power mode) or until an 1000BASE-T1 OAM message with SNR<1:0> set to 01 is transmitted to or received from the link partner (indicating that the LPI refresh is insufficient to maintain the SNR). At the next wake frame window the PCS transmits a wake frame composed of an entire PHY frame containing only Idle. The wake frame shall be sent only during alternating PHY frame counts.

The wake signal occurs at the beginning of every second PHY frame boundary, and the maximum duration of the PHY wake time is 10.8 µs (lpi_wake_timer = T_{w_phy} as defined by Clause 78).

97.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 80B/81B receive state diagram in Figure 97–12 and the PCS Receive bit ordering in Figure 97–6 including compliance with the associated state variables as specified in 97.3.6.

The PCS Receive function accepts received symbols provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the PMA training alignment to correctly align the 81B-RS frames. The received 81B-RS frames are decoded with error correction; the framing is checked; and the 80B/81B blocks are converted to 10 data octets to obtain the signals RXD<7:0>, RX_DV, and RX_ER for transmission to the GMII.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the parameter scr_status to OK.

When the PCS Synchronization process has obtained synchronization, the PHY frame error rate (RFER) monitor process monitors the signal quality asserting hi_rfer if excessive PHY frame errors are detected (RS parity error). If 40 consecutive PHY frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD<7:0>, RX_DV and RX_ER for transmission to the GMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.request primitive. It attains PHY frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes 1 bit pattern every 180 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an InfoField, which is inserted in the 15th PCS partial PHY frame. When the PCS Synchronization process is synchronized to the PHY frame boundary using this pattern, block_lock is asserted. One partial PHY frame codeword is defined to be 1/15 of a PHY frame. Fifteen partial PHY frames concatenated back to back form one PHY frame. The start of the first partial PHY frame coincides with the start of the PHY frame.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 97.3.6.

The link partner signals a transition to the LPI mode of operation by transmitting one PHY frame composed entirely of 80B/81B blocks of LP_IDLES. When blocks of LP_IDLES are detected at the output of the 80B/81B decoder, rx_lpi_active is asserted by the PCS receive function and the LPI character is continuously asserted at the receive GMII. After the sleep frame the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses PHY frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 97.3.5. The quiet-refresh cycle continues until the PHY detects the wake frame. The PHY receive function sends Idles to the GMII for the remainder of the wake frame and then resumes normal power mode operation.

97.3.2.3.1 Frame and block synchronization

When operating in the data mode, the receiving PCS shall form a PAM3 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_data<0> to rx_data<2699> (see Figure 97–6). It obtains block lock to the PHY frames during the PAM2 training pattern using synchronization bits provided in the training sequence.

97.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<7:0> to the GMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial per Equation (97–4) and the SLAVE PHY shall employ the receiver descrambler generator polynomial per Equation (97–3).

97.3.2.3.3 Valid and invalid blocks

An 80B/81B block is invalid if any of the following conditions exists:

a) The block contains an invalid pointer
b) Any control character contains a value not in Table 97–1
c) The PHY frame containing this 80B/81B block is uncorrectable

Invalid blocks are replaced with Error.

97.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 97–5, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero. When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 97–6. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero, however there is the possibility that the RS-FEC decoder may have corrected some errors. This mode is further described as test mode 7 in 97.5.2.

97.3.4 PMA training side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation (97–5)

$$g_M(x) = 1 + x^{13} + x^{33} \qquad (97\text{–}5)$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation (97–6)

$$g_S(x) = 1 + x^{20} + x^{33} \qquad (97\text{–}6)$$

as transmitter side-stream scrambler generator polynomial. An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 97–9. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

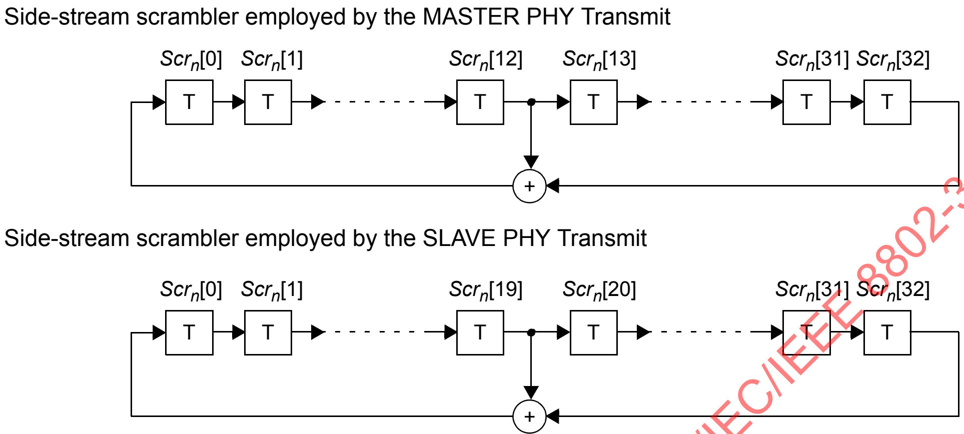


Figure 97–10—Realization of side-stream scramblers by linear feedback shift registers

97.3.4.1 Generation of S_n

During PMA training, the training pattern is embedded with indicators to establish alignment to the RS-FEC block and the 15 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners. PMA training signal encoding is based on the generation, at time n, of the bit S_n. The first bit is inverted in the first 14 partial PHY frames of each RS-FEC block. The first 96 bits of the 15th partial PHY frame is XORed with the contents of the InfoField. Each partial PHY frame is 180 bits long, beginning at S_n where $(n \bmod 180) = 0$. See Equation (97–7).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 180)} & 2520 \le (n \bmod 2700) \le 2615 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 180) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad (97\text{–}7)$$

97.3.4.2 Generation of symbol T_n

The bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$.

97.3.4.3 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation (97–6) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation (97–5).

97.3.5 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates a sleep signal composed of 80B/81B blocks containing only LPI control characters, as described in 97.3.2.2.15. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 97–11). The first part of this cycle is known as the *quiet period* and lasts for a time lpi_quiet_time equal to 354 partial PHY frame periods. The quiet period is defined in 97.3.5.2. The second part of this cycle is known as the *refresh period* and lasts for a time lpi_refresh_time equal to 6 partial PHY frame periods. The refresh period is defined in 97.3.5.3. A cycle composed of one quiet period and one refresh period is known as an LPI cycle and lasts for an lpi_qr_time equal to 24 × 15 = 360 partial PHY frame periods.

lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the partial PHY frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 + 15. It is used to ensure refresh signals and wake start times are appropriately offset by the link partners.

PHYs begin the transition from the LPI receive mode when they detect the wake frame.

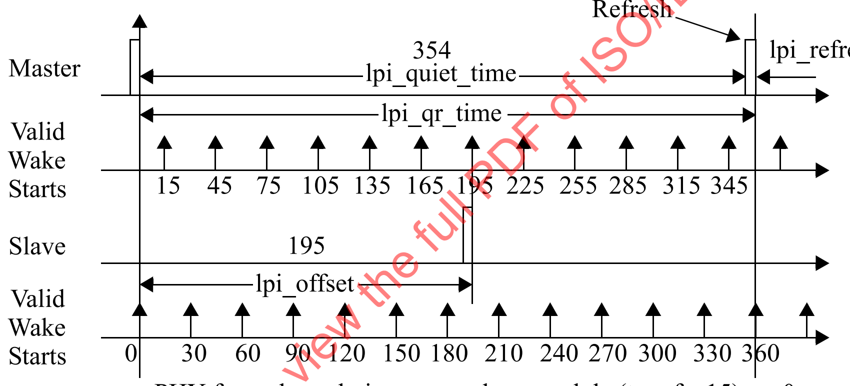


Figure 97–11—LPI signal timing

97.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs shall synchronize refresh intervals during the LPI mode. The quiet-refresh cycle is established from the Master partial PHY frame Count (PFC24) during PMA Training. At the MASTER, partial PHY frame zero and all multiples of 360 partial PHY frames thereafter denote the start of the cycle.

An EEE-capable PHY in SLAVE mode is responsible for synchronizing its partial PHY frame count to the MASTER's partial PHY frame count during link up. The SLAVE shall ensure that its partial PHY frame count is synchronized to the MASTER's partial PHY frames within 1 partial PHY frame. The start of the SLAVE quiet-refresh cycle is delayed from the MASTER by 13 PHY frames (195 partial PHY frames). This offset ensures that the MASTER and SLAVE wake/sense windows are offset from each other and that the refresh periods are nearly a half cycle offset.

Following the transition to PAM3, the PCS continues to count transmitted partial PHY frames (tx_pfc), and uses the counter to generate refresh and wake control signals for the transmit functions.

Wake frames may be sent at the beginning of every second PHY frame boundary starting at the beginning of the refresh PHY frame. This sets wake_period to 30 partial PHY frames. The MASTER and SLAVE allowable wake positions do not overlap. The wake frame may start in the same PHY frame as a planned refresh and obviate this refresh.

The MASTER and SLAVE shall derive the tx_refresh_active and tx_wake_start signals from the transmitted partial PHY frames (tx_pfc) as shown in Table 97–3 and Table 97–4.

Table 97–3—Synchronization logic derived from SLAVE signal partial PHY frame count

Slave-side Variable	u = tx_pfc
tx_refresh_active=true	lpi_offset – lpi_refresh_time ≤ mod(u, lpi_qr_time) < lpi_offset
tx_wake_start=true	mod(u, wake_period) = 0

Table 97–4—Synchronization logic derived from MASTER signal partial PHY frame count

Master-side variable	v = tx_pfc
tx_refresh_active=true	mod(v, lpi_qr_time) ≥ lpi_quiet_time
tx_wake_start=true	mod(v, wake_period) = wake_period/2

97.3.5.2 Quiet period signaling

During the quiet period the transmitter shall put PAM3 symbol zero on to the MDI. During the quiet period the transmitter may be turned off to save power.

97.3.5.3 Refresh period signaling

During the LPI mode 1000BASE-T1 PHYs use staggered, out-of-phase refresh signaling to maximize power savings. PAM3 refresh symbols are generated from the output of the data mode PCS side-stream scrambler polynomials described in 97.3.2.2.12 with PCS transmit data masked to zero. The scramblers run continuously regardless of the transmit mode. The refresh occupies the last 6 partial PHY frames of where the PHY frame would occur if it were transmitted.

The 1000BASE-T1 OAM symbols and the RS parity symbols are XORed with the scrambler stream at the same relative position to the RS boundaries as they occupy during normal mode. The parity is generated using Equation (97–2) with D_{405} ... D_1 = 0 and D_0 = OAM.

97.3.6 Detailed functions and state diagrams

97.3.6.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of constants, variables, functions, counters, and messages. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

97.3.6.2 State diagram parameters

97.3.6.2.1 Constants

EBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing symbol errors in all 10 character locations.

IBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing idles in all 10 character locations.

IBLOCK_T<99:0>
TYPE: bit vector
100-bit vector to be sent to the encoder containing idles in all 10 character locations.

LPBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing LP_IDLEs in all 10 character locations.

LPBLOCK_T<99:0>
TYPE: bit vector
100-bit vector to be sent to the encoder containing LP_IDLEs in all 10 character locations.

RFER_CNT_LIMIT
TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error rate interval.

ZBLOCK_T<80:0>
TYPE: bit vector
81-bit vector containing all zero bits.

97.3.6.2.2 Variables

RFER_test_lf
Boolean variable that is set true when a new PHY frame is available for testing and false when RFER_TEST_LF state is entered. A new PHY frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next PHY frame.

block_lock
Boolean variable that is set true when receiver acquires block delineation.

hi_rfer
Boolean variable that is asserted true when the rfer_cnt reaches RFER_CNT_LIMIT indicating a bit error ratio > 4×10^{-4}.

pcs_reset

When this variable is set to ON, all PCS functions are reset. Otherwise, this variable holds the value of OFF. This variable is set by the PCS Reset function.

rx_coded<81:0>

Vector containing the input to the 80B/81B decoder including a block valid flag. The format for rx_coded<80:0> is shown in Figure 97–6. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<80>. rx_coded<81> (not shown in the figure) is set to 1 if all parity checks of the Reed-Solomon frame are satisfied, otherwise it is set to 0.

rf_valid

Boolean indication that is set true if received Reed-Solomon frame is valid. The frame is valid if all parity checks of the coded bits are satisfied.

rx_lpi_active

This variable is set true upon detection of LP_IDLE. Set false upon detection of a wake frame.

rx_raw<99:0>

Vector containing 10 successive GMII output transfers. Each transfer is numbered from 0 to 9 with the first transfer numbered as the 0th transfer. The nth GMII transfer is labeled as RX_DV[n], RX_ER[n], RXD[n]<7:0>.
For n = 0 to 9, RX_DV[n] = rx_raw<10n>, RX_ER[n] = rx_raw<10n+1>,
RXD[n]<7:0> = rx_raw<10n+9:10n+2>

rx_wake_frame_complete

This variable is set true at end of WAKE PHY frame, otherwise false.

tx_coded<80:0>

Vector containing the output from the 80B/81B encoder. The format for this vector is shown in Figure 97–5. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<80>.

tx_data_mode

Set true when tx_mode = SEND_N, otherwise false.

tx_lpi_active

This variable is set false at the next wake frame window if any of the following conditions is true:

— a non-LP_IDLE is detected on GMII in any block
— the PHY receives SNR<1:0> set to 01 by its link partner
— the PHY transmits SNR<1:0> set to 01 to its link partner as defined in 97.3.8.2.14

This variable is set true on next PHY frame if all of the following conditions are true:

— an LP_IDLE detected on GMII during the entire last 80B/81B block
— the PHY does not receive SNR<1:0> set to 01 by its link partner
— the PHY does not transmit SNR<1:0> set to 01 to its link partner as defined in 97.3.8.2.14

tx_raw<99:0>

Vector containing 10 successive GMII transfers. Each transfer is numbered from 0 to 9 with the first transfer numbered as the 0th transfer. The nth GMII transfer is labeled as TX_EN[n], TX_ER[n], TXD[n]<7:0>.
For n = 0 to 9, tx_raw<10n> = TX_EN[n], tx_raw<10n+1> = TX_ER[n], tx_raw<10n+9:10n+2
> = TXD[n]<7:0>

tx_sleep_frame_complete

This variable is set to true when PHY is transitioning to the LPI mode and the sleep signal transmission is completed. This variable is set to false when the PHY is transitioning out of the LPI mode.

tx_wake_frame_complete

This variable is set to true at the end of a complete wake frame. This variable is set to false otherwise.

lpi_tx_mode

A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request(tx_symb) interface.
lpi_tx_mode controls tx_symb only when tx_mode is set to SEND_N.
The variable is set to NORMAL when !tx_lpi_active, indicating that the PCS is in the normal power mode of operation.
The variable is set to REFRESH when (tx_lpi_active * tx_refresh active).
The variable is set to QUIET when (tx_lpi_active * !tx_refresh active).

97.3.6.2.3 Functions

DECODE(rx_coded<81:0>)

In the PCS Receive process, this function takes as its argument 82-bit rx_coded<81:0> from the Reed-Solomon decoder and descrambler. If rx_coded<81> = 1 then the decoder decodes the 81B-Reed-Solomon bit vector rx_coded<80:0> returning a vector rx_raw<99:0>, which is sent to the GMII. The DECODE function shall decode the block based on code specified in 97.3.2.2.2. If rx_coded<81> = 0 then the decoder returns EBLOCK_R.

ENCODE(tx_raw<99:0>)

Encodes the 100-bit vector received from the GMII, returning 81-bit vector tx_coded. The ENCODE function shall encode the block as specified in 97.3.2.2.2. The ENCODE function shall only encode LPI_IDLE while in the SEND_LPI state. Otherwise LPI_IDLE is converted to Idle in the ENCODE function.

97.3.6.2.4 Counters

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt

Count number Reed-Solomon frames received during current period.

97.3.6.3 Messages

PCS_status

Indicates whether the PCS is in a fully operational state. (See 97.3.7.1.)

PMA_UNITDATA.indication(rx_symb)

A signal sent by PMA Receive indicating that a PAM3 symbol is available in rx_symb.

PMA_UNITDATA.request(tx_symb)

A signal sent to PMA Transmit indicating that a PAM3 symbol is available in tx_symb.

RX_AGGREGATE
A signal sent to PCS Receive indicating that nine aligned 9-bit Reed-Solomon symbols are aggregated in rx_coded. This signal is asserted even when the receiver is in low power idle mode at the time when the nine 9-bit RS-FEC symbols would be aggregated in rx_coded if the receiver was operating in non-lpi mode.

RX_FRAME
A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

TX_AGGREGATE
A signal sent to PCS Transmit indicating that 10 GMII transfers are aggregated in tx_raw<99:0>.

97.3.6.4 State diagrams

The RFER Monitor state diagram shown in Figure 97–13 monitors the received signal for high PHY frame error ratio. The 80B/81B Transmit state diagram shown in Figure 97–14 controls the encoding of 81B transmitted blocks. It makes exactly one transition for each 81B transmit block processed. The 80B/81B Receive state diagram shown in Figure 97–12 controls the decoding of 81B received blocks. It makes exactly one transition for each receive block processed. The PCS shall perform the functions of PCS Receive, RFER monitor, and PCS Transmit, as specified in Figure 97–12, Figure 97–13, and Figure 97–14, respectively.

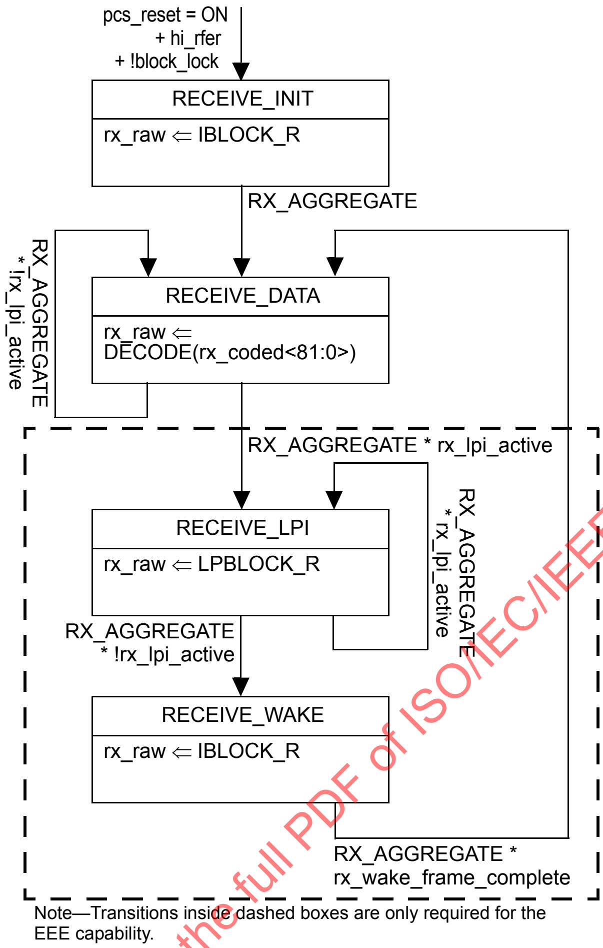


Figure 97–12—PCS Receive state diagram

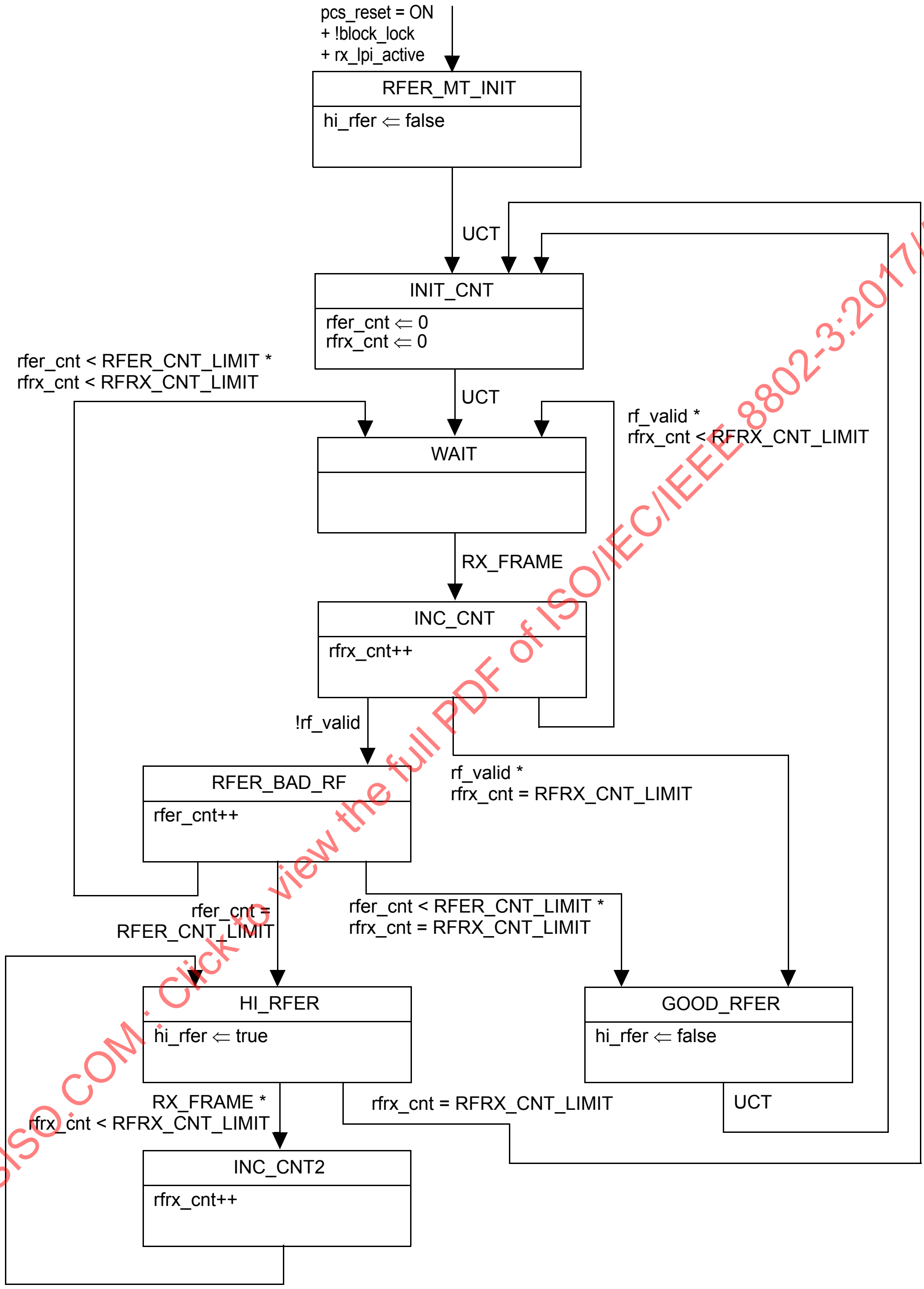
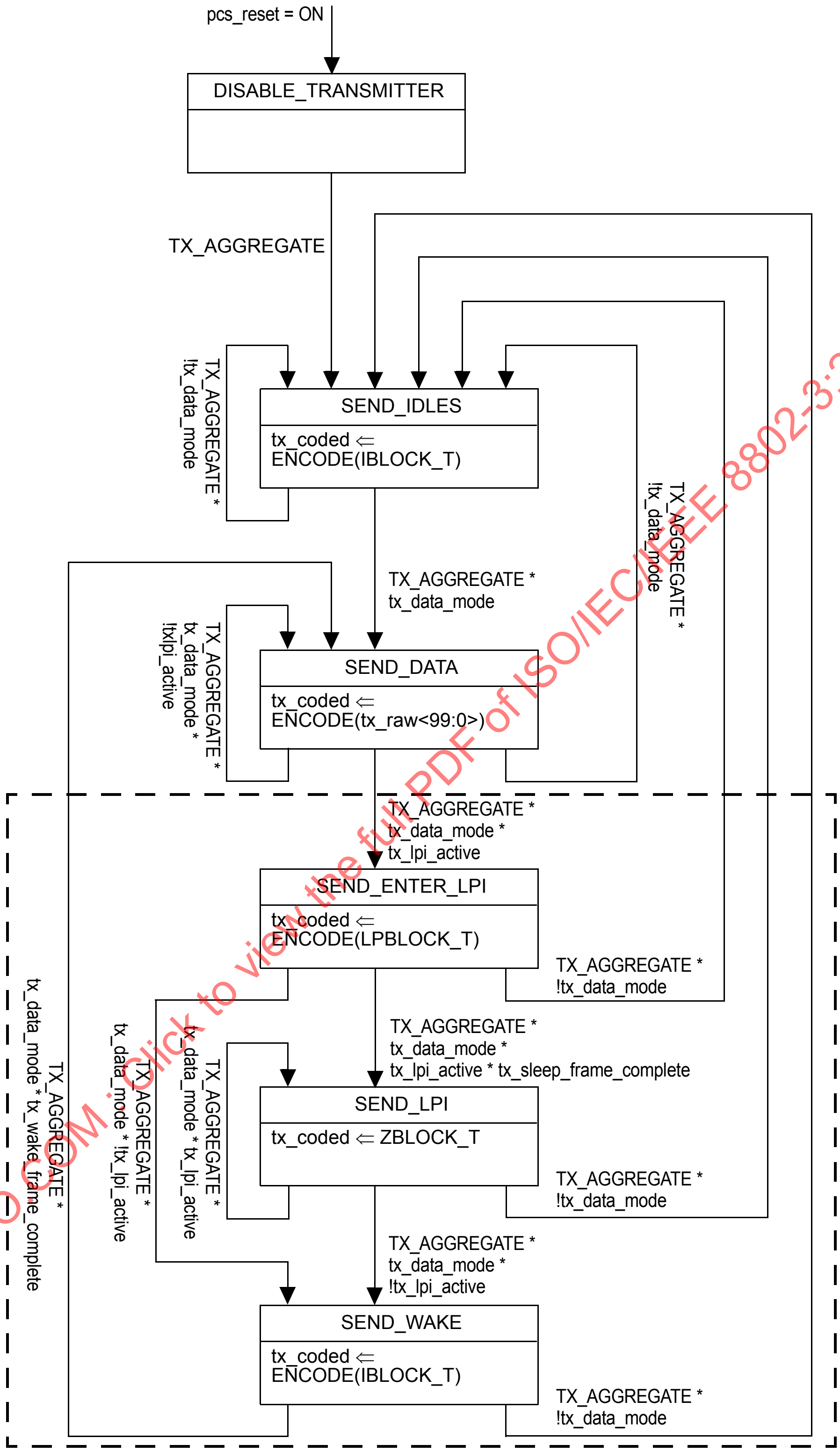


Figure 97–13—RFER monitor state diagram



Note—Transitions inside dashed boxes are only required for the EEE capability.

Figure 97–14—PCS Transmit state diagram

97.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

97.3.7.1 Status

PCS_status:
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_rfer is false. This status is reflected in MDIO register 3.2306.10. A latch low view of this status is reflected in MDIO register 3.2305.2 and the inverse of this status is reflected in MDIO register 3.2305.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.2306.8. A latch low view of this status is reflected in MDIO register 3.2306.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO register 3.2306.9. A latch high view of this status is reflected in MDIO register 3.2306.7.

Rx LPI indication:
: For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to true (register bit set to one) when the PCS Receive state diagram (Figure 97–12) is in the RECEIVE_LPI or RECEIVE_WAKE states. This status is reflected in MDIO register 3.2305.8. A latch high view of this status is reflected in MDIO register 3.2305.10 (Rx LPI received).

Tx LPI indication:
: For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to true (register bit set to one) when the PCS Transmit state diagram (Figure 97–14) is in the SEND_LPI or SEND_WAKE states. This status is reflected in MDIO register 3.2305.9. A latch high view of this status is reflected in MDIO register 3.2305.11 (Tx LPI received).

97.3.7.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time RFER_BAD_RF of the RFER monitor state diagram (see Figure 97–13) is entered. This counter is reflected in MDIO register bits 3.2306.5:0. The counter is reset when register 3.2306 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

97.3.7.3 Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.2304.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the GMII and return it on the receive path to the GMII. In addition, the PCS shall transmit a continuous stream of GMII data to the 81B encoder and on further to the PMA sublayer and shall ignore all data presented to it by the PMA sublayer.

97.3.8 1000BASE-T1 Operations, Administration, and Maintenance (OAM)

The 1000BASE-T1 PCS level Operations, Administration, and Maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. The 1000BASE-T1 OAM information is exchanged in-band between two PHYs using excess bandwidth available on the link. The 1000BASE-T1 OAM is strictly between two 1000BASE-T1 PHYs on the physical layer and their associated management entities if present. Passing 1000BASE-T1 OAM information to other layers is outside the scope of this standard.

1000BASE-T1 OAM is operational as long as both PHYs implement this mechanism and link is up. It continues to be operational during low power idle albeit the information is transferred at a slower rate during the refresh cycle.

The 1000BASE-T1 OAM frame data is carried in the OAM9 field described in 97.3.2.2.4 for the normal power data mode and 97.3.5.3 for low power mode. This 9-bit field is used to exchange 1000BASE-T1 OAM frames. The implementation of 1000BASE-T1 OAM frame exchange function is optional. However, if 1000BASE-T1 EEE is implemented, then the 1000BASE-T1 OAM frame exchange function is implemented to exchange, at a minimum, the link partner health status.

For the remainder of this subclause, the term 1000BASE-T1 OAM is specific to the 1000BASE-T1 PCS level OAM.

97.3.8.1 Definitions

1000BASE-T1 OAM frame: A frame consisting of 12 octets of data with 12 parity bits.

1000BASE-T1 OAM symbol: A 9-bit symbol consisting of one data octet plus a parity bit. Twelve 1000BASE-T1 OAM symbols make up an 1000BASE-T1 OAM frame.

1000BASE-T1 OAM field: The OAM9 field in each PHY frame as described in 97.3.2.2.11 or in each refresh cycle as described in 97.3.5.3.

1000BASE-T1 OAM message: A message contains a 4-bit message number plus 8 octets of message data embedded in an 1000BASE-T1 OAM frame. The same 1000BASE-T1 OAM message can be repeated on multiple 1000BASE-T1 OAM frames.

97.3.8.2 Functional specifications

97.3.8.2.1 1000BASE-T1 OAM Frame Structure

Each 1000BASE-T1 OAM frame is made up of 12 octets of data and 12 parity bits. Each symbol consists of 8 bits of data and one parity bit. The parity bit value for symbol 0 should be such that the sum of the number of 1s in the nine bits is even. The parity bit value for symbols 1 to 11 should be such that the sum of the number of 1s in the nine bits is odd.

	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Even Parity	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Odd Parity	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Odd Parity	Message<0><7:0>							
Symbol 3	Odd Parity	Message<1><7:0>							
Symbol 4	Odd Parity	Message<2><7:0>							
Symbol 5	Odd Parity	Message<3><7:0>							
Symbol 6	Odd Parity	Message<4><7:0>							
Symbol 7	Odd Parity	Message<5><7:0>							
Symbol 8	Odd Parity	Message<6><7:0>							
Symbol 9	Odd Parity	Message<7><7:0>							
Symbol 10	Odd Parity	CRC16							first bit
Symbol 11	Odd Parity	final bit CRC16							

Figure 97–15—OAM Frame

One 1000BASE-T1 OAM symbol is placed in the 9-bit 1000BASE-T1 OAM field in each PHY frame during normal power operation in the data mode. One 1000BASE-T1 OAM symbol is placed in the 9-bit 1000BASE-T1 OAM field in each refresh cycle during low power idle. The 12 1000BASE-T1 OAM symbols are consecutively inserted into 12 consecutive PHY frames and/or refresh cycles. Once the 12 symbols of the current 1000BASE-T1 OAM frame are inserted, the 12 symbols of the next 1000BASE-T1 OAM frame are inserted. This process is continuous without any break in the insertion of 1000BASE-T1 OAM symbols.

Bit 0 of each 1000BASE-T1 OAM symbol is the first bit transmitted in the 9-bit 1000BASE-T1 OAM field. Symbol 0 is the first symbol transmitted in each 1000BASE-T1 OAM frame.

The 1000BASE-T1 OAM frame boundary can be found at the receiver by determining the symbol parity. Symbol 0 has even parity while all other symbols have odd parity.

If 1000BASE-T1 OAM is not implemented then the 9-bit 1000BASE-T1 OAM field shall be set to all 0s. If the link partner does not implement 1000BASE-T1 OAM, the 9-bit 1000BASE-T1 OAM field will remain static and the symbol parity will not change.

97.3.8.2.2 1000BASE-T1 OAM Frame Data

The 1000BASE-T1 OAM frame data is shown in Figure 97–15. OAM<x><y> refers to symbol x, bit y of the 1000BASE-T1 OAM frame. Reserved fields shall be set to 0.

97.3.8.2.3 Ping RX

The Ping RX is indicated in OAM<0><3>.

This bit is set by the PHY to the same value as the Ping TX bit received from the link partner.

97.3.8.2.4 Ping TX

The Ping TX is indicated in OAM<0><2>.

This bit is set by the PHY to for the link partner to echo on Ping RX.

97.3.8.2.5 PHY Health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame
- 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)
- 10: PHY SNR is marginal
- 11: PHY SNR is good

97.3.8.2.6 1000BASE-T1 OAM Message Valid

The 1000BASE-T1 OAM message valid (Valid) is indicated in OAM<1><7>.

- 0: Current 1000BASE-T1 OAM frame does not contain a valid 1000BASE-T1 OAM message
- 1: Current 1000BASE-T1 OAM frame contains a valid 1000BASE-T1 OAM message

97.3.8.2.7 1000BASE-T1 OAM Message Toggle

The 1000BASE-T1 OAM message toggle (Toggle) is indicated in OAM<1><6>.

The toggle bit is used to ensure proper 1000BASE-T1 OAM message synchronization between the PHY and the link partner. The toggle bit in the current 1000BASE-T1 OAM message is set to the opposite value of the toggle bit in the previous 1000BASE-T1 OAM message only if link partner acknowledge the 1000BASE-T1 OAM message is received. This allows one 1000BASE-T1 OAM message to be delineated from a second 1000BASE-T1 OAM message since the same 1000BASE-T1 OAM message may be repeated over multiple 1000BASE-T1 OAM frames. This bit is valid only if Valid is set to 1.

97.3.8.2.8 1000BASE-T1 OAM Message Acknowledge

The 1000BASE-T1 OAM message Acknowledge (Ack) is indicated in OAM<1><5>.

Ack is set by the PHY to let the link partner know that the 1000BASE-T1 OAM message sent by the link partner was successfully received as defined in 97.3.8.2.13 and the PHY is ready to accept a new 1000BASE-T1 OAM message. An 1000BASE-T1 OAM message is defined to be Message_Number<3:0> and Message<7:0><7:0>.

- 0: No Acknowledge
- 1: Acknowledge

97.3.8.2.9 1000BASE-T1 OAM Message Toggle Acknowledge

The 1000BASE-T1 OAM message Toggle Acknowledge (TogAck) is indicated in OAM<1><4>.

TogAck is set by the PHY to let the link partner know which the 1000BASE-T1 OAM message is being acknowledged. TogAck takes the value of Toggle bit of the 1000BASE-T1 OAM message being acknowledged. This bit is valid only if Ack is set to 1.

97.3.8.2.10 1000BASE-T1 OAM Message Number

The 1000BASE-T1 OAM message number is indicated in OAM<1><3:0>.

This field is user-defined but is recommended that it be used to indicate the meaning of the 8-octet message that follows. If used this way, up to 16 different 8-octet messages can be exchanged.

The message number is user-defined and its definition is outside the scope of this standard.

97.3.8.2.11 1000BASE-T1 OAM Message Data

The 1000BASE-T1 OAM message data is indicated in OAM<9:2><7:0>.

The 8-octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the 1000BASE-T1 OAM frame sent by the link partner is successfully received as defined The 1000BASE-T1 OAM frame octet is the lower 8 bits of the 9-bit 1000BASE-T1 OAM symbol. Twelve octets form the 1000BASE-T1 OAM data.

97.3.8.2.12 CRC16

The CRC16 is indicated in OAM<11:10><7:0>.

The CRC16 implements the polynomial $(x+1)(x^{15}+x+1)$ of the previous 10 octets. The CRC16 shall produce the same result as the implementation shown in Figure 97–16. The 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards OEM<9:0><7:0> presented in their transmitted order as described in 97.3.8.2.1 are used to compute the CRC16 with the switch connected, which is setting CRC gen in Figure 97–16. Note that the parity bit is not used in the CRC16 calculation. After all the 10 octets have been processed, the switch is disconnected (setting CRC out) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0. S15 is indicated in OAM<10><0> and S0 is indicated in OAM<11><7>.

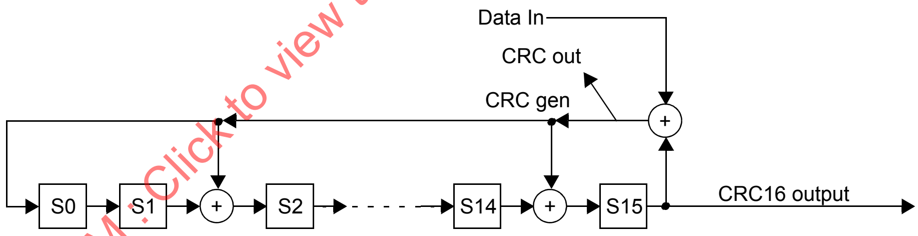


Figure 97–16—1000BASE-T1 OAM CRC16

97.3.8.2.13 1000BASE-T1 OAM Frame Acceptance Criteria

All fields of the 1000BASE-T1 OAM frame shall be accepted and updated, unless any of the following occurs:

a) Incorrect parity on any of the 12 symbols
b) Incorrect CRC16
c) Uncorrectable PHY frame on any of the 12 symbols

97.3.8.2.14 PHY Health Indicator

The PHY current health is sent to the link partner on a per 1000BASE-T1 OAM frame basis using the SNR<1:0> bits as described in 97.3.8.2.5. It lets the link partner have an early indication of potential problems that may cause the PHY to drop link or have high error rates.

If EEE is implemented, there may be a case where a PHY's receiver can no longer maintain good SNR based on quiet/refresh cycles. Instead of dropping the link, the PHY can attempt to recover the link by forcing the link partner to exit LPI in its egress direction so that the PHY can use normal power mode to recover. This is done by transmitting SNR<1:0> with a value of 01.

If a PHY receives SNR<1:0> set to 01 by its link partner, then it cannot enter into LPI in the egress direction. If the PHY is already in LPI then the PHY shall immediately exit LPI.

97.3.8.2.15 Ping

The PingTx bit is set based on the value in mr_tx_ping. The PingRx bit is set based on the latest PingTx received from the link partner. The value in mr_rx_ping is set based on the received PingRx from the link partner. The user can determine that the link partner 1000BASE-T1 OAM is operating properly by togging mr_tx_ping and observing mr_rx_ping matches after a short delay.

The Ping bits are updated on a per 1000BASE-T1 OAM frame basis.

97.3.8.2.16 1000BASE-T1 OAM Message Exchange

Unlike the PHY health indicator and the ping function that operate on a per 1000BASE-T1 OAM frame basis, the 1000BASE-T1 OAM message exchange operates on a per 1000BASE-T1 OAM message basis that will occur over many 1000BASE-T1 OAM frames. The 1000BASE-T1 OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass 1000BASE-T1 OAM messages and verify their delivery.

The 1000BASE-T1 OAM message is first written into the 1000BASE-T1 OAM transmit registers in the PHY. The 1000BASE-T1 OAM message is then read out of the 1000BASE-T1 OAM transmit registers and transmitted to the link partner. After the link partner receives the 1000BASE-T1 OAM message it transfers it into the link partner's 1000BASE-T1 OAM receive registers and also sends an acknowledge back to the PHY indicating that the next 1000BASE-T1 OAM message can be transmitted. One 1000BASE-T1 OAM message can be loaded into the 1000BASE-T1 OAM transmit registers while another 1000BASE-T1 OAM message is being transmitted by the PHY to the link partner while yet another 1000BASE-T1 OAM message is being read out at the link partner's 1000BASE-T1 OAM receive registers. The exchange of 1000BASE-T1 OAM messages are occurring concurrently and bi-directionally.The transfers between the management entities can be done asynchronously. On the transmit side mr_tx_valid = 0 indicates that the next 1000BASE-T1 OAM message can be written into the 1000BASE-T1 OAM transmit registers. Once the registers are written the management entity sets mr_tx_valid to 1 to indicate that the 1000BASE-T1 OAM transmit registers contains a valid 1000BASE-T1 OAM message. Once the message is read out atomically, the state machine clears the mr_tx_valid to 0 to indicate that the registers are ready to accept the next 1000BASE-T1 OAM message.

On the receive side mr_rx_lp_valid indicates that valid 1000BASE-T1 OAM message can be read from the 1000BASE-T1 OAM receive registers. Once these registers are read, the mr_rx_lp_valid should be cleared to 0 to indicate that the registers are ready to receive the next 1000BASE-T1 OAM message. If mr_rx_lp_valid is not cleared then the 1000BASE-T1 OAM message transfer will eventually stall since the sender cannot send new 1000BASE-T1 OAM messages if the receiver does not acknowledge that an 1000BASE-T1 OAM message has been transferred into the 1000BASE-T1 OAM receive registers.

The management entities can asynchronously read mr_tx_valid and mr_rx_lp_valid to know when 1000BASE-T1 OAM messages can be transferred in and out of the 1000BASE-T1 OAM registers.

The toggle bit alternates between 0 and 1, which lets the management entity determine which 1000BASE-T1 OAM message is being referred to. The toggle bit transitioning rules between one 1000BASE-T1 OAM frame to the next 1000BASE-T1 OAM frame are shown in Table 97–5.

Table 97–5—Toggle bit transition rules

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
0	0	0	0	No valid 1000BASE-T1 OAM message
0	0	0	1	Illegal transition (Error)
0	0	1	0	New 1000BASE-T1 OAM message starting
0	0	1	1	Illegal transition (Error)
0	1	0	0	Illegal transition (Error)
0	1	0	1	No valid 1000BASE-T1 OAM message
0	1	1	0	Illegal transition (Error)
0	1	1	1	New 1000BASE-T1 OAM message starting
1	0	0	0	Illegal transition (Error)
1	0	0	1	Received acknowledge, no new 1000BASE-T1 OAM message to send
1	0	1	0	Repeating current 1000BASE-T1 OAM message, waiting for link partner's acknowledge
1	0	1	1	Previous 1000BASE-T1 OAM message ending, new 1000BASE-T1 OAM message starting
1	1	0	0	Received acknowledge, no new 1000BASE-T1 OAM message to send
1	1	0	1	Illegal transition (Error)
1	1	1	0	Previous 1000BASE-T1 OAM message ending, new 1000BASE-T1 OAM message starting
1	1	1	1	Repeating current 1000BASE-T1 OAM message, waiting for link partner's acknowledge

97.3.8.3 State diagram variable to 1000BASE-T1 OAM register mapping

The state diagrams of Figure 97–18 and Figure 97–17 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface to communicate the 1000BASE-T1 OAM information to and from the management entity. Clause 45 MDIO registers are defined in MMD3 to support the 1000BASE-T1 OAM. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended. Table 97–6 describes the MDIO register to the state diagrams variable mapping.

Table 97–6—State Variables to 1000BASE-T1 OAM Register Mapping

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
1000BASE-T1 OAM Message Valid	1000BASE-T1 OAM transmit register	3.2308.15	mr_tx_valid
Toggle Value	1000BASE-T1 OAM transmit register	3.2308.14	mr_tx_toggle
1000BASE-T1 OAM Message Received	1000BASE-T1 OAM transmit register	3.2308.13	mr_tx_received
Received Message Toggle Value	1000BASE-T1 OAM transmit register	3.2308.12	mr_tx_received_toggle
Message Number	1000BASE-T1 OAM transmit register	3.2308.11:8	mr_tx_message_num[3:0]
Ping Received	1000BASE-T1 OAM transmit register	3.2308.3	mr_rx_ping
Ping Transmit	1000BASE-T1 OAM transmit register	3.2308.2	mr_tx_ping
Local SNR	1000BASE-T1 OAM transmit register	3.2308.1:0	mr_tx_SNR[1:0]
1000BASE-T1 OAM Message 0	1000BASE-T1 OAM message register	3.2309.7:0	mr_tx_message[7:0]
1000BASE-T1 OAM Message 1	1000BASE-T1 OAM message register	3.2309.15:8	mr_tx_message[15:8]
1000BASE-T1 OAM Message 2	1000BASE-T1 OAM message register	3.2310.7:0	mr_tx_message[23:16]
1000BASE-T1 OAM Message 3	1000BASE-T1 OAM message register	3.2310.15:8	mr_tx_message[31:24]
1000BASE-T1 OAM Message 4	1000BASE-T1 OAM message register	3.2311.7:0	mr_tx_message[39:32]
1000BASE-T1 OAM Message 5	1000BASE-T1 OAM message register	3.2311.15:8	mr_tx_message[47:40]
1000BASE-T1 OAM Message 6	1000BASE-T1 OAM message register	3.2312.7:0	mr_tx_message[55:48]
1000BASE-T1 OAM Message 7	1000BASE-T1 OAM message register	3.2312.15:8	mr_tx_message[63:56]
Link Partner 1000BASE-T1 OAM Message Valid	1000BASE-T1 OAM receive register	3.2313.15	mr_rx_lp_valid
Link Partner Toggle Value	1000BASE-T1 OAM receive register	3.2313.14	mr_rx_lp_toggle

Table 97–6—State Variables to 1000BASE-T1 OAM Register Mapping *(continued)*

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
Link Partner Message Number	1000BASE-T1 OAM receive register	3.2313.11:8	mr_rx_lp_message_-num[3:0]
Link Partner SNR	1000BASE-T1 OAM receive register	3.2313.1:0	mr_rx_lp_SNR[1:0]
Link Partner 1000BASE-T1 OAM Message 0	Link partner 1000BASE-T1 OAM message register	3.2314.7:0	mr_rx_lp_message[7:0]
Link Partner 1000BASE-T1 OAM Message 1	Link partner 1000BASE-T1 OAM message register	3.2314.15:8	mr_rx_lp_message[15:8]
Link Partner 1000BASE-T1 OAM Message 2	Link partner 1000BASE-T1 OAM message register	3.2315.7:0	mr_rx_lp_message[23:16]
Link Partner 1000BASE-T1 OAM Message 3	Link partner 1000BASE-T1 OAM message register	3.2315.15:8	mr_rx_lp_message[31:24]
Link Partner 1000BASE-T1 OAM Message 4	Link partner 1000BASE-T1 OAM message register	3.2316.7:0	mr_rx_lp_message[39:32]
Link Partner 1000BASE-T1 OAM Message 5	Link partner 1000BASE-T1 OAM message register	3.2316.15:8	mr_rx_lp_message[47:40]
Link Partner 1000BASE-T1 OAM Message 6	Link partner 1000BASE-T1 OAM message register	3.2317.7:0	mr_rx_lp_message[55:48]
Link Partner 1000BASE-T1 OAM Message 7	Link partner 1000BASE-T1 OAM message register	3.2317.15:8	mr_rx_lp_message[63:56]

97.3.8.4 Detailed functions and State Diagrams

97.3.8.4.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

97.3.8.4.2 State diagram parameters

97.3.8.4.3 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_rx_lp_message[63:0]
: Eight octet 1000BASE-T1 OAM message from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1.

mr_rx_lp_message_num[3:0]
Four bit message number from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1.

mr_rx_lp_SNR[1:0]
Link partner health status.
Values:
- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame
- 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).
- 10: PHY SNR is marginal
- 11: PHY SNR is good

The threshold for the status is implementation dependent.

mr_rx_lp_toggle
The toggle bit value associated with the eight octet 1000BASE-T1 OAM message from the link partner.
Values:
The toggle bit alternates between 0 and 1.

mr_rx_lp_valid
Indicates whether 1000BASE-T1 OAM message in mr_rx_lp_message[63:0], mr_rx_lp_message_num[3:0] and the toggle bit in mr_rx_lp_toggle is valid or not. This variable should be cleared when mr_rx_lp_message[63:48] is read and is not explicitly shown in the state machine. The clearing of this variable indicates to the state machine that the 1000BASE-T1 OAM message is read by the user and the state machine can proceed to load in the next 1000BASE-T1 OAM message.
Values:
- 0: invalid
- 1: valid

mr_rx_ping
Echoed ping value from the link partner.
Values:
The value can be 0 or 1.

mr_tx_message[63:0]
Eight octet 1000BASE-T1 OAM message transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is 1.

mr_tx_message_num[3:0]
Four bit message number transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is 1.

mr_tx_ping
Ping value transmitted by the local PHY.
Values:
The value can be 0 or 1.

mr_tx_received
Indicates whether the most recently transmitted 1000BASE-T1 OAM message with a toggle bit value of mr_tx_received_toggle was received, read, and acknowledged by the link partner. This variable shall clear on read.

Values:
- 0: 1000BASE-T1 OAM message not received and read by the link partner
- 1: 1000BASE-T1 OAM message received by the link partner

mr_tx_received_toggle

Toggle bit value of the 1000BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if mr_tx_received is 1.

Values:

The value can be 0 or 1.

mr_tx_SNR[1:0]

Status register indicating PHY health status.

Values:
- 00: PHY link is failing and will drop link and relink within 2 to 4 ms after the end of the current 1000BASE-T1 OAM frame
- 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)
- 10: PHY SNR is marginal
- 11: PHY SNR is good

The threshold for the status is implementation dependent.

mr_tx_toggle

The toggle bit value associated with the eight octet 1000BASE-T1 OAM message transmitted by the PHY. The value is automatically set by the state machine and cannot be set by the user. This bit should be read and recorded prior to setting mr_tx_valid to 1.

Values:

The toggle bit alternates between 0 and 1.

mr_tx_valid

Indicates whether 1000BASE-T1 OAM message in mr_tx_message[63:0] and mr_rx_lp_message_num[3:0] is valid or not. This register will be cleared by the state machine to indicate whether the next 1000BASE-T1 OAM message can be written into the registers.

Values:
- 0: invalid
- 1: valid

reset

Reset

Values:
- false: 1000BASE-T1 OAM circuit not in reset
- true: 1000BASE-T1 OAM circuit is in reset

rx_ack

Acknowledge from link partner in response to PHY’s 1000BASE-T1 OAM message.

Values:
- 0: no acknowledge
- 1: acknowledge

rx_ack_toggle

The toggle value corresponding to the PHY’s 1000BASE-T1 OAM message that the link partner is acknowledging. This value is valid only if the rx_ack is set to 1.

Values:

The toggle bit can take on values of 0 or 1.

rx_boundary
This variable is set to true whenever the receive data stream reaches the end of a Reed-Solomon frames during normal power operation in the data mode, or at the end of a received refresh cycle during low power idle operation. This variable is set to false at other times.
Values:
false: receive stream not at a boundary end
true: receive stream at a boundary end

rx_exp_toggle
This variable holds the expected toggle value of the next 1000BASE-T1 OAM message. This is normally the opposite value of the current toggle value, but shall reset on error conditions where two back to back 1000BASE-T1 OAM messages separated by 1000BASE-T1 OAM frames without a valid message have the same toggle value.
Values:
The toggle bit can take on values of 0 or 1.

rx_lp_ack
Acknowledge from PHY in response to link partner's 1000BASE-T1 OAM message. Indicates whether valid 1000BASE-T1 OAM message from the link partner has been sampled into the PHY's registers.
Values:
0: no acknowledge / not sampled
1: acknowledge / sampled

rx_lp_ping
Ping value received from the link partner that should be looped back.
Values:
The value can be 0 or 1.

rx_lp_toggle
The toggle bit value in the previous 1000BASE-T1 OAM frame received from the link partner.
Values:
The toggle bit alternates between 0 and 1.

rx_lp_valid
Indicates whether 1000BASE-T1 OAM message in previous 1000BASE-T1 OAM frame received from the link partner is valid or not.
Values:
0: invalid
1: valid

rx_oam_field<8:0>
Nine bit 1000BASE-T1 OAM symbol extracted from a received Reed-Solomon frame during normal power operation in the data mode, or from a received refresh cycle during low power idle operation.

rx_oam<11 to 0><8:0>
Raw 12 symbol 1000BASE-T1 OAM frame received from the link partner.

SNR[1:0]

PHY health status.

Values:

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame
- 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)
- 10: PHY SNR is marginal
- 11: PHY SNR is good

Both the status threshold and condition for generating this status are implementation dependent.

tx_boundary

This variable is set to true whenever the transmit data stream reaches the start of a PHY frame during normal power operation in the data mode, or at the start of a transmit refresh cycle during low power idle operation. This variable is set to false at other times.

Values:

- false: transmit stream not at a boundary end
- true: transmit stream at a boundary end

tx_oam_field<8:0>

Nine bit 1000BASE-T1 OAM symbol inserted into a transmitted Reed-Solomon frame during normal power operation in the data mode, or into a transmitted refresh cycle during low power idle operation.

tx_oam<11 to 0><8:0>

Raw 12 symbol 1000BASE-T1 OAM frame transmitted from the PHY.

tx_lp_ready

Indicates whether the link partner is ready to receive the next 1000BASE-T1 OAM message from the PHY. If ready, then the PHY will load the next 1000BASE-T1 OAM message from the registers and begin transmitting them.

Values:

- 0: not ready
- 1: ready

tx_toggle

The toggle bit value being send in the current 1000BASE-T1 OAM frame transmitted by the PHY.

Values:

The value can be 0 or 1.

97.3.8.4.4 Counters

rx_cnt

A count of received 1000BASE-T1 OAM frames.

Values:

The value can be any integer from 0 to 12, inclusive.

tx_cnt

1000BASE-T1 OAM frame transmit symbol count.

Values:

The value can be any integer from 0 to 12, inclusive.

97.3.8.4.5 Functions

CRC16(10 octets)
This function outputs a 16-bit CRC value using 10-octet input as defined in 97.3.8.2.12.

CRC16_Check(12 octets)
This function checks whether the 12-octet frame has the correct CRC16 as defined in 97.3.8.2.12.
Values:

BAD:	CRC16 check is bad
GOOD:	CRC16 check is good

Parity(12 octets)
This function outputs 12 parity bits, one for each of the 12 input octets. An even parity bit is output for the first octet, and odd parity bits are output for each of the remaining 11 octets.

Parity_Check(9-bit symbol)
This function calculates the bit parity of the 9-bit symbol.
Values:

Even:	symbol has even parity
Odd:	symbol has odd parity

97.3.8.4.6 State Diagrams

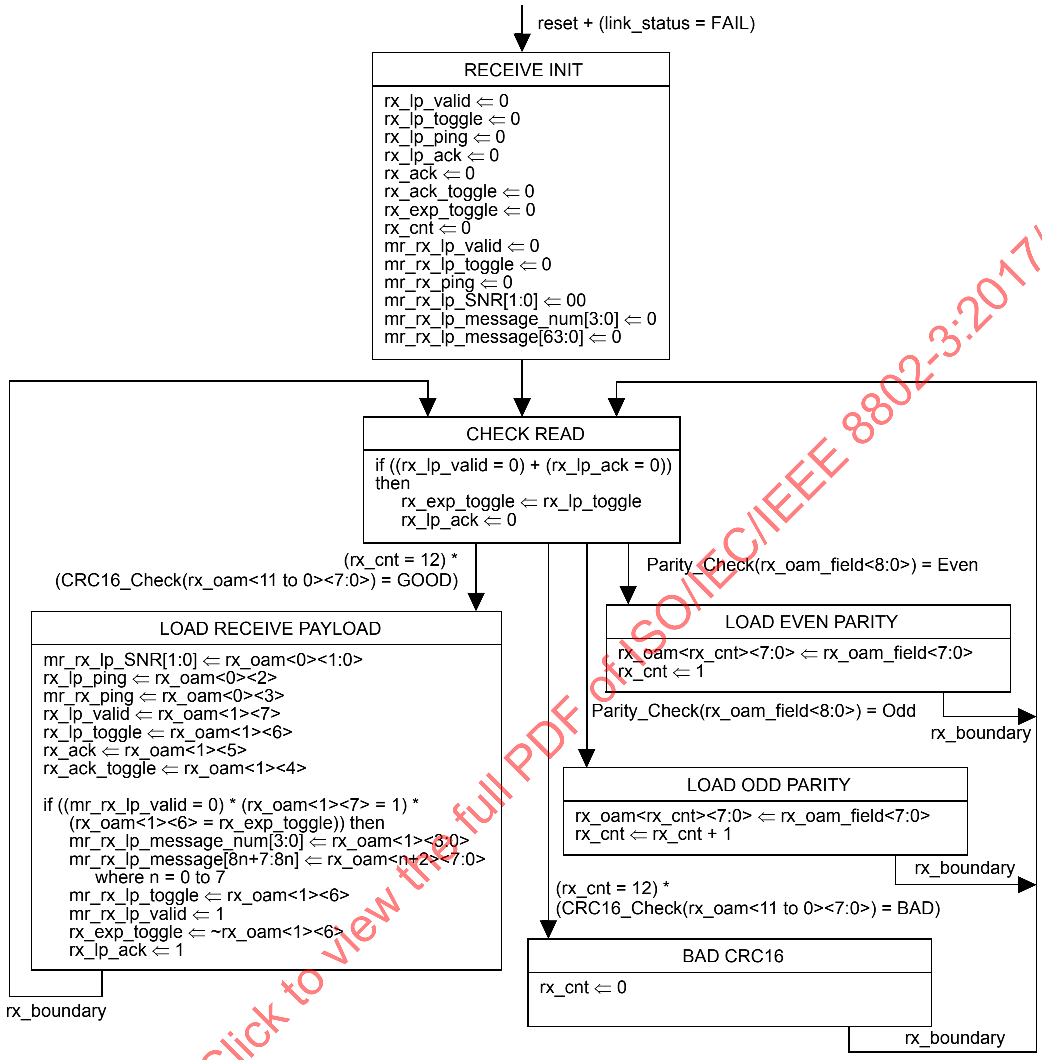


Figure 97–17—Receive state diagram

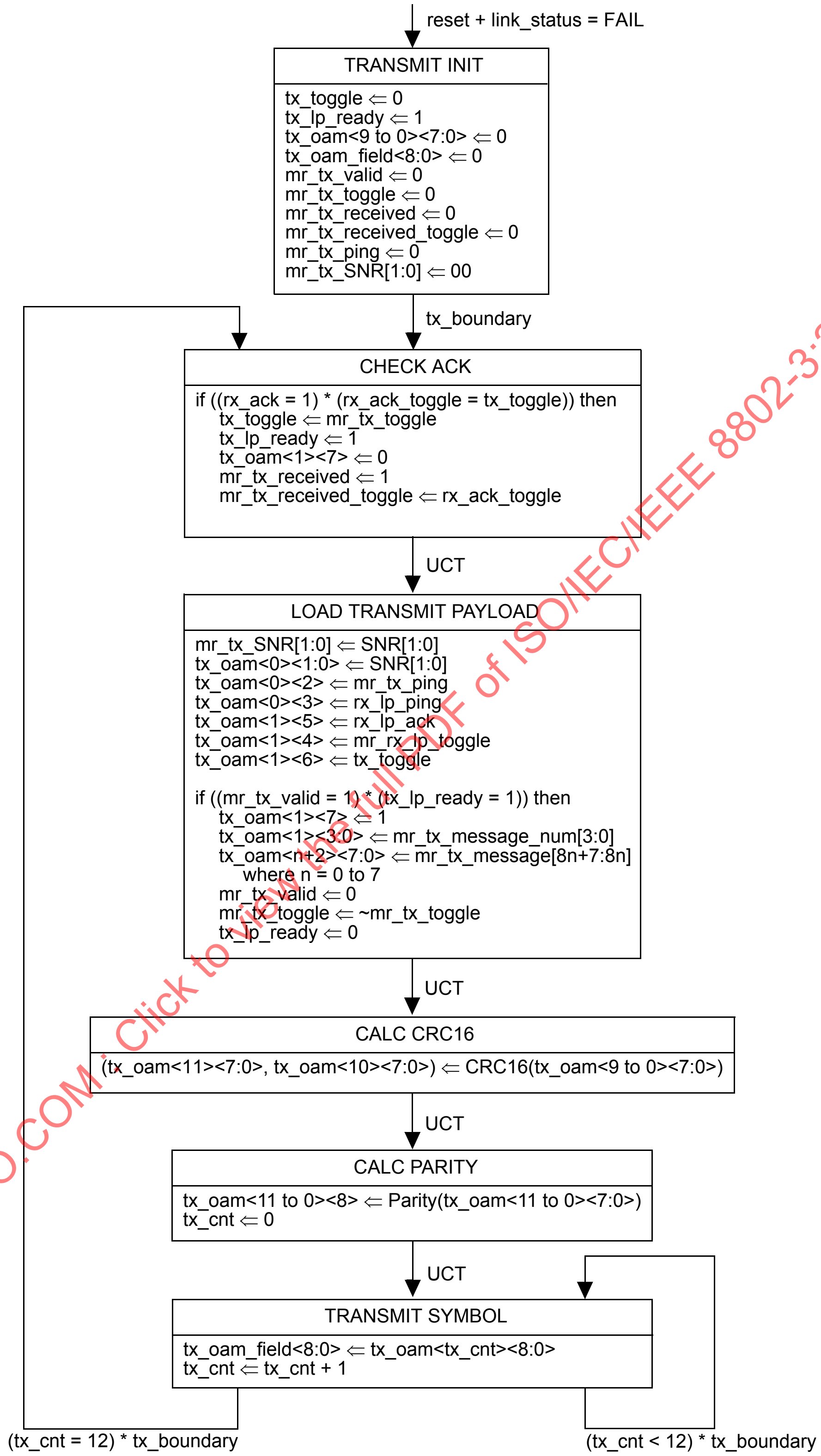


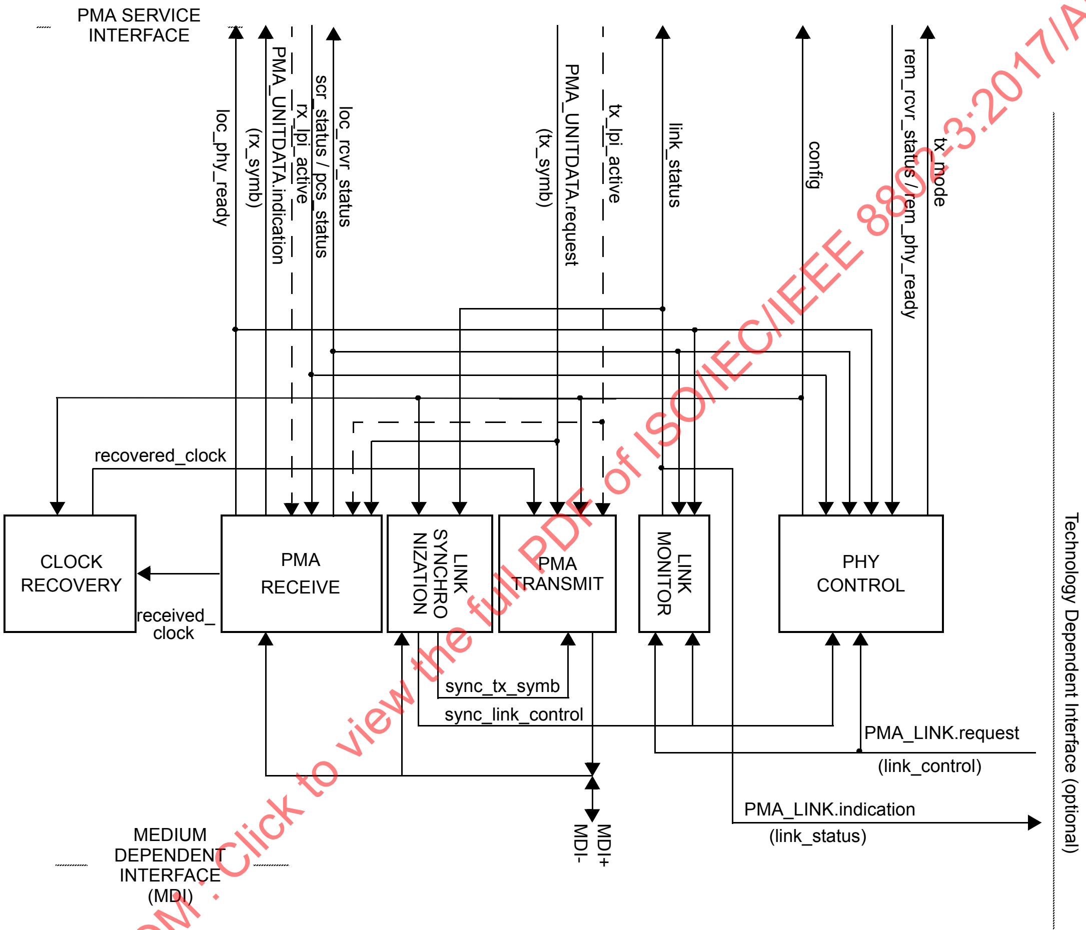
Figure 97–18—Transmit state diagram

97.4 Physical Medium Attachment (PMA) sublayer

97.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 97.2.2 to the 1000BASE-T1 baseband medium, specified in 97.5.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 97.7.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 97–19—PMA reference diagram

97.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 97–19, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 97–19.

97.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state
b) The receipt of a request for reset from the management entity

PMA Reset sets pma_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

97.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a three level modulated signal on the single twisted-pair copper cable. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb when sync_link_control = ENABLE, or the sync_tx_symb output by the PHY Link Synchronization function when sync_link_control = DISABLE, after processing with optional transmit filtering, digital-to-analog conversion (DAC) and subsequent analog filtering. The signals generated by PMA Transmit shall comply with the electrical specifications given in 97.5.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 97.5.3.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 97.4.2.8 while meeting the jitter requirements of 97.5.3.3.

97.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to true, this function shall turn off the transmitter so that the transmitter Average Launch Power of the Transmitter is less than –53 dBm.

97.4.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM3 signals on the twisted-pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the twisted-pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 3.6×10^{-7} after RS-FEC decoding, over a channel meeting the requirements of 97.6.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb is needed to perform echo cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other values (see PHY Control state diagram in Figure 97–26). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.134.6.

97.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 97–26.

During PMA training (TRAINING and COUNTDOWN states in Figure 97–26), PHY Control information is exchanged between link partners with a 12-octet InfoField, which is XORed with the first 96 bits of the 15th partial PHY frame (bits 2520 to 2615) of the PHY frame. The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM3 transition.

The 12-octet InfoField shall include the fields in 97.4.2.4.2 through 97.4.2.4.8, also shown in the overview Figure 97–20, and the more detailed Figure 97–21 and Figure 97–22. Each InfoField shall be transmitted at least 256 times to ensure detection at link partner.

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10			octets 11/12
0xBB	0xA7	0x00	PFC24	Message	MSG24	MSG24	MSG24	CRC16

Figure 97–20—InfoField format

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	SeedUsrCfgCap	CRC16

Figure 97–21—InfoField TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 97–22—InfoField COUNTDOWN format

97.4.2.4.1 InfoField notation

For all the InfoField notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The InfoField is transmitted following the notation described in 97.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

97.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 3 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Oct1<7:0> and so forth.

97.4.2.4.3 Partial PHY frame Count (PFC24)

The start of partial PHY frame Count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 15 partial PHY frames per PHY frame and the InfoField is embedded within the 15th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 14.

97.4.2.4.4 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 97–7 for the MASTER and Table 97–8 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 97–7 for the MASTER and the first or second row of Table 97–8 for the SLAVE. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the InfoField variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 97–7—InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 97–8—InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

97.4.2.4.5 PHY Capability Bits, User Configurable Register, and Data Mode Scrambler Seed

When PMA_state<7:6> = 00, then [0ct8<7:0>, 0ct9<7:0>, 0ct10<7:0>] contains the two PHY capability bits, the user configurable register bits, and the 15-bit data mode scrambler seed (Seed). Each octet is sent LSB first.

The format of PHY capability bits is Oct9<7> = EEEen and Oct10<0> = OAMen, indicating EEE and 1000BASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of optional capabilities by setting the corresponding capability bits.

The data mode scrambler seed contains bits S14 (sent first) to S0 (sent last) to indicate the initial state of the data mode transmit scrambler of the local device upon reaching the data switch partial PHY frame count. The state of the scrambler in Figure 97–9 shall be S14:S0 at the first bit of the first PHY frame when the partial PHY frame counter equals to the DataSwPFC24 value, see 97.4.2.4.6. The format of Seed is Oct8<7:0> = S<7:14> and Oct9<6:0> = S<0:6>. Seed S<14:0> shall not be all zeros.

The remaining 7-bit Oct10<7:1> form a user-configurable register. See 97.4.2.4.11 for details.

97.4.2.4.6 Data Switch partial PHY frame Count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from PAM2 to PAM3, which occurs at the start of an RS-FEC block. The last value of PFC24 prior to the transition is DataSwPFC24 - 1. DataSwPFC24 shall be set to an integer multiple of 15. This value of DataSwPFC24 guarantees that the switch from PAM2 to PAM3 occurs on a PHY frame boundary.

97.4.2.4.7 Reserved Fields

When PMA_state<7:6> is greater than 01, then [Oct8<1:0>, Oct9<1:0>, Oct10<7:0>] contains a reserved field. All InfoField fields denoted Reserved are reserved for future use.

97.4.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 97–23. In Figure 97–23 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct4 through Oct10 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 97–23. After all the 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

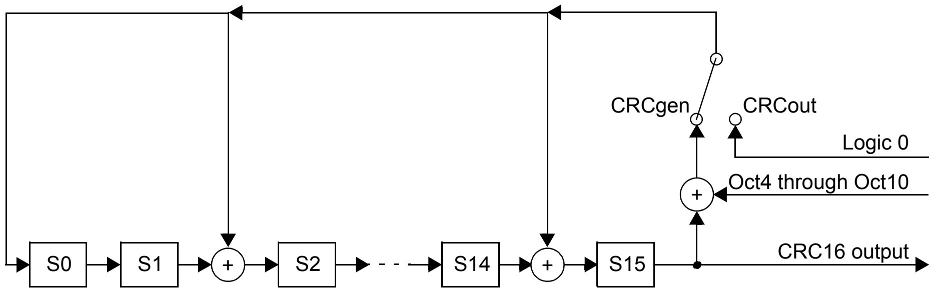


Figure 97–23—CRC16

97.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 97–9. Mapping of MDIO status variables to PMA status variables is shown in Table 97–10.

Table 97–9—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1 / 1000BASE-T1 PMA control register	1.0.15 / 1.2304.15	pma_reset
Transmit disable	1000BASE-T1 PMA control register	1.2304.14	PMA_transmit_disable

Table 97–10—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	1000BASE-T1 PMA status register	1.2305.1	PMA_receive_fault

97.4.2.4.10 Start-up sequence

The start-up sequence shall comply with the state diagram description given in Figure 97–26. If the Auto-Negotiation function is not implemented, or mr_autoneg_en = false, PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

The Auto-Negotiation function is optional for 1000BASE-T1 PHYs. If the Auto-Negotiation function is used, during the Auto-Negotiation process PHY Control is in the DISABLE_TRANSMITTER state and the transmitter is disabled. If the Auto-Negotiation function is not used, during the PHY Link Synchronization stage the PHY Control remains in the DISABLE_TRANSMITTER state and the Link Synchronization function (see 97.4.2.6) is the data source for the PMA Transmit function.

When the Auto-Negotiation asserts link_control = ENABLE, or PHY Link Synchronization process asserts sync_link_control = ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering the INIT_MAXWAIT_TIMER state, the maxwait_timer is started. PHY Control then transitions to the SILENT state where the minwait_timer is started and the PHY transmits zeros (tx_mode = SEND_Z).

In MASTER mode PHY Control transitions to the TRAINING state once the minwait_timer expires.

Upon entering the TRAINING state, the minwait_timer is started and the PHY Control asserts tx_mode = SEND_T sending PAM2 together with InfoFields. The PHY Control also sets PMA_state = 00 and sends the PHY capability bits, the user configurable register bits, and the Seed value used by the local device for the data mode scrambler initialization, see 97.4.2.4.5.

The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen = 1. The optional 1000BASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx = 0, which is communicated to the link partner via the InfoField. After the MASTER has sufficiently converged the necessary circuitry, the MASTER shall set en_slave_tx = 1 to allow the SLAVE to transition to TRAINING.

In SLAVE mode PHY Control transitions to the TRAINING state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin = OK. The SLAVE shall align its transmit 81B-RS frame to within +0/–1 partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE InfoField partial PHY frame Count shall match the MASTER InfoField partial PHY frame Count for the aligned frame.

Upon entering TRAINING state the SLAVE initially sets timing_lock_OK = 0 until it has acquired timing lock at which point the SLAVE sets timing_lock_OK = 1.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner’s value for loc_rcvr_status is stored in the local device parameter rem_rcvr_status. Upon expiration of the minwait_timer and when the condition loc_rcvr_status = OK and rem_rcvr_status = OK is satisfied, PHY control transitions to the COUNTDOWN state.

Upon entering the COUNTDOWN state, PHY Control sets PMA_state = 01 and DataSwPFC24 to the value of the partial PHY frame count when the transmitter switches from PAM2 to PAM3.

Upon reaching DataSwPFC24 partial PHY frame count PHY Control transitions to the SEND_IDLE1 state and forces transmission into the idle mode by asserting tx_mode = SEND_I.

Once the link partner has transitioned from PAM2 to PAM3, PHY Control transitions to the SEND_IDLE2 state and starts the minwait_timer.

Upon expiration of the minwait_timer and when the condition loc_phy_ready = OK and rem_phy_ready = OK is satisfied, PHY control transitions to the SEND_DATA state.

Upon entering the SEND_DATA state, PHY Control starts the minwait_timer and enables frame transmission to the link partner by asserting tx_mode = SEND_N.

The operation of the maxwait_timer requires that the PHY complete the start-up sequence from state INIT_MAXWAIT_TIMER to SEND_DATA in the PHY Control state diagram state diagram (Figure 97–26) in less than 97.5 ms to avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure 97–27).

97.4.2.4.11 PHY Control Registers

The PHY control registers are shown in Table 97–11.

Table 97–11—PHY Control Registers

MDIO control/status variable	PMA register name	Register/ bit number	PMA control/status variable
MASTER-SLAVE	BASE-T1 PMA/PMD control register	1.2100.14	force_config (see 97.4.2.6.1)
Type selection	BASE-T1 PMA/PMD control register	1.2100.3:0	force_PHY_type (see 97.4.2.6.1)
1000BASE-T1 OAM Ability	1000BASE-T1 PMA status register	1.2305.11	
EEE Ability	1000BASE-T1 PMA status register	1.2305.10	
User Field	1000BASE-T1 training register	1.2306.10:4	PMA_state<7:6> = 00, Oct10<7:1>
1000BASE-T1 OAM Advertisement	1000BASE-T1 training register	1.2306.1	PMA_state<7:6> = 00, Oct10<0>
EEE Advertisement	1000BASE-T1 training register	1.2306.0	PMA_state<7:6> = 00, Oct9<7>
Link Partner User Field	1000BASE-T1 link partner training register	1.2307.10:4	LP PMA_state<7:6> = 00, Oct10<7:1>
Link Partner 1000BASE-T1 OAM Advertisement	1000BASE-T1 link partner training register	1.2307.1	LP PMA_state<7:6> = 00, Oct10<0>
Link Partner EEE Advertisement	1000BASE-T1 link partner training register	1.2307.0	LP PMA_state<7:6> = 00, Oct9<7>

97.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the auto-negotiation (if enabled) or synchronization (if auto-negotiation is not enabled) process.

The Link Monitor function shall comply with the state diagram of Figure 97–27.

Upon power on, reset, or release from power down, the Auto-Negotiation function set link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. During this period, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote 1000BASE-T1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state machines begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, the variable link_status = OK is asserted, upon which further PHY operations can take place.

97.4.2.6 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function is responsible for establishing the start of PHY PMA training as defined in 97.4.2.4.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 97.4.2.2), and generates a signal, SEND_S, used by the MASTER and SLAVE to discover the link partner and synchronize the start of PMA training.

Link Synchronization employs the SEND_S signal to achieve synchronization prior to link training. If the PHY is configured as MASTER, Link Synchronization shall employ Equation (97–8) as the PN sequence generator.

$$p_M(x) = x^8 + x^4 + x^3 + x^2 + 1 \qquad (97\text{–}8)$$

If the PHY is configured as SLAVE, Link Synchronization shall employ Equation (97–9) as PN sequence generator.

$$p_{MS}(x) = x^8 + x^6 + x^5 + x^4 + 1 \qquad (97\text{–}9)$$

The period of both PN sequences is 255.

An implementation of MASTER and SLAVE PHY SEND_S PN sequence generators by linear-feedback shift registers is shown in Figure 97–24. The bits stored in the shift register delay line at time n are denoted by Sn[7:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Sn[0] is generated. The PN sequence generator shift registers shall be reset to a non-zero value upon entering into the TRANSMIT_DISABLE state (see Figure 97–25). The receiver may not necessarily receive a continuous PN sequence between separate periods of SEND_S.

The bit $S_n[0]$ is mapped to the transmit symbol Tn as follows: if $S_n[0] = 0$ then Tn = +1, if $S_n[0] = 1$ then Tn = –1.

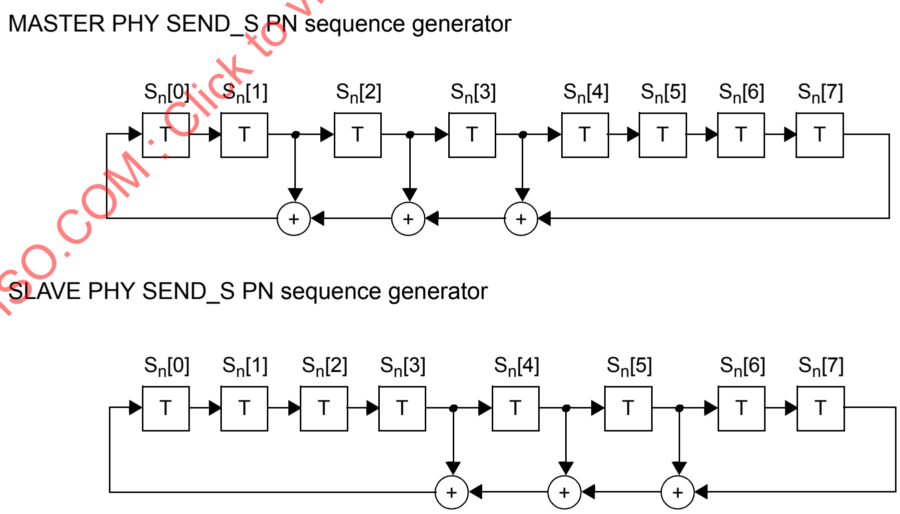


Figure 97–24—SEND_S PN sequence generator by linear feedback shift registers S_n

The synchronization state diagram in Figure 97–25 shall be used to synchronize 1000BASE-T1 PHYs prior to the 1000BASE-T1 link training. If Clause 98 Auto-Negotiation function is enabled, then the Auto-Negotiation function shall be used as the mechanism for PHY synchronization and the synchronization state diagram in Figure 97–25 remains in the SYNC_DISABLE state.

97.4.2.6.1 State diagram variables

force_config
: This variable indicates whether the PHY operates as a MASTER or as a SLAVE. The variable takes on one of the following values:
  - MASTER: this value is continuously asserted when the PHY operates as a MASTER
  - SLAVE: this value is continuously asserted when the PHY operates as a SLAVE

force_phy_type
: This variable indicates what speed the PHY is to operate when Auto-Negotiation is disabled or not implemented. The variable takes on one of the following values:
  - 1000-T1: if Auto-Negotiation is disabled or not implemented and 1000BASE-T1 is selected
  - 100-T1: if Auto-Negotiation is disabled or not implemented and 100BASE-T1 is selected
  - None: else

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_enable:
: see 98.5.1

mr_main_reset
: see 98.5.1

power_on
: see 98.5.1

send_s_sigdet
: This variable indicates whether the SEND_S pattern was detected. This variable shall be set false no later than 1 µs after the signal goes quiet on the MDI.
  Values:
  - true: SEND_S pattern detected
  - false: SEND_S pattern not detected

sync_link_control
: This variable indicates the data source for the PMA Transmit function.
  Values:
  - DISABLE: The data source is the PHY Link Synchronization function (sync_tx_symb)
  - ENABLE: The data source is PMA_UNITDATA.request (tx_symb)

sync_tx_mode
: This variable indicates what symbols are sent by the PHY Link Synchronization process.
  Values:
  - SEND_S: this value is continuously asserted to enable transmission of the PN sequence defined in 97.4.2.6
  - SEND_Z: this value is asserted to disable transmission

97.4.2.6.2 State diagram timers

break_link_timer
: see 98.5.2

link_fail_inhibit_timer
: see 98.5.2

send_s_timer
: This timer is used to control the duration SEND_S is transmitted. The timer shall expire 1.0 µs±0.04 µs after being started.

sigdet_wait_timer
: This timer is used to control the wait time after transmitting or detecting the end of SEND_S. The timer shall expire 4 µs±0.1 µs after being started.

97.4.2.6.3 Messages

sync_tx_symb
: A signal sent from Link Synchronization block to PMA Transmit indicating that a PAM2 (SEND_S) or zero (SEND_Z) symbol is available. The Link Synchronization block generates sync_tx_symb synchronously with every transmit clock cycle.

97.4.2.6.4 State diagrams

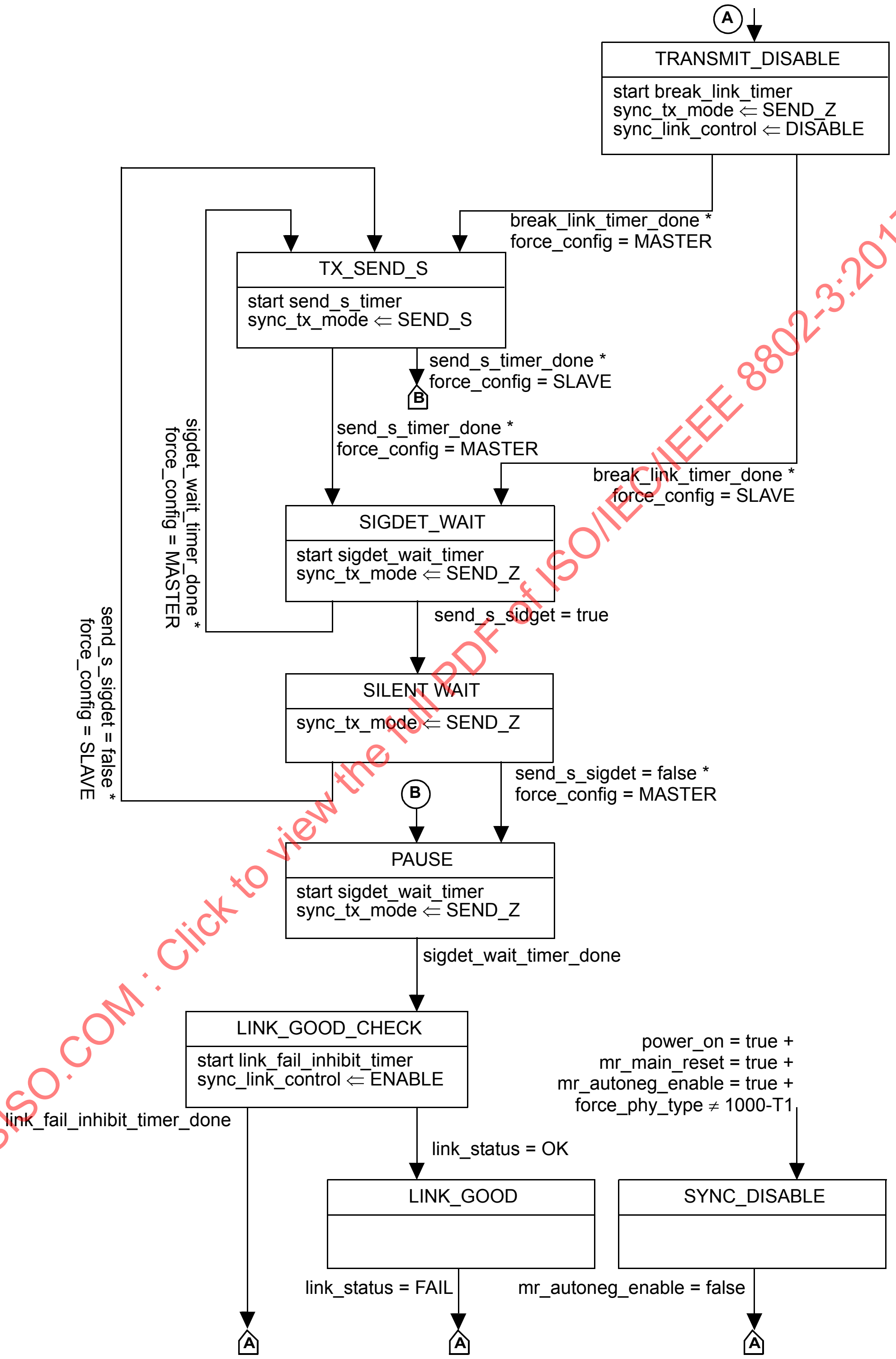


Figure 97–25—PHY Link Synchronization state diagram

97.4.2.7 Refresh Monitor function

A 1000BASE-T1 PHY supporting the EEE capability shall implement the Refresh monitor function. The Refresh monitor operates when the PHY is in the LPI receive mode. If Refresh is not reliably detected within a moving window of 50 Q/R cycles (4.32 ms), the refresh monitor shall set PMA_refresh_status to FAIL, which sets link_status to FAIL. Subsequently the PHY restarts auto-negotiation (if auto-negotiation is enabled) or synchronization (if auto-negotiation is disabled). PMA_refresh_status shall be set to OK when the Link Monitor state diagram (Figure 97–27) enters the LINK_UP state.

97.4.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RS FER indicated in 97.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

97.4.3 MDI

Communication through the MDI is summarized in 97.4.3.1 and 97.4.3.2.

97.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The modulation scheme used over each pair is PAM3. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \quad (97\text{–}10)$$

In Equation (97–10), a_n is the PAM3 modulation symbol from the set {–1, 0, 1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 97.5.

97.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \quad (97\text{–}11)$$

In Equation (97–11) $h_R(t)$ denotes the symbol response of the overall channel impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources including uncancelled echo. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

97.4.4 State variables

97.4.4.1 State diagram variables

auto_neg_imp
This variable indicates if an optional Auto-Negotiation sublayer is associated with the PMA.
Values:
true: An optional Auto-Negotiation sublayer is associated with the PMA
false: An optional Auto-Negotiation sublayer is not associated with the PMA

config
The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.
Values:
MASTER
SLAVE

en_slave_tx
The en_slave_tx variable in the InfoField received by the SLAVE.
Values:
0: Master is not ready for the SLAVE to transmit
1: Master is ready for the SLAVE to transmit

infofield_complete
This variable indicates that a complete set of InfoField messages has been sent (see 97.4.2.4).
Values:
false: a complete set of InfoField messages has not been sent
true: a complete set of InfoField messages has been sent

link_control
This variable is defined in 97.2.1.1.1.

link_status
The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

loc_phy_ready
This variable is set by the PMA Receive function to indicate the local PHY is ready or not ready to receive data. The value of loc_phy_ready is equal to OK only if loc_rcvr_status = OK and pcs_status = OK. Otherwise its value is NOT_OK. This variable is conveyed to the link partner by the PCS as defined in Table 97–1.
Values:
OK: the local PHY is ready to receive data
NOT_OK: the local PHY is not ready to receive data

loc_countdown_done
This variable is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to true immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

loc_rcvr_status
Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY. This variable is transmitted in the loc_rcvr_status bit of the InfoField by the local PHY.
Values:
OK: the receive link for the local PHY is operating reliably
NOT_OK: operation of the receive link for the local PHY is unreliable

loc_SNR_margin
This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.
Values:
OK: the local device has sufficient SNR margin
NOT_OK: the local device does not have sufficient SNR margin

PMA_refresh_status
This variable indicates the status of the Refresh Monitor as described in 97.4.3.
Values:
OK: refresh is detected reliably
FAIL: refresh is not detected reliably

pma_reset
Allows reset of all PMA functions. It is set by PMA Reset.
Values:
ON
OFF

PMA_state
Variable for the value transmitted in the PMA_state<7:6> of the InfoField by the local PHY.
Values:
00: TRAINING state
01: COUNTDOWN state

PMA_watchdog_status
Variable indicating the status of the PAM3 monitor.
Values:
OK: the local device has received sufficient PAM3 transitions
NOT_OK: the local device has not received sufficient PAM3 transitions
During normal operation NOT_OK is assigned when:

— PAM3 symbol 0 consecutively seen on the line for longer than 2 μs ± 0.1 μs
— PAM3 symbol +1 consecutively seen on the line for longer than 3.9 μs ± 0.1 μs
— PAM3 symbol –1 consecutively seen on the line for longer than 3.9 μs ± 0.1 μs

During Low Power Idle operation NOT_OK is assigned when:

— PAM3 symbol not toggling on the line during one full refresh window

rem_countdown_done
This variable is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state and is set to true once the receiver has transitioned from PAM2 to PAM3 mode and has received a valid PHY frame containing all IDLEs.

rem_phy_ready
This variable is set by the PCS Receive function to indicate whether the remote PHY is ready or not ready to receive data. This variable is received from the link partner by the PCS as defined in Table 97–1. The variable retains its value until the next normal Inter-Frame idle is received.
Values:
OK: the remote PHY is ready to receive data
NOT_OK: the remote PHY is not ready to receive data

rem_rcvr_status
Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. This variable is received in the loc_rcvr_status bit in the InfoField from the remote PHY. This variable is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY.
Values:
OK: the receive link for the remote PHY is operating reliably
NOT_OK: reliable operation of the receive link for the remote PHY is not detected

sync_link_control
This variable is defined in 97.4.2.6.1.

tx_mode
The PMA generates this variable continuously and passes it to the PCS via the PMA_TX-MODE.indication primitive.
Values:
SEND_N: this value is continuously asserted when transmission of sequences of symbols representing a GMII data stream take place
SEND_I: this value is continuously asserted when transmission of sequences of symbols representing an idle stream takes place
SEND_T: this value is continuously asserted when transmission of sequences of symbols representing the training sequences of symbols is to take place
SEND_Z: this value is asserted when transmission of zero symbols is to take place

97.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

maxwait_timer
A timer used to limit the amount of time during which a receiver dwells in the SILENT and TRAINING states. The timer shall expire 97.5 ms ± 0.5 ms after being started.
This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if either of the following conditions is true:

- the PMA_watchdog_status is NOT_OK
- the timer expires and loc_phy_ready is NOT_OK
- the PMA_refresh_status is FAIL

See Figure 97–26 and Figure 97–27.

minwait_timer
A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING, SEND IDLE2, and SEND DATA states. The timer shall expire 975 µs ± 50 µs after being started.

97.4.5 State diagrams

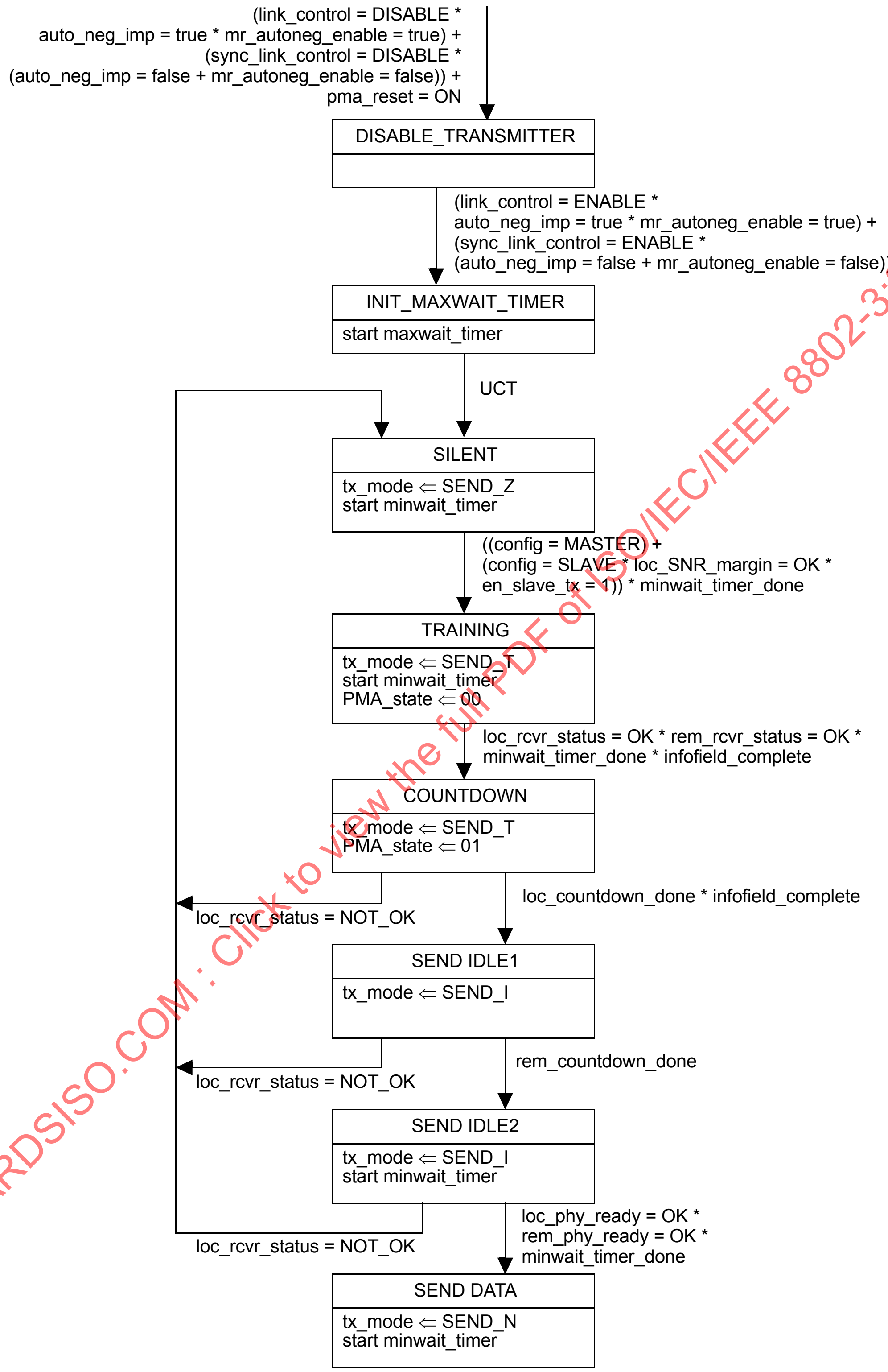
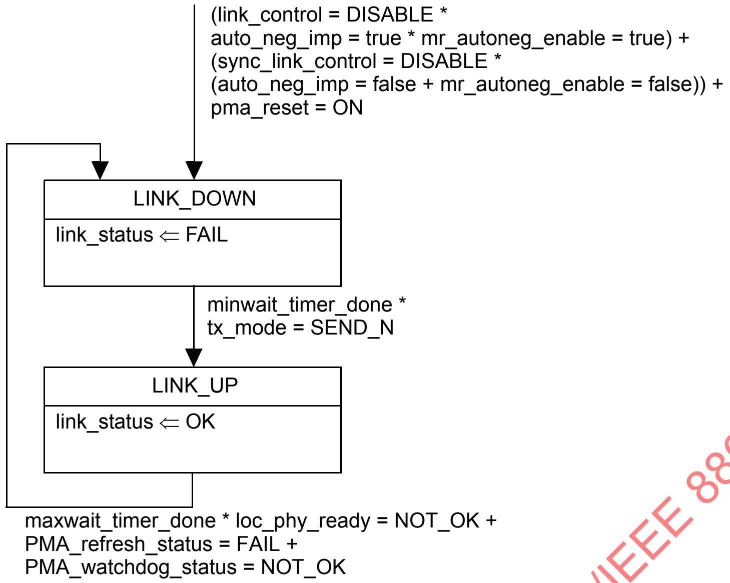


Figure 97–26—PHY Control state diagram



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 97–26).

NOTE 2—The variables link_control and link_status are designated as link_control_1GigT1 and link_status_1GigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–7) if the optional Auto-Negotiation function is implemented.

Figure 97–27—Link Monitor state diagram

97.5 PMA electrical specifications

This subclause specifies the electrical characteristics of the PMA for a 1000BASE-T1 Ethernet PHY.

97.5.1 EMC Requirements

See 96.5.1.

97.5.1.1 Immunity—DPI test

See 96.5.1.1.

97.5.1.2 Emission—150 Ω conducted emission test

See 96.5.1.2.

97.5.2 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER testing.

These test modes shall be enabled by setting a control register 1.2308.15:13 as shown in Table 97–12. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Table 97–12—MDIO management registers settings for test modes

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in MASTER mode.
011	Reserved.
100	Test mode 4—Transmit distortion test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE 1000BASE-T1 PHYs are connected over a link segment defined in 97.6. When in this mode, the 1000BASE-T1 PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125. This 125 MHz test clock is one sixth frequency divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on MDI when transmitter is in MASTER timing mode. When test mode 2 is enabled, the 1000BASE-T1 PHY shall transmit a continuous pattern of three {+1} symbols followed by three {–1} symbols with the transmitted symbols timed from its local clock source of 750 MHz. The transmitter output is a 125 MHz signal.

Test mode 3 is not defined and the corresponding register is reserved for future use.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, 1000BASE-T1 PHY shall transmit the sequence of symbols generated by the scrambler generator polynomial per Equation (97–12).

$$g(x) = 1 + x^9 + x^{11} \tag{97–12}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (2/750 MHz). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive ORed together to generate the next $Scr_n[0]$ bit. The bit sequences $x0_n$, $x1_n$, and $x2_n$ generated from combinations of the scrambler bits, as shown in Equation (97–13), shall be used to generate the ternary symbols, $T0_n$ and $T1_n$, as shown in Table 97–13. The transmitter shall time the transmitted symbols from a 750 MHz ± 0.01% clock in the MASTER timing mode. The transmit signal level and spectral shaping in this mode shall be same as normal (non-test) mode. A typical transmitter output for transmitter test mode 4 is shown in Figure 97–28.

$$\begin{aligned} x0_n &= Scr_n[0] \\ x1_n &= Scr_n[1] \wedge Scr_n[4] \\ x2_n &= Scr_n[1] \wedge Scr_n[5] \end{aligned} \tag{97–13}$$

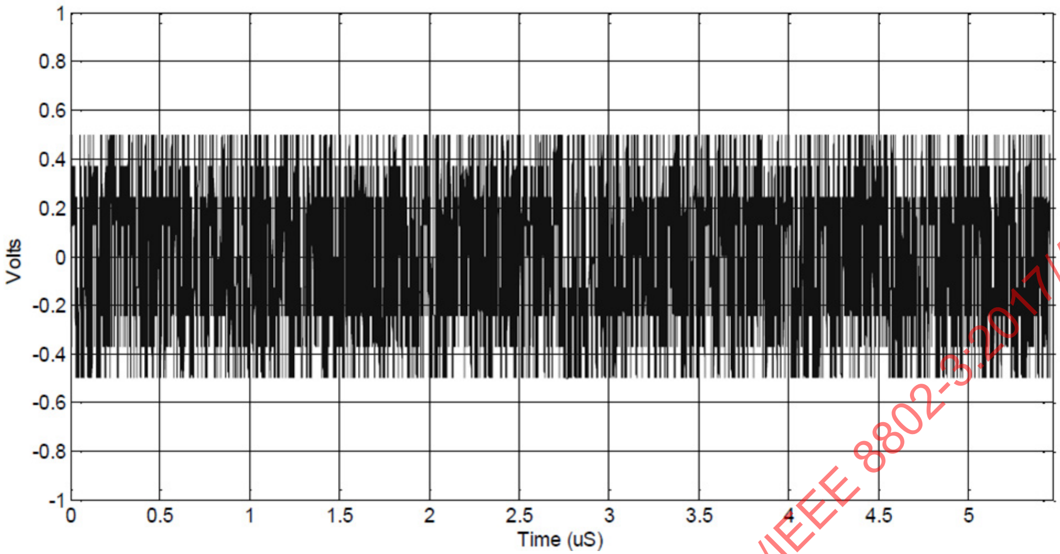


Figure 97–28—Typical transmitter output for transmitter test mode 4

Table 97–13—Transmit test mode 4 symbol mapping

$x2_n$	$x1_n$	$x0_n$	$T1_n$	$T0_n$
0	0	0	–1	–1
0	0	1	0	–1
0	1	0	–1	0
0	1	1	–1	+1
1	0	0	+1	0
1	0	1	+1	–1
1	1	0	+1	+1
1	1	1	0	+1

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, 1000BASE-T1 PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals.

When test mode 6 is enabled, 1000BASE-T1 PHY shall transmit a continuous pattern of fifteen {+1} symbols followed by fifteen {–1} symbols with the transmitted symbols timed from its local clock source of 750 MHz. The transmitter output is a 25 MHz signal.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder / decoder, transmit and receive analog front ends of 1000BASE-T1 PHY, and a cable connecting two 1000BASE-T1 PHYs. This mode reuses the 1000BASE-T1 normal (non-test) mode with zero data pattern. Instead of encoding received data from MAC, continuous zero data pattern is encoded. In the receive side, after FEC and 80B/81B decoding, zero data sequence is expected with no error. Any non-zero data bit received is counted as error and calculated in BER.

97.5.2.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 97–29, Figure 97–30, Figure 97–31, Figure 97–32, and Figure 97–33, in stated respective tests, shall be used for measuring the transmitter specifications for data communication only. The tolerance of resistors shall be ± 0.1%.

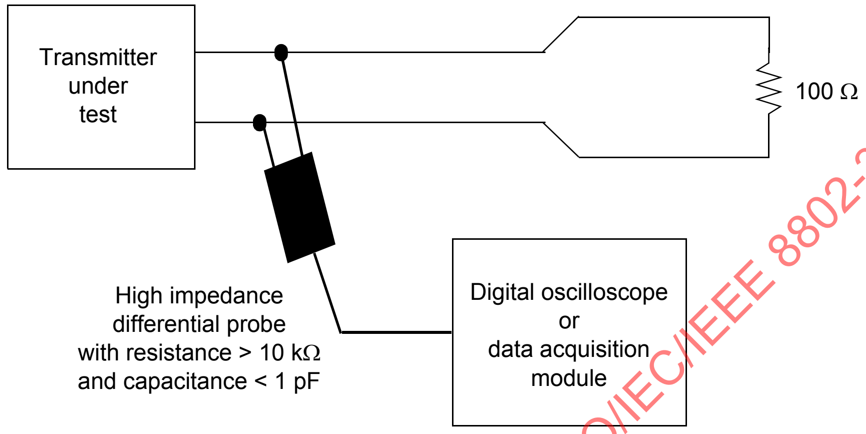


Figure 97–29—Transmitter test fixture 1 for transmitter droop measurement

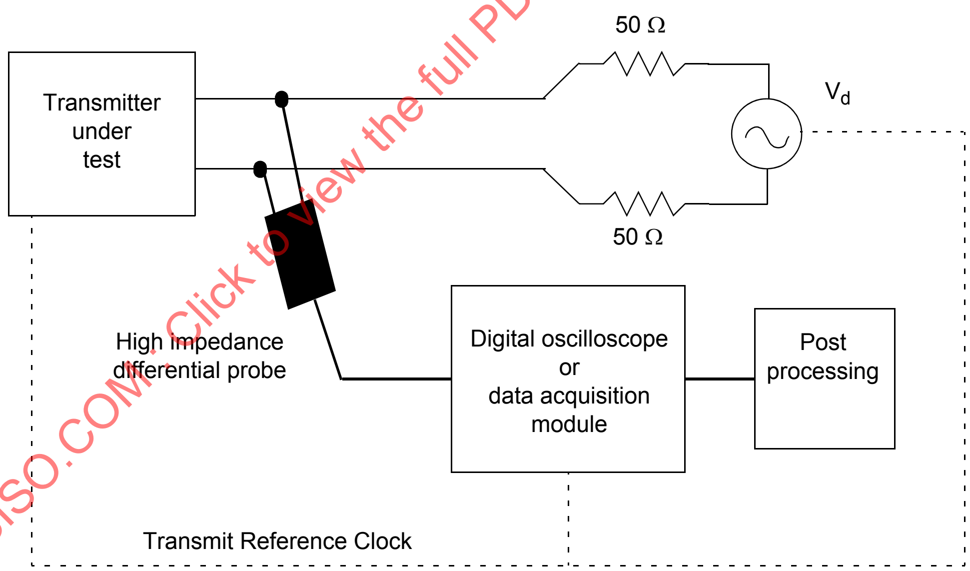


Figure 97–30—Transmitter test fixture 2 for transmitter distortion measurement

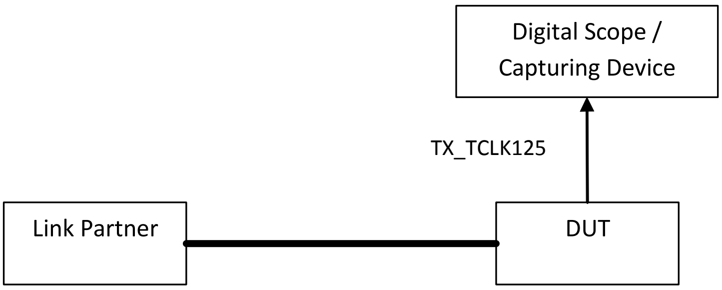


Figure 97–31—Transmitter test fixture 3 for MASTER and SLAVE clock jitter measurement

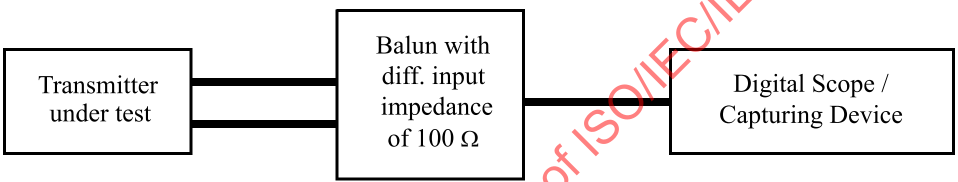


Figure 97–32—Transmitter test fixture 4 for MDI jitter measurement

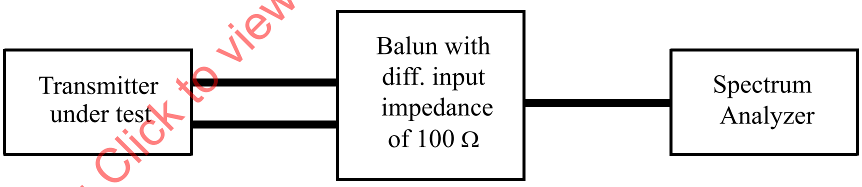


Figure 97–33—Transmitter test fixture 5 for power spectral density measurement and transmit power level measurement

97.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in 97.4.2.2 in accordance with the electrical specifications of this clause. The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to the transmitter output.

97.5.3.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than 10%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).

97.5.3.2 Transmitter distortion

In Figure 97–30, the sinusoidal disturbing signal Vd, shall have amplitude of 3.6 V peak-to-peak differential, and frequency given by one-sixth of the symbol rate (125 MHz) synchronous with the test pattern. The generator of the disturbing signal shall have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output.

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 2. The peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signal shall be at least 40 µs long and be sampled with the minimum sampling rate of 7.5 Gs/s (10 times the transmit symbol rate of 750 Ms/s).

The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 15 mV. Notice the peak signal level is normalized to 1 V in the processing code. The pseudo-code removes the sinusoidal disturbing signal from the measured data and computes the peak distortion. The code assumes the disturber signal and the data acquisition clock are frequency locked to the DUT transmit clock.

```
% Post processing pseudo-code for 1000BASE-T1 transmitter distortion
clear
Ns=2^11-1; % Scrambler length
Nc=70;  % Canceller length

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
  scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% 1000BASE-T1 2D-PAM3 assignment
tm4=ones(Ns,1);
map=[-1 -1;-1 0;0 -1;1 -1;0 1;-1 1;1 1;1 0];
scr3=[scr, mod(circshift(scr,1) + circshift(scr,4),2),...
    mod(circshift(scr,1) + circshift(scr,5),2)];
data = 4*scr3(:,3)+ 2*scr3(:,2)+scr3(:,1);
for n=1:length(data)
    tm4([2*n-1,2*n]) =map(data(n)+1,:);
end
Ns=2*Ns;

% Test mode4 matrix
for i=1:Nc
    X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file, 40us long, 7.5GSample/sec, high resolution capture
fid=fopen('RawData.bin','r');
tx = fread(fid,inf,'double');
fclose(fid);

% LPF 375MHz
[A,B]=butter(2,1/10,'low');
tx=filter(A,B,tx);
```

```
% HPF 12MHz
tx = filter([1,-1],[1,-exp(-2*pi/625)],tx);

% Select six periods, 10x oversampling, a row vector
tx=tx((1:6*Ns*10)+2e3)'; % removes HPF transient

% Disturber removal and integration (average) of six periods
TX=fft(tx);
tx=ifft(TX(1:6:end));

% Level normalization to 1V
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 clock phases
for n=1:10
tx1=tx(n:10:end);

% Align data and test pattern
temp=xcorr(tx1,tm4);
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);

% Compute coefficients that minimize squared error
coef=tx1/X;

% Linear canceller
err=tx1-coef*X;

% Peak distortion
dist(n) = max(abs(err));
end

% Print distortion in mV (normalized) for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist'
```

97.5.3.3 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK125 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 3 shown in Figure 97–31.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK125 jitter relative to an unjittered reference shall be less than 5 ps. The peak-to-peak value of the MASTER TX_TCLK125 jitter relative to an unjittered reference shall be less than 50 ps.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK125 jitter relative to an unjittered reference shall be less than 10 ps. The peak-to-peak value of the SLAVE TX_TCLK125 jitter relative to an unjittered reference shall be less than 100 ps.

TX_TCLK125 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be larger than 2 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK125. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

For PHYs supporting LPI mode, in order for the transmit jitter to be similar to normal power mode operation, the clock reference used to clock transmit-symbols shall be continuous going from normal power mode into and out of LPI mode.

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 and using test fixture 4 as shown in Figure 97–32. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than 5 ps. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 50 ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 2 MHz. Unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

$$UpperPSD(f) = \begin{cases} -80 & \text{dBm/Hz} \quad 0 < f \le 100 \\ -76 - \dfrac{f}{25} & \text{dBm/Hz} \quad 100 < f \le 400 \\ -85.6 - \dfrac{f}{62.5} & \text{dBm/Hz} \quad 400 < f \le 600 \end{cases} \tag{97–14}$$

$$LowerPSD(f) = \begin{cases} -86 & \text{dBm/Hz} \quad 40 < f \le 100 \\ -82 - \dfrac{f}{25} & \text{dBm/Hz} \quad 100 < f \le 400 \end{cases} \tag{97–15}$$

where

f is the frequency in MHz

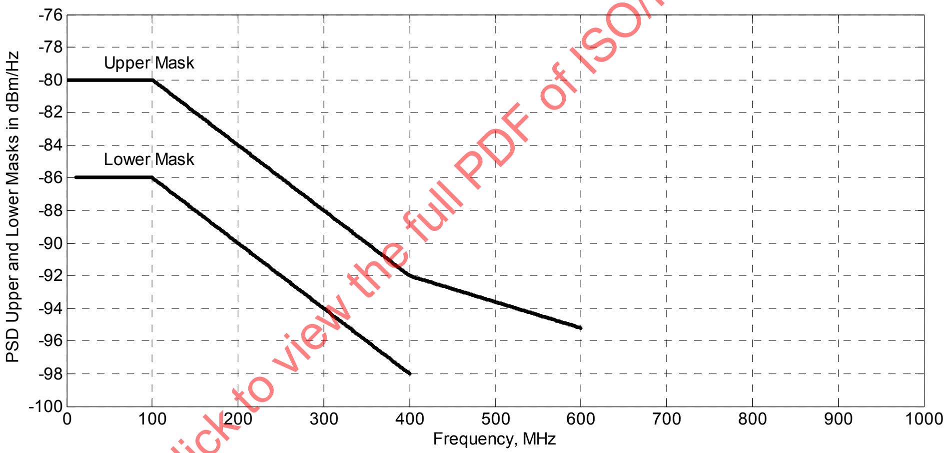


Figure 97–34—Transmitter Power Spectral Density, upper and lower masks

97.5.3.4 Transmitter Power Spectral Density (PSD) and power level

In test mode 5 (normal operation), the transmit power shall be less than 5 dBm and the power spectral density of the transmitter, measured into a 100 Ω load using the test fixture 5 shown in Figure 97–33 shall be between the upper and lower masks specified in Equation (97–14) and Equation (97–15). The masks are shown in Figure 97–34. The measurements need to be calibrated for insertion loss of the differential Balun used in the test. The resolution bandwidth of 100 kHz and sweep time of larger than 1 second are considered in PSD measurement.

97.5.3.5 Transmitter peak differential output

When measured with 100 Ω termination, transmit differential signal at MDI shall be less than 1.30 V peak-to-peak. This limit applies to all transmit modes including SEND_S, SEND_T, SEND_I, and SEND_N modes.

97.5.3.6 Transmitter clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 750 MHz ± 100 ppm.

For a MASTER PHY, when the transmitter is in the LPI transmit mode, the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

97.5.4 Receiver electrical specifications

97.5.4.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 97.5.3 and have passed through a link segment type A (specified in 97.6.1 and 97.6.3) are received with a BER less than 10^{-10} and sent to the PCS after link reset completion. This BER specification shall be satisfied by a frame loss ratio less than 10^{-7} for 125-octet frames. Operation on link segment type B is optional. If supported, the frame loss ratio shall also be met for link segments specified at 97.6.2 and 97.6.4.

97.5.4.2 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidth of 550 MHz and magnitude of –100 dBm/Hz for devices supporting type A link segments and –110 dBm/Hz for devices supporting type B link segments. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 97–35, with a link segment as defined in 97.6. The noise is added at the MDI of the DUT. The BER is expected to be less than 10^{-10}, and to satisfy this specification the frame loss ratio is less than 10^{-7} for 125-octet packets measured at MAC/PLS service interface.

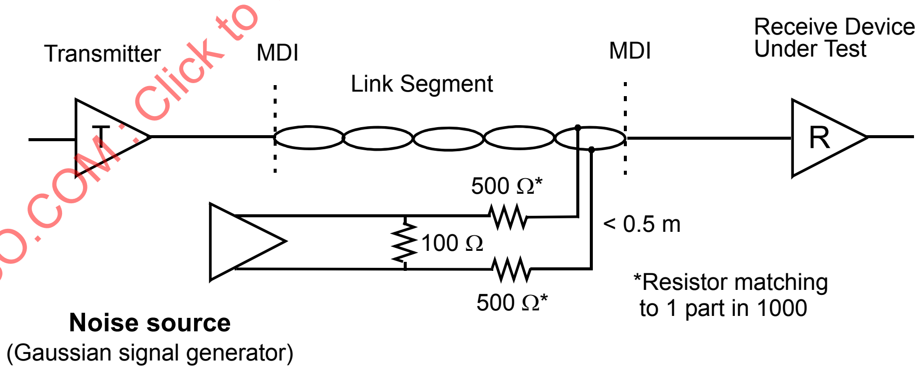


Figure 97–35—Alien crosstalk noise rejection test setup

97.6 Link segment characteristics

1000BASE-T1 is designed to operate over a single twisted-pair copper cable that meets the requirements specified in this subclause. The single twisted-pair copper cable supports an effective data rate of 1 Gb/s in each direction simultaneously. The term *link segment* used in this clause refers to a single twisted-pair copper cable operating in full duplex.

Two link segments are specified:

a) A link segment optimized for use in automotive applications that supports up to four in-line connectors using a single twisted-pair copper cable for up to at least 15 m. This link segment is referred to as *link segment type A*.
b) An optional link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 40 m to support applications requiring additional physical reach, such as industrial and automation controls and transportation (aircraft, railway, bus and heavy trucks). This link segment is referred to as *link segment type B*.

97.6.1 Link transmission parameters for link segment type A

The transmission characteristics for type A link segment are specified to support operation over automotive temperature and electromagnetic conditions.

97.6.1.1 Insertion loss

The insertion loss of each type A link segment shall meet the values determined using Equation (97–16).

$$\text{InsertionLoss}(f) \le 0.0023f + 0.5907\sqrt{f} + 0.0639/\sqrt{f} \quad \text{dB} \qquad (97\text{–}16)$$

where

f is the frequency in MHz; $1 \le f \le 600$

The insertion loss for the link segment calculated using Equation (97–16) accounts for the insertion loss of a single twisted-pair copper cable and four in-line connectors within each link segment. The insertion loss is illustrated in Figure 97–36.

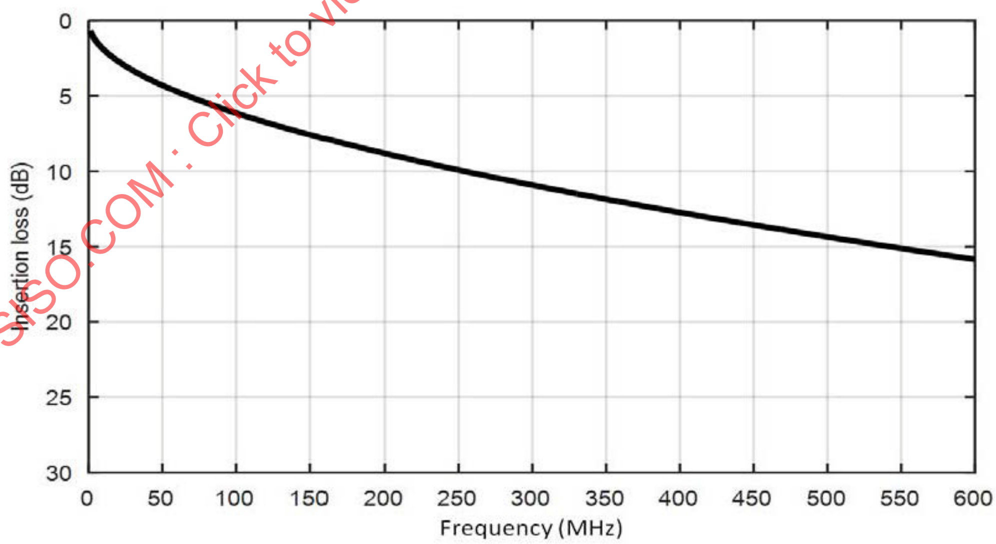


Figure 97–36—Insertion loss calculated using Equation (97–16)

97.6.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of each type A link segment is 100 Ω for all frequencies between 1 MHz and 600 MHz.

97.6.1.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches each type A link segment shall meet the values determined using Equation (97–17) at all frequencies from 1 MHz to 600 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return Loss} \geq \left\{ \begin{array}{cc} 19 & 1 \leq f < 10 \\ 24 - 5\log_{10}f & 10 \leq f < 40 \\ 16 & 40 \leq f < 130 \\ 37 - 10\log_{10}f & 130 \leq f < 400 \\ 11 & 400 \leq f \leq 600 \end{array} \right\} \text{dB} \qquad (97\text{–}17)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

The return loss is illustrated in Figure 97–37.

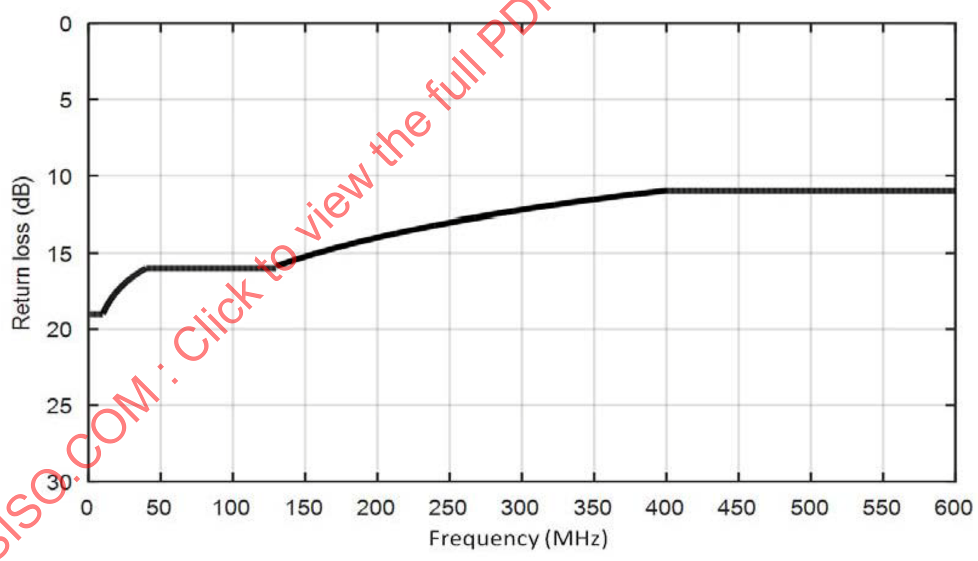


Figure 97–37—Return loss calculated using Equation (97–17)

97.6.1.4 Differential to common mode conversion

The balance of the type A link segment is characterized by the differential to common mode conversion. Each type A link segment shall meet the values determined using Equation (97–18) at all frequencies from 10 MHz to 600 MHz.

$$\text{ConversionLoss}(f) \geq \begin{cases} 50 & 10 \leq f \leq 80 \\ 72 - 11.51\log_{10} f & 80 < f \leq 600 \end{cases} \text{ dB} \quad (97\text{–}18)$$

where

f is the frequency in MHz; $10 \leq f \leq 600$

The function ConversionLoss(f) represents the mode conversion loss at frequency f. The conversion loss is illustrated in Figure 97–38.

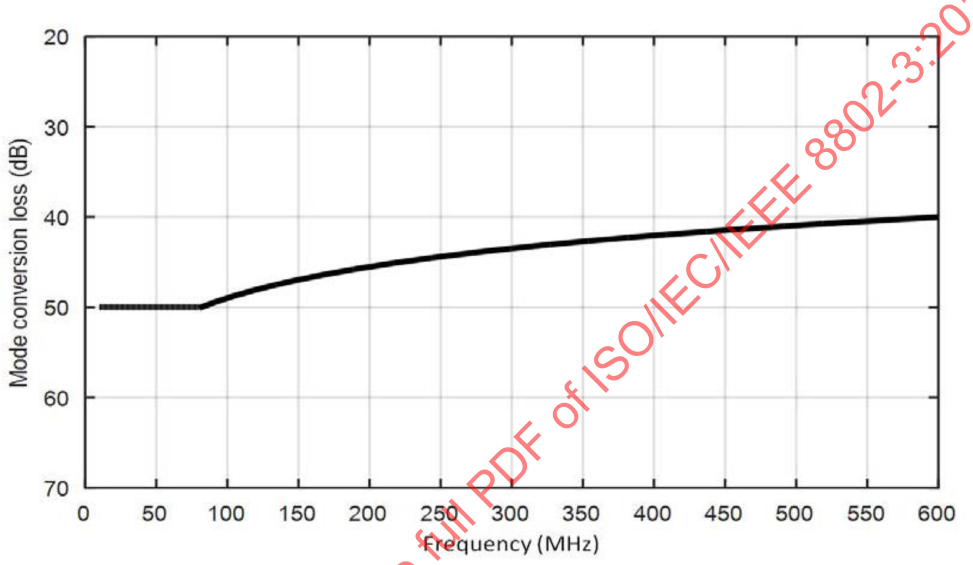


Figure 97–38—Conversion loss calculated using Equation (97–18)

The mode conversion specification applies to:

— Longitudinal conversion loss (LCL) with s-parameter SDC11/SDC22 and description common mode to differential mode return loss
— Transverse conversion loss (TCL) with s-parameter SCD11/SCD22 and description differential mode to common mode return loss
— Longitudinal conversion transmission loss (LCTL) with s-parameter SDC12/SDC21 and description common mode to differential mode insertion loss
— Transverse conversion transmission loss (TCTL) with s-parameter SCD12/SCD21 and description differential mode to common mode insertion loss

For compliance to the specification measurements of LCL and LCTL are sufficient as LCL and TCL are considered reciprocal and LCTL and TCTL are considered reciprocal. The differential to common mode conversion loss test methodologies are specified in Annex 97A.

97.6.1.5 Maximum link delay

The propagation delay of a type A link segment shall not exceed 94 ns at all frequencies between 2 MHz and 600 MHz.

97.6.2 Link transmission parameters for link segment type B

The transmission characteristics for type B link segment are specified to support applications requiring additional reach such as industrial and automation controls and transportation (aircraft, railway, bus, and heavy trucks) for up to at least 40 m. Type B link segment may be shielded or screened, consistent with the specification in 97.6.2.5 and 97.6.4.

97.6.2.1 Insertion loss

The insertion loss of each type B link segment shall meet the values determined using Equation (97–19).

$$\text{InsertionLoss}(f) \le 0.7131\sqrt{f} + 0.0040f + (0.1100/\sqrt{f}) + 0.08\sqrt{f} + 0.018\sqrt{f} \text{ dB} \quad (97\text{–}19)$$

where

f is the frequency in MHz; $1 \le f \le 600$

The insertion loss is illustrated in Figure 97–39.

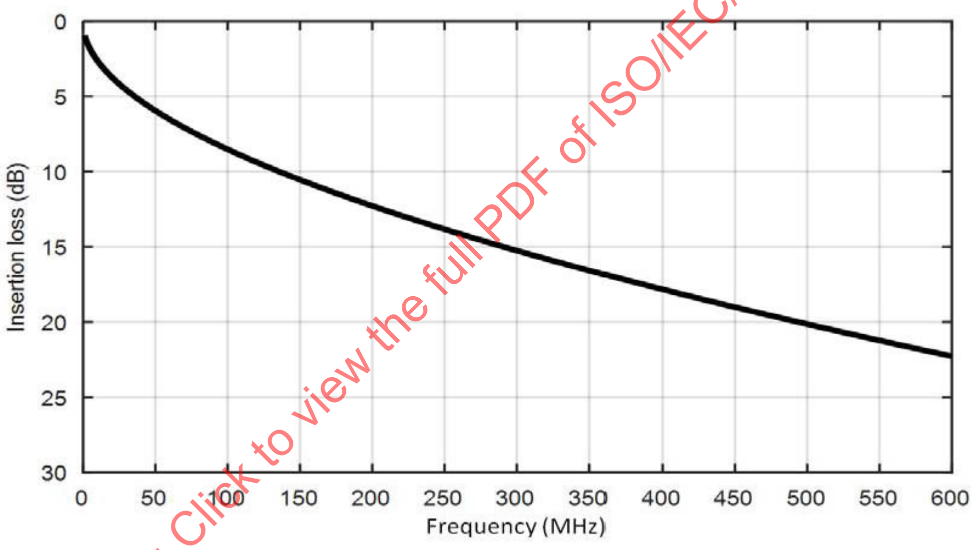


Figure 97–39—Insertion loss calculated using Equation (97–19)

The insertion loss for the link segment calculated using Equation (97–19) accounts for the insertion loss of a single twisted-pair copper cable and four in-line connectors within each link segment.

97.6.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each type B link segment is 100 Ω for all frequencies between 1 MHz and 600 MHz.

97.6.2.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches each type B link segment shall meet the values determined using Equation (97–20) at all frequencies from 1 MHz to 600 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return Loss} \geq \begin{cases} 19 & 1 \leq f < 10 \\ 24 - 5\log_{10}(f) & 10 \leq f < 40 \\ 16 & 40 \leq f < 130 \\ 37 - 10\log_{10}(f) & 130 \leq f < 400 \\ 11 & 400 \leq f \leq 600 \end{cases} \text{ dB} \quad (97\text{–}20)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

The return loss is illustrated in Figure 97–40.

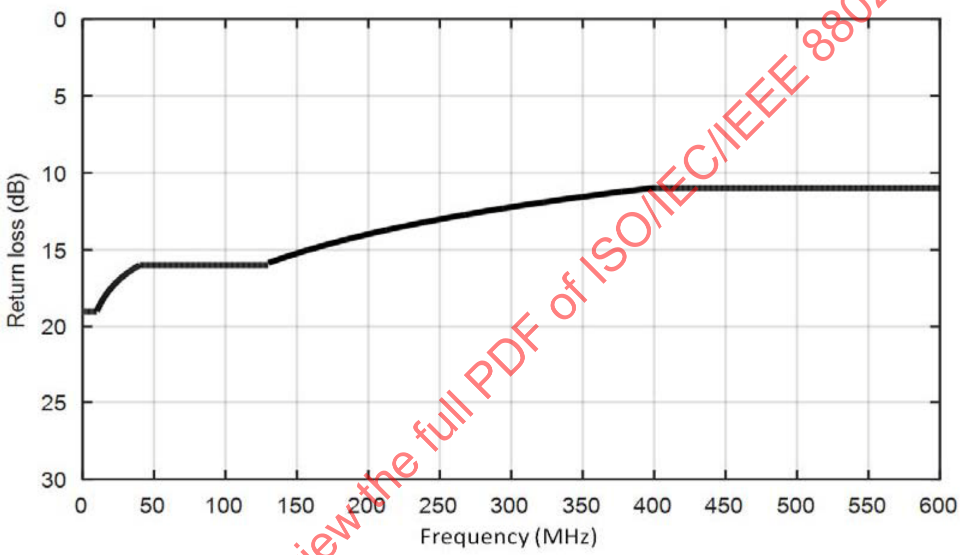


Figure 97–40—Return loss calculated using Equation (97–20)

97.6.2.4 Maximum link delay

The propagation delay of a type B link segment shall not exceed 234 ns at all frequencies between 2 MHz and 600 MHz.

97.6.2.5 Coupling attenuation

The coupling attenuation requirements of the type B link segment depend on the electromagnetic noise environment. The requirements in Table 97–14 shall be met based on the local environment as described by the electromagnetic classifications given in Table 97–15, E_1, E_2, or E_3. The coupling attenuation is tested as specified in IEC 62153-4–14.

Table 97–14—Coupling attenuation Type B link segment

Frequency (MHz)	Minimum (dB)		
	E_1	E_2	E_3
$30 \le f \le 600$	$80 - 20\log_{10}(f)$ (Max 40 dB)	$90 - 20\log_{10}(f)$ (Max 50 dB)	$100 - 20\log_{10}(f)$ (Max 60 dB)

Table 97–15—Electromagnetic classifications Type B link segment

Electromagnetic	Minimum (dB)		
	E_1	E_2	E_3
Radiated RF – AM	3 V/m at (80 MHz to 1000 MHz) 3 V/m at (1400 MHz to 2000 MHz) 1 V/m at (2000 MHz to 2700 MHz)	3 V/m at (80 MHz to 1000 MHz) 3 V/m at (1400 MHz to 2000 MHz) 1 V/m at (2000 MHz to 2700 MHz)	10 V/m at (80 MHz to 1000 MHz) 3 V/m at (1400 MHz to 2000 MHz) 1 V/m at (2000 MHz to 2700 MHz)
Conducted RF	3 V at 150 kHz to 80 MHz	3 V at 150 kHz to 80 MHz	10 V at 150 kHz to 80 MHz

97.6.3 Coupling parameters between type A link segments

Noise coupled between the disturbed type A link segment and the disturbing type A link segment is referred to as *alien crosstalk noise*. To ensure the total alien NEXT loss and alien FEXT loss coupled between type A link segments is limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified. The test methodologies are specified in Annex 97A and Annex 97B.

97.6.3.1 Multiple disturber alien near-end crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a type A link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed type A link segment and the disturbing type A link segment is specified to meet the bit error ratio objective. To ensure the total alien NEXT coupled into a type A link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

97.6.3.2 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–21).

$$\mathrm{PSANEXTloss}_N(f) \ge -10\log_{10}\left(\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN}(f)_{j,N}}{10}}\right) \mathrm{dB} \quad (97\text{–}21)$$

where the function $AN(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing type A link segment j (1 to m) for the disturbed type A link segment N.

The power sum ANEXT loss between a disturbed type A link segment and the disturbing type A link segment shall meet the values determined using Equation (97–22).

$$PSANEXT\,loss(f) \geq \left\{ \begin{array}{ll} 54 - 10\log_{10}\left(\frac{f}{100}\right) & 1 \leq f \leq 100 \\ 54 - 15\log_{10}\left(\frac{f}{100}\right) - 6\left(\frac{f-100}{400}\right) & 100 < f \leq 600 \end{array} \right\} \text{dB} \qquad (97–22)$$

where

f is the frequency in MHz

PSANEXT is illustrated in Figure 97–41.

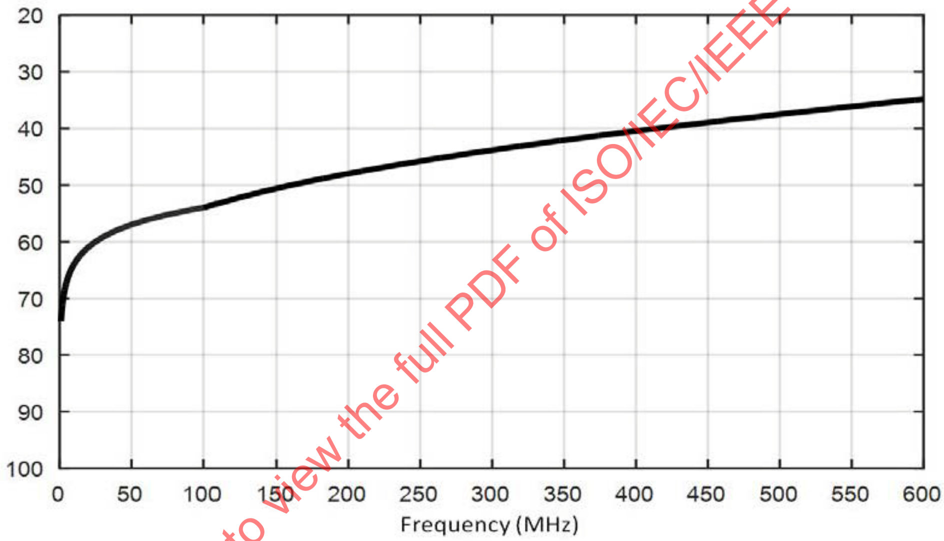


Figure 97–41—PSANEXT calculated using Equation (97–22)

97.6.3.3 Multiple disturber alien far-end crosstalk (MDAFEXT) loss

In order to limit the alien crosstalk at the far-end of a type A link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed type A link segment and the disturbing type A link segment is specified to meet the bit error ratio objective. To ensure the total alien FEXT coupled into a type A link segment, multiple disturber attenuation to crosstalk ratio far-end ACRF is specified as the power sum of the individual alien ACRF disturbers.

97.6.3.4 Multiple disturber power sum alien attenuation crosstalk ratio far-end (PSAACRF)

PSAACRF is determined by summing the power of the individual pair-to-pair differential alien ACRF values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–23).

$$\mathrm{PSAACRF}_N(f) \geq -10\log_{10}\left(\sum_{j=1}^{m} 10^{\frac{-\mathrm{AF}(f)_{j,N}}{10}}\right) \mathrm{dB} \qquad (97\text{–}23)$$

where the function $\mathrm{AF}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien ACRF of the disturbing type A link segment j (1 to m) for disturbed type A link segment N.

The power sum AACRF between a disturbed type A link segment and the disturbing type A link segment shall meet the values determined using Equation (97–24).

$$\mathrm{PSAACRF}(f) \geq -20\log_{10}\left(10^{\frac{(-10)\log_{10}0.15 + 38.2 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}} + 4 \times 10^{\frac{67 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right) \mathrm{dB} \qquad (97\text{–}24)$$

where

f is the frequency in MHz

PSAACRF is illustrated in Figure 97–42.

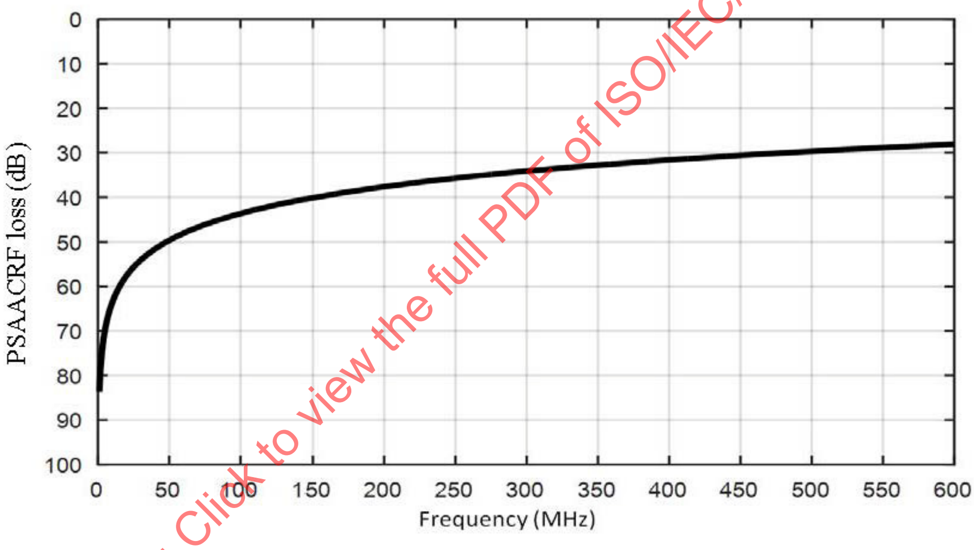


Figure 97–42—PSAACRF calculated using Equation (97–24)

97.6.4 Coupling parameters between type B link segments

Noise coupled between the disturbed type B link segment and the disturbing type B link segment is referred to as alien crosstalk noise. To ensure the total alien NEXT loss and alien FEXT loss coupled between type B link segments is limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified.

97.6.4.1 Multiple disturber alien near-end crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a type B link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed type B link segment and the disturbing type B link segment is specified to meet the bit error ratio objective. To ensure the total alien NEXT coupled into a type

B link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

97.6.4.2 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–25).

$$\mathrm{PSANEXT}_N(f) \geq -10\log_{10} \sum_{j=1}^{m} 10^{\frac{-\mathrm{AN}(f)_{j,N}}{10}} \ \mathrm{dB} \qquad (97\text{–}25)$$

where the function $\mathrm{AN}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing type B link segment j (1 to m) for the disturbed type B link segment N.

The power sum ANEXT loss between a disturbed type B link segment and the disturbing type B link segment shall meet the values determined using Equation (97–26).

$$\mathrm{PSANEXT}(f) \geq 65 \ \ \mathrm{dB} \qquad (97\text{–}26)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

97.6.4.3 Multiple disturber alien far-end crosstalk (MDAFEXT) loss

In order to limit the alien crosstalk at the far-end of a type B link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed type B link segment and the disturbing type B link segment is specified to meet the bit error ratio objective. To ensure the total alien FEXT coupled into a type B link segment, multiple disturber attenuation to crosstalk ratio far-end ACRF is specified as the power sum of the individual alien ACRF disturbers.

97.6.4.4 Multiple disturber power sum alien attenuation crosstalk ratio far-end (PSAACRF)

PSAACRF is determined by summing the power of the individual pair-to-pair differential alien ACRF values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–27).

$$\mathrm{PSAACRF}_N(f) \geq -10\log_{10} \sum_{j=1}^{m} 10^{\frac{-\mathrm{AF}(f)_{j,N}}{10}} \ \mathrm{dB} \qquad (97\text{–}27)$$

where the function $\mathrm{AF}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien ACRF of the disturbing type B link segment j (1 to m) for disturbed type B link segment N.

The power sum AACRF between a disturbed type B link segment and the disturbing type B link segment shall meet the values determined using Equation (97–28) or 70 dB, whichever is less.

$$\mathrm{PSAACRF}(f) \geq 61 - 20\log_{10}(f/100) \ \ \mathrm{dB} \qquad (97\text{–}28)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

97.7 Media Dependent Interface (MDI)

97.7.1 MDI connectors

The mechanical interface to the balanced cabling is a 2-pin connector or 2 pins of a multi-pin connector. Further specification of the mechanical interface is beyond the scope of this standard.

97.7.2 MDI electrical specification

The electrical requirements specified in 97.5.3 and 97.5.4 shall be met when the PHY is connected to the MDI connector mated with a specified balanced twisted-pair cable connector

97.7.2.1 MDI return loss

The differential impedance at the MDI (see Figure 97–43) for each transmit/receive channel shall be such that any reflection (due to differential signals incident upon the MDI with a test port having a differential impedance of 100 Ω) is attenuated relative to the incident signal per Equation (97–29).

$$\text{Return Loss}(f) \geq \left\{ \begin{array}{ll} 18 - 18\log_{10}\frac{20}{f} & 2 \leq f < 20 \\ 18 & 20 \leq f < 100 \\ 18 - 16.7\log_{10}\frac{f}{100} & 100 \leq f \leq 600 \end{array} \right\} \text{dB} \qquad (97\text{–}29)$$

where f is the frequency in MHz.

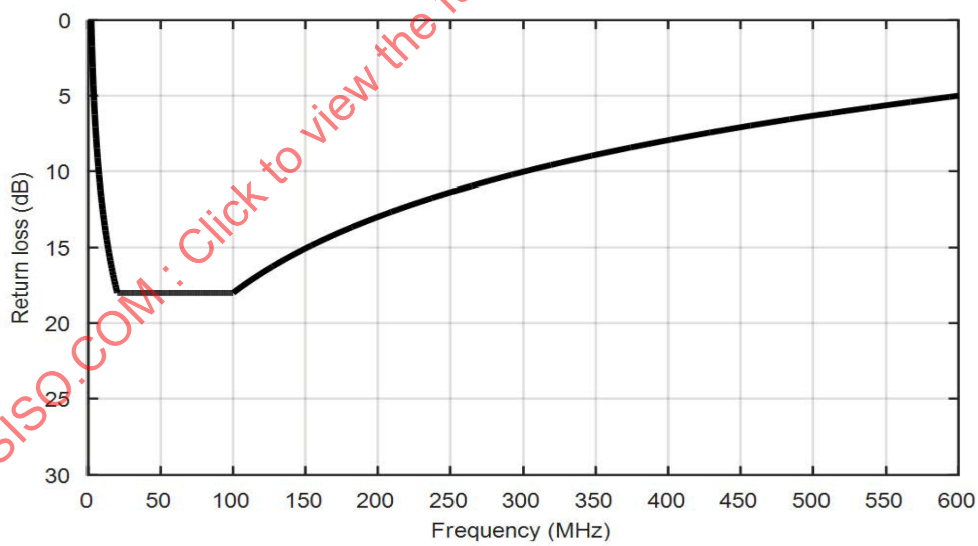


Figure 97–43—Return loss calculated using Equation (97–29)

97.7.2.2 MDI mode conversion loss

Mode conversion LCL (Sdc11) or TCL (Scd11) of the PHY measured at MDI shall meet the values determined using Equation (97–30) at all frequencies from 10 MHz to 600 MHz.

$$\text{ConversionLoss}(f) \geq \left\{ \begin{array}{cc} 55 & 10 \leq f \leq 80 \\ 77 - 11.51\log_{10} f & 80 < f \leq 600 \end{array} \right\} \text{dB} \qquad (97\text{–}30)$$

where

f is the frequency in MHz; $10 \leq f \leq 600$

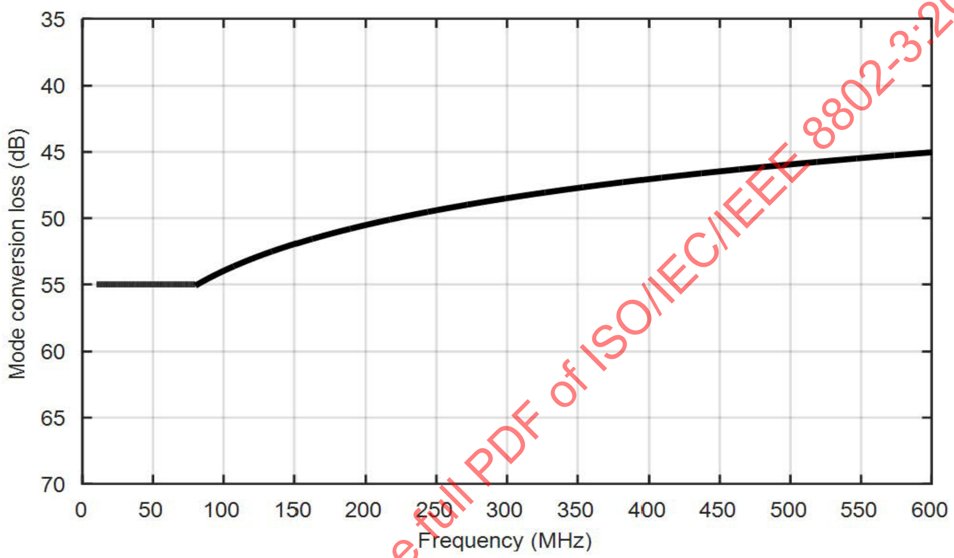


Figure 97–44—MDI mode conversion loss calculated using Equation (97–30)

97.7.3 MDI fault tolerance

See 96.8.3.

97.8 Management interfaces

1000BASE-T1 makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by the optional Auto-Negotiation (Clause 98).

97.8.1 Optional Support for Auto-Negotiation

If Auto-Negotiation is supported and enabled the mechanism described in Clause 98 shall be used.

Auto-Negotiation is performed as part of the initial setup of the link, and allows the PHYs at each end to advertise their capabilities and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 1000BASE-T1:

a) To negotiate that the PHY is capable of supporting 1000BASE-T1 transmission
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link

97.9 Environmental specifications

97.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1. All equipment subject to this clause and intended for motor vehicle applications shall conform to ISO 26262. All equipment subject to this clause may be additionally required to conform to any applicable local, state, or national motor vehicle standards or as agreed to between the customer and supplier.

97.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. In automotive applications, all 1000BASE-T1 cabling is routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764.

97.9.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, shall conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750–1
b) Electrical loads: ISO 16750-2, ISO 7637-2:2008, and ISO 8820–1
c) Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103–1
d) Climatic loads: ISO 16750-4 and IEC 60068-2–1/27/30/38/52/64/78
e) Chemical loads: ISO 167540-5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

97.9.2.2 Electromagnetic compatibility

A system integrating the 1000BASE-T1 PHY shall comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements as agreed upon between customer and supplier, for the limitation of electromagnetic interference. A 1000BASE-T1 PHY shall be tested according to IEC CISPR 25 test methods defined to measure the PHY's EMC performance in terms of radio frequency (RF) immunity and RF emissions. When used in an automotive environment, a 1000BASE-T1 PHY is expected to meet the following motor vehicle EMC requirements:

a) Radiated/conducted emissions: CISPR 25, IEC 61967–1/4, and IEC 61000-4-21
b) Radiated/conducted immunity: ISO 11452, IEC 62132–1/4, and IEC 61000-4-21
c) Electrostatic discharge: ISO 10605 and IEC 61000-4-2/3
d) Electrical disturbances: IEC 62215-3 and ISO 7637-2/3

Exact test setup and test limit values may be adapted to each specific application, subject to agreement between the customer and the supplier.

97.10 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 1000BASE-T1 PHY shall not exceed 7168 bit times (14 pause_quanta or 7168 ns). Transmit data delay is measured from the input of a given unit of data at the GMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the GMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

97.11 Protocol implementation conformance statement (PICS) proforma for Clause 97, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1[4]

97.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 97, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

97.11.2 Identification

97.11.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

97.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bp-2016, Clause 97, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bp-2016.)	

Date of Statement	

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

97.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
GMII	PHY associated with GMII	97.1	Interface is supported	O	Yes [ ] No [ ]
*EEE	EEE capability	97.1.2.3		O	Yes [ ] No [ ]
PCS	1000BASE-T1 PCS	97.3		M	Yes [ ]
PMA	1000BASE-T1 PMA	97.4		M	Yes [ ]
AN	Auto-negotiation	97.1, 98		O	Yes [ ] No [ ]
*CHNL	Channel	97.6	Channel specification not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*MDIO	MDIO Capability	45.1	Register and Interface supported	O	Yes [ ] No [ ]
*AUTO	Automotive environment installation	97.9		O	Yes [ ] No [ ]
*LSTB	Operation on link segment type B	97.5.4.1	Optional	O	Yes [ ] No [ ]

97.11.4 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	MASTER-SLAVE relationship when Auto-Negotiation is not used	97.1.2	Established by management of hardware configuration of the PHYs	M	Yes [ ]
G2	Test circuit accuracy	97.1.5	Within ±1% unless otherwise stated	M	Yes [ ]
G3	Sum of the transmit and receive data delays	97.10	Not exceed 7168 bit times (14 pause_quanta or 7168 ns)	M	Yes [ ]
G4	Auto-negotiation	97.8.1	If supported per Clause 98	O	Yes [ ] No [ ]

97.11.5 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCT1	PCS Transmit state diagram	97.3.2.2	Conform to Figure 97–14	M	Yes [ ]
PCT2	PCS Transmit bit ordering	97.3.2.2	Conform to Figure 97–5 and Figure 97–7	M	Yes [ ]
PCT3	PCS data transmission	97.3.2.2	45 80B/81B blocks are aggregated, encoded by a PHY frame encode, and then scrambled by a PCS scrambler	M	Yes [ ]
PCT4	PCS data encoding	97.3.2.2	Frames are encoded into a sequence of PAM3 symbols and transferred to the PMA	M	Yes [ ]
PCT5	Transmitted Control codes	97.3.2.2.6	Values not in Table 97–1 are not to be transmitted	M	Yes [ ]
PCT5a	Received Control codes	97.3.2.2.6	Values not in Table 97–1 are treated as an error if received	M	Yes [ ]
PCT6	Idle characters	97.3.2.2.7	Not be added within a data frame	M	Yes [ ]
PCT7	LP_IDLE characters	97.3.2.2.8	Not be added within a data frame	M	Yes [ ]
PCT8	EEE IDLE conversion	97.3.2.2.8	Convert LP_IDLE to IDLE if EEE is not supported	EEE:M	Yes [ ] N/A [ ]
PCT9	FEC	97.3.2.2.11	Reed-Solomon code (450,406)	M	Yes [ ]
PCT10	RS-FEC encoder	97.3.2.2.11	Follow the bit order described in 97.3.2.2.3	M	Yes [ ]
PCT11	Parity calculation	97.3.2.2.11	Produce the same result as the shift register implementation shown in Figure 97–8	M	Yes [ ]
PCT12	RS-FEC encoder shift register initialization	97.3.2.2.11	Set to zero before the parity calculation begins	M	Yes [ ]
PCT13	PCS MASTER scrambler	97.3.2.2.12	Conform to Figure 97–9	M	Yes [ ]
PCT14	PCS SLAVE scrambler	97.3.2.2.12	Conform to Figure 97–9	M	Yes [ ]
PCT15	PCS scrambler seed values	97.3.2.2.12	Non-zero and transmitted during the InfoField exchange	M	Yes [ ]
PCT16	EEE compliant PHYs	97.3.2.2.15	Implement Figure 97–14	EEE:M	Yes [ ] N/A [ ]
PCT17	EEE RS partial IDLE	97.3.2.2.15	Transmit no PHY frames partially filled with LP_IDLES	EEE:M	Yes [ ] N/A [ ]
PCT18	EEE without SEND_N	97.3.2.2.15	lpi_tx_mode variable is ignored when the PMA_TX-MODE.indication message does not have the values SEND_N	EEE:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PCT19	EEE NORMAL	97.3.2.2.15	The PCS passes coded data to the PMA via the PMA_UNIT-DATA.request primitive when the lpi_tx_mode variable takes the value NORMAL and when the PMA asserts SEND_N	EEE:M	Yes [ ] N/A [ ]
PCT20	EEE QUIET	97.3.2.2.15	The PCS passes zeros to the PMA via the PMA_UNIT-DATA.request primitive when the lpi_tx_mode variable takes the value QUIET and when the PMA asserts SEND_N	EEE:M	Yes [ ] N/A [ ]
PCT21	EEE REFRESH	97.3.2.2.15	The PCS passes zero data encoded through PCS data path to the PMA via the PMA_UNITDATA.request primitive when the lpi_tx_mode variable takes the value REFRESH and when the PMA asserts SEND_N	EEE:M	Yes [ ] N/A [ ]
PCT22	Wake frame	97.3.2.2.15	Be sent only during alternating PHY frame counts	EEE:M	Yes [ ] N/A [ ]
PCT23	PCS reset execution	97.3.1	When power for the device containing the PMA has reached the operating state, or on the receipt of a request for reset from the management entity	M	Yes [ ]

97.11.6 PCS Receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	PCS receive state diagram	97.3.2.3	Conform to Figure 97–12	M	Yes [ ]
PCR2	PCS Receive bit ordering	97.3.2.3	Conform to Figure 97–6	M	Yes [ ]
PCR3	PAM3 stream	97.3.2.3.1	Form stream from PMA_UNITDATA.indication primitive by concatenating requests in order from rx_data<0> to rx_data<2699>	M	Yes [ ]
PCR4	PCS descrambler	97.3.2.3	Descramble the data stream for generation of RXD<7:0> to the GMII	M	Yes [ ]
PCR5	MASTER side-stream descrambler	97.3.2.3.2	Equation (97–4)	M	Yes [ ]
PCR6	SLAVE side-stream descrambler	97.3.2.3.2	Equation (97–3)	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PCR7	Transmit PCS test pattern mode	97.3.3	Transmit continuously as illustrated in Figure 97–5	M	Yes [ ]
PCR8	Receive PCS test pattern mode	97.3.3	Receive continuously as illustrated in Figure 97–6	M	Yes [ ]
PCR9	MASTER side-stream scrambler	97.3.4	Equation (97–5)	M	Yes [ ]
PCR10	SLAVE side-stream scrambler	97.3.4	Equation (97–6)	M	Yes [ ]
PCR11	Initialized scrambler state	97.3.4	Never all zeros	M	Yes [ ]
PCR12	Scramble status	97.3.4.3	Acquire and report descrambler state synchronization via scr_status	M	Yes [ ]
PCR13	DECODE function	97.3.6.2.3	Decode the block as specified in 97.3.2.2.2	M	Yes [ ]
PCR14	ENCODE function	97.3.6.2.3	Encode the block as specified in 97.3.2.2.2	M	Yes [ ]
PCR15	Encode function encode LPI_IDLE	97.3.6.2.3	Only in SEND_LPI state	EEE:M	Yes [ ] N/A [ ]
PCR16	PCS Receive, RFER monitor, and PCS Transmit state diagrams	97.3.6.4	Figure 97–12, Figure 97–13, and Figure 97–14	M	Yes [ ]

97.11.7 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCO1	PCS loopback mode	97.3.7.3	Enabled when MDIO register 3.2304.14 is set to a one.	MDIO:M	Yes [ ]
PCO2	PCS loopback enabled	97.3.7.3	PCS accepts data on the transmit path from the GMII and return it on the receive path to the GMII when in loopback mode when in loopback mode	M	Yes [ ]
PCO3	PCS loopback enabled	97.3.7.3	Transmit a continuous stream of GMII data to the 81B encoder and then to PMA sublayer and ignore all data presented to it by the PMA sublayer	M	Yes [ ]

97.11.8 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Value/Comment	Status	Support
PMF1	PMA Reset function	97.4.2.1		M	Yes [ ]
PMF2	PMA Transmit function	97.4.2.2	Continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb after processing with optional transmit filtering.	M	Yes [ ]
PMF3	Signals generated by PMA transmit	97.4.2.2	Comply with 97.5	M	Yes [ ]
PMF4	MASTER TX_TCLK source	97.4.2.2	Local clock source while meeting the transmit jitter requirements of 97.5.3.3	M	Yes [ ]
PMF5	The MASTER-SLAVE relationship	97.4.2.2	Include loop timing	M	Yes [ ]
PMF6	SLAVE TX_TCLK source	97.4.2.2	Recovered clock of 97.4.2.8 while meeting the jitter requirements of 97.5.3.3.	M	Yes [ ]
PMF7	PMA_transmit_disable variable	97.4.2.2.1	When set to true, turn off the transmitter so that the transmitter Average Launch Power of the Transmitter is less than –53 dBm	M	Yes [ ]
PMF8	Quality of rx_symb symbols	97.4.2.3	Allow RFER of less than 3.6×10^{-7} after RS-FEC decoding, over a channel meeting the requirements of 97.6	M	Yes [ ]
PMF9	PMA receive fault function	97.4.2.3	Contribute to the receive fault bit specified in 45.2.1.134.6	MDIO:O	Yes [ ] N/A [ ]
PMF10	PHY Control	97.4.2.4	Comply with Figure 97–26	M	Yes [ ]
PMF11	12-octet InfoField	97.4.2.4	Include the fields in 97.4.2.4.2 through 97.4.2.4.8	M	Yes [ ]
PMF12	Each unique InfoField	97.4.2.4	Transmitted at least 256 times	M	Yes [ ]
PMF13	InfoField Reserved bits	97.4.2.4.1	Set to zero on transmit and ignored when received by the link partner	M	Yes [ ]
PMF14	Start of Frame Delimiter	97.4.2.4.2	Hexadecimal value 0xB-BA700	M	Yes [ ]
PMF15	PMA_state<7:6>	97.4.2.4.4	Communicate the state of the transmitting transceiver to the link partner	M	Yes [ ]
PMF16	Any Message Field value not listed in Table 97–7 or Table 97–8	97.4.2.4.4	Not be transmitted and ignored at the receiver	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PMF17	The Message Field setting for the first transmitted PMA frame	97.4.2.4.4	First row of Table 97–7 for the MASTER and the first or second row of Table 97–8 for the SLAVE	M	Yes [ ]
PMF18	Indicate support of optional capabilities	97.4.2.4.5	Set the corresponding capability bits	M	Yes [ ]
PMF19	State of the scrambler	97.4.2.4.5	S14:S0 at the first bit of the first PHY frame when the partial PHY frame counter equals to the DataSwPFC24 value	M	Yes [ ]
PMF20	Seed S<14:0>	97.4.2.4.5	Not all zeros	M	Yes [ ]
PMF21	DataSwPFC24	97.4.2.4.6	Set to an integer multiple of 15	M	Yes [ ]
PMF22	CRC16 (2 octets)	97.4.2.4.8	Implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 7 octets	M	Yes [ ]
PMF23	CRC16	97.4.2.4.8	Figure 97–23	M	Yes [ ]
PMF24	CRC16 delay elements	97.4.2.4.8	Initialized to zero	M	Yes [ ]
PMF25	Start-up sequence	97.4.2.4.10	Comply with Figure 97–26	M	Yes [ ]
PMF26	Enable EEE capability	97.4.2.4.10	Enabled if both PHYs set EEEen = 1	EEE:M	Yes [ ] N/A [ ]
PMF27	Set en_slave_tx = 1	97.4.2.4.10	After the MASTER has sufficiently converged the necessary circuitry, allowing the SLAVE to transition to TRAINING	M	Yes [ ]
PMF28	Enable 1000BASE-T1 OAM capability	97.4.2.4.10	Enabled only if both PHYs set OAMen = 1	M	Yes [ ]
PMF29	SLAVE PHY TRAINING	97.4.2.4.10	Align transmit 81B-RS frame within +0/–1 partial PHY frames of the MASTER	M	Yes [ ]
PMF30	SLAVE InfoField partial PHY frame Count	97.4.2.4.10	Match MASTER InfoField partial PHY frame Count for the aligned frame	M	Yes [ ]
PMF31	Link Monitor function	97.4.2.5	Comply with Figure 97–27	M	Yes [ ]
PMF32	Refresh monitor function	97.4.3		EEE:M	Yes [ ] N/A [ ]
PMF33	Set PMA_refresh_status to FAIL	97.4.3	When Refresh is not detected within a moving window of 50 Q/R cycles	EEE:M	Yes [ ] N/A [ ]
PMF34	Set PMA_refresh_status to OK	97.4.3	When Link Monitor state diagram enters LINK_UP state	EEE:M	Yes [ ] N/A [ ]
PMF35	Clock Recovery function	97.4.2.8	Provide a clock suitable for signal sampling so that RS FER is achieved	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PMF36	maxwait_timer	97.4.4.2	Expire 97.5 ms ± 0.5 ms after being started	M	Yes [ ]
PMF37	minwait_timer	97.4.4.2	Expire 975 μs ± 50 μs after being started	M	Yes [ ]
PMF38	sigdet_wait_timer	97.4.2.6.2	Expires 4 μs ± 0.1 μs after being started	M	Yes [ ]
PMF39	send_s_timer	97.4.2.6.2	Expires 1.0 μs ± 0.04 μs after being started	M	Yes [ ]
PMF40	send_s_sigdet	97.4.2.6.1	Set to false no later than 1 μs after the signal goes quiet on the MDI	M	Yes [ ]
PMF41	Auto-Negotiation function used for PHY synchronization	97.4.2.6		M	Yes [ ]
PMF42	Function of Figure 97–25	97.4.2.6	Used to synchronize 1000BASE-T1 PHYs prior to the 1000BASE-T1 link training	M	Yes [ ]
PMF43	PN sequence generator shift registers reset	97.4.2.6	The PN sequence generator shift registers are reset to a non-zero value upon entering into the TRANSMIT_DISABLE state (see Figure 97–25)	M	Yes [ ]
PMF44a	SLAVE PN sequence generator	97.4.2.6	See Equation (97–9)	M	Yes [ ]
PMF44b	MASTER PN sequence generator	97.4.2.6	See Equation (97–8)	M	Yes [ ]
PMF45	The next Message Field setting	97.4.2.4.4	Equal to the same Message Field setting or the Message Field setting corresponding to a row below the current setting	M	Yes [ ]

97.11.9 PMA electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PME1	DPI and 150 Ω emission tests	97.5.1	Used to establish a baseline for PHY EMC performance	M	Yes [ ]
PME2	DPI method of IEC 62132-4	97.5.1.1	Used to test the sensitivity of the PMA receiver to radio frequency noise	M	Yes [ ]
PME3	150 Ω direct coupling method of IEC 61967-4	97.5.1.2	Used to test the conducted CM emission of the PMA transmitter to its electrical environment	M	Yes [ ]
PME4	Test modes	97.5.2	Provided to allow for testing the transmitter	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PME5	Test modes	97.5.2	Enabled by setting control register 1.2308.15:13	MDIO:M	Yes [ ] N/A [ ]
PME6	Test mode change data only	97.5.2	The test modes only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.	M	Yes [ ]
PME7	Test mode 1	97.5.2	Provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125 when in test mode 1	M	Yes [ ]
PME8	Test mode 2	97.5.2	Transmit three {+1} symbols followed by three {–1} symbols continually	M	Yes [ ]
PME9	Test mode 3	97.5.2	Transmit three {+1} symbols followed by three {–1} symbols continually	M	Yes [ ]
PME10	Test mode 4	97.5.2	Transmit the sequence of symbols generated by the scrambler generator polynomial per Equation (97–12) when in test mode 4	M	Yes [ ]
PME10a	Test Mode 4 transmit clock	97.5.2	750 MHz ± 0.01% clock when in MASTER timing mode	M	Yes [ ]
PME10b	Test mode 4 signal level	97.5.2	Same as non-test mode	M	Yes [ ]
PME10c	Test mode 4 Sequence generator clock	97.5.2	2/750 MHz	M	Yes [ ]
PME10d	Test mode 4 ternary symbols $T0_n$ and $T1_n$	97.5.2	Generated from bits $x0_n$, $x1_n$, and $x2_n$ of the test mode 4 sequence generator	M	Yes [ ]
PME11	Test mode 5	97.5.2	Transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals	M	Yes [ ]
PME12	Test mode 6	97.5.2	Transmit fifteen {+1} symbols followed by fifteen {–1} symbols continually	M	Yes [ ]
PME12a	Test fixtures	97.5.2.1	Per Figure 97–29, Figure 97–30, Figure 97–31, Figure 97–32, and Figure 97–33 or equivalent	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PME12b	Disturbing signal characteristics	97.5.2.1	Sinusoidal, amplitude of 3.6 V peak-to-peak differential, and frequency of one-sixth the symbol rate (125 MHz) synchronous with the test pattern	M	Yes [ ]
PME13	Tolerance of resistors used in test fixtures	97.5.2.1	± 0.1%	M	Yes [ ]
PME14	Disturbing signal generator	97.5.2.1	Have sufficient linearity and range so it does not introduce any appreciable distortion	M	Yes [ ]
PME15	Coupling	97.5.3	Operate with AC coupling to the MDI	M	Yes [ ]
PME16	Resistive differential load	97.5.3	Meet electrical requirements of this clause with a 100 Ω resistive differential load connected to transmitter output if load is not specified	M	Yes [ ]
PME17	Magnitude of both the positive and negative droop	97.5.3.1	Less than 10% measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing	M	Yes [ ]
ME17a	Transmitter distortion signal capture	97.5.3.2	At least 40 µs long and sampled at a rate of at least 7.5 Gs/s (10 times the transmit symbol rate of 750 Ms/s)	M	Yes [ ]
PME18	Transmitter distortion	97.5.3.2	Less than 15 mV for at least 10 measured equally spaced phases	M	Yes [ ]
PME19	Transmitter distortion test mode 4 capture	97.5.3.2	Minimum of 40 µs long and minimum sampling rate of 7.5 Gs/s	M	Yes [ ]
PME20	MASTER TX_TCLK125 jitter RMS	97.5.3.3	Less than 5 ps RMS	M	Yes [ ]
PME21	MASTER TX_TCLK125 jitter Peak-to-Peak	97.5.3.3	Less than 50 ps peak-to-peak	M	Yes [ ]
PME22	SLAVE TX_TCLK125 jitter RMS	97.5.3.3	Less than 10 ps RMS	M	Yes [ ]
PME23	SLAVE TX_TCLK125 jitter Peak-to-Peak	97.5.3.3	Less than 100 ps peak-to-peak	M	Yes [ ]
PME23b	TX_TCLK125 jitter measurement bandwidth	97.5.3.3	Larger than 2 MHz	M	Yes [ ]
PME24	Reference clock	97.5.3.3	Reference clock is continuous when transitioning into or out of LPI mode	EEE:M	Yes [ ] N/A [ ]
PME25	MDI output jitter RMS	97.5.3.3	Less than 5 ps RMS	M	Yes [ ]
PME25a	MDI output jitter Peak to Peak	97.5.3.3	Less than 50 ps RMS	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PME25b	MDI jitter measurement bandwidth	97.5.3.3	Larger than 2 MHz	M	Yes [ ]
PME26	Transmit power in test mode 5	97.5.3.4	Less than 5 dBm	M	Yes [ ]
PME27	Power spectral density in test mode 5	97.5.3.4	Between the upper and lower masks specified in Equation (97–14) and Equation (97–15), when measured into a 100 Ω load using the test fixture 5 shown in Figure 97–33	M	Yes [ ]
PME28	TX_TCLK125 jitter measurement	97.5.3.3	Measured over an interval of 1 ms ± 10%	M	Yes [ ]

97.11.10 MDI electrical requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PMI1	Transmit differential signal	97.5.3.5	Less than 1.30 V peak-to-peak for all transmit modes when measured with 100 Ω reference termination	M	Yes [ ]
PMI2	MASTER PHY symbol transmission rate	97.5.3.6	Within the range 750 MHz ± 100 ppm	M	Yes [ ]
PMI3	LPI mode the short-term rate of frequency variation	97.5.3.6	Less than 0.1 ppm/second	EEE:M	Yes [ ] N/A [ ]
PMI4	Receiver differential input signals	97.5.4.1	Frame loss ratio less than 10^{-7} for 125-octet frames	M	Yes [ ]
PMI5	Frame loss ratio for operation on link segment type B	97.5.4.1	Met for link segments specified at 97.6.2 and 97.6.4	LSTB:M	Yes [ ] N/A [ ]

97.11.10.1 Characteristics of the link segment

Item	Feature	Subclause	Value/Comment	Status	Support
LKS2	Insertion loss of each type A link segment	97.6.1.1	Equation (97–16)	CHNL:M	Yes [ ] N/A [ ]
LKS3	Return loss (with 100 Ω reference impedance) of each type A link segment	97.6.1.3	Equation (97–17)	CHNL:M	Yes [ ] N/A [ ]
LKS4	Differential to common mode conversion of each type A link segment	97.6.1.4	Equation (97–18) for all frequencies from 10 MHz to 600 MHz	CHNL:M	Yes [ ] N/A [ ]
LKS5	Maximum link delay for type A link segment	97.6.1.5	Not exceed 94 ns at all frequencies between 2 MHz and 600 MHz	CHNL:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
LKS6	Insertion loss of each type B link segment	97.6.2.1	Equation (97–19)	CHNL:M	Yes [ ] N/A [ ]
LKS7	Return loss (with 100 Ω reference impedance) of each type B link segment	97.6.2.3	Equation (97–20)	CHNL:M	Yes [ ] N/A [ ]
LKS8	Maximum link delay for type B link segment	97.6.2.4	Not exceed 234 ns at all frequencies between 2 MHz and 600 MHz	CHNL:M	Yes [ ] N/A [ ]
LKS9	Coupling attenuation of the type B link segment	97.6.2.5	Table 97–14	CHNL:M	Yes [ ] N/A [ ]
LKS10	Power sum ANEXT loss between a disturbed type A link segment and the disturbing type A link segment	97.6.3.2	Equation (97–22)	CHNL:M	Yes [ ] N/A [ ]
LKS11	Power sum AACRF between a disturbed type A link segment and the disturbing type A link segment	97.6.3.4	Equation (97–24)	CHNL:M	Yes [ ] N/A [ ]
LKS12	Power sum ANEXT loss between a disturbed type B link segment and the disturbing type B link segment	97.6.4.2	Equation (97–26)	CHNL:M	Yes [ ] N/A [ ]
LKS13	Power sum AACRF between a disturbed type B link segment and the disturbing type B link segment	97.6.4.4	The lesser of Equation (97–28) and 70 dB	CHNL:M	Yes [ ] N/A [ ]

97.11.11 MDI Requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	Symbol response	97.4.3.1	Comply with 97.5	M	Yes [ ]
MDI2	MDI electrical specification	97.7.2	Meet the electrical requirements specified in 97.5.3 and 97.5.4 when the PHY is connected to the MDI connector mated with a specified balanced twisted-pair cable connector	M	Yes [ ]
MDI3	Return loss	97.7.2.1	Equation (97–29)	M	Yes [ ]
MDI4	MDI wire pair short circuit	96.8.3	Under all operating conditions withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time	M	Yes [ ]
MDI5	Operation after short circuit	96.8.3	Resume normal operation	M	Yes [ ]
MDI6	MDI wire pair transients and ESD	96.8.3	Under all operating conditions, withstand without damage high voltage transient noise and ESD per application requirements	M	Yes [ ]
MD17	MDI mode conversion loss	97.7.2.2	Equation (97–30)	M	Yes [ ]

97.11.12 EEE capability requirements

Item	Feature	Subclause	Value/Comment	Status	Support
EEE1	Transition to and from LPI mode	97.1.2.3	Cause no data frames be lost or corrupted.	EEE:M	Yes [ ] N/A [ ]
EEE2	Normal power resumption	97.1.2.3	Resume normal power mode on the PHY frame following a PCS transmission of a wake frame	EEE:M	Yes [ ] N/A [ ]
EEE3	LPI synchronization	97.3.5.1	Synchronize refresh intervals during LPI mode	EEE:M	Yes [ ] N/A [ ]
EEE4	Partial PHY frame count synchronization	97.3.5.1	When SLAVE, synchronize partial PHY frame count to MASTER's partial PHY frame count within 1 partial PHY frame	EEE:M	Yes [ ] N/A [ ]
EEE5	tx_refresh_active and tx_wake_start signals	97.3.5.1	Derive tx_refresh_active and tx_wake_start signals from the transmitted PHY frames	EEE:M	Yes [ ] N/A [ ]
EEE6	Quiet period	97.3.5.2	Transmit PAM3 symbol zero on to the MDI	EEE:M	Yes [ ] N/A [ ]

97.11.13 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	97.9.1	Conforms to IEC 60950-1 (for IT and motor vehicle applications) and to ISO 26262 (for motor vehicle applications only, if required by the given application)	M	Yes [ ]
ES1a	Conforms to ISO 26262	97.9.1	If intended for motor vehicle applications	AUTO: M	Yes [ ] N/A[ ]
ES2	Environmental safety	97.9.2.1	Conform to the potential environmental stresses with respect to their mounting location, as defined in: ISO 16750-1, ISO 16750-2, ISO 17637-2:2008, ISO 8820-1, ISO 16750-3, ASTM D4728, ISO 12103-1, ISO 16750-4, IEC 60068-2–1/27/30/38/52/64/78, ISO 167540-5, and ISO 20653	AUTO: M	Yes [ ] N/A[ ]
ES3	Electromagnetic compatibility: local and national codes	97.9.2.2	Compliance with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]
ES4	Electromagnetic compatibility: EMC test methods	97.9.2.2	Tested according to IEC CISPR 25 test methods defined to measure the PHY's EMC performance	M	Yes [ ]
ES5	Electromagnetic compatibility: motor vehicle EMC requirements	97.9.2.2	Meet the following motor vehicle EMC requirements: CISPR 25, IEC 61967–1/4, IEC 61000-4-21, ISO 11452, IEC 62132–1/4, IEC 61000-4-21, ISO 10605, IEC 61000-4-2/3, IEC 62215-3, ISO 7637-2/3	AUTO: M	Yes [ ] N/A[ ]

98. Auto-Negotiation for single differential-pair media

98.1 Overview

98.1.1 Scope

Clause 98 describes the single twisted-pair Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. Annex 98A describes the Selector Field that is used by Auto-Negotiation to identify the type of message being sent.

The objective of the single twisted-pair Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. It has the additional objective of providing a common synchronization time between two devices prior to link training.

Single twisted-pair Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC balanced signal. DME does not add packet or upper layer overhead to the network devices. DME is transferred in a half-duplex manner over the single twisted-pair copper cable.

Single twisted-pair Auto-Negotiation does not test the link segment characteristics.

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The single twisted-pair Auto-Negotiation function allows the identification of the operational mode of the link partner. Should multiple modes be present, management may select between the various offered modes. How such selection is done is beyond the scope of this standard.

98.1.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The single twisted-pair Auto-Negotiation function is provided at the Physical Layer of the ISO/IEC OSI reference model as shown in Figure 98–2. A device that supports multiple modes of operation may advertise its capabilities using the single twisted-pair Auto-Negotiation function. The actual transfer of information is observed only at the MDI.

98.2 Functional specifications

The single twisted-pair Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PHY type, where more than one PHY type may exist. A management interface provides control and status of single twisted-pair Auto-Negotiation, but the presence of a management agent is not required.

Auto-Negotiation shall provide the following functions (as shown in Figure 98–1):

a) Transmit
b) Receive
c) Half duplex
d) Arbitration

These functions shall comply with the state diagrams from Figure 98–7 through Figure 98–10. The single twisted-pair Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology Dependent Interface (see 98.4).

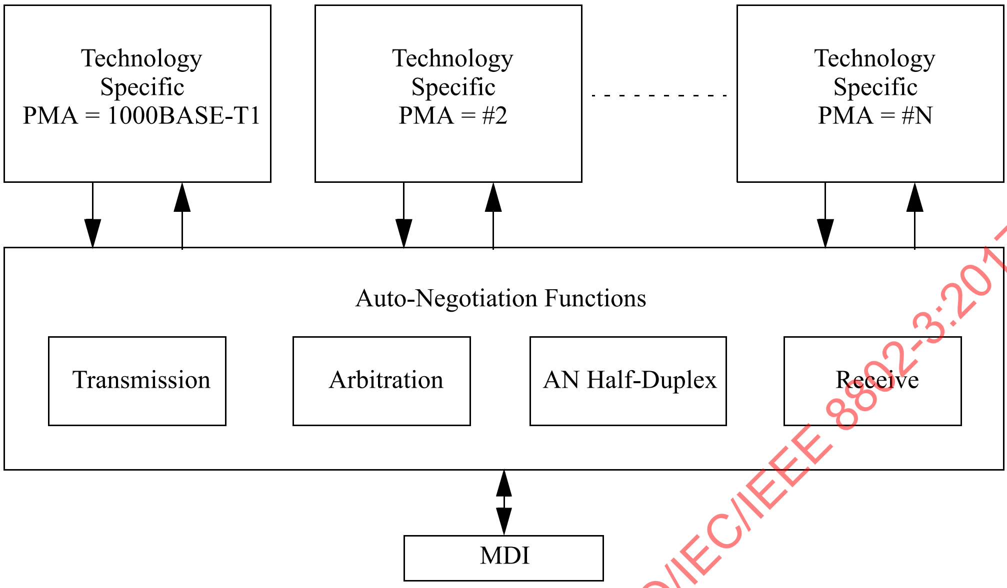


Figure 98–1—High-level model

98.2.1 Transmit function requirements

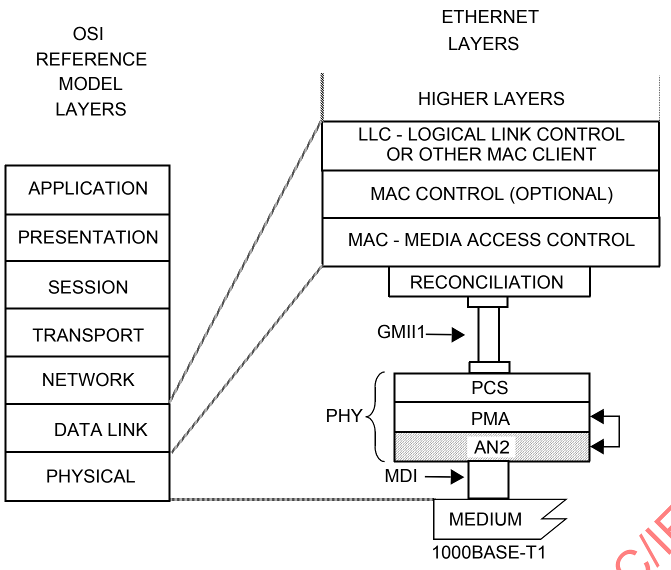
The Transmit function provides the ability to transmit pages. The first pages exchanged by the local device and its link partner after Power-On, link restart, or renegotiation contain the base link codeword defined in Table 98–2. The local device may modify the link codeword to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multi-ability devices may Auto-Negotiate to a mode lower in priority than the highest common ability.

98.2.1.1 DME transmission

Auto-Negotiation’s method of communication builds upon the encoding mechanism known as differential Manchester encoding (DME). The DME page encodes the data that is used to control the Auto-Negotiation function. DME pages shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PHY has been enabled.

98.2.1.1.1 DME page encoding

A DME page carries a 48-bit Auto-Negotiation page. It consists of 157 evenly spaced transition positions starting from the initial transition from silent to active in the preamble. The page contains a Start Delimiter, the 48-bit page, 16-bit CRC, and an end delimiter (see Figure 98–6). The odd-numbered transition positions represent clock information. The even numbered transition positions represent data information. DME pages are alternately transmitted between the two devices with quiet period separating the DME pages. When the DME page is active, the PHY shall transmit either +1 or –1 level with the voltage levels as specified in 98.2.1.1.4.



MDI = MEDIUM DEPENDENT INTERFACE
GMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

NOTE 1—GMII is optional.
NOTE 2—Auto-Negotiation is optional. Auto-Negotiation communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.

Figure 98–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

The first 26 transition positions contain the Start Delimiter, which marks the beginning of the page. The Start Delimiter contains a transition from quiet to active at position 1 followed by transitions at positions 2, 3, 5, 7, 8, 12, 13, 14, 15, 19, 21, 24, 25, 26 and no transitions at the remaining positions.

The final 2 transition positions contain the ending delimiter, which marks the end of the page. The ending delimiter contains a transition at position 155 and no transitions at the remaining positions. Position 157 contains a transition from active to quiet.

Each of the remaining 64 odd-numbered transition positions between the starting and ending delimiters shall contain a transition. The remaining 64 even-numbered transition positions shall represent data information as follows:

— A transition present in an even-numbered transition position represents a logical one.
— A transition absent from an even-numbered transition position represents a logical zero.

The first 48 of these positions shall carry the data of the Auto-Negotiation page. The final 16 positions carry the 16-bit CRC.

The CRC16 polynomial is $x^{16} + x^{15} + x^2 + 1$. The CRC16 shall produce the same result as the implementation shown in Figure 98–3. The 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards the 48 data bits are used to compute the CRC16 with the switch connected (setting CRCgen). After all the 48 bits have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

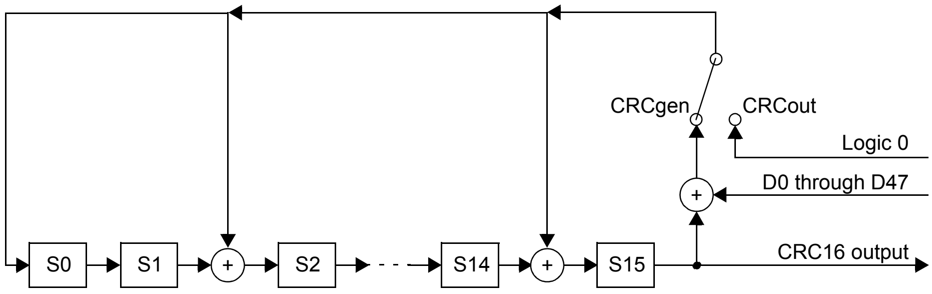


Figure 98–3—CRC16

The polarity at position 0 is randomly determined in an implementation specific manner.

The purpose of randomizing the starting polarity is to remove the spectral peaks that would otherwise occur when sending the same DME page repeatedly. Randomly choosing the starting polarity results in randomly inverting or not inverting the encoded page so that repetitions of the same page no longer produce a periodic signal.

Clock transition positions are differentiated from data transition positions by the spacing between them, as shown in Figure 98–4 and enumerated in Table 98–1.

The encoding of data using DME bits in a DME page is illustrated in Figure 98–4.

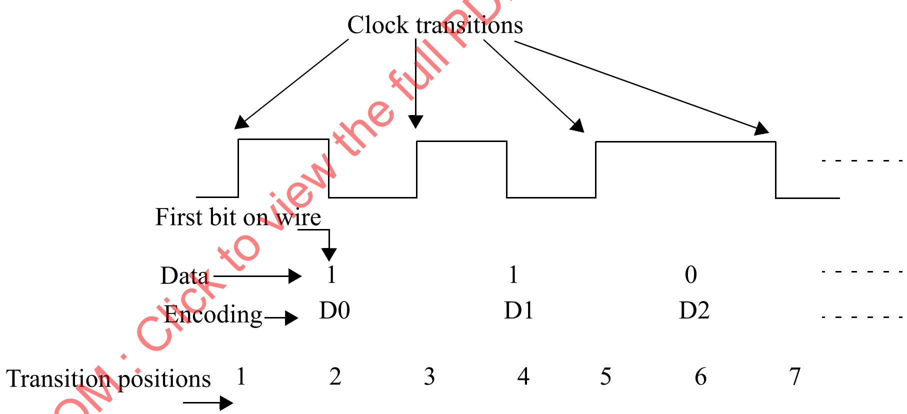


Figure 98–4—Data bit encoding within DME pages

98.2.1.1.2 DME page timing

The timing parameters for DME pages shall be followed as in Table 98–1. The transition positions within a DME page are spaced with a period of T1. T2 is the separation between clock transitions. T3 is the time from a clock transition to a data transition representing a one. The period, T1, shall be 30.0 ns ± 0.01%. Transitions shall occur within ± 0.8 ns of their ideal positions.

T5 specifies the duration of a DME page. The minimum number of transitions and maximum number of transitions in a page is represented by T4a. T4b indicates that the start of a DME page begins with a transition from 0 to ±1 and the end of the DME page is a transition from ±1 to 0.