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INTERNATIONAL STANDARD

colour inside

Information technology – Small computer system interface (SCSI) – Part 154: Serial Attached SCSI - 3 (SAS-3)

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INFORMATION TECHNOLOGY – SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 154: Serial Attached SCSI - 3 (SAS-3)

FOREWORD

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International Standard ISO/IEC 14776-154 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

This publication contains attached files in the form of S-parameter files required for electrical performance measurements and examples of scripts for running simulations.

The list of all currently available parts of the ISO/IEC 14776 series, under the general title *Information technology – Small computer system interface (SCSI)*, can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2, except as described in 3.4 and 3.5..

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INTRODUCTION

General

The SCSI family of standards provides for many different transport protocols that define the rules for exchanging information between different SCSI devices. This document specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer - 3 (SPL-3) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 3 (SAS-3), defining the rules for exchanging information between SCSI devices using a serial interconnect. Other SCSI transport protocol standards define the rules for exchanging information between SCSI devices using other interconnects.

Figure 1 shows the relationship of this document to the other standards and related projects in the SCSI family of standards.

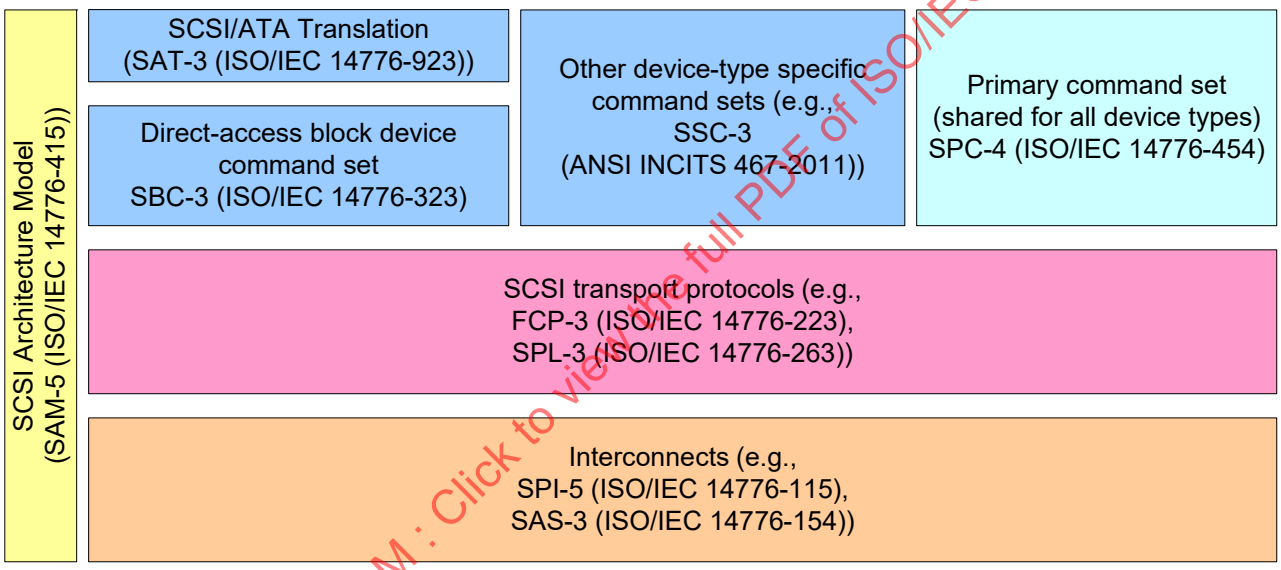

Figure 1 – SCSI document relationships

Figure 2 shows the relationship of this document to other standards and related projects in the ATA family of standards.

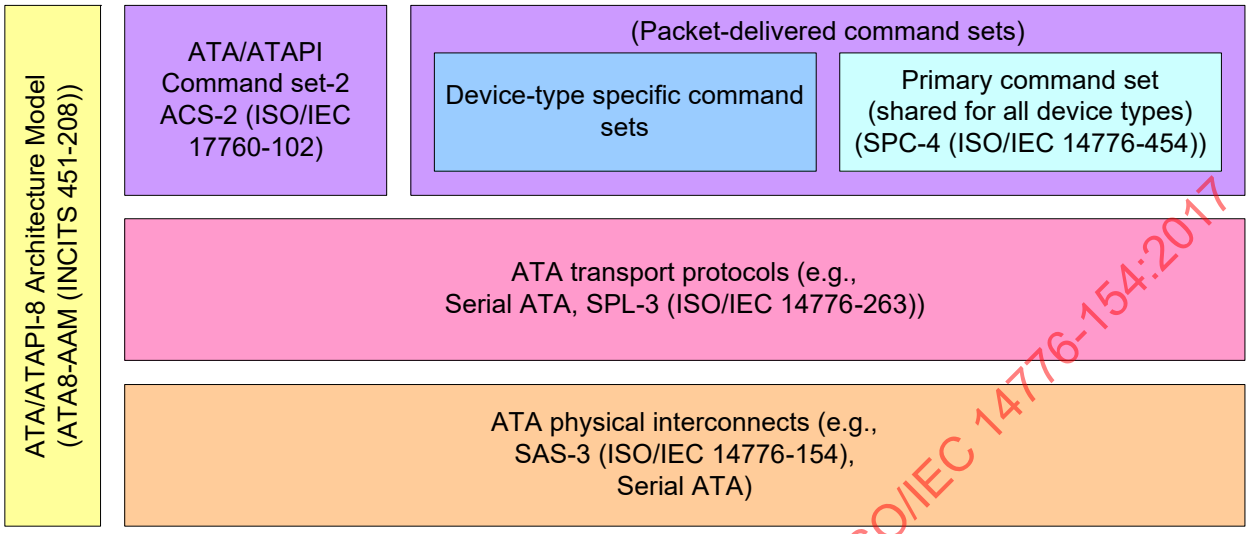

Figure 2 – ATA document relationships

Figure 1 and figure 2 show the general relationship of the documents to one another, and do not imply a relationship such as a hierarchy, protocol stack or system architecture.

These standards specify the interfaces, functions and operations necessary to ensure interoperability between conforming implementations. This document is a functional description. Conforming implementations may employ any design technique that does not violate interoperability.

INFORMATION TECHNOLOGY – SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 154: Serial Attached SCSI - 3 (SAS-3)

1 Scope

This part of ISO/IEC 14776 defines the physical layer of the Serial Attached SCSI (SAS) interconnect.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC TR 14165-117, *Information technology – Fibre channel – Part 117: Methodologies for jitter and signal quality (MJSQ)* [1] [2]

ISO/IEC 14776-151, *Information technology - Small Computer System Interface (SCSI) – Part 151: Serial Attached SCSI -1.1 (SAS-1.1)*

ISO/IEC 14776-153, *Information Technology - Small Computer System Interface (SCSI) – Part 153: Serial Attached SCSI - 2.1 (SAS-2.1)*

INCITS 457-2010, *Information Technology - Serial Attached SCSI - 2 (SAS-2)*

INCITS 492-2015, *SAS Protocol Layer-3 (SPL-3)*

INCITS 515-2016, *SCSI Architecture Model - 5 (SAM-5)*

Serial ATA Revision 3.1 (SATA). 18 July 2011 [3]

SFF-8086, *Compact Multilane Series: Common Elements* [4]

SFF-8087, *Compact Multilane Series: Unshielded* [4]

SFF-8088, *Compact Multilane Series: Shielded* [4]

SFF-8147, *54mm x 71mm Form Factor w/micro SAS Connector* [4]

SFF-8223, *2.5" Drive Form Factor with Serial Connector* [4]

SFF-8323, *3.5" Drive Form Factor with Serial Connector* [4]

SFF-8410, *HSS Copper Testing and Performance Requirements* [4]

SFF-8416, *Measurement and Performance Requirements for HPEI Bulk Cable* [4]

SFF-8449, *Mini Multilane Series Management Interface* [4]

SFF-8460, *HSS Backplane Design Guidelines* [4]

SFF-8484, *Multi-Lane Unshielded Serial Attachment Connectors* [4]

SFF-8485, *Serial GPIO (SGPIO) Bus* [4]

SFF-8486, *Serial Attachment Micro Connector* [4]

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1. INCITS TR-35-2004
2. When MJSQ is referenced from this document, the FC Port terminology used within MJSQ is substituted with SAS phy terminology.
3. Serial ATA specifications are available from the Serial ATA International Organization (see http://www.sata-io.org).
4. SFF specifications are available from the SNIA SFF Technology Affiliate (see http://www.snia.org/sff).

SFF-8523, *5.25" Drive Form Factor with Serial Connector* [4]

SFF-8630, *Serial Attachment 12 Gbs 4X Unshielded Connector (Style B)* [4]

SFF-8636, *Shielded Cables Common Management Interface* [4]

SFF-8639, *Multifunction 12 Gb/s 6X Unshielded Connector* [4]

SFF-8643, *Mini Multilane Series: Unshielded HD Integrated Connector* [4]

SFF-8644, *Mini Multilane Series: Shielded HD Integrated Connector* [4]

SFF-8680, *Serial Attachment 12 Gb/s 2X Unshielded Connector* [4]

SFF-8685, *QSFP+ 14 Gb/s 4X Pluggable Transceiver Solution (QSFP14)* [4]

SFF-9639, *Multifunction 12 Gb/s 6X Unshielded Connector Pinouts* [4]

Touchstone® *File Format Specification*. Revision 1.1. IBIS Open Forum [1]

1. Touchstone® is a registered trademark of Agilent Corporation. This information is given for the convenience of users of this document and does not constitute an endorsement by IEC or ISO. For more information on the Touchstone specification, contact the IBIS Open Forum (see http://www.eigroup.org).

3 Terms, definitions, symbols, abbreviations, keywords, and conventions

3.1 Terms and definitions

For the purposes of this document the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

"IEC Electropedia: available at http://www.electropedia.org/
"ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
active cable assembly
cable assembly (see 3.1.9) that requires power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.2
alternating current
A.C.
non-D.C. component of a signal

Note 1 to entry: In this document, all frequency components greater than or equal to 100 kHz.

3.1.3
baud rate
nominal signaling speed, expressed as the maximum number of times per second that the signal (see 3.1.97) may change the state of the physical link (see 3.1.67)

Note 1 to entry: Each state change produces a transition (i.e., signal edge).

Note 2 to entry: Baud rate is the reciprocal of the UI (i.e., $f_{baud} = 1 / UI$) (see 3.1.116).

3.1.4
bit error ratio
BER
number of logical bits output from a receiver circuit that differ from the correct transmitted logical bits, divided by the number of transmitted logical bits

Note 1 to entry: BER is computed on the raw bit stream before 10b8b decoding.

Note 2 to entry: BER is usually expressed as a coefficient and a power of 10 (e.g., 2 erroneous bits out of 100 000 bits transmitted is expressed as 2 out of 10^5 or 2×10^{-5}).

Note 3 to entry: See MJSQ.

3.1.5
bit time
nominal duration of a signal transmission bit (e.g., 666.$\overline{6}$ ps at 1.5 Gbit/s, 333.$\overline{3}$ ps at 3 Gbit/s, 166.$\overline{6}$ ps at 6 Gbit/s, and 83.$\overline{3}$ ps at 12 Gbit/s)

3.1.6
bounded uncorrelated jitter
BUJ
part of DJ (see 3.1.24) not aligned in time with the signal being measured

Note 1 to entry: Specifically, BUJ excludes ISI (see 3.1.48) and duty cycle distortion.

Note 2 to entry: See MJSQ.

3.1.7
burst time
part of an OOB signal (see 3.1.61) where the OOB burst (see 3.1.57) is transmitted

Note 1 to entry: See 5.11.

3.1.8
byte
sequence of eight contiguous bits considered as a unit

3.1.9
cable assembly
bulk cable with a separable connector at each end plus any retention, backshell, shielding features, or circuitry used for cable management or signal transmission

Note 1 to entry: See 5.4.3.

3.1.10
clock data recovery
CDR
function provided by the receiver circuit responsible for producing a regular clock signal (i.e., the recovered clock) from the received signal and for aligning the recovered clock to the symbols (i.e., bits) being transmitted with the signal

Note 1 to entry: CDR uses the recovered clock to recover the bits.

Note 2 to entry: See MJSQ.

3.1.11
common SSC transmit clock
implementation that employs a single transmit clock for multiple transmitter devices and enables or disables SSC (see 5.8.6) on the transmit clock signal to all transmitter devices in common rather than allowing each transmitter device to independently control SSC

3.1.12
compliance point
interoperability point where interoperability specifications are met

Note 1 to entry: See 5.3.

3.1.13
compliant jitter tolerance pattern
CJTPAT
test pattern for jitter testing

Note 1 to entry: See 5.8.3.5 and Annex A.

3.1.14
connector
electro-mechanical components consisting of a receptacle and a plug that provide a separable interface between two transmission segments

Note 1 to entry: See 5.4.3.

3.1.15
consecutive identical digits
CID
serial bit stream with repeated data bits of the same binary value

3.1.16
cumulative distribution function
CDF
probability that jitter (see 3.1.49) is less than a given value

Note 1 to entry: See MJSQ.

3.1.17
D.C. idle
differential signal level that is nominally 0 V(P-P), used during the idle time (see 3.1.46) and negation time (see 3.1.56) of an OOB signal (see 3.1.61) when D.C. mode (see 3.1.18) is enabled

Note 1 to entry: See 5.8.4.

3.1.18
D.C. mode
mode in which D.C. idle (see 3.1.17) is used during the idle time (see 3.1.46) and negation time (see 3.1.56) of an OOB signal (see 3.1.61)

3.1.19
data dependent jitter
DDJ
jitter (see 3.1.49) that is added when the transmission pattern is changed from a clock-like to a non-clock-like pattern

Note 1 to entry: See MJSQ.

3.1.20
decibel
dB
ten times the common logarithm (i.e., $\log_{10}$) of the ratio of relative powers

Note 1 to entry: The ratio of powers P_1 and P_2 in dB is $10 \times \log_{10} (P_1 / P_2)$. If $P_1 = V_1^2 / R_1$, $P_2 = V_2^2 / R_2$, and $R_1 = R_2$, then this ratio is equivalent to 20 times the common logarithm of the relative voltage ratio (i.e., dB is $20 \times \log_{10} (V_1 / V_2)$). A ratio of 1 results in a dB value of 0 (e.g., $20 \times \log_{10} (1) = 0$ dB), a ratio greater than 1 results in a positive dB value (e.g., $20 \times \log_{10} (2) = 6$ dB) and a ratio less than 1 results in a negative dB value (e.g., $20 \times \log_{10} (0.5) = -6$ dB).

3.1.21
dB millivolts
dBmV
decibel ratio of an rms voltage value relative to 1 mV

Note 1 to entry: 20 mV(rms) is equal to $20 \times \log_{10}(20 \text{ mV} / 1 \text{ mV}) = 26$ dBmV. This does not depend on the impedance level.

3.1.22
dB milliwatts
dBm
decibel ratio of a power value relative to 1 mW

Note 1 to entry: 20 mW is equal to $10 \times \log_{10}(20 \text{ mW} / 1 \text{ mW}) = 13$ dBm. If power is measured with a 50 Ω impedance level, then 20 mW is equivalent to $(0.02 \text{ W} \times 50 \Omega)^{(1/2)} = 1$ V or 60 dBmV. If power is measured with a 25 Ω impedance level (i.e., the reference impedance for common mode measurements), then 20 mW is equivalent to $(0.02 \text{ W} \times 25 \Omega)^{(1/2)} = 0.707$ V or 57 dBmV.

3.1.23
decision feedback equalizer
DFE
nonlinear equalizer that uses a feedback loop based on previously decoded symbols

3.1.24
deterministic jitter
DJ
jitter (see 3.1.49) with non-Gaussian distribution that is bounded in amplitude and has specific causes

Note 1 to entry: See MJSQ.

3.1.25
direct current
D.C.
non-A.C. component of a signal

Note 1 to entry: In this document, all frequency components below 100 kHz.

3.1.26
disparity
difference between the number of ones and zeros in a character

Note 1 to entry: See SPL-3.

3.1.27
dispersion
signal pulse broadening and distortion from all causes

3.1.28
duty cycle distortion
DCD
one-half of the difference of the average width of a one and the average width of a zero in a signal waveform eye pattern measurement

Note 1 to entry: See MJSQ.

3.1.29
dword
sequence of four contiguous bytes or four contiguous characters considered as a unit

Note 1 to entry: See SPL-3.

3.1.30
electromagnetic interference
EMI
any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics/electrical equipment

3.1.31
enclosure
box, rack, or set of boxes providing the powering, cooling, mechanical protection, EMI protection, and external electronic interfaces for one or more end device(s) (see 3.1.35) and/or expander device(s) (see SPL-3)

Note 1 to entry: Provides the outermost electromagnetic boundary and acts as an EMI barrier.

3.1.32
enclosure in port
set of expander phys with subtractive routing attributes using the same external connector (see 5.4.3.5)

Note 1 to entry: See SPL-3.

3.1.33
enclosure out port
set of expander phys with table routing attributes in an expander device that does not support table-to-table attachment using the same external connector (see 5.4.3.5)

Note 1 to entry: See SPL-3.

3.1.34
enclosure universal port
set of expander phys with table routing attributes in an expander device that supports table-to-table attachment using the same external connector (see 5.4.3.5)

Note 1 to entry: See SPL-3.

3.1.35
end device
SAS device or SATA device that is not contained within an expander device (see 3.1.38)

Note 1 to entry: See SPL-3.

3.1.36
end to end simulation
simulation performed from a reference transmitter or from a captured signal to a reference receiver device

3.1.37
etch
printed circuit board copper conductor path

3.1.38
expander device
device that is part of a service delivery subsystem (see SAM-5), facilitates communication between SAS devices (see 3.1.89) and SATA devices (see 3.1.93)

Note 1 to entry: See SPL-3.

3.1.39
expander phy
phy in an expander device that interfaces to a service delivery subsystem (see SAM-5)

Note 1 to entry: See SPL-3.

3.1.40
expander port
expander device object that interfaces to a service delivery subsystem (see SAM-5) and to SAS ports in other devices

Note 1 to entry: See SPL-3.

3.1.41
external connector
bulkhead connector (see 3.1.14) that carries signals into and out of an enclosure (see 3.1.31) and exits the enclosure with only minor compromise to the shield effectiveness of the enclosure (e.g., a Mini SAS 4x receptacle or Mini SAS HD receptacle)

Note 1 to entry: See 5.4.3.5.

3.1.42
eye contour
locus of points in a signal level versus time eye diagram where the CDF of 10^{-12} in the actual signal population exists

Note 1 to entry: Comparison of the measured eye contour to the jitter eye mask determines whether a jitter eye mask violation has occurred.

Note 2 to entry: For simulations, a CDF of 10^{-15} is used.

Note 3 to entry: See 5.8.3 and MJSQ.

3.1.43
fall time
time interval for the falling signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this document, the measurement points are the 80 % and 20 % voltage levels.

Note 2 to entry: Also see rise time (see 3.1.88).

3.1.44
fanout cable assembly
cable assembly with one connector on one end and multiple connectors on the other end

Note 1 to entry: See 5.4.4.1.3.

3.1.45
field
group of one or more contiguous bits

3.1.46
idle time
part of an OOB signal (see 3.1.61) where OOB idle (see 3.1.17) is being transmitted

Note 1 to entry: See 5.11.

3.1.47
insertion loss
ratio, usually expressed in dB, of incident power to delivered power

Note 1 to entry: The dB magnitude of S_{12} or S_{21} is the negative of insertion loss in dB.

Note 2 to entry: See clause F.11.

3.1.48
intersymbol interference
ISI
reduction in the distinction of a pulse caused by overlapping energy from neighboring pulses

Note 1 to entry: Neighboring pulses are pulses that are close enough to have significant energy overlapping the affected pulse and does not imply or exclude adjacent pulses (i.e., many bit times (see 3.1.5) may separate the pulses, especially in the case of reflections).

Note 2 to entry: May result in DDJ and vertical eye closure.

Note 3 to entry: Produced by several mechanisms (e.g., dispersion, reflections, and circuits that lead to baseline wander).

Note 4 to entry: See MJSQ.

3.1.49
jitter
collection of instantaneous deviations of signal edge times at a defined signal level of the signal from the reference times (e.g., as defined by the jitter timing reference) for those events

Note 1 to entry: See MJSQ.

3.1.50
jitter timing reference
signal used as the basis for calculating the jitter in the signal under test

Note 1 to entry: See MJSQ.

3.1.51
jitter tolerance
ability of the receiver device to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal applied to the receiver device compliance point

Note 1 to entry: See MJSQ.

3.1.52
jitter tolerance pattern
JTPAT
data test pattern for jitter testing of a receiver device contained within CJTPAT

Note 1 to entry: See Annex A.

3.1.53
least mean square
LMS
algorithm for adaptively adjusting the tap coefficients of a DFE (see 3.1.23) based on the difference between the desired and actual signal

3.1.54
managed connector category
category of connectors that support a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.55
near-end crosstalk
NEXT
crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the disturbing channel

Note 1 to entry: The terminals of the disturbed channel, at which the near-end crosstalk is present, and the energized terminals of the disturbing channel are usually near each other.

3.1.56
negation time
part of an OOB signal (see 3.1.61) during which OOB idle (see 3.1.58) is transmitted after the last OOB burst (see 3.1.57)

Note 1 to entry: See 5.11.

3.1.57
OOB burst
transmission of signal transitions or ALIGN3 primitives for a burst time (see 3.1.7)

Note 1 to entry: See 5.11.1.

3.1.58
OOB idle
transmission of D.C. idle (see 3.1.17) when D.C. mode (see 3.1.18) is enabled or a defined sequence of dwords when optical mode (see 3.1.62) is enabled

3.1.59
OOB interval
time basis for burst times (see 3.1.7), idle times (see 3.1.46), negation times (see 3.1.56), and signal times (see 3.1.100) used to create OOB signals (see 3.1.61)

Note 1 to entry: See 5.11.1.

3.1.60
OOB sequence
sequence where two phys exchange OOB signals (see 3.1.61)

Note 1 to entry: See SPL-3.

3.1.61
OOB signal
pattern of idle time (see 3.1.46), burst time (see 3.1.7), and negation time (see 3.1.56) used during the link reset sequence

Note 1 to entry: See 5.11.

3.1.62
optical mode
mode in which a defined sequence of dwords is used during the idle time (see 3.1.46) and negation time (see 3.1.56) of an OOB signal (see 3.1.61)

Note 1 to entry: See 5.11.

3.1.63
passive cable assembly
cable assembly (see 3.1.9) that does not require external power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.64
passive TxRx connection
complete simplex signal path between the transmitter circuit (see 3.1.109) and receiver circuit (see 3.1.75) that does not include powered circuitry used in the transmission of the signal through the TxRx connection (see 3.1.114)

Note 1 to entry: See 5.5.1.

3.1.65
phy
object in a device that is used to interface to other devices

EXAMPLE - An expander phy (see 3.1.39) or a SAS phy (see 3.1.90).

Note 1 to entry: See 4.1.

3.1.66
physical interconnect TxRx connection segment
PICS
TxRx connection segment (see 3.1.115) used to model channel loss between the TDCS (see 3.1.113) and the RDCS (see 3.1.79)

Note 1 to entry: See 5.3.3.

3.1.67
physical link
two differential signal pairs, one pair in each direction, that connect two physical phys (see 3.1.65)

Note 1 to entry: See 4.1.

3.1.68
physical link rate
link rate between two physical phys established as a result of speed negotiation between those phys

3.1.69
power on
power being applied

3.1.70
probe point
physical position in a test load where signal characteristics for compliance points are measured

Note 1 to entry: See 5.6.

3.1.71
post cursor equalization ratio
R_{post}
ratio of the equalization peak signal voltage to the nominal signal voltage after a signal voltage change

Note 1 to entry: See 5.8.4.7.1.

3.1.72
precursor equalization ratio
R_{pre}
ratio of the equalization peak signal voltage to the nominal signal voltage prior to a signal voltage change

Note 1 to entry: See 5.8.4.7.1.

3.1.73
random jitter
RJ
jitter (see 3.1.49) that is characterized by a Gaussian distribution and is unbounded

Note 1 to entry: See MJSQ.

3.1.74
rate
data transfer rate of a physical or logical link

EXAMPLE - 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, or 12 Gbit/s.

3.1.75
receiver circuit
electronic circuit that converts an analog serial input signal to a logic signal

3.1.76
receiver circuit TxRx connection segment
RCCS
TxRx connection segment (see 3.1.115) used to model package loss within the simulated receiver circuit (see 3.1.75)

3.1.77
reference clock
clock generated by the PLL

Note 1 to entry: This clock is filtered by the JTF (see 5.8.3.2) and aligned with the zero-crossing instants.

3.1.78
receiver device
Rx
device downstream from a receiver device compliance point (see 3.1.12) containing a portion of the physical link and a receiver circuit (see 3.1.75)

3.1.79
receiver device TxRx connection segment
RDCS
TxRx connection segment (see 3.1.115) between the simulated receiver circuit (see 3.1.75) and a separable connector

3.1.80
reference pulse response cursor
peak to peak
cursor that is twice the amplitude of the response to a one UI wide positive pulse of the same amplitude and transmitter equalization as the data stream it represents (see 5.7.3), sampled at the reference sampling instant (see 3.1.83)

3.1.81
reference receiver device
set of parameters defining electrical performance characteristics that provide a set of minimum electrical performance requirements for a receiver device and that are also used in mathematical modeling to determine compliance of a TxRx connection or transmitter device

Note 1 to entry: See 5.8.5.7.3.

3.1.82
reference sampling clock
reference clock (see 3.1.77) shifted by 0.5 UI (see 3.1.116)

3.1.83
reference sampling instant
instant at which a reference sampling clock (see 3.1.82) samples the maximum amplitude of the response to a positive pulse generated using the reference sampling clock

Note 1 to entry: See figure 118.

3.1.84
reference transmitter device
set of parameters defining electrical performance characteristics of a transmitter device that are used in mathematical modeling to determine compliance of a TxRx connection

Note 1 to entry: See 5.8.4.6.5 and 5.8.4.7.3.

3.1.85
reference transmitter test load
set of S-parameters defining the electrical characteristics of a TxRx connection used as the basis for transmitter device and receiver device performance evaluation through mathematical modeling

Note 1 to entry: See 5.6.5.

3.1.86
reflection coefficient
ρ
ratio of reflected voltage to incident voltage

3.1.87
return loss
ratio, usually expressed in dB, of incident power to reflected power

Note 1 to entry: The dB magnitude of S_{11} or S_{22} is the negative of return loss in dB.

Note 2 to entry: See clause F.11

3.1.88
rise time
time interval for the rising signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this document, the measurement points are the 20 % and 80 % voltage levels.

Note 2 to entry: Also see fall time (see 3.1.43).

3.1.89
SAS device
SAS initiator device (see SPL-3) and/or SAS target device (see SPL-3)

3.1.90
SAS phy
phy in a SAS device (see 3.1.89) that interfaces to a service delivery subsystem (see SAM-5)

3.1.91
SAS target device
device containing SSP, STP, and/or SMP target ports in a SAS domain

Note 1 to entry: See SPL-3.

3.1.92
SAS target device circuitry
at a minimum, the circuitry in the SAS target device (see SPL-3) providing control of the SAS phy (see 3.1.90) and protocol support for communication through the physical link (see 3.1.67)

Note 1 to entry: Application of power to the SAS target device circuitry results in actions defined for power on (see SPL-3).

3.1.93
SATA device
ATA device that contains a SATA device port in an ATA domain

Note 1 to entry: See SPL-3.

3.1.94
SATA phy
phy in a SATA device (see SPL-3) or SATA port selector (see SPL-3) that interfaces to a service delivery subsystem (see SAM-5)

Note 1 to entry: Analogous to a SAS phy (see 3.1.90).

3.1.95
Serial ATA
SATA
protocol defined by SATA (see clause 2)

3.1.96
Serial Attached SCSI
SAS
set of protocols defined in SPL-3 and the interconnect defined by this document

3.1.97
signal
detectable transmitted energy that is used to carry information

3.1.98
signal amplitude
property of the overall signal (see 3.1.97) that describes the peak or peak to peak values of the signal level (see 3.1.99)

3.1.99
signal level
instantaneous intensity of a signal (see 3.1.97) measured in volts

3.1.100
signal time
time of an OOB signal (see 3.1.61), consisting of six burst times (see 3.1.7), six idle times (see 3.1.46), and one negation time (see 3.1.56)

Note 1 to entry: See 5.11.

3.1.101
signal tolerance
ability of the receiver device to recover transmitted bits in an incoming data stream with maximum jitter and minimum amplitude

Note 1 to entry: See MJSQ.

3.1.102
significant crosstalk
crosstalk source having a magnitude point of its transfer function in excess of -50 dB in the range of frequencies up to 6 GHz

3.1.103
sinusoidal jitter
SJ
single frequency jitter applied during signal tolerance testing

Note 1 to entry: See MJSQ.

3.1.104
spread spectrum clocking
SSC
technique of modulating the operating frequency of a transmitted signal (i.e., the physical link rate) to reduce the measured peak amplitude of radiated emissions

Note 1 to entry: See SPL-3.

3.1.105
symbol
smallest unit of data transmission on a physical link (i.e., a bit)

Note 1 to entry: A symbol represents a single transition if the maximum transition rate (i.e., a 0101b pattern) is occurring.

3.1.106
total jitter
TJ
jitter (see 3.1.73) from all sources

Note 1 to entry: See MJSQ.

3.1.107
trained
physical link rate negotiated with Train_Rx-SNW

Note 1 to entry: See SPL-3.

3.1.108
transceiver
physical entity that contains both a transmitter device (see 3.1.112) and a receiver device (see 3.1.78)

3.1.109
transmitter circuit
electronic circuit that converts a logic signal to an analog serial output signal

3.1.110
transmitter circuit TxRx connection segment
TCCS
TxRx connection segment (see 3.1.115) used to model package loss within the simulated transmitter circuit (see 3.1.109)

3.1.111
transmitter compliance transfer function
TCTF
mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask

Note 1 to entry: See 5.8.4.1.

3.1.112
transmitter device
Tx
device upstream from a transmitter device compliance point (see 3.1.12) containing a portion of the physical link and a transmitter circuit (see 3.1.109)

3.1.113
transmitter device TxRx connection segment
TDCS
TxRx connection segment (see 3.1.115) between the transmitter circuit (see 3.1.109) and a separable connector

3.1.114
TxRx connection
complete simplex signal path between the transmitter circuit (see 3.1.109) and receiver circuit (see 3.1.75)

Note 1 to entry: See 5.5.1.

3.1.115
TxRx connection segment
portion of a TxRx connection (see 3.1.114) delimited by separable connectors or changes in the conductive material

Note 1 to entry: See 5.5.1.

3.1.116
unit interval
UI
normalized, dimensionless, nominal duration of a symbol (see 3.1.105)

EXAMPLE - 666.$\overline{6}$ ps at 1.5 Gbit/s, 333.$\overline{3}$ ps at 3 Gbit/s, 166.$\overline{6}$ ps at 6 Gbit/s, and 83.$\overline{3}$ ps at 12 Gbit/s.

Note 1 to entry: The UI is the reciprocal of the baud rate (i.e., UI = 1 / f_{baud}) (see 3.1.3).

3.1.117
unmanaged active connector category
category of connectors that support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2) but do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.118
unmanaged passive connector category
category of connectors that do not support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2) and do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.119
untrained
physical link rate not negotiated with Train_Rx-SNW

Note 1 to entry: See SPL-3.

3.1.120
usage variable
SASWDP parameter set to a value that determines if the stressor file is to be added to the simulation

Note 1 to entry: See Annex B.

3.1.121
voltage modulation amplitude
VMA
difference in electrical voltage of a signal (see 3.1.97) between the stable one level and the stable zero level

3.1.122
waveform dispersion penalty
WDP
simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device

Note 1 to entry: See 5.8.4.6.1 and Annex B.

3.2 Symbols and abbreviations

3.2.1 Abbreviations

See Annex J for abbreviations of standards bodies (e.g., ISO).

Units and abbreviations used in this Document:

Abbreviation	Meaning
A.C.	alternating current (see 3.1.2)
ATA	AT attachment

Abbreviation	Meaning
AWG	American wire gauge (see ASTM Standard B 258-02) (see Bibliography)
BER	bit error ratio (see 3.1.4)
BUJ	bounded uncorrelated jitter (see 3.1.6)
C1	coefficient 1 (see 5.8.4.7.3)
C2	coefficient 2 (see 5.8.4.7.3)
C3	coefficient 3 (see 5.8.4.7.3)
CDF	cumulative distribution function (see 3.1.16)
CDR	clock data recovery (see 3.1.10)
CIC	compliance interconnect channel (see SATA)
CID	consecutive identical digits (see 3.1.15)
CJTPAT	compliant jitter tolerance pattern (see 3.1.13)
CR	inter-enclosure (i.e., cabinet) receiver device compliance point (see 5.3)
CT	inter-enclosure (i.e., cabinet) transmitter device compliance point (see 5.3)
D.C.	direct current (see 3.1.25)
DCD	duty cycle distortion (see 3.1.28)
DDJ	data dependent jitter (see 3.1.19)
DFE	decision feedback equalizer (see 3.1.23)
DJ	deterministic jitter (see 3.1.24)
EMI	electromagnetic interference (see 3.1.30)
ER	end to end transmitter device compliance point (see 5.3)
ESD	electrostatic discharge
ET	end to end receiver device compliance point (see 5.3)
G1	generation 1 physical link rate (i.e., 1.5 Gbit/s)
G2	generation 2 physical link rate (i.e., 3 Gbit/s)
G3	generation 3 physical link rate (i.e., 6 Gbit/s)
G4	generation 4 physical link rate (i.e., 12 Gbit/s)
Gbit/s	gigabit per second (i.e., 10^9 bits per second)
Gen1i	SATA generation 1 physical link rate (i.e., 1.5 Gbit/s) (see SATA)
Gen2i	SATA generation 2 physical link rate (i.e., 3 Gbit/s) (see SATA)
Gen3i	SATA generation 3 physical link rate (i.e., 6 Gbit/s) (see SATA)
GPIO	general purpose input/output
HD	high-density
IR	intra-enclosure (i.e., internal) receiver device compliance point (see 5.3)
ISI	intersymbol interference (see 3.1.48)
IT	intra-enclosure (i.e., internal) transmitter device compliance point (see 5.3)
JMD	jitter measurement device
JTF	jitter transfer function (see 5.8.3.2)
JTPAT	jitter tolerance pattern (see 3.1.52)
LED	light-emitting diode
LMS	least mean square (see 3.1.53)
MJSQ	Methodologies for Jitter and Signal Quality Specification (see clause 2)
N/A	not applicable

Abbreviation	Meaning
NEXT	near-end crosstalk (see 3.1.55)
OOB	out-of-band
OOBI	out-of-band interval (see 3.1.59)
PCB	printed circuit board
PICS	physical interconnect TxRx connection segment (see 3.1.66)
PJ	periodic jitter
PLL	phase lock loop
P-P	peak to peak
RCCS	receiver circuit TxRx connection segment (see 3.1.76)
RD	running disparity (see SPL-3)
RDCS	receiver device TxRx connection segment (see 3.1.79)
RJ	random jitter (see 3.1.73)
RR	receiver device die attachment point to RCCS
Rx	receiver device (see 3.1.78)
RTTL	reference transmitter test load (see 3.1.85)
SAM-5	SCSI Architecture Model - 5 standard (see clause 2)
SAS	Serial Attached SCSI (see 3.1.96)
SAS-1.1	Serial Attached SCSI 1.1 (see clause 2)
SAS-2	Serial Attached SCSI 2 (see clause 2)
SAS-2.1	Serial Attached SCSI 2.1 (see clause 2)
SATA	Serial ATA (see 3.1.95) or the Serial ATA 3.1 specification (see clause 2)
SCSI	Small Computer System Interface
SGPIO	serial GPIO (see clause 2)
SJ	sinusoidal jitter (see 3.1.103)
SMA	subminiature version A connector (see Bibliography)
SPC-4	SCSI Primary Commands - 4 standard (see Bibliography)
SPL-3	SAS Protocol Layer - 3 (see clause 2)
SSC	spread spectrum clocking
STP	Serial ATA Tunneled Protocol
TCCS	transmitter circuit TxRx connection segment (see 3.1.110)
TCTF	transmitter compliance transfer function (see 3.1.111)
TDCS	transmitter device TxRx connection segment (see 3.1.113)
TDNA	time domain network analyzer (i.e., TDR/TDT plus analysis software that performs a VNA-style output)
TDR	time domain reflectometer
TDT	time domain transmission
TJ	total jitter (see 3.1.106)
TTIU	transmitter training information unit (see SPL-3)
Tx	transmitter device (see 3.1.112)
UI	unit interval (see 3.1.116)
VMA	voltage modulation amplitude (see 3.1.121)
VNA	vector network analyzer

Abbreviation	Meaning
WDP	waveform dispersion penalty (see 3.1.122)
XCS	crosstalk connection segment (see 5.5.6)

3.2.2 Symbols

3.2.2.1 Units

Units used in this document:

Units	Meaning
dB	decibel (see 3.1.20)
dBm	decibel milliwatts (see 3.1.22)
dBmV	decibel millivolts (see 3.1.21)
GHz	gigahertz (i.e., 10^9 cycles per second)(i.e., s^{-9})
Hz	hertz (i.e., cycles per second)(i.e., s^{-1})
kHz	kilohertz (i.e., 10^3 cycles per second)(i.e., s^{-3})
kΩ	kiloohm (i.e., 10^3 ohms)
µA	microampere (i.e., 10^{-6} amperes)
µs	microsecond (i.e., 10^{-6} seconds)
m	meter
mA	milliampere (i.e., 10^{-3} amperes)
MBps	megabytes per second (i.e., 10^6 bytes per second)
MHz	megahertz (i.e., 10^6 cycles per second)(i.e., s^{-6})
ms	millisecond (i.e., 10^{-3} seconds)
mV	millivolt (i.e., 10^{-3} volts)
mW	milliwatt (i.e., 10^{-3} watts)
nF	nanofarad (i.e., 10^{-9} farads)
ns	nanosecond (i.e., 10^{-9} seconds)
ppm	parts per million (i.e., 10^{-6})
ps	picosecond (i.e., 10^{-12} seconds)
rms	root mean square (i.e., quadratic mean)
s	second (i.e., unit of time)
V	volt
W	watt

3.2.2.2 Mathematical operators

Mathematical operators used in this document:

Mathematical Operators	Meaning
e	2.718 28..., the base of the natural (i.e., hyperbolic) system of logarithms
sgn	signum function (i.e., sign function)
^	exclusive logical OR
<	less than
≤	less than or equal to

Mathematical Operators	Meaning
>	greater than
≥	greater than or equal to
±	plus or minus
×	multiplication
/	division
|v|	the absolute value (i.e., magnitude) of v
~	approximately equal to
⊗	convolution

3.2.2.3 Other symbols

Other symbols used in this document:

Symbols	Meaning
Dxx.y	data character (see 3.1.19)
K_0	output gain
R_{post}	post cursor equalization ratio (see 3.1.71)
R_{pre}	precursor equalization ratio (see 3.1.72)
®	registered trademark
S_{ij}	S-parameter for port j to port i (see clause F.11)
S_{CCij}	S-parameter for common mode to common mode port j to port i (see clause F.11)
S_{CDij}	S-parameter for differential to common mode port j to port i (see clause F.11)
S_{DCij}	S-parameter for common mode to differential port j to port i (see clause F.11)
S_{DDij}	S-parameter for differential to differential port j to port i (see clause F.11)
Δ (delta)	difference operator
ϕ (phi)	phase
π (pi)	3.141 59... , the ratio of the circumference of a circle to its diameter
ρ (rho)	reflection coefficient (see 3.1.86)
τ (tau)	time constant
Ω (omega)	ohm (i.e., unit of electrical resistance)

3.3 Keywords

3.3.1
invalid
keyword used to describe an illegal or unsupported bit, byte, word, field or code value

Note 1 to entry: Receipt of an invalid bit, byte, word, field or code value shall be reported as an error.

3.3.2
mandatory
keyword indicating an item that is required to be implemented as defined in this document

3.3.3
may
keyword that indicates flexibility of choice with no implied preference

3.3.4
may not
keyword that indicates flexibility of choice with no implied preference

3.3.5
obsolete
keyword indicating that an item was defined in prior SCSI standards but has been removed from this document

3.3.6
option, optional
keywords that describe features that are not required to be implemented by this document

Note 1 to entry: If any optional feature defined by this document is implemented, then it shall be implemented as defined in this document.

3.3.7
prohibited
keyword used to describe a feature, function, or coded value that is defined in a a non-SCSI standard (i.e., a standard that is not a member of the SCSI family of standards) to which this document makes a normative reference where the use of said feature, function, or coded value is not allowed for implementations of this standard

3.3.8
reserved
keyword referring to bits, bytes, words, fields, and code values that are set aside for future standardization

Note 1 to entry: A reserved bit, byte, word, or field shall be set to zero, or in accordance with a future extension to this document.

Note 2 to entry: Recipients are not required to check reserved bits, bytes, words, or fields for zero values.

Note 3 to entry: Receipt of reserved code values in defined fields shall be reported as error.

3.3.9
restricted
keyword referring to bits, bytes, words, and fields that are set aside for other identified standardization purposes

Note 1 to entry: A restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears.

3.3.10
shall
keyword indicating a mandatory requirement

Note 1 to entry: Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this document.

3.3.11
should
keyword indicating flexibility of choice with a strongly preferred alternative

3.3.12
vendor specific
something (e.g., a bit, field, code value) that is not defined by this document

Note 1 to entry: Specification of the referenced item is determined by the SCSI device vendor and may be used differently in various implementations.

3.4 Editorial conventions

Certain words and terms used in this document have a specific meaning beyond the normal English meaning. These words and terms are defined either in the glossary or in the text where they first appear.

Uppercase is used when referring to the name of a numeric value defined in this document or a formal attribute possessed by an entity. When necessary for clarity, names of objects, procedure calls, arguments or discrete states are capitalized or set in bold type. Names of fields are identified using small capital letters (e.g., NACA bit).

Quantities having a defined numeric value are identified by large capital letters (e.g., CHECK CONDITION). Quantities having a discrete but unspecified value are identified using small capital letters. (e.g., TASK COMPLETE, indicates a quantity returned by the **Execute Command** procedure call). Such quantities are associated with an event or indication whose observable behavior or value is specific to a given implementation standard.

Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a) red (i.e., one of the following colors):
   A) crimson; or
   B) amber;
b) blue; or
c) green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 - The following list shows an ordered relationship between the named items:

1) top;
2) middle; and
3) bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a) or 1) entry).

If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

Notes and examples do not constitute any requirements for implementors and notes are numbered consecutively throughout this document.

3.5 Numeric and character conventions

3.5.1 Numeric conventions

A binary number is represented in this document by any sequence of digits comprised of only the Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Underscores or spaces may be included in binary number representations to increase readability or delineate field boundaries (e.g., 00010101 11001110b, 00010101_11001110b, 0 0101 1010b, or 0_0101_1010b).

A hexadecimal number is represented in this document by any sequence of digits comprised of only the Arabic numerals 0 to 9 and/or the upper-case English letters A to F immediately followed by a lower-case h (e.g., FA23h). Underscores or spaces may be included in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h or B_FD8C_FA23h).

A decimal number is represented in this document by any sequence of digits comprised of only the Arabic numerals 0 to 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

A range of numeric values is represented in this document in the form “a to z”, where a is the first value included in the range, all values between a and z are included in the range, and z is the last value included in the range (e.g., the representation “0h to 3h” includes the values 0h, 1h, 2h, and 3h).

Variables (i.e., alphanumeric names that represent values in computations and other statements) are represented in the same San-serif font as other information is this document.

This document uses the following conventions for representing decimal numbers:

a) the decimal separator (i.e., separating the integer and fractional portions of the number) is a period;
b) the thousands separator (i.e., separating groups of three digits in a portion of the number) is a space;
c) the thousands separator is used in both the integer portion and the fraction portion of a number; and
d) the decimal representation for a year is 1999 not 1,999.

Table 1 shows some examples of decimal numbers using various conventions.

Table 1 – Numbering conventions

ISO/IEC	United States	This document
0,6	0.6	0.6
3,141 592 65	3.14159265	3.141 592 65
1 000	1,000	1 000
1 323 462,95	1,323,462.95	1 323 462.95

3.5.2 Units of measure

This document represents values using both decimal units of measure and binary units of measure. Values are represented by the following formats:

a) for values based on decimal units of measure:
   1) numerical value (e.g., 100);
   2) space;
   3) prefix symbol and unit:
      1) decimal prefix symbol (e.g., M) (see table 2); and
      2) unit abbreviation;

   and

b) for values based on binary units of measure:
   1) numerical value (e.g., 1 024);
   2) space;
   3) prefix symbol and unit:
      1) binary prefix symbol (e.g., Gi) (see table 2); and
      2) unit abbreviation.

Table 2 compares the prefix, symbols, and power of the binary and decimal units.

Table 2 – Comparison of decimal prefixes and binary prefixes

Decimal			Binary		
Prefix name	**Prefix symbol**	**Power (base-10)**	**Prefix name**	**Prefix symbol**	**Power (base-2)**
kilo	k	10^3	kibi	Ki	2^{10}
mega	M	10^6	mebi	Mi	2^{20}
giga	G	10^9	gibi	Gi	2^{30}
tera	T	10^{12}	tebi	Ti	2^{40}
peta	P	10^{15}	pebi	Pi	2^{50}
exa	E	10^{18}	exbi	Ei	2^{60}
zetta	Z	10^{21}	zebi	Zi	2^{70}
yotta	Y	10^{24}	yobi	Yi	2^{80}

3.5.3 Byte encoded character strings conventions

When this document requires one or more bytes to contain specific encoded characters, the specific characters are enclosed in single quotation marks. The single quotation marks identify the start and end of the characters that are required to be encoded but are not themselves to be encoded. The characters that are to be encoded are shown in the case that is to be encoded.

An ASCII space character (i.e., 20h) may be represented in a string by the character '¬' (e.g., 'SCSI¬device').

The encoded characters and the single quotation marks that enclose them are preceded by text that specifies the character encoding methodology and the number of characters required to be encoded.

EXAMPLE - Using the notation described in this subclause, stating that eleven ASCII characters 'SCSI device' are to be encoded would be the same writing out the following sequence of byte values: 53h 43h 53h 49h 20h 64h 65h 76h 69h 63h 65h.

4 General

4.1 Physical links and phys

A physical link is a set of four wires used as two differential signal pairs. One differential signal transmits in one direction while the other differential signal transmits in the opposite direction. Data may be transmitted in both directions simultaneously.

A physical phy contains a transceiver which electrically interfaces to a physical link, which attaches to another physical phy.

Phys are contained in ports (see SPL-3). Phys interface to a service delivery subsystem (see SAM-5).

Figure 3 shows two phys attached with a physical link.

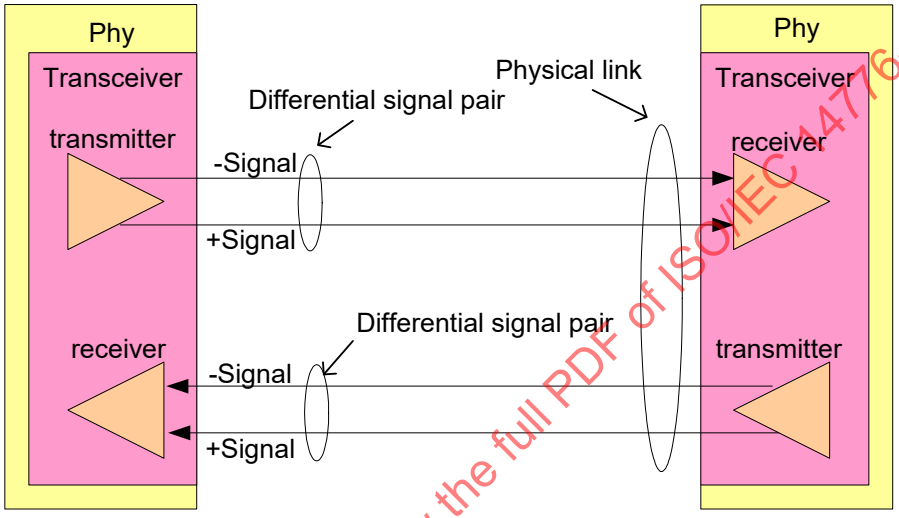


Figure 3 – Physical links and phys

An attached phy is the phy to which a phy is attached over a physical link.

The transceiver follows the electrical specifications defined in 5.8. Phys transmit and receive bits at physical link rates defined in 5.8. The bits are parts of 10-bit characters (see SPL-3), which are parts of dwords (see SPL-3). The physical link rates supported by a phy are specified or indicated by the following fields in the SMP DISCOVER response (see SPL-3), the SMP PHY CONTROL request (see SPL-3), and the Phy Control and Discover mode page (see SPL-3):

a) the NEGOTIATED PHYSICAL LINK RATE field;
b) the HARDWARE MINIMUM PHYSICAL LINK RATE field;
c) the HARDWARE MAXIMUM PHYSICAL LINK RATE field;
d) the PROGRAMMED MINIMUM PHYSICAL LINK RATE field; and
e) the PROGRAMMED MAXIMUM PHYSICAL LINK RATE field.

4.2 Phy test functions

Phy test functions (e.g., transmission of test patterns) are used for phy and interconnect characterization and diagnosis. The phy may be attached to test equipment while performing a phy test function. See SPL-3 for the optional mechanisms for invoking phy test function.

Each phy test function is optional.

If the phy test function requires a specific phy test pattern and/or phy test function physical link rate, then the mechanism for invoking the phy test function (see SPL-3) also specifies the phy test pattern and phy test function physical link rate.

5 Physical layer

5.1 Physical layer overview

The physical layer defines:

a) passive interconnect (e.g., connectors and cable assemblies); and
b) transmitter and receiver device electrical characteristics.

Within this document, references to connector gender use the terms plug and receptacle as equivalent to the terms free and fixed, respectively, that may be used in the references that define the connectors. Fixed and free terminology has no relationship to the application of the connector.

5.2 Conventions for defining maximum limits for S-parameters

The following values are specified by this document to define the maximum limits for certain S-parameters (e.g., for cable assemblies and backplanes (see 5.5.3), transmitter devices (see 5.8.4.6.3), and receiver devices (see 5.8.5.7.2)):

a) L is the maximum value in dB at the low frequency asymptote;
b) N is the maximum value in dB at 3 GHz;
c) H is the maximum value in dB at the high frequency asymptote;
d) S is the slope in dB/decade;
e) f_{min} is the minimum frequency of interest; and
f) f_{max} is the maximum frequency of interest.

The frequencies at which L and H intersect the slope S may or may not be within the region of f_{min} to f_{max}. The frequency for N is based on the Nyquist at 6 Gbit/s.

Figure 4 shows the values in a graph.

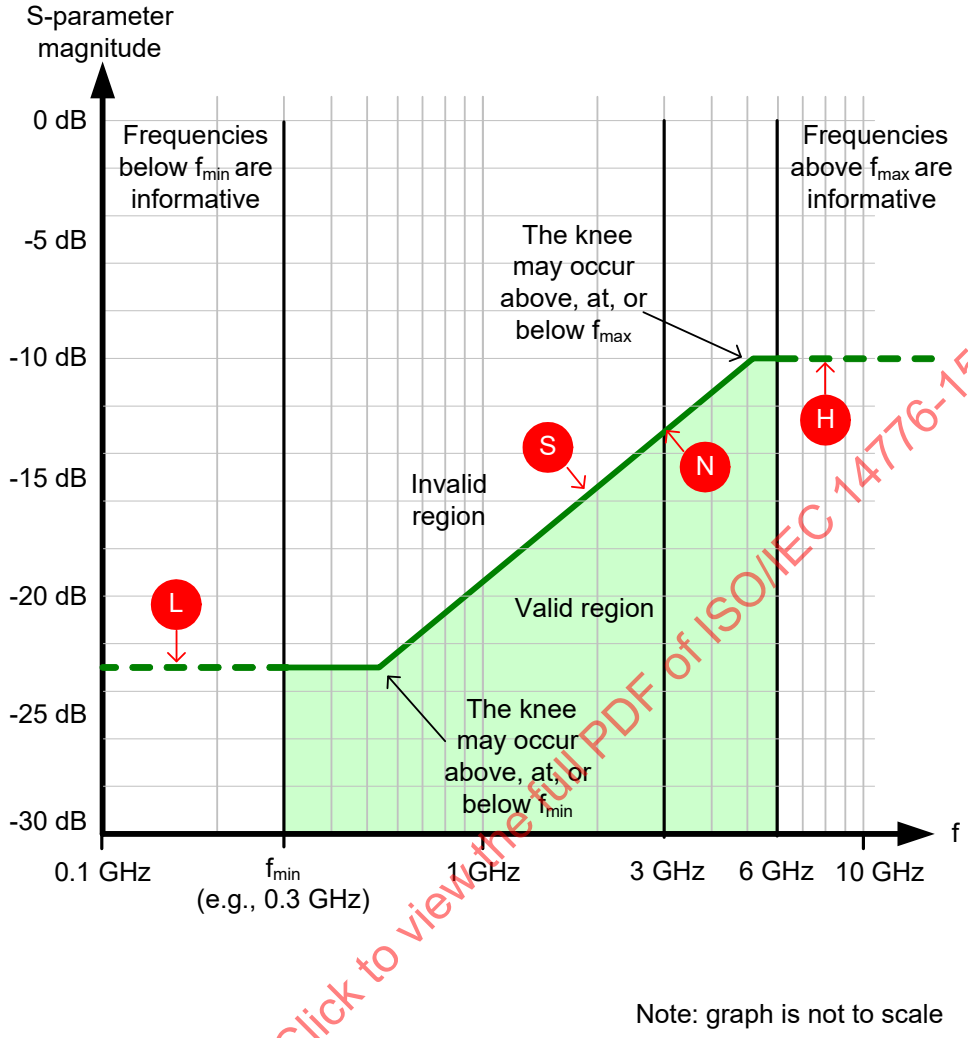


Figure 4 – Maximum limits for S-parameters definitions

5.3 Compliance points

5.3.1 Compliance points overview

A TxRx connection is the complete simplex signal path between the transmitter circuit and receiver circuit.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in conductive material.

This document defines the electrical requirements of the signal at the following compliance points in a TxRx connection (see table 3):

a) for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT, IR, CT, and CR; and
b) for 12 Gbit/s IT, IR, CT, CR, ET, and ER.

Each compliant phy shall be compatible with these electrical requirements to allow interoperability within a SAS environment.

The TxRx connection characteristics are defined in 5.5.

Signal behavior at separable connectors requires compliance with signal characteristics defined by this document only if the connectors are identified as compliance points by the supplier of the parts that contain the candidate compliance point.

Signal characteristics for compliance points are measured at physical positions called probe points in a test load (see 5.6). Measurements at the probe points in a test load approximate measurements at the compliance point in the actual TxRx connection. Some components in the test load may be de-embedded as described in F.5.

Table 3 – Compliance points

Compliance point	Type	Description
1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s compliance points		
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device, as measured at probe points in a test load attached with an internal connector.
IT_S	intra-enclosure (i.e., internal)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector.
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device, as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector.
CT_S	inter-enclosure (i.e., cabinet)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector.
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.
12 Gbit/s only compliance points		
ET	transmitter circuit	The output signal from a transmitter circuit measured with the test load, TDCS, and TCCS de-embedded.
ER	receiver post equalization	A point defined at the output of the reference receiver device.

5.3.2 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s compliance points

The 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s TxRx connection includes the characteristics of the mated connectors at both the transmitter device and receiver device ends. One end of a TxRx connection is a IT_S compliance point or CT_S compliance point, and the other end of the TxRx connection is the corresponding IR compliance point or CR compliance point.

Figure 5 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s CT compliance points and CR compliance points using an external cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

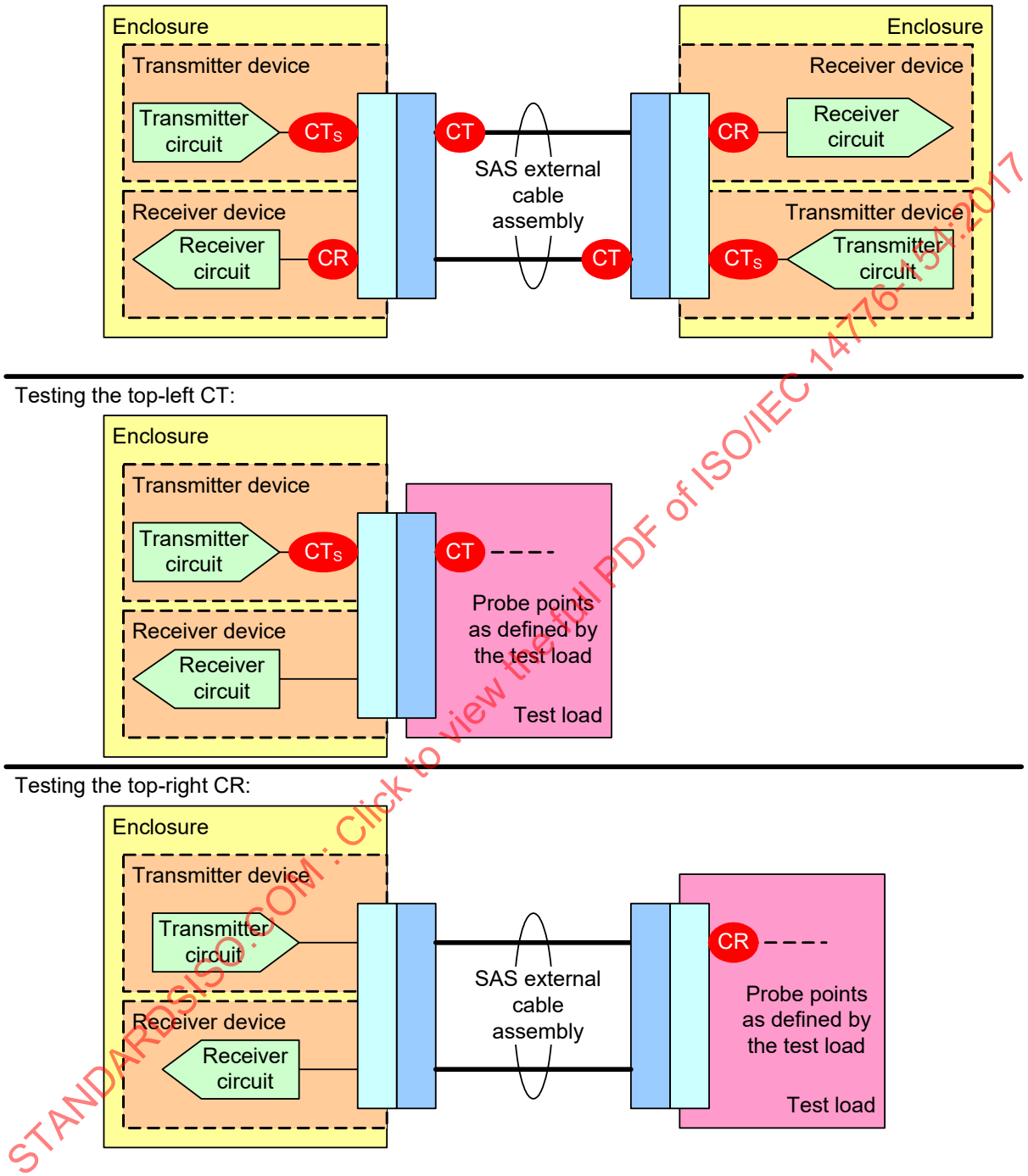


Figure 5 – 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s External cable assembly CT compliance points and CR compliance points

Figure 6 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a backplane with a SAS Drive backplane receptacle (see 5.4.3.4.1.3) that is not using SATA and shows how the compliance points are tested using test loads (see 5.6).

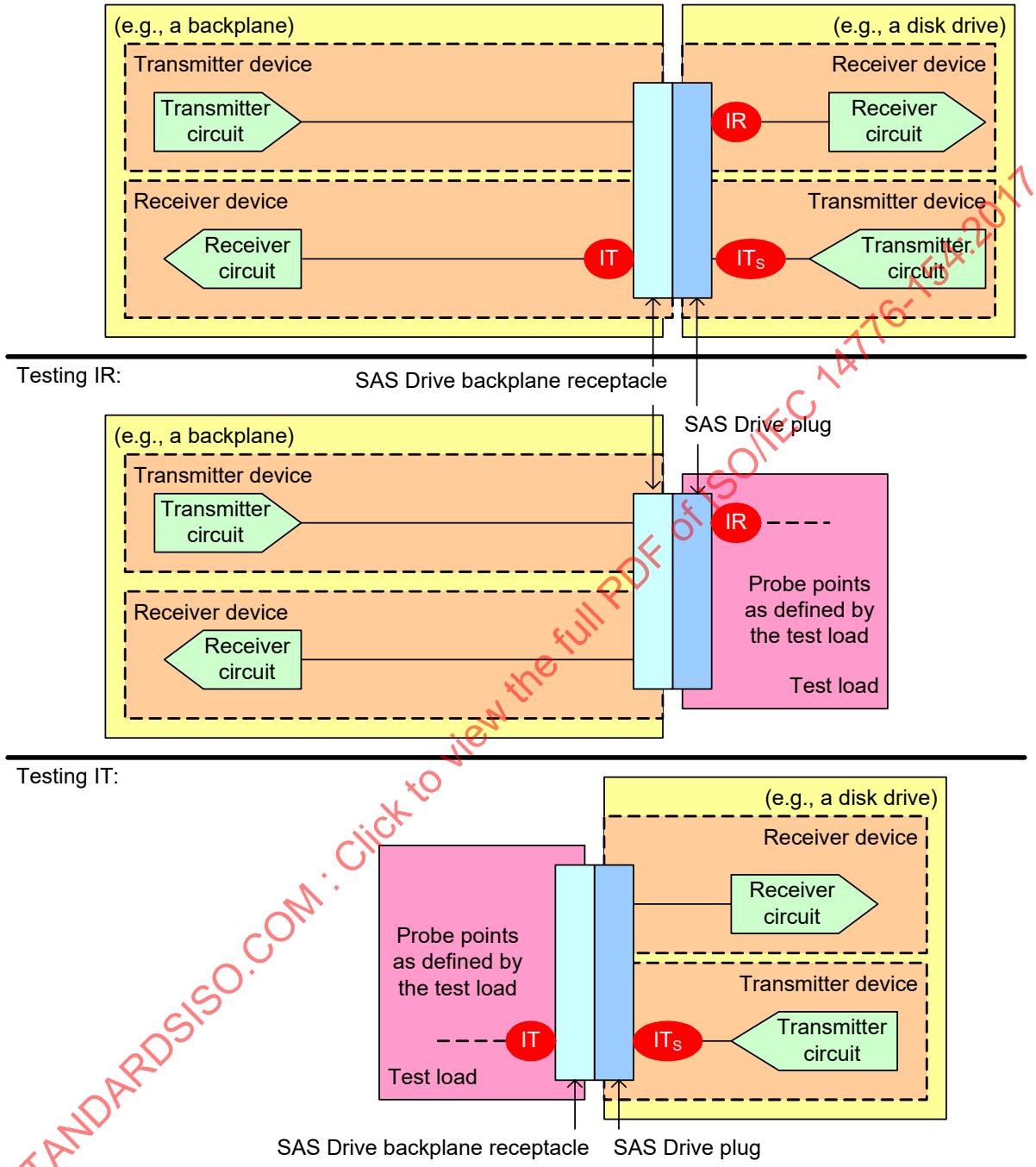


Figure 6 – Backplane with SAS Drive connector 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

If the backplane supports SATA, then there are no 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points or IR compliance points. SATA defines the signal characteristics that the SATA phy delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 7.

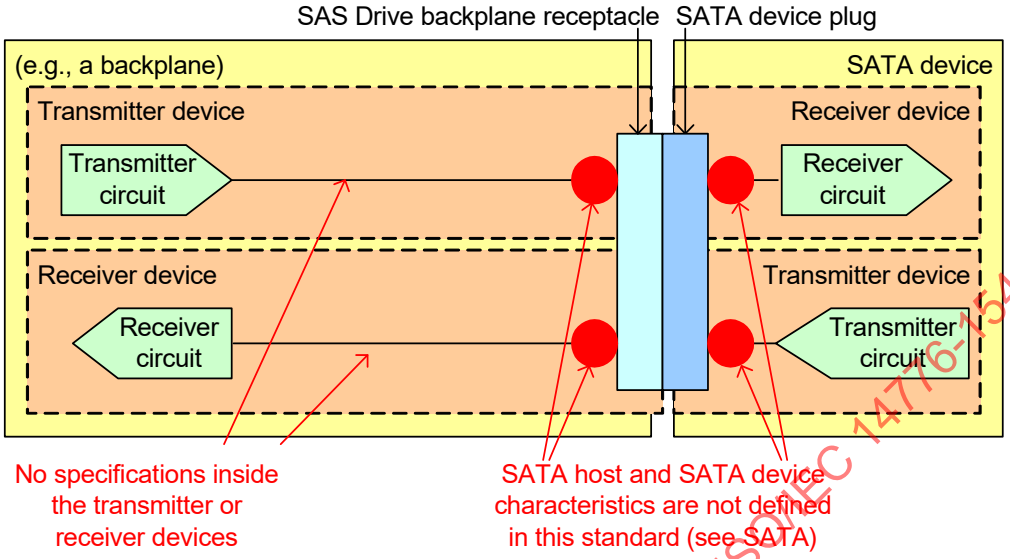


Figure 7 – Backplane with SAS Drive connector 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s compliance points with SATA phy attached

Figure 8 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS multilane internal cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

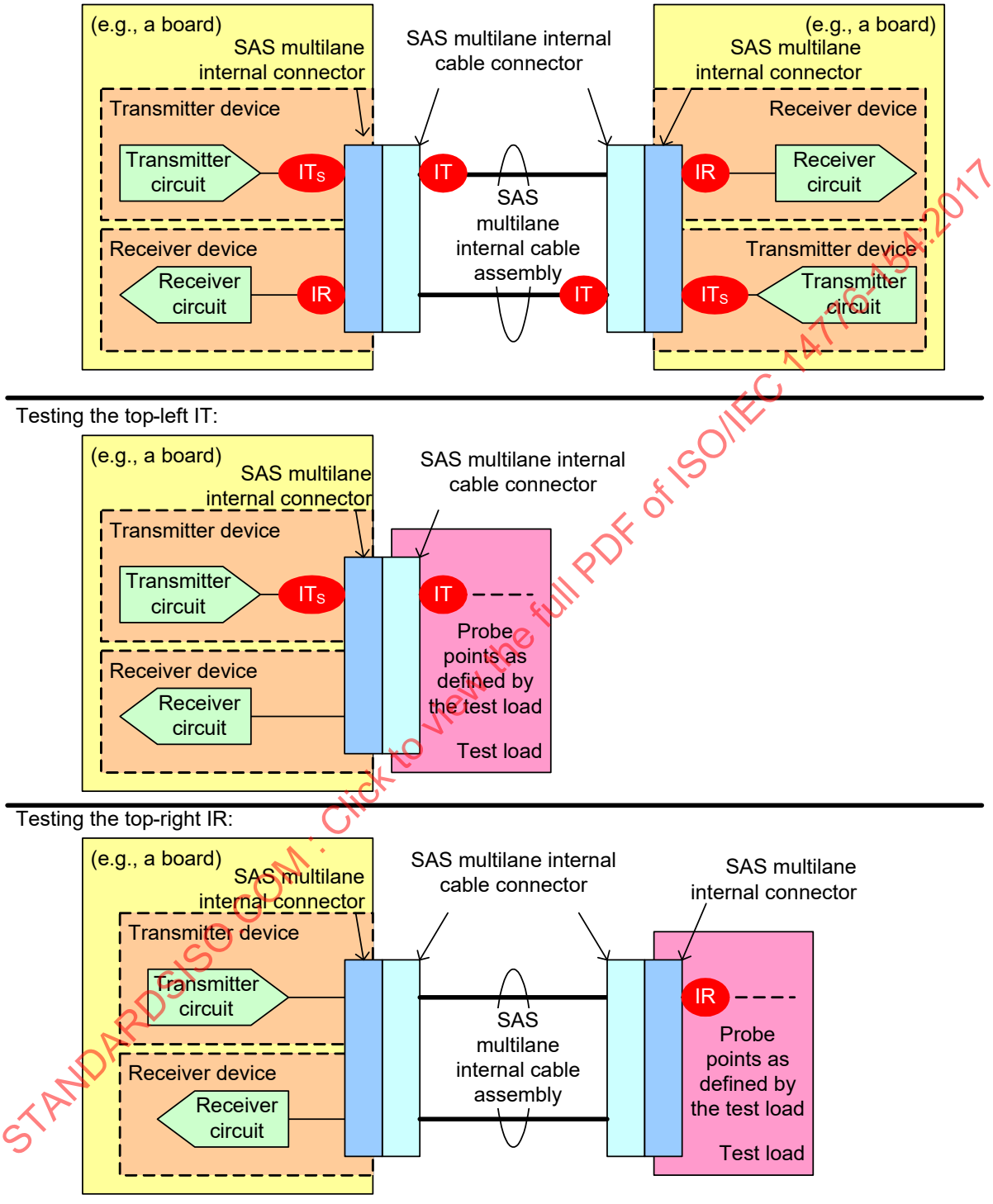


Figure 8 – SAS multilane internal cable assembly 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

Figure 9 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.4.1.3), where the backplane is not attached to a SATA device, and shows how two of the compliance points are tested using test loads (see 5.6).

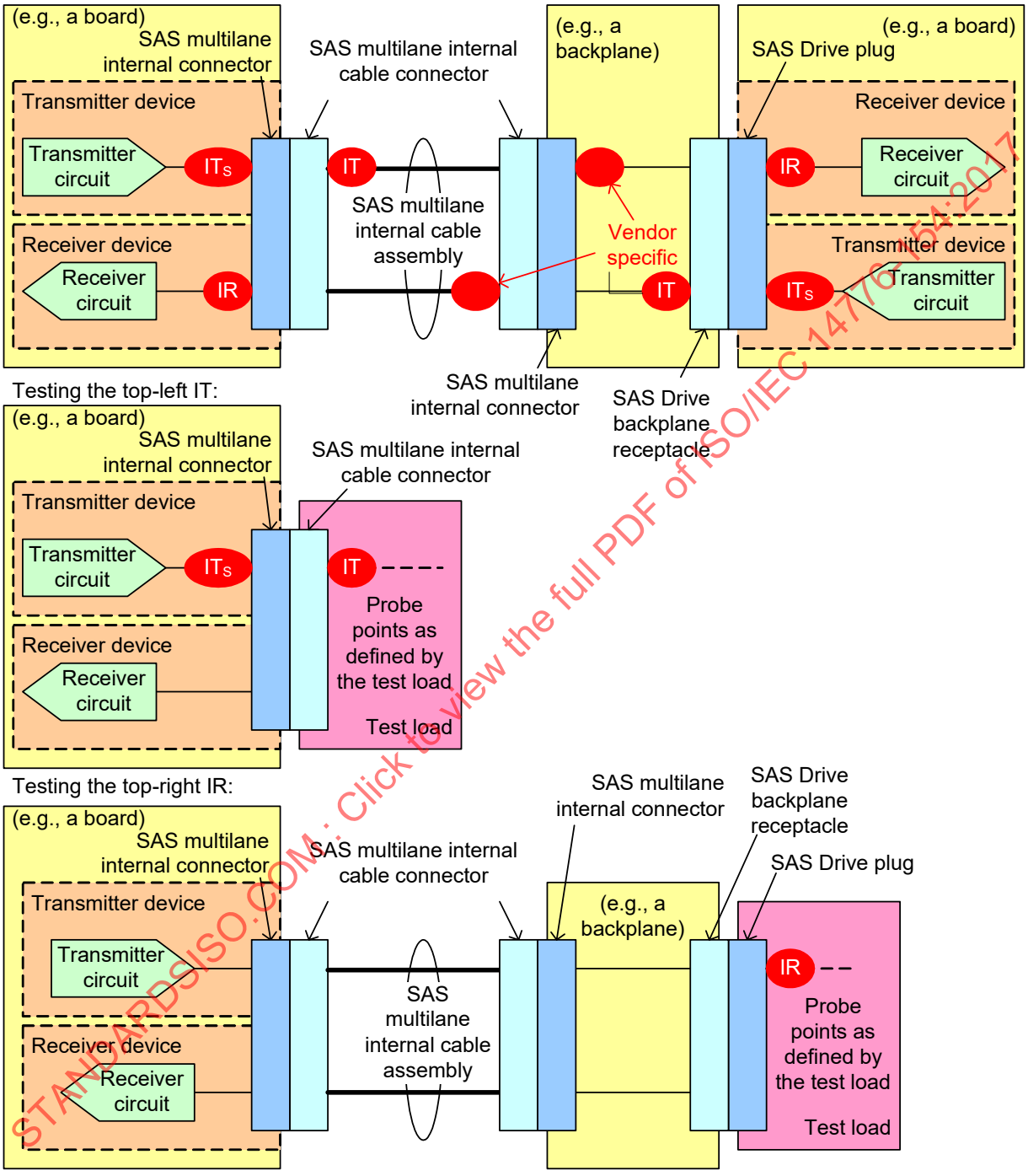


Figure 9 – SAS multilane internal cable assembly and backplane 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

Figure 10 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.4.1.3) that supports being attached to a SATA device. There are no IT compliance points and IR compliance points at the SAS Drive backplane receptacle connector when a SATA device is attached. In that case, SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device. There are compliance points at the SAS multilane internal connector.

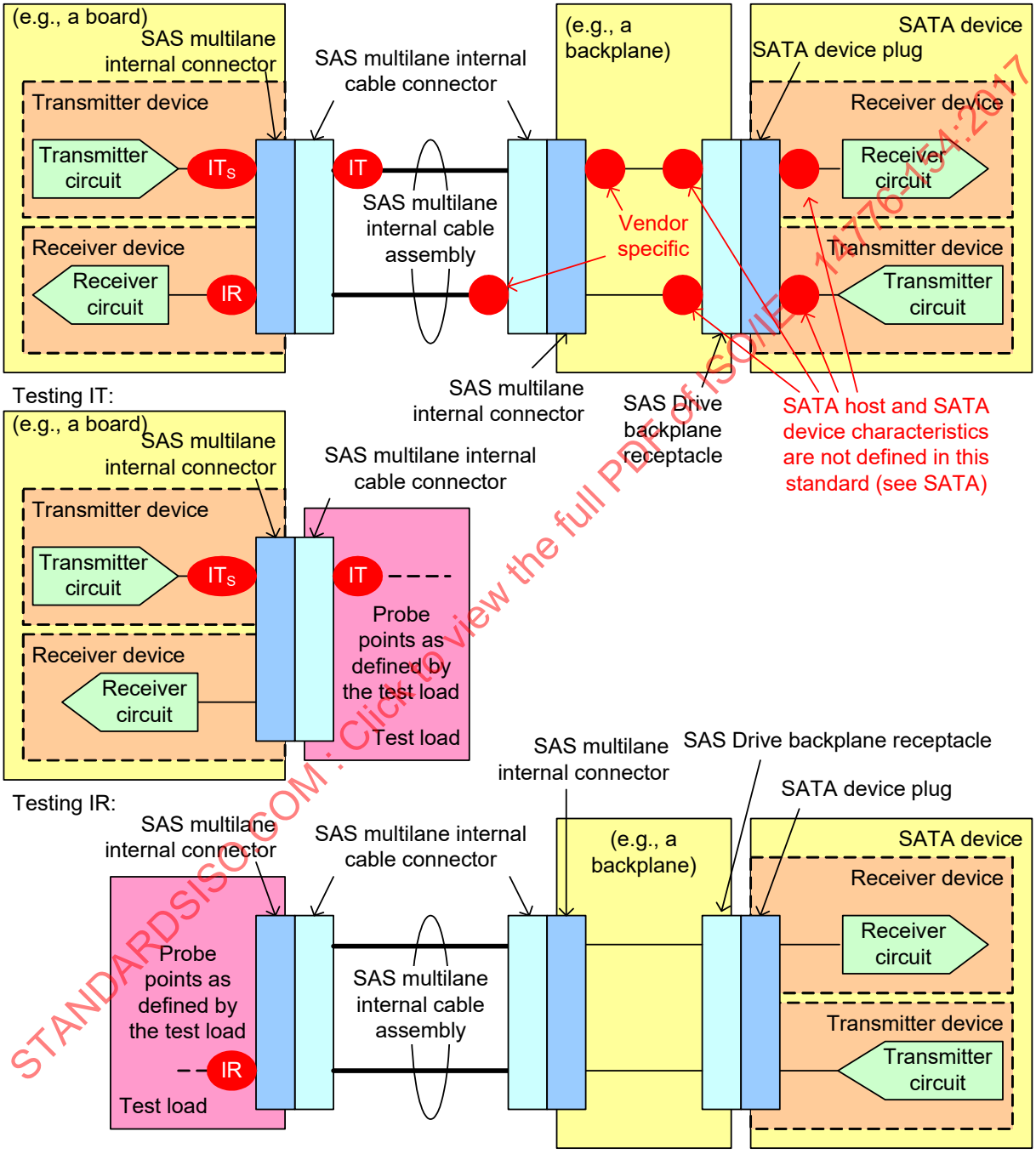


Figure 10 – SAS multilane internal cable assembly and backplane 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points with SATA device attached

Figure 11 shows the locations of the 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points using a SAS Drive cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

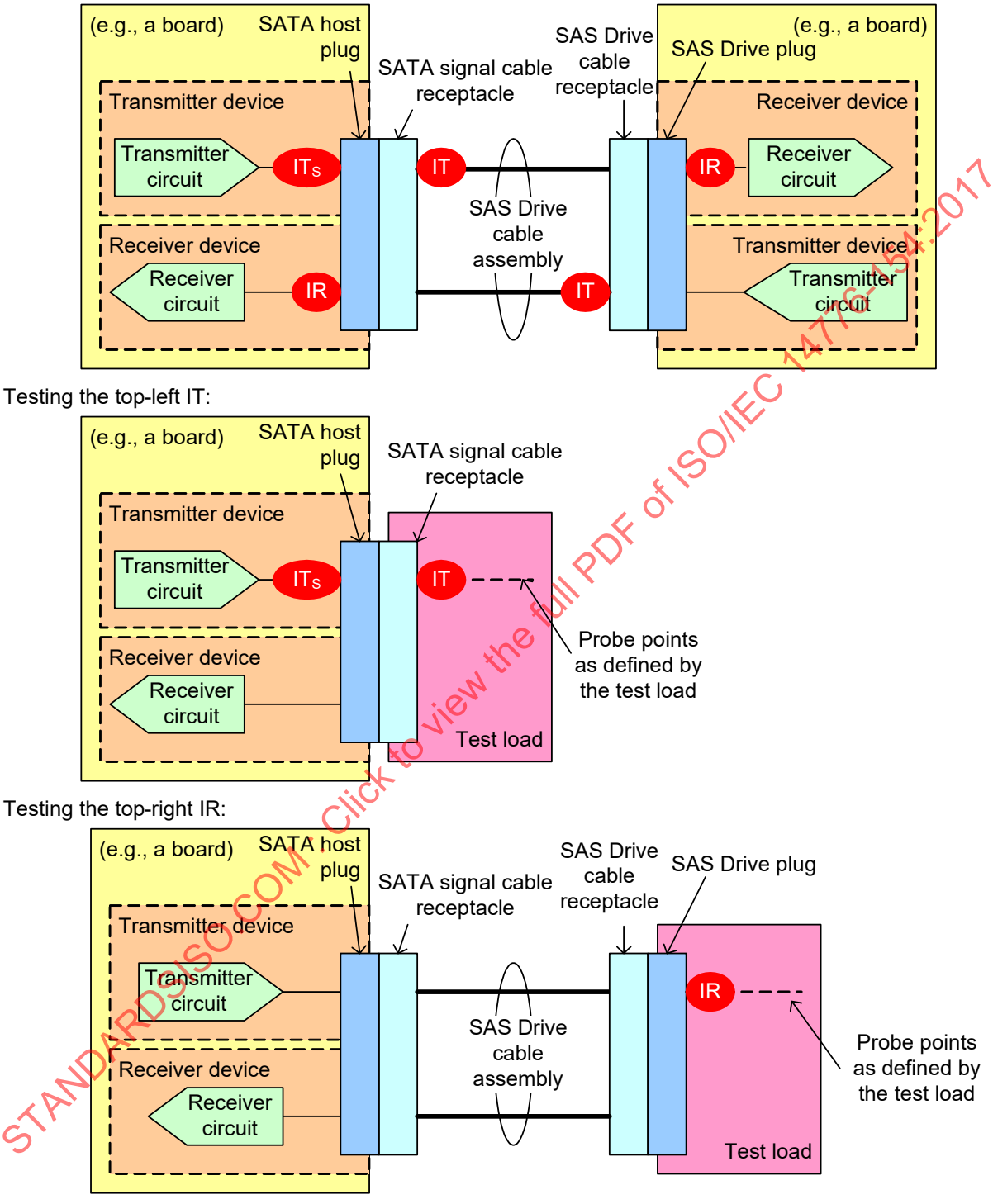


Figure 11 – SAS Drive cable assembly 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s IT compliance points and IR compliance points

5.3.3 12 Gbit/s compliance points

Figure 12 shows an example TxRx connection for trained 12 Gbit/s where PICS is the physical interconnect connection segment.

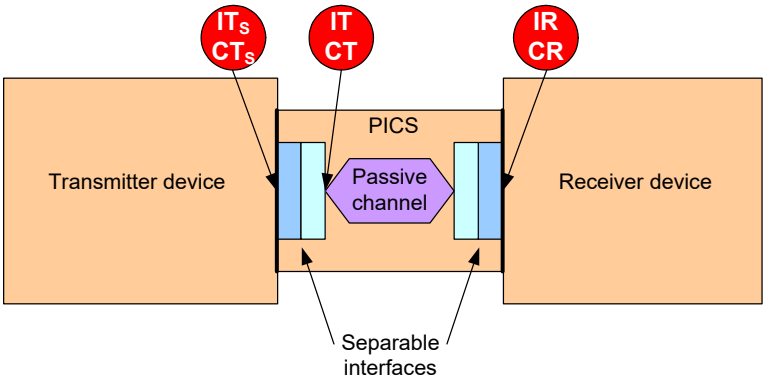


Figure 12 – 12 Gbit/s TxRx connection and compliance points

Figure 13 shows an example of a simulated TxRx connection for trained 12 Gbit/s where:

a) TDCS is the transmitter device TxRx connection segment;
b) TCCS is the transmitter circuit TxRx connection segment;
c) RDCS is the receiver device TxRx connection segment;
d) RCCS is the receiver circuit TxRx connection segment; and
e) PICS is the physical interconnect connection segment.

If simulations use a captured signal, then the TxRx connection segments located between ET and the compliance point used to capture the signal should be modeled as a single TxRx connection segment. End to end simulations (see 5.7.1) compute characteristics of the signal at ET and ER, using measurements taken:

a) at:
   A) IT;
   B) CT;
   C) IR; or
   D) CR;
   or
b) between:
   A) CT_S and CR; or
   B) IT_S and IR.

If the reference TxRx connection segment models provided for end to end simulations (see clause D.2) represent TxRx connection segments that are adjacent in the TxRx connection segment, then the TxRx connection segment models may be combined to simulate a single TxRx connection segment model.

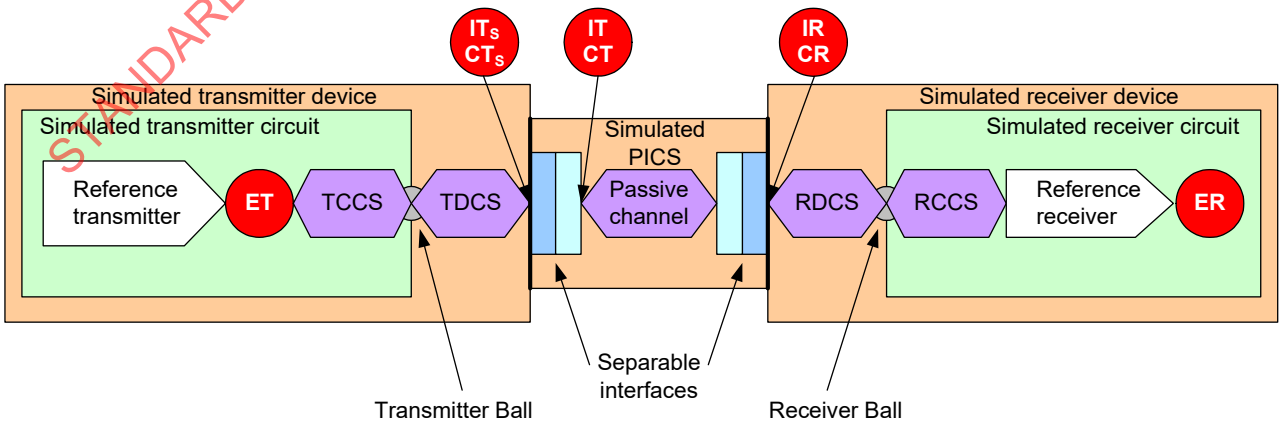


Figure 13 – Simulated 12 Gbit/s TxRx connection and compliance points

Figure 14 shows:

a) the locations of the CT_S compliance points and CR compliance points of an enclosure using an external cable connector; and
b) how the enclosure CT_S compliance point and the SAS active cable assembly for 12 Gbit/s CR compliance point are tested using test loads (see 5.6).

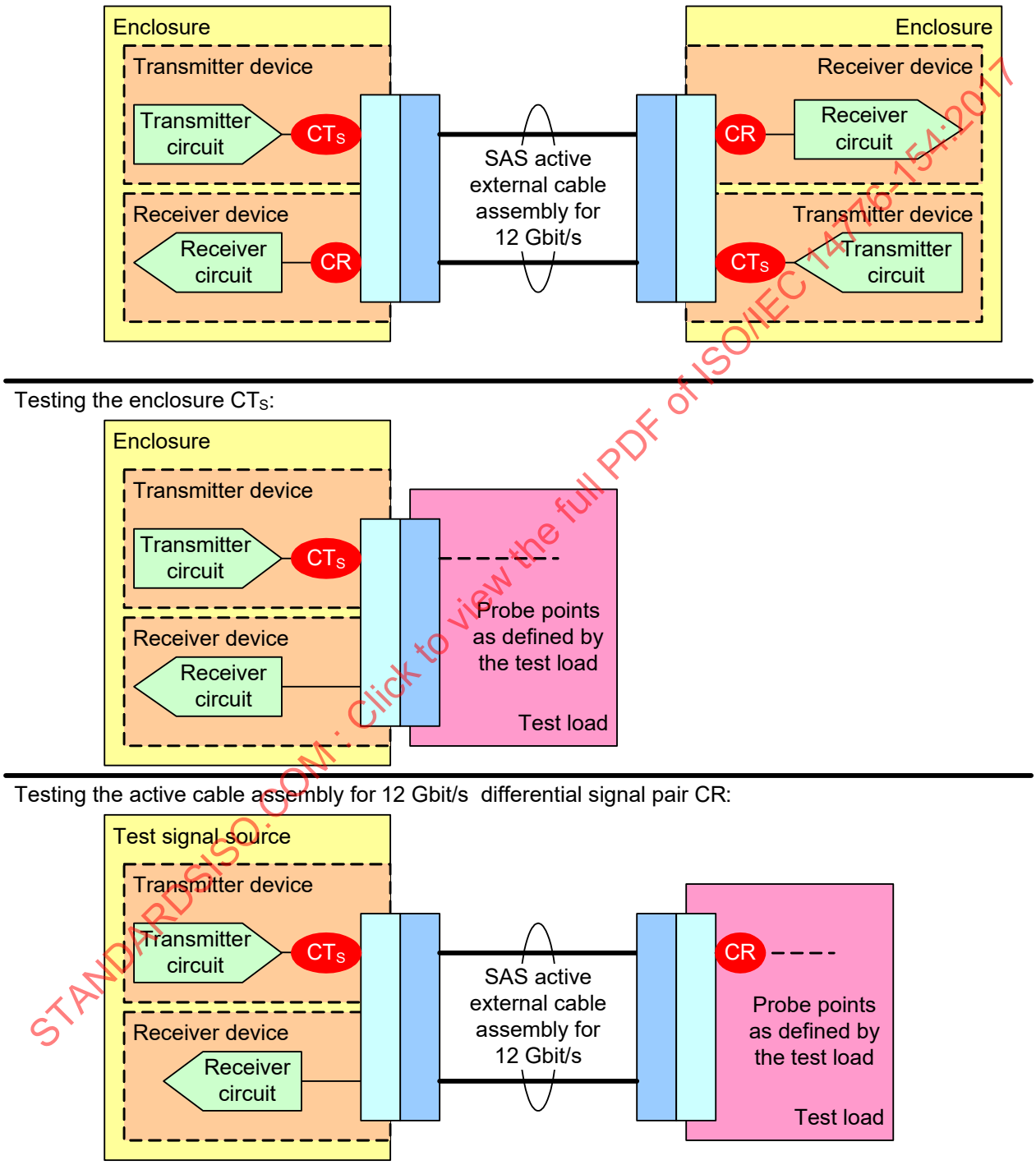


Figure 14 – 12 Gbit/s CT_S and CR compliance points

5.4 Interconnects

5.4.1 SATA connectors and cable assemblies

Figure 15 shows a representation of the connectors and cables defined by SATA. A SATA host is analogous to a SAS initiator device (see SPL-3) and a SATA device is analogous to a SAS target device (see SPL-3).

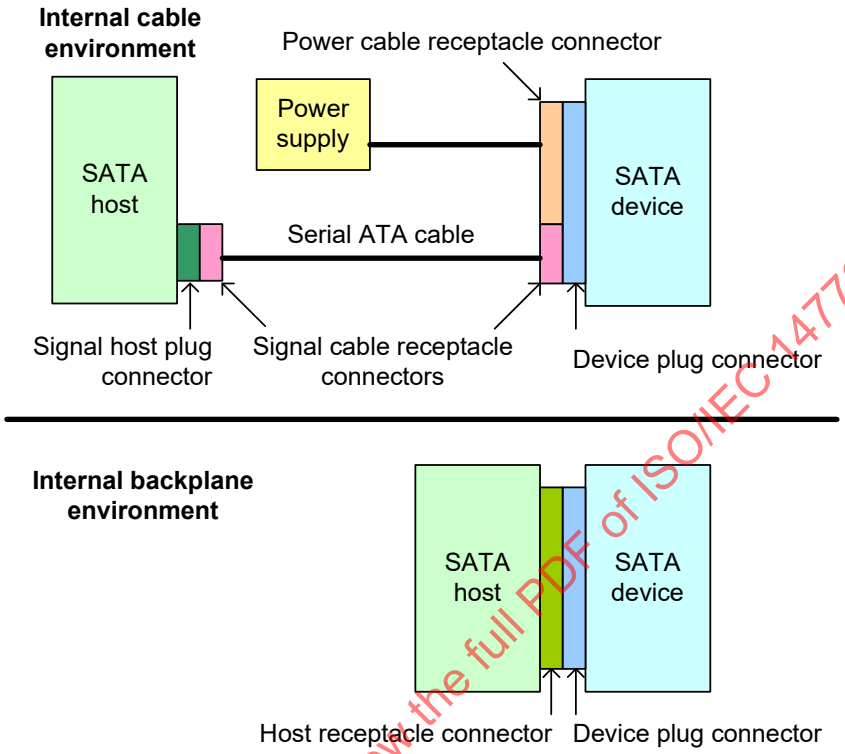


Figure 15 – SATA connectors and cables

5.4.2 SAS connectors and cables

This document defines SAS Drive cable, SAS Drive backplane, SAS internal cable, and SAS external cable environments.

Figure 16 shows a representation of the SAS Drive cable environments.

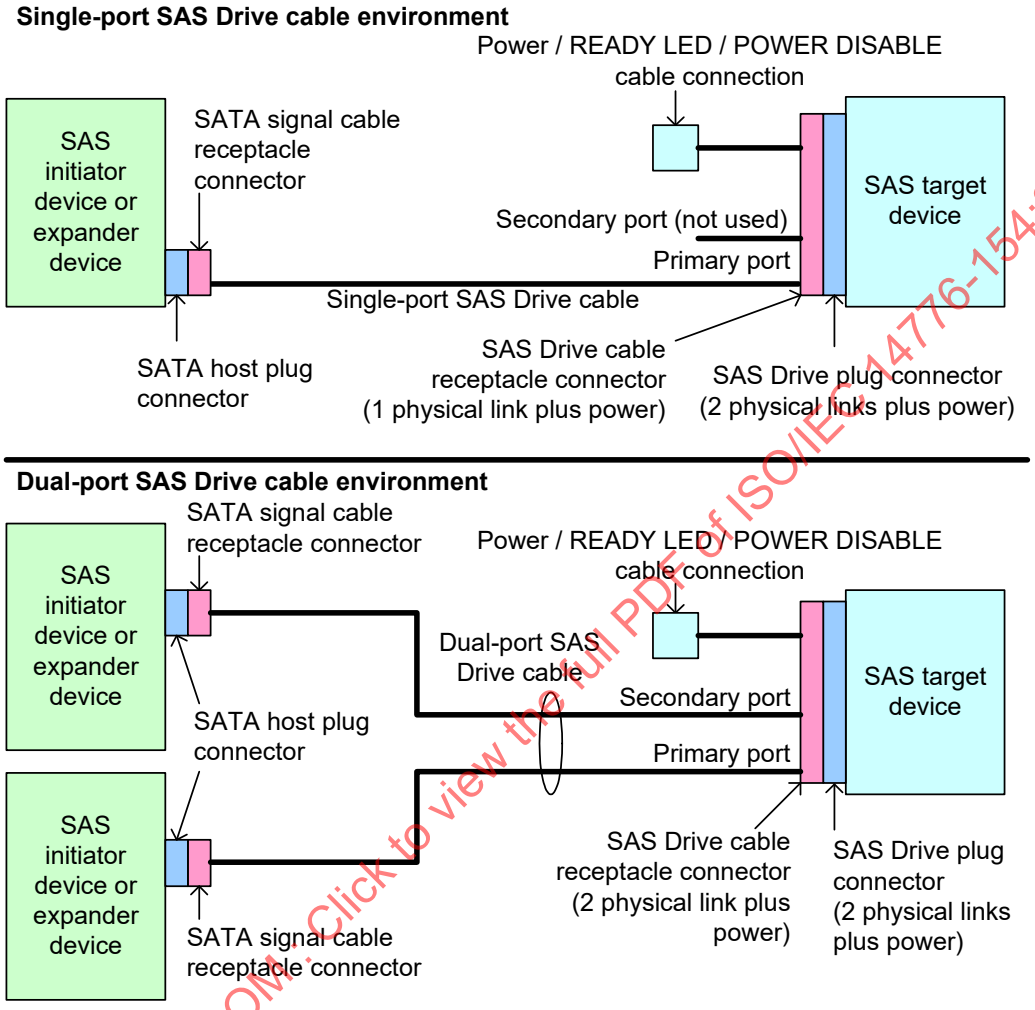


Figure 16 – SAS Drive cable environments

Figure 17 shows a representation of the SAS Drive backplane environment.

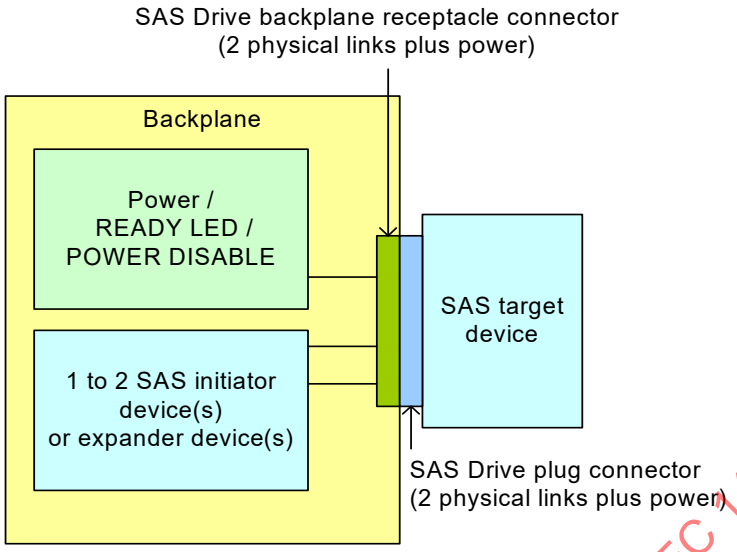


Figure 17 – SAS Drive backplane environment

Figure 18 shows a representation of the SAS external cable environment.

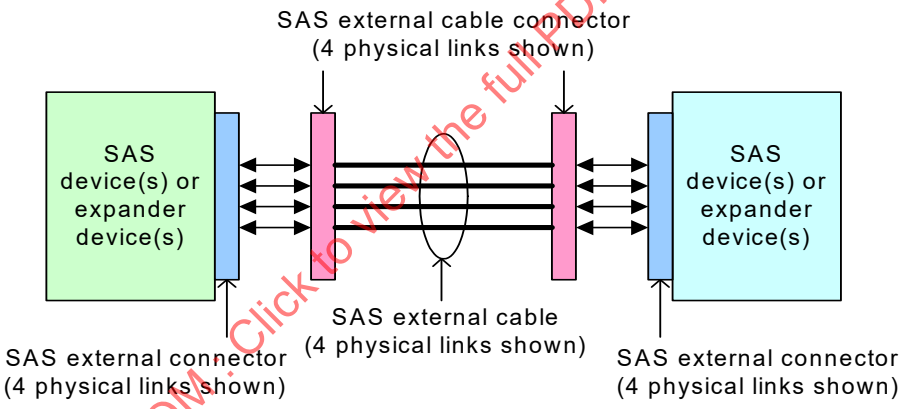


Figure 18 – SAS external cable environment

Figure 19 shows a representation of the SAS internal cable environment attaching a controller to a backplane using a SAS internal symmetric cable (see 5.4.4.1.2).

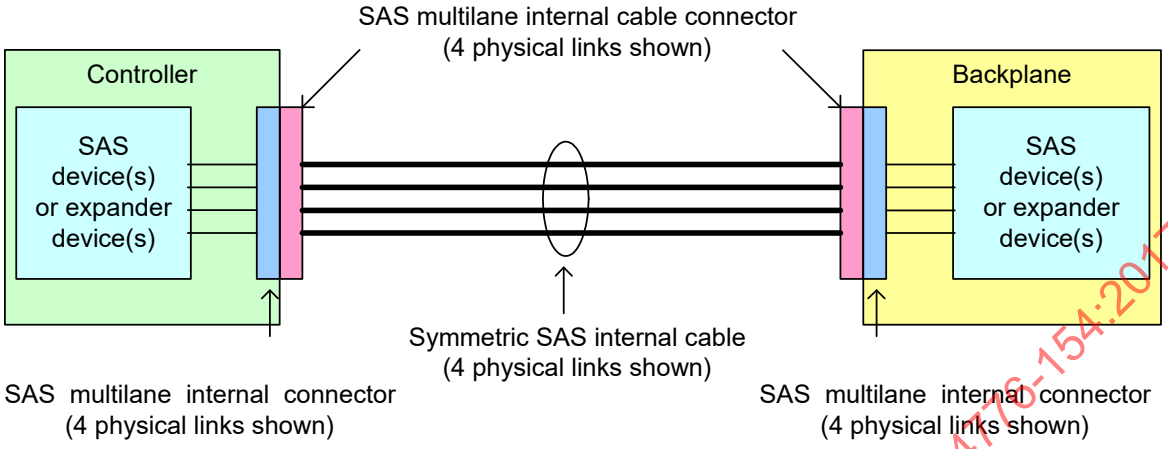


Figure 19 – SAS internal symmetric cable environment - controller to backplane

A SAS internal symmetric cable provides one to eight physical links, and may be used as any combination of wide links and narrow links (see SPL-3) using those physical links.

Figure 20 shows a representation of the SAS internal cable environment attaching a controller to a controller using a SAS internal symmetric cable (see 5.4.4.1.2).

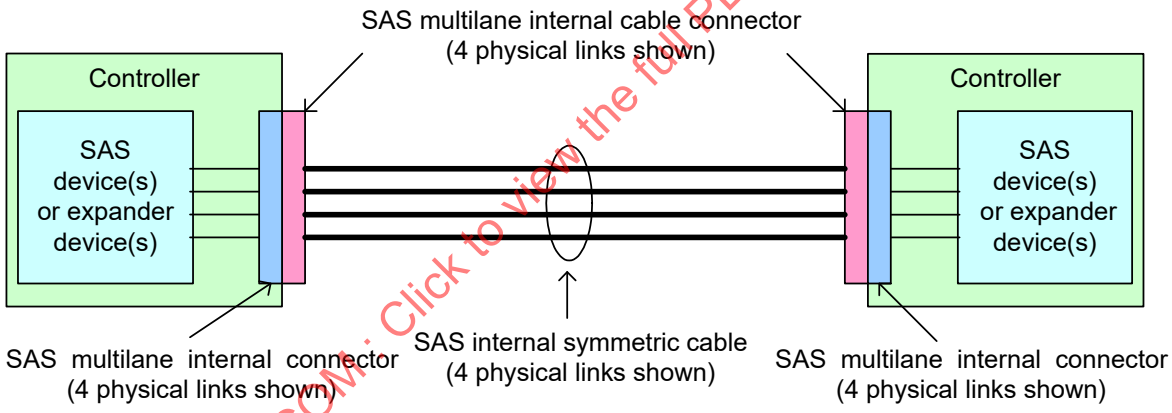


Figure 20 – SAS internal symmetric cable environment - controller to controller

Figure 21 shows a representation of the SAS internal cable environment using a SAS controller-based fanout cable (see 5.4.4.1.3).

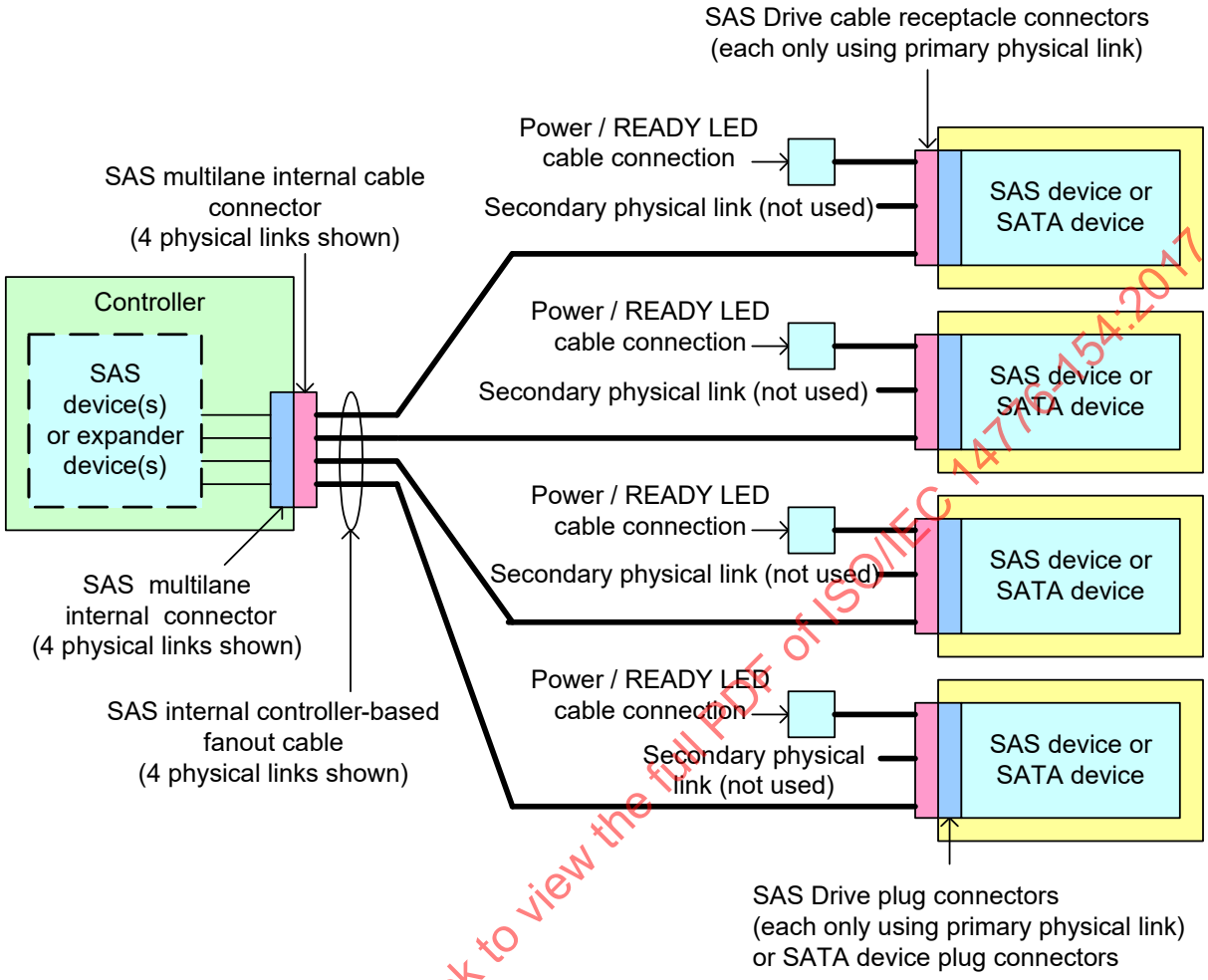


Figure 21 – SAS internal controller-based fanout cable environment

Figure 22 shows a representation of the SAS internal cable environment using a SAS backplane-based fanout cable (see 5.4.4.1.3).

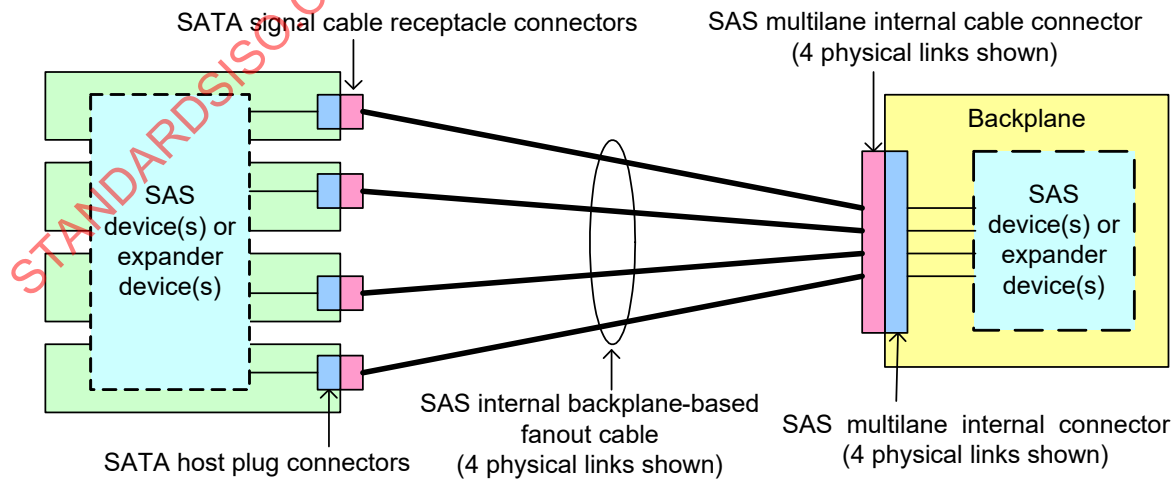


Figure 22 – SAS internal backplane-based fanout cable environment

5.4.3 Connectors

5.4.3.1 Connectors overview

Table 4 summarizes the connectors defined in this document.

Table 4 – Connectors (part 1 of 3)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SATA internal connectors used by SAS					
SATA signal cable receptacle	1	SATA	SATA host plug	1	SATA
SATA host plug	1	SATA	SATA signal cable receptacle	1	SATA
SATA device plug	1	SATA	SAS Drive cable receptacle	1 or 2	5.4.3.4.1.2
			SAS Drive backplane receptacle	2	5.4.3.4.1.3
			SAS MultiLink Drive cable receptacle	4	5.4.3.4.1.6
			SAS MultiLink Drive backplane receptacle	4	5.4.3.4.1.7
			Multifunction 12 Gbit/s 6x Unshielded receptacle connector	6 [a]	SFF-8639
Micro SATA device plug	1	SATA	Micro SAS receptacle	2	5.4.3.4.1.10
SAS internal connectors - SAS Drive connectors					
SAS Drive plug	2	5.4.3.4.1.1	SAS Drive cable receptacle	1 or 2	5.4.3.4.1.2
			SAS Drive backplane receptacle	2	5.4.3.4.1.3
			SAS MultiLink Drive cable receptacle	4	5.4.3.4.1.6
			SAS MultiLink Drive backplane receptacle	4	5.4.3.4.1.7
			Multifunction 12 Gbit/s 6x Unshielded receptacle connector	6 [a]	SFF-8639
SAS Drive cable receptacle	1 or 2	5.4.3.4.1.2	SAS Drive plug	2	5.4.3.4.1.1
			SAS MultiLink Drive plug	4	5.4.3.4.1.5
			SATA device plug	1	SATA
SAS Drive backplane receptacle	2	5.4.3.4.1.3	SAS Drive plug	2	5.4.3.4.1.1
			SAS MultiLink Drive plug	4	5.4.3.4.1.5
			SATA device plug	1	SATA

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 3 Gbit/s.
[c] Not recommended for rates greater than 6 Gbit/s.

Table 4 – Connectors (part 2 of 3)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
SAS Multilink Drive plug	4	5.4.3.4.1.5	SAS Drive cable receptacle	1 or 2	5.4.3.4.1.2
			SAS Drive backplane receptacle	2	5.4.3.4.1.3
			SAS MultiLink Drive cable receptacle	4	5.4.3.4.1.6
			SAS MultiLink Drive backplane receptacle	4	5.4.3.4.1.7
			Multifunction 12 Gbit/s 6x Unshielded receptacle connector	6 [a]	SFF-8639
SAS MultiLink Drive cable receptacle	4	5.4.3.4.1.6	SAS Drive plug	2	5.4.3.4.1.1
			SAS MultiLink Drive plug	4	5.4.3.4.1.5
			SATA device plug	1	SATA
SAS MultiLink Drive backplane receptacle	4	5.4.3.4.1.7	SAS Drive plug	2	5.4.3.4.1.1
			SAS MultiLink Drive plug	4	5.4.3.4.1.5
			SATA device plug	1	SATA
Multifunction 12 Gbit/s 6x Unshielded receptacle connector	6 [a]	SFF-8639	SAS Drive plug	2	5.4.3.4.1.1
			SAS MultiLink Drive plug	4	5.4.3.4.1.5
			SATA device plug	1	SATA
Micro SAS plug	2	5.4.3.4.1.9	Micro SAS receptacle	2	5.4.3.4.1.10
Micro SAS receptacle	2	5.4.3.4.1.10	Micro SAS plug	2	5.4.3.4.1.9
			Micro SATA device plug	1	SATA
SAS internal connectors - other					
SAS 4i cable receptacle [b]	4	5.4.3.4.2.1	SAS 4i plug [b]	4	5.4.3.4.2.2
SAS 4i plug [b]	4	5.4.3.4.2.2	SAS 4i cable receptacle [b]	4	5.4.3.4.2.1
Mini SAS 4i cable plug	4	5.4.3.4.3.1	Mini SAS 4i receptacle	4	5.4.3.4.3.2
Mini SAS 4i receptacle	4	5.4.3.4.3.2	Mini SAS 4i cable plug	4	5.4.3.4.3.1
Mini SAS HD 4i cable plug	4	5.4.3.4.4.1	Mini SAS HD 4i receptacle	4	5.4.3.4.4.3
			Mini SAS HD 8i receptacle	8	5.4.3.4.4.4
			Mini SAS HD 16i receptacle	16	5.4.3.4.4.5
Mini SAS HD 8i cable plug	8	5.4.3.4.4.2	Mini SAS HD 8i receptacle	8	5.4.3.4.4.4
			Mini SAS HD 16i receptacle	16	5.4.3.4.4.5
Mini SAS HD 4i receptacle	4	5.4.3.4.4.3	Mini SAS HD 4i cable plug	4	5.4.3.4.4.1
Mini SAS HD 8i receptacle	8	5.4.3.4.4.4	Mini SAS HD 4i cable plug	4	5.4.3.4.4.1
			Mini SAS HD 8i cable plug	8	5.4.3.4.4.2

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 3 Gbit/s.
[c] Not recommended for rates greater than 6 Gbit/s.

Table 4 – Connectors (part 3 of 3)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
Mini SAS HD 16i receptacle	16	5.4.3.4.4.5	Mini SAS HD 4i cable plug	4	5.4.3.4.4.1
			Mini SAS HD 8i cable plug	8	5.4.3.4.4.2
SAS external connectors					
Mini SAS 4x cable plug [c]	4	5.4.3.5.1.1	Mini SAS 4x receptacle [c] Mini SAS 4x active receptacle [c]	4	5.4.3.5.1.2
Mini SAS 4x receptacle [c]	4	5.4.3.5.1.2	Mini SAS 4x cable plug [c]	4	5.4.3.5.1.1
Mini SAS 4x active cable assembly plug [c]	4	5.4.3.5.1.1	Mini SAS 4x active receptacle [c]	4	5.4.3.5.1.2
Mini SAS 4x active receptacle [c]	4	5.4.3.5.1.2	Mini SAS 4x cable plug [c] Mini SAS 4x active cable assembly plug [c]	4	5.4.3.5.1.1
Mini SAS HD 4x cable plug	4	5.4.3.5.2.1	Mini SAS HD 4x receptacle	4	5.4.3.5.2.3
			Mini SAS HD 8x receptacle	8	5.4.3.5.2.4
			Mini SAS HD 16x receptacle	16	5.4.3.5.2.5
Mini SAS HD 8x cable plug	8	5.4.3.5.2.2	Mini SAS HD 8x receptacle	8	5.4.3.5.2.4
			Mini SAS HD 16x receptacle	16	5.4.3.5.2.5
Mini SAS HD 4x receptacle	4	5.4.3.5.2.3	Mini SAS HD 4x cable plug	4	5.4.3.5.2.1
Mini SAS HD 8x receptacle	8	5.4.3.5.2.4	Mini SAS HD 4x cable plug	4	5.4.3.5.2.1
			Mini SAS HD 8x cable plug	8	5.4.3.5.2.2
Mini SAS HD 16x receptacle	16	5.4.3.5.2.5	Mini SAS HD 4x cable plug	4	5.4.3.5.2.1
			Mini SAS HD 8x cable plug	8	5.4.3.5.2.2
QSFP+ cable plug	4	5.4.3.5.3.1	QSFP+ receptacle	4	5.4.3.5.3.2
QSFP+ receptacle	4	5.4.3.5.3.2	QSFP+ cable plug	4	5.4.3.5.3.1

[a] A maximum of four physical links support SAS applications.
[b] Not recommended for rates greater than 3 Gbit/s.
[c] Not recommended for rates greater than 6 Gbit/s.

A SAS icon (see annex I) should be placed on or near each SAS connector.

5.4.3.2 Connector categories

The relationship between connector categories and connectors is shown in table 5.

Table 5 – Connector categories

Connector category	Connectors in category
Unmanaged passive	All connectors listed in table 4 (see 5.4.3.1) that are not listed elsewhere in this table
Unmanaged active	Mini SAS 4x active connectors (see 5.4.3.5.1)
Managed	Mini SAS HD external connectors (see 5.4.3.5.2) QSFP+ connectors (see 5.4.3.5.3)

5.4.3.3 Recommended electrical performance limits for mated connector pairs supporting rates of 12 Gbit/s

Recommended electrical performance limits for connector mated pairs supporting rates of 12 Gbit/s are defined in Table 6 and shown in figure 23. The TxRx connection shall meet the requirements of 5.5.6 or 5.5.7 for 12 Gbit/s applications.

Table 6 – Recommended electrical performance limits for the mated connector pairs that support rates of 12 Gbit/s

Characteristic [a] [b]	Units	Value
Maximum near-end crosstalk (NEXT) for each signal pair [c] [d]	dB	-35
Maximum far-end crosstalk (FEXT) for each signal pair [c] [d]	dB	-35
Maximum S_{DD22}	dB	-12
Maximum S_{CC22}	dB	-3.0
Minimum S_{DD21}	dB	-1.0

[a] All measurements apply to connector mated pairs supporting rates of 12 Gbit/s and include the mounting footprint or wire termination.

[b] All characteristic values apply to the frequency range from 100 MHz to 6 000 MHz. The measurement output should include results to a minimum of 20 GHz.

[c] Determine all near-end and far-end significant crosstalk transfer modes. The sum of the crosstalk transfer ratios is measured in the frequency domain. The following equation details the summation process of the valid near-end crosstalk sources:

$$\mathrm{TotalNEXT}(f) = 10 \times \log_{10} \sum_{1}^{n} 10^{\langle \mathrm{NEXT}(f)/10 \rangle}$$

where:

f frequency; and

n number of the near-end crosstalk source.

All NEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

The following equation details the summation process of the valid far-end crosstalk sources:

$$\mathrm{TotalFEXT}(f) = 10 \times \log_{10} \sum_{1}^{n} 10^{\langle \mathrm{FEXT}(f)/10 \rangle}$$

where:

f frequency; and

n number of the far-end crosstalk source.

All FEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

[d] Total TxRx connection crosstalk should be at least 15 dB less than its total insertion loss. A total TxRx connection crosstalk of -35 dB implies an acceptable TxRx connection total insertion loss of 20 dB.

Figure 23 shows the recommended $|S_{DD21}|$, $|S_{CC22}|$, $|S_{DD22}|$, NEXT, and FEXT limits connector mated pairs supporting rates of 12 Gbit/s.

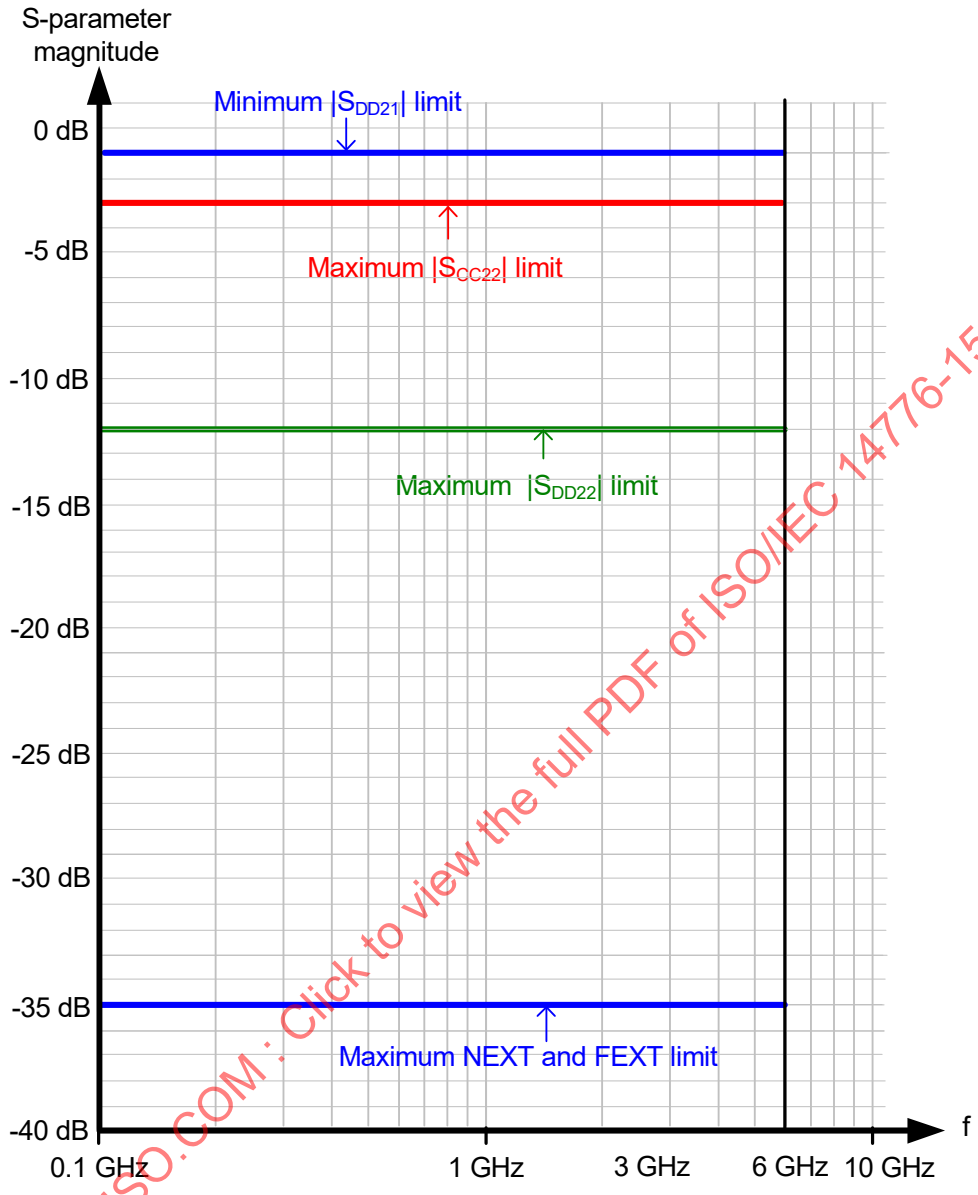


Figure 23 – Recommended $|S_{DD21}|$, $|S_{CC22}|$, $|S_{DD22}|$, NEXT, and FEXT limits for connector mated pairs supporting rates of 12 Gbit/s

5.4.3.4 SAS internal connectors

5.4.3.4.1 SAS Drive connectors

5.4.3.4.1.1 SAS Drive plug connector

The SAS Drive plug connector is the Device Free (Plug) connector defined in SFF-8680.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 24 shows the SAS Drive plug connector.

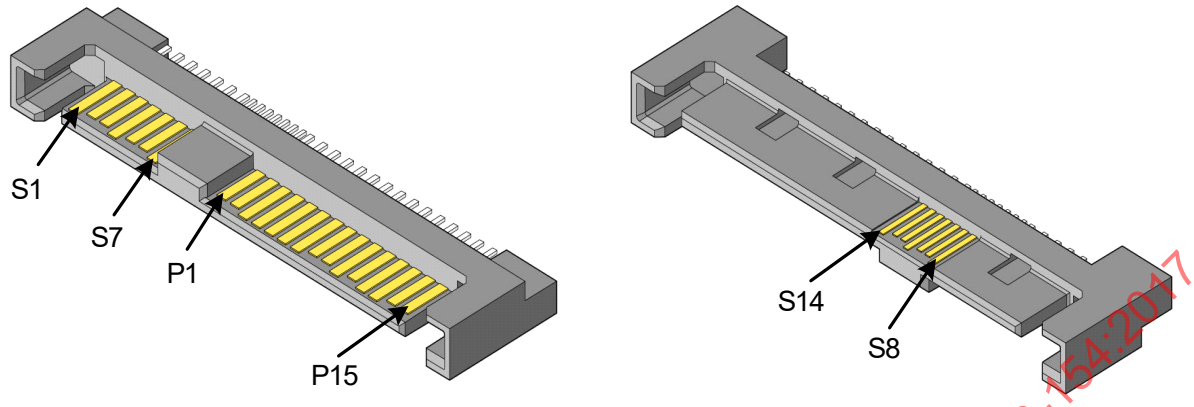


Figure 24 – SAS Drive plug connector

Table 7 (see 5.4.3.4.1.4) defines the pin assignments for the SAS Drive plug connector.

5.4.3.4.1.2 SAS Drive cable receptacle connector

The SAS Drive cable receptacle connector is the Internal Cable Fixed (Receptacle) connector defined in SFF-8680.

The single-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and only the primary physical link; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 25 shows the single-port version of the SAS Drive cable receptacle connector.

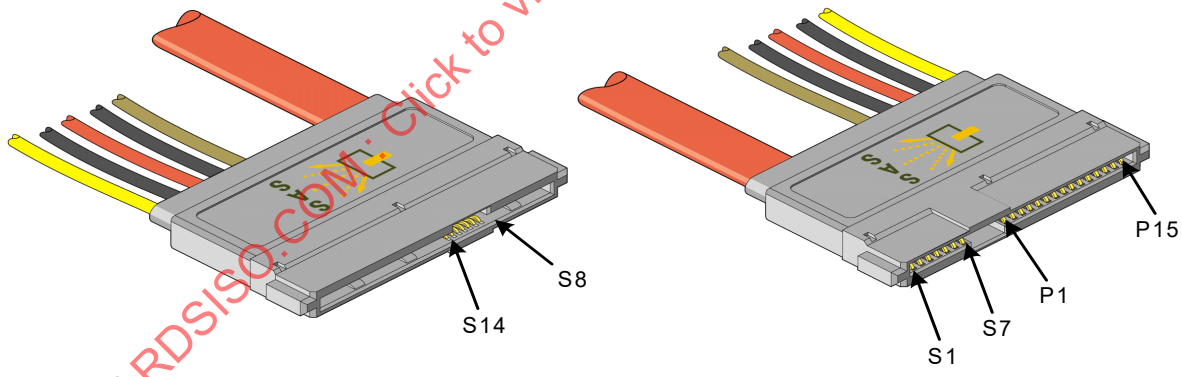


Figure 25 – Single-port SAS Drive cable receptacle connector

The dual-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links;
c) a SAS MultiLink Drive plug connector, providing contact for the power pins and both the primary and secondary physical links; or
d) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 26 shows the dual-port version of the SAS Drive cable receptacle connector.

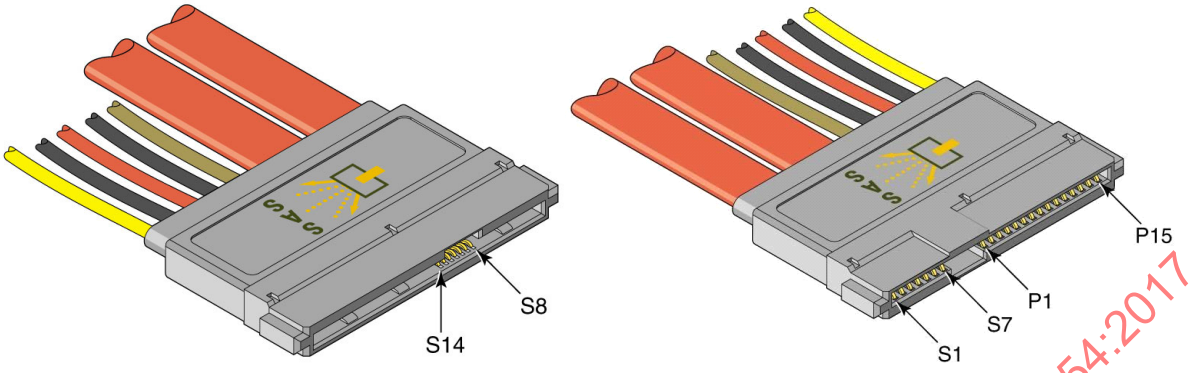


Figure 26 – Dual-port SAS Drive cable receptacle connector

Table 7 (see 5.4.3.4.1.4) defines the pin assignments for the SAS Drive cable receptacle connector. The secondary physical link (i.e., pins S8 through S14) is not supported by the single-port internal cable receptacle.

5.4.3.4.1.3 SAS Drive backplane receptacle connector

The SAS Drive backplane receptacle connector is the Backplane Fixed (Receptacle) connector defined in SFF-8680.

The SAS Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links;
c) a SAS MultiLink Drive plug connector, providing contact for the power pins and both primary and secondary physical links; or
d) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 27 shows the SAS Drive backplane receptacle connector.

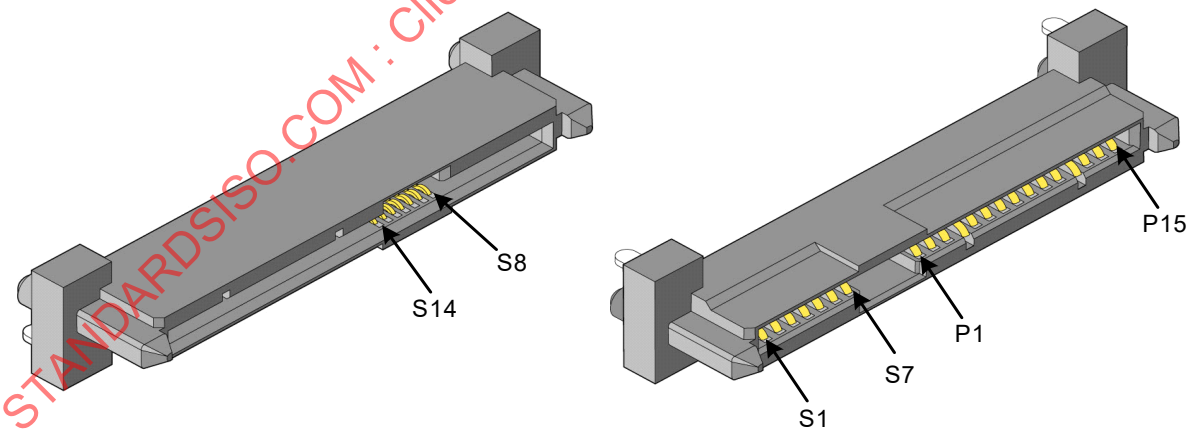


Figure 27 – SAS Drive backplane receptacle connector

Table 7 (see 5.4.3.4.1.4) defines the pin assignments for the SAS Drive backplane receptacle connector.

5.4.3.4.1.4 SAS Drive connector pin assignments

Table 7 defines the SAS target device pin assignments for the SAS Drive plug connector (see 5.4.3.4.1.1), the SAS Drive cable receptacle connector (see 5.4.3.4.1.2), and the SAS Drive backplane receptacle connector (see 5.4.3.4.1.3). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

SAS Drive plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a SATA device plug connector (see SATA).

Table 7 – SAS Drive connector pin assignments (part 1 of 2)

Segment	Pin	Backplane receptacle	SAS Drive plug and SAS Drive cable receptacle
Primary signal segment	S1	SIGNAL GROUND	
	S2	TP+	RP+
	S3	TP-	RP-
	S4	SIGNAL GROUND	
	S5	RP-	TP-
	S6	RP+	TP+
	S7	SIGNAL GROUND	
Secondary signal segment [a]	S8	SIGNAL GROUND	
	S9	TS+	RS+
	S10	TS-	RS-
	S11	SIGNAL GROUND	
	S12	RS-	TS-
	S13	RS+	TS+
	S14	SIGNAL GROUND	

[a] S8 through S14 are not connected on single-port implementations.
[b] SAS drive backplane receptacle connectors and SAS Drive cable receptacle connectors provide V_5 and V_{12}. SAS Drive plug connectors receive V_5 and V_{12}.
[c] Behind a SAS Drive plug connector, P1 and P2 are only connected to each other.
[d] SAS devices (see SPL-3) with SAS Drive plug connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together. SAS Drive backplane connectors and SAS Drive cable receptacle connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide $V_{3.3}$ to P1, P2, and P3.
[e] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors (see 5.4.3.4.1.7), and SAS MultiLink Drive cable receptacle connectors (see 5.4.3.4.1.6) are beyond the scope of this specification.
[f] Devices supporting other interfaces have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[g] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[h] Behind a SAS Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[i] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-3. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

Table 7 – SAS Drive connector pin assignments (part 2 of 2)

Segment	Pin	Backplane receptacle	SAS Drive plug and SAS Drive cable receptacle
Power segment [b]	P1	Vendor specific [d e]	See [c d f]
	P2	Vendor specific [d e]	See [c d f]
	P3	Vendor specific or POWER DISABLE [d f g]	POWER DISABLE [d f g]
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [h]	
	P8	V_5 [h]	
	P9	V_5 [h]	
	P10	GROUND	
	P11	READY LED [i]	
	P12	GROUND	
	P13	V_{12}, precharge [h]	
	P14	V_{12} [h]	
	P15	V_{12} [h]	

[a] S8 through S14 are not connected on single-port implementations.
[b] SAS drive backplane receptacle connectors and SAS Drive cable receptacle connectors provide V_5 and V_{12}. SAS Drive plug connectors receive V_5 and V_{12}.
[c] Behind a SAS Drive plug connector, P1 and P2 are only connected to each other.
[d] SAS devices (see SPL-3) with SAS Drive plug connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together. SAS Drive backplane connectors and SAS Drive cable receptacle connectors compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide $V_{3.3}$ to P1, P2, and P3.
[e] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors (see 5.4.3.4.1.7), and SAS MultiLink Drive cable receptacle connectors (see 5.4.3.4.1.6) are beyond the scope of this specification.
[f] Devices supporting other interfaces have different electrical characteristics and functions. See SFF-9639 for a list of interface references and their respective pin assignments.
[g] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[h] Behind a SAS Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[i] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-3. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.4.3.4.1.5 SAS MultiLink Drive plug connector

The SAS MultiLink Drive plug connector is the Device free (plug) connector defined in SFF-8630.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 28 shows the SAS MultiLink Drive plug connector

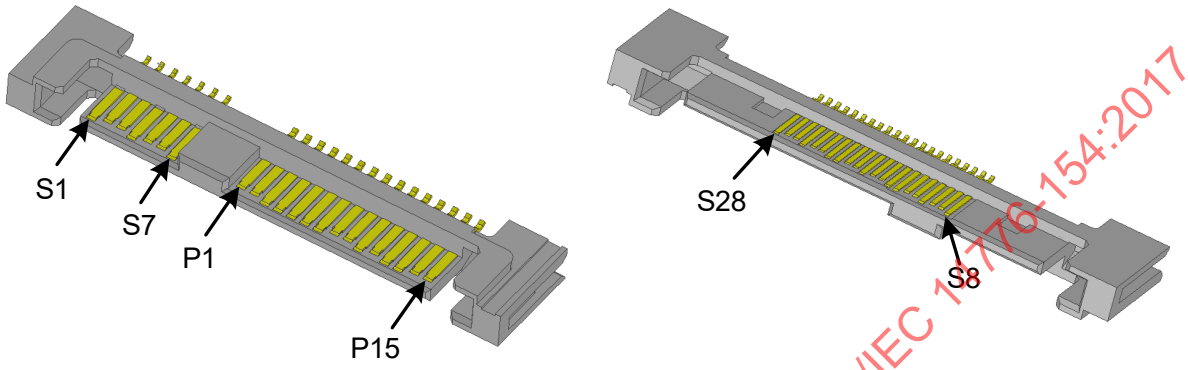


Figure 28 – SAS MultLink Drive plug connector

Table 8 (see 5.4.3.4.1.8) defines the pin assignments for the SAS MultiLink Drive plug connector.

5.4.3.4.1.6 SAS MultiLink Drive cable receptacle connector

The SAS MultiLink Drive cable receptacle connector is the Internal Cable Fixed (Receptacle) connector defined in SFF-8630.

The SAS MultiLink Drive cable receptacle attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and four physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 29 shows the SAS MultiLink Drive cable receptacle connector.

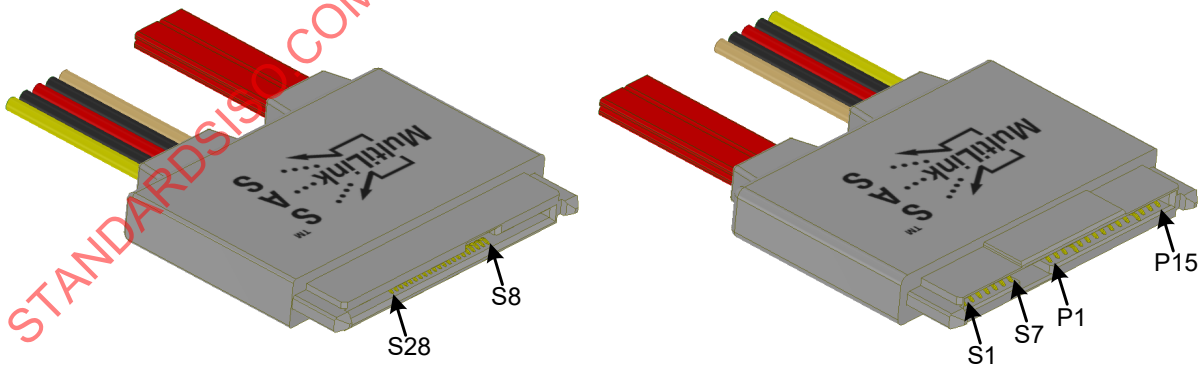


Figure 29 – SAS MultiLink Drive cable receptacle connector

Table 8 (see 5.4.3.4.1.4) defines the pin assignments for the SAS MultiLink Drive cable receptacle connector.

5.4.3.4.1.7 SAS MultiLink Drive backplane receptacle connector

The SAS MultiLink Drive backplane receptacle connector is the Backplane Fixed (Receptacle) connector defined in SFF-8630.

The SAS MultiLink Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links;
b) a SAS MultiLink Drive plug connector, providing contact for the power pins and four physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 30 shows the SAS MultiLink Drive backplane receptacle connector.

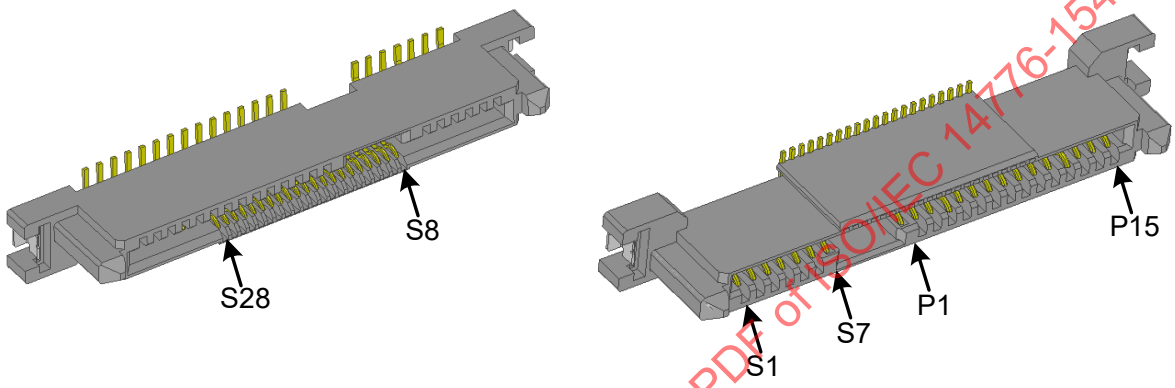


Figure 30 – SAS MultiLink Drive backplane receptacle connector

Table 8 (see 5.4.3.4.1.8) defines the pin assignments for the SAS MultiLink Drive backplane receptacle connector.

5.4.3.4.1.8 SAS MultiLink Drive connector pin assignments

Table 8 defines the SAS target device pin assignments for the SAS MultiLink Drive plug connector (see 5.4.3.4.1.5), the SAS MultiLink Drive cable receptacle connector (see 5.4.3.4.1.6), and the SAS MultiLink Drive backplane receptacle connector (see 5.4.3.4.1.7). TX0+, TX0-, RX0+, and RX0- are used by the signal segment 0 physical link. TX1+, TX1-, RX1+, and RX1- are used by the signal segment 1 physical link, if any. TX2+, TX2-, RX2+, and RX2- are used by the signal segment 2 physical link, if any. TX3+, TX3-, RX3+, and RX3- are used by the signal segment 3 physical link, if any.

Table 8 – SAS MultiLink connector pin assignments (part 1 of 3)

Segment	Pin	SAS MultiLink Drive backplane receptacle	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle
Signal segment 0	S1	SIGNAL GROUND	
	S2	TX 0+	RX 0+
	S3	TX 0-	RX 0-
	S4	SIGNAL GROUND	
	S5	RX 0-	TX 0-
	S6	RX 0+	TX 0+
	S7	SIGNAL GROUND	
Signal segment 1 [a]	S8	SIGNAL GROUND	
	S9	TX 1+	RX 1+
	S10	TX 1-	RX 1-
	S11	SIGNAL GROUND	
	S12	RX 1-	TX 1-
	S13	RX 1+	TX 1+
	S14	SIGNAL GROUND	
	S15	RESERVED	

[a] S8 through S28 are not connected on single-port implementations.
[b] S15 through S28 are not connected on dual-port implementations.
[c] S22 through S28 are not connected on triple-port implementations.
[d] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[e] Behind a SAS MultiLink Drive plug connector, P1 and P2 are only connected to each other.
[f] SAS devices (see SPL-3) with SAS Drive plug connectors (see 5.4.3.4.1.1) compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together.
[g] SAS Drive backplane connectors (see 5.4.3.4.1.3) and SAS Drive cable receptacle connectors (see 5.4.3.4.1.2) compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[h] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors, and SAS MultiLink Drive cable receptacle connectors are beyond the scope of this specification.
[i] Devices supporting other interfaces that intermate with SAS devices, backplanes, or cables may have different electrical characteristics and functions on P1, P2, and P3. See SFF-9639 for a list of interface references and their respective pin assignments.
[j] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[k] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[l] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-3. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

Table 8 – SAS MultiLink connector pin assignments (part 2 of 3)

Segment	Pin	SAS MultiLink Drive backplane receptacle	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle
Signal segment 2 [a] [b]	S16	SIGNAL GROUND	
	S17	TX 2+	RX 2+
	S18	TX 2-	RX 2-
	S19	SIGNAL GROUND	
	S20	RX 2-	TX 2-
	S21	RX 2+	TX 2+
	S22	SIGNAL GROUND	
Signal segment 3 [a] [b] [c]	S23	TX 3+	RX 3+
	S24	TX 3-	RX 3-
	S25	SIGNAL GROUND	
	S26	RX 3-	TX 3-
	S27	RX 3+	TX 3+
	S28	SIGNAL GROUND	

[a] S8 through S28 are not connected on single-port implementations.
[b] S15 through S28 are not connected on dual-port implementations.
[c] S22 through S28 are not connected on triple-port implementations.
[d] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[e] Behind a SAS MultiLink Drive plug connector, P1 and P2 are only connected to each other.
[f] SAS devices (see SPL-3) with SAS Drive plug connectors (see 5.4.3.4.1.1) compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together.
[g] SAS Drive backplane connectors (see 5.4.3.4.1.3) and SAS Drive cable receptacle connectors (see 5.4.3.4.1.2) compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[h] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors, and SAS MultiLink Drive cable receptacle connectors are beyond the scope of this specification.
[i] Devices supporting other interfaces that intermate with SAS devices, backplanes, or cables may have different electrical characteristics and functions on P1, P2, and P3. See SFF-9639 for a list of interface references and their respective pin assignments.
[j] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[k] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[l] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-3. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

Table 8 – SAS MultiLink connector pin assignments (part 3 of 3)

Segment	Pin	SAS MultiLink Drive backplane receptacle	SAS MultiLink Drive plug and SAS MultiLink Drive cable receptacle
Power segment [d]	P1	Vendor specific [f g h i]	See [e f g h i]
	P2	Vendor specific [f g h i]	See [e f g h i]
	P3	Vendor specific or POWER DISABLE [f g h i j]	POWER DISABLE [f g h i j]
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [k]	
	P8	V_5 [k]	
	P9	V_5 [k]	
	P10	GROUND	
	P11	READY LED [l]	
	P12	GROUND	
	P13	V_{12}, precharge [k]	
	P14	V_{12} [k]	
	P15	V_{12} [k]	

[a] S8 through S28 are not connected on single-port implementations.
[b] S15 through S28 are not connected on dual-port implementations.
[c] S22 through S28 are not connected on triple-port implementations.
[d] SAS MultiLink Drive backplane receptacle connectors and SAS MultiLink Drive cable receptacle connectors provide V_5 and V_{12}. SAS MultiLink Drive plug connectors receive V_5 and V_{12}.
[e] Behind a SAS MultiLink Drive plug connector, P1 and P2 are only connected to each other.
[f] SAS devices (see SPL-3) with SAS Drive plug connectors (see 5.4.3.4.1.1) compliant with SAS-1.1, SAS-2, or SAS-2.1 connected P1, P2, and P3 together.
[g] SAS Drive backplane connectors (see 5.4.3.4.1.3) and SAS Drive cable receptacle connectors (see 5.4.3.4.1.2) compliant with SAS-1.1, SAS-2, or SAS-2.1 may provide V_{33} to P1, P2, and P3.
[h] Electrical characteristics and functions behind SAS Drive backplane connectors, SAS Drive cable receptacles, SAS MultiLink Drive backplane connectors, and SAS MultiLink Drive cable receptacle connectors are beyond the scope of this specification.
[i] Devices supporting other interfaces that intermate with SAS devices, backplanes, or cables may have different electrical characteristics and functions on P1, P2, and P3. See SFF-9639 for a list of interface references and their respective pin assignments.
[j] P3 is not connected behind a SAS Drive plug connector if the POWER DISABLE signal is unsupported. Electrical characteristics for the POWER DISABLE signal are defined in 5.10.
[k] Behind a SAS MultiLink Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).
[l] Electrical characteristics for READY LED are defined in 5.9 and signal behavior is defined in SPL-3. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.4.3.4.1.9 Micro SAS plug connector

The Micro SAS plug connector is defined in SFF-8486. The Micro SAS plug mates with the Micro SAS Receptacle (see 5.4.3.4.1.10), but not the Micro SATA receptacle (see SATA).

See SFF-8147 for the Micro SAS plug connector locations on common form factors. Figure 31 shows the Micro SAS plug connector.

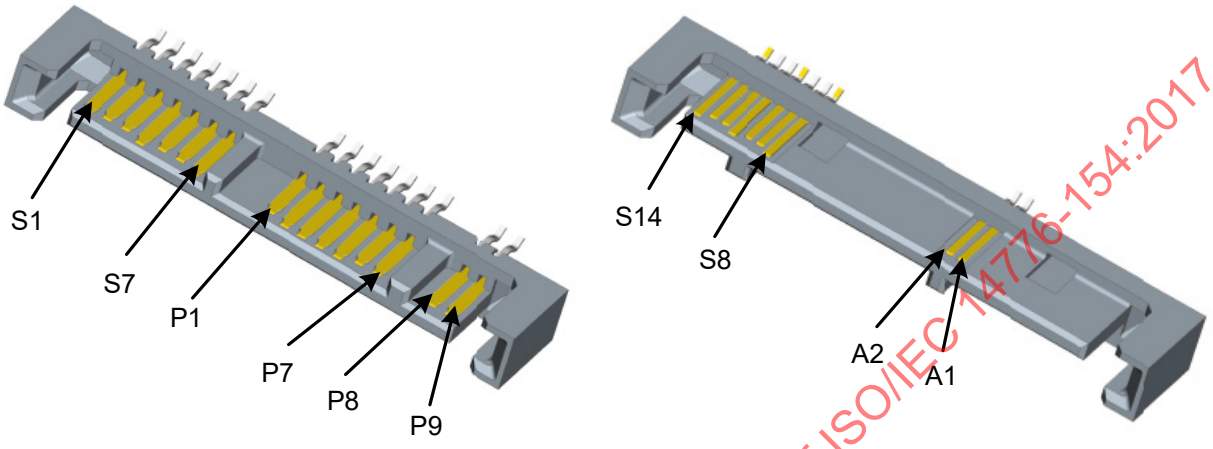


Figure 31 – Micro SAS plug connector

5.4.3.4.1.10 Micro SAS receptacle connector

The Micro SAS receptacle connector is defined in SFF-8486. The Micro SAS receptacle mates with the Micro SAS plug connector (see 5.4.3.4.1.9) or the Micro SATA device plug (see SATA).

Figure 32 shows the Micro SAS receptacle connector.

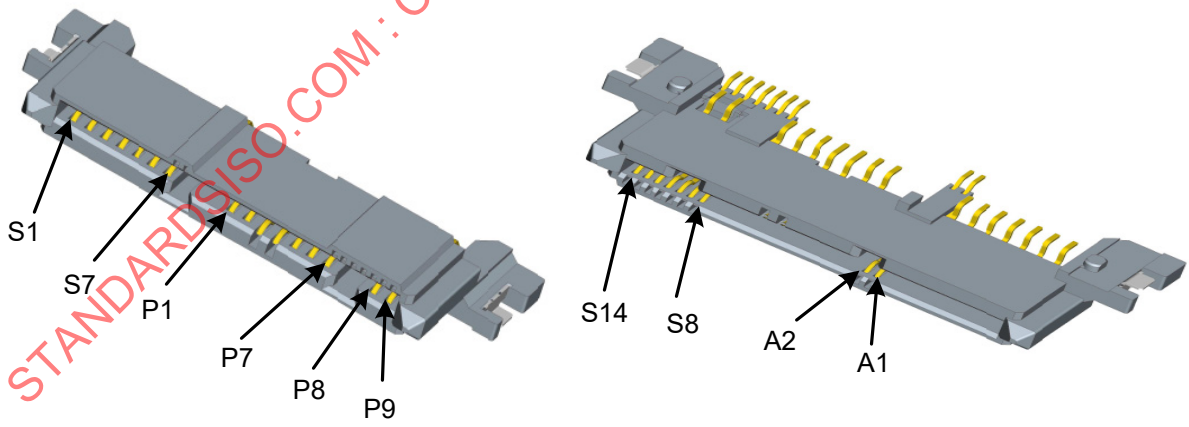


Figure 32 – Micro SAS receptacle connector

5.4.3.4.1.11 Micro SAS connector pin assignments

Table 9 defines the SAS target device pin assignments for the Micro SAS plug connector (see 5.4.3.4.1.9) and the Micro SAS receptacle connector (see 5.4.3.4.1.10). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

Micro SAS plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a Micro SATA device plug connector (see SATA).

Table 9 – Micro SAS connector pin assignments

Segment	Pin	Micro SAS receptacle	Micro SAS plug	Mating level [a]
Primary signal segment	S1	SIGNAL GROUND		Second
	S2	TP+	RP+	Third
	S3	TP-	RP-	Third
	S4	SIGNAL GROUND		Second
	S5	RP-	TP-	Third
	S6	RP+	TP+	Third
	S7	SIGNAL GROUND		Second
Secondary signal segment [b]	S8	SIGNAL GROUND		Second
	S9	TS+	RS+	Third
	S10	TS-	RS-	Third
	S11	SIGNAL GROUND		Second
	S12	RS-	TS-	Third
	S13	RS+	TS+	Third
	S14	SIGNAL GROUND		Second
Power segment [c]	P1	V_{33} [d]		Third
	P2	V_{33}, precharge [d]		Second
	P3	GROUND		First
	P4	GROUND		First
	P5	V_5, precharge [d]		Second
	P6	V_5 [d]		Third
	P7	Reserved		Third
	P8	Not connected	Manufacturing diagnostic	Third
	P9	Not connected	Manufacturing diagnostic	Third
Auxiliary contacts	A1	Vender specific		Third
	A2	Vender specific		Third

[a] The mating level assumes zero angular offset between connectors and indicates the physical dimension of the contact (see SFF-8486 and SATA).
[b] S8 through S14 are not connected on single-port implementations.
[c] The Micro SAS receptacle connector (see 5.4.3.4.1.10) provides V_{33} and V_5. The Micro SATA power receptacle connector (see SATA) provides V_{33} and optionally V_5. The Micro SAS plug connector (see 5.4.3.4.1.9) receives V_{33} and V_5.
[d] Behind a Micro SAS plug connector (see 5.4.3.4.1.9), the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_{33}, precharge pin P2 is connected to the V_{33} pin P1).

5.4.3.4.2 SAS 4i connectors

5.4.3.4.2.1 SAS 4i cable receptacle connector

The SAS 4i cable receptacle connector is the 4 Lane Cable Receptacle (fixed) with Backshell connector defined in SFF-8484. The SAS 4i cable receptacle connector should not be used for rates greater than 3 Gbit/s.

Figure 33 shows the SAS 4i cable receptacle connector.

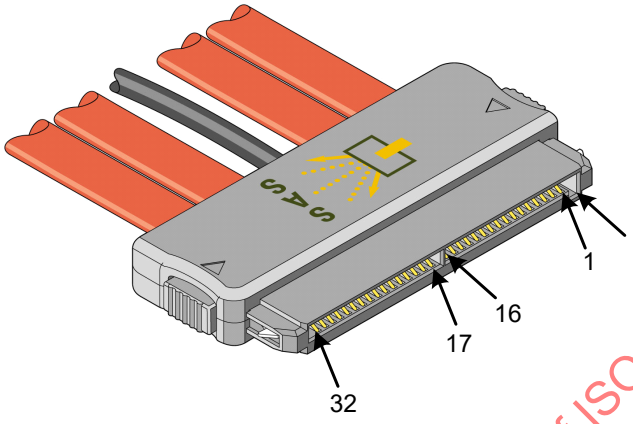


Figure 33 – SAS 4i cable receptacle connector

Table 10 and table 11 (see 5.4.3.4.2.3) define the pin assignments for the SAS 4i cable receptacle connector.

5.4.3.4.2.2 SAS 4i plug connector

The SAS 4i plug connector is the 4 Lane Vertical Plug (free) or 4 Lane R/A Plug (free) connector defined in SFF-8484. The SAS 4i plug connector should not be used for rates greater than 3 Gbit/s.

Figure 34 shows the SAS 4i plug connector.

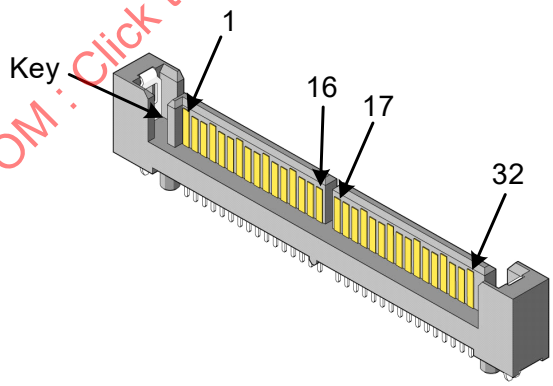


Figure 34 – SAS 4i plug connector

Table 10 and table 11 (see 5.4.3.4.2.3) define the pin assignments for the SAS 4i plug connector.

5.4.3.4.2.3 SAS 4i connector pin assignments

Table 10 defines the pin assignments for SAS 4i cable receptacle connectors (see 5.4.3.4.2.1) and SAS 4i plug connectors (see 5.4.3.4.2.2) for controller applications using one, two, three, or four of the physical links.

Table 10 – Controller SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly			
	One	Two	Three	Four
RX 0+	2	2	2	2
RX 0-	3	3	3	3
TX 0-	5	5	5	5
TX 0+	6	6	6	6
RX 1+	N/C	8	8	8
RX 1-	N/C	9	9	9
TX 1-	N/C	11	11	11
TX 1+	N/C	12	12	12
SIDEBAND 0	14	14	14	14
SIDEBAND 1	15	15	15	15
SIDEBAND 2	16	16	16	16
SIDEBAND 3	17	17	17	17
SIDEBAND 4	18	18	18	18
SIDEBAND 5	19	19	19	19
RX 2+	N/C	N/C	21	21
RX 2-	N/C	N/C	22	22
TX 2-	N/C	N/C	24	24
TX 2+	N/C	N/C	25	25
RX 3+	N/C	N/C	N/C	27
RX 3-	N/C	N/C	N/C	28
TX 3-	N/C	N/C	N/C	30
TX 3+	N/C	N/C	N/C	31
SIGNAL GROUND	1, 4, 7, 10, 13, 20, 23, 26, 29, 32			

Key:

N/C = not connected

The use of the sideband signals by a controller is vendor specific. One implementation of the sideband signals by a controller is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 11 defines the pin assignments for SAS 4i plug connectors (see 5.4.3.4.2.1) and SAS 4i cable receptacle connectors (see 5.4.3.4.2.1) for backplane applications using one, two, three, or four of the physical links.

Table 11 – Backplane SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly			
	One	Two	Three	Four
RX 3+	N/C	N/C	N/C	2
RX 3-	N/C	N/C	N/C	3
TX 3-	N/C	N/C	N/C	5
TX 3+	N/C	N/C	N/C	6
RX 2+	N/C	N/C	8	8
RX 2-	N/C	N/C	9	9
TX 2-	N/C	N/C	11	11
TX 2+	N/C	N/C	12	12
SIDEBAND 5	14	14	14	14
SIDEBAND 4	15	15	15	15
SIDEBAND 3	16	16	16	16
SIDEBAND 2	17	17	17	17
SIDEBAND 1	18	18	18	18
SIDEBAND 0	19	19	19	19
RX 1+	N/C	21	21	21
RX 1-	N/C	22	22	22
TX 1-	N/C	24	24	24
TX 1+	N/C	25	25	25
RX 0+	27	27	27	27
RX 0-	28	28	28	28
TX 0-	30	30	30	30
TX 0+	31	31	31	31
SIGNAL GROUND	1, 4, 7, 10, 13, 20, 23, 26, 29, 32			
Key: N/C = not connected				

The use of the sideband signals by a backplane is vendor specific. One implementation of the sideband signals by a backplane is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.4.3 Mini SAS 4i connectors

5.4.3.4.3.1 Mini SAS 4i cable plug connector

The Mini SAS 4i cable plug connector is the free (plug) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 35 shows the Mini SAS 4i cable plug connector.

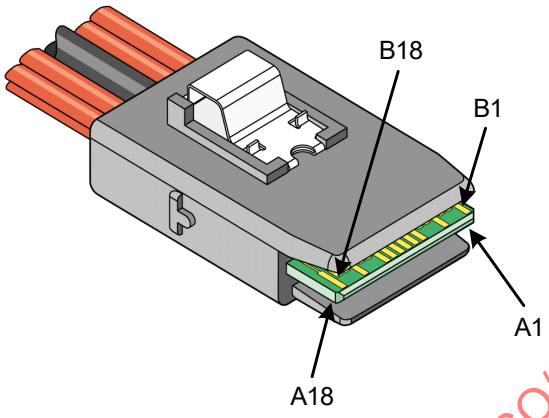


Figure 35 – Mini SAS 4i cable plug connector

Table 12 and table 13 (see 5.4.3.4.3.3) define the pin assignments for the Mini SAS 4i cable plug connector.

5.4.3.4.3.2 Mini SAS 4i receptacle connector

The Mini SAS 4i receptacle connector is the fixed (receptacle) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 36 shows the Mini SAS 4i receptacle connector.

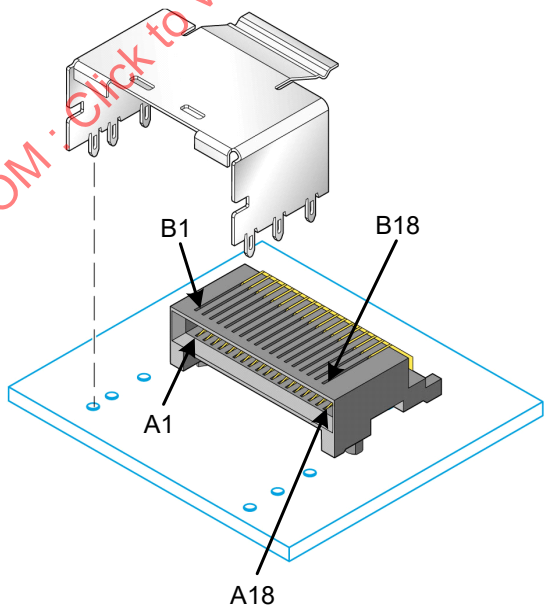


Figure 36 – Mini SAS 4i receptacle connector

Table 12 and table 13 (see 5.4.3.4.4.6) define the pin assignments for the Mini SAS 4i receptacle connector.

5.4.3.4.3.3 Mini SAS 4i connector pin assignments

Table 12 defines the pin assignments for Mini SAS 4i plug connectors (see 5.4.3.4.3.1) and Mini SAS 4i cable receptacle connectors (see 5.4.3.4.3.2) for controller applications using one, two, three, or four of the physical links.

Table 12 – Controller Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
SIDEBAND 7	A8	A8	A8	A8	First
SIDEBAND 3	A9	A9	A9	A9	
SIDEBAND 4	A10	A10	A10	A10	
SIDEBAND 5	A11	A11	A11	A11	
RX 2+	N/C	N/C	A13	A13	Third
RX 2-	N/C	N/C	A14	A14	
RX 3+	N/C	N/C	N/C	A16	
RX 3-	N/C	N/C	N/C	A17	
TX 0+	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
SIDEBAND 0	B8	B8	B8	B8	First
SIDEBAND 1	B9	B9	B9	B9	
SIDEBAND 2	B10	B10	B10	B10	
SIDEBAND 6	B11	B11	B11	B11	
TX 2+	N/C	N/C	B13	B13	Third
TX 2-	N/C	N/C	B14	B14	
TX 3+	N/C	N/C	N/C	B16	
TX 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

Key:

N/C = not connected

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 13 defines the pin assignments for Mini SAS 4i plug connectors (see 5.4.3.4.3.1) and Mini SAS 4i cable receptacle connectors (see 5.4.3.4.3.2) for backplane applications using one, two, three, or four of the physical links.

Table 13 – Backplane Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
SIDEBAND 0	A8	A8	A8	A8	First
SIDEBAND 1	A9	A9	A9	A9	
SIDEBAND 2	A10	A10	A10	A10	
SIDEBAND 6	A11	A11	A11	A11	
RX 2+	N/C	N/C	A13	A13	Third
RX 2-	N/C	N/C	A14	A14	
RX 3+	N/C	N/C	N/C	A16	
RX 3-	N/C	N/C	N/C	A17	
TX 0+	B2	B2	B2	B2	Third
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
SIDEBAND 7	B8	B8	B8	B8	First
SIDEBAND 3	B9	B9	B9	B9	
SIDEBAND 4	B10	B10	B10	B10	
SIDEBAND 5	B11	B11	B11	B11	
TX 2+	N/C	N/C	B13	B13	Third
TX 2-	N/C	N/C	B14	B14	
TX 3+	N/C	N/C	N/C	B16	
TX 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

Key:

N/C = not connected

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.4.4 Mini SAS HD internal connectors

5.4.3.4.4.1 Mini SAS HD 4i cable plug connector

The Mini SAS HD 4i cable plug connector is the four lane cable (free) connector defined in SFF-8643. Figure 37 shows the Mini SAS HD 4i cable plug connector.

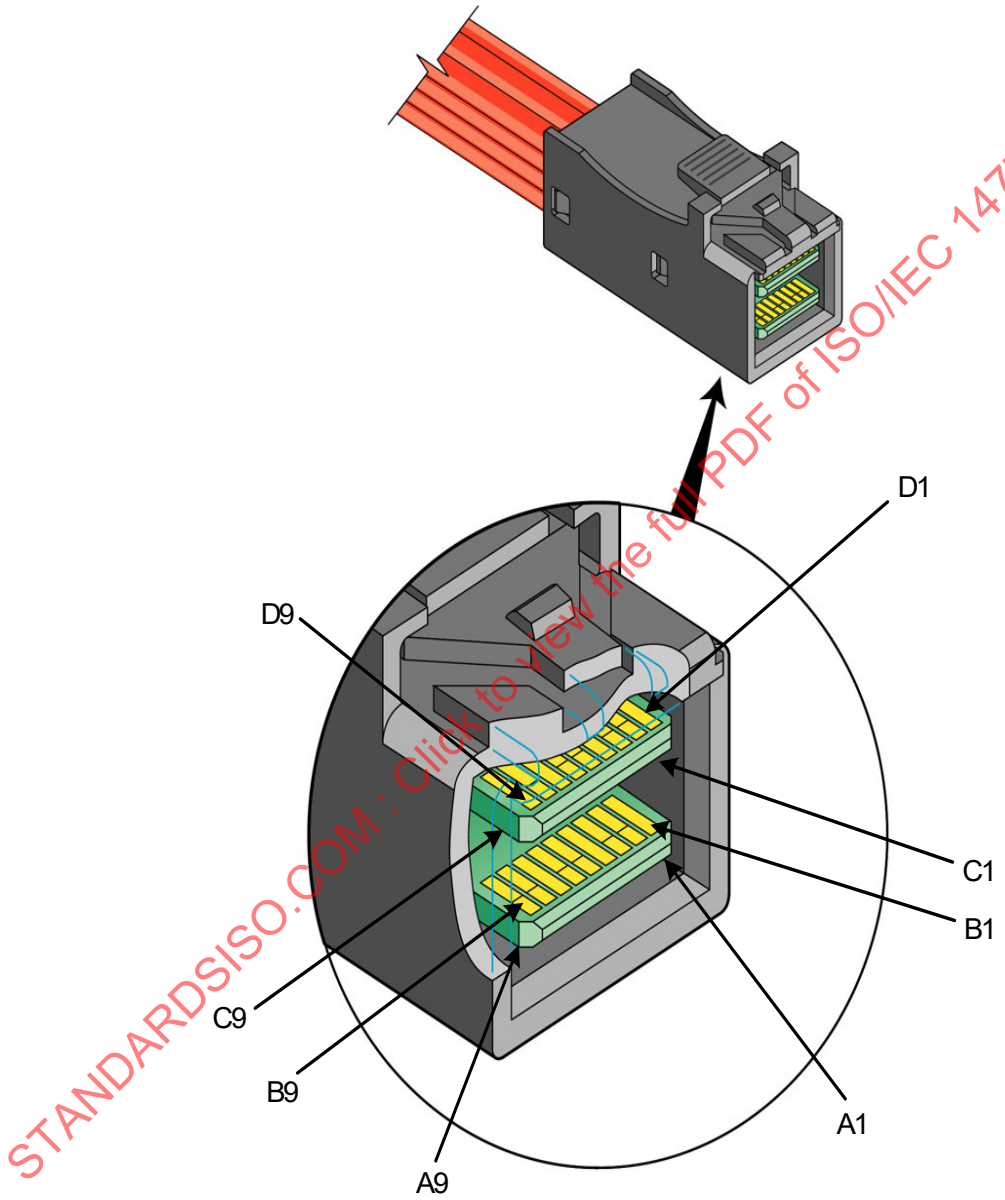


Figure 37 – Mini SAS HD 4i cable plug connector

Table 12 and table 13 (see 5.4.3.4.4.6) define the pin assignments for the Mini SAS HD 4i cable plug connector.

5.4.3.4.4.2 Mini SAS HD 8i cable plug connector

The Mini SAS HD 8i cable plug connector is the dual four lane cable plug (free) connector defined in SFF-8643.

Figure 38 shows the Mini SAS HD 8i cable plug connector. This connector is a modular version of repeating Mini SAS HD 4i cable plug connectors (see 5.4.3.4.4.1). Module labeling is shown in figure 38. See figure 37 (see 5.4.3.4.4.1) for pin designations.

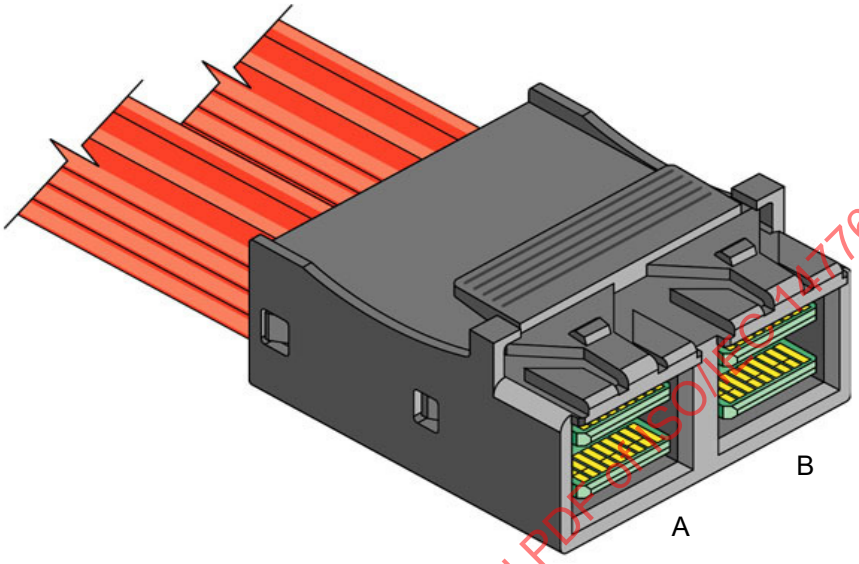


Figure 38 – Mini SAS HD 8i cable plug connector

Table 12 and table 13 (see 5.4.3.4.4.6) define the pin assignments for the Mini SAS HD 4i cable plug connector (see 5.4.3.4.4.1). The pin assignments are repeated for each module of the Mini SAS 8i cable plug connector.

5.4.3.4.4.3 Mini SAS HD 4i receptacle connector

The Mini SAS HD 4i receptacle connector is the four lane receptacle (fixed) connector defined in SFF-8643. Figure 39 shows the Mini SAS HD 4i receptacle connector.

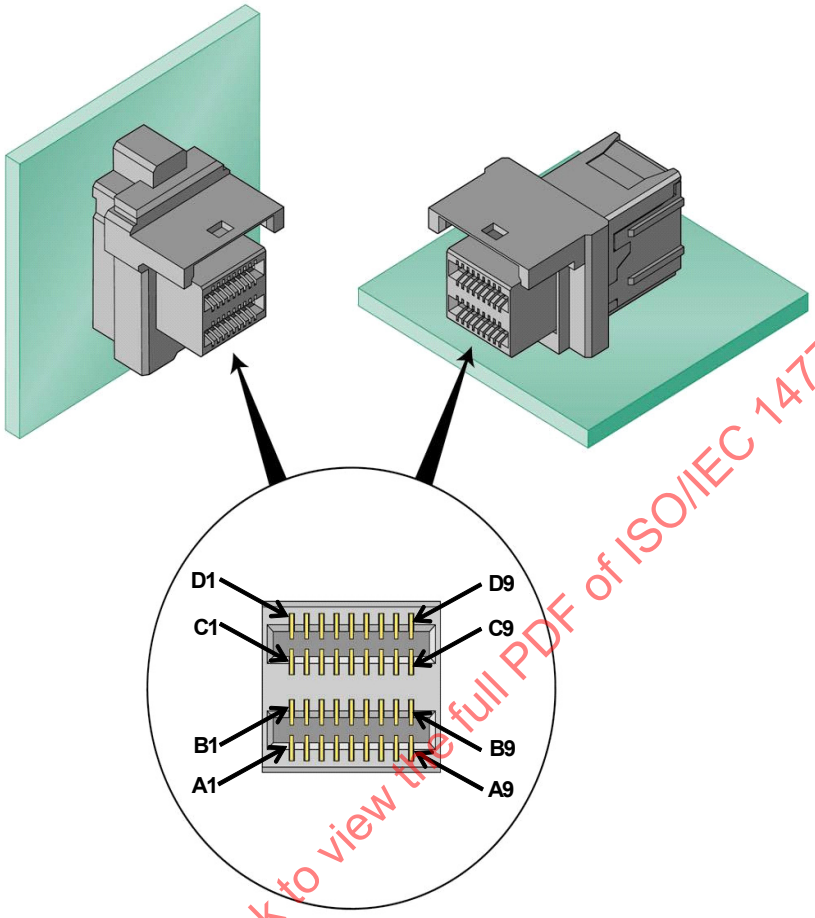


Figure 39 – Mini SAS HD 4i receptacle connector

Table 12 and table 13 (see 5.4.3.4.4.6) define the pin assignments for the Mini SAS HD 4i receptacle connector.

5.4.3.4.4.4 Mini SAS HD 8i receptacle connector

The Mini SAS HD 8i receptacle connector is a dual four lane receptacle (fixed) connector defined in SFF-8643. Figure 40 shows the Mini SAS HD 8i receptacle connector. This connector is a modular version of the Mini SAS HD 4i receptacle connector (see 5.4.3.4.4.3). Module labeling is shown in figure 40. See figure 39 (see 5.4.3.4.4.3) for pin designations.

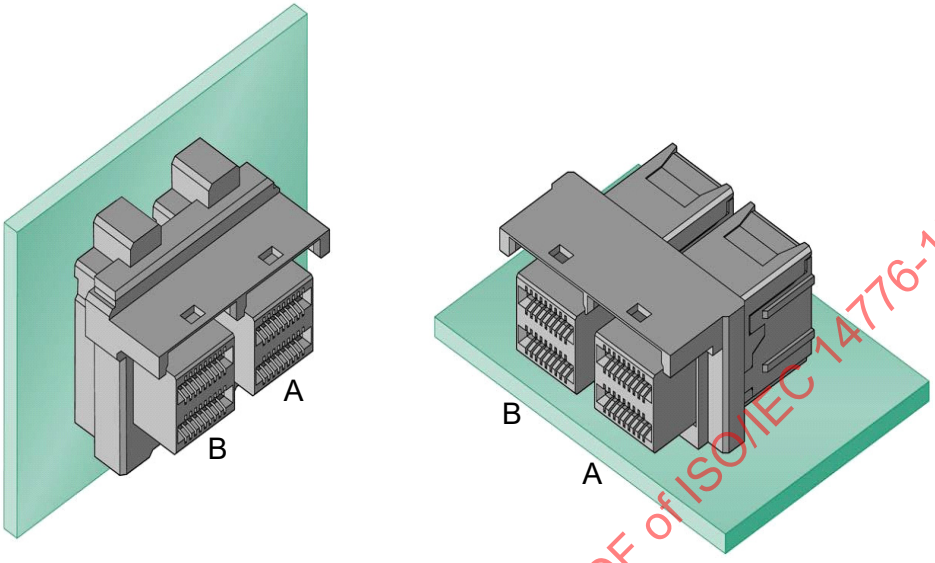


Figure 40 – Mini SAS HD 8i receptacle connector

Table 14 and table 15 (see 5.4.3.4.4.6) define the pin assignments for the Mini SAS HD 8i receptacle connector. The connector is a modular design of repeating Mini SAS HD 4i receptacles (see 5.4.3.4.4.3). This connector accepts one Mini SAS HD 8i cable plug connector (see 5.4.3.4.4.2) or two Mini SAS HD 4i cable plug connectors (see 5.4.3.4.4.1).

5.4.3.4.4.5 Mini SAS HD 16i receptacle connector

The Mini SAS HD 16i receptacle connector is a quad four lane receptacle (fixed) connector defined in SFF-8643. Figure 41 shows the Mini SAS HD 16i receptacle connector. This connector is a modular version of the Mini SAS HD 4i receptacle connector (see 5.4.3.4.4.3). Module labeling is shown in figure 41. See figure 39 (see 5.4.3.4.4.3) for pin designations.

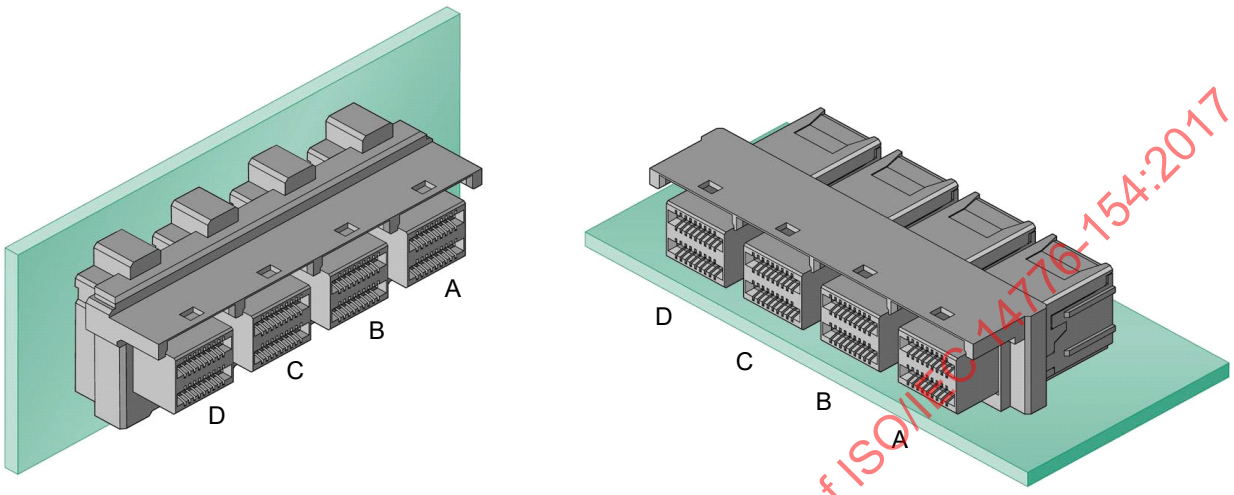


Figure 41 – Mini SAS HD 16i receptacle connector

Table 14 and table 15 (see 5.4.3.4.4.6) define the pin assignments for the Mini SAS HD 16i receptacle connector. The connector is a modular design of repeating Mini SAS HD 4i receptacles (see 5.4.3.4.4.3). The Mini SAS HD 16i receptacle connector accepts:

a) one or two Mini SAS HD 8i cable plug connectors (see 5.4.3.4.4.2);
b) one, two, three, or four Mini SAS HD 4i cable plug connectors (see 5.4.3.4.4.1); or
c) a combination of one Mini SAS HD 8i cable plug connector (see 5.4.3.4.4.2) and one or two Mini SAS HD 4i cable plug connectors (see 5.4.3.4.4.1).

A Mini SAS HD 4i cable plug connector (see 5.4.3.4.4.1) may be plugged into module A, module B, module C, or module D. A Mini SAS HD 8i cable plug connector (see 5.4.3.4.4.2) may be plugged into module A and module B, module B and module C, or module C and module D.

5.4.3.4.4.6 Mini SAS HD 4i connector pin assignments

Table 14 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.4.3.4.4.1) and Mini SAS HD 4i receptacle connectors (see 5.4.3.4.4.3) for controller applications using one, two, three, or four of the physical links.

Table 14 – Controller Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	B4	B4	B4	B4	Third
RX 0-	B5	B5	B5	B5	
RX 1+	N/C	A4	A4	A4	
RX 1-	N/C	A5	A5	A5	
SIDEBAND 7	A1	A1	A1	A1	Second
SIDEBAND 3	B1	B1	B1	B1	
SIDEBAND 4	C1	C1	C1	C1	
SIDEBAND 5	D1	D1	D1	D1	
RX 2+	N/C	N/C	B7	B7	Third
RX 2-	N/C	N/C	B8	B8	
RX 3+	N/C	N/C	N/C	A7	
RX 3-	N/C	N/C	N/C	A8	
TX 0+	D4	D4	D4	D4	Third
TX 0-	D5	D5	D5	D5	
TX 1+	N/C	C4	C4	C4	
TX 1-	N/C	C5	C5	C5	
SIDEBAND 0	A2	A2	A2	A2	Second
SIDEBAND 1	B2	B2	B2	B2	
SIDEBAND 2	C2	C2	C2	C2	
SIDEBAND 6	D2	D2	D2	D2	
TX 2+	N/C	N/C	D7	D7	Third
TX 2-	N/C	N/C	D8	D8	
TX 3+	N/C	N/C	N/C	C7	
TX 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

Key:

N/C = not connected

[a] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 15 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.4.3.4.4.1) and Mini SAS HD 4i receptacle connectors (see 5.4.3.4.4.3) for backplane applications using one, two, three, or four of the physical links.

Table 15 – Backplane Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	B4	B4	B4	B4	Third
RX 0-	B5	B5	B5	B5	
RX 1+	N/C	A4	A4	A4	
RX 1-	N/C	A5	A5	A5	
SIDEBAND 0	A1	A1	A1	A1	Second
SIDEBAND 1	B1	B1	B1	B1	
SIDEBAND 2	C1	C1	C1	C1	
SIDEBAND 6	D1	D1	D1	D1	
RX 2+	N/C	N/C	B7	B7	Third
RX 2-	N/C	N/C	B8	B8	
RX 3+	N/C	N/C	N/C	A7	
RX 3-	N/C	N/C	N/C	A8	
TX 0+	D4	D4	D4	D4	Third
TX 0-	D5	D5	D5	D5	
TX 1+	N/C	C4	C4	C4	
TX 1-	N/C	C5	C5	C5	
SIDEBAND 7	A2	A2	A2	A2	Second
SIDEBAND 3	B2	B2	B2	B2	
SIDEBAND 4	C2	C2	C2	C2	
SIDEBAND 5	D2	D2	D2	D2	
TX 2+	N/C	N/C	D7	D7	Third
TX 2-	N/C	N/C	D8	D8	
TX 3+	N/C	N/C	N/C	C7	
TX 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

Key:

N/C = not connected

[a] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.5 SAS external connectors

5.4.3.5.1 Mini SAS 4x connectors

5.4.3.5.1.1 Mini SAS 4x cable plug connector

The Mini SAS 4x cable plug connector and the MiniSAS 4x active plug connector are the free (plug) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086. The Mini SAS 4x cable plug connector should not be used for rates greater than 6 Gbit/s.

Figure 42 shows the Mini SAS 4x cable plug connector.

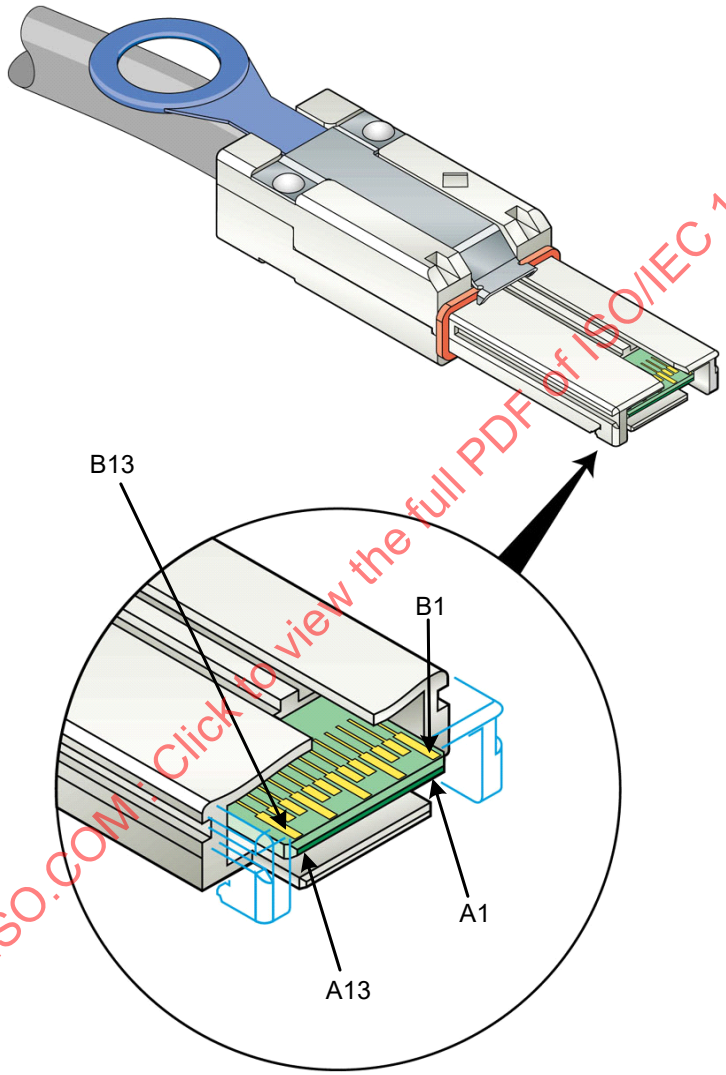


Figure 42 – Mini SAS 4x cable plug connector

If constructed with a pull tab as shown in figure 42, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 18 (see 5.4.3.5.1.3) and table 19 (see 5.4.3.5.1.3) define the pin assignments for the Mini SAS 4x cable plug connector.

Mini SAS 4x cable plug connectors shall include key slots to allow attachment to Mini SAS 4x receptacle connectors (see 5.4.3.5.1.2) with matching keys and key slots.

To ensure active cable assemblies are not intermateable with Mini SAS 4x receptacles that do not support active cable assemblies, differentiating keying shall be provided by having a blocking key on the plug connector in addition to the key slots. Table 16 defines the icons that shall be placed on or near Mini SAS 4x cable plug connectors and the key slot and key positions (see SFF-8088) that shall be used by Mini SAS 4x cable plug connectors.

Table 16 – Mini SAS 4x cable plug connector and Mini SAS 4x active cable plug connector icons, key slot positions, and key positions

End of a SAS external cable		Icon	Key slot positions	Key positions	Reference
Electrical compliance	**Attaches to**				
Untrained 1.5 Gbit/s and 3 Gbit/s [a]	Out or in [b]	Diamond and circle	2, 4, 6	none	Figure 43
	Out [c]	Diamond	2, 4	none	Figure 44
	In [d]	Circle	4, 6	none	Figure 45
Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [e]	Out or in [b]	Two diamonds and two circles	2, 4, 6	3	Figure 46
	Out [c]	Two diamonds	2, 4	3	Figure 47
	In [d]	Two circles	4, 6	3	Figure 48
	Out or in [b]	Two triangles, diamond, and circle	2, 4, 6	5	Figure 49 [f]
	Out [c]	Two triangles and diamond	2, 4	5	Figure 50 [f]
	In [d]	Two triangles and circle	4, 6	5	Figure 51 [f]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[b] Attaches to an end device, an enclosure out port, an enclosure in port, or an enclosure universal port.
[c] Attaches to an end device, an enclosure out port, or an enclosure universal port.
[d] Attaches to an end device, an enclosure in port, or an enclosure universal port.
[e] Complies with the TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[f] Mini SAS 4x active cable plug connector.

Figure 43 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 53, figure 56, and figure 59 in 5.4.3.5.1.2), an enclosure out port (see figure 54, figure 57, and figure 60 in 5.4.3.5.1.2), or an enclosure in port (see figure 55, figure 58, and figure 61 in 5.4.3.5.1.2).

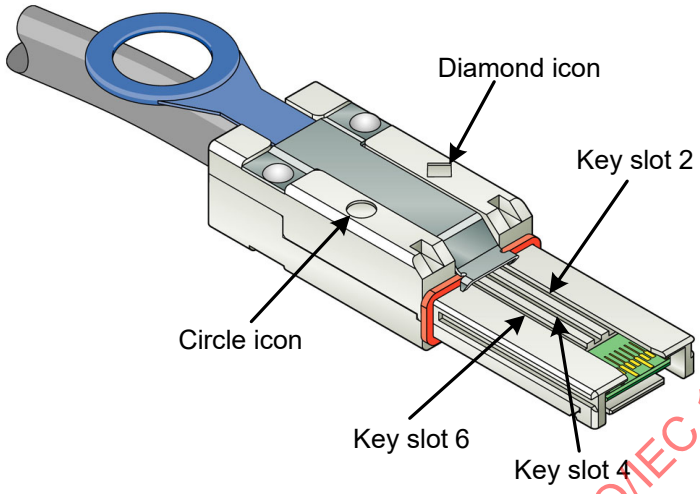


Figure 43 – Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 44 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 53, figure 56, and figure 59 in 5.4.3.5.1.2) or an enclosure out port (see figure 54, figure 57, and figure 60 in 5.4.3.5.1.2).

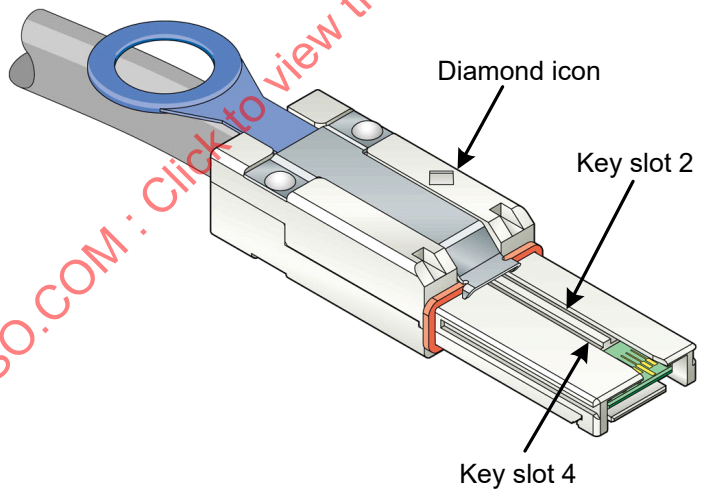


Figure 44 – Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port

Figure 45 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 53, figure 56, and figure 59 in 5.4.3.5.1.2) or an enclosure in port (see figure 55, figure 58, and figure 61 in 5.4.3.5.1.2).

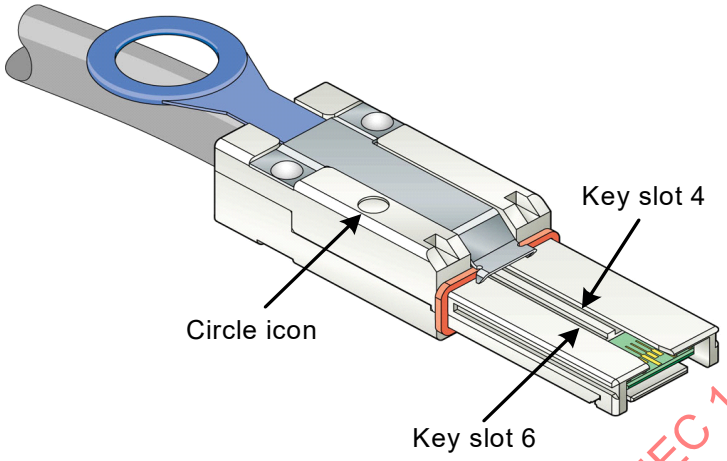


Figure 45 – Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure in port

Figure 46 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 56 and figure 59 in 5.4.3.5.1.2), an enclosure out port (see figure 57 and figure 60 in 5.4.3.5.1.2), or an enclosure in port (figure 58 and figure 61 in 5.4.3.5.1.2).

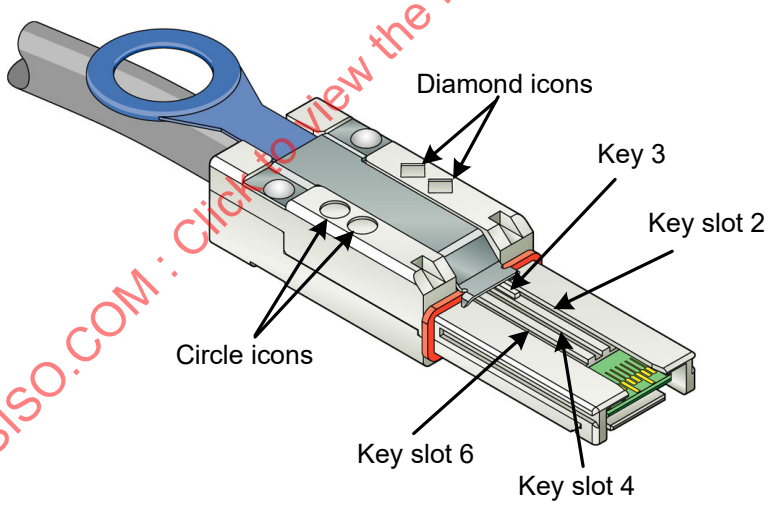


Figure 46 – Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 47 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 56 and figure 59 in 5.4.3.5.1.2) or an enclosure out port (see figure 57 and figure 60 in 5.4.3.5.1.2).

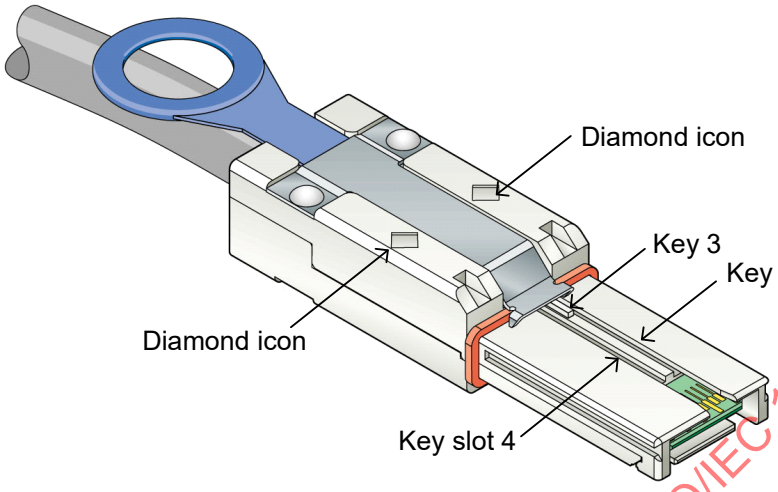


Figure 47 – Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port

Figure 48 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 56 and figure 59 in 5.4.3.5.1.2) or an enclosure in port (see figure 58 and figure 61 in 5.4.3.5.1.2).

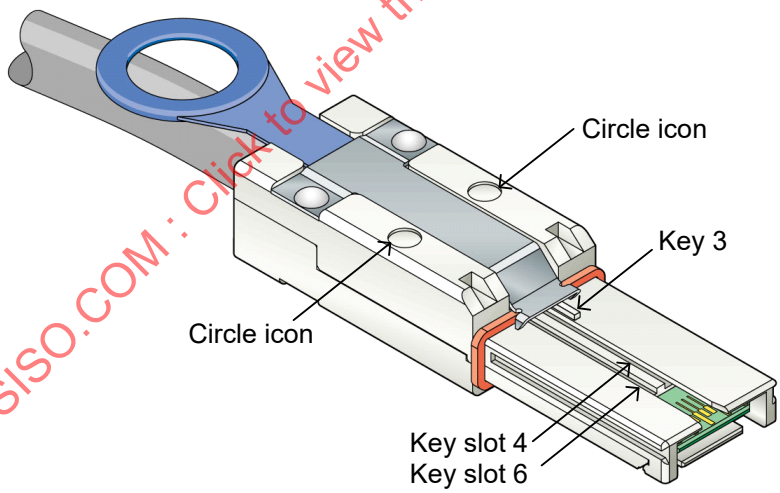


Figure 48 – Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure in port

Figure 49 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 59 in 5.4.3.5.1.2), an enclosure out port (see figure 60 in 5.4.3.5.1.2), or an enclosure in port (see figure 61 in 5.4.3.5.1.2).

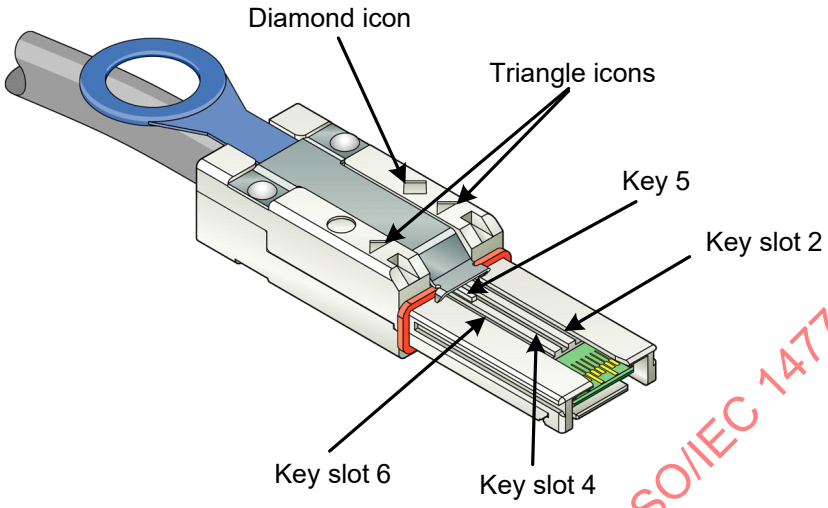


Figure 49 – Mini SAS 4x active cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 50 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 59 in 5.4.3.5.1.2) or enclosure out port (see figure 60 in 5.4.3.5.1.2).

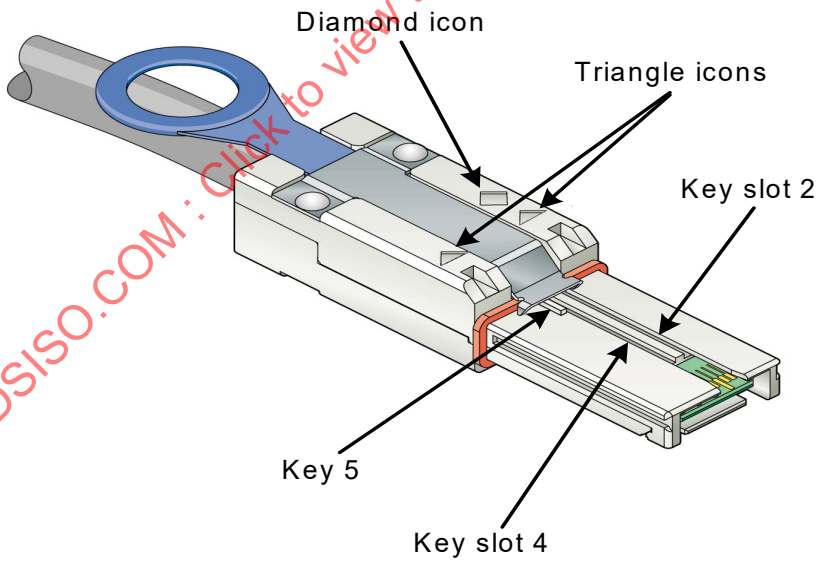


Figure 50 – Mini SAS 4x active cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port

Figure 51 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 59 in 5.4.3.5.1.2) or an enclosure in port (see figure 61 in 5.4.3.5.1.2).

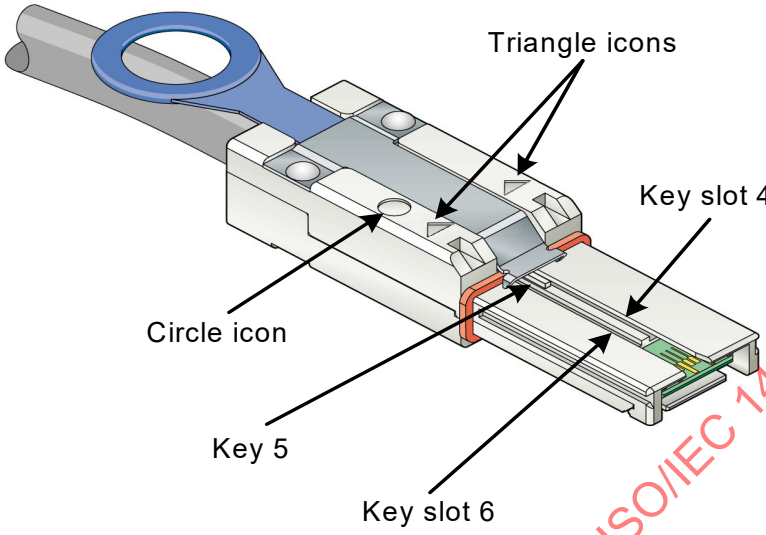


Figure 51 – Mini SAS 4x active cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure in port

5.4.3.5.1.2 Mini SAS 4x receptacle connector

The Mini SAS 4x receptacle connector is the fixed (receptacle) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086. The Mini SAS 4x receptacle connector should not be used for rates greater than 6 Gbit/s.

A Mini SAS 4x receptacle connector may be used by one or more SAS devices (e.g., one SAS device using physical links 0 and 3, another using physical link 1, and a third using physical link 2).

A Mini SAS 4x receptacle connector shall be used by no more than one expander device at a time, and all physical links shall be used by the same expander port (i.e., all the expander phys shall have the same routing attribute (e.g., subtractive or table) (see SPL-3)).

Figure 52 shows the Mini SAS 4x receptacle connector.

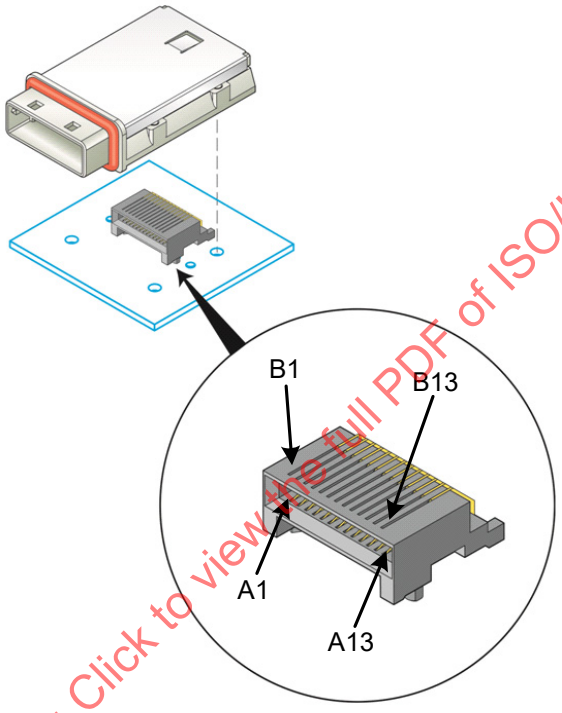


Figure 52 – Mini SAS 4x receptacle connector

Table 18 (see 5.4.3.5.1.3) and table 19 (see 5.4.3.5.1.3) define the pin assignments for the Mini SAS 4x receptacle connector.

Mini SAS 4x receptacle connectors and Mini SAS 4x active receptacle connectors shall include keys and key slots to prevent attachment to Mini SAS 4x cable plug connectors (see 5.4.3.5.1.1) without matching keys and key slots.

Table 17 defines the icons that shall be placed on or near Mini SAS 4x receptacle connectors and the key and key slot positions (see SFF-8088) that shall be used by Mini SAS 4x receptacle connectors.

Table 17 – Mini SAS 4x receptacle connector icons, key positions, and key slot positions

Electrical compliance	Use	Icons	Key position	Key slot position	Reference
Untrained 1.5 Gbit/s and 3 Gbit/s [a]	End device or enclosure universal port	Diamond and circle	4	none	Figure 53
	Enclosure out port	Diamond	2	none	Figure 54
	Enclosure in port	Circle	6	none	Figure 55
Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [b]	End device or enclosure universal port	Two diamonds and two circles	4	3	Figure 56
	Enclosure out port	Two diamonds	2	3	Figure 57
	Enclosure in port	Two circles	6	3	Figure 58
	End device or enclosure universal port	Two triangles, diamond, and circle	4	3, 5	Figure 59 [c]
	Enclosure out port	Two triangles and diamond	2	3, 5	Figure 60 [c]
	Enclosure in port	Two triangles and circle	6	3, 5	Figure 61 [c]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[b] Complies with the TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[c] Mini SAS 4x active receptacle.

Figure 53 shows the key on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 43, figure 44, and figure 45 (see 5.4.3.5.1.1) may be attached to this connector.

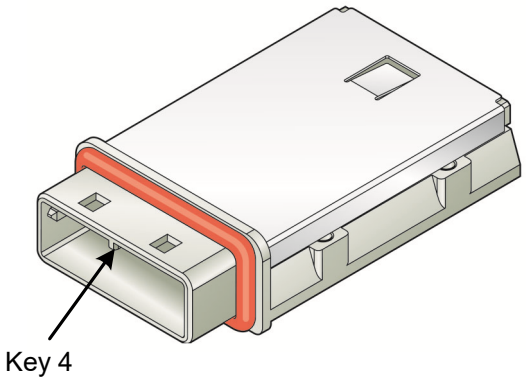


Figure 53 – Mini SAS 4x receptacle connector - end device or enclosure universal port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 54 shows the key on a Mini SAS 4x receptacle connector used by an enclosure out port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 43 and figure 44 (see 5.4.3.5.1.1) may be attached to this connector.

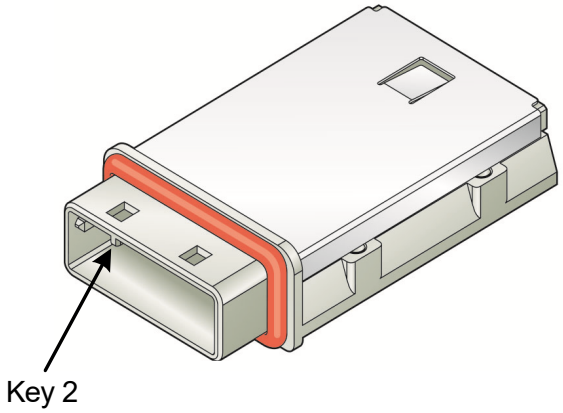


Figure 54 – Mini SAS 4x receptacle connector - enclosure out port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 55 shows the key on a Mini SAS 4x receptacle connector used by an enclosure in port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 43 and figure 45 (see 5.4.3.5.1.1) may be attached to this connector.

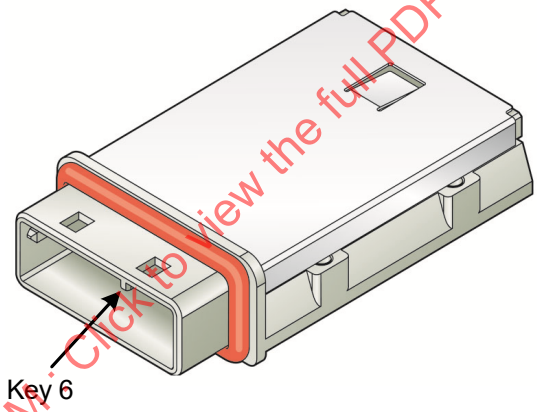


Figure 55 – Mini SAS 4x receptacle connector - enclosure in port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 56 shows the key and key slot on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 43, figure 44, figure 45, figure 46, figure 47, and figure 48 (see 5.4.3.5.1.1) may be attached to this connector.

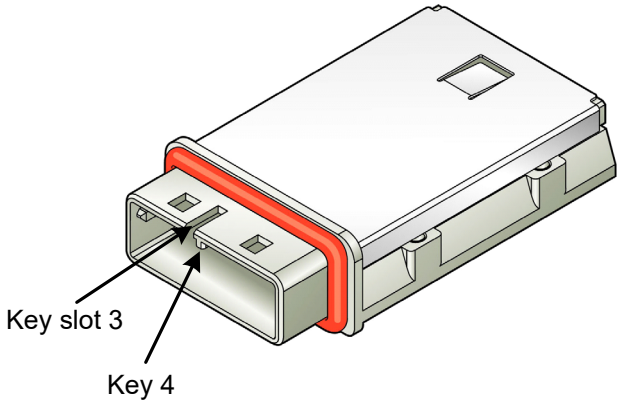


Figure 56 – Mini SAS 4x receptacle connector - end device or enclosure universal port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 57 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 43, figure 44, figure 46, and figure 47, (see 5.4.3.5.1.1) may be attached to this connector.

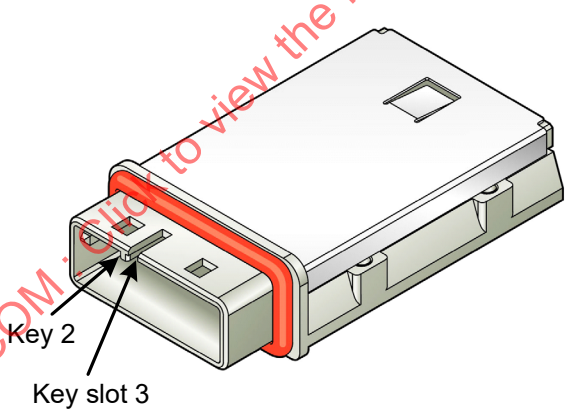


Figure 57 – Mini SAS 4x receptacle connector - enclosure out port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 58 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 43, figure 45, figure 46, and figure 48 (see 5.4.3.5.1.1) may be attached to this connector.

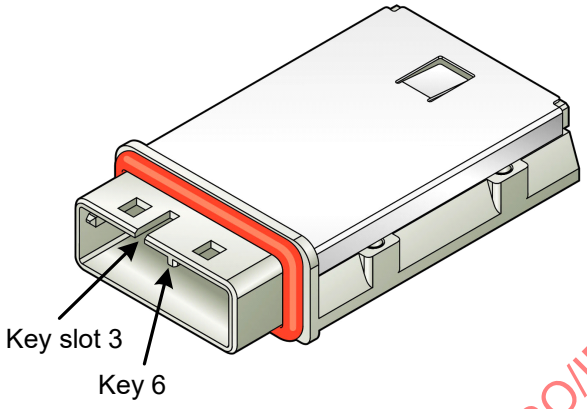


Figure 58 – Mini SAS 4x receptacle connector - enclosure in port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 59 shows an Mini SAS 4x active receptacle connector used by end devices or an enclosure universal port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 43, figure 44, figure 45, figure 46, figure 47, figure 48, figure 49, figure 50, and figure 51 (see 5.4.3.5.1.1) may be attached to this connector.

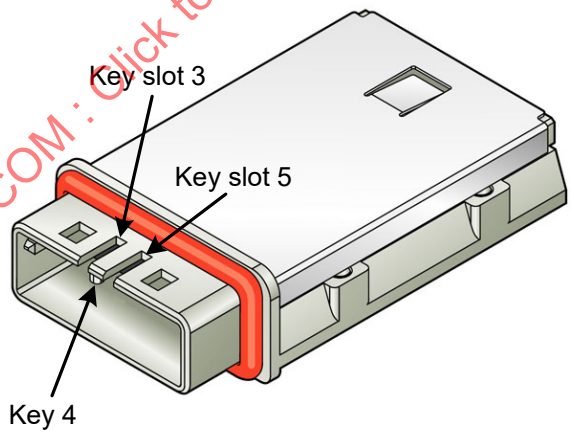


Figure 59 – Mini SAS 4x active receptacle connector - end device or enclosure universal port

Figure 60 shows an Mini SAS 4x active receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 43, figure 44, figure 46, figure 47, figure 49, and figure 50 (see 5.4.3.5.1.1) may be attached to this connector.

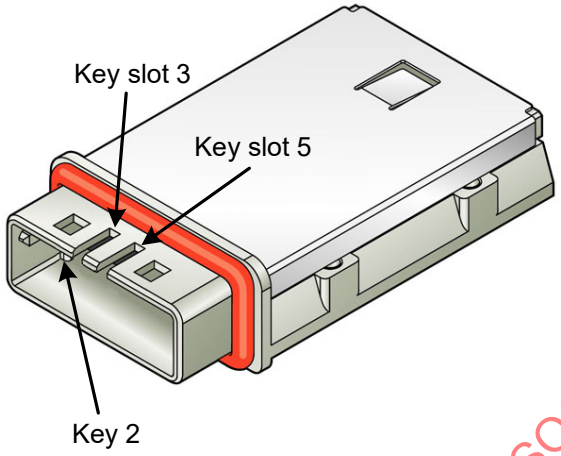


Figure 60 – Mini SAS 4x active receptacle connector - enclosure out port

Figure 61 shows an Mini SAS 4x active receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 43, figure 45, figure 46, figure 48, figure 49, and figure 51 (see 5.4.3.5.1.1) may be attached to this connector.

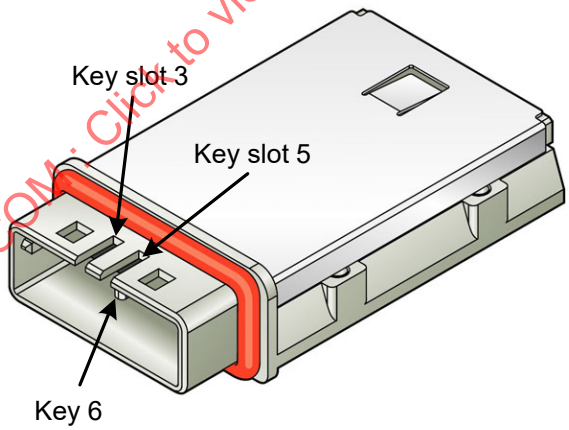


Figure 61 – Mini SAS 4x active receptacle connector - enclosure in port

5.4.3.5.1.3 Mini SAS 4x connector pin assignments

Table 18 defines the pin assignments for Mini SAS 4x cable plug connectors (see 5.4.3.5.1.1) and Mini SAS 4x receptacle connectors (see 5.4.3.5.1.2) for applications using one, two, three, or four of the physical links.

Table 18 – Mini SAS 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
RX 2+	N/C	N/C	A8	A8	
RX 2-	N/C	N/C	A9	A9	
RX 3+	N/C	N/C	N/C	A11	
RX 3-	N/C	N/C	N/C	A12	
TX 0+	B2	B2	B2	B2	
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
TX 2+	N/C	N/C	B8	B8	
TX 2-	N/C	N/C	B9	B9	
TX 3+	N/C	N/C	N/C	B11	
TX 3-	N/C	N/C	N/C	B12	
SIGNAL GROUND	A1, A4, A7, A10, A13 B1, B4, B7, B10, B13				First
CHASSIS GROUND	Housing				N/A

Key:

N/C = not connected.

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.4.3.5.1.4 Mini SAS 4x active connector pin assignments

Table 19 defines the pin assignments for Mini SAS 4x active cable plug connectors (see 5.4.3.5.1.1) and Mini SAS 4x active receptacle connectors (see 5.4.3.5.1.2) for implementations using one, two, three, or four of the physical links.

Table 19 – Mini SAS 4x active connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0+	A2	A2	A2	A2	Third
RX 0-	A3	A3	A3	A3	
RX 1+	N/C	A5	A5	A5	
RX 1-	N/C	A6	A6	A6	
RX 2+	N/C	N/C	A8	A8	
RX 2-	N/C	N/C	A9	A9	
RX 3+	N/C	N/C	N/C	A11	
RX 3-	N/C	N/C	N/C	A12	
TX 0+	B2	B2	B2	B2	
TX 0-	B3	B3	B3	B3	
TX 1+	N/C	B5	B5	B5	
TX 1-	N/C	B6	B6	B6	
TX 2+	N/C	N/C	B8	B8	
TX 2-	N/C	N/C	B9	B9	
TX 3+	N/C	N/C	N/C	B11	
TX 3-	N/C	N/C	N/C	B12	
SENSE [b]	B1				
V_{CC} [c]	B13				
SIGNAL GROUND	A1, A4, A7, A10, A13, B4, B7, B10				First
CHASSIS GROUND	Housing				

Key:

N/C = not connected

[a] The mating level indicates the physical dimension of the contact (see SFF-8086).
[b] Electrical characteristics are defined in 5.4.3.5.1.5.
[c] Electrical characteristics are defined in 5.4.3.5.1.5.

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.4.3.5.1.5 Mini SAS 4x active cable power requirements

Mini SAS 4x active cable assemblies may contain integrated circuitry (e.g., drivers, repeaters, or equalizers). To enable the operation of circuitry inside the Mini SAS 4x active cable assemblies, Mini SAS 4x active receptacle connectors provide power when connected to a Mini SAS 4x active cable assembly (see 5.4.4.2.2). Mini SAS 4x active receptacle connectors shall be intermateable with Mini SAS 4x passive cable assemblies. To be intermateable, Mini SAS 4x active receptacle connectors define a pin (i.e., SENSE (see table 19) (see 5.4.3.5.1.4)) to allow control of power. Power shall only be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x active cable assembly is present. Power shall not be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x passive cable assembly or no cable assembly is present. An example of a power supply logic circuitry design is shown in Annex H.

The voltage and current requirements for the power supplied to the Mini SAS 4x active cable receptacle enable support for Mini SAS 4x active cable assemblies with power consumption of up to 1 W per each end of the cable assembly. These requirements are defined in table 20.

Table 20 – Mini SAS 4x active cable supplied power requirements

Characteristic	Units	Minimum	Nominal	Maximum
Supply voltage	V	3.135 [a]	3.3	3.465 [b]
Supply current	mA			319.4 [c]
Current consumption	mA			288.6 [d]
Power consumption	mW			1 000 [d] [e]

[a] At the maximum supply current.
[b] The power supply shall not exceed this value at any current.
[c] The power supply shall deliver this amount of current at the minimum voltage of 3.135 V.
[d] Maximum consumption for each end of the active cable assembly at the maximum voltage of 3.465 V.
[e] This is a derived quantity obtained from: (maximum supply voltage) x (maximum current consumption).

The Mini SAS 4x active cable assembly shall provide a connection of the SENSE pin to ground through a 5 kΩ resistor with a relative tolerance of ±5 %.

The active cable power circuitry shall enable power to the Mini SAS 4x receptacle connector only when the presence of the sense resistor is detected and power shall be disabled if the SENSE pin is open (i.e., no Mini SAS 4x cable assembly plugged in) or shorted to ground (i.e., Mini SAS 4x passive cable plugged in).

The active cable power circuitry shall have protection against the connection of the V_{CC} pin to ground or excessive current loading.

To support hot plugging, the active cable power circuitry shall be able to detect the sense resistor and provide full current within 50 ms of active cable assembly connection.

The active cable assembly and Mini SAS active cable receptacle power pins (i.e., the V_{CC} pin and SENSE pin) shall be coupled to ground via bypass capacitors so that they possess low impedance to ground from 100 MHz to 1.5 times the fundamental frequency of the maximum baud rate supported by the attached transmitter device and the attached receiver device.

The power planes of the printed circuit board on the receptacle side shall be coupled to ground.

In implementations where the circuitry in the Mini SAS 4x active cable assembly requires voltages other than the provided 3.3 V, voltage regulators may be located within the Mini SAS 4x active cable assembly.

5.4.3.5.2 Mini SAS HD external connectors

5.4.3.5.2.1 Mini SAS HD 4x cable plug connector

The Mini SAS HD 4x cable plug connector is the free (plug) 36-circuit connector defined in SFF-8644.

Figure 62 shows the Mini SAS HD 4x cable plug connector.

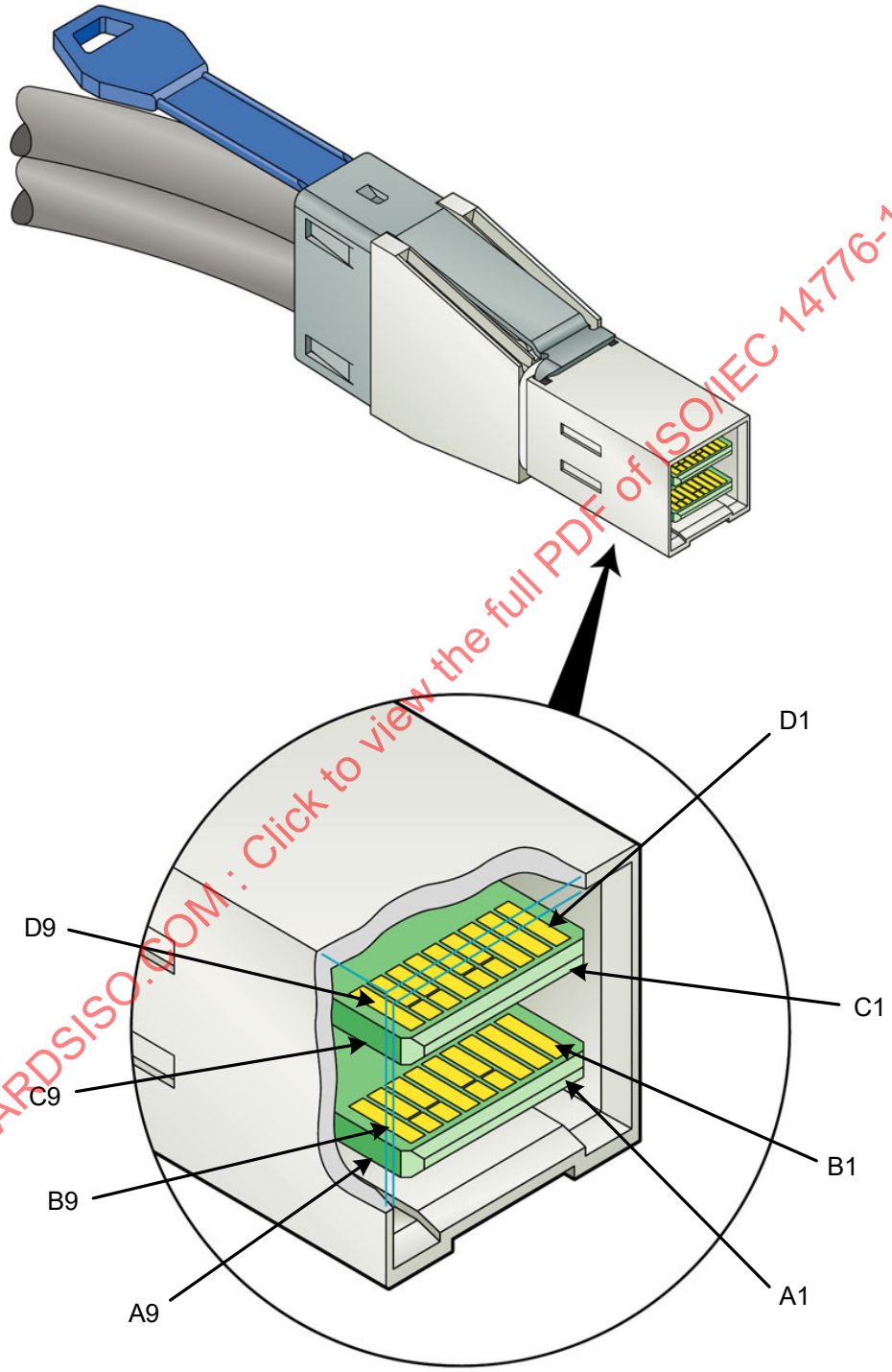


Figure 62 – Mini SAS HD 4x cable plug connector

If constructed with a pull tab as shown in figure 62, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 21 (see 5.4.3.5.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector.

The Mini SAS HD 4x cable plug connectors shall not include keying.

5.4.3.5.2.2 Mini SAS HD 8x cable plug connector

The Mini SAS HD 8i cable plug connector is the dual four lane cable plug (free) connector defined in SFF-8644. Figure 63 shows the Mini SAS HD 8x cable plug connector. This connector is a modular version of repeating Mini SAS HD 4x cable plug connectors (see 5.4.3.5.2.1). Module labeling is shown in figure 63. See figure 62 (see 5.4.3.5.2.1) for pin designations. Mini SAS HD 8x cable plug connectors shall not include keying.

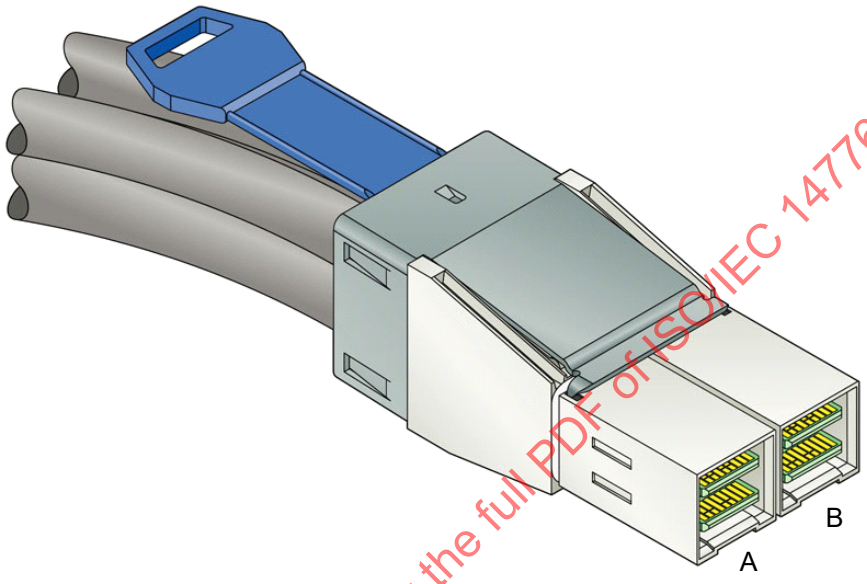


Figure 63 – Mini SAS HD 8x cable plug connector

Table 21 (see 5.4.3.5.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector (see 5.4.3.5.2.1). The pin assignments are repeated for each module of the Mini SAS 8x cable plug connector.

5.4.3.5.2.3 Mini SAS HD 4x receptacle connector

The Mini SAS HD 4x receptacle connector is the four-lane receptacle (fixed) connector defined in SFF-8644. Figure 64 shows the Mini SAS HD 4x receptacle connector.

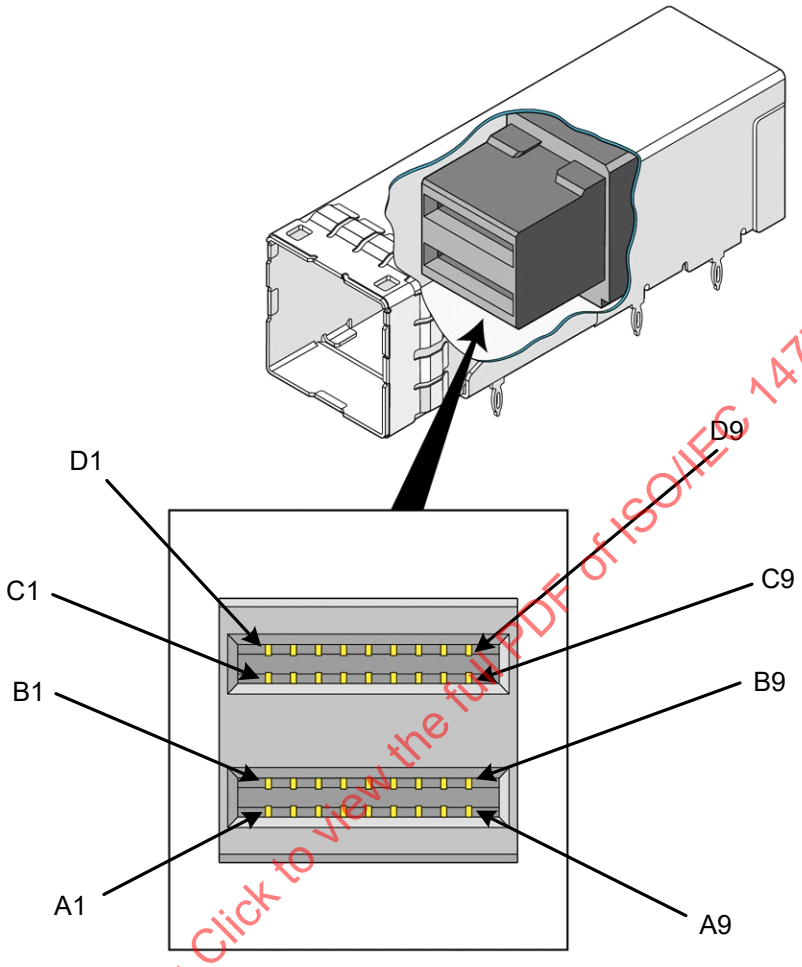


Figure 64 – Mini SAS HD 4x receptacle connector

Table 21 (see 5.4.3.5.2.6) defines the pin assignments for the Mini SAS HD 4x receptacle connector.

5.4.3.5.2.4 Mini SAS HD 8x receptacle connector

The Mini SAS HD 8x receptacle connector is a dual four-lane receptacle (fixed) connector defined in SFF-8644. Figure 65 shows the Mini SAS HD 8x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.4.3.5.2.3). Module labeling is shown in figure 65. See figure 64 (see 5.4.3.5.2.3) for pin designations.

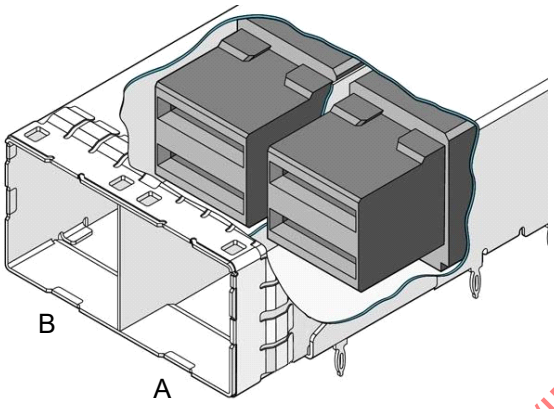


Figure 65 – Mini SAS HD 8x receptacle connector

Table 21 (see 5.4.3.5.2.6) defines the pin assignments for the Mini SAS HD 8x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.4.3.5.2.3). The Mini SAS HD 8x receptacle connector accepts one Mini SAS HD 8x plug connector (see 5.4.3.5.2.2) or one or two Mini SAS HD 4x plug connectors (see 5.4.3.5.2.1).

5.4.3.5.2.5 Mini SAS HD 16x receptacle connector

The Mini SAS HD 16x receptacle connector is a quad four-lane receptacle (fixed) connector defined in SFF-8644. Figure 66 shows the Mini SAS HD 16x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.4.3.5.2.3). Module labeling is shown in figure 66. See figure 64 (see 5.4.3.5.2.3) for pin designations.

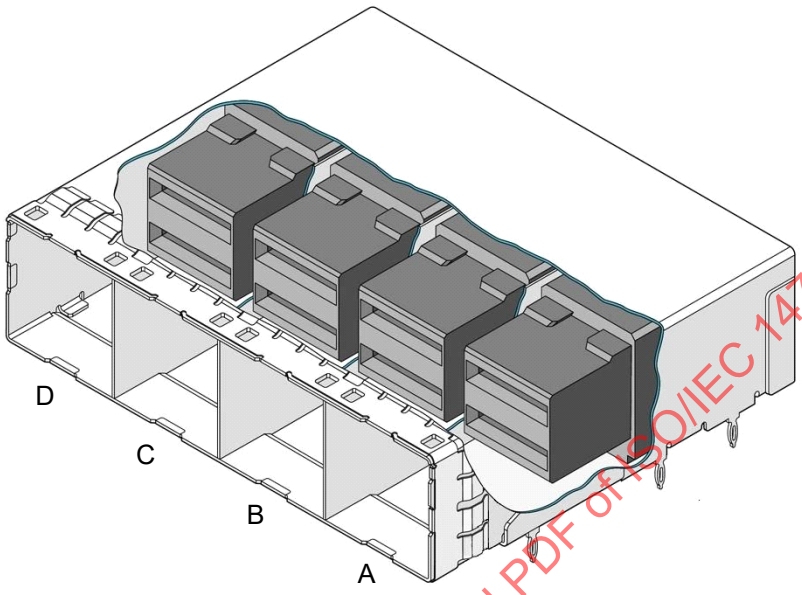


Figure 66 – Mini SAS HD 16x receptacle connector

Table 21 (see 5.4.3.5.2.6) defines the pin assignments for the Mini SAS HD 16x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.4.3.5.2.3). The Mini SAS HD 16x receptacle connector accepts:

a) one or two Mini SAS HD 8x cable plug connectors (see 5.4.3.5.2.2);
b) one, two, three, or four Mini SAS HD 4x cable plug connectors (see 5.4.3.5.2.1); or
c) a combination of one Mini SAS HD 8x cable plug connector (see 5.4.3.5.2.2) and one or two Mini SAS HD 4x cable plug connectors (see 5.4.3.5.2.1).

A Mini SAS HD 4x cable plug connector (see 5.4.3.5.2.1) may be plugged into module A, module B, module C, or module D. A Mini SAS HD 8x cable plug connectors (see 5.4.3.5.2.2) may be plugged into module A and module B, module B and module C, or module C and module D.

5.4.3.5.2.6 Mini SAS HD 4x connector pin assignments

Table 21 defines the pin assignments for Mini SAS HD 4x cable plug connectors (see 5.4.3.5.2.1) and Mini SAS HD 4x receptacle connectors (see 5.4.3.5.2.3) for controller applications using one, two, three, or four of the physical links.

Table 21 – Mini SAS HD 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly				Mating level [a]
	One	Two	Three	Four	
RX 0-	B5	B5	B5	B5	Third
RX 0+	B4	B4	B4	B4	
RX 1-	N/C	A5	A5	A5	
RX 1+	N/C	A4	A4	A4	
IntL [b]	A2	A2	A2	A2	Second
Reserved [b]	A1	A1	A1	A1	
ModPrsL [b]	B2	B2	B2	B2	
Vact [b]	B1	B1	B1	B1	
RX 2-	N/C	N/C	B8	B8	Third
RX 2+	N/C	N/C	B7	B7	
RX 3-	N/C	N/C	N/C	A8	
RX 3+	N/C	N/C	N/C	A7	
TX 0-	D5	D5	D5	D5	Third
TX 0+	D4	D4	D4	D4	
TX 1-	N/C	C5	C5	C5	
TX 1+	N/C	C4	C4	C4	
SDA [b]	C2	C2	C2	C2	Second
SCL [b]	C1	C1	C1	C1	
Vman [b]	D2	D2	D2	D2	
Vact [b]	D1	D1	D1	D1	
TX 2-	N/C	N/C	D8	D8	Third
TX 2+	N/C	N/C	D7	D7	
TX 3-	N/C	N/C	N/C	C8	
TX 3+	N/C	N/C	N/C	C7	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

Key:

N/C = not connected

[a] The mating level indicates the physical dimension of the contact (see SFF-8644).
[b] Table 22 (see 5.4.3.5.2.7) defines the connection requirements of this signal.

5.4.3.5.2.7 Mini SAS HD external connector management interface

Each 4x module shall include a two-wire serial management interface to:

a) monitor circuitry residing in the cable assembly;
b) control circuitry residing in the cable assembly; and
c) obtain physical characteristics of the cable encoded in a non-volatile storage device located in the cable assembly.

Table 22 defines the connection requirements of the management interface signals. The following connectors shall support the signals in table 22 in each 4x module:

a) Mini SAS HD 4x receptacle connectors (see 5.4.3.5.2.3);
b) Mini SAS HD 8x receptacle connectors (see 5.4.3.5.2.4);
c) Mini SAS HD 16x receptacle connectors (see 5.4.3.5.2.5);
d) Mini SAS HD 4x cable plug connectors (see 5.4.3.5.2.1); and
e) Mini SAS HD 8x cable plug connectors (see 5.4.3.5.2.2).

See SFF-8449 and SFF-8636 for a complete signal definition, management interface memory map, and timing diagrams for the two-wire interface.

Table 22 – Management interface connection requirements

Signal	Connection requirements [a]
IntL	**Active Low Module Interrupt**: This pin shall be connected to Vman (see SFF-8449) on the receptacle side of the management interface. The source of the interrupt may be identified using the two-wire serial management interface. If the cable assembly supports interrupts, then the cable assembly shall assert this pin to indicate an interrupt bit has been set to one in the management interface memory map. If a cable assembly does not support interrupts, then all interrupt bits in the cable management interface memory map shall be set to zero and the cable assembly shall negate this pin (e.g., all interrupt bits of a passive cable assembly may be programmed to a clear state and the IntL pin not connected on the cable plug side of the management interface).
ModPrsL	**Active Low Module Present**: On the cable plug side of the management interface, ModPrsL shall be connected directly to the signal ground pins specified in table 21 (see 5.4.3.5.2.6). ModPrsL shall be connected to Vman (see SFF-8449) on the receptacle side of the management interface to negate this signal when the plug is not fully mated to the receptacle.
Reserved	This pin shall be not connected on the receptacle side and cable plug side of the management interface.
SCL	**Two-wire interface clock**: The receptacle side of the management interface shall connect this signal to Vman (see SFF-8449).
SDA	**Two-wire interface data**: The receptacle side of the management interface shall connect this signal to Vman (see SFF-8449).
Vact	**Active cable power**: If the receptacle side of the management interface supports active cable assemblies, then it shall provide all non-management interface power to the cable assembly on the Vact pins. To support equal loading, both Vact pins shall be connected together on the receptacle side of the management interface. If the receptacle side of the management interface does not support active cable assemblies, then the Vact pins should be not connected.
Vman	**Management interface power**: The receptacle side of the management interface shall provide power on the Vman pin to enable the management interface circuitry of the cable. Power may be removed to reset the management circuitry in the cable assembly.

[a] Electrical characteristics are defined in SFF-8449.

5.4.3.5.2.8 Mini SAS HD external connector memory map

SFF-8636 defines the Mini SAS HD external connector management interface memory map. The Mini SAS HD external cable assembly shall support the following management interface memory map registers:

a) supported SAS baud rate;
b) vendor name;
c) vendor part number;
d) vendor revision;
e) copper cable attenuation;
f) power class;
g) minimum operating voltage;
h) transmitter technology;
i) cable width; and
j) propagation delay.

5.4.3.5.3 QSFP+ connectors

5.4.3.5.3.1 QSFP+ cable plug

The QSFP+ cable plug connector is the free (plug) 38-circuit connector defined in SFF-8685. Figure 67 shows the QSFP+ cable plug connector.

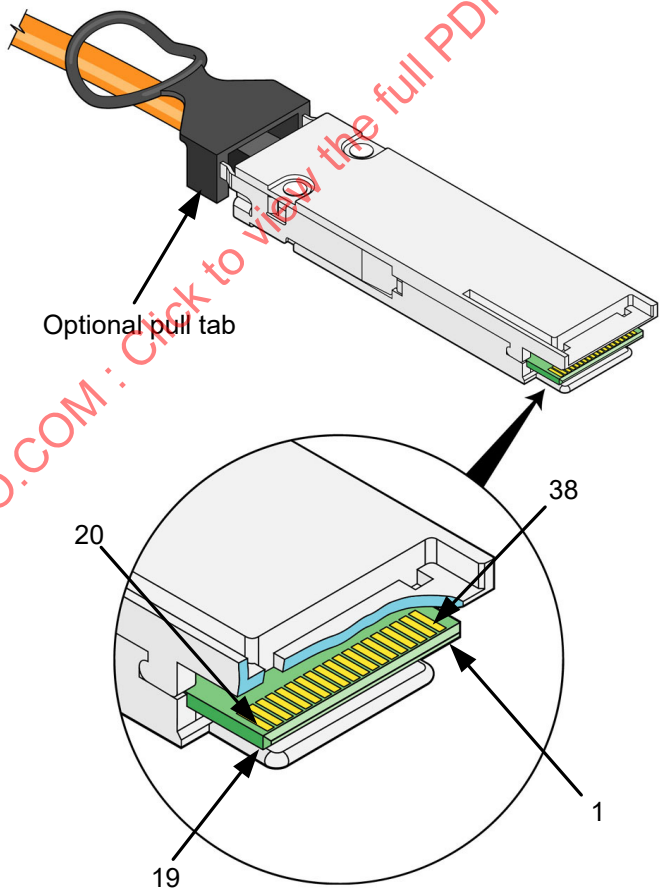


Figure 67 – QSFP+ cable plug connector

Table 23 (see 5.4.3.5.3.3) defines the pin assignments for the QSFP+ cable plug connector.

The QSFP+ cable plug connectors shall not include keying.

5.4.3.5.3.2 QSFP+ receptacle

The QSFP+ receptacle connector is the fixed (receptacle) 38-circuit connector defined in SFF-8685. Figure 68 shows the QSFP+ receptacle connector.

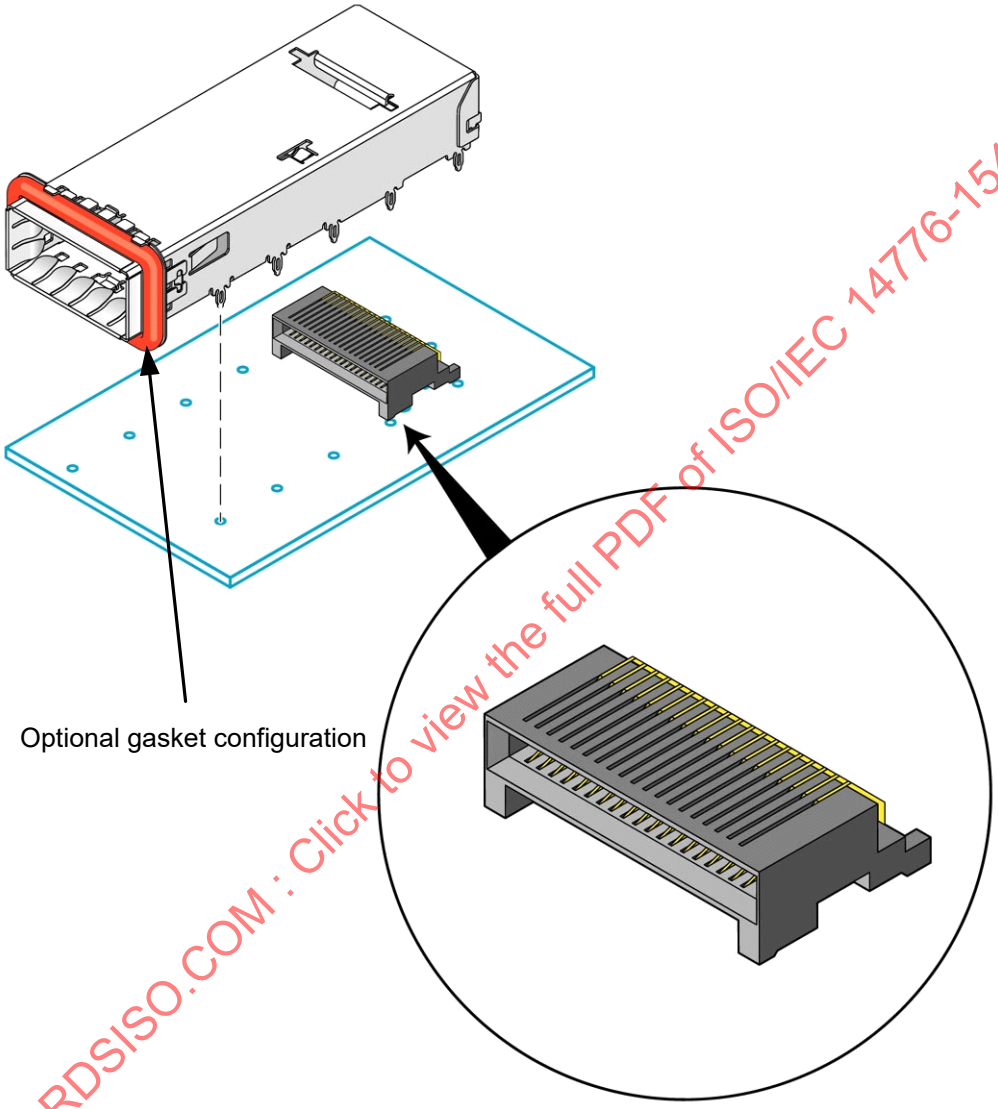


Figure 68 – QSFP+ receptacle connector

Table 23 (see 5.4.3.5.3.3) defines the pin assignments for the QSFP+ receptacle connector.

The QSFP+ receptacle connectors shall not include keying.

5.4.3.5.3.3 QSFP+ connector pin assignments

Table 23 defines the pin assignments for QSFP+ connectors (see 5.4.3.5.3.1 and 5.4.3.5.3.2). Specific pins are used to provide managed cable communication and power to the cable assembly.

Table 23 – QSFP+ connector pin assignments (part 1 of 2)

Pin	Signal	Description	Mating level [a]
1	GND [b]	Ground	First
2	Tx2n	Transmitter inverted data input	Third
3	Tx2p	Transmitter non-inverted data input	Third
4	GND [b]	Ground	First
5	Tx4n	Transmitter inverted data input	Third
6	Tx4p	Transmitter non-inverted data input	Third
7	GND [b]	Ground	First
8	ModSelL	Module select	Third
9	ResetL	Module reset	Third
10	Vcc Rx [c]	+3.3 V power supply receiver	Second
11	SCL	two-wire serial interface clock	Third
12	SDA	two-wire serial interface data	Third
13	GND [b]	Ground	First
14	Rx3p	Receiver non-inverted data output	Third
15	Rx3n	Receiver inverted data output	Third
16	GND [b]	Ground	First
17	Rx1p	Receiver non-inverted data output	Third
18	Rx1n	Receiver inverted data output	Third
19	GND [b]	Ground	First
20	GND [b]	Ground	First
21	Rx2n	Receiver inverted data output	Third
22	Rx2p	Receiver non-inverted data output	Third
23	GND [b]	Ground	First
24	Rx4n	Receiver inverted data output	Third
25	Rx4p	Receiver non-inverted data output	Third
26	GND [b]	Ground	First
27	ModPrsL	Module present	Third
28	IntL	Interrupt	Third

[a] The mating level indicates the physical dimension of the contact. See SFF-8685.
[b] GND is the symbol for signal ground and power ground for QSFP+. Signal ground and power ground are common within the QSFP+ cable connector and all voltages are referenced to this ground unless otherwise specified. Signal ground and power ground shall be connected directly to the host board signal ground.
[c] Power shall be applied concurrently to Vcc Rx, Vcc1, and Vcc Tx. Within the QSFP+ cable connector, Vcc Rx, Vcc1, and Vcc Tx may be connected in any combination.

Table 23 – QSFP+ connector pin assignments (part 2 of 2)

Pin	Signal	Description	Mating level [a]
29	Vcc Tx [c]	+3.3 V power supply transmitter	Second
30	Vcc1 [c]	+3.3 V power supply	Second
31	LPMode	Low power mode	Third
32	GND [b]	Ground	First
33	Tx3p	Transmitter non-inverted data input	Third
34	Tx3n	Transmitter inverted data input	Third
35	GND [b]	Ground	First
36	Tx1p	Transmitter non-inverted data input	Third
37	Tx1n	Transmitter inverted data input	Third
38	GND [b]	Ground	First

[a] The mating level indicates the physical dimension of the contact. See SFF-8685.
[b] GND is the symbol for signal ground and power ground for QSFP+. Signal ground and power ground are common within the QSFP+ cable connector and all voltages are referenced to this ground unless otherwise specified. Signal ground and power ground shall be connected directly to the host board signal ground.
[c] Power shall be applied concurrently to Vcc Rx, Vcc1, and Vcc Tx. Within the QSFP+ cable connector, Vcc Rx, Vcc1, and Vcc Tx may be connected in any combination.

5.4.3.5.3.4 QSFP+ memory map

The memory map for QSFP+ is used for identification information, cable characteristics, control functions, and digital monitoring. The two-wire serial interface is required for all QSFP+ devices. SFF-8636 defines the supported SAS baud rate codes. See SFF-8636 for register map details and the operation of the two-wire serial interface.

5.4.4 Cable assemblies

5.4.4.1 SAS internal cable assemblies

5.4.4.1.1 SAS Drive cable assemblies

A SAS Drive cable assembly is either:

a) a single-port SAS Drive cable assembly;
b) a dual-port SAS Drive cable assembly; or
c) a MultiLink SAS Drive cable assembly.

A SAS single-port Drive cable assembly or SAS dual-port Drive cable assembly has:

a) a SAS Drive cable receptacle connector (see 5.4.3.4.1.2) on the SAS target device end; and
b) a SATA signal cable receptacle connector (see SATA) on the SAS initiator device or expander device end (see SPL-3).

A SAS MultiLink Drive cable assembly has:

a) a SAS MultiLink Drive cable receptacle connector (see 5.4.3.4.1.2) on the SAS target device end; and
b) a SATA signal cable receptacle connector (see SATA) on the SAS initiator device or expander device end (see SPL-3).

The power, READY LED, and POWER DISABLE signal connection is vendor specific.

A SAS initiator device shall use a SATA host plug connector (see SATA) for connection to a SAS Drive cable assembly. The signal assignment for the SAS initiator device or expander device (see SPL-3) with this connector shall be the same as that defined for a SATA host (see SATA).

Figure 69 shows the Single-port SAS Drive cable assembly.

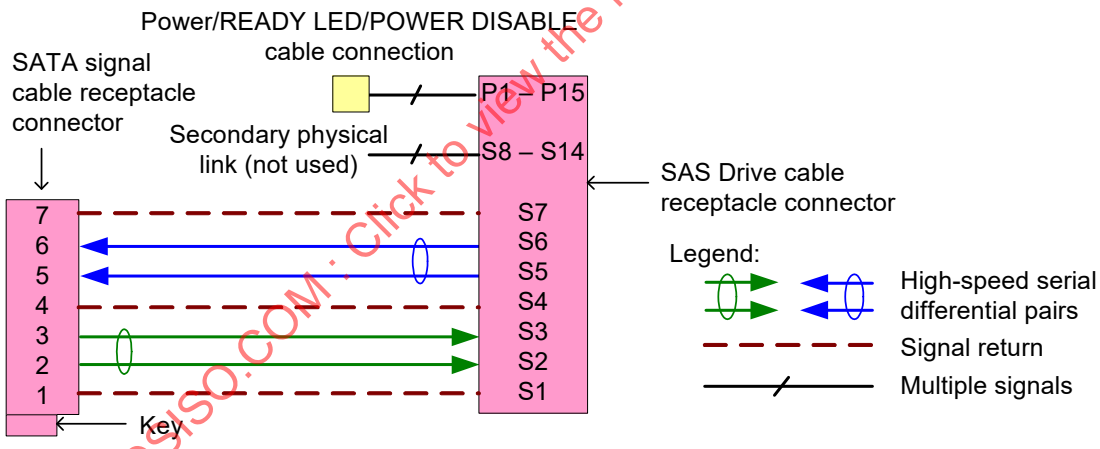


Figure 69 – Single-port SAS Drive cable assembly

Figure 70 shows the Dual-port SAS Drive cable assembly.

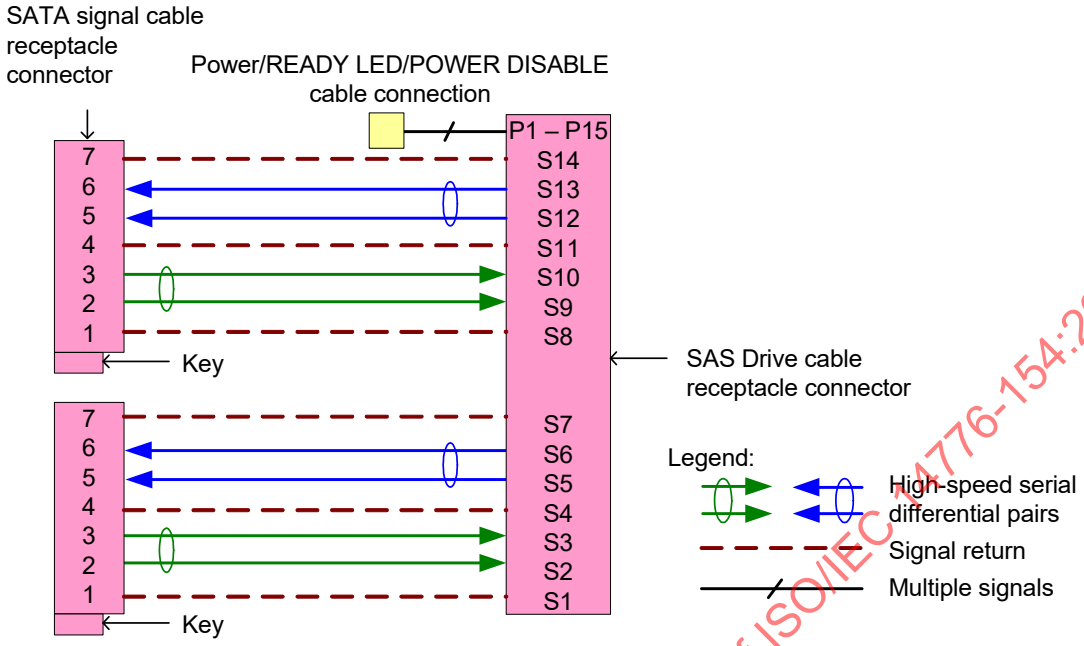


Figure 70 – Dual-port SAS Drive cable assembly

Figure 71 shows the MultiLink SAS Drive cable assembly.

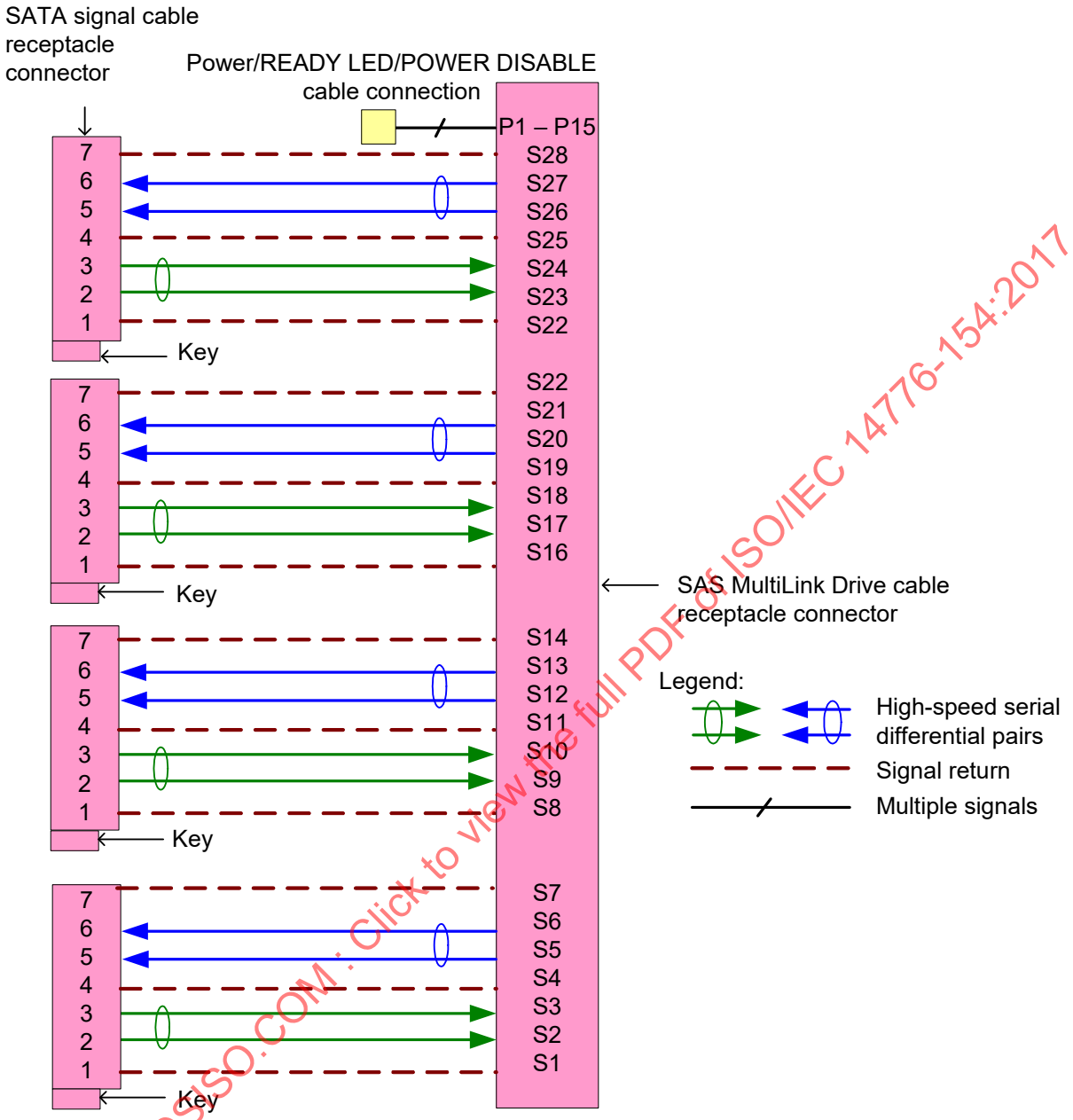


Figure 71 – MultiLink SAS Drive cable assembly

5.4.4.1.2 SAS internal symmetric cable assemblies

5.4.4.1.2.1 SAS internal symmetric cable assemblies overview

A SAS internal symmetric cable assembly has:

a) a SAS 4i cable receptacle connector (see 5.4.3.4.2.1) on each end (see 5.4.4.1.2.2);
b) a Mini SAS 4i cable plug connector (see 5.4.3.4.3.1) on each end (see 5.4.4.1.2.3);
c) a Mini SAS HD 4i cable plug connector on each end (see 5.4.4.1.2.4);
d) a Mini SAS HD 8i cable plug connector on each end (see 5.4.4.1.2.5);
e) a SAS 4i cable receptacle connector on one end and a Mini SAS 4i cable plug connector on the other end, with vendor-specific sidebands (see 5.4.4.1.2.5);
f) a SAS 4i cable receptacle connector on the controller end and a Mini SAS 4i cable plug connector on the backplane end, with sidebands supporting SGPIO (see 5.4.4.1.2.7);

g) a Mini SAS 4i cable plug connector on the controller end and a SAS 4i cable receptacle connector on the backplane end, with sidebands supporting SGPIO (see 5.4.4.1.2.8); or
h) a Mini SAS 4i cable plug connector on one end and a Mini SAS HD 4i cable plug connector on the other end (see 5.4.4.1.2.9).

In a SAS internal symmetric cable assembly, the TX signals on one end shall be connected to RX signals on the other end (e.g., a TX+ of one connector shall connect to an RX+ of the other connector). SAS internal symmetric cable assemblies should be labeled to indicate how many physical links are included (e.g., 1X, 2X, 3X, and 4X on each connector's housing). A SAS internal cable with a SAS 4i cable receptacle on either end should not be used for rates greater than 3 Gbit/s.

5.4.4.1.2.2 SAS internal symmetric cable assembly - SAS 4i

Figure 72 shows the SAS internal symmetric cable assembly with SAS 4i cable receptacle connectors at each end.

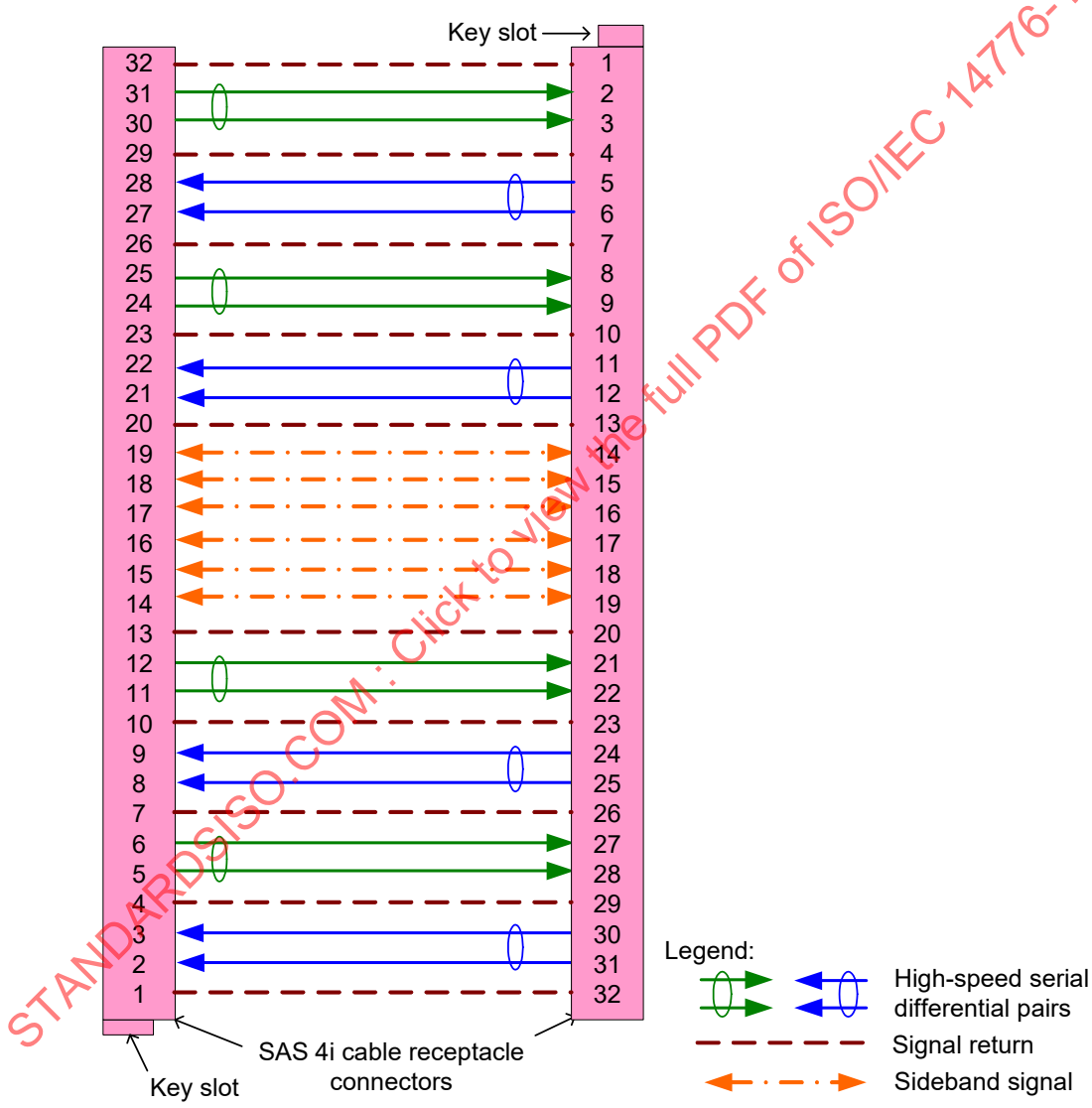


Figure 72 – SAS internal symmetric cable assembly - SAS 4i

In addition to the signal return connections shown in figure 72, one or more of the signal returns may be connected together in this cable assembly.

For controller-to-backplane applications, this cable assembly may support one to four physical links. SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, this cable assembly shall support all four physical links and the controllers should use all four physical links, because one controller's physical links 0 and 1 are attached the other controller's physical links 3 and 2, respectively. If both controllers use one or two physical links starting with physical links 0, communication is not possible. If both controllers use physical links 0, 1, and 2, then only communication over physical links 1 and 2 is possible. SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND5 of the other controller).

5.4.4.1.2.3 SAS internal symmetric cable assembly - Mini SAS 4i

Figure 73 shows the SAS internal cable assembly with Mini SAS 4i cable plug connectors at each end.

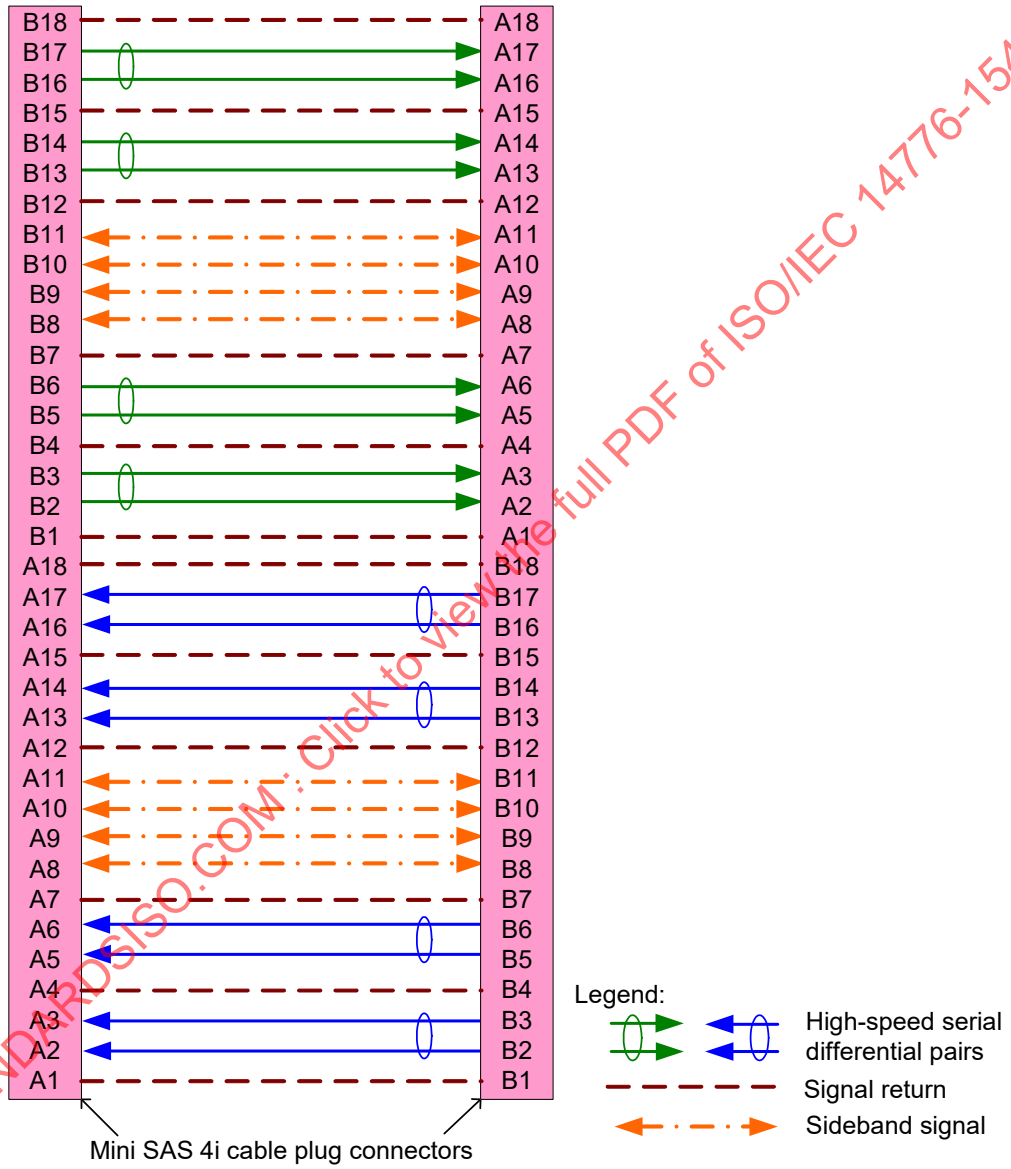


Figure 73 – SAS internal symmetric cable assembly - Mini SAS 4i

In addition to the signal return connections shown in figure 73, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.2.4 SAS internal symmetric cable assembly - Mini SAS HD 4i

Figure 74 shows the SAS internal cable assembly with Mini SAS HD 4i cable plug connectors at each end.

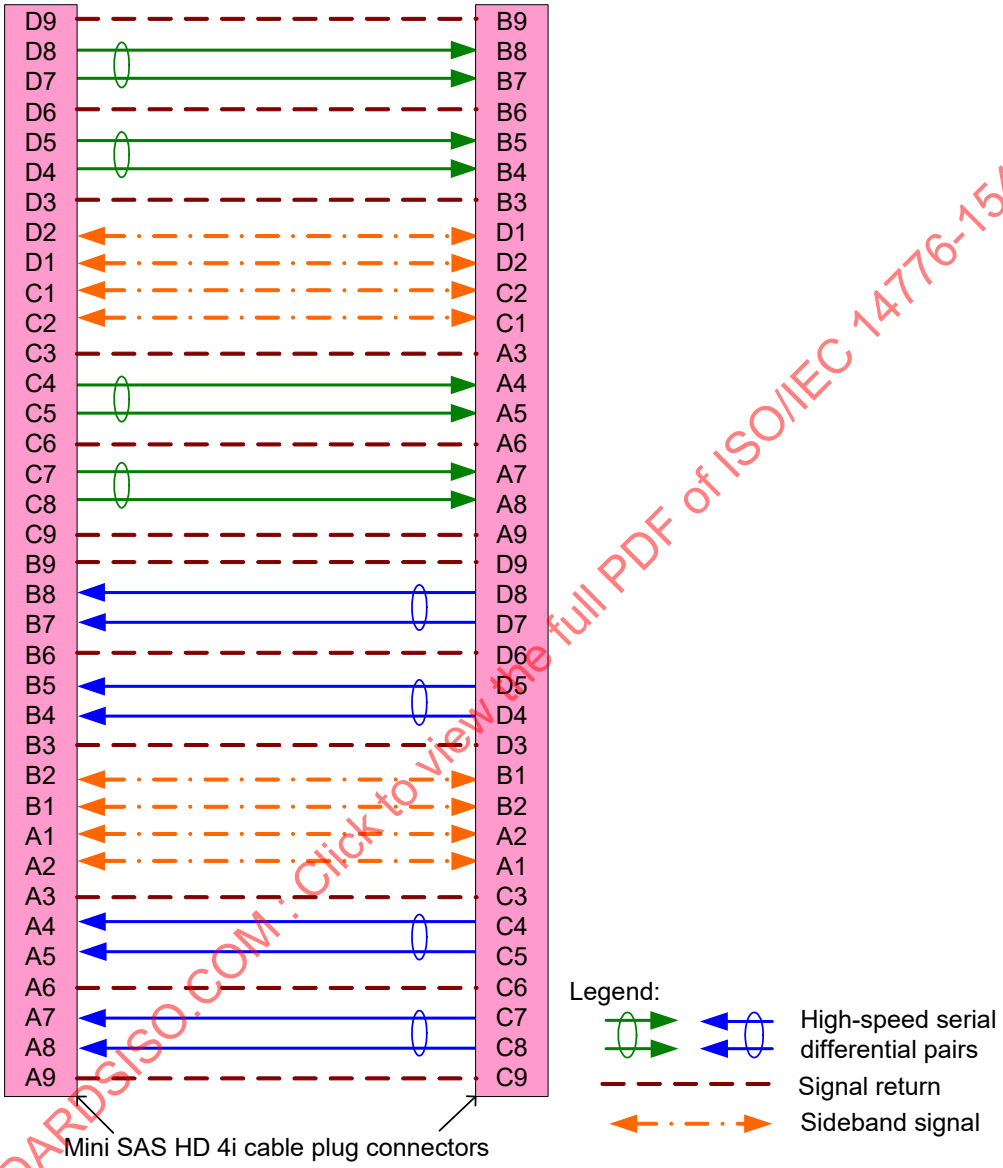


Figure 74 – SAS internal symmetric cable assembly - Mini SAS HD 4i

In addition to the signal return connections shown in figure 74, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.2.5 SAS internal symmetric cable assembly - Mini SAS HD 8i

Figure 75 shows the SAS internal cable assembly with Mini SAS HD 8i cable plug connectors at each end.

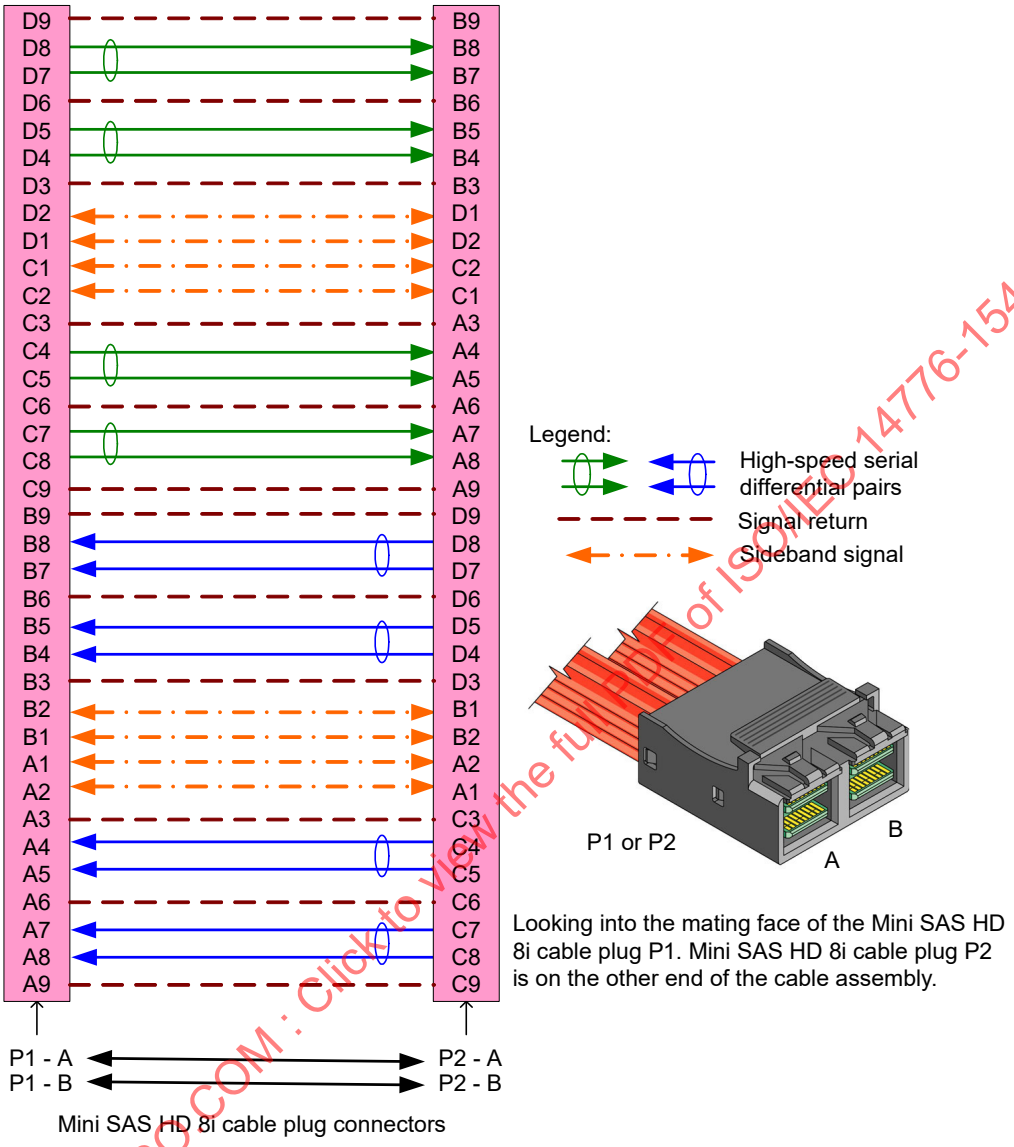


Figure 75 – SAS internal symmetric cable assembly - Mini SAS HD 8i

In addition to the signal return connections shown in figure 75, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.4.3.4.4.6 for connector module pin assignments.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.2.6 SAS internal symmetric cable assembly - SAS 4i to Mini SAS 4i with vendor-specific sidebands

Figure 76 shows the SAS internal symmetric cable assembly with a SAS 4i cable receptacle connector at one end and a Mini SAS 4i cable plug connector at the other end, with vendor-specific sidebands.

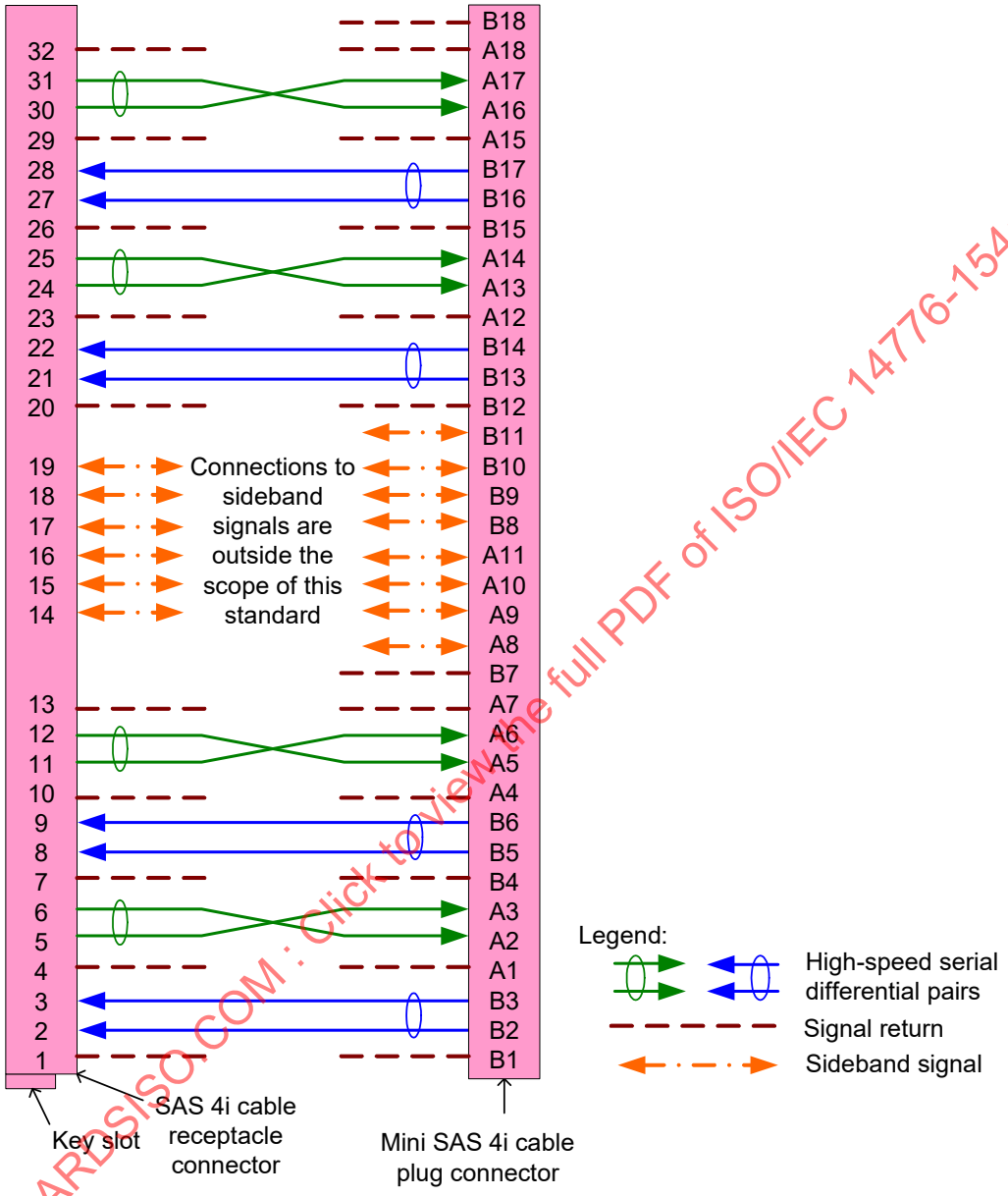


Figure 76 – SAS internal symmetric cable assembly - SAS 4i to Mini SAS 4i with vendor-specific sideband signals

The cable assembly shown in figure 76 may require different SIDEBAND signal routing based on whether the controller or backplane is using the SAS 4i connector.

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

For controller-to-backplane applications with the SAS 4i cable receptacle connector on the controller end, this cable assembly may support one to four physical links.

For controller-to-controller applications, this cable assembly may support one to four physical links.

For controller-to-backplane applications with the Mini SAS 4i cable receptacle connector on the controller end, this cable assembly shall support all four physical links and the controller should use all four physical links, because the controller's physical links 0, 1, 2, and 3 are attached to the backplane's physical links 3, 2, 1, and 0, respectively. If both the controller and the backplane use one or two physical links starting with physical links 0, communication is not possible. If both the controller and the backplane use physical links 0, 1, and 2, then only communication over physical links 1 and 2 is possible.

5.4.4.1.2.7 SAS internal symmetric cable assembly - SAS 4i controller to Mini SAS 4i backplane with SGPIO

Figure 77 shows the SAS internal symmetric cable assembly with a SAS 4i cable receptacle connector at the controller end and a Mini SAS 4i cable plug connector at the backplane end, with sidebands connected to support SGPIO (see SFF-8485).

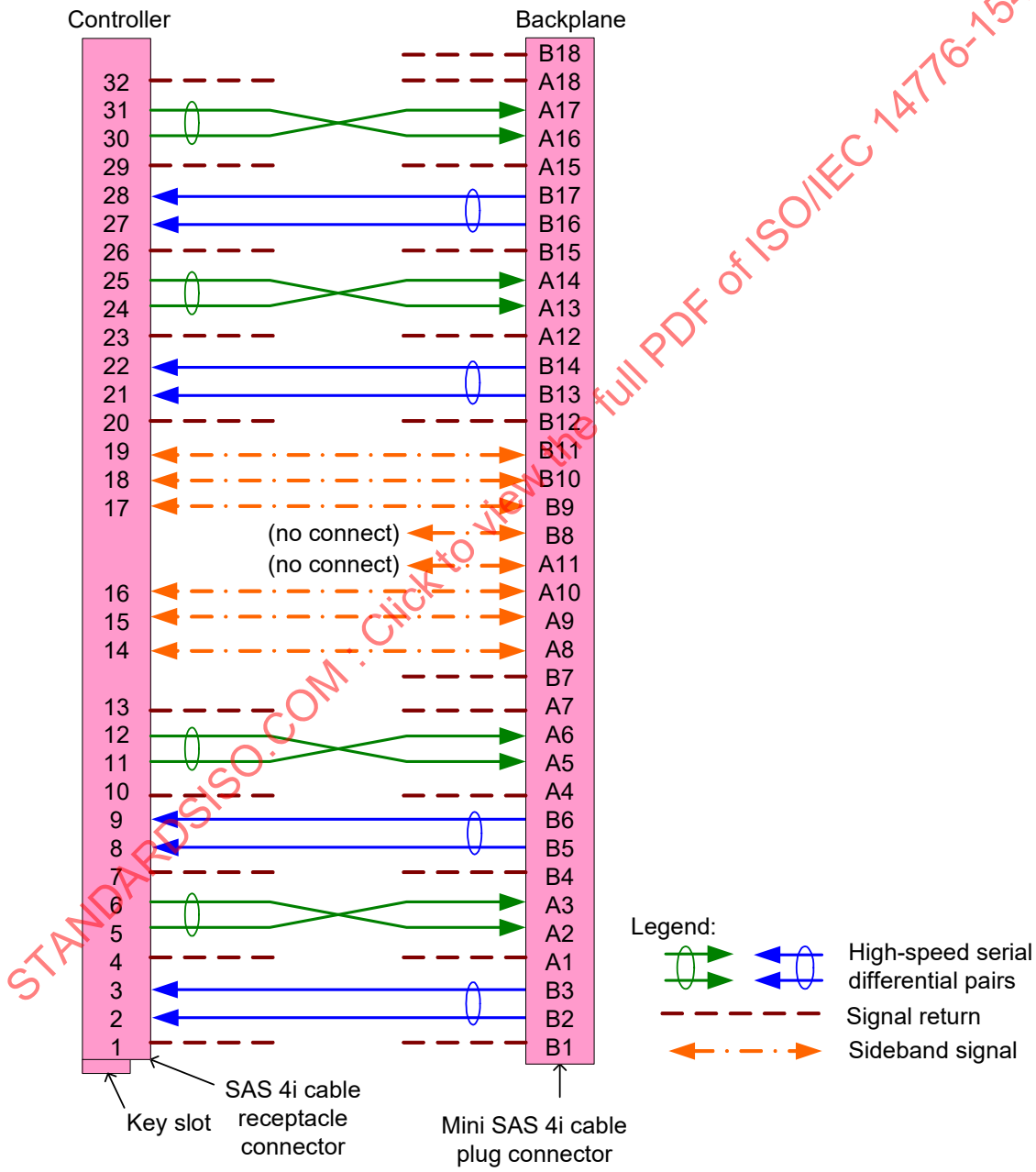


Figure 77 – SAS internal symmetric cable assembly - SAS 4i controller to Mini SAS 4i backplane with SGPIO connections

Each signal return on one end of the cable assembly shown in figure 77 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

5.4.4.1.2.8 SAS internal symmetric cable assembly - Mini SAS 4i controller to SAS 4i backplane with SGPIO

Figure 78 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable receptacle connector at the controller end and a SAS 4i cable plug connector at the backplane end, with sidebands connected to support SGPIO (see SFF-8485).

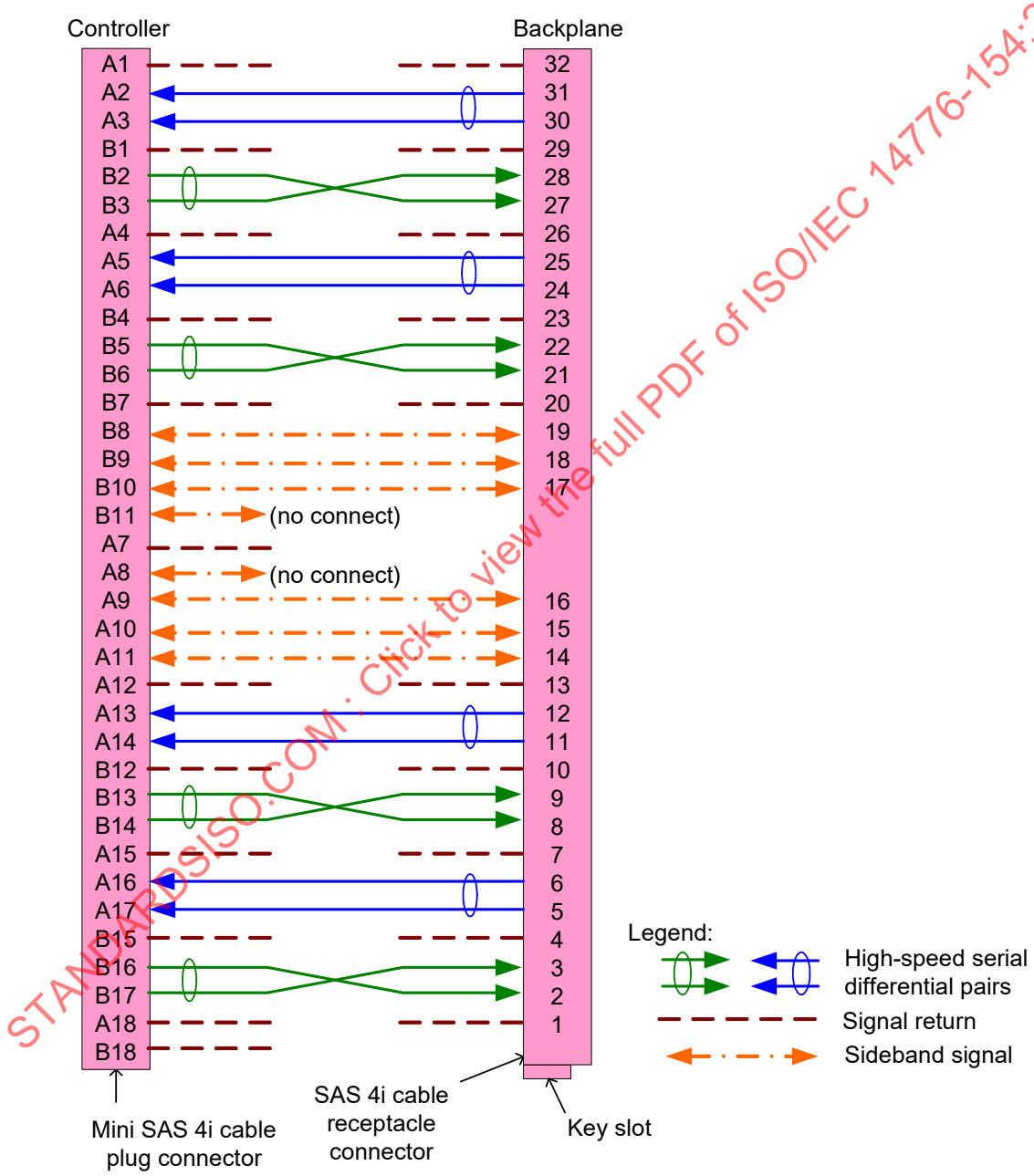


Figure 78 – SAS internal symmetric cable assembly - Mini SAS 4i controller to SAS 4i backplane with SGPIO connections

Each signal return on one end of the cable assembly shown in figure 78 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

5.4.4.1.2.9 SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

Figure 79 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable plug connector at one end and a Mini SAS HD 4i cable plug connector at the other end.

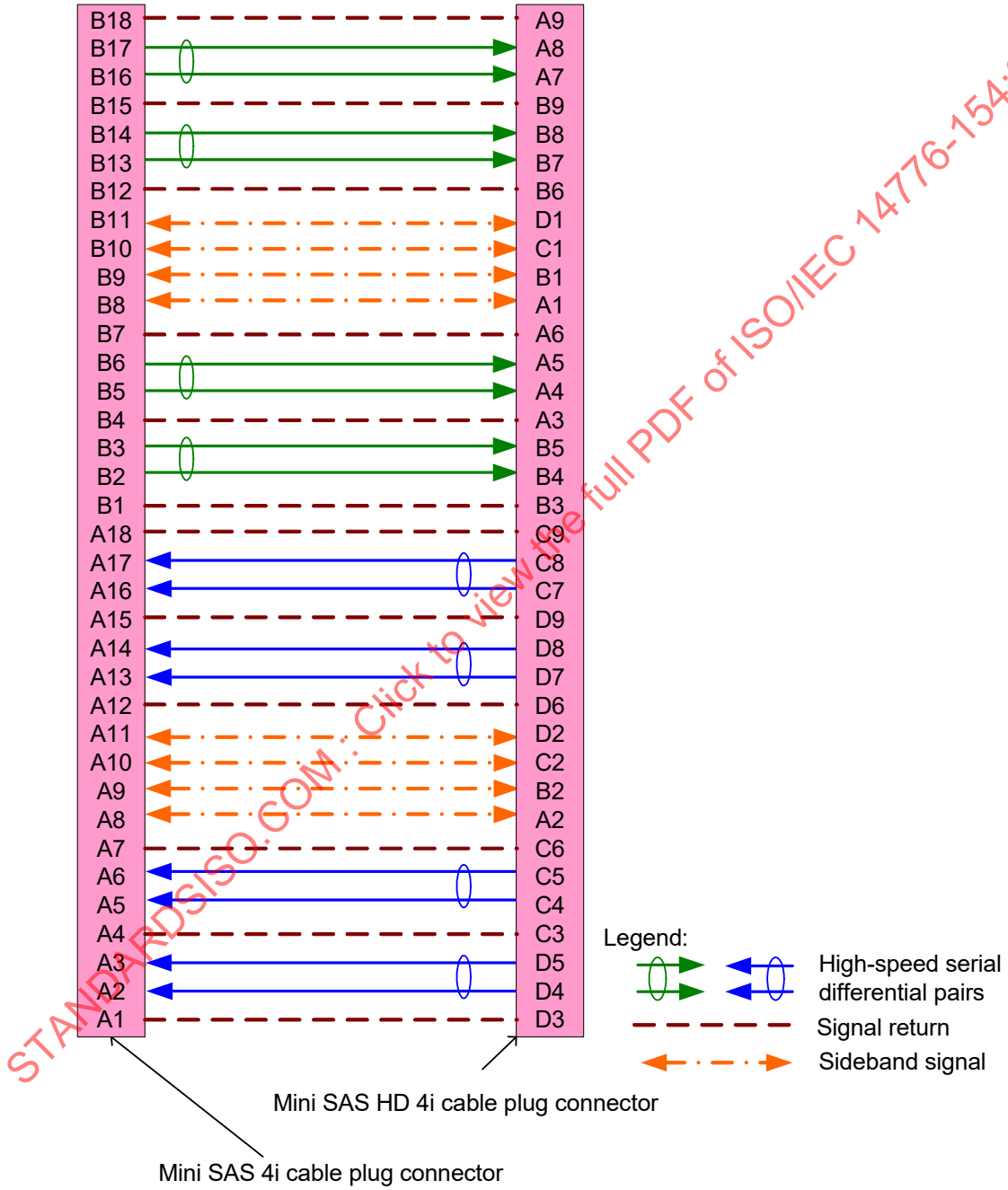


Figure 79 – SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

In addition to the signal return connections shown in figure 79, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.3 SAS internal fanout cable assemblies

5.4.4.1.3.1 SAS internal fanout cable assemblies overview

A SAS internal fanout cable assembly is either:

a) a SAS internal controller-based fanout cable assembly (see 5.4.4.1.3.2) with:
   A) a SAS 4i cable receptacle connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end;
   B) a Mini SAS 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end; or
   C) a Mini SAS HD 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end;

   or

b) a SAS internal backplane-based fanout cable assembly (see 5.4.4.1.3.3) with:
   A) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a SAS 4i cable receptacle connector on the other end (i.e., the backplane end);
   B) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS 4i cable plug connector on the other end (i.e., the backplane end); or
   C) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS HD 4i cable plug connector on the other end (i.e., the backplane end).

In a SAS internal fanout symmetric cable assembly, the TX signals on one end shall be connected to RX signals on the other end (e.g., a TX+ of one connector shall connect to an RX+ of the other connector).

5.4.4.1.3.2 SAS internal controller-based fanout cable assemblies

Figure 80 shows the SAS internal controller-based fanout cable assembly with a SAS 4i cable receptacle connector at the controller end.

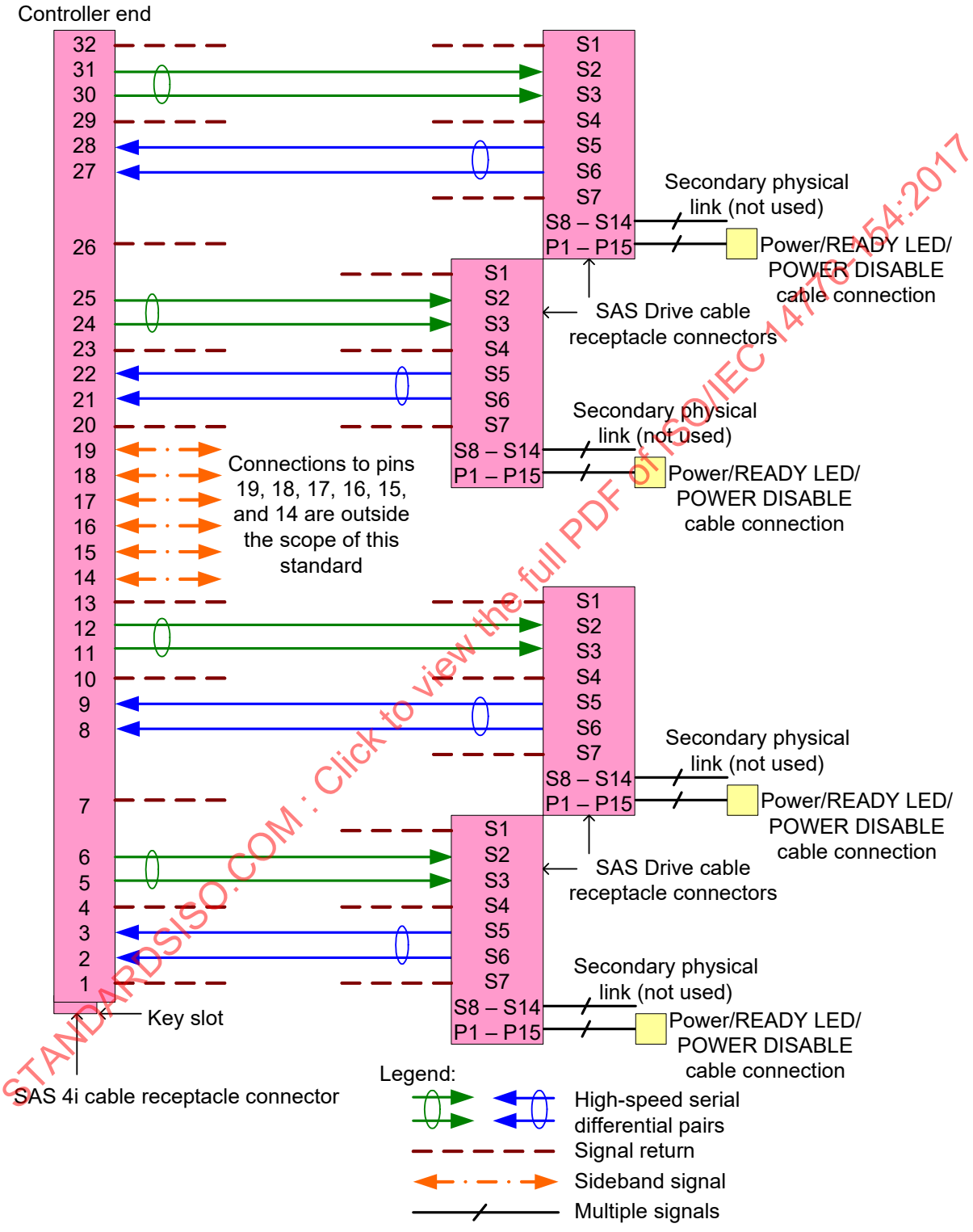


Figure 80 – SAS internal controller-based fanout cable assembly - SAS 4i

Each signal return on one end of the cable assembly shown in figure 80 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 81 shows the SAS internal controller-based fanout cable assembly with a Mini SAS 4i cable plug connector at the controller end.

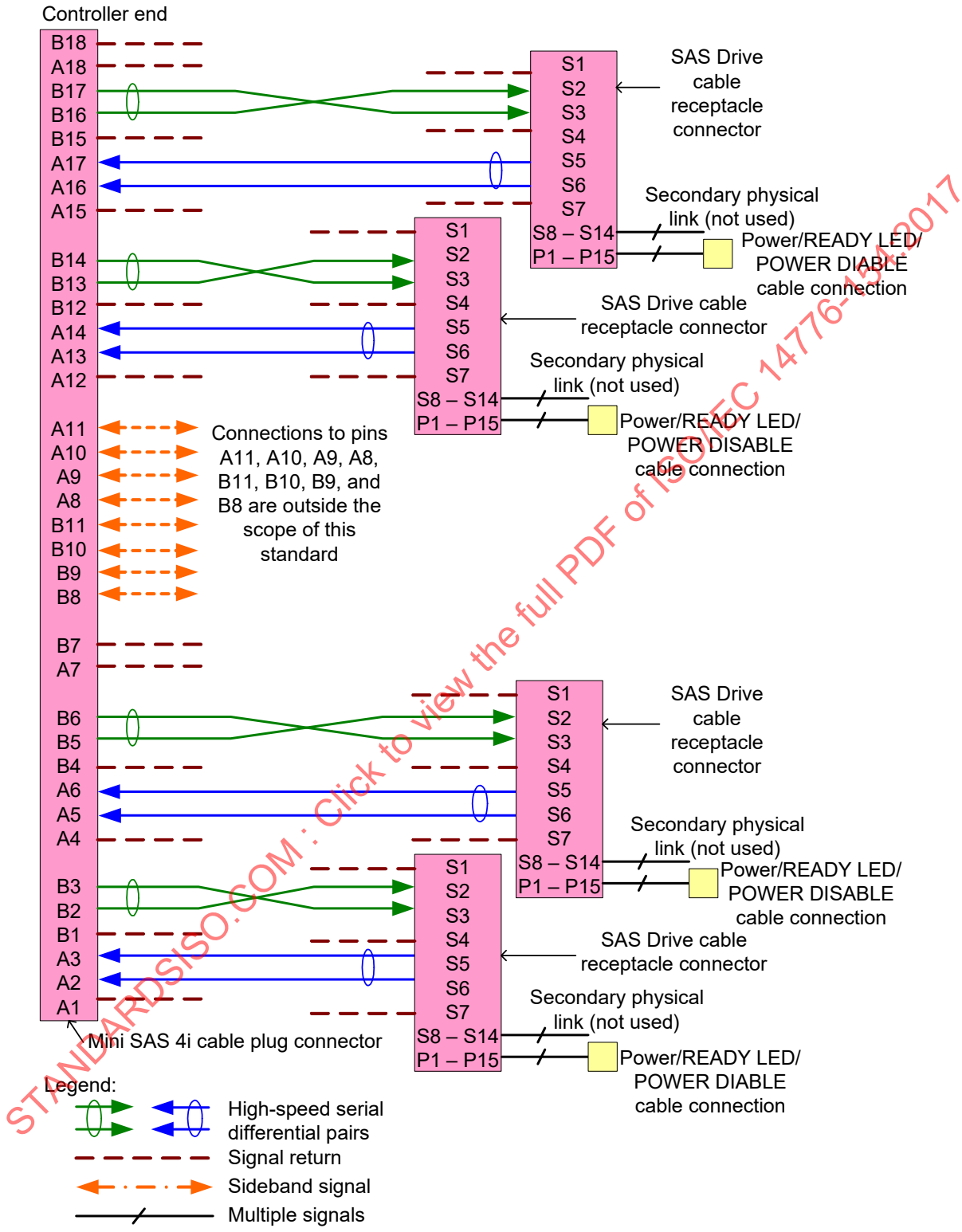


Figure 81 – SAS internal controller-based fanout cable assembly - Mini SAS 4i

Each signal return on one end of the cable assembly shown in figure 81 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 82 shows the SAS internal controller-based fanout cable assembly with a Mini SAS HD 4i cable plug connector at the controller end.

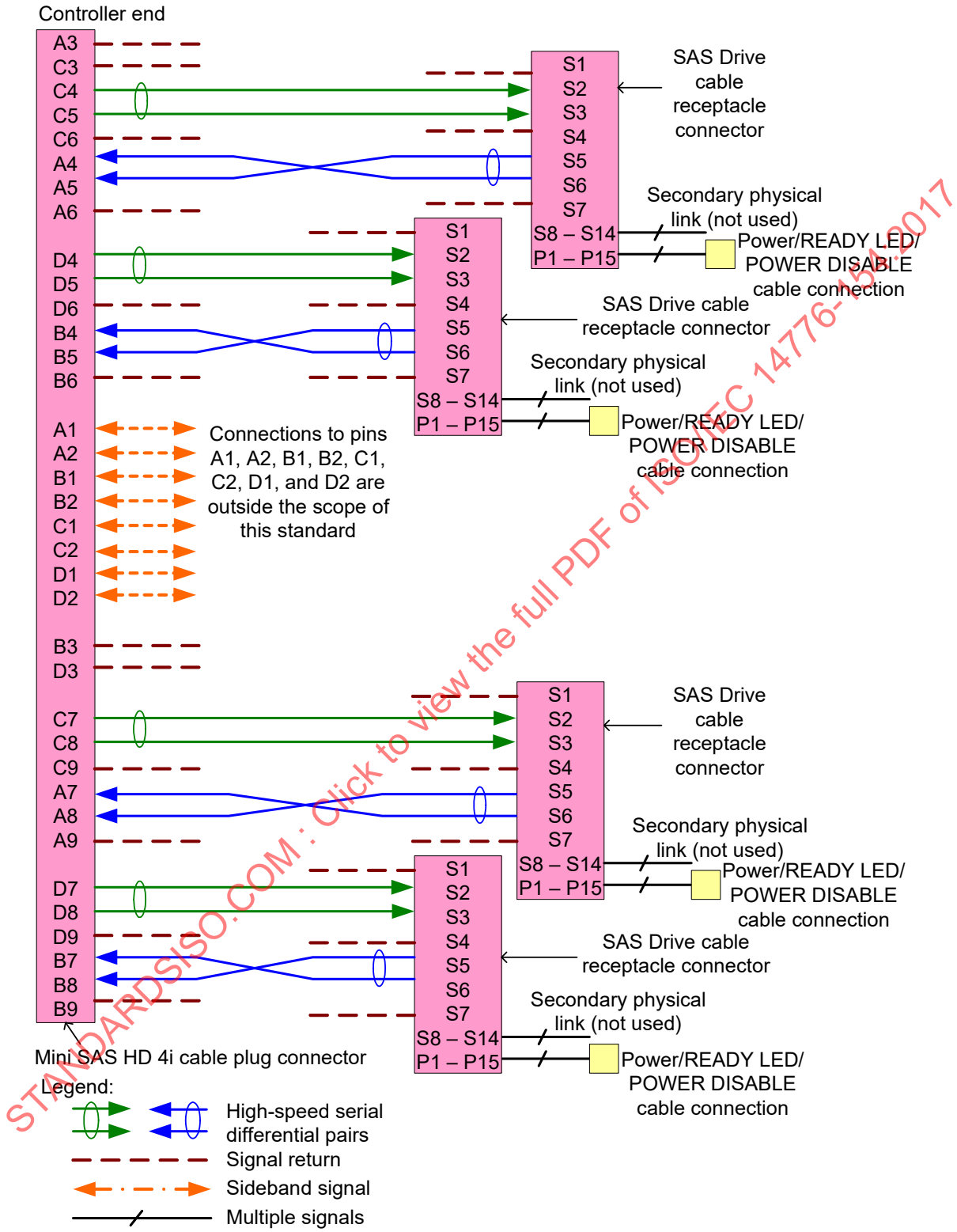


Figure 82 – SAS internal controller-based fanout cable assembly - Mini SAS HD 4i

Each signal return on one end of the cable assembly shown in figure 82 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.1.3.3 SAS internal backplane-based fanout cable assemblies

Figure 83 shows the SAS internal backplane-based fanout cable assembly with the SAS 4i cable receptacle connector.

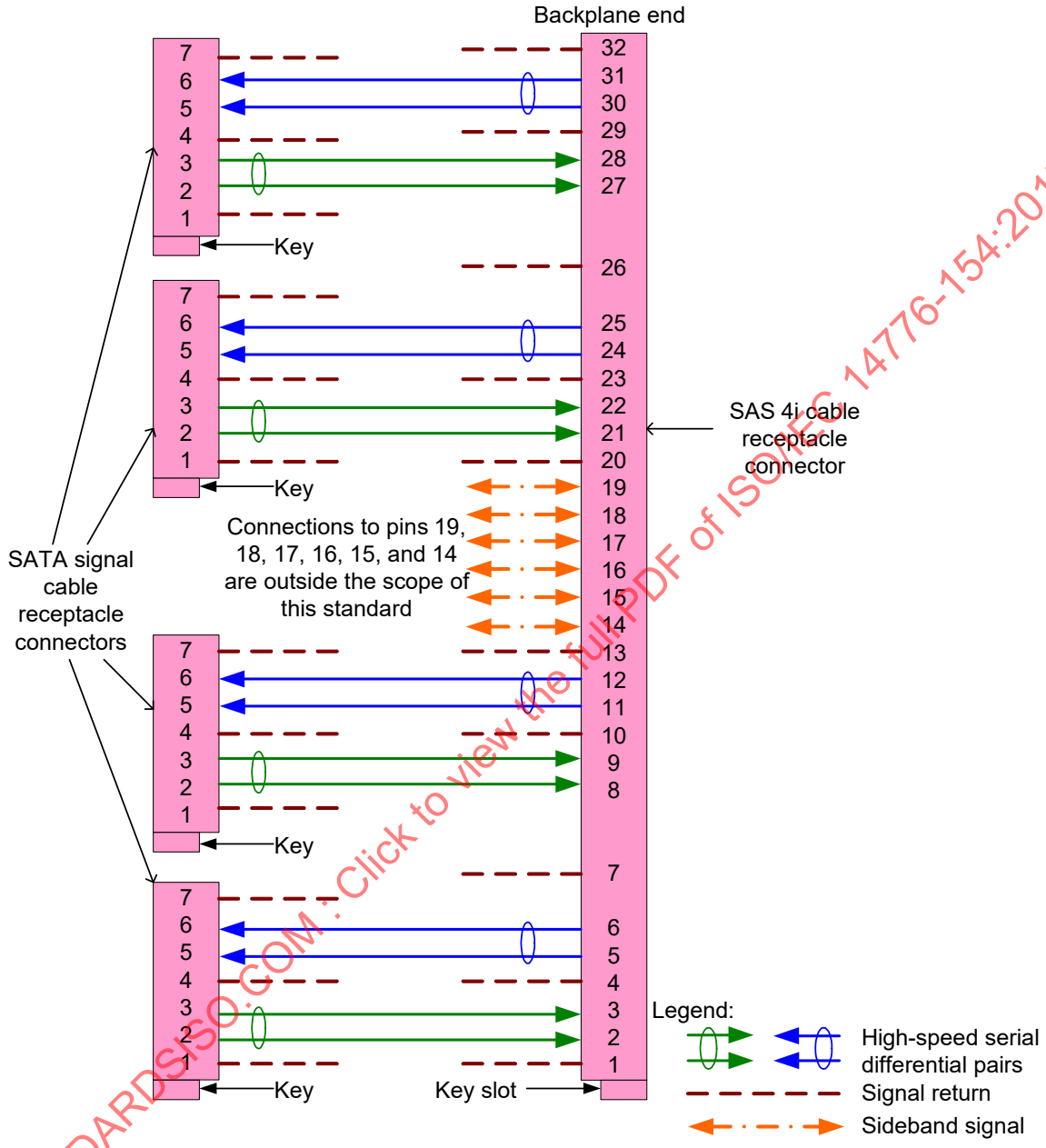


Figure 83 – SAS internal backplane-based fanout cable assembly - SAS 4i

Each signal return on one end of the cable assembly shown in figure 83 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 84 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS 4i cable receptacle connector.

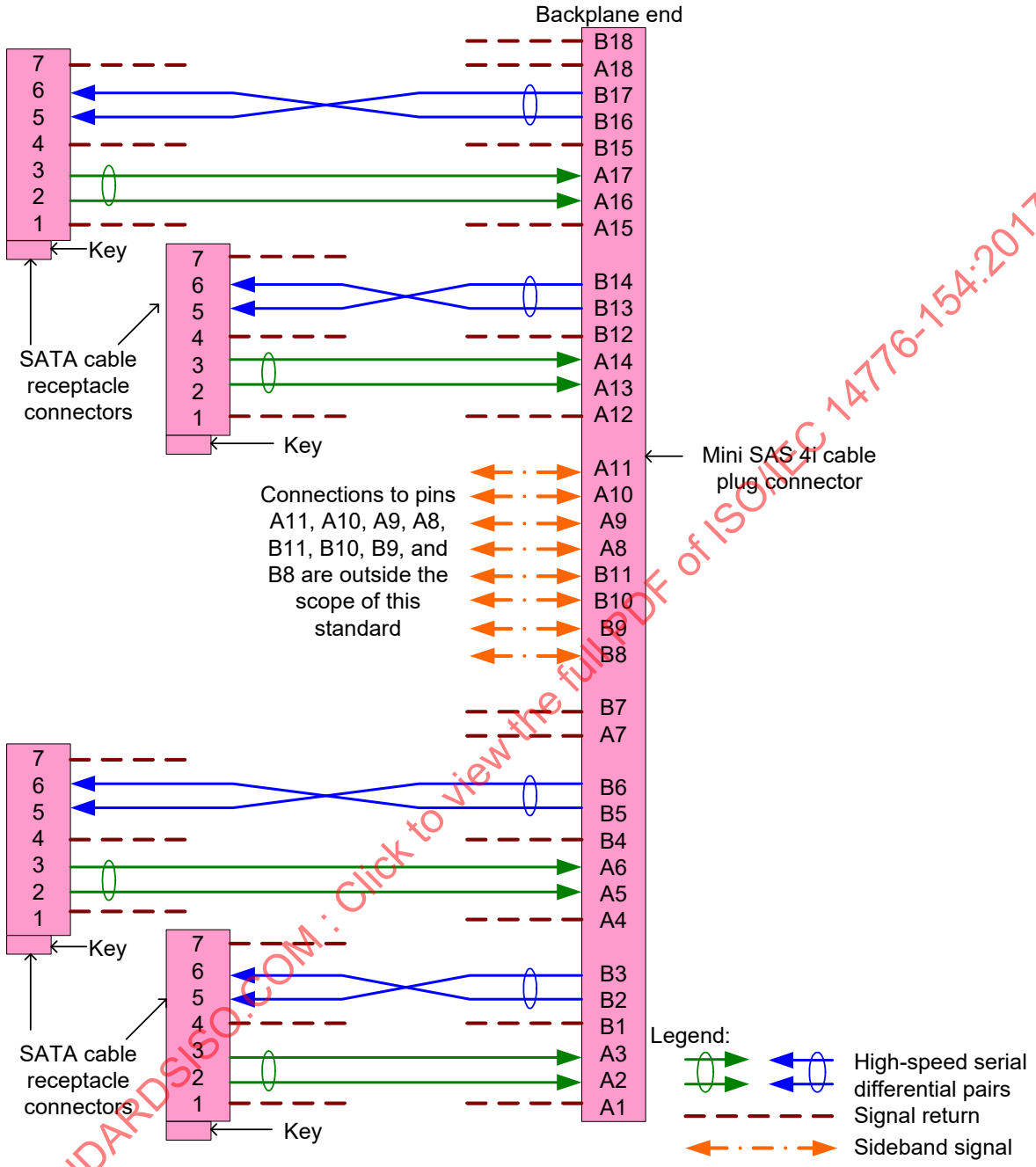


Figure 84 – SAS internal backplane-based fanout cable assembly - Mini SAS 4i

Each signal return on one end of the cable assembly shown in figure 84 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 85 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS HD 4i cable receptacle connector.

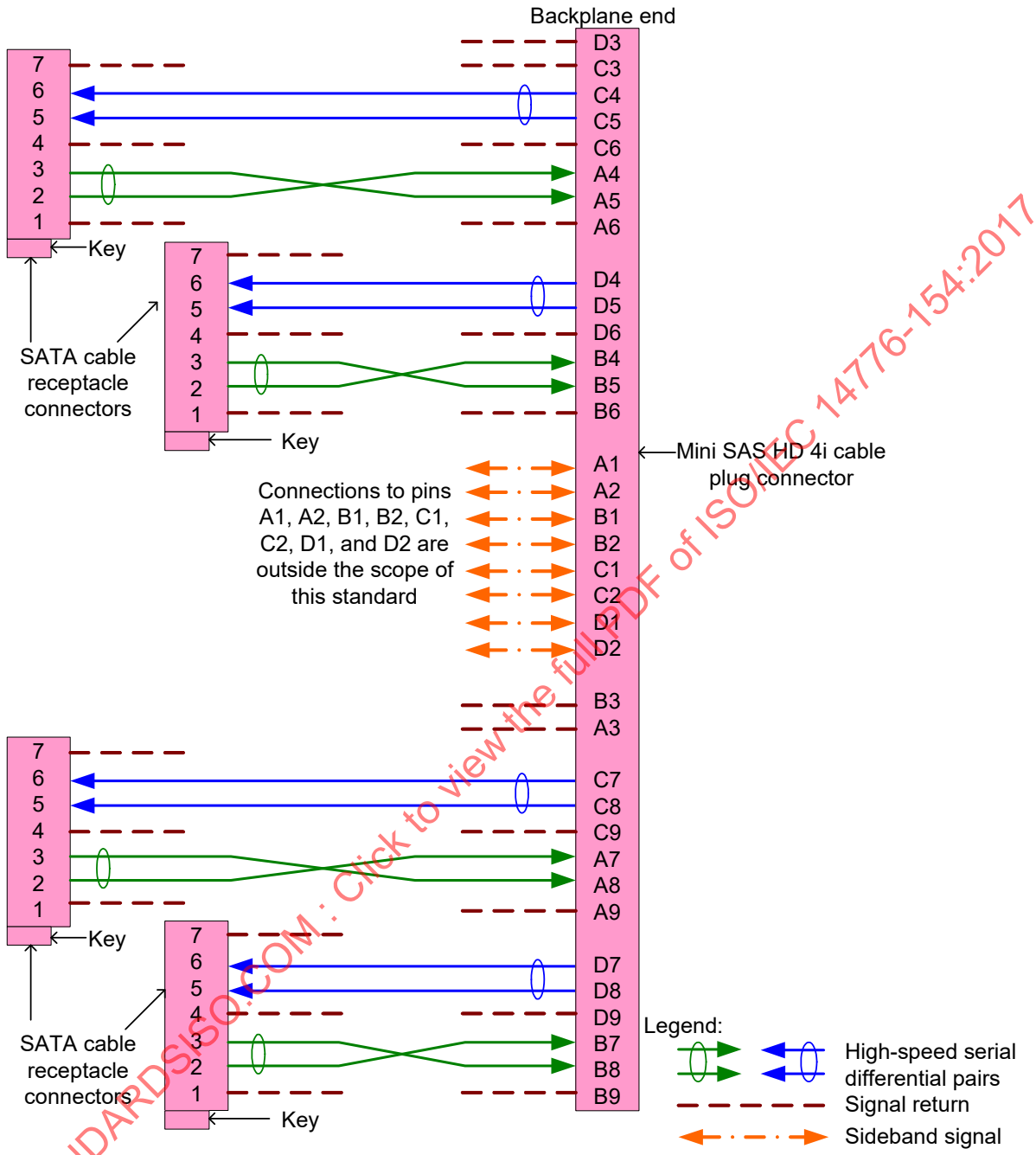


Figure 85 – SAS internal backplane-based fanout cable assembly - Mini SAS HD 4i

Each signal return on one end of the cable assembly shown in figure 85 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.2 SAS external cable assemblies

5.4.4.2.1 SAS external cable assemblies overview

A SAS external cable assembly has:

a) a Mini SAS 4x cable plug connector (see 5.4.3.5.1.1) at each end (see 5.4.4.2.2);
b) a Mini SAS HD 4x cable plug connector (see 5.4.3.5.2.1) at each end (see 5.4.4.2.3);
c) a Mini SAS HD 8x cable plug connector (see 5.4.3.5.2.2) at each end (see 5.4.4.2.4);
d) a Mini SAS HD 8x cable plug connector (see 5.4.3.5.2.2) at one end and two Mini SAS HD 4x cable plug connectors (see 5.4.3.5.2.1) at the other end (see 5.4.4.2.5);
e) a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end (see 5.4.4.2.6); or
f) a QSFP+ cable plug connector (see 5.4.3.5.3.1) at each end (see 5.4.4.2.7).

SAS external cable assemblies do not include power, the READY LED signal, or the POWER DISABLE signal.

Although the connector always supports four or eight physical links, a SAS external cable assembly may support one to eight physical links. SAS external cable assemblies should be labeled to indicate how many physical links are included (i.e., 1X, 2X, 3X, 4X, 5X, 6X, 7X, or 8X on each connector's housing).

The TX signals on one end shall be connected to the corresponding RX signals of the other end (e.g., TX0+ of one connector shall be connected to RX0+ of the other connector).

Signal returns shall not be connected to CHASSIS GROUND in the cable assembly.

In addition to the SAS icon (see Annex I), additional icons are defined for external connectors to guide users into making compatible attachments (i.e., not attaching expander device table routing phys to expander device table routing phys in externally configurable expander devices (see SPL-3), which is not allowed (see SPL-3)). Connectors that have one or more matching icons are intended to be attached together. Connectors that do not have a matching icon should not be attached together.

One end of the SAS external cable assembly shall support being attached to an end device, an enclosure out port, or an enclosure universal port. The other end of the SAS external cable assembly shall support being attached to an end device, an enclosure in port, or an enclosure universal port. If a Mini SAS 4x cable plug connector is used, then it shall include icons and key slots as defined in 5.4.3.5.1.1.

5.4.4.2.2 SAS external cable assembly - Mini SAS 4x

Figure 86 shows the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end. This cable assembly should not be used for rates greater than 6 Gbit/s.

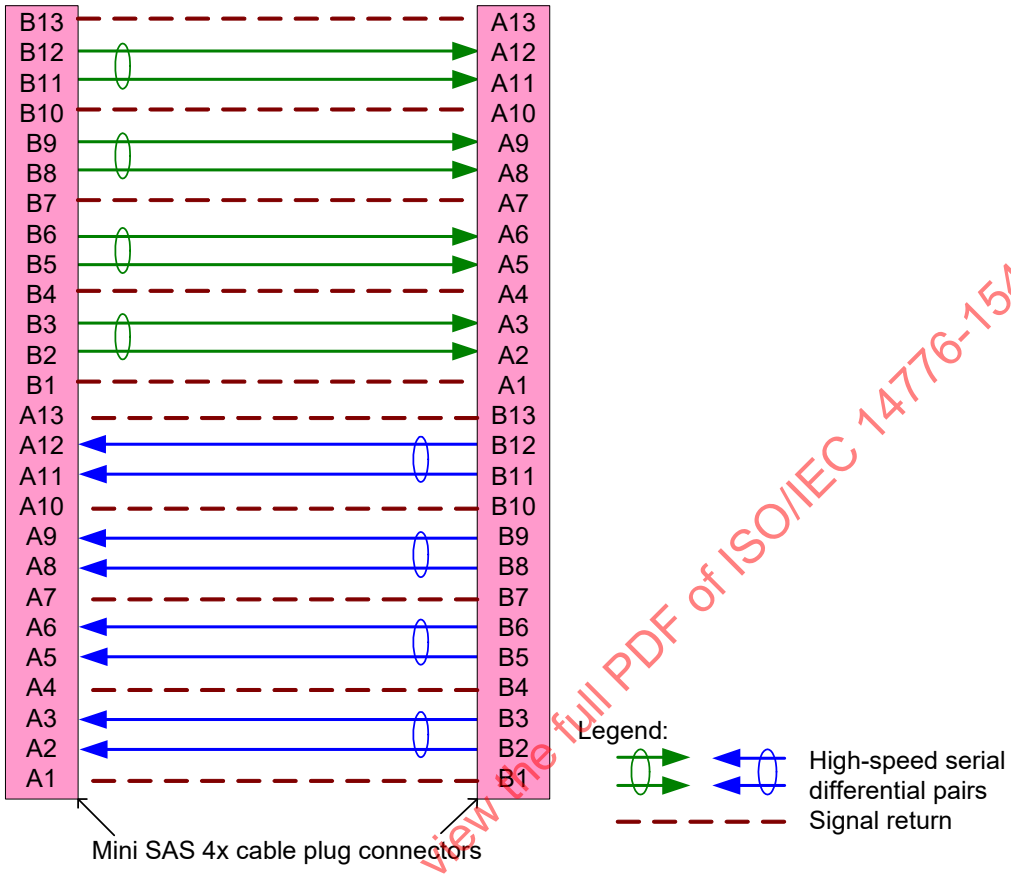


Figure 86 – Mini SAS 4x external cable assembly

In addition to the signal return connections shown in figure 86, one or more of the signal returns may be connected together in this cable assembly.

Figure 87 shows the SAS external cable assembly with Mini SAS 4x active cable assembly plug connectors at each end.

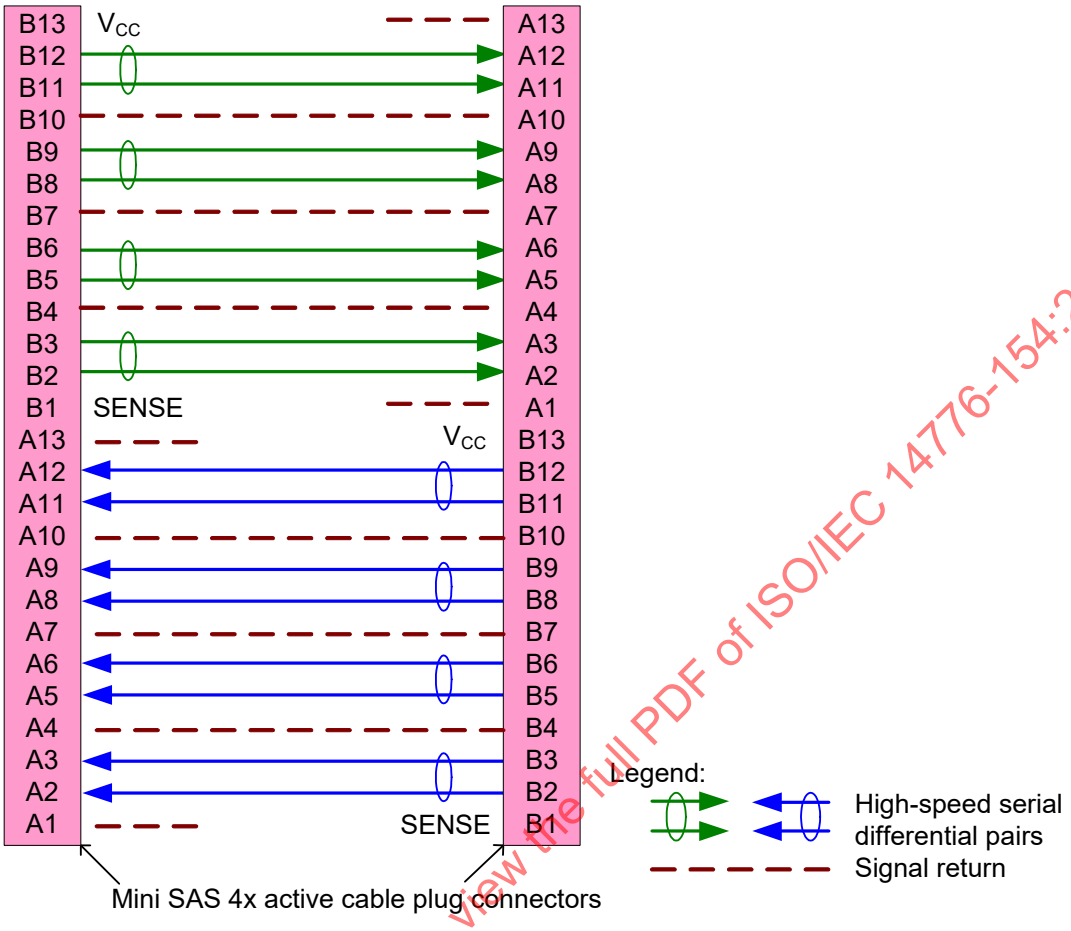


Figure 87 – Mini SAS 4x active external cable assembly

In addition to the signal return connections shown in figure 87, one or more of the signal returns may be connected together in this cable assembly.

Figure 88 shows the an example cable with icons and key slots in the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end. Depending on the cable configuration, the Mini SAS 4x cable connectors may also include different icon, key slot, and key combinations than shown in figure 88 (see 5.4.3.5.1.1).

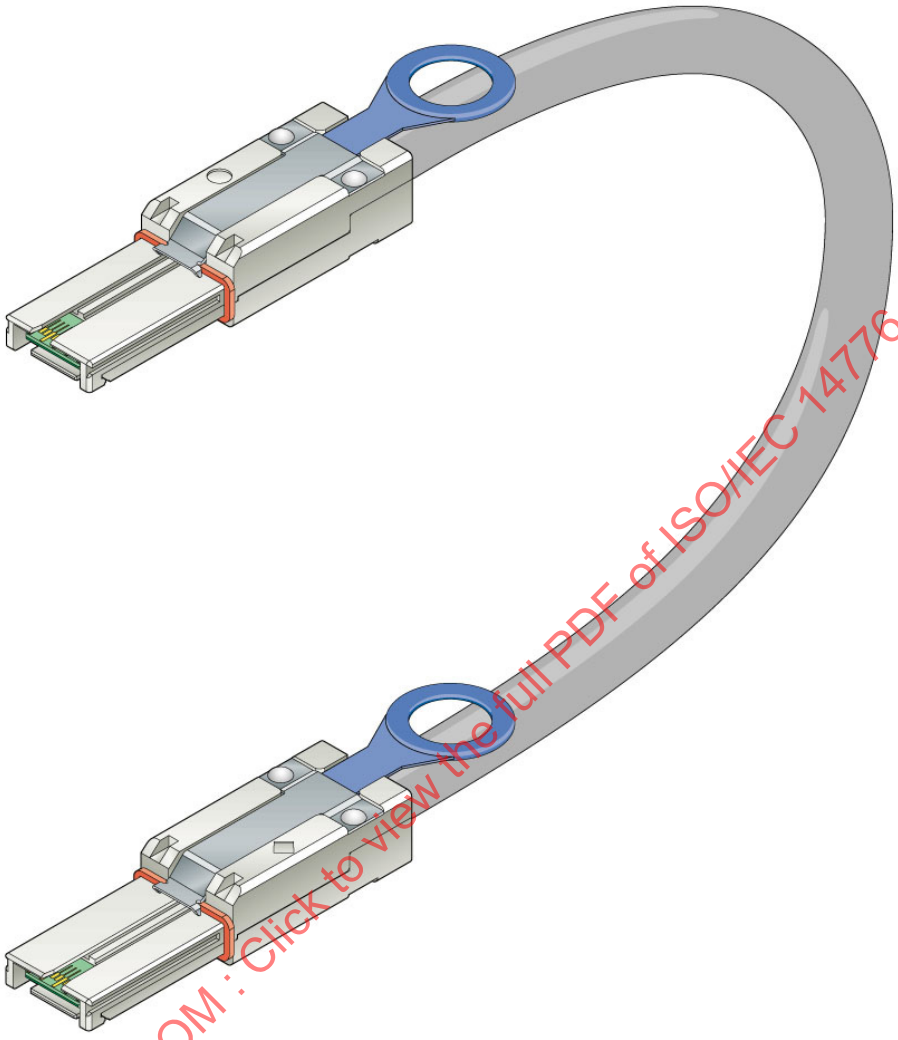


Figure 88 – SAS external cable assembly with Mini SAS 4x cable plug connectors

Although the topology is supported by this document and SPL-3, a SAS external cable assembly with Mini SAS 4x cable plug connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this document and SPL-3.

5.4.4.2.3 SAS external cable assembly - Mini SAS HD 4x

Figure 89 shows the SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

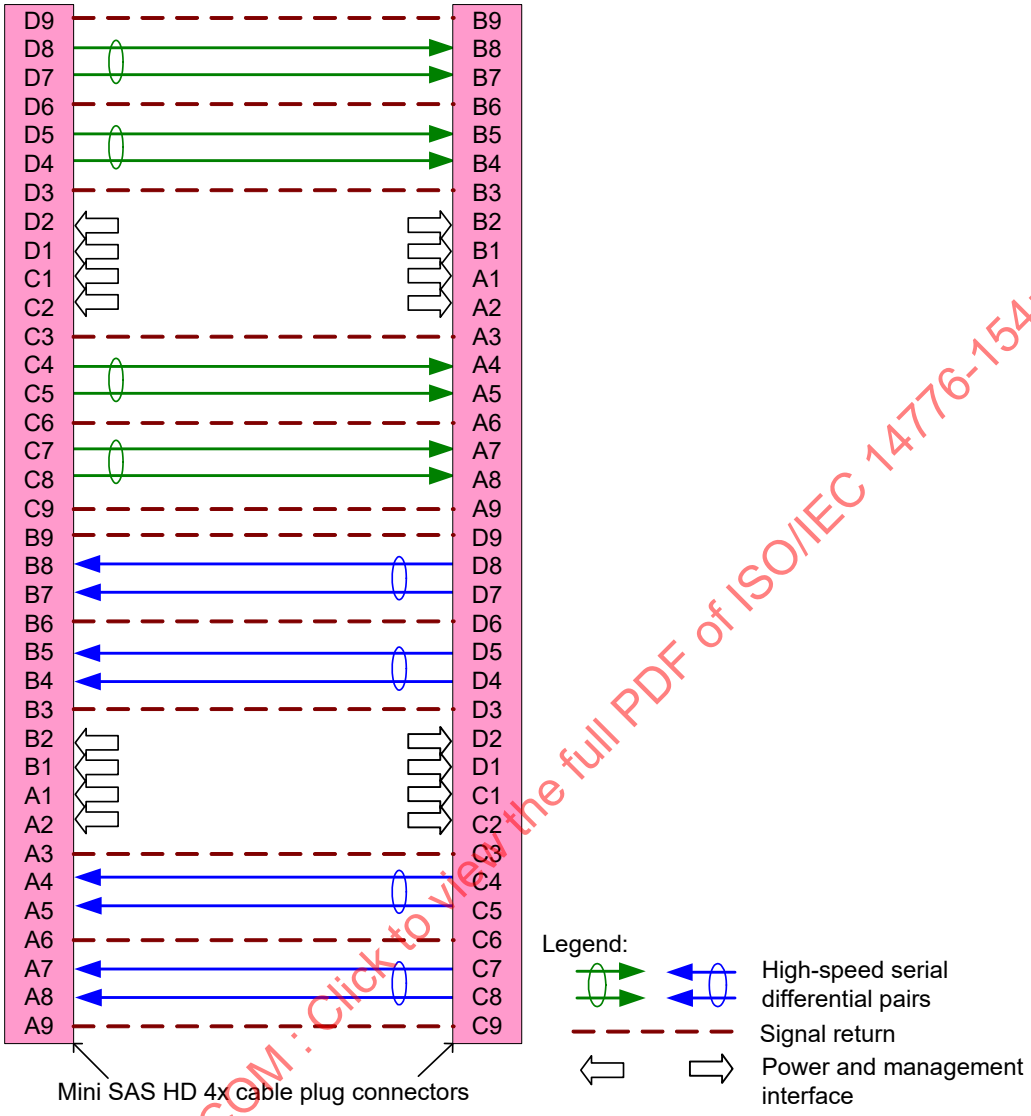


Figure 89 – SAS external cable assembly - Mini SAS HD 4x

In addition to the signal return connections shown in figure 89, one or more of the signal returns may be connected together in this cable assembly.

Figure 90 shows an example SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

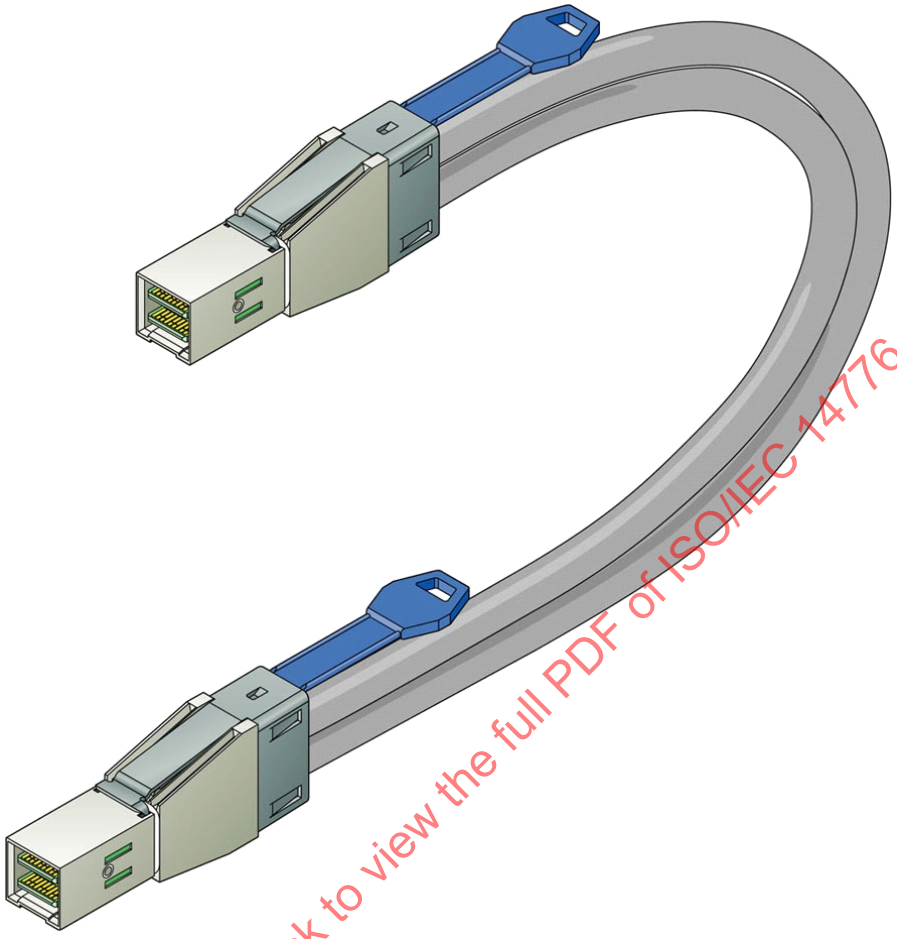


Figure 90 – SAS external cable assembly with Mini SAS HD 4x cable plug connectors

5.4.4.2.4 SAS external cable assembly - Mini SAS HD 8x

Figure 91 shows the SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

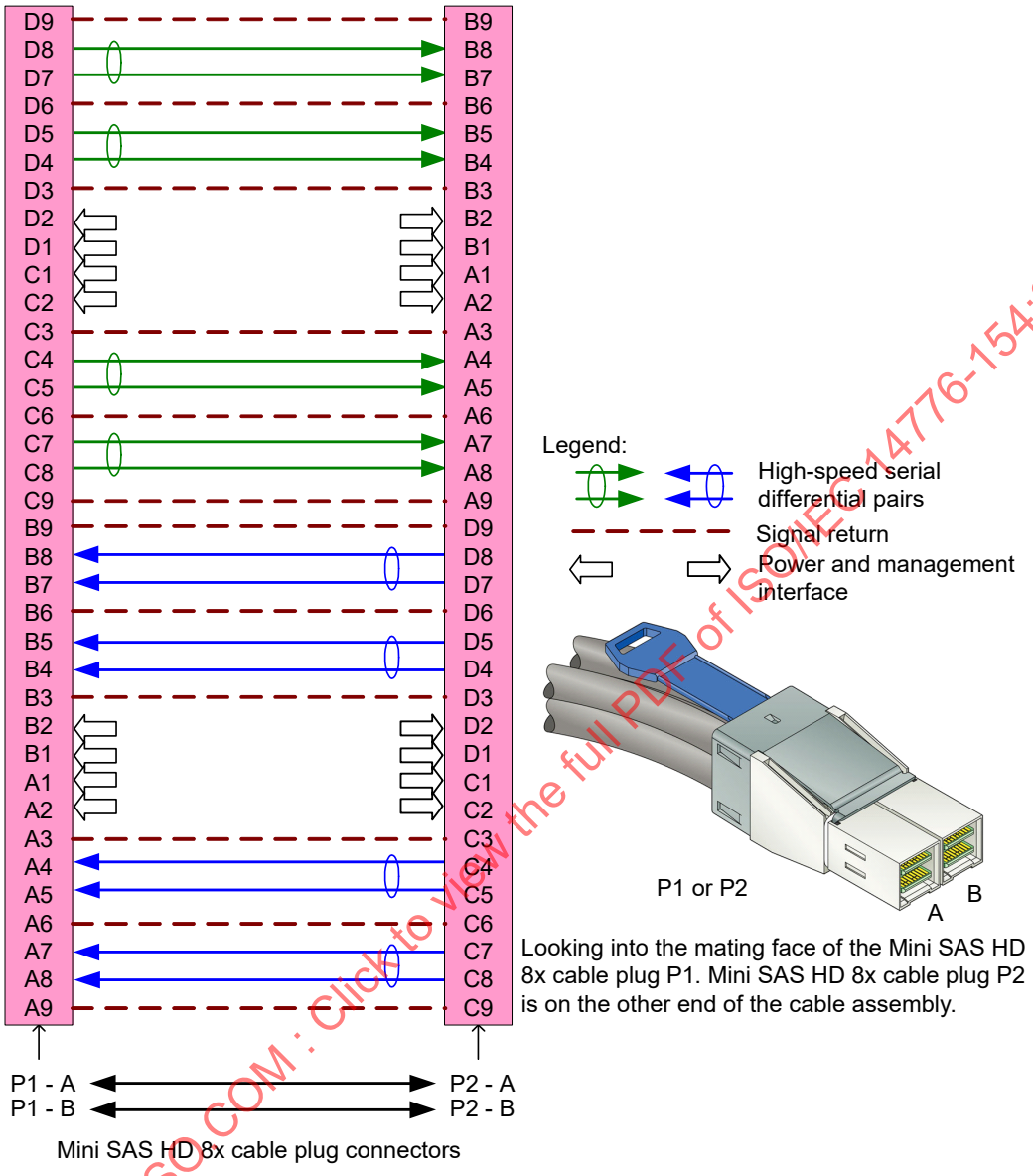


Figure 91 – SAS external cable assembly - Mini SAS HD 8x

In addition to the signal return connections shown in figure 91, one or more of the signal returns may be connected together in this cable assembly.

The cable assembly shown in figure 91 may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.4.3.5.2.6 for connector module pin assignments.

Figure 92 shows an example SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

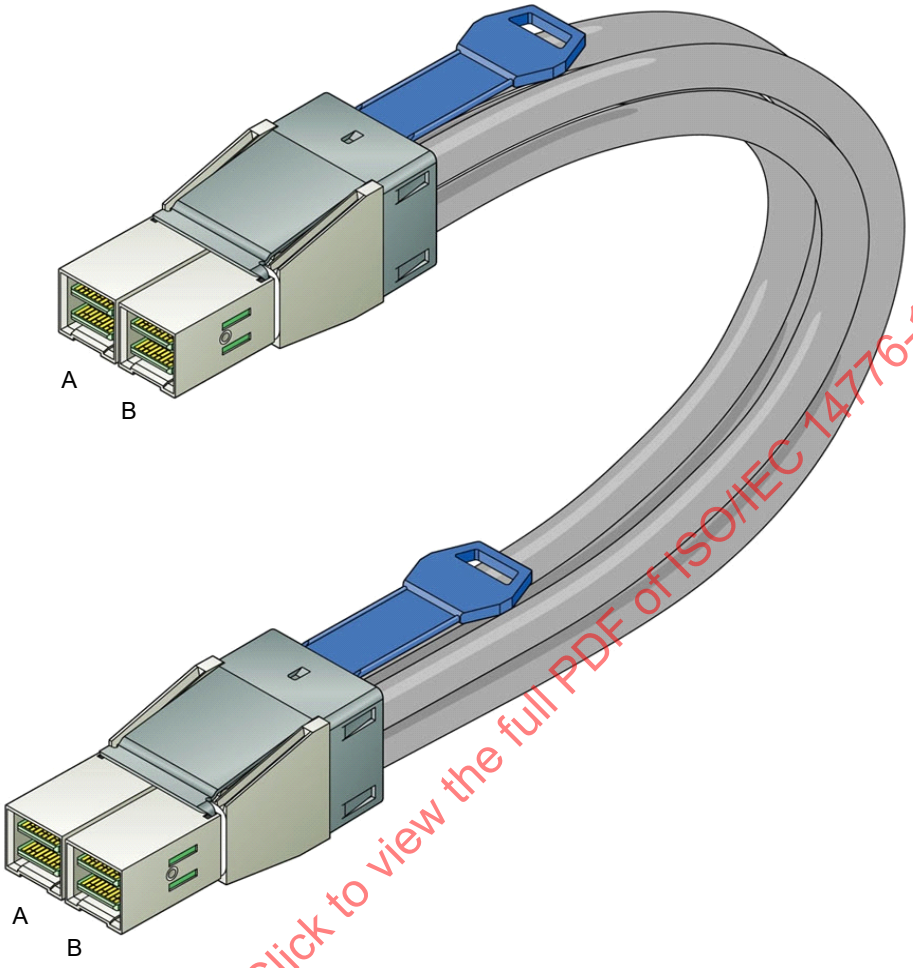


Figure 92 – SAS external cable assembly with Mini SAS HD 8x cable plug connectors

5.4.4.2.5 SAS external cable assembly - Mini SAS HD 8x to Mini SAS HD 4x

Figure 93 shows the SAS external cable assembly with a Mini SAS HD 8x cable plug connector at one end and two Mini SAS HD 4x cable plug connectors at the other end.

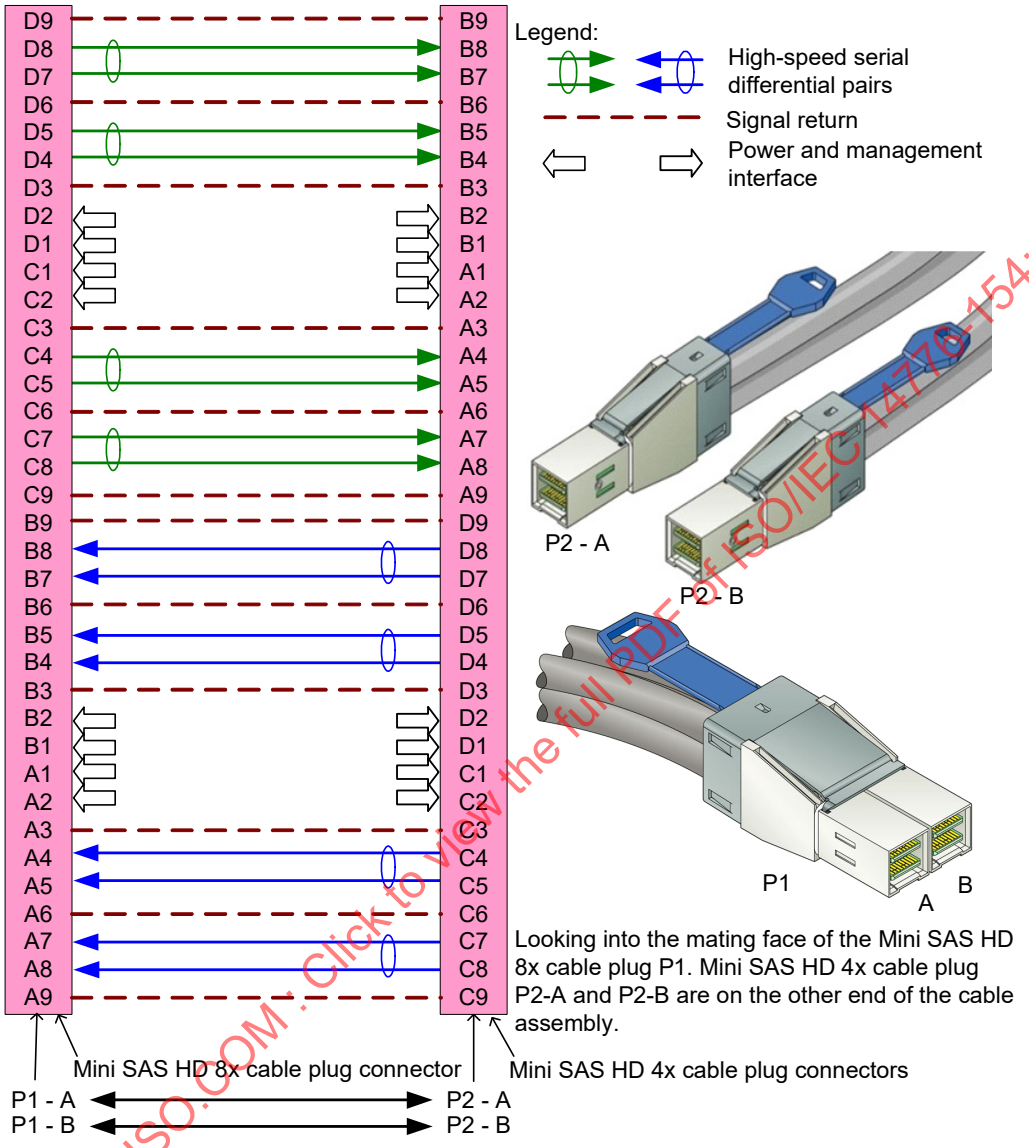


Figure 93 – SAS external cable assembly - Mini SAS HD 8x to Mini SAS HD 4x

In addition to the signal return connections shown in figure 93, one or more of the signal returns may be connected together in this cable assembly.

The cable assembly shown in figure 93 may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical links connected). See 5.4.3.5.2.6 for connector module pin assignments.

Figure 94 shows an example SAS external cable assembly with a Mini SAS HD 8x cable plug connector at one end and two Mini SAS HD 4x cable plug connectors at the other end.

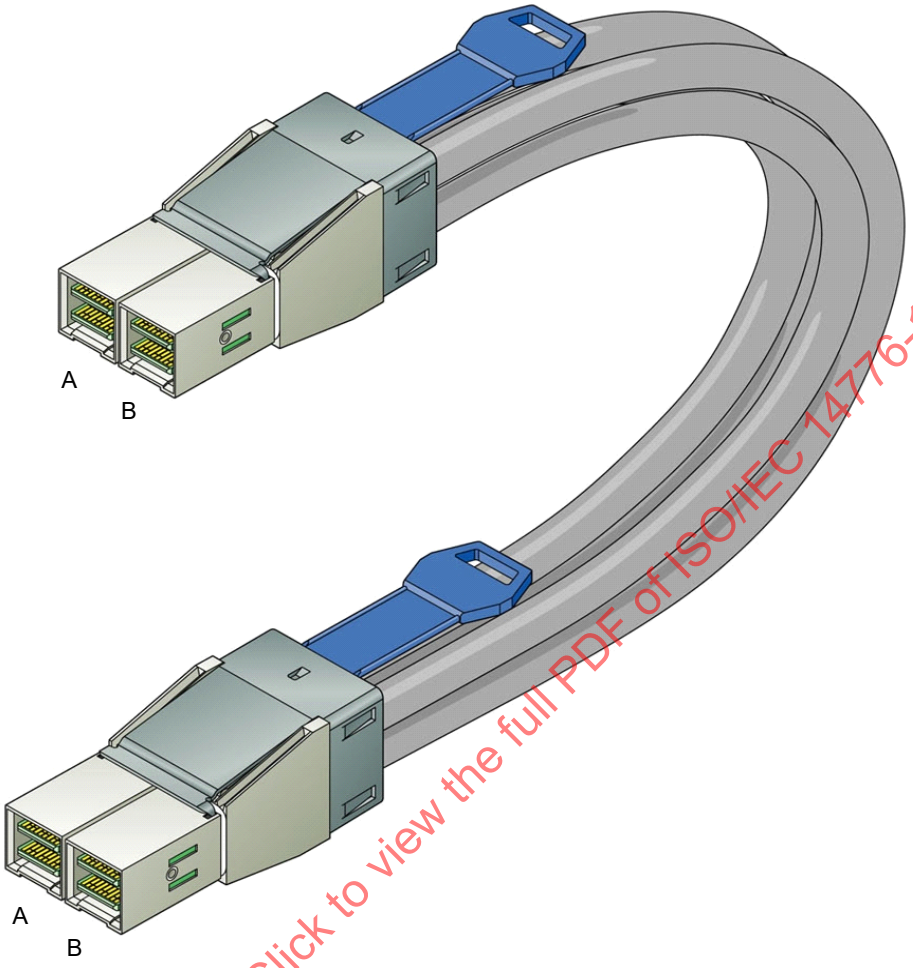


Figure 94 – SAS external cable assembly with a Mini SAS HD 8x cable plug connector and two Mini SAS HD 4x cable plug connectors

5.4.4.2.6 SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Figure 95 shows the SAS external cable assembly with a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end. This cable assembly should not be used for rates greater than 6 Gbit/s.

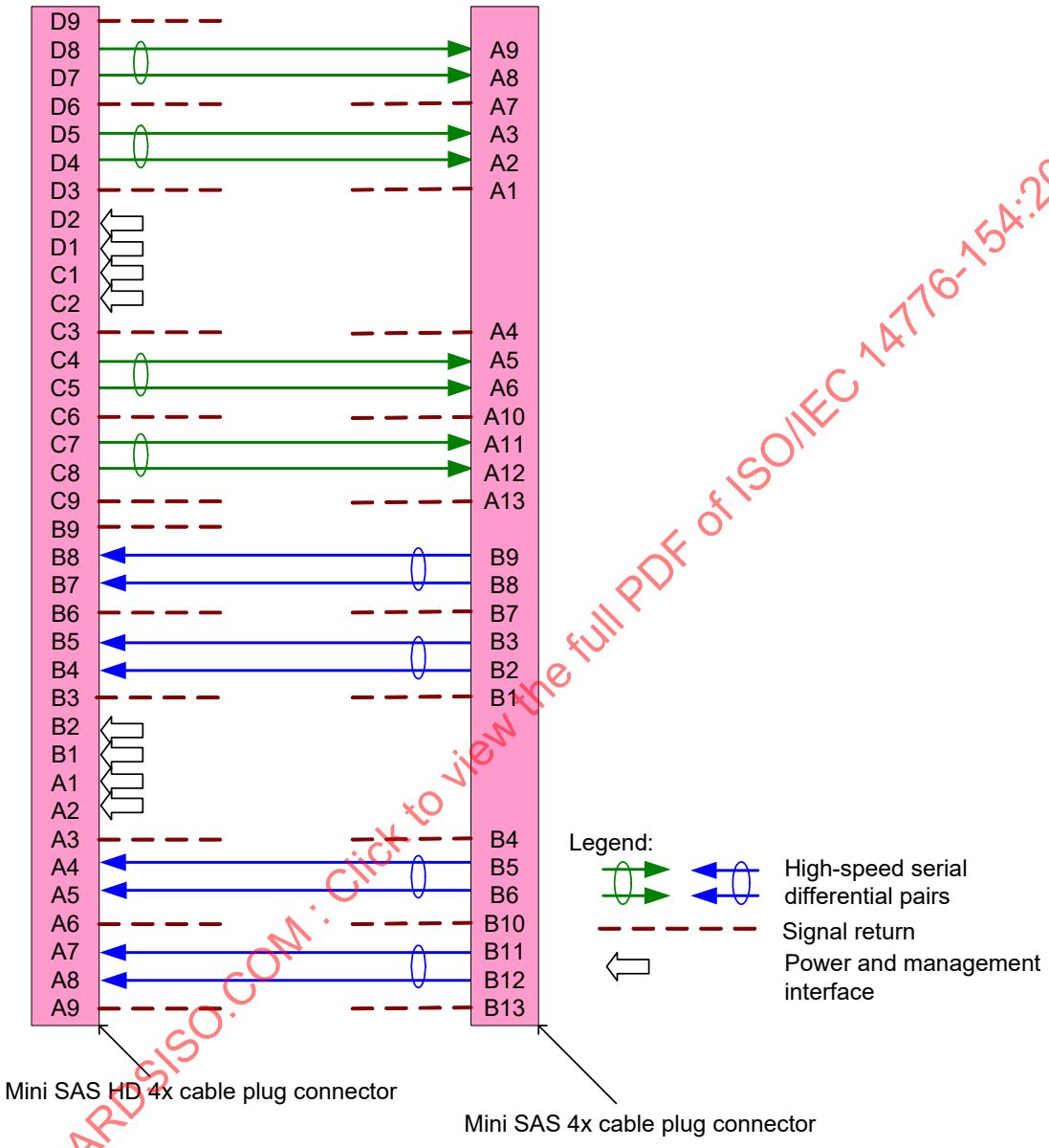


Figure 95 – SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Figure 94 shows a example SAS external cable assembly with a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end.

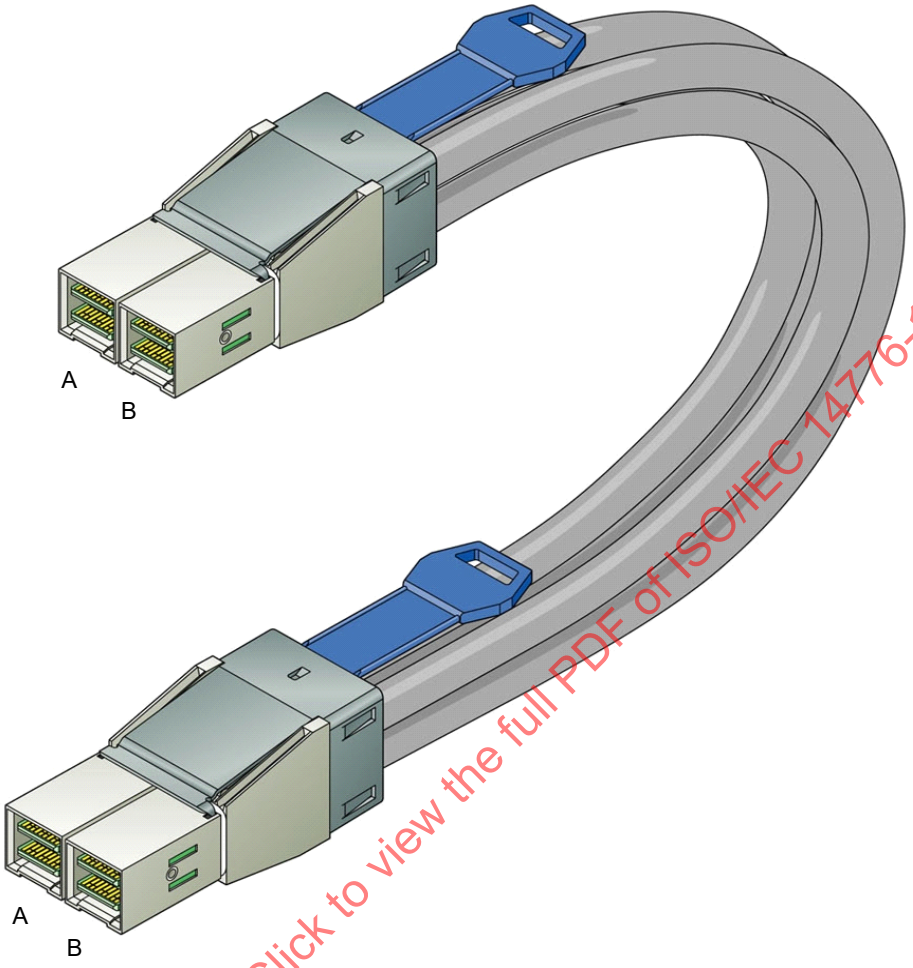


Figure 96 – SAS external cable assembly with a Mini SAS HD 4x cable plug connector and a Mini SAS 4x cable plug connector

Each signal return on one end of the cable assembly shown in figure 96 shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.2.7 SAS external cable assembly - QSFP+

QSFP+ cable assemblies are defined in SFF-8685. QSFP+ cable assemblies for SAS shall comply with the TxRx connection characteristics specified in this document (see 5.5).

5.4.5 Backplanes

SAS backplane designs should follow the recommendations in SFF-8460.

5.5 TxRx connection characteristics

5.5.1 TxRx connection characteristics overview

Each TxRx connection shall support a bit error ratio (BER) that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits). The parameters specified in this document support meeting this requirement under all conditions including the minimum input and output amplitude levels.

A TxRx connection may be constructed from multiple TxRx connection segments (e.g., backplanes and cable assemblies). It is the responsibility of the implementer to ensure that the TxRx connection is constructed from individual TxRx connection segments such that the overall TxRx connection requirements are met. Loss characteristics for individual TxRx connection segments are beyond the scope of this document.

Each TxRx connection segment shall comply with the impedance requirements detailed in 5.5.2 for the conductive material from which they are formed. A passive equalizer network, if present, shall be considered part of the TxRx connection.

TxRx connections shall be applied only to homogeneous ground applications (e.g., between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane).

Compliance points referenced in the electrical requirement tables are shown in 5.3 unless otherwise specified.

5.5.2 TxRx connection general characteristics

Table 24 defines the TxRx connection general characteristics.

Table 24 – TxRx connection general characteristics

Characteristic [a] [b]	Units	Value
Differential impedance (nominal)	Ω	100
Bulk cable or backplane:		
Differential characteristic impedance [d] [e]	Ω	100
Mated connectors:		
Differential characteristic impedance [f]	Ω	100
Passive cable assembly and backplane:		
Maximum propagation delay [c]	ns	53
Minimum $\|S_{DD21}\|$ for internal cable assemblies from 10 MHz to 4 500 MHz [g]	dB	-6
Minimum $\|S_{DD21}\|$ for internal cable assemblies from 4 500 MHz to 9 000 MHz [g] [h]	dB	-11
Minimum $\|S_{DD21}\|$ for external cable assemblies and backplanes	See 5.5	
Mini SAS 4x active cable assembly:		
Maximum propagation delay [i]	ns	133
Differential characteristic impedance [f]	Ω	100
Managed cable assembly:		
Maximum propagation delay [j]	ns	510
Differential characteristic impedance [f]	Ω	100

[a] All measurements are made through mated connector pairs.

[b] The equivalent maximum TDR rise time from 20 % to 80 % shall be 70 ps. Filtering may be used to obtain the equivalent rise time. The filter consists of the two-way launch/return path of the test fixture, the two-way launch/return path of the test cable, and the software or hardware filtering of the TDR scope. The equivalent rise time is the rise time of the TDR scope output after application of all filter components. When configuring software or hardware filters of the TDR scope to obtain the equivalent rise time, filtering effects of test cables and test fixtures shall be included.

[c] This is based on propagation delay for a 10 m Mini SAS 4x passive cable assembly. See SPL-3 for STP flow control details.

[d] The impedance measurement identifies the impedance mismatches present in the bulk cable or backplane when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the bulk cable or backplane, when present, but includes any intermediate connectors or splices.

[e] Where the bulk cable or backplane has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[f] The characteristic impedance is a measurement reference impedance for the test environment.

[g] An internal cable assembly may be a TxRx connection segment or a full TxRx connection. The full TxRx connection is required to comply with the requirements at intra-enclosure compliance points defined in 5.3 and 5.3.3.

[h] This requirement applies only for 12 Gbit/s passive cable assemblies.

[i] This is based on propagation delay for a 25 m Mini SAS 4x active cable assembly. TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL-3 for STP flow control details.

[j] This is based on propagation delay for a 100 m optical cable. Managed cables shall report the propagation delay through the cable management interface (see 5.4.3.5.2.7). TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL-3 for STP flow control details.

5.5.3 Passive TxRx connection S-parameter limits

S-parameters limits are calculated per the following formula:

$$\text{Measured value} < \max [\, L, \min [\, H, N + 13.3 \times \log_{10}(f / 3\ \text{GHz}) \,] \,]$$

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 25 defines the maximum limits for S-parameter of the passive TxRx connection segment between IT_S and IR or CT_S and CR.

Table 25 – Maximum limits for S-parameters of the passive TxRx connection between IT_S and IR or CT_S and CR

Characteristic [a b c d]	L [e] dB	N [e] dB	H [e] dB	S [e] dB/decade	f_{min} [e] MHz	f_{max} [e] GHz	f_{max} [e g] GHz
$[20 \times \log_{10}(\lvert S_{CD21} \rvert)] - [20 \times \log_{10}(\lvert S_{DD21} \rvert)]$	-10			0	100	6.0	9.0
Maximum near-end crosstalk (NEXT) for each receive signal pair [f h]	-26			0	100	6.0	
$20 \times \log_{10}(\lvert S_{DD22} \rvert)$	-10	-7.9	-3.9	13.3	100	6.0	9.0
$20 \times \log_{10}(\lvert S_{CD22} \rvert)$	-26	-12.7	-10	13.3	100	6.0	9.0
$20 \times \log_{10}(\lvert S_{CD21} \rvert)$	-18			0	100	6.0	9.0
Insertion loss to crosstalk ratio (ICR(f)) [g h i j]	-15			0	100		6.0

[a] All measurements are made through mated connector pairs.

[b] Specifications apply to any combination of cable assemblies and backplanes that are used to form a passive TxRx connection.

[c] $|S_{CC22}|$ and $|S_{DC22}|$ are not specified.

[d] For 12 Gbit/s, these characteristics only apply to cable assemblies between CT_S and CR compliance points. 12 Gbit/s passive cable assemblies shall also comply with passive TxRx connection characteristics for trained 12 Gbit/s (see 5.5.6).

[e] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

[f] Only applies for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

[g] Only applies for 12 Gbit/s.

[h] Determine all near-end and far-end significant crosstalk sources. The sum of the crosstalk transfer ratios is measured in the frequency domain. The following equation details the summation process of the valid near-end crosstalk sources:

$$\text{TotalNEXT}(f) = 10 \times \log_{10} \sum_{1}^{n} 10^{\langle \text{NEXT}(f)/10 \rangle}$$

where:

f is frequency; and

n is the number of the near-end crosstalk source.

All NEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

The following equation details the summation process of the valid far-end crosstalk sources:

$$\text{TotalFEXT}(f) = 10 \times \log_{10} \sum_{1}^{n} 10^{\langle \text{FEXT}(f)/10 \rangle}$$

where:

f is frequency; and

n is the number of the far-end crosstalk source.

[i] All FEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

[j] The following equation defines the insertion loss to crosstalk ratio:

$$\text{ICR}(f) = [10 \times \log_{10}(10^{\text{TotalNEXT}(f)/10} + 10^{\text{TotalFEXT}(f)/10})] - [20 \times \log_{10}(\lvert S_{DD21} \rvert)]$$

where:

f	is frequency;
TotalNEXT(f)	is near-end crosstalk;
TotalFEXT(f)	is far-end crosstalk; and
S_{DD21}	is insertion loss.

Figure 97 shows the passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits defined in table 25.

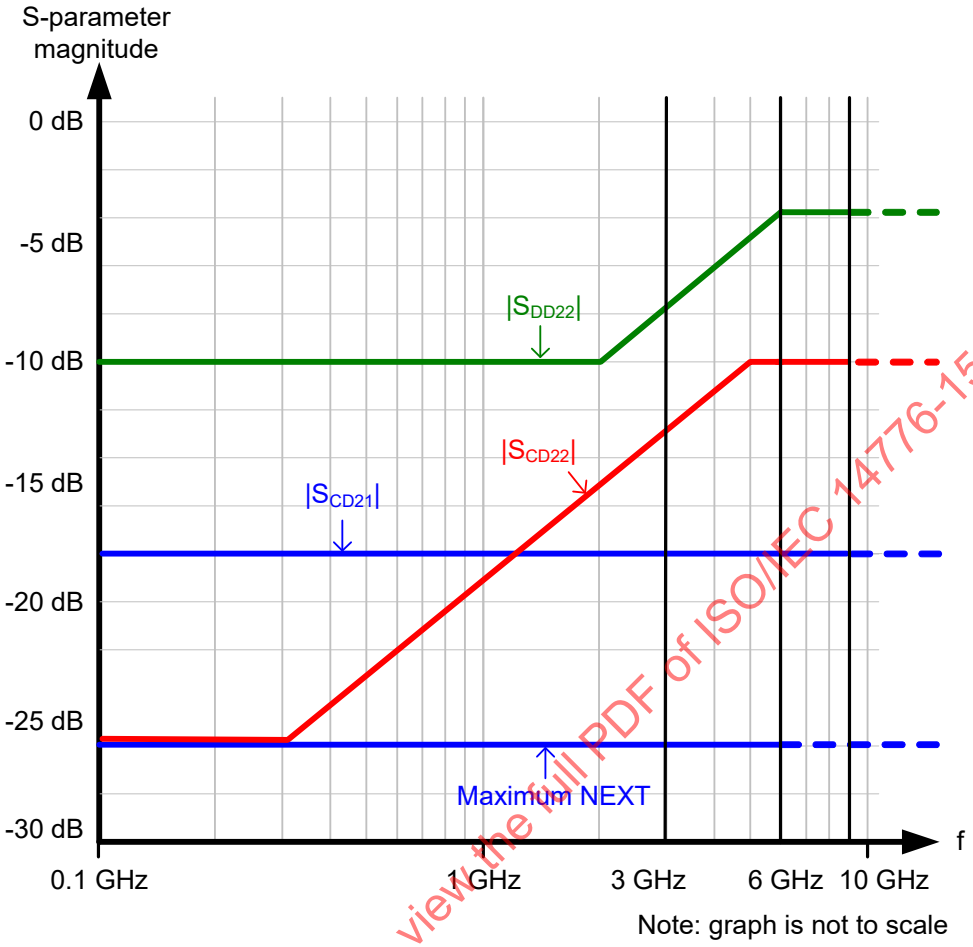


Figure 97 – Passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits

5.5.4 Passive TxRx connection characteristics for untrained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

For untrained 1.5 Gbit/s and 3 Gbit/s, each external passive TxRx connection shall be designed such that its loss characteristics are less than the loss of the TCTF test load plus ISI at CT at 3 Gbit/s (see figure 108 in 5.6.3) over the frequency range of 50 MHz to 3 000 MHz.

For untrained 1.5 Gbit/s and 3 Gbit/s, each internal passive TxRx connection shall be designed such that its loss characteristics are less than:

a) the loss of the TCTF test load plus ISI at IT at 3 Gbit/s (see figure 107 in 5.6.3) over the frequency range of 50 MHz to 3 000 MHz; or
b) the loss of the low-loss TCTF test load plus ISI (see figure 112 in 5.6.4) over the frequency range of 50 MHz to 3 000 MHz if the system supports SATA devices using Gen2i levels (see SATA) and the receiver device does not support SATA Gen2i levels through the TCTF test load (see table 54 in 5.8.5.4).

For untrained 1.5 Gbit/s and 3 Gbit/s, each passive TxRx connection shall meet the delivered signal specifications in table 54 (see 5.8.5.4).

For untrained 6 Gbit/s (i.e., SATA devices using Gen3i levels (see SATA)), then the internal passive TxRx connection should be less than the CIC (see SATA). See SATA for delivered signal specifications.

For external cable assemblies, these electrical requirements are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included in the TxRx connection.

5.5.5 Passive TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the passive TxRx connection shall support a bit error ratio (BER) that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based on simulation results using:

a) S-parameter measurements of the passive TxRx connection;
b) the reference transmitter device (see 5.8.4.6.5); and
c) the reference receiver device (see 5.8.5.7.3).

The simulation shall not include sources of crosstalk. Since simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} is expected to yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e., the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 98 shows an example circuit for simulation. The specific simulation program used is not specified by this document. Annex C includes the StatEye program from http://www.stateye.org, which is one such simulation program.

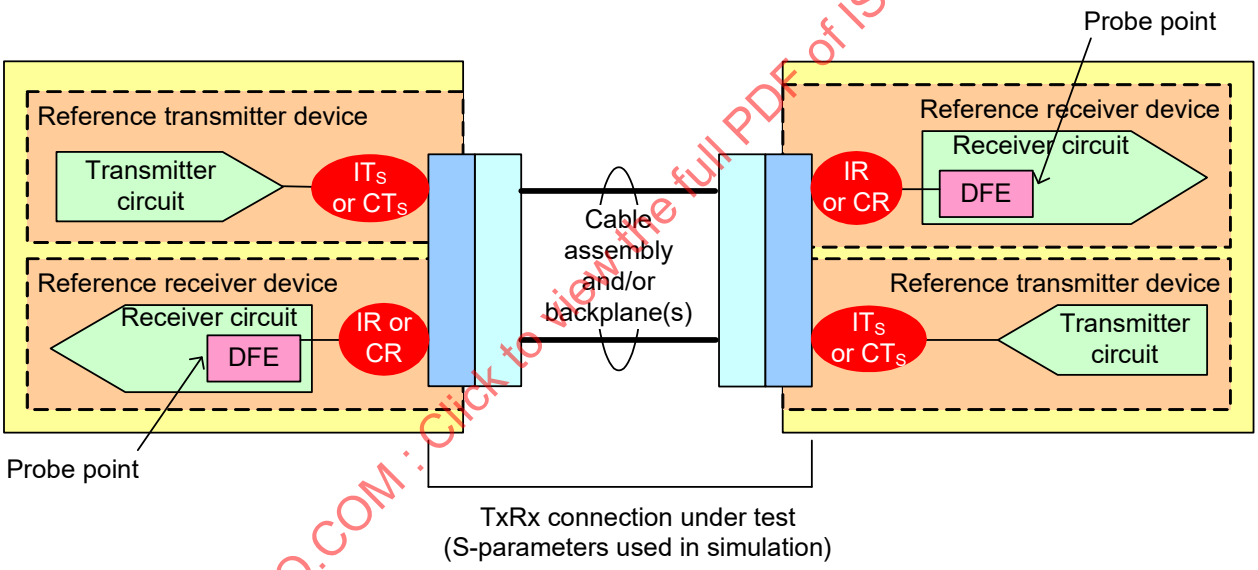


Figure 98 – Example of a passive TxRx connection compliance testing for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Table 26 defines the required passive TxRx connection characteristics.

Table 26 – Passive TxRx connection characteristics for trained 6 Gbit/s

Characteristic	Units	6 Gbit/s
Minimum voltage [a]	mV(P-P)	84
Maximum TJ [a]	UI	0.64

[a] As reported by simulation of the passive TxRx connection S-parameters with the reference transmitter device and the reference receiver device. Values are reported at a BER of 10^{-15} inside the reference receiver device after equalization at 6 Gbit/s. This document does not define values for trained 3 Gbit/s and 1.5 Gbit/s. Passive TxRx connections that comply with the 6 Gbit/s characteristics are expected to operate correctly at slower physical link rates.

For external cable assemblies, these electrical requirements are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 10 m long, provided that no other TxRx connection segments are included in the TxRx connection.

A passive TxRx connection supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s may not support untrained 1.5 Gbit/s and 3 Gbit/s and may not support SATA. Trained transceiver devices incorporate features to allow them to operate over the following passive TxRx connections:

a) passive TxRx connections with higher loss than TxRx connections;
b) passive TxRx connections defined in this document for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4); and
c) passive TxRx connections supporting SATA.

5.5.6 Passive TxRx connection characteristics for trained 12 Gbit/s

For trained 12 Gbit/s, the passive TxRx connection shall support a BER that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based on end to end simulation results (see 5.7.1) using:

a) S-parameter measurements or model of the passive TxRx connection segment from CT_S to CR or IT_S to IR (see figure 13);
b) S-parameter measurements of the passive connection, S-parameter models of the passive connection, or reference S-parameter models (see clause D.2) from all significant crosstalk aggressors;
c) reference transmitter devices (see 5.8.4.7.3) providing signals to the through channel and crosstalk channels:
   A) using the reference transmitter device peak to peak voltage defined in table 47;
   B) using reference equalization coefficients (see 5.7.4); and
   C) generating no RJ or TJ;
d) the reference receiver device with optimal DFE weights (see 5.8.5.7.3 and table 27); and
e) reference S-parameter models to complete the simulation diagram (see figure 99), according to the appropriate usage model (see D.2.3).

The simulation shall include all significant crosstalk sources. The crosstalk sources shall be modeled as asynchronous to the TxRx connection segment under test (see clause D.1).

Simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} is expected to yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e. the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 99 shows an example TxRx connection for trained 12 Gbit/s.The TxRx connection segment under test is the segment between CT_S and CR or IT_S and IR. XCS_n represents the crosstalk connection segments, where n is a numerical index identifying multiple crosstalk aggressors.

The specific simulation program used is not specified by this document. See Annex D and Annex E.

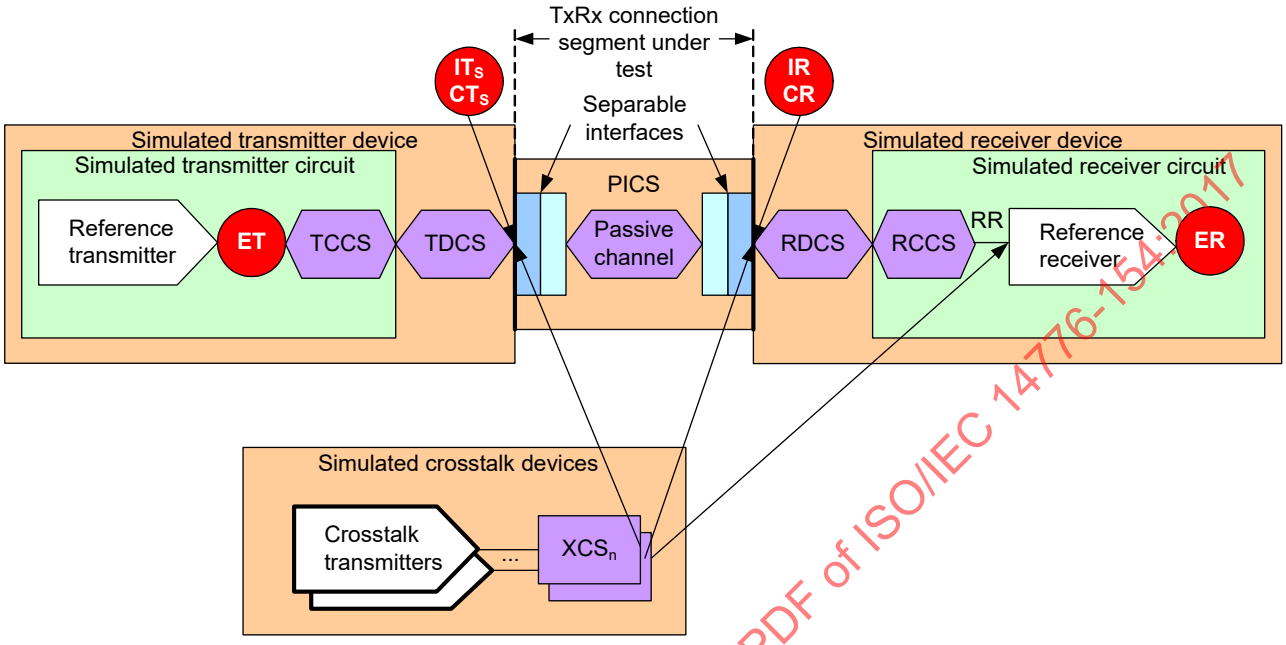


Figure 99 – Example passive TxRx connection compliance testing for trained 12 Gbit/s

The following reference through S-parameter files shall be used for this simulation, according to the appropriate usage model:

a) **<usage>_ET_ITs.s4p**: through between ET and CT_S or between ET and IT_S; and
b) **<usage>_CR_RR.s4p**: through between CR and RR or between IR and RR.

Labels beginning by <usage> indicate reference S-parameter files. <usage> represents a prefix that is set according to the selected usage model (see D.2.3). RR is the receiver die attachment point to RCCS.

Symmetrical models have the same through transfer function between ET and CT_S or between ET and IT_S as between CR and RR or between IR and RR. Symmetrical models shall use the same transfer function for both directions (i.e., **<usage>_ET_ITs.s4p**).

Asymmetrical models do not have the same through transfer function between ET and CT_S or between ET and IT_S as between CR and RR or between IR and RR. For asymmetrical models, the reverse transfer function between ET and CT_S or between ET and IT_S shall also be used (i.e., **<usage>_ET_ITs_rev.s4p**).

For each usage model, four types of crosstalk aggressor reference S-parameter files are defined for this simulation:

a) **<usage>_ET_ITs_FEXT.s4p**: crosstalk caused by elements between ET and CT_S or between ET and IT_S;
b) **<usage>_CR_RR_FEXT.s4p**: crosstalk caused by elements between CR and RR or between IR and RR;
c) **<usage>_CR_RR_NEXT.s4p**: crosstalk caused by elements between CR and RR or between IR and RR; and
d) **<usage>_ET_ITs_NEXT.s4p**: crosstalk caused by elements between ET and CT_S or between ET and IT_S.

Figure 100 shows the usage of the crosstalk and through files defined for the end to end simulation of TxRx connection segments between CT_S and CR or IT_S and IR. The boxes labeled PICS FEXT, PICS NEXT, PICS rev, and PICS indicate measured transfer functions (e.g., S-parameters). The boxes with a dashed boundary indicate reference S-parameter files. <usage> represents a prefix that is set according to the selected usage model (see D.2.3).

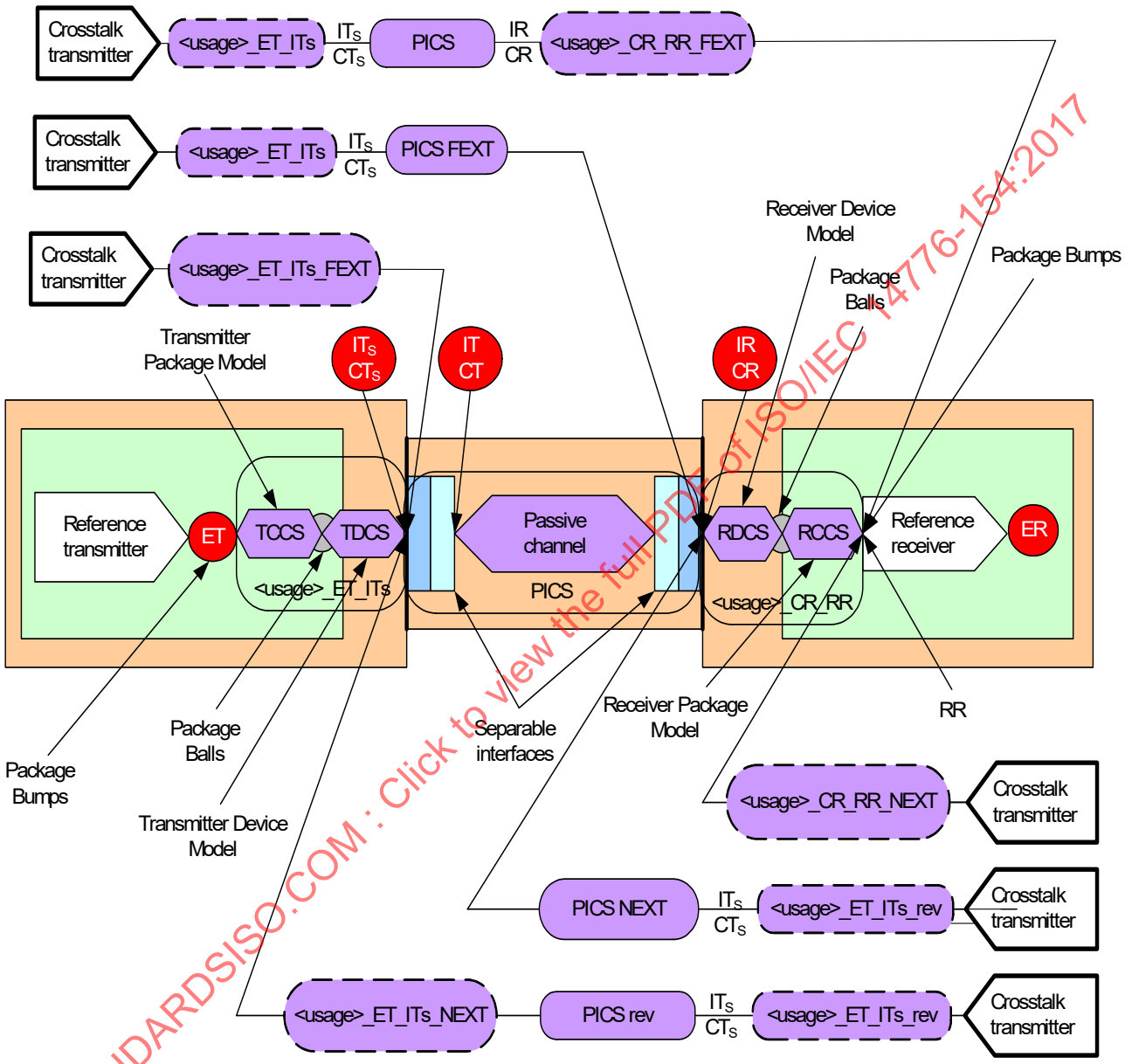


Figure 100 – Passive TxRx connection segment between CT_S and CR or IT_S and IR end to end simulation diagram for trained 12 Gbit/s

Table 27 defines the required passive TxRx connection characteristics. Refer to the reference transmitter device (see 5.8.4.7.3) for definitions of coefficient 1 (i.e., C1), coefficient 2 (i.e., C2), and coefficient 3 (i.e., C3) used in table 27.

Table 27 – Passive TxRx connection characteristics for trained 12 Gbit/s at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Coefficient 1 (i.e., C1) [a b c]	V/V	-0.15	0	ET
VMA [d e]	mV(P-P)	80		ET
Coefficient 3 (i.e., C3) [a b f]	V/V	-0.3	0	ET
Reference pulse response cursor peak to peak amplitude [g]	mV(P-P)	135		ER
Vertical eye opening to reference pulse response cursor ratio [h i]	%	45		ER
DFE coefficient amplitude to reference pulse response cursor ratio [j]	%	-50	50	ER

[a] If C1 or C3 exceeds its maximum (positive) limit, then that coefficient is forced to its maximum limit and the other coefficients are recalculated.

[b] C2 = 1 - |C1| - |C3|.

[c] If C1 exceeds its minimum (negative) limit, then that coefficient is forced to its minimum limit and C3 is recalculated.

[d] $VMA = 2K_0 (C1 + C2 + C3)$
where:
K_0 is the output gain;
C1 is coefficient 1 (see 5.8.4.7.3);
C2 is coefficient 2 (see 5.8.4.7.3); and
C3 is coefficient 3 (see 5.8.4.7.3).

[e] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (C3' - C3^2))^{0.5}$$

where:
C1' and C3' are values that satisfy the minimum VMA criterion.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 118.

[h] The vertical eye opening includes the effects of crosstalk (see clause D.1).

[i] The end to end simulation removes any remaining RJ and TJ (i.e., non-ISI) of the transmitter device.

[j] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(di)) divided by the reference pulse response cursor) (see 5.8.5.7.3).

For external cable assemblies, these electrical requirements are consistent with using good quality passive Mini SAS HD cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included between CT_S and CR in the TxRx connection and the total ICR is below the limit specified in table 25.

5.5.7 TxRx connection characteristics for active cable assemblies

5.5.7.1 Active cable assembly electrical characteristics for trained 6 Gbit/s overview

Active cable assemblies shall support a bit error ratio (BER) that is less than 10^{-12} when used with transmitter devices and trained receiver devices defined in 5.8.

In addition to complying with electrical characteristics necessary for the required BER performance, active cable assemblies shall comply with the OOB signaling defined in 5.11. The circuitry incorporated in unmanaged cable assemblies shall operate in the D.C. mode. Managed active cable assemblies supporting 6 Gbit/s operation may operate in the D.C. mode or in the optical mode (see 5.11). The circuitry incorporated in active cable assemblies shall preserve OOB signals with response times that support the OOB signal receiver device detection requirements in table 78 (see 5.11.3).

5.5.7.2 Active cable assembly output electrical characteristics for trained 6 Gbit/s

Table 28 defines active cable assembly output electrical characteristics for trained 6 Gbit/s.

Table 28 – Active cable assembly output electrical characteristics for trained 6 Gbit/s

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage	mV (P-P)	400		1 200
RJ [a b d]	UI			0.22
TJ [a c d]	UI			0.56

[a] Based on TX input per table 37 (see 5.8.4.6.1) and recommended TX interoperability settings per table 40 (see 5.8.4.6.4).
[b] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[c] The TJ measurement shall be performed with at least 58 dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC enabled.
[d] The measurement shall include the effects of the JTF (see 5.8.3.2).

For active cable assemblies, these characteristics are consistent with good quality half-active (i.e., with circuitry only on the receive end of the assembly) cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 25 m long, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbit/s and 3 Gbit/s. Active cables that comply with trained 6 Gbit/s characteristics should operate within the specified error rate at slower physical link rates.

5.5.7.3 Active cable assembly S-parameter limits for trained 6 Gbit/s and trained 12 Gbit/s

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × $\log_{10}$(f / 3 GHz)]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 29 defines the maximum limits for S-parameters of the active cable assembly.

Table 29 – Maximum limits for S-parameters for active cable assemblies

Characteristic [a] [b]	L [c] dB	N [c] dB	H [c] dB	S [c] dB / decade	f_{min} [c] MHz	f_{max} [c] [d] GHz	f_{max} [c] [e] GHz
$\lvert S_{CC22} \rvert$ [f]	-6.0	-5.0	-1.0	13.3	100	6.0	9.0
$\lvert S_{DD11} \rvert$, $\lvert S_{DD22} \rvert$ [f]	-10	-7.9	-3.9	13.3	100	6.0	9.0
$\lvert S_{CD11} \rvert$, $\lvert S_{CD22} \rvert$ [f]	-20	-12.7	-10	13.3	100	6.0	9.0

[a] Power shall be applied to the active cable assembly during these measurements.
[b] $\lvert S_{CC11} \rvert$, $\lvert S_{DC11} \rvert$ and $\lvert S_{DC22} \rvert$ are not specified.
[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.
[d] Applies for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.
[e] Applies for 12 Gbit/s.
[f] For $\lvert S_{CC22} \rvert$, $\lvert S_{DD22} \rvert$ and $\lvert S_{CD22} \rvert$ measurements, the transmitter device attached to the active cable assembly under test shall transmit a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See F.11.4.4 and F.11.4.5

Figure 101 shows the active cable assembly $|S_{CC22}|$, $|S_{DD11}|$, $|S_{DD22}|$, $|S_{CD11}|$ and $|S_{CD22}|$ limits defined in table 29.

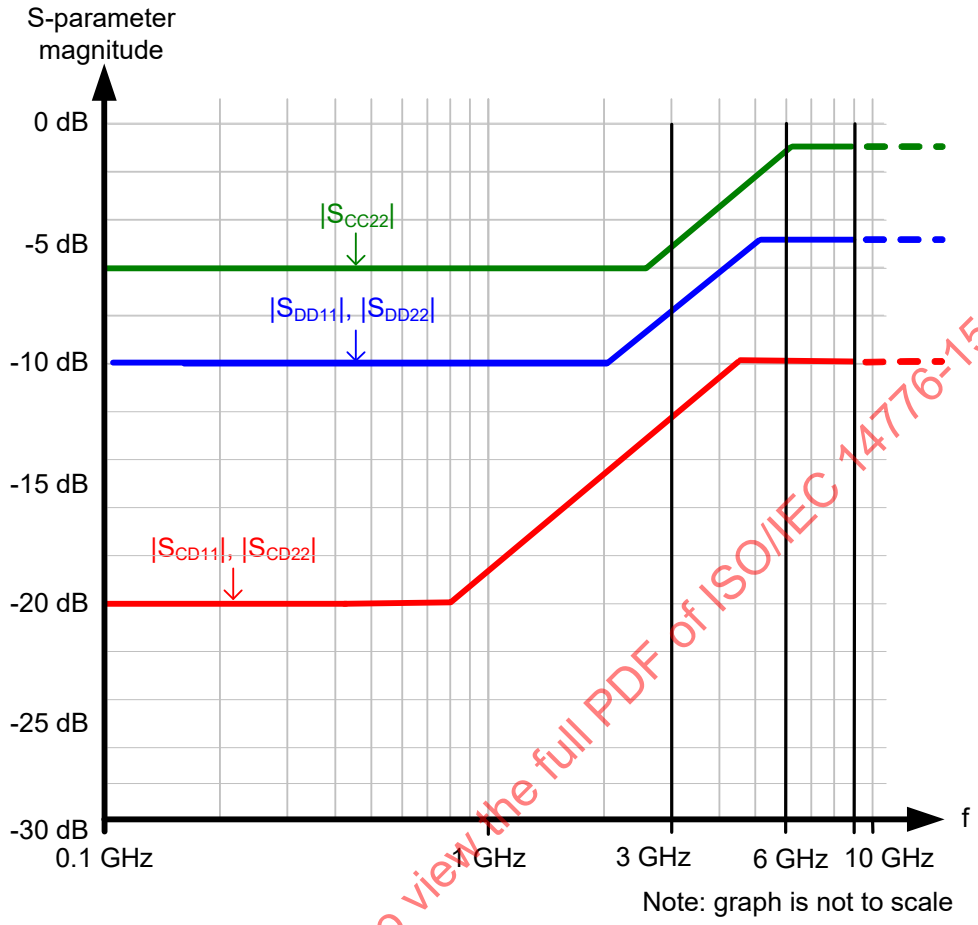


Figure 101 – Active cable S-parameter limits

5.5.7.4 Active cable assembly electrical characteristics overview for 12 Gbit/s

Active cable assemblies supporting 12 Gbit/s operation shall comply with OOB in the optical mode (see 5.11) and shall support pass through of SSC. The optical mode does not support transmitter training. The circuitry incorporated in these cable assemblies preserves OOB signals with response times that support the OOB signal receiver device detection requirements in table 78 (see 5.11.3).

5.5.7.5 Active cable assembly electrical characteristics for 12 Gbit/s

Figure 102 describes the eye mask used to calibrate the input in an active cable assembly at CT_S (see figure 14) to test the output of an active cable assembly at CR (see figure 14) for 12 Gbit/s.

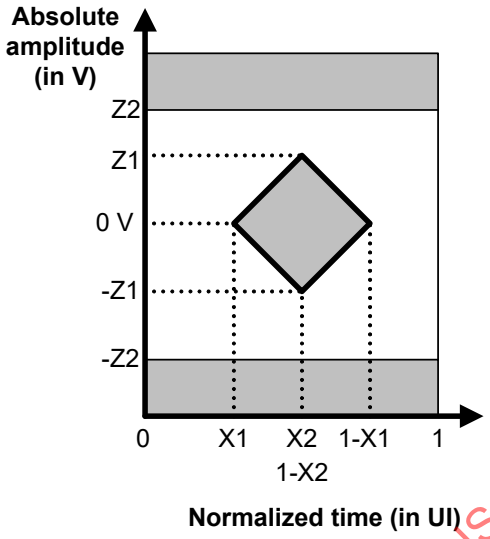


Figure 102 – Active cable eye mask for 12 Gbit/s

Table 30 defines the signal input and output characteristics for an active cable assembly for 12 Gbit/s.

Table 30 – Active cable assembly electrical characteristics for 12 Gbit/s

Signal characteristic	Units	CT_S [a]	CR
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 102) [b c d]	mV(P-P)	1 200	1 200
Minimum eye opening (i.e., 2 × Z1 in figure 102) [b c e]	mV(P-P)	200	360
Maximum half of TJ (i.e., X1 in figure 102) [b c e f]	UI	0.175	0.35
Maximum RJ [b d f g]	UI	0.15	0.45
Center of bit time (i.e., X2 in figure 102)	UI	0.5	0.5

[a] This column represents signal input characteristics to a cable assembly under test.
[b] All crosstalk sources shall be active with representative traffic during the measurement.
[c] Maximum TJ at CT_S and maximum RJ at CT_S shall be applied during this measurement.
[d] The maximum peak to peak voltage measurement and RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[e] The minimum eye opening measurement and TJ measurement shall be performed with the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC enabled for a period of at least 33.3 µs (i.e., a full SSC cycle).
[f] The measurement shall include the effects of the JTF (see 5.8.3.2).
[g] The maximum RJ at CT_S shall be applied during this measurement.

For active cable assemblies, these characteristics are consistent with good quality full-active cable assemblies (i.e., with circuitry on both ends of each differential signal pair of the cable assembly) constructed with shielded twinaxial cable with 26 AWG solid wire up to 15 m or optical cable assemblies up to 100 m, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbit/s and 3 Gbit/s. Active cable assemblies that comply with active cable assembly electrical characteristics for 12 Gbit/s characteristics should also comply with active cable assembly electrical characteristics for 6 Gbit/s (see 5.5.7) with optical mode enabled and should operate within the specified bit error ratio at slower physical link rates.

5.6 Test loads

5.6.1 Test loads overview

This document uses a test load methodology to specify transmitter device signal output characteristics (see 5.8.4.4 and 5.8.4.5) and delivered signal characteristics (see 5.8.5.4). This methodology specifies the signal as measured at specified probe points in specified test loads.

For untrained 1.5 Gbit/s and 3 Gbit/s (e.g., the physical link rate is negotiated in Final-SNW (see SPL-3) or the physical link is SATA), the test loads used by the methodology are:

a) zero-length test load (see 5.6.2): used for testing transmitter device compliance points and receiver device compliance points;
b) transmitter compliance transfer function (TCTF) test load (see 5.6.3): used for testing transmitter device compliance points;
c) low-loss TCTF test load (see 5.6.4): used for testing transmitter device compliance points if SATA devices using Gen2i levels (see SATA) are supported and the SAS receiver device does not support the signal levels received through a full TCTF test load (see 5.6.3); and
d) CIC (see SATA): used for testing transmitter device compliance points if SATA devices using Gen3i levels (see SATA) are supported.

For trained (e.g., the physical link rate is negotiated in Train_Rx-SNW (see SPL-3)) 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the test loads used by the methodology are:

a) zero-length test load (see 5.6.2) used for:
   A) testing transmitter device compliance points;
   B) testing receiver device compliance points; and
   C) used with a reference receiver device (see 5.8.5.7.3) in simulation to determine the delivered signal;

   and
b) reference transmitter test load (see 5.6.5): used with a reference receiver device (see 5.8.5.7.3) in simulation to determine the delivered signal.

For 12 Gbit/s, the zero-length test load (see 5.6.2) test load is used for:

a) testing transmitter device compliance points;
b) testing receiver device compliance points;
c) measuring crosstalk; and
d) capturing signals for use in simulation.

In addition to measurement with the zero-length test load, 12 Gbit/s may end use to end simulation and, depending on the usage model, use reference transfer functions to determine the delivered signal. See 5.7 and Annex D.

Physical positions denoted as probe points identify the position in the test load where the signal properties are measured, but do not imply that physical probing is used for the measurement. Physical probing may be disruptive to the signal and should not be used unless verified to be non-disruptive.

5.6.2 Zero-length test load

Figure 103 shows the zero-length test load as used for testing a transmitter device compliance point.

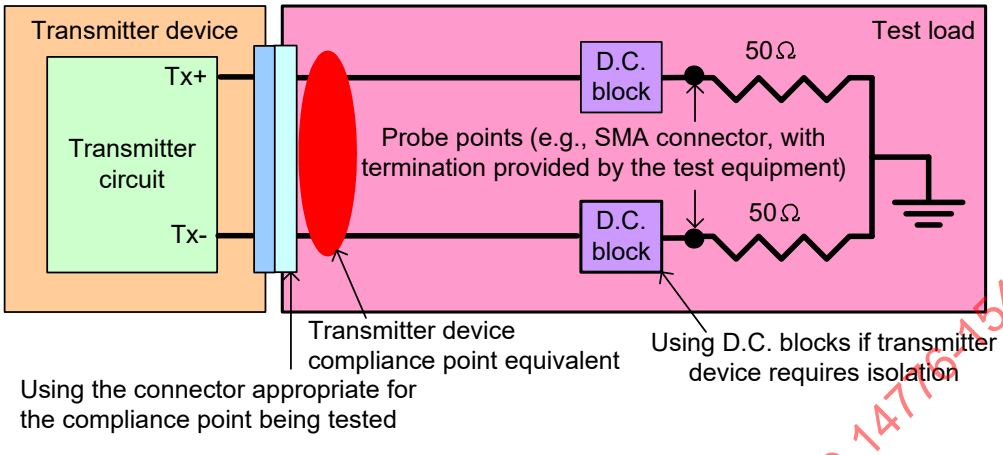


Figure 103 – Zero-length test load for transmitter device compliance point

Figure 104 shows the zero-length test load as used for testing a receiver device compliance point.

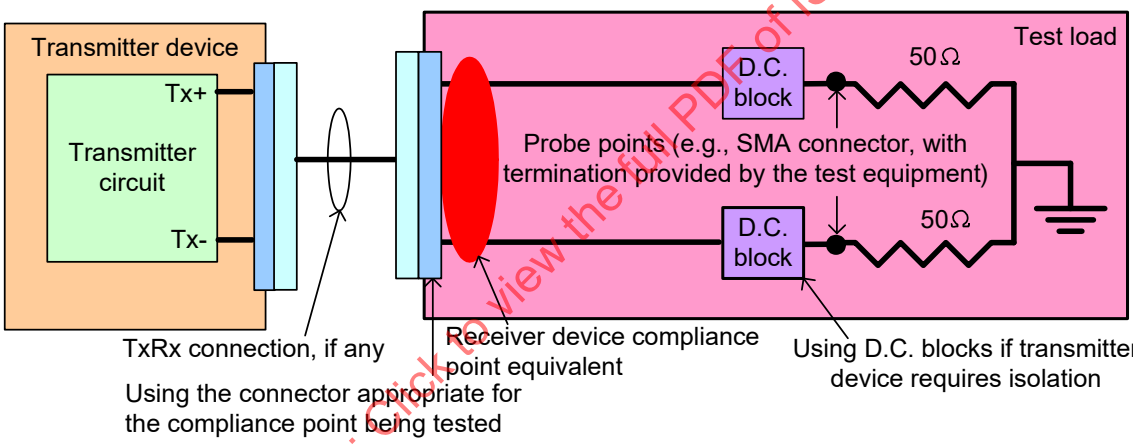


Figure 104 – Zero-length test load for receiver device compliance point

Figure 103 and figure 104 show ideal designs. Implementations may include:

a) insertion loss between the compliance and probe points; and
b) return loss due one or more impedance mismatches between the compliance point and 50 Ω termination points.

Not shown are non-ideal effects of the test equipment raw measurements (e.g., additional insertion loss and return loss). For de-embedding methods to remove non-ideal effects, see Annex F.

Usage of fixturing and test equipment shall comply with the requirements defined in this subclause. The requirements in this subclause include the combined effects of the fixturing and test equipment.

The zero-length test load is defined by a set of S-parameters (see clause F.11). Only the magnitude of $S_{DD21}(f)$ and the magnitude of $S_{DD11}(f)$ are specified by this document.

The zero-length test load, including all fixturing and instrumentation required for the measurement, shall comply with the following equations:

For 50 MHz < f ≤ 6.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.0 \times 10^{-6} \times f^{0.5}) + (2.8 \times 10^{-11} \times f) + (5.3 \times 10^{-21} \times f^{2})) - 0.2 \text{ dB}$$

$$|S_{DD11}(f)| \leq -15 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$;

$|S_{DD11}(f)|$ magnitude of $S_{DD11}(f)$; and

f signal frequency in Hz.

Figure 105 shows the allowable $|S_{DD21}(f)|$ of a zero-length test load and the $|S_{DD21}(f)|$ of a sample zero-length test load.

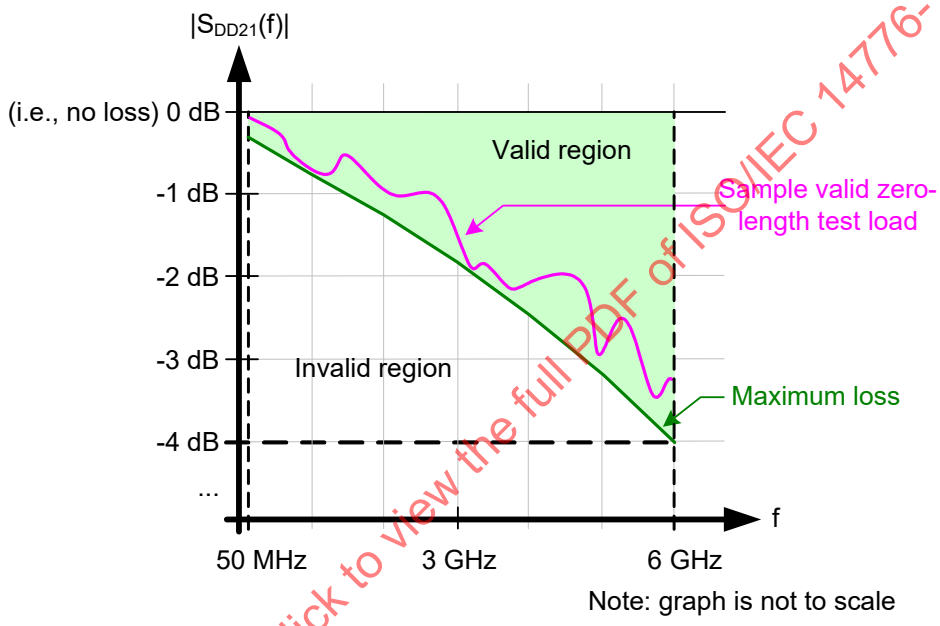


Figure 105 – Zero-length test load $|S_{DD21}(f)|$ requirements

5.6.3 TCTF test load

Figure 106 shows the TCTF test load. This test load is used for untrained 1.5 Gbit/s and 3 Gbit/s characterization.

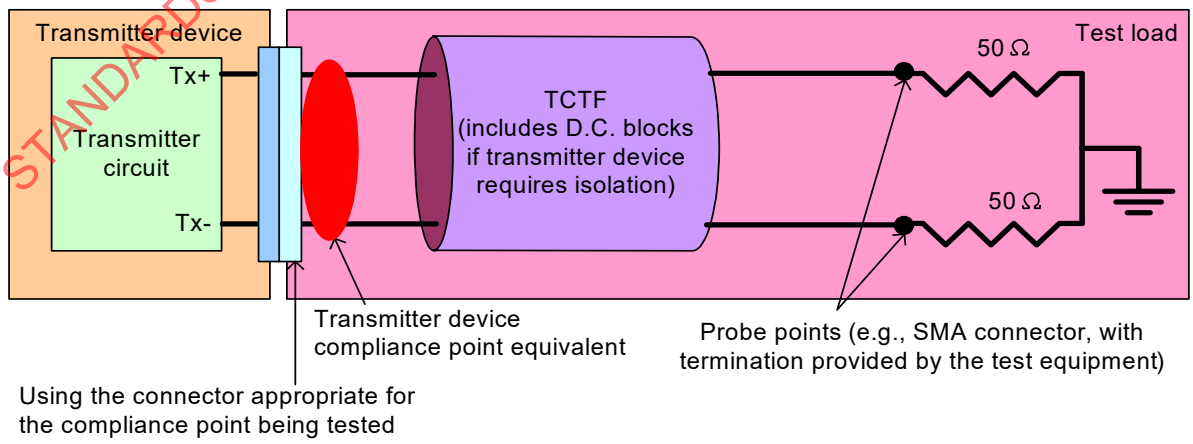


Figure 106 – TCTF test load

The TCTF test load shall meet the requirements in 5.5.2. The nominal impedance shall be the target impedance.

The TCTF test load is defined by a set of S-parameters (see clause F.11). Only the magnitude of $S_{DD21}(f)$ is specified by this document.

For testing an untrained 3 Gbit/s transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((6.5 \times 10^{-6} \times f^{0.5}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^{2})) \text{ dB}$$

and for 3.0 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -10.9 \text{ dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 300 \text{ MHz})| - |S_{DD21}(f = 1\,500 \text{ MHz})| > 3.9 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 107 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 3 Gbit/s.

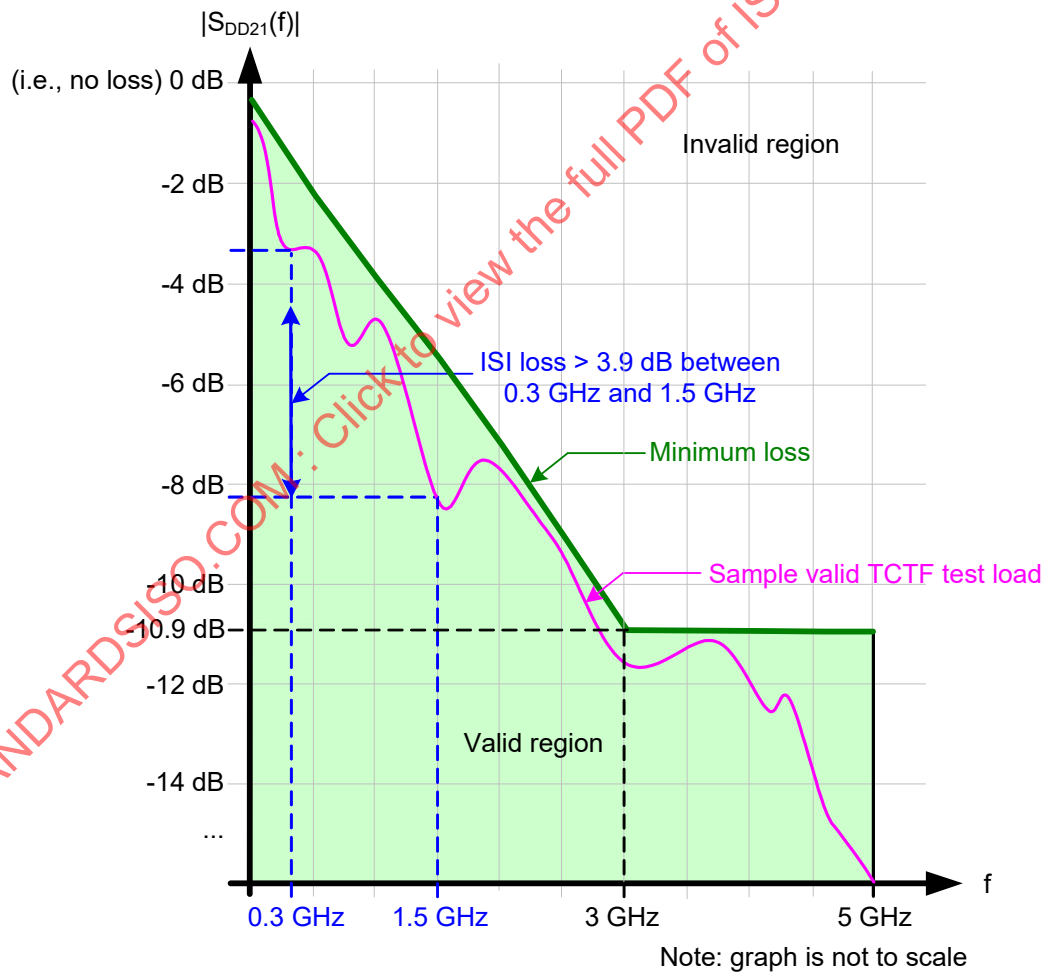


Figure 107 – TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 3 Gbit/s

For testing an untrained 3 Gbit/s transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.7 \times 10^{-5} \times f^{0.5}) + (1.0 \times 10^{-10} \times f)) \text{ dB}$$

and for 3.0 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -10.7 \text{ dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 300 \text{ MHz})| - |S_{DD21}(f = 1\,500 \text{ MHz})| > 3.9 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 108 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 3 Gbit/s.

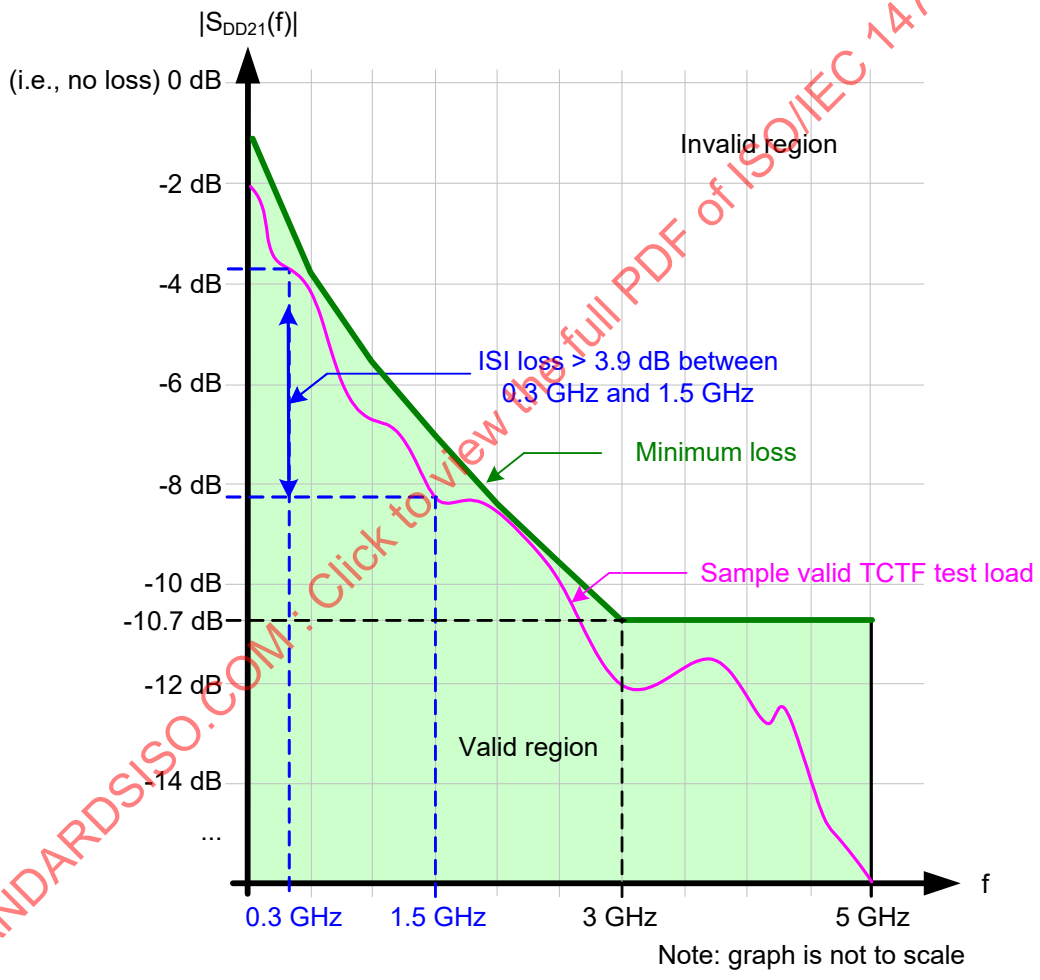


Figure 108 – TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 3 Gbit/s

For testing an untrained 1.5 Gbit/s transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((6.5 \times 10^{-6} \times f^{0.5}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^{2}))\ \text{dB}$$

and for 1.5 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -5.4\ \text{dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 150\ \text{MHz})| - |S_{DD21}(f = 750\ \text{MHz})| > 2.0\ \text{dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 109 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 1.5 Gbit/s.

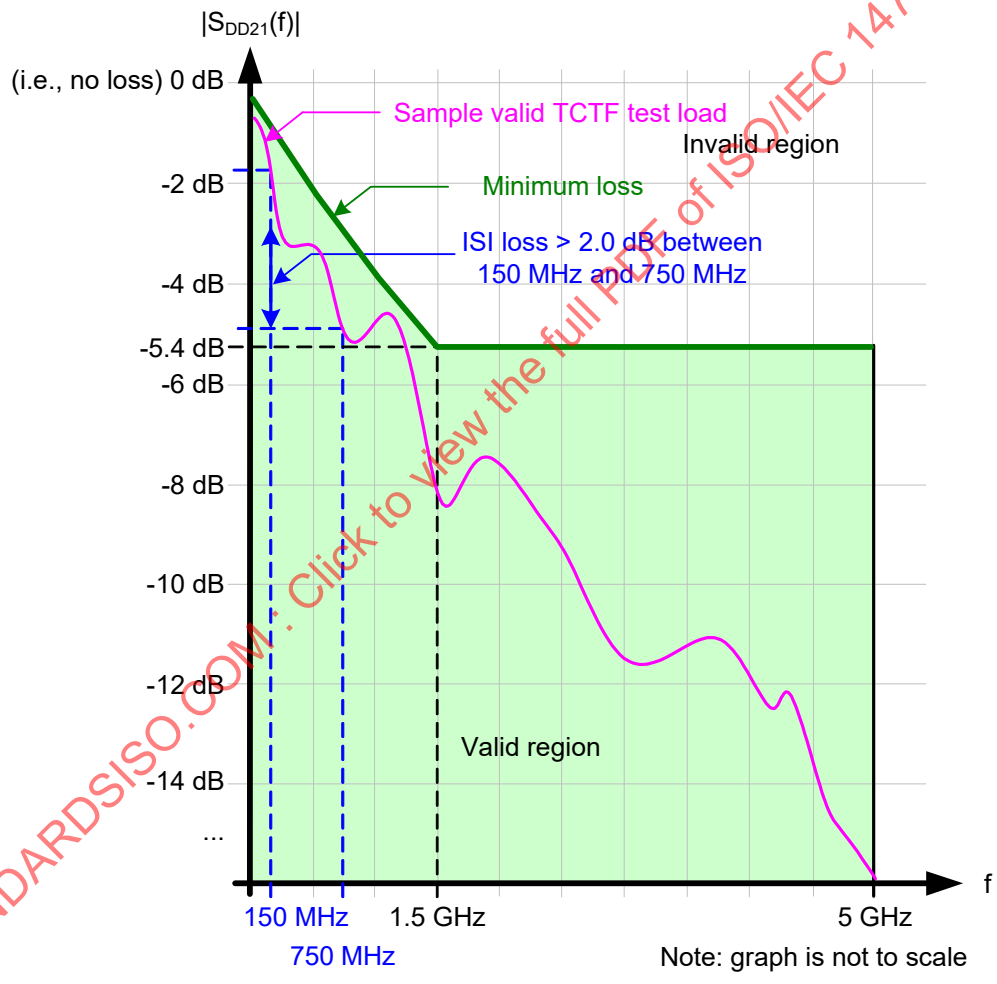


Figure 109 – TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 1.5 Gbit/s

For testing an untrained 1.5 Gbit/s transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.7 \times 10^{-5} \times f^{0.5}) + (1.0 \times 10^{-10} \times f)) \text{ dB}$$

and for 1.5 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -7.0 \text{ dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 150 \text{ MHz})| - |S_{DD21}(f = 750 \text{ MHz})| > 2.0 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 110 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 1.5 Gbit/s.

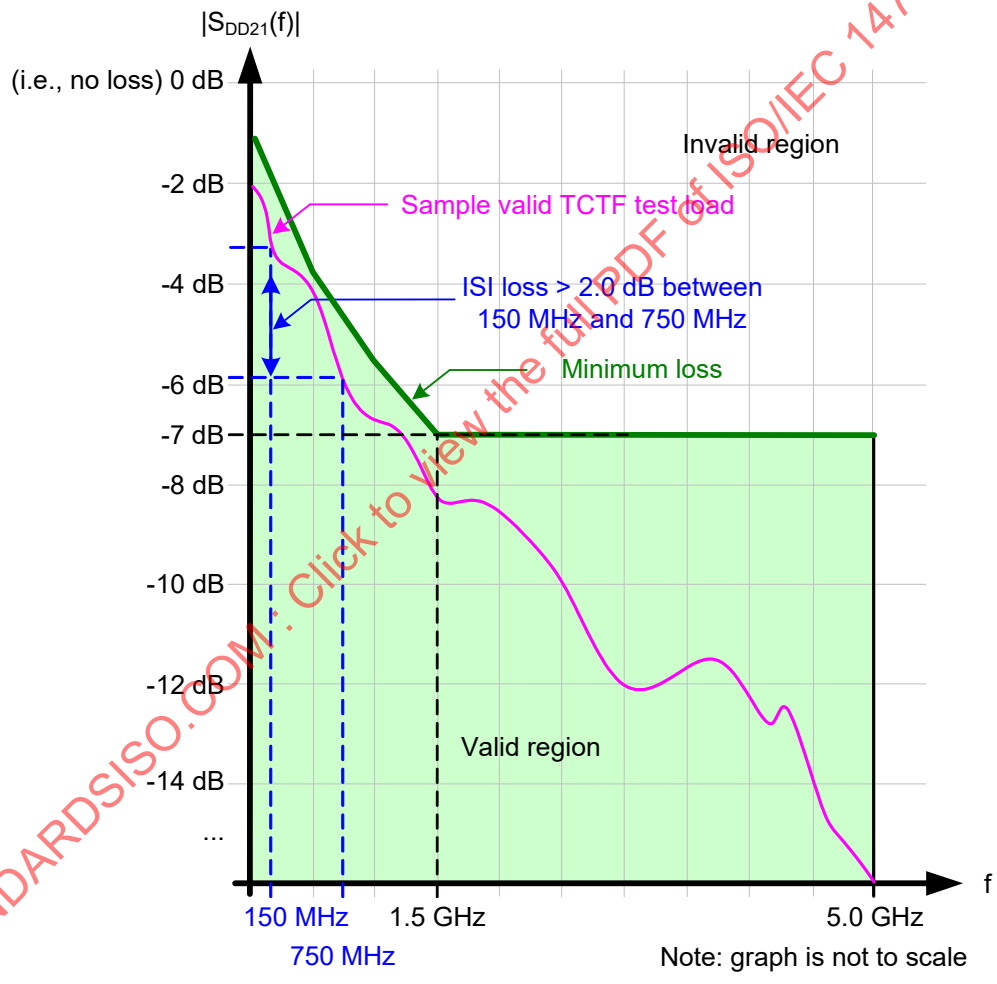


Figure 110 – TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 1.5 Gbit/s

5.6.4 Low-loss TCTF test load

Figure 111 shows the low-loss TCTF test load. This test load is used for untrained 1.5 Gbit/s and 3 Gbit/s characterization.

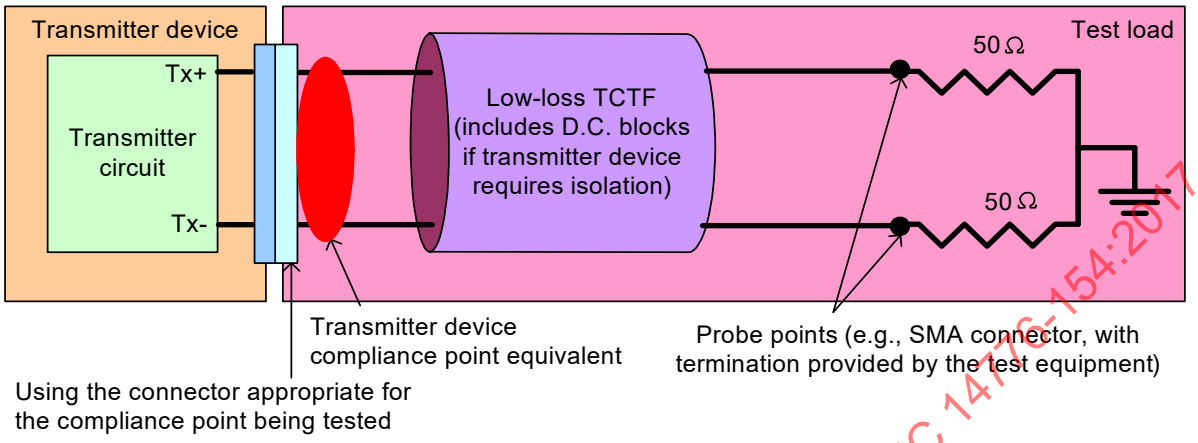


Figure 111 – Low-loss TCTF test load

The low-loss TCTF test load shall meet the requirements defined in 5.5.2. The nominal impedance shall be the target impedance.

The low-loss TCTF test load is defined by a set of S-parameters (see clause F.11). Only the magnitude of $S_{DD21}(f)$ is specified by this document.

The low-loss TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((2.2 \times 10^{-6} \times f^{0.5}) + (6.9 \times 10^{-11} \times f) + (1.1 \times 10^{-20} \times f^{2})) \text{ dB}$$

for 3.0 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -3.7 \text{ dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 300 \text{ MHz})| - |S_{DD21}(f = 1\,500 \text{ MHz})| > 1.3 \text{ dB}$$

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 112 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a low-loss TCTF test load and the $|S_{DD21}(f)|$ of a sample low-loss TCTF test load.

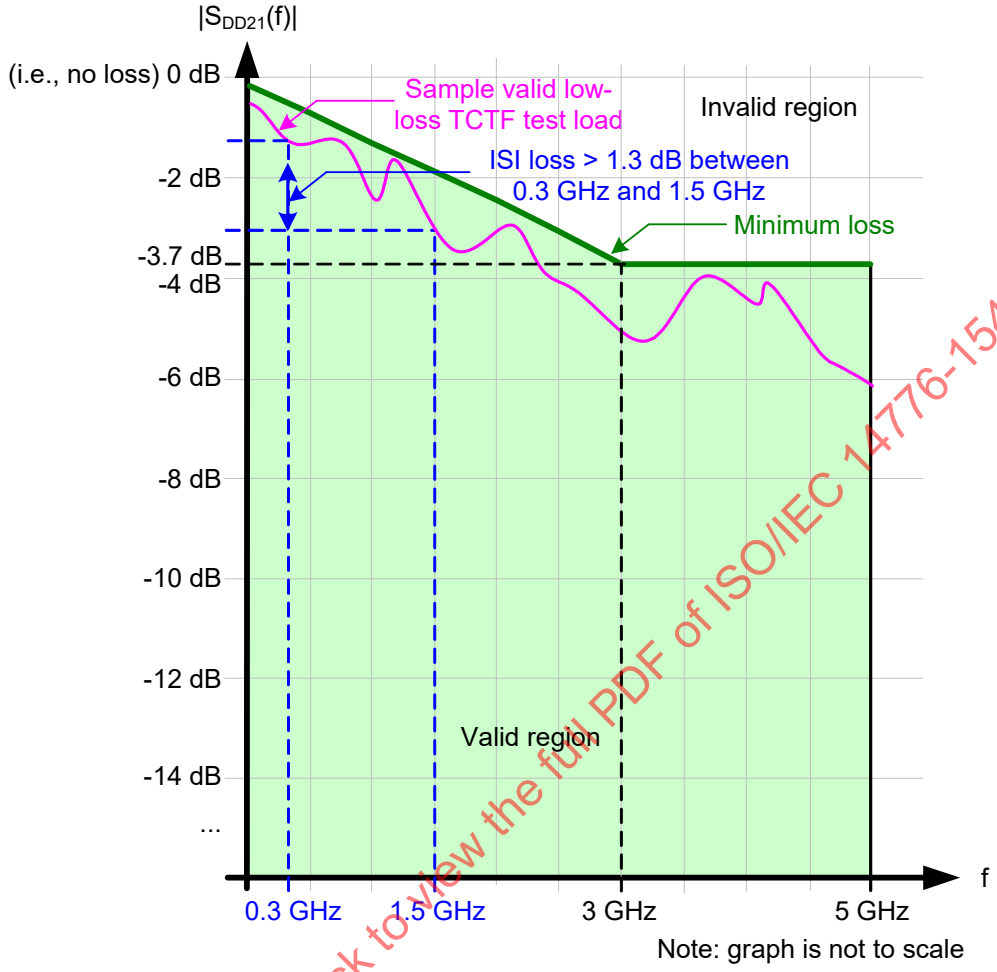


Figure 112 – Low-loss TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements

5.6.5 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load

The reference transmitter test load for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is a set of parameters defining the electrical performance characteristics of a 10 m Mini SAS 4x cable assembly, used:

a) in simulation to determine compliance of a transmitter device (see 5.8.4.6); and
b) as a representative component of an ISI generator used to determine compliance of a receiver device (see 5.8.5.7.6).

The following Touchstone model of the reference transmitter test load is included in this document:

a) SAS2_transmittertestload.s4p.

See Annex G for a description of how the Touchstone model was created.

Figure 113 shows the reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz.

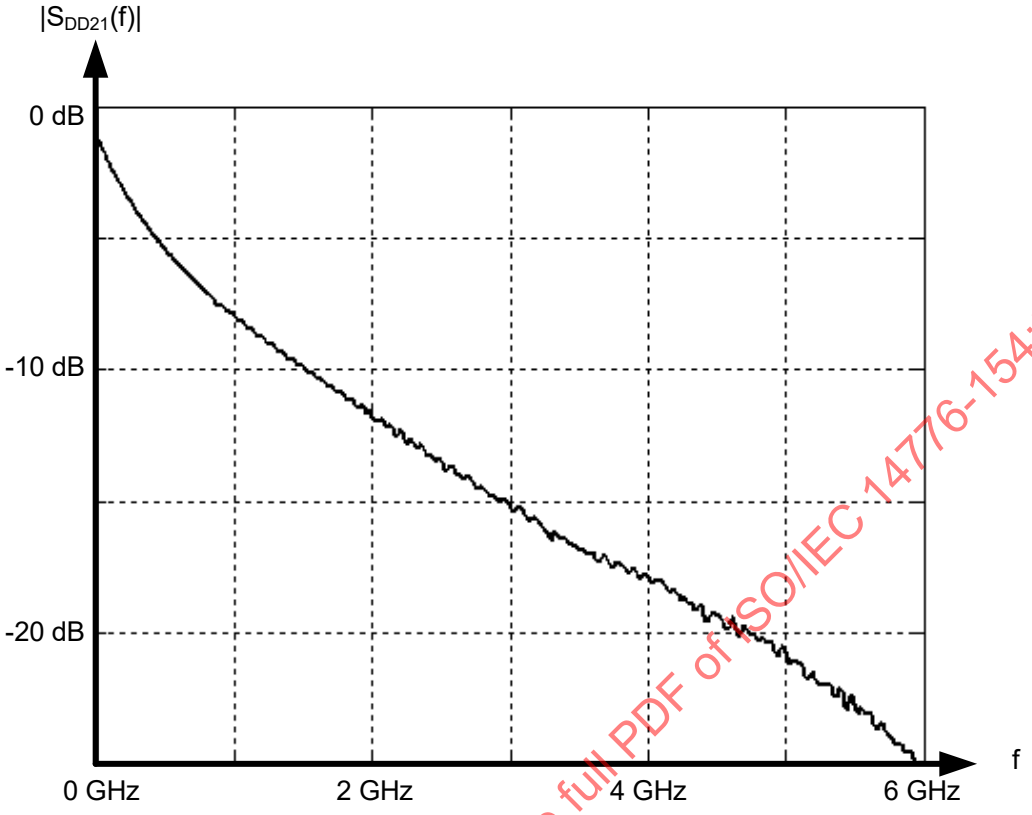


Figure 113 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter with a test load $|S_{DD21}(f)|$ up to 6 GHz

Figure 114 shows the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load pulse response.

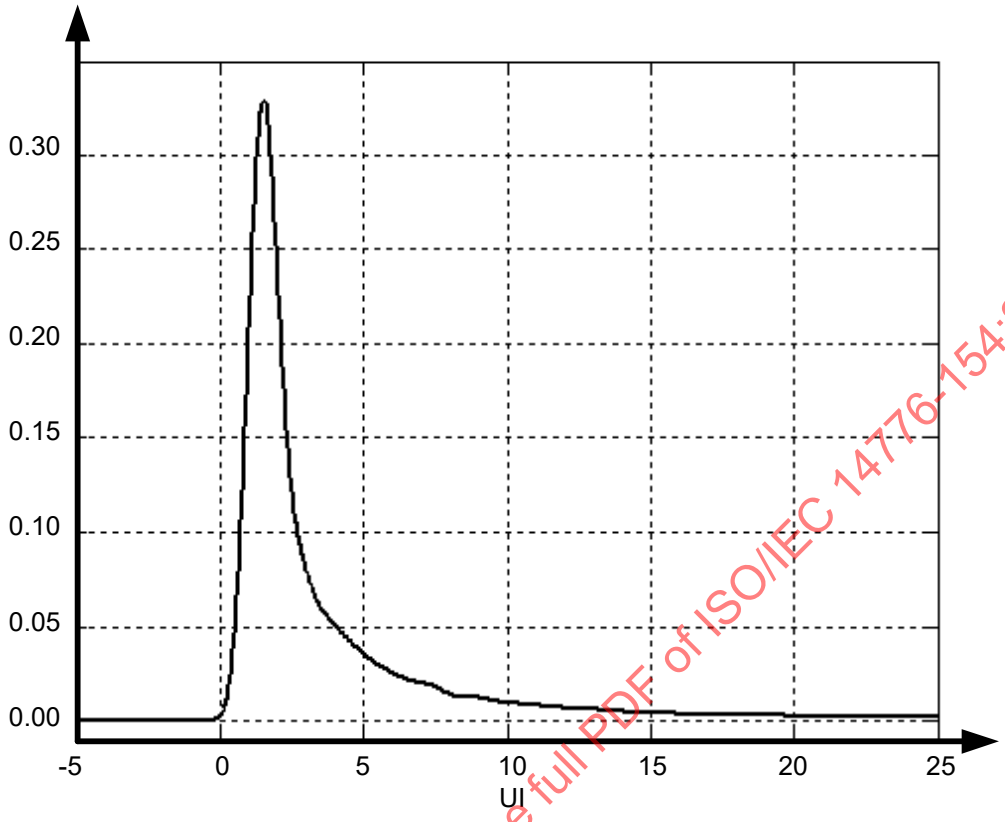


Figure 114 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load pulse response

The following impulse response model of the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load is included with this document:

a) sas2_stressor_6g0_16x.txt.

Figure 115 shows the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load impulse response found in the sas2_stressor_6g0_16x.txt.

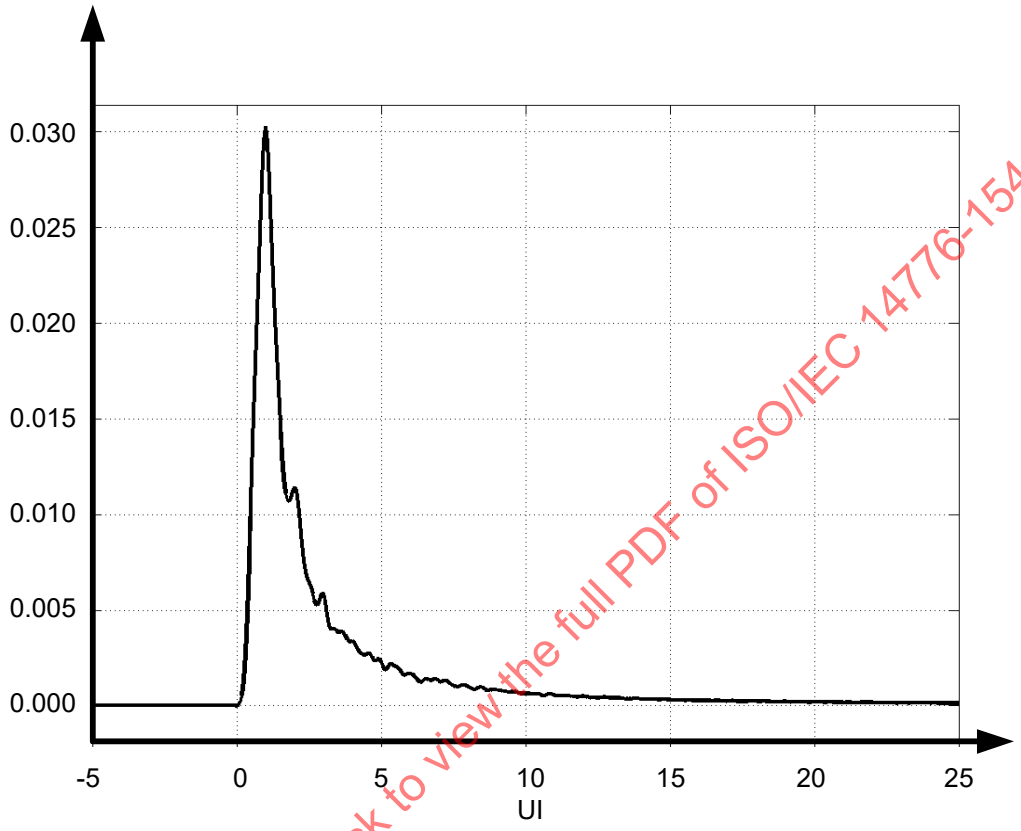


Figure 115 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load impulse response for 6 Gbit/s

Figure 116 shows the trained 1.5 Gbit/s, 3 Gbit/s, an 6 Gbit/s reference transmitter test load repeating 0011b pattern or 1100b pattern (e.g., D24.3) response.

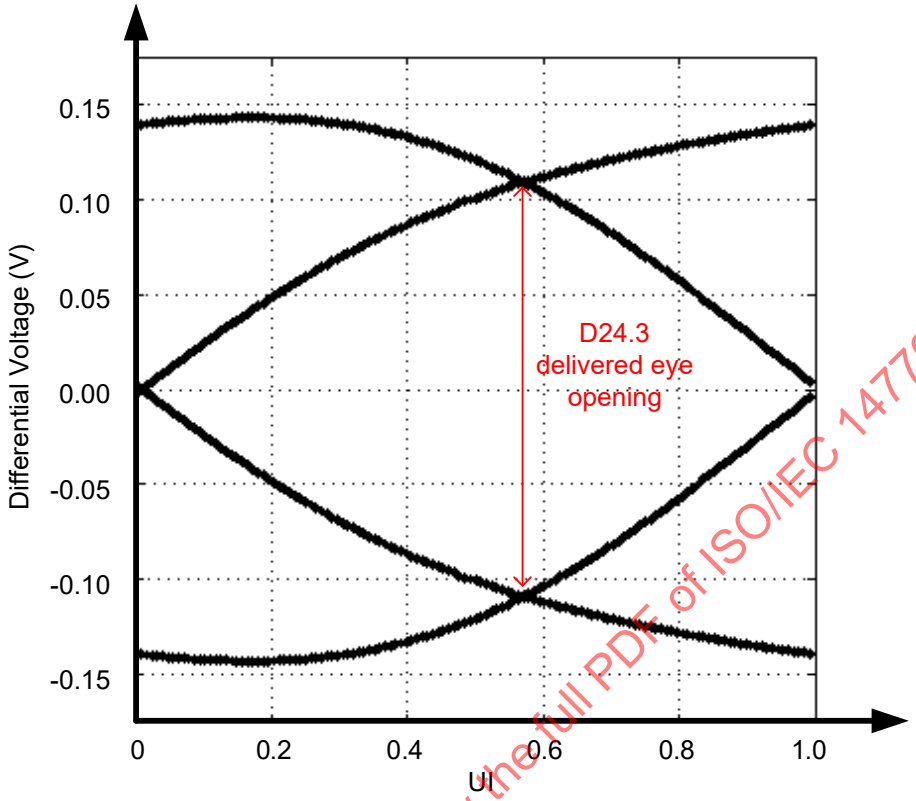


Figure 116 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter test load D24.3 response

5.7 End to end simulation for trained 12 Gbit/s

5.7.1 End to end simulation for trained 12 Gbit/s overview

End to end simulation shall be used to verify characteristics of:

b) transmitter devices connected to passive TxRx connections (see 5.8.4.7.4);
c) passive TxRx connections (see 5.5.6); and
d) ISI generators providing the stressed receiver signal input for receiver devices connected to passive TxRx connections (see 5.8.5.7.6.6).

The specific end to end simulation procedures defined in 5.8.4.7.4, 5.5.6, and 5.8.5.7.6.6 follow this sequence:

1) capture the signal from a transmitter device with no equalization and without SSC into a zero-length test load or model the transmitter using the reference transmitter (see 5.8.4.7.3);
2) connect passive TxRx connection segments, crosstalk, reference transmitter, and reference receiver according to the reference end to end simulation diagram (see 5.7.2 and D.2);
3) in the simulator, set the transmitter reference equalization (see 5.7.3 and figure 147) and set the receiver reference DFE equalization (see 5.8.5.7.3); and
4) perform a linear simulation, including the effects of edge rates, ISI, and crosstalk (see clause D.1).

The end to end simulation uses a reference transmitter with RJ and TJ set to zero. RJ and TJ and non-linear behavior present in the captured signal used for simulation are removed by the simulation process. Margins

for these effects are provided in the required simulation characteristics. The simulation characteristics are processed at a BER of 10^{-15}.

Crosstalk transmitters are simulated using reference transmitters. These reference transmitters shall be set to the characteristics of table D.1. The crosstalk transmitters shall be asynchronous to the data sent to the channel under test.

Characteristics are measured from the simulation at specified measurement points for the usage model and characterization type (see table 27, table 48, and table 63).

5.7.2 Usage models for end to end simulation for trained 12 Gbit/s

A set of transfer functions is required to complement the measured S-parameter or captured signal to provide an end to end simulation model. D.2 describes the different S-parameter files that shall be used for each usage model, with their associated measurement points.

Each transmitter device, receiver device, or passive TxRx connection segment shall be simulated with the appropriate usage model (see clause D.2).

The S-parameter files provided in ISO/IEC 14776-154_2017.zip use the port mapping of F.11.3. The FEXT S-parameters and NEXT S-parameters are extracted as shown in figure 117.

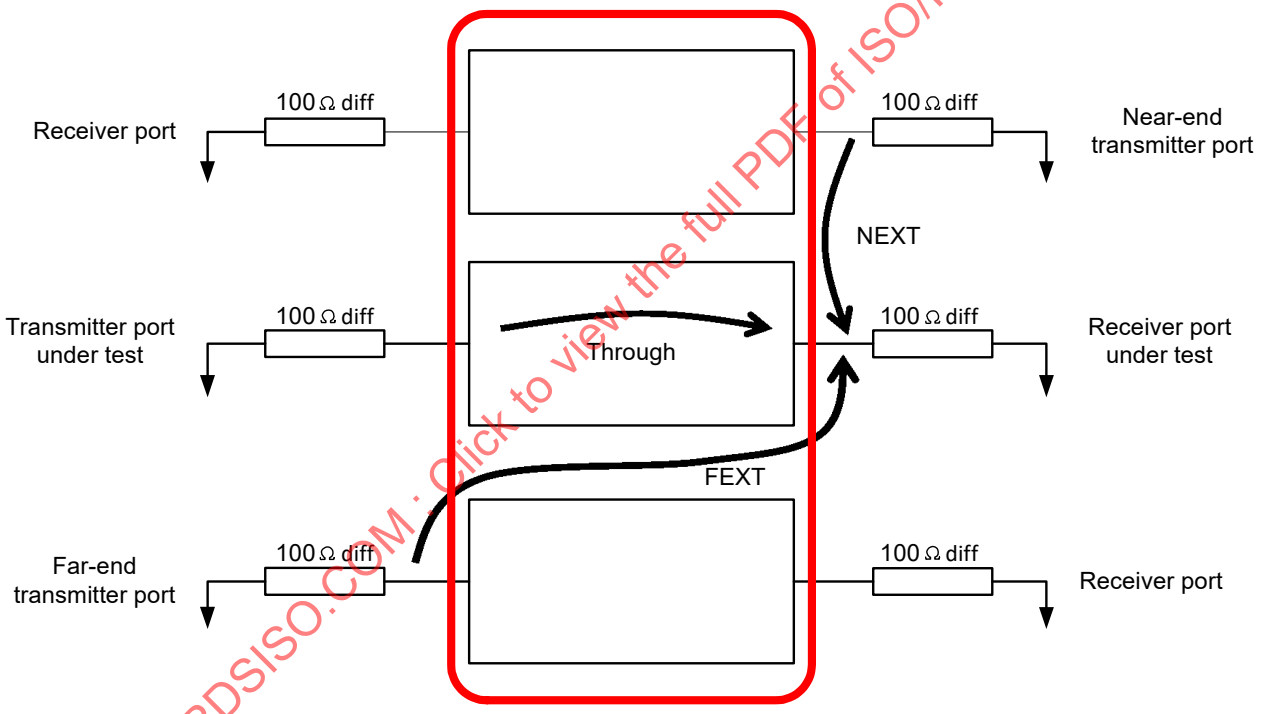


Figure 117 – NEXT and FEXT measurement definition

See Annex D for a description of the procedure that shall be used for end to end simulations. See clause E.1 for additional information regarding the S-parameter for 12 Gbit/s simulations.

5.7.3 Reference transmitter equalization for trained 12 Gbit/s

The reference transmitter equalization shall be calculated using the procedure described in this subclause, which requires the unequalized pulse response of the TxRx connection between ET and the input of the reference receiver (i.e., RR) (see clause D.2). Extraction of pulse responses from captured signals or transfer functions is beyond the scope of this document, however, an example is provided in SAS3_EYEOPENING (see ISO/IEC 14776-154_2017.zip).

The reference transmitter equalization procedure is as follows:

1) compute the reference sampling instant from the un-equalized pulse response between ET and RR (see figure 118);
2) set coefficient 2 (i.e., C2) of a reference transmitter to one and K_0 to one;
3) provide the un-equalized pulse response between ET and RR as the input of the reference transmitter, and compute the coefficient 1 (i.e., C1) and coefficient 3 (i.e., C3) that result in a pulse response with the smallest sum of squared error to an ideal pulse, at instants separated from the reference sampling instant by integer multiples of a one UI period (see figure 119);
4) calculate an equalized pulse response by convolving the coefficients obtained in steps 2) and 3) with the un-equalized pulse response between ET and RR;
5) calculate the reference sampling instant from the equalized pulse response;
6) repeat steps 2) through 5) until the coefficients and sampling point converge (see figure 120); and
7) normalize the final coefficients found in steps 3) and 4) by dividing them by (|C1| + |C3| + 1).

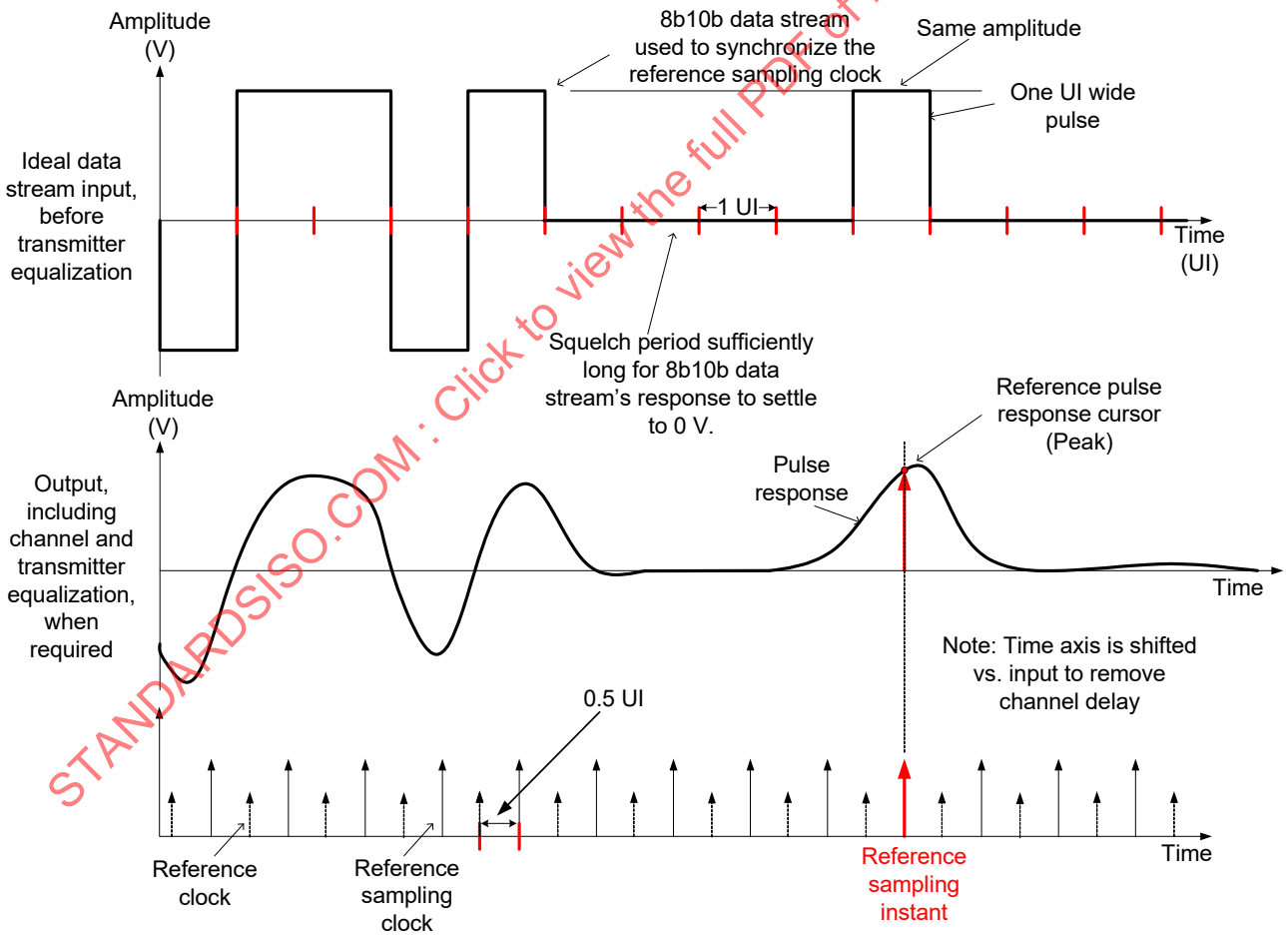


Figure 118 – Reference sampling point and reference pulse response cursor

Figure 119 shows the computations of step 3). A one UI spaced filter of coefficients [C1, C2 = 1, C3] is convolved with the extracted end to end pulse response. Coefficient 1 and coefficient 3 are computed to produce an equalized pulse response that has the smallest sum of squared errors at the sampling instants defined by a reference sampling clock.

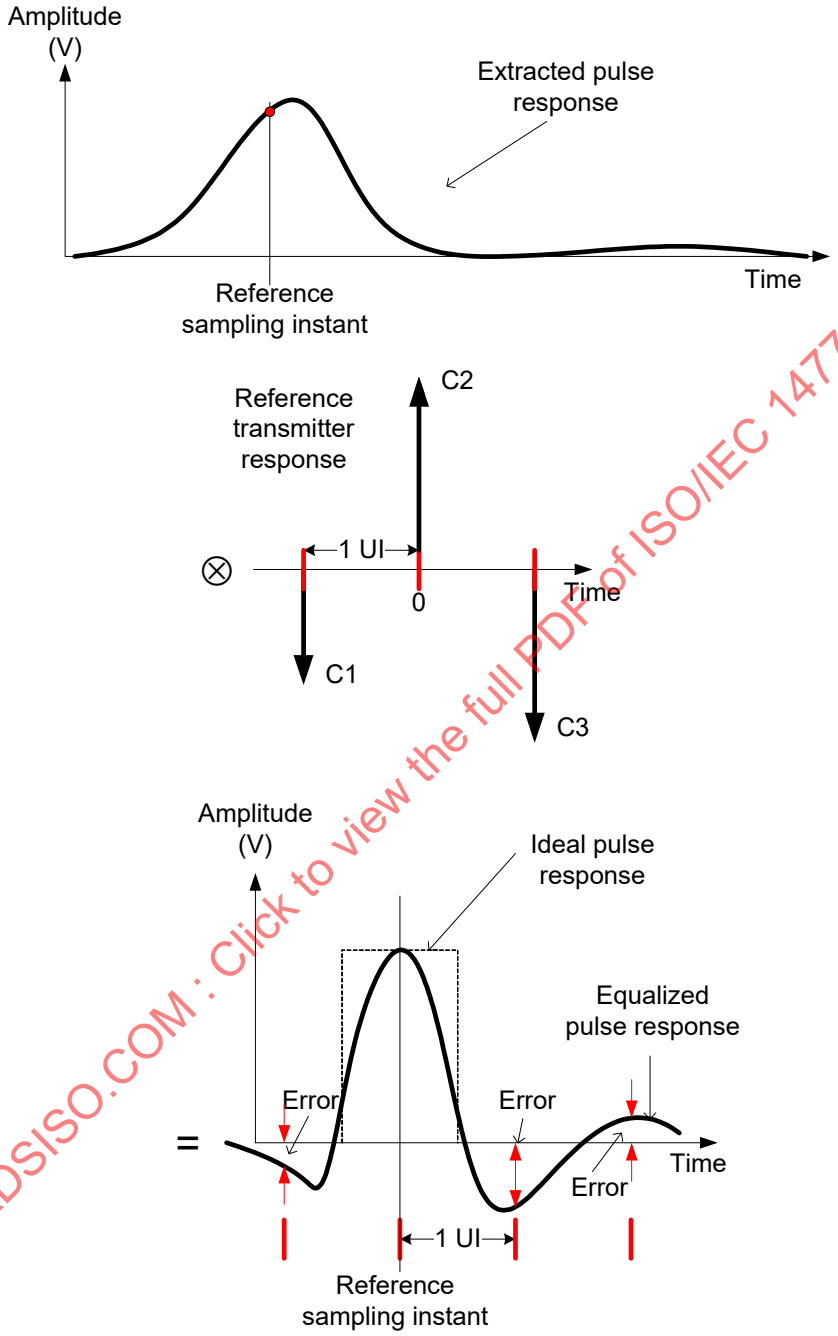


Figure 119 – Reference transmitter coefficient error computation

The reference sampling instant is computed from:

1) the un-equalized pulse response from ET to RR, for the first iteration; and
2) the equalized pulse response using transmitter coefficients from the previous iteration, for other iterations.

The reference sampling instant changes when the coefficients from the current iteration are used to compute the equalized pulse response. As shown in figure 120, the process of calculating C1 and C3 is repeated with the reference sampling instant computed from the last equalized pulse response, until the coefficients and reference sampling instant converge to stable values.

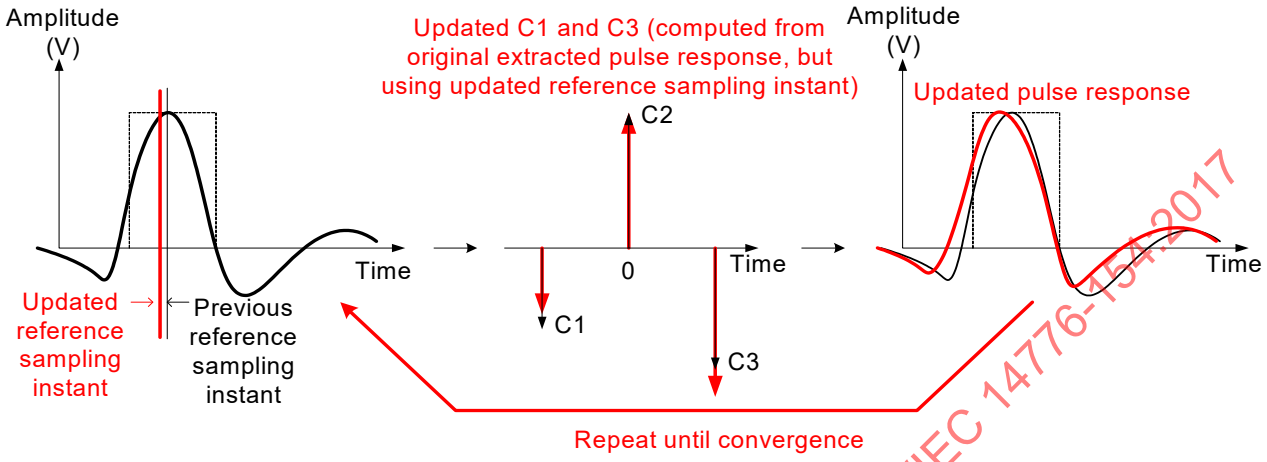


Figure 120 – Convergence of reference transmitter equalization

If either coefficient 1 (i.e., C1) or coefficient 3 (i.e., C3) takes a positive value during this procedure, its value is forced to zero and only the other coefficient is computed. The procedure stops if both coefficients need to be forced to zero.

5.7.4 Crosstalk measurement for end to end simulations and 12 Gbit/s jitter tolerance

End to end channel simulation shall include crosstalk. Crosstalk shall be measured using:

a) crosstalk transfer functions (e.g., S-parameters, see clause F.11); or
b) total peak to peak crosstalk measurement.

The following procedure shall be used to measure total peak to peak crosstalk:

1) calculate the reference transmitter equalization for the TxRx connection segment under test (see 5.7.3);
2) terminate the TxRx connection segment under test on the transmitter end;
3) connect 12 Gbit/s transmitters to the source of all or a subset of crosstalk channels;
4) set the crosstalk transmitters to transmit asynchronous IDLE dwords (see SPL-3) using the characteristics in table D.1;
5) measure the asynchronous amplitude histogram at the end of the TxRx connection segment under test, into a zero-length test load, with an acquisition bandwidth of at least 9 GHz, and a capture of at least 2×10^7 UI;
6) repeat steps 2) through 4) until all crosstalk sources have been measured;
7) when multiple measurements are made, convolve the histograms to obtain the total crosstalk histogram; and
8) from the total crosstalk histogram evaluate the crosstalk amplitude that is met or exceeded at a cumulative probability of 10^{-6} using the following procedure:
    1) separate positive samples from negative samples, ensuring at least 10^7 samples are collected for each type;
    2) calculate the vertical histogram for the positive samples;
    3) from the histogram, compute the crosstalk voltage that is met or exceeded at a probability of 10^{-6};
    4) calculate the vertical histogram for the opposite of the negative samples (i.e., zero minus the samples);
    5) from the histogram, calculate the crosstalk voltage that is met or exceeded at a probability of 10^{-6}; and
    6) sum the peak crosstalk voltages calculated in steps 3) and 5).

To provide a variety of pattern combinations for the crosstalk measurement, the digital IDLE dwords should be aligned differently one crosstalk channel to another and the transmission frequencies of the crosstalk transmitters should be different one from another.

The channel under test shall be terminated with the characteristics of the transmitter device termination (see table 34) on the transmitter end. The termination should be implemented using:

a) a high-bandwidth termination having impedance close to the nominal differential impedance (see table 24), for TxRx connection segments; or
b) a transmitter device set to transmit D.C. idle while maintaining the characteristics of table 34 for transmitter circuits and ISI generators.

Active circuits create noise when transmitting signals, including D.C. idle. By measuring the crosstalk with active circuits connected, the crosstalk value reported includes this noise. This is representative of the noise generated when the active circuit is transmitting data. When multiple crosstalk measurements are performed, this noise may however be overestimated in the final crosstalk amplitude calculation. Appropriate measurement techniques should be used to minimize these effects.

For transmitter device characterization, the crosstalk transmitters shall set coefficient 1 (i.e., C1) to zero, set coefficient 3 (i.e., C3) to zero, and set maximum peak to peak voltage.

For receiver ISI stress generators, the crosstalk is measured into a zero-length test load, and shall not include crosstalk from the receiver under test. A crosstalk generator channel should be selected to provide signal characteristics as close as possible to the required crosstalk signal characteristics (see table D.5), with the crosstalk generator characteristics defined by table D.1. Peak to peak voltage should then be adjusted to meet the required crosstalk characteristics.

5.8 Transmitter device and receiver device electrical characteristics

5.8.1 General electrical characteristics

Table 31 defines the general electrical characteristics, which apply to both transmitter devices and receiver devices.

Table 31 – General electrical characteristics

Characteristic	Units	1.5 Gbit/s (i.e., G1)	3 Gbit/s (i.e., G2)	6 Gbit/s (i.e., G3)	12 Gbit/s (i.e., G4)
Physical link rate (nominal)	MBps	150	300	600	1 200
Unit interval (UI) (nominal) [a]	ps	666.$\overline{6}$	333.$\overline{3}$	166.$\overline{6}$	83.$\overline{3}$
Baud rate (f_{baud}) (nominal)	Gigasymbols/s	1.5	3	6	12
Maximum A.C. coupling capacitor [b]	nF	12			
Maximum noise during OOB idle time [c d]	mV(P-P)	120			

[a] 666.$\overline{6}$ (i.e., 2 000 / 3), 333.$\overline{3}$ (i.e., 1 000 / 3), 166.$\overline{6}$ (i.e., 500 / 3), and 83.$\overline{3}$ (i.e., 250 / 3).
[b] The coupling capacitor value for A.C. coupled transmit and receive pairs. See 5.8.4.2 for coupling requirements for transmitter devices. See 5.8.5.2 for coupling requirements for receiver devices. The equivalent series resistance at 3 GHz should be less than 1 Ω.
[c] With a measurement bandwidth of 1.5 × f_{baud} (e.g., 18 GHz for 12 Gbit/s), no signal level during the idle time shall exceed the specified maximum differential amplitude.
[d] This is not applicable when optical mode is enabled.

5.8.2 Transmitter device and receiver device transients

Transients may occur at transmitter devices or receiver devices as a result of changes in supply power conditions or mode transitions.

A mode transition is an event that may result in a measurable transient due to the response of the transmitter device or receiver device. The following conditions constitute a mode transition:

a) enabling or disabling driver circuitry;
b) enabling or disabling receiver common mode circuitry;
c) hot plug event;
d) adjusting driver amplitude;
e) enabling or disabling de-emphasis; and
f) adjusting terminator impedance.

Transmitter device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 121 during all power state and mode transitions. Receiver device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 122 during all power state and mode transitions. Test conditions shall include power supply power on and power off conditions, voltage sequencing, and mode transitions.

Figure 121 shows the test circuit attached to IT or CT to test transmitter device transients.

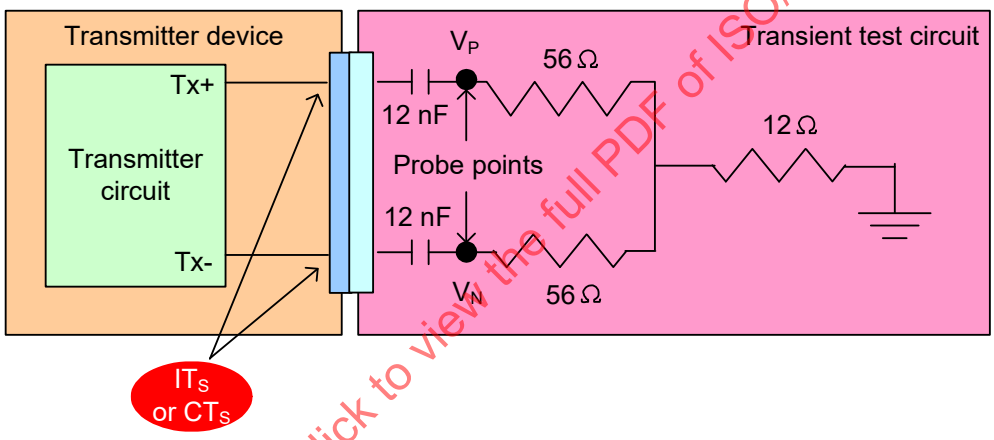


Figure 121 – Transmitter device transient test circuit

Figure 122 shows the test circuit attached to IR or CR to test receiver device transients.

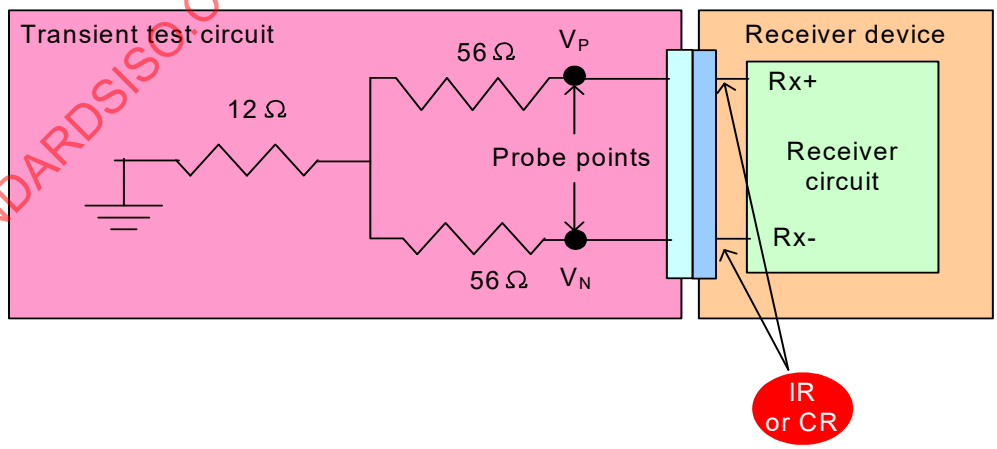


Figure 122 – Receiver device transient test circuit

5.8.3 Eye masks and the JTF

5.8.3.1 Eye masks overview

The eye masks shown in 5.8.3 shall be interpreted as graphical representations of the voltage and time limits of the signal. The eye mask boundaries define the eye contour of:

a) the 10^{-12} jitter population for untrained 1.5 Gbit/s and 3 Gbit/s measured eyes; and
b) the 10^{-15} jitter population for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s simulated eyes.

For untrained 1.5 Gbit/s and 3 Gbit/s, equivalent time sampling oscilloscope technology is not practical for measuring compliance to the eye masks. See MJSQ for methods that are suitable for verifying compliance to these eye masks.

CJTPAT (see Annex A) shall be used for all jitter testing unless otherwise specified. Annex A defines the required pattern on the physical link and provides information regarding special considerations for running disparity (see SPL-3) and scrambling (see SPL-3).

5.8.3.2 JTF

With the possible presence of SSC, the application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667) as specified in SAS-1.1 does not separate the SSC component from the actual jitter and this may overstate the transmitter device jitter. To differentiate between allowable timing variation due to SSC and jitter, the frequency-weighting JTF shall be applied to the signal at the compliance point when determining the eye mask.

The jitter measurement device shall comply with the JTF. The reference clock characteristics are controlled by the resulting JTF characteristics obtained by taking the time difference between the PLL output (i.e., the reference clock) and the data stream sourced to the PLL. The PLL's closed loop transfer function's -3 dB corner frequency and other adjustable parameters (e.g., peaking) are determined by the value required to meet the requirements of the JTF.

The JTF shall have the characteristics specified in table 32 for a repeating 0011b pattern or 1100b pattern (e.g., D24.3). See the phy test patterns in the Protocol Specific diagnostic page in SPL-3.

The JTF -3 dB corner frequency and the magnitude peaking requirements shall be measured with SJ applied, with a peak to peak amplitude of 0.3 UI, with a relative tolerance of ± 10 %. The relative attenuation at 30 kHz shall be measured with sinusoidal phase (i.e., time) modulation applied, with a peak to peak amplitude of 20.8 ns with a relative tolerance of ± 10 %. See Annex F for the calibration procedure.

A proportional decrease of the JTF -3 dB corner frequency should be observed for a decrease in pattern transition density compared to a 0.5 transition density. If a JMD shifts the JTF -3 dB corner frequency in a manner that does not match this characteristic, or does not shift at all, then measurements of jitter with patterns with transition densities different than 0.5 may lead to discrepancies in reported jitter levels. In the case of reported jitter discrepancies between JMDs, the JMD with the shift of the -3 dB corner frequency that is closest to the proportional characteristic of the reference transmitter test load (see 5.6.5) shall be considered correct. This characteristic may be measured with the conditions defined above for measuring the -3 dB corner frequency but substituting other patterns with different transition densities.

Table 32 – JTF parameters

Characteristic	Without SSC support				With SSC support			
	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s
JTF -3 dB point (kHz) [a] [b]	900 ± 500	1 800 ± 500	3 600 ± 500	3 600 ± 500	1 300 ± 500	1 838 ± 500	2 600 ± 500	2 600 ± 500
JTF slope (dB/decade)	20	20	20	20	40	40	40	40
Attenuation at 30 kHz ± 1 % (dB) [c]	N/A	N/A	N/A	N/A	61.5 ± 1.5	67.5 ± 1.5	73.5 ± 1.5	73.5 ± 1.5
Maximum Peaking (dB)	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5

Key:

N/A = not applicable

f_{baud} = Hz (i.e., 1.5 GHz for 1.5 Gbit/s, 3.0 GHz for 3 Gbit/s, 6.0 GHz for 6 Gbit/s). 12 Gbit/s uses the value for 6 Gbit/s.

[a] For untrained or trained without SSC support this value equals f_{baud}/1 667 ± 500 kHz for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. 12 Gbit/s uses the value for 6 Gbit/s.

[b] For untrained or trained with SSC support this value equals $(f_{baud})^{0.5}$ x 33.566 x $Hz^{0.5}$ ± 500 kHz for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. 12 Gbit/s uses the value for 6 Gbit/s.

[c] For untrained or trained with SSC support this value equals 73.5 dB + [20 x $\log_{10}(f_{baud} / 6 \times 10^9$ Hz)] dB ± 1.5 dB for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. 12 Gbit/s uses the value for 6 Gbit/s.

5.8.3.3 Transmitter device eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 123 describes the eye mask used for testing the signal output of the transmitter device at IT and CT for untrained 1.5 Gbit/s and 3 Gbit/s (see table 36 in 5.8.4.5) and OOB signals (see table 50 in 5.8.4.8). This eye mask applies to jitter after the application of the JTF (see 5.8.3.2).

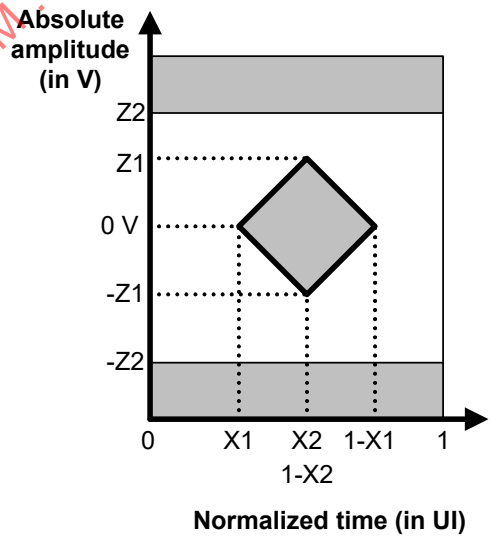


Figure 123 – Transmitter device eye mask

Verifying compliance with the limits represented by the transmitter device eye mask should be done with reverse channel traffic present on the channel under test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.8.3.4 Receiver device eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 124 describes the eye mask used for testing the signal delivered to the receiver device at IR and CR for untrained 1.5 Gbit/s and 3 Gbit/s (see table 54 in 5.8.5.4). This eye mask applies to jitter after the application of the JTF (see 5.8.3.2). This requirement accounts for the low frequency tracking properties and response time of the CDR circuitry in receiver devices.

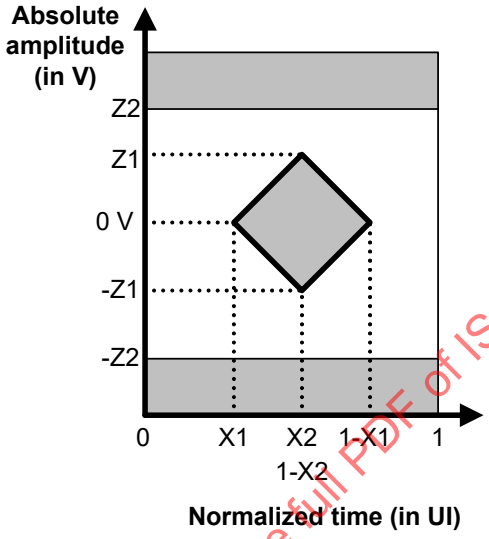


Figure 124 – Receiver device eye mask

Verifying compliance with the limits represented by the receiver device eye mask should be done with reverse channel traffic present on the channel under test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.8.3.5 Receiver device jitter tolerance eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 125 describes the eye mask used to test the jitter tolerance of the receiver device at IR and CR for untrained 1.5 Gbit/s and 3 Gbit/s (see table 54 in 5.8.5.4). For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, jitter tolerance is included in the delivered signal specifications for stressed receiver device jitter tolerance testing (see 5.8.5.7.6).

The eye mask shall be constructed as follows:

a) X2 and Z2 shall be the values for the delivered signal listed in table 54 (see 5.8.5.4);
b) $X1_{OP}$ shall be half the value of TJ for maximum delivered jitter listed in table 55 (see 5.8.5.5); and
c) $X1_{TOL}$ shall be half the value of TJ for receiver device jitter tolerance listed in table 56 (see 5.8.5.6), for applied SJ frequencies above (f_{baud} / 1 667).

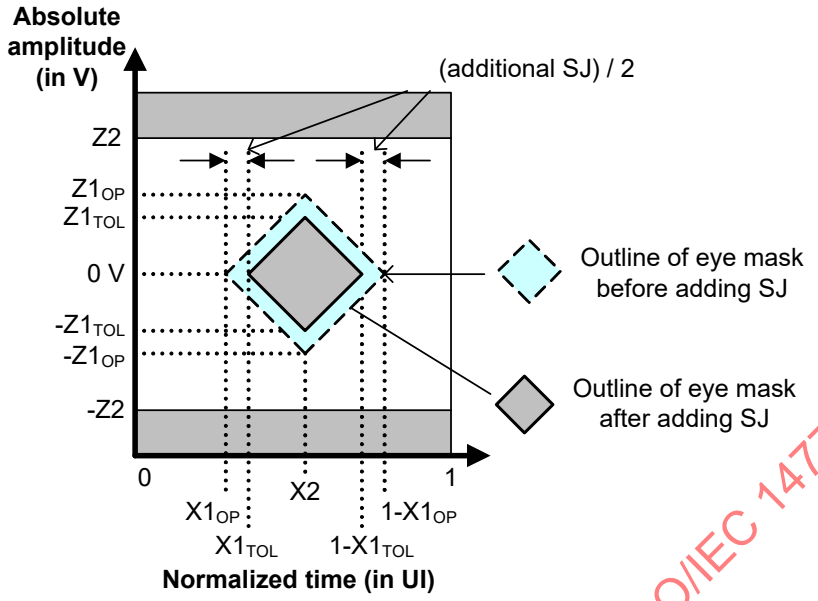


Figure 125 – Deriving a receiver device jitter tolerance eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

The leading and trailing edge slopes of the receiver device eye mask in figure 124 (see 5.8.3.4) shall be preserved. As a result, the amplitude value of Z1 is less than that given for the delivered signal in table 54 (see 5.8.5.4), and $Z1_{TOL}$ and $Z1_{OP}$ shall be defined from those slopes by the following equation:

$$Z1_{TOL} = Z1_{OP} \times \frac{X2 - \left(\frac{ASJ}{2}\right) - X1_{OP}}{X2 - X1_{OP}}$$

where:

$Z1_{TOL}$	is the value for Z1 to be used for the receiver device jitter tolerance eye mask;
$Z1_{OP}$	is the Z1 value for the delivered signal in table 54;
$X1_{OP}$	is the X1 value for the delivered signal in table 54;
X2	is the X2 value for the delivered signal in table 54; and
ASJ	is the additional SJ for applied SJ frequencies above (f_{baud} / 1 667) (see figure 139 in 5.8.5.6).

The X1 points in the receiver device jitter tolerance eye mask (see figure 125) are greater than the X1 points in the receiver device eye mask (see figure 124) due to the addition of SJ.

5.8.4 Transmitter device characteristics

5.8.4.1 Transmitter device characteristics overview

Transmitter devices operating at 1.5 Gbit/s, 3 Gbit/s, or 6 Gbit/s may or may not incorporate de-emphasis (i.e., pre-emphasis) and other forms of compensation. The transmitter device operating at 1.5 Gbit/s, 3 Gbit/s, or 6 Gbit/s shall use the same settings (e.g., de-emphasis and voltage swing) with both the zero-length test load and the appropriate TCTF test load or reference transmitter test load (see 5.6). Transmitter devices operating at 6 Gbit/s should use the transmitter equalization settings provided in table 40. Transmitter devices operating at 12 Gbit/s shall support transmitter training (see SPL-3) unless the transmitter device is operating in the optical mode.

Compliance points referenced in the electrical requirement tables are shown in 5.3 unless otherwise specified.

See clause F.7 for a methodology for measuring transmitter device signal output.

5.8.4.2 Transmitter device coupling requirements

Coupling requirements for transmitter devices are as follows:

a) transmitter devices using inter-enclosure TxRx connections (i.e., attached to CT compliance points) should be D.C. coupled, however, may be A.C. coupled to the interconnect through a transmission network; or
b) transmitter devices using intra-enclosure TxRx connections (i.e., attached to IT compliance points) should be D.C. coupled, however, may be A.C. coupled.

If the transmitter device is attached to an IT compliance point supporting SATA, then the coupling requirements of Gen1i devices (see SATA) should be considered regarding its impact to the implementation.

See table 31 (see 5.8.1) for the coupling capacitor value.

5.8.4.3 Transmitter device general electrical characteristics

Table 33 defines the transmitter device general electrical characteristics.

Table 33 – Transmitter device general electrical characteristics

Characteristic	Units	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s
Physical link rate accuracy [a] at IT and CT	ppm	± 100			
Physical link rate SSC modulation at IT and CT	ppm	See table 68, table 69, and table 70 in 5.8.6			
Maximum transmitter device transients [b]	V	± 1.2			

[a] Physical link rate accuracy shall be measured over a minimum of 1 x 10^6 UI and should be measured using a minimum resolution of 100 Hz.
[b] See 5.8.2 for transient test circuits and conditions.

Table 34 defines the transmitter device termination characteristics.

Table 34 – Transmitter device termination characteristics

Characteristic	Units	Untrained 1.5 Gbit/s and 3 Gbit/s	Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s	Trained 12 Gbit/s
Differential impedance [a]	Ω	60 minimum 115 maximum	See 5.8.4.6.1	See 5.8.4.7.1
Maximum differential impedance imbalance [a] [b]	Ω	5	See 5.8.4.6.3 [c]	See 5.8.4.7.2 [c]
Common mode impedance [b]	Ω	15 minimum 40 maximum	See 5.8.4.6.1	See 5.8.4.7.1

[a] All transmitter device termination measurements are made through mated connector pairs.
[b] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.
[c] Measurement replaced by S_{CD22} specifications (i.e., differential to common mode conversion).

5.8.4.4 Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load

Table 35 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load (see 5.6.2) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.8.4.6 for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device signal output characteristics. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 35 – Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load at IT and CT

Signal characteristic [a]	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Maximum intra-pair skew [b]	ps	20	15
Maximum transmitter device off voltage [c d]	mV(P-P)	50	
Maximum (i.e., slowest) rise/fall time [e]	ps	273	137
Minimum (i.e., fastest) rise/fall time [e]	ps	41.6	
Maximum transmitter output imbalance [f]	%	10	

[a] All tests in this table shall be performed with zero-length test load (see 5.6.2).

[b] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the TX+ and TX- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the TX+ signal and the TX- signal.

[c] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[d] This is not applicable when optical mode is enabled.

[e] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link.

[f] The maximum difference between the V+ and V- A.C. rms transmitter device amplitudes measured with CJTPAT (see Annex A) into the zero-length test load shown in figure 103 (see 5.6.2), as a percentage of the average of the V+ and V- A.C. rms amplitudes.

5.8.4.5 Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load

Table 36 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load (i.e., the zero-length test load (see 5.6.2) and either the TCTF test load (see 5.6.3) or the low-loss TCTF test load (see 5.6.4)) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.8.4.6 for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device signal output characteristics. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 36 – Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load at IT and CT

Signal characteristic	Units	IT, untrained		CT, untrained	
		1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 123) if SATA is not supported	mV(P-P)	1 600			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 123) if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 123), if SATA is not supported	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 123), if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Maximum DJ [b c d]	UI	0.35			
Maximum half of TJ (i.e., X1 in figure 123) [b c d e f g h]	UI	0.275			
Center of bit time (i.e., X2 in figure 123)	UI	0.50			
Maximum intra-pair skew [i]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this document differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this document may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] All DJ and TJ values are level 1 (see MJSQ).

[c] The values for jitter in this table are measured at the average signal amplitude point.

[d] The DJ and TJ values in this table apply to jitter measured as described in 5.8.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.

[e] TJ is specified at a CDF level of 10^{-12}.

[f] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.

Jitter peak to peak measured < (maximum TJ - |asymmetry|).

[g] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability, direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[h] The value for X1 is also half the value of TJ for maximum delivered jitter listed in table 55 (see 5.8.5.5). The test or analysis shall include the effects of the JTF (see 5.8.3.2).

[i] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the TX+ and TX- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the TX+ signal and the TX- signal at the probe points.

5.8.4.6 Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

5.8.4.6.1 Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s overview

Table 37 specifies the signal output characteristics for the transmitter device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s as measured with the zero-length test load (see 5.6.2), unless otherwise specified, attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements except for common mode measurements.

Table 37 – Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s at IT and CT

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage [b c]	mV(P-P)			50
Withstanding voltage (non-operational)	mV(P-P)	2 000		
Rise/fall time [d]	ps	41.6		
Reference differential impedance [e]	Ω		100	
Reference common mode impedance [e]	Ω		25	
Common mode voltage limit (rms) [f]	mV			30
RJ [g h]	UI			0.15 [i]
TJ [h j]	UI			0.25 [k]
WDP at 6 Gbit/s [l]	dB			13
WDP at 3 Gbit/s [l]	dB			7
WDP at 1.5 Gbit/s [l]	dB			4.5

[a] See 5.8.4.6.6 for the V_{P-P} measurement method.
[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).
[c] This is not applicable when optical mode is enabled.
[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link.
[e] See 5.8.4.6.3 for transmitter device S-parameters characteristics.
[f] This is a broadband limit. For additional limits on spectral content, see figure 126 and table 38.
[g] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.
[h] The measurement shall include the effects of the JTF (see 5.8.3.2).
[i] 0.15 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[j] The TJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.
[k] 0.25 UI is 41.6 ps at 6 Gbit/s, 83.3 ps at 3 Gbit/s, and 166.6 ps at 1.5 Gbit/s.
[l] See 5.8.4.6.2 for the transmitter device test procedure.

Table 38 defines the transmitter device common mode voltage limit characteristics.

Table 38 – Transmitter device common mode voltage limit characteristics

Characteristic	Reference	L [a] dBmV [b]	N [a] dBmV [b c]	S [a] dBmV/decade [b]	f_{min} [a] MHz	f_{max} [a] GHz
Spectral limit of common mode voltage [d]	Figure 126	12.7	26.0	13.3	100	6.0

[a] See figure 4 in 5.2 for definitions of L, N, S, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (rms). Hence, 0 dBm is 1 mW which is 158 mV (rms) across 25 Ω (i.e., the reference impedance for common mode voltage) which is 20 × $\log_{10}$(158) = +44 dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at the Nyquist frequency (i.e., 3 GHz) (see figure 126).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Figure 126 shows the transmitter device common mode voltage limit defined in table 38.

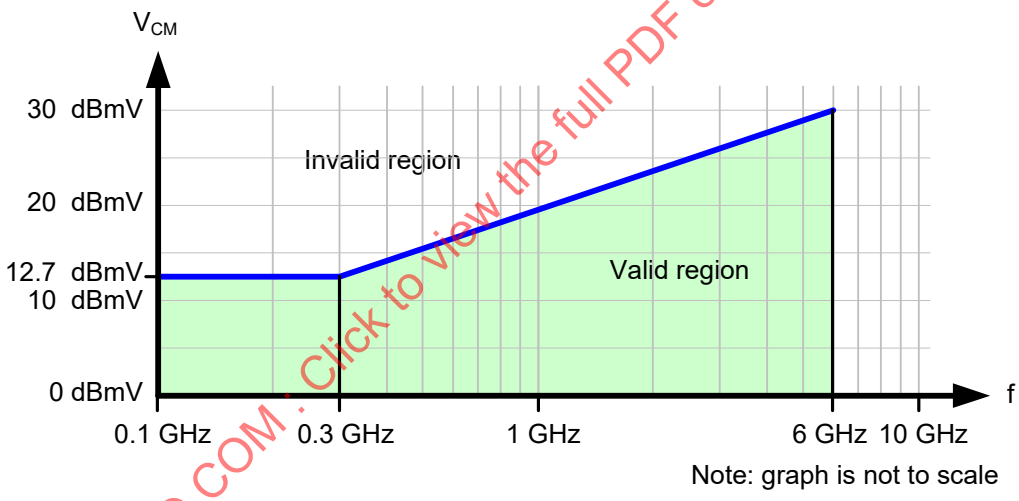


Figure 126 – Transmitter device common mode voltage limit

5.8.4.6.2 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device test procedure

The transmitter device test procedure is as follows:

1) attach the transmitter device to a zero-length test load, where its signal output is captured by an oscilloscope;
2) configure the transmitter device to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3);
3) configure the transmitter device to minimize DCD and BUJ;
4) capture multiple sets of the first 58 data dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern. Use averaging to minimize RJ; and
5) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to 'SAS2_TWDP'.

The WDP value is a characterization of the signal output within the reference receiver device (see 5.8.5.7.3) after equalization. WDP values computed by SASWDP are influenced by all sources of eye closure including

DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

5.8.4.6.3 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s Transmitter device S-parameter limits

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × $\log_{10}$(f / 3 GHz)]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 39 defines the maximum limits for S-parameters of the transmitter device.

Table 39 – Maximum limits for S-parameters at IT_S or CT_S

Characteristic [a] [b]	L [c] dB	N [c] dB	H [c] dB	S [c] dB / decade	f_{min} [c] MHz	f_{max} [c] GHz
$\|S_{CC22}\|$	-6.0	-5.0	-1.0	13.3	100	6.0
$\|S_{DD22}\|$	-10	-7.9	-3.9	13.3	100	6.0
$\|S_{CD22}\|$	-26	-12.7	-10	13.3	100	6.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). The amplitude applied by the test equipment shall be less than -4.4 dBm (i.e., 190 mV zero to peak) per port (see F.11.4.2).
[b] $|S_{DC22}|$ is not specified.
[c] See figure 4 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 127 shows the transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 39.

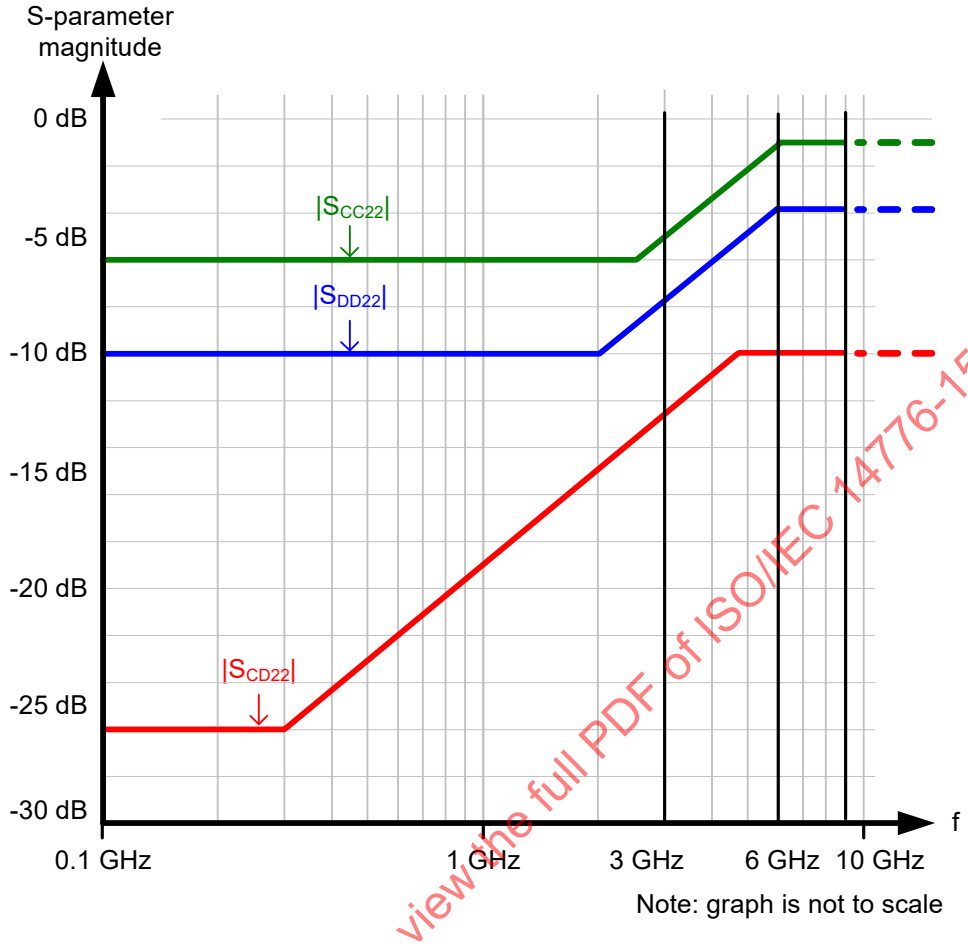


Figure 127 – Transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.8.4.6.4 Recommended trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device settings for interoperability

Table 40 defines recommended values for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter devices to provide interoperability with a broad range of implementations utilizing compliant TxRx connections and compliant receiver devices. The values are based on the evaluation of simulations with a variety of characterized physical hardware. Use of the recommended values does not guarantee that an implementation is capable of achieving a specific BER.

Specific implementations may obtain increased margin by deviating from the recommended values, however, such implementations are beyond the scope of this document.

Table 40 – Recommended trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device settings at IT and CT compliance point

Characteristic	Units	Minimum	Nominal	Maximum
Differential voltage swing (mode) (VMA) [a]	mV	600	707	
Transmitter equalization [a]	dB	2	3	4
[a] See 5.8.4.6.6 for measurement method.				

5.8.4.6.5 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device characteristics

The trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device is a set of parameters defining the electrical performance characteristics of a transmitter device used in simulation to determine compliance of a TxRx connection (see 5.5.5).

Figure 128 shows a trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device.

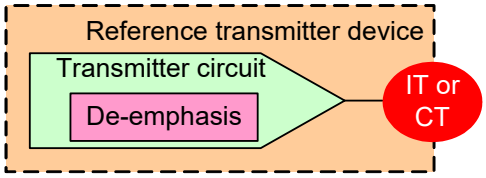


Figure 128 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device

Table 41 defines the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device characteristics.

Table 41 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device characteristics at IT and CT compliance point

Characteristic	Units	Value
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850
Transmitter equalization [a]	dB	2
Maximum (i.e., slowest) rise/fall time [b]	UI	0.41 [c]
RJ	UI	0.15 [d]
BUJ	UI	0.10 [e]

[a] See 5.8.4.6.6 for measurement method.
[b] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3).
[c] 0.41 UI is 68.$\overline{3}$ ps at 6 Gbit/s, 136.$\overline{6}$ ps at 3 Gbit/s, and 273.$\overline{3}$ ps at 1.5 Gbit/s.
[d] 0.15 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[e] 0.10 UI is 16.$\overline{6}$ ps at 6 Gbit/s, 33.$\overline{3}$ ps at 3 Gbit/s, and 66.$\overline{6}$ ps at 1.5 Gbit/s.

The following Touchstone model of the reference transmitter device termination is included in this document:

f) SAS2_TxRefTerm.s4p.

Figure 129 shows the S-parameters of the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device termination model.

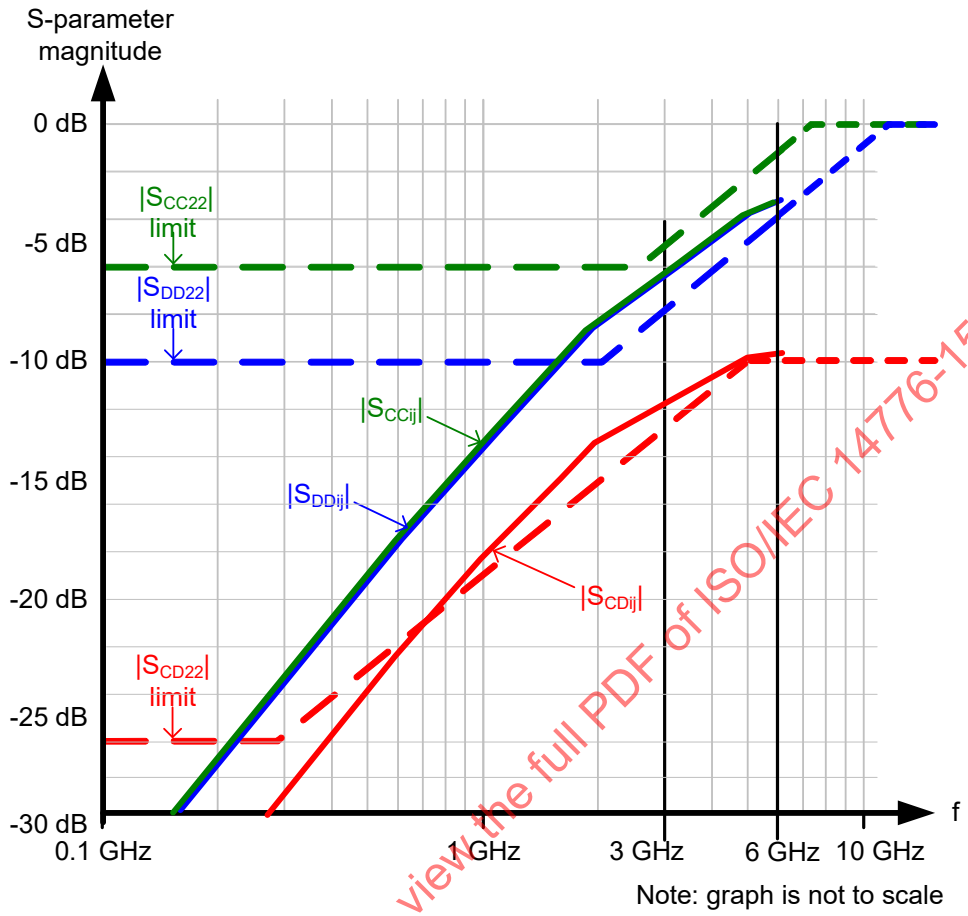


Figure 129 – Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference transmitter device termination S-parameters model

The Touchstone model does not exactly match the $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in 5.8.4.6.3 at all frequencies, however, it is a reasonable approximation for use in simulations. See Annex G for a description of how the Touchstone model was created.

5.8.4.6.6 Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s Transmitter equalization, VMA, and V_{P-P} measurement

The trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter equalization measurement shall be based on the following values:

a) VMA: a mode (i.e., the most frequent value of a set of data) measurement; and
b) V_{P-P}: a peak to peak measurement with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3).

The VMA and V_{P-P} measurements shall be made with the transmitter device terminated through the interoperability point into a zero-length test load (see 5.6.2).

The VMA and V_{P-P} measurements shall be made using an equivalent time sampling scope with a histogram function with the following or an equivalent procedure:

1) calibrate the sampling scope for measurement of a 3 GHz signal; and
2) determine VMA and V_{P-P} as shown in figure 130. A sample size of 1 000 minimum to 2 000 maximum histogram hits for VMA shall be used to determine the values. The histogram is a combination of two histograms (i.e., an upper histogram for TX+ and a lower histogram for TX-). The histograms on the left represent the test pattern signal displayed on the right. VMA and V_{P-P} are determined by adding the values measured for TX+ and TX-.

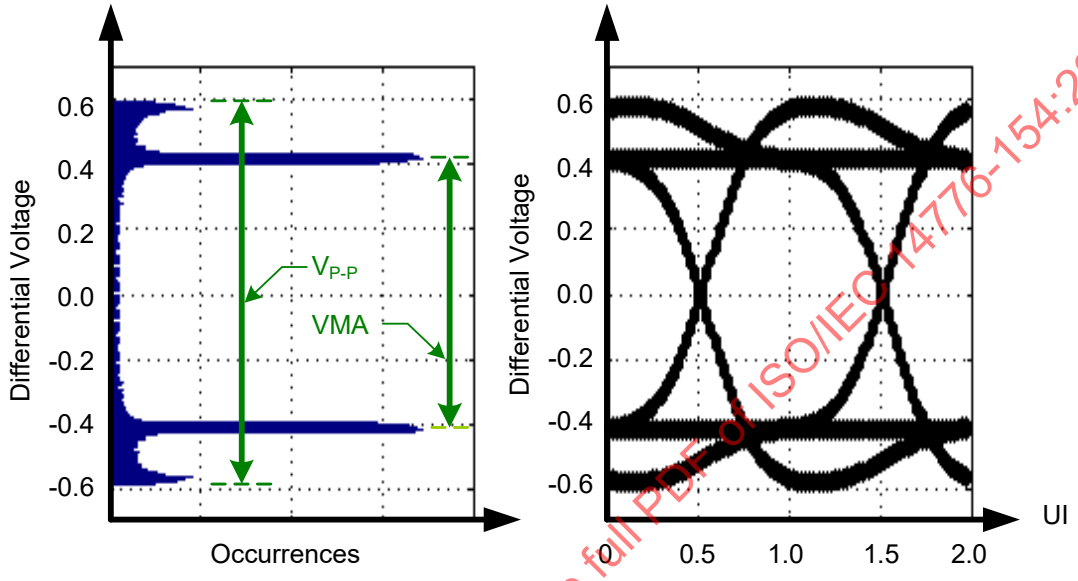


Figure 130 – Transmitter equalization measurement

The following formula shall be used to calculate the transmitter equalization value:

Transmitter equalization = $20 \times \log_{10} (V_{P-P} / \text{VMA})$ dB

where:

V_{P-P} is the peak to peak value; and
VMA is the mode value.

5.8.4.7 Transmitter device signal output characteristics for trained 12 Gbit/s

5.8.4.7.1 Transmitter device signal output characteristics for trained 12 Gbit/s overview

Table 42 specifies the signal output characteristics for the transmitter device for trained 12 Gbit/s.

Table 42 – Transmitter device signal output characteristics for trained 12 Gbit/s at ET, IT, and CT
(part 1 of 2)

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage at IT or CT [b c]	mV(P-P)			50
Withstanding voltage (non-operational) at IT or CT	mV(P-P)	2 000		
Rise/fall time at IT or CT [d]	ps	20.8		
Reference differential impedance at IT or CT [e]	Ω		100	
Reference common mode impedance at IT or CT [e]	Ω		25	

[a] The V_{P-P} measurement shall be made with the transmitter device set to no equalization (see table 45) and amplitude set to maximum. The minimum value applies at ET (see 5.3.3) and the maximum value applies at IT (see 5.3.3) or CT (see 5.3.3). The measurement is made with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). If using SAS3_EYEOPENING or equivalent tool for the measurement at ET, then IDLE dwords (see SPL-3) may be used for the test pattern.

[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[c] If optical mode is enabled the transmitter device off voltage is not applicable.

[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link.

[e] See 5.8.4.7.2 for transmitter device S-parameters characteristics.

[f] Ratio measured with post cursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-3 and figure 134). When both precursor and post cursor equalization are active the maximum observed R_{pre} may be as high as 3.8 at the VMA limit.

[g] If a simulation tool (e.g., SAS3_EYEOPENING) is used, then this measurement may be performed with IDLE dwords (see SPL-3) as the test pattern.

[h] Ratio measured with precursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-3 and figure 134). When both precursor and post cursor equalization are active the maximum observed R_{post} may be as high as 5.5 at the VMA limit.

[i] Measured as v_2 - v_5 (see figure 134) with a repeating TRAIN_DONE primitive (see SPL-3).

[j] This is a broadband limit. For additional limits on spectral content, see figure 132 and table 43.

[k] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.

[l] The measurement shall include the effects of the JTF (see 5.8.3.2).

[m] RJ and TJ are measured at IT (see 5.3.3) or CT (see 5.3.3).

[n] 0.15 UI is 12.5 ps at 12 Gbit/s.

[o] The TJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.

[p] 0.25 UI is 20.8 ps at 12 Gbit/s.

Table 42 – Transmitter device signal output characteristics for trained 12 Gbit/s at ET, IT, and CT
(part 2 of 2)

Signal characteristic	Units	Minimum	Nominal	Maximum
Precursor equalization ratio R_{pre} [f g]	V/V	1		1.66̄
Post cursor equalization ratio R_{post} [g h]	V/V	1		3.33̄
VMA [g i]	mV(P-P)	80		
Common mode voltage limit (rms) [j]	mV			30
RJ [k l m]	UI			0.15 [n]
TJ [l m o]	UI			0.25 [p]

[a] The V_{P-P} measurement shall be made with the transmitter device set to no equalization (see table 45) and amplitude set to maximum. The minimum value applies at ET (see 5.3.3) and the maximum value applies at IT (see 5.3.3) or CT (see 5.3.3). The measurement is made with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). If using SAS3_EYEOPENING or equivalent tool for the measurement at ET, then IDLE dwords (see SPL-3) may be used for the test pattern.

[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[c] If optical mode is enabled the transmitter device off voltage is not applicable.

[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link.

[e] See 5.8.4.7.2 for transmitter device S-parameters characteristics.

[f] Ratio measured with post cursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-3 and figure 134). When both precursor and post cursor equalization are active the maximum observed R_{pre} may be as high as 3.8 at the VMA limit.

[g] If a simulation tool (e.g., SAS3_EYEOPENING) is used, then this measurement may be performed with IDLE dwords (see SPL-3) as the test pattern.

[h] Ratio measured with precursor equalization disabled and peak to peak voltage set to maximum with a repeating TRAIN_DONE primitive (see SPL-3 and figure 134). When both precursor and post cursor equalization are active the maximum observed R_{post} may be as high as 5.5 at the VMA limit.

[i] Measured as v_2 - v_5 (see figure 134) with a repeating TRAIN_DONE primitive (see SPL-3).

[j] This is a broadband limit. For additional limits on spectral content, see figure 132 and table 43.

[k] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.

[l] The measurement shall include the effects of the JTF (see 5.8.3.2).

[m] RJ and TJ are measured at IT (see 5.3.3) or CT (see 5.3.3).

[n] 0.15 UI is 12.5 ps at 12 Gbit/s.

[o] The TJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.

[p] 0.25 UI is 20.8 ps at 12 Gbit/s.

In addition to table 42, figure 131 specifies the transmitter coefficient ranges when the transmitter peak to peak voltage is maximum. The coefficients are defined according to the reference transmitter (see 5.8.4.7.3). The bottom left area of the minimum and maximum ranges in figure 131 are limited by VMA and vary according to $V_{P\text{-}P\_noeq}$. $V_{P\text{-}P\_noeq}$ is the amplitude at ET measured with the no_equalization setting as specified in table 45.

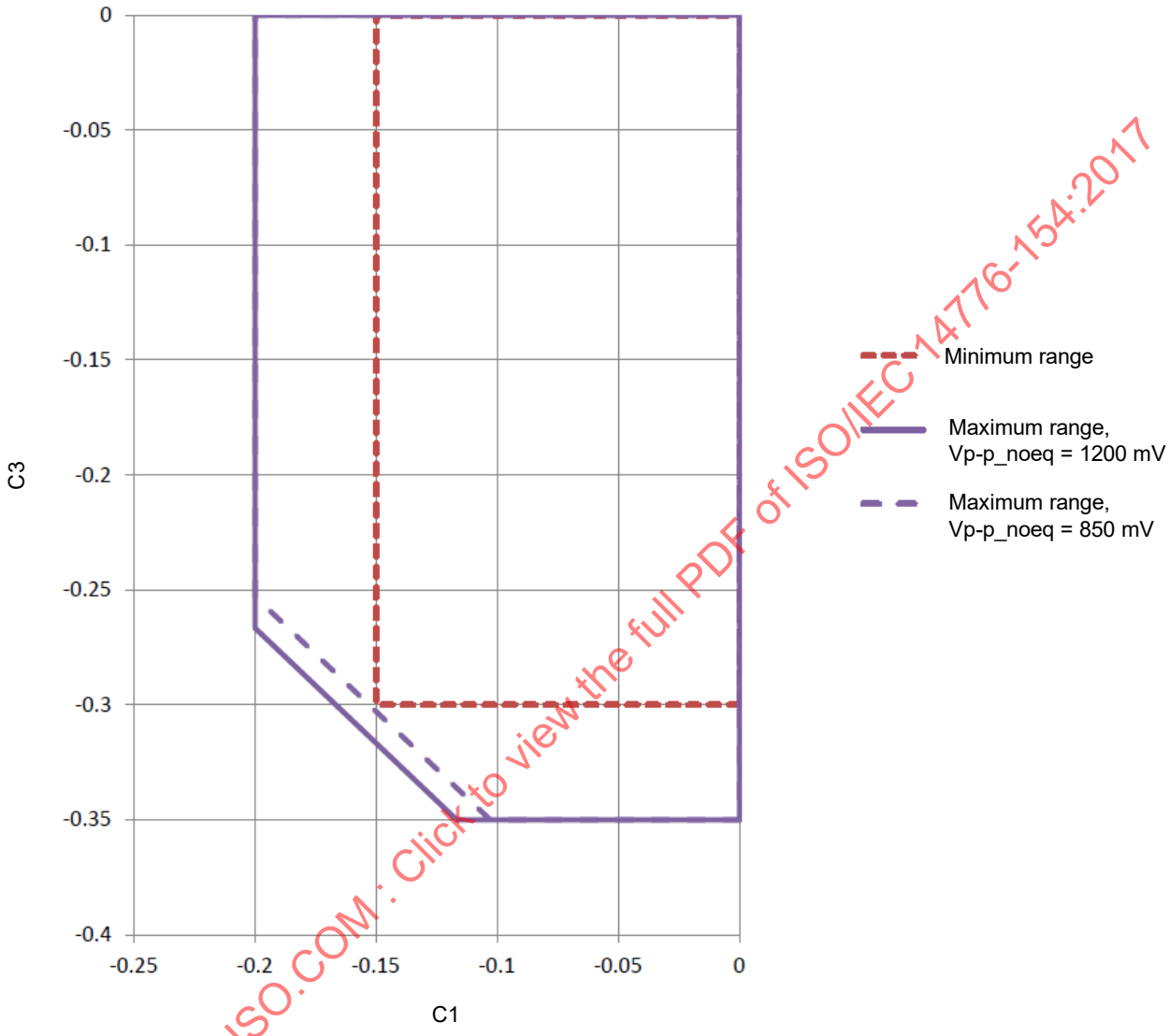


Figure 131 – Minimum and maximum coefficient ranges at maximum peak to peak voltage

Table 43 defines the transmitter device common mode voltage limit characteristics.

Table 43 – 12 Gbit/s transmitter device common mode voltage limit characteristics

Characteristic	Reference	L [a] dBmV [b]	N [a] dBmV [b c]	S [a] dBmV/decade [b]	H [a] dBmV [b]	f_{min} [a] MHz	f_{max} [a] GHz
Spectral limit of common mode voltage [d]	Figure 132	12.7	26.0	13.3	30.0	100	9.0

[a] See figure 4 in 5.2 for definitions of L, N, S, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (rms). Hence, 0 dBm is 1 mW which is 158 mV (rms) across 25 Ω (i.e., the reference impedance for common mode voltage) which is 20 × $\log_{10}$(158) = +44 dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at 3 GHz (see figure 132).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Figure 132 shows the transmitter device common mode voltage limit defined in table 43.

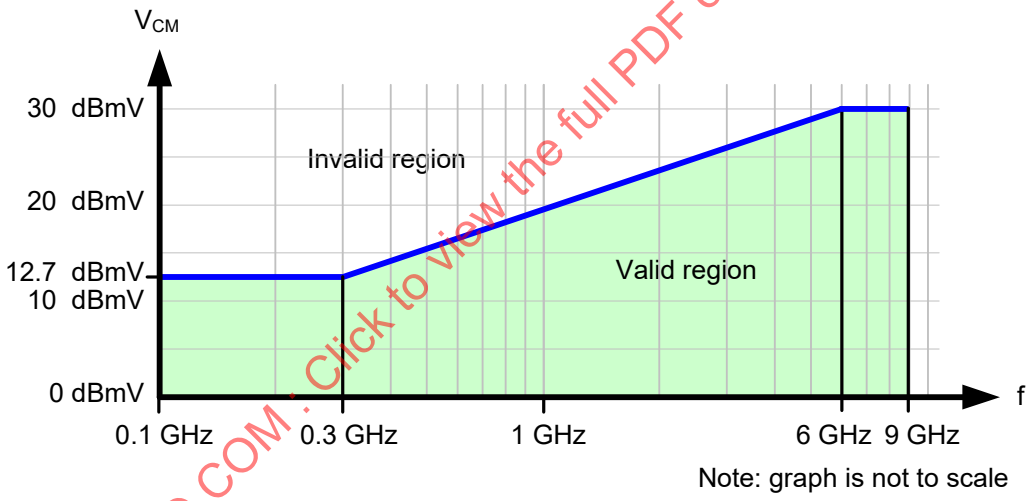


Figure 132 – 12 Gbit/s transmitter device common mode voltage limit

Transmitter equalization coefficient adjustments are controlled using the protocol defined in SPL-3. Transmitter circuits that support 12 Gbit/s, if not operating in optical mode, shall:

a) support the coefficient requests shown in table 44; and
b) provide equalization equivalent to the reference transmitter device (see 5.8.4.7.3).

The algorithm for optimizing the transmitter coefficient is beyond the scope of this Document.

Table 44 – Transmitter coefficient requests and corresponding transmitter circuit response

Coefficient 1 request	Coefficient 2 request	Coefficient 3 request	Description	$v_{HL}(k+1)$- $v_{HL}(k)$ mV(P-P)	$v_1(k+1)$ - $v_1(k)$ mV	$v_2(k+1)$ - $v_2(k)$ mV	$v_3(k+1)$ - $v_3(k)$ mV
hold	hold	hold	Hold peak to peak voltage and hold equalization	-20 to +20 [a]	-10 to +10 [a]	-10 to +10 [a]	-10 to +10 [a]
dec	dec	hold	Increase precursor and hold peak to peak voltage	-20 to +20	-40 to -10	-40 to -10	-10 to +10
inc	inc	hold	Decrease precursor and hold peak to peak voltage	-20 to +20	+40 to +10	+40 to +10	-10 to +10
hold	dec	dec	Increase post cursor and hold peak to peak voltage	-20 to +20	-10 to +10	-40 to -10	-40 to -10
hold	inc	inc	Decrease post cursor and hold peak to peak voltage	-20 to +20	-10 to +10	+40 to +10	+40 to +10
hold	dec	hold	Decrease peak to peak voltage and hold equalization	-40 to -10	-20 to -5	-20 to -5	-20 to -5
hold	inc	hold	Increase peak to peak voltage and hold equalization	+40 to +10	+20 to +5	+20 to +5	+20 to +5
dec	hold	hold	Increase precursor and increase peak to peak voltage	+40 to +10	-20 to -5	-20 to -5	+20 to +5
inc	hold	hold	Decrease precursor and decrease peak to peak voltage	-40 to -10	+20 to +5	+20 to +5	-20 to -5
hold	hold	dec	Increase post cursor and increase peak to peak voltage	+40 to +10	+20 to +5	-20 to -5	-20 to -5
hold	hold	inc	Decrease post cursor and decrease amplitude	-40 to -10	-20 to -5	+20 to +5	+20 to +5

Key:

hold = Requests no change be made to the coefficient. Equivalent to hold in SPL-3.
dec = Request to make the coefficient more negative. Equivalent to decrement in SPL-3.
inc = Request to make the coefficient more positive. Equivalent to increment in SPL-3.

[a] The peak to peak voltage and equalization voltage differences between the initial condition and following any single or consecutive hold/hold/hold command shall not be greater than the specified range.

The transmitter circuit responses specified in table 44 shall be measured with a zero-length test load as shown in figure 133. The test fixture is de-embedded back to output of the transmitter circuit ET. D.C. losses are not de-embedded. For de-embedding methods see clause F.5.

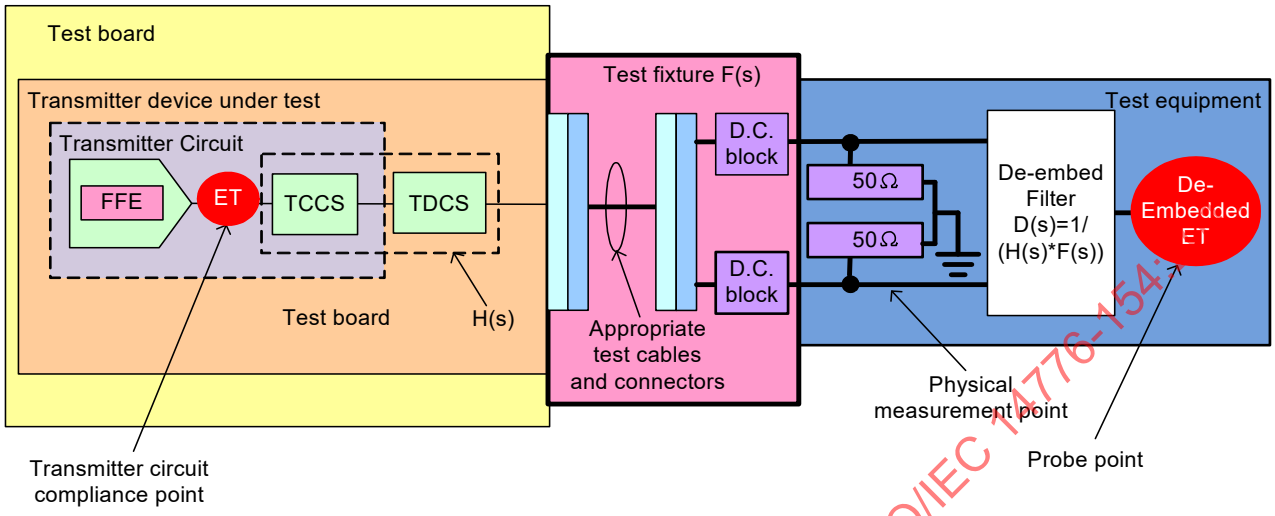


Figure 133 – Transmitter circuit compliance test configuration

All response specifications are based on differential measurements.The output waveform for a TRAIN_DONE primitive (see SPL-3) is shown in figure 134 where:

a) T is the symbol period;
b) t_1 is the zero-crossing point of the rising edge of the positive 5 UI CID;
c) t_2 is the zero-crossing point of the falling edge of the positive 5 UI CID;
d) t_3 is the zero-crossing point of the falling edge of the negative 5 UI CID;
e) t_4 is the zero-crossing point of the rising edge of the negative 5 UI CID;
f) v_1 is the maximum voltage measured in the interval t_1 to t_1 + T;
g) v_2 is the average voltage measured in the interval t_1 + 2T to t_1 + 3T;
h) v_3 is the maximum voltage measured in the interval t_2 - T to t_2;
i) v_4 is the minimum voltage measured in the interval t_3 to t_3 + T;
j) v_5 is the average voltage measured in the interval t_3 + 2T to t_3 + 3T;
k) v_6 is the maximum voltage measured in the interval t_4 - T to t_4;
l) VMA is v_2 - v_5; and
m) v_{HL} is the peak to peak voltage measured in the interval t_1 to t_1 + 80T.

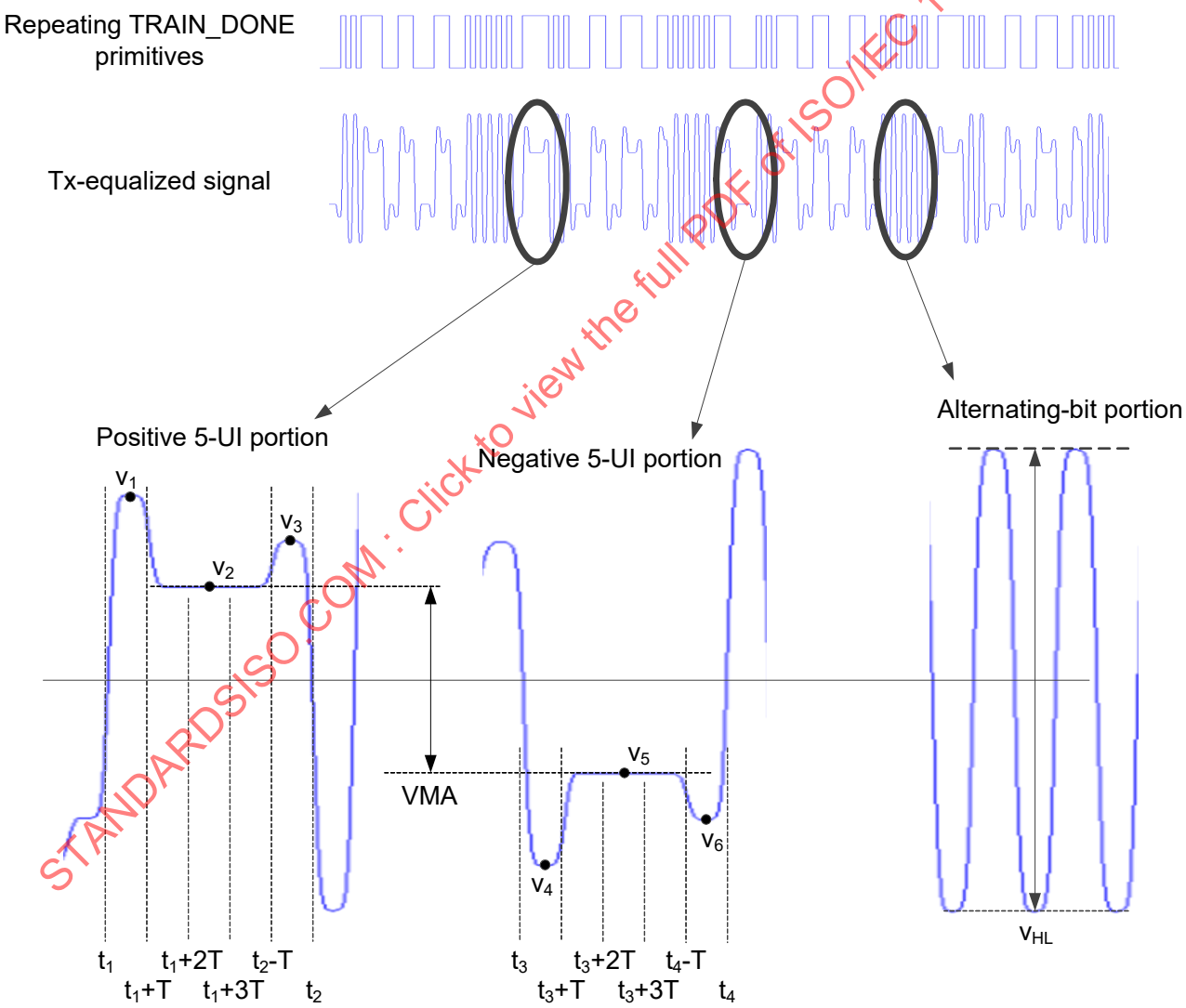


Figure 134 – 12 Gbit/s transmitter circuit output waveform

Equalization ratios are defined based on these voltages,

$$R_{post} = \frac{v_1}{v_2}$$

$$R_{pre} = \frac{v_3}{v_2}$$

Transmitter coefficient presets may be requested using a protocol that is defined in the SPL-3 standard. Transmitter circuits that support 12 Gbit/s shall:

a) support the coefficient settings shown in table 45; and
b) provide equalization equivalent to the reference transmitter device (see 5.8.4.7.3).

Table 45 – Transmitter circuit coefficient presets at ET

Coefficient settings [a]	R_{pre} (V/V) [b]			R_{post} (V/V) [b]		
	Min	Nom	Max	Min	Nom	Max
normal [c]						
reference_1 [d e]	2.10	2.52	2.97	2.94	3.52	4.16
reference_2 [e f]	1.05	1.26	1.49	1.19	1.43	1.68
no_equalization [e g]	0.84	1.00	1.19	0.84	1.00	1.19

Key:

Max = Maximum
Min = Minimum
Nom = Nominal

[a] The coefficient setting field in the TTIU (see SPL-3).
[b] All measurements are performed with a repeating TRAIN_DONE primitive (see SPL-3 and figure 133). If a simulation tool (e.g., SAS3_EYEOPENING) is used then this measurement may be performed with IDLE dwords (see SPL-3) as the test pattern.
[c] See SPL-3.
[d] Equivalent to the reference transmitter setting transmitter circuit coefficient 1 (i.e., C1) set to -0.15, coefficient 2 (i.e., C2) set to 0.6, and coefficient 3 (i.e., C3) set to -0.25 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.
[e] The reference_1, reference_2, and no_equalization presets shall set the transmitter to its maximum peak to peak voltage (V_{P-P}).
[f] Equivalent to the reference transmitter setting transmitter circuit C1 set to -0.075, C2 set to 0.8, and C3 set to -0.125 with a ± 1.5 dB tolerance on R_{pre} and R_{post}.
[g] Equivalent to the reference transmitter setting transmitter circuit C1 set to zero, C2 set to one, and C3 set to zero with a ± 1.5 dB tolerance on R_{pre} and R_{post}.

5.8.4.7.2 12 Gbit/s Transmitter device S-parameter limits

S-parameter limits are calculated per the following formula:

$$\text{Measured value} < \max [L, \min [H, N + 13.3 \times \log_{10}(f / 3\ \text{GHz})]]$$

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 46 defines the maximum limits for S-parameters of the 12 Gbit/s transmitter device.

Table 46 – 12 Gbit/s maximum limits for S-parameters at IT_S or CT_S

Characteristic [a] [b]	L [c] dB	N [c] dB	H [c] dB	S [c] dB / decade	f_{min} [c] MHz	f_{max} [c] GHz
$\|S_{CC22}\|$	-6.0	-5.0	-1.0	13.3	100	9.0
$\|S_{DD22}\|$	-10	-7.9	-3.9	13.3	100	9.0
$\|S_{CD22}\|$	-26	-12.7	-10	13.3	100	9.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b pattern or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol Specific diagnostic page in SPL-3). The amplitude applied by the test equipment shall be less than -4.4 dBm (i.e., 190 mV zero to peak) per port (see F.11.4.2).
[b] $|S_{DC22}|$ is not specified.
[c] See figure 4 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 135 shows the 12 Gbit/s transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 46.

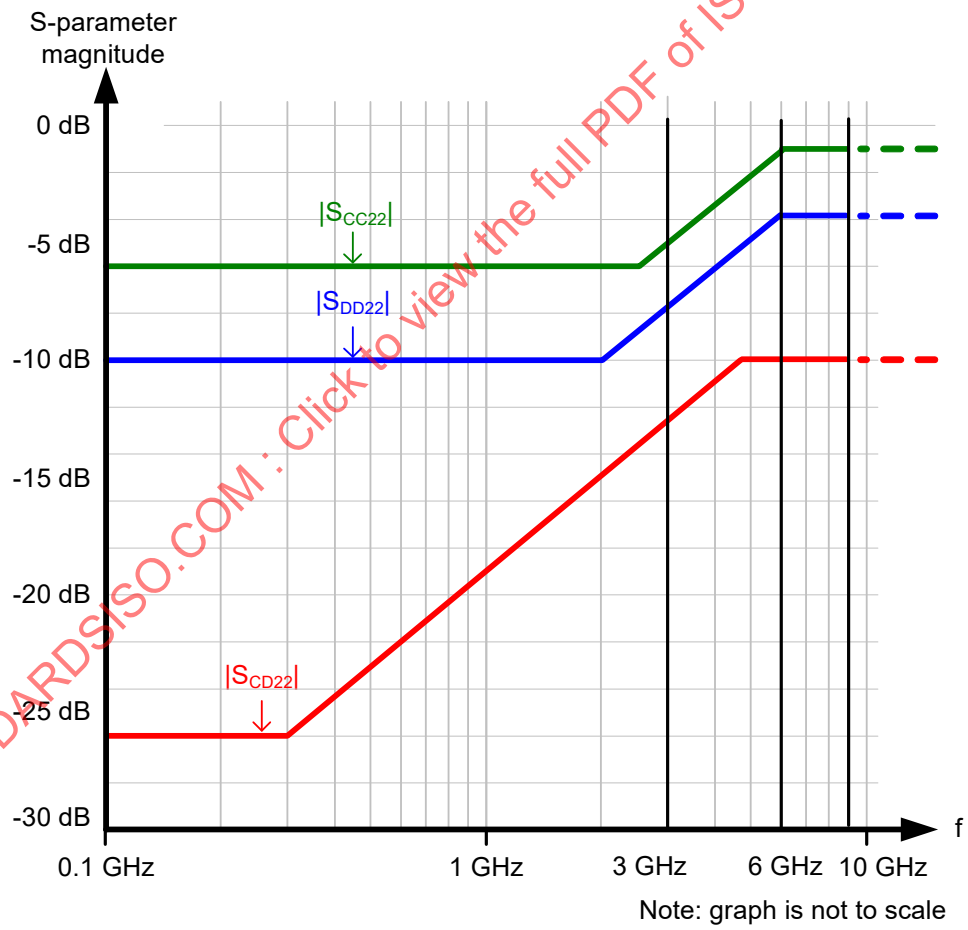


Figure 135 – 12 Gbit/s transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.8.4.7.3 12 Gbit/s reference transmitter device

The 12 Gbit/s reference transmitter device is a set of parameters and equalization filters defining the electrical performance characteristics of a transmitter circuit used in simulation. Figure 136 illustrates the reference transmitter device.

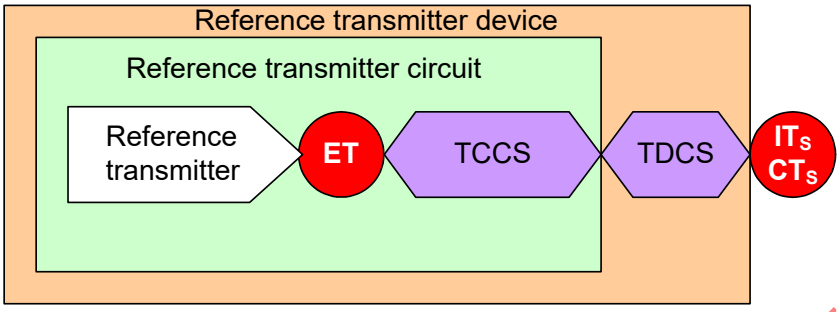


Figure 136 – 12 Gbit/s reference transmitter device

Figure 137 shows the reference transmitter generating the signal at ET. Passive TxRx connection segments TCCS and TDCS simulate the reference TxRx connection segment between ET and CT_S or ET and IT_S. See clause D.2 for the description of the reference TxRx connection segments.

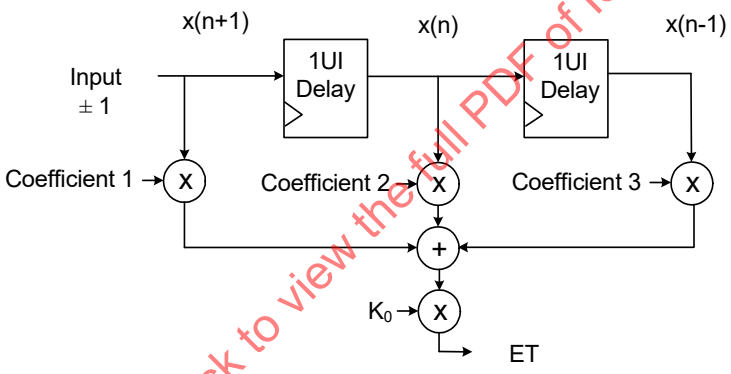


Figure 137 – 12 Gbit/s reference transmitter

During 12 Gbit/s end to end simulations (see 5.7), the reference transmitter device parameters are optimized to maximize the eye opening at the output of the reference receiver device (5.8.5.7.3) using the procedure defined in 5.7.3. Table 47 defines the reference transmitter device characteristics. The reference transmitter device shall use the minimum peak to peak voltage and minimum rise/fall time. The input is a unitless stream of pulses representing transmitted data. The amplitude of these pulses reach +1 or -1. The stream of pulses contain the jitter and rise/fall time characteristics defined in table 47.

Table 47 – 12 Gbit/s reference transmitter device characteristics at ET

Signal characteristic	Units	Minimum	Nominal	Maximum
Output gain (K_0)	V/V	0.425		
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		
Precursor coefficient (i.e., coefficient 1) [a]	V/V	-0.15		0
VMA [b]	mV(P-P)	80		
Post cursor coefficient (i.e., coefficient 3) [a]	V/V	-0.3		0
Rise/fall time [c]	ps	25		
RJ [d e]	UI			0.15
DJ [f]	UI			0.1

[a] V_{P-P} is constrained in the reference transmitter device by
C2 = 1 - |C1| - |C3|
where:
C1 = coefficient 1;
C2 = coefficient 2; and
C3 = coefficient 3.

[b] VMA = $2K_0$ (C1 + C2 + C3) V.

[c] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3).

[d] 0.15 UI is 12.5 ps at 12 Gbit/s.

[e] RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.

[f] 0.1 UI is 8.3 ps at 12 Gbit/s.

5.8.4.7.4 Transmitter device end to end simulation characteristics for trained 12 Gbit/s

The end to end simulation procedure for transmitter devices connected to passive TxRx connections is as follows:

1) set the transmitter to output IDLE dwords (see SPL-3);
2) set the transmitter to the no_equalization coefficient setting (see SPL-3);
3) capture the signal at IT (see 5.3.3) or CT (see 5.3.3) into a zero-length test load (see 5.6.2);
4) measure the total crosstalk amplitude (see 5.7.4) or extract crosstalk transfer functions (e.g., S-parameters);
5) connect TxRx connection segments, crosstalk segments, reference transmitter and reference receiver according to the reference end to end simulation diagram (see 5.7.2, D.2.1 and D.2.2);
6) set the reference transmitter equalization (see 5.7.3) and reference receiver DFE equalization (see 5.8.5.7.3); and
7) perform a linear simulation, including the effects of edge rates, ISI and crosstalk (see clause D.1).

The characteristics of the signal at specified points in the simulation are defined in table 48. See the reference transmitter device (see 5.8.4.7.3) for definitions of coefficient 1 (i.e., C1), coefficient 2 (i.e., C2), and coefficient 3 (i.e., C3).

Table 48 – Transmitter device characteristics for trained 12 Gbit/s at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Coefficient 1 (i.e., C1) [a b c]	V/V	-0.15	0	ET
VMA [d e]	mV(P-P)	80		ET
Coefficient 3 (i.e., C3) [a b f]	V/V	-0.3	0	ET
Reference pulse response cursor peak to peak amplitude [g]	mV(P-P)	135		ER
Vertical eye opening to reference pulse response cursor ratio [h i]	%	45		ER
DFE coefficient amplitude to reference pulse response cursor ratio [j]	%	-50	50	ER

[a] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.

[b] C2 = 1 - |C1| - |C3|.

[c] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.

[d] VMA = $2K_0$ (C1 + C2 + C3) V. See 5.8.4.7.3.

[e] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (C3' - C3)^2)^{0.5}$$

where:

C1' and C3' are values that satisfy the minimum VMA criterion.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] The average amplitude of the eye for an IDLE pattern (see SPL-3) digital input at the compliance point may be used for this measurement. See figure 118.

[h] The vertical eye opening includes the effects of crosstalk (see clause D.1).

[i] The end to end simulation removes any remaining RJ and TJ (i.e., non-ISI) of the transmitter device.

[j] The maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(d_i)) divided by the reference pulse response cursor (see 5.8.5.7.3).

The transmitter coefficients are simulated by replacing the test transmitter by the reference transmitter generating no jitter (i.e., no RJ or TJ). This is equivalent to inserting a jitter-free reference transmitter with K_0 set to one (i.e., unit-less value) at the output of the transmitter device (see 5.8.4.7.3), using the transmitter device output as the input of the reference transmitter instead of the +1/-1 digitized stream (see figure 138). For non-separable TxRx connection segments, the reference simulation channel (i.e., <usage>_IR_RR) does not include the reference PICS.

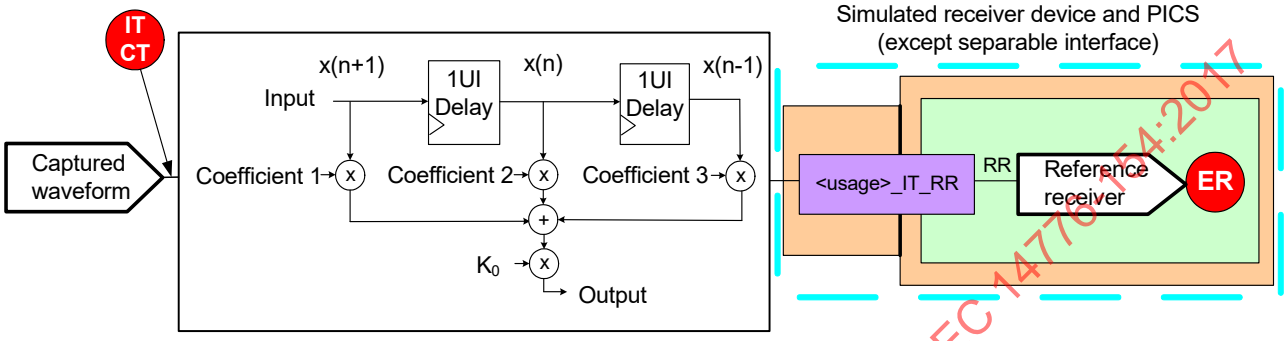


Figure 138 – Simulation of the reference transmitter from a captured signal

5.8.4.7.5 Transmitter device signal output characteristics at CT_S for 12 Gbit/s when an active cable is connected

Transmitter devices supporting trained 12 Gbit/s that are connected to an external cable connector shall support the signal characteristics specified in table 49 at CT_S when an active cable is connected.

Table 49 – Transmitter device signal output characteristics for 12 Gbit/s at CT_S when an active cable is connected

Signal characteristic	Units	CT_S
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 102) [a] [b]	mV(P-P)	1 200
Minimum eye opening (i.e., 2 × Z1 in figure 102) [a] [c]	mV(P-P)	200
Maximum half of TJ (i.e., X1 in figure 102) [a] [c] [d]	UI	0.175
Maximum RJ [a] [b] [d]	UI	0.15
Center of bit time (i.e., X2 in figure 102)	UI	0.5

[a] All crosstalk sources shall be active with representative traffic during the measurement.
[b] The maximum peak to peak voltage measurement and RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[c] The minimum eye opening measurement and TJ measurement shall be performed with the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) with SSC enabled for a period of at least 33.3 µs (i.e., a full SSC cycle).
[d] The measurement shall include the effects of the JTF (see 5.8.3.2).

5.8.4.8 Transmitter device signal output characteristics for OOB signals

Transmitter devices supporting SATA shall use SATA Gen1i, Gen2i, or Gen3i signal output levels (see SATA) during the first OOB sequence (see SPL-3) after a power on or hard reset. If the phy does not receive COMINIT within a hot-plug timeout (see SPL-3), then the transmitter device shall increase its transmit levels

to the OOB signal output levels specified in table 50 and perform the OOB sequence again. If no COMINIT is received within a hot-plug timeout of the second OOB sequence, then the transmitter device shall initiate another OOB sequence using SATA Gen1i, Gen2i, or Gen3i signal output levels. The transmitter device shall continue alternating between transmitting COMINIT using SATA Gen1i, Gen2i, or Gen3i signal output levels and transmitting COMINIT with SAS signal output levels until the phy receives COMINIT.

If the phy both transmits and receives COMSAS (i.e., a SAS phy or expander phy is attached), then the transmitter device shall set its transmit levels to the SAS signal output levels (see 5.8.4.4, 5.8.4.5, and 5.8.4.6) prior to beginning the SAS speed negotiation sequence (see SPL-3). If transmitter device had been using SATA Gen1i, Gen2i, or Gen3i signal output levels, this mode transition (i.e., output voltage change) may result in a transient (see 5.8.2) during the idle time between COMSAS and the SAS speed negotiation sequence.

If the transmitter device is using SAS signal output levels and the phy does not receive COMSAS (i.e., a SATA phy is attached), then the transmitter device shall set its transmit levels to the SATA Gen1i, Gen2i, or Gen3i signal output levels and restart the OOB sequence.

Transmitter devices that do not support SATA or that have optical mode enabled shall transmit OOB signals using SAS signal output levels. In phy low power conditions (see SPL-3) the output common mode specification OOB common mode delta (see table 50) is relaxed to enable transmitter device power savings. During phy low power conditions, the transmitter device should reduce its output swing level to save power. Before exiting a phy low power condition the transmitter device shall wait for its common mode to settle.

Table 50 defines the transmitter device signal output characteristics for OOB signals.

Table 50 – Transmitter device signal output characteristics for OOB signals

Characteristic	Units	IT	CT
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 123) [a]	mV(P-P)	1 600	
OOB offset delta [b c]	mV	± 25	
OOB common mode delta [c d]	mV	± 50	
Minimum OOB burst amplitude [e], if SATA is not supported	mV(P-P)	240 [f]	
Minimum OOB burst amplitude [e], if SATA is supported	mV(P-P)	240 [f g]	N/A

[a] The recommended maximum peak to peak voltage is 1 200 mV(P-P).
[b] The maximum difference in the average differential voltage (D.C. offset) component between the burst times and the idle times of an OOB signal.
[c] This is not applicable when optical mode is enabled or in phy low power conditions.
[d] The maximum difference in the average of the common mode voltage between the burst times and the idle times of an OOB signal.
[e] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst as measured with each test load at IT and CT.
[f] The OOB burst contains either 1.5 Gbit/s repeating 0011b pattern or 1100b pattern (e.g., D24.3), 1.5 Gbit/s ALIGN (0) primitives, or 3 Gbit/s ALIGN (0) primitives (see SPL-3 and SATA).
[g] Amplitude measurement methodologies of SATA and this document differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this document may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.8.5 Receiver device characteristics

5.8.5.1 Receiver device characteristics overview

The receiver device shall operate within the required BER (see 5.5.1) when a signal with valid voltage and timing characteristics is delivered to the receiver device compliance point from a nominal 100 Ω source. The received signal shall be considered valid if it meets the voltage and timing limits specified in table 54 (see 5.8.5.4) for untrained 1.5 Gbit/s and 3 Gbit/s and table 58 (see 5.8.5.7.1) for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) receiver device requirements.

Additionally, for untrained 1.5 Gbit/s and 3 Gbit/s the receiver device shall operate within the required BER when the signal has additional SJ present as specified in table 56 (see 5.8.5.6) with the common mode signal V_{CM} as specified in table 51 (see 5.8.1). Jitter tolerance for receiver device compliance points is shown in figure 125 (see 5.8.3.5). Figure 125 assumes that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver device, the additional 0.1 UI of SJ may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiver device. The additional jitter reduces the eye opening in both voltage and time. For trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s the additional jitter is included in the stressed receiver device jitter tolerance test (see 5.8.5.7.6).

Compliance points referenced in the electrical requirement tables are shown in 5.3 unless otherwise specified.

See clause F.10 for a methodology for measuring receiver device signal tolerance.

A receiver device shall provide equivalent performance to the reference receiver device (see 5.8.5.7.3) and shall operate within the required BER when attached to:

a) any transmitter device compliant with this document (see 5.8.4); and
b) any TxRx connection compliant with this document (see 5.5).

5.8.5.2 Receiver device coupling requirements

Coupling requirements for receiver devices are as follows:

a) all receiver devices (i.e., attached to IR (see 5.3) or CR (see 5.3) compliance points) shall be A.C. coupled to the interconnect through a receive network.

See table 31 (see 5.8.1) for the coupling capacitor value.

5.8.5.3 Receiver device general electrical characteristics

Table 51 defines the receiver device general electrical characteristics.

Table 51 – Receiver device general electrical characteristics

Characteristic	Units	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s
Physical link rate accuracy [a] tolerance at IR if SATA is not supported	ppm	± 100			
Physical link rate accuracy [a] tolerance at IR if SATA is supported	ppm	± 350			
Physical link rate SSC modulation tolerance at IR and CR	ppm	See table 71 in 5.8.6.3			
Maximum receiver device transients [b]	V	± 1.2			
Minimum receiver A.C. common mode voltage tolerance V_{CM} [c d]	mV(P-P)	150			
Receiver A.C. common mode frequency tolerance range F_{CM} [c]	MHz	2 to 200			

[a] Physical link rate accuracy shall be measured over a minimum of 1 x 10^6 UI and should be measured using a minimum resolution of 100 Hz.
[b] See 5.8.2 for transient test circuits and conditions.
[c] Receiver devices shall tolerate sinusoidal common mode noise components within the peak to peak amplitude (V_{CM}) and the frequency range (F_{CM}).
[d] The measurement shall be made with a channel equivalent to the channel used in the zero-length test load (see figure 105) (see 5.6.2).

The common mode frequency tolerance range for 6 Gbit/s and 12 Gbit/s is extended to include the effects of duty cycle distortion. Measurement methods for testing the extended frequency ranges for A.C. common mode tolerance are not defined by this document; therefore the common mode signal characteristics defined in table 52 are recommended design guidelines for receiver devices supporting 6 Gbit/s and 12 Gbit/s.

Table 52 – Recommended receiver device common mode tolerance for 6 Gbit/s, and 12 Gbit/s

Characteristic	Units	6 Gbit/s	12 Gbit/s
Minimum receiver A.C. common mode voltage tolerance V_{CM} [a b]	mV(P-P)	150	
Receiver A.C. common mode frequency tolerance range F_{CM} [b]	MHz	2 to 3 000	2 to 6 000

[a] Receiver devices should be designed to tolerate sinusoidal common mode noise components within the peak to peak amplitude (V_{CM}) and the frequency range (F_{CM}).
[b] The value represents the signal characteristic at IR or CR when the channel between the transmitter device and IR or CR is equivalent to the channel used in the zero-length test load (see figure 105) (see 5.6.2).

Table 53 defines the receiver device termination characteristics.

Table 53 – Receiver device termination characteristics

Characteristic	Units	Untrained		Trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s
		1.5 Gbit/s	3 Gbit/s	
Differential impedance [a b c]	Ω	100 ± 15		See 5.8.5.7.1
Maximum differential impedance imbalance [a b c d]	Ω	5		See 5.8.5.7.2 [e]
Maximum receiver termination time constant [a b c]	ps	150	100	N/A
Common mode impedance [a b]	Ω	20 minimum 40 maximum		See 5.8.5.7.1

[a] All receiver device termination measurements are made through mated connector pairs.

[b] The receiver device termination impedance specification applies to all receiver devices in a TxRx connection and covers all time points between the connector nearest the receiver device, the receiver device, and the transmission line terminator. This measurement shall be made from that connector.

[c] At the time point corresponding to the connection of the receiver device to the transmission line, the input capacitance of the receiver device and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. With impedance measured using amplitude in units of ρ (i.e., the reflection coefficient, a dimensionless unit) and duration in units of time, the area of the impedance dip caused by this capacitance is the receiver termination time constant. The receiver termination time constant shall not be greater than the values shown in this table.

An approximate value for the receiver termination time constant is given by the following equation:

RTTC = amp × width

where:

RTTC receiver termination time constant in seconds;

amp amplitude of the dip in units of ρ (i.e., the difference between the reflection coefficient at the nominal impedance and the reflection coefficient at the minimum impedance point); and

width width of the dip in units of time, as measured at the half amplitude point.

The value of the receiver device excess input capacitance is given by the following equation:

$$C = \frac{RTTC}{(R_0 \| R_R)}$$

where:

C receiver device excess input capacitance in farads;

RTTC receiver termination time constant in seconds;

R_0 transmission line characteristic impedance in Ω;

R_R termination resistance at the receiver device in Ω; and

$(R_0 \| R_R)$ parallel combination of R_0 and R_R.

[d] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.

[e] Measurement replaced by S_{CD11} specifications (i.e., differential to common mode conversion).

5.8.5.4 Delivered signal characteristics for untrained 1.5 Gbit/s and 3 Gbit/s

Table 54 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.6.2) at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) for untrained 1.5 Gbit/s and 3 Gbit/s. These also serve as the required signal tolerance characteristics of the receiver device. For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, see 5.8.5.7.

Table 54 – Delivered signal characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load at IR and CR

Signal characteristic	Units	IR, untrained		CR, untrained	
		1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 124) if a SATA phy is not attached	mV(P-P)	1 600		1 600	
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 124) if a SATA phy is attached	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 124), if a SATA phy is not attached	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 124), if a SATA phy using Gen1i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.6.3)	mV(P-P)	225 [a]	N/A	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 124), if a SATA phy using Gen2i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.6.3)	mV(P-P)	N/A	175 [a]	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 124) if a SATA phy is attached and the TxRx connection is characterized with the low-loss TCTF test load (see 5.6.4)	mV(P-P)	275 [a]		N/A	
Jitter tolerance (see figure 125 in 5.8.3.5) [b] [c]	N/A	See table 56 in 5.8.5.6			
Maximum half of TJ (i.e., X1 in figure 124) [d]	UI	0.275			
Center of bit time (i.e., X2 in figure 124)	UI	0.50			
Maximum intra-pair skew [e]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this document differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this document may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[c] SSC shall be enabled if the receiver device supports being attached to SATA. Jitter setup shall be performed prior to application of SSC.

[d] The value for X1 shall be half the value given for TJ in table 55. When SSC is disabled, the test or analysis shall include the effects of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667).

[e] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b pattern or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Rx+ and Rx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Rx+ signal and the Rx- signal at the probe points.

5.8.5.5 Maximum delivered jitter for untrained 1.5 Gbit/s and 3 Gbit/s

Table 55 defines the maximum jitter the system shall deliver to the receiver device at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) for untrained 1.5 Gbit/s and 3 Gbit/s. For trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s see 5.8.5.7.6.

Table 55 – Maximum delivered jitter for untrained 1.5 Gbit/s and 3 Gbit/s at IR and CR

Signal characteristic [a b]	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Deterministic jitter (DJ) [c]	UI	0.35	
Total jitter (TJ) [c d e]	UI	0.55	

[a] All DJ and TJ values are level 1 (see MJSQ).
[b] The values for jitter in this table are measured at the average signal amplitude point.
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.8.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] TJ is specified at a CDF level of 10^{-12}.
[e] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.

Jitter peak to peak measured < (maximum TJ - |Asymmetry|)

5.8.5.6 Receiver device jitter tolerance for untrained 1.5 Gbit/s and 3 Gbit/s

Table 56 defines the amount of jitter the receiver device shall tolerate at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) for untrained 1.5 Gbit/s and 3 Gbit/s. Receiver device jitter testing shall be performed with the maximum (i.e., slowest) rise/fall times, minimum signal amplitude, and maximum TJ, and should be performed with normal activity in the receiver device (e.g., with other transmitter circuits and receiver circuits on the same board as the receiver device performing normal activity) with SSC enabled if SSC is supported by the receiver device. Jitter setup shall be performed prior to application of SSC. For trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s see 5.8.5.7.6.

Table 56 – Receiver device jitter tolerance for untrained 1.5 Gbit/s and 3 Gbit/s at IR and CR

Signal characteristic	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Applied sinusoidal jitter (SJ) from f_c to f_{max} [a]	UI	0.10 [e]	0.10 [f]
Deterministic jitter (DJ) [b c]	UI	0.35 [g]	0.35 [h]
Total jitter (TJ) [b c d]	UI	0.65	

[a] The jitter values given are normative for a combination of applied SJ, DJ, and TJ that receiver devices shall be able to tolerate without exceeding the required BER (see 5.5.1). Receiver devices shall tolerate applied SJ of progressively greater amplitude at lower frequencies than f_c, according to figure 139, with the same DJ and RJ levels as were used from f_c to f_{max}.
[b] All DJ and TJ values are level 1 (see MJSQ).
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.8.3.4. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] No value is given for RJ. For compliance with this document, the actual RJ amplitude shall be the value that brings TJ to the stated value at a probability of 10^{-12}. The additional 0.1 UI of applied SJ is added to ensure the receiver device has sufficient operating margin in the presence of external interference.
[e] Applied sinusoidal swept frequency for 1.5 Gbit/s: 900 kHz to 5 MHz.
[f] Applied sinusoidal swept frequency for 3 Gbit/s: 1 800 kHz to 7.5 MHz.
[g] The measurement bandwidth for 1.5 Gbit/s shall be 900 kHz to 750 MHz.
[h] The measurement bandwidth for 3 Gbit/s shall be 1 800 kHz to 1 500 MHz.

Figure 139 defines the applied SJ for table 56.

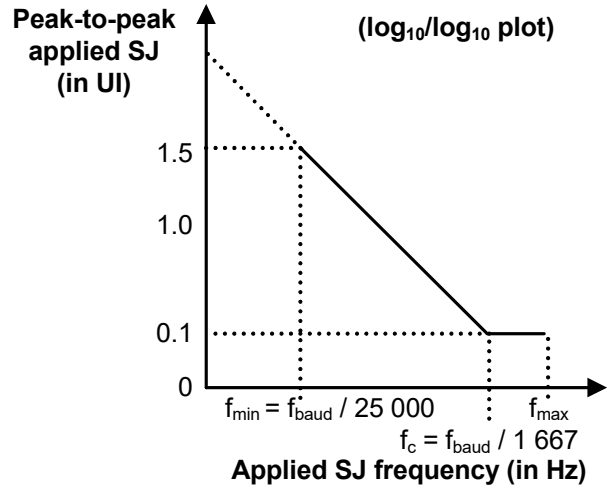


Figure 139 – Applied SJ for untrained 1.5 Gbit/s and 3 Gbit/s

Table 57 defines f_{min}, f_c, and f_{max} for figure 139. f_{baud} is defined in table 31 (see 5.8.1).

Table 57 – f_{min}, f_c, and f_{max} for untrained 1.5 Gbit/s and 3 Gbit/s

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbit/s	60 kHz	900 kHz	5 MHz
3 Gbit/s	120 kHz	1 800 kHz	7.5 MHz

5.8.5.7 Receiver device and delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s

5.8.5.7.1 Delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s

Table 58 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.6.2), unless otherwise specified, attached at the receiver device compliance point (i.e., IR (see 5.3) or CR (see 5.3)) for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s. These also specify the required signal tolerance characteristics of the receiver device. All specifications are based on differential measurements unless otherwise stated.

Table 58 – Delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s at IR and CR compliance point

Characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s [a] [b] [c]	mV(P-P)			1 200
Non-operational input voltage	mV(P-P)			2 000
Reference differential impedance [d]	Ω		100	
Reference common mode impedance [d]	Ω		25	

[a] See 5.8.4.6.6 for the measurement method for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.
[b] See table 42 for the measurement method for 12 Gbit/s.
[c] During OOB, SNW-1, SNW-2, and SNW-3 (see SPL-3), the untrained 1.5 Gbit/s and 3 Gbit/s specifications in 5.8.5.4 apply.
[d] For receiver device S-parameter characteristics, see 5.8.5.7.2.

5.8.5.7.2 Receiver device S-parameter limits

S-parameter limits are calculated per the following formula:

$$\text{Measured value} < \max [L, \min [H, N + 13.3 \times \log_{10}(f / 3\ \text{GHz})]]$$

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at 3 GHz;
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

The frequency for N is based on the Nyquist at 6 Gbit/s.

Table 59 defines the maximum limits for S-parameters of the receiver device.

Table 59 – Maximum limits for S-parameters at IR or CR

Characteristic [a]	L [b] dB	N [b] dB	H [b] dB	S [b] dB / decade	f_{min} [b] MHz	f_{max} [b c] GHz	f_{max} [d] GHz
$\|S_{CC11}\|$	-6.0	-5.0	-1.0	13.3	100	6.0	9.0
$\|S_{DD11}\|$	-10	-7.9	-3.9	13.3	100	6.0	9.0
$\|S_{CD11}\|$	-26	-12.7	-10	13.3	100	6.0	9.0

[a] $|S_{DC11}|$ is not specified.
[b] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.
[c] Applies only for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.
[d] Applies only for 12 Gbit/s.

Figure 140 shows the receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in table 59.

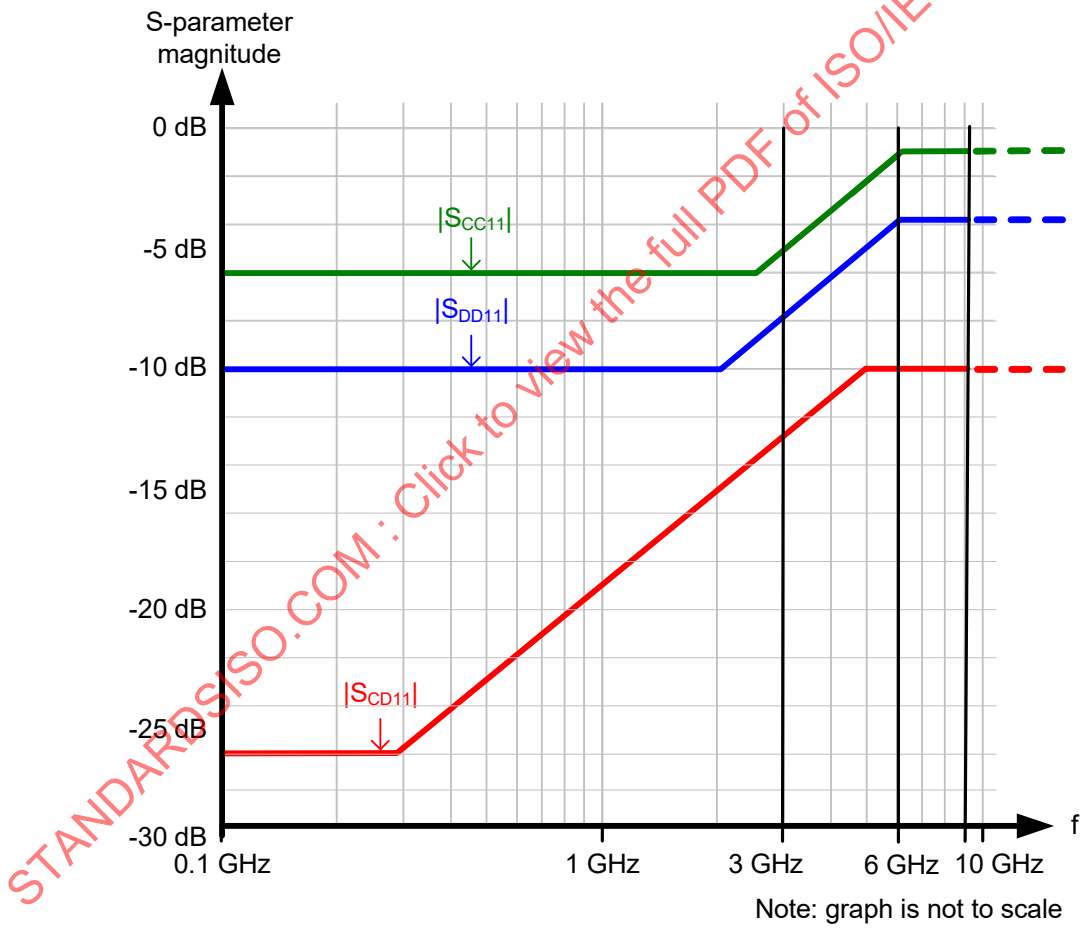


Figure 140 – Receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits

5.8.5.7.3 Reference receiver device characteristics

5.8.5.7.3.1 Reference receiver device overview

The reference receiver device is a set of parameters defining the electrical performance characteristics of a receiver device used in simulation to:

a) determine compliance of a transmitter device (see 5.8.4.6 and 5.8.4.7); and
b) determine compliance of a TxRx connection (see 5.5.5 and 5.5.6).

Figure 141 shows the reference receiver device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

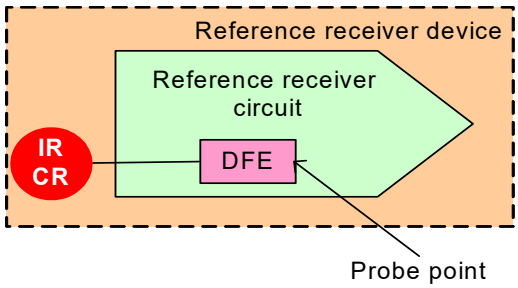


Figure 141 – Reference receiver device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Figure 142 shows the reference receiver device for trained 12 Gbit/s. Passive TxRx connection segments RDCS and RCCS simulate the reference TxRx connection segment between IR and RR or CR and RR. See clause D.2 for the description of the reference TxRx connection segments.

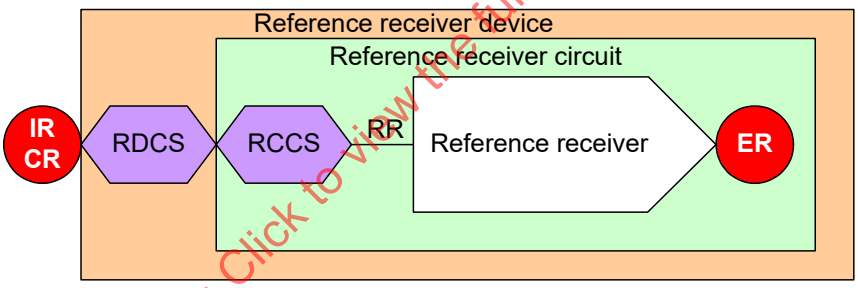


Figure 142 – Reference receiver device for trained 12 Gbit/s

For trained 1.5 Gbit/s, 3 Gbit/s and 6 Gbit/s, the reference receiver circuit performs the reference DFE equalization at the center of the eye.

For trained 12 Gbit/s, the reference receiver device:

1) applies the reference receiver equalization (see 5.8.5.7.3.3);
2) samples the incoming data according to a reference sampling clock (see 3.1.82); and
3) performs the reference DFE equalization.

The signal at the probe point or at ER is an analog signal.

5.8.5.7.3.2 Reference receiver device DFE

The reference receiver device includes a multiple tap DFE with infinite precision taps and unit interval tap spacing. The reference coefficient adaptation algorithm is the LMS algorithm. The DFE may be modeled at the reference sampling instants as:

$$y_k = x_k - \sum_{i=1}^{N_{dfe}} d_i \times \mathrm{sgn}(y_{k-i})$$

where:

y	is the equalizer differential output voltage;
x	is the equalizer differential input voltage;
d	is the equalizer feedback coefficient;
k	is the sample index in UI; and
N_{dfe}	is the number of equalizer DFE taps. N_{dfe} = 3 for the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s reference receiver device. N_{dfe} = 5 for the 12 Gbit/s reference receiver device.

The trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s reference receiver device feedback coefficients (i.e., d_i) have absolute magnitudes that are less than 0.5 times the peak of the equivalent pulse response of the reference receiver device.

NOTE 1 - For more information on DFE and LMS, see John R. Barry, Edward A. Lee, and David G. Messerschmitt. *Digital Communication - Third Edition*. Kluwer Academic Publishing, 2003.

5.8.5.7.3.3 Reference receiver device equalization for trained 12 Gbit/s

The reference receiver applies a filter composed of three cascaded identical equalization stages. Each of these stages has the characteristics described in table 60. The frequency response of each stage is of the form:

$$H(s) = (1 + s/(2\pi \times fz_0)) / [(1 + s/(2\pi \times fp_0)) \times (1 + s/(2\pi \times fp_1))]$$

where:

s	represents $2\pi \times f \times (-1)^{0.5}$;
fz_0	is the zero corner frequency;
fp_0	is the first pole corner frequency; and
fp_1	is the second pole corner frequency.

Table 60 – Reference receiver equalization stage characteristics for trained 12 Gbit/s

Characteristic	Units	Value
Zero corner frequency (fz_0)	GHz	2.5
First pole corner frequency (fp_0)	GHz	4
Second pole corner frequency (fp_1)	GHz	10

5.8.5.7.4 Reference receiver device termination characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The following Touchstone model of the reference receiver device termination is included with this document:

a) SAS2_RxRefTerm.s4p.

Figure 143 shows the S-parameters of the reference receiver device termination model for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

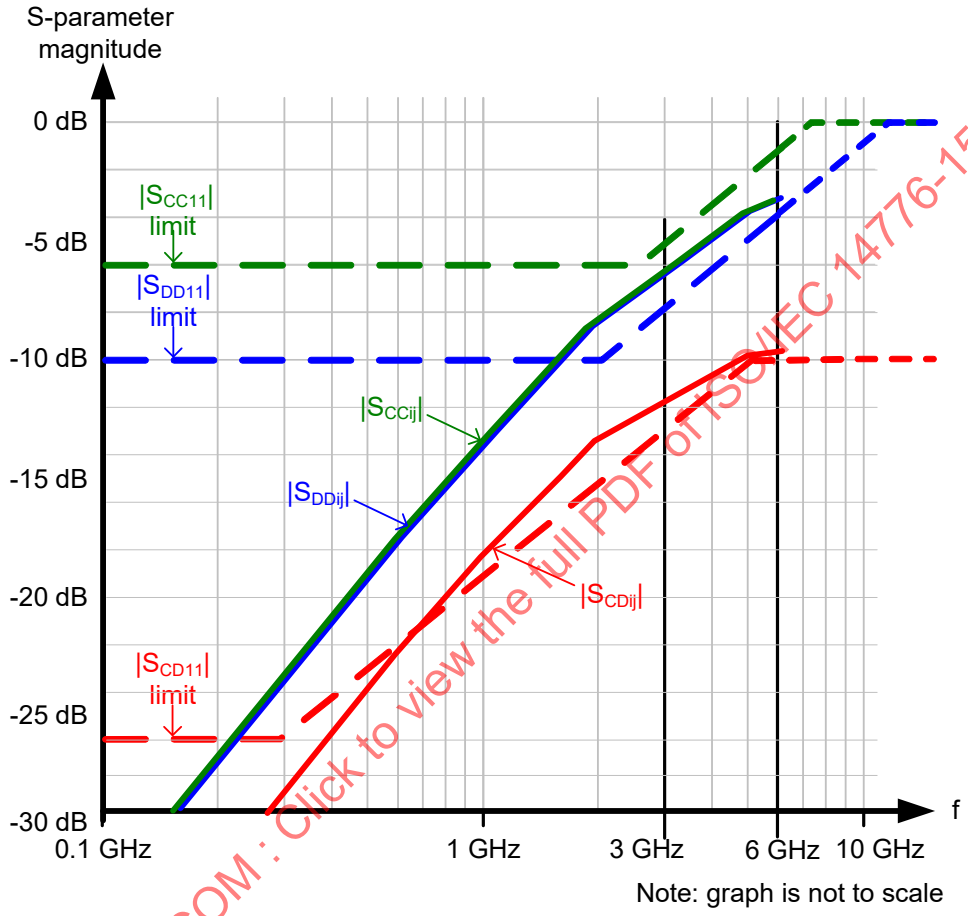


Figure 143 – Reference receiver device termination S-parameters for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The Touchstone model does not exactly match the $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in 5.8.5.7.2 at all frequencies, however, it is a reasonable approximation for use in simulations. See Annex G for a description of how the Touchstone model was created.

5.8.5.7.5 Reference receiver device termination characteristics for trained 12 Gbit/s

The termination characteristics of the reference receiver device for trained 12 Gbit/s are determined by the reference TxRx connection segments used in the simulations (see clause D.2). The reference transmitter presents an ideal termination at RR.

5.8.5.7.6 Stressed receiver device jitter tolerance test

5.8.5.7.6.1 Stressed receiver device jitter tolerance test overview for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

A receiver device shall pass the stressed receiver device jitter tolerance test described in this subclause.

The stressed receiver device jitter tolerance test for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s shall be applied at the receiver device compliance point (i.e., IR (see 5.3.2) or CR (see 5.3.2)) as a means to perform physical validation of predicted performance of the receiver device. Any implementation of the stressed signal generation hardware is permitted for the stressed receiver signal as long as it provides the ISI-stressed signal with jitter and noise as defined in this subclause.

Figure 144 shows the block diagram of the stressed receiver device jitter tolerance test.

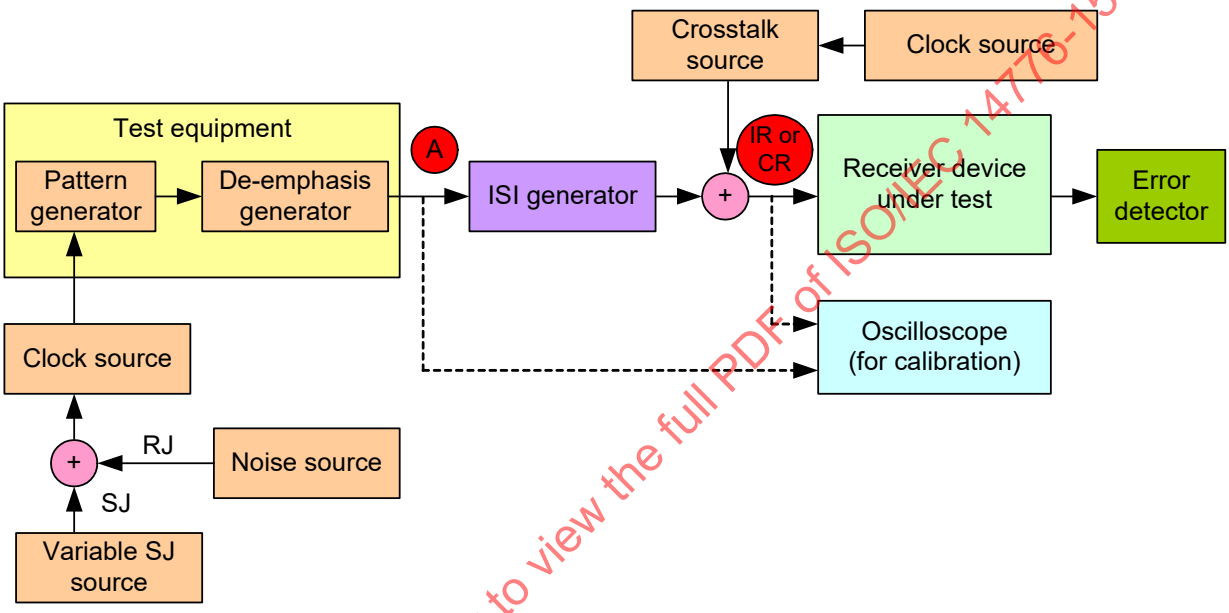


Figure 144 – Stressed receiver device jitter tolerance test block diagram for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The ISI generator shall be representative of, and at least as stressful as, the reference transmitter test load (see 5.6.5). The reference transmitter test load (see 5.6.5), with a nominal $|S_{DD21}|$ of -15 dB at (f_{baud} / 2), may be used as a component of the ISI generator.

The receiver device under test demonstrates its ability to compensate for channel intersymbol interference (ISI) representative of the reference transmitter test load (see 5.6.5) while subjected to the budgeted jitter and crosstalk sources.

Table 61 defines the stressed receiver device jitter tolerance test characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. Unless otherwise noted, characteristics are measured at IR (see 5.3.2) or CR (see 5.3.2) in figure 144.

Table 61 – Stressed receiver device jitter tolerance test characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Characteristic	Units	Minimum	Nominal	Maximum	Reference
TX peak to peak voltage [a]	mV(P-P)		850		5.8.4.6.1
Transmitter equalization [a]	dB		2		5.8.4.6.6
TX RJ [b c d]	UI	0.135 [e]	0.150 [f]	0.165 [g]	5.8.4.6.1
TX SJ [c]	UI	See figure 148 and figure 149			5.8.5.7.6.9
WDP at 6 Gbit/s [b h]	dB	13		14.5	
WDP at 3 Gbit/s [b h]	dB	7		8.5	
WDP at 1.5 Gbit/s [b h]	dB	4.5		6	
D24.3 eye opening [b i]	mV(P-P)	200	215	230	5.8.3.4
NEXT offset frequency [i j k]	ppm	2 500			
Total crosstalk amplitude [i k]	mV_{rms}	4			
Receiver device configuration [l]					

[a] For a characteristic with only a nominal value, the test setup shall be configured to be as close to that value as possible while still complying with other characteristics in this table.
[b] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.
[c] Measured at point A in figure 144.
[d] Measured after application of the JTF (see 5.8.3.2).
[e] 0.135 UI is 22.5 ps at 6 Gbit/s, 45 ps at 3 Gbit/s, and 90 ps at 1.5 Gbit/s.
[f] 0.150 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[g] 0.165 UI is 27.5 ps at 6 Gbit/s, 55 ps at 3 Gbit/s, and 110 ps at 1.5 Gbit/s.
[h] This value is obtained by simulation with SASWDP (see Annex B). BUJ and RJ shall be minimized for WDP simulations. The WDP value is a characterization of the signal output within the reference receiver device (see 5.8.5.7.3) after equalization.
[i] The repeating 0011b pattern or 1100b pattern (e.g., D24.3) eye opening pertains to the delivered signal at IR or CR. Figure 145 defines this value in an eye diagram.
[j] The NEXT source may use SSC modulation rather than have a fixed offset frequency.
[k] Observed with a histogram of at least 1 000 samples. Additional pseudo-random crosstalk shall be added, if needed, to meet the total crosstalk amplitude specification.
[l] All transmitter devices and receiver devices adjacent to the receiver device under test shall be active with representative traffic with their maximum amplitude and maximum frequency of operation.

Figure 145 shows the stressed receiver device jitter tolerance test repeating 0011b pattern or 1100b pattern (e.g., D24.3) eye opening for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s.

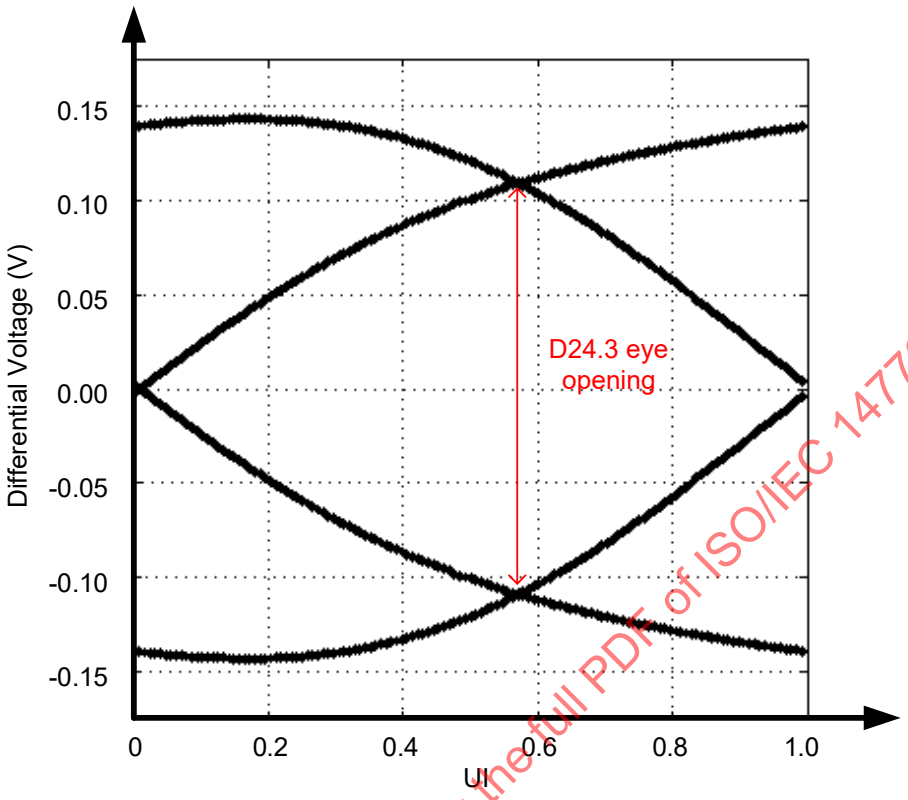


Figure 145 – Stressed receiver device jitter tolerance test D24.3 eye opening for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

5.8.5.7.6.2 Stressed receiver device jitter tolerance test procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The stressed receiver device jitter tolerance test procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.8.5.7.6.3;
2) calibrate the crosstalk source as specified in 5.8.5.7.6.4;
3) attach the test equipment and ISI generator and the crosstalk source to the receiver device under test;
4) configure the pattern generator to transmit a Train_Rx-SNW pattern (see SPL-3);
5) allow the receiver device to complete the Train_Rx-SNW;
6) configure the applied SJ as specified in 5.8.5.7.6.9;
7) configure the pattern generator to transmit CJTPAT (see Annex A); and
8) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

This procedure requires the receiver under test to train during Train_Rx-SNW as specified in SPL-3. This training may be performed by:

a) using the mechanisms defined in SPL-3; or
b) using an equivalent procedure.

The use of an equivalent procedure is outside the scope of this document.

Table 62 defines the number of bits that shall be received with a certain number of errors to have a confidence level of 95 % that the BER is less than 10^{-12}.

Table 62 – Number of bits received per number of errors for desired BER

Number of errors	Number of bits
0	3.00×10^{12}
1	4.74×10^{12}
2	6.30×10^{12}
3	7.75×10^{12}
4	9.15×10^{12}
5	1.05×10^{13}

5.8.5.7.6.3 Test equipment calibration and ISI generator calibration for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The test equipment and ISI generator calibration procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is as follows:

1) ensure that the ISI generator has an $|S_{DD21}|$ comparable to that of the reference transmitter test load (see 5.6.5). $|S_{DD21}|$ delivered by the ISI generator shall be measured by observing the D24.3 eye opening at IR or CR as defined in table 61;
2) attach the test equipment and ISI generator to a zero-length test load, where its signal output is captured by an oscilloscope;
3) disable the crosstalk source;
4) disable the variable SJ source and the random noise source;
5) configure the pattern generator to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3);
6) capture multiple sets of the first 58 data dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern. Waveform averaging shall be used to minimize the impact of measurement noise and jitter on the WDP calculations;
7) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to 'SAS2_LDP'; and
8) adjust the ISI generator until the WDP is within the range defined in table 61 (see 5.8.5.7.6.1).

WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

5.8.5.7.6.4 Crosstalk source calibration for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

The crosstalk source calibration procedure for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s is as follows:

1) attach the test equipment and ISI generator and the crosstalk source to a zero-length test load, where its signal output is captured by an oscilloscope;
2) disable the pattern generator;
3) enable the crosstalk source;
4) set the center frequency of the crosstalk source to be frequency offset from the pattern generator to sweep all potential relative phase alignments between the crosstalk source and the signal from the ISI generator;
5) generate a histograph of the signal delivered to the test equipment; and
6) adjust the crosstalk source until the crosstalk amplitude complies with table 61 (see 5.8.5.7.6.1).

5.8.5.7.6.5 Stressed receiver device jitter tolerance test procedure for trained 12 Gbit/s

The stressed receiver device jitter tolerance test procedure for 12 Gbit/s is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.8.5.7.6.6;
2) calibrate the crosstalk source as specified in 5.8.5.7.6.7;
3) attach the test equipment and ISI generator and the crosstalk generator to the receiver device under test;
4) configure the devices on the receiver device board to transmit and receive representative traffic, including the transmitter device associated with the receiver device under test;
5) configure the pattern generator to transmit a Train_Tx-SNW pattern (see SPL-3);
6) allow the receiver to complete the Train_Tx-SNW;
7) configure the pattern generator to transmit a Train_Rx-SNW pattern (see SPL-3);
8) allow the receiver to complete the Train_Rx-SNW;
9) configure the applied RJ as specified in 5.8.5.7.6.8;
10) configure the applied SJ as specified in 5.8.5.7.6.9;
11) configure the pattern generator to transmit CJTPAT (see Annex A); and
12) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

The configuration of the transmitter device associated with the receiver device under test may be performed after the receiver training completes.

This procedure requires the receiver under test to train during Train_Tx-SNW and Train_Rx-SNW as specified in SPL-3 (see figure 146). This training may be performed by:

a) using the mechanisms defined in SPL-3; or
b) using an equivalent procedure.

The test equipment shall be capable of adjusting its transmitter coefficients as requested by the receiver under test. The use of an equivalent procedure is outside the scope of this document.

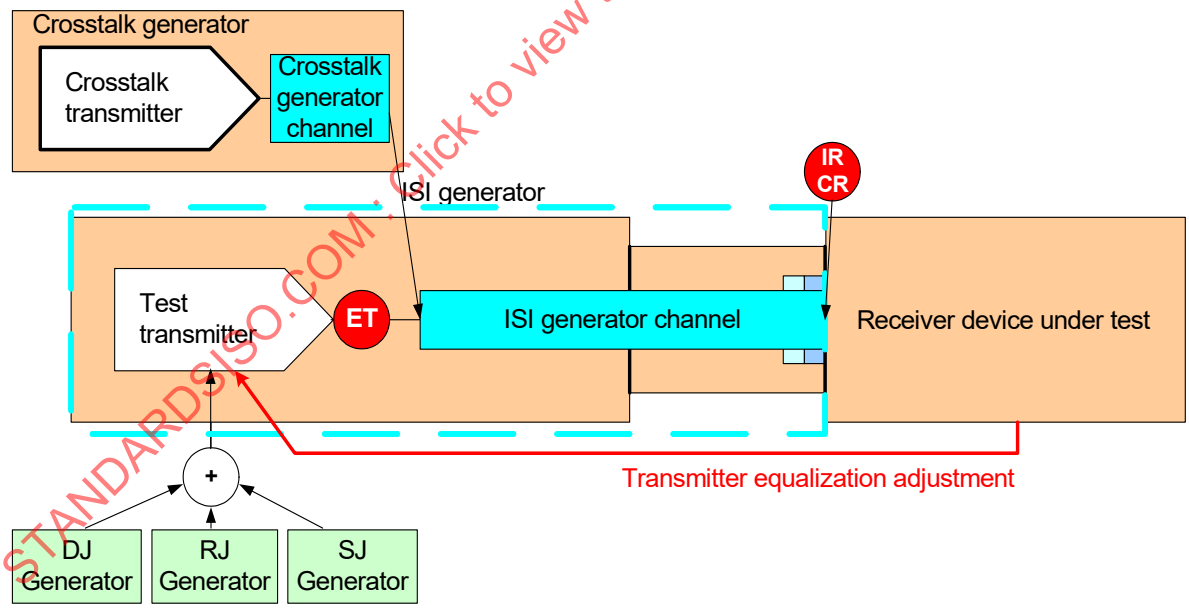


Figure 146 – Stressed receiver transmitter equalization adjustment for 12 Gbit/s

5.8.5.7.6.6 ISI generator calibration for trained 12 Gbit/s

The delivered signal for stressed receiver device jitter tolerance test for 12 Gbit/s (see 5.8.5.7.6) shall provide ISI characteristics defined in table 63.

The characteristics at ER shall be measured using end to end simulations (see 5.7.1 and Annex D).

To simplify de-embedding to ET, the peak to peak voltage may be measured from the output of the ISI generator's transmitter, if the ISI channel has insertion loss less than 1.5 dB at 10 MHz (e.g.,10 MHz represents effective D.C., excluding A.C. coupling). Using this method, the peak to peak voltage is computed by scaling down the measured amplitude by the loss of the ISI channel at 10 MHz. This simplified de-embedding method requires verification of the ISI channel insertion loss.

The effective ISI generator's transmitter output may include attenuators or power combiners. The characteristics of the ISI generator's transmitter, including transmitter circuit response to coefficient steps and coefficient preset settings, are measured including the attenuators or power combiners.

The transmitter coefficients are simulated by replacing the test transmitter by the reference transmitter generating no jitter (i.e., no RJ or TJ). This is equivalent to inserting a jitter free reference transmitter with K_0 set to 1 (unit-less value) at the output of the ISI generator, using the ISI generator's output as the input of the reference transmitter, instead of the +1/-1 digitized stream (see figure 147).

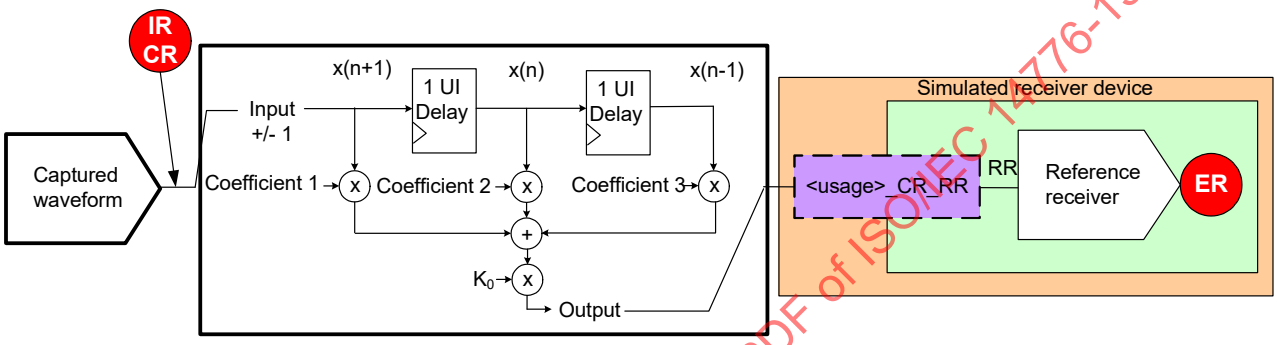


Figure 147 – Simulation of the reference transmitter from a captured signal

The ISI generator's transmitter device shall have the trained 12 Gbit/s transmitter characteristics (see 5.8.4.7). The ISI generator shall be capable of changing its equalization in response to the attached receiver device's back channel requests (see SPL-3). This may be performed using a duplex link as defined in SPL-3, or through the use of an equivalent procedure. The use of an equivalent procedure is outside the scope of this document.

The ISI generator calibration procedure is as follows:

1) set the transmitter of the ISI generator to output no equalization (i.e. coefficient 1 set to zero, coefficient 2 set to one, coefficient 3 set to zero);
2) attach the test equipment and ISI generator to a zero-length test load;
3) disable:
   A) the crosstalk source;
   B) the RJ source;
   C) the DJ source;
   D) the SSC source; and
   E) the variable SJ source;
4) configure the pattern generator to transmit a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3);
5) set the transmitter peak to peak voltage to the characteristics of table 63;
6) configure the pattern generator to transmit IDLE dwords (see SPL-3);
7) capture the signal at IR or CR;
8) simulate signal characteristics and reference transmitter characteristics (see clause D.1), using reference <usage>_CR_RR channel models of the appropriate usage model (see clause D.2); and
9) adjust the ISI generator channel for end to end simulation characteristics defined in table 63.

Table 63 defines the characteristics measured in end to end simulation of the delivered signal for trained 12 Gbit/s stressed receiver device jitter tolerance test.

See the reference transmitter device (see 5.8.4.7.3) for definitions of coefficient 1 (i.e., C1), coefficient 2 (i.e., C2), and coefficient 3 (i.e., C3) used in table 63.

Table 63 – ISI generator characteristics for trained 12 Gbit/s at ET and ER

Characteristic	Units	Minimum	Maximum	Compliance point
Peak to peak voltage [a b]	mV(P-P)	850	1 000	ET (see 5.3.3)
Coefficient 1 (i.e., C1) [c d e]	V/V	-0.15	0	ET
Coefficient 3(i.e., C3) [c d f]	V/V	-0.3	0	ET
VMA [g h]	mV(P-P)	80		ET
Reference pulse response cursor peak to peak amplitude [i j]	mV(P-P)	125	145	ER (see 5.3.3)
Vertical eye opening to reference pulse response cursor ratio [j k l]	%	65	80	ER
DFE coefficient magnitude to reference pulse response cursor ratio [m]	%	5	50	ER

[a] The measurement shall be made with the ISI generator transmitter set to no equalization and a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol Specific diagnostic page in SPL-3).

[b] The peak to peak voltage is adjusted as close as possible to the minimum limit.

[c] If C1 or C3 exceeds its maximum (positive) limit, then it is forced to its maximum limit and the other coefficients are recalculated.

[d] C2 = 1 - |C1| - |C3|.

[e] If C1 exceeds its minimum (negative) limit, then it is forced to its minimum limit and C3 is recalculated.

[f] If C3 exceeds its minimum limit, then it is forced to its minimum limit and C1 is recalculated. If C1 had already reached or exceeded its minimum limit, then both C1 and C3 are forced to their minimum limit.

[g] VMA = $2K_0$ (C1 + C2 + C3) V. See 5.8.4.7.3.

[h] If VMA exceeds its minimum limit, then C1 and C3 are forced to values that have the smallest distance to a point compliant to the VMA specification in the C1/C3 plane. The distance is defined as:

$$((C1' - C1)^2 + (C3' - C3)^2)^{0.5}$$

where:

C1' and C3' are values that satisfy the minimum VMA criterion.

[i] The average amplitude of the eye for a random pattern digital input at the compliance point may be used for this measurement. See figure 118.

[j] The end to end simulation removes any remaining RJ and TJ (i.e., non-ISI) of the ISI generator's transmitter.

[k] The vertical eye opening does not include crosstalk. Crosstalk representing FEXT is calibrated as specified in 5.8.5.7.6.7, while representative traffic is present during the test to provide NEXT crosstalk (see 5.8.5.7.6.5).

[l] The ISI generator is adjusted as close as possible to the maximum reference pulse response cursor and vertical eye opening to reference pulse response cursor ratio limits.

[m] This is the maximum of the absolute value of the reference DFE coefficients (i.e., max(abs(d_i)) divided by the reference pulse response cursor (see 5.8.5.7.3)).

5.8.5.7.6.7 Crosstalk calibration for the trained 12 Gbit/s stressed receiver device jitter tolerance test

Total peak to peak crosstalk noise shall be measured as defined in 5.7.4 at IR (see 5.3.3) or CR (see 5.3.3). The crosstalk is added to the simulation as a measured peak to peak amplitude at a cumulative probability of 10^{-6} (see 5.7.4). The characteristics of the crosstalk amplitude are defined in table D.5. The crosstalk shall be generated by a single transmitter with:

a) a minimum fixed offset frequency of 1 000 ppm; or
b) using SSC modulation rather than the fixed offset frequency.

5.8.5.7.6.8 Applied RJ for trained 12 Gbit/s stressed receiver device jitter tolerance test

The delivered signal for stressed receiver device jitter tolerance test (see 5.8.5.7.6.5) shall provide RJ characteristics defined in table 64.

Table 64 – RJ characteristics for trained 12 Gbit/s stressed receiver device tolerance test

Characteristic	Units	Minimum	Nominal	Maximum
RJ [a b c d]	UI	0.135 [e]	0.150 [f]	0.165 [g]

[a] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.
[b] Measured at ER, IR, or CR as shown in figure 147.
[c] The RJ measurement shall be performed with a repeating 0011b pattern or 1100b pattern (e.g., D24.3) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.
[d] Measured after application of the JTF (see 5.8.3.2).
[e] 0.135 UI is 11.25 ps at 12 Gbit/s.
[f] 0.150 UI is 12.5 ps at 12 Gbit/s.
[g] 0.165 UI is 13.75 ps at 12 Gbit/s.

5.8.5.7.6.9 Applied SJ

Figure 148 defines the applied SJ for trained receiver devices that do not support SSC.

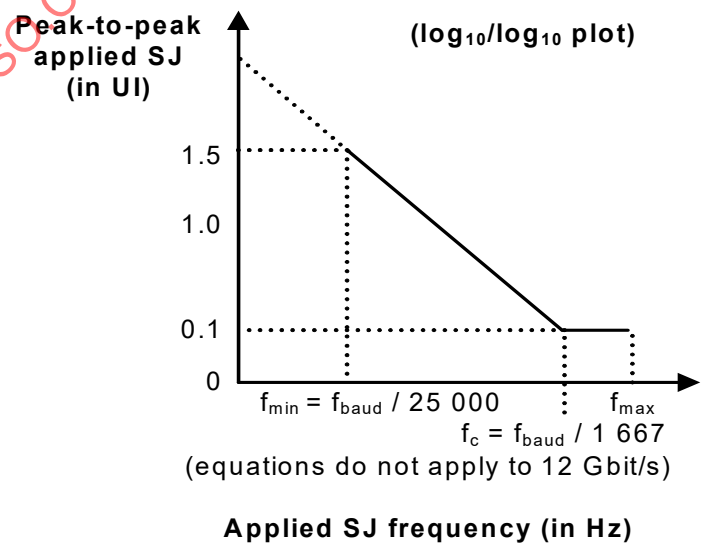


Figure 148 – Applied SJ for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s without SSC support

Table 65 defines f_{min}, f_c, and f_{max} for figure 148. f_{baud} is defined in table 31 (see 5.8.1).

Table 65 – f_{min}, f_c, and f_{max} for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s without SSC support

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbit/s	60 kHz	900 kHz	5 MHz
3 Gbit/s	120 kHz	1 800 kHz	7.5 MHz
6 Gbit/s	240 kHz	3 600 kHz	15 MHz
12 Gbit/s	240 kHz	3 600 kHz	15 MHz

Figure 149 defines the applied SJ for trained receiver devices that support SSC.

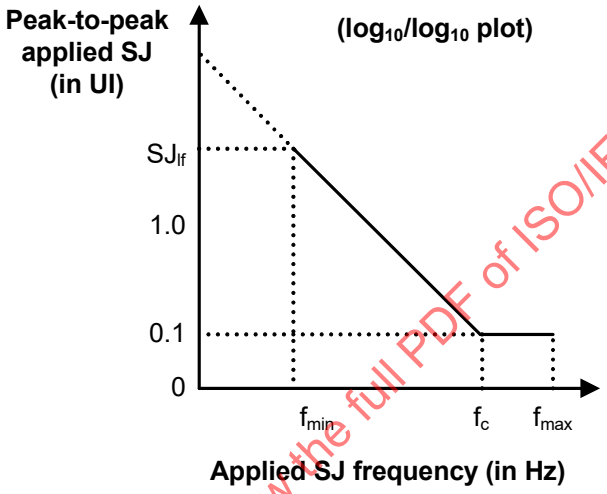


Figure 149 – Applied SJ for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s and 12 Gbit/s with SSC support

Table 66 defines f_{min}, f_c, f_{max}, and SJ_{lf} for figure 149.

Table 66 – f_{min}, f_c, f_{max}, and SJ_{lf} for trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s, and 12 Gbit/s with SSC support

Physical link rate	f_{min}	f_c	f_{max}	SJ_{lf}
1.5 Gbit/s	97 kHz	1.03 MHz	5 MHz	11.3 UI
3 Gbit/s	97 kHz	1.46 MHz	7.5 MHz	22.6 UI
6 Gbit/s	97 kHz	2.06 MHz	15 MHz	45.3 UI
12 Gbit/s	111 kHz	2.06 MHz	15 MHz	34.6 UI

5.8.5.8 Delivered signal characteristics for OOB signals

Table 67 defines the amplitude requirements of the OOB signal delivered by the system with the zero-length test load (see 5.6.2) at the receiver device compliance point (i.e., IR (see 5.3) or CR (see 5.3)). These also serve as the required signal tolerance characteristics of the receiver device.

Table 67 – Delivered signal characteristics for OOB signals

Characteristic	Units	IR	CR
Minimum OOB burst amplitude [a], if SATA is not supported	mV(P-P)	240 [b]	
Minimum OOB burst amplitude [a], if SATA is supported	mV(P-P)	225 [c d]	N/A

[a] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst.
[b] The OOB burst contains either 1.5 Gbit/s repeating 0011b pattern or 1100b pattern (e.g., D24.3), 1.5 Gbit/s ALIGN (0) primitives, or 3 Gbit/s ALIGN (0) primitives (see SPL-3).
[c] The OOB burst contains either 1.5 Gbit/s repeating 0011b pattern or 1100b pattern (e.g., D24.3) or 1.5 Gbit/s ALIGN (0) primitives (see SPL-3 and SATA).
[d] Amplitude measurement methodologies of SATA and this document differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this document may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.8.6 Spread spectrum clocking (SSC)

5.8.6.1 SSC overview

Spread spectrum clocking (SSC) is the technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions.

Phys transmit with SSC as defined in 5.8.6.2 and receive with SSC as defined in 5.8.6.3.

Table 68 defines the SSC modulation types.

Table 68 – SSC modulation types

SSC modulation type	Maximum SSC frequency deviation (SSC_{tol}) [a]			
	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	12 Gbit/s
Center-spreading	+2 300 / -2 300 ppm			+1 000 / -1 000 ppm
No-spreading	+0 / -0 ppm			+0 / -0 ppm
Down-spreading	+0 / -2 300 ppm			+0 / -1 000 ppm
SATA down-spreading [b]	+0 / -5 000 ppm			N/A

[a] This is in addition to the physical link rate accuracy and tolerance defined in table 33 (see 5.8.4.3) and table 51 (see 5.8.5.3).
[b] This is only used as a receiver parameter.

A phy may transmit with a different SSC modulation type than it receives (e.g., a phy may transmit with center-spreading while it receives with down-spreading).

If the SSC modulation type is not no-spreading, then the phy shall transmit within the specified maximum SSC frequency deviation with an SSC modulation frequency that is a minimum of 30 kHz and a maximum of 33 kHz.

The SSC modulation profile (e.g., triangular) is vendor specific, but should provide the maximum amount of EMI reduction. For center-spreading, the average amount of up-spreading (i.e., > 0 ppm) in the SSC modulation profile shall be the same as the average amount of down-spreading (i.e., < 0 ppm). The amount of asymmetry in the SSC modulation profile shall be less than 288 ppm.

NOTE 2 - 288 ppm is the rate of deletable primitives (see SPL-3) that are left over after accounting for the physical link rate accuracy. It is calculated as the deletable primitive rate defined in the SAS standard of 1 / 2 048 (i.e., 488 ppm) minus the width between the extremes of the physical link rate accuracy of +100 ppm to -100 ppm (i.e., 200 ppm).

SSC induced jitter is included in TJ at the transmitter output.

The slope of the frequency deviation should not exceed 850 ppm/µs when computed over any 0.27 µs ± 0.01 µs interval of the SSC modulation profile, after filtering of the transmitter device jitter output by a second order Butterworth low pass filter with a cutoff frequency of 3.7 MHz ± 0.2 MHz.

The slope is computed from the difference equation:

slope = (f(t) - f(t - 0.27 µs)) / 0.27 µs

where:

f(t) is the SSC frequency deviation expressed in ppm.

A ± 2 300 ppm triangular SSC modulation profile has a slope of approximately 310 ppm/µs and meets the informative slope specification. Other SSC modulation profiles (e.g., exponential) may not meet the slope requirement. A modulation profile that has a slope of ± 850 ppm/µs over 0.27 µs creates a residual jitter of approximately 16.7 ps (i.e., 0.10 UI at 6 Gbit/s) after filtering by the JTF. This consumes the total BUJ budget of the transmitter device, which does not allow the transmitter device to contribute any other type of BUJ.

Activation or deactivation of SSC on a physical link that is not OOB idle or negotiation idle (see SPL-3) shall be done without violating TJ at the transmitter device output after application of the JTF.

5.8.6.2 Transmitter SSC modulation

A SAS phy transmits with the SSC modulation types defined in table 69.

Table 69 – SAS phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Mandatory	**Optional**
While attached to a phy that does not support SSC	No-spreading	
While attached to a phy that supports SSC	No-spreading	Down-spreading

[a] SAS phys compliant with SAS-1.1 only transmitted with an SSC modulation type of no-spreading.

An expander phy transmits with the SSC modulation types defined in table 70.

Table 70 – Expander phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Mandatory	**Optional**
While attached to a SAS phy or expander phy that does not support SSC	No-spreading	
While attached to a SAS phy or expander phy that supports SSC	No-spreading	Center-spreading
While attached to a SATA phy	No-spreading	Down-spreading

[a] Expander phys compliant with SAS-1.1 only transmitted with an SSC modulation type of no-spreading.

A SAS device (see SPL-3) or expander device (see SPL-3) should provide independent control of SSC on each transmitter device. However, a SAS device or expander device may implement a common SSC transmit clock in which multiple transmitter devices do not have independent controls to enable and disable SSC. In such implementations, SSC may be disabled on a transmitter device that is already transmitting with SSC enabled if another transmitter device sharing the same common SSC transmit clock is required to perform SNW-1, SNW-2, SNW-3, or Final-SNW (see SPL-3) or SAS speed negotiation (see SPL-3).

If any transmitter device sharing a common SSC transmit clock enters a non-SSC transmission state (e.g., SNW-1, SNW-2, Final-SNW, Train_Tx-SNW, or Train_Rx-SNW with SSC disabled (see SPL-3)), then any transmitter device sharing that common SSC transmit clock may disable SSC. These transmitter devices are compliant with the SSC requirements even if the transmitter device has negotiated SSC enabled but its transmit clock has SSC disabled, provided that the transmitted signal does not exceed the maximum SSC frequency deviation limits specified in table 68.

The disabling and enabling of SSC may occur at any time (see 5.8.6.1) except during SNW-1, SNW-2, and Final-SNW (see SPL-3).

5.8.6.3 Receiver SSC modulation tolerance

SAS phys and expander phys support (i.e., tolerate) receiving with SSC modulation types defined in table 71.

Table 71 – Receiver SSC modulation types tolerance

Type of phys	SSC modulation type(s) [a] [b]	
	Mandatory	**Optional** [c]
Phys that support being attached to SATA phys	No-spreading and SATA down-spreading	Center-spreading and down-spreading
Phys that do not support being attached to SATA phys	No-spreading	Center-spreading and down-spreading

[a] This is in addition to the physical link rate accuracy tolerance defined in table 51 (see 5.8.5.3).
[b] Phys compliant with SAS-1.1 that do not support being attached to SATA devices were only required to tolerate an SSC modulation type of no-spreading. Phys compliant with SAS-1.1 that support being attached to SATA devices were only required to tolerate SSC modulation types of no-spreading and SATA down-spreading.
[c] If either the SSC modulation type of center-spreading or down-spreading is supported, then both shall be supported.

5.8.6.4 Expander device center-spreading tolerance buffer

Expander devices supporting the SSC modulation type of center-spreading shall support a center-spreading tolerance buffer for each connection with the buffer size defined in table 72. The expander device uses this buffer to hold any dwords that it receives during the up-spreading portions of the SSC modulation period that expander device is unable to forward as a result of:

a) the ECR (see SPL-3) and/or the transmitting expander phy is slower than the receiving expander phy; and
b) the dword stream does not include enough deletable primitives (see SPL-3).

The expander device unloads the center-spreading tolerance buffer during the down-spreading portions of the SSC modulation period when the receiving expander phy is slower than the ECR and the transmitting expander phy.

Table 72 – Expander device center-spreading tolerance buffer

Physical link rate	Minimum buffer size
12 Gbit/s	14 dwords
6 Gbit/s	14 dwords
3 Gbit/s	8 dwords
1.5 Gbit/s	4 dwords

NOTE 3 - The minimum buffer size is based on the number of dwords that may be transmitted during half of the longest allowed SSC modulation period (i.e., half of the period indicated by 30 kHz) at the maximum physical link rate (i.e., +2 400 ppm for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s or +1 100 ppm for 12 Gbit/s) minus the number that may be transmitted at the minimum physical link rate (i.e., -2 400 ppm for 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s or -1 100 ppm for 12 Gbit/s). This accounts for forwarding dwords in a connection (see SPL-3) that originated from a phy compliant with SAS-1.1 (i.e., a phy with an SSC modulation type of no-spreading and inserting deletable primitives at a rate supporting only the frequency accuracy).

Figure 150 shows an example of center-spreading tolerance buffer usage.

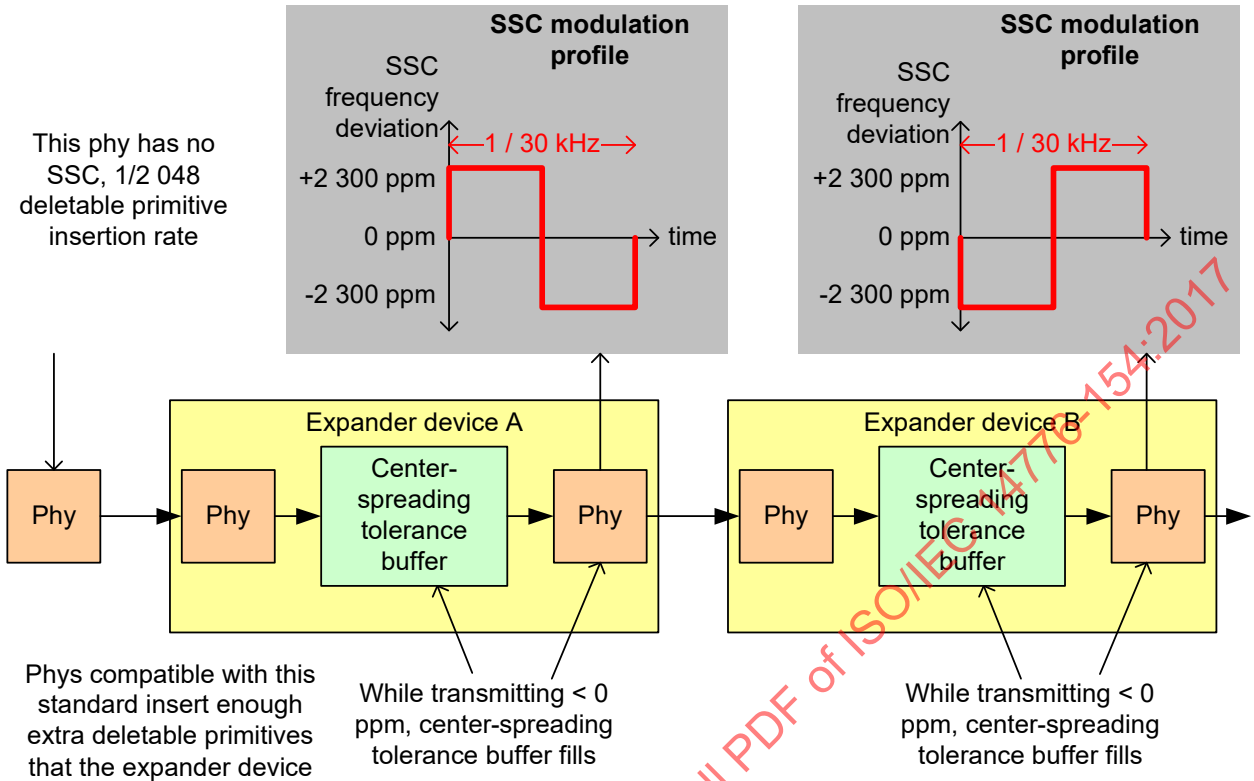


Figure 150 – Center-spreading tolerance buffer

5.8.7 Non-tracking clock architecture

Transceivers shall be designed with a non-tracking clock architecture (i.e., the receive clock derived from the bit stream received by the receiver device shall not be used as the transmit clock by the transmitter device).

Receiver devices that support SATA shall tolerate clock tracking by the SATA device. Receiver devices that do not support SATA are not required to tolerate clock tracking by the SATA device.

5.9 READY LED signal electrical characteristics

A SAS target device uses the READY LED signal to activate an externally visible LED that indicates the state of readiness and activity of the SAS target device.

All SAS target devices (see SPL-3) using the SAS Drive plug connector (see 5.4.3.4.1.1) or SAS MultiLink Drive plug connector (see 5.4.3.4.1.5) shall support the READY LED signal.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain transmitter circuit. The LED and the current limiting circuitry shall be external to the SAS target device.

Table 73 describes the output characteristics of the READY LED signal.

Table 73 – Output characteristics of the READY LED signal

State	Test condition	Requirement
Negated (LED off)	$0 V \leq V_{OH} \leq 3.6 V$	$-100 \mu A < I_{OH} < 100 \mu A$
Asserted (LED on)	$I_{OL} = 15 mA$	$0 \leq V_{OL} \leq 0.225 V$

The READY LED signal behavior is defined in SPL-3.

NOTE 4 - SATA devices use the pin used by the READY LED signal (i.e., P11) for activity indication and disable staggered spin-up (see SATA). The output characteristics differ from those in table 73.

5.10 POWER DISABLE signal electrical characteristics

The POWER DISABLE signal, if implemented, may be used to disable power to the SAS target device circuitry.

If the POWER DISABLE signal is supported by a SAS target device with the SAS Drive plug connector (see 5.4.3.4.1.1) or SAS MultiLink Drive plug connector (see 5.4.3.4.1.5), then the SAS target device shall:

a) indicate that the POWER DISABLE signal is supported on the Protocol Specific Port Information VPD page and the IDENTFY address frame (see SPL-3);
b) allow power to be applied to the SAS target device circuitry if the POWER DISABLE signal is not connected on the SAS Drive backplane receptacle (see 5.4.3.4.1.3), SAS Drive cable receptacle (see 5.4.3.4.1.2), SAS MultiLink Drive backplane receptacle (see 5.4.3.4.1.7), or SAS MultiLink Drive cable receptacle (see 5.4.3.4.1.6);
c) allow power to be applied to the SAS target device circuitry if the POWER DISABLE signal is negated as defined in table 74;
d) disable power applied to the SAS target device circuitry if:
   1) the minimum negated hold time in table 74 is met; and
   2) the POWER DISABLE signal is asserted as defined in table 74;
e) perform the actions defined for power on (see SPL-3) if:
   1) the minimum negated hold time in table 74 is met;
   2) the POWER DISABLE signal is asserted as defined in table 74; and
   3) the POWER DISABLE signal transitions from asserted to negated;
   and
f) not respond to a change of the POWER DISABLE signal from negated to asserted or asserted to negated until the POWER DISABLE signal is held at the asserted or negated level for a minimum of 1 µs.

Table 74 describes the characteristics of the POWER DISABLE signal applied to the SAS target device.

Table 74 – Characteristics of the POWER DISABLE signal applied to the SAS target device

Characteristic	Units	Minimum	Typical	Maximum
Absolute maximum input voltage range	V	-0.5		3.6
Negated voltage (power enabled) [a] [b]	V	-0.5		0.7
Asserted voltage (power disabled) [c]	V	2.1		3.6
Driver sink/source current capability [b] [c]	µA	100		
POWER DISABLE asserted hold time [d] [e]	s	5.0		
POWER DISABLE negated hold time [d] [e]	s	30.0		

[a] The SAS target device shall allow power to be applied to the SAS target device circuitry if P3 is not connected on the SAS Drive backplane receptacle (see 5.4.3.4.1.3), SAS Drive cable receptacle (see 5.4.3.4.1.2), SAS MultiLink Drive backplane receptacle (see 5.4.3.4.1.7), or SAS MultiLink Drive cable receptacle (see 5.4.3.4.1.6).

[b] The POWER DISABLE signal should be actively negated. If the POWER DISABLE signal is not actively negated (e.g., open), then the specified values for POWER DISABLE signal negated voltage and driver sink current capability applied to the SAS target device do not apply.

[c] The POWER DISABLE signal shall be actively asserted.

[d] The hold time is the length of time the POWER DISABLE signal is asserted or negated. The length of time after the POWER DISABLE signal is asserted or negated until the disabling or allowing of power application to the SAS target device circuitry is vendor specific.

[e] The POWER DISABLE signal should not transition from negated to asserted or asserted to negated for the negated hold time:

a) after power is applied to the SAS Drive backplane receptacle (see 5.4.3.4.1.3), SAS Drive cable receptacle (see 5.4.3.4.1.2), SAS MultiLink Drive backplane receptacle (see 5.4.3.4.1.7), or SAS MultiLink Drive cable receptacle (see 5.4.3.4.1.6); or

b) after the detection of a hot-plug event.

5.11 Out of band (OOB) signals

5.11.1 OOB signals overview

If D.C. mode is enabled, then OOB signals are low-speed signal patterns that do not appear in normal data streams. If optical mode is enabled, then OOB signals consist of a defined series of dwords. OOB signals consist of defined amounts of idle time followed by defined amounts of burst time. During the idle time, the physical link carries OOB idle. During the burst time, the physical link carries dwords. The signals are differentiated by the length of idle time between the burst times. OOB signals are not decoded unless dword synchronization has been lost (see SPL-3). Once high-speed data transfers are underway, the data pattern amplitude may fall to levels that are falsely detected as OOB signals. A phy shall either have D.C. mode enabled or optical mode enabled. The method to enable D.C. mode or optical mode is outside the scope of this Document.

SATA defines two OOB signals (i.e., COMINIT/COMRESET and COMWAKE). COMINIT and COMRESET are used in this document interchangeably. Phys compliant with this document identify themselves with an additional SAS specific OOB signal called COMSAS.

Table 75 defines the timing specifications for OOB signals.

Table 75 – OOB signal timing specifications

Parameter	Minimum	Nominal	Maximum	Comments
OOB Interval (OOBI) [a]	665.0$\overline{6}$ ps [b]	666.$\overline{6}$ ps [c]	668.2$\overline{6}$ ps [d]	The time basis for burst times and idle times used to create OOB signals.
COMSAS detect timeout	13.686 µs [e]			The minimum time a receiver device shall allow to detect COMSAS after transmitting COMSAS.

[a] OOBI is different than UI(OOB) defined in SATA (e.g., SAS has tighter physical link rate accuracy and different SSC frequency deviation). OOBI is based on:
  A) 1.5 Gbit/s UI (see table 31 in 5.8.1);
  B) physical link rate accuracy (see table 33 in 5.8.4.3); and
  C) center-spreading SSC (see table 68 in 5.8.6.1).

[b] 665.0$\overline{6}$ ps equals 666.$\overline{6}$ ps × (1 - 0.002 4).

[c] 666.$\overline{6}$ ps equals 2 000 ps / 3.

[d] 668.2$\overline{6}$ ps equals 666.$\overline{6}$ ps × 1.002 4.

[e] 13.686 µs is 512 × 40 × Maximum OOBI.

To interoperate with interconnects compliant with SAS-1.1, phys should create OOB burst times and idle times based on the UI for 1.5 Gbit/s without SSC modulation.

NOTE 5 - SAS-1.1 defined OOBI based on the nominal UI for 1.5 Gbit/s (see table 31 in 5.8.1) with physical link rate accuracy (see table 33 in 5.8.4.3) but not with SSC modulation (see table 68 in 5.8.6.1). Interconnects compliant with SAS-1.1 may have assumed phys had that characteristic.

5.11.2 Transmitting OOB signals

Table 76 describes the OOB signal transmitter requirements for the burst time, idle time, negation times, and signal times that are used to form each OOB signal.

Table 76 – OOB signal transmitter device requirements

Signal	Burst time	Idle time	Negation time	Signal time [a]
COMWAKE	160 OOBI [b]	160 OOBI [b]	280 OOBI [c]	2 200 OOBI [g]
COMINIT/COMRESET	160 OOBI [b]	480 OOBI [d]	800 OOBI [e]	4 640 OOBI [i]
COMSAS	160 OOBI [b]	1 440 OOBI [f]	2 400 OOBI [h]	12 000 OOBI [j]

[a] A signal time is six burst times plus six idle times plus one negation time.
[b] 160 OOBI is nominally 106.$\overline{6}$ ns (see table 75 in 5.11.1).
[c] 280 OOBI is nominally 186.$\overline{6}$ ns.
[d] 480 OOBI is nominally 320 ns.
[e] 800 OOBI is nominally 533.$\overline{3}$ ns.
[f] 1 440 OOBI is nominally 960 ns.
[g] 2 200 OOBI (e.g., COMWAKE) is nominally 1 466.$\overline{6}$ ns.
[h] 2 400 OOBI is nominally 1 600 ns.
[i] 4 640 OOBI (e.g., COMINIT/COMRESET) is nominally 3 093.$\overline{3}$ ns.
[j] 12 000 OOBI (e.g., COMSAS) is nominally 8 000 ns.

If D.C. mode is enabled, then an OOB idle consists of the transmission of D.C. idle.

If optical mode is enabled, then an OOB idle consists of repetitions of the following steps:

1) transmission of six OOB_IDLE primitives with either starting disparity at 3 Gbit/s; and
2) transmission of up to 512 data dwords (e.g., two data dwords for COMWAKE idle time, 18 data dwords for COMINIT/COMRESET idle time, and 66 data dwords for COMSAS idle time) set to 0000_0000h that are 8b10b encoded, scrambled, and transmitted at 3 Gbit/s.

An OOB burst consists of:

a) if D.C. mode is enabled, then transmission of a repeating 0011b pattern or 1100b pattern (e.g., D24.3) or ALIGN (0) primitives with either starting disparity. The OOB burst should consist of a repeating 0011b pattern or 1100b pattern (e.g., D24.3) at 1.5 Gbit/s; or
b) if optical mode is enabled, then transmission of ALIGN (3) primitives with either starting disparity at 3 Gbit/s.

To transmit an OOB signal, the transmitter device shall:

1) transmit OOB idle for an idle time;
2) transmit an OOB burst for a burst time; and
3) repeat steps 1) and 2) five additional times.

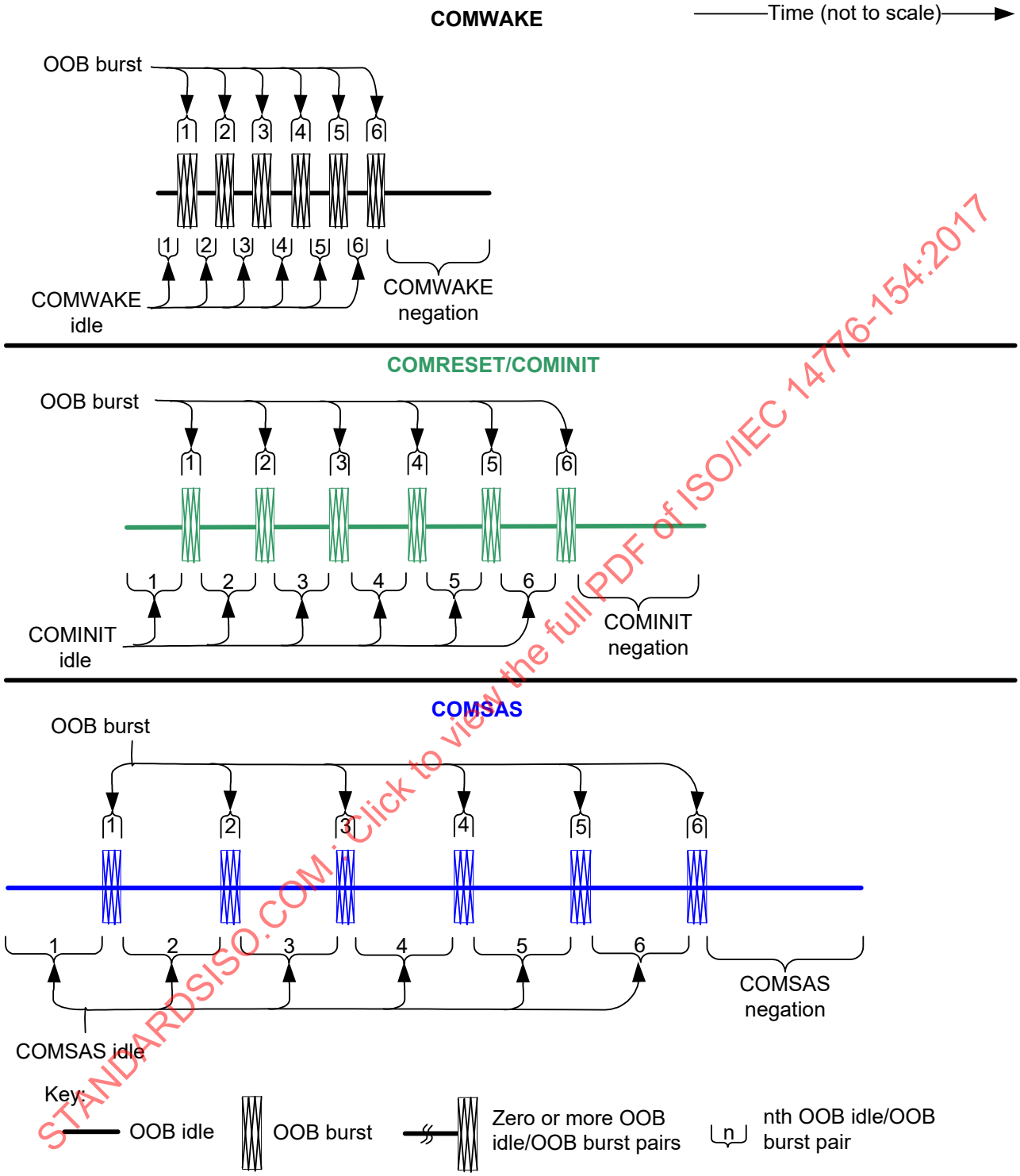
The transmitter device shall then transmit OOB idle for an OOB signal negation time.

The transmitter device shall use signal output levels during burst time and idle time as described in 5.8.4.8.

If D.C. mode is enabled, then the repeating 0011b pattern or 1100b pattern (e.g., D24.3) or ALIGN (0) primitives (see SPL-3) used in OOB signals shall be transmitted and the OOB burst is only required to generate an envelope for the detection circuitry, as required for any signaling that may be A.C. coupled. A burst of a repeating 0011b pattern or 1100b pattern (e.g., D24.3) at 1.5 Gbit/s is equivalent to a square wave pattern that has a one for two OOBI and a zero for two OOBI. A transmitter may use this square wave pattern for the OOB burst. The start of the pattern may be one or zero. The signal rise and fall times:

a) shall be greater than (i.e., slower) or equal to the minimum (i.e., fastest) rise and fall times allowed by the fastest supported physical link rate of the transmitter device (see table 35 in 5.8.4.4); and
b) shall be less than (i.e., faster) or equal to the maximum (i.e., slowest) rise and fall times allowed at 1.5 Gbit/s.

Figure 151 describes OOB signal transmission.



Note: OOB idle is shown here as a neutral signal for visual clarity only.

Figure 151 – OOB signal transmission

5.11.3 Receiving OOB signals

Table 77 describes the OOB signal receiver device requirements for detecting burst times, assuming T_{burst} is the length of the detected burst time. The burst time is not used to distinguish between signals.

Table 77 – OOB signal receiver device burst time detection requirements

Signal [a]	may detect	shall detect
COMWAKE	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 ns < $T_{burst} \leq 112$ ns
COMINIT/COMRESET	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 ns < $T_{burst} \leq 112$ ns
COMSAS	$T_{burst} \leq 100$ ns or $T_{burst} > 112$ ns	100 ns < $T_{burst} \leq 112$ ns

[a] Each burst time is transmitted as 160 OOBI, which is nominally 106.$\overline{6}$ ns (see table 76 in 5.11.2).

Table 78 describes the OOB signal receiver device requirements for detecting idle times, assuming T_{idle} is the length of the detected idle time.

Table 78 – OOB signal receiver device idle time detection requirements

Signal	may detect	shall detect	shall not detect
COMWAKE [a]	35 ns ≤ T_{idle} < 175 ns	101.3 ns ≤ $T_{idle} \leq 112$ ns	T_{idle}< 35 ns or $T_{idle} \geq 175$ ns
COMINIT/ COMRESET [b]	175 ns ≤ T_{idle} < 525 ns	304 ns ≤ $T_{idle} \leq 336$ ns	T_{idle} < 175 ns or $T_{idle} \geq 525$ ns
COMSAS [c]	525 ns ≤ T_{idle} < 1 575 ns	911.7 ns ≤ $T_{idle} \leq 1\,008$ ns	T_{idle} < 525 ns or $T_{idle} \geq 1\,575$ ns

[a] COMWAKE idle time is transmitted as 160 OOBI, which is nominally 106.$\overline{6}$ ns (see table 76 in 5.11.2).
[b] COMINIT/COMRESET idle time is transmitted as 480 OOBI, which is nominally 320 ns.
[c] COMSAS idle time is transmitted as 1 440 OOBI, which is nominally 960 ns.

Table 79 describes the OOB signal receiver device requirements for detecting negation times, assuming T_{idle} is the length of the detected idle time.

Table 79 – OOB signal receiver device negation time detection requirements

Signal	shall detect
COMWAKE [a]	T_{idle} > 175 ns
COMINIT/COMRESET [b]	T_{idle} > 525 ns
COMSAS [c]	T_{idle} > 1 575 ns

[a] COMWAKE negation time is transmitted as 280 OOBI, which is nominally 186.$\overline{6}$ ns (see table 76 in 5.11.2).
[b] COMINIT/COMRESET negation time is transmitted as 800 OOBI, which is nominally 533.$\overline{3}$ ns.
[c] COMSAS negation time, which is transmitted as 2 400 OOBI, which is nominally 1 600 ns.

If D.C. mode is enabled, then a SAS receiver device shall detect OOB bursts formed from any of the following:

a) D24.3 characters (see SPL-3) at 1.5 Gbit/s;
b) ALIGN (0) primitives (see SPL-3) at 1.5 Gbit/s; or
c) ALIGN (0) primitives at 3 Gbit/s.

NOTE 6 - Detection of ALIGN (0) primitives at 3 Gbit/s provides interoperability with transmitter devices compliant with SAS-1.1.

If D.C. mode is enabled, then a SAS receiver device shall not qualify the OOB burst based on the characters received.

If optical mode is enabled, then a SAS receiver device shall detect OOB bursts formed from ALIGN (3) primitives at 3 Gbit/s.

5.11.4 Transmitting the SATA port selection signal

The SATA port selection signal shown in figure 152 causes the attached SATA port selector (see SPL-3) to select the attached phy (i.e., one of the SATA port selector's host phys) as the active phy (see SATA).

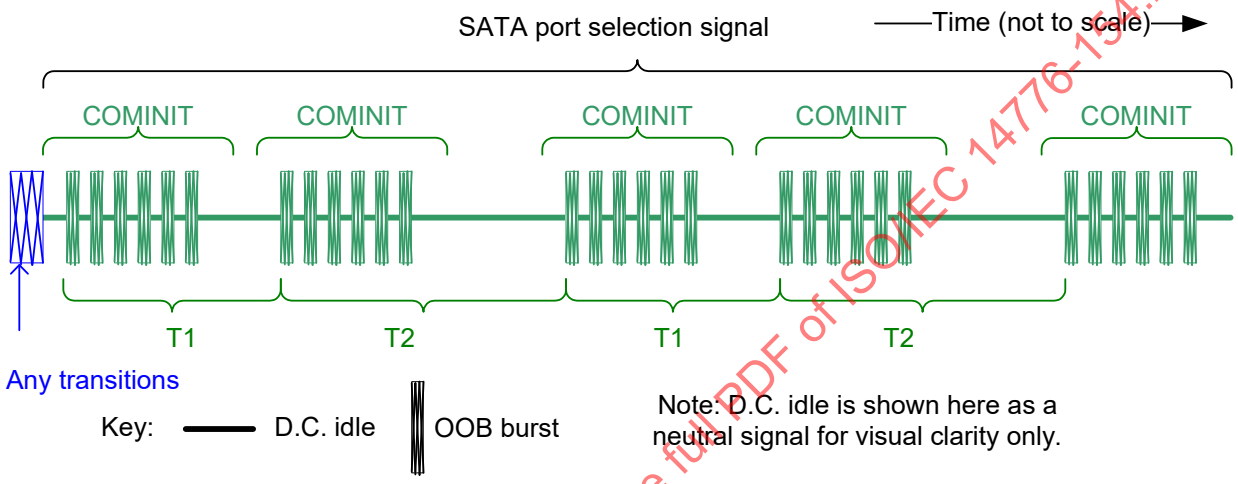


Figure 152 – SATA port selection signal

The SATA port selection signal shall be composed of five COMINIT signals, each starting a specified time interval, T1 or T2, as shown in figure 152, after the start of the OOB burst portion of the previous COMINIT signal. The values of T1 and T2 shall be as shown in table 80.

Table 80 – SATA port selection signal transmitter device requirements

Parameter	Time
T1	3 x 10^6 OOBI [a]
T2	12 x 10^6 OOBI [b]

[a] 3 x 10^6 OOBI is nominally 2 ms (see table 75 in 5.11.1).
[b] 12 x 10^6 OOBI is nominally 8 ms.

See SPL-3 for information on usage of the SATA port selection signal.

Annex A
(normative)

Jitter tolerance pattern (JTPAT)

The jitter tolerance pattern (JTPAT) consists of:

1) a long run of low transition density pattern;
2) a long run of high transition density pattern; and
3) another short run of low transition density pattern.

The transitions between the pattern segments stress the receiver. The JTPAT is designed to contain the phase shift in both polarities, from zero to one and from one to zero. The critical pattern sections with the phase shifts are underlined in table A.1 and table A.2.

Table A.1 shows the JTPAT when there is positive running disparity (RD+) (see SPL-3) at the beginning of the pattern. The 8b and 10b values of each character (see SPL-3) are shown.

Table A.1 – JTPAT for RD+

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD+
		10 0001 1100b	01 1110 0011b	10 0001 1100b	01 1110 0011b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D20.3 (74h)	RD-
		10 0001 1100b	01 1110 0011b	10 0001 1100b	00 1011 1100b	
	The above dword containing phase shift 111 0000 1011b is sent one time					
42	RD-	D30.3 (7Eh)	D11.5 (ABh)	D21.5 (B5h)	D21.5 (B5h)	RD+
		01 1110 0011b	11 0100 1010b	10 1010 1010b	10 1010 1010b	
	The above dword containing phase shift 000 1111 0100b is sent one time					
43 to 54	RD+	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	RD+
		10 1010 1010b	10 1010 1010b	10 1010 1010b	10 1010 1010b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD+	D21.5 (B5h)	D30.2 (5Eh)	D10.2 (4Ah)	D30.3 (7Eh)	RD+
		10 1010 1010b	10 0001 0101b	01 0101 0101b	01 1110 0011b	
	The above dword containing phase shift 0101 0000b and 1010 1111b is sent one time					

If the same 8b characters specified in table A.1 are used when there is negative running disparity (RD-) at the beginning of the pattern, then the resulting 10b pattern is different than the positive running disparity for the same 8b character and does not provide the critical phase shifts. To achieve the same phase shift effects with RD-, a different 8b pattern is required. Table A.2 shows the JTPAT when there is negative running disparity (RD-) at the beginning of the pattern. The 8b and 10b values of each character are shown.

Table A.2 – JTPAT for RD-

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD-
		01 1110 0011b	10 0001 1100b	01 1110 0011b	10 0001 1100b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D11.3 (6Bh)	RD+
		01 1110 0011b	10 0001 1100b	01 1110 0011b	11 0100 0011b	
	The above dword containing phase shift 000 1111 0100b is sent one time					
42	RD+	D30.3 (7Eh)	D20.2 (54h)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		10 0001 1100b	00 1011 0101b	01 0101 0101b	01 0101 0101b	
	The above dword containing phase shift 111 0000 1011b is sent one time					
43 to 54	RD-	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		01 0101 0101b	01 0101 0101b	01 0101 0101b	01 0101 0101b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD-	D10.2 (4Ah)	D30.5 (BEh)	D21.5 (B5h)	D30.3 (7Eh)	RD-
		01 0101 0101b	01 1110 1010b	10 1010 1010b	10 0001 1100b	
	The above dword containing phase shift 10101111b and 01010000b is sent one time					

The compliant jitter tolerance pattern (CJTPAT) is the JTPAT for RD+ (see table A.1) and RD- (see table A.2) included as the payload in an SSP DATA frame or an SMP frame. A phy or test equipment transmitting CJTPAT outside connections may transmit it with fixed content. See SPL-3.

Annex B
(normative)

SASWDP

B.1 SASWDP introduction

SASWDP is a MATLAB program used for transmitter device compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.8.4.6.1) and for receiver device compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.8.5.7.6). Equivalent simulation programs may be used if they lead to the same results.

B.2 SASWDP.m

```
% MATLAB (R) script to compute TWDP, WDP, and NC-DDJ %%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Version: 1.9
% Date: September 11, 2009
%
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% SELLING, OFFERING FOR SALE OR IMPORTING OF THE SOFTWARE OR PRODUCTS MAKING
% USE OF THE SOFTWARE.
%
% Based on original TWDP methodology described in IEEE Std 802.3aq(TM)-2006
%
% Reference: N. L. Swenson, P. Voois, T. Lindsay, and S. Zeng, "Standards
% compliance testing of optical transmitters using a software-based equalizing
% reference receiver", paper NWC3, Optical Fiber Communication Conference and
% Exposition and The National Fiber Optic Engineers Conference on CD-ROM
% (Optical Society of America, Washington, DC), Feb. 2007
%
% Syntax:
% [xWDP, ncDDJ, MeasuredxMA, yout] = SASWDP( WaveformFile, TxDataFile, ...
%     SymbolRate, OverSampleRate, Usage, ShowEye )
```

```
%
% Inputs:
% -------
% WaveformFile: The waveform consists of exactly N samples per unit interval
%  T, where N is the oversampling rate. The waveform must be circularly
%  shifted to align with the transmit data sequence. The file format is ASCII
%  with a single column of chronological numerical samples, in signal level,
%  with no headers or footers. Enter as a string.
%  This may also be entered as a row or column vector of values.
% TxDataFile: The transmit data sequence should be one of standard test
%  patterns The file format is ASCII with a single column of chronological
%  ones and zeros with no headers or footers. Enter as a string.
%  This may also be entered as a row or column vector of values.
% SymbolRate: The reciprocal of the unit interval in GBd. Enter as a double.
% OverSampleRate: Number of samples, N, per unit interval. Enter as a double.
% Usage: Defines the parameter set specific to the requirement to be verified.
%  In this version, the only permissible values are 'SAS2_TWDP' and
%  'SAS2_LDP'. Enter as a string.
% ShowEye: Controls the graphical display of the slicer input eye. Any value
% greater than zero enables the display (and is the figure number for the
% first figure generated). Enter as a double.
%
% Outputs:
% --------
% xWDP: Waveform Dispersion Penalty (dBe)
% ncDDJ: non-compensable DDJ. This is computed from twice the worst-case eye
%        closure and should be improved.
% MeasuredxMA: Approximative magnitude of the waveform (from 40-60% amplitude
%              of a 5-zeros/5-ones pattern)
% yout is the result of the convolution with the channel response
%      (for debugging purposes).
%
% This script requires the file 'sas2_stressor_6g0_16x.txt' in
% the same directory

%% Function: SASWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [xWDP,ncDDJ,MeasuredxMA,yout]=...
    SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,ShowEye)
%% Program constants
SymbolPeriod=1/SymbolRate;
Q0=7.94; % BER = 10^(-15)
%% Load input waveform and data sequence, generate filter and other matrices
% Accept vectors
if ischar(WaveformFile)
  yout0=load(WaveformFile);
else
  yout0=WaveformFile(:);
end
if ischar(TxDataFile)
  XmitData=load(TxDataFile);
else
  % Convert to double otherwise toeplitz may think it is logical...
  XmitData=double(TxDataFile(:));
end
%yout0=load(WaveformFile);
%XmitData=load(TxDataFile);

PtrnLength=length(XmitData);
TotLen=PtrnLength*OverSampleRate;
Fgrid=(-TotLen/2:TotLen/2-1).'/(PtrnLength*SymbolPeriod);

% MG as a first thing, convolve with channel. MeasuredxMA is unused in GetParams
[EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
```

```
    GetParams(Usage,Fgrid,SymbolPeriod,1);

yout0=real(ifft(fft(yout0).*fftshift(H_chan)));

%% Enforce column vectors
yout0 = yout0(:);
XmitData = XmitData(:);
%% Normalize the received OMA or VMA to 1. Estimate the xMA of the captured
%% waveform by using a linear fit to estimate a pulse response, synthesize a
%% square wave, and calculate the xMA of the synthesized square wave per IEEE
%% 802.3, clause 52.9.5.
ant=4; mem=40; % Anticipation and memory parameters for linear fit
X=zeros(ant+mem+1,PtrnLength); % Size data matrix for linear fit
Y=zeros(OverSampleRate,PtrnLength); % Size observation matrix for linear fit
for ind=1:ant+mem+1 % Wrap appropriately for linear fit
    X(ind,:)=XmitData(mod((0:PtrnLength-1)-ind+ant+1,PtrnLength)+1).';
end
X=[X;ones(1,PtrnLength)]; % The all-ones row is included to compute the bias
for ind=1:OverSampleRate
    Y(ind,:)=yout0((0:PtrnLength-1)*OverSampleRate+ind)'; % 1 bit per column
end
Qmat=Y*X'*(X*X')^(-1); % Coefficient matrix resulting from linear fit. Each
%% column (except the last) is one bit period of the pulse response. The last
%% column is the bias.
SqWvPer=10; % Even number; sets the period of the sq wave used to compute xMA
SqWv=[zeros(SqWvPer/2,1);ones(SqWvPer/2,1)]; % One period of sq wave (column)
X=zeros(ant+mem+1,SqWvPer); % Size data matrix for synthesis
for ind=1:ant+mem+1 % Wrap appropriately for synthesis
    X(ind,:)=SqWv(mod((0:SqWvPer-1)-ind+ant+1,SqWvPer)+1).';
end
X=[X;ones(1,SqWvPer)]; % Include the bias
Y=Qmat*X;Y=Y(:); % Synthesize the modulated square wave, put into one column
Y=AlignY(Y,SqWvPer,OverSampleRate);
avgpos=(0.4*SqWvPer/2*OverSampleRate:0.6*SqWvPer/2*OverSampleRate);
ZeroLevel=mean(Y(round(avgpos),:)); % Average over middle 20% of "zero" run
%% Average over middle 20% of "one" run, compute xMA
MeasuredxMA=mean(Y(round(SqWvPer/2*OverSampleRate+avgpos),:))-ZeroLevel;
%% Subtract zero level and normalize xMA
youtn=(yout0-ZeroLevel)/MeasuredxMA;
%% Get usage parameters for the application

%[MG] Removing the second call to GetParams
%[EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
%    GetParams(Usage,Fgrid,SymbolPeriod,MeasuredxMA);

ONE=ones(PtrnLength,1);
%% Set search range for equalizer delay, specified in symbol periods. Lower end
%% of range is minimum channel delay less 5 for a guardband. Upper end of range
%% accounts for the FFE. Round up and add 5 to guardband for the channel and
%% antialiasing filter.
EqDelMin=-5;
EqDelMax=ceil(EqNf/2)+5;
%% Compute the minimum slicer MSE and corresponding xWDP and ncDDJ
X=toeplitz(XmitData,[XmitData(1);XmitData(end:-1:end+1-EqNb)]);
Xtil=toeplitz(XmitData(mod((0:PtrnLength-1)-EqDelMin,PtrnLength )+1),...
    XmitData(mod(-EqDelMin:-1:-(EqDelMax+EqNb),PtrnLength)+1));
Rxx=X'*X; % Used in MSE calculation
for ii=1:size(H_chan,2) % index for stressor
    %% Compute the noise autocorrelation sequence at the output of the front-end
    %% antialiasing filter and rate-2/T sampler.
    N0=SymbolPeriod/2/(Q0*10^(PAlloc(ii)/dBscale))^2;
    Snn=N0/2*fftshift(abs(H_r).^2)*1/SymbolPeriod*OverSampleRate;
    Rnn=real(ifft(Snn));
```

```
    Corr=Rnn(1:OverSampleRate/2:end);
    C=toeplitz(Corr(1:EqNf));
    % [MG] Removing convolution at this point
    yout=youtn;
%    yout=real(ifft(fft(youtn).*fftshift(H_chan(:,ii))));
    if AAfilter > 0
        %% Process signal through front-end antialiasing filter
        yout=real(ifft(fft(yout).*fftshift(H_r)));
    end
    %% Compute the sampling function and sample the processed waveform
    [yk,tk,index1]=CDRSample(yout,OverSampleRate,PtrnLength,UseLAMP);
    %% Compute MMSE-DFE %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %% The MMSE-DFE filter coefficients computed below minimize mean-squared
    %% error at the slicer input. The derivation follows from the fact that the
    %% slicer input over the period of the data sequence can be expressed as
    %% Z = (R+N)*W - X*[0 B]', where R and N are Toeplitz matrices constructed
    %% from the signal and noise components, respectively, at the sampled
    %% output of the antialiasing filter, W is the feedforward filter, X is a
    %% Toeplitz matrix constructed from the input data sequence, and B is the
    %% feedback filter. The computed W and B minimize the mean square error
    %% between the input to the slicer and the transmitted sequence due to
    %% residual ISI and Gaussian noise. Minimize MSE over FFE delay and
    %% determine BER.
    Rout=toeplitz(yk,[yk(1);yk(end:-1:end-EqNf+2)]);
    R=Rout(index1:2:end,:);
    RINV=inv([R'*R+PtrnLength*C,R'*ONE;ONE'*R,PtrnLength]);
    R=[R,ONE]; % Add all-ones column to compute optimal offset
    Rxr=Xtil'*R; Px_r=Rxr*RINV*Rxr';
    %% Minimize MSE over equalizer delay
    MseOpt=Inf;
    for kk=1:EqDelMax-EqDelMin+1
        SubRange=(kk:kk+EqNb);
        SubRange=mod(SubRange-1,PtrnLength)+1;
        P=Rxx-Px_r(SubRange,SubRange);
        P00=P(1,1); P01=P(1,2:end); P11=P(2:end,2:end);
        Mse=P00-P01*inv(P11)*P01';
        if (Mse < MseOpt)
            MseOpt=Mse;
            B=-inv(P11)*P01'; % Feedback filter
            XSel=Xtil(:,SubRange);
            W=RINV*R'*XSel*[1;B]; % Feedforward filter
            Z=R*W-XSel*[0;B]; % Input to slicer
            %% Compute BER using semi-analytic method
            MseGaussian=W(1:end-1)'*C*W(1:end-1);
            Ber=mean(0.5*erfc((abs(Z-0.5)/sqrt(MseGaussian))/sqrt(2)));
        end
    end
    %% Compute equivalent SNR %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %% This function computes the inverse of the Gaussian error probability
    %% function. The built-in function erfcinv() is not sensitive enough for
    %% low probability of error cases.
    if Ber>10^(-12),Q=sqrt(2)*erfinv(1-2*Ber);
    elseif Ber>10^(-323),Q=2.1143*(-1.0658-log10(Ber)).^0.5024;
    else Q=min(abs(Z-0.5))/sqrt(MseGaussian);
    end
    %% Compute penalty and ncDDJ %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    RefSNR=dBscale*log10(Q0)+PAlloc(ii);
    xWDP(ii)=RefSNR-dBscale*log10(Q);
    xWDP(ii)=xWDP(ii)-xMAGain(ii); % Offset xWDP by the eligible xMA gain
    ncDDJ(ii)=AnalyzeEye(yout,tk,index1,W,B,XSel,MseGaussian,...
        ShowEye,Usage,ii,MeasuredxMA,Q,Q0,xWDP(ii),dBscale);
end
%% End of SASWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%% Subfunction: GetParams %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
    GetParams(Usage,Fgrid,SymbolPeriod,MeasuredxMA)
switch upper(Usage)
    case 'SAS2_TWDP'
        EqNf=1;
        EqNb=3;
        %% Import stressor response from file %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        %% stressorFile : Contains the stressor impulse response(s) sampled
        %% at an interval of "stressorStep". The file format is ASCII with a
        %% column of chronological numerical samples for each stressor with
        %% no headers or footers.
        stressorFile='sas2_stressor_6g0_16x.txt';
        stressorStep=1/(16*6.0);
        %% Resample the stressor at an interval of "SymbolPeriod/OverSampleRate"
        OverSampleRate=round(length(Fgrid)*mean(diff(Fgrid))*SymbolPeriod);
        stressor0=load(stressorFile);
        stressor0Time=(0:length(stressor0)-1)*stressorStep;
        stressorTime=(0:length(Fgrid)-1)*SymbolPeriod/OverSampleRate;
        stressor=interp1(stressor0Time,stressor0.',stressorTime,'linear',0);
        stressor=stressor*SymbolPeriod/(OverSampleRate*stressorStep);
        H_chan=fftshift(fft(stressor.'),1);
        %% AAFilter disables anti-aliasing filter processing of the signal
        %% under test (noise is still shaped). This parameter is used by
        %% Fibre Channel but recommended to be set to 1 for other
        %% applications.
        AAfilter=1;
        %% Denominator coefficients for 7.5 GHz 4-port Butterworth filter
        a=[1,123.140658357,7581.81087032,273453.656327,4931335.23359];
       AABW=0.75/SymbolPeriod;  % Scale coefficients for different bandwidth
        sc=(AABW/7.5).^[0:4]; a=a.*sc;
        H_r=a(end)./polyval(a,j*2*pi*Fgrid);
        PAlloc=15.4;
        dBscale=20;
        xMAGain=0;
        UseLAMP=0;
        % UseLAMP=1;
    case 'SAS2_LDP'
        EqNf=1;
        EqNb=3;
        H_chan=1;
        %% AAFilter disables anti-aliasing filter processing of the signal
        %% under test (noise is still shaped). This parameter is used by
        %% Fibre Channel but recommended to be set to 1 for other
        %% applications.
        AAfilter=1;
        %% Denominator coefficients for 7.5 GHz 4-port Butterworth filter
        a=[1,123.140658357,7581.81087032,273453.656327,4931335.23359];
        AABW=0.75/SymbolPeriod;  % Scale coefficients for different bandwidth
        sc=(AABW/7.5).^[0:4]; a=a.*sc;
        H_r=a(end)./polyval(a,j*2*pi*Fgrid);
        PAlloc=15.4;
        dBscale=20;
        xMAGain=0;
        UseLAMP=0;
        % UseLAMP=1;
    otherwise
        error('Usage not recognized.');
end
%% End of GetParams %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: AlignY %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
function Y = AlignY(Y0,SqWvPer,OverSampleRate)
%% Aligns the mid crossing of the xMA square waveform to its ideal position.
Y=Y0-mean(Y0); % AC-couple so crossings are at 0.
%% Look only for the crossing in the middle by ignoring any within ~2 UI from
%% its beginning. Due to possible misalignment of the captured waveform, this
%% is the only crossing that is certain.
%% x=find(sign(Y(2*OverSampleRate:end-1))~=...
%%     sign(Y(2*OverSampleRate+1:end)),1)+2*OverSampleRate-1;
x=min(find(sign(Y(2*OverSampleRate:end-1))~=...
    sign(Y(2*OverSampleRate+1:end))))+2*OverSampleRate-1;
%% Find a more exact crossing point.
xinterp=interp1([Y(x),Y(x+1)],[x,x+1],0);
%% Shift to create the aligned square waveform.
SqWvLen=SqWvPer*OverSampleRate;
Y=Y0(mod((0:SqWvLen-1)-SqWvLen/2+x,SqWvLen)+1); % Coarse shift.
X=(1:length(Y))';Y=interp1(X,Y,(1:length(Y))'+xinterp-x,'spline'); % Fine shift.
%% End of AlignY %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: CDRSample %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [yk,tk,index1] = ...
    CDRSample(yout,OverSampleRate,PtrnLength,UseLAMP)
%% Derive normalized frequency grid from the input arguments
TotLen=OverSampleRate*PtrnLength;
Fgridn=(-TotLen/2:TotLen/2-1).'/PtrnLength;
%% Compute the frequency response for spectral line bandpass filter
w1=2*pi*(1-1/3000); % Define the pass band (normalized to signaling speed)
w2=2*pi*(1+1/3000);
w0=sqrt(w1*w2);
Bw=w2-w1;
% Denominator and numerator coefficients for a prototype low pass filter
ap=[1,2,1];
bp=[0,2,1];
% Apply frequency transformation to realize the desired bandpass filter
s=j*2*pi*Fgridn(find(Fgridn ~= 0));
sprime=(s.^2+w0^2)./(Bw*s);
Hp=zeros(1,TotLen);
Hp(find(Fgridn ~= 0))=polyval(bp,sprime)./polyval(ap,sprime);
%% Compute the sampling function and sample the waveform
km1=mod((0:TotLen-1)-1,TotLen)+1;
kp1=mod((0:TotLen-1)+1,TotLen)+1;
if UseLAMP > 0
    ylim=tanh(10*(yout-mean(yout)));
    yclk=real(ifft(fft(abs(ylim(kp1)-ylim(km1))).*fftshift(Hp(:))));
else
    yclk=real(ifft(fft(abs(yout(kp1)-yout(km1))).*fftshift(Hp(:))));
end
yclk=yclk(kp1)-yclk(km1);
time=(0:TotLen).'/OverSampleRate; % Wrap waveforms to ensure all edges are
yout=[yout;yout(1)];              % are detected
yclk=[yclk;yclk(1)];
yclk=yclk/(max(yclk)-min(yclk))+0.5; % Normalize clock waveform
kr=find(diff(yclk > 0.5) > 0); % Eye center index
kf=find(diff(yclk > 0.5) < 0); % Eye crossing index
k=sort([kr;kf]);
index1=double(kr(1) > kf(1))+1; % Index of the first eye center
tk=time(k)-(1/OverSampleRate)*(yclk(k)-0.5)./(yclk(k+1)-yclk(k));
yk=interp1(time,yout,tk);
%% End of CDRSample %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: AnalyzeEye %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function ncDDJ=AnalyzeEye(yout,tk,index1,W,B,XSel,MseGaussian, ...
    showEye,usage,ii,MeasuredxMA,Q,Q0,xWDP,dBscale)
%% Extract required equalizer parameters from the input arguments.
```

```
EqNf=length(W)-1; % Number of T/2-spaced feed-forward taps
EqNb=length(B); % Number of T-spaced feedback taps
xr=XSel(:, 1); % Error-free decisions
%% Define the axes of the bit error ratio map
dphi=1/100; % Phase step (unit interval)
dvee=1/200; % Eye diagram amplitude step (unit amplitude)
phiList=linspace(-0.5,0.5,round(1/dphi)+1);
veeList=linspace(-0.5,0.5,round(1/dvee)+1);
if ~(showEye > 0),veeList = 0;end
%% Compute the bit error ratio at each point in the time-amplitude grid.
PtrnLength=length(xr);
OverSampleRate=round(length(yout)/PtrnLength);
time=(0:OverSampleRate*PtrnLength).'/OverSampleRate;
yout=[yout;yout(1)];
for jj=1:length(phiList)
    phi=phiList(jj);
    yk=interp1(time,yout,mod(tk+phi,time(end)));
    Y=toeplitz(yk,[yk(1);yk(end:-1:end-EqNf+2)]);
    Y=Y(index1:2:end,:);
    Y=[Y,ones(PtrnLength,1)];
    zk=Y*W-XSel*[0; B];
    %% Compute the minimum distance from the noiseless, equalized samples
    %% to the decision threshold.
    eyeLid0(jj)=max(zk(find(xr == 0)));
    eyeLid1(jj)=min(zk(find(xr == 1)));
    %% Compute the bit error ratio as a function of offset from the nominal
    %% sampling time and decision threshold.
    dk=ones(length(veeList),1)*zk.'-veeList(:)*ones(1,PtrnLength);
    dk(:,find(xr == 0))=0.5-dk(:,find(xr == 0));
    dk(:,find(xr == 1))=dk(:,find(xr == 1))-0.5;
    berMap(:, jj)=mean(erfc(dk/sqrt(2*MseGaussian))/2,2);
end
eyeList=2*min([0.5-eyeLid0;eyeLid1-0.5]);
%% Compute the non-compensable jitter.
kDDJ=find(abs(diff(eyeList > 0)) > 0);
phiDDJ=phiList(kDDJ)-dphi*eyeList(kDDJ)./(eyeList(kDDJ+1)-eyeList(kDDJ));
if length(phiDDJ) == 0
    phiDDJ=[0,0];
end
if length(phiDDJ) == 1
    phiDDJ=sort([phiDDJ,-sign(phiDDJ)/2]);
end
ncDDJ=1-2*max(min([-phiDDJ(1),phiDDJ(2)]),0);
%% Display the bit error ratio map, if requested.
if showEye > 0
    figure(showEye-1+ii);
    clf;
    imagesc(phiList,veeList+0.5,log10(berMap));
    hold on
    plot(phiList,eyeLid0,'--','Color','white');
    plot(phiList,eyeLid1,'--','Color','white');
    hold off
    jetColors=jet;
    colormap(jet);
    caxis([round(log10(erfc(Q0/sqrt(2))/2)),0]);
    colorbar;
    set(gca,'YDir','normal');
    set(gca,'Color',jetColors(end,:));
    if dBscale == 10,units={'W','dBo'};
    else units={'V','dBe'};end
    tapStr=sprintf('\nxMA = %.3e %s',MeasuredxMA,units{1});
    tapStr=[tapStr,sprintf('\nW = [%.3f', W(1))];
    for jj=2:EqNf
```

```
        tapStr=[tapStr,sprintf(', %.3f',W(jj))];
    end
    tapStr=[tapStr, ']'];
    if EqNb > 0
        tapStr=[tapStr,sprintf('\nB = [%.3f',B(1))];
        for jj=2:EqNb
            tapStr=[tapStr,sprintf(', %.3f',B(jj))];
        end
        tapStr=[tapStr,']'];
    else
        tapStr=[tapStr,sprintf('\nB = []')];
    end
    eyeStr=sprintf('SNR = %.1f %s\n',dBscale*log10(Q),units{2});
    eyeStr=[eyeStr,sprintf('xWDP = %.1f %s\n',xWDP,units{2})];
    eyeStr=[eyeStr,sprintf('NC-DDJ = %.3f UI\n',ncDDJ)];
    titleStr=sprintf('[SASWDP] %s',usage);
    titleStr=[titleStr,sprintf('(%d): Bit error ratio map',ii)];
    text(-0.45,0.90,tapStr,'Color','white');
    text(-0.45,0.10,eyeStr,'Color','white');
    title(titleStr, 'Interpreter','none');
    ylabel('Normalized amplitude');
    xlabel('Time (UI)');
end
%% End of AnalyzeEye %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

B.3 SASWDP_testcase.m

The following MATLAB program runs SASWDP with a variety of input files.

```
% SASWDP_testcase.m
clear all,close all
format compact
x1='SCRAMBLED_0RDP10m_symbols.txt';
x2='SCRAMBLED_0RDN10m_symbols.txt';
x3='SCRAMBLED_0RDP_symbols.txt';
x4='SCRAMBLED_0RDN_symbols.txt';
y1='SCRAMBLED_0RDP10m_samples.txt';
y2='SCRAMBLED_0RDN10m_samples.txt';
y3='SCRAMBLED_0RDP_samples.txt';
y4='SCRAMBLED_0RDN_samples.txt';
if 1==0 % to check oversample rate
z=load('WaveformFile_0m-prbs10.txt')
plot(mod([1:length(z)],12),z,'.')
clf,plot(mod([1:length(z)],16),z,'.')
end
for i=1:2
eval(['WaveformFile = y',num2str(i),';'])
eval(['TxDataFile = x',num2str(i),';'])
SymbolRate = 6;
OverSampleRate = 16;
Usage = 'SAS2_LDP';
ShowEye = 1;
[WDP,ncDDJ,MeasuredxMA]=SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,Sh
    owEye)
end
for i=3:4
eval(['WaveformFile = y',num2str(i),';'])
eval(['TxDataFile = x',num2str(i),';'])
SymbolRate = 6;
OverSampleRate = 16;
Usage = 'SAS2_TWDP';
ShowEye = 1;
[WDP,ncDDJ,MeasuredxMA]=SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,Sh
```

```
    owEye)
end
```

Annex C
(informative)

StatEye

C.1 StatEye introduction

StatEye[1] is a Python program that may be used for simulating TxRx connection compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5).

C.2 analysis.py

The following Python file loads pattern measurement files, and is not used for TxRx connection compliance simulations.

```
from string import rstrip
from re import split, search

version = "071210.a"

def loadcsv(filename,startline,endline,timecol,sigcol) :
time = []
signal = []
_line = 0
flag = 0

for line in file('%s.csv'%filename) :
      if flag == 0:
            if search('^[0-9,]',line) :
                  flag = 1

      if flag == 1:
            _line += 1
            if (_line > endline) and (endline>0) :
                  break
            if _line > startline :
                  line = rstrip(line)
                  a = split(',',line)
                  _time = eval(a[timecol])
                  _signal = eval(a[sigcol])
                  time += [_time]
                  signal += [_signal]

return([time,signal])

def loadtxt(filename,startline,endline,timecol,sigcol) :
time = []
signal = []
_line = 0
flag = 0

for line in file('%s.txt'%filename) :
      if flag == 0:
            if search('^[0-9,]',line) :
```

1. This information is given for the convenience of users of this document and does not constitute an endorsement by IEC or ISO. See http://www.stateye.org for more information on StatEye. Equivalent simulation programs may be used if they lead to the same results.

```
                    flag = 1

        if flag == 1:
              _line += 1
              if (_line > endline) and (endline>0) :
                    break
              if _line > startline :
                    line = rstrip(line)
                    a = split(' ',line)
                    _time = eval(a[timecol])
                    _signal = eval(a[sigcol])
                    time += [_time]
                    signal += [_signal]

  return([time,signal])


  def polar2rect(r, w, deg=0):# radian if deg=0; degree if deg=1
      from math import cos, sin, pi
      if deg:
  w = pi * w / 180.0
      return [r * cos(w), r * sin(w)]

  def rect2polar(x, y, deg=0):# radian if deg=0; degree if deg=1
      from math import hypot, atan2, pi
      if deg:
  return hypot(x, y), 180.0 * atan2(y, x) / pi
      else:
  return [hypot(x, y), atan2(y, x)]
```

C.3 cdr.py

The following Python file extracts the clock from a pattern measurement and is not used for TxRx connection compliance simulations.

```
  from numpy import *
  from pylab import *

  # version 071210.a

  def cdr (edges,k,m,name) :

  period0 = min(diff(edges[10:2000]))

  period = [period0]

  phase = [edges[0]]
  phaseError = []
  nperiod = []
  phaseInOld = edges[0]-period[-1]

  for phaseIn in edges :
        nperiod += [ floor( (phaseIn+0.5*period[-1] - phaseInOld) /
  period[-1]) ]
        phaseInOld = phaseIn
        _phaseError = phaseIn - phase[-1] + period[-1]/2
```

```
        phaseError += [ mod( _phaseError , period[-1]) - period[-1]/2 ]
        period += [period[-1] + phaseError[-1] * k]
        phase += [phase[-1] + phaseError[-1] * m + nperiod[-1]*period[-1]]

    figure()
    subplot(3,1,1)
    hold(0)
    plot(phase/mean(period))
    hold(1)
    plot(edges/mean(period))
    grid(1)
    xlabel('time [UI]')
    ylabel('Absolute Phase[UI]')
    title(name)

    subplot(3,1,2)
    plot(diff(edges))
    hold(1)
    plot(array(period))
    grid(1)
    xlabel('time [UI]')
    ylabel('Period\nDeviation [%mean]')

    subplot(3,1,3)
    plot(array(phaseError) / mean(period) )
    grid(1)
    xlabel('time [UI]')
    ylabel('Phase Error[UI]')

    savefig('cdrExtraction.png')

    return([phaseError, period])
```

C.4 extractJitter.py

The following Python file extracts jitter from a pattern measurement and is not used for TxRx connection compliance simulations.

```
from numpy import *
from pylab import *

# version 071210.a

def extractJitter(inputT, outputsignalF, signalF, offset, RJ, timestep,
mylength) :

# the offset parameter will eventually be automatically calculated

from scipy.special import erfinv
from penrose import
extractApproxEdge,extractAccurateEdge,extractAccurateEdge
from cdr import cdr
import pdb

_inputT = extractApproxEdge(inputT)
_outputsignalF = extractAccurateEdge(outputsignalF)
```

```
_signalF = extractAccurateEdge(signalF)

j = array(_inputT)[offset:len(_outputsignalF)+offset] - (
array(_outputsignalF) - array(_signalF)[offset:len(_outputsignalF)+offset] )

# extract the noise inbetween two edges
# this could be improved!!
noise = []
for i in range(len(_outputsignalF)-1) :
      noise += [ signalF[ int( (_signalF[offset+i]+_signalF[offset+i+1])/2.0
) ] - outputsignalF[ int( (_outputsignalF[i]+_outputsignalF[i+1])/2.0 ) ] ]


figure()
hold(0)
plot(noise)
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
title('Transmitter Noise')
savefig('noise.png')

outtime  = arange(len(noise)) * timestep
outfile = open('noise.csv','w')
for index in range(len(outtime)) :
      outfile.writelines('%e,%e\n'%(outtime[index],noise[index]))
outfile.close()

if 0:
      figure()
      hold(0)
      plot(_inputT,'x')
      hold(1)
      plot(_outputsignalF,'x')
      plot(_signalF,'x')
      plot(j,'o')
      grid(1)

[pe,per]=cdr(j,0.005,0.005,'CDR Jitter Extraction')

_per = mean(per[1000:])
[pdf,t]=histogram(array(pe[1000:])/_per,100)

# pdb.set_trace()

pdf[find(pdf<5)] = 0
pdf = pdf*1.0 / sum(pdf)
mid = min(find(t>0))
left = max(find(pdf[:mid] == 0)) + 1
rght = min(find(pdf[mid:] == 0)) - 1 + mid

leftcdf = cumsum(pdf[left:mid])
leftcdf[find(leftcdf==1)] = 1-1e-15
rghtcdf = flipud(cumsum(flipud(pdf[mid:rght])))
rghtcdf[find(rghtcdf==1)] = 1-1e-15

leftt = t[left:mid]
rghtt = t[mid:rght]
```

```
Qleft = -sqrt(2) * erfinv( 2.0 * (1 - leftcdf) -1 )
Qrght = -sqrt(2) * erfinv( 2.0 * (1 - rghtcdf) -1 )

npoints = 4
# Pleft = polyfit(leftt[0:npoints],Qleft[0:npoints],1)
# Prght = polyfit(rghtt[-npoints:],Qrght[-npoints:],1)

_Qleft = concatenate(( [-7] , Qleft ))
_Qrght = concatenate(( Qrght , [-7] ))

# _RJ = ( 1.0 / abs(Pleft[0]) + 1.0 / abs(Prght[0]) ) / 2.0
DJ = -Qrght[-1] * RJ - Qleft[0] * RJ

_leftt = concatenate(( [ leftt[0] - (Qleft[0]+7)*RJ ] , leftt ))
_rghtt = concatenate(( rghtt , [ rghtt[-1] + (Qrght[-1]+7)*RJ ] ))

print 'Extracted RJ = %0.4f, DJ = %0.4f'%(RJ, DJ)

figure()
hold(0)
plot(_leftt,_Qleft)
hold(1)
plot(_rghtt,_Qrght)
grid(1)
xlabel('Time [UI]')
ylabel('Q')
title('Extracted Transmit Jitter, RJ = %0.4f, DJ = %0.4f'%(RJ, DJ) )
savefig('ExtractedJitter.png')

return([RJ,DJ])
```

C.5 penrose.py

The following Python file extracts the step response from a pattern measurement and is not used for TxRx connection compliance simulations.

```
from analysis import *
from numpy import *
import numpy
from pylab import *
import time
from string import rsplit, rstrip
from scipy import linalg, interp
from re import *
import pdb

# version 080110.a

def extractApproxEdge(x) :
y = find( abs(diff( (array(x)>0)*1.0 )) == 1.0 )
return(y)


def extractAccurateEdge(x) :
from scipy import interp
```

```
y = []
for i in range(len(x)-1) :
      if ( ((x[i] < 0.0) and (x[i+1] > 0.0)) or ((x[i] > 0.0) and (x[i+1] <
0.0)) ) :
            _y = interp([0],[x[i],x[i+1]],[i,i+1])[0]
            y += [_y]
return(y)

def filter(x,k) :
y = [x[0]]
for _x in x:
      y += [ (_x-y[-1])*k + y[-1] ]
return(y)

def buildM(x,l) :
M = []
for i in range(len(x)-l) :
      M += [ x[i:i+l] ]
return(M)


def penrose(filename, mylength,start,finish,timecol,sigcol) :
#mylength = 800
#start      = 37000
#finish     = 41000
signalFilter= 0.90
stimFilter= 0.90
outputFilter= 0.90


[time,signal]=loadcsv(filename,start,finish,timecol,sigcol)
start = (array(signal)<0).nonzero()[0][0]
end = (array(signal)>0).nonzero()[0][-1]

print 'Signal analysis from %d to %d'%(start,end)

signalF = filter(signal,signalFilter)
signalF = signalF[start:end+1]
inputT      = (array(signalF)>0)*2.0-1.0
inputF      = filter(inputT,stimFilter)
M_inputF = buildM(inputF,mylength)
IM_inputF = linalg.pinv(transpose(M_inputF))
taps        =
matrixmultiply(transpose(IM_inputF),(signalF[mylength/2:mylength/2 +
len(IM_inputF)]))
outputsignal= matrixmultiply(M_inputF,taps)
outputsignalF = filter(outputsignal,outputFilter)

testT             = ones(mylength*10)*-1.0
testT[mylength*5:]= 1.0
testF             = filter(testT,stimFilter)
M_testF           = buildM(testF,mylength)
outputtest  = matrixmultiply(M_testF,taps)
outputtestF = filter(outputtest,outputFilter)

#figure()
#hold(0)
#plot(taps)
```

```
#grid(1)
#xlabel('time [sample #]')
#ylabel('amplitude [V]')
#savefig('taps.png')

figure()
llength = 10000
hold(0)
plot(signalF[mylength/2-1:llength])
hold(1)
plot(inputF[mylength/2-1:llength])
plot(outputsignalF[:llength])
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
legend(['Measured Signal', 'Fundamental Transmitter', 'Reconstructed'])
title('Signal Reconstruction')
axis([axis()[1]/2,axis()[1]/2+1000,axis()[2],axis()[3]])
savefig('inAndOutSignal.png')

figure()
hold(0)
plot(outputtestF)
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
#axis([4900,5100,axis()[2],axis()[3]])
title('Extracted Step Response')
savefig('step.png')

outtime  = arange(len(outputtestF)) * (time[1]-time[0])
outfile = open('extractedStep.csv','w')
for index in range(len(outtime)) :
      outfile.writelines('%e,%e\n'%(outtime[index],outputtestF[index]))
outfile.close()

return([inputT, outputsignalF, signalF, time[1]-time[0]])
```

C.6 portalocker.py

The following Python file locks files for exclusive access.

NOTE 7 - See the ActiveState Code web site at http://aspn.activestate.com/ASPN/Cookbook/Python/Recipe/65203 for information about the portalocker code recipe.

```
# portalocker.py - Cross-platform (posix/nt) API for flock-style file
locking.
#                  Requires python 1.5.2 or better.
# The MIT License
#
# Copyright (c) 2008 Jonathan Feinberg
#
# Permission is hereby granted, free of charge, to any person obtaining a
copy
# of this software and associated documentation files (the "Software"), to
```

```
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# AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER
# LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING
FROM,
# OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN
# THE SOFTWARE.

"""Cross-platform (posix/nt) API for flock-style file locking.

Synopsis:

   import portalocker
   file = open("somefile", "r+")
   portalocker.lock(file, portalocker.LOCK_EX)
   file.seek(12)
   file.write("foo")
   file.close()

If you know what you're doing, you may choose to

   portalocker.unlock(file)

before closing the file, but why?

Methods:

   lock( file, flags )
   unlock( file )

Constants:

   LOCK_EX
   LOCK_SH
   LOCK_NB

Exceptions:

    LockException

Notes:

For the 'nt' platform, this module requires the Python Extensions for
Windows.
Be aware that this may not work as expected on Windows 95/98/ME.

History:
```

```
I learned the win32 technique for locking files from sample code
provided by John Nielsen <nielsenjf@my-deja.com> in the documentation
that accompanies the win32 modules.

Author: Jonathan Feinberg <jdf@pobox.com>,
        Lowell Alleman <lalleman@mfps.com>
Version: $Id: portalocker.py 5474 2008-05-16 20:53:50Z lowell $

"""


__all__ = [
    "lock",
    "unlock",
    "LOCK_EX",
    "LOCK_SH",
    "LOCK_NB",
    "LockException",
]

import os

class LockException(Exception):
    # Error codes:
    LOCK_FAILED = 1

if os.name == 'nt':
    import win32con
    import win32file
    import pywintypes
    LOCK_EX = win32con.LOCKFILE_EXCLUSIVE_LOCK
    LOCK_SH = 0 # the default
    LOCK_NB = win32con.LOCKFILE_FAIL_IMMEDIATELY
    # is there any reason not to reuse the following structure?
    __overlapped = pywintypes.OVERLAPPED()
elif os.name == 'posix':
    import fcntl
    LOCK_EX = fcntl.LOCK_EX
    LOCK_SH = fcntl.LOCK_SH
    LOCK_NB = fcntl.LOCK_NB
else:
    raise RuntimeError, "PortaLocker only defined for nt and posix platforms"

if os.name == 'nt':
    def lock(file, flags):
        hfile = win32file._get_osfhandle(file.fileno())
        try:
            win32file.LockFileEx(hfile, flags, 0, -0x10000, __overlapped)
        except pywintypes.error, exc_value:
            # error: (33, 'LockFileEx', 'The process cannot access the file
because another process has locked a portion of the file.')
            if exc_value[0] == 33:
                raise LockException(LockException.LOCK_FAILED, exc_value[2])
            else:
                # Q:  Are there exceptions/codes we should be dealing with
here?
                raise
```

```
    def unlock(file):
        hfile = win32file._get_osfhandle(file.fileno())
        try:
            win32file.UnlockFileEx(hfile, 0, -0x10000, __overlapped)
        except pywintypes.error, exc_value:
            if exc_value[0] == 158:
                # error: (158, 'UnlockFileEx', 'The segment is already
unlocked.')
                # To match the 'posix' implementation, silently ignore this
error
                pass
            else:
                # Q:  Are there exceptions/codes we should be dealing with
here?
                raise

elif os.name == 'posix':
    def lock(file, flags):
        try:
            fcntl.flock(file.fileno(), flags)
        except IOError, exc_value:
            #  IOError: [Errno 11] Resource temporarily unavailable
            if exc_value[0] == 11:
                raise LockException(LockException.LOCK_FAILED, exc_value[1])
            else:
                raise

    def unlock(file):
        fcntl.flock(file.fileno(), fcntl.LOCK_UN)



if __name__ == '__main__':
    from time import time, strftime, localtime
    import sys
    import portalocker

    log = open('log.txt', "a+")
    portalocker.lock(log, portalocker.LOCK_EX)

    timestamp = strftime("%m/%d/%Y %H:%M:%S\n", localtime(time()))
    log.write( timestamp )

    print "Wrote lines. Hit enter to release lock."
    dummy = sys.stdin.readline()

    log.close()
```

C.7 stateye.py

The following Python file computes the statistical eye.

```
from numpy import *
import pdb
import time
```

```
from matplotlib import *

############################################################
# stateye class

class stateye :

############################################################
# constructor

def __init__(self) :

      self.version='080110.a'

      # debug file
      self.debug = open('stateye.debug','w')

      # transitionState[currentState] = [<possible next state>]
      self.transitionState= []

      # edge[currentState] = [<edge index corresponding to transitionState>]
      self.edge   = []

      # step[<edge index>] = [<time vs. amplitude>]
      # where @t=0;a=0, @t=inf;a=final
      self.step   = []

      # length of each step must be the same and equal to rxLength
      self.UImax  = 0

      # number of states.
      self.nStates= 0

      # bins construction
      # bins is a Markov pdf; bin[<state>][<amplitude index>]
      self.bins   = []
      # see binIndex and binValue for explanation of bin coefficients
      self.noBins = 4001
      self.midBin = 2001
      self.kBin   = 2000
      self.binMax = 2.0
      self.binaxis= (arange(self.noBins) - self.midBin) * self.binMax /
self.kBin

      # parameters for cursor to step time conversion
      # are loaded when generating step responses
      # see cursor2index for details
      self.nomUI  = 1         # number of time indexes in step response for
UI
      self.nomOffset= 0       # simple offset for peak centring
      # amplitude of pulse width shrinkage
      self.pws    = 0         # in UI

def __del__(self) :
      self.debug.flush()
      self.debug.close()

############################################################
```

```
# simple routine to index into pdf bins given a value
def binIndex(self, x) :
      return( round(x / self.binMax * self.kBin) + self.midBin )

############################################################
# simple route to find value for pdf bin given a index
def binValue(self, i):
      return( 1.0 * (i-self.midBin) / self.kBin * self.binMax )

############################################################
# simple routine to convert cursor index and sweep offset into time index of
step response
def cursor2index(self, cursor, sweep) :
      return( int( round( (cursor+sweep) * self.nomUI + self.nomOffset ) ) )

############################################################
# simple routine to convert index to cursor
def index2cursor(self, index) :
      return( (index - self.nomOffset) * 1.0 / self.nomUI )

############################################################
# shift a pdf bin description as convolution
def binShift(self, bin, x) :
      i = self.midBin - self.binIndex(x)
      if i < 0 :
            return( concatenate(( bin[-i:], zeros(-i) )) )
      if i > 0 :
            return( concatenate(( zeros(i), bin[0:-i] )) )
      if i==0 :
            return(bin)

# perform stateye algorithm for single sample phase
# clearly includes pws but not mid band jitter
def calcpdf(self,sweepdelta,startCursor,lastCursor,dj,rj,noise_x,noise_y) :
                from pylab import find
      import pdb
      self.cdf=[]
      self.sweep = arange(-0.75,0.75,sweepdelta)
      #self.sweep = [0.0]
      self.pdf=zeros(( len(self.sweep), len(self.binaxis) ))

      # generate a pre-indexed step response for acceleration of the pdf
calculation
      # should consider this for other variable as well, e.g. dfecoef
      self.stepK = []
      for _step in self.step :
            _stepK = []
            for __step in _step :
                  _stepK += [self.midBin - self.binIndex(__step)]
            self.stepK += [ _stepK ]

      print 'folding %d steps'%len(self.sweep)
      binstore = [ 1.0*zeros((self.nStates,self.noBins)),
1.0*zeros((self.nStates,self.noBins)) ]
      for i_sweep in range(len(self.sweep)) :
            #self.debug.writelines('at sweep %d from
%d\n'%(i_sweep,len(self.sweep)))
            #delta = time.time() - tag
```

```
                print 'sd'%(i_sweep+1),
                #tag = time.time()
                # scan from last cursor to first cursor
                # i.e. back cursor tracing
                # for debug
                bintag = 0
                _bins = binstore[bintag]
                bins = binstore[1-bintag]
                bins = self.start_bins
                _bins[:] = 0.0
                # the value of the step for the given cursor and sweep
                _sweep      = self.sweep[i_sweep]
                for cursor in flipud(range(startCursor,lastCursor)) :
                      # self.debug.writelines('at cursor %d\n'%cursor)
                      #print 'at cursor %d'%cursor

                      # where am I on the time axis
                      currentIndex = self.cursor2index(cursor,_sweep)

                      # next Markov pdf contents
                      # perform Markov convolution
                      # scan through each state
                      for state in range(self.nStates) :

                            # enable for tracking speed of exection
                            # print 'at state %d'%state

                            # scan each possible transition from this state
                            for transition in
range(len(self.transitionState[state])) :
                                  # sweep the pws assuming a simple dirac
distribution
                                  # for debug
                                  # for pws in [-self.pws,self.pws] :
                                  for pws in [0] :
                                        # calculate the next state for the given
state
                                        _nextState =
self.transitionState[state][transition]

                                        # the edge needed to get to this state
                                        _edge       =
self.edge[state][transition]

                                        # when pws is enabled then currentIndex
clearly needs to be correctly modulated
                                        _delta      = -self.stepK[ _edge ][
currentIndex + pws]

                                        # perform a convoltion using a simple
shift and addition for the state given
                                        if _delta==0 :
                                              _bins[_nextState]+=  bins[state]
                                        else :
                                              if (_delta<0) :
                                                    _t = bins[state][-_delta:]
                                                    _bins[_nextState][:len(_t)]
+=  _t
```

```
                                        else :
                                              _t = bins[state][:-_delta]
                                              _bins[_nextState][-len(_t):]
+= _t


                  # enable for dumping the pdfs as they are built up
                  #for _state in range(self.nStates) :
                  #     if len(pylab.find(bins[_state]>0) > 0) :
                  #           print '%s =
%s'%(self.states[_state],array2string(self.binValue(pylab.find(bins[_state]>
0))))

                  bintag = 1-bintag
                  _bins = binstore[bintag]
                  bins = binstore[1-bintag]
                  _bins[:] = 0.0

                  # dfe condition
                  # this is also taking a second
                  if cursor==2 :
                        for dfeCoef in self.dfeCoef :
                              for state in range(self.nStates) :

                                    # going to make a big assumption here!!!
That the threshold for greater than and less than is the same
                                    # also going to make a bug assumption
that the gt and lt results index are also inverse
                                    if 1:
                                          _threshold =
self.binIndex(self.gt_h0[state])

                                          _shift      = self.binShift( \
                                                concatenate(( \

zeros(_threshold), bins[state][_threshold:] )), \

-self.gt_true[state] * dfeCoef )
                                          _bins[state] = add(_bins[state],
_shift)

                                          _shift      = self.binShift( \
                                                concatenate(( \

bins[state][:_threshold],  zeros(self.noBins - _threshold) )), \

-self.gt_false[state] * dfeCoef )
                                          _bins[state] = add(_bins[state],
_shift)
                                    else :
                                          for binIndex in range(self.noBins)
:

                                                if self.binValue(binIndex) >
self.gt_h0[state] :

                                                      _binValue =
self.binValue(binIndex) + self.gt_true[state] * dfeCoef
                                                else :
                                                      _binValue =
```

```
self.binValue(binIndex) + self.gt_false[state] * dfeCoef

_bins[state][self.binIndex(_binValue)] += bins[state][binIndex]

                                bintag = 1-bintag
                                _bins = binstore[bintag]
                                bins = binstore[1-bintag]
                                _bins[:] = 0.0

                          # enable for dumping the pdfs as they are built up
                          #for _state in range(self.nStates) :
                          #     if len(pylab.find(bins[_state]>0) > 0) :
                          #           print '%s =
%s'%(self.states[_state],array2string(self.binValue(pylab.find(bins[_state]>
0))))

            _pdf = zeros(self.noBins)

            # typical good place to break for debugging
            # pdb.set_trace()
            # firstly what if sum = 0; secondly the sum for difference states
may be different???
            # this scaling of the pdf is still not quite workig correctly
            bins = bins / bins.sum()
            for state in range(self.nStates) :
                  _pdf = add(_pdf, bins[state])
                  # this additional of the fliped array is mainly for 8b10b
support. As we only run one set of the codes
                  # we need to add in the other half. I believe this is
correct, but am checking it again
                  _pdf = add(_pdf, flipud(bins[state]))
            _pdf = _pdf / _pdf.sum()
            self.pdf[i_sweep] = _pdf
            self.debug.writelines('final =
%s\n'%(array2string(self.binValue(find(_pdf>0)))))

      print '\nfolding noise'
      # convolve the noise into
      if 0:
            self.pdf_n = zeros(( len(self.sweep), len(self.binaxis) ))
            for i_sweep in range(len(self.sweep)) :
                  for _noise in range(len(noise_x)) :
                        if noise_y[_noise] >0 :
                              _shift = self.binShift(self.pdf[i_sweep],
noise_x[_noise] ) * noise_y[_noise]
                              self.pdf_n[i_sweep]  =
add(self.pdf_n[i_sweep], _shift)
                  self.pdf_n[i_sweep] = self.pdf_n[i_sweep] /
(self.pdf_n[i_sweep]).sum()
      else :
            self.pdf_n = self.pdf

      print 'folding jitter'
      # final pdf containing the jittered version
      if 1:
        self.p = []
        sigma = rj;
        mean  = dj/2;
```

```
        for _sweep in self.sweep :
            p = 1/(sigma*sqrt(2*pi)) * exp(-((_sweep-mean)**2)/(2*sigma**2))
+ \
                  1/(sigma*sqrt(2*pi)) *
exp(-((_sweep+mean)**2)/(2*sigma**2)) + \
                  1/(sigma*sqrt(2*pi)) * exp(-((_sweep)**2)/(2*sigma**2));
            if p>1.0e-12 :
                  self.p += [p]
            else :
                  self.p += [0.0]

        self.p = self.p / sum(self.p);

        self.pdf_pj=zeros(( len(self.sweep), len(self.binaxis) ))
        _jmid = len(self.sweep)/2
        for _i in range(len(self.sweep)) :
                  #print 'at sweep %d'%_i
                            for _j in range(len(self.sweep)) :
                                _k = _i + _j - _jmid
                                if (_k > 0) and (_k<len(self.sweep)) :
                  self.pdf_pj[_i] += self.p[_j] * self.pdf_n[_k]
                  self.pdf_pj[_i] = self.pdf_pj[_i] / self.pdf_pj[_i].sum()

def loadStep(self, inputStep, _ui, _pws) :
      from pylab import find
      # define pulse response
      self.inputStep = inputStep
      self.converge= max(inputStep)
      self.pulse = add(-inputStep[:_ui], +inputStep[_ui:])
      self.nomOffset = find(self.pulse==max(self.pulse))[0]

      # load the step response parameters for
      self.nomUI= _ui
      self.pws= _pws

      # start and last cursor must allow for some margin
      self.startCursor =
(range(self.nomOffset,0,-_ui)[-2]-self.nomOffset)/_ui
      self.lastCursor=
(range(self.nomOffset,len(inputStep),_ui)[-2]-self.nomOffset)/_ui
      self.xindex =
arange(self.cursor2index(self.startCursor,0),self.cursor2index(self.lastCurs
or,0))

      #print 'start cursor %d, finish cursor
%d'%(self.startCursor,self.lastCursor)

def create2TapFIR(self, c, noDFEtaps) :
      from pylab import find
      # input step is the fundamental step response of the system to a 1V
step, and is assumed to be 0@t=0
      # c is a 1x2 array containing the FIR coefficients
      # this function defines the transitionStates, edge transitions and
generates the necessary steps

      self.nStates = 4

      # for each state x
```

```
        #                               0       1       2       3
        x                   = [   [0,0],       [0,1],       [1,0],       [1,1] ]
        x = array(x)*2.0 - 1.0
        self.states = [   '00',       '01',       '10',       '11'   ]
        # load the possible state transition
        self.transitionState = [ [0,1], [2,3], [0,1],   [2,3] ]
        # define the edge used to move from state to state
        self.edge   = [   [0,1],      [2,3],      [4,5],      [6,7] ]
        # load empty steps
        self.step   = [     [],[],        [],[],[],[],[],[] ]

        # preload the Markov pdf with the converged values for the two stable
states,
        # leave the other state empty
        self.start_bins                 = zeros((self.nStates,self.noBins))
        self.start_bins[0][self.binIndex( sum(x[0]*c)*self.converge )] = 1
        self.start_bins[3][self.binIndex( sum(x[3]*c)*self.converge )] = 1

        # this could be more efficient in storage of the indexes, but for a
simple example it doesn't matter
        # for each state and transitions an edge is defined
        # copy the inputStep into each step array, given the correct factor
needed to move states
        for _state in range(self.nStates) :
              for _transition in range(len(self.edge[_state])) :
                    k =
(sum(x[self.transitionState[_state][_transition]]*flipud(c)) -
sum(x[_state]*flipud(c)))
                    self.debug.writelines('in state %d, transitioning to state
%d, using %0.3f\n'\

%(_state,self.transitionState[_state][_transition],k))
                    self.step[self.edge[_state][_transition]] = self.inputStep
* k

        # this is the post equalised step response
        self.pulse = add( add ( \
                    self.step[ self.edge[0][1] ][self.nomUI*2:] , \
                    self.step[ self.edge[1][0] ][self.nomUI:-self.nomUI] ) , \
                    self.step[ self.edge[2][0] ][:-self.nomUI*2] )
        self.pulse = self.pulse/2.0
        self.nomOffset = find(self.pulse==max(self.pulse))[0]

        self.dfeCoef = []
        h0 = self.pulse[self.cursor2index(0 , 0)]
        print 'found h0=%0.3f'%h0
        #                   00    01    10    11
        self.gt_h0 = [-h0, +h0, -h0,  +h0]
        self.gt_true = [-1.0, -1.0,-1.0,-1.0]
        self.gt_false = [+1.0, +1.0,+1.0,+1.0]
        self.lt_h0 = [-h0,+h0,  -h0,  +h0]
        self.lt_true = [+1.0,+1.0,+1.0, +1.0]
        self.lt_false = [-1.0,-1.0,-1.0, -1.0]

        # clearly we need to include here the proper algorithm for finding the
optimum sampling point!!
        for cursor in range(noDFEtaps) :
              self.dfeCoef += [ abs( self.pulse[self.cursor2index(cursor+1,
```

```
0)] ) ]
            print 'Extracting cursor %d, found %0.3f'%(cursor+1,
self.dfeCoef[-1])


def create8b10b_2TapFIR(self,c,noDFEtaps) :
      from pylab import find
      import pdb

      word10b_p = def8b10b()
      words = sort(word10b_p)
      states = ['x','x']

      # scan through all possible 8b10b codes, truncating to a given length l
      # collect all possible codes
      for l in range(1,11) :
            for _words in words :
                  short = _words[:l]
                  if not(any(array(states)==short)) :
                        states += [short]

      # initialise the transition state matrix
      transitionState = []
      for i in range(len(states)) :
            transitionState += [[]]

      # fill transition state matrx
      for i in range(len(states)) :
            # as we search for where this code could have come from, we only
start searching when the
            # code would be a minimum of 2 characters long. e.g. if the code
word is 1001, we search for
            # 100 as the source of this code word
            if len(states[i])>1 :
                  # find the index into the state matrix, for the source of
the current word
                  source = find(states[i][:-1]==array(states))[0]
                  # add this code word index to the transition matrix entry
for the source of this code wor
                  # clearly we will only find one single source per code word
                  transitionState[source] += [i]
            # if we are at the final word, then also add the transitions to
this entry in the transition
            # matrix for getting back to 0 & 1. However, as we are
implementing a 2 tap FIR, we must maintain
            # also the second entry, hence the starting states are 00,01,10 &
11
            if len(states[i])==10 :
                  if states[i][-1]=='0' :
                        transitionState[i] += [0]
                        transitionState[i] += [1]
                  if states[i][-1]=='1' :
                        transitionState[i] += [2]
                        transitionState[i] += [3]

      # as stated above we must over write the first four states to be
correct
      states[0:4] = ['00','01','10','11']
```

```
        transitionState[0] = transitionState[2]
        transitionState[1] = transitionState[3]

        # generate all possible transitions
        k = []
        transitionLookUp = []
        step  = []
        for _i in range(2**3) :
              if _i > 0 :
                    transitionLookUp += [binary_repr(_i)]
              else :
                    transitionLookUp += ['']
              while(len(transitionLookUp[-1])<3) :
                    transitionLookUp[-1] = '0' + transitionLookUp[-1]
              _k = 0
              for _j in range(2) :
                    # the polarity here needs to be checked
                    _k -= (eval(transitionLookUp[-1][_j])*2.0-1.0) *
flipud(c)[_j] - (eval(transitionLookUp[-1][_j+1])*2.0-1.0) * flipud(c)[_j]
              k += [_k]
              step += [self.inputStep * _k]
              self.debug.writelines('edge %s/%d is
%0.3f\n'%(transitionLookUp[-1],_i,_k))

        # scan through actual transitions and enter edge index into array
        edgeText = []
        edge = []
        for _state in range(len(states)) :
              _edgeText=[]
              _edge=[]
              for _transition in range(len(transitionState[_state])) :
                    _nextstate = transitionState[_state][_transition]
                    __edgeText = states[_state][-2:] + states[_nextstate][-1]
                    _edgeText += [__edgeText]
                    __edge = find( __edgeText == array(transitionLookUp) )
                    _edge += [__edge]
                    self.debug.writelines('from %s to %s using
%s/%d\n'%(states[_state],states[_nextstate],__edgeText,__edge))
              edge += [_edge]
              edgeText += [_edgeText]

        self.states = states
        self.transitionState = transitionState
        self.edge   = edge
        self.step   = step

        self.nStates      = len(self.states)
        self.start_bins               = zeros((self.nStates,self.noBins))
        # this is the current initialisation matrix which need extending
        # see the commented conditional statements below
        if 0 :
              self.start_bins[0][self.binIndex( self.converge *
sum(array([-1,-1])*c) )] = 1
              self.start_bins[3][self.binIndex( self.converge *
sum(array([+1,+1])*c) )] = 1
        else :
              for _states in range(len(states)) :
                    if (states[_states][-2:]=='00') :
```

```
                        self.start_bins[_states][self.binIndex(
self.converge * sum(array([-1,-1])*c) )] = 1
                    #if (states[_states][-2:]=='01') :
                    #     self.start_bins[_states][self.binIndex(
self.converge * sum(array([-1,+1])*c) )] = 1
                    #if (states[_states][-2:]=='10') :
                    #     self.start_bins[_states][self.binIndex(
self.converge * sum(array([+1,-1])*c) )] = 1
                    if (states[_states][-2:]=='11') :
                          self.start_bins[_states][self.binIndex(
self.converge * sum(array([+1,+1])*c) )] = 1

      # this is the post equalised step response
      self.pulse = add( add ( \
                  self.step[ 1 ][self.nomUI*2:] , \
                  self.step[ 2 ][self.nomUI:-self.nomUI] ) , \
                  self.step[ 4 ][:-self.nomUI*2] )
      self.pulse = self.pulse/2.0
      self.nomOffset = find(self.pulse==max(self.pulse))[0]
      self.dfeCoef = []
      h0 = self.pulse[self.cursor2index(0 , 0)]

      # clearly we need to include here the proper algorithm for finding the
optimum sampling point!!
      for cursor in range(noDFEtaps) :
            self.dfeCoef += [ abs( self.pulse[self.cursor2index(cursor+1,
0)] ) ]
            print 'Extracting cursor %d, found %0.3f'%(cursor+1,
self.dfeCoef[-1])

      # setup the DFE correction matrix
      self.gt_h0 = []
      self.gt_true = []
      self.gt_false= []
      self.lt_h0 = []
      self.lt_true = []
      self.lt_false= []
      #pdb.set_trace()
      for _states in states :
            if (_states[-2:]=='00') or (_states[-2:]=='10') :
                  self.gt_h0 += [-h0]
                  self.gt_true+= [-1.0]
                  self.gt_false+= [+1.0]
                  self.lt_h0 += [-h0]
                  self.lt_true+= [+1.0]
                  self.lt_false+= [-1.0]
            if (_states[-2:]=='01') or (_states[-2:]=='11') :
                  self.gt_h0 += [+h0]
                  self.gt_true+= [-1.0]
                  self.gt_false+= [+1.0]
                  self.lt_h0 += [+h0]
                  self.lt_true+= [+1.0]
                  self.lt_false+= [-1.0]



# simple example based on step.py in steptheory
# probably doesn't work anymore since extending the code to support more
```

```
features
def bist(self) :
      # states are
      # 0 = 0 0
      # 1 = 0 1
      # 2 = 1 0
      # 3 = 1 1
      self.transitionState = [[0,1],[2,3],[0,1],[2,3]]
      self.edge            = [[0,1],[2,3],[4,5],[6,7]]
      self.step   = [[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 1.04,
1.3600000000000001, 1.5200000000000002, 1.6000000000000001,
1.6000000000000001, 1.6000000000000001], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
-1.1700000000000002, -1.53, -1.7100000000000002, -1.8, -1.8, -1.8], [0.0,
0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, -0.12999999999999998,
-0.16999999999999996, -0.18999999999999997, -0.19999999999999996,
-0.19999999999999996, -0.19999999999999996], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.12999999999999998, 0.16999999999999996, 0.18999999999999997,
0.19999999999999996, 0.19999999999999996, 0.19999999999999996], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
1.1700000000000002, 1.53, 1.7100000000000002, 1.8, 1.8, 1.8], [0.0, 0.0,
0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, -1.04, -1.3600000000000001,
-1.5200000000000002, -1.6000000000000001, -1.6000000000000001,
-1.6000000000000001], \
                  [0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0]]
      self.stepLength= 15
      self.nStates= 4
      self.start_bins= 1.0*zeros((self.nStates,self.noBins))
      self.start_bins[0][self.binIndex(-0.7)] = 1.0
      self.start_bins[3][self.binIndex(+0.7)] = 1.0
      self.calcpdf()


##########################################################
# simple functions to load all the possible 8b10b words
##########################################################
def def8b10b() :
word8b=[
“00000000”, “00000001”, “00000010”, “00000011”,
“00000100”, “00000101”, “00000110”, “00000111”,
“00001000”, “00001001”, “00001010”, “00001011”,
“00001100”, “00001101”, “00001110”, “00001111”,
“00010000”, “00010001”, “00010010”, “00010011”,
“00010100”, “00010101”, “00010110”, “00010111”,
“00011000”, “00011001”, “00011010”, “00011011”,
“00011100”, “00011101”, “00011110”, “00011111”,
“00100000”, “00100001”, “00100010”, “00100011”,
“00100100”, “00100101”, “00100110”, “00100111”,
“00101000”, “00101001”, “00101010”, “00101011”,
“00101100”, “00101101”, “00101110”, “00101111”,
“00110000”, “00110001”, “00110010”, “00110011”,
“00110100”, “00110101”, “00110110”, “00110111”,
“00111000”, “00111001”, “00111010”, “00111011”,
“00111100”, “00111101”, “00111110”, “00111111”,
```