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Information Technology – Microprocessor Systems – Heterogeneous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction)

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Abstract: Enabling the construction of high-performance, scalable, modular, parallel systems with low system integration cost is discussed. Complementary use of physical connectors and cables, electrical properties, and logical protocols for point-to-point serial scalable interconnect, operating at speeds of 10 200 Mb/s and at 1 Gb/s in copper and optic technologies, is described.

Keywords: flow control, encoding schemes, OMI/HIC, packet routing, parallelism, point-to-point serial scalable interconnect, protocols, routing fabric, serial links, serialization, silicon integration, switch chip, transaction layer, wormhole routing.

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INFORMATION TECHNOLOGY – MICROPROCESSOR SYSTEMS – HETEROGENEOUS INTERCONNECT (HIC) (LOW-COST, LOW-LATENCY SCALABLE SERIAL INTERCONNECT FOR PARALLEL SYSTEM CONSTRUCTION)

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International Standard ISO/IEC 14575 was prepared by subcommittee 26: Microprocessor systems, of ISO/IEC joint technical committee 1: Information technology.

International Standards are drafted in accordance with ISO/IEC Directives, Part 3.

Annexes A, B and C form an integral part of this standard.

Annexes D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R and S are for information only.

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INTRODUCTION

(This introduction is not a normative part of ISO/IEC 14575:2000, but is included for information only.)

The construction of high-performance systems with parallel communications, parallel processing, and/or parallel I/O demands a fast, low-cost, low-latency interconnect. It must be fast and low-latency, otherwise it will be the limiting factor in system performance; and it must be low-cost, or it will dominate the system cost. It must also scale well in both performance and cost relative to the system size, otherwise highly parallel systems will be limited in performance or too expensive. Existing standards do not meet these criteria, because they are designed for communication over long distances (which incurs high costs), or because they aim at the extreme of currently achievable performance (which again increases costs), or because they are based on a restricted model such as a bus, which limits overall performance and scalability. A detailed rationale for this standard is given in annex D.

This standard has been developed to complement recent technical developments of highly integrated, low-power interconnect technology implemented in high-volume commodity VLSI processes, and to exploit the simplifications in encodings and protocols resulting from the use of relatively reliable media over relatively short distances. Aspects of the baseline for this standard have their origins in work on parallel systems, which has taken place in a number of ESPRIT projects. In particular, the routing strategy was established in the PUMA project, and the DS-Links were developed partially in the GP MIMD project. Work at interconnect for high-performance mainframe computers at Bull led to the development of the gigabit link technology implemented in Bi-CMOS and CMOS processes. More recently, these developments, together with corresponding optical technology, have been brought together in the OMI/HIC Project (Open Microprocessor Systems Initiative – High Performance Heterogeneous Interconnect – ESPRIT 7252).

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IEEE Std 1355-1995 was approved by the American National Standards Institute on 8 April 1996.

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INFORMATION TECHNOLOGY – MICROPROCESSOR SYSTEMS – HETEROGENEOUS INTERCONNECT (HIC) (LOW-COST, LOW-LATENCY SCALABLE SERIAL INTERCONNECT FOR PARALLEL SYSTEM CONSTRUCTION)

1 Scope and object

This International Standard applies to physical connectors and cables, electrical properties, and logical protocols for point-to-point serial scalable interconnect, operating at speeds of 10 Mbit/s to 200 Mbit/s and at 1 Gbit/s in copper and optic technologies (as developed in Open Microprocessor Systems Initiative/Heterogeneous InterConnect Project (OMI/HIC)).

The object of this International Standard is to enable high-performance, scalable, modular, parallel systems to be constructed with low system integration cost; to support communications systems fabric; to provide a transparent implementation of a range of high-level protocols (communications, e.g. ATM, message passing, shared memory transactions, etc.), and to support links between heterogeneous systems.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of ISO and IEC maintain registers of currently valid International Standards.

CISPR 22, *Information technology equipment – Radio disturbance characteristics – Limits of methods of measurement*

IEC 60352-5:1995, *Solderless connections – Part 5: Solderless press-in connections – General requirements, test methods and practical guidance*

IEC 60512-2:1985, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 2: General examination, electrical continuity and contact resistance tests, insulation tests and voltage stress tests*

IEC 60512-3:1976, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 3: Current-carrying capacity tests*

IEC 60512-4:1976, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 4: Dynamic stress tests*

IEC 60512-5:1992, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 5: Impact tests (free components), static load tests (fixed components), endurance tests and overload tests*

IEC 60512-6:1984, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 6: Climatic tests and soldering tests*

IEC 60512-7:1993, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 7: Mechanical operating tests and sealing tests*

IEC 60512-8:1993, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 8: Connector tests (mechanical) and mechanical tests on contacts and terminations*

IEC 60512-9:1992, *Electromechanical components for electronic equipment; basic testing procedures and measuring methods – Part 9: Miscellaneous tests*

IEC 60793-1, *Optical fibres – Part 1: Generic specification*

IEC 60793-2:1998, *Optical fibres – Part 2: Product specifications*

IEC 60825-1:1993, *Safety of laser products – Part 1: Equipment classification, requirements and user's guide*

IEC 60825-2:2000, *Safety of laser products – Part 2: Safety of optical fiber communication systems*

IEC 60874-1:1999, *Connectors for optical fibres and cables – Part 1: Generic specification*

IEC 60917 (all parts), *Modular order for the development of mechanical structures for electronic equipment practices*

IEC 61000-4-4:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 4: Electrical fast transient/burst immunity test. Basic EMC publication*

IEC 61076-4-101:1995, *Connectors with assessed quality for use in d.c., low-frequency analogue and in digital high-speed applications – Part 4: Printed board connectors – Section 101: Detail specification for two-part connector modules having a grid of 2.0 mm for printed boards and backplanes*

IEC 61076-4-107, — *Connectors – Part 4-107: Detail specification for a twopart connector with assessed quality, for a basic grid of 2.0 mm, with free connectors for non-accessible insulation displacement* [1)]

IEC 61300 (all parts), *Fibre optic interconnecting devices and passive components – Basic test and measurement procedures*

IEC 61156-1:1994, *Multicore and symmetrical pair/quad cables for digital communications – Part 1: Generic specification*

IEC 61196-1:1995, *Radio-frequency cables – Part 1: Generic specification – General, definitions, requirements and test methods*

IEC 61196-2:1995, *Radio-frequency cables – Part 2: Sectional specification for semi-rigid radio-frequency and coaxial cables with polytetrafluoroethylene (PTFE) insulation*

IEC 61754-6:1997, *Fibre optic connector interfaces – Part 6: Type MU connector family*

IEEE Std 100-1996, *The IEEE Standard Dictionary of Electrical and Electronics Terms*

IEEE Std 1301.3-1992, *IEEE Standard for Metric Practice for Microcomputers – Convection Cooled with 2.5 mm Connector (ANSI)*

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1) To be published.

3 Definitions

3.1 General

Common terms are as defined in IEEE Std 100-1996. The terms defined in this clause are specific to this International Standard.

The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform with the standard and from which no deviation is permitted.

The word *should* is used to indicate that among several possibilities one is particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited.

The word *may* is used to indicate a course of action permissible within the limits of the standard.

3.2 Glossary

3.2.1
bit error rate (BER)
ratio of errors to the total number of bits being sent in a data transmission from one location to another

3.2.2
box
a mechanical unit that contains links; the links may either remain inside the box, connecting internal devices, or may leave the box in order to connect internal devices to external ones. A box is assumed to be an EMC compliant enclosure operating under a single electrical environment

3.2.3
character
a group of consecutive bits used to represent control or data information

Characters are of two types: normal characters (N_chars) or link characters (L_chars).

See also: **control character, data character, link character, normal character**.

3.2.4
character layer
layer of the protocol stack that specifies the representation of characters in terms of groups of consecutive bits

The character layer provides the service to the higher layers of the transmission of a continuous sequence of characters on a link.

3.2.5
coding
translation from the original set of bits (character) to a new set of bits (coded character) suitable for serial transmission

See also: **decoding**.

3.2.6
control character
character used for signalling purposes by the exchange, packet or transaction layers of the stack

Both N_chars and L_chars are used as control characters

See also: **link character; normal character**.

3.2.7
data character
character used for packet payload or packet header

A data character represents one of the values of a byte, i.e 0 to 255 (decimal). Only N_chars are used as data characters

See also: **link character; normal character**.

3.2.8
decoding
translation from the coded set of bits (coded character) to the original set of bits (character)

See also: **coding**.

3.2.9
deserialization
assembly of a coded character from the sequence of serial bits

See also: **serialization**.

3.2.10
destination
one or more destination_identifiers, identifying the destination node(s) to which the packet is to be transmitted

See also: **destination_identifier**.

3.2.11
destination_identifier (dest_id)
an implementation dependent identity of a destination node for a packet

3.2.12
destination node
terminal node(s) that is/are to receive a particular packet

See also: **node**.

3.2.13
digital sum variation
difference between the number of logical 1s and the logical 0s transmitted by a link output since commencing operation

See also: **running disparity**.

3.2.14
disparity
difference between the number of logical 1s and logical 0s in a character

A positive or negative disparity indicates an excess of 1s or 0s, respectively.

3.2.15
end_of_packet marker
a control character that indicates the end of a packet

See also: **packet**.

3.2.16
exchange layer
describes the procedure of the node-to-node exchange of characters to ensure the proper functioning of the link

The exchange layer provides the service to the higher layers of the transmission of an indefinite sequence of N_chars.

3.2.17
fabric
a device or a collection of devices that provide(s) a general routing capability, constructed from one or more switches using links

See also: **link; switch**.

3.2.18
flow control character (FCC)
a control character transmitted on a link in the opposite direction to data flow for each direction of data flow, i.e. to the transmitter of data from the receiver, indicating that the receiver has space reserved to receive a further F N_chars

The value of F is specified separately for each technology in this standard.

3.2.19
functional
a link interface becomes functional when the start-up procedure has successfully completed and the link interface is ready to transmit data

3.2.20
link
means of communicating digital information bidirectionally in serial format between two devices or subsystems

A link comprises two link interfaces connected by an appropriate medium (or media, for connections between boards or cabinets), such that the link output of each interface is connected to the link input of the other.

3.2.21
link cable
physical medium connecting two link interfaces, comprising two or more electrical or optical cables

3.2.22
link character (or L_char)
control characters used on a link in order to ensure flow control and the proper functioning of the link

See also: **normal character**.

3.2.23
link input
connection point for receiving signals

See also: **link interface**.

3.2.24
link interface (or port)
connection point comprising a link input and a link output and implementing one of the relevant conformance subsets defined in 10.2

See also: **link**.

3.2.25
link output
a connection point for transmitting signals

See also: **link interface**.

3.2.26
network
any set of devices or subsystems connected by links (directly or indirectly) joining a set of terminal nodes

3.2.27
node
a device or subsystem having one or more link interfaces

A node may be a terminal node (q.v.). A node may perform a routing function, routing packets between its node interfaces according to the information in the destination field of the packet.

3.2.28
node interface
link interface on a switch

See also: **link interface; switch**.

3.2.29
normal character (or N_char)
N_chars represent, at the minimum, the 256 values of a byte (i.e. all the data characters) plus a control character representing an end_of_packet marker

3.2.30
packet
a sequence of N_chars with a specific order and format

A packet consists of a destination followed by a payload. A packet is delimited by an end_of_packet marker.

See also: **destination; payload**.

3.2.31
packet layer
the layer of the protocol concerned with end-to-end transmission of information, possibly through a number of intermediate routers

It is at the packet layer that the routing decisions are taken.

3.2.32
payload
data (a message, a memory access request, an acknowledgment, etc.) that is to be transferred from the source node to the destination node

The data has a specific format, defined in the transaction layer. Note that a payload may be null.

See also: **packet**.

3.2.33
physical medium
See: transmission medium.

3.2.34
port
See: link interface.

3.2.35
routing function
inside a switch, this function determines to which numbered node interface a packet is to be sent, based on the information contained in the packet destination

See also: **switch**.

3.2.36
run length
maximum number of successive bits of the same value that can occur in the coded bit stream

3.2.37
running disparity
cumulative sum of the disparities of characters transmitted from the start of operation of the link up to the present time

A link has two running disparities, one for each direction.

3.2.38
serialization
the process of transmitting coded characters, one bit at a time

See also: **deserialization**.

3.2.39
signal
a measurable quantity (e.g. a voltage) that varies in time in order to transmit information

A signal propagates along a wire or an optic fiber. It is interpreted as a sequence of bits that is grouped into a sequence of characters by the character layer of the protocol stack. Signals are generated by a link output and are absorbed by a link input.

3.2.40
signal layer
the layer of the protocol stack at which signals are specified

3.2.41
sink
consumer of normal characters at a link interface

See also: **normal character**.

3.2.42
source
generator of normal characters at a link interface

See also: **normal character**.

3.2.43
source node
terminal node that originates data

See also: **destination node**.

3.2.44
switch
a routing device (for example, a box or board) providing a set of numbered node interfaces, constructed from one or more switch chips (or by other methods)

See also: **fabric, node interface, switch chip**.

3.2.45
switch chip
a very large scale integration (VLSI) integrated circuit with two or more link interfaces, between which it provides packet routing

See also: **link; switch**.

3.2.46
terminal node
node with one or more link interfaces that are used to originate or consume data across an interconnect complying with this standard

See also: **source; sink**.

3.2.47
transaction
a sequence of packets sent between two or more terminal nodes to perform some function

See also: **transaction layer**.

3.2.48
transaction layer
layer above the packet layer for use by applications

The transaction layer is unspecified in this standard.

See also: **transaction**.

3.2.49
transmission medium
means of transporting electrical or optical signals

See also: **signal**.

4 Physical media and logical layers

This International Standard defines a set of rules for information exchange (the logical layers) together with the ways in which it shall be implemented on a variety of physical media. The logical layers are defined as a protocol stack. Each layer of the protocol stack defines representations (information formats) in terms of the immediately lower layer, together with rules (protocols) for the exchange of these representations.

The use of the physical media and logical layers is illustrated in figure 1. The physical medium and the signal, character and exchange layers are concerned with point-to-point communication between adjacent nodes, while the packet layer provides end-to-end communication between terminal nodes.

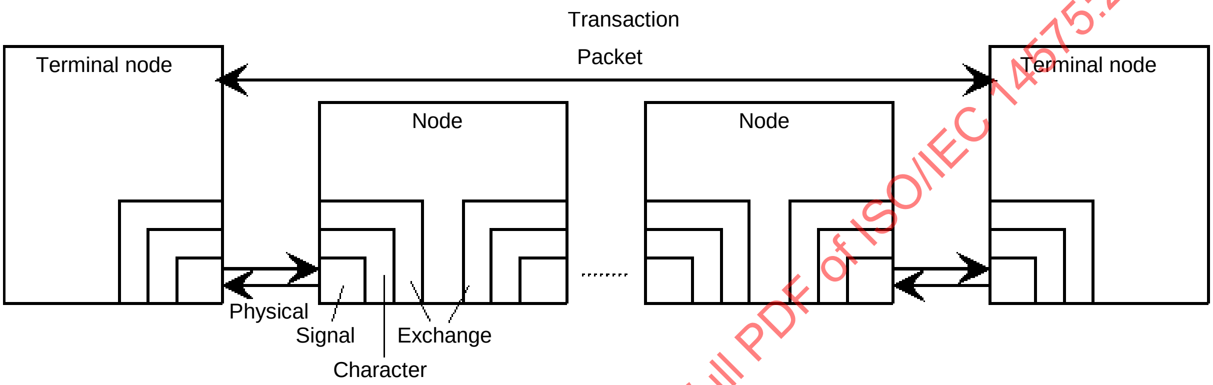


Figure 1 – Protocol stack between nodes

4.1 Physical media

For electrical links, the physical characteristics include the specification of

a) circuit board physical characteristics,
b) connectors and contacts,
c) cables,
d) shielding requirements,
e) line impedance,
f) crosstalk,
g) electromagnetic emission,
h) ESD susceptibility.

For optical links, the physical characteristics include the specification of

– optical transceiver properties,
– optical connectors,
– optical fiber.

4.2 Logical layers

4.2.1 Layer 0: signal layer

4.2.1.1 General description

For electrical links, the signal layer includes the specification of

a) line signal levels and rates

b) power budget, from which transmission distance may be calculated, taking into account the loss from the cables and connectors

c) noise margins.

For optical links, the signal layer includes the specification of

– spectral center wavelength, aperture

– optical power budget.

It is important to note that there is a difference between signals and bits. Signals are the values of a measurable quantity (e.g. voltage levels) that are on the transmission line; bits are the logical 1s and 0s that the signals represent. The measurable quantities vary both in nature and in value depending on the implementation (CMOS, ECL, CML, light pulses on a fiber optic cable, etc.).

The signals may have various properties, such as limited running disparity, limited run length, and/or d.c. balance, over a period of time.

4.2.2 Layer 1: character layer

4.2.2.1 Definition of a character

Bits are transmitted in groups called characters. The character layer provides the service to the higher layers of the transmission of a continuous sequence of characters on a link.

4.2.2.2 General description

Characters are used by the higher layers of the protocol to communicate both data information and control information. The number and representations of the various control characters and the representations of the 256 possible data values varies according to the different types of links specified in this International Standard.

4.2.3 Layer 2: exchange layer

4.2.3.1 Definition of the exchange layer

A link is the means of communicating digital information bidirectionally in serial format between two very large scale integration (VLSI) devices. A link comprises two link interfaces connected by an appropriate medium (or media, for connections between boards or cabinets), such that the link output of each link interface is connected to the link input of the other.

The exchange layer describes the procedure of the node-to-node exchange of characters to ensure the proper functioning of the link.

4.2.3.2 General description

Two types of characters are defined: link character (L_char) and normal character (N_char).

a) L_chars: L_chars are used on a node-to-node link in order to ensure flow control and the proper functioning of the link.

b) N_chars: N_chars represent, at the minimum, the 256 values of a byte plus an end_of_packet marker. The exchange layer provides the service to the higher layers of the transmission of an indefinite sequence of N_chars. It is specified in such a way as to ensure that N_chars are not lost due to limitations of resources (e.g. lack of available buffer space).

L_chars may be arbitrarily interleaved with N_chars on the link as required by the exchange layer.

Note that in the text of this International Standard the data values of a byte (0 to 255) are referred to as data characters, and all the other used characters (i.e. all L_chars and the remainder of the N_chars) as control characters.

Consider two connected nodes, NODE_A and NODE_B (see figure 2). Each node uses a link interface or port (LINK_INTERFACE_A and LINK_INTERFACE_B, respectively) in order to communicate with the other node. Note that a node may have more than one link interface. Each link interface is divided into two parts: a transmitter and a receiver, referred to as transmitter_A and receiver_A for NODE_A and transmitter_B and receiver_B for NODE_B.

Each link interface has a N_char source (SOURCE_A and SOURCE_B) that supply N_chars to transmitter_A and transmitter_B, respectively, and a N_char sink (SINK_A and SINK_B) that accept data from receiver_A and receiver_B, respectively.

Exchange layer information generated and sent, for example, by transmitter_A is received and filtered by the receiver_B and passed directly to transmitter_B (and vice-versa). L_chars shall not be generated by the source nor written into the sink.

4.2.3.3 Flow control

The N_char sink associated with a link interface has a maximum capacity, defined by the physical implementation. N_chars are written into the sink by the receiver as it receives them at the link interface, and are read from the sink by the application using the link. In order to prevent sink overrun a flow control mechanism shall be implemented.

The source (at the other end of the link) maintains a credit associated with the receiving link interface that indicates how many N_chars the source can transmit over the link without overrunning the sink at the receiving end. For every N_char that the source sends, it shall decrement the credit by one. When the credit reaches zero, the source shall not send any further N_chars, but it may continue to send L_chars. The credit maintained by the source shall be increased by a block value (sometimes referred to as a "flit") of F characters when the source receives a Flow Control Character (FCC) from the opposite receiver. If this happens when the credit was zero (which will have inhibited the transmission of N_chars), then the source may recommence transmitting N_chars. An implementation may restrict the amount of credit that a source can record. If a FCC is received when this credit has its maximum value, the FCC may be discarded (ignored) without affecting the operation of the link. A source shall be able to record at least F N_chars of credit.

The initial value of the credit shall be 0. The block size (value of F) is defined as a function of the technology used.

The sink should send a FCC to the source when it has the space to receive F N_chars. Each time the sink authorizes the sending of a FCC it shall reserve the space corresponding to F N_chars. While the sink has unreserved space available it should send FCCs until all its space associated with the link interface is reserved. One of the first actions of each sink after the link has been started from a reset condition should therefore be to send the number of FCCs corresponding to its unreserved space.

Using the flow control mechanism described above, there exists a theoretical maximum line length over which "continuous transmission" can be obtained in the case where every N_char written into the sink is immediately read out of the sink by the receiving application. This maximum length is determined by the size of the sink (which determines the number of FCCs that the receiver sends to the transmitter after the link has been started from a reset condition and thus the initial transmitter credit) and a number of implementation-dependent parameters. This is detailed in annex H.

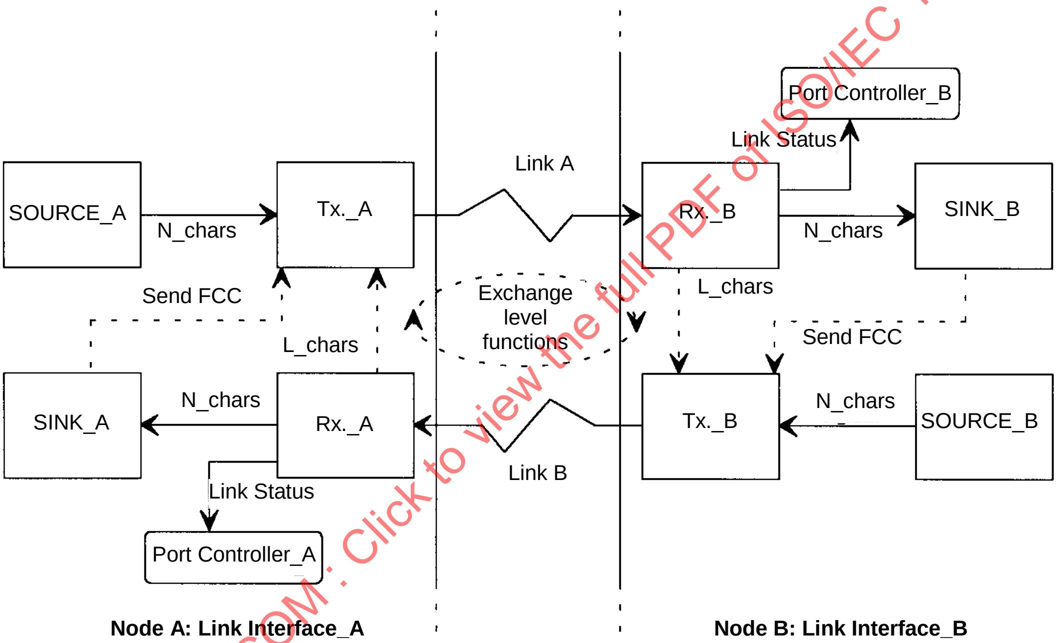


Figure 2 – Exchange layer

Exchange layer flow control greatly simplifies the higher layers of the protocol, since it prevents data from being lost due to buffer overflow and so removes the need for re-transmission unless errors occur. To the user of the system, the net result is that a link functions as a pair of fully handshaken first-in, first-outs, one in each direction. Note that the link interface regulates the flow of data items without regard to the higher layer objects that they may constitute. At any instant the N_chars buffered by a link interface may form part or all of one or more consecutive higher layer objects. L_chars, including FCC, do not belong to such objects and are not buffered.

4.2.4 Layer 3: packet layer

4.2.4.1 Definition of a packet

A packet is a sequence of characters (N_chars only) with a specific order and format. Constituent characters of different packets shall not be interleaved on a link. A packet consists of *a destination* followed by a *payload*. A packet is delimited by an end_of_packet marker.

4.2.4.2 General description

Terminal nodes generate (source node) and consume (destination node) packets. A network is any set of devices connected by links joining (directly or indirectly) a set of terminal nodes.

The protocol assumes the use of packet-switched networks in which the routing information necessary to correctly transmit the packet across the network is contained in the first K N_chars of the packet (where K is fixed throughout a subnetwork). It is at the packet layer that the routing decisions are taken. The protocol does not define a specific (or maximum) size for a packet. Successive packets transmitted on a link may have different lengths and/or destinations. Each packet is transmitted in its entirety, i.e. the transmission of a packet on a link shall be completed before the transmission of the successive packet may commence. Packets sent from a given source node to a given destination node over a network may be delivered in an order different from the sending order. The details of mechanisms to ensure in-order delivery are outside the scope of this International Standard.

4.2.4.3 Destination

The destination contains one or more destination identifiers (dest_id) that are used as the input to the routing function, enabling the routing network to transit the packet from its source node to its destination node. The destination could be null for specific case of a point-to-point link (i.e. the network is just one link). More than one dest_id may denote the same destination node. The method of allocating dest_ids to destinations is outside the scope of this International Standard. See also clause 9 and annex E.

4.2.4.4 Payload

The payload is the data (a message, a memory access request, an acknowledgment, etc.) that has to be transferred from the source node to the destination node. It has a specific format, defined in the transaction layer. Note that a payload may be null.

4.2.4.5 End of packet marker

A packet is delimited by an end of packet marker.

4.2.5 Layer 4: transaction layer

A transaction is a sequence of packets sent between two or more terminal nodes to perform some function. At this layer there are two concepts:

a) definition of the specific payload formats necessary to perform the function;

b) definition of the sequence of exchanges of packets necessary to perform the required function.

The definition of any form of transaction is outside the scope of this International Standard. Annexes F and I illustrate the use of the transaction layer.

4.3 Interaction of layers

The interaction of the layers is illustrated in figure 3.

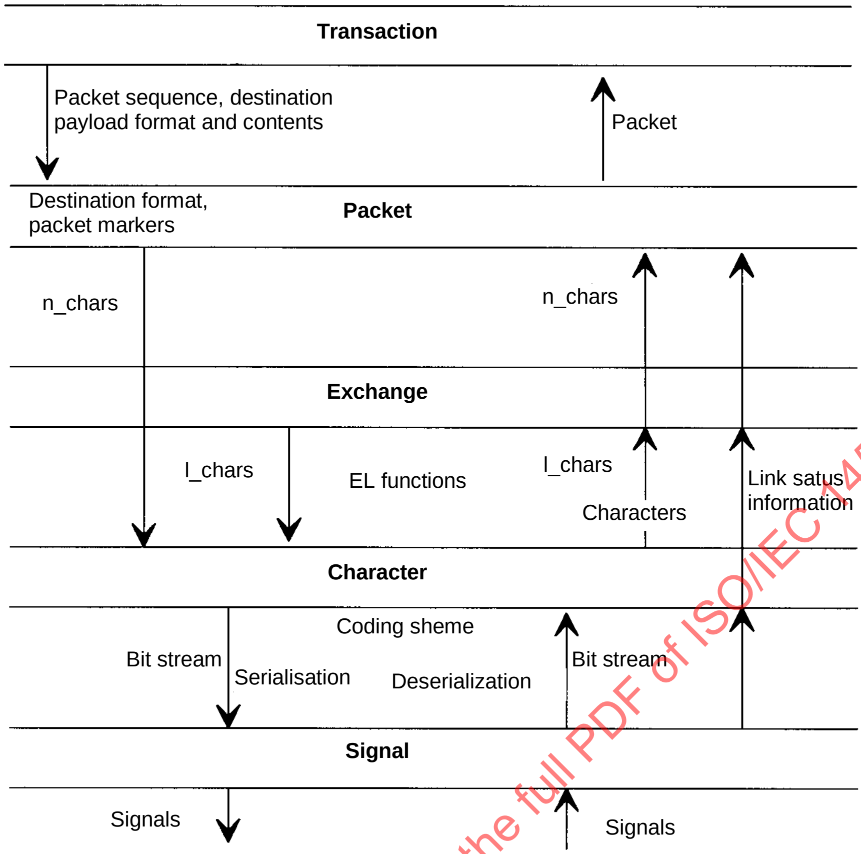


Figure 3 – Protocol stack diagram showing interaction of layers

4.3.1 "Downward going"

4.3.1.1 Transaction layer to packet layer

The transaction layer provides packets to the packet layer. The packet sequence, payload contents and destination address(es) are all determined by the transaction layer. The packet layer forms the packet destination from the destination address(es) and appends the packet with the appropriate end_of_packet marker.

4.3.1.2 Packet layer to exchange layer

The packet layer provides the sequence of N_chars that forms each packet to the exchange layer.

4.3.1.3 Exchange layer to character layer

The exchange layer passes the N_chars that have been provided to it by the packet layer onto the character layer. In order to perform the exchange layer functions, it interleaves L_chars arbitrarily into the sequence of N_chars. The sequence of N_chars is unchanged.

4.3.1.4 Character layer to signal layer

The character layer translates the characters (N_chars and L_chars) it receives from the exchange layer into a bit stream that it passes to the signal layer. The translation is formed of two parts: coding and serialization. Coding is the translation from the original set of bits (character) to a new set of bits (coded character) suitable for serial transmission. Serialization is the process of transmitting coded characters one bit at a time.

4.3.1.5 Signal layer

The signal layer takes the bit stream and outputs signals onto the physical medium.

4.3.2 Upward going

4.3.2.1 Signal layer to character layer

At the receiver end, the signal layer receives signals from the line and generates the corresponding bit stream.

4.3.2.2 Character layer to exchange layer

The character layer deserializes and decodes the bit stream to produce a sequence of characters. Deserialization is the assembly of a coded character from the sequence of serial bits. Decoding is the translation from the coded set of bits (coded character) to the original set of bits (character). The characters are passed to the exchange layer.

4.3.2.3 Exchange layer to packet layer

The exchange layer filters out L_chars for exchange layer functions and passes the N_chars to the packet layer.

4.3.2.4 Packet layer to transaction layer

The packet layer reconstitutes the packets from the received N_chars. This is a logical reconstitution and need not imply that a whole packet is physically assembled. Routing functions are carried out at the packet layer, based on the information in the packet destination. When necessary (e.g. when a packet has arrived at its destination node), the packets are delivered to the transaction layer.

4.3.2.5 Link status information

Link status information is passed up between the layers from the signal layer to the packet layer. The link status information necessary is dependent on the implementation of the link and includes, for example, information on the calibration of the receiver, parity errors, etc. It is for each layer to filter the information that is relevant to its functioning and to pass up the remaining information.

4.4 Implementations defined in this International Standard

The physical and logical layers defined in this International Standard are illustrated in figure 4.

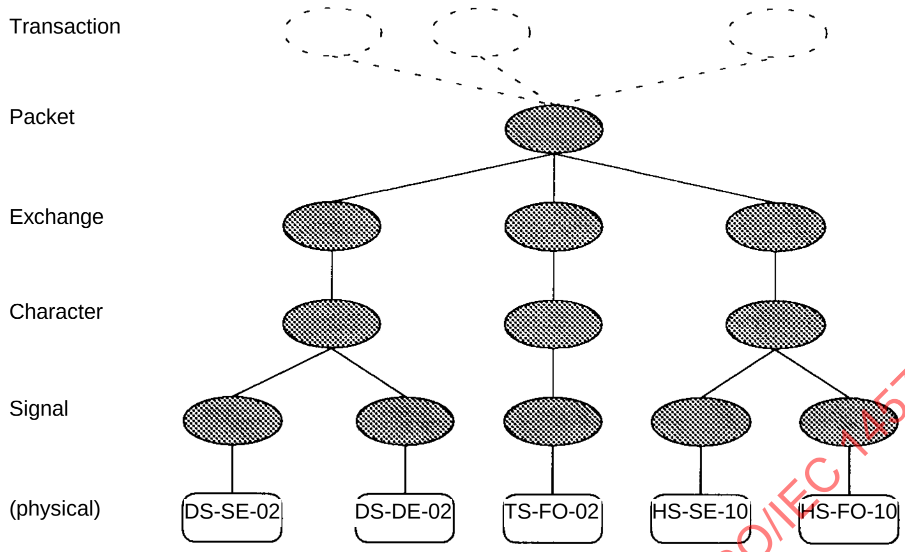


Figure 4 – Defined implementation of physical and logical layers

The physical layer may be implemented in a number of different technologies, identified according to signalling convention, transmission medium, and maximum operating speed.

The format for this identification is given by three parameters:

SC-TM-dd

The possible values of these parameters are given in table 1.

Table 1 – Identification format for technologies

Parameter	Values	Description
SC	DS	Data/strobe encoding
	TS	Three-of-six encoding
	HS	High-speed encoding
TM	SE	Single-ended electrical transmission
	DE	Differential electrical transmission
	FO	Fiber optic transmission
dd	Two digits, representing the maximum operating speed in units of 100 MBd	

Table 2 provides the major properties of each of the defined implementations.

Table 2 – Defined implementations

Technology	Baud rate	Maximum bidirectional data rate	Type of transmission (full duplex)	Maximum distance	Connector specification
Units	Bd	MByte/s	–	m	–
DS-SE-02	1.333-200 M	38	4 wires	1	None
TS-FO-02	250 M	39.4	2 multimode fibers	300	IEC 61754-6
DS-DE-02	1.333-200 M	38	8 wires	10	IEC 61076-4-107
HS-SE-10	700-1 000 M	160	2 coaxial cables	8	IEC 61076-4-107
HS-FO-10	700-1 000 M	160	2 62.5 µm multimode fibers	100	IEC 61754-6
			2 50 µm multimode fibers	1 000	IEC 61754-6
			2 single-mode fibers	3 000	IEC 61754-6

DS-SE links are intended for use for chip-to-chip and board-to-board interconnect. This International Standard does not therefore specify any cable/connector system for these links. DS-DE links are intended for interconnecting sub-racks and adjacent racks using a protocol compatible with DS-SE link from the character layer upwards. TS-FO links are intended to provide longer distance transmission using, necessarily, optical technology, but at speeds compatible with DS-SE links. The use of optical technology necessitates some differences at the exchange layer. HS-SE links are intended for high speed rack-to-rack interconnect. They can, of course, also be used between chips and between boards (across a backplane), given suitable attention to maintaining appropriate signal integrity. HS-FO links are intended to provide longer distance transmission using a protocol compatible with HS-SE links from the character layer upwards.

This International Standard specifies an appropriate cable/connector system for each of the technologies specified within this standard, with the exception of DS-SE links. The connector system is intended as a front-panel adapter and matching cable mounted connector.

This International Standard does not specify any backplane or mezzanine connector standards. This is considered more appropriately specified as an adjunct to specific existing backplane standards.

5 DS-SE and DS-DE

5.1 General

The DS-SE and DS-DE links are designed for point-to-point communication that may be on a single PCB, board to board (DS-SE links), or box to box (DS-DE links). Since this implies that transmission line problems might be present, the electrical level is specified as a transmission line system. In order to reduce the power required for each link (permitting single chips to have a large number of link ports) source-only termination is used for DS-SE links.

A DS-SE/DS-DE input is self-clocking, which means that in any particular system the actual operating speed may be chosen to suit the system, rather than the more normal case of having to engineer a system to suit a pre-determined transmission speed. The maximum speed at which it may run is a function of the maximum speed of the circuitry at each end, plus the properties of the medium connecting the two ends. A link may be operated at lower speeds, for example to provide power saving, down to a level at which the disconnection detection mechanism is triggered.

A link shall operate at a speed of 10 MBd unless and until the system in which it operates determines that it may operate at a different speed. The electrical specification of the link has been designed to allow operating speeds of up to 200 MBd, but the actual operating speed is left open to allow the design of any particular system to trade off engineering costs against operating speed. The means of setting the speed of a link is not defined within this International Standard.

5.2 DS-SE: physical medium

5.2.1 Transmission line requirements

For distances greater than a few centimeters, signal integrity considerations dictate that the link line has to be considered as a transmission line. Discontinuities or variations in characteristic impedance should be kept to a minimum. The transmission line may be made on PCBs but care shall be taken to provide a good ground or power plane beneath the link track and crosstalk with other tracks should be minimized (including between data and strobe lines of the same link). The longest length of line achievable will depend on the materials used for interconnect and the grounding arrangements.

DS-SE supports two standard nominal characteristic impedances for the physical medium, 50 Ω and 100 Ω. Drivers conforming to the DS-SE electrical standard shall support one of these impedances and may support both. Each direction (i.e. the data and the strobe line) of a single point-to-point link shall use either one or other impedance throughout the length of the link and use a matched driver. The opposing directions of a single point-to-point link may, however, use different impedances.

5.3 DS-SE signal level

5.3.1 General

Each connection of a DS-SE link shall be implemented as a unidirectional point-to-point transmission line. The transmission line shall have a characteristic impedance of either 50 Ω or 100 Ω and shall be terminated by high impedance at the receiver. The transmission line may be provided by PCB, coaxial or other suitable controlled impedance interconnect. The receiver shall be designed to accept standard TTL input switching levels with a high input impedance. The driver output impedance should be close to the characteristic impedance of the transmission line both when the driver is driving low or high and also while switching. This is to ensure that reflections generated by the receiver are sufficiently damped by the driver that they do not cause spurious transitions. The range 0.8 V to –2.0 V at the receiver is defined as the transition region. It is very important that the signal at the receiver is monotonic in the transition region, and that the reflections do not cause spurious transitions. This should be ensured by careful design of the interconnect and the driver output.

The propagation of signals is as follows. Assuming that the line is in a steady-state low condition, a high going transition is output by the driver. Because of the relatively high output impedance of the driver compared to the line, this is attenuated, typically to a level of about 1.4 V at the driver output. At the receiver, the high input impedance of the receiver (effectively an open circuit) causes this to appear as a 2.8 V step (taking the input cleanly through the transition region), and the reflection travels back down the line to the driver. Depending on how closely the driver output impedance is matched to the line, this may cause further reflections. It is crucial that the driver is matched sufficiently well that these reflections do not cause spurious transitions at the receiver, or interfere with subsequent output transitions. Propagation for a low-going transition is similar. Figure 1 shows example waveforms for the driver and the receiver end of the transmission line for a 100 Ω system operating from a 5 V supply.

Note that the signal levels at the receiver and the specification of the driver allows DS-SE links to be interconnected between devices operating from 5 V and 3.3 V supply rails as long as the inputs of the 3.3 V devices are tolerant of 5 V signals.

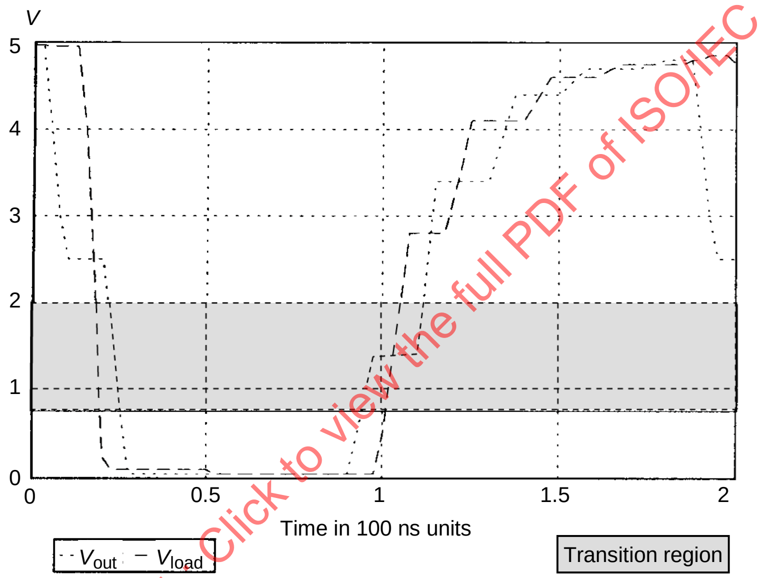


Figure 5 – DS-SE link signal propagation

5.3.2 DS-SE link driver

Each driver should have a nominal output impedance of either 50 Ω or 100 Ω depending on the transmission medium to terminate the reflections from the receiver. The output impedance shall be controlled when the output is fully on driving a high or low level, and also while switching. In order to be adequately matched, the characteristics of the driver and the transmission line shall be related as shown in the table 3.

Table 3 – Driver to line impedance matching table

		V_{dd} = 3.0 V to 3.6 V				V_{dd} = 4.5 V to 5.5 V			
		Z_n		Z_p		Z_n		Z_p	
	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Z_o = 45 – 55	Ω	29	56	37	67	32	52	55	123
Z_o = 90 – 110	Ω	58	112	73	135	64	104	110	247

Z_o is the characteristic impedance of the transmission line. Z_n is the impedance of the driver when the output is driving low, and Z_p the impedance when it is driving high. The figures depend on the supply voltage used by the driver because the input threshold is fixed.

It is recommended that nominal 50 Ω characteristic impedance transmission lines be used in nominal 3.3 V systems and on backplanes.

On power on and reset, a DS-SE link output shall hold both the data and strobe signals low.

Annex J gives an example DS-SE link driver circuit for a 100 Ω transmission line with 5 V supplies.

5.3.3 DS-SE link receiver

A DS-SE link input shall present a high impedance termination to the transmission line. An impedance of >10 kΩ is recommended. This high input impedance is essential to ensure that the correct signal levels are produced at the receiver input.

The input threshold of the receiver is nominally 1.4 V and shall be within the transition region, which is defined as 0.8 V to 2.0 V.

The input capacitance is modeled as described in 5.3.4 (see figure 6) and specified in table 4.

Table 4 – DS-SE input capacitance

Symbol	Parameter	Units	10 MBd		100 MBd		200 MBd		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
C_i	Input capacitance	pF	–	300	–	30	–	4	–

5.3.4 DS-SE link timing

A link shall operate at a speed of 10 MBd, until the system in which it operates shall determine it may operate at a different speed. A link may be operated at a speed lower than its nominal speed to suit the transmission medium. If a link is operated at a lower speed, the same timing constraints shall apply at the receiver inputs.

DS-SE parameters are relative to a reference model, as shown in figure 6.

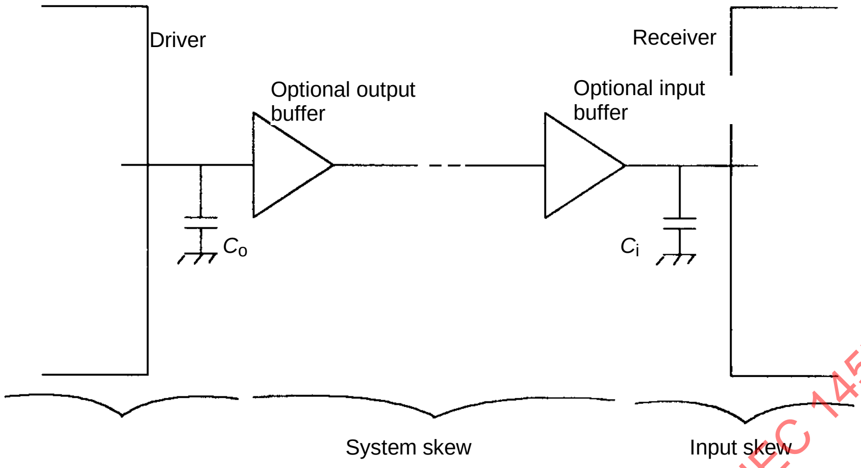


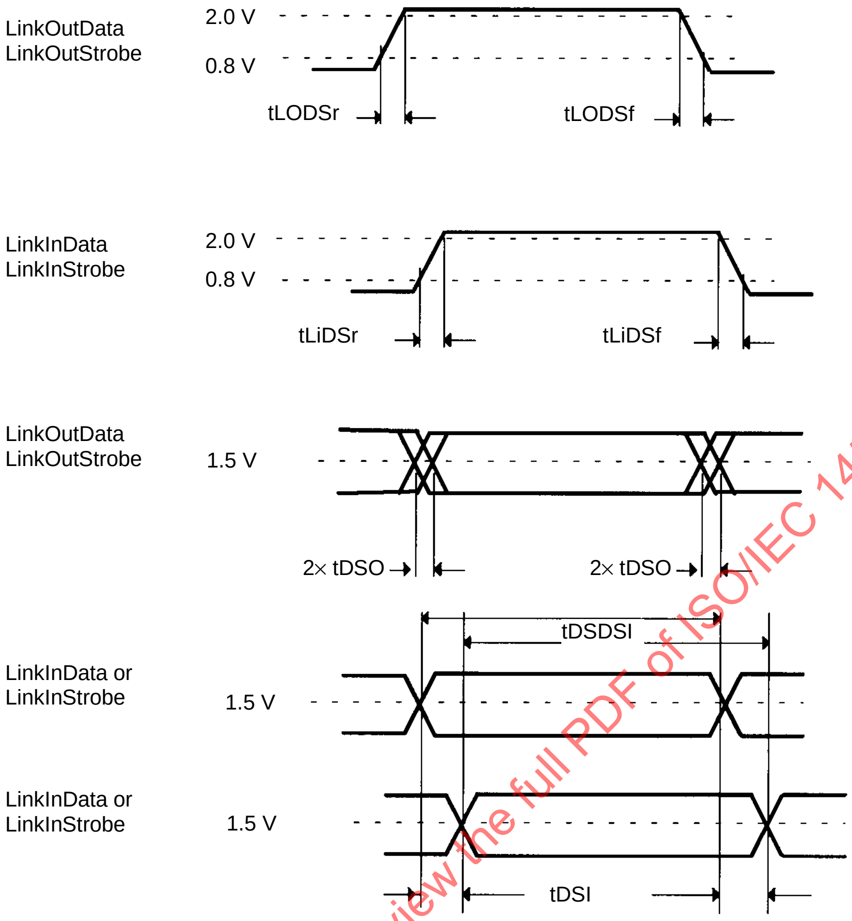
Figure 6 – DS-SE timing reference model

This model shows the possibility of buffers in the signal path, in which case the output impedance of the second buffer is assumed to be not more than 100 Ω, and C_o is assumed to be not more than C_i. If buffers are not used then C_i and C_o are combined into a single capacitive load that may be twice the figure given in table 4. If the output drivers are matched to 100 W, and it is required to use 50 Ω transmission lines, then buffers will be required.

Three sets of timing parameters are defined (see table 5 and figure 7), to allow for operation at the default speed of 10 MBd (DS-SE-00 links), 100 MBd (DS-SE-01 links), and 200 MBd (DS-SE-02 links). A higher speed link type will always be able to operate at a lower speed.

Table 5 – DS-SE timing and swings

Symbol	Parameter	Units	10 MBd		100 MBd		200 MBd		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
tDSI	D/S edge min. separation	ns	–	20	–	2.5	–	1	1.2
tDSDSI	Sustainable input bit period	ns	80	750	9	750	4.5	750	3
tLIDSf	Input fall time (2.0 V – 0.8 V)	ns	–	100	–	100	–	100	4
tLIDSr	Input rise time (0.8 V – 2.0 V)	ns	–	100	–	100	–	100	4



NOTE 1 tDSI is the minimum separation between consecutive edges on the data and strobe inputs (one edge of either sense on each wire) that the link can discriminate correctly. An implementation shall not require this to be greater than the appropriate value specified in table 5.

NOTE 2 The same figure applies to consecutive edges of opposite sense on either the data or the strobe input.

NOTE 3 In general a link input cannot handle a continuous stream of edges separated by tDSI. This figure specifies the sustained bit period that shall be accepted for the nominal baud rate. The maximum nominal bit time is determined by disconnect time-out period of the link receiver.

NOTE 4 This is the slowest edge that the input shall accept.

Figure 7 – DS-SE link timings

The output skew is determined by parameters given in table 6.

Table 6 – DS-SE output skew parameters

Symbol	Parameter	Units	10 MBd		100 MBd		200 MBd		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
tDSO	Output D/S skew	ns	–	±5	–	±1	–	±0.5	1
tLODSf	Output fall time (2.0 V – 0.8 V)	ns	–	40	–	4	–	2	–
tLODSr	Output rise time (0.8 V – 2.0 V)	ns	–	40	–	4	–	2	–

NOTE This is a skew measured at the 1.5 V threshold relative to the nominal time at which it is specified to cross it, defined in terms of consecutive edges. For example, if two consecutive edges are nominally 5 ns apart, the length of time between the time at which each will cross the threshold can be 5 ns ± tDSO.

Allowable system skew is determined by the constraint that the sum of tDSI, the range of tDSO and the system skew shall not exceed nominal bit time. Thus, for DS-SE-01 links the system skew shall not exceed 5.5 ns.

5.3.5 DS-SE link signals

Information on a DS-SE link shall be transmitted using two connections, referred to as data and strobe respectively, in each direction. Each connection shall satisfy the electrical constraints specified in the previous subclause. The data line carries binary data values, and the accompanying strobe line changes state each time the next bit has the same value as the previous one (this does not correspond with the usual meaning of "strobe", which would be a signal that indicates every time that another signal is valid). By this means each DS pair carries an encoded clock, in a way that allows up to a full bit-time of skew-tolerance between the two connections. Figure 8 shows the form of signals on the data and strobe connections.

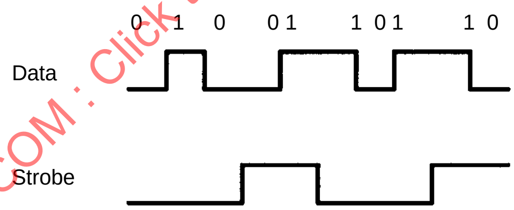


Figure 8 – DS-SE link signal encoding

Since the data-strobe system carries a clock, the links are asynchronous; the receiving device synchronizes to the incoming data. This means that DS-SE (and DS-DE) links autobaud; the only restriction on the transmission rate is that it does not exceed the maximum speed of the receiver. This also simplifies clock distribution within a system, since the exact phase or frequency of the clock on a pair of communicating devices is not critical. It is not essential that both link outputs of one link connection should operate at the same speed, nor that a link output operates at a constant speed. A link output might choose to vary its speed of operation to reduce power consumption when there is no data to be transmitted, for example. The only constraint on the transmission rate is that the bit time limits given in table 5 are not violated, and that it is high enough to prevent a disconnect timeout being triggered (see 5.7.4.2).

A DS-SE link output transmits information on a pair of lines, and a DS-SE link input receives information on a pair of lines. A DS-SE link interface shall comprise a DS-SE link output and a DS-SE link input.

A device providing one or more DS-SE link interfaces shall identify the pins used for each link interface by a convention (using subscription where multiple links are supported) based on function and direction of transmission as shown in table 7.

Table 7 – Identification of multiple link interfaces

DS_SE_data_in	For input of data to the device through the link interface
DS_SE_strobe_in	
DS_SE_data_out	For output of data from the device through the link interface
DS_SE_strobe_out	

A DS-SE link is constructed by connecting the DS_SE_data_out and DS_SE_strobe_out of one link interface to the DS_SE_data_in and DS_SE_strobe_in respectively of the other link interface, and vice versa.

The DS_SE_data_out and DS_SE_strobe_out of a link interface may be connected to the DS_SE_data_in and DS_SE_strobe_in respectively of the same link interface to create a loopback, e.g. for link testing.

5.4 DS-DE: physical medium

5.4.1 Link cable

A DS-DE link cable shall provide ten connections. Eight connections (in four pairs) shall support the eight signals in the DS-DE link; the ninth and tenth connections shall support an optional remote power facility.

A recommendation for the DS-DE cable is given in annex M.

Each connection in the cable shall be color coded as given in table 8 and have the characteristics as given in table 9. Note that attenuation and skew budgets are given in 5.5.3 and 5.5.4.

Table 8 – DS-DE cable color code

Component	Conductor 1	Conductor 2
Pair 1	Red	Green
Pair 2	Brown	Blue
Pair 3	Orange	Yellow
Pair 4	Violet	Gray
Pair 5	Black	White

The link cable shall be clearly marked "ISO/IEC 14575 DS-DE Link Cable".

5.4.2 Connector

The connector system consists of a through-panel (fixed) connector and a cable-mounted (free) connector.

It provides the following features:

a) A full duplex link connection per connector
b) Option for multiple connections on the cable connector
c) Complete screening
d) Robust
e) Latching
f) Small size

The DS-DE connectors shall be as specified in IEC 61076-4-107.

Table 9 – Electrical and mechanical characteristics and safety certification of DS-DE cable

Electrical characteristics	
Differential impedance	95 Ω ± 10 Ω
EMC	Cable shall allow system to meet CISPR limits
Near end crosstalk (backward)	2 % maximum at 100 MHz measured on 10 m sample in differential mode
Far end crosstalk (forward)	4 % maximum at 100 MHz measured on 10 m sample in differential mode
Mechanical performance	
Flexibility	A 60 mm maximum radius shall result when 610 mm of cable is loaded with a suspended weight of 100 g
Flex life	1 000 cycles through 180° at 60 mm bend radius and 100 g load. Following this test, the insulation and jacket should be free of cracks and the conductors free of opens and shorts.
Minimum bending radius (static operation)	40 mm
Safety certification	
For cables up to 10 ft (3 m) in the US	IEC 61156: AWM style 20276, 80C, 30 V, VW1
For cables 10 ft (3 m) to 100 m	IEC 61156 class 2 power limited circuit cable (CL2)

The (free) connector at either end of the cable shall be connected to the conductors in the cable according to table 10.

Table 10 – DS-DE link cable conductors/connectors wiring

Pin	Conductor	Pin
1a	Pair 2 brown	2e
2a	Pair 2 blue	1e
1b	Pair 1 red	2d
2b	Pair 1 green	1d
1c	Pair 5 white	1c
2c	Pair 5 black	2c
1d	Pair 3 orange	2b
2d	Pair 3 yellow	1b
1e	Pair 4 violet	2a
2e	Pair 4 grey	1a

Note that the effect of the cable/plugs assembly is to provide a single twist in each of Pairs 1, 2, 3, and 4, and to provide a single twist between Pairs 1 and 3 and between Pairs 2 and 4. This is shown in figure 9 using Pairs 2 and 4 as an example.

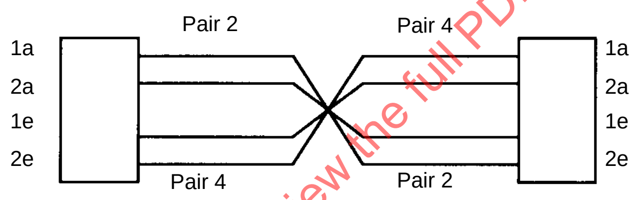


Figure 9 – DS-DE cable assembly twist example

Any extension adapters allowing multiple segments of cables to be used shall also provide such a twist, so that the effect of any such cable/adapter/cable combination is to provide a single twist, as illustrated in figure 10.

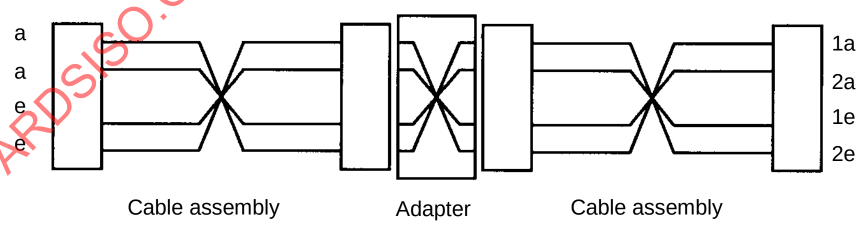


Figure 10 – DE-DE extension adapter

The allocation of DS-DE signals to the connector pins shall be as given in table 11 (which is oriented to correspond to the external view of the through-panel (fixed) connector when mounted on the upper surface of a horizontal PCB. See figure 11.) The direction of the signals is as on the fixed connector.

Table 11 – Pin allocation of DS-DE connector

	2	1	
e	DS_DE_data_in_plus	DS_DE_data_in_minus	(Chamfer corners at this side of the connector)
d	DS_DE_strobe_in_plus	DS_DE_strobe_in_minus	
c	No connect or optional power return	No connect or optional power	
b	DS_DE_strobe_out_minus	DS_DE_strobe_out_plus	
a	DS_DE_data_out_minus	DS_DE_data_out_plus	

Table 12 – DS-DE connector modularity specifications

Characteristic	Specification
Modularity	Fixed connector modules shall be placed on a 6 mm pitch, or their centerlines separated by more than 12 mm
Connector width	5.9 mm maximum

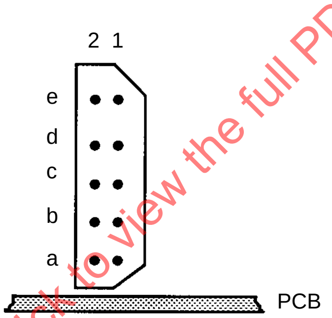


Figure 11 – DS-DE fixed connector external view

Pins 1c and 2c of the DS-DE fixed connector are either both left unconnected on the PCB, or are used to implement an optional power supply, as specified in 5.4.4. It is recommended that fixed DS-DE link connectors with neither source nor sink power connections should include 10 MΩ bleeders to ground on pins 1c and 2c to prevent static build-up on otherwise unconnected power conductors.

In addition to the interface specification of IEC 61076-4-107, the connectors shall have the properties described in table 12.

Annex L provides a recommendation for the PCB layout of the fixed connector.

5.4.3 Environmental constraints

The environmental requirements for the DS-DE link cables and connectors are application dependent. However, as a minimum, the cables and connectors shall meet the constraints in table 13. Note that specific applications may have requirements for extended temperature range, or other environmental parameters.

Table 13 – DS-DE environmental constraints

Parameter	Value
Operating temperature	–10 °C to +60 °C
Non-operating temperature	–40 °C to +85 °C

5.4.4 Optional power supply to DS-DE cable

5.4.4.1 Optional power supply

An explanation of the remote power, and recommendations of components that should meet the following specification, are given in annex K.

Pin 1c either provides an output power supply based on the equipment's 5 V VCC, with a self-healing fuse for overcurrent protection and a (Schottky) diode for reverse-current protection, or provides power to local circuitry from a remote source. Components should be chosen to meet the specification given in table 14. Pin 2c provides for power return.

Table 14 – Optional power supply

Symbol	Parameter	Value
IpHold	Hold current, the operating current that the overcurrent protection device will pass without going high impedance	750 mA minimum
VpOHmin.	Output voltage with respect to pin 2c at maximum steady-state output current	3.75 V minimum at 750 mA
VpOHmax.	Output voltage with respect to pin 2c at any output current greater than a leakage current of 1 mA	5.0 V maximum
IpReverse	Reverse-current	1 mA maximum at reverse voltage of 12 V with respect to pin 2c

The load drawn from this power supply at the end of 500 mm cable with conductors as specified for the DS-DE link cable, shall meet the specification given in table 15. The product of power used and cable length shall not exceed 1 W $\times$ m.

Table 15 – Optional power supply load

Symbol	Parameter	Value
Pp	Power consumption	2.5 W maximum
VpRemoteLow	Lowest input voltage with respect to pin 2c at remote power supply at which the remote power supply is able to supply the required power	3.5 V maximum
VpRemoteHigh	Highest input voltage with respect to pin 2c at remote power supply that the remote power supply can tolerate	5.0 V minimum

5.4.4.2 Power supply protection

The above specification for the remote power supply defines the minimal requirements for operation in the absence of a fault. It is recommended that the overcurrent protection device meets the specification given in table 16 in the event of an overcurrent fault.

Table 16 – Optional power supply protective device

Symbol	Parameter	Value
IpTrip	Trip current, the minimum current that will cause the overcurrent protection device to switch to a high-impedance state	2.5 A
TpTrip	Trip time, the maximum time for the over-current protection device to switch to its high impedance state with a fault current of 10 A	0.5 s
TpReset	Reset time, the time from when a fault is removed to when the over-current protection device returns to its specified characteristics	1 h maximum (but note typical recovery to within 20 % of specification, normally within less than 1 min)

5.4.4.3 Layout convention

It is recommended that in any block of adjacent DS-DE link connectors, the end connector with space adjacent to its pins 1 (the end with the D chamfers of the connector pointing outwards from the block), be supplied with power on pin 1c, and that if more than one connector in any block be supplied with power, all such connectors should be adjacent (see figure 12). Equipment need not have special markings to identify connectors supplying power, but it is recommended that such connectors are clearly documented.

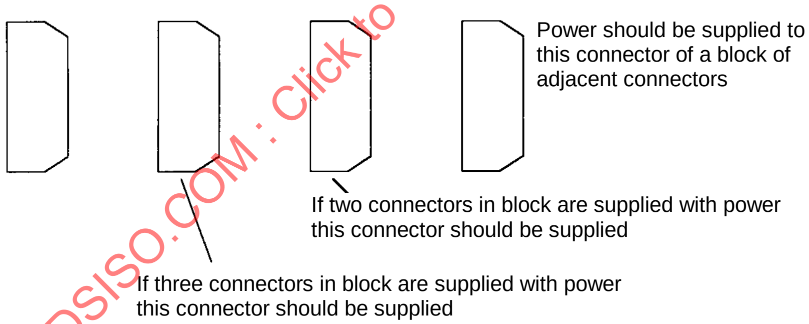


Figure 12 – Multiple power connectors

5.5 DS-DE signal level

5.5.1 General

Differential signalling may be used, e.g. for connections between equipment. Differential signalling provides the following advantages over single-ended signalling.

a) Increased noise immunity

b) Avoidance of ground loops between equipment

A DS-DE link interface may be constructed by connecting two differential drivers and two differential receivers to a DS-SE link interface as follows.

– Each connection point of the DS-SE link output is connected to the input of a differential driver, generating a pair of balanced signals from the on-board DS-SE electrical specification. The two pairs of signals form the DS-DE link output.
– Each connection point of the DS-SE link input is connected to the output of a differential receiver, converting two pairs of balanced signals into two signals conforming to the on-board DS-SE electrical specification. The two pairs of signals form the DS-DE link input.

A DS-DE link interface shall have the logical properties that it would inherit if connected to a DS-SE link interface in this way. This is the recommended implementation of a DS-DE link interface.

A DS-DE link is constructed by connecting two DS-DE link interfaces by a suitable eight-wire transmission line, in the manner defined in 5.4.

A system built using DS-DE links shall meet CISPR limits concerning electromagnetic emissions.

5.5.2 DS-DE signals

Each connection in a DS-DE link shall be made with a nominal 95 Ω transmission line. The transmission line shall be terminated at the receiver inputs: the combination of receiver input impedance and line termination shall be 100 Ω.

The signalling uses a pair of balanced pseudo-ECL signals. Pseudo-ECL signals have ECL-levels shifted by 5 V. See table 17.

Table 17 – DS-DE signal levels

Parameter	Units	Min.	Typ	Max.
Driver differential output voltage	V	0.8	1.0	1.4
Driver common mode output voltage	V	2.5	–	4
Driver output rise time (20 % – 80 %)	ns	0.5	–	2
Receiver input impedance (including termination resistance)	Ω	90	100	110
Receiver input common mode voltage	V	–1.2	–	7.2
Receiver sensitivity	mV	200	–	–

The relevant buffer shall not be placed more than 3 cm from the corresponding fixed connector unless the tracks between the buffer and the connector are matched to 100 Ω.

The DS-SE connection consists of four signals. Each pair of DS-DE signals is specified by reference to a corresponding DS-SE signal, as defined in table 18. Note that DS-DE signals need not be implemented by being derived from the corresponding DS-SE signals.

Table 18 – DS-DE correspondence

Single-ended side	Differential side	
DS_SE_data_out	DS_DE_data_out_plus	DS_DE_data_out_minus
DS_SE_strobe_out	DS_DE_strobe_out_plus	DS_DE_strobe_out_minus
DS_SE_data_in	DS_DE_data_in_plus	DS_DE_data_in_minus
DS_SE_strobe_in	DS_DE_strobe_in_plus	DS_DE_strobe_in_minus

In each differential pair, the plus version of the signal is positive going when the corresponding single ended signal is positive going, and vice versa.

A link shall connect two sets of differential pairs by connecting the DS_DE_data_out_plus of one set to DS_DE_data_in_plus of the other set, DS_DE_strobe_out_plus of one set to DS_DE_strobe_in_plus of the other set, and similarly for the _minus signals.

5.5.3 DS-DE attenuation budget

The total attenuation for each of the DS-DE signals (from output of the driver to input of the receiver) shall be less than or equal to 6 dB at 100 MHz. This attenuation shall be divided following the guidelines given in table 19.

Table 19 – Attribution of attenuation budget

Parameter	Maximum attenuation / dB
Output of driver to output of connector	0.5
Across cable	5
Input to connector and input of receiver	0.5

5.5.4 DS-DE skew budget

The skew shall be divided following the guidelines given in table 20.

Table 20 – Attribution of skew budget

Parameter	Maximum skew between D and S/ns		
	10 MBd	100 MBd	200 MBd
Output of differential driver to output of connector	5	0.5	0.35
Across cable	15	1.5	1.3
Input to connector and input of differential receiver	5	0.5	0.35

If the DS-DE links are implemented by using transceivers to convert between the differential signals and the corresponding single ended DS-SE signals, then the differential skew between D and S shall be controlled so that the resulting single ended signal respects the guidelines given in 5.3.1.

5.5.5 DS-DE link timing

DS-DE link timing is as for DS-SE timing (see 5.3.4, with references to DS-SE replaced by DS-DE).

5.5.6 EM susceptibility

A system using DS-DE links shall meet or exceed IEC 60801-4 specifications on EM susceptibility as a function of the intended operating environment. To reduce susceptibility to EMC it is recommended that it is ensured that the fixed connector is connected to housings by using appropriate EMC brackets and/or gaskets (similar to B.3), or that small common-mode chokes are used in series on the signal lines, and the power lines if connected. A suitable specification for such chokes is 200 Ω min at 20 Hz to 300 MHz, 800 Ω typ at 100 MHz.

5.6 DS-SE and DS-DE character level

In order to provide efficient support for higher level protocols, it is useful to be able to encode characters that may contain a data byte or control information (in other standards these might be referred to as symbols). Each character shall start with a parity bit followed by a control bit that is used to distinguish between data and control characters. In addition to the parity and control bits, data characters contain 8 b of data, and control characters have 2 b to indicate the character type. This is illustrated in figure 13.

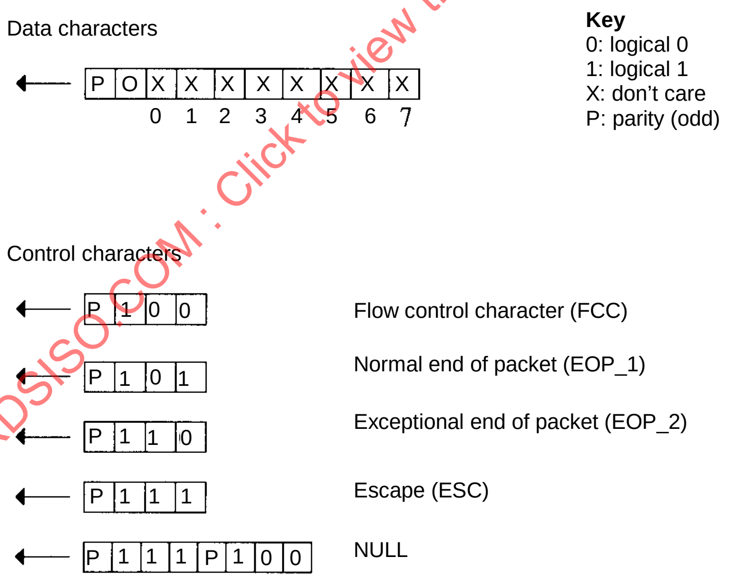


Figure 13 – DS-SE/DS character encoding

Data bits shall be transmitted using the "little endian" convention, i.e. the least significant bit of data shall be transmitted first (immediately after the zero control bit). The first bit transmitted after a reset state shall be a zero (which implies that the first transition is on the strobe wire).

The parity bit in any character covers the parity of the data/control flag in the same character, and the data or control bits in the previous character, as in figure 14. This allows an error in any single bit of a character, including the character type flag, to be detected even though the characters are not all the same length. The parity bit is set such that the total number of 1s in all the bits covered (including the parity bit) is odd.

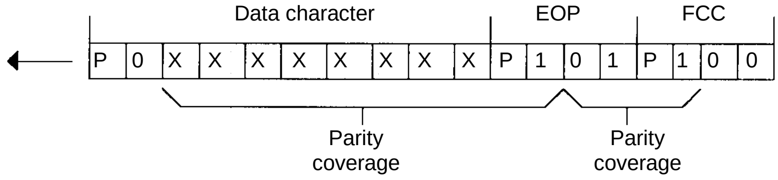


Figure 14 – DS-SE/DS-DE parity coverage

DS-SE/DS-DE links code the N_chars EOP_1 and EOP_2 as shown in table 21, in which P indicates the position of the parity bit in the character.

DS-SE/DS-DE links define and code L_chars as shown in table 22, and their application is discussed in 5.7.

The null character is composed of two characters. The scope of the parity bit in a character that follows a null character includes only the second 4 b control character of the null character; i.e. it will be a one if the following character is a data character, and will be a zero if the following character is a control character.

Table 21 – Terminator character codings

Name	Description	Code
EOP_1	Normal end_of_packet marker	P101
EOP_2	Exceptional end_of_packet marker	P110

Table 22 – Link control character codings

Name	Description	Code
FCC	Flow control character	P100
ESC	Escape character	P111
NULL	Null character	ESC P100

5.7 DS-SE and DS-DE exchange level

5.7.1 General

Once a link output has been started it shall send characters continuously at such a rate that the bit time constraints given in table 4 are never exceeded, unless and until instructed to cease operation or an error is detected. In the absence of other characters, a DS-SE/DS-DE link transmits NULL characters. This ensures the following:

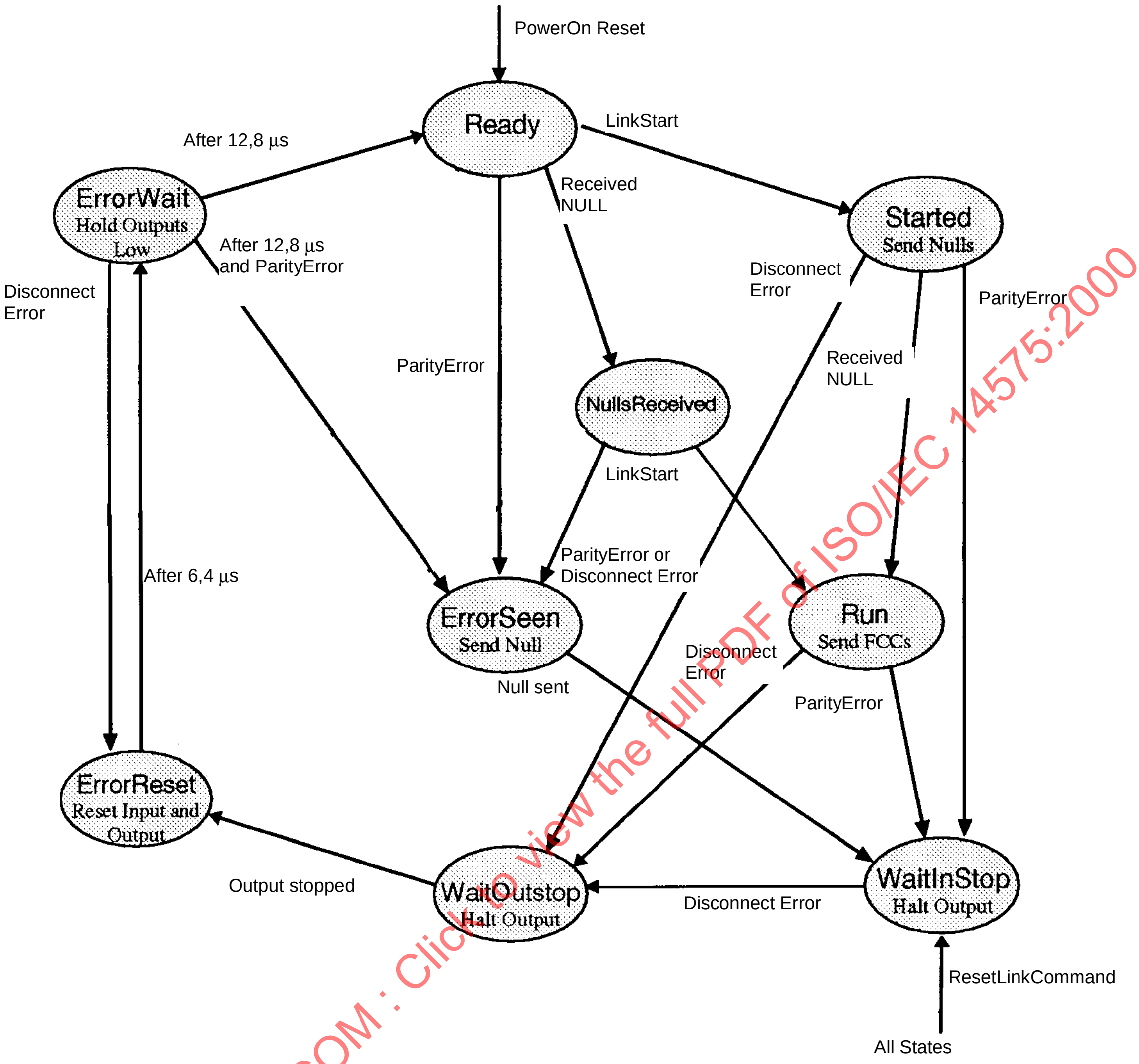
a) physical disconnection of a link is immediately detected; because a DS-SE/DS-DE link transmits characters continuously even in the absence of a message, a physical disconnect can be assumed if the inputting link detects that there are no characters being received, given that some have been received previously;

b) the final parity bit of a packet is transmitted immediately; because the parity of each character is validated by the parity bit of the following character, the validation of the final character of a packet would otherwise be delayed for an arbitrary amount of time.

5.7.2 DS-SE and DS-DE initialization

After reset, a DS-SE link output shall maintain both signals at their reset level until started, i.e. instructed to begin operation (note that receipt of a character by the corresponding link input may be taken as such an instruction). Thereafter it shall send only NULL characters unless and until at least one character has been received by the corresponding link input since reset. After the link output has been started and at least one character has been received by the corresponding link input since reset, the link shall begin normal operation. In normal operation, N_chars provided for transmission are sent when there is flow control credit available, and flow control credit is issued by transmitting FCCs corresponding to available space in the link input buffer. A timeline diagram illustrating DS-DE and DS-DE initalization and reset is given in figure 16.

If a link interface is reset during normal operation, then it shall cease to transmit. This will be detected as a disconnection error by the receiving interface, which then will also cease to transmit. After the exchange of silence protocol, described in 5.7.4.2 and illustrated in figures 15 and 16, both ends of the link will enter the ready state and normal operation may begin. The exchange of silence protocol allows the reset procedure to have the desired effect if the two links are operating in separate reset domains.



NOTE In the ErrorReset state, all transitions on the link input shall be ignored, and the flow-control credit counters and input buffer shall be reset.

Figure 15 – DS link states

5.7.3 Flow control

The credit value (F) of each Flow Control Character (FCC) is set at 8 N_chars.

5.7.4 DS-SE and DS-DE error detection

5.7.4.1 General

DS-SE/DS-DE links can detect various types of errors. The handling of link errors is a subject of annex G.

The DS-SE/DS-DE link exchange protocol allows two common types of error to be detected. First, because each output link, once started, continues to transmit an uninterrupted stream of characters, the physical disconnection of a link can be detected. Second, the parity system will detect all single bit errors at the DS-SE/DS-DE link exchange level.

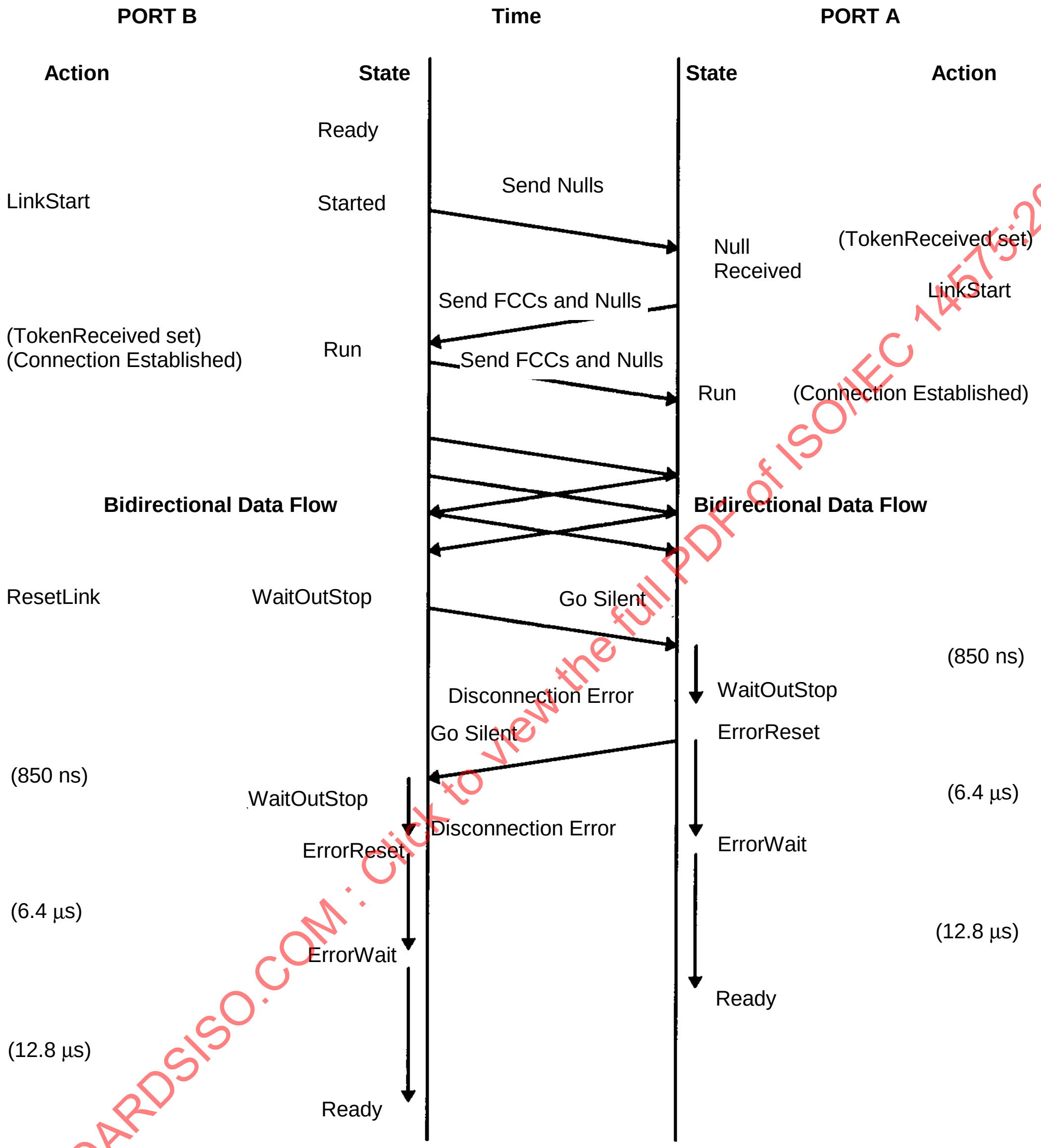


Figure 16 – DS link start-up and reset

5.7.4.2 Disconnection errors

If the links are disconnected for any reason while they are running, then flow control and character synchronization may be lost. In order to restart the link it is therefore necessary to reset both ends to a known flow control and character synchronization point.

Disconnection is detected if, after a bit has been received, no bits are seen by a link input in any 850 ns window. Once a disconnection error has been detected the link shall halt its output. This will subsequently be detected as a disconnect error at the other end, and will cause that link to halt its output also. Once the output has halted, the link shall reset both its transmitter and its receiver for 6.4 µs, during which time its receiver is insensitive to transitions on the data and strobe inputs. After this, the link shall wait at least 12.8 µs before allowing communication to restart. This time is sufficient to ensure that both ends of the link have observed disconnection and cycled through reset back into the waiting state. The connection may now be restarted as described above. If a link interface detects a disconnect error before it has started, it shall start, transmit at least one character, and then halt, to ensure that a disconnection error is also detected by the other end, in the case that it was caused by an externally applied reset rather than physical disconnection. Figure 15 illustrates a suitable state machine for DS-SE and DS-DE error handling.

5.7.4.3 Parity errors

Following a parity error, both character-level synchronization and flow control status are no longer valid, therefore both ends of the link must be reset. This is done autonomously by the DS-SE/DS-DE link using an exchange-of-silence protocol.

When a link interface detects a parity error on its input it shall halt its output. This will subsequently be detected as a disconnect error at the other end, and will cause that link interface to halt its output also, causing a disconnect to be detected at the first end. The normal disconnect behavior described above will then ensure that both ends are reset (irrespective of line delay) before either is allowed to restart. If a link interface detects a parity error before it has been started, it shall start, transmit at least one character, and then stop to ensure that a disconnection error is detected by the other end.

6 TS-FO-02 fiber optic link

6.1 Physical medium

6.1.1 General optical characteristics

The TS-FO-02 optical link cable is a fiber cable containing two fibers, one for transmission in each direction. A 62.5 µm multimode fiber shall be used, and shall meet, at minimum, the specifications given in IEC 60793-1-A1-b. A summary of the main optical characteristics (as specified in IEC 60793-1-A1-b) of the fiber is given in table 23.

The link cable shall be clearly marked "ISO/IEC 14575 TS-FO Link Cable". A recommendation for fiber construction is given in annex S.

Table 23 – Summary of main optical characteristics of TS-FO fibers

Parameter	Units	Value
Fiber type	–	Multimode
Core diameter	µm	62.5
Cladding diameter	µm	125
NA	–	0.275
Attenuation	dB/km	4 maximum at 850 nm

6.1.2 Optical connector

The TS-FO link optical connector is a MU connector-duplex. The MU connector-duplex consists of a through-panel (fixed) adapter and a cable mounted (free) plug. It provides the following features:

a) a dual multimode fiber connection per connector;

b) push-pull coupling;

c) small size.

The connectors shall be as specified in IEC 61754-6. In addition to the interface specification of IEC 61754-6, the connectors shall have the properties described in table 24.

Table 24 – TS-FO connector modularity specifications

Characteristic	Specification
Modularity	Connector modules shall be placed on a 14 mm pitch, or their centerlines separated by more than 28 mm
Connector width	13.9 mm maximum
Overall connector length (to end of boot)	55 mm maximum

The plug at either end of the cable shall be connected to the fibers in the cable in such a way as to connect ferrule 1 in one plug with ferrule 2 in the other plug, and vice versa, as shown in figure 17.

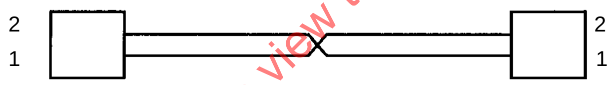


Figure 17 – TS-FO cable fibers/plugs wiring

Note that the effect of the cable/plugs assembly is to provide a single twist. Any extension adapters allowing multiple segments of cables to be used shall also provide such a twist, so that the effect of any such cable/adapter/cable combination is to provide a single twist, as illustrated in figure 18.

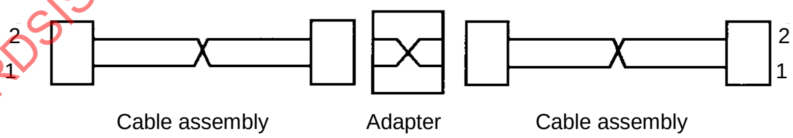


Figure 18 – TS-FO extension adapter

The allocation of TS-FO signals to the plug ferrules and adapter shall be as given in table 25 (which is oriented to correspond to the external view of the through-panel (fixed) adapter when mounted on the upper surface of a horizontal PCB, see figure 19). The direction of the signals is relative to the fixed adapter.

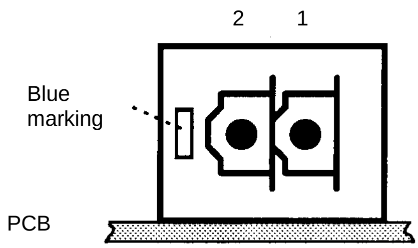


Figure 19 – TS-FO fixed adaptor, external view and ferrule allocation

Table 25 – TS-FO signal allocation

Ferrule	2	1
Signal	TS_FO_in	TS_FO_out

6.1.3 Environmental constraints

The environmental requirements for the TS-FO link cables and connectors are application dependent. However, as a minimum, the cables and connectors shall meet the constraints in table 26. Note that specific applications may have requirements for extended temperature range or other environmental parameters.

Table 26 – TS-FO environmental constraints

Parameter	Value
Operating temperature	–10 °C to +6 °C
Non-operating temperature	–40 °C to +85 °C

Further environmental specifications are given in table C.2.

6.2 Signal level

6.2.1 Transmitter and receiver characteristics

Launch power and sensitivity are strongly dependent on the kind of optical components used and on the configuration of the LED/laser modulation and of the photodiode amplifier. Table 27 gives the recommended transceiver characteristics for an LED-based system.

Table 27 – TS-FO recommended transceiver characteristics

Parameter	Units	Value		
		Minimum	Typ	Maximum
Operating speed	MBd	–	–	250
TS-FO transmitter	–	–	–	–
(LED into 62.5 µm fiber)	–	–	–	–
Launch power	dBm	–13	–	–10
Wavelength	nm	760	–	900
Spectral width (FWHM)	nm	–	60	–
TS-FO receiver	–	–	–	–
Sensitivity at BER 10^{-12}	dBm	–22	–	–
Dynamic range	dB	12	–	–

6.2.2 TS-FO link timing

The TS-FO link shall operate at 250 MBd ± 10^{-10} ppm.

6.2.3 TS-FO reference link

A link comprises two link interfaces connected by appropriate media, and transmits information bidirectionally. For specification and test purposes, a TS-FO Reference Link is defined as a transceiver (the link interface), connected by a pair of fibers to an adapter, connected by a plug-cable-plug assembly to another adapter, connected to another transceiver by a pair of fibers, as shown in figure 20. This figure also shows reference test points TP1 and TP4 (where TPx are at the extremities of the optical cable).

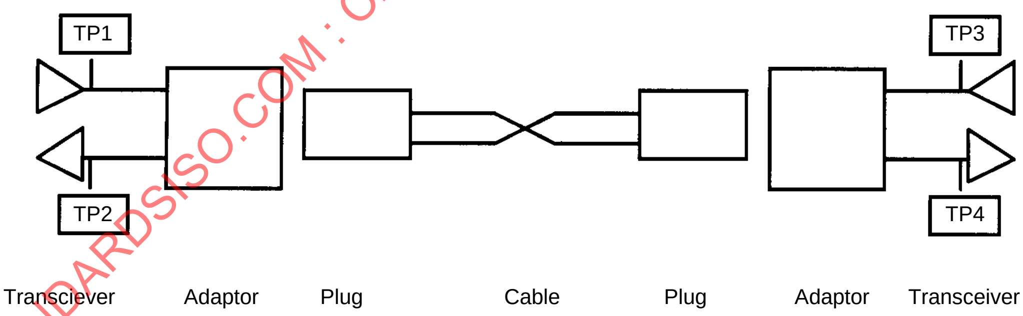


Figure 20 – TS-FO reference list

6.2.4 Link performance

The performance of the various components of the link system shall be as in table 28. The International Standard specifies a power budget for a link, i.e. the maximum loss. A "loopback" plug is defined as a single plug with a minimum length of fiber that connects ferrule 1 to ferrule 2. This is used to provide the specification of the loss of a connector system and a reference specification for the power budget for the cable assembly. The performance of a minimum length reference cable is assumed to be equivalent to the performance of the loopback system. Note that this provides a high degree of confidence of interoperability within a practical test environment, but does not provide a guarantee of interoperability.

Table 28 – TS-FO link performance specification

Characteristic	Specification	Test specification
Link length	300 m maximum	
Power budget (total loss in a link)	6.5 dB maximum	TP1 to TP4 and TP3 to TP2
Loopback test loss	1.5 dB maximum	Loss between TP1 and TP2 using a loopback plug
Cable assembly additional attenuation	5 dB maximum	Difference in loss between the loss measured from TP1 to TP4 (and TP3 to TP2) with cable under test and the loopback test loss as defined above

6.2.5 Eye safety

IEC 60825 is the most stringent standard for laser radiation eye safety. It is for the implementor to take appropriate measures to ensure eye safety.

6.3 TS-FO character level

6.3.1 General

The coding is chosen to ensure that single-bit errors do not generate multiple-bit errors on decoding, and to avoid the overheads of CRC checking (which would double the length of small packets).

6.3.2 Symbols

Each character is coded as two six-bit symbols, where each symbol has three ones and three zeros, hence, the code is described as a "three-of-six" code. There are twenty valid symbols that have three ones and three zeros, of which sixteen values are used for data and two values are used for control. The remaining two values are unused. Table 29 shows the symbols allocated to the sixteen data nibbles (the symbols are drawn as on a oscilloscope trace, with the least significant bit, i.e. the first transmitted, on the left).

Table 29 – Symbols allocated for character coding of data values

Hex	LSB MSB
0	011010
1	101001
2	011001
3	110001
4	001101
5	101100
6	011100
7	110100
8	001011
9	100011
A	010011
B	110010
C	001110
D	100110
E	010110
F	100101

This selection of data symbols for the particular four bit values has several advantages. Apart from the values 0 and F the coding is systematic in respect of bits 0, 1, 3, and 4. The redundant bits, 2 and 5, are placed in such a manner as to guarantee transitions within each symbol in at least two locations, each location occurring in one of two places. Thus, there will always be a transition either between the first and second bits or the second and third bits, and either between the fourth and fifth bits or the fifth and sixth bits.

The symbols 000111 and 111000 are not utilized because they increase the run length and digital sum variation (DSV) of the code. Furthermore, the symbols 010101 and 101010 are not used for data symbols so as to limit the number of adjacent alternating bits in a data stream, but are reserved as symbols used for control characters.

Control characters are formed by composing two symbols, called CONTROL and CONTROL*. Each of these two symbols is always one of 101010 and 010101, depending upon the final bit of the preceding symbol, as shown in table 30.

Table 30 – Symbols for control characters

Previous symbol	CONTROL	CONTROL*
xxxxx0	010101	101010
xxxxx1	101010	010101

Control characters are readily identifiable as having a greater number of transitions than any data symbol. This definition enables

a) the boundaries between data characters and control characters to be easily identified,

b) character synchronization to be checked.

6.3.3 Data characters

Data characters are comprised of two data symbols. Bits 0 to 3 of each data character are transmitted by the first symbol and bits 4 to 7 are transmitted in the second symbol.

6.3.4 Control characters

The control characters NULL and FCC are comprised of CONTROL and CONTROL* symbols. The control characters EOP_1 and EOP_2 are comprised of a control symbol and a data symbol, where the data symbol is the longitudinal error check code described in 6.4.4.2. See table 31.

Table 31 – Coding of control characters

Control character	Symbols	Previous symbol	Symbols (binary)
NULL	CONTROL CONTROL*	xxxxx1	101010 101010
		xxxxx0	010101 010101
FCC	CONTROL CONTROL	xxxxx1	101010 010101
		xxxxx0	010101 101010
EOP_1	CONTROL checksum	xxxxx1	101010 checksum
		xxxxx0	010101 checksum
EOP_2	checksum CONTROL	checksum=xxxxx1	checksum 101010
		checksum=xxxxx0	checksum 010101

A final control character, comprised of four symbols, is used for initialization. This is a sequence of as many transitions as possible, as shown in table 32.

Table 32 – Coding of INIT

Control character	Symbols	Previous symbol	Symbols (binary)
INIT	CONTROL CONTROL* CONTROL* CONTROL*	xxxxx1	101010 101010 101010 101010
		xxxxx0	010101 010101 010101 010101

6.4 TS-FO exchange level

6.4.1 General

In normal operation and in the absence of other characters, a TS-FO link shall transmit NULL characters.

6.4.2 Initialization

When a link interface starts it shall transmit INIT characters. The very first INIT character is selected by assuming a "previous" symbol of xxxxx0. When a link interface has been both transmitting and receiving INIT characters for 125 µs ± 5 µs, it shall then send NULL characters. When a link interface has been transmitting and receiving NULL characters for at least 125 µs ± 5 µs, it shall then transmit a single INIT character, followed by NULL characters. When a link interface has both sent and received a single INIT character, it may send FCC characters. When a link interface has received at least one FCC, it is free to start normal operation. An appropriate state machine is illustrated in figure 21 and a timeline in figure 22.

If a link interface has been sending NULL characters for more than 400 µs, but has not received the INIT character, or if the link interface has received any character other than NULL since the first NULL character it received and before the INIT and FCC characters, the link interface shall restart the initialization sequence by reverting to transmitting continuous INIT characters.

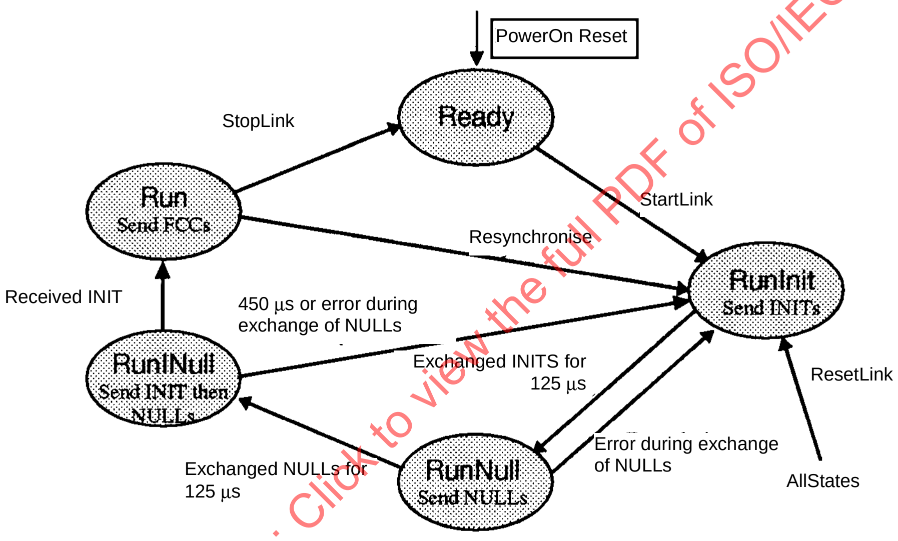


Figure 21 – TS-FO link states

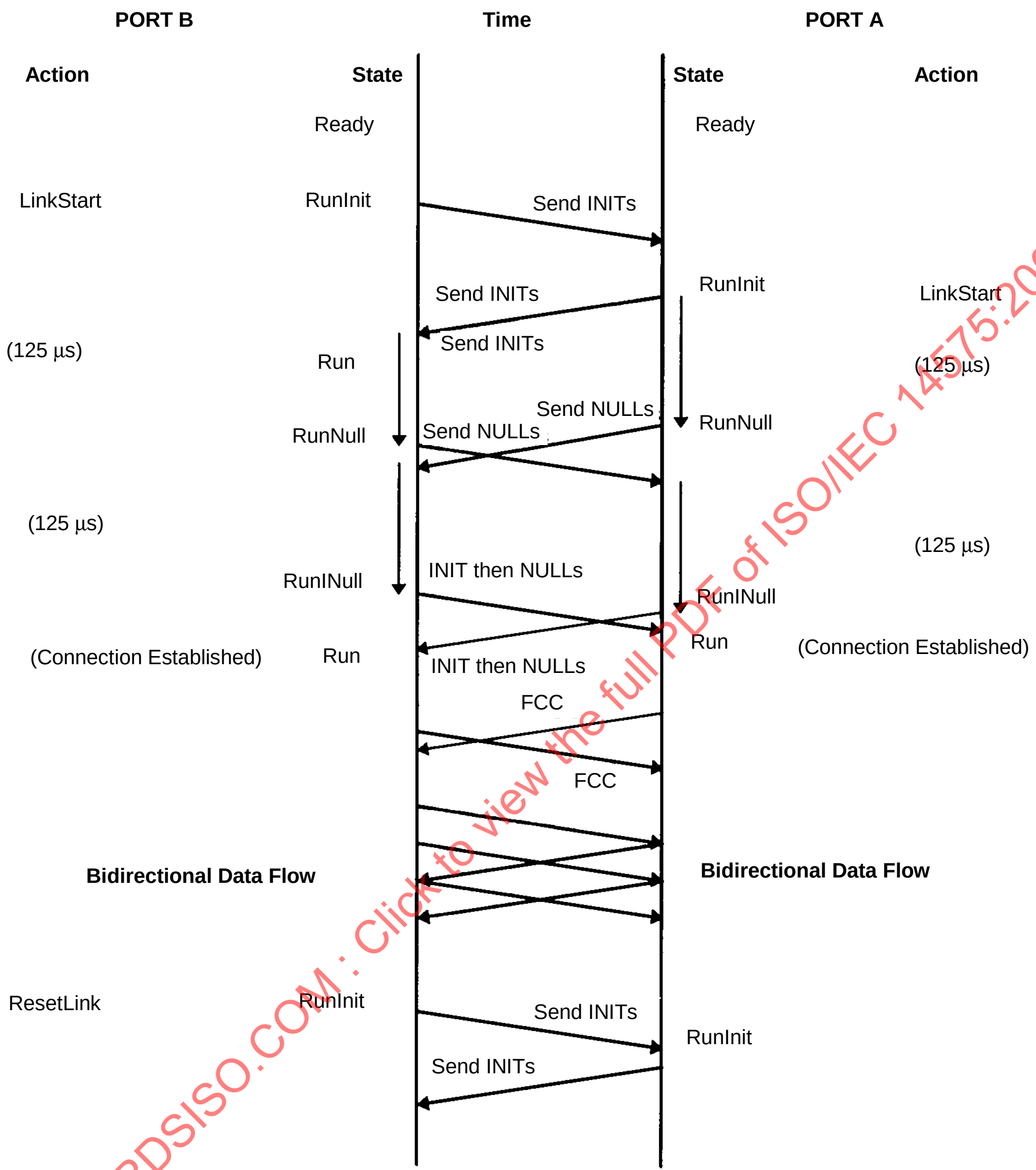


Figure 22 – TS link start-up and reset

6.4.3 Flow control

Exchange level flow control (i.e. control of the flow of characters between link interfaces) shall be performed on each link. The additional characters used are not visible to the higher-level packet protocol.

The credit value (F) of each Flow Control Character (FCC) is set at 16 N_chars.

6.4.3.1 Maximum transmission line length and latency

The appropriate formulas are given in annex H. Note that in a given implementation, the appropriate N_char sink size will have to be chosen in order to prevent the flow control mechanism periodically stalling the data flow over long lengths of fiber.

6.4.4 Error detection

Although DS-SE/DE, and fiber interfaced TS-FO links are designed to be reliable, the attenuation, dynamic range, and distance of fiber connected links mean they are prone to errors and these errors shall be detected. Checks are applied to the connection itself, to packets, to characters, to symbols, and to bit-sequences.

6.4.4.1 Disconnection

During normal operation, if a link interface is reset, it shall start transmitting INIT characters and shall revert to the initialization sequence. During normal operation, the reception of at least two consecutive INIT characters implies disconnection. This allows links operating in separate reset domains to resynchronize correctly.

6.4.4.2 Packets checked with longitudinal error check code

The code for each symbol allows an unusually rigorous check, checking for all single-bit errors and only missing errors when one bit is turned from a one to a zero, and another is turned from a zero to a one. Such errors shall be detected by a longitudinal check covering all the data symbols in the packet. The check used shall be a longitudinal even parity check of the nibbles of each data character. The data characters and the parity are subsequently encoded as six bit data symbols.

The four check bits shall be converted into the corresponding data symbol for transmission, decoded on receipt, and compared with the check computed from the received data symbols. The conversion of a packet into its encoded form, incorporating the encoded parity in either the EOP_1 or the EOP_2 character, as desired, is shown in figure 23.

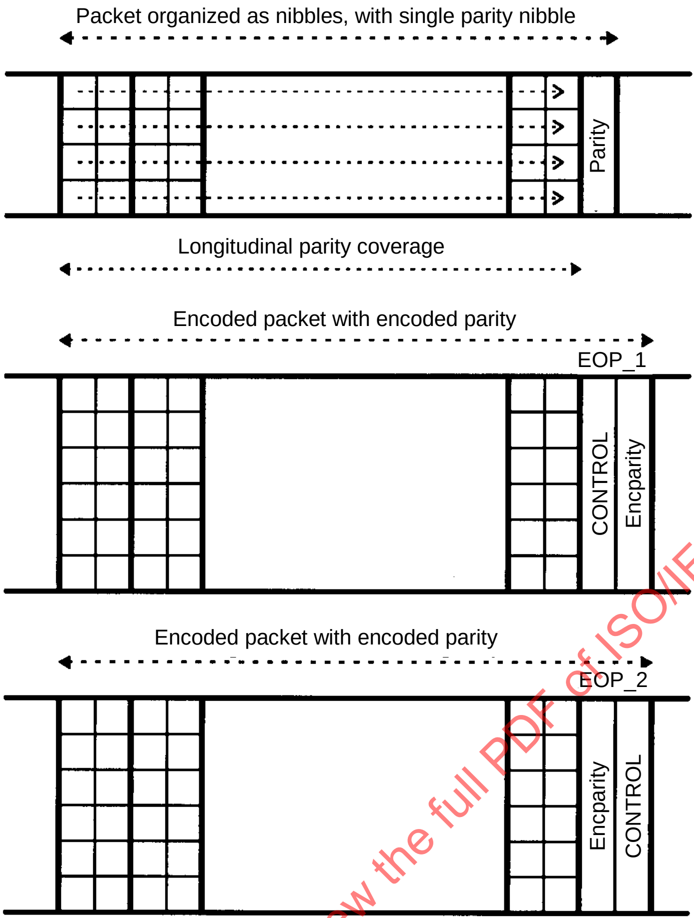


Figure 23 – TS-FO packet encoding

6.4.4.3 Character level checks

All characters shall be checked. Any illegal character that is not otherwise reported as being a symbol or synchronization error shall result in immediate link reset.

6.4.4.4 Bit-level checks and synchronization

Once the receiver has established character boundaries, it should stay in synchronization with these character boundaries thereafter. If a control character is received that is not in synchronism, an error has occurred.

The INIT, NULL and FCC characters all have at least nine alternating bits, whereas the longest length of alternating bits possible with data characters is eight. If a count is detected, therefore, of nine alternating bits, there should be exactly three more bits to make the character; if there are more or fewer bits to the character boundary, synchronization has been lost.

6.4.4.5 Recovery of character synchronization

On loss of character synchronization, the receiver shall disconnect and reinitialize, or shall attempt to resynchronize with the new timing. In either case, the (part) packet immediately preceding the loss of synchronization shall be discarded. If the receiver attempts to resynchronize without reinitializing, the (part) packets received until after synchronization has been reestablished shall also be discarded. The receiver shall not set itself into synchronization until it has received at least two control characters with the same character boundary.

7 HS-SE-10

7.1 HS-SE physical medium

7.1.1 General electrical characteristics

7.1.1.1 Characteristic impedance

The characteristic impedance of the complete transmission line from the serial output buffer to the serial input buffer shall be 50 Ω ± 10 %.

7.1.1.2 Other characteristics

Other characteristics are given in table 33.

Table 33 – HS-SE-10 links general characteristics

Characteristic	Value	
	Min.	Max.
Crosstalk	–	5 %
ESD susceptibility	12 kV	–
Sector noise	1 kV	–
E field	3 V/m	–

A system built using HS-SE links shall meet CISPR limits concerning electromagnetic emissions.

7.1.2 Printed circuit board (PCB)

A PCB track carrying HS-SE signals shall have the characteristics given in table 34.

Table 34 – PCB track characteristics

Characteristic	Value
Characteristic impedance at 1 GHz	50 Ω ± 10 %
Crosstalk between adjacent tracks	2 %

The maximum recommended bend angle is 120°.

7.1.3 Single minicoaxial cable

This subclause describes the basic characteristics of a single minicoaxial cable.

7.1.3.1 Physical

The physical characteristics of a single minicoaxial cable shall be as in table 35.

Table 35 – Physical characteristics of a single coaxial cable

Characteristic	Value
Central conductor size	AWG 22
External diameter	2.85 mm maximum

These characteristics are needed in order to be compatible with the coaxial contact.

7.1.3.2 Electrical

The electrical characteristics of a single minicoaxial cable shall be as in table 36.

Table 36 – Electrical characteristics of a single coaxial cable

Characteristic	Value
Characteristic impedance	50 Ω ± 10 %

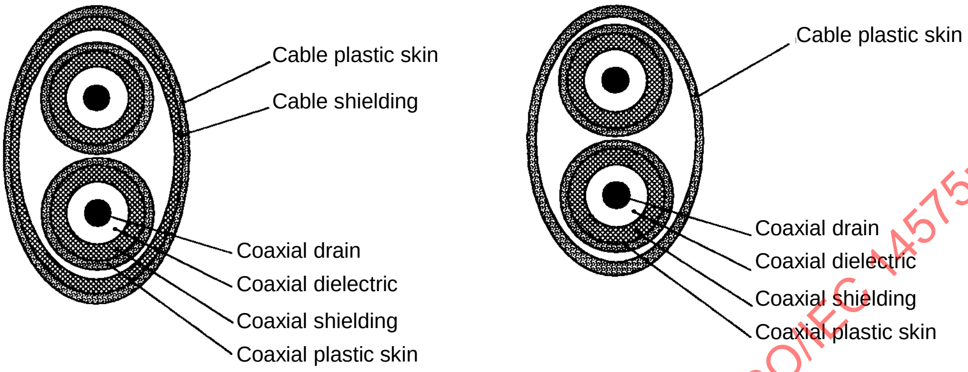
7.1.4 Link cable

7.1.4.1 General

The basic bidirectional HS link cable contains two coaxial cables (one for each direction), and is referred to as "single-link" cable. All the individual coaxial cables in a link cable shall conform to the characteristics described above.

7.1.4.2 Shielding

A link cable may be shielded or unshielded (double braid or single braid respectively; see figure 24). Double braiding may be used in order to comply with the EMC specifications and to protect the transmission line from external noise sources. Link cables supplied for use outside a box shall be shielded. Link cables for use inside a box may be shielded.



a) Shielded (double braid) link cable

b) Unshielded (single braid) link cable

Figure 24 – Single braid and double braid link cables

A recommendation for the shielded cable is given in annex P.

The link cable shall be clearly marked "ISO/IEC 14575 HS-SE Link Cable (shielded)" or "ISO/IEC 14575 HS-SE Link Cable (unshielded)" as appropriate.

7.1.4.3 Mechanical performance

Link cables shall have mechanical performance and safety certification as given in table 37.

Table 37 – Mechanical performance and safety certification of link cables

Mechanical performance		
Characteristic	Value (shielded)	Value (unshielded)
Minimum bending radius (static operation)	30 mm	30 mm
Safety certification		
For cables up to 3 m (10 ft) in the US	UL listing: AWM style 20276, 80C, 30 V, VW1	
For cables 3 m (10 ft) to 100 m	UL listed class 2 power limited circuit cable (CL2)	

7.1.5 Link connectors

7.1.5.1 General

The connector system consists of a cable-mounted free connector; and a PCB-mounted through-panel fixed connector. It provides the following features:

a) A single link connection per connector

b) Option for multiple connections on the cable connector

c) Complete screening

d) Robust

e) Latch fixing (screw fixing may be used as an option)

f) Small size

The connectors and coaxial contacts shall be as specified in IEC 61076-4-107. See annex B.

The connector at either end of the single link cable shall be connected to the central conductors of the two coaxial cables in the cable in such a way as to connect pin a in one connector with pin b in the other connector, and vice versa, i.e. as shown in figure 25.

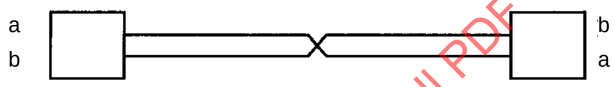


Figure 25 – HS-SE cable pins/connectors wiring

Note that the effect of the cable/connector assembly is to provide a single twist. Any extension adapters allowing multiple segments of cables to be used shall also provide such a twist, so that the effect of any such cable/adapter/cable combination is to provide a single twist, as illustrated in figure 26.

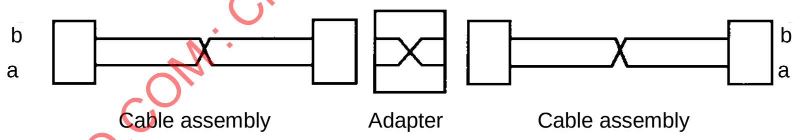


Figure 26 – HS-SE extension adapter

The allocation of signals to the connector pins shall be as given in table 38 (which is oriented to correspond to the external view of the through-panel (fixed) connector when mounted on the upper surface of a horizontal PCB; see figure 27). The direction of the signals is relative to the through-panel (fixed) adapter.

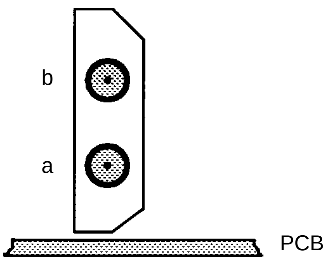


Figure 27 – HS-SE fixed connector external view

Table 38 – Pin allocation of HS-SE connector

b	HS_SE_in
a	HS_SE_out

In addition to the interface specification of IEC 61076-4-107, the connectors shall have the properties described in table 39.

Table 39 – HS-SE environmental constraints

Characteristic	Specification
Modularity	Fixed connector modules shall be placed on a 6 mm pitch, or their centerlines separated by more than 12 mm
Connector width	5.9 mm maximum

Annex O provides a recommendation for the PCB layout for the fixed connector.

7.1.6 Environmental constraints

The environmental requirements for the HS-SE link cables and connectors are application dependent. However, as a minimum, the cables and connectors shall meet the constraints in table 40. Note that specific applications may have requirements for extended temperature range, or other environmental parameters.

Table 40 – HS-SE environmental constraints

Parameter	Value
Operating temperature	–10 °C to +60 °C
Non-operating temperature	–40 °C to +85 °C

7.2 HS-SE signal level

7.2.1 General

HS-SE-10 signal levels are single ended. A HS-SE link shall operate in the ranges given in table 41.

Table 41 – Operating rates for HS-SE-10 links

Characteristic	Value
Operating signalling speed	700 MBd to 1 GBd
Bit period	1.428 ns to 1 ns
Maximum rise and fall time at the transmitter (10 % – 90 %)	300 ps
Minimum rise and fall time at the transmitter (10 % – 90 %)	100 ps

The electrical model of the link input and output buffers is shown in figure 28.

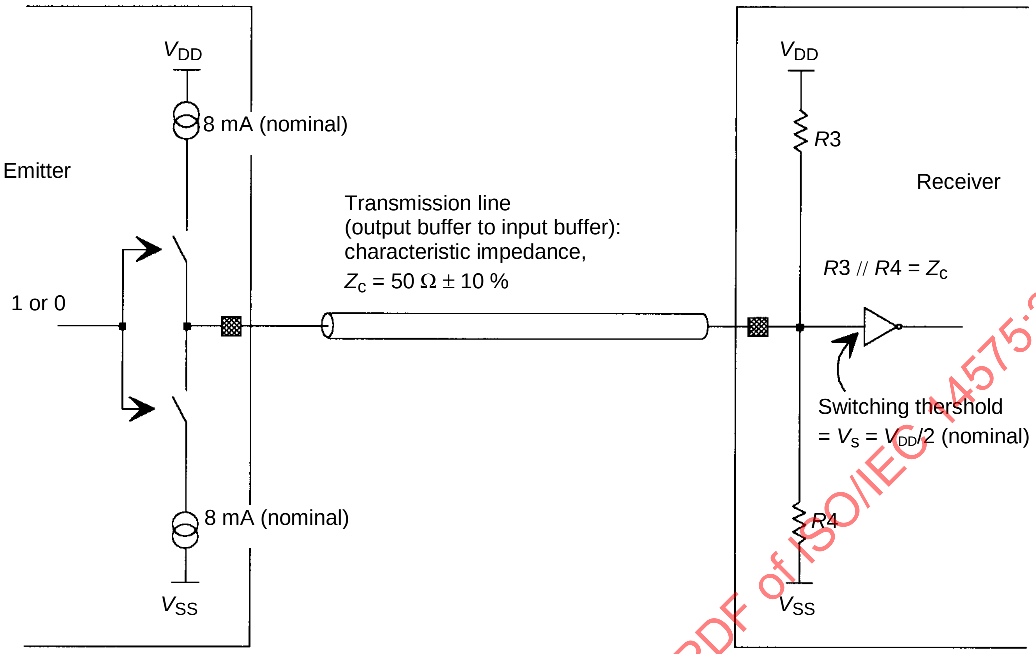


Figure 28 – Input and output buffer electrical model

The receiver amplifier should be polarized around its switching threshold, nominally at $V_{DD}/2$ for a CMOS inverter. This results in a maximum receiver sensitivity. The receiver input impedance (defined by $R3$ // $R4$) shall be 50 Ω ± 10 %.

The driver is modeled by two current sources, pulling the line to logic level 1 or logic level 0 as a function of the bit to be sent. The nominal signal levels corresponding to these logic levels are as follows:

$$V_S = \text{threshold voltage of the receiver amplitude} \approx \frac{V_{DD}}{2}$$

and

$$(V_S - V_L) = (V_H - V_S) \approx 400 \text{ mV}$$

where

V_L is voltage level corresponding to logic level 0 on the line

V_H is voltage level corresponding to logic level 1 on the line

and

$$R3 // R4 = Z_c$$

where

Z_c is characteristic impedance of the transmission line (50 W)

7.2.2 Attenuation budget

The total attenuation for each of the HS-SE signals (from output of the driver to input of the receiver) shall be less than or equal to 7.6 dB at 500 MHz. This attenuation shall be divided following the guidelines given in table 42.

Table 42 – Attribution of attenuation budget

Parameter	Maximum attenuation (dB)
Output of driver to output of connector	0.8
Across cable	6
Input to connector and input of receiver	0.8

7.2.3 Line signal levels driver side

Owing to the nature of the line signal levels, the latter should be observed via a high impedance probe on a fully connected line. For observation purposes at the driver side of the line, the line loss of the transmission medium shall be less than 0.5 dB. The levels shall meet the requirements shown in table 43 or V_{DD} = 3.3 V (nominal) and table 44 for V_{DD} = 5.0 V (nominal).

Table 43 – Driver side line logic levels for V_{DD} = 3.3 V (nominal)

Symbol	Parameter	Units	Min.	Typ	Max.
V_{OLS}	Serial output low level	V	1.15	1.25	1.35
V_{OHS}	Serial output high level	V	1.95	2.05	2.15

Table 44 – Driver side line logic levels for V_{DD} = 5.0 V (nominal)

Symbol	Parameter	Units	Min.	Typ	Max.
V_{OLS}	Serial output low level	V	2.0	2.1	2.2
V_{OHS}	Serial output high level	V	2.8	2.9	3.0

Alternatively, the output of the driver may be a.c. coupled (see below) directly into the 50 Ω termination of an oscilloscope. This allows measurement of the line swing only (as d.c. levels are masked by the a.c. coupling). The swings shall meet the requirements shown in table 45.

Table 45 – Driver side line swing when a.c. coupled into 50 Ω termination

Symbol	Parameter	Units	Min.	Typ	Max.
V_{SW}	Serial line swing	V	0.6	0.8	1.0

7.2.4 AC coupling of the link

The HS Link 8B/12B coding scheme is d.c. balanced, with a maximum disparity of 8 b. This d.c. balance allows the code to be transmitted across a.c. coupled links, which is advantageous for both fiber and coaxial cable systems. Therefore the HS-SE-10 links using such media should be a.c. coupled.

If the a.c. coupling poles are too high in frequency, long strings of 1s or 0s will distort and degrade the opening of the data eye. This distortion is called baseline wander. In order for the baseline wander to degrade the eye opening by less than 4 % of the total, the a.c. coupling needs to follow the following guidelines:

a) If the node (transmit or receive) has a single dominant a.c. coupling pole in series, the pole frequency shall be 800 kHz or lower.

b) If the node (transmit or receive) has two equal a.c. coupling pole in series, the pole frequency shall be 400 kHz or lower.

Transformer coupling or capacitive coupling may be used.

Because of static electricity considerations, it is undesirable to leave the cable conductors completely isolated from ground. A bleeder resistor (10 MΩ) should be included.

For HS Links that operate between two components on the same PCB (i.e. using only PCB tracks), a.c. coupling may be used, but is less essential.

7.2.5 Receiver electrical

The receiver shall meet the electrical characteristics given in table 46.

Table 46 – Receiver electrical characteristics

Characteristic	Value
Minimum sensitivity	250 mV
Maximum input voltage	1 200 mV peak-to-peak
Minimum discrete connector return loss	20 dB

7.2.6 EM susceptibility

A system using HS-SE links shall meet or exceed IEC 61000-4-4 specifications on EM susceptibility as a function of the intended operating environment.

7.3 HS character level (8B/12B code)

7.3.1 General

The HS-SE-10 uses an 8B/12B d.c. balanced code. This code provides the following features.

a) A positive going synchronization transition at the beginning of every character, to simplify clock recovery.

b) An odd parity bit per character, enabling the detection of single bit errors.

c) DC balance, with a maximum disparity of 8 b.

d) Out-of-bound control characters.

7.3.2 Transmission characters

Define d[7:0] to be the byte to be transmitted, where d[7] is the most significant bit. To each byte, an odd parity, AP, and an inversion bit, I, are added to form the encoded character (on 10 b). The transmission character (on 12 b) is the encoded character plus the Start (1) and Stop (0) bits that provide the positive going synchronization transition.

The transmission character therefore has the form:

Start ('1') AP e[0] e[1] e[2] e[3] e[4] e[5] e[6] e[7] Invert, I Stop ('0')

where

e[7:0] is d[7:0] or d[7:0], as defined in 7.3.3.

On the serial line the bits shall be sent in the order Start to Stop ([0] = LSB).

The AP bit is defined as follows:

AP is 1 if there is an even number of 1s in e[7:0] and I

AP is 0 if there is an odd number of 1s in e[7:0] and I

7.3.3 DC balance

A code that is d.c. balanced is one that has a constant d.c. component regardless of the data pattern. This provides many advantages for high data rate transmission on fibre optic and long distance copper media.

Assigning +1 and –1 to bit levels 1 and 0 respectively provides a measure of the d.c. component in each transmitted character. The disparity, D, of a data word is the difference between the number of 1s and the number of 0s in the word-positive and negative disparities refer to an excess of 1s and 0s respectively. The running disparity, RD, is the running (cumulative) sum of the disparities of all previous characters. In a code that is "ideally" d.c. balanced each transmitted character has a D = 0 and thus RD is always equal to 0. However, perfect d.c. balance is not required in practice.

To maintain d.c. balance, a non-zero RD has always to tend towards zero. For each character to be sent, the following algorithm is used: calculate the disparity D of the encoded character (since the Start and Stop bits are 1 and 0 respectively, they do not affect the disparity) with I = 0. If the result will reduce the absolute value of RD, then transmit the character as it is (i.e. e[7:0] = d[7:0], I = 0). If the result will increase the absolute value of RD, then invert the encoded character and set I = 1 (i.e. e[7:0] = d[7:0], I = 1), so that the inverted character reduces or leaves unchanged the absolute value of RD. The receiver uses the bit I to determine whether the character has been inverted or not. By its definition, the AP is also inverted if d[7:0] and I are inverted. In summary:

If RD ≤ 0 and D > 0 then I = 0, e[7:0] = d[7:0] (character non-inverted)

If RD < 0 and D ≤ 0 then I = 1, e[7:0] = d[7:0] (character inverted)

If RD ≥ 0 and D < 0 then I = 0, e[7:0] = d[7:0] (character non-inverted)

If RD > 0 and D ≥ 0

then I = 1, e[7:0] = d[7:0] (character inverted)

If RD = 0 and D = 0 then I = 1, e[7:0] = d[7:0] (character inverted)

7.3.4 Control characters

When the disparity of the encoded character is zero it does not effect the RD, and can therefore be transmitted either non-inverted or inverted. This property enables the transmission of control characters. As defined above, if D = 0, the character is transmitted inverted. Control characters are therefore defined as characters that have D = 0 but are transmitted non-inverted. This gives 126 possible control characters.

7.3.5 The code

Table 47 details the 256 data characters, giving the decimal value, the binary value, the transmission character and the disparity. For data characters which have a $D \neq 0$, the non-inverted (first row) and inverted forms (second row) of the character is shown. Note that D can take the values 0, ±4 and ±8 only.

Table 48 details the 126 control characters, giving the control character ID (0 to 125), the decimal value, the binary value, and the transmission character (the disparity being zero and the character being non-inverted).

Table 47 – Data characters

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
0	00000000	1 1 000000000 0	–8
		1 0 111111111 0	8
1	10000000	1 0 100000000 0	–8
		1 1 011111111 0	8
2	01000000	1 0 010000000 0	–8
		1 1 101111111 0	8
3	11000000	1 1 110000000 0	–4
		1 0 001111111 0	4
4	00100000	1 0 001000000 0	–8
		1 1 110111111 0	8
5	10100000	1 1 101000000 0	–4
		1 0 010111111 0	4
6	01100000	1 1 011000000 0	–4
		1 0 100111111 0	4
7	11100000	1 0 111000000 0	–4
		1 1 000111111 0	4
8	00010000	1 0 000100000 0	–8
		1 1 111011111 0	8
9	10010000	1 1 100100000 0	–4
		1 0 011011111 0	4
10	01010000	1 1 010100000 0	–4
		1 0 101011111 0	4
11	11010000	1 0 110100000 0	–4
		1 1 001011111 0	4
12	00110000	1 1 001100000 0	–4
		1 0 110011111 0	4
13	10110000	1 0 101100000 0	–4
		1 1 010011111 0	4
14	01110000	1 0 011100000 0	–4
		1 1 100011111 0	4
15	11110000	1 0 000011111 0	0
16	00001000	1 0 000010000 0	–8
		1 1 111101111 0	8
17	10001000	1 1 100010000 0	–4
		1 0 011101111 0	4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
18	01001000	1 1 010010000 0	–4
		1 0 101101111 0	4
19	11001000	1 0 110010000 0	–4
		1 1 001101111 0	4
20	00101000	1 1 001010000 0	–4
		1 0 110101111 0	4
21	10101000	1 0 101010000 0	–4
		1 1 010101111 0	4
22	01101000	1 0 011010000 0	–4
		1 1 100101111 0	4
23	11101000	1 0 000101111 0	0
24	00011000	1 1 000110000 0	–4
		1 0 111001111 0	4
25	10011000	1 0 100110000 0	–4
		1 1 011001111 0	4
26	01011000	1 0 010110000 0	–4
		1 1 101001111 0	4
27	11011000	1 0 001001111 0	0
28	00111000	1 0 001110000 0	–4
		1 1 110001111 0	4
29	10111000	1 0 010001111 0	0
30	01111000	1 0 100001111 0	0
31	11111000	1 1 000001111 0	0
32	00000100	1 0 000001000 0	–8
		1 1 111110111 0	8
33	10000100	1 1 100001000 0	–4
		1 0 011110111 0	4
34	01000100	1 1 010001000 0	–4
		1 0 101110111 0	4
35	11000100	1 0 110001000 0	–4
		1 1 001110111 0	4
36	00100100	1 1 001001000 0	–4
		1 0 110110111 0	4
37	10100100	1 0 101001000 0	–4
		1 1 010110111 0	4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
38	01100100	1 0 011001000 0	–4
		1 1 100110111 0	4
39	11100100	1 0 000110111 0	0
40	00010100	1 1 000101000 0	–4
		1 0 111010111 0	4
41	10010100	1 0 100101000 0	–4
		1 1 011010111 0	4
42	01010100	1 0 010101000 0	–4
		1 1 101010111 0	4
43	11010100	1 0 001010111 0	0
44	00110100	1 0 001101000 0	–4
		1 1 110010111 0	4
45	10110100	1 0 010010111 0	0
46	01110100	1 0 100010111 0	0
47	11110100	1 1 000010111 0	0
48	00001100	1 1 000011000 0	–4
		1 0 111100111 0	4
49	10001100	1 0 100011000 0	–4
		1 1 011100111 0	4
50	01001100	1 0 010011000 0	–4
		1 1 101100111 0	4
51	11001100	1 0 001100111 0	0
52	00101100	1 0 001011000 0	–4
		1 1 110100111 0	4
53	10101100	1 0 010100111 0	0
54	01101100	1 0 100100111 0	0
55	11101100	1 1 000100111 0	0
56	00011100	1 0 000111000 0	–4
		1 1 111000111 0	4
57	10011100	1 0 011000111 0	0
58	01011100	1 0 101000111 0	0
59	11011100	1 1 001000111 0	0
60	00111100	1 0 110000111 0	0
61	10111100	1 1 010000111 0	0
62	01111100	1 1 100000111 0	0

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
63	11111100	1 1 111111000 0	4
		1 0 000000111 0	–4
64	00000010	1 0 000000100 0	–8
		1 1 111111011 0	8
65	10000010	1 1 100000100 0	–4
		1 0 011111011 0	4
66	01000010	1 1 010000100 0	–4
		1 0 101111011 0	4
67	11000010	1 0 110000100 0	–4
		1 1 001111011 0	4
68	00100010	1 1 001000100 0	–4
		1 0 110111011 0	4
69	10100010	1 0 101000100 0	–4
		1 1 010111011 0	4
70	01100010	1 0 011000100 0	–4
		1 1 100111011 0	4
71	11100010	1 0 000111011 0	0
72	00010010	1 1 000100100 0	–4
		1 0 111011011 0	4
73	10010010	1 0 100100100 0	–4
		1 1 011011011 0	4
74	01010010	1 0 010100100 0	–4
		1 1 101011011 0	4
75	11010010	1 0 001011011 0	0
76	00110010	1 0 001100100 0	–4
		1 1 110011011 0	4
77	10110010	1 0 010011011 0	0
78	01110010	1 0 100011011 0	0
79	11110010	1 1 000011011 0	0
80	00001010	1 1 000010100 0	–4
		1 0 111101011 0	4
81	10001010	1 0 100010100 0	–4
		1 1 011101011 0	4
82	01001010	1 0 010010100 0	–4
		1 1 101101011 0	4
83	11001010	1 0 001101011 0	0

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
84	00101010	1 0 001010100 0	–4
		1 1 110101011 0	4
85	10101010	1 0 010101011 0	0
86	01101010	1 0 100101011 0	0
87	11101010	1 1 000101011 0	0
88	00011010	1 0 000110100 0	–4
		1 1 111001011 0	4
89	10011010	1 0 011001011 0	0
90	01011010	1 0 101001011 0	0
91	11011010	1 1 001001011 0	0
92	00111010	1 0 110001011 0	0
93	10111010	1 1 010001011 0	0
94	01111010	1 1 100001011 0	0
95	11111010	1 1 111110100 0	4
		1 0 000001011 0	–4
96	00000110	1 1 000001100 0	–4
		1 0 111110011 0	4
97	10000110	1 0 100001100 0	–4
		1 1 011110011 0	4
98	01000110	1 0 010001100 0	–4
		1 1 101110011 0	4
99	11000110	1 0 001110011 0	0
100	00100110	1 0 001001100 0	–4
		1 1 110110011 0	4
101	10100110	1 0 010110011 0	0
102	01100110	1 0 100110011 0	0
103	11100110	1 1 000110011 0	0
104	00010110	1 0 000101100 0	–4
		1 1 111010011 0	4
105	10010110	1 0 011010011 0	0
106	01010110	1 0 101010011 0	0
107	11010110	1 1 001010011 0	0
108	00110110	1 0 110010011 0	0
109	10110110	1 1 010010011 0	0
110	01110110	1 1 100010011 0	0
111	11110110	1 1 111101100 0	4
		1 0 000010011 0	–4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
112	00001110	1 0 000011100 0	–4
		1 1 111100011 0	4
113	10001110	1 0 011100011 0	0
114	01001110	1 0 101100011 0	0
115	11001110	1 1 001100011 0	0
116	00101110	1 0 110100011 0	0
117	10101110	1 1 010100011 0	0
118	01101110	1 1 100100011 0	0
119	11101110	1 1 111011100 0	4
		1 0 000100011 0	–4
120	00011110	1 0 111000011 0	0
121	10011110	1 1 011000011 0	0
122	01011110	1 1 101000011 0	0
123	11011110	1 1 110111100 0	4
		1 0 001000011 0	–4
124	00111110	1 1 110000011 0	0
125	10111110	1 1 101111100 0	4
		1 0 010000011 0	–4
126	01111110	1 1 011111100 0	4
		1 0 100000011 0	–4
127	11111110	1 0 111111100 0	4
		1 1 000000011 0	–4
128	00000001	1 0 000000010 0	–8
		1 1 111111101 0	8
129	10000001	1 1 100000010 0	–4
		1 0 011111101 0	4
130	01000001	1 1 010000010 0	–4
		1 0 101111101 0	4
131	11000001	1 0 110000010 0	–4
		1 1 001111101 0	4
132	00100001	1 1 001000010 0	–4
		1 0 110111101 0	4
133	10100001	1 0 101000010 0	–4
		1 1 010111101 0	4
134	01100001	1 0 011000010 0	–4
		1 1 100111101 0	4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
135	11100001	1 0 000111101 0	0
136	00010001	1 1 000100010 0	–4
		1 0 111011101 0	4
137	10010001	1 0 100100010 0	–4
		1 1 011011101 0	4
138	01010001	1 0 010100010 0	–4
		1 1 101011101 0	4
139	11010001	1 0 001011101 0	0
140	00110001	1 0 001100010 0	–4
		1 1 110011101 0	4
141	10110001	1 0 010011101 0	0
142	01110001	1 0 100011101 0	0
143	11110001	1 1 000011101 0	0
144	00001001	1 1 000010010 0	–4
		1 0 111101101 0	4
145	10001001	1 0 100010010 0	–4
		1 1 011101101 0	4
146	01001001	1 0 010010010 0	–4
		1 1 101101101 0	4
147	11001001	1 0 001101101 0	0
148	00101001	1 0 001010010 0	–4
		1 1 110101101 0	4
149	10101001	1 0 010101101 0	0
150	01101001	1 0 100101101 0	0
151	11101001	1 1 000101101 0	0
152	00011001	1 0 000110010 0	–4
		1 1 111001101 0	4
153	10011001	1 0 011001101 0	0
154	01011001	1 0 101001101 0	0
155	11011001	1 1 001001101 0	0
156	00111001	1 0 110001101 0	0
157	10111001	1 1 010001101 0	0
158	01111001	1 1 100001101 0	0
159	11111001	1 1 111110010 0	4
		1 0 000001101 0	–4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
160	00000101	1 1 000001010 0	–4
		1 0 111110101 0	4
161	10000101	1 0 100001010 0	–4
		1 1 011110101 0	4
162	01000101	1 0 010001010 0	–4
		1 1 101110101 0	4
163	11000101	1 0 001110101 0	0
164	00100101	1 0 001001010 0	–4
		1 1 110110101 0	4
165	10100101	1 0 010110101 0	0
166	01100101	1 0 100110101 0	0
167	11100101	1 1 000110101 0	0
168	00010101	1 0 000101010 0	–4
		1 1 111010101 0	4
169	10010101	1 0 011010101 0	0
170	01010101	1 0 101010101 0	0
171	11010101	1 1 001010101 0	0
172	00110101	1 0 110010101 0	0
173	10110101	1 1 010010101 0	0
174	01110101	1 1 100010101 0	0
175	11110101	1 1 111101010 0	4
		1 0 000010101 0	–4
176	00001101	1 0 000011010 0	–4
		1 1 111100101 0	4
177	10001101	1 0 011100101 0	0
178	01001101	1 0 101100101 0	0
179	11001101	1 1 001100101 0	0
180	00101101	1 0 110100101 0	0
181	10101101	1 1 010100101 0	0
182	01101101	1 1 100100101 0	0
183	11101101	1 1 111011010 0	4
		1 0 000100101 0	–4
184	00011101	1 0 111000101 0	0
185	10011101	1 1 011000101 0	0
186	01011101	1 1 101000101 0	0
		1 0 010000101 0	–4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
187	11011101	1 1 110111010 0	4
		1 0 001000101 0	–4
188	00111101	1 1 110000101 0	0
189	10111101	1 1 101111010 0	4
		1 0 010000101 0	–4
190	01111101	1 1 011111010 0	4
		1 0 100000101 0	–4
191	11111101	1 0 111111010 0	4
		1 1 000000101 0	–4
192	00000011	1 1 000000110 0	–4
		1 0 111111001 0	4
193	10000011	1 0 100000110 0	–4
		1 1 011111001 0	4
194	01000011	1 0 010000110 0	–4
		1 1 101111001 0	4
195	11000011	1 0 001111001 0	0
196	00100011	1 0 001000110 0	–4
		1 1 110111001 0	4
197	10100011	1 0 010111001 0	0
198	01100011	1 0 100111001 0	0
199	11100011	1 1 000111001 0	0
200	00010011	1 0 000100110 0	–4
		1 1 111011001 0	4
201	10010011	1 0 011011001 0	0
202	01010011	1 0 101011001 0	0
203	11010011	1 1 001011001 0	0
204	00110011	1 0 110011001 0	0
205	10110011	1 1 010011001 0	0
206	01110011	1 1 100011001 0	0
207	11110011	1 1 111100110 0	4
		1 0 000011001 0	–4
208	00001011	1 0 000010110 0	–4
		1 1 111101001 0	4
209	10001011	1 0 011101001 0	0
210	01001011	1 0 101101001 0	0
211	11001011	1 1 001101001 0	0

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
212	00101011	1 0 110101001 0	0
213	10101011	1 1 010101001 0	0
214	01101011	1 1 100101001 0	0
215	11101011	1 1 111010110 0	4
		1 0 000101001 0	–4
216	00011011	1 0 111001001 0	0
217	10011011	1 1 011001001 0	0
218	01011011	1 1 101001001 0	0
219	11011011	1 1 110110110 0	–4
		1 0 001001001 0	4
220	00111011	1 1 110001001 0	0
221	10111011	1 1 101110110 0	4
		1 0 010001001 0	–4
222	01111011	1 1 011110110 0	4
		1 0 100001001 0	–4
223	11111011	1 0 111110110 0	4
		1 1 000001001 0	–4
224	00000111	1 0 000001110 0	–4
		1 1 111110001 0	4
225	10000111	1 0 011110001 0	0
226	01000111	1 0 101110001 0	0
227	11000111	1 1 001110001 0	0
228	00100111	1 0 110110001 0	0
229	10100111	1 1 010110001 0	0
230	01100111	1 1 100110001 0	0
231	11100111	1 1 111001110 0	4
		1 0 000110001 0	–4
232	00010111	1 0 111010001 0	0
233	10010111	1 1 011010001 0	0
234	01010111	1 1 101010001 0	0
235	11010111	1 1 110101110 0	4
		1 0 001010001 0	–4
236	00110111	1 1 110010001 0	0
237	10110111	1 1 101101110 0	4
		1 0 010010001 0	–4

Table 47 *(continued)*

Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S	D
238	01110111	1 1 011101110 0	4
		1 0 100010001 0	4
239	11110111	1 0 111101110 0	4
		1 1 000010001 0	–4
240	00001111	1 0 111100001 0	0
241	10001111	1 1 011100001 0	0
242	01001111	1 1 101100001 0	0
243	11001111	1 1 110011110 0	4
		1 0 001100001 0	–4
244	00101111	1 1 110100001 0	0
245	10101111	1 1 101011110 0	4
		1 0 010100001 0	–4
246	01101111	1 1 011011110 0	4
		1 0 100100001 0	–4
247	11101111	1 0 111011110 0	4
		1 1 000100001 0	–4
248	00011111	1 1 111000001 0	0
249	10011111	1 1 100111110 0	4
		1 0 011000001 0	4
250	01011111	1 1 010111110 0	4
		1 0 101000001 0	4
251	11011111	1 0 110111110 0	4
		1 1 001000001 0	4
252	00111111	1 1 001111110 0	4
		1 0 110000001 0	4
253	10111111	1 0 101111110 0	4
		1 1 010000001 0	4
254	01111111	1 0 011111110 0	4
		1 1 100000001 0	4
255	11111111	1 1 111111110 0	8
		1 0 000000001 0	8

Table 48 – Control characters

ID	Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S
0	15	11110000	1 1 11110000 0 0
1	23	11101000	1 1 11101000 0 0
2	27	11011000	1 1 11011000 0 0
3	29	10111000	1 1 10111000 0 0
4	30	01111000	1 1 01111000 0 0
5	31	11111000	1 0 11111000 0 0
6	39	11100100	1 1 11100100 0 0
7	43	11010100	1 1 11010100 0 0
8	45	10110100	1 1 10110100 0 0
9	46	01110100	1 1 01110100 0 0
10	47	11110100	1 0 11110100 0 0
11	51	11001100	1 1 11001100 0 0
12	53	10101100	1 1 10101100 0 0
13	54	01101100	1 1 01101100 0 0
14	55	11101100	1 0 11101100 0 0
15	57	10011100	1 1 10011100 0 0
16	58	01011100	1 1 01011100 0 0
17	59	11011100	1 0 11011100 0 0
18	60	00111100	1 1 00111100 0 0
19	61	10111100	1 0 10111100 0 0
20	62	01111100	1 0 01111100 0 0
21	71	11100010	1 1 11100010 0 0
22	75	11010010	1 1 11010010 0 0
23	77	10110010	1 1 10110010 0 0
24	78	01110010	1 1 01110010 0 0
25	79	11110010	1 0 11110010 0 0
26	83	11001010	1 1 11001010 0 0
27	85	10101010	1 1 10101010 0 0
28	86	01101010	1 1 01101010 0 0
29	87	11101010	1 0 11101010 0 0
30	89	10011010	1 1 10011010 0 0
31	90	01011010	1 1 01011010 0 0
32	91	11011010	1 0 11011010 0 0
33	92	00111010	1 1 00111010 0 0
34	93	10111010	1 0 10111010 0 0

Table 48 *(continued)*

ID	Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S
35	94	01111010	1 0 01111010 0 0
36	99	11000110	1 1 11000110 0 0
37	101	10100110	1 1 10100110 0 0
38	102	01100110	1 1 01100110 0 0
39	103	11100110	1 0 11100110 0 0
40	105	10010110	1 1 10010110 0 0
41	106	01010110	1 1 01010110 0 0
42	107	11010110	1 0 11010110 0 0
43	108	00110110	1 1 00110110 0 0
44	109	10110110	1 0 10110110 0 0
45	110	01110110	1 0 01110110 0 0
46	113	10001110	1 1 10001110 0 0
47	114	01001110	1 1 01001110 0 0
48	115	11001110	1 0 11001110 0 0
49	116	00101110	1 1 00101110 0 0
50	117	10101110	1 0 10101110 0 0
51	118	01101110	1 0 01101110 0 0
52	120	00011110	1 1 00011110 0 0
53	121	10011110	1 0 10011110 0 0
54	122	01011110	1 0 01011110 0 0
55	124	00111110	1 0 00111110 0 0
56	135	11100001	1 1 11100001 0 0
57	139	11010001	1 1 11010001 0 0
58	141	10110001	1 1 10110001 0 0
59	142	01110001	1 1 01110001 0 0
60	143	11110001	1 0 11110001 0 0
61	147	11001001	1 1 11001001 0 0
62	149	10101001	1 1 10101001 0 0
63	150	01101001	1 1 01101001 0 0
64	151	11101001	1 0 11101001 0 0
65	153	10011001	1 1 10011001 0 0
66	154	01011001	1 1 01011001 0 0
67	155	11011001	1 0 11011001 0 0
68	156	00111001	1 1 00111001 0 0
69	157	10111001	1 0 10111001 0 0
70	158	01111001	1 0 01111001 0 0

Table 48 *(continued)*

ID	Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S
71	163	11000101	1 1 11000101 0 0
72	165	10100101	1 1 10100101 0 0
73	166	01100101	1 1 01100101 0 0
74	167	11100101	1 0 11100101 0 0
75	169	10010101	1 1 10010101 0 0
76	170	01010101	1 1 01010101 0 0
77	171	11010101	1 0 11010101 0 0
78	172	00110101	1 1 00110101 0 0
79	173	10110101	1 0 10110101 0 0
80	174	01110101	1 0 01110101 0 0
81	177	10001101	1 1 10001101 0 0
82	178	01001101	1 1 01001101 0 0
83	179	11001101	1 0 11001101 0 0
84	180	00101101	1 1 00101101 0 0
85	181	10101101	1 0 10101101 0 0
86	182	01101101	1 0 01101101 0 0
87	184	00011101	1 1 00011101 0 0
88	185	10011101	1 0 10011101 0 0
89	186	01011101	1 0 01011101 0 0
90	188	00111101	1 0 00111101 0 0
91	195	11000011	1 1 11000011 0 0
92	197	10100011	1 1 10100011 0 0
93	198	01100011	1 1 01100011 0 0
94	199	11100011	1 0 11100011 0 0
95	201	10010011	1 1 10010011 0 0
96	202	01010011	1 1 01010011 0 0
97	203	11010011	1 0 11010011 0 0
98	204	00110011	1 1 00110011 0 0
99	205	10110011	1 0 10110011 0 0
100	206	01110011	1 0 01110011 0 0
101	209	10001011	1 1 10001011 0 0
102	210	01001011	1 1 01001011 0 0
103	211	11001011	1 0 11001011 0 0
104	212	00101011	1 1 00101011 0 0
105	213	10101011	1 0 10101011 0 0
106	214	01101011	1 0 01101011 0 0

Table 48 *(continued)*

ID	Dec	Bin, d[0:7]	S–AP–e[0:7]-I–S
107	216	00011011	1 1 00011011 0 0
108	217	10011011	1 0 10011011 0 0
109	218	01011011	1 0 01011011 0 0
110	220	00111011	1 0 00111011 0 0
111	225	10000111	1 1 10000111 0 0
112	226	01000111	1 1 01000111 0 0
113	227	11000111	1 0 11000111 0 0
114	228	00100111	1 1 00100111 0 0
115	229	10100111	1 0 10100111 0 0
116	230	01100111	1 0 01100111 0 0
117	232	00010111	1 1 00010111 0 0
118	233	10010111	1 0 10010111 0 0
119	234	01010111	1 0 01010111 0 0
120	236	00110111	1 0 00110111 0 0
121	240	00001111	1 1 00001111 0 0
122	241	10001111	1 0 10001111 0 0
123	242	01001111	1 0 01001111 0 0
124	244	00101111	1 0 00101111 0 0
125	248	00011111	1 0 00011111 0 0

NOTE Shaded control characters indicate that they are defined by the exchange level or by the packet level.

7.4 HS exchange level

7.4.1 General

The exchange level shall perform the following functions that correspond to normal operation of a bidirectional link:

a) Start-up

b) Shutdown

c) Flow control

The exchange level shall perform the following additional functions:

– Parity error detection and recovery

– Receiver calibration loss detection and recovery

– Disconnection detection and recovery

– Reset

All exchange level functions remain invisible to the packet level during normal operation.

The exchange level uses the reserved L_chars detailed in table 49.

Table 49 – Reserved L_chars for exchange level functions

Symbol	Control character ID	Name
IDLE	0	Idle
START_REQ	5	Start request
START_ACK	1	Start acknowledge
STOP_REQ	2	Stop request
STOP_ACK	3	Stop acknowledge
STOP_NACK	4	Stop negative acknowledge
FCC	125	Flow control
RESET	6	Reset

Consider two connected nodes, NODE_A and NODE_B (see figure 29). Each port is divided into two parts: a transmitter and a receiver, referred to as transmitter_A and receiver_A for NODE_A and transmitter_B and receiver_B for NODE_B.

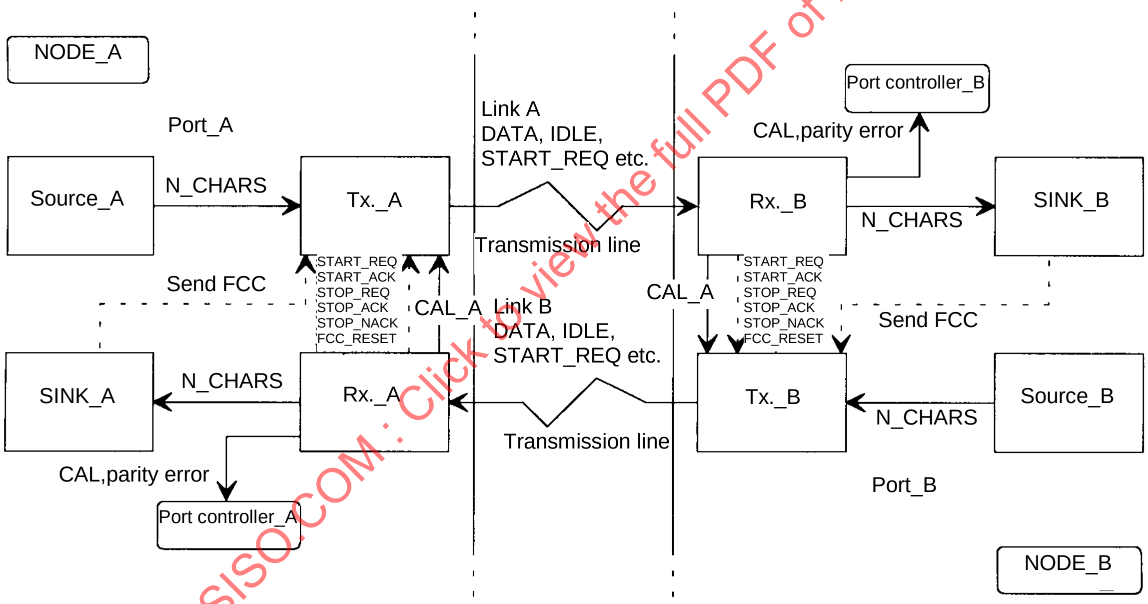


Figure 29 – Exchange level interconnection between two nodes

Each port has a N_char source (SOURCE_A and SOURCE_B) which supply N_chars to transmitter_A and transmitter_B respectively and a N_char sink (SINK_A and SINK_B) which accept data from receiver_A and receiver_B respectively.

Exchange level information (i.e. the L_chars detailed in table 49) generated and sent by, for example, transmitter_A, are received and filtered by the receiver_B and passed directly to transmitter_B (and vice versa). L_chars shall not be generated by the source nor written into the sink.

Each receiver shall have a flag, CAL, which indicates its state. When CAL is low, this indicates that the receiver is not calibrated to the incoming serial data stream. When in this state, all characters shall be filtered by the receiver. When CAL is high, this indicates that the receiver is calibrated to the incoming serial data stream. When in this state, all N_chars shall be passed to the N_char sink and all L_chars shall be passed to the port's transmitter.

Each transmitter and receiver is controlled by a state machine. (See figures 30, 31, 32 and 33).

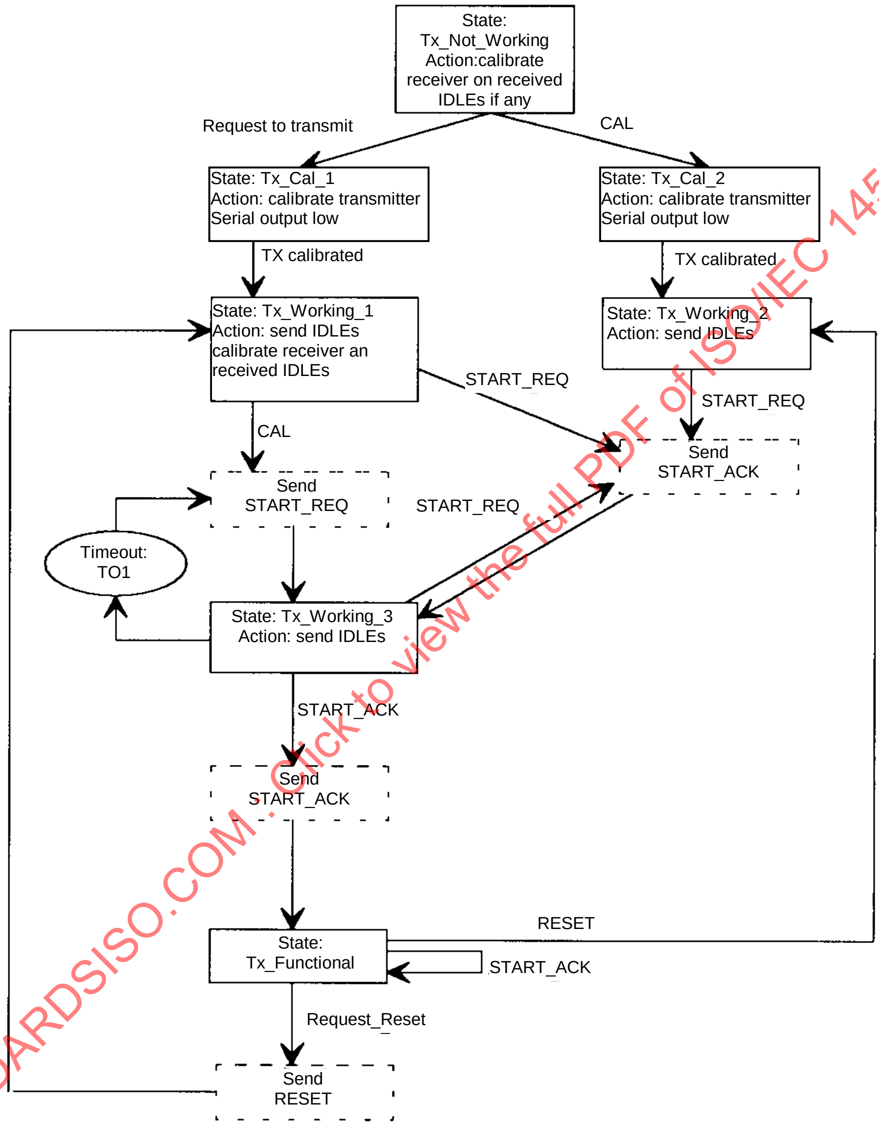


Figure 30 – Transmitter state machine controller-start-up

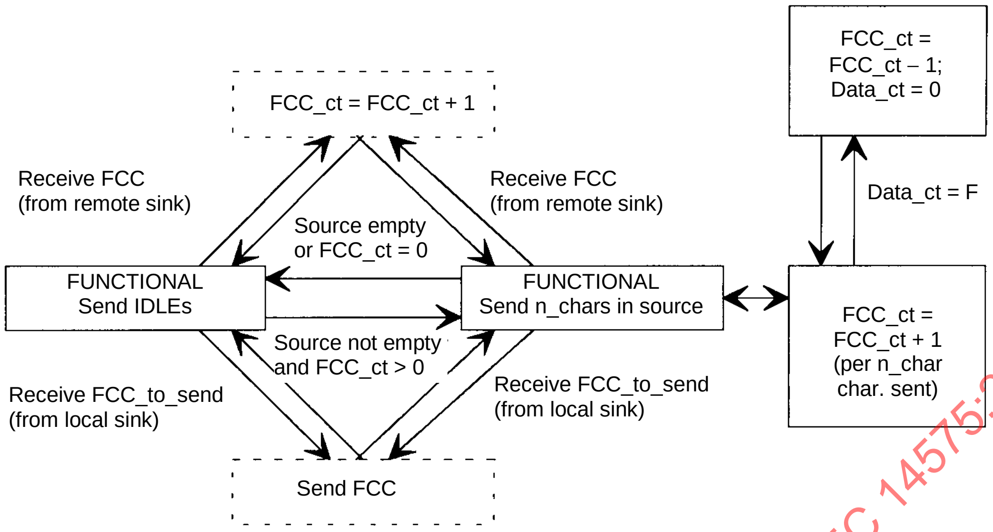


Figure 31 – Transmitter state machine controller-functional

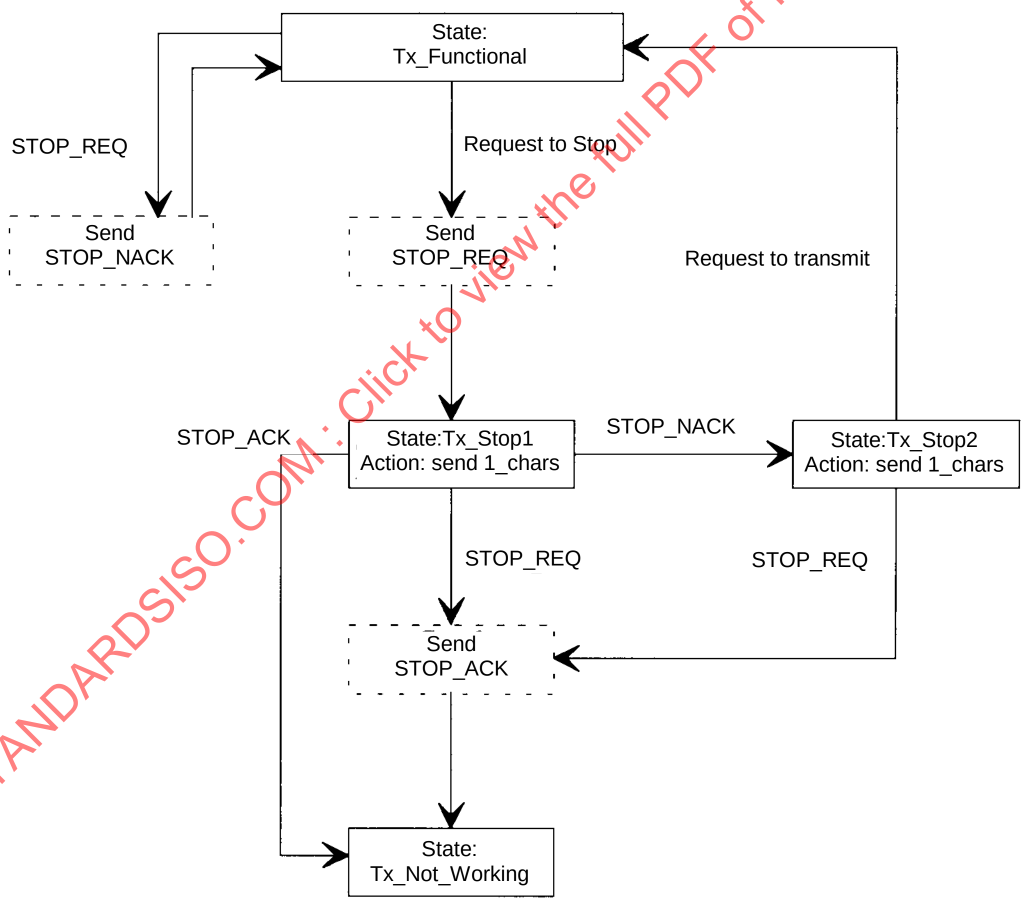


Figure 32 – Transmitter state machine controller-shutdown

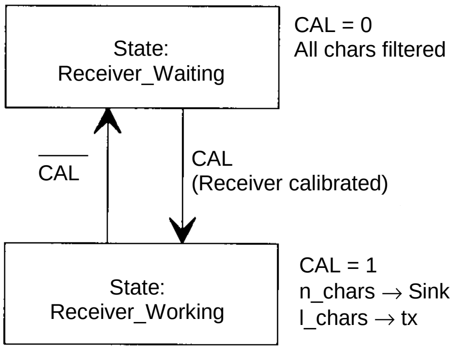


Figure 33 – Receiver state machine controller

7.4.2 Start-up

A request to transmit in one direction automatically activates the complete bidirectional link, this being necessary to allow the exchange level functions. There are two different types of start-up possible:

a) unidirectional;

b) bidirectional.

The start-up procedure uses the L_char IDLE (control character ID = 0) in order to calibrate the receiver. IDLE has the characteristic that the only positive going edges in the character are the synchronization edges. This enables the clock recovery circuit to correctly lock onto these edges.

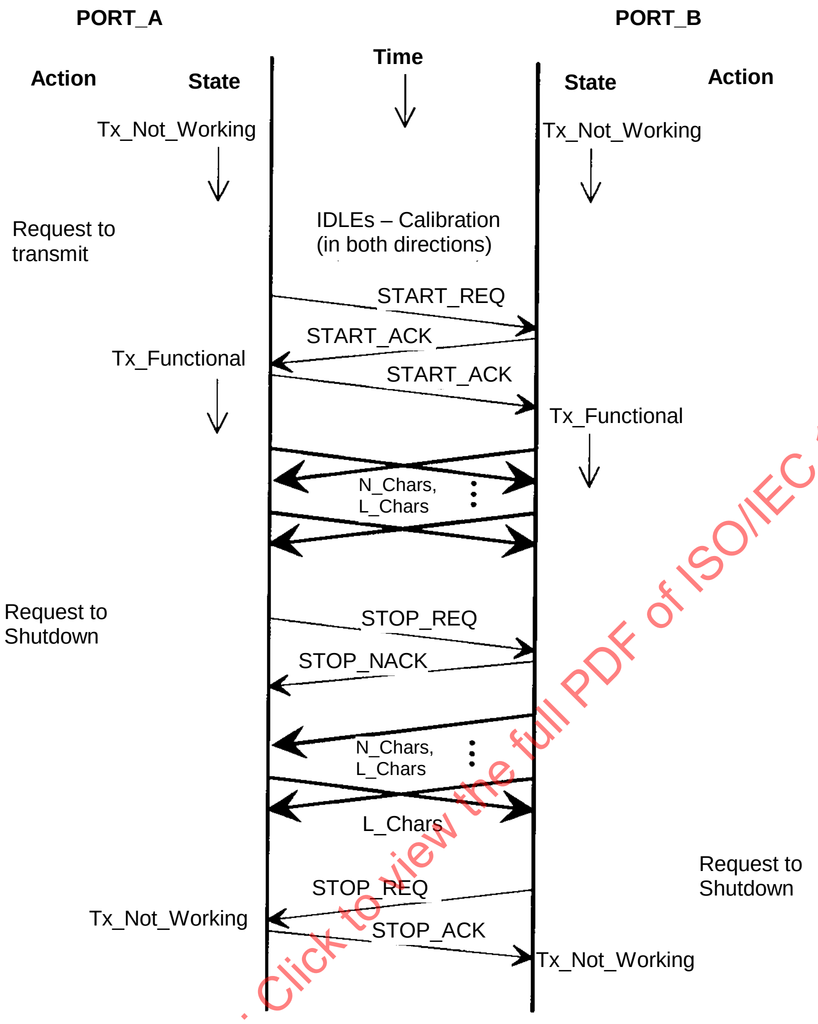
7.4.2.1 Unidirectional start-up

In figure 29, NODE_A requests to transmit to NODE_B. At first the transmitter_A is started and IDLEs are sent to calibrate receiver_B. When receiver_B is calibrated (flag CAL_B goes high), this automatically starts the transmitter_B and IDLEs are sent to calibrate receiver_A. When receiver_A is calibrated, PORT_A sends a start_request (START_REQ) to PORT_B. PORT_B responds by sending a start_acknowledge (START_ACK) to PORT_A.

On receipt of START_ACK, PORT_A replies by sending a START_ACK to PORT_B. PORT_A becomes functional (see below). N_chars in the SOURCE_A are transmitted from A to B (if SOURCE_A is empty, IDLEs shall be sent) and flow control information is transmitted from A to B when necessary.

On receipt of START_ACK, PORT_B becomes functional. N_chars in the SOURCE_B are transmitted from B to A (if SOURCE_B is empty, IDLEs shall be sent) and flow control information is transmitted from B to A when necessary. Note that PORT_B is functional, even if NODE_B has not been explicitly requested to transmit to NODE_A.

This exchange is shown in figure 34.



NOTE In reality, the link_characters (IDLE, START_REQ, START_ACK, STOP_REQ, STOP_ACK and STOP_NACK) are interleaved with the DATA, they are not separate in time as shown here.

Figure 34 – Exchange for start-up, functional and shutdown

7.4.2.2 Bi-directional start-up

This is the case in which NODE_A and NODE_B request to transmit quasi-simultaneously (for example, they request to transmit on power-up). IDLEs are sent in both directions and, when the appropriate CAL goes high, both transmitter_A and transmitter_B send START_REQ and both reply with START_ACK. Both then reply to the START_ACK with another START_ACK (since each side does not "know" that it is a bi-directional start-up); these last 2 START_ACKs have no effect.

This exchange is shown in figure 35.

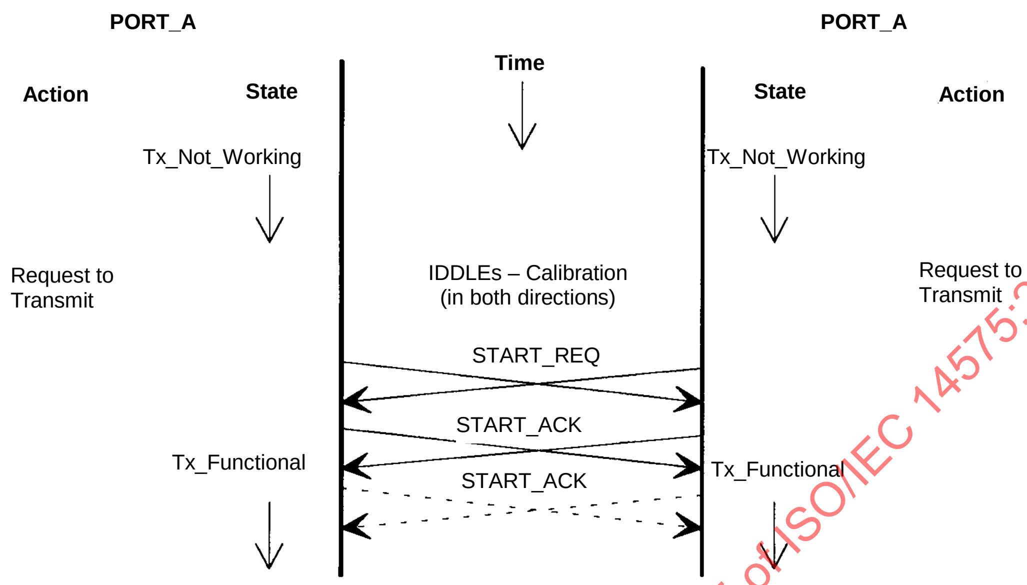


Figure 35 – Exchange for bidirectional start-up

7.4.3 Errors on start-up

7.4.3.1 Loss of START_REQ

In the case of a bidirectional start-up, it is possible that the START_REQ is sent before the opposite receiver is calibrated (this is not possible during an unidirectional start-up). If this is the case, the START_REQ sent will be filtered and lost by the opposite port. Therefore, after a time-out period, t_{TO1}, the START_REQ is resent. The value of t_{TO1} is given in table 50.

7.4.3.2 Destination node not connected or not under power

If a node requests to transmit and the opposite node is not connected or not under power, the transmitter state machine will block in state Tx_Cal_1. If, after a time-out period t_{TO2}, the transmitter state machine has not been able to indicate to the port controller that it is functional, then it shall be returned to the Not_Working state.

NOTE The same timeout will cover any other failure to start up. It is then for the port controller to signal the failure of start-up and to request to transmit as and when appropriate (these details are outside the scope of this International Standard).

This functionality is desirable for two reasons.

a) The system is notified that there has been a failure of start-up on the link.

b) Fiber-optic safety. If the link is on a fiber-optic medium, and the fiber is disconnected, the laser must not continue to indefinitely emit into an open fiber for eye safety reasons.

Table 50 – Time-out values

Symbol	Unit	Value
t_{TO1}	ms	5
t_{TO2}	ms	50

7.4.3.3 Other errors

It is possible that other transmission errors (e.g. loss of receiver calibration, parity error, unexpected or no response from opposite node) could interrupt the start-up mechanism. If any of these errors occur during start-up, the transmitter should return to the Not_Working state for the reasons stated above in 7.4.3.2.

7.4.4 Functional

7.4.4.1 General

When functional, the following information shall be sent across the link in order of decreasing priority.

a) Link characters other than IDLE (primarily FCC, i.e. flow control information for the opposite going link)

b) N_chars in the SOURCE, in a flow-controlled manner (see 7.4.4.2)

c) IDLEs when there are no SOURCE N_chars to send (the SOURCE is empty), or when flow control prevents the transmission of SOURCE N_chars

All L_chars shall be filtered by the receiver controller: IDLEs are discarded; other L_chars are passed to the transmitter controller which acts appropriately on them. N_chars shall be written into the SINK.

7.4.4.2 Flow control

The credit value (F) of each Flow Control Character (FCC) is set at 32 N_chars.

A link interface shall send at least four other characters between each FCC. Note in particular that this may require at least four IDLE characters to be transmitted after the first FCC on link startup. Note that in normal operation a link interface will issue an FCC for every 32 N_chars received, and therefore would normally transmit at least 32 characters between each FCC.

7.4.4.3 Maximum transmission line length and latency

The appropriate formulae are given in annex H.

7.4.5 Link reset mechanism

A port may require to reset the bidirectional link (Request_Reset). The port sends the RESET L_char and its transmitter passes to the Tx_Working_1 state. On receipt of RESET, the opposite port's transmitter passes into the Tx_Working_2 state. The unidirectional start-up procedure then proceeds as described above (7.4.4.1). A Request_Reset also implies a reset of the flow control: the transmitter resets its credit to zero and the receiver clears its sink and resends the appropriate number of FCCs.

7.4.6 Errors when functional

Note that a further discussion on the handling of errors is provided in annex G.

7.4.6.1 Loss of receiver calibration

Loss of receiver calibration on the incoming serial data stream is indicated by the flag CAL passing low. The port whose receiver has lost calibration has two options in order to recalibrate the link:

a) Initiate the reset mechanism described in 7.4.5.

b) Hold its serial output low, which will force a receiver calibration error in the opposite port. The bidirectional start-up procedure then proceeds as described in 7.4.2.2.

Calibration errors should be reported to the port controller for error logging purposes. The handling of packets that have been interrupted by a loss of calibration is outside the scope of this International Standard.

7.4.6.2 Parity error detected

The precise handling of parity errors is outside the scope of this International Standard. Parity errors should be reported to the port controller for error logging purposes. If a parity error and a receiver calibration error occur simultaneously, the port should follow the calibration error procedure described in 7.4.6.1.

7.4.7 Shutdown

The bidirectional link shall not be shutdown unless both NODE_A and NODE_B have requested a shutdown. This is done by a request to stop demand from the port. The transmitter sends a stop_request (STOP_REQ). The response to a STOP_REQ is either a stop_acknowledge (STOP_ACK) if the opposite user is ready to stop, or a stop_not_acknowledge (STOP_NACK) if the opposite user is not ready to stop. Once a request to stop has been demanded, any new N_chars placed in the source shall not be transmitted: the transmitter shall only send L_chars (primarily IDLEs and FCCs). If the port receives a STOP_NACK in reply to its request_to_stop, it may restart transmission by a request to transmit.

When shut down, the transmitter is in the Not_Working state and the serial output shall be static.

8 HS-FO-10 fiber optic link

8.1 Physical medium

8.1.1 General optical characteristics

The HS-FO optical link cable is a fiber cable containing two fibers, one for transmission in each direction. 62.5 µM or 50 µm multimode shall be used (50 µm allows longer reach), and shall meet at minimum, the specifications given in IEC 60793-1-A1-a. Where even longer reach is required, a single-mode fiber, as specified in IEC 60793-1-B1, may be used. A summary of the main optical characteristics (as specified in IEC 60793-1-A1-a and IEC 60793-1-B1) of these fibers is given table 51.

The link cable shall be clearly marked "ISO/IEC 14575 HS-FO Link Cable (multimode)" or "ISO/IEC 14575 HS-FO Link Cable (single-mode)" as appropriate. A recommendation for fiber construction is given in annex S.

Table 51 – Summary of main optical characteristics of HS-FO fibers

Parameter	Units	Value		
Fiber type	–	Multimode	Multimode	Single-mode
Core diameter	Micrometers	62.5	50	9
Cladding diameter	Micrometers	125	125	125
NA	–	0.275	0.2	–
Attenuation	dB/km	4 maximum at 850 nm	4 maximum at 850 nm	0.5 maximum at 1 300 nm

8.1.2 Optical connector

The HS-FO link optical connector is a MU connector-duplex. The MU connector-duplex consists of a through-panel (fixed) adapter and a cable mounted (free) plug. It provides the following features.

a) A dual multimode or single-mode fiber connection per connector

b) Push-pull coupling

c) Small size

The connectors shall be as specified in IEC 61754-6. In addition to the interface specification of IEC 61754-6, the connectors shall have the properties described in table 52.

Table 52 – THS-FO connector modularity specifications

Characteristic	Specification
Modularity	Fixed connector modules shall be placed on a 14 mm pitch, or their centerlines separated by more than 28 mm
Connector width	13.9 mm maximum
Overall connector length (to end of boot)	55 mm maximum

The plug at either end of the cable shall be connected to the fibers in the cable in such a way as to connect ferrule 1 in one plug with ferrule 2 in the other plug, and vice versa, as shown in figure 36.

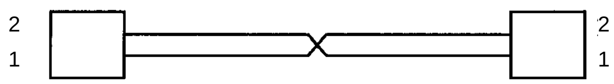


Figure 36 – HS-FO cable fibers/plugs wiring

Note that the effect of the cable/connector assembly is to provide a single twist. Any extension adapters allowing multiple segments of cables to be used shall also provide such a twist, so that the effect of any such cable/adapter/cable combination is to provide a single twist, as illustrated in figure 37.

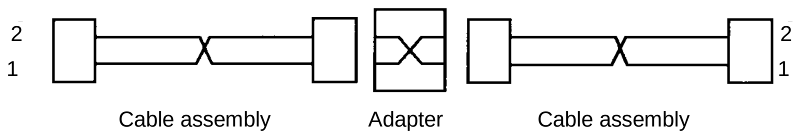


Figure 37 – HS-FO extension adapter

The allocation of HS-FO signals to the plug ferrules and adapter shall be as given in table 53 (which is oriented to correspond to the external view of the through-panel (fixed) adapter when mounted on the upper surface of a horizontal PCB, see figure 38). The direction of the signals is relative to the fixed adapter.

Table 53 – HS-FO signal allocation

Ferrule	2	1
Signal	HS_FO_in	HS_FO_out

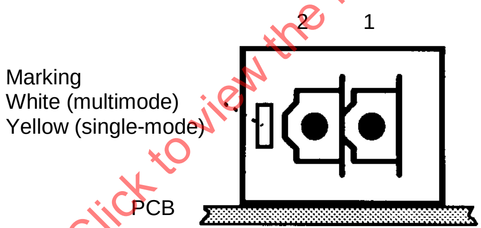


Figure 38 – HS-FO fixed adapter, external view and ferrule allocation

8.1.3 Environmental constraints

The environmental requirements for the HS-FO link cables and connectors are application dependent. However, as a minimum, the cables and connectors shall meet the constraints in table 54. Note that specific applications may have requirements for extended temperature range or other environmental parameters.

Table 54 – HS-FO environmental constraints

Parameter	Value
Operating temperature	–10 °C to +60 °C
Non-operating temperature	–40 °C to +85 °C

Further environmental specifications are given in annex C.

8.2 Signal level

8.2.1 General

The HS-SE-10 electrical signal levels operate with a nominal swing of 800 mV, equivalent to ECL or PECL swings. Because the link may be a.c. coupled, the electrical driver and receiver can be directly interfaced with standard fiber optic transceiver components (which operate on ECL or PECL levels).

The a.c. coupling requirements are as for the HS-SE-10 electrical link (see 7.2.4).

8.2.2 Transmitter and receiver characteristics

Launch power and sensitivity are strongly dependent on the kind of optical components used and on the configuration of the LED/laser modulation and of the photodiode amplifier. Table 55 gives the recommended transceiver characteristics for a laser based system for multimode fiber, and table 56 gives the recommended transceiver characteristics for monomode fiber.

Table 55 – HS-FO recommended transceiver characteristics for multimode fiber

Parameter	Units	Value		
		Min.	Typ	Max.
Operating speed	MBd	–	–	1 000
HS-FO transmitter (Laser into 50 or 62.5 µm fiber)				
Launch power	dBm	–13		–11
Wavelength	nm	760		900
Spectral width FWHM	nm	–	60	–
HS-FO receiver				
Sensitivity at BER = 10^{-12}	dBm	–21	–	–
Dynamic range	dB	10	–	–

Table 56 – HS-FO recommended transceiver characteristics for single mode fiber

Parameter	Units	Value		
		Min.	Typ	Max.
Operating speed	MBd	–	–	1 000
HS-FO transmitter				
Launch power	dBm	–12	–	–8
Wavelength	nm	1 250	–	1 340
Spectral width FWHM	nm	–	2	–
HS-FO receiver				
Sensitivity at BER = 10^{-12}	dBm	–20	–	–
Dynamic range	dB	12	–	–

8.2.3 HS-FO reference link

A link comprises of two link interfaces connected by appropriate media, and transmits information bidirectionally. For specification and test purposes, an HS-FO reference link is defined as a transceiver (the link interface), connected by a pair of fibers to an adapter, connected by a plug-cable-plug assembly to another adapter, connected to another transceiver by a pair of fibers, as shown in figure 39. This figure also shows reference test points TP1 and TP4 (where TPx are at the extremities of the optical cable).

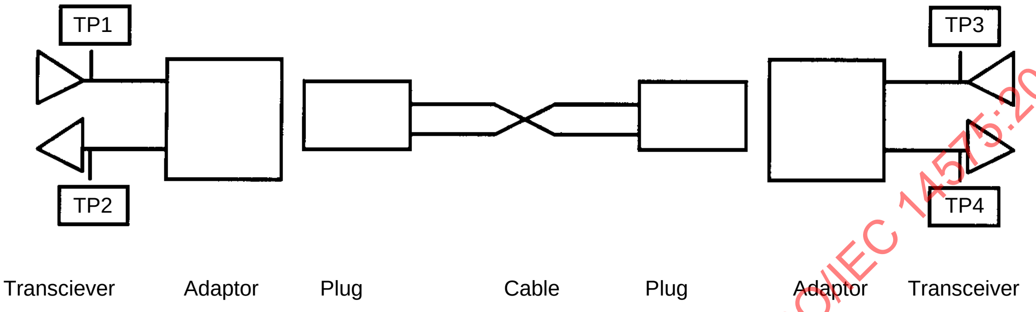


Figure 39 – HS-FO reference link

8.2.4 Link performance

The performance of the various components of the link system shall be as in table 57. The International Standard specifies a power budget for a link, i.e. the maximum loss. A "loopback" plug is defined as a single plug with a minimum length of fiber which connects ferrule a to ferrule b. This is used to provide the specification of the loss of a connector system and a reference specification for the power budget for the cable assembly. The performance of a minimum length reference cable is assumed to be equivalent to the performance of the loopback system. Note that this provides a high degree of confidence of interoperability within a practical test environment, but does not provide a guarantee of interoperability.

Table 57 – HS-FO link performance specification

Characteristic	Specification	Test specification
Link length (62.5 µm multimode fiber)	100 m maximum	–
Link length (50 µm multimode fiber)	1 000 m maximum	–
Link length (single-mode fiber)	3 000 m maximum	–
Power budget (total loss in a link)	5.5 dB maximum	TP1 to TP4 and TP3 to TP2
Loopback test loss	1.5 dB maximum	Loss between TP1 and TP2 using a loopback plug
Cable assembly additional attenuation	4 dB maximum	Difference in loss between the loss measured from TP1 to TP4 (and TP3 to TP2) with cable under test and the loopback test loss as defined above

8.2.5 Eye safety

IEC 60825 is the most stringent standard for laser radiation eye safety. It is for the implementor to take appropriate measures to ensure eye safety.

8.3 Character level and exchange level

The character level and exchange level are identical to the HS-SE-10 implementation. See 7.3 and 7.4.

Note that in a given implementation, an appropriately large N_char sink size will have to be chosen in order to prevent the flow control mechanism periodically stalling the data flow over long lengths of fiber. See annex H.

9 Common packet level

9.1 General discussion

A packet is a sequence of characters (N_chars only) with a specific order and format. Constituent characters of different packets shall not be interleaved on a link. A packet consists of a destination followed by a payload. A packet is delimited by an end_of_packet marker.

This International Standard does not define a specific size (or maximum size) for packets. This enables different packet formats to be carried by a HIC network. However, packets should be limited in size so that no very long packet can occupy the network for an extended period of time. A limited known packet size also enables an upper bound to be placed on the latency of any packet transmission.

Terminal nodes generate (source node) and consume (destination node) packets. A network is any set of devices connected by links joining (directly or indirectly) a set of terminal nodes.

The protocol assumes the use of packet-switched networks in which the routing information necessary to correctly transmit the packet across the network is contained in the first K N_chars of the packet (where K is fixed throughout a subnetwork). It is at the packet level that the routing decisions are taken. The protocol does not define a specific (or maximum) size for a packet. Successive packets transmitted on a link may have different destinations. Each packet is transmitted in its entirety, i.e. the transmission of a packet on a link shall be completed before the transmission of the successive packet may begin.

9.2 Packet format

A packet consists of a destination followed by a payload, and is delimited by an end_of_packet marker:

<DEST> <PAYLOAD> <End_Of_Packet>

9.2.1 Destination

The destination normally contains a list of one or more destination identifiers (dest_id) which are used to enable a network to transmit the packet from its source node to its destination node. A dest_id is a fixed size field (K bytes long, where $K \geq 1$), its size being known to the (sub)network.

The list is not delimited and only the first dest_id is used by a switch for routing purposes. The switch shall treat the other dest_id(s) in the list (if they exist) as part of the payload. A switch may provide a facility for deleting the first dest_id as it outputs the packet, so that the next switch uses the next dest_id in the original list. This mechanism may be used to connect (sub)networks which use different size dest_ids (different values for K). The method of allocating dest_ids to destinations is outside the scope of this International Standard.

The destination may be null, for example for the specific case of a point-to-point link (i.e. the network is just one link).

9.2.2 Payload

The payload is the data (a message, a memory access request, an acknowledgment, etc.) that is to be transferred from the source node to the destination node. It has a specific format, defined in the transaction level. A payload may be null. The definition of any packet format is outside the scope of this International Standard.

9.2.3 End_of_packet marker

The end_of_packet marker (EOP in its generic form) is a N_char, and shall always be the last character of a packet; it acts as the packet delimiter. Packets do not have a start_of_packet marker: the first N_char received after an EOP shall be taken as the first character of the next packet.

Different EOP markers are defined in table 58.

Table 58 – End_of_packet markers

Name	Description
EOP_1	Normal end_of_packet marker
EOP_2	Exceptional end_of_packet marker

The exceptional_end_of_packet marker may be used to signal an end of message or an error. Implementations may provide more than one type of exceptional_end_of_packet marker.The N_char codes used for the EOP markers in DS and HS Links are as given in table 59.

Table 59 – Codes for EOP markers

Name	Description	Code for DS-SE and DS-DE	Code for HS-SE and HS-FO
EOP_1	Normal end_of_packet marker	P101	Control char ID = 7
EOP_2	Exceptional end_of_packet marker	P110	Control char ID = 8

Note that the N_char codes for TS-FO links have a more complex format, and a longitudinal checksum.

9.3 Networks and routing

The (sub)network routes the packet using the information contained in the destination field of the packet. The routing algorithm takes the fixed size dest_id as its input in order to determine how to route the packet within the (sub)network. The routing algorithm is outside the scope of this International Standard.

Packets sent from a given source node to a given destination node over a network may be delivered in an order different from the sending order. The details of mechanisms to ensure in-order delivery are outside the scope of this International Standard.

9.4 Error detection, recovery, and reporting

The function of the protocol is to deliver an error free packet from its source-terminal-node to its destination node. At the packet level or above, a system of high-level error checking may be required. It is the responsibility of the transaction level to define the high-level check that is to be used and therefore any definition of a high-level check is outside the scope of this International Standard. In general, a high-level check is required at the packet level if the low level is suspected of being error prone and there is no higher level check (e.g. a message level CRC in a message passing system).

A further discussion is given in annex G.

10 Conformance criteria

10.1 Conformance statements

Many implementations will implement only a subset of the protocol stack. For example, an interface on a box may comply with a vertical "slice" through the stack to incorporate the necessary elements for a particular speed/medium combination, whereas for a cable assembly only the physical parameters are relevant. Accordingly, a number of subsets are defined, to which implementations may claim conformance. Any such conformance statement shall take the following form "(The interfaces on) this implementation/product conform(s) to the [identification] specification of ISO/IEC 14575". The text to be substituted for [identification], and the clauses of this International Standard to which the corresponding implementation shall conform, are given in 10.2 (see tables 60, 61, 62 and 63).

10.2 Definition of subsets

An implementation of a connector shall conform to all of the mandatory specifications given in all of the clauses for one of the identifications given in table 60.

Table 60 – Conformance identifications for connectors

Identification	Relevant clauses
DS-DE connector	5.4.2, A.2
HS-SE connector	7.1.5, B.2, B.3, B.4
TS-FO/HS-FO connector (MM)	6.1.2, C.2, C.4, C.5
HS-FO connector (SM)	8.1.2, C.3, C.4, C.5

An implementation of a link cable shall conform to all of the mandatory specifications given in all of the clauses for one of the identifications given in table 61.

Table 61 – Conformance identifications for link cables

Identification	Relevant clauses
DS-DE link cable	5.4.1
HS-SE link cable	7.1.3, 7.1.4
TS-FO link cable	6.1.1
HS-FO link cable	8.1.1

An implementation of a link cable assembly shall conform to all of the mandatory specifications given in all of the clauses for one of the identifications given in table 62.

Table 62 – Conformance identifications for link cable assemblies

Identification	Relevant clauses
DS-DE link cable assembly	5.4, A.2
HS-SE link cable assembly	7.1, B.2, B.3, B.4
TS-FO/HS-FO link cable assembly (MM)	6.1, C.2, C.4, C.5
HS-FO link cable assembly (SM)	8.1, C.3, C.4, C.5

An implementation of a link interface shall conform to all of the appropriate mandatory specifications given in all of the clauses for one of the identifications given in table 63.

Table 63 – Common identifications for link interfaces

Identification	Relevant clauses
DS-SE-00 link interface	5.1, 5.2, 5.3, 5.6, 5.7, 9
DS-DE-00 link interface	5.1, 5.5, 5.6, 5.7, 9
DS-SE-01 link interface	5.1, 5.2, 5.3, 5.6, 5.7, 9
DS-DE-01 link interface	5.1, 5.5, 5.6, 5.7, 9
DS-SE-02 link interface	5.1, 5.2, 5.3, 5.6, 5.7, 9
DS-DE-02 link interface	5.1, 5.5, 5.6, 5.7, 9
HS-SE-10 link interface	7.2, 7.3, 7.4, 9
TS-FO-02 link interface	6.2, 6.3, 6.4, 9
HS-FO-10 link interface	8.2, 8.3, 9

Annex A
(normative)

DS-DE connector specification

A.1 General

The DS-DE connectors shall be as specified in IEC 61076-4-107. The connector system comprises a through-panel (fixed) connector, which connects to a cable mounted (free) connector. A connector is required to support one DS-DE link. An option (described in annex N) allows a connector to support multiple DS-DE links, by arraying multiple DS-DE connectors.

Any properties not specified in IEC 61076-4-107 shall be as in the following specification.

A.2 Specification

The connectors shall be implemented according to table A.1 and be of dimensions specified in figures A.1 to A.7.

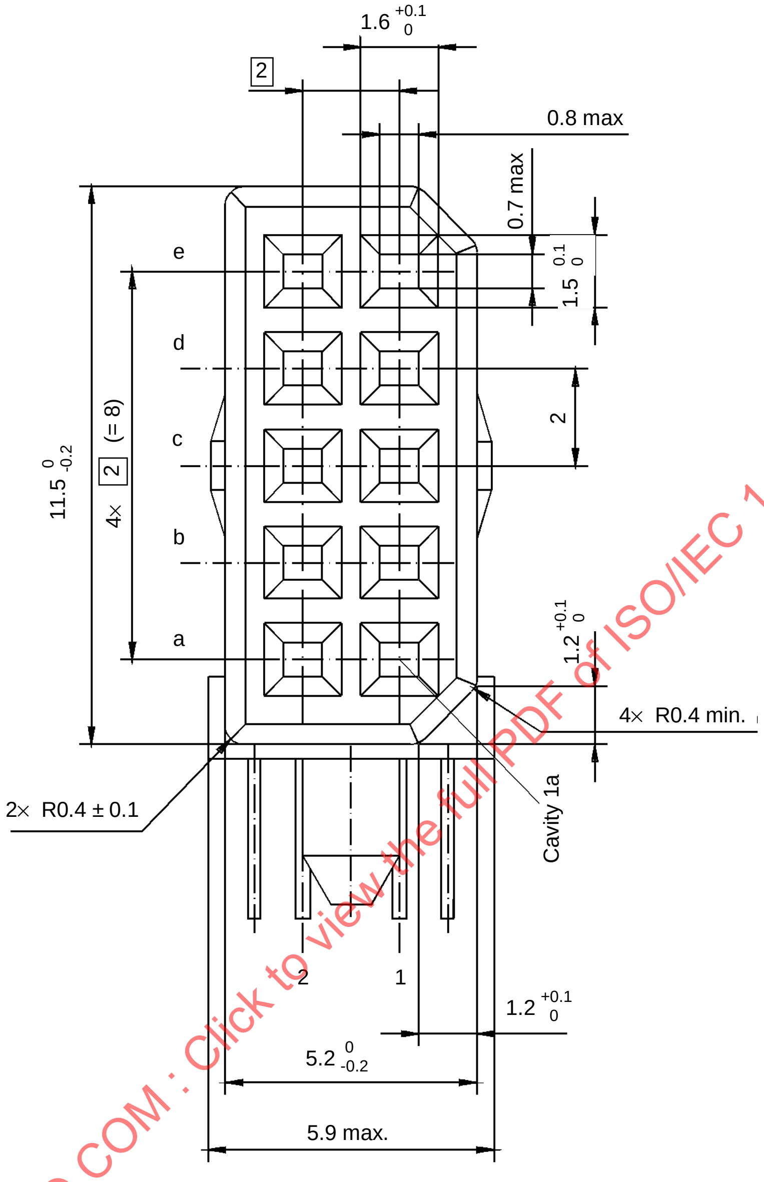
Table A.1 – DS-DE connector requirements

Characteristic		Specification	Test specification	Conditions
Contacts	10 per connector; arranged as two rows of 5 contacts	IEC 61076-4-107	IEC 60512-2, Test 1a	–
Contact grid	2 mm * 2 mm	IEC 60917; IEC 61076-4-107	IEC 60512-2, Test 1b	–
Connector width	5.9 mm maximum	IEC 61076-4-107	IEC 60512-2, Test 1b	–
Connector pitch	6.0 mm	IEC 61076-4-107	IEC 60512-2, Test 1b	–
Modularity	Adjacent connectors shall be placed on a 6 mm pitch. Non-adjacent connectors shall have their centerlines separated by at least 12 mm	IEC 61076-4-107	–	–
Shielding	Completely shielded	IEC 61076-4-107	IEC 60512-2, Test 1a	–
Polarization	Chamfer design prevents 180° incorrect mating	IEC 61076-4-107	IEC 60512-7, Test 13e	–
Male-female contact overlap	0.9 mm minimum when mated	IEC 61076-4-107	–	–
Misalignment in transverse and longitudinal axes	±0.45 mm	IEC 61076-4-107	–	–
Inclination of transverse and longitudinal axes	±7° maximum	IEC 61076-4-107	–	–
Voltage proof V r.m.s	750 V contact/contact 750 V contact/shielding	IEC 61076-4-107	IEC 60512-2, Test 4a	–

Table A.1 *(continued)*

Characteristic	Specification	Test specification	Conditions	
Current-carrying capacity	1.5 A at 70 °C	IEC 61076-4-107	IEC 60512-3, Test 5b	All contacts fully loaded
Contact resistance	35 mΩ maximum	IEC 61076-4-107	IEC 60512-2, Test 2a	–
Insulation resistance	10^4 MΩ minimum contact/ contact 10^4 MΩ minimum contact/shielding	IEC 61076-4-107	IEC 60512-2, Test 3a	–
Crosstalk	Data/strobe: 3.6 % Data/data: 1.2 %	IEC 61076-4-107	–	Tr = 1 ns; differential wiring
Impedance	110 Ω ± 20 Ω	IEC 61076-4-107	IEC 48 (B) 141[a]	Differential wiring
Skew	80 ps maximum	IEC 61076-4-107	–	Between row a and row e
Temperature range	–10 °C to +60 °C	IEC 61076-4-107	IEC 60512-6, Test 11	–
Creepage and clearance distance: contact/contact contact/shielding	0.65 mm minimum	IEC 61076-4-107	IEC 60512-2, Test 1b	–
Mechanical operations	250 operations	IEC 61076-4-107	IEC 60512-5, Test 9a	–
Total insertion force	10 N maximum per connector module	IEC 61076-4-107	IEC 60512-7, Test 13b	Max. speed of operation: 10 mm/s
Withdrawal force by pulling on latch	2 N minimum per connector module	IEC 61076-4-107	IEC 60512-7, Test 13b	Max. speed of operation: 10 mm/s
Withdrawal force with closed latch	100 N minimum per connector module	IEC 61076-4-107	IEC 60512-8, Test 15f	–
Tensile strength of cable-connector clamp	110 N minimum per connector module	IEC 61076-4-107	IEC 60512-9, Test 17c	–
Vibration	20 g / 10 Hz to 500 Hz / 8 cycles/ 2 h per axis contact disturbance 1 µs maximum	IEC 61076-4-107	IEC 60512-4, Test 6d	–
Shock	49 g / 5 ms / 5 shocks per plane contact disturbance 1 µs maximum	IEC 61076-4-107	IEC 60512-4, Test 6c	

[a] Time domain reflectometry (Under consideration).

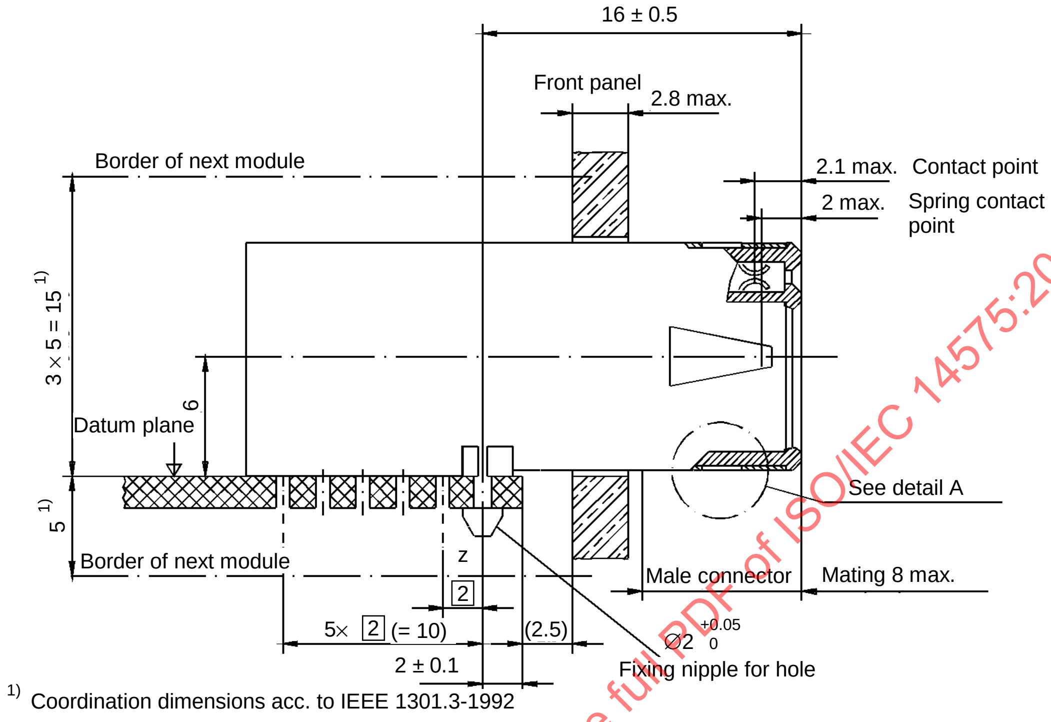


Dimensions in millimetres

Reference to grid *n* × 2 mm

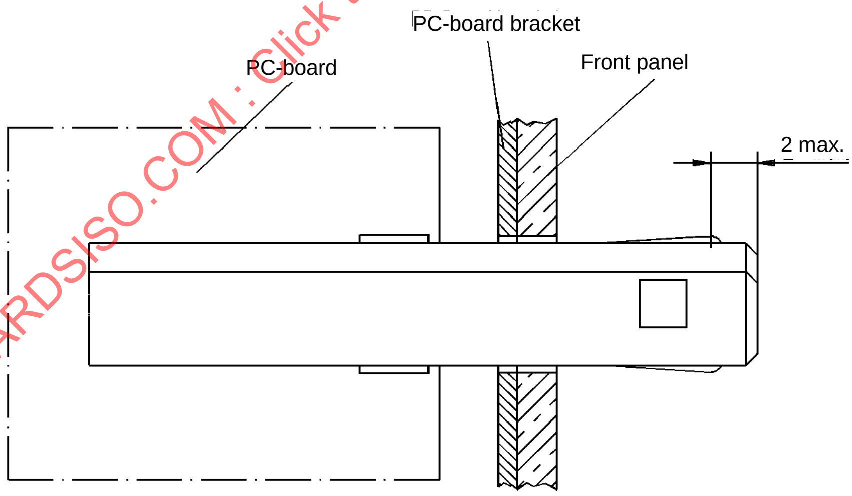
Figure A.1 – DS-DE fixed connector front view

Nothing in the connector design shall impede the assembly of systems which meet CISPR limits.



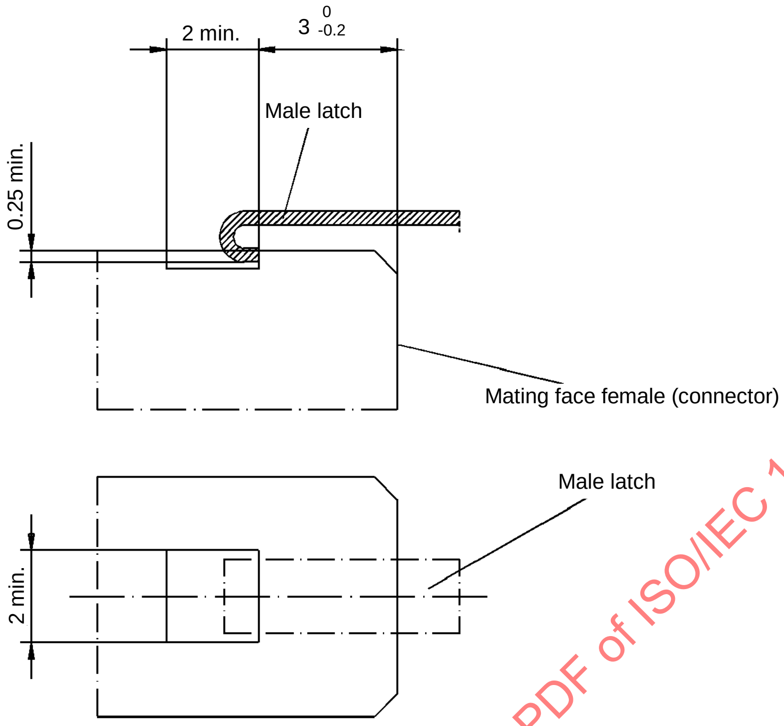
Dimensions in millimetres

Figure A.2 – DS-DE fixed connector side view



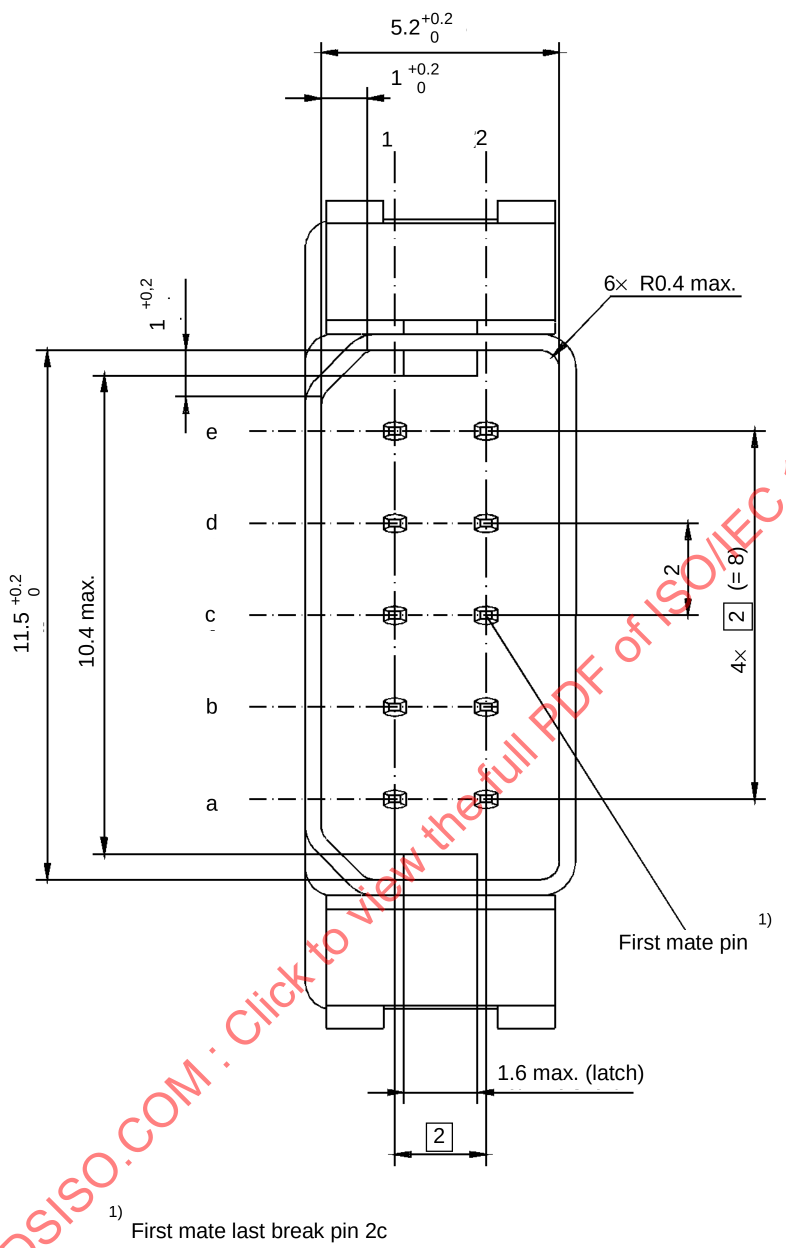
Dimensions in millimetres

Figure A.3 – DS-DE fixed connector top view



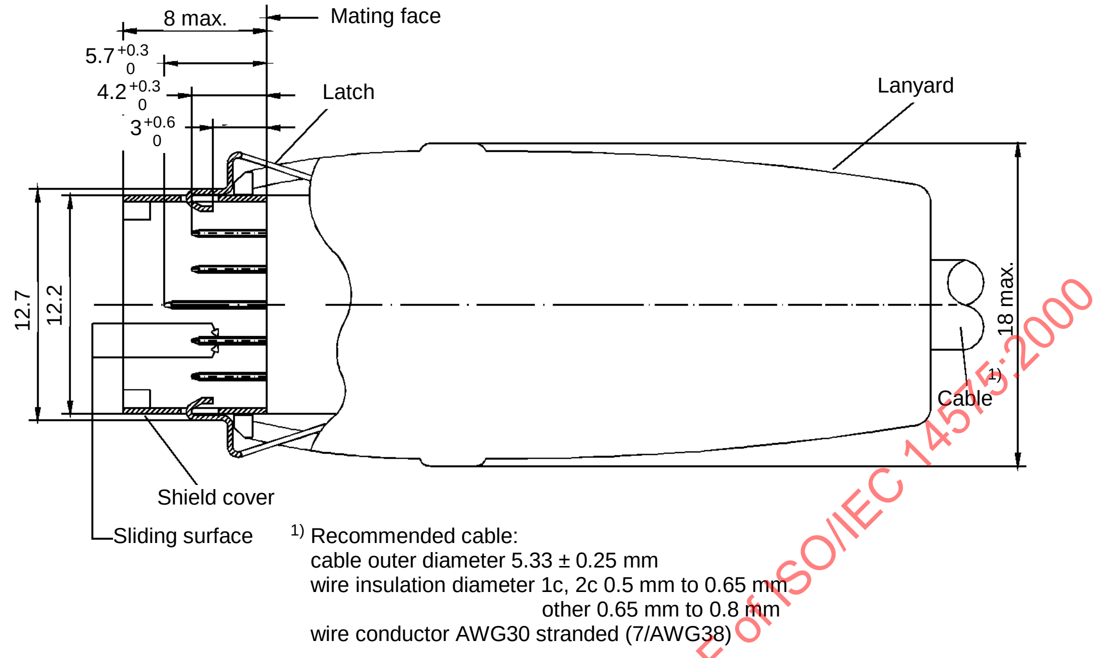
Dimensions in millimetres

Figure A.4 – DS-DE connector latch



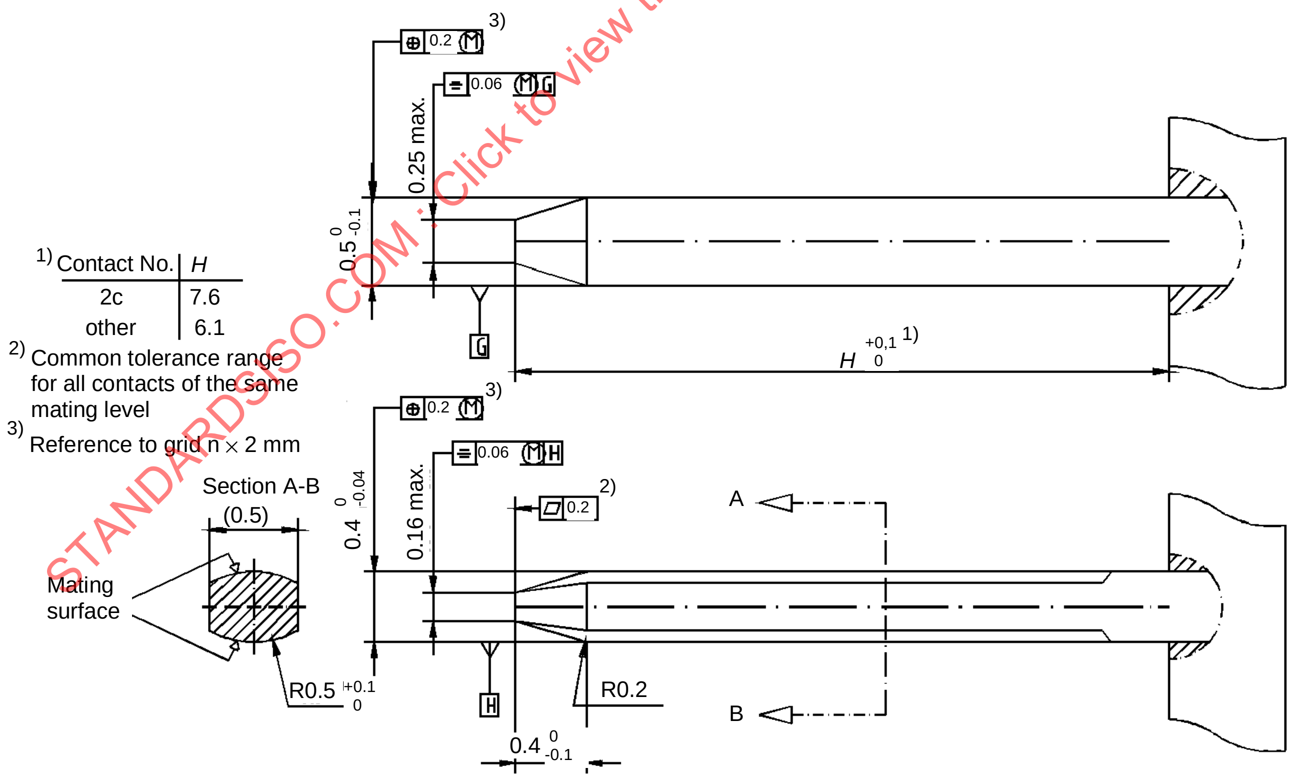
Dimensions in millimetres

Figure A.5 – DS-DE free connector front view



Dimensions in millimetres

Figure A.6 – DS-DE free connector side view



Dimensions in millimetres

NOTE All contacts shall be loaded in the insulator housing.

Figure A.7 – DS-DE free connector contact

Annex B
(normative)

HS-SE connector specification

B.1 General

The HS-SE connectors shall be as specified in IEC 61076-4-107. Any properties not specified in IEC 61076-4-107 shall be as in the following specification. The connector system comprises a through-panel (fixed) connector, which connects to a cable mounted (free) connector. A connector is required to support one HS-SE link. An option (described in annex Q) allows a connector to support multiple HS-SE links, by arraying multiple HS-SE connectors.

B.2 Specification

The connectors shall be implemented according to table B.1, with dimensions specified in figures B.1 to B.5.

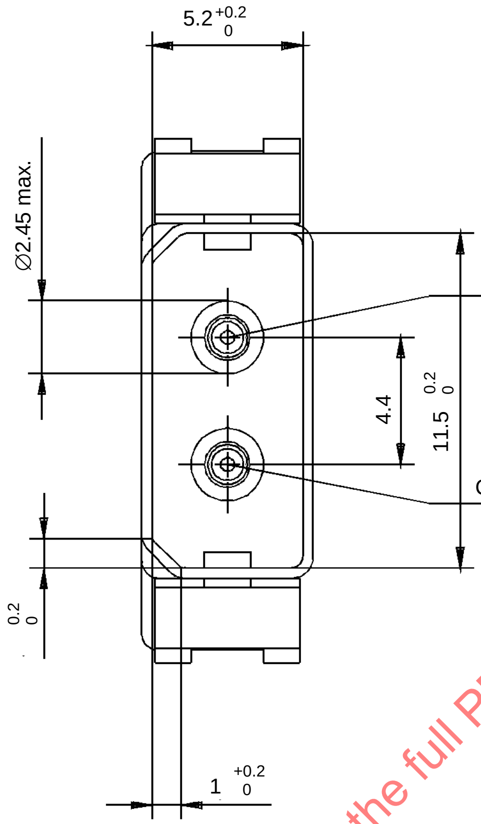
Table B.1 – HS-SE connector requirements

Characteristic		Specification	Test specification	Conditions
Coaxial contacts	2 per connector	IEC 61076-4-107	IEC 60512-2, Test 1a	–
Connector width	5.9 mm maximum	IEC 61076-4-107	IEC 60512-2, Test 1b	–
Connector pitch	6.0 mm	IEC 61076-4-107	IEC 60512-2, Test 1b	–
Modularity	Adjacent connectors shall be placed on a 6 mm pitch. Non-adjacent connectors shall have their centerlines separated by 12 mm or more	IEC 61076-4-107	–	–
Shielding	Completely shielded	IEC 61076-4-107	IEC 60512-2, Test 1a	–
Polarization	Chamfer design prevents 180° incorrect mating	IEC 61076-4-107	IEC 60512-7, Test 13e	–
Male-female contact overlap	2.0 mm minimum when mated	IEC 61076-4-107	–	–
Misalignment in transverse axes	±0.6 mm	IEC 61076-4-107	–	–
Misalignment in longitudinal axes	±0.9 mm	IEC 61076-4-107	–	–
Inclination of transverse axes	±2° maximum	IEC 61076-4-107	–	–
Inclination of longitudinal axes	±3° maximum	IEC 61076-4-107	–	–

Table B.1 *(continued)*

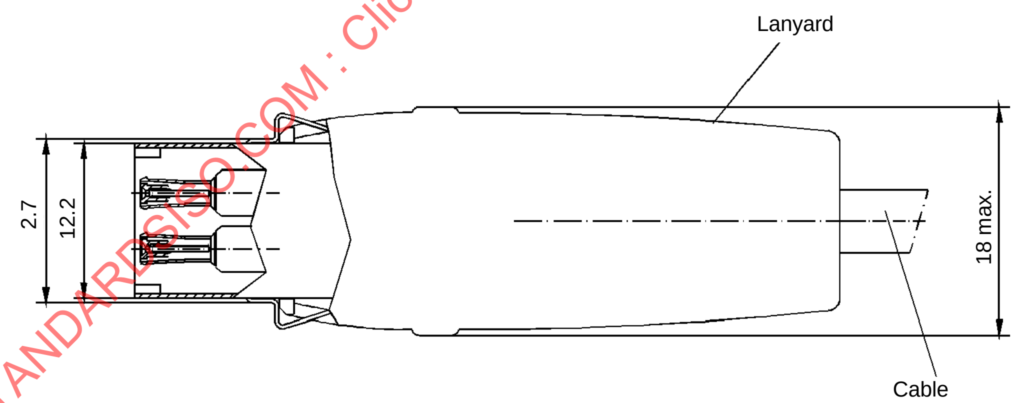
Characteristic		Specification	Test specification	Conditions
Voltage proof V r.m.s: center contact / ground contact	1 000 V	IEC 61076-4-107	IEC 60512-2 Test 4a	–
Contact resistance: center contact ground contact shielding contact	12 mΩ max. 6 mΩ max. 30 mΩ max.	IEC 61076-4-107	IEC 60512-2 Test 2a	–
Insulation resistance	5 000 MΩ min.	IEC 61076-4-107	IEC 60512-2, Test 3a	–
Insertion loss	max. 0.3 dB $\sqrt{F}$ (F in GHz)	IEC 61076-4-107	IEC 61156-1	–
HF leakage	Min. 40 dB at 3 GHz	IEC 61076-4-107	Under consideration	–
Crosstalk attenuation	Min. 35 dB at 3 GHz	IEC 61076-4-107	IEC 61156-1	–
VSWR	<1.3 at 3 GHz	IEC 61076-4-107	Under consideration	Mated couple male + female contact
Impedance	50 Ω ± 10%	IEC 61076-4-107	Under consideration	–
Temperature range	–10 °C to +60 °C	IEC 61076-4-107	IEC 60512-6, Test 11	–
Mechanical operations	500 operations	IEC 61076-4-107	IEC 60512-5, Test 9A	–
Insertion force	3.0 N max. per coaxial line	IEC 61076-4-107	IEC 60512-7, Test 13b	–
Withdrawal force	0.5 N min. per coaxial line	IEC 61076-4-107	IEC 60512-7, Test 13b	–
Withdrawal force with closed latch	100 N min. per connector module	IEC 61076-4-107	IEC 60512-8, Test 15f	–
Tensile strength of cable connector clamp	50 N single braid cable; 100 N double braid cable	IEC 61076-4-107	IEC 60512-9, Test 17c	–
Vibration	15 g / 10 Hz to 60 Hz / 30 min per axis contact disturbance 1 µs max.	IEC 61076-4-107	–	–
Shock	50 g / 5 ms / 3 shocks per plane Contact disturbance 1 µs max.	IEC 61076-4-107	IEC 60512-4, Test 6c	–

Nothing in the connector design shall impede the assembly of systems which meet CISPR limits.



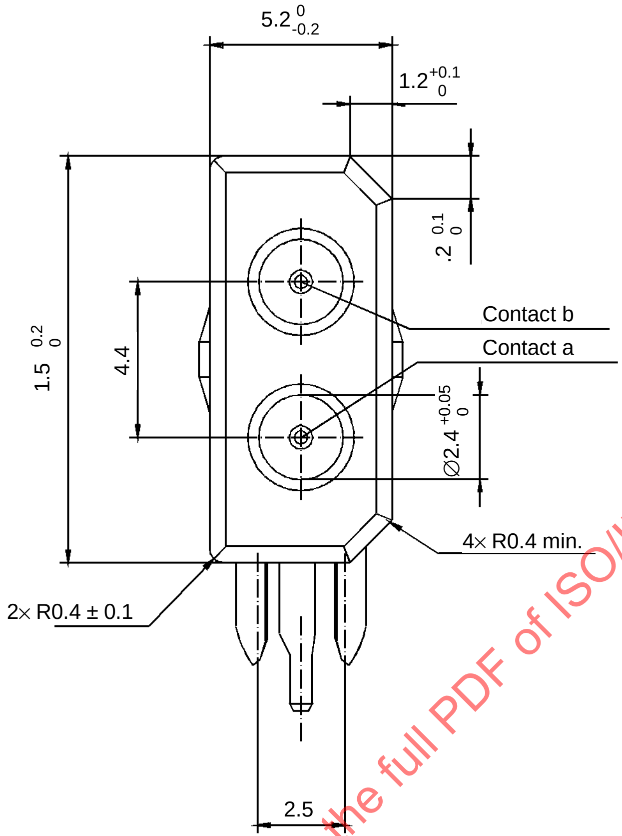
Dimensions in millimetres

Figure B.1 – HS-SE free connector front view



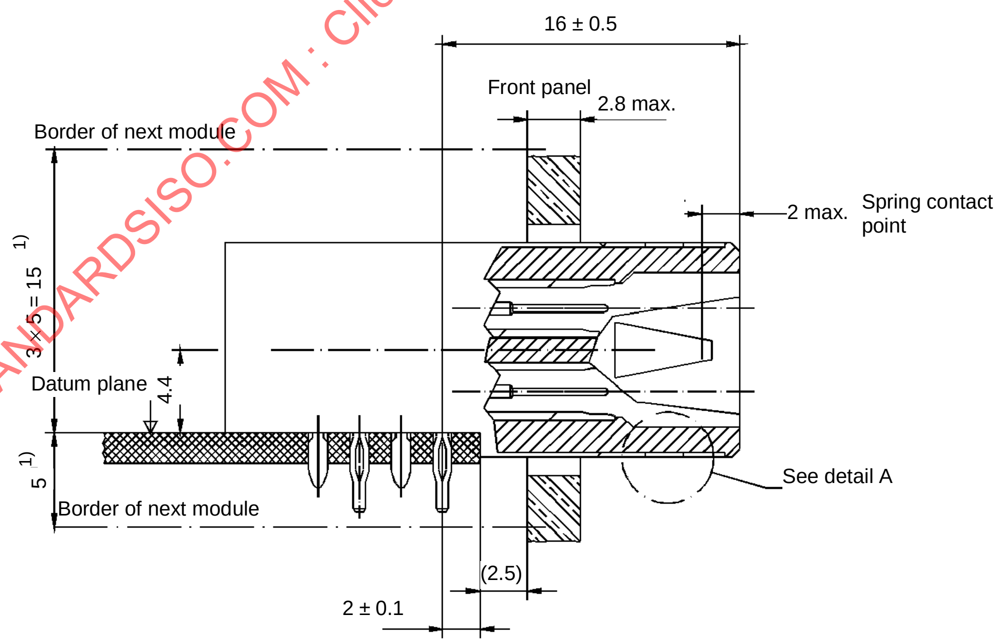
Dimensions in millimetres

Figure B.2 – HS-SE free connector side view



Dimensions in millimetres

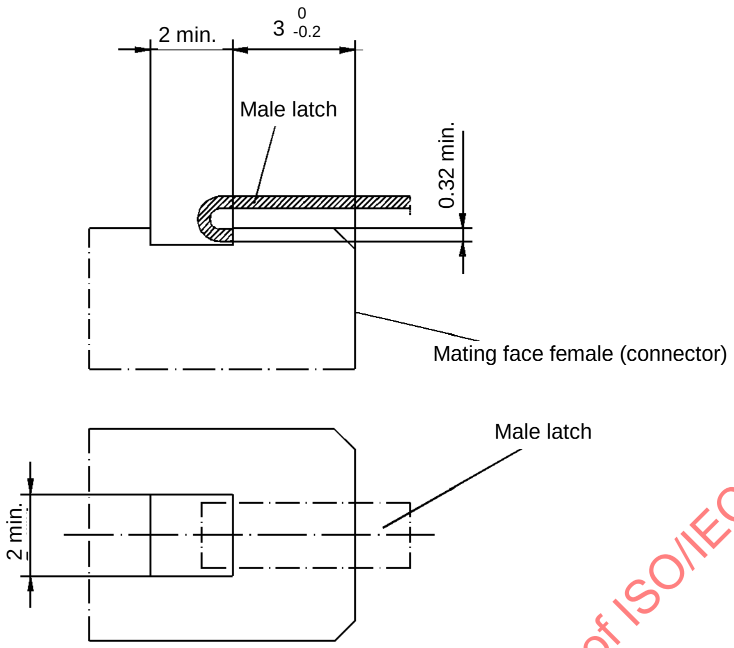
Figure B.3 – HS-SE fixed connector front view



1) Coordination dimensions according to IEEE 1301.3-1992

Dimensions in millimetres

Figure B.4 – HS-SE fixed connector side view



Dimensions in millimetres

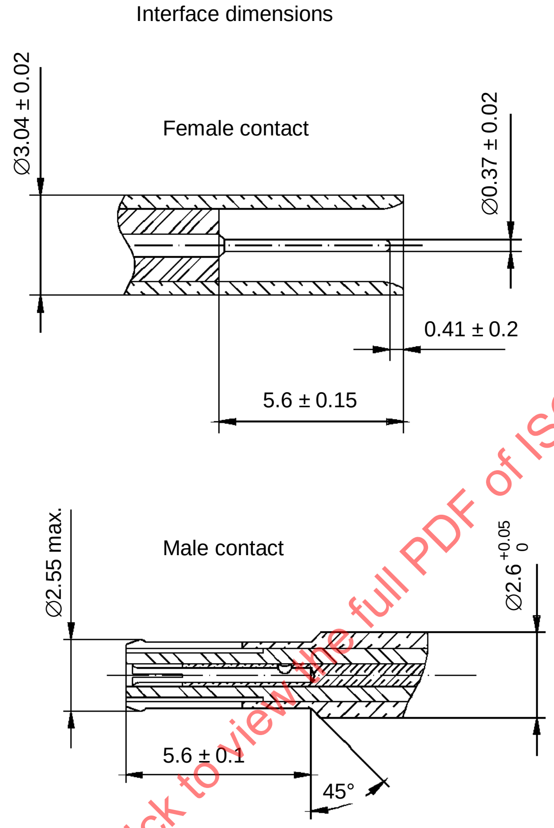
Figure B.5 – HS-SE connector link

B.3 Shielding

A link connector shall be shielded if the link cable is shielded. There shall be a 360° mechanical connection between the outer braid of the link cable and the connector housing. In case of high electromagnetic compatibility (EMC) requirements, additional parts (e.g. EMC brackets and gaskets) may be used to ensure mechanical connection between the panel and connector housings.

B.4 Coaxial contacts

An HS-SE connector contains two coaxial contacts. The contacts shall be of dimensions shown in B.6.



Dimensions in millimetres

Figure B.6 – HS-SE contact interface dimensions

Annex C
(normative)

TS-FO and HS-FO connector specifications

C.1 General

The TS-FO and HS-FO connectors shall be as specified in IEC 61754-6. Any properties not specified in IEC 61754-6 shall be as in the following specification.

C.2 TS-FO and HS-FO multimode connector

The TS-FO and HS-FO (multimode) connectors shall be implemented according to table C.1 (interface specifications) and table C.2 (performance and environmental specifications), and be of dimensions specified in figures C.1 to C.2.

Table C.1 – TS-FO and HS-FO (multimode) connector requirements

Characteristic	Specification	Test specification reference
		IEC 60874-1 (IEC 61300)
Plug interface dimension		IEC 61754-6-2, Duplex plug connector interface-push/pull
Adapter interface dimension		IEC 61754-6-4, Duplex adapter connector interface-push/pull
Ferrule spacing	4.5 mm	–
Connector width	14 mm	–
Contact	2 per connector	–
Shielding		–
Modularity		
Polarization	Keyed	
Coupling	Push/pull	
(Mechanical operation) mechanical endurance	Requirements: – Attenuation: deviation from the initial value less than 0.2 dB – Return loss: more than 20 dB	IEC 61300-2-2 – Cycles: 500 – Specimen optically functioning – Preconditioning procedure: none – Recovery procedure: clean plug and adapter after every 25 matings – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

Table C.1 *(continued)*

Characteristic	Specification	Test specification reference
Cable pulling	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB – The specimen has no mechanical damage	IEC 61300-2-4 Magnitude: 70 N – Rate of application of the tensile load: 50 N/min < Load rate < 250 N/min – Point of application of the tensile load: 22 cm – 28 cm from the connector – Specimen optically non-functioning – Preconditioning procedure: clean plug and adapter before testing – Recovery procedure: none – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Cable torsion	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performancerequirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB – The specimen has no mechanical damage	IEC 61300-2-5 Tensile load: 5 N – Application of load: twist cable 2.5 turns in one direction with specified load applied, then twist it 5 turns in other direction and back 5 turns for 5 cycles – Point of application of the tensile load: 22 cm – 28 cm from the connector – Specimen optically non-functioning – Preconditioning procedure: none – Recovery procedure: none – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Strength of coupling mechanism	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB – The specimen has no mechanical damage	IEC 61300-2-6 – Magnitude: 70 N – Rate of application of the tensile load: 50 N/min < Load rate < 250 N/min – Point of application of the tensile load: 22 cm – 28 cm from connector – Specimen optically non-functioning – Preconditioning procedure: none – Recovery procedure: none – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

Table C.1 *(continued)*

Characteristic	Specification	Test specification reference
Vibration	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB – The specimen has no mechanical damage	IEC 61300-2-1 – Frequency range; 10 Hz – 55 Hz – Vibration amplitude: 0.75 mm constant displacement – Sweep time: 1 octave/min – Endurance duration per axis: 30 min – Method of mounting; an adapter shall be mounted rigidly to the mounting fixture – Specimen optically non-functioning – Preconditioning procedure: none – Recovery procedure: clean plug and adapter before final measurement – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Drop	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB – The specimen has no mechanical damage	IEC 61300-2-1 – Method: A – Number of drops: 5 – Drop height: 1 000 mm – Specimen optically non-functioning – Preconditioning procedure: with dust cap – Recovery procedure: clean plug and adapter before final measurement – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Engagement and separation force	Engagement force: max. 30 N Separation force: max. 30 N	IEC 61300-3-11 – Preconditioning procedure: none – Deviation: as necessary – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

Table C.2 – Performance and environmental specification for TS-FO and HS-FO (multimode) connector

Characteristic	Specification	Test specification référence
Attenuation	Less than 0.5 dB against reference plug In random connection Less than 0.75 dB (50 or 62.5/125 µm multimode fiber)	IEC 61300-3-4 – Method 7 – Equilibrium mode condition – Definitions of reference plug are as follows: • Ferrule outer diameter is 1.249 mm ± 0.0003 mm • Eccentricity of the fiber core with the outer diameter of the ferrule is less than 0.3 µm • Angular misalignment of ferrule is less than 0.2° • Eccentricity of spherical polished ferrule endface is less than 30 µm – Reference adapter shall be in accordance with IEC 61754-6-4; Duplex adapter connector interface-push/pull – Number of measurements to be averaged: 5 – Source: LD – Peak wavelength: 1.3 µm – Preconditioning procedure: the plug and adapter shall be cleaned
Return loss	More than 20 dB (50 or 62.5/125 µm multimode fiber)	IEC 61300-3-6 – Method 3 – Source: LD – Peak wavelength: 1.3 µm – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Cold	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss; more than 20 dB	IEC 61300-2-17 – Temperature: –10 °C – Duration: 96 h – Specimen optically functioning – Conditioning procedure: specimen lowered to test temperature and returned to room temperature at a rate not to exceed 1 °/min – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull – Monitoring method of attenuation and return loss shall be in accordance with IEC 61300-3-2

Table C.2 *(continued)*

Characteristic	Specification	Test specification référence
Dry heat	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss; more than 20 dB	IEC 61300-2-18 – Temperature: 60 °C – Duration: 96 h – Specimen optically functioning – Conditioning procedure: specimen raised to test temperature and returned to room temperature at a rate not to exceed 1°/min – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull – Monitoring method of attenuation and return loss shall be in accordance with IEC 61300-3-20
Damp heat (steady state)	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss; more than 20 dB	IEC 61300-2-19 – Temperature: 40 °C – Relative humidity: 90 % – 95 % – Duration: 4 days – Precautions regarding surface moisture removal: none – Specimen optically functioning – Conditioning procedure: Specimen raised to test temperature and returned to room temperature at a rate not to exceed 1°/min – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/ pull – Monitoring method of attenuation and return loss shall be in accordance with IEC 61300-3-2
Operation temperature	–10 °C to +60 °C	
Change of temperature (Test NA)	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB	IEC 61300-2-22 – Test method: NA – High temperature: 70 °C – Low temperature: –25 °C – Duration of extreme temperature: 30 min – Change over time: 0.5 min – Number of cycles: 5 – Specimen optically non-functioning – Preconditioning procedure: with dust cap – Recovery procedure: after test, specimens shall be maintained in room temperature condition for 2 h. Clean endface before final measurement – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

C.3 HS-FO single-mode connector

The HS-FO (single-mode) connector shall be implemented according to the table C.3 (interface specifications) and table C.4 (performance and environmental specifications) and be of dimensions specified in figures C.1 to C.2.

Table C.3 – HS-FO (single-mode) connector requirements

Characteristic	Specification	Test specification reference
	–	IEC 60874-1 (IEC 61300)
Plug interface dimension	–	IEC 61754-6-2, Duplex plug connector interface-push/pull
Adapter interface dimension	–	IEC 61754-6-4, Duplex adapter connector interface-push/pull
Ferrule spacing	4.5 mm	–
Connector width	14 mm	–
Contact	2 per connector	–
Shielding	–	–
Modularity	–	–
Polarization	Keyed	–
Coupling	Push/pull	–
Mechanical endurance (mechanical operation)	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss; more than 26 dB	IEC 61300-2-2 – Cycles: 500 – Specimen optically functioning – Preconditioning procedure: none – Recovery procedure: clean plug and adapter after every 25 matings – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Cable pulling	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 20 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB – The specimen has no mechanical damage	IEC 61300-2-4 Magnitude: 70 N – Rate of application of the tensile load: 50 N/min < Load rate < 250 N/min – Point of application of the tensile load: 22 cm – 28 cm from the connector – Specimen optically non-functioning – Preconditioning procedure: clean plug and adapter before testing – Recovery procedure: none – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

Table C.3 *(continued)*

Characteristic	Specification	Test specification référence
Cable torsion	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB – The specimen has no mechanical damage	IEC 61300-2-5 Tensile load: 5 N – Application of load: twist cable 2.5 turns in one direction with specified load applied, then twist 5 turns in other direction and back 5 turns for 5 cycles – Point of application of the tensile load: 22 cm – 28 cm from the connector – Specimen optically non-functioning – Preconditioning procedure: none – Recovery procedure: none – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Strength of coupling mechanism	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB – The specimen has no mechanical damage	IEC 61300-2-6 – Magnitude: 70 N – Rate of application of the tensile load: 50 N/min < Load rate < 250 N/min – Point of application of the tensile load: 22 cm – 28 cm from connector – Specimen optically non-functioning – Preconditioning procedure: none – Recovery procedure: none – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Vibration	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB – The specimen has no mechanical damage	IEC 61300-2-1 – Frequency range: 10 Hz – 55 Hz – Vibration amplitude: 0.75 mm constant displacement – Sweep time: 1 octave/min – Endurance duration per axis: 30 min – Method of mounting: an adapter shall be mounted rigidly to the mounting fixture – Specimen optically non-functioning – Preconditioning procedure: none – Recovery procedure: clean plug and adapter before final measurement – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

Table C.3 *(continued)*

Characteristic	Specification	Test specification reference
Drop	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB – The specimen has no mechanical damage	IEC 61300-2-1 – Method A – Number of drops: 5 – Drop height: 1 000 mm – Specimen optically non-functioning – Preconditioning procedure: with dust cap – Recovery procedure: clean plug and adapter before final measurement – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Engagement and separation force	Engagement force: max. 30 N Separation force: max. 30 N	IEC 61300-3-11 – Preconditioning procedure: none – Deviation: as necessary – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

Table C.4 – Performance and environmental specification for HS-FO (single-mode) connector

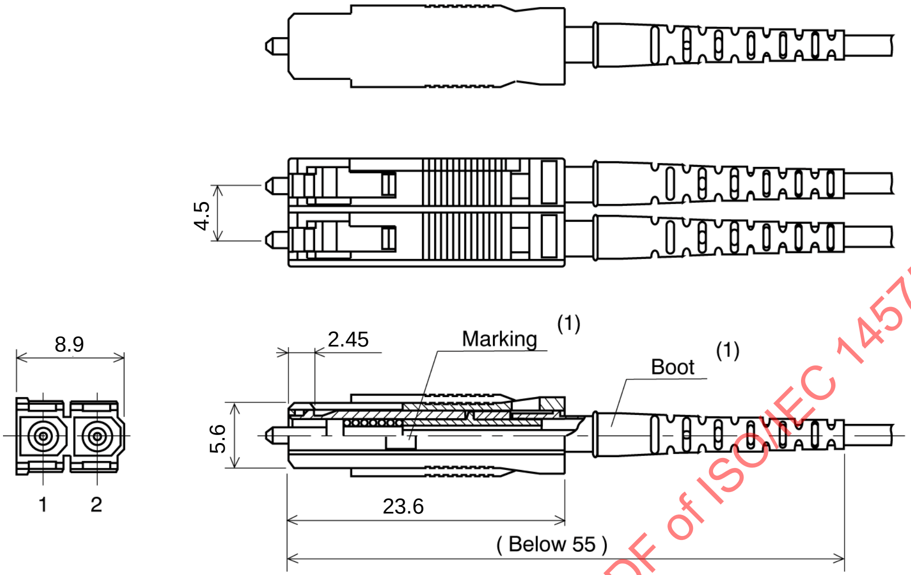
Characteristic	Specification	Test specification reference
Attenuation	Less than 0.5 dB against reference plug In random connection Untuned Less than 0.35 dB (average) Less than 0.75 dB (95 % probability) Tuned Less than 0.5 dB (average) Less than 0.5 dB	IEC 61300-3-4 – Method 7 – Definition of reference plug are as follows: • Ferrule outer diameter is 1.249 mm ± 0.0003 mm • Eccentricity of the fiber core with the outer diameter of the ferrule is less than 0.3 µm • Angular misalignment of ferrule is less than 0.2° • Eccentricity of spherical polished ferrule endface is less than 30 µm – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter connector interface-push/pull – Number of measurements to be averaged: 5 – Source: LD – Peak wavelength: 1.3 µm – Preconditioning procedure; the plug and adapter shall be cleaned
Return loss	More than 26 dB	IEC 61300-3-6 – Method 3 – Source: LD – Peak wavelength: 1.3 µm – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull
Cold	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss: more than 26 dB	IEC 61300-2-17 – Temperature: –10 °C – Duration: 96 h – Specimen optically functioning – Conditioning procedure; specimen lowered to test temperature and returned to room temperature at a rate not to exceed 1°/min – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull – Monitoring method of attenuation and return loss shall be in accordance with IEC 61300-3-20

Table C.4 *(continued)*

Characteristic	Specification	Test specification reference
Dry heat	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss, more than 26 dB	IEC 61300-2-18 – Temperature: 60 °C – Duration: 96 h – Specimen optically functioning – Conditioning procedure; specimen raised to test temperature and returned to room temperature at a rate not to exceed 1°/min – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull – Monitoring method of attenuation and return loss shall be in accordance with IEC 61300-3-20
Damp heat (steady state)	Requirements: – Attenuation; deviation from the initial value less than 0.2 dB – Return loss; more than 26 dB	IEC 61300-2-19 – Temperature: 40 °C – Relative humidity: 90 % – 95 % – Duration: 4 days – Precautions regarding surface moisture removal: none – Specimen optically functioning – Conditioning procedure: specimen raised to test temperature and returned to room temperature at a rate not to exceed 1°/min – Deviations: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull – Monitoring method of attenuation and return loss shall be in accordance with IEC 61300-3-2
Operation temperature	–10 °C to +60 °C	
Change of temperature (test NA)	Initial measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB Final measurement and performance requirements: – Attenuation; less than 0.75 dB – Return loss; more than 26 dB – The specimen has no mechanical damage	IEC 61300-2-22 – Test method: NA – High temperature: 70 °C – Low temperature: –25 °C – Duration of extreme temperature: 30 min – Change over time: 0.5 min – Number of cycles: 5 – Specimen optically non-functioning – Preconditioning procedure: with dust cap – Recovery procedure: after test, specimens shall be maintained in room temperature condition for 2 h; clean endface before final measurement – Deviation: none – Reference adapter shall be in accordance with IEC 61754-6-4, Duplex adapter interface-push/pull

C.4 TS-FO/HS-FO multimode and HS-FO single-mode connector dimensions

Annex R shows the recommended PCB footprint for the fixed connector and annex S the recommended fiber.



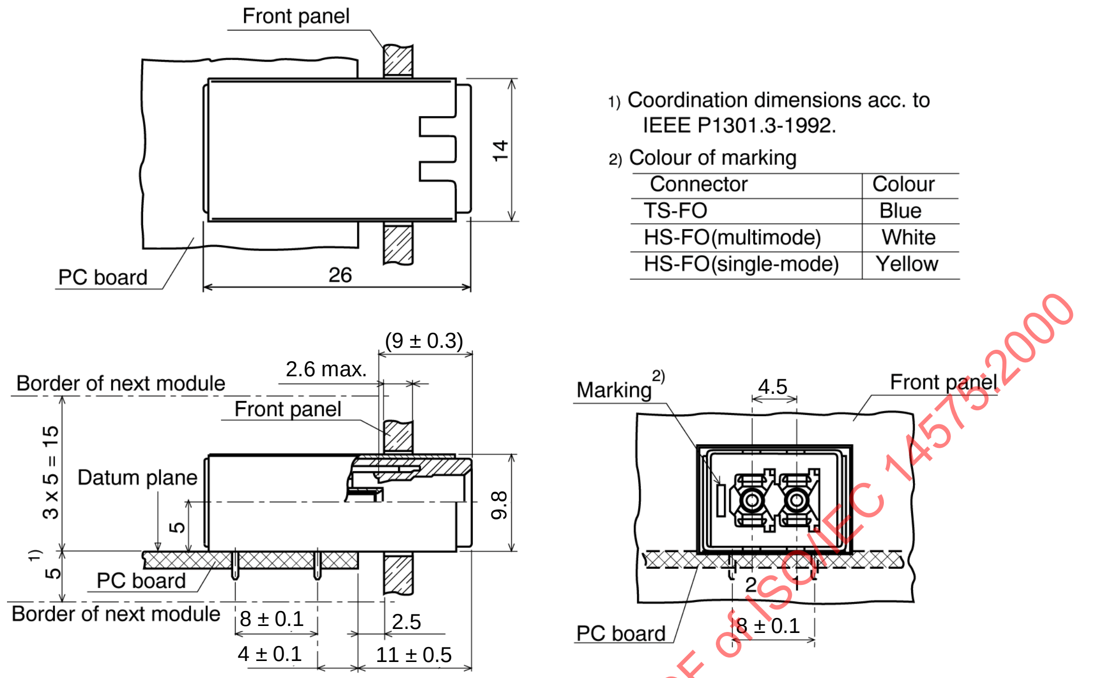
(1) Colour of marking and boot

Plug	Colour
TS-FO	Blue
HS-FO(multimode)	White
HS-FO(single-mode)	Yellow

All dimensions are in mm.

Dimensions in millimetres

Figure C.1 – TS-FO/HS-FO link free connector



Dimensions in millimetres

Figure C.2 – TS-FO/HS-FO link fixed connector

C.5 Color coding of connector

The connectors for TS-FO, HS-FO multimode and HS-FO single-mode are externally physically identical. In order to distinguish between the different types of connector, the keying mark on the fixed and free connectors shall be color coded as shown in table C.5.

Table C.5 – Color coding of TS/HS-FO connectors

Type of interconnect	Color
TS-FO	Blue
HS-FO multimode	White
HS-FO single-mode	Yellow

Annex D
(informative)

Rationale

D.1 Need for a new standard

It is widely recognized that the most economic way to build high-performance systems is by using parallelism. Parallel systems can provide very high computational power (in machines such as the CM-5 and the Parsytec GC-machine), fast response (for transaction processing or distributed control), very large I/O throughput (in RAID systems) and extremely high reliability (in redundant fault-tolerant systems). They also have the potential to be more maintainable and more expandable than conventional, monolithic systems.

The construction of high-performance systems with parallel processing and/or parallel I/O demands a fast, low-cost, low-latency interconnect. It must be fast and low-latency, otherwise it will be the limiting factor in system performance; and it must be low-cost, or it will dominate the system cost. It must also scale well in both performance and cost relative to the system size, otherwise highly parallel systems will be limited in performance or too expensive. Existing standards do not meet these criteria, either because they are designed for communication over long distances (which incurs high costs), or because they aim at the extreme of currently achievable performance (which again increases costs), or because they are based on a restricted model such as a bus, which limits overall performance and scalability.

The purpose of this new interconnect standard is to enable high-performance, scalable, modular, parallel systems to be constructed with low-cost, where "cost" must include not only the price of components, but also the engineering effort required to use them successfully. This International Standard specifies the physical connectors and cables to be used, the electrical/optical properties of the interconnect, and a cleanly-separated set of logical protocols to perform the interconnection in the simplest possible way.

D.2 Aspects of a parallel systems interconnect

D.2.1 Parallel interconnect

The requirements of performance, scalability and low-cost can be met in a way that is similar to the requirements of the whole parallel system: by allowing many instances of a cheap component to operate concurrently. Thus the interconnect should consist of many separate connections operating simultaneously to give a high aggregate performance. Provided each connection can be utilized at a reasonable level, its raw performance need not be very high, which allows both component and engineering costs to be kept down. For maximum simplicity, modularity, and fault-tolerance, each connection should be point-to-point.

The requirement of low-cost implies that, at the very least, a connection to the interconnect can be implemented with a relatively small amount of circuitry in a non-exotic technology. Ideally, such a connection could be integrated onto a chip with a processor or other device to minimize costs. The requirement of a small amount of circuitry implies that protocols must be simple and require minimal buffering. At the system level, cost limits the number of signal connections which can be used. Too large a number would make integration with a processor impractical; for example, would limit the maximum number of connections available on a device, and lead to skew-control problems at the system level.

D.2.2 Routing

To connect many devices together, it is not possible to provide a direct, physical connection between every pair. Nor is it acceptable to connect only certain pairs unless the connection pattern happens to match that required by the application. To enable every pair of devices to communicate without necessarily having a direct connection, data must be routed in some way through intermediate nodes.

In order for every pair of devices to be able to communicate, data must be routed in different ways at different times. This can be achieved either by configuring intermediate nodes to make each connection before the data is sent, or by making the data self-routing so that it contains within it information which determines which way it should be routed. Configuring the nodes in advance of the data requires that the destination of the data must be supplied to a central controller, which increases latency, and creates the danger that the controller will become a system bottleneck. Self-routed systems enable the control function to be distributed, and to scale in performance with the size of the system.

A piece of data together with its associated routing information is called a packet. If a packet is sent directly from sender to receiver, it is not necessary for the length of the packet to be represented within it; it is only necessary to ensure that the sender and receiver agree on the length. However, where packets pass through intermediate nodes, it must be possible for these nodes to determine the length of the packet passing through, to determine when the task of routing a particular packet is complete. The requirement of low-latency implies that packets must be limited in length, since otherwise connections could be occupied indefinitely by long packets. Since for many purposes short messages are required, the overhead on each packet must be small, and the packet size must be variable. This requires that the protocol provides an indication of the packet length, such as a termination marker or an initial length count.

D.2.3 Wormhole routing

In most serial packet-switching networks each intermediate node inputs a packet, decodes the header, and then forwards the packet to the next node. This is undesirable for a parallel systems interconnect for two reasons:

a) it requires storage in each node for transmitted packets, which either limits the capacity of the node or requires a separate memory (which increases costs).

b) it causes potentially long delays between the output of a packet and its reception, because each node waits for the whole packet to be received before starting re-transmission, thereby increasing latency.

A more suitable approach is wormhole routing, in which only the header of the packet is initially read in by the node. The routing decision is taken, the header is output, and the rest of the packet is sent directly from the input to the output without being stored in the node. This means that a packet can be passing through several nodes at the same time, and the head of the packet may be received by the destination before the whole packet has been transmitted by the source. Thus this method can be thought of as a form of dynamic circuit switching, in which the header of the packet, in passing through the network, creates a temporary circuit (the "wormhole") through which the data flows. As the tail of the packet is pulled through, the circuit vanishes (the analogy of an earthworm pushing its way through sand is very apt). The transmission of a single packet may thus be pipelined through a series of devices.

Note that, as far as the senders and receivers of packets are concerned, the wormhole routing is invisible. Its only effect is to minimize the latency in the message transmission. If one or more intermediate nodes were to store-and-forward the packet it would still be delivered correctly. Note also, however, that wormhole routing has the further advantage that it is independent of the packet length. In a store-and-forward system, the maximum packet size must be determined in advance so that buffering can be provided; if few packets are of this size, then the extra buffering is largely unused. In addition, independence from the packet length is desirable because it achieves a clean separation of layers of the protocol.

D.2.4 Flow control

Guaranteeing that physical connections will be available for each stage of a packet's journey requires global information about the state of the system. Accumulating global information is time-consuming and inherently non-scalable. Thus, in a low-latency, scalable system, the possibility exists that the header of a packet will be input by a node but be unable to proceed because the required output is already in use. The body of the packet will still be passing through previous nodes. There are then three possibilities:

a) the incoming packet body is buffered in the node where the packet is stalled;

b) the incoming data is discarded;

c) a flow-control mechanism stops the flow of data.

The first of these, a), is a return to store-and-forward routing, with the disadvantage of requiring buffer resources in each routing node. This increases cost and destroys the packet length independence of the routing. The second option, b), is undesirable because it forces the end-equipment to engage in complex protocols to deal with the possibility of data loss. In addition, once part of a packet has been lost the packet is probably useless and may as well be entirely destroyed. A system using this scheme could then easily degenerate into a state where most of the connections were carrying packets to the point of their destruction. Clearly it would be preferable to propagate information about a stall back along the path of the packet, and to implement a system of flow-control, as in c).

Rather than provide buffering for an entire packet, the flow-control system must be capable of stalling the flow of data part-way through a packet. This implies that it operates on a level below that of packets. It is the flow of the sub-units of which packets are composed which must be controlled. With this scheme, when a packet is unable to proceed, data may continue to move until all buffering along the path of the packet is filled. The flow-control mechanism must then ensure that data movement ceases so that no buffers are overwritten. This means that all links which are still occupied by the packet will be idle; however, this is an improvement on the previous scenario in which the links would be busy moving data to the point at which it is discarded.

D.3 Comparison with other types of system

In this subclause we consider how the requirements for a parallel system interconnect compares with those of other types of communication systems.

D.3.1 Telecommunications systems

The principal feature of digital telecommunications systems is they operate over long distances. This means the actual, physical medium of communication is large and expensive; most of the attributes of such systems are a consequence of this. Because the medium (ordinary cable, optical fiber or satellite, etc.) is expensive, it is worthwhile using expensive end-equipment to extract the most from it. It is justifiable to push the basic operating frequency to a level at which the bit-error rate (BER) is non-negligible and to compensate for errors with very sophisticated protocols if this results in a net improvement in data rate. Protocols may be further complicated by the need to perform a number of functions via the same medium, since in general there will not be an alternative connection (and if there were, it would not be economic to dedicate it only to functions which are used infrequently, however important).