INTERNATIONAL STANDARD

ISO/IEC 10859

First edition
1997-06

Information technology – 8-bit backplane interface: STEbus and mechanical core specifications for microcomputers

Technologies de l'information –
Interface de fond de panier 8 bits – Bus STE

Reference number
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FOREWORD

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committee established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 10859 was prepared by joint technical committee ISO/IEC JTC1, Information technology, SC 26: Microprocessor system.

This standard is a merging of IEEE Std 1000-1987 and IEEE 1101-1987. It has been submitted to the National Committees for vote under the Fast Track Procedure.

The numbering of the original clauses remains unchanged.

INTRODUCTION TO IEEE STANDARD FOR AN 8-BIT BACKPLANE INTERFACE: STEBUS

The initial concept for STEbus was to produce a European version of the STDBus using the Eurocard form factor with the DIN41612 connector. From that concept STE became known as STD-European.

When IEEE formed Working Group P1000 the brief specified a Standard 8-Bit Backplane Interface. At the inaugural meeting of Working Group P1000 it quickly became apparent that the opportunity was there to create a completely new, modern, high-performance 8-Bit bus, and all ideas of merely repinning the old STDbus were rapidly forgotten.

At the initial meeting of P1000 it was decided that the bus should be a part of the same family as VMEbus and Futurebus and as such should be an asynchronous bus with multimaster capability. Today it is often referred to as the baby brother of VMEbus. Unlike VMEbus though it was to be processor and manufacturer independent. This has proven to be an excellent decision as today there are many varied types of processor available on STEbus, from microcontrollers such as 8031, through Intel's 8085, 8088, and 80188; National Semiconductor's 32008 and 32016; Motorola's 6809, 68000, and 68008; Zilog's Z80 and Z280; Hitachi's 64180, and the Inmos Transputer with the promise of more to come.

A presentation was made to a packed audience at the IEE in London, England in early 1983. It met with critical acclaim. The first article about STEbus was also published about this time in an international magazine (EDN May 26, 1983).

Work continued internationally and in late 1984 Draft D3.1 was produced. This draft eradicated the daisy-chain bus request mechanism of D2.0 in favour of a simple solution that allowed position independence of cards in the rack.

This was the first firm specification and encouraged more manufacturers to look at the bus seriously. Among them were BICC-Vero, a major manufacturer of Eurocard enclosures and backplanes, and British Telecom, the UK's Telephone Utility. Market ground zero was early 1985 and since this time the number of manufacturers has continued to grow from 18 companies in Spring 1986 to more than 30 in mid-1987, with over 700 products available.

Much credit and praise is due Tim Elsmore who first conceived the idea for STEbus during his employment with GMT Electronic Systems Ltd. Paul Borrill was instrumental in negotiating with IEEE the formation of Working Group P1000 and Bill Shields was appointed Chairman.

This standard was prepared by Working Group P1000 of the Microprocessor Standards Committee.

Information technology – 8-bit backplane interface: STEbus and mechanical core specifications for microprocessors

1 General

1.1 *Scope*

The overall level of performance that may be achieved by any computer system is determined, in large part, by the system bus that is used to effect communication between the various system elements. System performance characteristics, measured in terms of speed, reliability, suitability to a variety of purposes, and adaptability to changing technology are ultimately dependent on the particular bus structure that is used and its associated protocols.

This standard defines the IEEE Std 1000 Bus, which may be used to implement general purpose, high-performance 8-bit microcomputer systems. Such a system may be used in a stand-alone configuration, or in larger multiple-bus architectures, as a private (or secondary) bus or a high-speed I/O channel. This standard is applicable to those systems and system elements with the common commercial designation STEbus. It is intended for those users who plan to evaluate, implement, or design various system elements that are compatible with the IEEE 1000 Std Bus system structure.

The physical attributes and method of interconnect utilized by boards and modules conforming to this standard are derived from several International Electrotechnical Commission (IEC) standards. These standards, when implemented jointly in a systems environment, result in a mechanical configuration commonly referred to as *Eurocard.* Appendix B lists such applicable standards which, where referenced, are considered as if incorporated with this standard. In particular, the connector used by IEEE Std 1000 Bus boards is a 64-pin male connector utilizing the outside two rows (designated *a* and c rows), specified in IEC 60603-2, and the mating female connector is used on IEEE Std 1000 Bus backplanes. The recommended size for IEEE Std 1000 Bus boards is 100 mm × 160 mm (3,937 in × 6,299 in), commonly referred to as a *single height standard depth* Eurocard.

The IEEE Std 1000 Bus structure is based on the master-slave concept in which a master, having gained control of the bus, may address and command slaves. Masters and slaves communicate with each other by use of an asynchronous interlocked handshake protocol. This technique allows for the construction of computer systems that incorporate devices of widely varying speeds. Multiple masters may be implemented within a single system.

Two independent address spaces are supported: memory and I/O. Memory transactions reference a 1 megabyte physical address space, while I/O transactions reference a 4 kilobyte physical address space. System integrity during all such transactions is enhanced by provision of a transfer error signal.

Provision is made for interboard condition alerts such as interrupt requests, DMA requests, system-specific error conditions, or other specialized status conditions. Within this scheme eight prioritized attention request levels, each with vectored response capability, are available for user assignation.

This standard deals only with those characteristics that must be specified so as to ensure the successful design and implementation of compatible boards and systems. Issues relating to individual design specifications, and performance or safety requirements are not addressed.

1.2 *Features*

The fundamental features offered by IEEE Std 1000 Bus are as follows:

8-bit Data Field Width

1 Megabyte Memory Address Range

4 Kilobyte I/O Address Range

Asynchronous Data Transfer

Transfer Error Signal

Multiple Masters

Eight Attention Request Lines

IEC 603-2 Connector

Single or Double Eurocard Boards and Modules

5 V, ±12 V and Standby Power Supply Distribution

Total Position Independence of Boards and Modules in Backplane

Total Inter-Board Compatibility

Total Central Processing Unit (CPU) Generic Device Family Independence

Potential 5 Megabyte per Second Data Transfers

1.3 *Objects*

This standard is intended to

1) define a general purpose microcomputer board interface;

2) specify those device-independent electrical, mechanical, and functional interface parameters that must be met so as to effect unambiguous communication between system elements and to effect physical compatibility;

3) specify the terminology and definitions related to the specification;

4) enable the interconnection of a wide variety of independently manufactured boards within a single functional system;

5) define a standard that places the minimum number of restrictions on the performance characteristics of boards within a conforming system;

6) allow microcomputer system users of relatively modest experience to assemble modularly expandable computer systems with a high probability of success.

1.4 *Definitions*

The following general definitions apply throughout this standard. Additional detailed definitions are given where appropriate.

1.4.1 *General system terms*

compatibility: The degree to which boards may be interconnected and used without modification when designed according to the specifications contained within this standard.

interface: A shared boundary between two or more systems, or between two or more elements within a system, through which information is conveyed.

interface system: The device-independent electrical, mechanical, and functional interface elements required for unambiguous communication between two or more devices. Typical elements include:

- driver and receiver circuitry;
- signal line descriptions;
- timing and control conventions;
- communication protocols;
- functional logic circuits.

system: A set of interconnected boards that achieve a specified objective by the performance of designated functions.

1.4.2 *Signals and paths*

address: The reference to a unit of data or the value represented by the address lines while ADRSTB* is active.

addressed board: A board that recognizes its address while ADRSTB* is active.

arbitration: The means whereby masters compete for control of the bus and the process by which a master is granted control of the bus.

backplane: A printed circuit board (pcb) on which connectors are mounted, into which boards or plug-in units are inserted.

block transfer: A sequence of data transfers, in the same direction, that occur during a single bus transaction.

board: A printed circuit board (pcb) that complies with this standard.

bus: A signal line or set of lines used by an interface system to connect a number of devices, and over which information is conveyed.

byte: A set of eight signals, individually referred to as bits, which are operated on as a unit.

handshake: An interlocked sequence of signals between interconnected boards in which each board waits for an acknowledgement of its previous signal before proceeding.

high state: The more positive voltage level used to represent one of two logical binary states.

low state: The more negative voltage level used to represent one of two logical binary states.

module: A plug-in unit consisting of one or more boards that contains at least one bus interface conforming to this standard, which plugs into the backplane.

protocol: The signalling rules used to convey information or commands between boards connected to the bus.

release: The action of a transmitter in ceasing to hold a signal line in the asserted state.

sequence: An indivisible bus transaction comprising one or more transfers.

settling time: The time taken for a signal line to settle unambiguously to a logical state when making a transition from one state to another.

signal: The physical representation of data.

signal level: The relative magnitude of a signal when considered in relation to an arbitrary reference. The unit of representation used within this standard is the volt.

signal line: One of a set of signal conductors in an interface system used to transfer data among interconnected boards.

signal parameter: That element of an electrical quantity whose values or sequence of values convey information.

tenure: The time during which a master has control of the bus.

transaction: The combination of data transfer sequences controlled by a master during a single bus tenure.

transfer: The movement of a single byte of data from the current master to the addressed slave(s) or from the addressed slave to the master.

1.4.3 *Generic signal names*

Throughout this standard bus request and acknowledge signals and attention request signals are sometimes referred to as BUSRQ*n**, BUSAK*n**, and ATNRQ*n** respectively. Such general references are equivalent to specific references RUSRQ0* or BUSRQ1* etc.

1.4.4 *Notation for bus signals*

Throughout this standard signals on a particular bus are referred to collectively using the form A<19..0>. This notation should be taken as an abbreviation of all of the address bus signals from A19 through to A0 inclusive.

In addition to the address bus signals, the notation is also used for the data lines (for example, D<7..0>), the common lines (for example, CM<2..0>), the attention request lines (for example, ATNRQ<7..0>*), the bus request lines (for example, BUSRQ<1..0>*) and the bus acknowledge lines (for example, BUSAK< 1..0 >*).

1.5 *Logical and electrical state relationships*

Throughout this standard the term *asserted* is used to indicate the logical true state of the particular signal referenced. The corresponding term *negated,* however, is not used because it comprises a potentially ambiguous representation when describing signals, which may be low or high true.

All signals that are low in their asserted state are designated by a nathan (asterisk), which follows the signal name (for example, ADRSTB*). The correlation between the terms true:false, high:low, and asserted:released is demonstrated in the following table, utilizing the signals ADRSTB* and CM<2..0> as an example.

Function	Electrical	Logical	State
CM<2..0>	High	1 True	Active, asserted
	Low	0 False	Active, released
	High Z	–	Inactive
ADRSTB*	Low	1 True	Active, asserted
	High	1 False	Active, released
	High Z	–	Inactive

2 Functional description

This section describes the functional elements of IEEE Std 1000 Bus interface. They are

1) System Controller
2) Arbiter
3) Masters
4) Slaves

An individual board attached to IEEE Std 1000 Bus backplane may consist of one or more of these elements.

2.1 *System controller*

Within any IEEE Std 1000 Bus system there shall be one, and only one, system controller. The system controller provides essential facilities for the proper operation of IEEE Std 1000 Bus systems. The system controller may be combined on a board with a master.

The system controller shall provide as a minimum the following requirements:

1) SYSCLK. A general-purpose clock signal in accordance with the specifications detailed in Section 3 of this standard.

2) SYSRST*. An initial power-on system reset signal in accordance with the specifications detailed in Section 3 of this standard.

3) TFRERR*. A transfer error signal in accordance with the specifications detailed in Section 3 of this standard.

2.2 *Arbiter*

All bus allocation grants shall be provided by the arbiter in accordance with the protocol described in Section 4 of this standard. There shall be one, and only one, arbiter within any IEEE Std 1000 Bus system. The arbiter may be combined on a board with a master.

2.3 *Masters*

A master is a board that is capable of controlling the transfer of data on the bus, by means of the protocols defined in Sections 4 and 5 of this standard. A master may contain a central processing unit (cpu) or logic necessary to transfer data over the bus (for example, DMA controller).

2.3.1 *Master types*

All masters must request allocation of IEEE Std 1000 Bus from the arbiter before they can control data transfers except in the special case of a default master.

default master: A master that is allocated control of the bus by the arbiter whenever the bus is not in use by another master. A default master is necessarily combined with the arbiter on the same board and has the lowest priority for bus allocation. There can be only one default master within a IEEE Std 1000 Bus system, though a IEEE Std 1000 Bus system need not include a default master.

All other masters (termed potential masters) request allocation of bus control from the arbiter. This request shall be made by asserting one of the two bus request *(BUSRQn*)* lines, or in the case of a master that is on the same board as the arbiter but is not configured as a default master, by asserting a third bus request line that is private to that board.

Multiple masters may exist within a system. The master's priority for bus control allocation and the means by which such allocation is accomplished are as described in Section 4.

2.3.2 *Master modes*

Masters may retain control for a period of time constrained only by the specific system requirements. Two modes of operation may be used by masters.

1) *Release-when-done.* The master retains control of the bus until all desired transfers have been accomplished.

2) *Release-on-request.* The master retains control of the bus indefinitely, relinquishing control when it determines that another master requires allocation of the bus. This determination may be made by several methods including receipt of an attention request signal, hardware polling, or by detection of a *BUSRQn** signal becoming active.

NOTE – By definition a default master always operates in release-on-request mode.

2.4 *Slaves*

Boards that are capable of being controlled over the IEEE Std 1000 Bus are designated slaves. Slaves decode the address lines and act upon the command provided by the current master. A slave may be combined with other functional elements on a board (for example, a board that contains both a master and memory that is accessible by other masters within the system).

Figure 1 shows one possible system configuration that utilizes a variety of boards in combination.

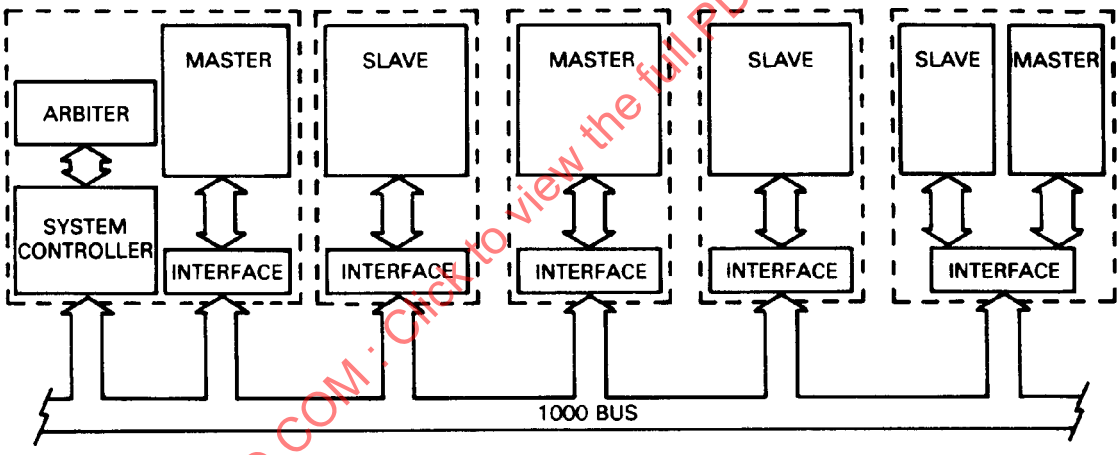


Figure 1 – Example of system configuration

3 Signal lines

This section provides specific definitions for all signal lines that are part of the IEEE Std 1000 Bus. Each of these signals has been assigned to one of five functional groups. These groups are

(1) Information Lines
  (a) Address Lines
  (b) Data Lines
  (c) Command Lines
(2) Synchronization Lines
(3) Attention Request Lines
(4) Bus Allocation Lines
(5) Utility lines

3.1 *Information lines*

3.1.1 *Address lines (A<19..0>)*

These unidirectional lines specify the address of the referenced memory or I/O location or, during a *vector fetch* response to an attention request, the level of the request being acknowledged. The most significant bit is A19 and A0 is the least significant.

The following table details the usage of the address lines during various types of operations.

Operation	Valid lines	Total addressed range
Memory read or write	A<19..0>	1 048 576 bytes
I/O read or write	A<11..0»	4 096 locations
Vector-fetch	A<2..0»	8 levels

3.1.2 *Data lines (D<7..0>)*

These eight bidirectional lines carry information between masters and slaves. The most significant bit is D7 and D0 is the least significant.

3.1.3 *Command lines (CM<2..0>)*

These signals are used by the current master to convey coded data to the slave describing the type of the current data transfer according to table 1.

Command codes marked *reserved* shall not be used, and IEEE Std 1000 boards shall not respond to or utilize these codes for any purpose so as to be considered in compliance with this standard. This is to guarantee compatibility with boards that may be designed to conform to future revisions of this standard.

Table 1 – Command codes

CM2	CM1	CM0	Transfer
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Vector-fetch
1	0	0	I/O write
1	0	1	I/O read
1	1	0	Memory write
1	1	1	Memory read

3.2 *Synchronization lines*

The following signals are classified as synchronization lines:

Signal	Function
ADRSTB*	Address strobe
DATSTB*	Data strobe
DATACK*	Data transfer acknowledge
TFRERR*	Transfer error

3.2.1 *Address strobe (ADRSTB*)*

This signal indicates the presence of valid data on the address lines.

3.2.2 *Data strobe (DATSTB*)*

This signal indicates the presence of valid data on the command lines CM<2..0>. During a read, or vector-fetch transfer, this signal indicates that the addressed slave may place data on the data lines. During a write transfer this signal indicates the presence of valid data on the data lines.

3.2.3 *Data transfer acknowledge (DATACK*)*

This signal is used to indicate to the master that the command has been performed: that data have been placed on, or accepted from, the data lines.

3.2.4 *Transfer error (TFRERR*)*

This signal may be asserted by any board to indicate an error during the current transfer. Specific timing requirements for this signal are detailed in Section 5 of this standard.

3.3 *Attention request lines (ATNRQ<7..0>*)*

These signals are configured for indicating user-specific events when a IEEE Std 1000 Bus system is commissioned. Such events may include, but are not limited to, interrupt requests, DMA requests, or notification of conditions, which exist either at the board or system level (for example, failure). Eight attention request lines are available. Three optional response protocols are described in Section 6 of this standard for the use of attention request lines as traditional interrupts.

These signals may be used by any board to request the attention of other boards within IEEE Std 1000 Bus systems. Any board within the system may be connected to any of the eight attention request lines. Multiple boards may be connected to the same attention request line allowing for the broadcast of events to one or more boards within a system. There is an implied priority with ATNRQ7* having highest priority and ATNRQ7* having the lowest.

3.4 *Bus allocation lines*

The bus allocation lines are:

Signal	Function
BUSRQ<1..0>*	Bus request lines
BUSAK<1..0>*	Bus acknowledge lines

3.4.1 *Bus request lines (BUSRQ<1..0>*)*

These signals may be asserted by any potential master that desires allocation of the IEEE Std 1000 Bus. In systems utilizing prioritized arbitration, BUSRQ0* shall have priority over BUSRQ1*.

3.4.2 *Bus acknowledge lines (BUSAK<1..0>*)*

These signals are used by the arbiter to indicate to a master requesting bus allocation that it may take control of the bus. BUSAK1* indicates a grant to the master requesting by way of BUSRQ1*, and BUSAK0* indicates a grant to the master requesting by way of BUSRQ0*.

3.5 *Utility lines*

The following signals are classified as utility lines:

Signal	Function
SYSCLK	System clock
SYSRST*	System reset

3.5.1 *System clock (SYSCLK)*

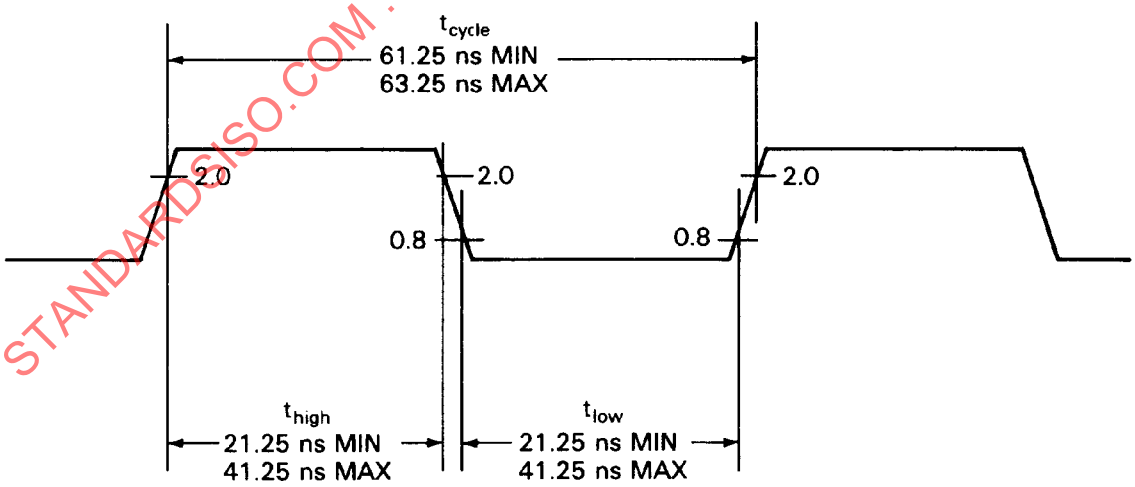
The system clock is a periodic signal of constant frequency that may be used as a generalized facility by masters or slaves. The system clock is independent of the protocol of any other bus signals, and is provided by the system controller. Figure 2 contains timing waveforms for SYSCLK.

3.5.2 *System reset (SYSRST*)*

The system reset signal is used to place the system in a known initial state. While SYSRST* is active all boards shall inhibit any access to the system bus. SYSRST* may be driven by any board. It is recommended that during a power-up sequence, any board capable of performing on-board diagnostic self-tests hold SYSRST* active until the successful completion of such tests.

The system controller shall provide an initial power-on system reset signal that is not <200 ms and not >500 ms in duration, measured from the point at which the +5 V d.c. supply reaches its designated minimum specification (see Section 7). The system controller also shall assert SYSRST* at any time that the system supply falls below its minimum specified tolerance, and shall continue to assert it for the entire period during which the supply is out of tolerance. The rise time of this signal shall not exceed 100 ns (10 %-90 %).

A recommended power-fail protocol, for implementation of systems where an early indication of primary power supply failure is available, is provided in Section 7.



t_{cycle} = 62,5 ns ± 1 ns (16,00 MHz)

t_{high} = 31,25 ns ± 10 ns

t_{low} = 31,25 ns ± 10 ns

Figure 2 – SYSCLK timing

3.6 *IEEE Std 1000 Bus connector pin allocations*

3.6.1 *Connector type*

The IEEE Std 1000 Bus connector pair shall be C064 from IEC 60603-2. The male connector shall be on the board and the female connector shall be on the backplane.

3.6.2 *Connector pin allocation*

The allocation of the signals described in this standard to pins on the IEEE Std 1000 Bus connector are in figure 3.

The backplane tracking arrangement shown is recommended so as to allow the signal 0 V return traces to provide guard track protection between strobes and signal sets.

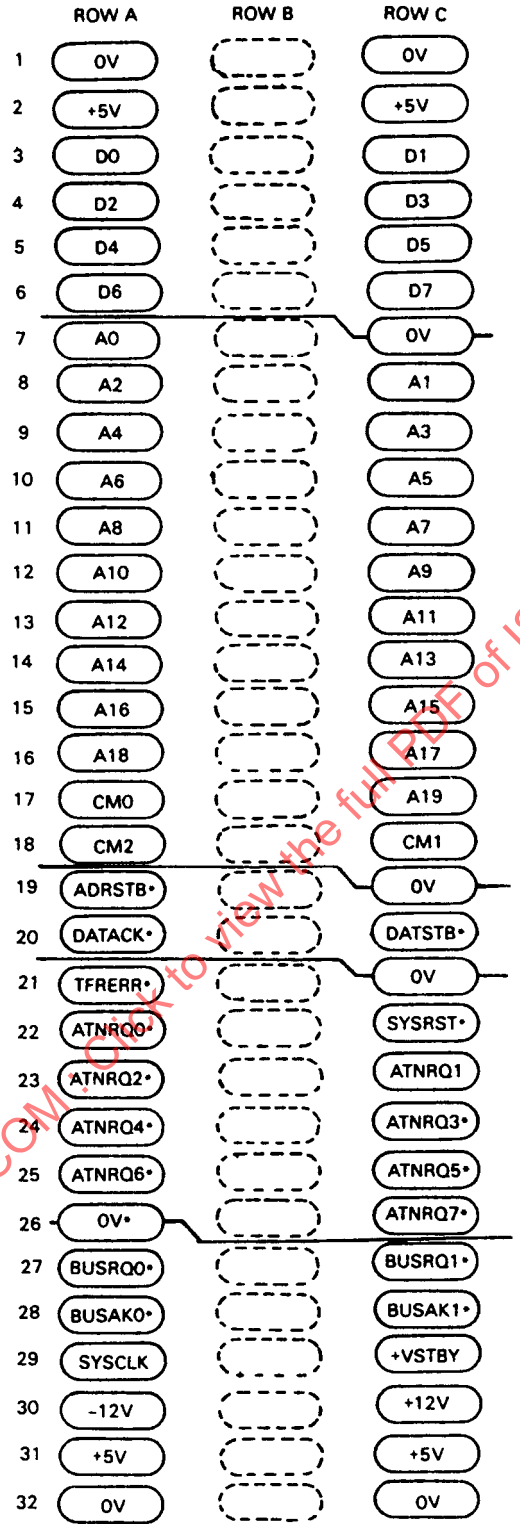


Figure 3 – IEEE Std 1000 Bus connector

4 Arbitration

This section defines the protocol that is used by IEEE Std 1000 Bus masters to gain control of the IEEE Std 1000 Bus.

The following signals are used to effect allocation of bus control within IEEE Std 1000 Bus systems:

BUSRQ<1..0>*

BUSAK<1..0>*

4.1 *Arbitration algorithm*

On power-up, or following a system reset, the arbiter shall have control of the bus. All masters (except default masters) must request and receive a control allocation grant from the arbiter prior to controlling the bus. Only the arbiter may effect a change in allocation of bus control within an IEEE Std 1000 Bus system.

Any algorithm may be used by the arbiter to determine which of the bus request levels will be granted when the current master releases the bus, although, by convention, the BUSRQ0*/BUSAK0*, request/grant pair have priority over BUSRQ1*/BUSAK1*. The arbiter may award preference to one requesting level on a priority basis, a *round-robin* basis, or by means of any other algorithm implementable within the control transfer protocol.

4.2 *Bus requests*

A Bus request may be initiated by any master within an IEEE Std 1000 Bus system at any time by asserting one of the BUSRQ* lines. Bus requests are level-triggered, meaning that a requesting condition is indicated by the relative voltage level present on a BUSRQ*n** line rather than by the active transition from one state to another.

A master, having asserted one of the BUSRQ*n** lines, shall continue to assert it for the entire period during which it desires to control the bus.

NOTE – Multiple masters may be connected to a single BUSRQ*n** line only when it can be assured that more than one master cannot request the bus at the same time, on the same requesting level.

4.3 *Bus grants*

BUSAK0* or BUSAK1* are asserted by the arbiter in response to the corresponding requests, BUSRQ0* and BUSRQ1*. The arbiter shall not assert either of these grant lines in the absence of a corresponding bus request. In addition, the arbiter shall not assert both bus acknowledge lines simultaneously under any circumstances.

A master asserting a bus request line and detecting the corresponding bus acknowledge line asserted may assume control of the bus. The arbiter, having asserted a bus acknowledge line, shall continue to assert it for the entire period during which the current master continues to assert the corresponding bus request line.

4.4 *Control allocation sequence*

Figure 4 shows the handshake-signal flow during an allocation of bus control. The sequence of events for all allocations of bus control shall conform to the following description:

A master may request allocation of the IEEE Std 1000 Bus at any time by asserting one of the BUSRQ* lines except that a master may not assert BUSRQ*n** until the corresponding BUSAK*n** has been released from a previous cycle.

The arbiter, upon detecting BUSRQ*n** active, and having first assured that the bus is available, shall assert BUSAK*n** indicating that the bus is available for use by the requesting master. The arbiter shall not assert BUSAK*n** in the absence of a corresponding BUSRQ*n**. The bus is available for arbitration if the arbiter is not issuing a bus grant to any master, either by asserting BUSAK*n** or by granting to the bus to its own on-board master (if one is present).

The requesting master, upon detecting that BUSAK*n** has been made active, shall assume control of the bus.

Upon completing the desired data transfer sequences, the current master shall cease driving all bus lines and shall then release BUSRQ*n**.

The arbiter, upon detecting that the BUSRQ*n** is no longer asserted, shall release BUSAK*n**.

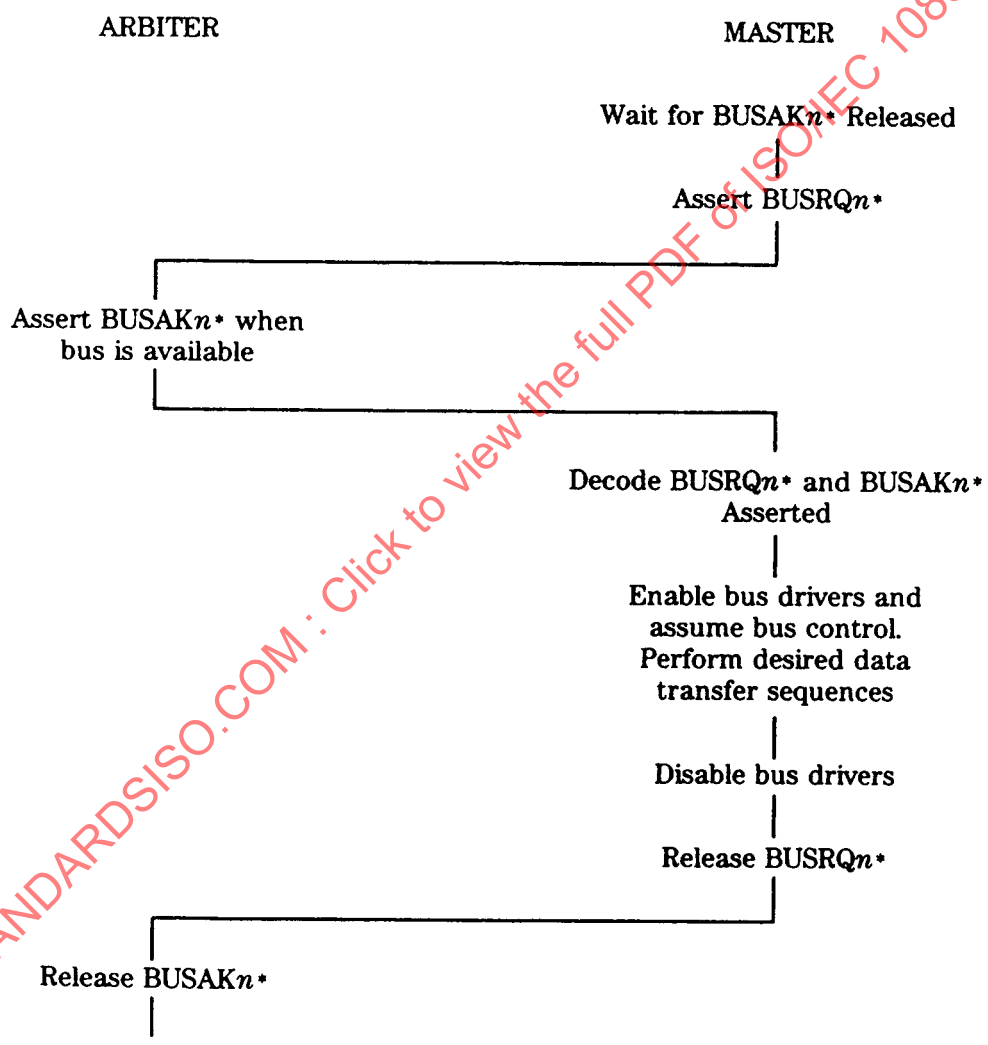


Figure 4 – Control transfer flow diagram

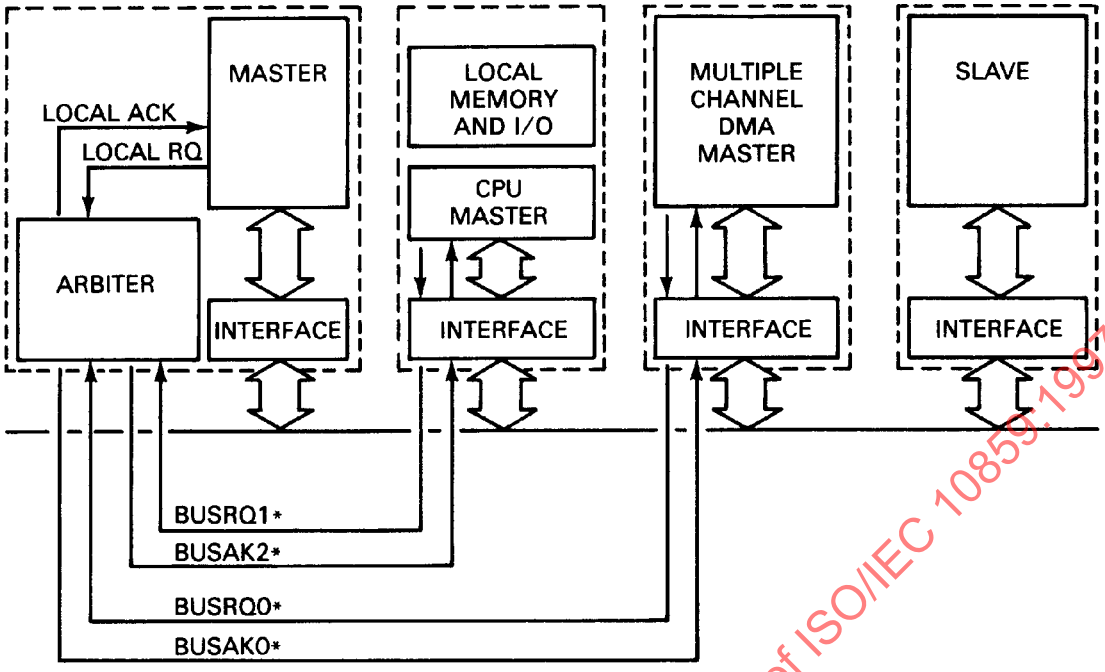


Figure 5 – Example of multiple master implementation

5 Data transfer protocol

This section defines the protocol and timing requirements necessary to effect data transfer sequences across the IEEE Std 1000 Bus. All data are transferred as single bytes using an asynchronous interlocked handshake. The asynchronous nature of the protocol allows communication between masters and slaves of widely differing speeds, and is essentially self-adaptive to changing system configurations.

Indivisible read-modify-write sequences are accommodated within the protocol, allowing synchronization of tasks in a multiple processor system by use of lock variables.

A high-speed *burst* mode of data transfer is also specified, allowing for rapid movement of contiguous data blocks between boards.

Figure 6 illustrates the various types of sequences accommodated by the IEEE Std 1000 Bus data transfer protocol.

The signals used for data transfer sequences are

Signal	Source
A<19..0>	Master
D<7..0>	Master during write, slave during read, and vector-fetch
CM<2..0>	Master
ADRSTB*	Master
DATSTB*	Master
DATACL*	Slave
TFRERR*	Any board

Throughout this section the word *master* implies current master, that is, it is assumed that the master discussed has been allocated control of the IEEE Std 1000 Bus by means of the protocol described in Section 4 of this standard.

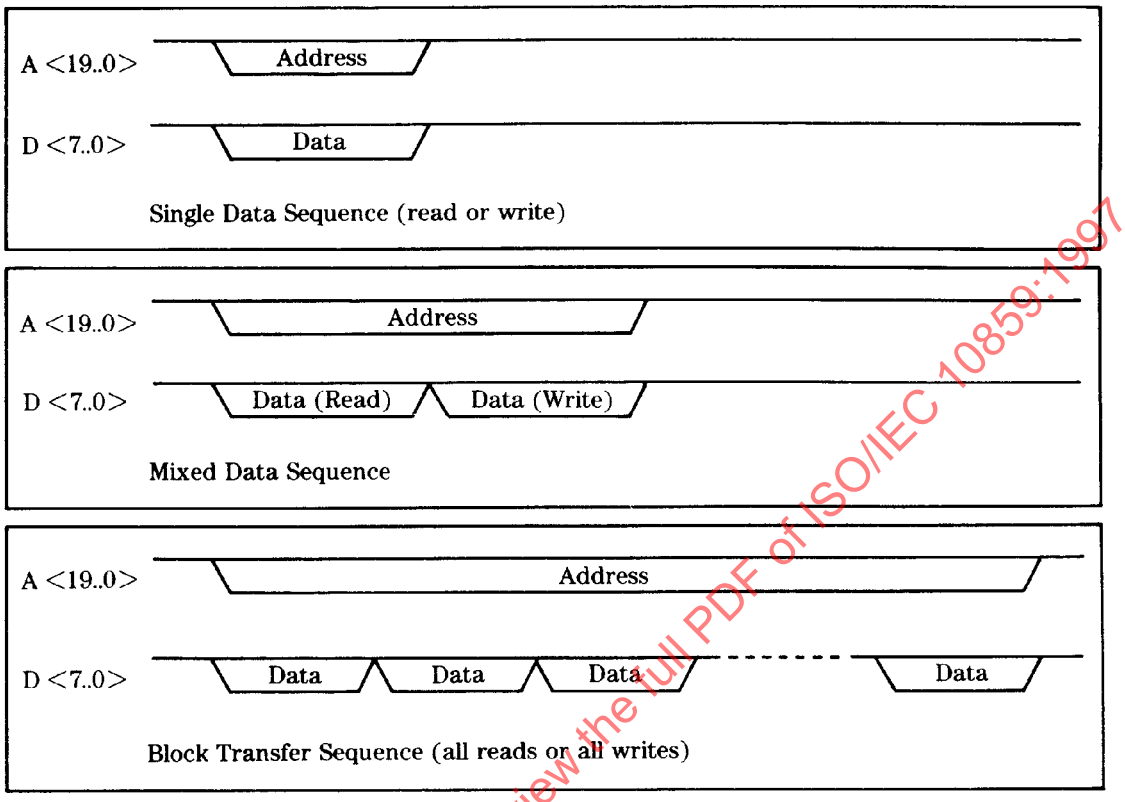


Figure 6 – IEEE Std 1000 Bus data transfer sequences

5.1 *Read sequence*

Data transfers from slave to master are designated read sequences. Figure 7 illustrates the handshake-signal flow, and figure 10 specifies the signal timing parameters for a read sequence. Read sequences shall conform to the following description:

1) The master places the address of the targeted memory or I/O location on the address lines.

NOTE – The master may assert the appropriate command code at this time.

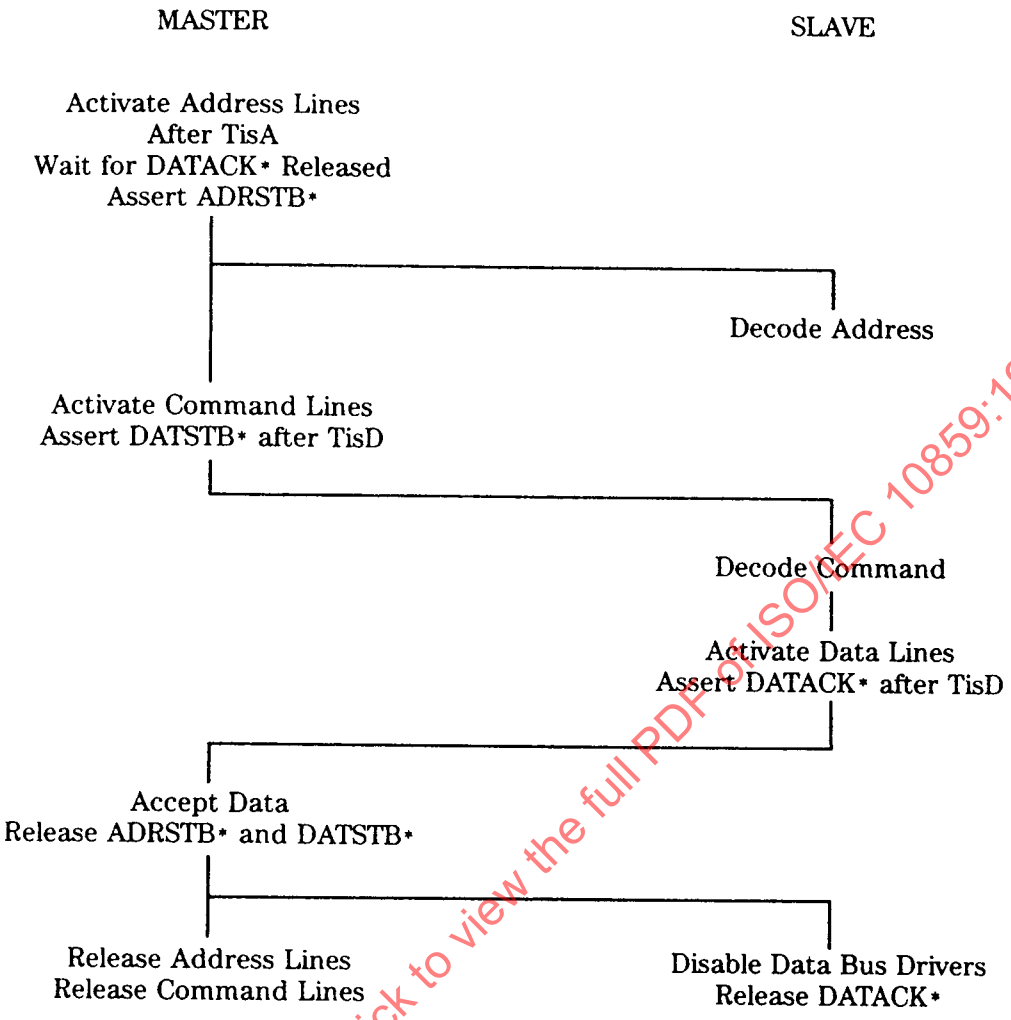


Figure 7 – Read sequence flow diagram

2) After a setup time, during which the address lines become valid, and having ensured that DATACK* is released from the previous cycle, the master shall assert ADRSTB*.

3) The master shall activate the command lines, CM<2..0>, to indicate the type of transfer.

CM2	CM1	CM0	Transfer
1	0	1	I/O read
1	1	1	Memory read

4) After a setup time during which the command lines become valid, the master shall assert DATSTB* indicating the presence of valid data on the command lines, and that it is ready to accept data.

5) The addressed slave shall enable its data bus drivers, placing requested data on the data lines.

6) After a setup time, during which the data lines become valid, the addressed slave shall assert DATACK* indicating that the data is available.

7) In response to DATACK* the master shall accept the data and shall release DATSTB* indicating to the slave that it must remove the data from the data lines.

8) Upon detecting either DATSTB* or ADRSTB* released, the slave disables its data bus drivers and releases DATACK* indicating that the sequence is complete.

5.2 *Write sequence*

Data transfers from masters to slaves are designated write sequences. Figure 8 illustrates the handshake signal flow, and figure 11 specifies the signal timing parameters for a write sequence. Write sequences shall conform to the following description:

1) The master places the address of the targeted memory or I/O location on the address lines.

NOTE – The master may assert the appropriate command code at this time.

2) After a setup time, during which the address lines become valid, and having ensured DATACK* is released from the previous cycle, the master shall assert ADRSTB*.

3) The master shall activate the command lines, CM<2..0>, to indicate the type of transfer, and shall place the data to be transferred on the data lines.

CM2	CM1	CM0	Transfer
1	0	0	I/O write
1	1	0	Memory write

4) After a setup time, during which the data lines and the command lines become valid, the master shall assert DATSTB* indicating the presence of valid data on the data and command lines.

5) The addressed slave shall accept the data and shall assert DATACK* to indicate that the transfer may be terminated.

6) In response to DATACK* the master shall release ADRSTB* and DATSTB*.

7) Upon detecting either DATSTB* or ADRSTB* released, the slave shall release DATACK* indicating that the sequence is complete.

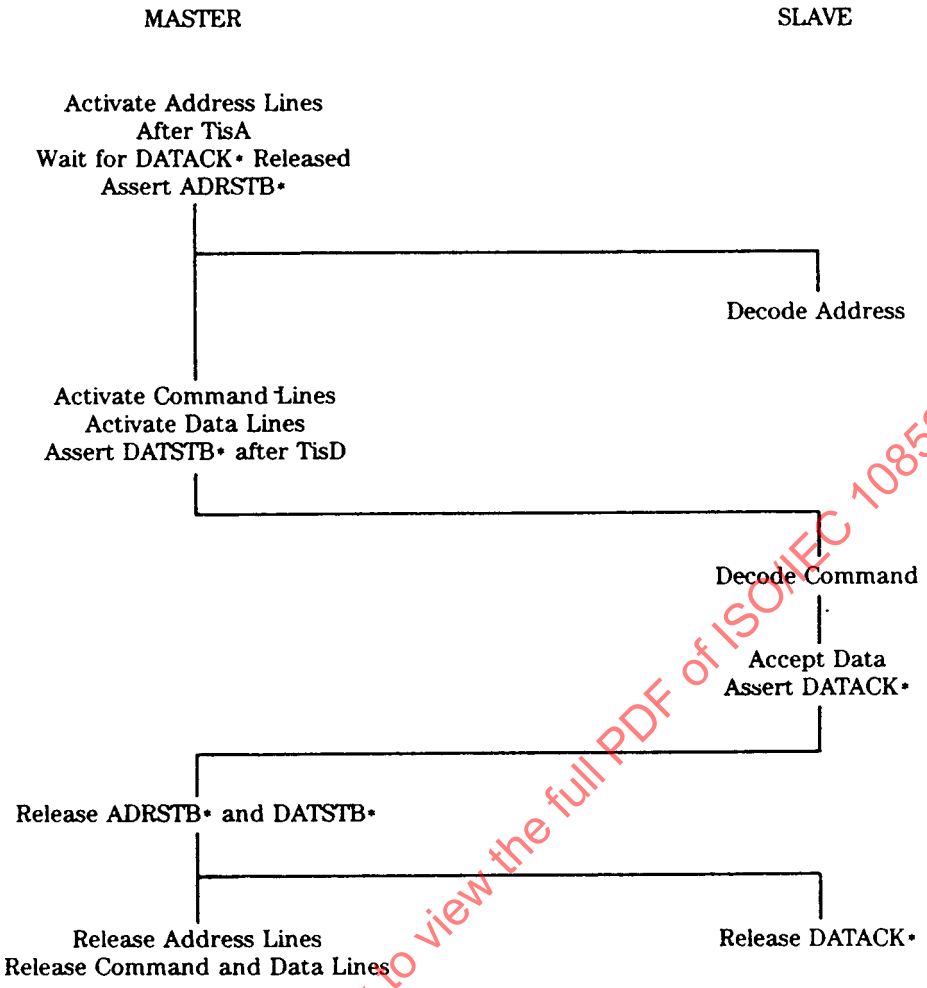


Figure 8 – Write sequence flow diagram

5.3 *Read-modify-write sequence*

Sequences during which the data is transferred to the master, operated on by the master, and subsequently transferred from the master to the same address, in a single indivisible sequence are designated read-modify-write sequences. Figure 9 illustrates the handshake signal flow, and figure 12 specifies the signal timing parameters for a read-modify-write sequence. Read-modify-write sequences shall conform to the following description:

1) The master places the address of the targeted memory or I/O location on the address lines.

NOTE – The master may assert the appropriate command code at this time.

2) After a setup time, during which the address lines become valid, and having ensured DATACK* is released from the previous cycle, the master shall assert ADRSTB*.

3) The master shall activate the command lines, CM<2..0>, to indicate the type of transfer.

CM2	CM1	CM0	Transfer
1	0	1	I/O read
1	1	1	Memory read

4) After a setup time during which the command lines become valid the master shall assert DATSTB* indicating the presence of valid data on the command lines, and that it is ready to accept data.

5) The addressed slave shall enable its data bus drivers, placing the requested data on the data lines. A slave shall not respond to DATSTB* unless ADRSTB* is asserted.

6) After setup time, during which the data lines become valid, the addressed slave shall assert DATACK* indicating that the data is available.

7) In response to DATACK* the master shall accept the data and shall release DATSTB*, indicating to the slave that it must remove the data from the data lines.

8) Upon detecting DATSTB* released, the slave disables its data bus drivers and releases DATACK* indicating that the read transfer is complete.

9) After operating on the data and detecting DATACK* released, the master shall activate command line CM0 logic 0), indicating a write command, and shall place the modified data to be transferred on the data lines.

10) After a setup time, during which the data lines and command line CM0 become valid, the master shall assert DATSTB* indicating the presence of valid data on the data and command lines.

11) The addressed slave shall accept the data and shall assert DATACK* to indicate that the transfer may be terminated.

12) In response to DATACK* the master shall release ADRSTB* and DATSTB*.

13) Upon detecting either DATSTB* or ADRSTB* released, the slave shall release DATACK* indicating that the sequence is complete.

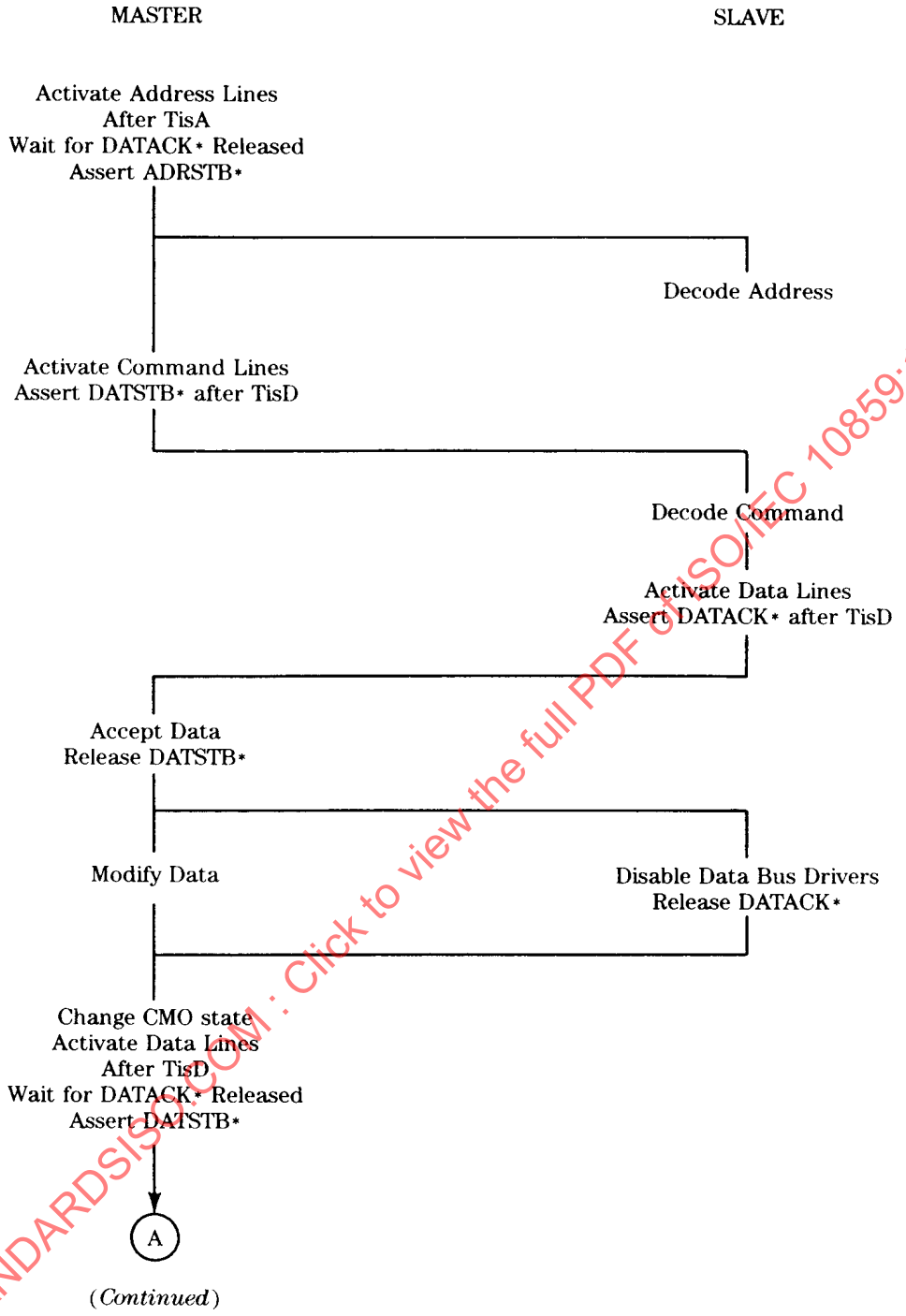


Figure 9 – Read-modify-write sequence flow diagram

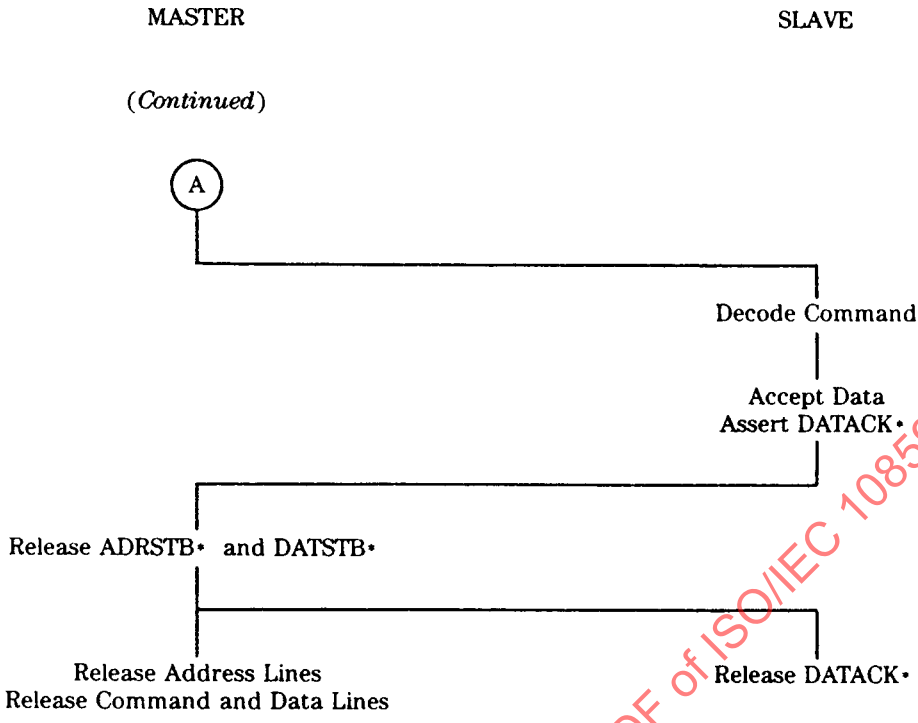


Figure 9 *(continued)* **– Read-modify-write sequence flow diagram**

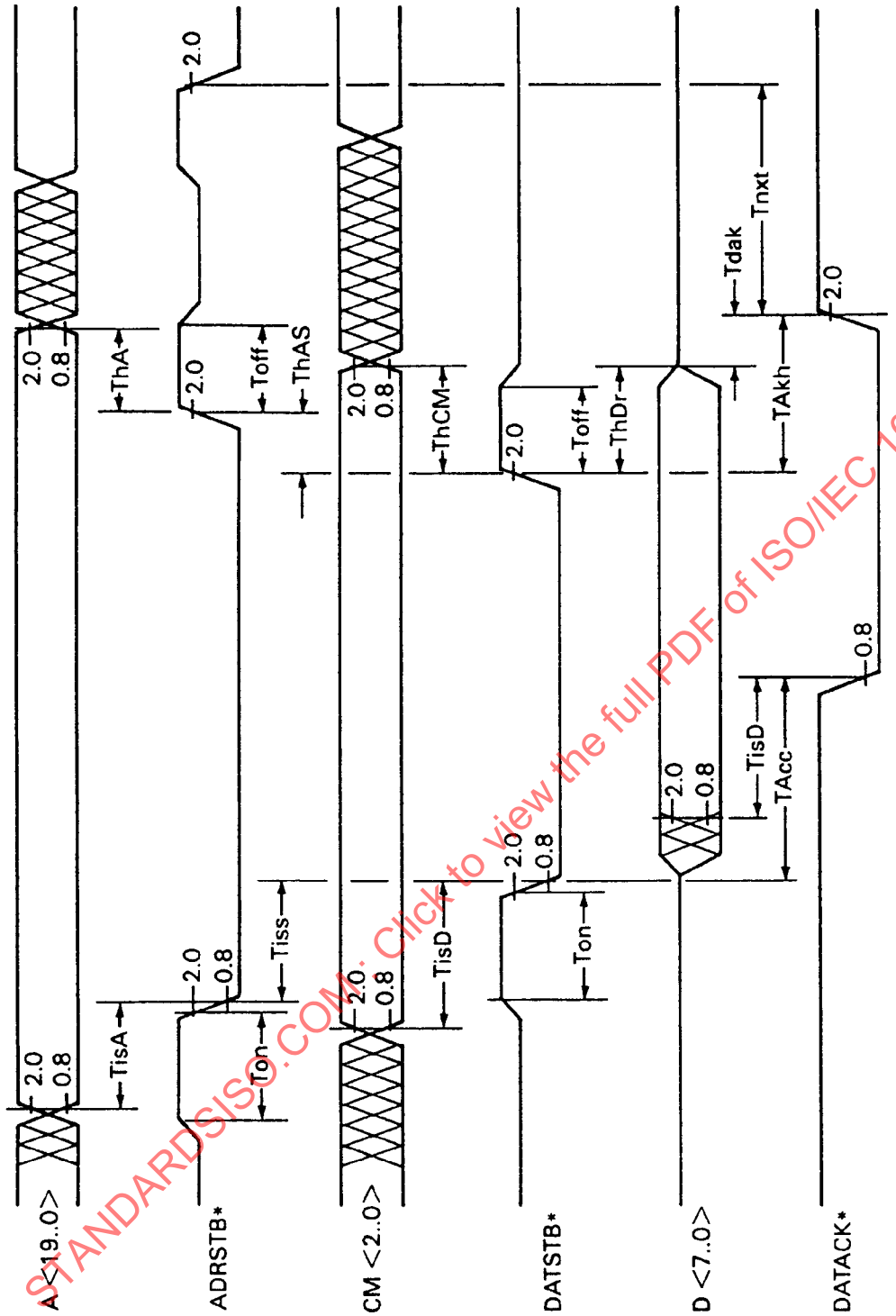


Figure 10 – Read sequence timing diagram

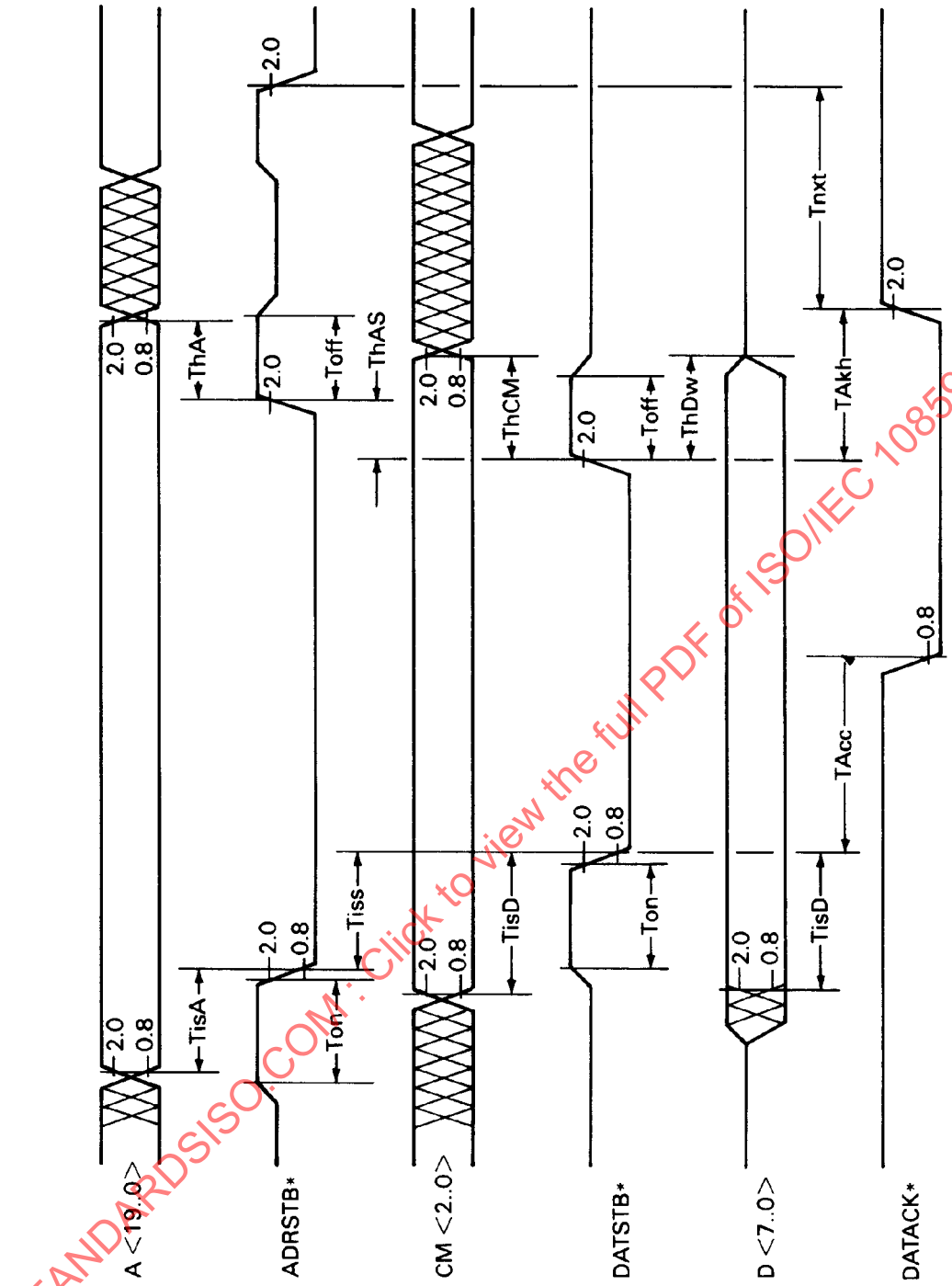


Figure 11 – Write sequence timing diagram

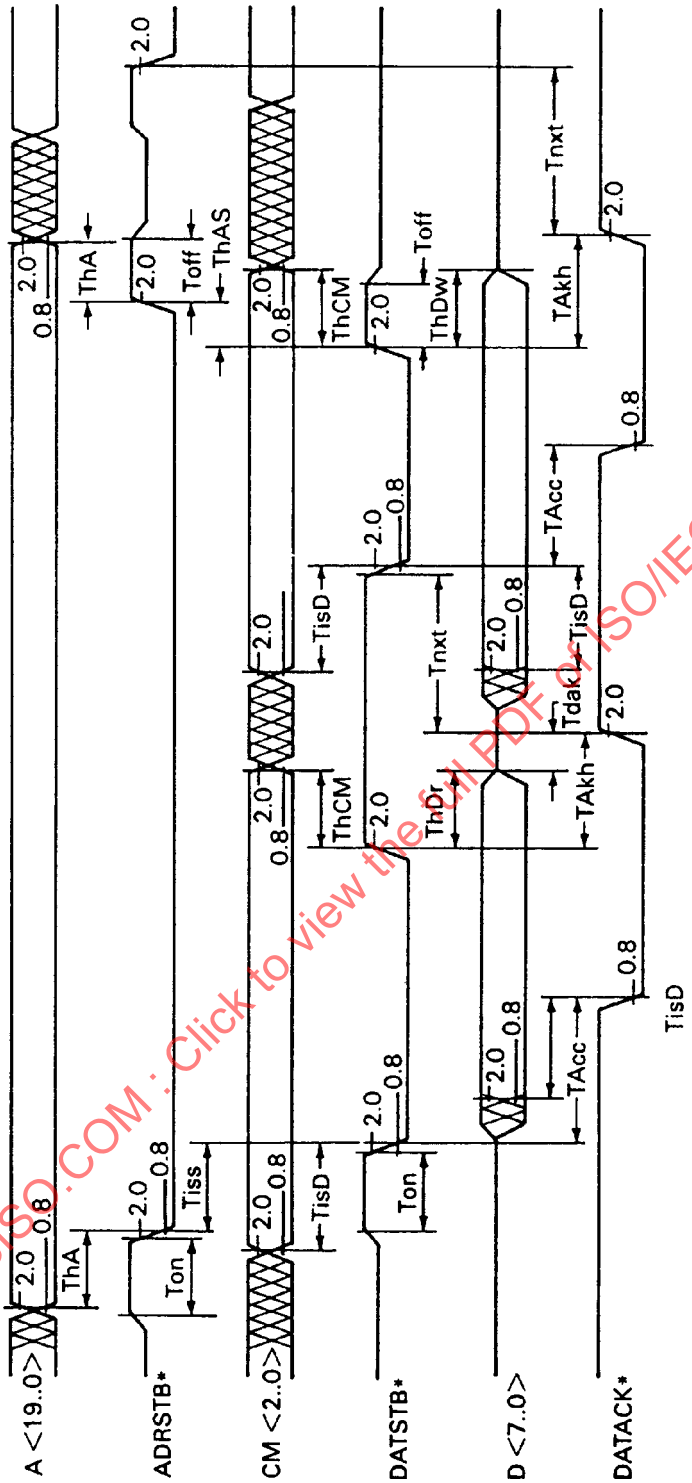


Figure 12 – Read-modify-write sequence timing diagram

5.4 *Vector-fetch*

In responding to an attention request as described in Section 6 of this standard, a master may perform a vector-fetch sequence. The protocol and signal timing parameters of a vector-fetch sequence are identical to those of a read sequence except that only address lines A<2..0> are valid and the command code is:

CM2	CM1	CM0	Transfer
0	1	1	Vector-fetch

5.5 *Burst transfer sequences*

A special form of either read, write, or vector-fetch sequence may be supported by IEEE Std 1000 Bus boards. This is referred to as *burst* transfer mode. During a burst data transfer the operation proceeds according to the previously described protocols except that multiple DATSTB*-DATACK* handshakes occur between the master and the addressed slave. ADRSTB* and all used address lines shall remain stable throughout the sequence. The command lines shall remain stable throughout the sequence.

A slave board may be configured to participate in burst-mode transfer sequences by including logic that auto-increments or auto-decrements the onboard address on active edges of DATSTB*, or by use of a *first-in, first-out* (FIFO) register array.

Figure 13 specifies the signal timing parameters for burst-mode transfer sequences.

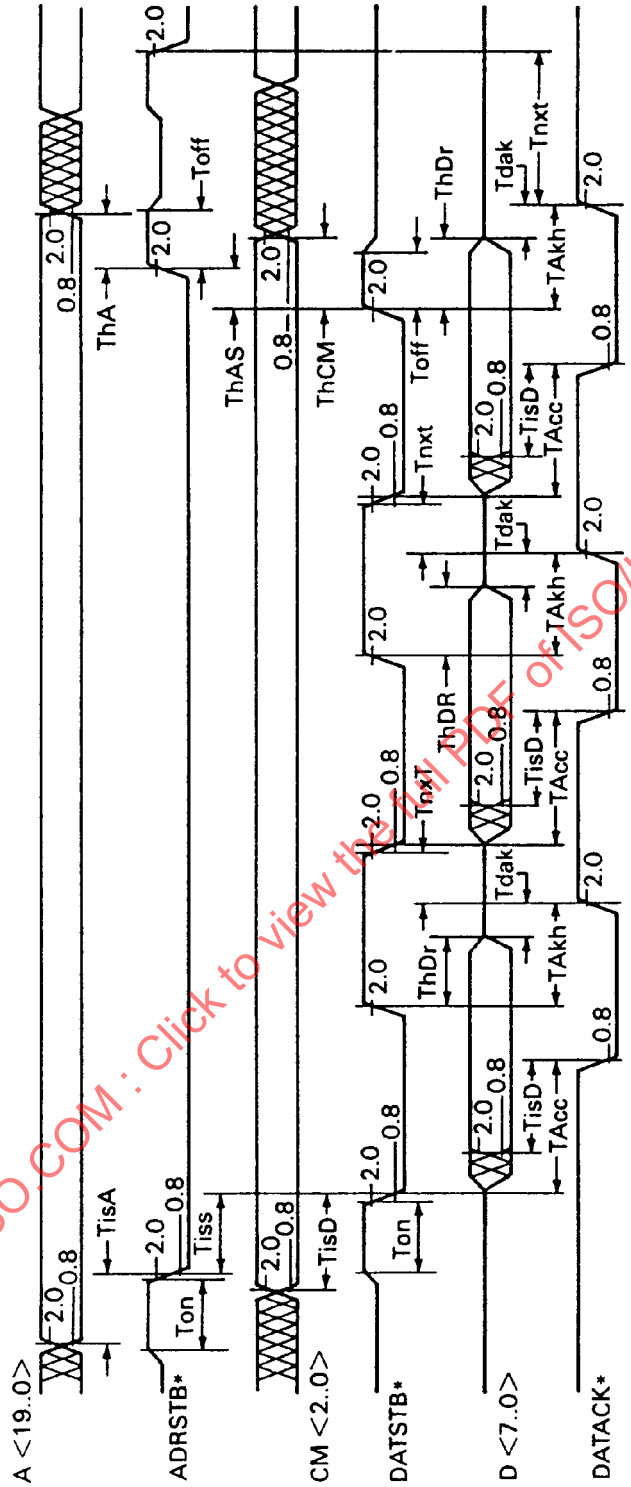


Figure 13 – Burst mode transfer sequence timing diagram
Read cycles illustrated

5.6 *General data transfer rules*

1) A master shall not assert DATSTB* while ADRSTB* is released.

2) A slave shall not respond to DATSTB* while ADRSTB* is released.

3) A slave shall not assert TFRERR* and DATACK* simultaneously.

4) All address lines used in any transfer sequence shall be valid when ADRSTB* is asserted, and shall remain valid until ADRSTB* is released.

5) All command lines shall be valid when DATSTB* is asserted, and shall remain valid until DATSTB* is released.

6) During read transfers all data lines shall be valid when DATACK* is asserted, and shall remain valid until DATSTB* is released.

7) During write transfers all data lines shall be valid when DATSTB* is asserted, and shall remain valid until DATSTB* is released.

5.7 *Transfer error*

A slave that determines the current address to be within its range but locally detects a problem with the transfer, such as an illegal access or a parity fail, may assert TFRERR* instead of DATACK*. TFRERR* may be asserted at any time that ADRSTB* and DATSTB* are both active and shall conform to the same signal timing protocol and parameters as DATACK* would otherwise have done. For example, the master shall terminate the transfer by releasing DATSTB* and ADRSTB*. The slave shall release TFRERR* and the master may initiate whatever system-specific action may be possible to recover from the exception.

5.8 *System time-out*

A *deadman* timer shall be provided to guard against system lockup since there exists a finite probability that a slave will not respond when utilizing an asynchronous protocol (such as when addressing a non-existent memory location or as the result of a metastable condition). This timer shall be present on the system controller, and may be additionally implemented on any other board.

The system controller shall monitor all bus transfer sequences and shall assert TFRERR* at any time that the period from an active transition of DATSTB* to the subsequent active transition of DATACK* exceeds a designated maximum (this period should be user selectable, and its range shall include at least one time-out period that <8 µs). In such an event the master shall terminate the transfer by releasing DATSTB*. The system controller shall release TFRERR* and the master may initiate whatever system-specific action may be possible to recover from this exception.

Table 2 – Data transfer timing parameters

Parameter	Description	Min ns	Max ns
TisA	Address set-up time prior to ADRSTB*	35	–
Ton	Duration of active, released state prior to transition to asserted state	0	–
TisD	Data and CM<2..0> set-up time prior qualifying state. NOTE (2)	35	–
TAcc	Slave access time DATSTB* asserted	–	NOTE (3)
ThDw	Data hold time after DATSTB* released (write)	0	45 ns
ThCM	Command hold time after DATSTB* released	0	–
ThDr	Data hold time after DATSTB* released (read)	0	–
Tdak	Delay between data lines inactive to DATACK* released	–20	–
ThAS	ADRSTB* hold time after DATSTB* released	0	–
ThA	Address hold time after ADRSTB* released	0	–
Toff	Hold time of active, released state	0	–
Tnxt	Delay between DATACK* released and ADRSTB* asserted for next cycle	0	–
TAkh	DATACK* hold time after DATSTB* released	0	120

NOTES

1 For high to low transitions timings are from/to low threshold. For low to high transitions timings are from/to high threshold.

2 Valid data is qualified by DATSTB* in write sequences and by DATACK* in read and vector-fetch sequences.

3 Maximum value specified by manufacturer. See 5.8.

6 Inter-board signalling

6.1 *Overview*

To enable IEEE Std 1000 Bus systems to perform optimally in real-time applications, to respond effectively to error conditions, and to support techniques for rapid movement of blocks of data, a set of eight attention request lines are provided. These lines allow signalling between boards that is essentially unrelated to, and independent of the data transfer protocol, otherwise used to effect inter-board communications.

The attention request lines are provided to allow a board to alert one or more other boards of the occurrence of some event that requires a change in flow or context of the current system activity. The event may be a need for service as in the case of a traditional *interrupt,* a need for DMA transfer, an error condition at the system-level (for example, power failure), an error condition at the board-level (for example, parity failure) or any other system-specific or time-critical event.

Figure 14 shows a typical implementation of the attention request lines.

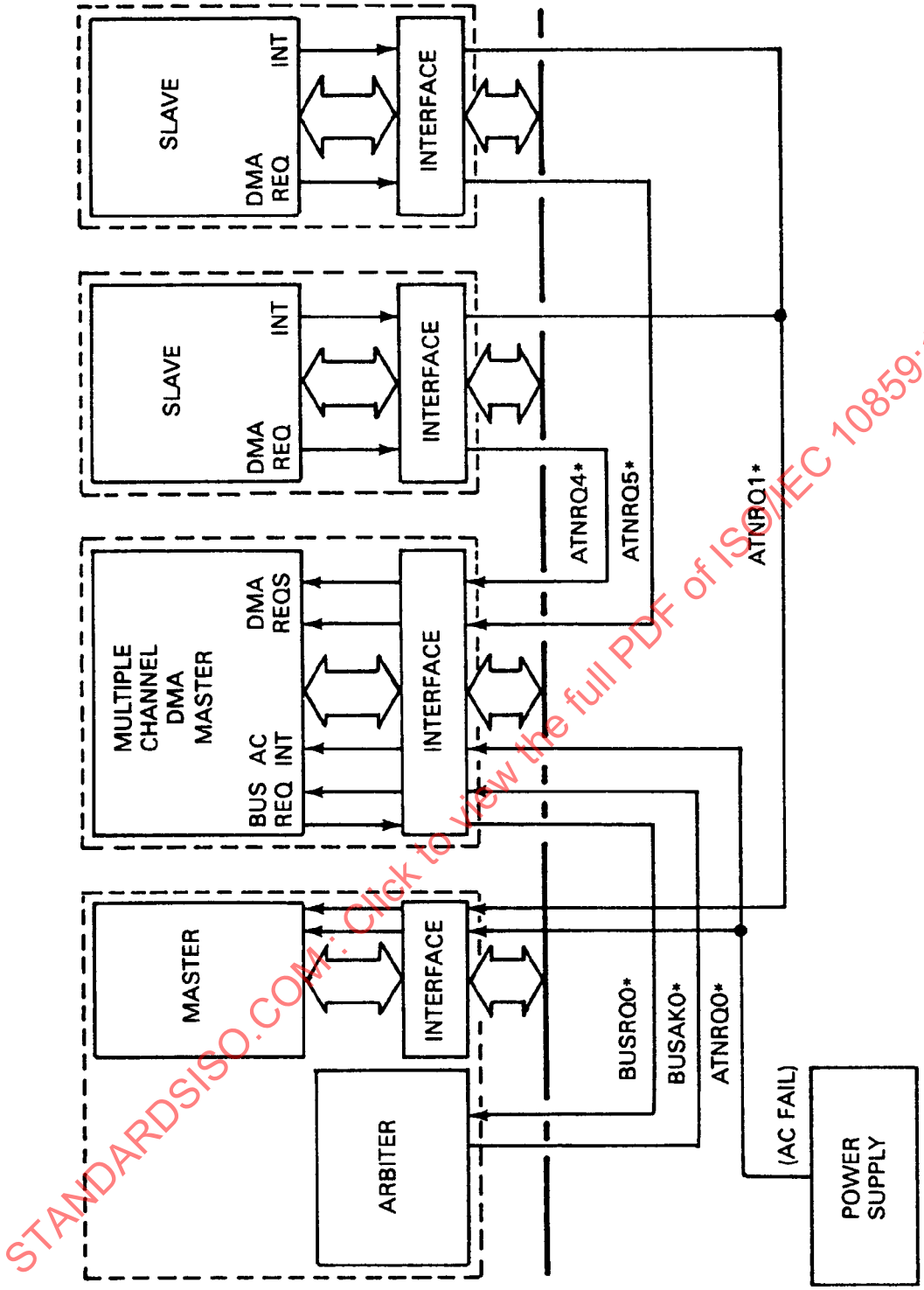


Figure 14 – Example ATNRQ*n implementation**

This section details the usage of the attention request lines, and the corresponding protocols that are utilized within IEEE Std 1000 Bus systems for specialized interboard communication.

The signal lines are

ATNRQ< 7..0 >*

A<2..0>

CM<2..0>

D<7..0>

ADRSTB*

DATSTB*

DATACK *

TFRERR*

6.2 *Attention request lines (ATNRQ<7..0>*)*

An attention request is initiated by a board asserting one of the eight attention request lines. A request may be used to gain the attention of one or more other boards. Any board may be connected to any of the eight request lines, and multiple boards may be connected to the same request line. In this way requests or status flags may be *broadcast* on a global level within a system.

Requests are level-triggered, meaning that a requesting condition is indicated by the relative voltage level present on any request line rather than by the active transition of the signal from one state to another.

It is recommended that boards capable of asserting an ATNRQ*n** line are designed in such a way that it is possible to disable or reassign the signal to any other ATNRQ*n** line, and that boards capable of responding to attention requests are designed in such a way that it is possible to inhibit or reassign an incoming ATNRQ*n** signal to any of its request inputs.

6.2.1 *Attention request priority*

Boards requesting attention within an IEEE Std 1000 Bus system may be assigned a priority for response. The attention request lines are assigned a priority with ATNRQ0* having the highest priority and ATNRQ7* having the lowest priority.

In general the priority schemes utilized within a given system are system-specific and will depend on the chosen function of each attention request line and the way in which specific functions are allocated to each attention request line. However, it is recommended that, in systems utilizing these lines for both DMA requests and interrupt (or other) requests, ATNRQ<3..0>* should be utilized for interrupt requests and ATNRQ<7..4>* for DMA requests.

It is not implied that interrupt requests, DMA request, or any other requests must participate in any larger priority scheme where one group of functional uses of attention request lines has priority over any other. Rather, it is assumed that several priority schemes may exist, which may or may not be related to one another, and which may be user assigned according to specific system requirements.

6.3 *Response to interrupt attention requests*

A master receiving an interrupt by way of an attention request line may respond in one of three ways

1) Implicit response
2) Explicit response
3) Local action response

6.3.1 *Implicit response*

An implicit response to an attention request is where a master uses one or more read or read-modify-write data transfer sequences to discover which device within a system is requesting attention (if necessary), and subsequently uses either a read, write, or read-modify-write data transfer sequence to acknowledge to the board requesting attention that its request has been granted and that the requesting device must release the attention request line.

6.3.2 *Explicit response*

An explicit response to an attention request is where a master uses the vector-fetch data transfer sequence to discover which device within a system is requesting attention, and to simultaneously acknowledge to the board requesting attention that its request has been granted and that the requesting device may release the attention request line. The specific protocol of the vector-fetch sequence shall conform to the following description:

1) The master places the number of the attention request line that it is responding to on address lines A<2..0>, according to the following table:

A2	A1	A0	Acknowledge line
0	0	0	ATNRQ0*
0	0	1	ATNRQ1*
0	1	0	ATNRQ2*
0	1	1	ATNRQ3*
1	0	0	ATNRQ4*
1	0	1	ATNRQ5*
1	1	0	ATNRQ6*
1	1	1	ATNRQ7*

2) After a setup time, during which the address lines become valid, the master shall assert ADRSTB*.

3) The master shall activate the command lines, CM<2..0>, to indicate a vector-fetch transfer.

CM2	CM1	CM0	Transfer
0	1	1	Vector-fetch

4) After a setup time during which the command lines become valid, the master shall assert DATSTB* indicating the presence of valid data on the command lines, and that it is ready to accept data.

5) The requesting device, upon decoding the address lines shall enable its data bus drivers, placing its unique identifying vector on the data lines.

6) After a setup time, during which the data lines become valid, the requesting boards shall assert DATACK* indicating that the vector data is available.

7) In response to DATACK* the master shall accept the vector data and shall release ADRSTB* and DATSTB*, indicating to the requesting device that it must remove the vector data from the data lines, and that it may release the attention request line.

8) Upon detecting either DATSTB* or ADRSTB* released, the requesting board disables its data bus drivers and releases DATACK* indicating that the sequence is complete.

Multiple bytes of vector data may be transferred by use of the burst-mode data transfer protocol.

Boards capable of supplying vector data to an explicit response, by way of a vector-fetch data transfer sequence, shall also be capable of supplying the same information to an implicit response.

The scheme that is used by an IEEE Std 1000 Bus master to locate the interrupt service routine that relates specifically to the transferred vector is specific to the CPU device used and is beyond the scope of this standard.

Masters capable of explicit response to interrupts by way of attention request lines shall also be capable of implicit response.

6.3.3 *Local action response*

A local action response is where a board receiving an interrupt by way of an attention request line does not acknowledge the board requesting attention but performs some kind of operation locally in response to the request. A local action response is typically used when error conditions, such as power failure indication, are broadcast by way of attention request lines.

6.4 *Excluded utilisations of attention request lines*

For any board to be considered IEEE Std 1000 Bus compatible, it shall remain in compliance with all parts of this standard in the absence of any signal applied to any ATNRQ*n** line. Note that while the performance of a given board may be seriously impaired in such absence, the operation of other IEEE Std 1000 Bus boards shall in no way be impaired whether such signals are absent or not. This stipulation is made to specifically exclude the use of ATNRQ*n** lines for implementing signals, which are processor or device-specific, generally synchronous in nature, and which may preclude the use of that board with any other board otherwise designed in accordance with this standard.

7 Electrical specifications

This section specifies the electrical characteristics for IEEE Std 1000 Bus compatible boards and power supplies. Recommendations are also given for compatible backplanes and termination networks.

The IEEE Std 1000 Bus provides an environment for the supply of d.c. power to boards and the transmission of digital logic signals between boards within a single subrack, on a single backplane that provides the following features:

1) Distribution of primary d.c. power using four pins on each connector for each of the +5 V and 0 V d.c. supplies.

2) Distribution of both negative and positive auxiliary supplies utilizing 1 pin per supply on each connector.

3) Distribution of a stand-by power supply that uses 1 pin on each connector.

4) Forty-nine controlled impedance signal lines, which are normally terminated at both ends of the backplane.

5) Four 0 V a.c. return lines each using 1 pin, which are embedded within the signal set as backplane guard tracks.

6) A maximum length for any signal line of 500 mm (20 in), including connection to the termination networks.

7) Provision for a maximum of 21 boards at a preferred horizontal pitch of 20,32 mm (0,8 in).

All boards conforming to the IEEE Std 1000 Bus standard shall adhere to the electrical specifications detailed in this section. These specifications are provided to create a reliable environment for boards to operate within, minimizing the problems of noise and crosstalk, and providing a defined time interval for signals to become valid after they initially become active.

These specifications do not require the use of any particular semiconductor technology, and circuitry implemented in any technology that meets these specifications is acceptable.

7.1 *Power supplies*

This subsection details the requirements, and makes additional recommendations, to aid the system designer (or *integrator)* in the choice of power supplies and the proper distribution of system power.

The +5 V logic supply is the primary power source within a system and will normally have the largest current requirement. No board shall require a maximum current that exceeds 4 A from this supply. Power supply distribution design shall be such that there is no voltage drop in the power distribution system, which results in the voltage available at any particular board being outside the limits of this specification.

The auxiliary (±12 V) voltage power supply units shall not be required to provide greater than 1 A from each supply by any one board within the system.

The standby supply specification provides for the distribution of backup power to boards within a system that requires power during periods when the primary system supply cannot be maintained. A board shall not require greater than 1 A current from this supply. In systems that do not require this supply, provision should be made for connecting this line to the +5 V logic supply.

The power supply sense point, if used, should be at the first point of connection of the power supply to the backplane.

7.1.1 *Supply tolerances*

Table 3 specifies the power supply requirements for IEEE Std 1000 Bus systems. Variation is the tolerance from the nominal specified voltage, as measured at any board position on the backplane through the connector, that is,

Variation = distribution + line regulation + load regulation

where

Distribution is the voltage loss caused by the power distribution system that consists of:

1) the backplane resistance;

2) the power supply to backplane interconnect scheme when the voltage is sensed by the power supply at other than the connection point of the power supply to the backplane;

3) line regulation and load regulation are as defined by the manufacturer of a particular power supply, according to a specified set of test conditions. These conditions should be specified in such a manner as to allow for a reliable calculation of the overall performance, which may be achieved within an actual system environment.

Table 3 – Power supply and distribution

Supply	Nominal V	Variation %	pk-pk ripple (below 10 MHz) mV	Maximum current (per board/per system) A
+Vcc	+05,00	+5, –2,5	50	4/50
+AUX V	+12,00	±5	50	1/4
–AUX V	–12,00	±5	50	1/4
+VSTBY	+05,00	+5*	50	1/4
GND	0,00	ref	ref	–/–
* Where +VSTBY is connected to +Vcc, the variation limits for +Vcc apply.				

The maximum current per board and per system are recommendations only as far as the power supplies are concerned, but are requirements for the capacity of the backplane power distribution. The following requirements are a minimum to enable this to be achieved.

7.1.2 *Power distribution*

The following specifications shall be met for all IEEE Std 1000 Bus compatible systems and backplanes:

1) The backplane shall present a resistance from the point at which the d.c. power is applied to any connector position of ≤5 mΩ (compare 25 mm [~ 1 in] wide, 1 oz copper track ~19 mΩ/m).

2) The backplane shall present a resistance from any signal pin on any connector position to the corresponding signal pin on any other connector position of <1 Ω (compare 0,5 mm [0,020 in] wide, 1 oz copper track ~0,8 Ω/m).

3) Power input cables shall include a conductor for the purpose of connecting the equipment to an infinite capacity reference potential such as ground.

7.1.3 *Power-failure*

In system implementations requiring orderly shutdown in the event of a power failure, and where an early indication of primary power supply failure is available, it is recommended that attention request line ATNRQ0* (see Section 6) be used to signal imminent power failure and that the following protocol be adhered to:

7.1.3.1 *Power-down*

1) The d.c. output of the system 5 V power supply shall remain within its specified tolerance for at least 4 ms after ATNRQO* is asserted.

2) After ATNRQO* has been asserted, the system controller shall wait at least 2 ms and then assert SYSRST*.

3) SYSRST* shall be asserted at least 50 µs before the d.c. output of the system 5 V power supply falls below its minimum specified tolerance.

7.1.3.2 *Power-Up*

1) SYSRST* shall remain asserted for at least 200 ms after the d.c. output of the system 5 V power supply reaches its minimum specified tolerance.

2) SYSRST* shall remain asserted for at least 200 ms after ATNRQ0* is released.

7.2 *Board-electrical requirements*

The following specifications shall be met by all IEEE Std 1000 Bus compatible boards:

1) During power-up, each board shall be responsible for its own reset operation as indicated by the SYSRST* signal.

2) Printed circuit board (pcb) traces for the synchronization signals ADRSTB*, DATSTB*, DATACK*, and TFRERR* shall not exceed 50 mm (~2 in) if the board is constructed with double-sided material, or 25 mm (~1 in) if constructed with multilayer material. This distance shall be measured from the corresponding driver output, or receiver input, to the first point of contact with the backplane connector.

3) On power-down (that is, when SYSRST* is active), each board shall inhibit any signal from driving IEEE Std 1000 Bus lines.

4) Under no circumstances will the average current taken through any IEEE Std 1000 Bus connector pin exceed 1 A.

7.2.1 *Connector-electrical specification*

All IEEE Std 1000 Bus connectors shall conform to IEC 603-2 (1980) specifications.

7.3 *Driver and receiver d.c. characteristics*

Any device may be used to drive the bus, or to receive from the bus, provided it meets the following specifications.

1) Receiver devices connected to the synchronization signals ADRSTB*, DATSTB*, DATACK*, TFRERR*, and SYSCLK shall exhibit schmitt trigger characteristics, with a hysteresis of ~ 200 mV.

2) It is recommended that all other receiver devices exhibit schmitt trigger characteristics, with a hysteresis of > 200 mV.

3) All devices connected to the bus should have a negative input-clamp voltage of ≤–1,4 V.

4) The minimum sink current capability of any driver on any line shall be 24 mA at 0,5 V. Further, it is recommended that drivers with minimum source capability of 24 mA at 2,4 V be used.

5) The minimum rise and fall transition times (10% - 90%) of any line driving device shall be >5 ns when driving a capacitive load of 45 pF.

6) Table 4 specifies the output topology of all signal driving devices used within an IEEE Std 1000 Bus interface system.

7) A receiver shall recognize a voltage of ≤0,8 V as a logic 0, and a voltage of ≥2,0 V as a logic 1.

8) Figure 15 shows the standard voltage levels expected of all signals that are in accordance with this standard.

Table 4 – Bus driver output topologies

Signal	Output device
A<19..0>	Tri-state
D<7..0>	Tri-state
CM<2..0>	Tri-state
ADRSTB*	Tri-state
DATSTB*	Tri-state
DATACK*	Open-collector (Open-drain)
BUSRQ<1..0>*	Open-collector (Open-drain)
TFRERR*	Open-collector (Open-drain)
ATNRQ<7..0>*	Open-collector (Open-drain)
SYSRST*	Open-collector (Open-drain)
SYSCLK	Totem-pole
BUSAK<1..0>*	Totem-pole

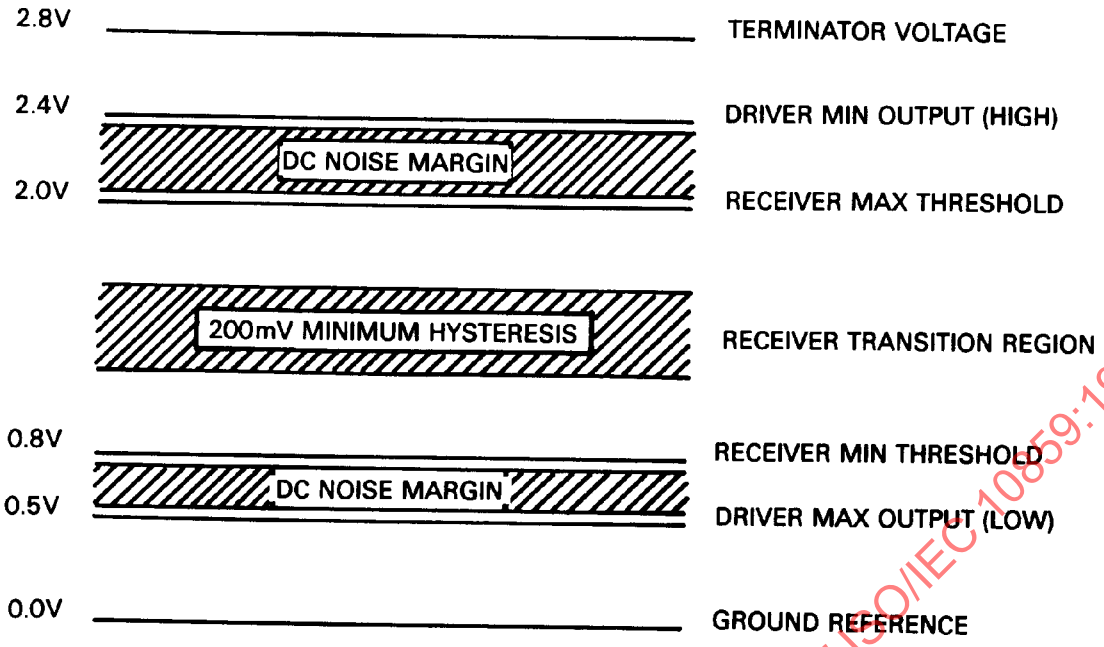


Figure 15 – Signal voltage levels

7.4 *Signal d.c. characteristics*

Any board connected to the IEEE Std 1000 Bus, while inactive, shall not exhibit a load (leakage) on to any bus line of >50 µA at 2,4 V and not >–200 µA at 0,5 V.

7.5 *Signal a.c. characteristics*

No board shall present a capacitance >20 pF to any backplane signal line. Approximately 1,6 pF/in should be allowed for the capacitive effect of polychlorinated biphenyls (PCB) trace spurs (compare 1 oz copper track, 0,98 mm [0,025 in] wide).

7.6 *Backplane a.c. specifications*

This subsection defines those characteristics that should be considered in the design of IEEE Std 1000 Bus compatible backplanes.

7.6.1 *Transmission-line environment*

All signal lines should be considered as transmission lines so as to reliably transmit high-speed digital information. For the purpose of calculation of the parameters of this environment, the following items apply.

1) The maximum length of any signal line on the backplane shall not exceed 500 mm (19,7 in).

2) The minimum separation between connectors shall be 20,32 mm (0,80 in).

3) The maximum length of any polychlorinated diphenyl (PCB) trace on any IEEE Std 1000 Bus signal line shall not exceed 50 mm (2 in) on any board.

7.6.2 *Characteristic impedance*

The IEEE Std 1000 Bus is designed to take into account the driving requirements of high-performance transmission-line backplanes. The transmission-line system, together with the specified maximum signal length, allow an accurate determination of the time required for a signal to be correctly received.

Backplanes should be designed using only microstrips for the signal lines, and should provide an unloaded characteristic impedance of 60 Ω ± 10 % including the effects of plated-through holes and connectors.

Backplane signal tracks should have a constant width throughout the length of the backplane so as to keep the same characteristic impedance throughout its length.

Groundplanes are required so as to form a well-defined transmission-line environment. All groundplanes shall be continuous, allowing breaks in the groundplane only around the holes where connector pins must pass through. Under no circumstances should slotlines be allowed to exist in the groundplane, whether in the horizontal, vertical, or any other direction relative to the signal lines.

7.7 *Termination Networks*

Termination shall be made at both ends of the backplane except in the case where there are five or fewer slot positions available and the total length of the backplane does not exceed 100 mm (3,937 in). In this event, termination may be made at one end only.

The following recommended termination, detailed in Appendix C, should be used:

1) Each bus line should be tied to a 2,8 V ±10 % active termination voltage through a 270 Ω series resistor. Alternatively, a passive termination network consisting of a 470 Ω resistor tied to a +5 V and a 600 Ω resistor tied to 0 V may be used. Any Thevenin equivalent termination may also be used.

2) In addition, the following lines should be diode clamped between 0 V and 0,5 V to minimize negative undershoot during transitions: SYSCLK, ADRSTB*, DATSTB*, DATACK*, and TFRERR*.

3) It is recommended that all termination networks be removable so as to accommodate variations in system implementations, and that they be connected within 20 mm (0,787 in) of the backplane ends.

Appendix A
(informative)

Applicable IEC Specifications

So as to provide maximum compatibility with existing international standards the mechanical specifications for IEEE Std 1000 Bus boards, modules, subracks, and connectors have been drawn extensively from the following IEC publications:

[1] IEC 60249-2: 1970, *Metal-clad base materials for printed circuits – Part 2: Specifications*

[2] IEC 60297-3:1984, *Dimensions of mechanical structures of the 482,6 mm (19 in) series – Part 3: Subracks and associated plug-in units.*

[3] IEC 60297-3: 1984, *Appendix A: Mounting of connectors in IEC 60603-2 (1980).*

[4] IEC 60603-2: 1980, *Connectors for frequencies below 3 MHz for use with printed boards – Part 2: Two-part connectors for printed boards, for basic grid of 2,54 mm (0,1 in) with common mounting features*

Appendix B
(informative)

Recommended bus termination arrangement

The following active termination circuit is recommended for use at both ends of IEEE Std 1000 Bus backplanes in systems utilizing more than 5-slot positions, and may be used at one end only in systems utilizing 5-slot positions or less.

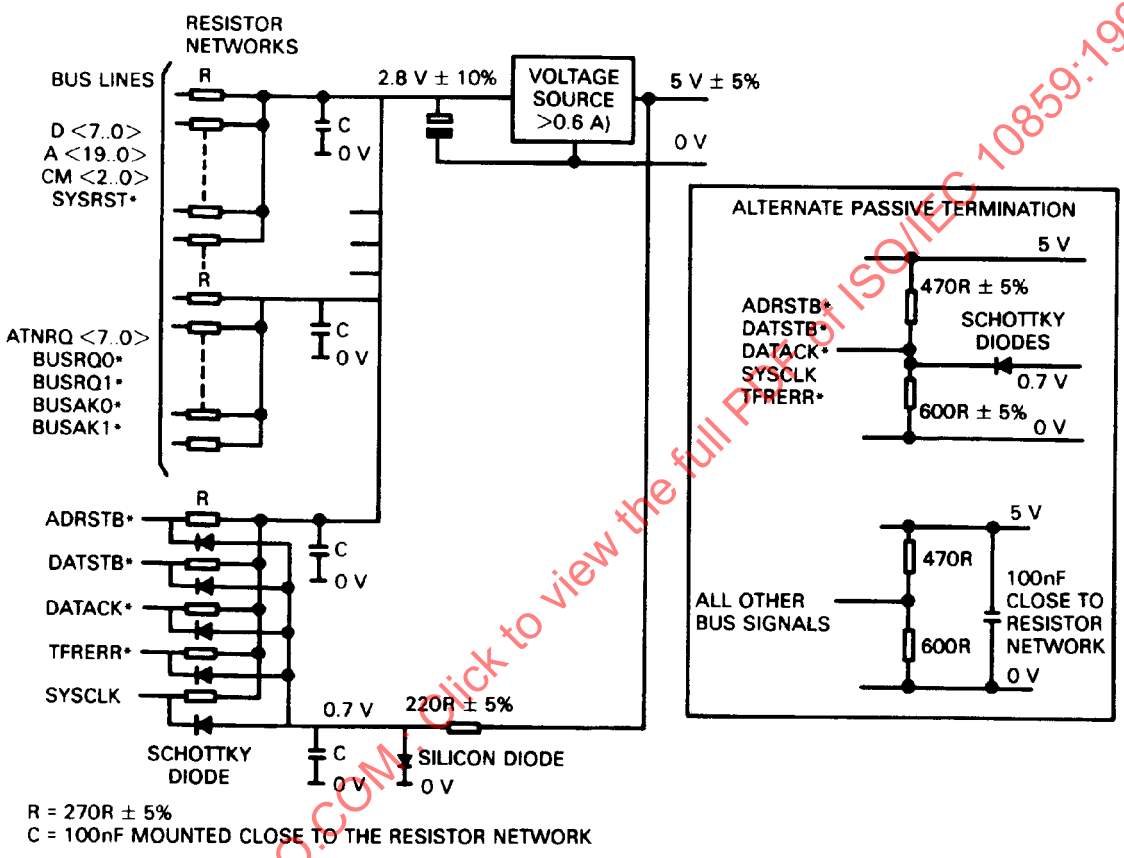


Figure B.1 – Bus termination arrangement

INTRODUCTION TO MECHANICAL CORE SPECIFICATIONS FOR MICROCOMPUTERS

With the introduction of international (IEC) microcomputer architectures based on the "Euroboard form factor," the IEEE Computer Society Technical Committee On Microprocessors and Microcomputers found it appropriate to form a separate IEEE Standard to expand upon the IEC 60297 series of standards, Dimensions of mechanical structures of the 482,6 mm Series (see [9] and [10] in Section 3 of this document).[1)]

This standard provides design engineers with the dimensions and tolerances necessary to ensure mechanical function compatibility. This standard provides environmental specifications as an addendum to IEC 60297-3: 1984, *Dimensions of mechanical structures of the 482,6 mm Series. Part 3: Subracks and associated plug-in units* [10].

This mechanical standard offers total system integration guidelines. It offers advantages such as reduction in design and development time, manufacturing cost savings, and distinct marketing advantages.

This document covers standardized dimensions of a range of modular subracks, and a compatible range of plug-in units, printed boards, backplanes, and connectors.

1) The numbers in brackets correspond to those of the references listed in section 3.

1 Scope

1.1 *Basic dimensions of subracks*

This standard covers the basic dimensions of a range of modular subracks conforming to IEC 60297-3-1984 [10], for mounting in equipment according to IEC 60297-1-1986 [9], and ANSI/EIA RS-310 [1], together with the basic dimensions of a compatible range of plug-in units, printed boards, and backplanes.

1.2 *Dimensions of plug-in units and connectors*

This standard will give the dimensions of associated plug-in units and connectors standardized by IEC 60603-2-1980 [12], together with applicable detail dimensions of the subrack.

1.3 *Environmental requirements of subracks*

This standard will state environmental requirements of subracks and their associated plug-in units.

2 Object

The purpose of this standard is the specification of dimensions that will ensure the mechanical interchangeability and environmental requirements of subracks and of plug-in units.

3 References

The following publications shall be used in conjunction with this standard.

[1] ANSI/EIA RS-310, *Racks, Panels, and Associated Equipment.*[2)]

[2] CFR (Code of Federal Regulations), *Title 47: Telecommunications*, Part 15J, published by Office of the Federal Register (FCC Rules and Regulations are contained within this document).[3)]

[3] IEC 60050, *International Electrotechnical Vocabulary.*

[4] IEC 60068-2-1: 1974, *Environmental testing – Part 2: Tests A: Cold.*

[5] IEC 60068-2-2: 1974, *Environmental testing – Part 2: Tests B: Dry heat.*

[6] IEC 60068-2-6: 1982, *Environmental testing – Part 2: Test Fc and Guidance: Vibration (sinusoidal).*

[7] IEC 60068-2-11: 1981, *Environmental testing – Part 2: Test Ka: Salt mist.*

[8] IEC 60068-2-27: 1972, *Environmental testing – Part 2: Test Ea: Shock.*

[9] IEC 60297-1: 1986, *Dimensions of mechanical structures of the 482,6 mm (19 in) Series – Part 1: Panels and racks.*

[10] IEC 60297-3: 1984, *Dimensions of mechanical structures of the 482,6 mm (19 in) Series – Part 3: Subracks and associated plug-in units.*

[11] IEC 60348: 1978, *Safety requirements for electronic measuring apparatus.*

[12] IEC 60603-2: 1980, *Connectors for frequencies below 3 MHz for use with printed boards – Part 2: Two-part connectors for printed boards, for basic grid of 2,54 mm (0,1 in), with common mounting features.*

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2) ANSI/EIA publications can be obtained from the Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018, or from the Standards Sales Office, Electronics Industries Association, 2001 Street, NW, Washington, DC 20006.

3) This document is available from the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402.

[13] IEC 60651: 1979, *Sound level meters.*

[14] IEC 60707: 1981, *Methods of test for the determination of the flammability of solid electrical insulating materials when exposed to an igniting source.*

[15] IEC 60916: 1988, *Mechanical structures for electronic equipment – Terminology*

[16] ISO TC-10 series on *Technical drawings, dimensioning, and tolerancing*.

4 General arrangement

Subracks may be mounted one above another or in combination with suitable instruments and panels in equipment complying with the rack and panel dimensions given in IEC 60297-1-1986 [9] and ANSI/EIA RS-310-1977 [1]. See figure 1.

NOTES

1 Generally, subracks are equipped with printed board or rack and panel type connectors at the rear side, and have guides for locating or supporting, or both, printed boards or plug-in units.

2 In principle the connector is mounted on the right side of the printed board as viewed from the front of the subrack.

3 Table 5 defines the dimensions required for mechanical interchangeability of plug-in units.

4 The drawings in this specification are not intended to indicate details of design. All dimensions are given in millimeters (with inches in brackets).

5 All drawings in this specification are shown in the first angle projection according to ISO/TC 10 [16].

6 Terminology is as per IEC 60916: 1988, Terminology for mechanical structures for electronic equipment [15], and IEC 60050, International Electrotechnical Vocabulary [3].

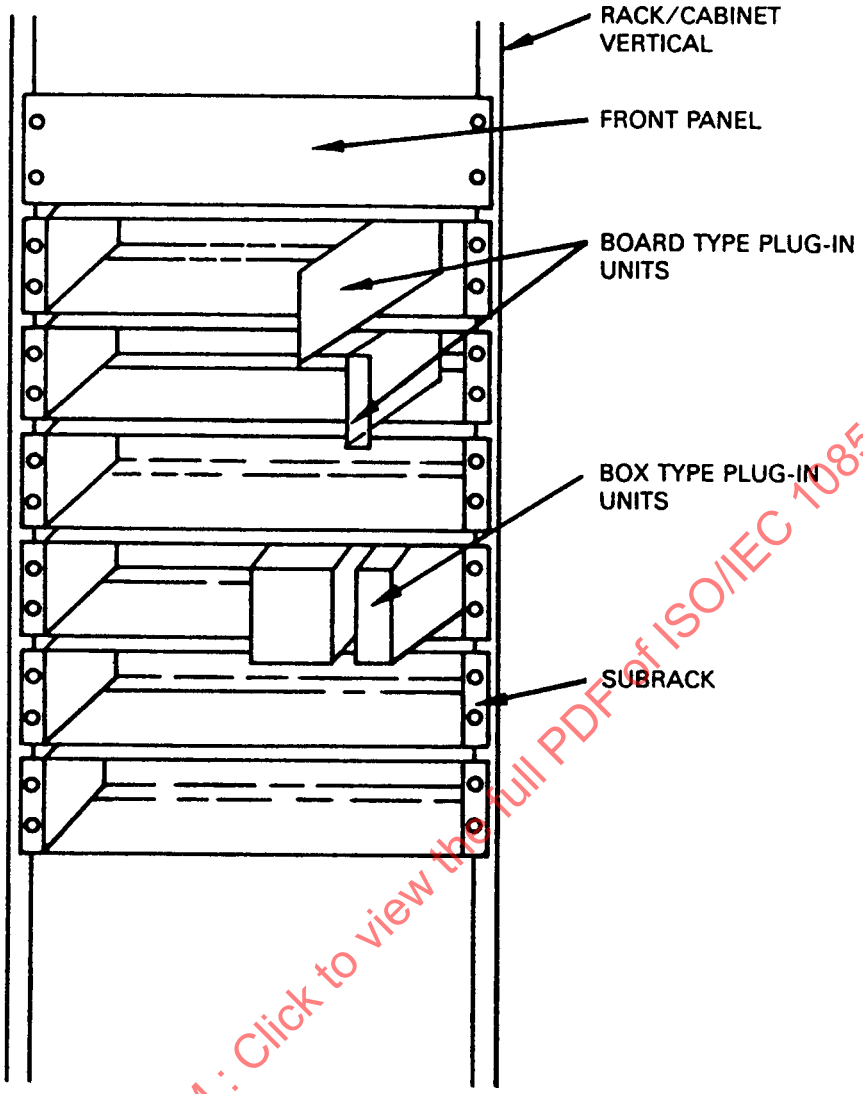


Figure 1 – General arrangement

5 Euroboard matrix

All references to board heights in this document are in units of 3U (133,35 mm, or 5,25 in). A board commonly called single height can be housed in a 3U high subrack or box type plug-in unit and may have a single connector (see IEC 60603-2 [12]) on its rear edge.

NOTES

1 For the 9U/12U high configuration the use of fixtures to mount the connectors will be required to guarantee intermateability.

2 Board heights may be incremented in units of 133,35 mm (5,25 in) after the initial 100 mm (3,937 in).

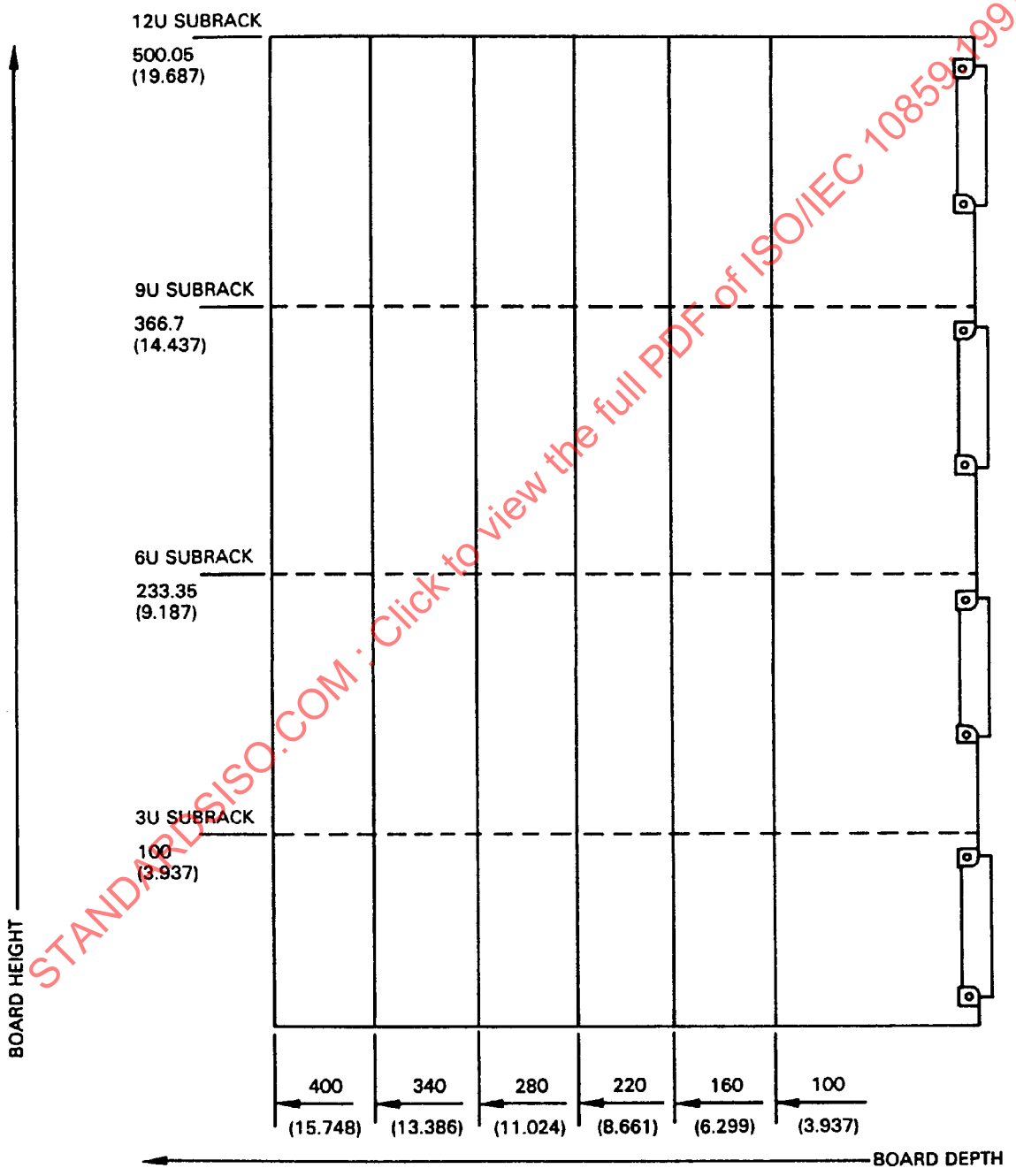


Figure 2 – Euroboard matrix

6 Euroboard sizes

6.1 *Euroboard height*

Table 1 – Euroboard height

U	3U	6U	9U	12U
Hb $^{+0}_{-0,3}$	100,0	233,35	366,7	500,05
$\left(^{+0}_{-0,012}\right)$	(3,937)	(9,188)	(14,437)	(19,687)

6.2 *Euroboard depth*

Table 2 – Euroboard depth

Db $^{+0}_{-0,3}$ $\left(^{+0}_{-0,012}\right)$	100 (3,937)	160 (6,299)	220 (8,661)	280 (11,024)	340 (13,386)	400 (15,748)
Db ±0,1 (±0,004)	93,67 (3,688)	153,67 (6,05)	213,67 (8,412)	273,67 (10,774)	333,67 (13,137)	393,67 (15,499)

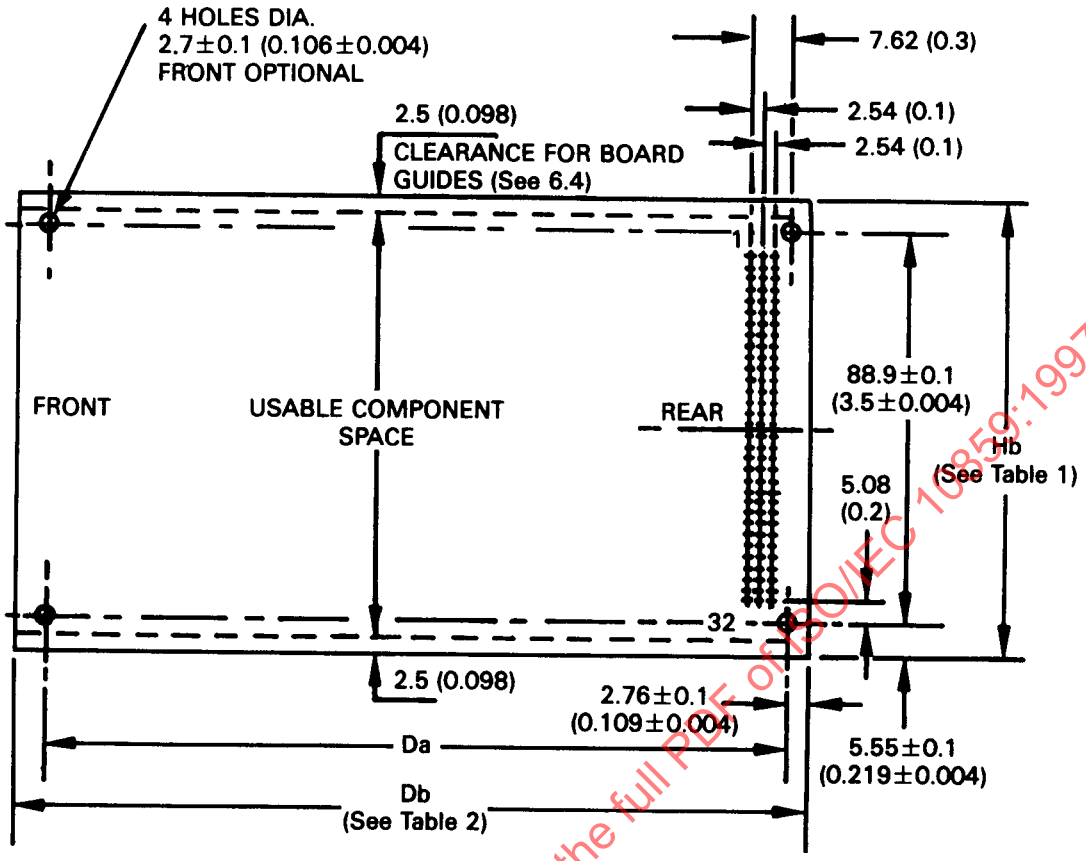
6.3 *Euroboard thickness*

The thickness of printed boards of plug-in units shall be 1,6 ± 0,2 mm (0,063 ± 0,008 in) in the area of the guides.

6.4 *Tracks and guides*

Copper tracks are not to extend beyond the usable component space on the outer planes. If metallic guides are used, board clearance may have to be increased. Printed circuits and components must be placed on the board in accordance with their electrical features.

NOTE – The clearance area for board guides may be used to provide a metallic contact between the subrack and the board in order to reduce EMI/RFI emissions, or to provide heat-sinking capability to the board, or both.

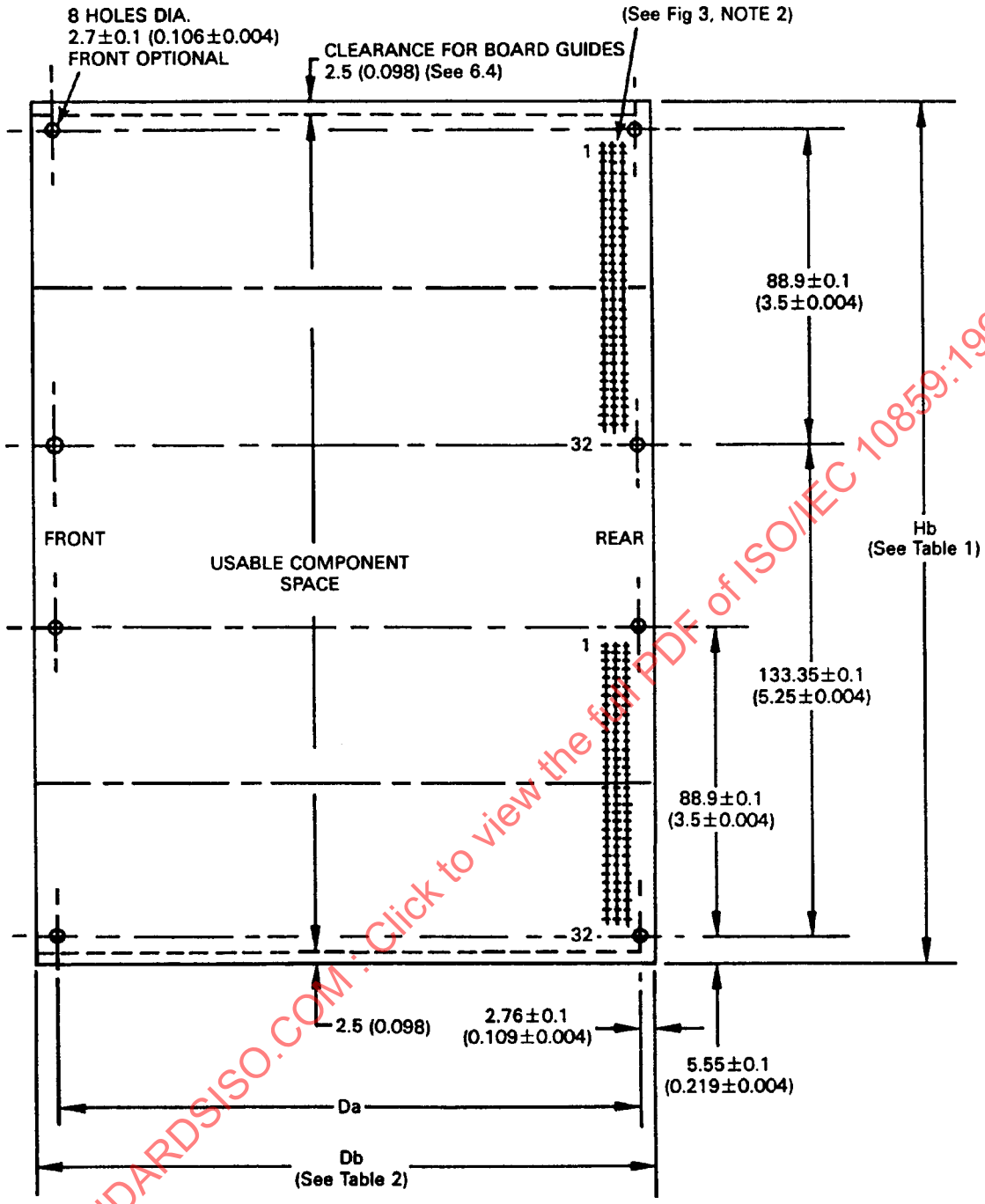


NOTES

1 For board thickness, see 6.3.

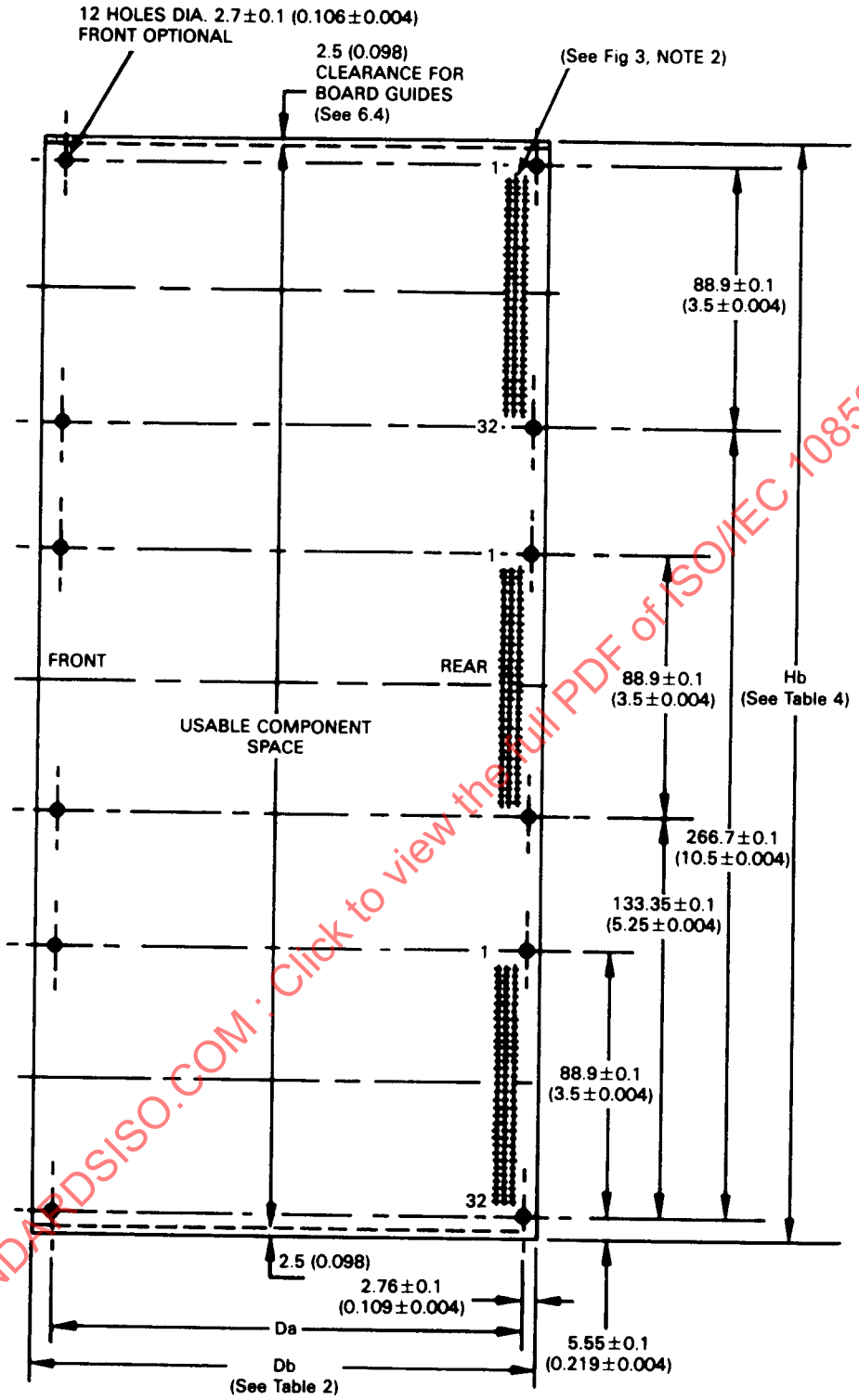
2 This connector pattern refers to IEC 60603-2:1980 [12] Type C connectors, but does not indicate tolerance. Recommended tolerance is ±0,05 mm (0,002 in).

Figure 3 – Single height board, component side view



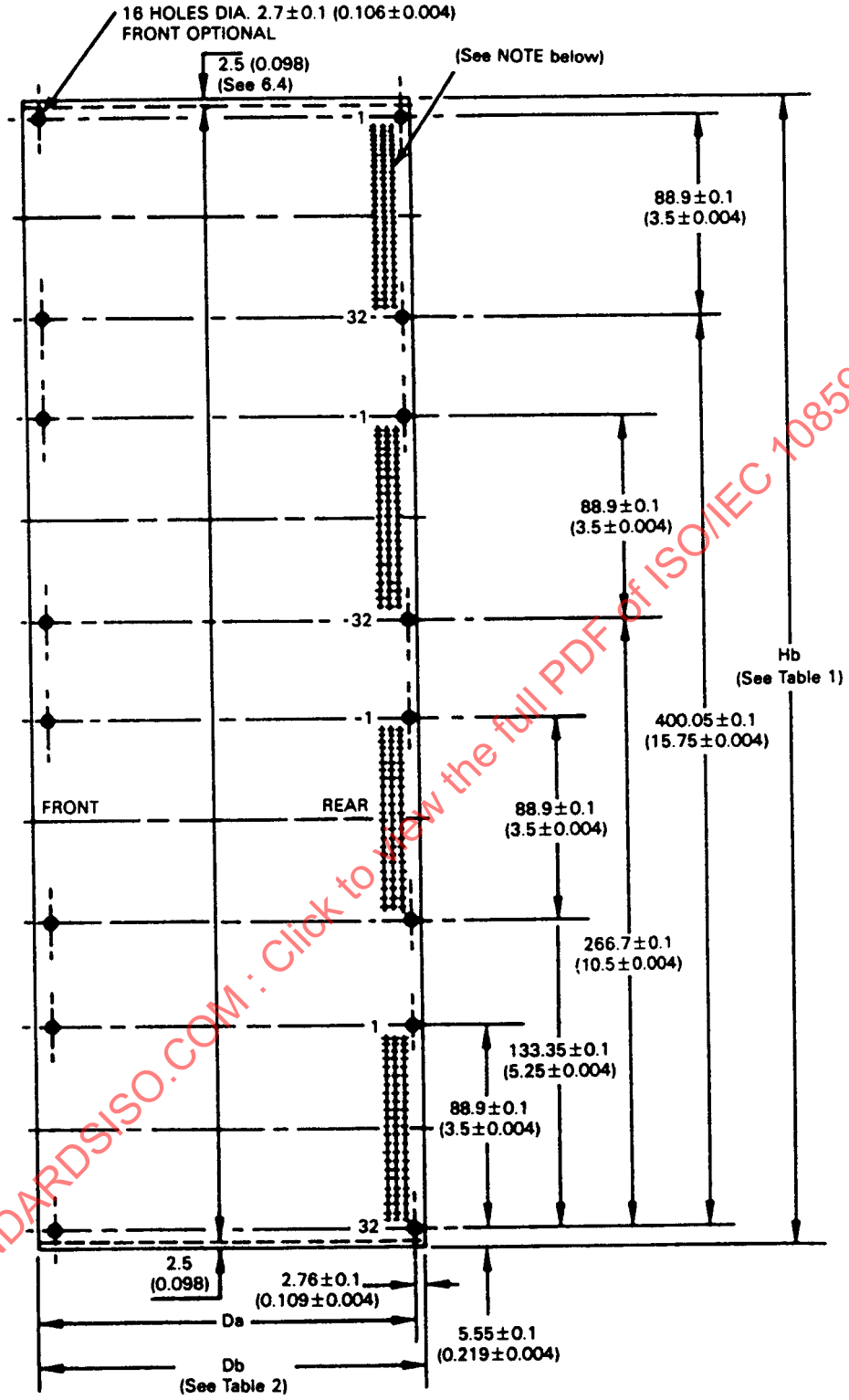
NOTES – For board thickness, see 6.3.

Figure 4 – Double height board, component side view



NOTE – Use fixtures to mount connectors. For board thickness, see 6.3.

Figure 5 – Triple height board, component side view



NOTE – Use fixtures to mount connectors. For board thickness, see 6.3.

Figure 6 – Quadruple height board, component side view

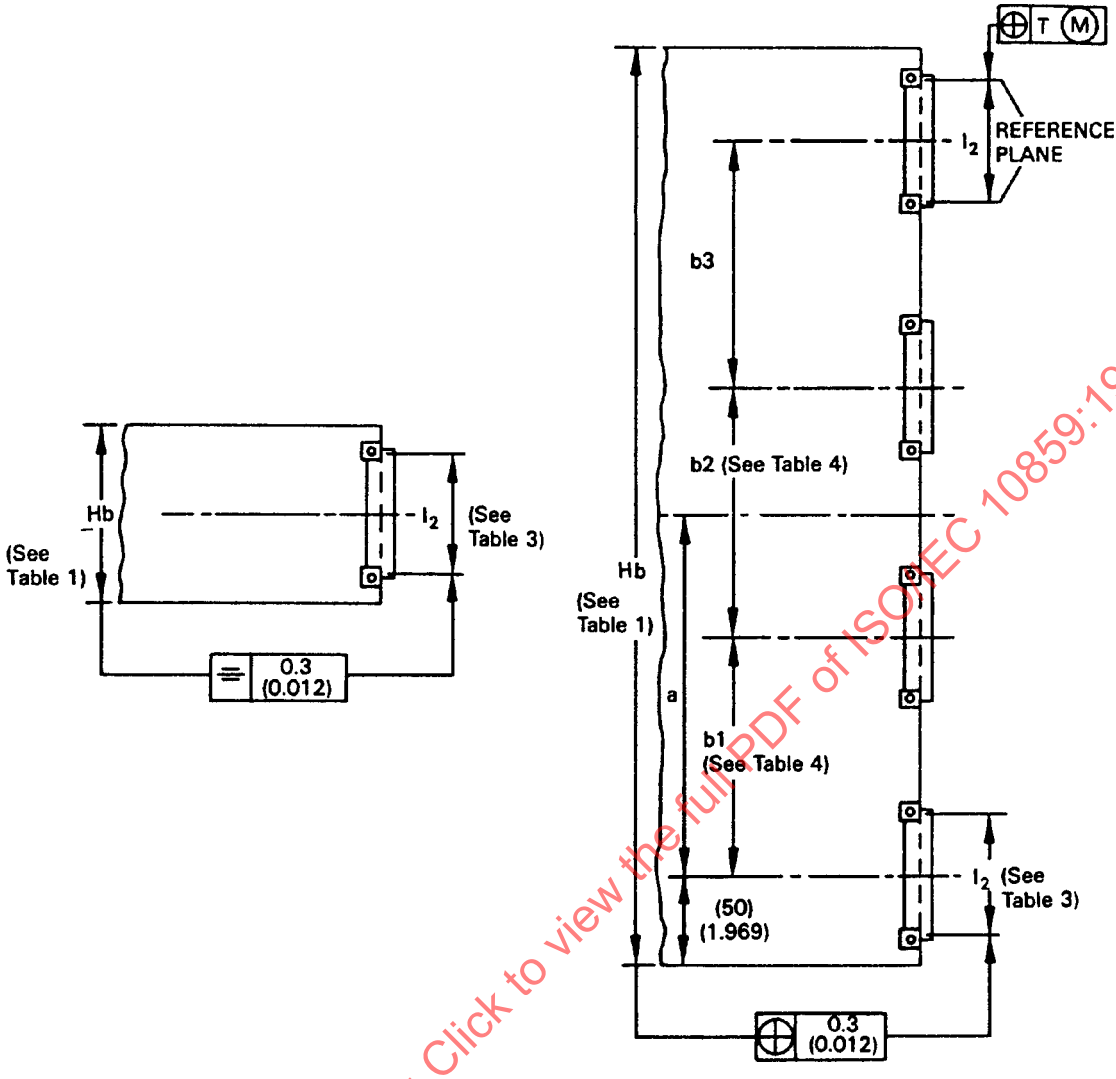
7 Position of plug-in unit mounted connectors (board type and box type)

Table 3 – Position of plug-in unit mounted connectors, board/box type

Connector type (see IEC 60603-2: 1980 [12])	T*	l_1	l_2
B + C (see figure 7)	0,05 (0,002)		$85{,}2\ ^{+0{,}2}_{-0}$ $\left(3{,}354\ ^{+0{,}008}_{-0}\right)$
Q + R (see figure 8)	0,05 (0,002)	$85{,}2\ ^{+0{,}2}_{-0}$ $\left(3{,}354\ ^{+0{,}008}_{-0}\right)$	
* The positional tolerance T is to be derived from the play between the plug-in unit mounted connector and the subrack mounted connector.			

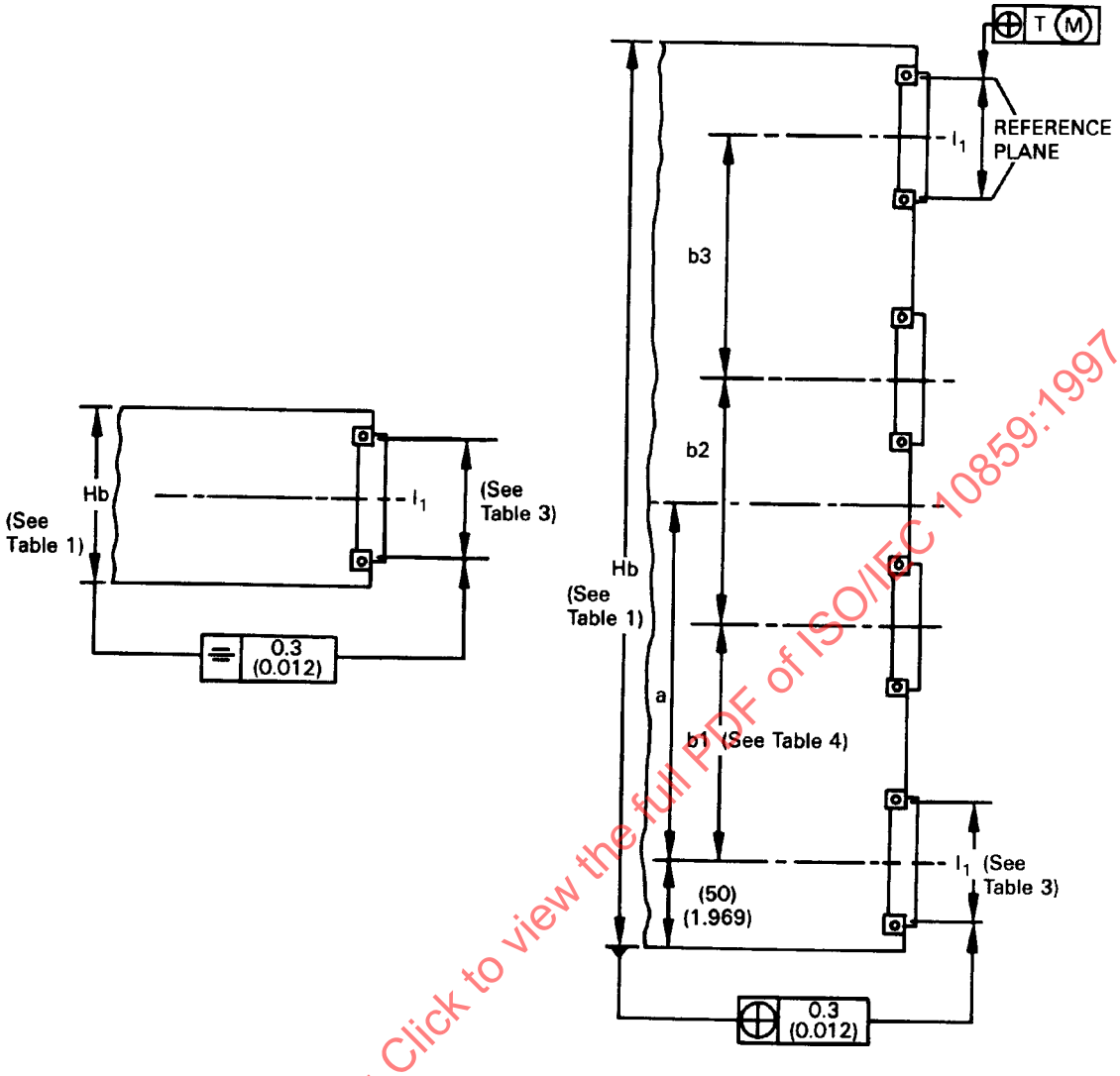
Table 4 – Position of plug-in unit mounted connectors

n x U*	3U	6U	9U	12U
a ± 0,1 (0,004)	0	66,67 (2,625)	133,35 (5,25)	200,02 (7,875)
b_1 ± 0,1 (0,004)		133,35 (5,25)		
b_2 ± 0,1 (0,004)			133,35 (5,25)	
b_3 ± 0,1 (0,004)				133,35 (5,25)
*Subracks are dimensioned in heights of U.1U = 44,45 mm (1,75 in). See IEC 60297-1-1986 [9], and ANSI/EIA RS-310-1977 [1].				



NOTE – Fixtures are required when mounting connectors on double, triple, and quadruple height boards.

Figure 7 – Position of connectors on plug-in units



NOTE – Fixtures are required when mounting connectors on double, triple, and quadruple height boards.

Figure 8 – Position of inverse connectors on plug-in units

8 Plug-in unit description

A plug-in unit can be of various types, as is shown in figure 1. It usually consists of a printed board assembly with connector(s), and optionally, handles(s), ejector(s), front panel, rear panel, mounting rails, and covers.

A plug-in unit can itself house a plurality of different types of plug-in units. Box type plug-in units may house board type plug-in units or other subassemblies.

9 Plug-in unit dimensions

9.1 *Board type plug-in units*

1) DT 2 in table 5 is the inspection dimension to ensure reliable connector mating.

2) For connector detail see IEC 60603-2 [12].

3) For a nominal 5,08 mm (0,2 in) width filler panel (see figure 16), the 7,62 mm (0,3 in) dimension is reduced to 2,5 mm (0,1 in).

4) Maximum dimensions for location features for front panel alignment, or screw retention, or both (figures 15 and 16). The standard M 2.5 screw mounting does not exclude other means of retention or quick release fasteners (to be agreed upon by vendor and user). Slotted or plus-type screw heads are permitted.

5) Double-sided surface mounted devices (SMD) mounting on plug-in boards may result in changes of the relationship of front panel, guide rail, and backplane positioning relative to the subrack (see figure 17).

6) The injector/ejector design detail can be derived from figures 9 and 10, and can be manufactured of various materials (see 12.6.2). This detail is restricted to individual boards plugged into the subrack, and is not suitable for front panel mounted boards or within a box type plug-in unit (see figure 21).

7) The dimension between front attachment plane and the beginning of the board guide is ≥6 mm (0,236 in) as specified in IEC 60297-3-1984 [10] (see figures 31-37), in order to allow for injector/ejector operation.

8) Board type plug-in units with front panels may require handles. The details of handles and their positioning on the front panels are to be agreed upon by supplier and user, or are specified in the individual application standard.

9) The recommended plug-in unit front panel thickness is 2,5 mm (0,098 in).

9.2 *Box type plug-in units*

1) DT 2 is the inspection dimension to ensure reliable connector mating. For inspection dimensions see table 5.

2) For connector details see IEC 60603-2-1980 [12].

3) Box type plug-in units are designed to interface with the subrack as specified in Section 11 via a single board, as specified in figures 3-6, with connectors attached. Additionally, the box type plug-in units are to house large components.

4) Box/board type plug-in units are designed to interface with the subrack as specified in Section 11 via one or more board type plug-in unit, as specified in figures 3-6 and 11-14, with connector(s) (see IEC 60603-2) attached. Individual front panels can be replaced by single plug-in unit front panels, or in other combinations of N X 5,08 mm (0,2 in).

5) Box and box/board type plug-in units may require handles. Dimensions of these are to be agreed upon by supplier and user, or are specified in the individual application standard (see 9.1 (8)).

10 Backplane design and mounting positions

10.1 *Rigidity*

Backplane and subrack mounting positions must be sufficiently rigid to withstand the insertion and withdrawal forces of the connectors, as in IEC 60603-2-1980 [12].

10.2 *Dimension*

The dimension 7,62 mm (0,3 in) is the minimum dimension to the first mounting hole. This dimension can be increased by increments of N X 5,08 mm (0,2 in).

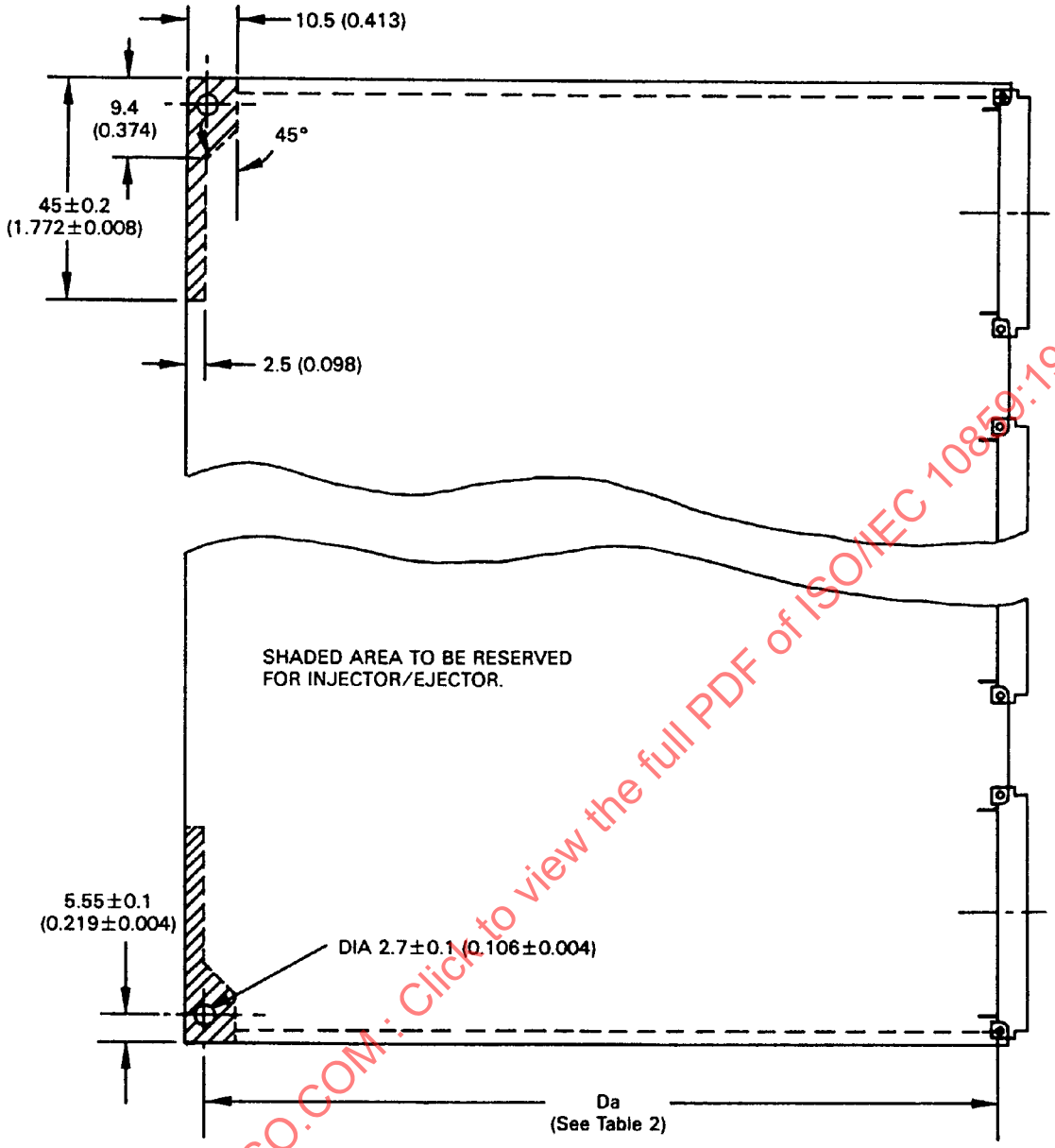
NOTE – For backplane, connector, board, and front panel relationships, see figure 17.

Table 5 – Inspection dimensions (figures 11-14)

Board depth	100	160	220	280	340	400
DT 2 ± 0,4 (±0,016)	109,93 (4,328)	169,93 (6,690)	229,93 (9,052)	289,93 (11,415)	349,93 (13,777)	409,93 (16,139)

Table 6 – Front Panel dimensions (figures 15, 16, 19, 21, 23-26; Backplane Dimensions (Figures 27-30)

Subrack heights	3U	6U	9U	12U
G $^{+0}_{-0,3}$ $\left(^{+0}_{-0,012}\right)$	128,7 (5,067)	262,05 (10,317)	395,40 (15,567)	528,75 (20,817)
F1	122,5 (4,823)			
F2 ± 0,2 (±0,008)		255,85 (10,073)		
F3			389,20 (15,323)	
F4				522,55 (20,573)

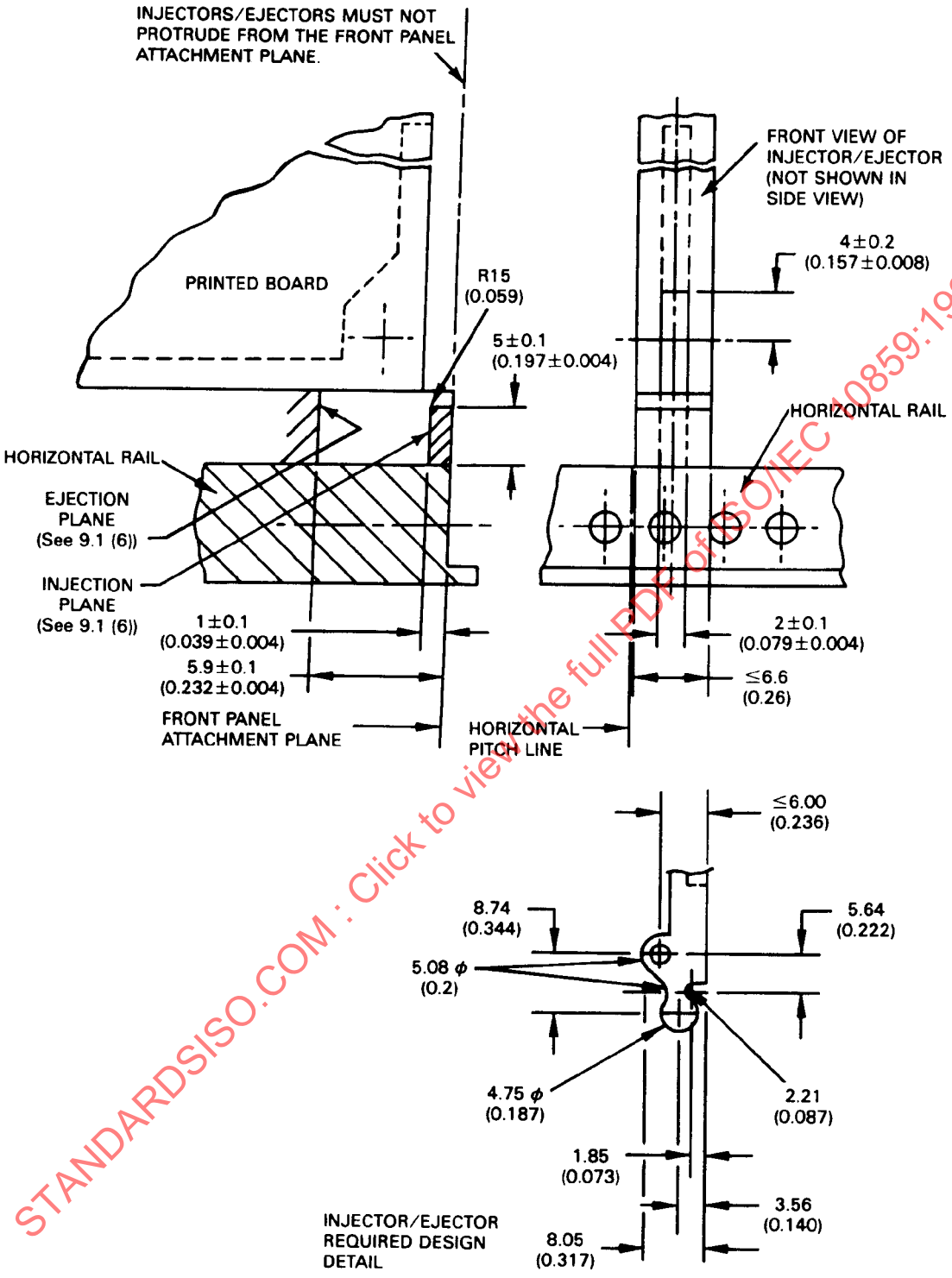


NOTES

1 Single height boards may use either one or two injectors/ejectors. Double, triple and quadruple height boards require two injectors/ejectors.

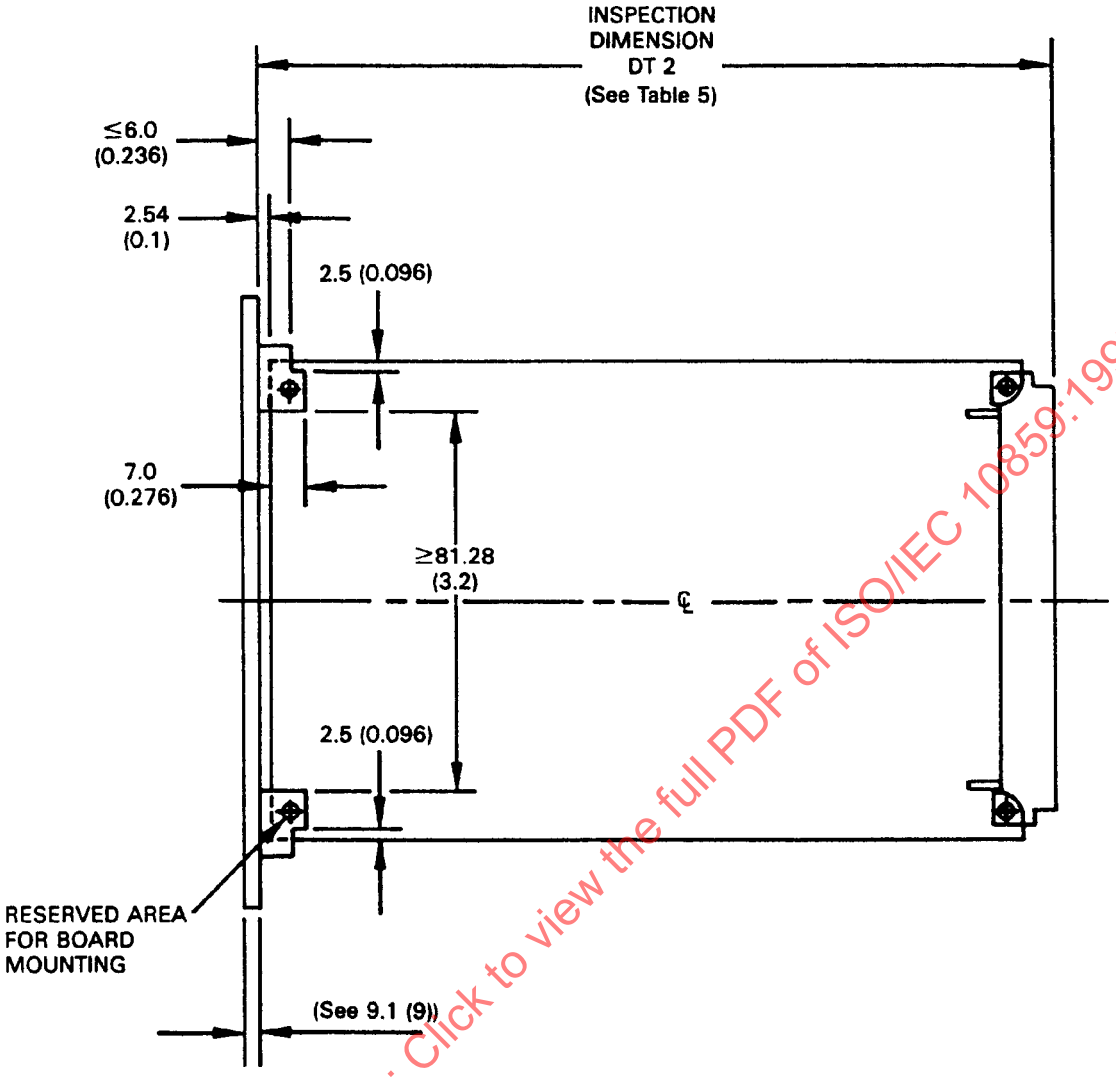
2 If metallic injectors/ejectors are used, printed circuits and components must be placed in accordance with their electrical failures (see 9.1 (6)).

Figure 9 – Injector/ejector mounting positions



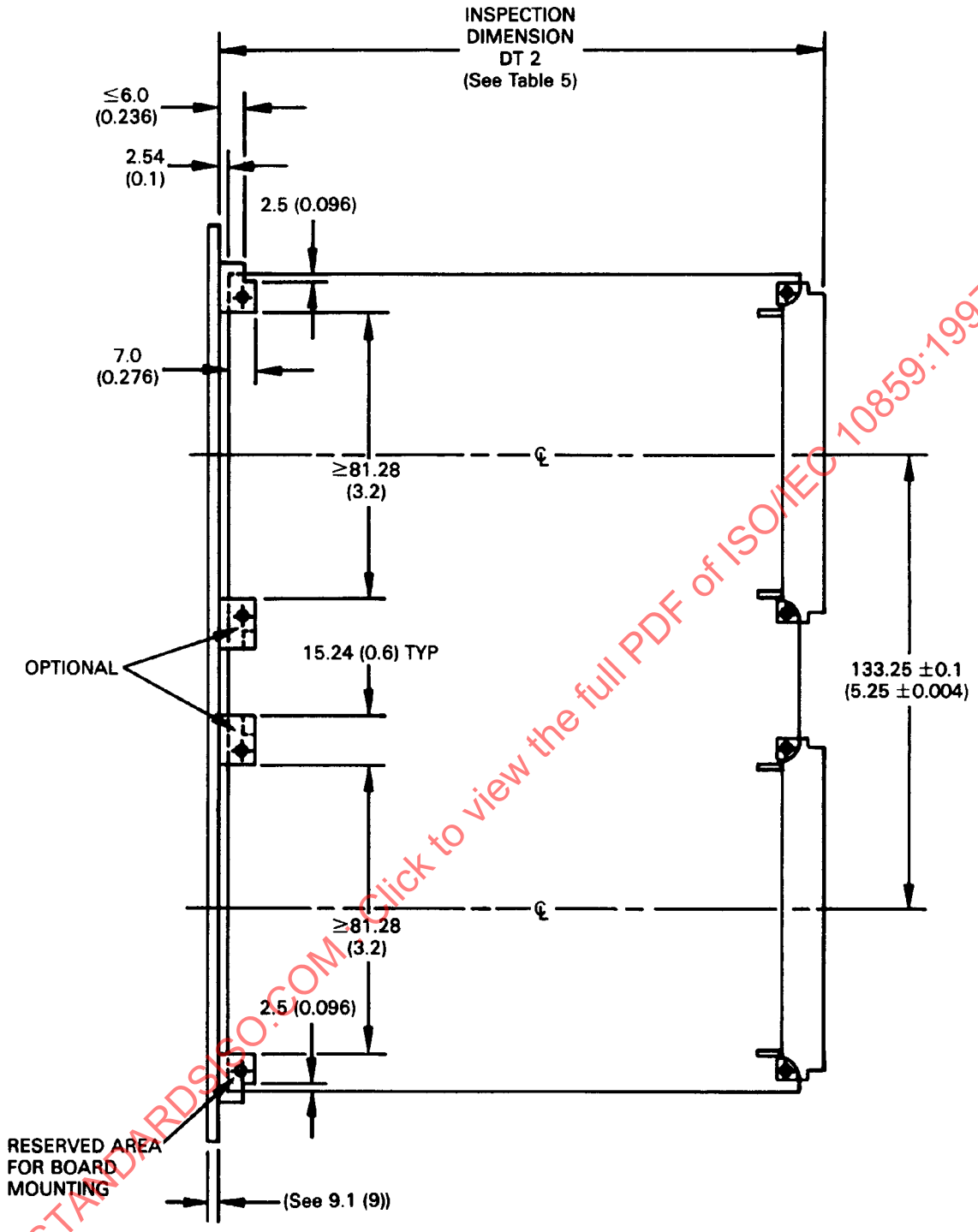
NOTE – Ejection and injection plane can be of individual or full width design (see 9.1 (6) and 9.1 (7)).

Figure 10 – Injector/ejector design detail



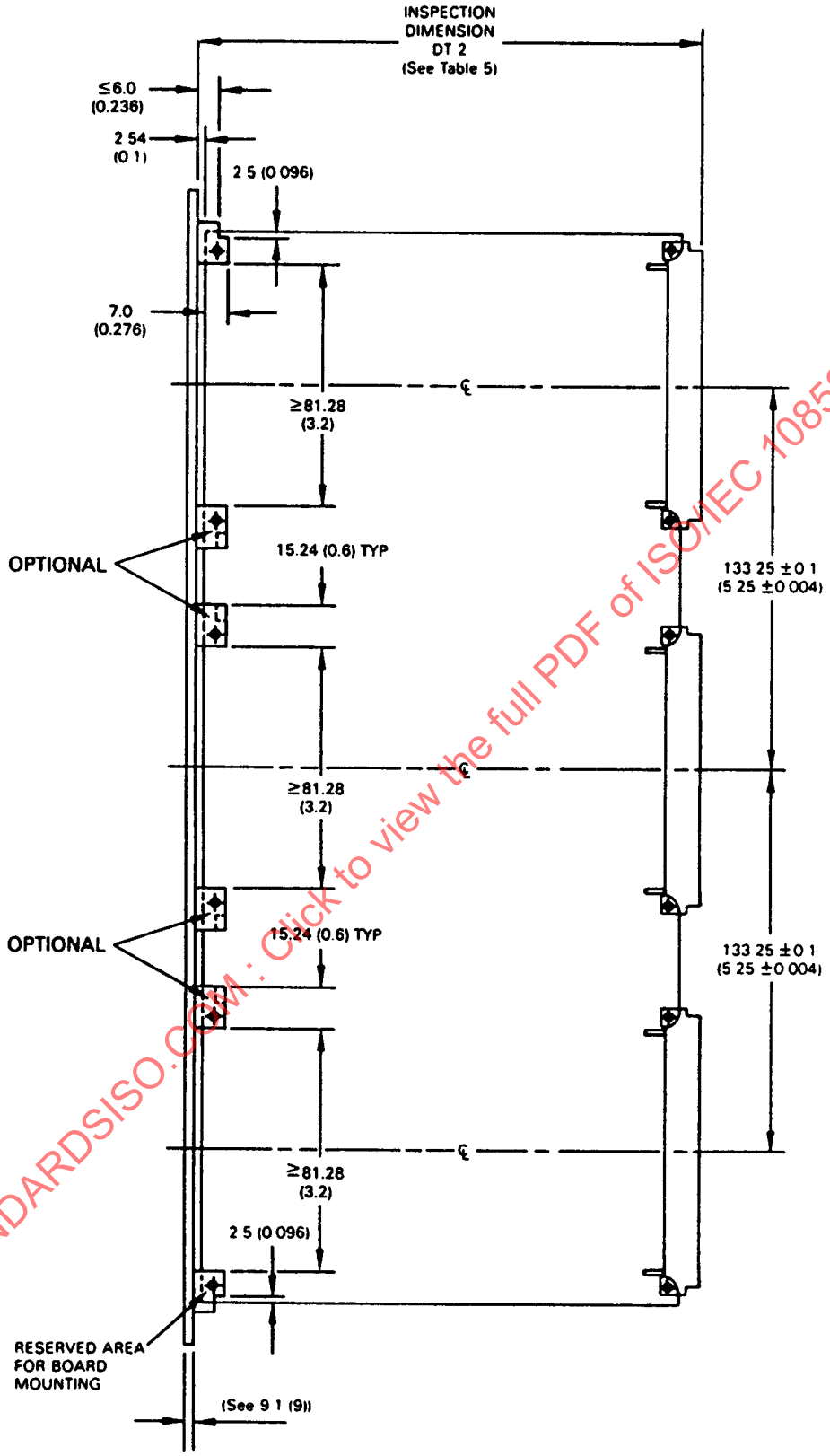
NOTE – For front panel handles, see 9.1 (8).

Figure 11 – Single height board type plug-in unit



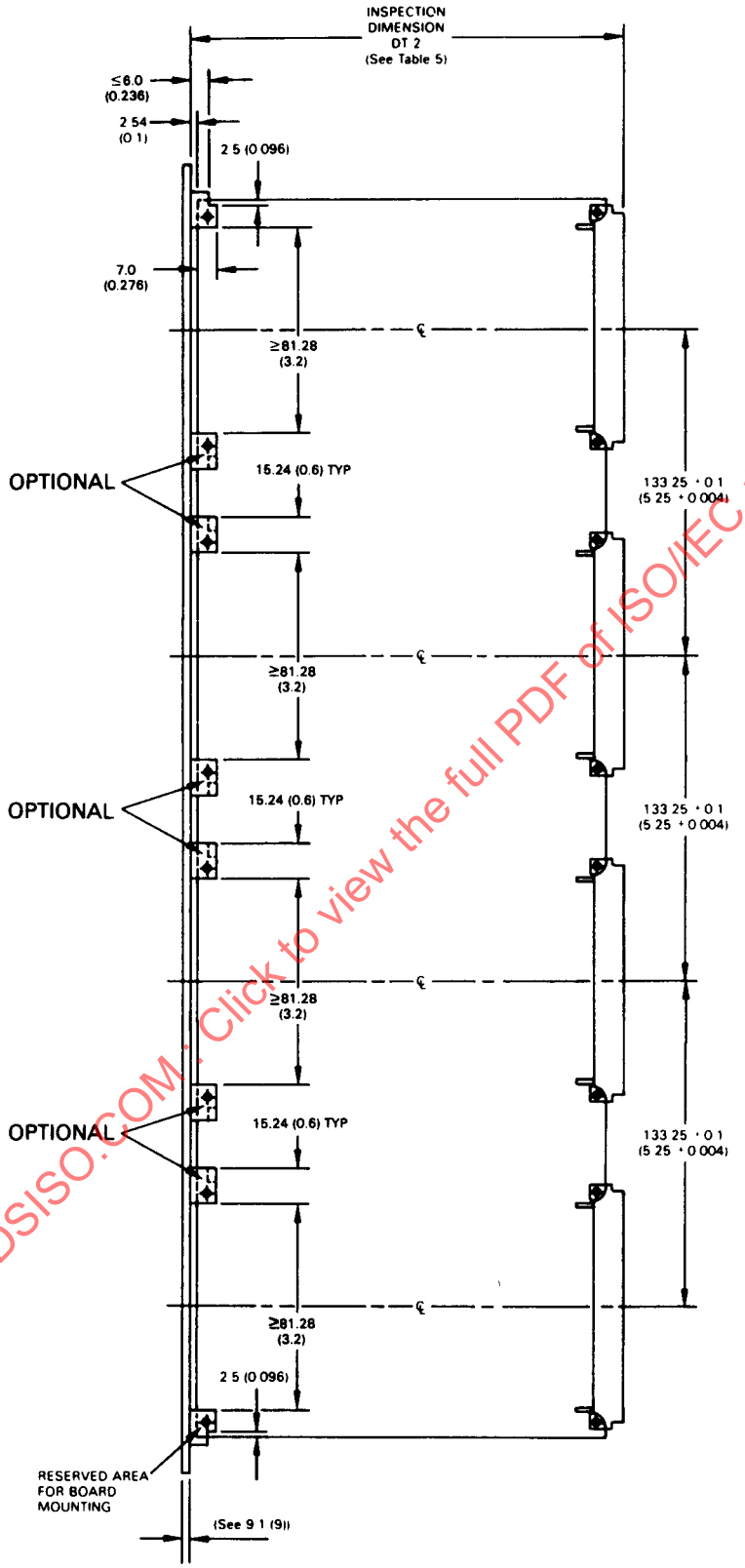
NOTE – For front panel handles, see 9.1 (8).

Figure 12 – Double height board type plug-in unit



NOTE – Board stiffeners are recommended. For front panel handles see 9.1 (8).

Figure 13 – Triple height board type plug-in unit



NOTE – Board stiffeners are recommended. For front panel handles see 9.1 (8).

Figure 14 – Quadruple height board type plug-in unit

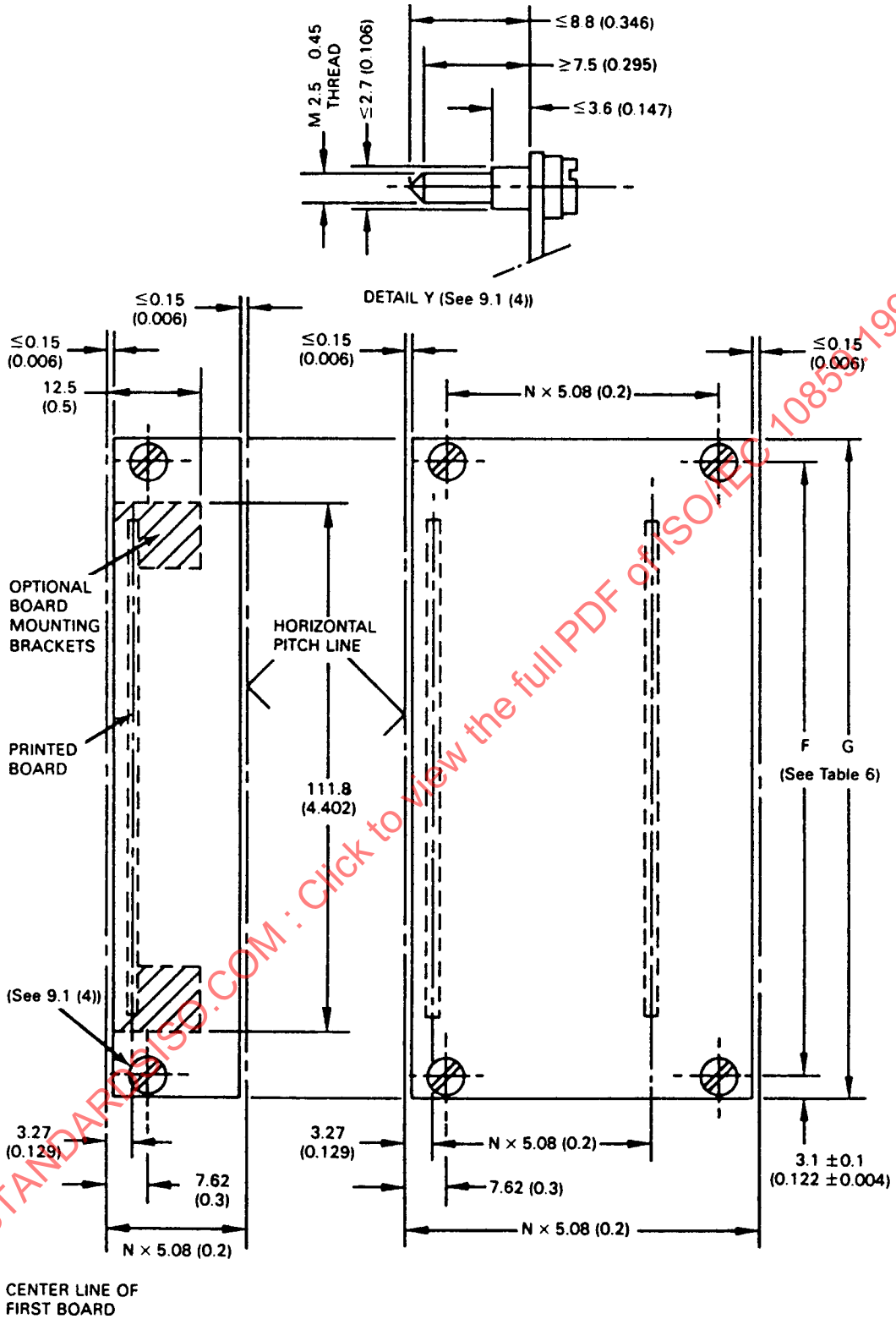


Figure 15 – Board type plug-in unit front panel

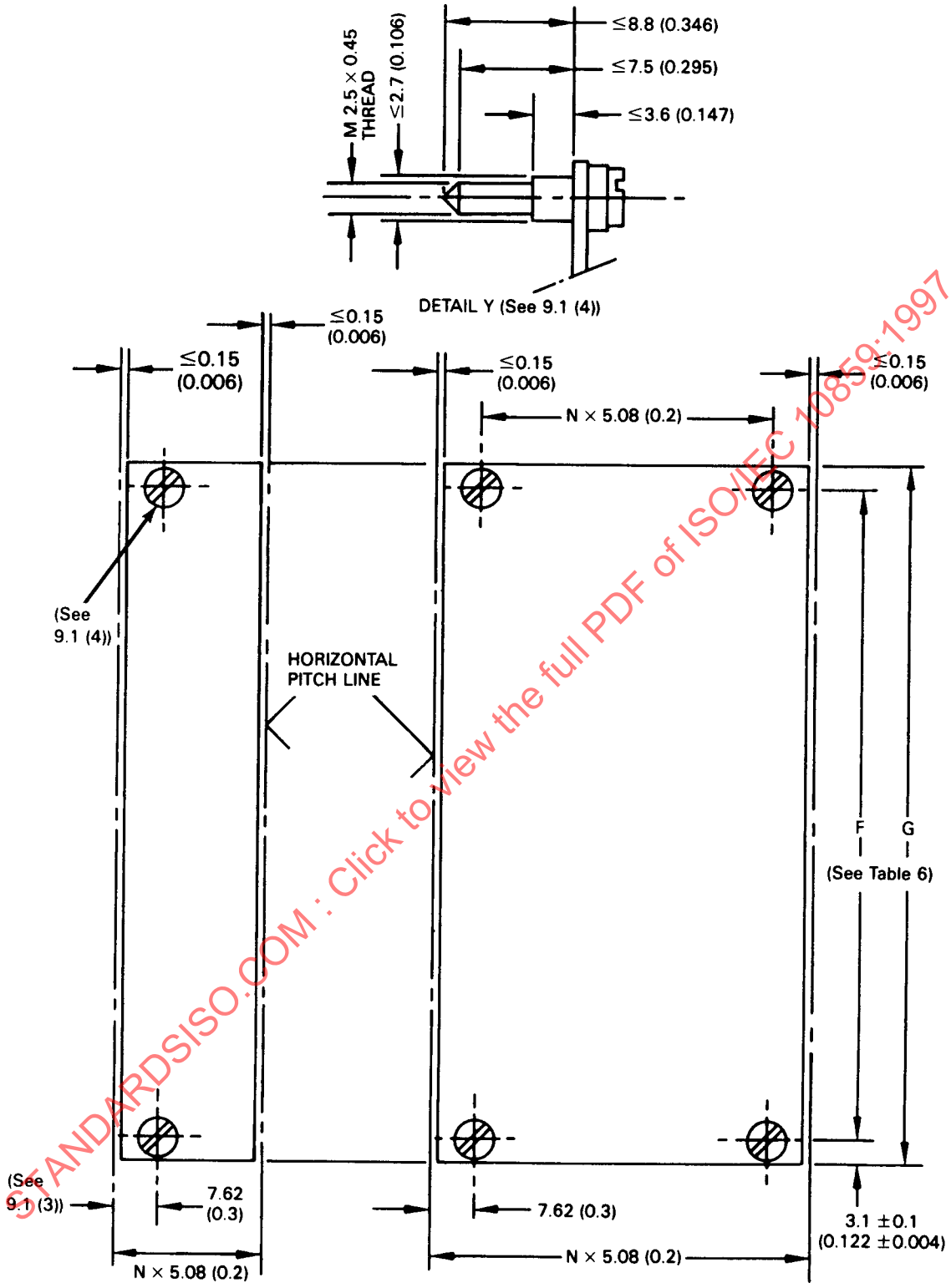
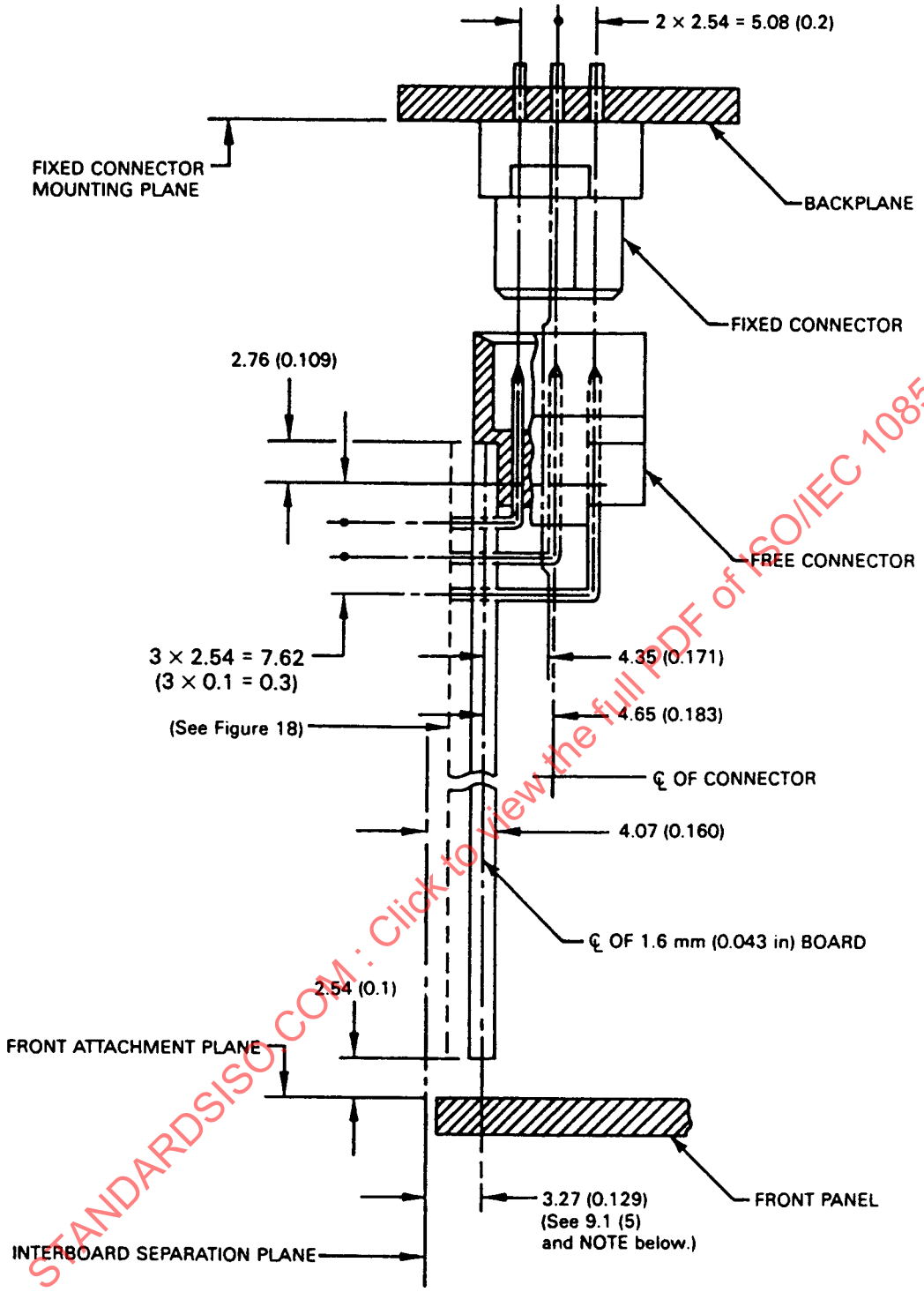
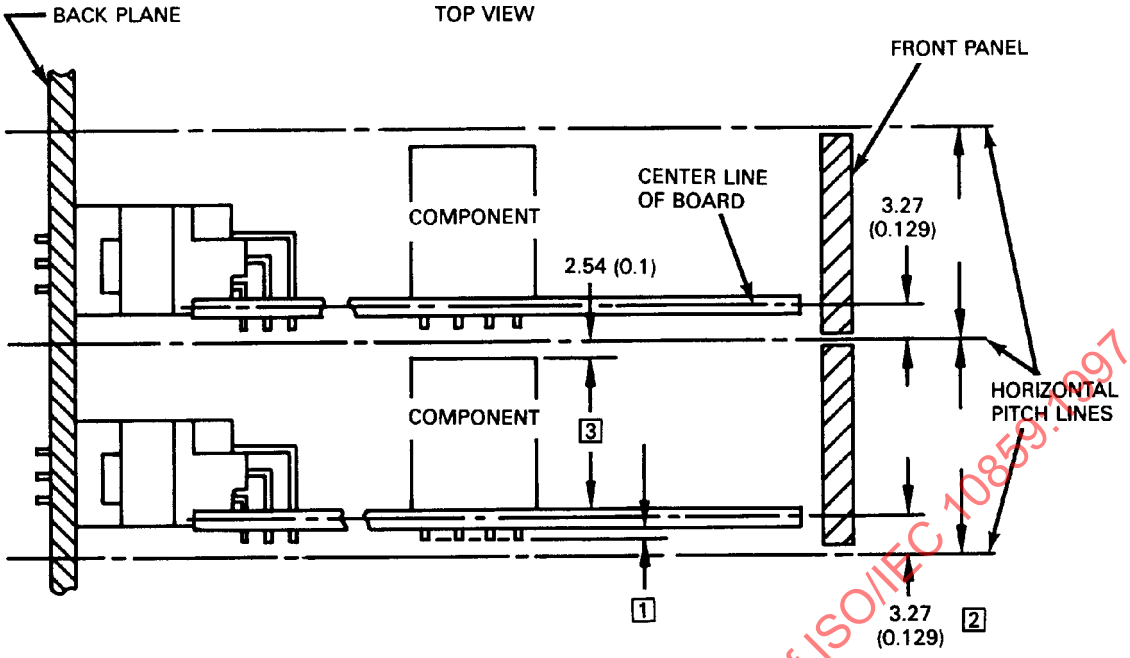


Figure 16 – Filler panels



NOTE – The dimension 3,27 mm (0,129 in) represents the first board position for conventional component mounting (solder-side/component side). For double-sided SMD mounted boards this dimension may be increased to 8,35 mm (0,329 in).

Figure 17 – Front panel, board, connector, backplane relationship

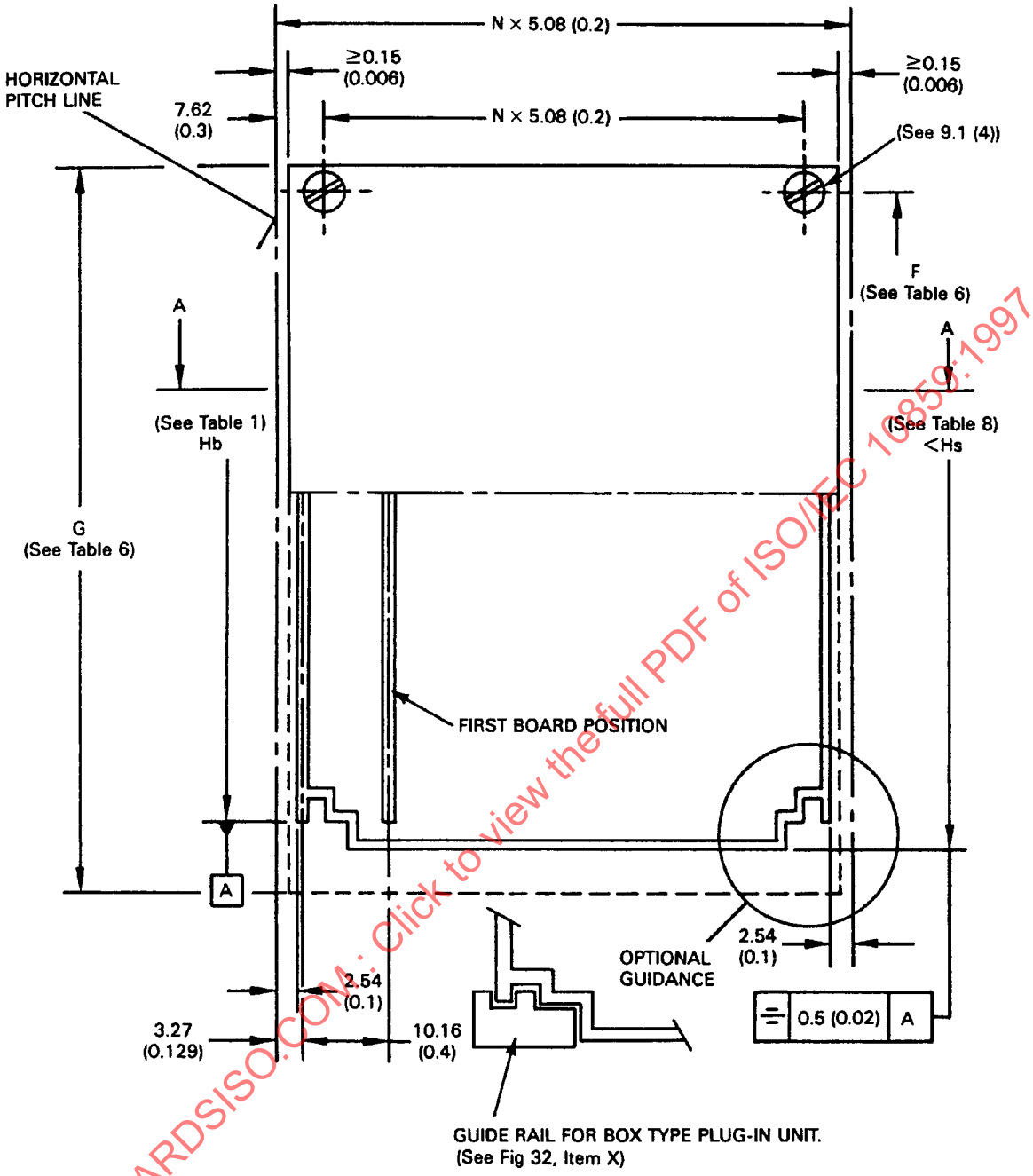


1 1,52 mm (0,06 in) maximum recommended pin length.

2 Solder pins of components and solder side mounted components shall not protrude the horizontal pitch line.

3 Components shall not protrude 2,54 mm (0,1 in) below the horizontal pitch line. Component height restrictions will vary depending on the manufacturer's ability to control board warp and thickness, measured on installed boards.

Figure 18 – Board warpage/board-to-board relationship



NOTE – See 6.4, 9.2 (3), and 9.2 (5).

Figure 19 – Box type plug-in unit, front view

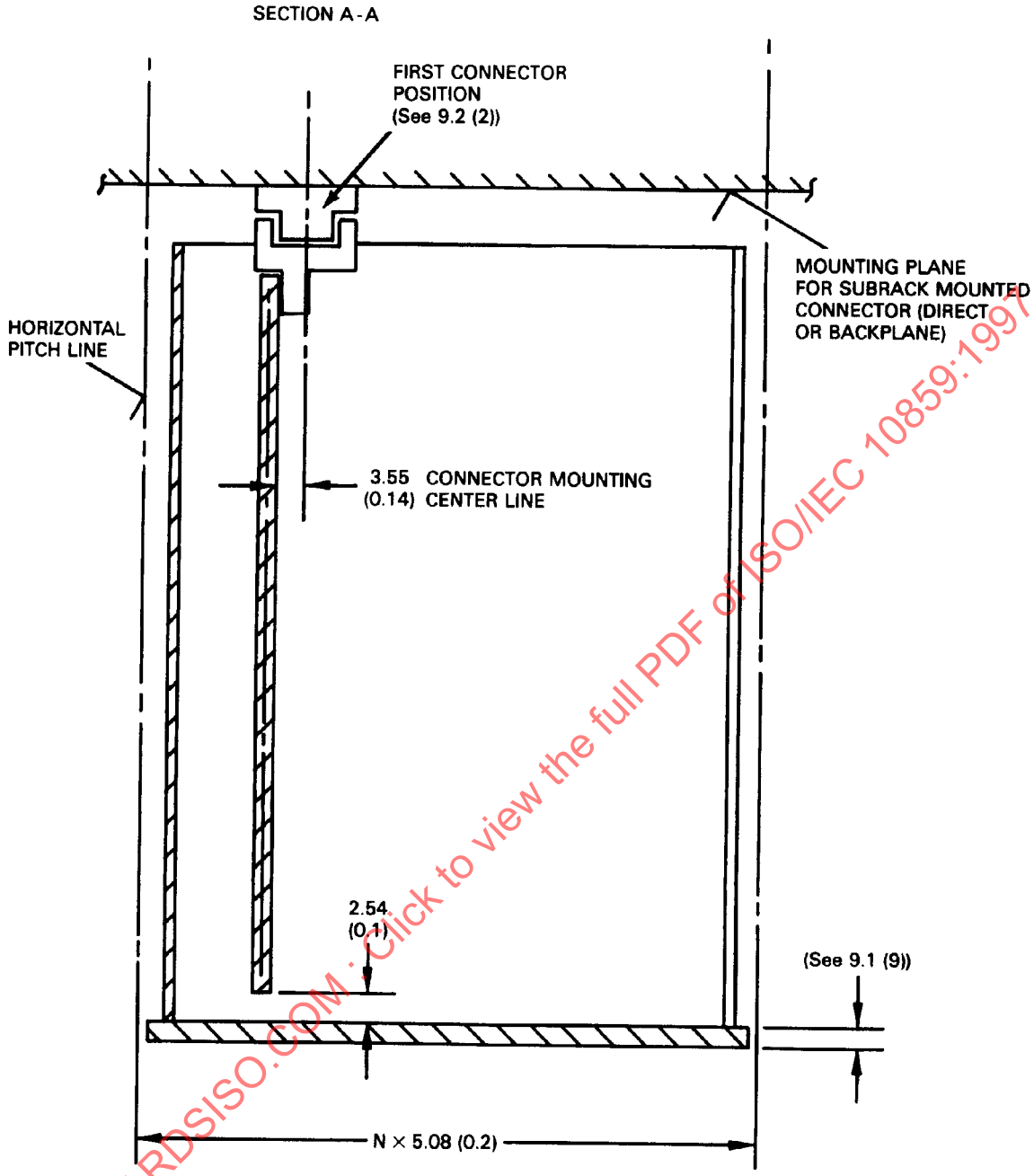
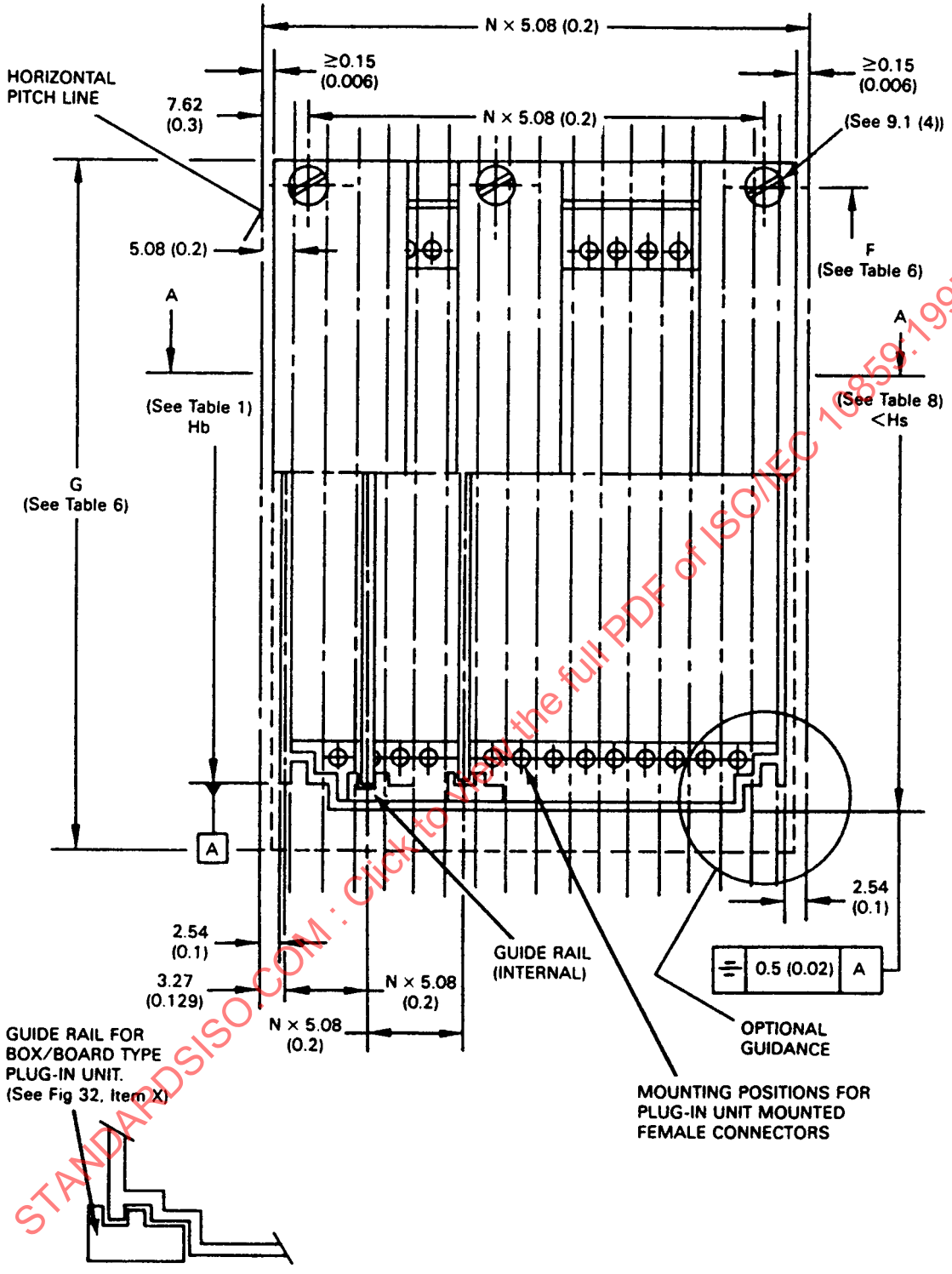


Figure 20 – Box type plug-in unit, plan view section A-A



NOTE – Known as well by the name "cassette." Internal guides have the same board slot feature as shown in figure 32, item X. See 6.4, 9.2 (4), and 9.2 (5).

Figure 21 – Box/board type plug-in unit, front view

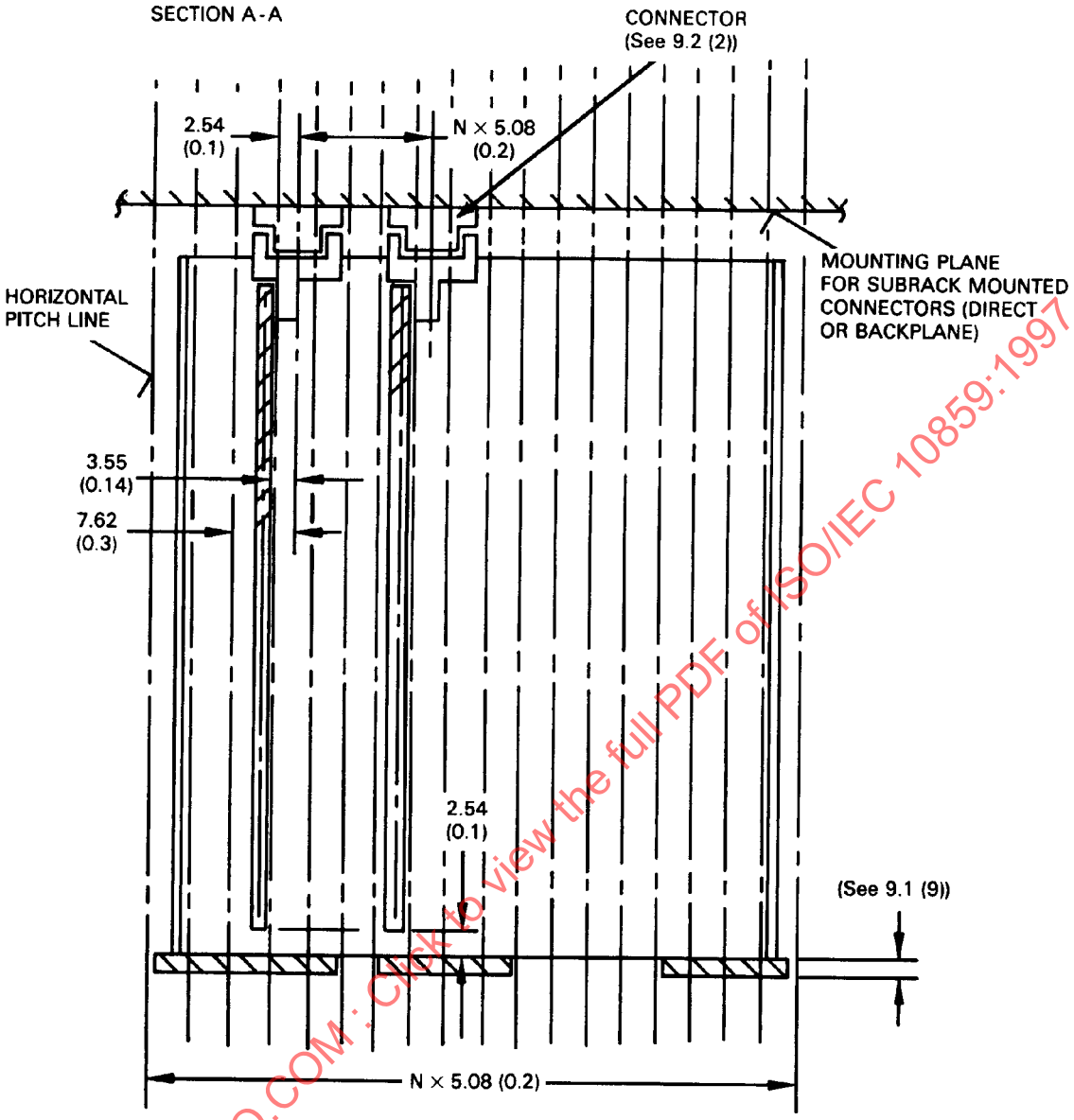
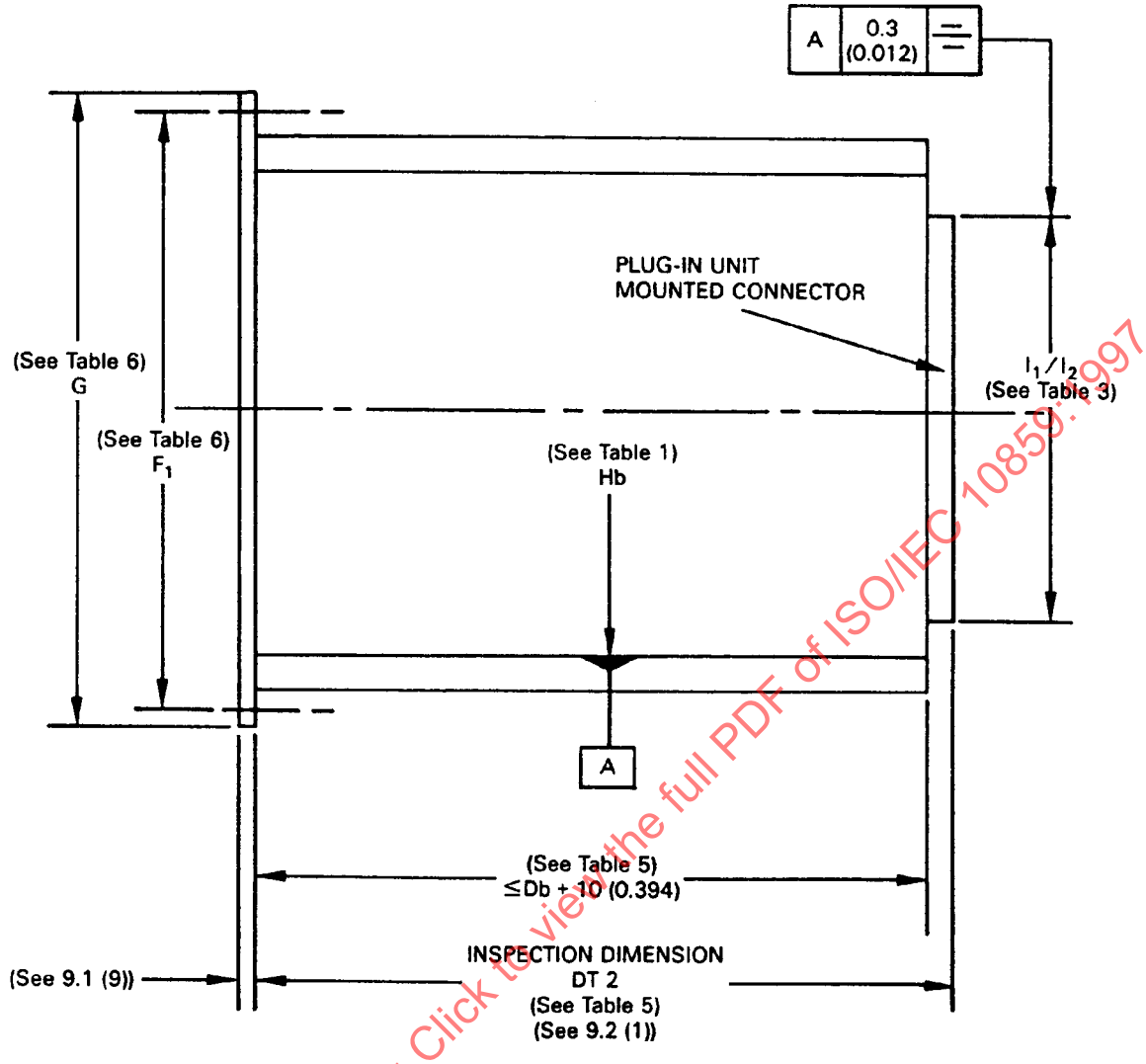
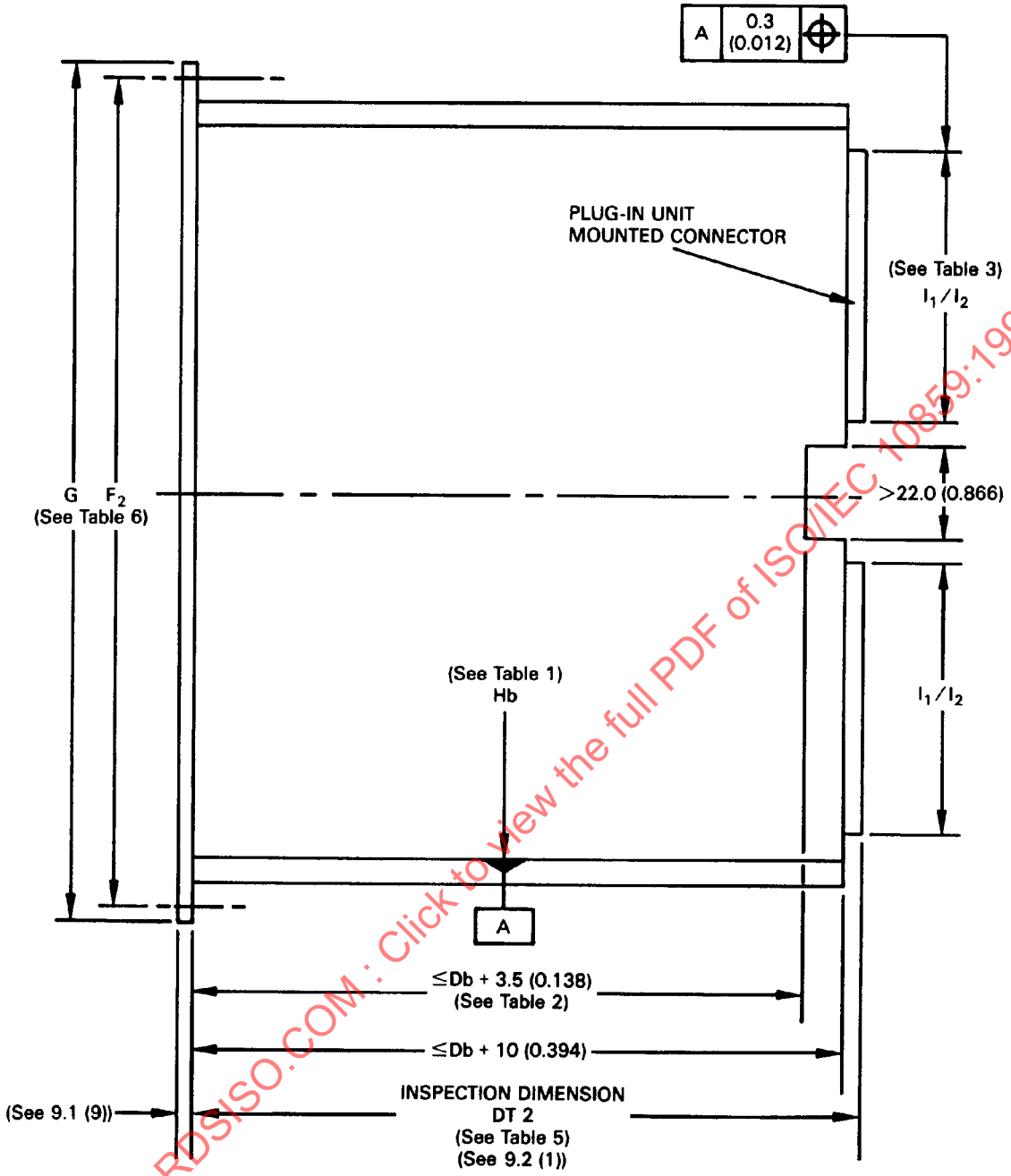


Figure 22 – Box/board type plug-in unit, plan view section A-A



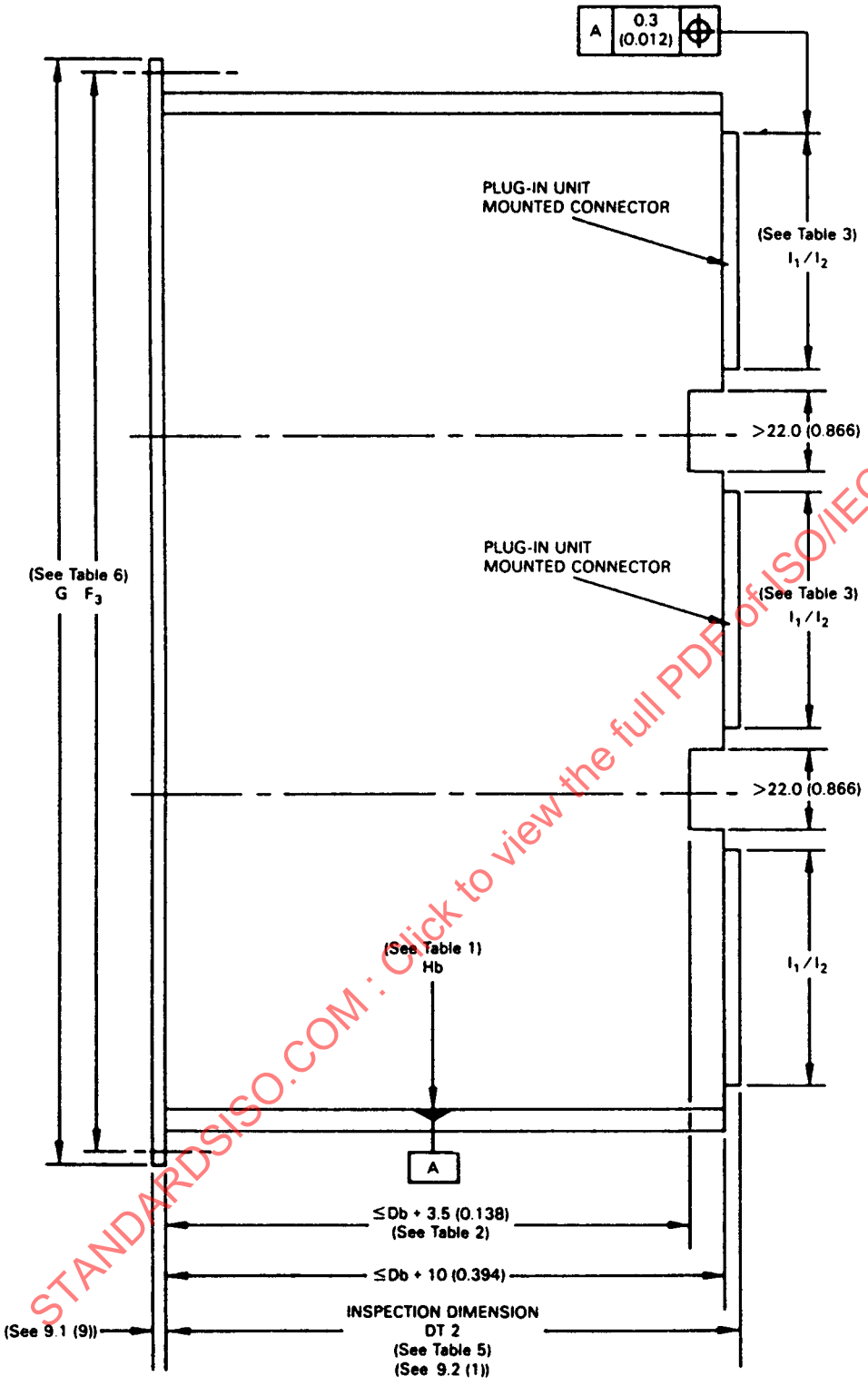
NOTE – See 9.2 (5).

Figure 23 – Box type, box/board type plug-in unit, single height side view



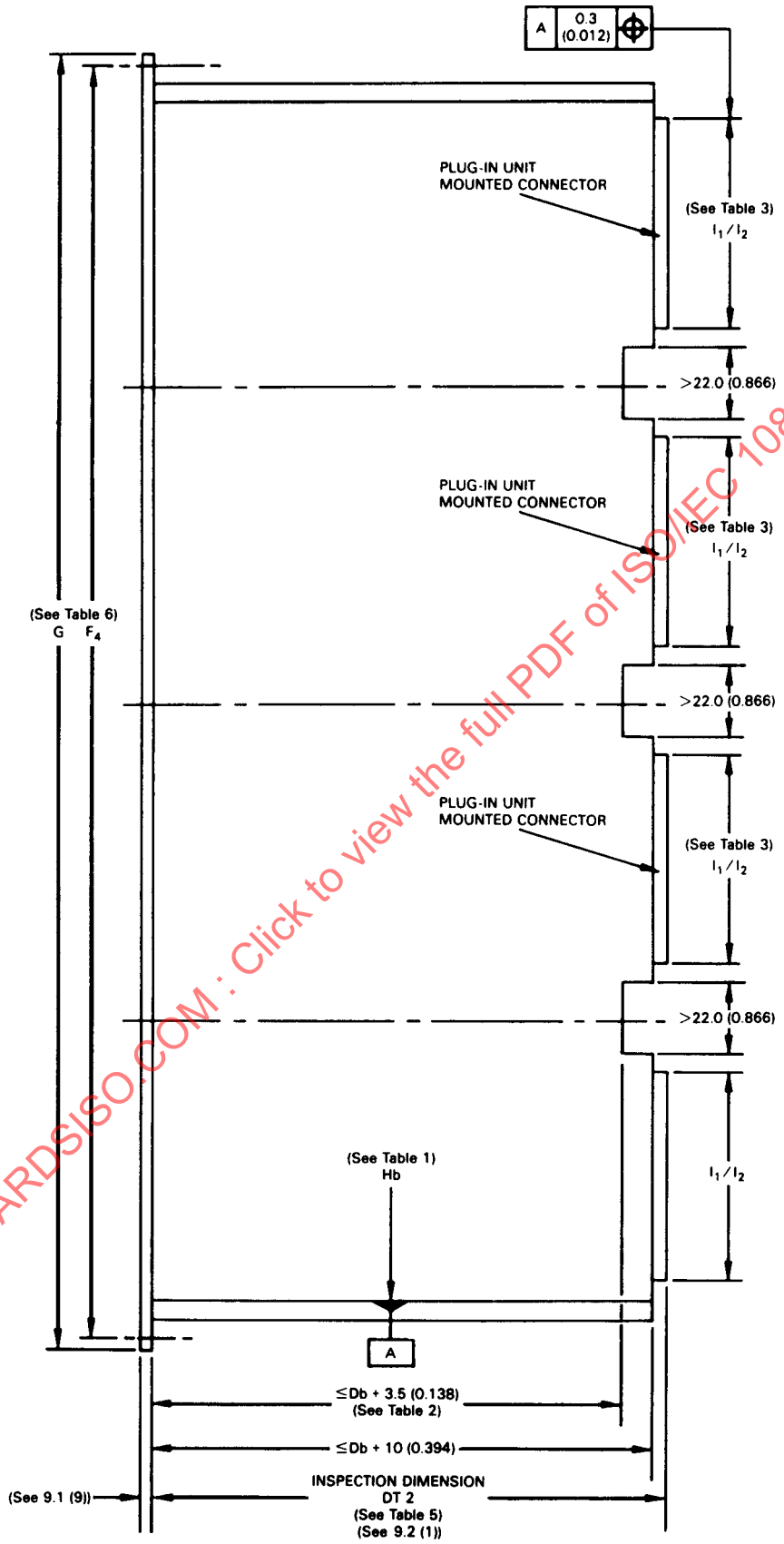
NOTE – See 9.2 (5).

Figure 24 – Box type, box/board type plug-in unit, double height side view



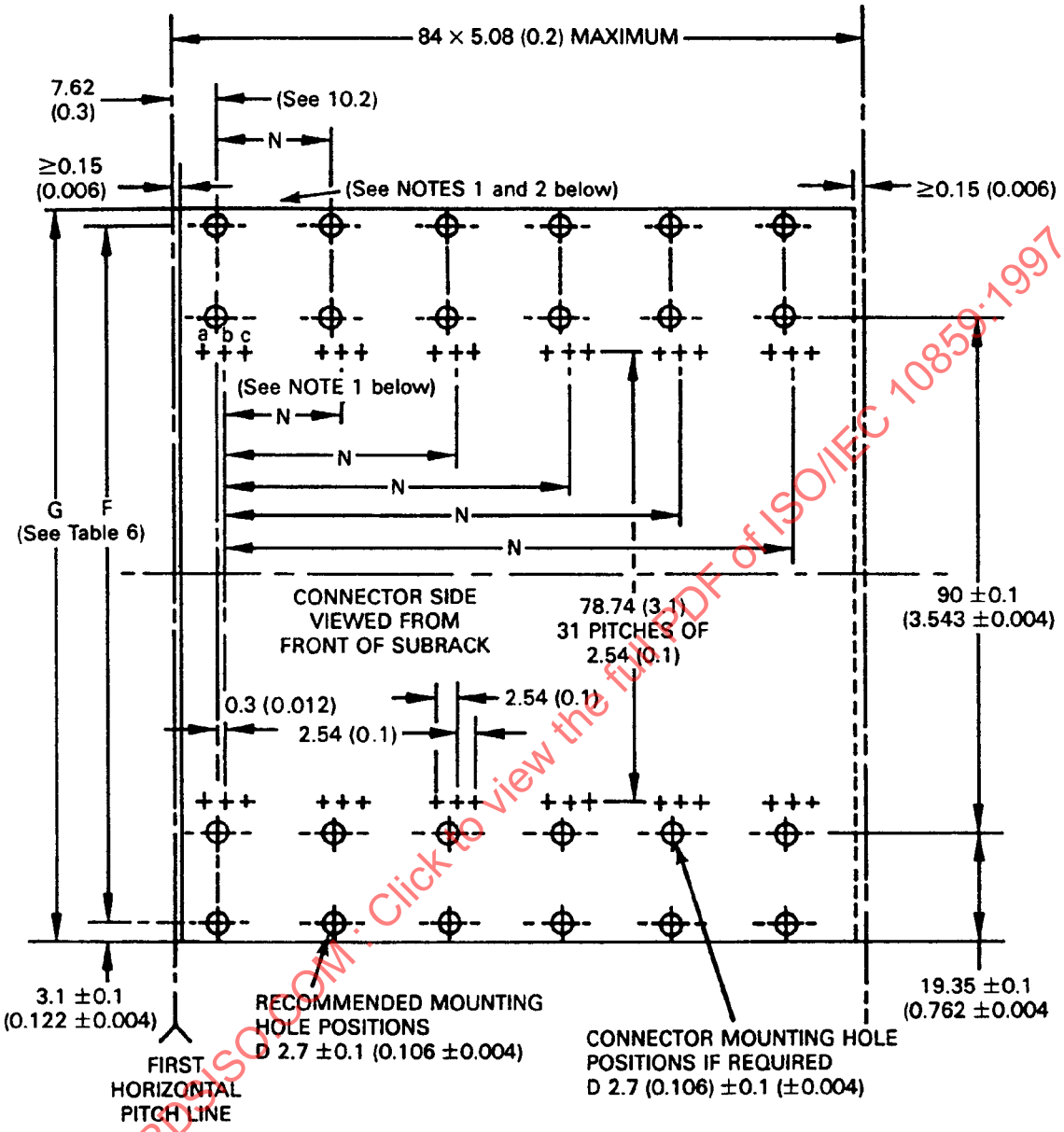
NOTE – See 9.2 (5).

Figure 25 – Box type, box/board type plug-in unit, triple height side view



NOTE – See 9.2 (5).

Figure 26 – Box type, box/board type plug-in unit, quadruple height side view

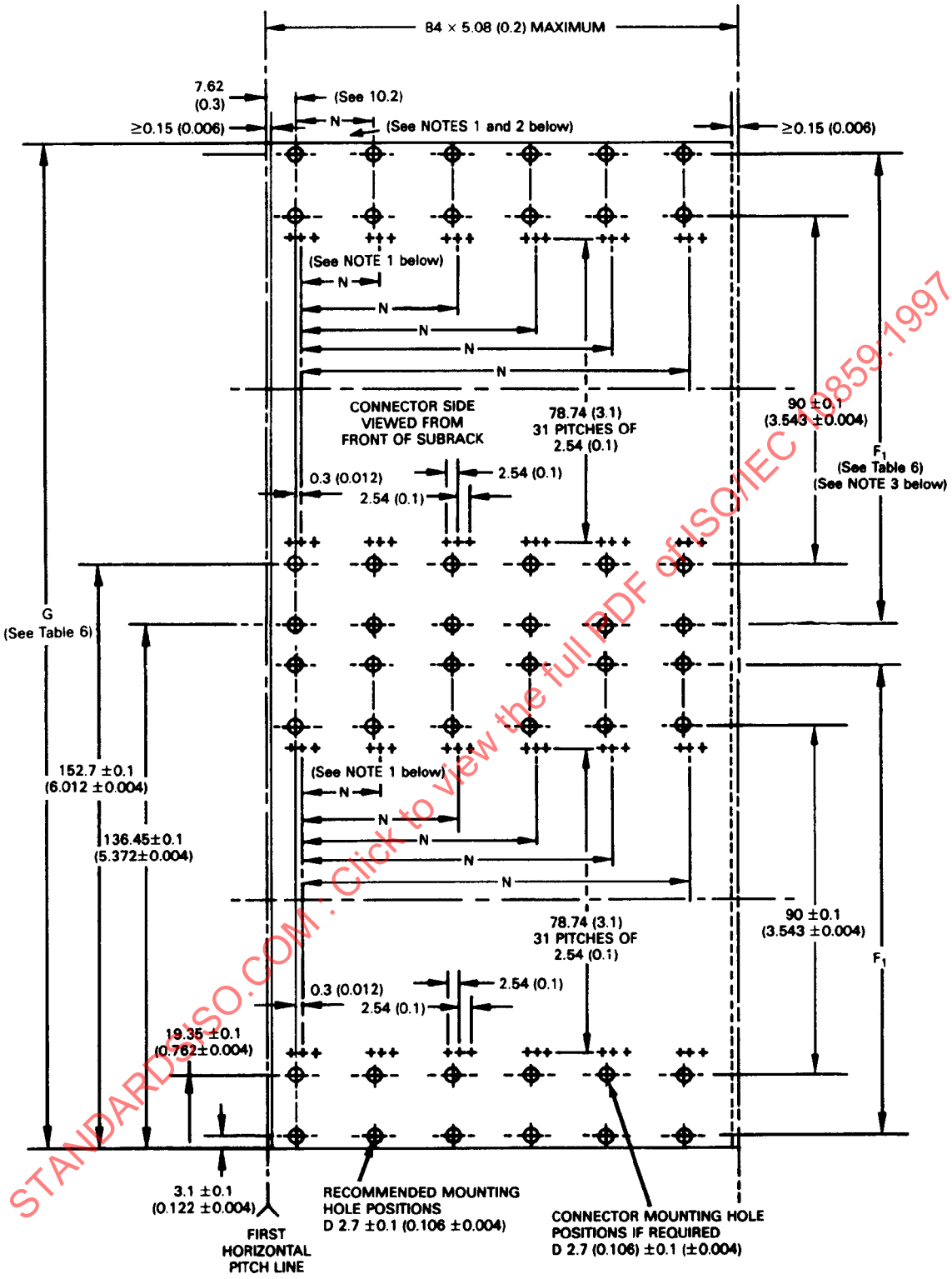


NOTES

1 N = multiples of 5,08 mm (0,2 in).

2 The distance between the subrack mounting holes has to be chosen to give adequate support to the backplane.

Figure 27 – Single height backplane



NOTES

1 N = multiples of 5,08 mm (0,2 in).

2 The distance between the subrack mounting holes has to be chosen to give adequate support to the backplane.

3 The use of fixtures may be required to mount connectors to guarantee intermateability.

Figure 28 – Double height backplane