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Aerospace — High-power solid-state power controller — General performance requirements

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Foreword

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The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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This document was prepared by Technical Committee ISO/TC 20, *Aircraft and space vehicles*, Subcommittee SC 1, *Aerospace electrical requirements*.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

For aircrafts electrical power systems, there is a trend toward higher voltage and higher current systems. There are several advantages in using a solid-state power controller (SSPC) for the distribution system. A standard of the SSPC for lower electrical power supply has been established (ISO 27027); but the standard for the SSPC for higher electrical power supply, which is intended for application in the primary power distribution of aircrafts, has not been established. Therefore, it is necessary to develop a standard for the high-power solid-state power controller (HPSSPC).

The purpose of this document is to standardize the requirements for HPSSPCs that are physically and environmentally diversified.

The HPSSPC:

a) consists of a solid-state switching device and its driver circuit;

b) turns on or off the power output by receiving the control signal;

c) detects the over current in the load which results in limiting or shutting down this current, and/or optionally detects the arc fault in the circuit which results in shutting down the fault;

d) has the built-in test function which can detect the health status of itself;

e) indicates the on or off status of the power output.

In order to satisfy this purpose, this document specifies requirements such as physical, environmental and individual items in accordance with the detail requirements that are issued individually.

Aerospace — High-power solid-state power controller — General performance requirements

1 Scope

This document specifies the general performance requirements and test methods to determine the performance of the high-power solid-state power controller (HPSSPC) for use in the primary power distribution of aircrafts.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 1540, *Aerospace — Characteristics of aircraft electrical systems*

ISO 7137:1995, *Aircraft — Environmental conditions and test procedures for airborne equipment*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

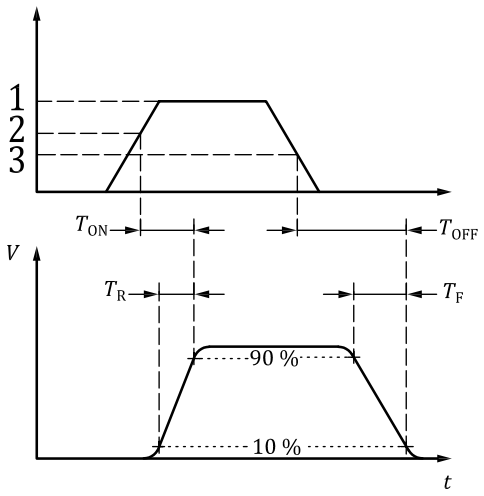
ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

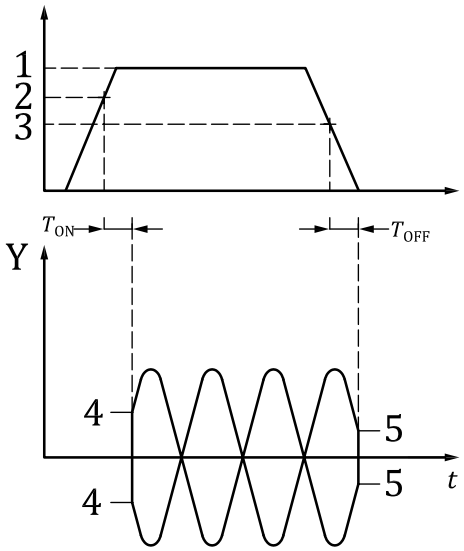
— IEC Electropedia: available at https://www.electropedia.org/

3.1
turn-on time
<DC device and non-zero-crossing turn-on AC device> time interval between the initiation of the *turn-on signal* (3.5) or the latest frame of the turn-on command data packet via the control signal bus and the time when the output reaches 90 % of its steady-state on value

Note 1 to entry: Shown in Figure 1 a).



a) DC HPSSPC



b) AC HPSSPC

Key

Y	load voltage
V	voltage
t	time
T_{ON}	turn-on time
T_{OFF}	turn-off time
T_R	rise time
T_F	fall time
1	rated control signal (which can optionally consist of control bus)
2	turn on (min)
3	turn off (max)
4	zero voltage turn-on
5	zero current turn-off

Figure 1 — Illustration of timing characteristics

3.2
turn-on time
<AC device with zero-crossing turn-on> time interval between the initiation of the *turn-on signal* (3.5) or the latest frame of the turn-on command data packet via the control signal bus and the time when the output switch is on at zero-crossing

Note 1 to entry: Shown in Figure 1 b).

3.3
turn-off time
<DC device and non-zero-crossing turn-on AC device> time interval between the initiation of the turn-off signal or the latest frame of the turn-off command data packet via the control signal bus and the time when the output reaches 10 % of its steady-state on value

Note 1 to entry: Shown in Figure 1 a).

3.4
turn-off time
<AC device with zero-crossing turn-on> time interval between the initiation of the turn-off signal or the latest frame of the turn-off command data packet via the control signal bus and the time when the output switch is off at zero-crossing

Note 1 to entry: Shown in Figure 1 b).

3.5
turn-on signal
control signal level or turn-on command data packet via the control signal bus at which the power controller is turned on

3.6
turn-off signal
control signal level or turn-off command data packet via the control signal bus at which the power controller is turned off

3.7
load voltage rise and fall time
time interval between 10 % and 90 % of the steady state *load voltage* (3.10) value

Note 1 to entry: This definition applies to DC devices and non-zero-crossing turn-off AC devices.

Note 2 to entry: The load voltage rise and fall time for DC devices is shown in Figure 1 a).

[SOURCE: ISO 27027:2014, 3.4, modified — "(DC devices and non-zero-crossing turn-off AC devices)" has been moved from the term to Note 1 to entry; the reference to Figure 1 a) has been moved from the end of the definition to Note 2 to entry.]

3.8
soft on/off
function for the power output current to increase linearly with the *turn-on signal* (3.5) or the turn-on command data packet via the control signal bus and to decrease linearly with the turn-off signal or the turn-off command data packet via the control signal bus

3.9
supply voltage
voltage applied between the power input terminal of the *HPSSPC* (3.13) and the power ground

3.10
load voltage
voltage between the power output terminal of the *HPSSPC* (3.13) and the power ground

3.11
voltage drop
voltage across load and line terminals of the *HPSSPC* (3.13) in the *on state* (3.20) at the specified load

3.12
rated current
supplied maximum current that the *HPSSPC* (3.13) continuously outputs from the output terminal without tripping

3.13
HPSSPC
high-power solid-state power controller
solid-state power controller (SSPC) which is applied on primary power distribution

3.14
power dissipation
power loss which includes all power dissipated in the power switching circuit, due to internal leakage currents and power supplies

Note 1 to entry: When the *HPSSPC* (3.13) is off, the power dissipation includes only dissipation due to leakage currents and internal power supplies.

3.15
HPSSPC trip
automatic reversion to the *off state* (3.21) of the *HPSSPC* (3.13) output caused by an overcurrent or a *short circuit* (3.22) condition or detection of an *arc fault* (3.28)

3.16
HPSSPC trip-free
feature which prevents subsequent re-closing unless preceded by a *reset* (3.19) signal, when the *HPSSPC* (3.13) has tripped due to an overcurrent or a *short circuit* (3.22) condition or detection of an *arc fault* (3.28)

3.17
trip time
time interval between the application of an overcurrent or a *short circuit* (3.22) condition or detection of an *arc fault* (3.28) and the 10 % value of rated output current

Note 1 to entry: In general, the higher the over current condition, the shorter the trip time.

3.18
trip curve
curve which sets the minimum and maximum trip points of the *HPSSPC* (3.13) and is plotted as current versus time

3.19
reset
restoration of the tripped *HPSSPC* (3.13) to a state from which it can be turned on

3.20
on state
condition in which, with the *turn-on signal* (3.5) applied, the device allows power to be passed to the load

[SOURCE: ISO 27027:2014, 3.6]

3.21
off state
condition in which, with the turn-off signal applied, the device prevents power from being passed to the load

[SOURCE: ISO 27027:2014, 3.5]

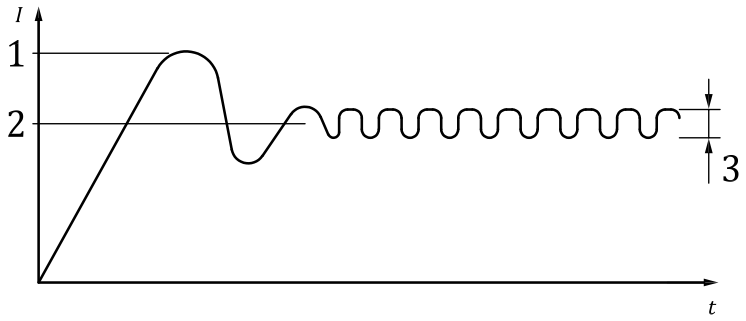
3.22
short circuit
circuit with the impedance of less than 1 mΩ applied between the output terminal and ground

[SOURCE: ISO 27027:2014, 3.13]

3.23
current limiting
function to limit the power output current to the required level within required time from overload or *short circuit* (3.22) conditions

Note 1 to entry: Shown in Figure 2.

[SOURCE: ISO 27027:2014, 3.2, modified — The reference to Figure 2 has been moved from the end of the definition to Note 1 to entry.]



Key

I	load current
t	time
1	peak let-through current
2	specified current limit
3	ripple

Figure 2 — Overload let-through current

3.24
peak let-through current
peak value of the current at the maximum system voltage that the *HPSSPC* (3.13) conducts for a specified time interval without damage

3.25
zero voltage turn-on
characteristic that requires the *HPSSPC* (3.13) to turn on only at the half-cycle zero-crossing point, regardless of when the control signal is applied

Note 1 to entry: This characteristic applies only to AC devices.

3.26
zero current turn-off
characteristic that requires the *HPSSPC* (3.13) to turn off only at the half-cycle zero-crossing point, regardless of when the control signal is removed

Note 1 to entry: This characteristic applies only to AC devices.

3.27
reverse current
current into the load terminal of the *HPSSPC* (3.13) from the load energy source

3.28
arc fault
sustained luminous discharge of electricity across a gap in a circuit or between conductors

Note 1 to entry: Arc impedance can reduce low-voltage fault current magnitudes appreciably.

[SOURCE: ISO 27027:2014, 3.1]

3.29
parallel arc fault
arc fault (3.28) condition in which arcing occurs in a circuit from line-to-line or line-to-ground and not through any load(s)

Note 1 to entry: Only the arc impedance and the system current impedance limit the magnitude of the arc fault current.

[SOURCE: ISO 27027:2014, 3.7]

3.30
series arc fault
arc fault (3.28) condition in which the current passes through the arc and each circuit load

Note 1 to entry: The load equipment limits the magnitude of the arc fault current.

[SOURCE: ISO 27027:2014, 3.12]

4 Requirements

4.1 Detail requirements

The individual item requirements shall be specified in accordance with the detail requirements that are issued individually. ISO 7137 should be used for the specification of environmental conditions and test procedures for the SSPCs installed in the airborne equipment.

4.2 Electrical characteristics

When tested as specified in 5.1, the HPSSPC shall operate with supply voltage variations in accordance with ISO 1540 or the detail requirements; and the HPSSPC shall be capable of controlling all type of loads as required by the detail requirements.

4.3 Performance

4.3.1 Control signals

When tested as specified in 5.2, the control signals shall be as specified in the detail requirements.

4.3.2 Turn-on and turn-off time

When tested as specified in 5.3, the turn-on and turn-off time shall be as specified in the detail requirements.

4.3.3 Load voltage rise and fall time (soft on/off function)

When tested as specified in 5.4, the rise and fall time as the soft on/off function shall be as specified in the detail requirements.

4.3.4 Isolation

When tested as specified in 5.5, the control/power isolation test voltage shall be as specified in the detail requirements.

4.3.5 Control signal levels

When tested as specified in 5.6, the control signal levels shall be as specified. Where maximum control signals are specified, the signals shall be applied for 10 min without any damage to the HPSSPC. The signals may be transferred via individual wire lines and/or buses.

4.3.6 Voltage drop

When tested as specified in 5.7, the voltage drop shall not exceed the values specified in the detail requirements for load current values from no load to 100 % rated.

4.3.7 Off state leakage current

When tested as specified in 5.8, the leakage current shall not exceed the values specified in the detail requirements.

4.3.8 Off state output voltage

When tested as specified in 5.9, the output voltage shall not exceed the values specified in the detail requirements.

4.3.9 Power dissipation

When tested as specified in 5.10, the power dissipation shall not exceed the values specified in the detail requirements.

4.3.10 Overload characteristics

4.3.10.1 Current limiting

When specified in the detail requirements and tested as specified in 5.11.1, the output current shall be within the trip curve specified. At the initiation of the overload condition, the peak let-through current (see 4.1) shall not exceed the value specified.

4.3.10.2 HPSSPC trip characteristics with the overload condition

4.3.10.2.1 HPSSPC trip characteristics with the short circuit condition

When tested as specified in 5.11.2.1, the HPSSPC shall not reset until commanded; the trip time shall be within the trip curve specified in the detail requirements without any damage.

4.3.10.2.2 HPSSPC trip characteristics with the overcurrent condition

When tested as specified in 5.11.2.2, the HPSSPC shall not reset until commanded, the trip time shall be within the trip curve specified in the detail requirements without any damage.

4.3.11 State indication

When tested as specified in 5.12, the HPSSPC shall provide the means of state indication specified in the detail requirements. State indication shall include the detection of load current above or below a minimum current threshold and the presence or absence of drive to the output power switches as specified in the detail requirements. These state indication means, in conjunction with the control signal, shall be capable of providing feedback on normal controller operation or controller faults as specified in the detail requirements.

4.3.12 HPSSPC trip-free characteristics

When tested as specified in 5.13, the HPSSPC shall reset, trip-out and stay tripped out for the duration of the test.

4.3.13 Zero voltage turn-on and zero current turn-off (AC HPSSPC)

When tested as specified in 5.14, the HPSSPC turn-on shall occur at zero voltage crossovers within the voltage or time specified; and the HPSSPC turn-off shall occur at zero current crossover within the current or time specified. The HPSSPC shall turn-on and turn-off at the same voltage slope when specified.

4.3.14 Reverse current

When specified in the detail requirements and tested as specified in 5.15, the HPSSPC shall be performed as specified without any damage.

4.3.15 Exponential rate of voltage rise

When tested as specified in 5.16, the HPSSPC shall achieve the specified output voltage within the specified time.

4.3.16 Arc fault characteristics

4.3.16.1 HPSSPC trip characteristics with parallel arc fault

When tested as specified in 5.17.1 and 5.17.2, the HPSSPC shall trip by the parallel arc fault; the trip time shall be within the trip curve specified in the detail requirements without any damage.

4.3.16.2 HPSSPC trip characteristics with series arc fault

When tested as specified in 5.17.3, the HPSSPC shall trip by the series arc fault; the trip time shall be within the HPSSPC trip characteristics specified in the detail requirements without any damage.

4.3.16.3 Compatibility with normal load

When tested as specified in 5.17.4, the HPSSPC shall not trip by normal loads.

4.3.16.4 Compatibility with arc fault of another line

When tested as specified in 5.17.5, the HPSSPC shall not trip by the arc fault on another circuit on the same source.

4.3.17 Built-in test

When specified in the detail requirements and tested as specified in 5.18, HPSSPC shall detect the health status of internal electrical and/or thermal circuits.

Unless otherwise specified, the HPSSPC should have BIT (built-in test) modes as follows. Actions and state indications against any fault on the HPSSPC's internal circuits should be designed.

— Mode 1: Initial BIT. The initial health status of HPSSPC should be tested just after its boot up condition has been done, before the HPSSPC accepts turn-on commands.

— Mode 2: Continuous BIT. The health status of HPSSPC should be tested while the HPSSPC can accept turn-on commands without degrading HPSSPC performance.

— Mode 3: Initiate BIT. The health status of HPSSPC should be tested on response to test requests via the input commands as specified in the detail requirements.

4.3.18 Setting change for the rated current

When specified in detail requirements and tested as specified in 5.19, the rated current of HPSSPC may be changed according to the requirements. The trip curve of HPSSPC should be changed to correspond to a specific setting change for the rated current. The setting changes for the trip curve should be limited within the range of rated value, not to exceed absolute maximum ratings of the HPSSPC. The HPSSPC should be optionally able to accept commands to change the rated current from other devices or systems than the HPSSPC.

The initial setting change during the boot-up period should be specified in detail requirements while the output currents are disabled. On-command setting change should be prohibited unless otherwise specified in detail requirements. In case this setting change is acknowledged, the on-command setting change should be validated according to the safety assessment.

5 Quality assurance provisions on electrical characteristics

5.1 General

When performing electrical tests, the HPSSPC shall be mounted on a suitable heat sink (see 4.1). Unless otherwise specified, all tests shall be made within the following ambient conditions:

a) ambient temperature: +15 °C to +35 °C;

b) relative humidity: not greater than 85 %;

c) ambient pressure: 84 kPa to 107 kPa, which correspond to the altitude between +1 525 m and −460 m (+5 000 feet and −1 500 feet).

5.2 Control signals

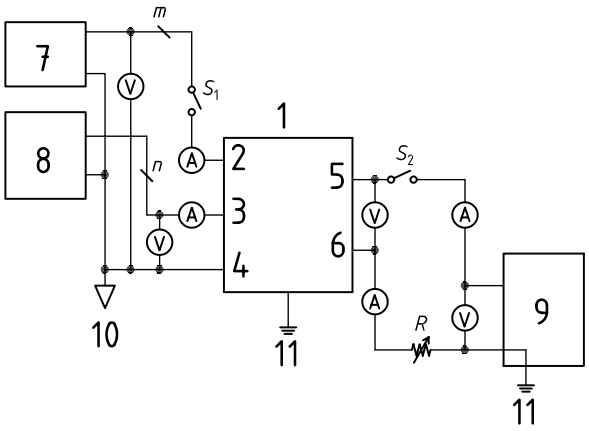
5.2.1 General

See 4.3.1.

The control signals shall be verified as specified in 5.2.2 and 5.2.3.

5.2.2 Turn-on signal

With the HPSSPC connected as shown in Figure 3, apply the rated supply voltage and adjust the load resistance for the rated load with a tolerance of ±5 %. Apply the minimum turn-on signals with the control function generator and note that the HPSSPC turns on. The signals may be transferred via individual wire lines and/or buses.



Key

1 HPSSPC under test
2 control (discrete signals and/or bus which may input control)
3 state indication(s) [discrete signals and/or bus which may optionally output state indication(s)]
4 signal ground
5 power in
6 power out
7 control function generator
8 state indication power supply
9 supply voltage AC or DC as applicable
10 signal ground
11 power ground
R load resistance
S_1 bounceless switch
S_2 bounceless switch
m wire count or optionally the number of the buses for control (m = 1, 2, 3, etc.)
n wire count or optionally the number of the buses for state indication(s) (n = 0, 1, 2, etc.)

Figure 3 — Test circuit

5.2.3 Turn-off signal

With the HPSSPC on at rated control signals, apply the maximum turn-off signals with the function generator and note that the HPSSPC turns off. The signals may be transferred via individual wire lines and/or buses.

5.3 Turn-on and turn-off time

Measure turn-on and turn-off time with the HPSSPC operated as in 5.2.2 and 5.2.3.

5.4 Load voltage rise and fall time

Measure the rise and fall time with the HPSSPC operated as in 5.2.2 and 5.2.3.

5.5 Isolation

See 4.3.4.

The power-in terminal, power-out terminal and power-ground terminal shall be shorted together. All remaining terminals shall be shorted together. The points of application shall be the signal ground and power ground terminals, and electrification time shall be maximum 2 min, as specified in the detail requirements, unless otherwise specified in the test procedure 3.9 in ISO 7137:1995, Table 1.

5.6 Control signal levels

See 4.3.5.

With the rated supply voltage applied, apply control signals with the level as specified and measure control current or voltage. Repeat test for each control signal level specified. The signals may be transferred via individual wire lines and/or buses.

5.7 Voltage drop

See 4.3.6.

With the HPSSPC connected as shown in Figure 3, measure the voltage between the power-in and the power-out terminals while operating at 10 %, 50 % and 100 % rated load. For the AC HPSSPC, a true root mean square voltmeter shall be used.

5.8 Off state leakage current

See 4.3.7.

Connect the HPSSPC as shown in Figure 3 with the load resistance adjusted for a maximum of 10 Ω, the rated supply voltage applied to the power-in terminal and the control circuit commanded off, read the leakage current.

5.9 Off state output voltage

See 4.3.8.

Connect the HPSSPC as shown in Figure 3, without the load resistance, with the rated supply voltage applied to the power-in terminal with the control circuit commanded off, read the output voltage on a voltmeter with a minimum internal resistance of 10 MΩ.

5.10 Power dissipation

See 4.3.9.

Connect the HPSSPC as shown in Figure 3 with the load resistance adjusted for short circuit, the rated supply voltage applied to the power in terminal and the controller commanded off. Calculate the power dissipation for the off state, including bias and control. With the controller commanded on, calculate the power dissipation for the on state for no load and loads of 10 %, 50 % and 100 % rated load, unless otherwise specified in the specification sheet, including bias and control power.

5.11 Overload characteristic tests

5.11.1 Current limiting

See 4.3.10.1.

Connect the HPSSPC as shown in Figure 3. With the load adjusted to the rated level, apply the rated supply voltage and turn-on the control. While monitoring the current out of the HPSSPC, apply a short circuit across the load and measure the peak let-through current and the current limit level.

5.11.2 HPSSPC trip characteristics

5.11.2.1 HPSSPC trip characteristics with the short circuit condition

See 4.3.10.2.1.

Connect the HPSSPC as shown in Figure 3. With the rated supply voltage, verify that the HPSSPC meets the HPSSPC trip characteristics at a simulated shorted current level (e.g. 1 000 % rated current) as specified in the detail requirements.

5.11.2.2 HPSSPC trip characteristics with the overcurrent condition

See 4.3.10.2.2.

Connect the HPSSPC as shown in Figure 3. With the rated supply voltage, verify that the HPSSPC meets the HPSSPC trip characteristics at various load levels specified in the detail requirements.

5.12 State indication signal(s)

See 4.3.11.

Connect the HPSSPC as shown in Figure 3. Apply the rated voltage and adjust the load resistance for 100 % rated load. Apply an off command to the control input. Monitor the specified (see 4.1) state indication feedback to verify the normal off operation and delay time. Apply an on command to the control input and verify the normal on operation and delay time. Reduce the load current below the indication. Increase the load current above the trip threshold and observe that the HPSSPC trips and verify the specified (see 4.1) trip indication and delay times.

5.13 HPSSPC trip-free characteristics

See 4.3.12.

Connect the HPSSPC as shown in Figure 3. Apply the rated voltage. Adjust the load resistor for short circuit and command controller on. Observe the HPSSPC trips out. Reset the controller and command controller on. Maintain the on command for 1 min minimum and verify that the HPSSPC resets and trips only once.

5.14 Zero voltage turn-on (ZVTO) and zero current turn-off (ZCTO)

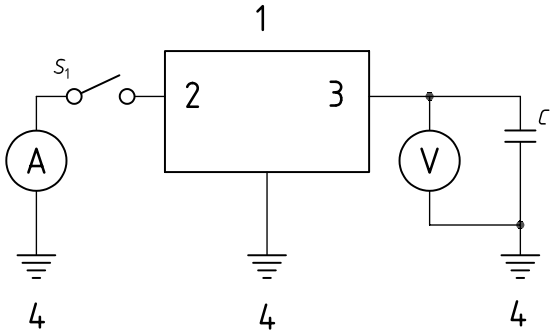
See 4.3.13.

Connect the HPSSPC as shown in Figure 3. Apply rated supply voltage and adjust load impedance for rated load with a 45 % lagging power factor. Apply the nominal turn-on signal and subsequently apply the nominal turn-off signal. Monitor the load voltage and current. Repeat the test 10 times. Adjust the load impedance to reduce the load current to below the minimum value specified (see 4.1) and repeat.

5.15 Reverse current

See 4.3.14.

Connect the HPSSPC as shown in Figure 4 with load capacitance according to the detail requirements. Charge the rated supply voltage to the load capacitor. While monitoring the current the power-in line of the HPSSPC, close S_1 and record the current waveforms. The HPSSPC shall perform as specified after dissipating a reverse energy.



Key

1 HPSSPC under test
2 power in
3 power out
4 power ground
C load capacitor
S_1 bounceless switch

Figure 4 — Test circuit for reverse current

5.16 Exponential rate of voltage rise

See 4.3.15.

The HPSSPC shall be tested for an exponential rate of voltage rise (when applicable) using the following procedure.

a) Set up the text in accordance with Figure 5.

b) Apply the specified control turn-off voltage.

c) Adjust the voltmeter V_1 to the maximum rated voltage. For the AC HPSSPC, V_1 is the maximum rated voltage:

$$V_1 = \sqrt{2}\, V_{\text{rated, RMS}}$$

where $V_{\text{rated, RMS}}$ is root mean square of AC voltage applied to HPSSPC.

d) With the power terminals (in and out) of the device disconnected, adjust the resistor R_1 to a value determined by

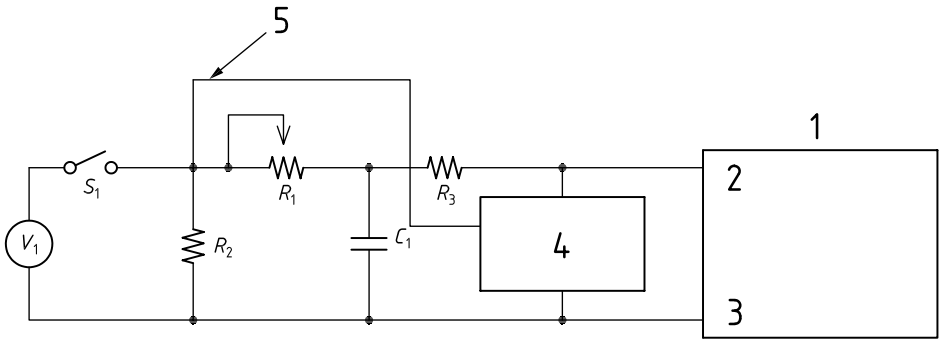
$$R_1 = 0{,}632 \times \frac{V_1}{C_1 (\mathrm{d}V / \mathrm{d}t)}$$

where dV/dt is as specified in Figure 6.

e) Reconnect the power terminals (in and out) of the device under test to the circuit shown in Figure 5.

f) Close and open the switch S_1 for a minimum of 10 times. After five cycles, reverse the leads to the device under test (for AC devices only).

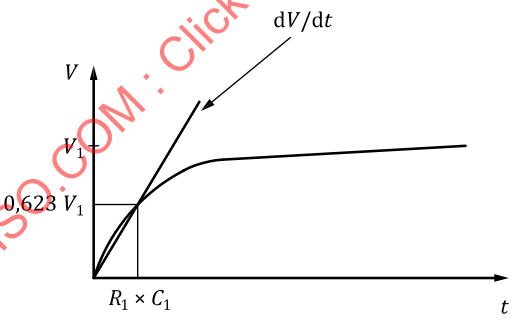
g) Verify with the oscilloscope (or an equivalent instrument) that the device achieves the specified output voltage within the specified time.



Key

1 HPSSPC under test
2 power in
3 power out
4 oscilloscope or equivalent instrument
5 trigger
V_1 voltmeter
S_1 10 A bounceless switch
R_1 $0{,}632 \times \dfrac{V_1}{C_1(\mathrm{d}V/\mathrm{d}t)}$
R_2 1,0 MΩ (5 %), 1/2 W
R_3 50 Ω (5 %)
C_1 0,01 µF (5 %)

Figure 5 — Test circuit for exponential rise in voltage



Key

V voltage
t time, expressed in microseconds
V_1 maximum rated output voltage (AC devices use $V_1 = V_{\text{rated, RMS}} \times \sqrt{2}$)

Figure 6 — Exponential rate of voltage rise

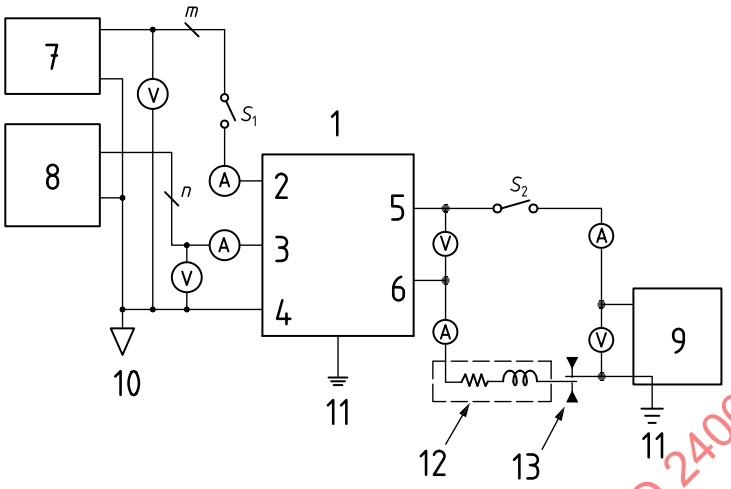
5.17 Arc fault characteristics

5.17.1 Guillotine test

See 4.3.16.1.

Connect the HPSSPC as shown in Figure 7. Apply the rated voltage and turn on the control. Apply the short-circuit with guillotine as shown in Figure 8. Verify that the HPSSPC meets the HPSSPC trip

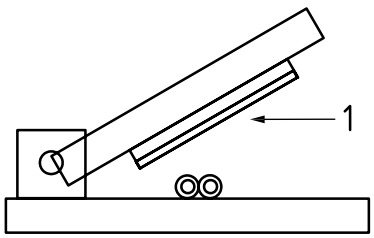
characteristics as specified in the detail requirements without any damage. Verify the current of guillotine and that the HPSSPC does not become trip state for the over current.



Key

1 HPSSPC under test
2 control (discrete signals and/or bus which may input control)
3 state indication(s) [discrete signals and/or bus which may optionally output state indication(s)]
4 signal ground
5 power in
6 power out
7 control function generator
8 state indication power supply
9 supply voltage AC or DC as applicable
10 signal ground
11 power ground
12 current limiting wires
13 guillotine
S_1 bounceless switch
S_2 bounceless switch
m wire count or optionally the number of the buses for control (m = 1, 2, 3, etc.)
n wire count or optionally the number of the buses for state indication(s) (n = 0, 1, 2, etc.)

Figure 7 — Test set up for Guillotine test



Key

1 sharp razor blade with one conductor

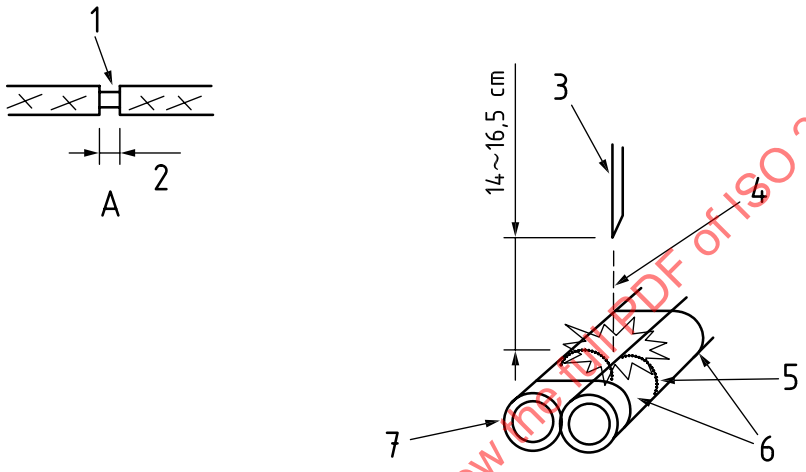
Figure 8 — Guillotine appearance example

5.17.2 Wet arc fault test

See 4.3.16.1.

Prepare an electrolyte solution by dissolving sodium chloride with a mass fraction of 3 % ± 0,5 % in distilled water. As shown in Figure 9, support the pre-damaged wires in free air. Position the delivery system so that the electrolyte contacts the wires from a height of 14 cm to 16,5 cm at a point which shall position the droplets into the gap point. The gap is specified in the detail requirements.

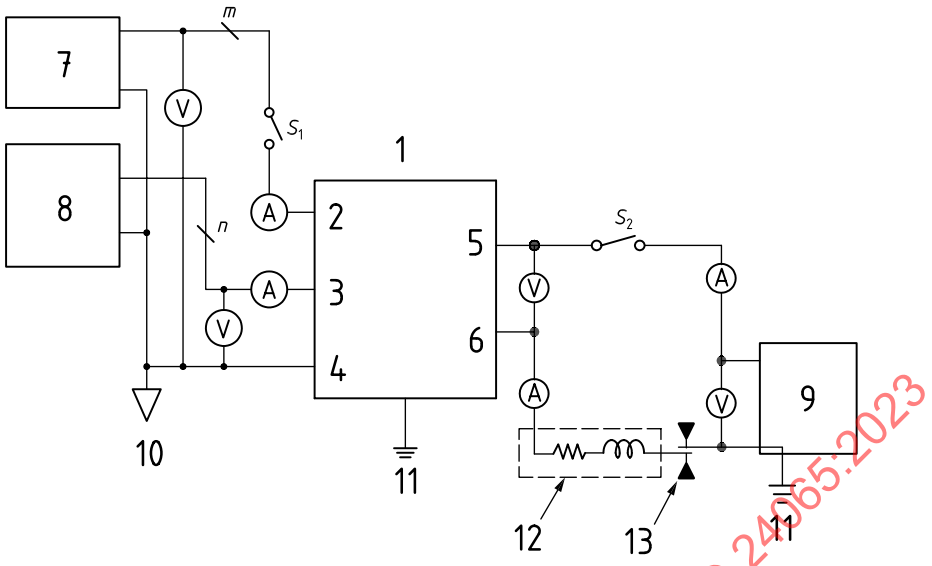
Connect the HPSSPC as shown in Figure 10. Apply the rated voltage and turn on the control. Apply the short-circuit with a continual salt-water drop into the gap between the insulation breaches of damaged wires. Verify that the HPSSPC meets the HPSSPC trip characteristics as specified in the detail requirements without any damage.



Key

1 pre-damaged point
2 gap
3 drop needle
4 water drops (8 to 10 drops per minute of 3 % ± 0,5 % sodium chloride solution)
5 gap between the insulation breaches (see pre-damaged wires detail)
6 tie wrap
7 pre-damaged wires (20 cm to 40 cm)
A pre-damaged wires detail

Figure 9 — Water drops appearance example



Key

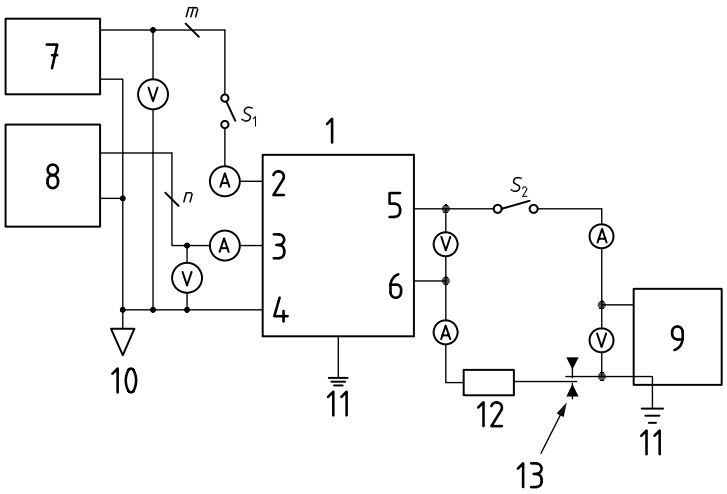
1 HPSSPC under test
2 control (discrete signals and/or bus which may input control)
3 state indication(s) [discrete signals and/or bus which may optionally output state indication(s)]
4 signal ground
5 power in
6 power out
7 control function generator
8 state indication power supply
9 supply voltage AC or DC as applicable
10 signal ground
11 power ground
12 current limiting wires
13 water drops
S_1 bounceless switch
S_2 bounceless switch
m wire count or optionally the number of the buses for control (m = 1, 2, 3, etc.)
n wire count or optionally the number of the buses for state indication(s) (n = 0, 1, 2, etc.)

Figure 10 — Test set up for Wet arc track test

5.17.3 Intermittent connection test

See 4.3.16.2.

Connect the HPSSPC as shown in Figure 11. Apply the rated voltage and turn on the control. Apply the loose connection with gap and vibration specified in the detail requirements as shown in Figure 12. Verify that the HPSSPC meets the HPSSPC trip characteristics as specified in the detail requirements without any damage. To minimize further damage to the test fixture, the test shall not exceed 1 min. Examples of the load include resistive load, inductive load, motor load, capacitive load, light, switching power supply and so on. The load current shall be 80 % of the rated current.



Key

1 HPSSPC under test
2 control (discrete signals and/or bus which may input control)
3 state indication(s) [discrete signals and/or bus which may optionally output state indication(s)]
4 signal ground
5 power in
6 power out
7 control function generator
8 state indication power supply
9 supply voltage AC or DC as applicable
10 signal ground
11 power ground
12 load
13 intermittent connection
S_1 bounceless switch
S_2 bounceless switch
m wire count or optionally the number of the buses for control (m = 1, 2, 3, etc.)
n wire count or optionally the number of the buses for state indication(s) (n = 0, 1, 2, etc.)

Figure 11 — Test set up for intermittent connection test