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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 9: 150-Mbit/s optical physical layer conformance test plan

Véhicules routiers — Système de transport axé sur les médias —

Partie 9: Plan d'essais de conformité de la couche optique physique à 150-Mbit/s

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Foreword

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21806 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The Media Oriented Systems Transport (MOST) communication technology was initially developed at the end of the 1990s in order to support complex audio applications in cars. The MOST Cooperation was founded in 1998 with the goal to develop and enable the technology for the automotive industry. Today, MOST[1)] enables the transport of high quality of service (QoS) audio and video together with packet data and real-time control to support modern automotive multimedia and similar applications. MOST is a function-oriented communication technology to network a variety of multimedia devices comprising one or more MOST nodes.

Figure 1 shows a MOST network example.

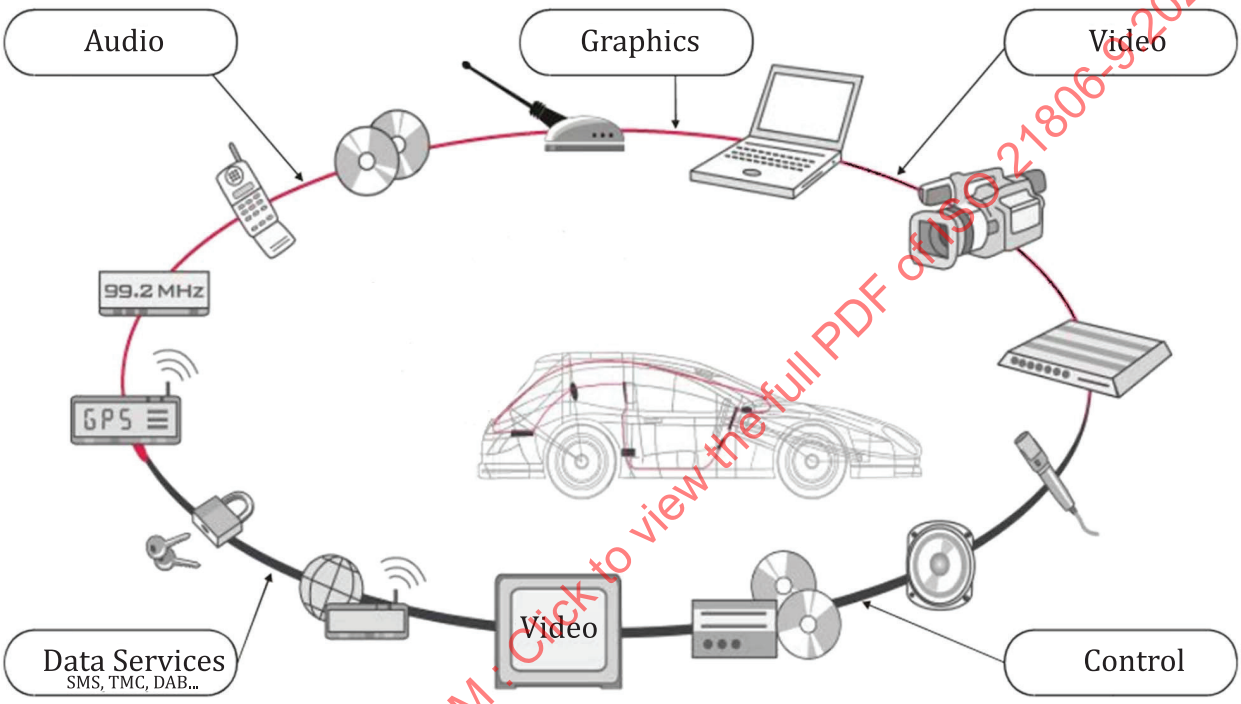

Figure 1 — MOST network example

The MOST communication technology provides

— synchronous and isochronous streaming,

— small overhead for administrative communication control,

— a functional and hierarchical system model,

— API standardization through a function block (FBlock) framework,

— free partitioning of functionality to real devices,

— service discovery and notification, and

— flexibly scalable automotive-ready Ethernet communication according to ISO/IEC/IEEE 8802-3[3].

MOST is a synchronous time-division-multiplexing (TDM) network that transports different data types on separate channels at low latency. MOST supports different bit rates and physical layers. The network clock is provided with a continuous data signal.

1) MOST® is the registered trademark of Microchip Technology Inc. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO.

Within the synchronous base data signal, the content of multiple streaming connections and control data is transported. For streaming data connections, bandwidth is reserved to avoid interruptions, collisions, or delays in the transport of the data stream.

MOST specifies mechanisms for sending anisochronous, packet-based data in addition to control data and streaming data. The transmission of packet-based data is separated from the transmission of control data and streaming data. None of them interfere with each other.

A MOST network consists of devices that are connected to one common control channel and packet channel.

In summary, MOST is a network that has mechanisms to transport the various signals and data streams that occur in multimedia and infotainment systems.

The ISO standards maintenance portal (https://standards.iso.org/iso/) provides references to MOST specifications implemented in today's road vehicles because easy access via hyperlinks to these specifications is necessary. It references documents that are normative or informative for the MOST versions 4V0, 3V1, 3V0, and 2V5.

The ISO 21806 series has been established in order to specify requirements and recommendations for implementing the MOST communication technology into multimedia devices and to provide conformance test plans for implementing related test tools and test procedures.

To achieve this, the ISO 21806 series is based on the open systems interconnection (OSI) basic reference model in accordance with ISO/IEC 7498-1[1] and ISO/IEC 10731[2], which structures communication systems into seven layers as shown in Figure 2. Stream transmission applications use a direct stream data interface (transparent) to the data link layer.

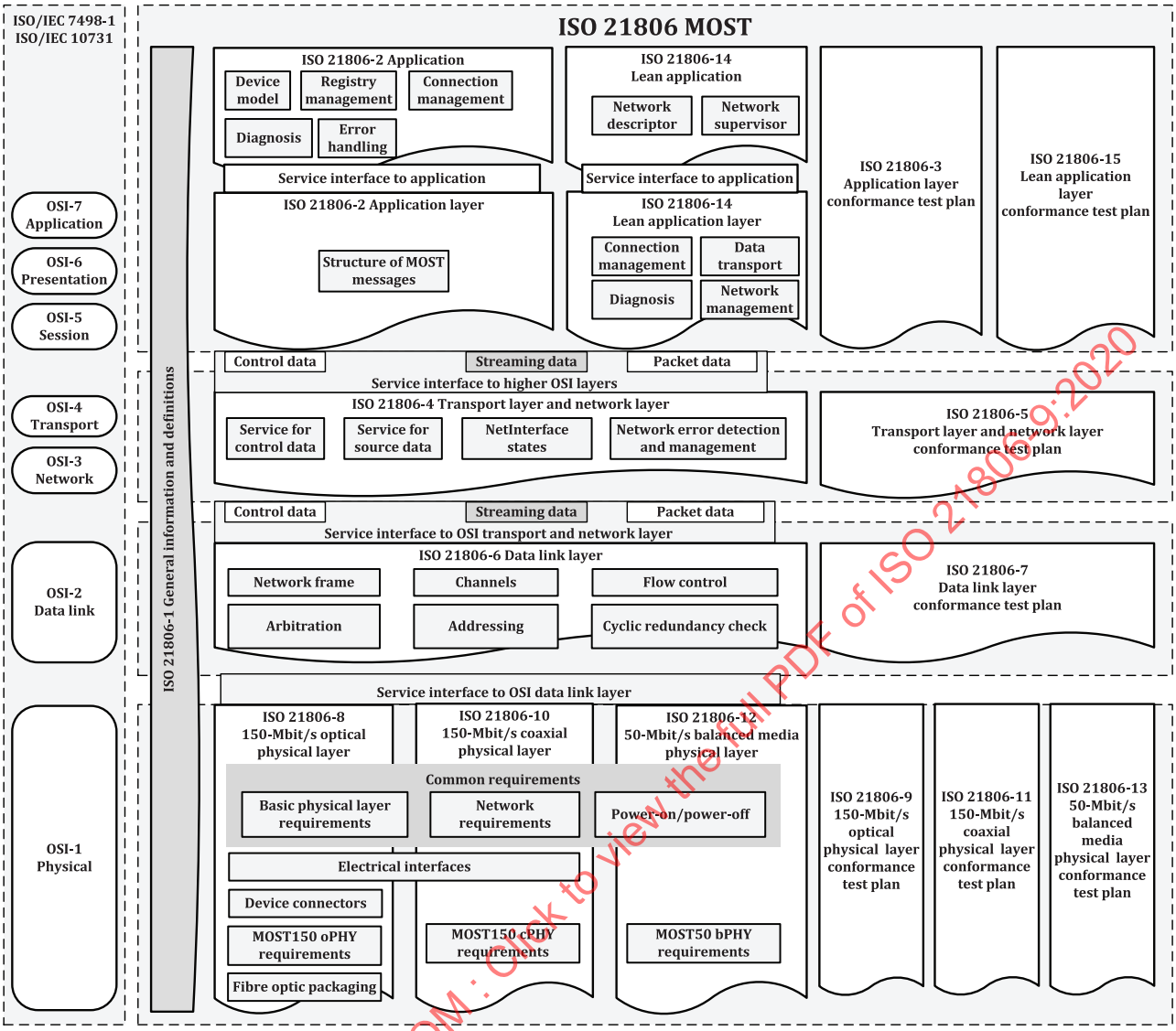

Figure 2 — The ISO 21806 series reference according to the OSI model

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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 9: 150-Mbit/s optical physical layer conformance test plan

1 Scope

This document specifies the conformance test plan for the 150-Mbit/s optical physical layer for MOST (MOST150 oPHY), a synchronous time-division-multiplexing network.

This document specifies the basic conformance test measurement methods, relevant for verifying compatibility of networks, nodes, and MOST components with the requirements specified in ISO 21806-8.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21806-1, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 1: General information and definitions*

ISO 21806-8:2020, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 8: 150-Mbit/s optical physical layer*

IEC 60793-1-40, *Optical fibres — Part 1-40: Measurement methods and test procedures — Attenuation*

IEC 61280-1-3, *Fibre optic communication subsystem test procedures — Part 1-3: General communication subsystems — Central wavelength and spectral width measurement, Method B*

IEC 61280-2-2, *Fibre optic communication subsystem test procedures — Part 2-2: Digital systems — Optical eye pattern, waveform and extinction ratio measurement*

IEC 61300-3-4, *Fibre optic interconnecting devices and passive components — Basic test and measurement procedures — Part 3-4: Examinations and measurements — Attenuation*

JEDEC No. JESD8C.01[2)], *Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits*

TIA/EIA-644-A[3)], *Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21806-1, ISO 21806-8, and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

2) Available at https://www.jedec.org/.

3) Available at https://www.tiaonline.org/standards/.

— IEC Electropedia: available at http://www.electropedia.org/

3.1
intersymbol interference
disturbance due to the overflowing into the signal element representing a wanted digit of signal elements representing preceding or following digits

[SOURCE: IEC Electropedia 702-08-33]

4 Symbols and abbreviated terms

4.1 Symbols

---	empty cell/undefined
t_{OSLE}	time of optical signal level detection end
t_{OSLS}	time of optical signal level detection start
ρ_{Fs}	frame rate
ρ_{BR}	bit rate

4.2 Abbreviated terms

For the purposes of this document, the abbreviated terms given in ISO 21806-1, ISO 21806-8, and the following apply.

AC	alternate current
AJ	alignment jitter
AWG	arbitrary waveform generator
BW	bandwidth
DC	direct current
DCD	duty cycle distortion
DSO	digital sampling oscilloscope
IUT	implementation under test
EMD	equilibrium mode power distribution
EOC	electrical optical converter
FOT	fibre optic transceiver
MNC	MOST network controller
NA	numerical aperture
OEC	optical electrical converter
PG	pattern generator
PHYSTT	physical layer stress test tool

PLL	phase lock loop
POF	plastic optical fibre
RMS	root mean square
SDA	serial data analyser
SMD	surface mount device
SNR	signal-to-noise ratio
SP	Specification Point
THM	through hole mount
TJ	transferred jitter
UI	unit interval
VCM	common mode voltage

5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[2].

6 Operating conditions and measurement tools, requested accuracy

6.1 Operating conditions

Temperature range for MOST components: T_A = −40 °C to +95 °C according to ISO 21806-8:2020, 11.4.

Voltage range for MOST components: V_{CC} = 3,135 V to 3,465 V according to ISO 21806-8:2020, Clause 10.

NOTE There are functional requirements for the EOC within an extended voltage supply range according to ISO 21806-8.

6.2 Apparatus — Measurement tools, requested accuracy

The following list provides state-of-the-art tools.

6.2.1 Oscilloscope

— digital sampling oscilloscope;

— sampling rate ≥10 gigasample/s;

— bandwidth ≥1,5 GHz;

— sampling memory ≥10 megasample;

— active probe (single-ended, differential).

6.2.2 High-speed OEC

— bandwidth ≥250 MHz (DC-coupled) for b_0/b_1 measurement to calculate extinction ratio r_{e2};

— bandwidth ≥750 MHz (DC- or AC-coupled) for all other measurements;

— performance recommendation:

  — response flatness: 1 dB (constant gain over bandwidth; linear transfer function over the optical input range);

  — low DC offset error (see 8.5).

6.2.3 High-speed EOC

— light source with a pulse shape representing a high-bandwidth emitter:

  — transition time t_r and t_f below 1 ns;

  — overshoot greater than 1,25 of normalized amplitude;

  — extinction ratio: 10 dB to 12 dB.

— light source with a pulse shape representing a low-bandwidth emitter:

  — transition time t_r and t_f between 1 ns and 0,5 UI;

  — overshoot: no overshoot;

  — extinction ratio: 10 dB to 12 dB.

6.2.4 Optical power meter

— accuracy: at least ±0,25 dB;

— accuracy optical power meter and SP2 adaptor: at least ±0,5 dB;

— wavelength: 650 nm;

— range: at least -60 dBm to 0 dBm;

— trigger input (for timing measurements).

6.2.5 Ampere meter

— accuracy ≤2 µA;

— trigger input (for timing measurements).

6.2.6 Pattern generator for generating MOST150 oPHY stress pattern

— bandwidth 300 Mbit/s;

— trigger output (for timing measurements).

6.2.7 Optical attenuator

— attenuation up to 40 dB;

— preferably attenuation via grey filter, not via air gap.

6.2.8 Optical Y–coupler.

6.2.9 Optical spectrometer

— resolution ≤1 nm;

— spectral range at least 500 nm to 800 nm.

7 Electrical characteristics

7.1 Test according to LVDS

Testing of MOST devices or MOST components shall be performed according to the measurement methods and set-ups specified in TIA/EIA-644-A. Parameters and their respective limits are also derived from TIA/EIA-644-A, with the exception of common mode voltage (V_{CM}) as specified in ISO 21806-8:2020, 12.1.

7.2 Test according to LVTTL

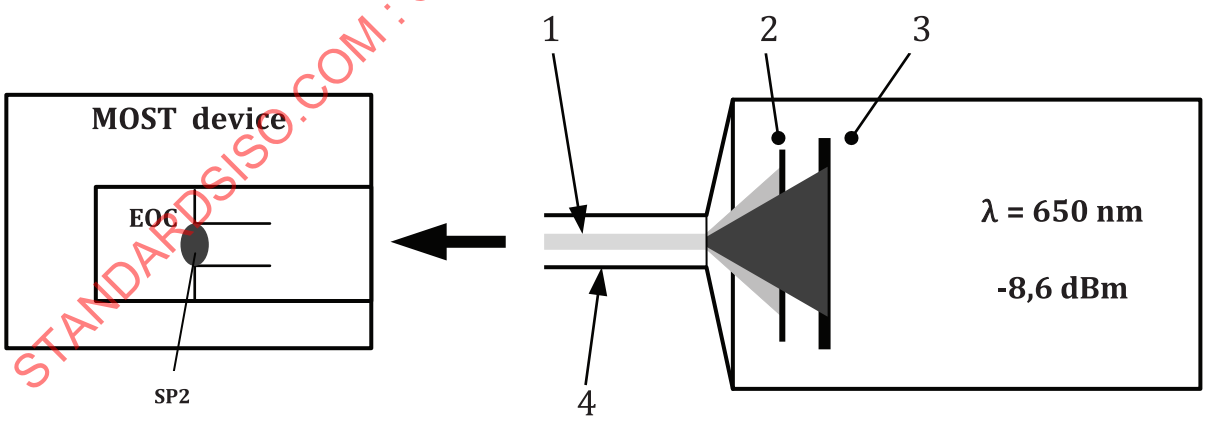
Testing of MOST devices or MOST components shall be performed in accordance with JEDEC No. JESD8C.01.

8 Optical characteristics

8.1 Measurement of optical output power at SP2

Figure 3 shows the schematic of an optical power meter. This measurement adaptor allows the test of parameter P_{opt2} considering the power within a far field angle of 30° (NA = 0,5) and a diameter of 1,0 mm.

The optical power at SP2 is transferred by a glass fibre with a numerical aperture of greater than 0,5, a core diameter of 1 000 µm, and a typical length of 30 mm. An aperture between glass fibre and photo detector confines the transferred beam to the required numerical aperture of 0,5. The size of the aperture depends on the distance between glass fibre and the aperture (see Figure 4). The end face of the glass fibre shall be polished to avoid scattering and a conversion of the beam waist from SP2 to the end of the glass fibre. The glass fibre is mounted into a ferrule, which can be inserted into an SP2-contact of a MOST device for measuring the optical power at SP2 (MOST compatible ferrule, i.e. derived from connector drawing).

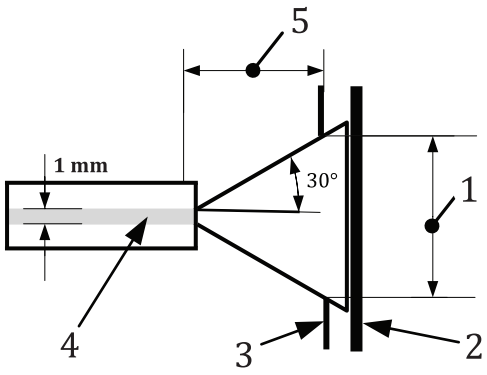


Key

1 glass fibre, D = 1 mm, NA ≥ 0,5
2 NA = 0,5
3 large area photo detector
4 MOST compatible ferrule

Figure 3 — Schematic of optical power meter

Figure 4 shows the calculation of aperture size d_B.



Key

1 aperture size d_B: see Formula (1)
2 photo detector
3 aperture
4 glass fibre
5 distance X between the glass fibre and the aperture

Figure 4 — Calculation of aperture size d_B

IMPORTANT — It should be ensured that the size of the photo detector is large enough to receive all the light after the aperture.

$$d_B = c + 2 \times X \times \tan(30°) \quad (1)$$

where

d_B is the aperture size;

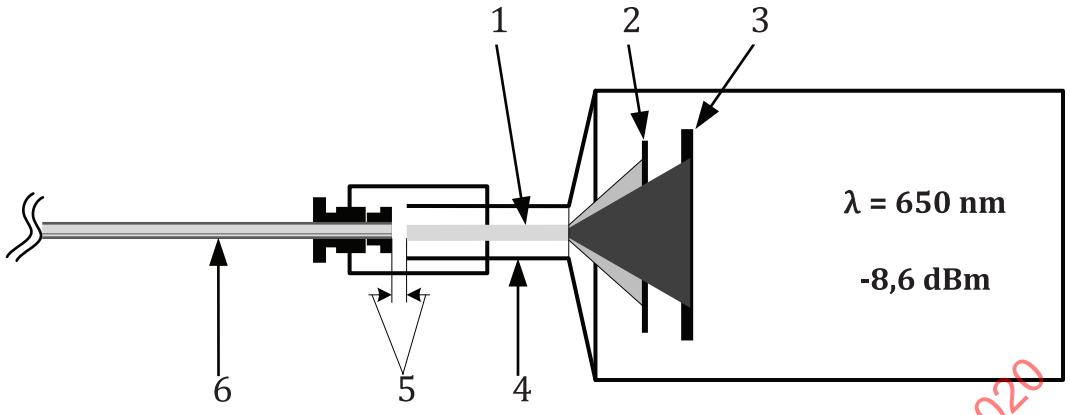
X is the distance between the glass fibre and the aperture;

c is the diameter: 1 mm.

8.2 Measurement of optical input power at SP3

The optical power measurement set-up is given in Figure 5. This measurement allows the testing of the parameter P_{opt3} considering the power within a far field angle of 30° (NA = 0,5) and a diameter of 1,0 mm.

Figure 5 shows the optical power measurement set-up for SP3.



Key

1 glass fibre, D = 1 mm, NA ≥ 0,5
2 NA = 0,5
3 large area photo detector
4 MOST ferrule
5 50 µm to 100 µm; see connector interfaces in ISO 21806-8
6 1 mm POF cable harness

Figure 5 — Optical power measurement set-up for SP3

A glass fibre and an aperture transfer the measured optical power-on a large area photo detector. For description and the calculation base for the aperture see 8.1.

In ISO 21806-8, P_{opt3} is the value of the optical power, when the incoming signal passes the receiving contact end face.

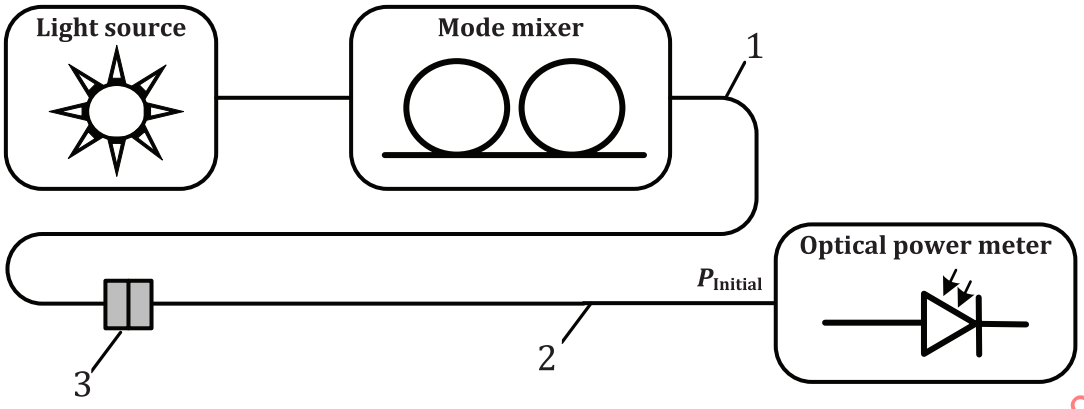
Compared to the glass fibre used in the measurement set-up, the surface quality of a real SP3 contact might be worse. This might result in a lower input power than shown by the measurement. This small mismatch is covered by the specified connection loss. The axial offset shown in Figure 5 considers a requirement defined in the connector interface drawings (see ISO 21806-8).

8.3 Measurement of pigtail fibre attenuation

8.3.1 General

Attenuation of a pigtail fibre is measured using the insertion method, which shall be in accordance with IEC 61300-3-4. The measurement set-up consists of a light source, a mode mixer, which shall be in accordance with IEC 60793-1-40, and a launching fibre for generating the stimulus signal. For detection of optical power, a power meter is used. The connection between IUT and power meter is realized with a secondary launching fibre or an equivalent arrangement.

The measurement is performed in two steps. The first step consists of the measurement of the initial power level $P_{Initial}$ (see Figure 6) while the second step provides the measurement of the power level with the connected pigtail fibre P_{IUT} (see Figure 7). Figure 6 shows the measurement of $P_{Initial}$.

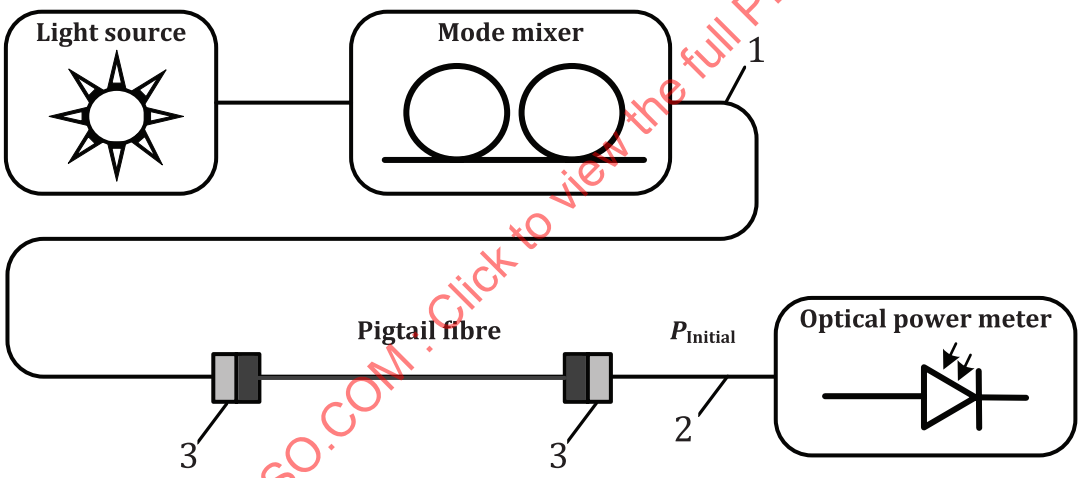


Key

1 launching fibre #1
2 launching fibre #2
3 connector

Figure 6 — Measurement of $P_{Initial}$

Figure 7 shows the measurement of P_{IUT}.



Key

1 launching fibre #1
2 launching fibre #2
3 connector

Figure 7 — Measurement of P_{IUT}

The optical power is measured in logarithmic scale (dBm). The attenuation of a pigtail fibre [see Formula (2)] is measured using the insertion method between $P_{Initial}$ and P_{IUT} expressed in (dB).

$$A_{\text{PigTail}} = P_{\text{IUT}} - P_{\text{Initial}} \quad (2)$$

where

A_{PigTail} is the attenuation of the pig tail;

P_{IUT} is the power implementation under test;

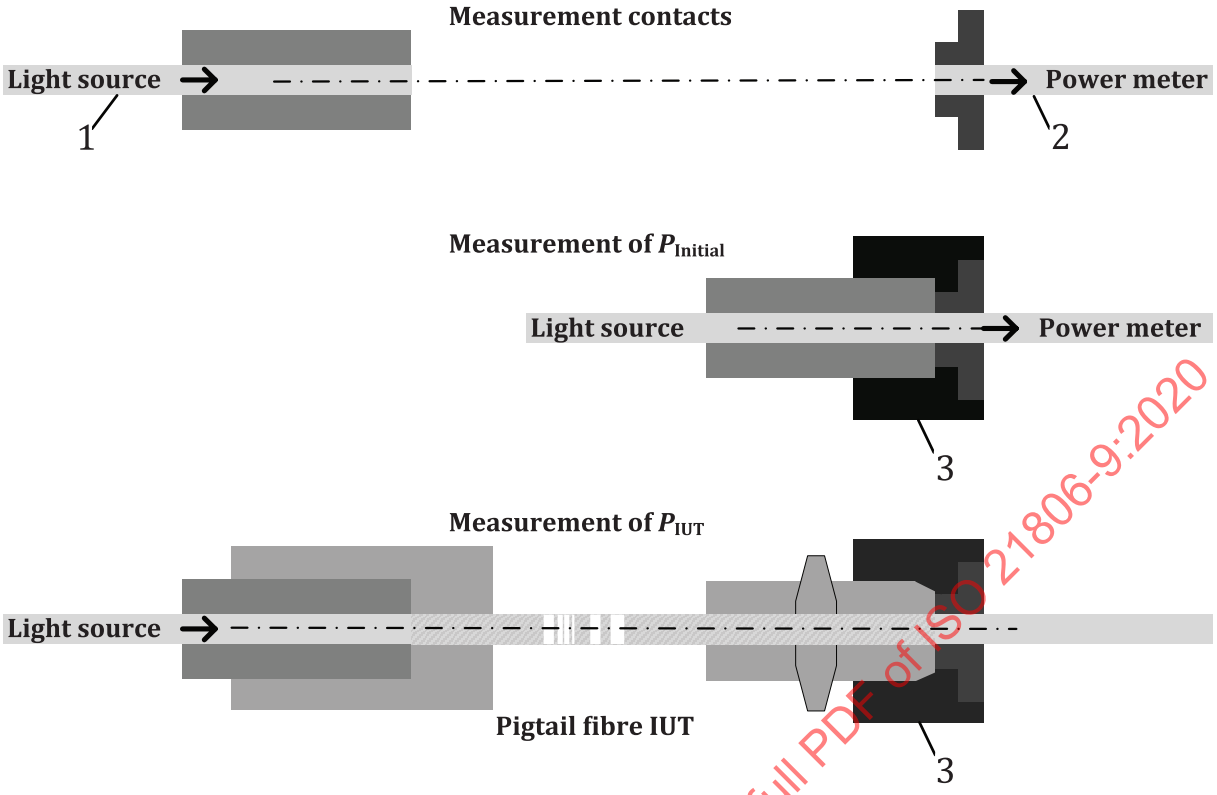
P_{Initial} is the power initial.

8.3.2 Practical considerations

The optical power levels are measured within a diameter of 1 mm and an acceptance angle of 30°. This represents the coupling characteristic of a POF with NA = 0,5, which is typically used in the wire harness. The light source in combination with the mode mixer and the launching fibre #1 creates the equilibrium mode power distribution (EMD). The pigtail fibre is tested using the EMD launch condition. The secondary launching fibre is used for interfacing with the pigtail fibre. It would also eliminate power above NA = 0,5, if it exists. As long as the pigtail fibre does not modify the power distribution, the filter function of set-up the secondary launching fibre is not required. For simplification, the launching fibre #2 can be replaced by an SP2 adaptor or equivalent set-ups.

For testing, optical terminals are created for interfacing with the SP2/SP3 contact geometry on one side and with the ferrules for the SMD transceiver on the other side. The contact shape of the FOT-side ferrules provides different diameters (mechanical coding). Apart from that, the SP2/SP3 contacts have different contact dimensions. According to IEC 61300-3-4 an adaptor may be used (known as “temporary joint”) for coupling of these differently shaped ferrules.

Figure 8 shows the usage of adaptors for matching different contact shapes.

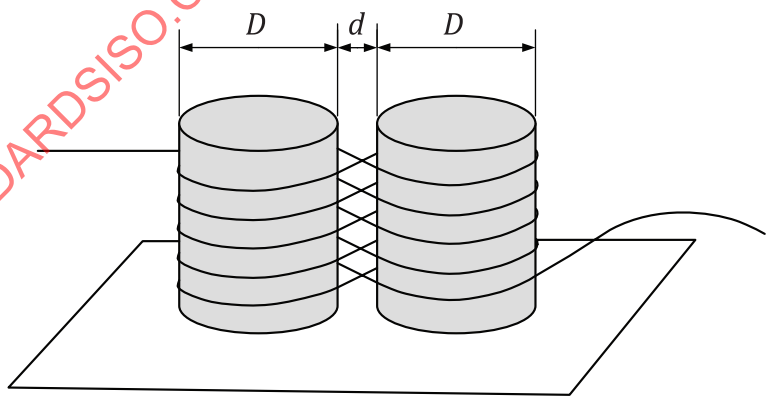


Key

1 launching fibre #1
2 launching fibre #2
3 adaptor “temporary joint”

Figure 8 — Usage of adaptors for matching different contact shapes

Figure 9 shows an example of a mode mixer (D = 42 mm, d = ~4,5 mm, number of turns = 10, length of optical fibre ≤15 m).



Key

d distance
D diameter

Figure 9 — Example of a mode mixer

8.4 Spectral parameters at SP2

Centre wavelength and spectral width

ISO 21806-8 defines the wavelength spectrum of a transmitter with the parameter centre wavelength and spectral width. This is necessary to consider possible spectral asymmetries of state-of-the-art light sources.

The measurement procedure shall be in accordance with IEC 61280-1-3 with the following constraints:

— measurement resolution is ≤1 nm;

— SNR for the measurement equipment is ≥20 dB;

— SNR determines the part, which may be cut from the spectrum; and

— dark calibration.

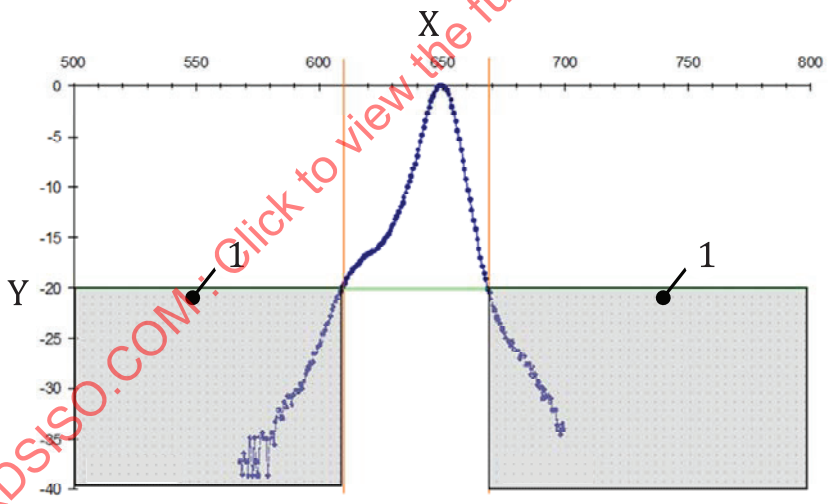
Measurement resolution shall be ≤1 nm:

— SNR for the measurement equipment at least 20 dB;

— SNR determines the part which may be cut from the spectrum;

— dark calibration necessary.

Figure 10 shows an example of how to determine centre wavelength and spectral width.



Key

X wavelength [nm]

Y relative optical power [dB]

1 measured values in grey zone are set to zero

Figure 10 — Example determination of spectral parameters

8.5 b_0/b_1 detection at SP2

To determine b_0/b_1 levels, the pattern generator shall generate the MOST150 oPHY stress pattern. At least 500 pulses (5 UI or 6 UI) shall be extracted out of the measured data. Extraction can be done by triggering on pulse-width ranges or by software-based selection on a prior acquired waveform. b_1 is the statistical mean of all amplitude samples lying in the slice between t_{OSLS} and t_{OSLE} for all acquired high pulses. b_0 is the statistical mean of all amplitude samples lying in the slice between t_{OSLS} and t_{OSLE} for all acquired low pulses. t_{OSLS} and t_{OSLE} are specified in Table 1.

Table 1 — Optical signal level measurement interval

Measurement region	Value	Unit
t_{OSLS}	2,5	UI
t_{OSLE}	4,0	UI

The measured optical amplitudes b_1 and b_0 are an integral part of further measurements at SP2. The accuracy of b_0/b_1 detection determines the accuracy of such a linked measurement. Any variation in a measurement set-up or in the environmental conditions has an impact on b_1 and b_0. Therefore, b_0/b_1 detection should be a part of the linked measurement.

For b_0/b_1 detection, DC-coupled or AC-coupled measurement OECs may be used but there are restrictions given due to the corresponding measurement. Table 2 shows the parameters, which are based on b_0/b_1 and the restriction for the measurement OEC.

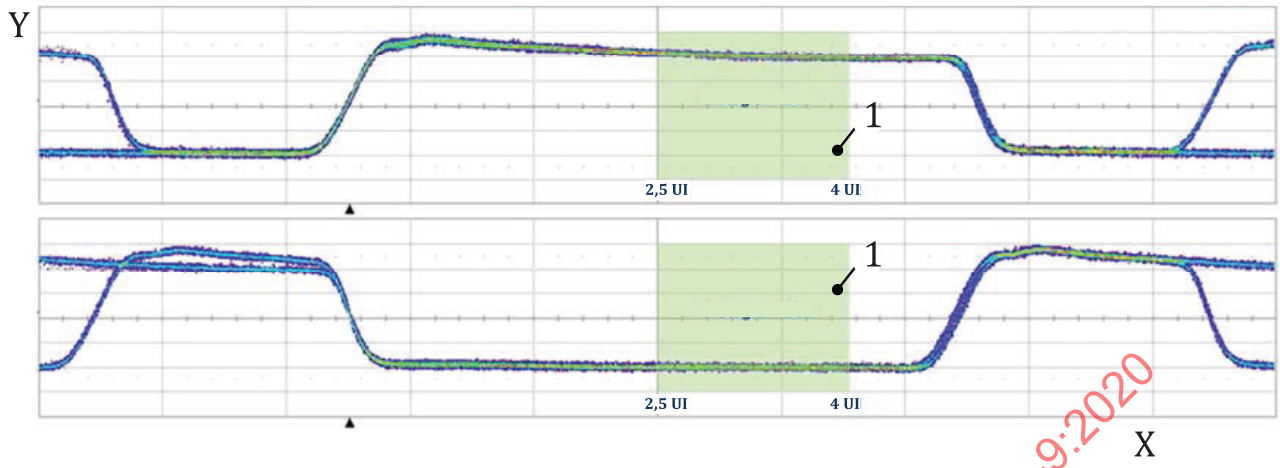
Measurement should compensate the DC offset of a DC-coupled OEC using dark calibration. For accurate measurement results, the signal-to-noise ratio (SNR) shall be in accordance with Annex B.

Table 2 — Restrictions for measurement OECs

Parameter	Symbol	Restriction	Usage of b_0 and b_1
Extinction ratio	r_{e2}	DC-coupled, BW > 250 MHz	Calculation, ratio of b_1 to b_0
Transition times	t_{r2}, t_{f2}	DC-coupled, BW > 750 MHz AC-coupled, BW > 750 MHz	Determination of the 20 % and 80 % amplitudes
Transferred jitter	J_{tr2}	DC-coupled, BW > 750 MHz AC-coupled, BW > 750 MHz	Determination of the trip-point, 50 % amplitude
Alignment jitter	---	DC-coupled, BW > 750 MHz AC-coupled, BW > 750 MHz	Normalization of the amplitude for adjusting the eye mask
Overshoot/ undershoot	---	DC-coupled, BW > 750 MHz AC-coupled, BW > 750 MHz	Normalization of the amplitude for adjusting the masks

In the case of using an AC-coupled measurement OEC for all measurements excluding extinction ratio, a DC-coupled OEC with lower bandwidth-setting such as used for MOST25 oPHY can be reused for determination of extinction ratio. See 6.2 for more detailed OEC requirements.

Figure 11 provides an example of how to measure b_0 and b_1 by a histogram method.



Key

X normalised timeline

Y normalised amplitude

1 histogram box

Oscilloscope measurements: b_{1mean} = 192,37 mV, b_{0mean} = −246,46 mV, ρ_{BR} = 147,455 989 Mbit/s.

Figure 11 — Detection of b_0 and b_1

Measuring optical signals at SP2 using averaging is described in Annex A.

8.6 Extinction ratio at SP2

Extinction ratio r_{e2} is calculated based on the measured optical levels for b_1 and b_0 as described in 8.5 by using a DC-coupled OEC according to Table 2.

The extinction ratio r_{e2} is given with Formulae (3).

$$r_{e2} = 10 \times \log\left(\frac{b_1}{b_0}\right) \tag{3}$$

where

r_{e2} is the extinction ratio;

b_0 is the optical signal level when a logic 0 is transmitted;

b_1 is the optical signal level when a logic 1 is transmitted.

For measuring b_1 and b_0, a DC-coupled OEC according to Table 2 shall be used. The measurement procedure shall be in accordance with IEC 61280-2-2.

8.7 Optical overshoot and undershoot at SP2

8.7.1 General

The optical pulse shape of an SP2 signal is tested with a parameterized mask. The mask parameters are given in normalized amplitude, which is based on the measured optical signal levels b_0 and b_1. Time parameters are specified in units of UI and the origin for the timescale is defined from the midpoint of the rising or falling edge of the signal. Overshoot and undershoot measurements contain only one edge of a pulse class, which forms the trigger edge. Timing variations that might be included in the data stream and be visible on subsequent edges are excluded from this measurement. The timing corridor

given around the trigger point (overshoot H_0, C_0, undershoot G_U, R_U given in this document) serves for tolerating noise coming from the measurement OEC. The test case shall verify that the measured signal does not touch the keep-out areas of the masks.

There are two basic strategies to perform the measurement:

a) Draw a mask that is adjusted in vertical and horizontal scale to the conditions (b_1, b_0, timing resolution) given by a particular measured waveform.

b) Predefine a fixed scheme for horizontal and vertical settings of the mask and normalize the measured waveform.

8.7.2, 8.7.3 and 8.7.4 show an overshoot and undershoot measurement using the basic strategy b). The oscilloscope's display grid is used (ten horizontal divisions and eight vertical divisions) to fix the tolerance scheme.

8.7.2 Overshoot measurement example

Horizontally, 2 UI are displayed. According to the requested timing extremes of −0,63 UI (A_0, F_0) and 1,37 UI (K_0, E_0) given in the mask parameters in this document, the zero point is set to 3,15 divisions. Vertically, the 50 % level of the amplitude swing is centred in the oscilloscope's grid; b_0 is set to −2 divisions (see Figure 12), b_1 is set to +2 divisions, which gives sufficient space for displaying the maximum tolerable overshoot of 40 %. The trigger is set to rising edge for all types of data pulses (2 UI to 6 UI).

The waveform's amplitude is normalised using Formulae (4), (5), and (6).

$$a_{\text{normal}}(i) = \frac{a(i) - v_{\text{offset}}}{v_{\text{scale}}} \tag{4}$$

where

a is the amplitude;

a_{normal} is the normalised amplitude;

i is the index, ranging between 1 and the length of the waveform;

v_{offset} is 50 % level;

v_{scale} is the full swing (b_1 - b_0), which is normalised to 4 divisions on the oscilloscope display.

$$v_{\text{offset}} = \frac{(b_1 + b_0)}{2} \tag{5}$$

where

v_{offset} is 50 % level;

b_0 is the optical signal level when a logic 0 is transmitted;

b_1 is the optical signal level when a logic 1 is transmitted.

$$v_{\text{scale}} = \frac{(b_1 - b_0)}{4} \tag{6}$$

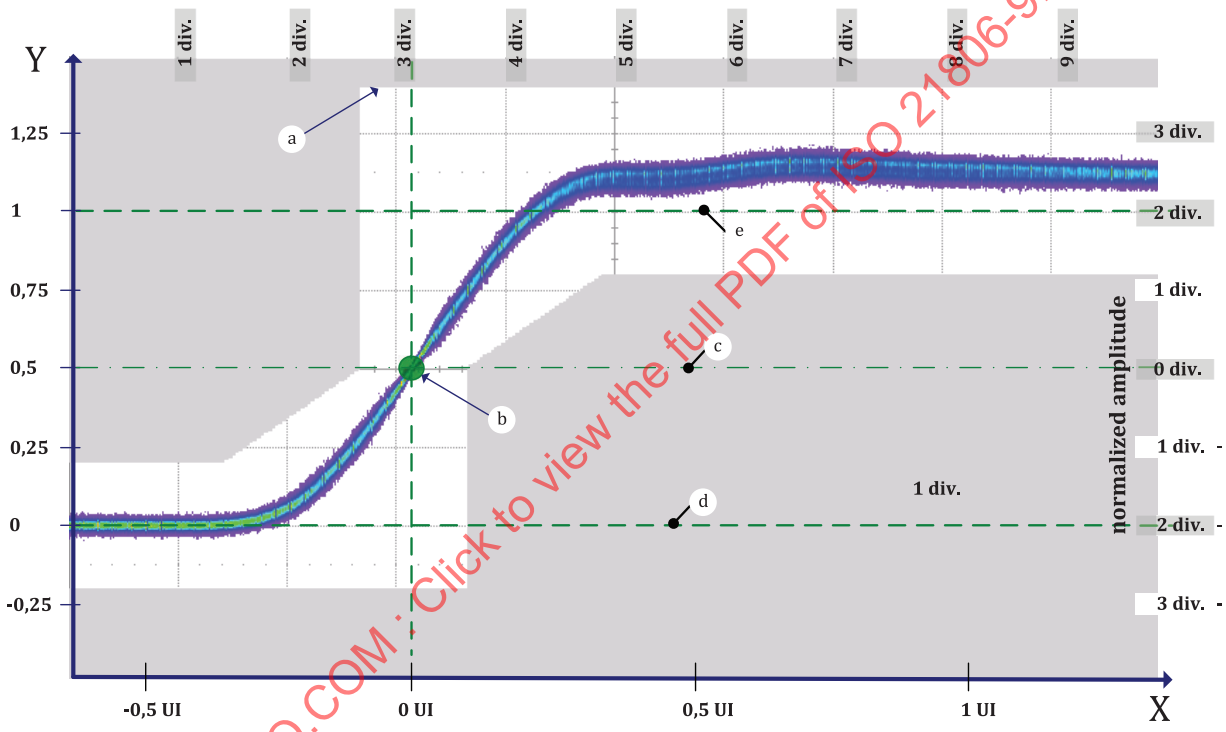
where

v_{scale} is the full swing (b_1 - b_0), which is normalised to 4 divisions on the oscilloscope display;

b_0 is the optical signal level when a logic 0 is transmitted;

b_1 is the optical signal level when a logic 1 is transmitted.

Figure 12 shows an example of an overshoot measurement.



Key

X normalised timeline

Y normalised amplitude

a Overshoot limit 40 %.

b Trigger on rising edge for all data pulses.

c 50 % of amplitude swing: (b_1 + b_0) × 0,5.

d b_0 level.

e b_1 level.

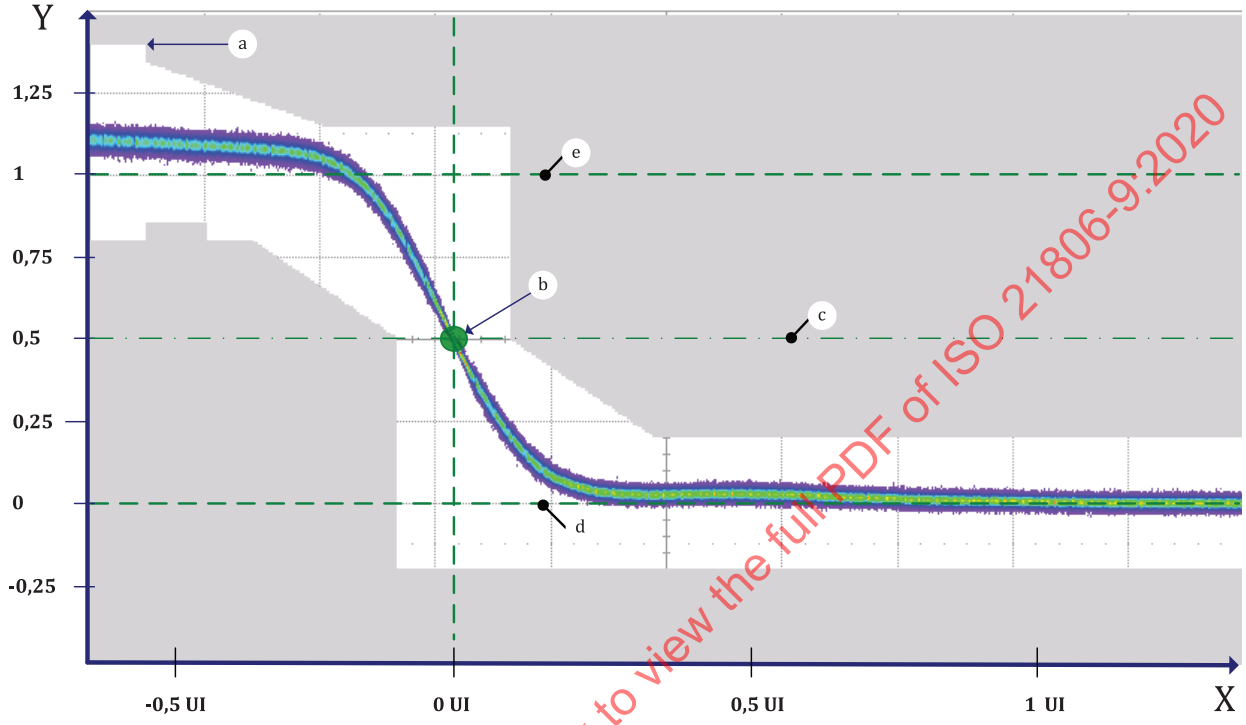
Figure 12 — Example of an overshoot measurement

For undershoot measurement, the oscilloscope shall provide masks for each pulse width (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). Between the overshoot region and the falling edge is a gate (±15 %), which limits the starting point of the transition in amplitude.

8.7.3 Undershoot (2 UI) measurement example

Horizontally, 2 UI are displayed. According to the requested timing extremes of −0,63 UI (A_U, K_U) and 1,37 UI (J_U, T_U) given in the mask parameters, the zero point is set to 3,15 divisions. Vertically, the 50 % level of the amplitude-swing is centred in the oscilloscope's grid; b_0 is set to −2 divisions, b_1 is set to +2 divisions.

Figure 13 shows an example of an undershoot (2 UI) measurement.



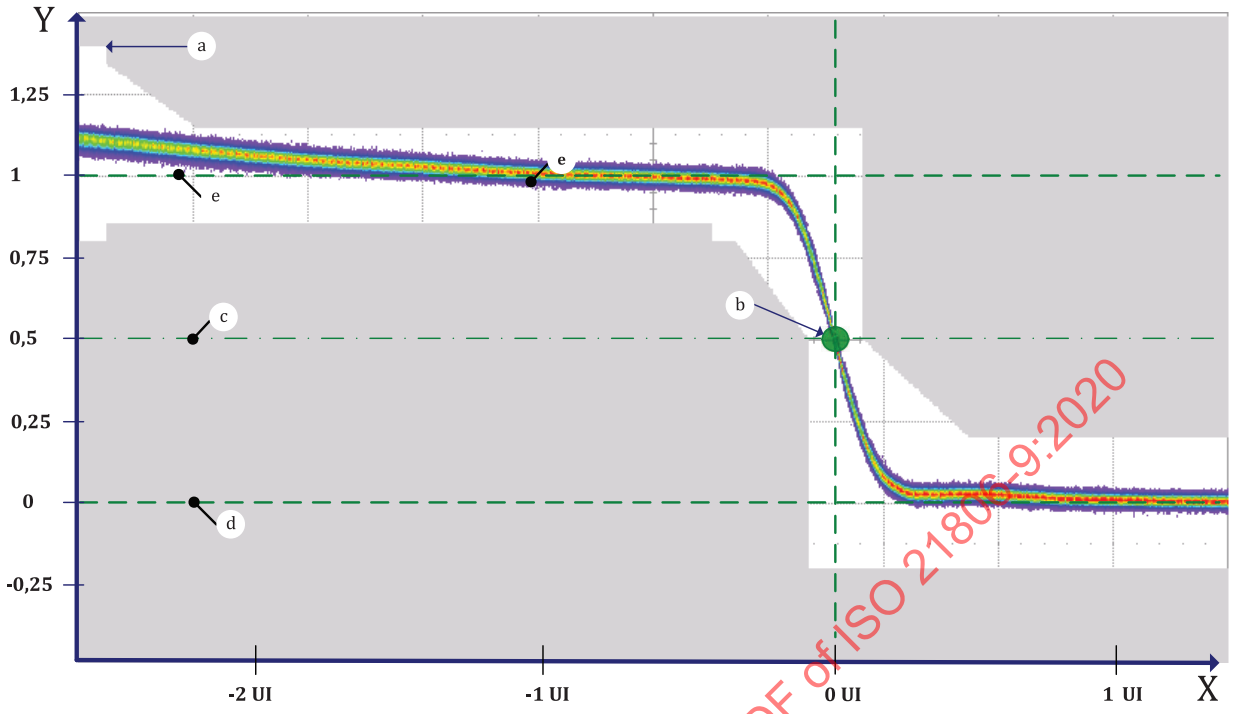
Key

X normalised timeline
Y normalised amplitude
a Overshoot limit 40 %.
b Trigger on falling edge for 2 UI data pulses only.
c 50 % of amplitude swing: $(b_1 + b_0) \times 0,5$.
d b_0 level.
e b_1 level.

Figure 13 — Example of an undershoot (2 UI) measurement

8.7.4 Undershoot (4UI) measurement example

Horizontally, 4 UI are displayed. According to the requested timing extremes of −2,63 UI (A_U, K_U) and 1,37 UI (J_U, T_U) given in the mask parameters, the zero point is set to 6,58 divisions. Figure 14 shows an example of an undershoot (4 UI) measurement.



Key

X normalised timeline
Y normalised amplitude
a Overshoot limit 40 %.
b Trigger on falling edge for 4 UI data pulses only.
c 50 % of amplitude swing: $(b_1 + b_0) \times 0,5$.
d b_0 level.
e b_1 level.

Figure 14 — Example of an undershoot (4UI) measurement

8.8 Transition times at SP2

Measurement shall detect the transition times for falling and rising edges which shall be detected at the time of an edge, when transitioning through the level range of 20 % and 80 % of the optical amplitude (b_1, b_0, see 8.5). Therefore, measurement shall perform the b_0 and b_1 detection beforehand.

Formula (7) and Formula (8) define the amplitude threshold levels.

$$h_{20} = \left[(b_1 - b_0) \times 0,2 \right] + b_0 \tag{7}$$

$$h_{80} = \left[(b_1 - b_0) \times 0,8 \right] + b_0 \tag{8}$$

where

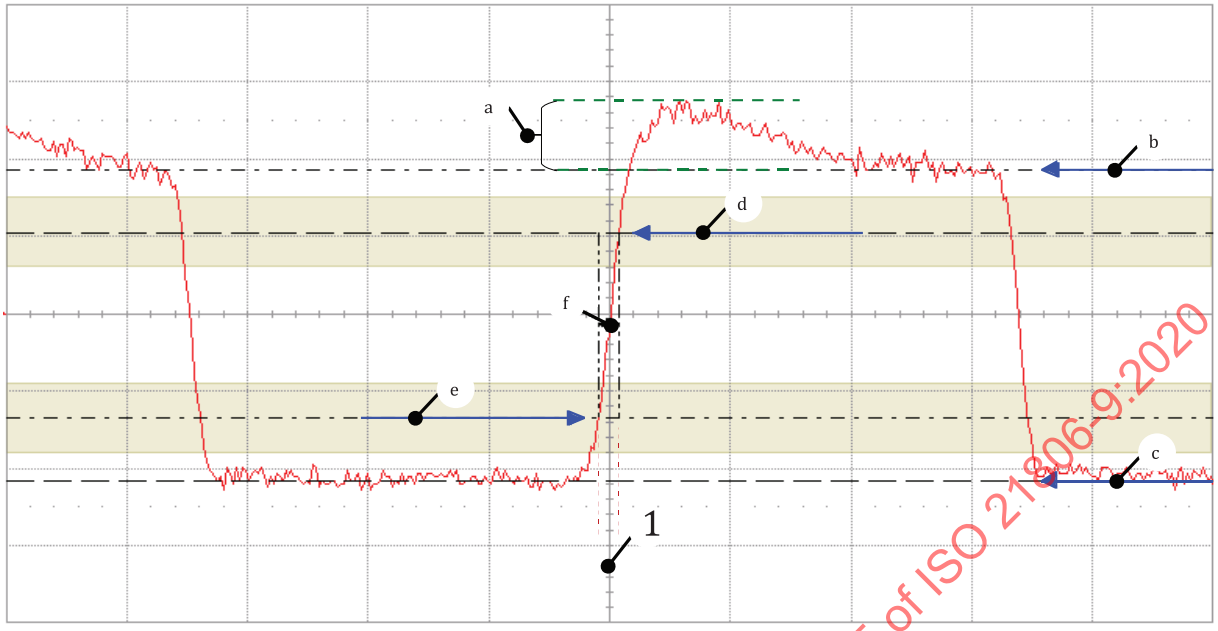
h_{20} is the 20 % threshold of the optical amplitude;

h_{80} is the 80 % threshold of the optical amplitude;

b_0 is the optical signal level when a logic 0 is transmitted;

b_1 is the optical signal level when a logic 1 is transmitted.

Figure 15 shows an example for detection of rise time.



Key

1 t_{rise}
a Overshoot.
b b_1 level.
c b_0 level.
d 80 % threshold.
e 20 % threshold.
f Rise at trigger level.

Figure 15 — Example for detection of rise time

Measured transition times are smaller than the specified limit in ISO 21806-8:2020, 9.3.1. The MOST150 oPHY stress pattern[9] should be used as data signal.

8.9 Stimulus creation for SP3

Measuring jitter at SP4 requires reasonable stimulus signals at SP3. When creating a stimulus signal, all possible impacts coming from various sources shall be considered.

— The SP2 signal can vary within the specified limits:
  — transition times, t_r and t_f can be different;
  — pulse shape, overshoot and undershoot;
  — extinction ratio;
  — alignment jitter, transferred jitter.
— The transport medium POF between SP2 and SP3 may further provide a limitation in bandwidth; for long fibres (up to 15 m) the following impacts are expected:
  — degradation of transition time;
  — intersymbol interference;

— duty cycle distortion, in the case of overshoot and/or duty cycle distortion on the input signal;

NOTE A model is given in ISO 21806-8, which enables approximation of the impact of the bandwidth limitation on the SP2 output signal.

— In the case of short fibres, the bandwidth limitation is negligible, but extreme pulse shapes, within the specified SP2 limits shall be considered.

— A main impact comes with the attenuation due to the transport medium an input power range as specified for an OEC shall be characterized.

These distortions appear in any combination and might have influence on an OEC's jitter performance. The severity of these distortions mainly depends on the way the OEC is designed; some distortions are compensated while other distortions may worsen the jitter performance directly. Even for particular OEC designs, there may be several aspects to be investigated using specific stimuli. Therefore, it is in the responsibility of the FOT supplier to create the worst-case stimuli for their particular OEC design.

9 Measurement of phase variation

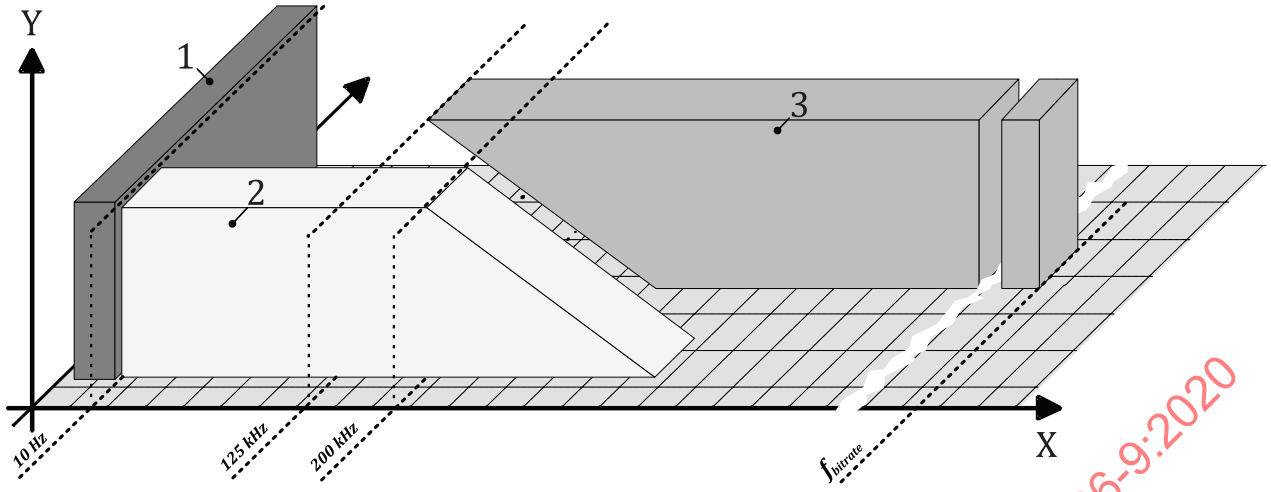
9.1 General

Phase variation is caused by data stream noise and distortion in the time domain. Based on spectral content of the variation, sub-categories of phase variation are defined. Table 3 specifies the measurement of phase variation.

Table 3 — Measurement of phase variation

Phase variation	Spectral limit
Wander	0 Hz to 10 Hz
Transferred jitter (TJ)	Jitter with 10 Hz up the limit given by the jitter filter
Alignment jitter (AJ)	Jitter with spectral content above the limit given by the Golden PLL

Figure 16 shows the sub-categories of phase variation.



Key

X frequency
Y jitter
1 wander
2 transferred jitter
3 alignment jitter

Figure 16 — Sub-categories of phase variation

MOST is a synchronous network; therefore, separating TJ and AJ is necessary. Due to the coding scheme used, a clock signal is embedded in the data stream. The receive unit of a node recovers the clock for sampling the received data stream from the data stream itself. The clock for sampling the output data of this node is derived from the recovered clock, which causes a certain correlation in phase between the receive unit and the output section of a node.

Clock recovery is realized by using a phase locked loop (PLL). The PLL enables the capability of tracking of phase variations. Phase variation in a lower spectral range on an incoming data stream is compensated by aligning the clock's phase accordingly. Therefore, low frequency jitter (below 200 kHz in Figure 16) does not impact the data recovery. The clock for generating the output data, which is derived from the recovered input clock, is affected by the alignment process and may transfer phase variation from input to output.

High frequency jitter (above 125 kHz in Figure 16) cannot be tracked by the PLL and leads to a temporary misalignment between sampling clock and input data, which limits the ability of error-free data recovery. A maximum misalignment (maximum alignment jitter) to be tolerated is defined with the eye masks for each specification point.

ISO 21806-8 provides two definitions for the dynamic characteristics of a PLL for a MOST node:

a) Golden PLL:

The Golden PLL is given in the form of a transfer function representing a low-pass filter. The Golden PLL serves two purposes:

1) It is used as a measurement tool for generating a time base, which is required for forming eye diagrams and determining AJ at each SP along a link. Based on the recovered UI clock an eye diagram is drawn. Eye masks, defined for each SP, give the limits for AJ respectively.

2) It determines the behaviour of an MNC when jitter is applied to its input data. It marks the minimum capability of a PLL to track incoming phase variations. Jitter within the spectral range described by the low-pass filter is tracked by aligning the clock. Jitter beyond the spectral range described by the low-pass filter may lead to misalignment. The Golden PLL in

combination with the eye mask for SP4 receiver tolerance specifies the minimum AJ tolerance of an MNC's receive section.

b) Jitter filter:

The jitter filter is given in the form of a transfer function representing a low-pass filter. It serves two purposes:

1) It is used as a measurement tool for extracting transferred jitter (TJ) out of the total jitter.

2) Additionally, it determines the worst-case jitter transfer characteristic over an MNC. Jitter below the spectral range described by the low-pass filter may be tracked by a PLL. The data stream being generated by this MNC and sampled with the recovered clock may transfer this low-frequency part of the total jitter.

9.2 Measuring alignment jitter

Table 4 specifies a procedure for detecting AJ in a data stream. Oscilloscopes, appropriate for the jitter measurements, are digital sampling oscilloscopes (DSO) with deep sampling memory and special software modules for serial data analysis.

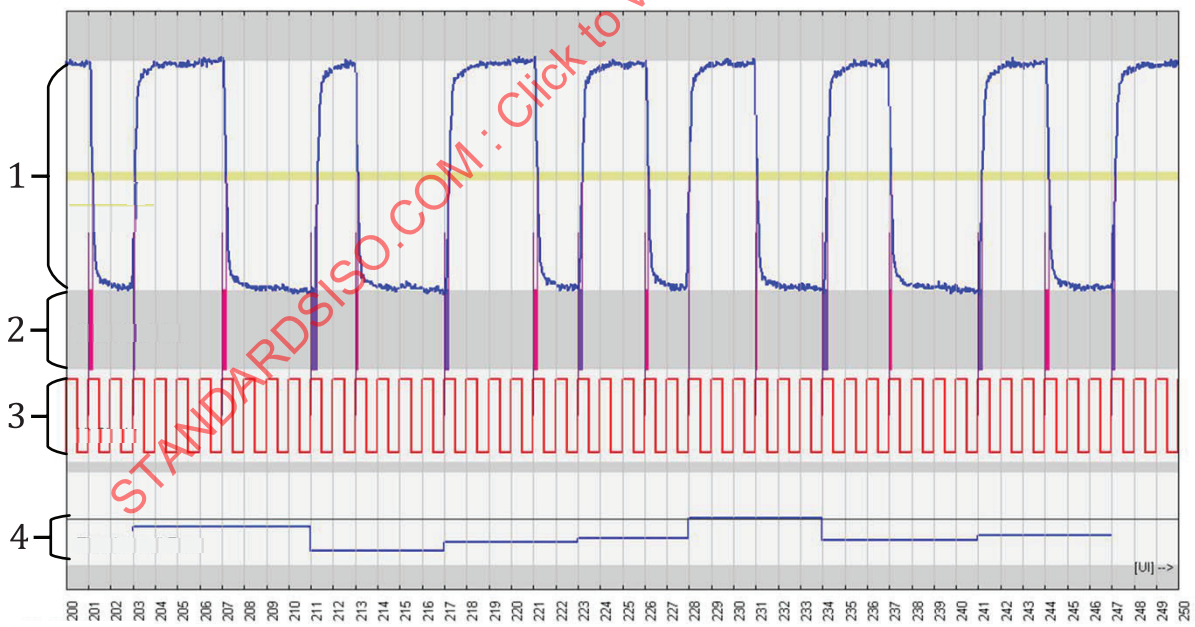
Table 4 — AJ measuring procedure

Action	Description
Acquiring a waveform	A probe (electrical or optical probe according to the SP under test) is connected to the IUT. The vertical scale is adjusted to achieve a sufficient vertical resolution. A sequence of the data stream ("waveform") is sampled into the oscilloscope's memory. For electrical interfaces, SP1 and SP4 masks are given in absolute amplitude. The SP2 mask is given in a relative scheme, which is a normalization of the waveform or an adaption of the mask to the particular amplitude (see 8.5 and 8.7).
Clock recovery	The DCA-coded MOST150 data stream contains clock and data. In a first step, the oscilloscope shall extract the clock. Data pulses range from 2 UI to 6 UI yielding five different pulse widths (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). The required clock has a cycle time of 1 UI, which is twice the bit rate (i.e. for an ρ_{Fs} of 48 kHz, the bit rate is 147,45 Mbit/s, the UI clock is 294,91 MHz). A method of extracting the UI clock from a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. MOST150 specifies that the Golden PLL is applied on positive edges of the data stream only; the approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only.
Applying low-pass filter given by Golden PLL	Once a first derivate of the UI clock is approximated, there might still be phase differences between rising data edges and the recovered UI clock, called time interval errors. Applying the low-pass filter (given by the Golden PLL) to the sequence of consecutive time interval errors results in a filtered phase deviation sequence. This sequence represents the minimum capability of the MNC to track incoming phase variations by adjusting the phase of its sampling clock. In order to recover this sampling clock, phases of the first derivate of the UI clock shall be compensated by the sequence of filtered phase deviations. The resulting new UI clock, which is used for further calculations, now represents the base UI clock incorporated in the data stream, overlaid with a modulation in phase that follows phase variations in the data stream. However, modulation capability is limited in spectrum given by the Golden PLL.
Calculating alignment jitter	Alignment jitter is the phase deviation between any edge of the waveform and the correlating transition of the recovered UI clock. Calculating the misalignment between clock and data for each data transition and drawing the successive phase deviations over runtime in a graph result in an "AJ track", which is the base for further evaluations. Calculating a frequency distribution out of the phase deviation results in an "AJ jitter histogram".

Table 4 *(continued)*

Action	Description
Drawing the eye diagram	For drawing the eye diagram, the waveform is sliced into intervals of 1 UI length aligned with the UI clock. The sliced waveform segments plus some overhead (i.e. 0,25 UI on both sides) are overlaid in one graph. As shown in Figure 17, each transition is drawn twice, first on the left side and second on the right side of the diagram. Therefore, the statistical distribution of transitions at the threshold level is identical on both sides of the eye diagram. Duty cycle distortion (DCD), if it exists, shifts the eye towards the mask. In the shown example, logic 0 pulses are shorter than logic 1 pulses. The UI clock is referenced to rising edges, which causes the rising edges to be adjusted to the UI borders, while the falling edges are shifted by the amount of the DCD.
Pass/fail test using eye masks	Signal integrity shall be checked using eye masks. The masks are defined as keep-out areas; each violation is interpreted as a bit error. The masks are defined by hexagons with points A, B, C, D, E and F. Points A and D are limiting AJ while B, C, E, and F build constraints for amplitude and pulse shape.
Bit error rate	The requested BER of 10^{-9} is represented by eye diagram showing at least 10^{9} bits without violation of the mask. 1 bit is represented in 2 UI. Therefore, at least 2×10^{9} samples are required. Alternatively, statistical methods for accelerated testing of BER are acceptable. Selection of a method for extrapolation and definition of the required database to be measured for extrapolation is in the responsibility of the user.

Figure 17 shows the example 1 of measuring alignment jitter. The UI clock is fitted in frequency and phase to the waveform. Remaining phase deviations are marked in the diagram. Phase deviations for rising edges are shown in the time interval error graph.



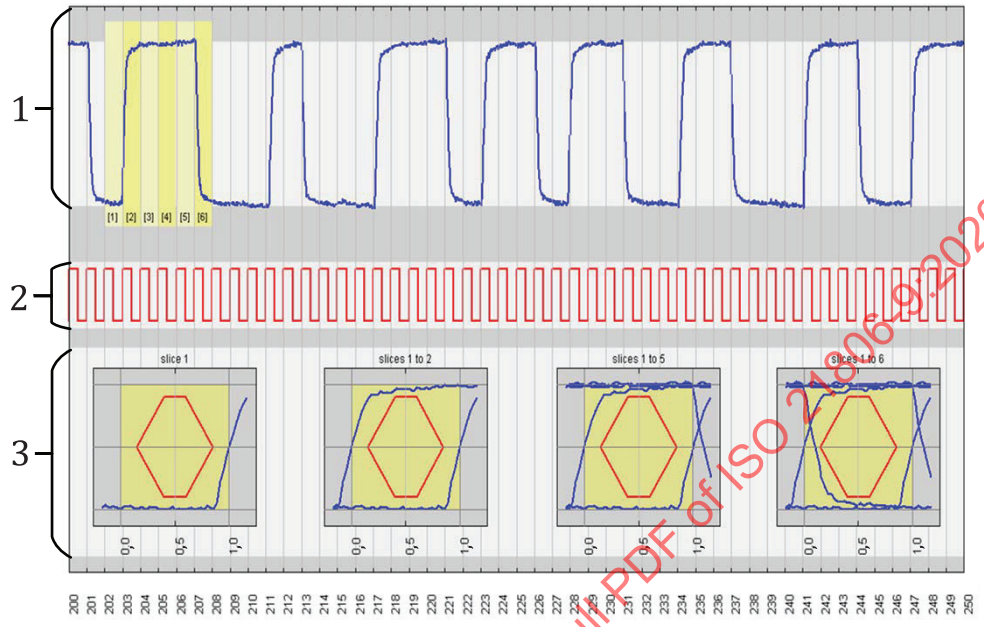
Key

1 waveform input signal
2 phase deviation
3 UI clock
4 time interval error

Figure 17 — Example 1 of measuring alignment jitter

NOTE In many oscilloscopes, visualization of the recovered UI clock is not possible.

Figure 18 shows the example 2 of measuring alignment jitter. The sliced waveform segments are marked in the waveform graph. The segments are overlaid in eye diagrams.



Key

1 waveform input signal
2 UI clock
3 eye diagrams

Figure 18 — Example 2 of measuring alignment jitter

9.3 Measuring transferred jitter

Table 5 specifies a procedure of determining TJ in a measured data stream. The following description provides a rough overview and highlights some MOST specific features.

Table 5 — Measuring transferred jitter

Action	Description
Acquiring a waveform	For this measurement, the maximum available sampling memory of the oscilloscope shall be used. A probe (electrical or optical probe according to the SP under test) is connected to the IUT interface. The vertical scale is adjusted to achieve a sufficient vertical resolution; refer to b_0/b_1 detection (see 8.5) and scaling channel mask (see 8.7). A sequence of the data stream, which is referred to as waveform, is sampled into the oscilloscope's memory. TJ is defined in the spectrum from 10 Hz (beyond wander) to 200 kHz. The determination of this jitter is limited by the size of memory of the oscilloscope.

Table 5 *(continued)*

Action	Description
Clock recovery	Similar to the AJ measurement procedure, the clock separation is provided by an oscilloscope internal function. The oscilloscope shall approximate the clock's phase based on the rising edges of the signals. Similar to the AJ measurement procedure, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. In contrast to the AJ measurement procedure, a PLL functionality for tracking phase variations is basically not necessary. Small deviations in the detected bit-rate might grow to a significant phase mismatch over the length of the acquired waveform and, therefore, affect further results. To enable a robust measurement procedure, it is tolerable to apply a PLL with lowest possible bandwidth (as close as possible to 10 Hz).
Extracting transferred jitter	Jitter is the phase deviation between an edge of the waveform and the correlating transition of the recovered UI clock. For transferred jitter, only phase variations coming with rising edges of the waveform are relevant, because only these deviations are tracked by the PLL and impact the recovered clock's phase. Calculating the misalignment between clock and data for rising edges and drawing the successive phase deviations over runtime in a graph result in a "jitter track". Successive phase deviations appear in pulse time intervals (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI), which correspond to the theoretical maximum jitter frequencies up to 150 MHz. With respect to the focused spectral range 10 Hz to 200 kHz, it is acceptable to reduce the amount of jitter values by skipping samples in regular intervals. The reduction might be helpful for accelerating the measurement process. In the next step, this jitter track (optionally reduced) shall be low-passed, using the transfer function given with the jitter filter definition, which results in the "filtered jitter".
Calculating transferred jitter	Transferred jitter is calculated by accumulating the phase deviations of the filtered jitter by using the root-mean-square method (RMS) as specified in Formula (9). If the spectrum of the filtered jitter contains values below 10 Hz (e.g. caused by a constant phase mismatch between clock and data), the standard deviation as specified in Formula (10) may be calculated instead of the RMS.

$$v_{\mathrm{RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} v_i^{\,2}} \tag{9}$$

where

v_{RMS} is the root mean square method (RMS);

N is the number of samples;

i is the index of summation;

v is the phase deviation.

$$S_{\mathrm{Dev}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} \left(v_i - v_{\mathrm{mean}}\right)^2} \tag{10}$$

where

S_{Dev} standard deviation;

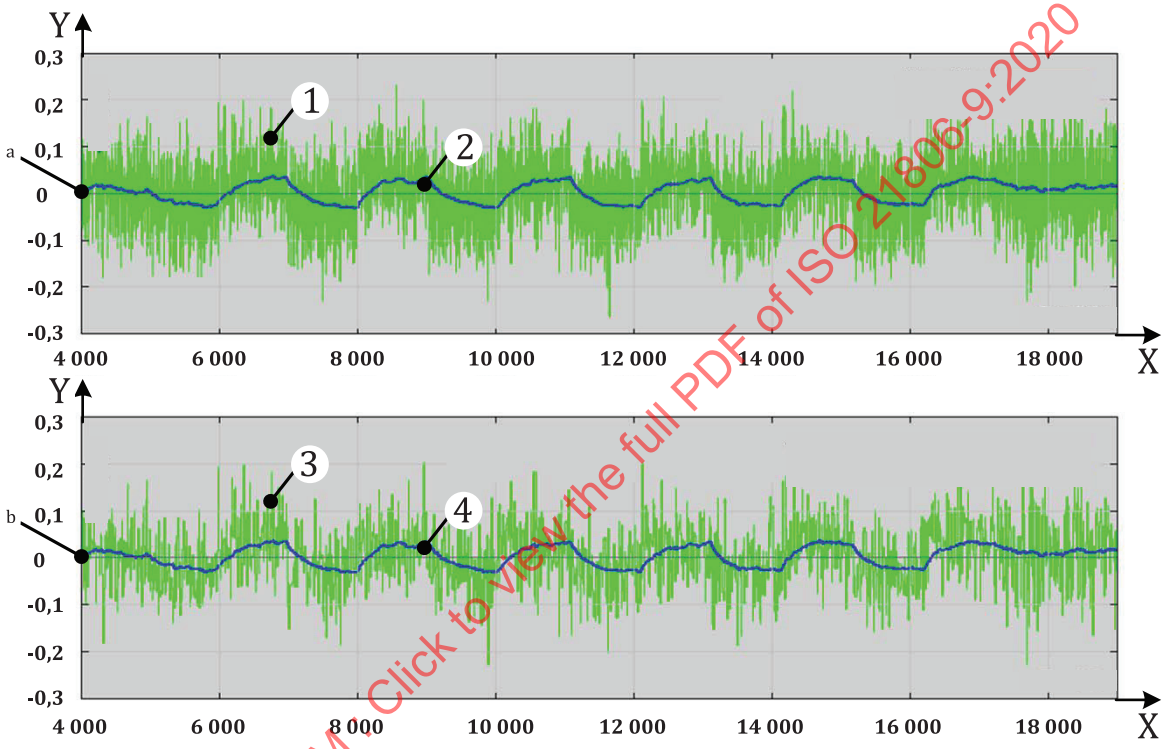
N is the number of samples;

i is the index of summation;

v is the phase deviation;

v_{mean} is the mean (average) phase deviation.

Figure 19 shows the example of measuring transferred jitter.



Key

1 jitter unfiltered (green signal)

2 jitter filtered (blue signal)

3 jitter unfiltered, reduced by 1/10 (green signal)

4 jitter filtered, reduced by 1/10 (blue signal)

X time [UI]

Y jitter [UI]

a Successive phase deviations are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).

b Successive phase deviations but reduced by factor 10 are shown over runtime (jitter unfiltered), weighting with the jitter filter leads to the low-passed version (jitter filtered).

Figure 19 — Example of measuring transferred jitter

9.4 Test set-ups

9.4.1 Relevant eye mask for MOST components

Link quality specifies the minimum alignment jitter performance of MOST components along a single link. Receiver tolerance determines the minimum alignment jitter tolerance of an MNC and

the maximum tolerable alignment jitter that may occur in any place in the network. Therefore, MOST components shall comply with alignment jitter limits given in link quality tables for SP1 to SP4 (see ISO 21806-8).

9.4.2 SP4 Jitter measurement (AJ and TJ)

There are various impacts that determine the characteristic of an input signal at SP3 to be considered for jitter measurements at SP4. Besides the pulse shape and timing distortion of an SP2-output signal, especially the attenuation of that signal along the optical link is relevant. The jitter performance of an OEC under test is checked over the complete sensitivity range (see ISO 21806-8).

The test set-up shall consider, in combination with fibre length, bandwidth limitation of the fibre. Therefore, two set-ups, representing extreme impact of fibre bandwidth, should be used for jitter measurements at SP4: a first set-up for low input power (see Table 6) and a second set-up for high input power (see Table 7) at SP3.

Low input power indicates a link using a long fibre (up to 15 m) with several inline couplers. In addition to the low input power, the impact due to the bandwidth limitations of the POF shall be considered. The set-up uses a light source followed by a mode mixer (according to IEC 60793-1-40). The mode mixer ensures a numerical aperture of a numerical aperture (NA) of 0,5 (EMD condition) independent of the characteristic of the light source. Signal degradation due to bandwidth limitation of the fibre is implemented by using 15 m of POF, which is the maximum specified fibre length.

Figure 20 shows the SP4 Jitter measurement set-up with long optical link.

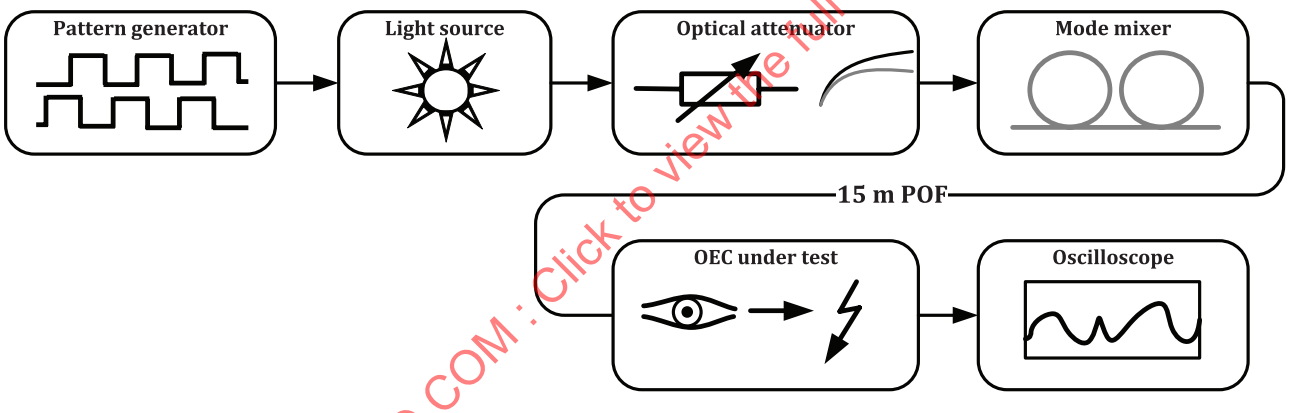


Figure 20 — SP4 Jitter measurement set-up with long optical link

NOTE The bandwidth limitation due to POF given in the MOST specification was calculated for a numerical aperture (NA) of 0,5 in uniform distribution. However, the mode mixer in the shown set-up creates an equilibrium distribution, which results in a lower impact on signal characteristics.

Table 6 specifies the SP4 jitter measurement set-up for low input power at SP3.

Table 6 — SP4 Jitter measurement set-up for low input power at SP3

Item	Content
Input power range	Minimum sensitivity limit (–22 dBm) of the OEC up to at least –20 dBm
Pattern generator	Providing MOST150 oPHY stress pattern Capability for generating dynamic jitter within jitter extremes for SP2 (in combination with the light source, jitter may be generated by the pattern generator or by the light source)
Light source with a pulse shape representing a high-bandwidth emitter	Transition time t_r and t_f below 1 ns Overshoot greater than 1,25 of normalized amplitude Extinction ratio: 10 dB to 12 dB

Table 6 *(continued)*

Item	Content
Light source with a pulse shape representing a low-bandwidth emitter	Transition time t_r and t_f between 1 ns and 0,5 UI No overshoot Extinction ratio: 10 dB to 12 dB
Attenuation tool	Preferably attenuation via grey filter, not via air gap
Mode mixer	According to IEC 60793-1-40
Fibre	15 m POF
OEC under test	Variation of V_{CC}, considering operating temperature range

Figure 21 shows the SP4 Jitter measurement set-up with short optical link.

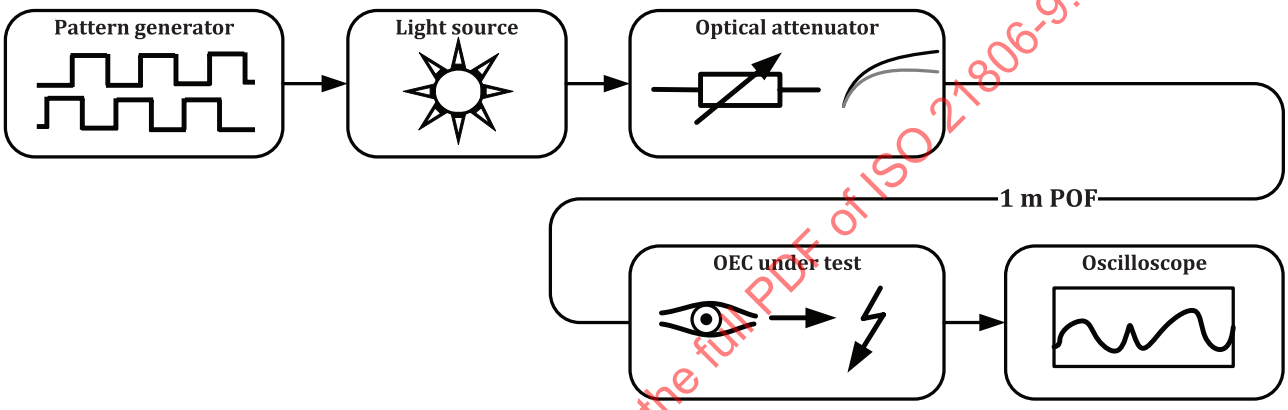


Figure 21 — SP4 Jitter measurement set-up with short optical link

High input power indicates a link using a short fibre without inline couplers. The impact due to bandwidth limitations of POF is negligible.

Table 7 specifies the SP4 jitter measurement, set-up for high input power at SP3.

Table 7 — SP4 jitter measurement, set-up for high input power at SP3

Item	Content
Input power range	Maximum sensitivity limit (−2 dBm) of the OEC down to less than −6 dBm
Pattern generator	Providing MOST150 oPHY stress pattern Capability for generating dynamic jitter within jitter extremes for SP2 (in combination with the light source, jitter may be generated by the pattern generator or by the light source)
Light source with a pulse shape representing a high-bandwidth emitter	Transition time t_r and t_f below 1 ns Overshoot greater than 1,25 of normalized amplitude Extinction ratio: 10 dB to 12 dB
Attenuation tool	Preferably attenuation via grey filter, not via air gap
Fibre	1 m POF
OEC under test	Variation of V_{CC}, considering operating temperature range

The set-up uses a light source, which shall provide fast transition times and overshoot, followed by a short piece of fibre.

9.4.3 SP2 jitter measurement (AJ and TJ)

Figure 22 shows the SP2 jitter measurement set-up.

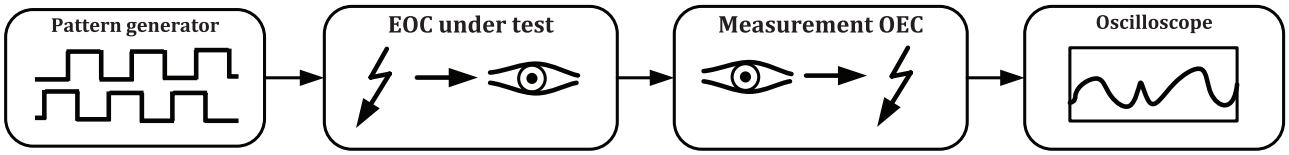


Figure 22 — SP2 jitter measurement set-up

Table 8 defines the SP2 jitter measurement.

Table 8 — SP2 jitter measurement

SP2 Jitter measurement	Description
Pattern generator	The pattern generator provides the MOST150 oPHY stress pattern and the capability for generating dynamic jitter within jitter extremes for SP1 according to ISO 21806-8.
EOC under test	Variation of V_{CC}, considering operating temperature range
Measurement OEC	Bandwidth according to 6.2, high-speed OEC

9.5 Crosstalk

9.5.1 General

In serial digital communication systems, electromagnetic and/or optical crosstalk can cause a reduction in receiver sensitivity. This subclause outlines a way to determine and quantify the crosstalk-induced penalty with measurement equipment used for MOST optical physical layer measurements. The crosstalk measurement is based on the set-up for the receiver's jitter performance vs. optical input power. Crosstalk is expected to be generated by the transmitter, which is placed close to the receiver. The test shall be used for SMD transceivers as well as for connector assemblies combining THM transmitters and THM receivers into transceiver components. The crosstalk penalty is determined by comparison of the jitter performance of the receiver with the transmit section of the transceiver (Tx) on vs. off.

9.5.2 Measurement set-up

Figure 23 shows the crosstalk measurement set-up.

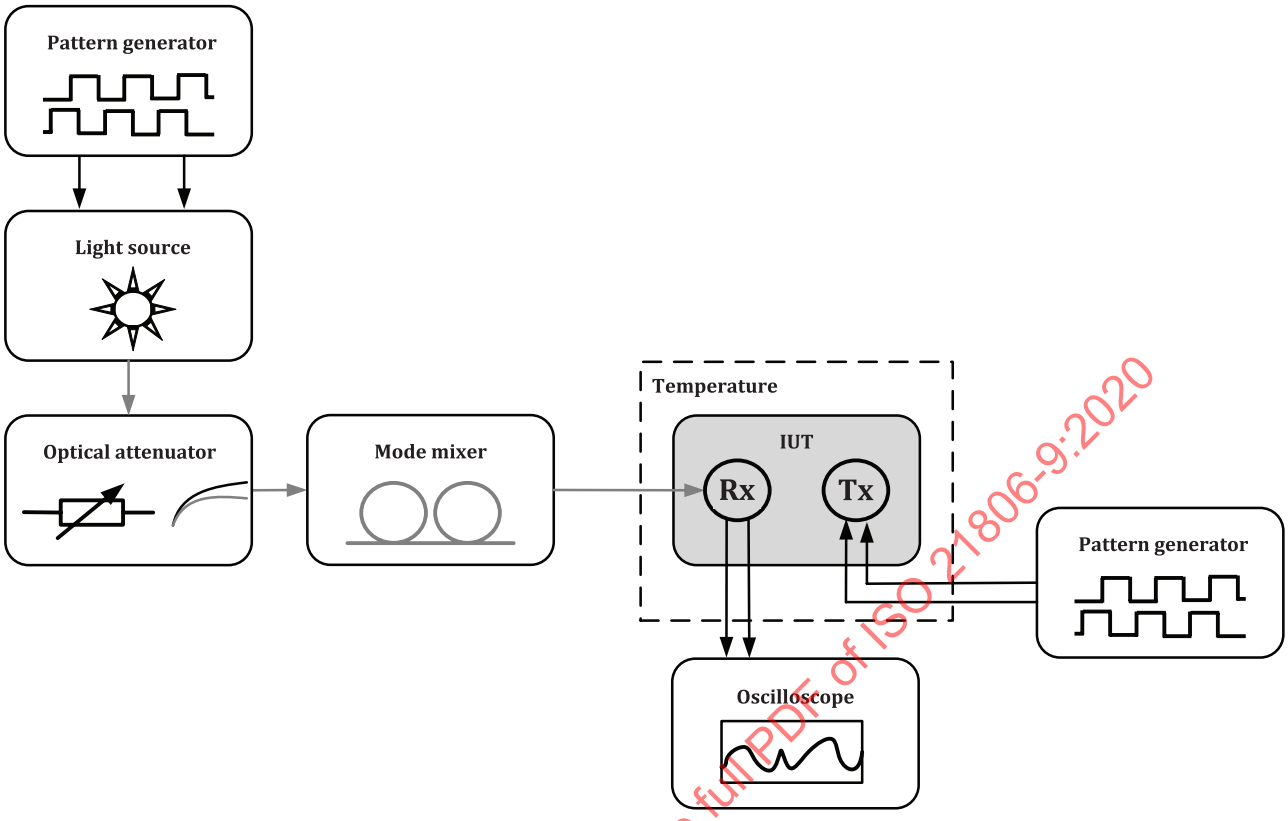


Figure 23 — Crosstalk measurement set-up

There is no crosstalk immunity limit specified in ISO 21806-8. This is considered when specifying AJ and TJ.

9.5.3 Procedure

The following procedure shows a method for quantifying the crosstalk penalty, if it exists:

— Two pattern sources are required. Both sources deliver square-wave signals (equivalent 2 UI) with slightly different frequency for creating uncorrelated phase relationship between both signals. The difference in frequency shifts the phase of the Tx pattern relative to the phase of the receiver pattern. A potential source of distortion (e.g. an edge of the Tx pattern) hits the receiver in any phase.

— The evaluation is based on detection of random jitter. Due to the single frequency pattern there is no data-dependent jitter expected, other deterministic jitter sources (application related) shall be eliminated for this test. Jitter is shown as an RMS figure or visualized by histograms or eye diagrams.

— The test is performed at the minimum sensitivity level (see Table 6) of the receiver, with variation of V_{CC} and temperature. For simplification, a single scenario creating the worst case is sufficient.

— Jitter measurement is performed first without Tx activity and then with Tx activated. In the case of a visible impact, the input power may be increased to reach the identical jitter level.

10 Power-on and power-off

10.1 General

This subclause defines several possible test set-ups and sequences to exercise as many functional EOC and OEC requirements as possible and also provides guidelines for the interpretation of results.

All test sequences shall be performed for the minimum, typical, and maximum of the operating voltage according to operating conditions specified in 6.1.

All test sequences shall be performed for the minimum, typical, and maximum temperature specifications.

When testing MOST modules, crosstalk effects should be considered. When testing one MOST module, the other MOST modules shall be active.

Some of the parameters specified in ISO 21806-8:2020, Clause 10 can be measured (t_{STATF}, t_{LVDSV4}, etc.), other parameters (t_{ON2}, t_{OFF2}, t_{ON4}, etc.) determine relations between operation states and do not have distinct boundaries. For the parameters that cannot be measured, this clause specifies test sequences including a timeout, which represents the maximum and minimum time interval allowed for the respective parameter. A triangle is used to mark the end of this in the signal charts (see Figure 25) as action point. It defines the time for a state validity evaluation.

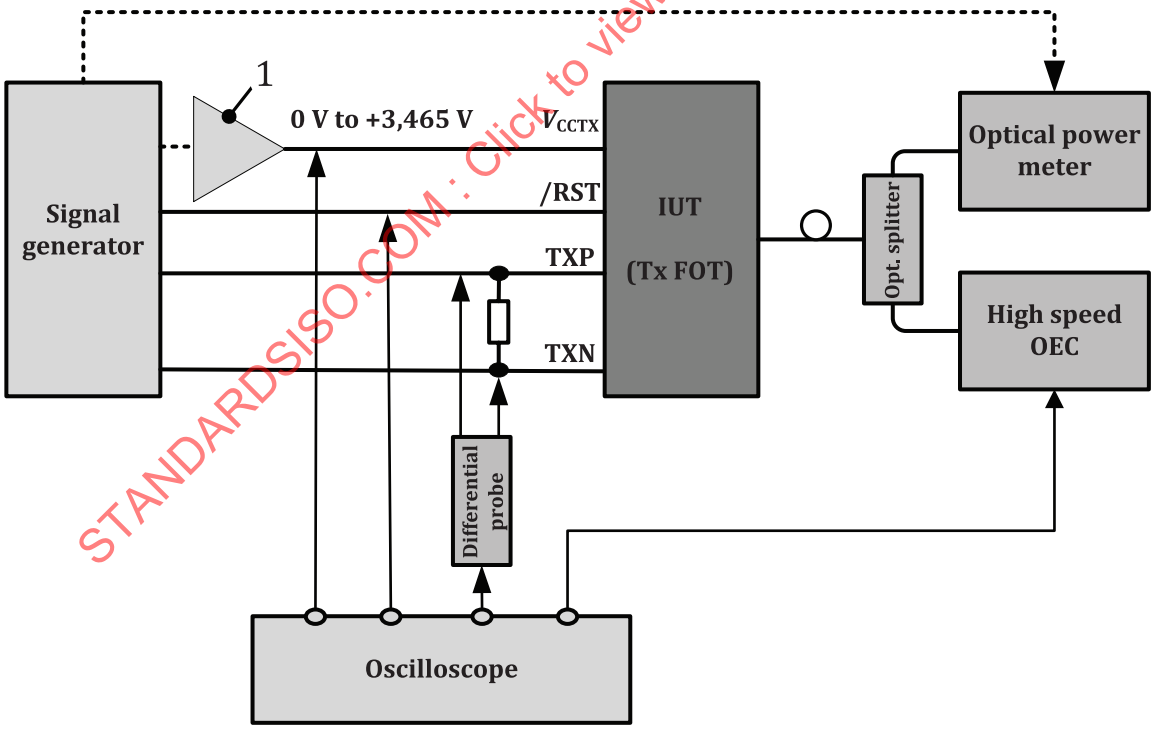
For example, t_{ON2}(max) time after the /RST signal transitions to logic 1 to start evaluating SP2 signal quality to check conformance to the requirements for valid MOST data.

Measuring electrical parameters such as LVTTL or LVDS conformance is beyond the scope of this document and not discussed in detail herein, but some guidelines are given to facilitate proper parameter interpretation.

10.2 Measuring EOC parameters

10.2.1 Measuring EOC parameters — Test set-up

Figure 24 shows an example of the set-up for the measurement of the EOC performance.



Key

1 power amplifier or programmable power supply

Figure 24 — Set-up for measuring EOC power-on and power-off parameters

The main parts of the set-up are:

— The IUT is fitted according to the manufacturer's recommended set-up.

— The signal generator is used to produce the stimuli (test patterns), produce the trigger signal for the optical power meter and control the EOC power supply.

— The optical splitter has a well-defined split ratio. Alternatively, the test can be performed in two stages (off-state to on-state test and on-state to off-state test), where the optical power meter can be connected directly to the IUT for the first stage and the high-speed OEC for the second stage. In this case, an optical splitter is not needed.

— The optical power meter measures the average optical power output of the IUT. The peak hold measurement should be used.

— The high-speed OEC converts the optical signal to an electrical signal.

— The oscilloscope captures input and output signal data. The SP1 signal is a differential signal. An active differential probe should be used for measurement.

— The power amplifier/programmable power supply turns the EOC power on and off and provides the desired supply voltage.

10.2.2 Measuring EOC parameters — Signal charts

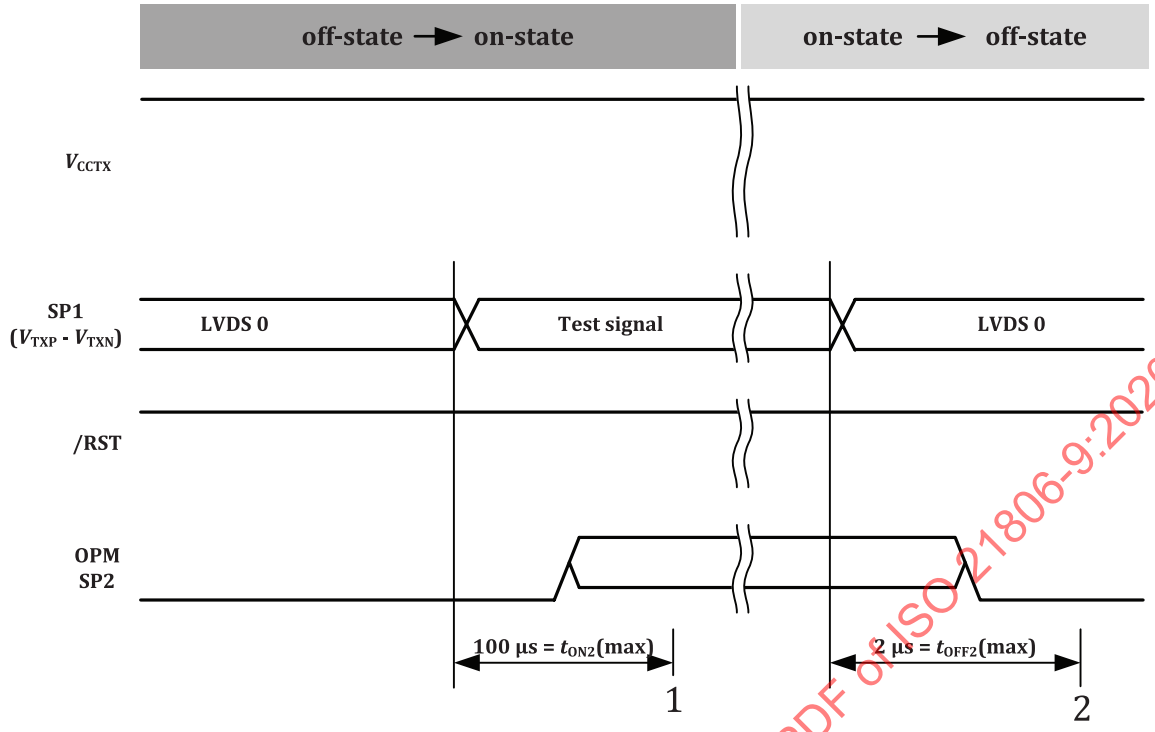
The signal charts represent the graphical view of test sequences. They show the location of the action points and provide the prerequisites for the corresponding tests for the EOC parameters.

The EOC parameter testing requires two different types of test sequences:

— In the first sequence, power-on and power-off behaviour is controlled by the signal content of SP1 while the /RST signal is logic 1 (Figure 25).

— In the second sequence, power-on and power-off behaviour is controlled by the /RST signal (Figure 26).

Figure 25 specifies the EOC signal chart No. 1 for measuring EOC parameters.



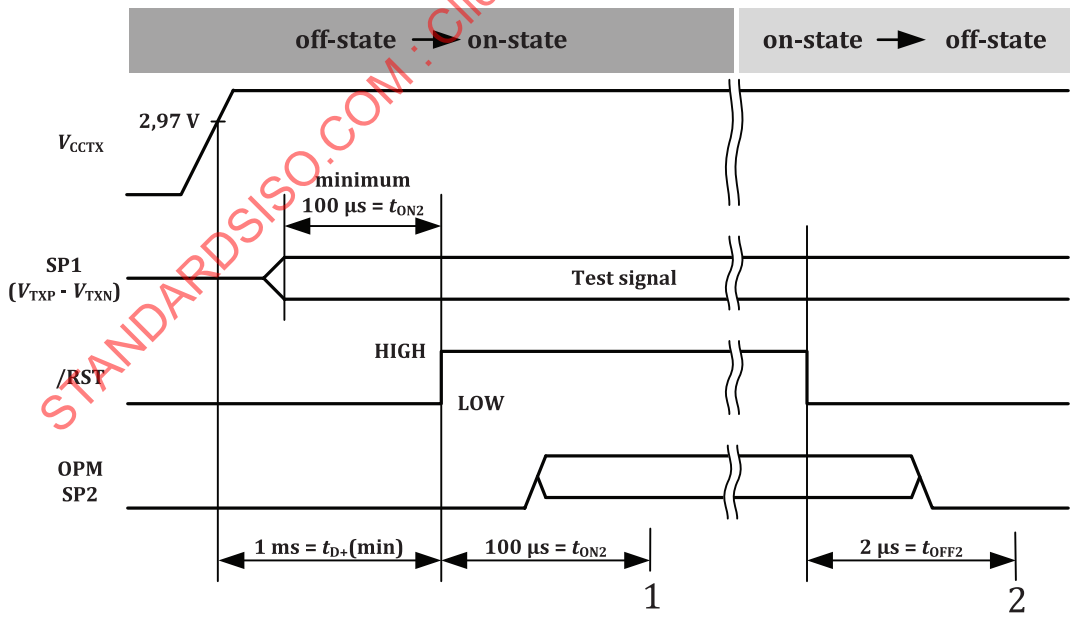
Key

1 marker action point 1

2 marker action point 2

Figure 25 — Measuring EOC parameters — EOC signal chart No. 1

Figure 26 specifies the EOC signal chart No. 2 for measuring EOC parameters.



Key

1 marker action point 1

2 marker action point 2

Figure 26 — Measuring EOC parameters — EOC signal chart No. 2

10.2.3 Measuring EOC parameters — Test sequences

10.2.3.1 EOC test sequence #1 — Off-state to on-state by SP1 signal

Table 9 specifies the EOC test sequence #1.

Table 9 — EOC test sequence #1

Item	Content	
Signal chart	Figure 25	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 1
	SP1 (V_{TXP} - V_{TXN}):	LVDS 0
Initial state: Output	SP2 (optical):	average output power below P_{OFF2}(max)
Test signal: Inputs	SP1 (V_{TXP} - V_{TXN}):	10 kHz square wave pattern
		LVDS compliant
Output/expected behaviour	The EOC remains in off-state with no average output power-on SP2 above P_{OFF2}(max) at any time.	

This test sequence checks the transition detection mechanism of the EOC. An optical power meter shall monitor the SP2 output before, during, and after the test to ensure the off-state requirement $P_{opt2} < P_{OFF2}$(max) is met.

10.2.3.2 EOC test sequence #2 — Off-state to on-state by SP1 signal

Table 10 specifies the EOC test sequence #2.

Table 10 — EOC test sequence #2

Item	Content	
Signal chart	Figure 25	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 1
	SP1 (V_{TXP} - V_{TXN}):	LVDS 0
		0 Hz to 10 kHz square wave pattern
		LVDS compliant
Initial state: Output	SP2 (optical):	average output power below P_{OFF2}(max)
Test signal: Inputs	SP1 (V_{TXP} - V_{TXN}):	12 MHz square wave pattern
		LVDS compliant
Output/expected behaviour	The EOC transitions to on-state within time t_{ON2}(max).	

This test sequence checks the transition detection mechanism of the EOC. In this particular test the F_{ON1}(min) conformance is checked.

The oscilloscope shall check the maximum allowed transition time from off-state to on-state. ISO 21806-8:2020, Clause 10 requires that the EOC is in on-state not later than t_{ON2}(max) time after all on conditions are met. In this case, the start of t_{ON2} is triggered by the first rising edge of the test stimulus.

Since there is no measurable marker that indicates when the EOC enters the on-state, an indirect method is used: after the maximum allowed time (end of t_{ON2}(max) – marked as action point 1 in the EOC signal Figure 25), a check of on-state requirements is started.

For this test, since the input is LVDS 0, only the optical power output of the SP2 interface is checked.

10.2.3.3 EOC test sequence #3 — On-state to off-state by SP1 signal

Table 11 specifies the EOC test sequence #3.

Table 11 — EOC test sequence #3

Item	Content	
Signal chart	Figure 25	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 1
	SP1 (V_{TXP} - V_{TXN}):	12 MHz LVDS compliant square wave
Initial state: Output	SP2 (optical):	average output power within P_{opt2}
Test signal: Inputs	SP1 (V_{TXP} - V_{TXN}):	LVDS 0
		0 Hz to 10 kHz square wave pattern
		LVDS compliant
Output/expected behaviour	The EOC transitions to off-state within time t_{OFF2}(max).	

This test sequence checks the transition detection mechanism of the EOC.

The oscilloscope shall check the maximum allowed transition time from on-state to off-state. ISO 21806-8:2020, Clause 10 requires that the EOC is in off-state not later than t_{OFF2}(max) time after one or more off conditions are met. In this case, the start of t_{OFF2} is triggered by the last falling edge of the initial state data pattern.

Since there is no measurable marker that indicates when the EOC enters the off-state, an indirect method is used: after the maximum allowed time (end of t_{OFF2}(max) – marked as action point 2 in the EOC signal chart Figure 25), a check of off-state requirements is started.

The optical power meter shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement $P_{opt2} < P_{OFF2}$(max) is met.

To trigger the start of the optical power measurement the signal generator may assert the trigger signal to the optical power meter t_{OFF2}(max) after switching the test signal to LVDS 0, for example, to initiate measurement of the optical power. The peak-hold function of the optical power meter ensures that short light blips are not "averaged" away.

10.2.3.4 EOC test sequence #4 — Off-state to on-state by SP1 signal

Table 12 specifies the EOC test sequence #4.

Table 12 — EOC test sequence #4

Item	Content	
Signal chart	Figure 25	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 1
	SP1 (V_{TXP} - V_{TXN}):	LVDS 0
		0 Hz to 10 kHz square wave pattern
		LVDS compliant
Initial state: Output	SP2 (optical):	average output power below P_{OFF2}(max)
Test signal: Inputs	SP1 (V_{TXP} - V_{TXN}):	LVDS compliant stress pattern with nominal bit rate (ρ_{BR})
Output/expected behaviour	The EOC transitions to on-state within time t_{ON2}(max).	

This test sequence checks the transition detection mechanism of the EOC.

The oscilloscope shall check the maximum allowed transition time from off-state to on-state. ISO 21806-8:2020, Clause 10 mandates that the EOC is in on-state not later than t_{ON2}(max) time after all on conditions are met. In this case, the start of t_{ON2} is triggered by the first rising edge of the test stimulus.

Since there is no measurable marker that indicates when the EOC enters the on-state, an indirect method is used: after the maximum allowed time (end of t_{ON2}(max) – marked as action point 1 in the EOC signal chart Figure 25) a check of on-state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality is checked. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP2 signal quality. To assist the capture of the SP2 data in on-state, the signal generator may assert the trigger signal to the oscilloscope t_{ON2}(max) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs), the oscilloscope is triggered by the SP1 signal with a delay of 100 µs.

10.2.3.5 EOC test sequence #5 — On-state to off-state by SP1 signal

Table 13 specifies the EOC test sequence #5.

Table 13 — EOC test sequence #5

Item	Content	
Signal chart	Figure 25	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 1
	SP1 (V_{TXP} - V_{TXN}):	LVDS compliant stress pattern with nominal bit rate (ρ_{BR})
Initial state: Output	SP2 (optical):	average output power within P_{opt2}
Test signal: Inputs	SP1 (V_{TXP} - V_{TXN}):	LVDS 0
		0 Hz to 10 kHz square wave pattern
		LVDS compliant
Output/expected behaviour	The EOC transitions to off-state within time t_{OFF2}(max).	

This test sequence checks the transition detection mechanism of the EOC.

The oscilloscope shall check the maximum allowed transition time from on-state to off-state. ISO 21806-8:2020, Clause 10 requires that the EOC is in off-state not later than t_{OFF2}(max) time after one or more off conditions are met. In this case, the start of t_{OFF2} is triggered by the last falling edge of the initial state data pattern.

Since there is no measurable marker that indicates when the EOC enters the off-state, an indirect method is used: after the maximum allowed time (end of t_{OFF2}(max) – marked as action point 2 in the EOC signal chart Figure 25), a check of off-state requirements is started.

The optical power meter shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement $P_{opt2} < P_{OFF2}$(max) is met.

To trigger the start of the optical power measurement, the signal generator may assert the trigger signal to the optical power meter t_{OFF2}(max) after switching the test signal to LVDS 0, for example, to initiate measurement of the optical power. The peak-hold function of the optical power meter ensures short light blips are not "averaged" away.

10.2.3.6 EOC test sequence #6 — Off-state to on-state by /RST signal

Table 14 specifies the EOC test sequence #6.

Table 14 — EOC test sequence #6

Item	Content	
Signal chart	Figure 26	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 0
	SP1 (V_{TXP} - V_{TXN}):	LVDS compliant stress pattern with nominal bit rate (ρ_{BR})
Initial state: Output	SP2 (optical):	average output power below P_{OFF2}(max)
Test signal: Inputs	/RST:	logic 1
Output/expected behaviour	The EOC transitions to on-state within time t_{ON2}(max).	

This test sequence checks the reset mechanism of the EOC and the minimal allowed time for the /RST signal to be set to logic 1 after the power supply crosses the V_T (min) voltage. There are two aspects for treating this minimal allowed time.

The first is the power supply application aspect; the reset generator providing the signal shall be designed to ensure the /RST signal does not transition to logic 1 before t_{D+}(min) time passes after the V_{CCTX} measured on the EOC power supply pins crosses V_T.

The second is the EOC parameter aspect; ISO 21806-8 requires that when being supplied with an operating voltage within V_{CCTXGR}, the internal circuitry of the EOC settles into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+}. By driving the /RST signal logic 1 at the t_{D+}(min) time it is checked if the EOC complies to that specification.

Since there is no measurable marker that indicates when the EOC enters the on-state, an indirect method is used for testing the t_{ON2}(max) conformance: after the maximum allowed time (end of t_{ON2}(max) – marked as action point 1 in the EOC signal chart Figure 26), a check of on-state requirements is started.

For this test, along with the output power of the SP2 interface, also the SP2 signal quality is checked. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP2 signal quality.

10.2.3.7 EOC test sequence #7 — On-state to off-state by /RST signal

Table 15 specifies the EOC test sequence #7.

Table 15 — EOC test sequence #7

Item	Content	
Signal chart	Figure 26	
Initial state: Inputs	V_{CCTX}:	according to operating conditions
	/RST:	logic 1
	SP1 (V_{TXP} - V_{TXN}):	LVDS compliant stress pattern with nominal bit rate (ρ_{BR})
Initial state: Output	SP2 (optical):	average output power within P_{opt2}
Test signal: Inputs	/RST:	logic 0
Output/expected behaviour	The EOC transitions to off-state within a time t_{OFF2}(max) after the /RST signal is set to logic 0 and it stays in off-state (with $P_{opt2} < P_{OFF2}$(max)) as long as the /RST signal is logic 0.	

This test sequence checks the reset mechanism of the EOC.

Since there is no measurable marker that indicates when the EOC enters the off-state, an indirect method is used: after the maximum allowed time (end of t_{OFF2}(max) – marked as action point 2 in the EOC signal chart Figure 26), a check of off-state requirements is started.

The optical power meter shall start monitoring the SP2 output after the time marked as action point 2 to ensure the off-state requirement $P_{opt2} < P_{OFF2}$(max) is met. A trigger signal from the signal generator may be used to activate the optical power meter.

10.3 Measuring OEC parameters

10.3.1 Measuring OEC parameters — Test set-up

Figure 27 outlines the set-up for measuring OEC power-on and power-off parameters.

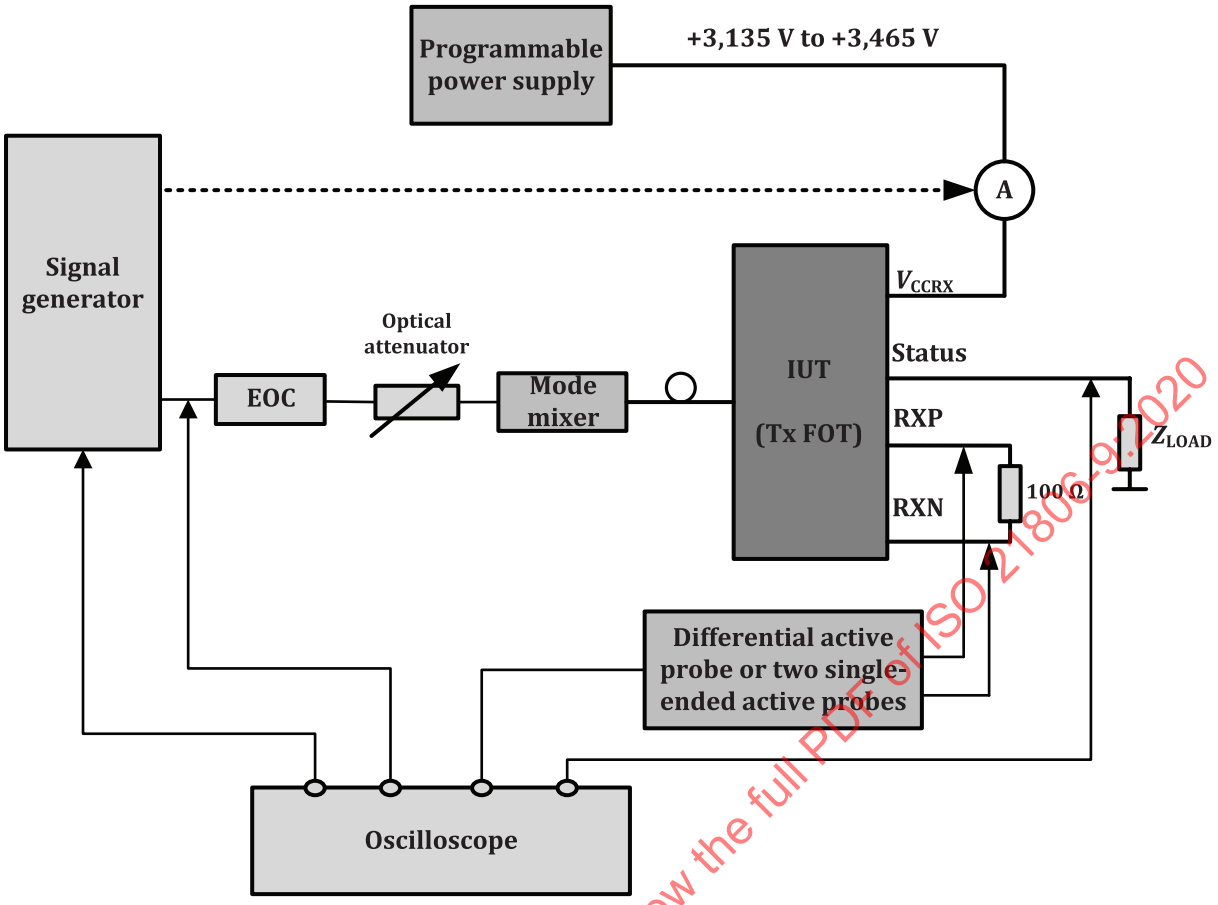


Figure 27 — Set-up for measuring OEC power-on and power-off parameters

The main parts of the set-up are:

— The IUT is fitted according to the manufacturer's recommended set-up and is powered constantly during the test(s).

— The signal generator is used to produce the test patterns and produce the trigger signal for the oscilloscope.

— The EOC/optical attenuator/mode mixer converts the electrical signal to an optical signal and shapes it to the requirements as specified in ISO 21806-8:2020, Clause 9. If applicable, the stimulus is applied according to the set-ups given in Table 6 and Table 7.

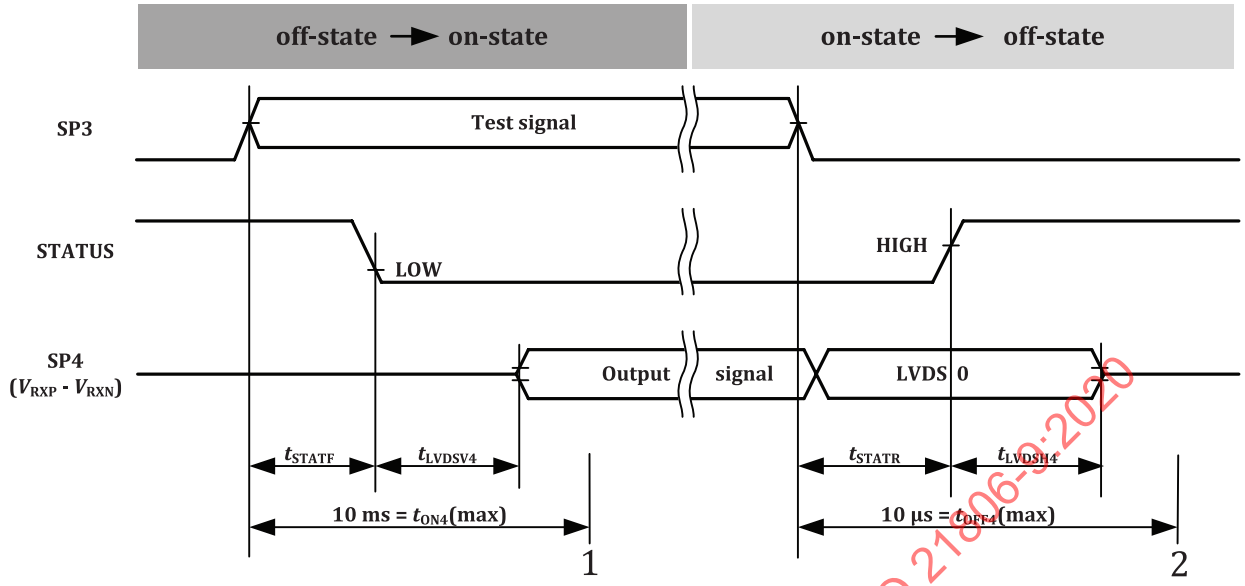
— The oscilloscope captures input and output signal data. The SP4 signal is a differential signal. An active differential probe should be used for measurement.

— The ampere meter measures the current consumption of the OEC under test (in off-state).

10.3.2 Measuring OEC parameters — Signal charts

The signal chart represents the graphical view of the test sequence. It shows the location of the action points and provides the prerequisites for the corresponding tests of the OEC parameters.

Figure 28 specifies the OEC signal chart for measuring OEC parameters.



Key

1 marker action point 1

2 marker action point 2

Figure 28 — Measuring OEC parameters — OEC signal chart

10.3.3 Measuring OEC parameters — Test sequences

10.3.3.1 OEC test sequence #1 — off-state to on-state

Table 16 specifies the OEC test sequence #1.

Table 16 — OEC test sequence #1

Item	Content	
Signal chart	Figure 28	
Initial state: Inputs	V_{CCRX}: SP3 (optical):	according to operating conditions P_{opt3}(avg) < P_{OFF3}(max)
Initial state: Output	STATUS: SP4 (V_{RXP} – $V_{RXN:}$)	logic 1 disabled
Test signal: Inputs	SP3 (optical):	continuous 10 kHz square wave P_{opt3}(avg): –22 dBm to –2 dBm
Output/expected behaviour	The OEC stays in off-state with STATUS logic 1 and SP4 outputs disabled. With input stimulus present, I_{CCRX} may exceed $I_{CCSLEEP}$(max).	

This test sequence checks the transition detection and wake-up mechanism of the OEC.

The stimulus shall be applied according to the set-ups given in Table 6 and Table 7.

The minimum and maximum values of the optical power levels (b_0, b_1) shall be tested. Test signals with multiple optical power levels should be used.

10.3.3.2 OEC test sequence #2 — Off-state to on-state

Table 17 specifies the OEC test sequence #2.

Table 17 — OEC test sequence #2

Item	Content	
Signal chart	Figure 28	
Initial state: Inputs	V_{CCRX}: SP3 (optical):	according to operating conditions P_{OPT3}(avg) < −50 dBm
Initial state: Output	STATUS: SP4 (V_{RXP} − V_{RXN})	logic 1 disabled
Test signal: Inputs	SP3 (optical):	continuous 12 MHz square wave P_{opt3}(avg): −35 dBm
Output/expected behaviour	The OEC stays in off-state with STATUS logic 1 and SP4 outputs disabled. With input stimulus present, I_{CCRX} may exceed $I_{CCSLEEP}$(max).	

This test sequence checks the transition detection and wake-up mechanism of the OEC. For power ranges outside the operating range, any light source can be used.

10.3.3.3 OEC test sequence #3 — Off-state to on-state

Table 18 specifies the OEC test sequence #3.

Table 18 — OEC test sequence #3

Item	Content	
Signal chart	Figure 28	
Initial state: Inputs	V_{CCRX}: SP3 (optical):	according to operating conditions P_{opt3}(avg) < −50 dBm
Initial state: Output	STATUS: SP4 (V_{RXP} − V_{RXN})	logic 1 disabled
Test signal: Inputs	SP3 (optical):	12 MHz square wave burst with duration ≤ t_{STATF} (min) P_{opt3}(avg): −22 dBm to −2 dBm
Output/expected behaviour	The OEC stays in off-state with STATUS logic 1 and SP4 outputs disabled. With input stimulus present, I_{CCRX} may exceed $I_{CCSLEEP}$(max).	

This test sequence checks the transition detection and wake-up mechanism of the OEC.

The stimulus shall be applied according to the set-ups given in Table 6 and Table 7.

The minimum and maximum values of the optical power levels (b_0, b_1) shall be tested. Test signals with multiple optical power levels should be used.

10.3.3.4 OEC test sequence #4 — Off-state to on-state

Table 19 specifies the OEC test sequence #4.

Table 19 — OEC test sequence #4

Item	Content
Signal charts	Figure 28
Initial state: Inputs	V_{CCRX}: according to operating conditions SP3 (optical): P_{opt3}(avg) < –50 dBm
Initial state: Output	STATUS: logic 1 SP4 (V_{RXP} – $V_{RXN:}$) disabled
Test signal: Inputs	SP3 (optical): 12 MHz square wave burst with duration > t_{STATF}(min) P_{opt3}(avg): –22 dBm to –2 dBm
Output/expected behaviour	The OEC transitions to on-state within time t_{ON4}(max) with STATUS logic 0 within t_{STATF}(min) to t_{STATF}(max), and valid LVDS levels within t_{LVDSV4}(max).

This test sequence checks the transition detection and wake-up mechanism of the OEC. The input signal represents no valid MOST data. Therefore, only the STATUS signal timing and SP4 LVDS conformance shall be checked.

The stimulus shall be applied according to the set-ups given in Table 6 and Table 7.

The minimum and maximum values of the optical power levels (b_0, b_1) shall be tested. Test signals with multiple optical power levels should be used.

10.3.3.5 OEC test sequence #5 — On-state to off-state

Table 20 specifies the OEC test sequence #5.

Table 20 — OEC test sequence #5

Item	Content
Signal chart	Figure 28
Initial state: Inputs	V_{CCRX}: according to operating conditions SP3 (optical): continuous 12 MHz square wave P_{opt3}(avg): –22 dBm to –2 dBm
Initial state: Output	STATUS: logic 0 SP4 (V_{RXP} – $V_{RXN:}$) LVDS compliant signal
Test signal: Inputs	SP3 (optical): P_{opt3}(avg) < –35 dBm
Output/expected behaviour	The OEC transitions to off-state with STATUS logic 1 within t_{STATR}(max) and SP4 outputs disabled within t_{OFF4}(max), but not earlier than t_{LVDSH4}(min) after STATUS transitions to Logic 1. After t_{OFF4}(max), I_{CCRX} is below $I_{CCSLEEP}$(max).

This test sequence checks the transition detection and shutdown mechanism of the OEC.

To trigger the start of the electrical current measurement, the signal generator may assert the trigger signal to the ampere meter t_{OFF4}(max) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

The stimulus shall be applied according to the set-ups given in Table 6 and Table 7.

The minimum and maximum values of the optical power levels (b_0, b_1) shall be tested. Test signals with multiple optical power levels should be used.

10.3.3.6 OEC test sequence #6 — Off-state to on-state

Table 21 specifies the OEC test sequence #6.

Table 21 — OEC test sequence #6

Item	Content	
Signal chart	Figure 28	
Initial state: Inputs	V_{CCRX}:	according to operating conditions
	SP3:	MOST150 oPHY stress pattern with nominal bit rate (ρ_{BR})
		P_{opt3}(avg) < –35 dBm
Initial state: Output	STATUS:	logic 1
	SP4 ($V_{RXP} - V_{RXN}$):	disabled
Test signal: Inputs	SP3:	P_{opt3}(avg): –22 dBm to –2 dBm
Output/expected behaviour	The OEC transitions to on-state within time t_{ON4}(max) with STATUS logic 0 within t_{STATF}(min) to t_{STATF}(max), and valid LVDS levels within t_{LVDSV4}(max).	

This test sequence checks the transition detection and wake-up mechanism of the OEC.

Since there is no measurable marker that indicates when the OEC enters the on-state, an indirect method is used for the t_{ON4}(max) parameter evaluation: after the maximum allowed time (end of t_{ON4}(max) – marked as action point 1 in the signal chart Figure 28) a check of on-state requirements is started.

For this test, along with checking for STATUS logic 0, the SP4 signal quality is evaluated. At action point 1, the oscilloscope shall start capturing the data sequence, which is used for evaluating the SP4 signal quality. To assist the capture of the SP4 data, the signal generator may assert the trigger signal to the oscilloscope t_{ON4}(max) after activation of the test signal. Alternatively (if the signal generator does not have enough outputs), the oscilloscope may be triggered by the SP1 signal with a delay of 10 ms.

The stimulus shall be applied according to the set-ups given in Table 6 and Table 7.

The minimum and maximum values of the optical power levels (b_0, b_1) shall be tested. Test signals with multiple optical power levels should be used.

10.3.3.7 OEC test sequence #7 — On-state to off-state

Table 22 specifies the OEC test sequence #7.

Table 22 — OEC test sequence #7

Item	Content	
Signal charts	Figure 28	
Initial state: Inputs	V_{CCRX}:	according to operating conditions
	SP3 (optical):	MOST150 oPHY stress pattern with nominal bit rate (ρ_{BR})
		P_{opt3}(avg): –22 dBm to –2 dBm
Initial state: Output	STATUS:	logic 0
	SP4 ($V_{RXP} - V_{RXN}$):	LVDS compliant valid MOST data
Test signal: Inputs	SP3 (optical):	P_{opt3}(avg) < –35 dBm
Output/expected behaviour	The OEC transitions to off-state with STATUS logic 1 within t_{STATR}(max) and SP4 outputs disabled within t_{OFF4}(max), but not earlier than t_{LVDSH4}(min) after STATUS transitions to logic 1. After t_{OFF4}(max), I_{CCRX} is below $I_{CCSLEEP}$(max).	

This test sequence checks the transition detection and shutdown mechanism of the OEC.

To trigger the start of the electrical current measurement, the signal generator may assert the trigger signal to the ampere meter t_{OFF4}(max) after application of the test signal to allow the ampere meter to perform current consumption measurement (used in t_{OFF4} requirement evaluation).

The stimulus shall be applied according to the set-ups given in Table 6 and Table 7.

The minimum and maximum values of the optical power levels (b_0, b_1) shall be tested. Test signals with multiple optical power levels should be used.

11 Detecting bit rate (frequency reference)

The bit rate is detected as follows:

— Data-pulses range from 2 UI to 6 UI yielding five different pulse widths (2 UI, 3 UI, 4 UI, 5 UI, and 6 UI). A clock at UI rate represents a cycle time of 1 UI, which is twice the bit rate (i.e. if ρ_{Fs} is 48 kHz, the bit rate is 147,45 Mbit/s and the UI clock is 294,91 MHz).

— A method of extracting the UI clock out of a waveform is a mandatory function to be provided with the oscilloscope. In a first step, the recovered UI clock is a linear approximation that fits best to the acquired waveform in terms of phase and frequency. The approximation of the clock's phase shall be performed with regard to the rising edges of the data stream only. Then the bit rate is half the UI rate.

— The bit rate can be measured with the MOST150 oPHY stress pattern or any other valid data pattern. Set-up of the oscilloscope shall follow the general requirements (see 6.2) using acquisition length of 10 megasample and a sampling rate of 10 gigasample/s.

12 System performance

12.1 General

The system-level specifications apply to an entire MOST network.

12.2 SP4 receiver tolerance

Unlike the link-level tests, which use a pattern generator as the signal source, the system-level tests use live data from a MOST150 ring. Using the same eye diagram methodologies developed in Clause 9, a measurement is taken at SP4 of the TimingMaster node. By taking the measurement in this way, one can quantify the total jitter accumulation around the ring. This measurement is applicable for every node in the network at SP4.

Figure 29 shows the SP4 receiver tolerance set-up.

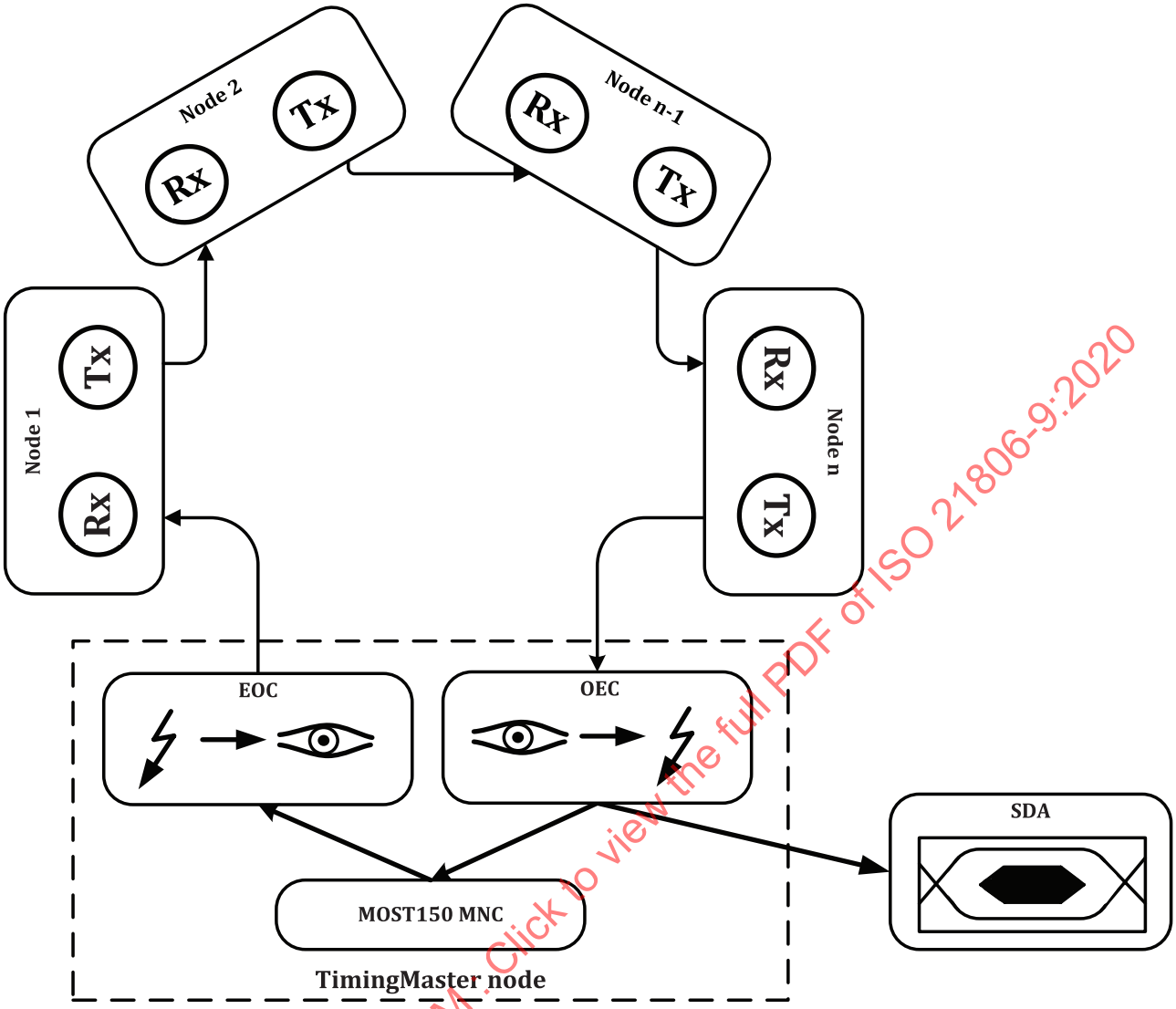


Figure 29 — SP4 receiver tolerance set-up

12.3 TimingMaster delay tolerance

TimingMaster delay tolerance is a measure of end-to-end delay and phase variation between SP1 and SP4 of the MOST device that contains the TimingMaster. To ensure proper network operation, the total network delay shall not exceed the specified maximum (see ISO 21806-8:2020, 11.2).

Following the set-up diagram shown in Figure 30, the total delay can be measured with an oscilloscope.

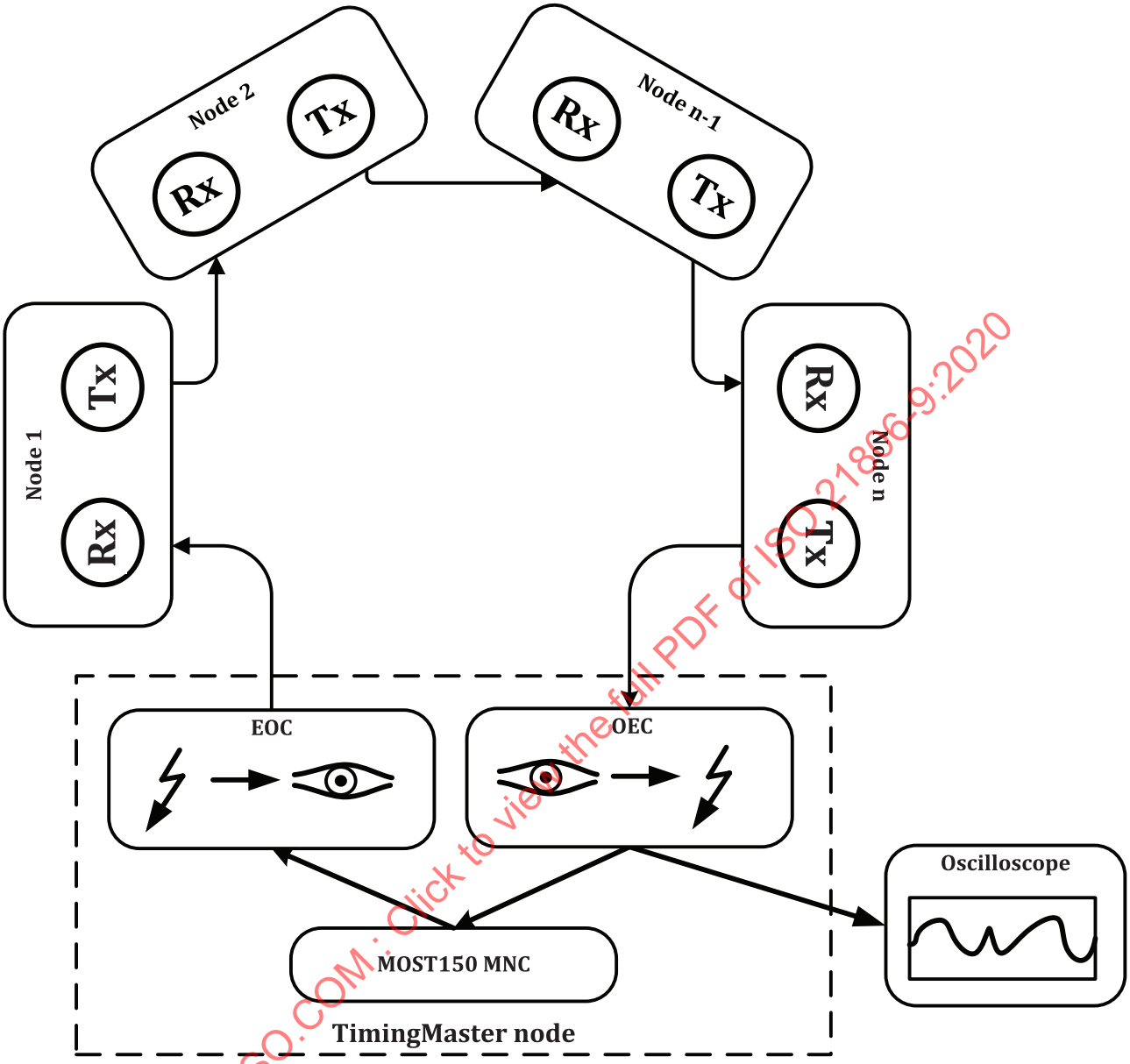


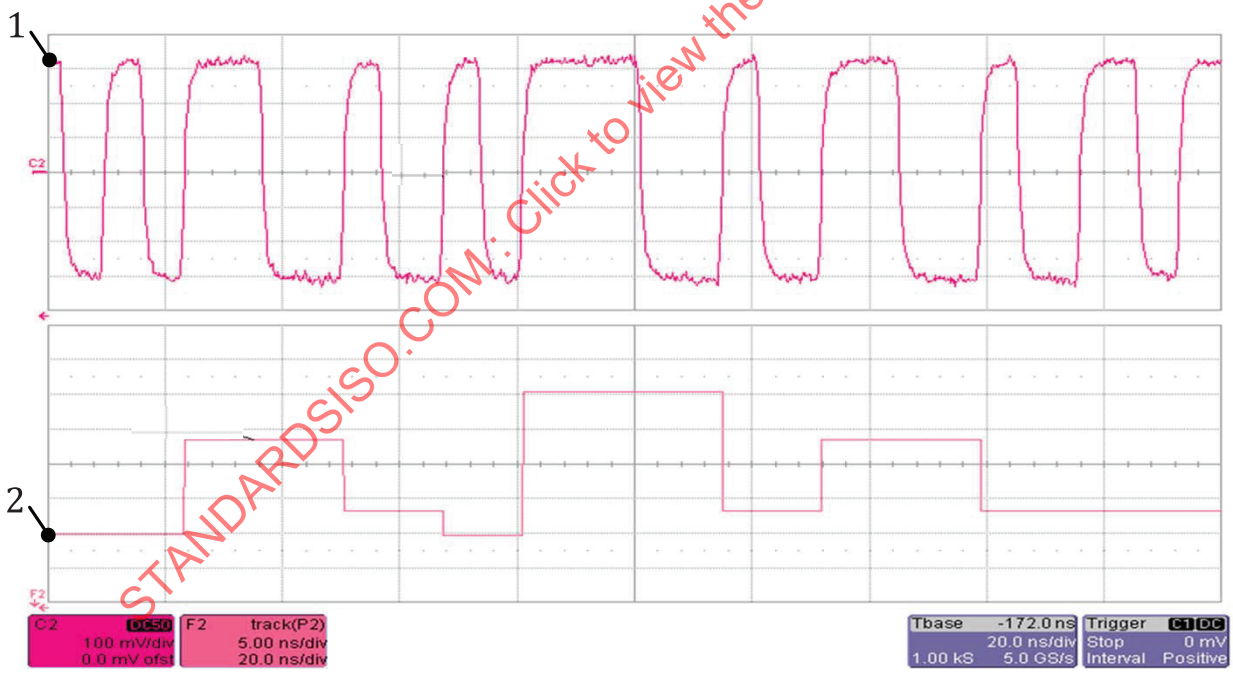
Figure 30 — TimingMaster delay tolerance set-up

Table 23 specifies the procedure used to measure the total delay. The oscilloscope used shall be able to trigger on a specified period and shall have software functions for tracking periods. Two differential probes are needed.

Table 23 — TimingMaster delay tolerance

Step	Description
Acquiring a waveform	For this measurement, the sampling memory of the oscilloscope should be adjusted to capture at least one frame of data. One differential probe is connected to SP1 of the TimingMaster node. A second differential probe is connected to SP4 of the TimingMaster node. The vertical scale is adjusted to achieve sufficient vertical resolution on both channels. The trigger settings are adjusted to trigger on the interval of rising edges (period) on SP1. The interval should be set to 10 UI ± 0,5 UI. The trigger mode should be normal. A sequence of the data stream ("waveform") is sampled into the oscilloscope's memory.
Measure period	The MOST150 data stream contains a period of 10 UI at the start of each frame. This long period can be used as a marker to measure the delay between any two points in the network. Configure the oscilloscope to measure the period of both SP1 and SP4.
Track the period	Configure the oscilloscope to display a "Track" waveform for both SP1 and SP4 period measurements. This should result in two waveforms (see Figure 31 and Figure 32) with time on the y-axis where the line indicates the length of the current period.
Measure the delay	Configure the oscilloscope display to show only the SP1 and SP4 period tracks. Turn on infinite persistence and adjust the display to show the 10 UI segment for both SP1 and SP4. Using the cursor, measure the total time between the trigger point and the rightmost edge of the SP4 10 UI period. This is the TimingMaster delay.

Figure 31 shows an example of tracking SP4 period.



Key

1 SP4

2 SP4 period

Figure 31 — Example of tracking SP4 period

Figure 32 shows how the TimingMaster delay is measured.

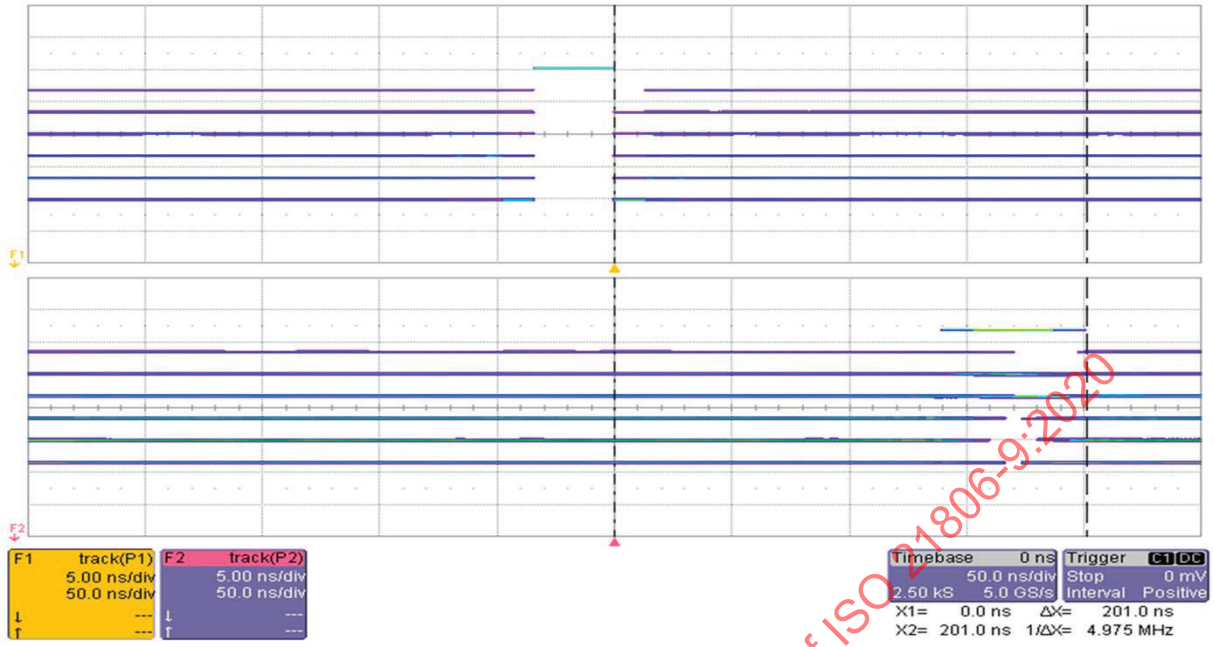


Figure 32 — TimingMaster delay

13 Conformance tests of 150-Mbit/s optical physical layer

13.1 Location of interfaces

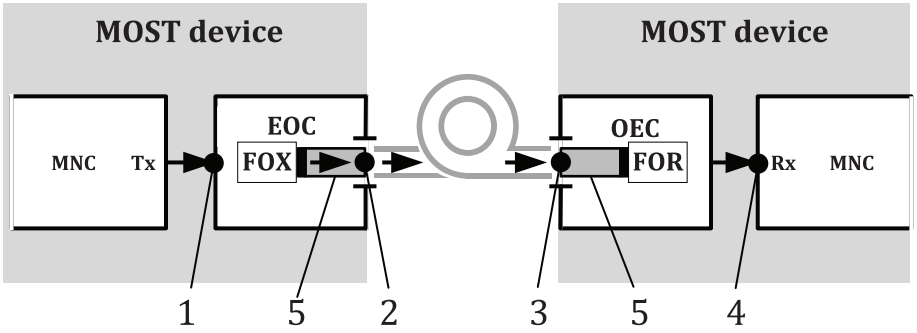
SP1 describes input parameters for the EOC. It also describes the output parameters of an MNC, including data path between MNC and EOC.

SP2 describes the optical output signal.

SP3 describes the optical input interface for the OEC. Signal characteristics at SP3 consider worst-case optical signal according to the SP2 definition plus deterioration due to the transport media.

SP4 link quality describes the output parameters for OECs including termination. SP4 receiver tolerance describes the input tolerance for MNCs.

Figure 33 shows the location of specification points (SP).



Key

1 SP1
2 SP2
3 SP3
4 SP4
5 optical pigtail

Figure 33 — Location of specification points

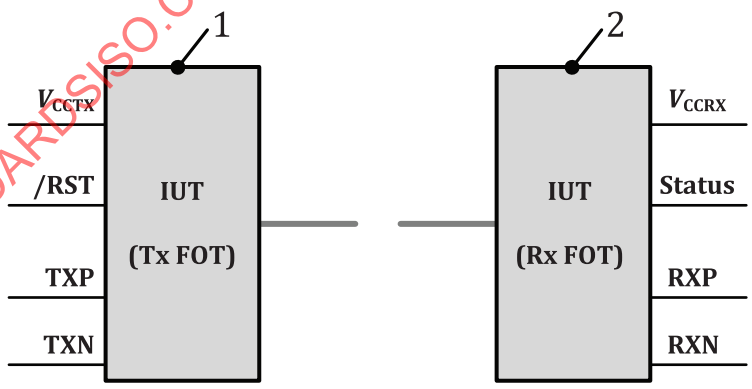
The MNC recovers signals that fulfil the SP4 parameters. Signals outside the ranges might cause bit errors. On Tx of the MNC (node n + 1) a recovered signal is available according to SP1 requirements and timing distortion (except transferred jitter) is eliminated.

13.2 Control signals

In addition to power supply terminals and data pins, an EOC provides an /RST input. The EOC provides activity detection in order to enable/disable light emission. Activity depends on the V_{CC} state, data content of SP1, and reset state.

The OEC also provides activity detection. Depending on the characteristics of the input signal (power level, signal content) the on-state/off-state is signalled by the status line.

Figure 34 shows the control signals for power-on and power-off behaviour.



Key

1 EOC power-on and power-off parameters
2 OEC power-on and power-off parameters

Figure 34 — Control signals for power-on and power-off behaviour

13.3 Limited access to specification points

On MOST device level, measurement has no access to SP1 and SP4. Therefore, conformance verification on MOST component and MOST module level is required. This is a precondition for simplification of the conformance verification of MOST devices, using the limited (access) conformance procedure.

Variation on input parameters can only be applied at SP3 (optical signal input of the MOST device). Parameters can only be measured at SP2. The power supply of the MNC, the EOC, and the OEC is fixed by the design of the MOST device and cannot be varied. Considering these circumstances, the limited physical layer conformance specifies a simplified test procedure that uses only the accessible interfaces of a MOST device, SP2 and SP3 (see Clause 16).

13.4 Parameter overview

Table 24 specifies the conformance procedures for the parameters of ISO 21806-8 that are relevant for physical layer conformance. For each parameter, it indicates how conformance can be achieved, depending on the type: MOST component (EOC/OEC), MOST module, or MOST device.

NOTE Developers of MOST components or MOST modules ensure that their products fulfil the specification under minimum/maximum conditions of their input parameters, considering environmental conditions and lifetime. The verification of these parameters is done using the procedure of the product characterization.

Table 24 — Conformance procedures for all parameters of specification points

SP	Parameter	Conformance procedure			
		MOST component		MOST module	MOST device
		EOC	OEC		
SP1	Bit rate	---[a]	---[a]	---[a]	M[c], V[b] (output via SP2)
	LVDS conformity	---[a]	---[a]	---[a]	---[a]
	Alignment jitter acc. to eye mask	---[a]	---[a]	---[a]	---[a]
	Transferred jitter RMS	---[a]	---[a]	---[a]	---[a]

[a] No conformance test necessary.

[b] V: Verification by datasheet of the used MOST components (no influence possible due to application).

The parameter shall be measured on the particular level (MOST component → MOST module → MOST device).

If characterization data are available of MOST components, which are used in MOST modules and if it is proved that the MOST module (application) has no influence to that parameter, the MOST module needs not be measured again for this parameter. This is the same when using characterized MOST components in MOST devices. The supplier may provide evidence for characterization/qualification process on lower level.

For example, spectral width is characterized and guaranteed by the LED manufacturer and cannot be influenced by other parameters like power supply. Therefore, FOT manufacturers or EOC manufacturers shall not characterize this parameter if they get characterization results of the LED from their suppliers. MOST device manufacturers just refer to the FOT datasheet for that parameter.

[c] Measure (T: temperature range, U: voltage range, P: optical input power range).

Table 24 *(continued)*

SP	Parameter	Conformance procedure			
		MOST component		MOST module	MOST device
		EOC	OEC		
SP2	Eye safety (see IEC 60825-1[4], IEC 60825-2[5])	V[b]	---[a]	---[a]	---[a]
	Centre wavelength	V[b]	---[a]	V[b]	---[a]
	Spectral width	V[b]	---[a]	V[b]	---[a]
	Optical output power	M[c] (TU), V[b]	---[a]	M[c] (TU), V[b]	M[c] (TU)
	Extinction ratio	M[c] (TU), V[b]	---[a]	V[b]	---[a]
	Transition time (rise and fall)	M[c] (TU), V[b]	---[a]	V[b]	M[c] (TU)
	Alignment jitter acc. to eye mask	M[c] (TU), V[b]	---[a]	V[b]	M[c] (TU)
	Transferred jitter RMS	M[c] (TU), V[b]	---[a]	V[b]	M[c] (TU)
	Optical overshoot/undershoot	M[c] (TU), V[b]	---[a]	V[b]	M[c] (TU)
	EOC test sequence #1 - off-state to on-state by SP1 signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
	EOC test sequence #2 - off-state to on-state by SP1 signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
	EOC test sequence #3 – on-state to off-state by SP1 signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
	EOC test sequence #4 - off-state to on-state by SP1 signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
	EOC test sequence #5 – on-state to off-state by SP1 signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
	EOC test sequence #6 - off-state to on-state by /RST signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
	EOC test sequence #7 - on-state to off-state by /RST signal	M[c] (U), V[b]	---[a]	V[b]	---[a]
SP3	Centre wavelength	V[b]	---[a]	V[b]	---[a]
	Spectral width	---[a]	V[b]	V[b]	---[a]
	Receivable optical power range for data recovery	---[a]	V[b]	V[b]	---[a]
	Limited physical layer test of data consistency	---[a]	---[a]	---[a]	M[c] (TU)

[a] No conformance test necessary.

[b] V: Verification by datasheet of the used MOST components (no influence possible due to application).

The parameter shall be measured on the particular level (MOST component → MOST module → MOST device).

If characterization data are available of MOST components, which are used in MOST modules and if it is proved that the MOST module (application) has no influence to that parameter, the MOST module needs not be measured again for this parameter. This is the same when using characterized MOST components in MOST devices. The supplier may provide evidence for characterization/qualification process on lower level.

For example, spectral width is characterized and guaranteed by the LED manufacturer and cannot be influenced by other parameters like power supply. Therefore, FOT manufacturers or EOC manufacturers shall not characterize this parameter if they get characterization results of the LED from their suppliers. MOST device manufacturers just refer to the FOT datasheet for that parameter.

[c] Measure (T: temperature range, U: voltage range, P: optical input power range).

Table 24 *(continued)*

SP	Parameter	Conformance procedure			
		MOST component		MOST module	MOST device
		EOC	OEC		
SP4	LVDS conformity	---[a]	V[b]	V[b]	---[a]
	Alignment jitter acc. to eye mask	---[a]	M[c] (TUP), V[b]	M[c] (TUP), V[b]	---[a]
	Transferred jitter RMS	---[a]	M[c] (TUP), V[b]	M[c] (TUP), V[b]	---[a]
	Current consumption in the off-state	---[a]	M[c] (TU), V[b]	V[b]	---[a]
	OEC test sequence #1 - off-state to on-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	OEC test sequence #2 - off-state to on-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	OEC test sequence #3 - off-state to on-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	OEC test sequence #4 - off-state to on-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	OEC test sequence #5 - on-state to off-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	OEC test sequence #6 - off-state to on-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	OEC test sequence #7 - on-state to off-state	---[a]	M[c] (U), V[b]	V[b]	---[a]
	Receiver tolerance	---[a]	---[a]	---[a]	---[a]
	TimingMaster delay tolerance	---[a]	---[a]	---[a]	---[a]
---	Mechanical interface requirements	---[a]	---[a]	M[c]	---[a]

[a] No conformance test necessary.

[b] V: Verification by datasheet of the used MOST components (no influence possible due to application).

The parameter shall be measured on the particular level (MOST component → MOST module → MOST device).

If characterization data are available of MOST components, which are used in MOST modules and if it is proved that the MOST module (application) has no influence to that parameter, the MOST module needs not be measured again for this parameter. This is the same when using characterized MOST components in MOST devices. The supplier may provide evidence for characterization/qualification process on lower level.

For example, spectral width is characterized and guaranteed by the LED manufacturer and cannot be influenced by other parameters like power supply. Therefore, FOT manufacturers or EOC manufacturers shall not characterize this parameter if they get characterization results of the LED from their suppliers. MOST device manufacturers just refer to the FOT datasheet for that parameter.

[c] Measure (T: temperature range, U: voltage range, P: optical input power range).

14 Physical layer verification for MOST components, MOST modules, and MOST devices

14.1 FOT

Full physical layer conformance verification shall be performed with one of five samples that shall be submitted by the manufacturer.

14.2 Pigtail

The conformance test plan covers pigtails with FOT:

a) THM: Full physical layer conformance test with subset pigtail shall be performed with one of five samples.

   The precondition is that the FOT passes full physical layer conformance verification successfully.

b) SMD: Pigtail fibre and connector are subject of full physical layer conformance verification.

14.3 MOST device

The conformance test plan covers MOST devices with FOT:

a) THM: limited physical layer conformance verification shall be performed with one MOST device that shall be submitted by the manufacturer.

   The precondition is that both the FOT and the pigtail have already passed full physical layer conformance verification successfully.

b) SMD: limited physical layer conformance verification

   The precondition is that the FOT has already passed full physical layer conformance verification successfully and that the pigtail has been characterized accordingly.

14.4 Development tool

The conformance verification of development tools is described in Annex C.

15 Full physical layer conformance

15.1 Overview

Full physical layer conformance refers to MOST modules or MOST components.

15.2 Consideration of FOT

Table 24 specifies parameters to be tested and verified.

For conformance testing according to Figure 37, V_{CCTX} shall have reached V_{CCTXOR} at the time of /RST signal transition to logic 1 (see ISO 21806-8).

15.3 Consideration of pigtail

Consideration of the pigtail depends on the FOT packaging as follows:

a) Pigtail with FOT (THM): full physical layer conformance test according to Table 24, column “MOST module”.

b) Pigtail with FOT (SMD): pigtail fibre and connector are subject of conformance verification.

   Pigtail fibre and connector are listed in the conformance test report together as an entity.

15.4 Consideration of connector interfaces

The conformance verification of the connector interface (check of dimensions) contains two steps. First, a characterization report, to be provided by the supplier, is checked. Second, three dimensions, arbitrarily chosen from the MOST connector drawings, are verified.

15.5 Generating test signals for the IUT

15.5.1 General information

With respect to full physical layer conformance, the generation of dynamic jitter for SP2 within the jitter extremes shall consider both deterministic and random jitter. The actual consistency of the jitter signal shall be reproducible.

15.5.2 Test set-up for jitter measurement

The test set-up for jitter measurement according to this document shall be used but with the following restrictions:

a) basic set-up (to be used for the complete input power range)

- POF length <2 m;
- light levels: –22 dBm to –2 dBm (minimum 6 steps);
- light source: transition time <1,00 ns.

b) low bandwidth set-up (to be used additionally for the minimum optical input power)

- POF length = 15 m (using mode mixer);
- light levels: –22 dBm;
- light source: transition time: 1,00 ns to 0,5 UI;
  extinction ratio: 10 dB to 12 dB.

16 Limited physical layer conformance

16.1 Overview

Limited physical layer conformance refers to MOST devices (see 13.3).

Generally, conformance testing requires access to all specification points. In addition, various test signals are applied to particular interface in order to check worst-case performance of MOST components and MOST modules that are connected to that interface. The physical layer conformance test considers all environment conditions (e.g. specified operating temperature, power supply variations).

An overview of the parameters to be tested and verified is shown in Table 24.

Figure 35 specifies the test set-up for limited physical layer verification comprising the following equipment:

- physical layer stress test tool (PHYSTT)[4];
- optical attenuator;
- mode mixer;
- optical splitter;
- optical power meter;
- measurement OEC;
- oscilloscope.

a) test set-up 1:

— check of lock capability depending on the variation of the optical input power;

— measurement of optical output power of SP2;

— check of data consistency by comparison of the IUT's input and output data stream.

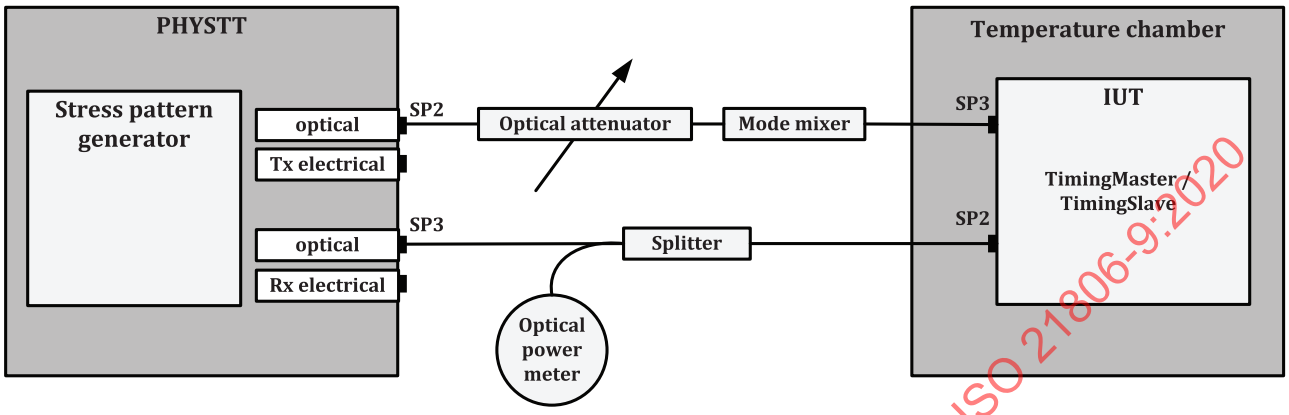


Figure 35 — Test set-up 1 for limited physical layer conformance test

b) test set-up 2: verification of signal integrity of optical signal at SP2 - IUT.

Verification of signal integrity includes measurement of pulse shape and timing characteristics at the IUT's optical SP2 interface. The test flow shown in 16.3 requires a closed loop between PHYSTT and IUT, providing functional communication over MOST. In addition, the measurement at SP2 of the IUT requires an OEC in the optical path with its electrical output coupled to the oscilloscope. The OEC's electrical output signal gives an analogue representation of the optical signal. Therefore, some kind of splitter functionality is required. Basically, there are two options. An optical splitter can be used, transferring a part of the optical signal to the measurement OEC and another part of the signal to the optical input of the PHYSTT. When using this approach, it shall be ensured that sufficient power is provided to both optical sinks for achieving sufficient SNR for the measurements and proper data recovery at the PHYSTT. The second option splits the electrical signal behind the OEC, while the IUT's optical signal is directly coupled to the OEC. The challenge of this approach is to realize the electrical splitter without degrading the electrical signal (e.g. by reflections).

Figure 36 specifies the test set-up 2a for limited physical layer conformance test.

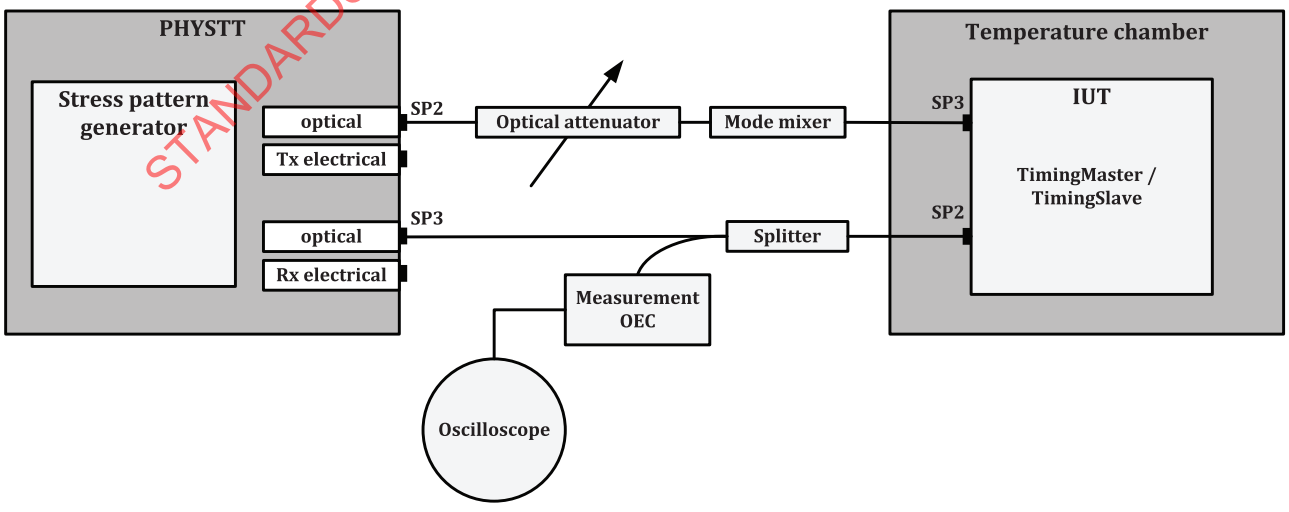


Figure 36 — Test set-up 2a for limited physical layer conformance test