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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 12:
50-Mbit/s balanced media physical layer

Véhicules routiers — Système de transport axé sur les médias —

Partie 12: Couche physique de support équilibré à 50-Mbit/s

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Foreword

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21806 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The Media Oriented Systems Transport (MOST) communication technology was initially developed at the end of the 1990s in order to support complex audio applications in cars. The MOST Cooperation was founded in 1998 with the goal to develop and enable the technology for the automotive industry. Today, MOST[1] enables the transport of high Quality of Service (QoS) audio and video together with packet data and real-time control to support modern automotive multimedia and similar applications. MOST is a function-oriented communication technology to network a variety of multimedia devices comprising one or more MOST nodes.

Figure 1 shows a MOST network example.
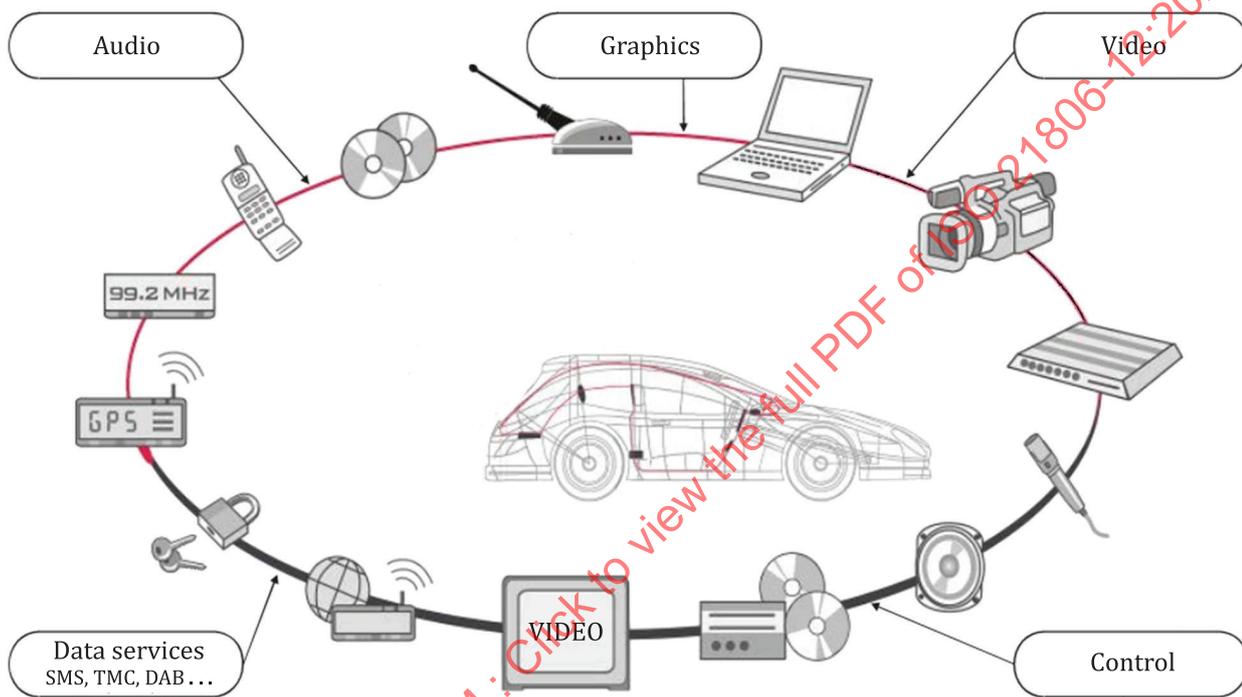
Figure 1 — MOST network example

The MOST communication technology provides:

— synchronous and isochronous streaming,

— small overhead for administrative communication control,

— a functional and hierarchical system model,

— API standardization through a function block (FBlock) framework,

— free partitioning of functionality to real devices,

— service discovery and notification, and

— flexibly scalable automotive-ready Ethernet communication according to ISO/IEC/IEEE 8802-3[2].

MOST is a synchronous time-division-multiplexing (TDM) network that transports different data types on separate channels at low latency. MOST supports different bit rates and physical layers. The network clock is provided with a continuous data signal.

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1)   MOST® is the registered trademark of Microchip Technology Inc. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO.

Within the synchronous base data signal, the content of multiple streaming connections and control data is transported. For streaming data connections, bandwidth is reserved to avoid interruptions, collisions, or delays in the transport of the data stream.

MOST specifies mechanisms for sending anisochronous, packet-based data in addition to control data and streaming data. The transmission of packet-based data is separated from the transmission of control data and streaming data. None of them interfere with each other.

A MOST network consists of devices that are connected to one common control channel and packet channel.

In summary, MOST is a network that has mechanisms to transport the various signals and data streams that occur in multimedia and infotainment systems.

The ISO standards maintenance portal (https://standards.iso.org/iso/) provides references to MOST specifications implemented in today's road vehicles because easy access via hyperlinks to these specifications is necessary. It references documents that are normative or informative for the MOST versions 4V0, 3V1, 3V0, and 2V5.

The ISO 21806 series has been established in order to specify requirements and recommendations for implementing the MOST communication technology into multimedia devices and to provide conformance test plans for implementing related test tools and test procedures.

To achieve this, the ISO 21806 series is based on the open systems interconnection (OSI) basic reference model in accordance with ISO/IEC 7498-1[1] and ISO/IEC 10731,[3] which structures communication systems into seven layers as shown in Figure 2. Stream transmission applications use a direct stream data interface (transparent) to the data link layer.
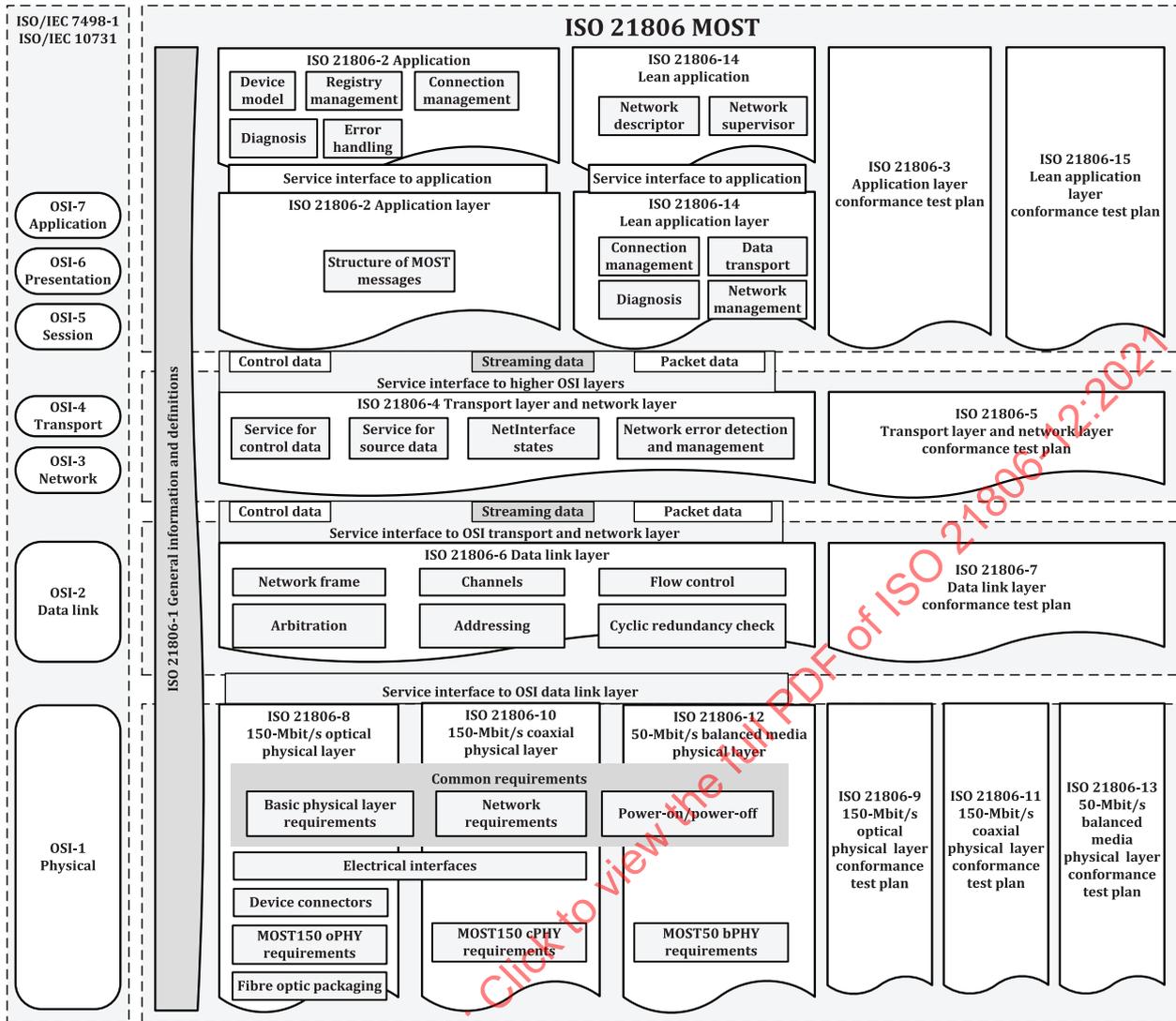
Figure 2 — The ISO 21806 series reference according to the OSI model

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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 12: 50-Mbit/s balanced media physical layer

1 Scope

This document specifies the 50-Mbit/s balanced media physical layer for MOST (MOST50 bPHY), a synchronous time-division-multiplexing network.

This document specifies the applicable constraints and defines interfaces and parameters, suitable for the development of products based on MOST50 bPHY. Such products include electrical interconnects, integrated receivers, transmitters, electrical to balanced media converters, and balanced media to electrical converters.

This document also establishes basic measurement techniques and actual parameter values for MOST50 bPHY.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21806-1, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 1: General information and definitions*

JEDEC No. JESD8C.01,[2)] *Interface Standard for Nominal 3 V/3,3 V Supply Digital Integrated Circuits*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21806-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1
balanced media
BM
unshielded or shielded twisted pair cable

3.2
BEC
balanced media to electrical converter
MOST component that converts a *balanced media* (3.1) signal into an electrical signal

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2)   Available at https://www.jedec.org/.

3.3
EBC
electrical to balanced media converter
MOST component that converts an electrical signal into a *balanced media* (3.1) signal

4 Symbols and abbreviated terms

4.1 Symbols

---	empty table cell or feature undefined
J_{tr}	transferred jitter
N_{BPF}	number of bits per frame
ρ_{Fs}	network frame rate
σ	standard deviation
t_{MDT}	TimingMaster delay tolerance
t_{UI}	unit interval
ρ_{BR}	bit rate
T_A	ambient temperature
V_{OH}	output high voltage
V_{OL}	output low voltage

4.2 Abbreviated terms

AC	alternating current
AFE	analogue frontend
BEC	balanced media to electrical converter
BM	balanced media
BPF	bits per frame
bPHY	balanced media physical layer
BR	bit rate
BTR	balanced media transceiver
DC	direct current
DCA	DC adaptive
DDJ	data-dependent jitter
DLL	data link layer
DSV	digital sum value

EBC   electrical to balanced media converter

ECU   electronic control unit

EMC   electromagnetic compatibility

EMI   electromagnetic interference

MNC   MOST network controller

PCB   printed circuit board

PDF   probability density function

PHY   physical layer

PLL   phase locked loop

PSD   power spectrum density

RBW   resolution bandwidth

RL   return loss

RMS   root mean square

Rx data   encoded digital bit stream being received

SP[n]   specification point

Tx data   encoded digital bit stream being transmitted

UI   unit interval

5   Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[3].

6   Physical layer service interface to OSI data link layer

6.1   Overview

The physical layer (PHY) service interface specifies the abstract interface to the OSI data link layer (DLL), see ISO 21806-6[4].

6.2   Data type definitions

The data type Enum is defined as an 8-bit enumeration.

6.3   Event indications and action requests

6.3.1   P_EVENT.INDICATE

The PHY shall use P_EVENT.INDICATE to indicate the occurrence of an event to the DLL.

```
P_EVENT.INDICATE{
    PHY_Event
}
```

     3

6.3.2   P_ACTION.REQUEST

`P_ACTION.REQUEST` shall trigger the execution of a request.

```
P_ACTION.REQUEST {
    PHY_Request
}
```

6.4   Parameters

6.4.1   PHY_Event

Table 1 specifies the `PHY_Event` parameter, which notifies the DLL about events.

Table 1 — Parameter passed from PHY to DLL

Parameter	Data type	Description

`PHY_Event`	`Enum {`
	
	`    PHY_Output_Off,`
	
	`    PHY_Network_Activity`
	
	`}`
		An event that is reported to the DLL.

Table 2 specifies the parameter values for the `PHY_Event` Enum.

Table 2 — PHY_Event Enum values

Enum value	Description
`PHY_Output_Off`	MNC transmit terminal is switched off.
`PHY_Network_Activity`	Network activity is detected at the MNC receive terminal.

6.4.2   PHY_Request

Table 3 specifies the `PHY_Request` parameter, which is passed from DLL to PHY.

Table 3 — Parameter passed from DLL to PHY

Parameter	Data type	Description

`PHY_Request`	`Enum {`
	
	`    cmd_Output_Off,`
	
	`    cmd_Output_On,`
	
	`    cmd_Open_Bypass,`
	
	`}`
		A request from the DLL

Table 4 specifies the parameter values for the `PHY_Request` Enum.

Table 4 — PHY_Request Enum values

Enum value	Description
`cmd_Output_Off`	Switching off the MNC transmit terminal is requested. By default, it is off.
`cmd_Output_On`	Switching on the MNC transmit terminal is requested. By default, it is off.
`cmd_Open_Bypass`	Opening the bypass is requested. By default, the bypass is closed.

7 Basic physical layer requirements

7.1 Logic terminology

7.1.1 Single-ended low-voltage digital signals

For the parameters provided in JEDEC No. JESD8C.01, Table 5 defines the corresponding terms for single-ended signals used in this document. These terms are used to describe the logic states of signals /RST and STATUS.

Table 5 — Terms for single-ended signals

Term	Corresponding JEDEC parameter
Low	V_{OL} (output low voltage)
Logic 0	
High	V_{OH} (output high voltage)
Logic 1	

7.1.2 Differential signals

Table 6 explains the expressions used to describe the logic states of the differential data signals.

Table 6 — Differential signals

Expression	Description
Disabled	The P and N terminals are in a high impedance state. Small leakage currents may exist which can cause an indeterminate voltage on the line/load.
Off	
Enabled	Both the P and N terminals are driving the line / load. The outputs may be in a transitioning phase or in the process to settle differential amplitude as well as common mode. The defined link quality parameter requirements may not be met.
On	
Valid MOST data	DCA encoded data that meets defined link quality parameters and bit rate requirements.

7.2 SPs

A physical connection of two MOST devices is called a link. Measurements are taken at specific locations along a link. These locations are called SPs. The location of the SPs is shown in Figure 3.

Key
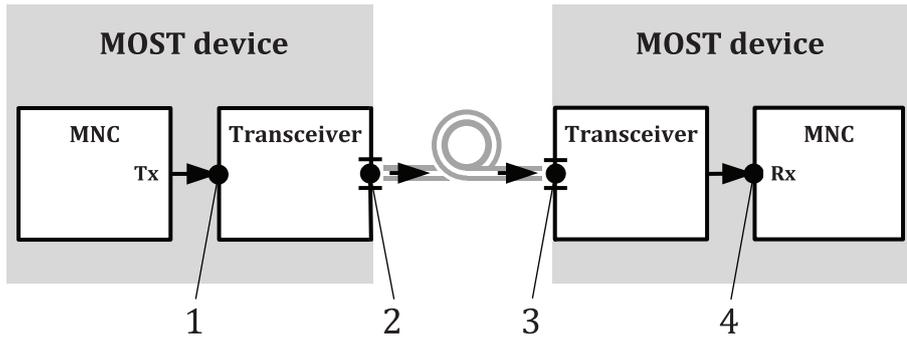
1   SP1

2   SP2

3   SP3

4   SP4

Figure 3 — Location of SPs along a link

SPs define interfaces that are boundaries between a transmitting and a receiving MOST component. For each of those interfaces, a set of requirements and properties is defined (e.g. signal timing, signal amplitude, connector interface drawings). SP1 and SP4 are located between a MOST network controller (MNC) and the corresponding transceiver. SP2 and SP3 are located between transceivers and a wiring harness.

For MOST components that are located between two adjacent SPs, requirements and properties can be derived. The definitions of the second SP of the pair specify the component's output performance to be achieved, considering input conditions as defined in the first SP. For example, a transmit converter component specification can be derived from SP1 and SP2. Receive converter component requirements are covered by SP3 and SP4. Wiring harness requirements can be derived from SP2 and SP3.

In addition to the definitions of the SPs for a point-to-point link, this document defines requirements covering the stability of the MOST network. Examples are requirements regarding jitter transfer through MOST devices, jitter accumulation through the MOST network, and power state transitions.

The specified parameters in this document are minimum values to ensure functionality of the MOST network in a wide range of environmental conditions.

7.3   Phase variation

7.3.1   General

Data stream timing and distortion cause phase variation.

7.3.2   Wander

Wander consists of any phase variation from 0 Hz to 10 Hz. All active MOST components in the MOST network create wander. Wander is a function of the temperature drift and propagates from node to node. Typically, wander does not affect alignment jitter eye masks.

NOTE   It is possible that wander impacts the TimingMaster.

7.3.3   Jitter

Jitter is any phase variation of frequencies above 10 Hz. Every MOST component and the transmission medium create jitter in the MOST network. Jitter is correlated or uncorrelated. The dominant jitter sources in the MOST network consist of PLL noise, link-induced DDJ, sensitivity-induced BEC noise,

crosstalk, or phenomena such as power supply coupling. Data scrambling is used to eliminate DDJ correlation between nodes.

There are two jitter categories as shown in Figure 4.

— Alignment jitter: jitter that affects the reception of data by degrading the receiver eye diagram with horizontal closure (influences eye diagram measurement); it has impact only on a link as data recovery is performed by the MNC.

— Transferred jitter: jitter that is accumulated over all links (does not influence eye diagram measurement); the TimingMaster jitter tolerance shall be determined accordingly.

As the jitter on the measured signal increases, the eye closes more and more. A keep-out mask is specified to detect possible error traces. If the eye does not hit the mask then data recovery is ensured. Mask design depends on the required receiver margin and the characteristics of the channel.

Figure 4 shows the phase variation measurements.
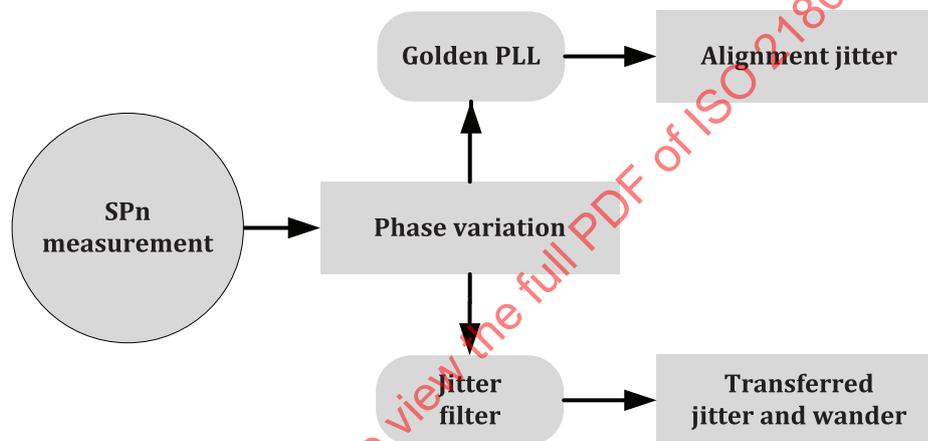
Figure 4 — Phase variation measurements

7.3.4   Clock recovery and reference clock

7.3.4.1   General

Phase variation can be measured directly on a data stream. To view alignment jitter and transferred jitter independently, special tools are required.

All MOST networks contain one device that implements the TimingMaster, which creates the reference clock. This clock is embedded within the data stream. All other MOST devices contain TimingSlaves that recover the clock from the data stream. Therefore, clock recovery is a basic functionality of an MNC. MOST components add phase variation to the data stream. This degrades the reference clock.

Receiver jitter tolerance and jitter transfer are basic operation properties of any MNC. Alignment jitter is measured by means of an eye diagram formed with a Golden PLL. Transferred jitter is measured with a jitter filter.

Figure 5 illustrates clock recovery and data recovery in an MNC. Therefore, there is a need for a Golden PLL model and a jitter filter model. Together they reflect the required jitter behaviour of an MNC.

Figure 5 — Clock and data recovery example

7.3.4.2 Golden PLL

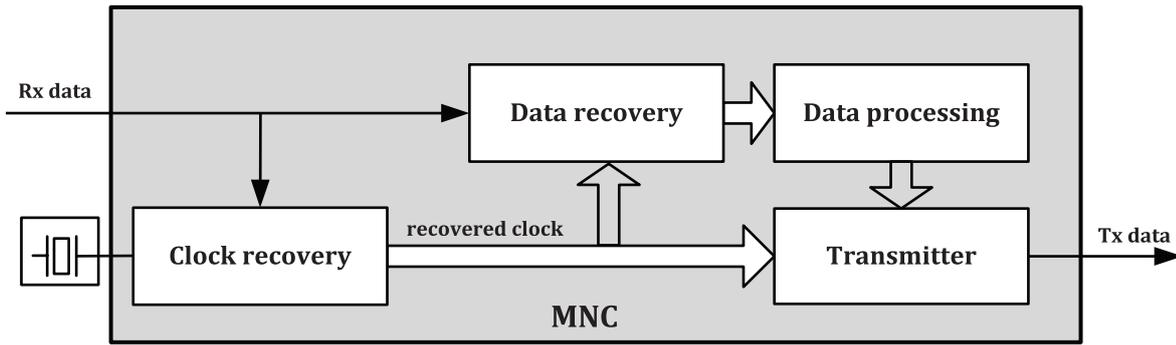The Golden PLL is a simplified model which represents the behaviour of the MNC when jitter is applied to its input. A Golden PLL can be constructed out of hardware or software, but shall obtain data from the SP and output a clock at the UI frequency for eye-diagram formation.

7.3.4.3 Jitter filter

The jitter filter is a simplified model which represents the worst-case MNC jitter transfer function. A jitter filter can be constructed out of hardware or software but shall obtain data from the SP and output the RMS value of the transferred jitter at the SP.

7.3.5 Link quality

7.3.5.1 General

Link quality describes the minimum performance of MOST components along a single link.

7.3.5.2 Alignment jitter

Link quality eye diagrams are used to specify and measure link operation and MOST network level performance. A jitter budget is created top down starting from SP4. The difference between the SPs gives the tolerable contribution of alignment jitter for the respective MOST component or transmission medium. As an example, link quality eyes can be required at every point along the link to allow each MOST component's alignment jitter contribution to be specified. Figure 6 shows an example of the eye diagrams that correspond to the SPs in a link.

Key
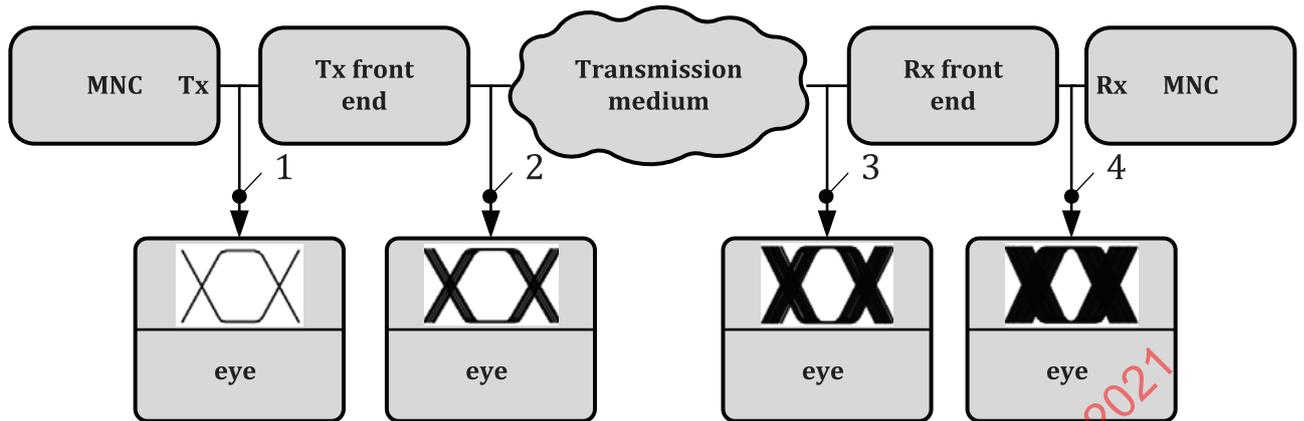
1 SP1
2 SP2
3 SP3
4 SP4

Figure 6 — Illustration of eye diagrams at SPs in a link

7.3.5.3 Transferred jitter

A portion of every jitter source in the MOST network has some spectral content below the jitter filter bandwidth. Jitter passed by the filter accumulates in the following nodes. Transferred jitter from all sources combines to form accumulated jitter in the network, starting with the first TimingSlave, accumulated jitter increases. Therefore, the total jitter at SP4 of the last MNC in the network consists of the total jitter generated in the final link and the accumulated jitter from all the links before. Transferred jitter is measured by filtering the phase variation at any SPn with a jitter filter. The RMS (standard deviation) of the output of this jitter filter is the amount of jitter contributed to accumulated jitter. Transferred jitter specifications are placed at every SP as shown in Figure 7.

Key
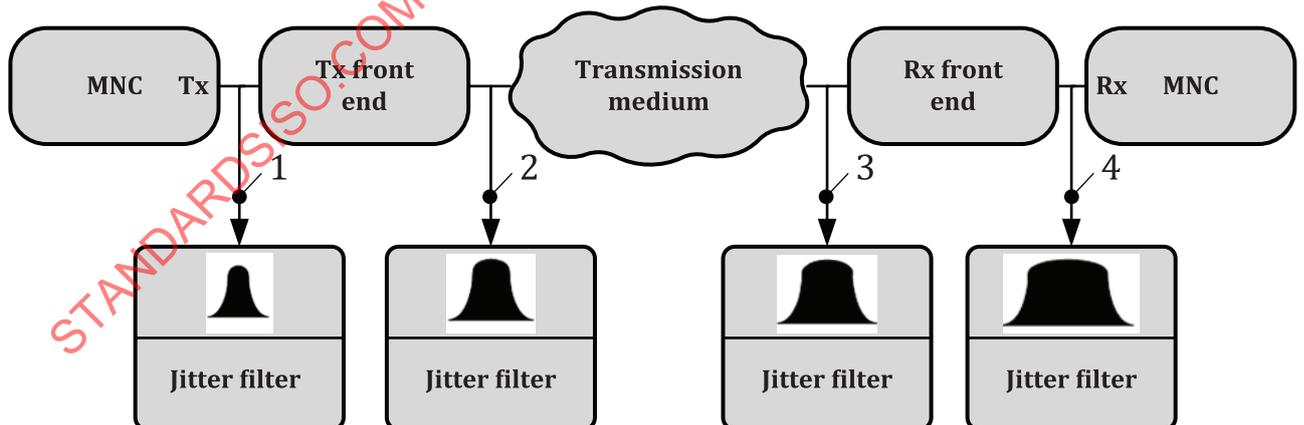
1 SP1
2 SP2
3 SP3
4 SP4

Figure 7 — Illustration of transferred jitter accumulation at various SPs in a link

7.3.6 MOST network quality

7.3.6.1 Receiver tolerance

Receiver tolerance describes the minimum alignment jitter tolerance of an MNC and the maximum tolerable alignment jitter that may occur at any place in the MOST network.

The minimum and maximum limits of the eye mask define the receiver tolerance. The closure of the eye mask originates from accumulated jitter in the MOST network. An MNC recovers all signals that fit into the SP4 receiver tolerance mask. A MOST device recovers all signals that satisfy the SP3 link quality requirements.

Figure 8 shows the typical SPs in a ring where the SP4 receiver tolerance limits can be applied as a test of MOST network performance.
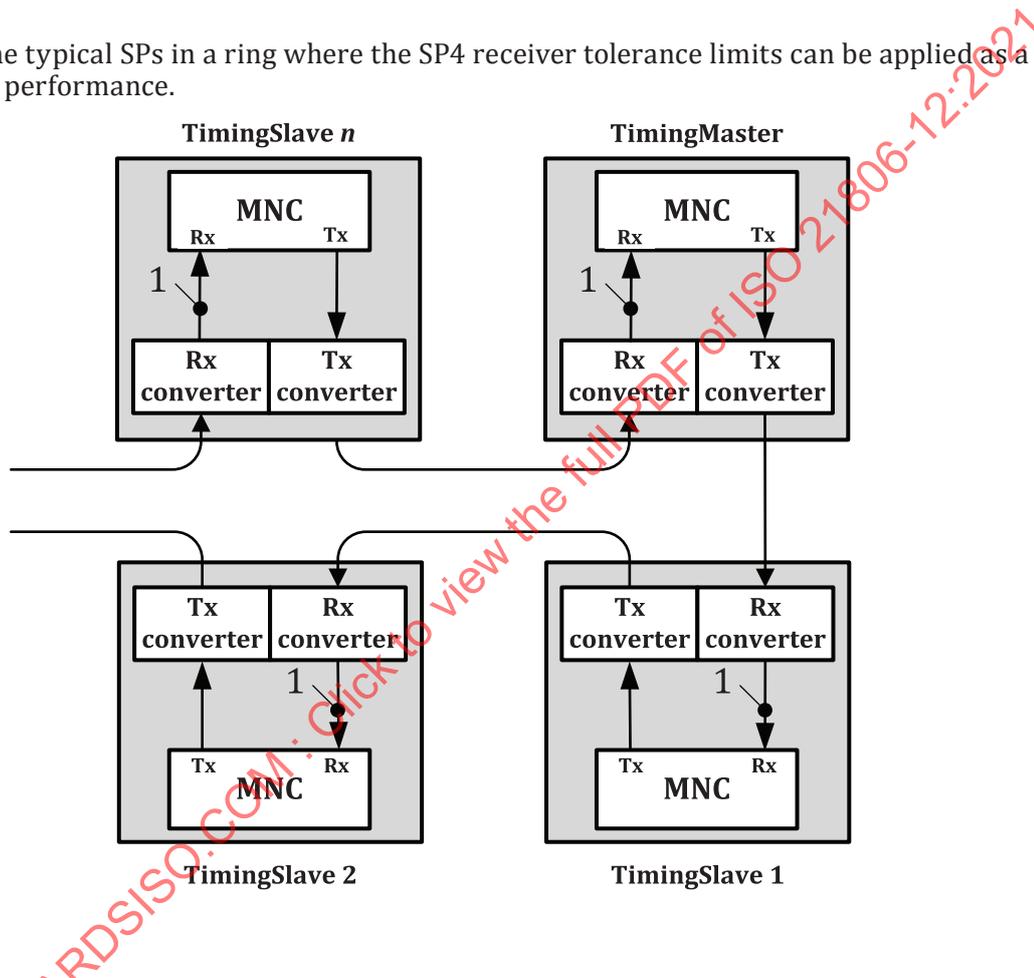
Key
1   SP4

Figure 8 — Locations where receiver tolerance eye mask can be applied

7.3.6.2 TimingMaster delay tolerance

The MOST network stability is determined by the ability of the TimingMaster node to tolerate the accumulated delay present at the end of the ring. TimingMaster delay tolerance is the maximum amount of accumulated delay for an MNC that is configured as TimingMaster.

TimingMaster delay tolerance is tied to the delay, transferred jitter, transferred wander and maximum node count.

Formula (1) defines the minimum for the TimingMaster delay tolerance (t_{MDT}). The relevance of the delay respectively different types of phase variation on the accumulate delay is shown in Table 7.

$$t_{MDT} \geq t_D(M) + \sum_{n=1}^{m-1} t_D(n) + \sum_{n=0}^{m-1} t_W(n) + t_{D\,Medium} + \alpha \times \sqrt{\sum_{n=0}^{m-1} [t_{TJ}(n)]^2} \tag{1}$$

where

t_{MDT}	is the TimingMaster delay tolerance;
M	is the position of the TimingMaster;
m	is the number of nodes in the network;
n	is the position of the node in the network;
$t_D(M)$	is the delay of the TimingMaster node caused by Rx and Tx converter;
$t_{D\,Medium}$	is the total delay caused by the medium;
α	is a scaling factor that depends on the BER, see Table 7;
$t_D(n)$	is the delay of a TimingSlave node, see Table 7;
$t_W(n)$	is the wander (phase drift) of the node and link (peak-to-peak);
$t_{TJ}(n)$	is the transferred jitter of the node (RMS) (i.e. $\alpha = 12$, derived from $\pm 6\sigma$ for BER = 10^{-9}).

Assumption

t_W	is correlated from node to node;
t_{TJ}	is uncorrelated from node to node.

Table 7 shows the purpose of the MOST network delay and jitter parameters that are combined in Formula (1).

Table 7 — MOST network delay and jitter variables

Variable	Formula	Description
Delay of TimingMaster node	(2)	$t_D(M)$ is the delay caused by Rx and Tx converter of the TimingMaster node.
Delay of a TimingSlave node	(3)	A MOST network operates properly if the TimingMaster complies with this formula.
Accumulation of delay of TimingSlave nodes	(4)	t_{DS} is the delay caused by the (m - 1) TimingSlave nodes. The delay per node is determined by the contribution of Rx converter, MNC, and Tx converter.
Delay of the medium	$t_{D\,Medium}$	It is the total delay caused by the medium (e.g. depending on the length of the medium in use).
Accumulation of wander	(5)	t_{W_SUM} is the accumulated wander of all nodes. Due to the low-frequency characteristic of wander, either most or all of this phase variation is transferred by a PLL. Wander is generated by all active MOST components of the link and by the MNC chip. Wander is most commonly caused by variations in temperature. It shall be specified in the data sheet of each active MOST component.

Table 7 *(continued)*

Variable	Formula	Description
Accumulation of transferred jitter	(6)	t_{TJ_SUM} is the accumulated transferred jitter of all nodes. Uncorrelated jitter sources add according to their variance. Scrambled data eliminates the correlation between DDJ on successive nodes. BEC noise and PLL noise sources are typically uncorrelated as well. This peak-to-peak number can be directly tied to a BER when the assumed jitter PDF is normal, e.g., $\alpha = 12$ in case of $\pm 6\ \sigma$ for BER = 10^{-9}.

$$t_{D}(M) = t_{D\,Rx}(M) + t_{D\,Tx}(M) \tag{2}$$

where

M is the position of the TimingMaster;

$t_{D}(M)$ is the delay of the node caused by Rx and Tx converter;

$t_{D\,Rx}(M)$ is the delay of the TimingMaster node caused by Rx converter;

$t_{D\,Tx}(M)$ is the delay of the TimingMaster node caused by Tx converter.

$$t_{D}(n) = t_{D\,Rx}(n) + t_{D\,MNC}(n) + t_{D\,Tx}(n) \tag{3}$$

where

n is the position of the node in the network;

$t_{D}(n)$ is the delay of a TimingSlave node, see Table 7;

$t_{D\,Rx}(n)$ is the delay of the node n caused by Rx converter;

$t_{D\,MNC}(n)$ is the delay of the node n caused by MNC;

$t_{D\,Tx}(n)$ is the delay of the node n caused by Tx converter.

$$t_{DS} = \sum_{n=1}^{m-1} t_{D}(n) \tag{4}$$

where

t_{DS} is the accumulated delay of the TimingSlave nodes;

$t_{D}(n)$ is the delay of a TimingSlave node;

n is the position of node in the network;

m is the number of nodes in the network.

$$t_{W\_SUM} = \sum_{n=0}^{m-1} t_W(n) \tag{5}$$

where

    t_{W_SUM} is the accumulated wander of all nodes;

    $t_W(n)$ is the wander (phase drift) per node and link (peak-to-peak);

    n is the position of node in the network;

    m is the number of nodes in the network.

$$t_{TJ\_SUM} = \alpha \times \sqrt{\sum_{n=0}^{m-1} [t_{TJ}(n)]^2} \tag{6}$$

where

    t_{TJ_SUM} is the accumulated transferred jitter of all nodes;

    $t_{TJ}(n)$ is the transferred jitter per node (RMS) (i.e. $\alpha = 12$, derived from $\pm 6\,\sigma$ for BER = 10^{-9});

    n is the position of node in the network;

    m is the number of nodes in the network.

8 MOST50 bPHY requirements

8.1 General MOST network parameters

8.1.1 MOST network coding

8.1.1.1 General

The following subclauses describe a technique of encoding digital data called DCA coding, which shall be used in MOST50 bPHY.

8.1.1.2 Pulse characteristics

The MOST50 bPHY signal is scrambled and encoded using DCA coding. Data pulses range from 2 UI to 6 UI, yielding five different pulse widths, as shown in Figure 9.
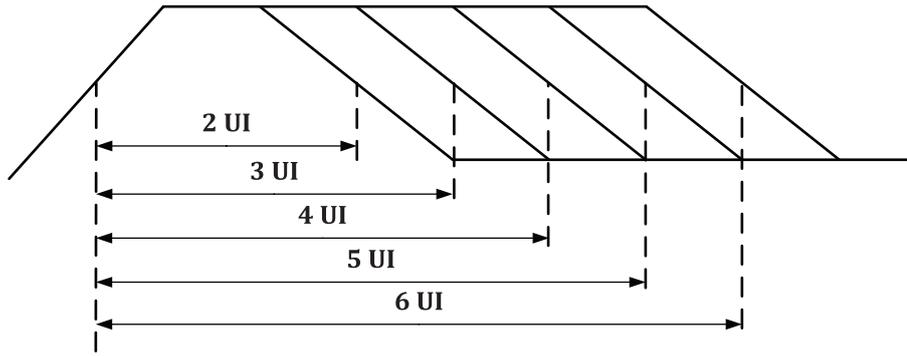
Figure 9 — Allowable pulse widths when using DCA coding

8.1.1.3 Unit interval definition

The unit interval (UI) width calculation is specified in Formula (7).

For MOST50 bPHY, there are 1 024 bits per frame (N_{BPF}). Using Formula (7) for a frame rate of 48 kHz results in a UI of 10,173 ns.

$$t_{UI} = \frac{1}{\rho_{Fs} \times 2 \times N_{BPF}}$$ (7)

where

t_{UI} is the unit interval (UI);

ρ_{Fs} is the network frame rate;

N_{BPF} is the bits per frame.

8.1.1.4 DC balance

DCA coding ensures absence of DC. Short-term imbalances in offset occur during data transmission. These imbalances are tracked with a running total called the digital sum value (DSV). The DSV is calculated by incrementing the sum for every UI where the level is logic 1 and decrementing the sum for every UI where the level is logic 0. The calculation for DSV is illustrated in Figure 10.

Dynamic properties of DCA coding:

— the DSV is periodically driven to logic 0 at least once per frame;

— the range of DSV values in a valid DCA stream are {-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5};

— the shortest DCA period is 4 UI;

— the longest DCA period is 10 UI;

— the data stream shall have a period of 10 UI at least once per frame. These 10 UI periods can either be made of pulses that are 4 UI high/low with 6 UI low/high, 6 UI high/low with 4 UI low/high, or 5 UI high/low with 5 UI low/high.

Figure 10 shows the DSV calculation.
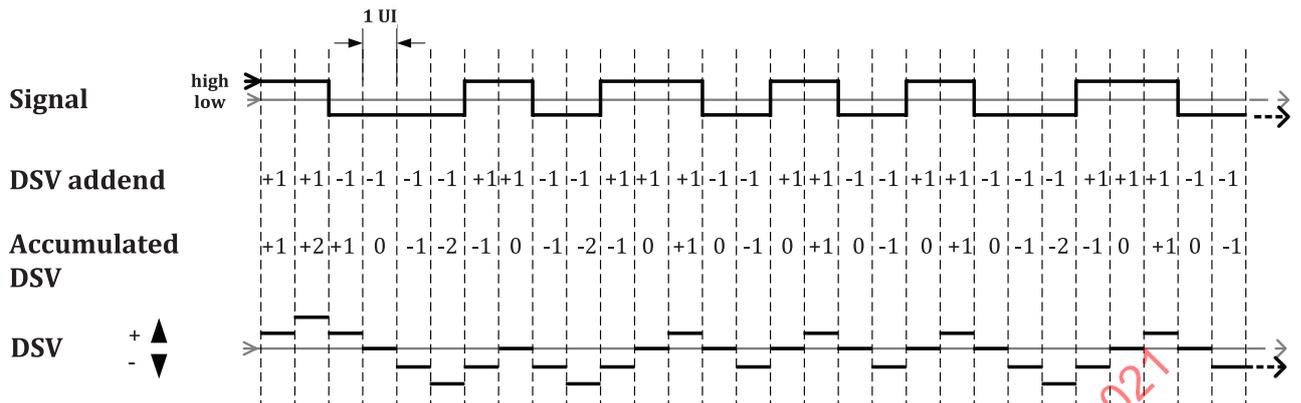
Figure 10 — DSV calculation

8.1.2   Link and interconnect type

MOST50 bPHY shall use automotive-grade balanced twisted pair cables and automotive-grade balanced connectors. The interconnect shall be end-terminated by 100 Ω.

The system supports separate interconnects for transmit and receive links. The communication is unidirectional using two separate ports and cables per node.

8.1.3   SP details

Table 8 defines the SP locations and interfaces.

Table 8 — SP locations and interfaces for integrated transceivers

Specification Point	Location	Interface
SP2[a]	Signal at transmit port of balanced media interface	analogue
SP3[a]	Signal at receive port of balanced media interface	analogue
[a] See Figure 11.		

Figure 11 shows the location of SPs.

Key
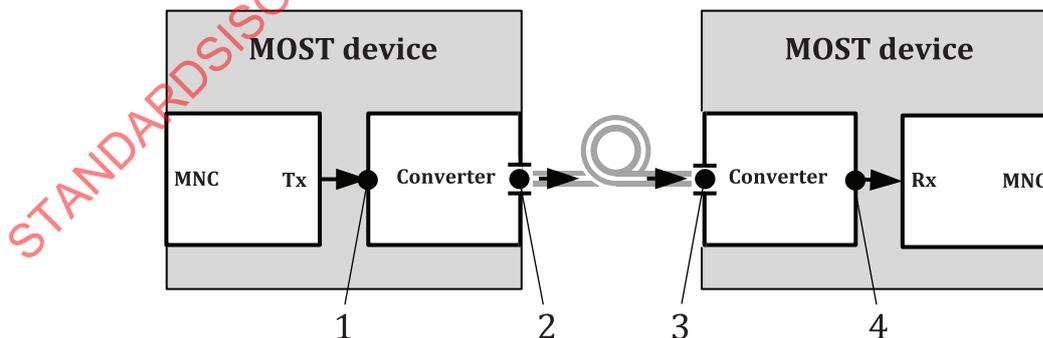
1   SP1
2   SP2
3   SP3
4   SP4

Figure 11 — General location of SPs

Systems that implement the MOST50 bPHY also implement components that convert electrical digital signals into differential signals, optimized for feeding into balanced media, and vice versa. They are called EBC (electrical to balanced media converter) and BEC (balanced media to electrical converter). There is also an important section between transceiver pins and balanced media connector, containing further passive circuitry, which is called analogue frontend (AFE).

For an optimized infrastructure, EBC and BEC are assumed to be integrated in the MNC. Inside the chip, the converter portions are connected with the MNC Tx/Rx section. In consequence, SP1 and SP4 are moving inside the MNC. There is no direct access possible. Therefore, this document omits definitions of SP1 and SP4 and instead focuses on SP2 and SP3.

Suppliers of MNCs are responsible for specifying their product's signal characteristics at the chip IOs, EBC Tx and EBC Rx, and suggest AFEs, which allow implementers to achieve the MOST requirements for SP2 and SP3.

Figure 12 illustrates a MOST50 bPHY interconnect. SP1, SP2, SP3, and SP4 indicate the forward signal path.

Key

1   Tx: MNC transmit terminal
2   SP2
3   SP3
4   Rx: MNC receive terminal
5   in-line connectors
6   channel, balanced media

Figure 12 — Location of SPs

Table 9 describes the SP locations and interfaces for integrated transceivers
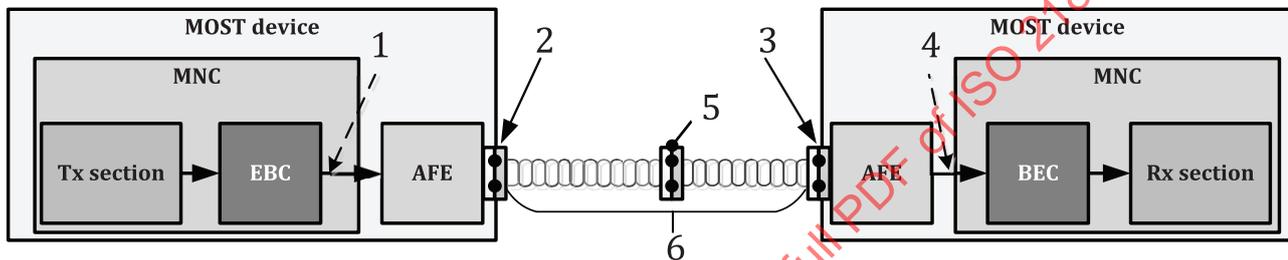
Table 9 — SP locations and interfaces for integrated transceivers

Specification Point	Location	Interface
SP2	Signal at transmit port of balanced media interface	analogue
SP3	Signal at receive port of balanced media interface	analogue

8.1.4   Analogue frontend

Suppliers of MNCs with balanced media transceivers provide a connection scheme that meets the requirements for connection and layout of the transceivers with balanced media connector, including passive components.

Required properties for AFE and associated characteristics depend on properties of individual transceiver designs (e.g. termination, band filter, common mode rejection).

NOTE   With the supplier product definition on EBC Tx and BEC Rx in combination with a suggested AFE, it is possible to meet the SP2 requirements.

8.2 Models and measurement methods

8.2.1 Golden PLL

The Golden PLL determines the required worst-case jitter performance of an MNC and is used to form receiver eye diagrams. The positive edge of the signal shall trigger the Golden PLL. The transfer function is a low-pass filter with unity gain at 0 Hz.

NOTE   For practicality of measurements, the transfer function is specified for 10 Hz and above.

Figure 13 shows the Golden PLL transfer function.
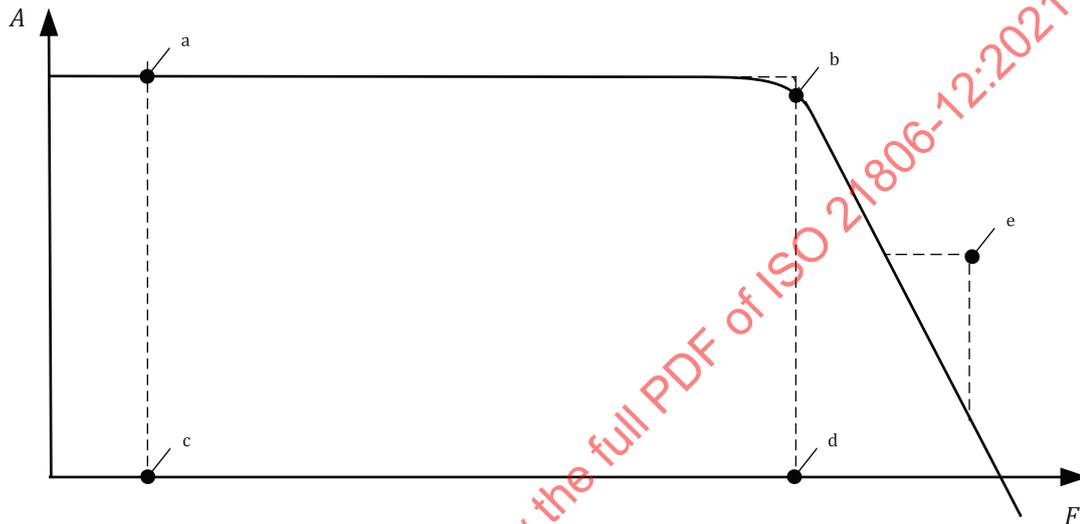
Key

a A_{P0}: amplitude point 0.

b A_{P1}: amplitude point 1.

c F_{P0}: frequency point 0.

d F_{P1}: frequency point 1.

e   Slope.

A   attenuation

F   frequency [Hz], logarithmic scale

Figure 13 — Golden PLL transfer function

Table 10 specifies the Golden PLL parameters.

Table 10 — Golden PLL parameters

Y	Value	Unit
A_{P0}	0	dB
F_{P0}	10	Hz
A_{P1}	-3	dB
F_{P1}	62,5	kHz
Slope	-20	dB/dec

8.2.2 Jitter filter

The jitter filter describes the worst-case jitter transfer function of an MNC and is used to calculate transferred jitter along the link. The transfer function is a low-pass filter with unity gain at 0 Hz.

NOTE   For practicality of measurements, the transfer function is specified for 10 Hz and above.

The jitter filter shall reference to the positive edge of the signal.

Figure 14 shows the jitter filter response.
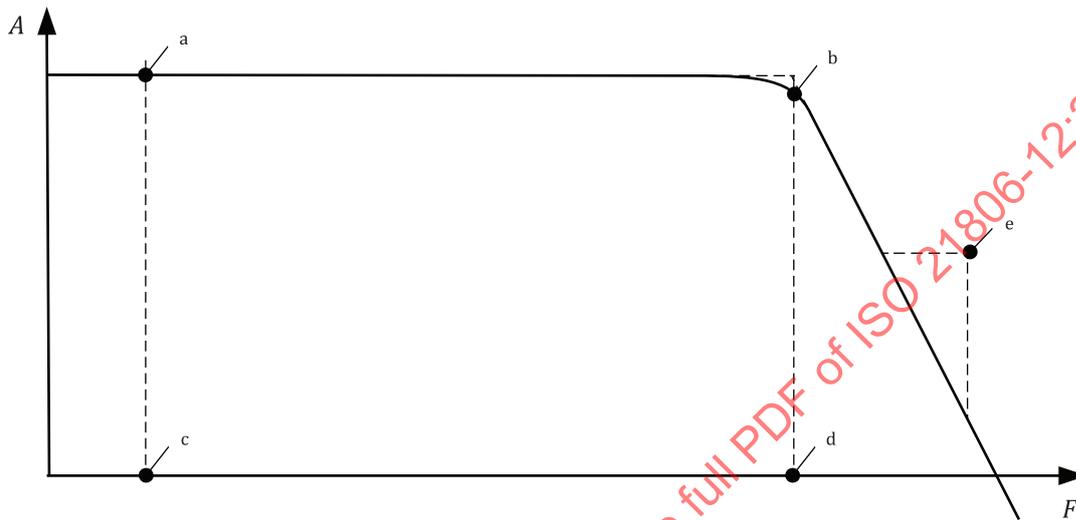
Key

a A_{J0}: amplitude point 0.

b A_{J1}: amplitude point 1.

c F_{J0}: frequency point 0.

d F_{J1}: frequency point 1.

e   Slope.

A attenuation

F frequency [Hz], logarithmic scale

Figure 14 — Jitter filter response

Table 11 defines the jitter filter specifications.

Table 11 — Jitter filter specifications

Parameter	Value	Unit
A_{J0}	0	dB
F_{J0}	10	Hz
A_{J1}	-3	dB
F_{J1}	100	kHz
Slope	-20	dB/dec

8.2.3 Stress pattern

The MOST50 bPHY stress pattern shall be used for:

— signal level detection, and

18

— all eye diagrams.

Table 12 defines the reference of the MOST50 bPHY stress pattern.

Table 12 — MOST50 bPHY stress pattern reference

Item	Item reference
Description code	MOST50 bPHY stress pattern
Filename	MOST50_Stress_Pattern-1v0.pat
Access location	ISO 21806-1:2020, Annex A
ZIP archive	MOST50_bPHY_Specification_1V0-0.zip

The MOST50 bPHY PSD pattern shall be used for PSD measurements.

Table 13 defines the reference of the MOST50 bPHY PSD pattern.

Table 13 — MOST50 bPHY PSD pattern reference

Item	Item reference
Description code	MOST50 bPHY PSD pattern
Filename	MOST50_PSD_Pattern-1v0.pat
Access location	ISO 21806-1:2020, Annex A
ZIP archive	MOST50_bPHY_Specification_1V0-0.zip

9 Link specifications

9.1 General

Different methods of validating characteristics of the serial data link exist.

The power spectrum density (PSD) method is used to evaluate the spectral content of a transmitted signal. A PSD mask specifies limits in the frequency domain. The PSD mask also limits minimum and maximum signal power.

For jitter and pulse shape evaluation, this document specifies eye diagrams. A large eye opening indicates a signal with low jitter and distortion. The eye diagram is specified such that a valid signal does not overlap the eye mask. A signal that overlaps the eye mask does not meet the requirements. Signals with slow rise times, low amplitude, jitter, or pulse width variations are represented by closures in the eye diagram.

All MOST components along the link shall operate with a BER lower than 10^{-9}.

9.2 SP2

The signal at SP2 shall meet the requirements in Table 14 and shall remain outside the keep-out area of the eye mask. Refer to 10.1, 11.3 and Clause 12 for operating conditions and interface specifications.

The PSD of the SP2 signal shall remain between the upper and the lower limit of the PSD mask in Table 16.

All parameters are evaluated using specified MOST50 bPHY stress pattern.

The signal at SP2 is an AC waveform and may be accompanied by a DC offset, especially when transporting power along with the data over the balanced media interconnect/channel. In this instance, the DC offset shall be eliminated before evaluating the signal. For Table 14, the DC value is assumed to be 0 V.

Table 14 — Link quality parameters of SP2

Link quality parameters of SP2	Condition	Symbol	Minimum	Typical	Maximum	Unit
RMS signal amplitude (using MOST50 bPHY stress pattern or MOST50 PSD pattern)	Cd4[d], Cd6[f]	V_{RMS2}	360	---	830	mV
Transferred jitter (RMS) (using MOST50 bPHY stress pattern)	Cd1[a], Cd6[f]	J_{tr2}	---	---	112	ps
Eye mask (see Figure 15) (using MOST50 bPHY stress pattern)	Cd2[b], Cd3[c], Cd5[e], Cd6[f]	A_2 to D_2	---	---	---	---
PSD mask (see Figure 16) (using MOST50 PSD pattern)	Cd7[g], Cd8[h]	U1 to U7 L1 to L4	---	---	---	dBm/Hz

[a]   Use the jitter filter as specified in 8.2.2.

[b]   Use the Golden PLL as specified in 8.2.1.

[c]   The DC offset is eliminated.

[d]   The minimum value considers the maximum attenuation of the AFE. The maximum value considers a non-zero AFE attenuation.

[e]   The mask amplitude parameters include tolerances for overshoot and ringing.

[f]   SP2 terminated with nominal impedance 100 Ω.

[g]   Averaged to achieve an effective RBW of 500 kHz.

[h]   The discrete power values forming the PSD are equivalent to the differential signal amplitude measured at 100 Ω. The accumulated power of the PSD corresponds to $V_{RMS2}^2/100$ Ω.
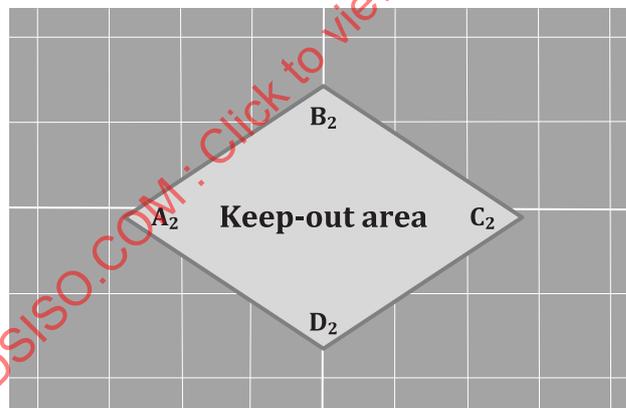
Key

A_2, B_2, C_2, and D_2 link quality parameters of SP2; see Table 15

Figure 15 — Link quality parameters of SP2 - Eye mask

Table 15 defines the link quality parameters of SP2 for the eye mask.

Table 15 — Link quality parameters of SP2 - Eye mask

Parameter [Key]	Amplitude [mV]	Timing [UI]
A_2	0	0,150
B_2	230	0,500
C_2	0	0,850

Table 15 *(continued)*

Parameter [Key]	Amplitude [mV]	Timing [UI]
D_2	230	0,500

Table 16 defines the upper and lower limits of the PSD mask.

Table 16 — Upper and lower limits of the PSD mask

Symbol for upper limit	Frequency [MHz]	Limit [dBm/Hz]	Symbol for lower limit	Frequency [MHz]	Limit [dBm/Hz]
U1	1	-75,0	L1	4	-81,0
U2	8	-66,0	L2	8	-81,0
U3	14	-59,0	L3	15	-74,0
U4	20	-59,0	L4	30	-87,0
U5	60	-80,0	---	---	---
U6	100	-80,0	---	---	---
U7	≥250	-113,0	---	---	---

Figure 16 shows the link quality parameters of SP2, PSD mask.
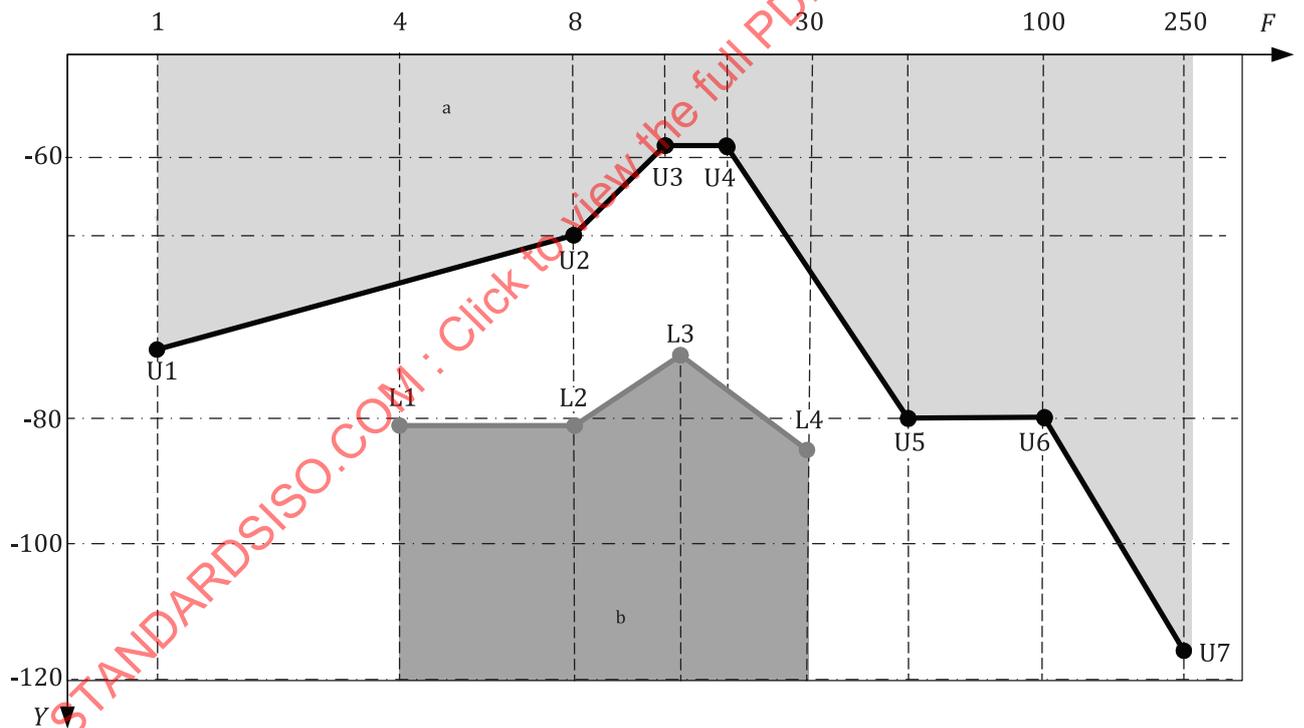
Key

a	PSD upper mask.
b	PSD lower mask.
F	frequency [MHz]
Y	PSD [dBm/Hz]
U1 to U7	upper limit of the PSD mask; see Table 16
L1 to L4	lower limit of the PSD mask; see Table 16

NOTE   Grey areas are "keep out" areas.

Figure 16 — Link quality parameters of SP2 – PSD mask

9.3 Electrical link requirements

9.3.1 General

This document defines the usage of differential characteristic impedance of 100 Ω balanced media cable and connectors. All measurements are defined using a differential 100 Ω termination.

MOST50 bPHY tolerates deviation from 100 Ω. For better interface matching, characteristic impedance centred with an offset to ideal 100 Ω may be used.

9.3.2 Electrical interconnect, length and attenuation

The balanced media interconnect parameter requirements and the maximum interconnect length are specified in Table 17. This length includes the balanced media cables and the connectors (device and in-line). A limitation on the number of in-line connectors is not required as long as the whole interconnect conforms to the specifications as specified in Table 17. Attenuation losses of balanced media interconnect shall not exceed limits given by the attenuation limit curve in dB.

Table 17 — Balanced media interconnect attenuation parameters

Parameter	Condition	Symbol	Minimum	Typical	Maximum	Unit
Balanced media interconnect length	Cd1[a]	---	0	---	15	m
Attenuation limit	1 MHz to 66 MHz	$A_{\text{Limit}}(F)$	---	---	---	---
	See Formula (8).					
[a] Parameter variations occur due to environmental conditions or mechanical stress being applied to the balanced media interconnect.						

Formula (8) expresses the attenuation versus frequency (in dB) for a balanced media interconnect.

$$A(F) = -0{,}30335 - \sqrt{\frac{F}{2{,}2795 \times 10^6}} - 2{,}31979 \times 10^{-8} \times F \tag{8}$$

where

$\quad A \quad$ is the attenuation;

$\quad F \quad$ is the frequency.

Figure 17 shows the attenuation limit.

Key

ᵃ   1 MHz / -1,0 dB.

ᵇ   10 MHz / -2,6 dB.

ᶜ   33 MHz / -4,9 dB.

ᵈ   66 MHz / -7,2 dB.

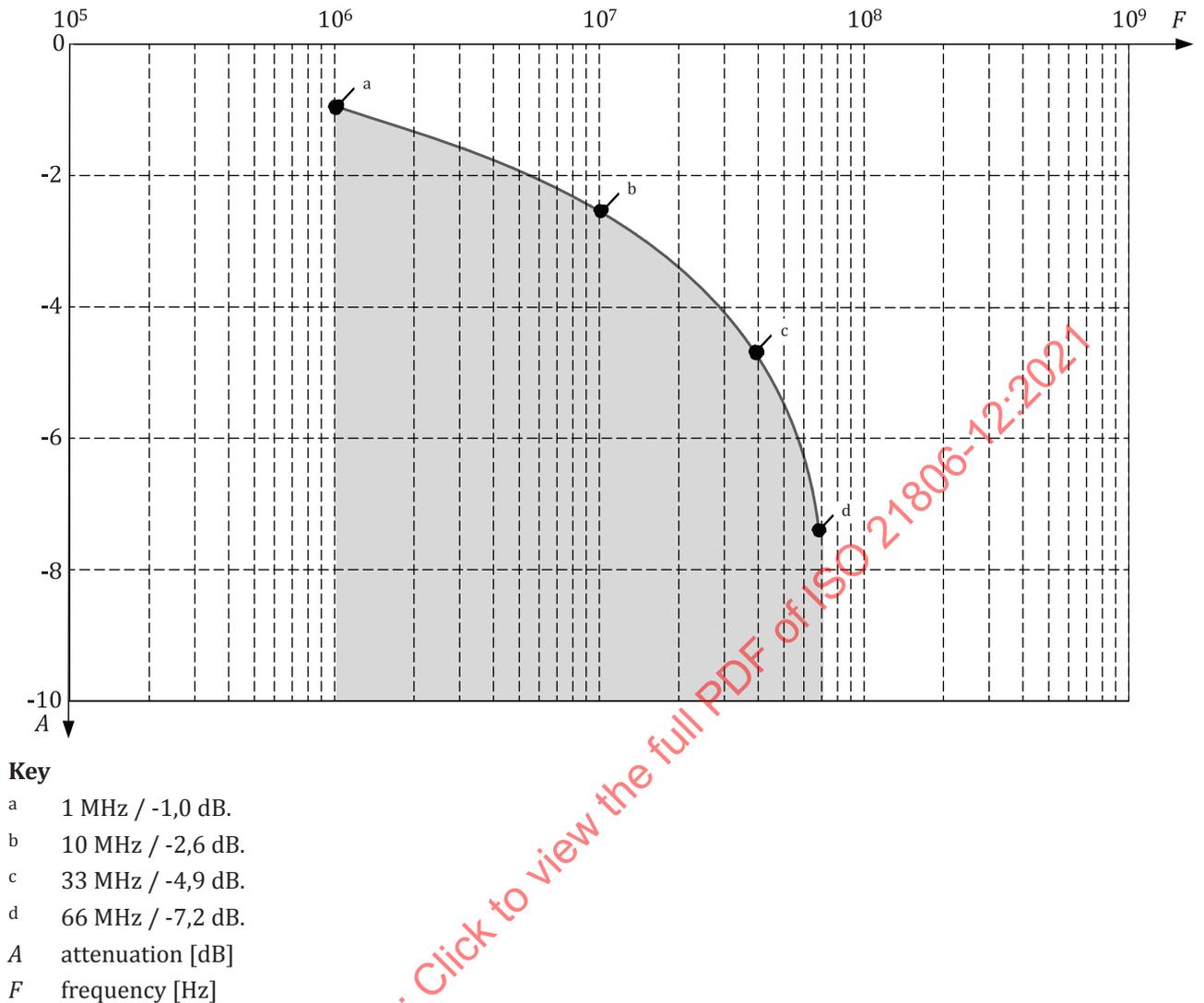A attenuation [dB]

F frequency [Hz]

Figure 17 — Attenuation limit

Insertion loss considers all kind of losses that occur on an interconnect between SP2 and SP3. This includes losses due to dissipation, radiation, reflection and mode conversion. In the relevant frequency range, connector insertion losses are negligible.

9.3.3   Characteristic impedance and return loss (RL)

9.3.3.1   General

In 9.3.3.2 to 9.3.3.3 requirements are specified for characteristic impedance of components forming a balanced media link and for AFE circuitry connecting to such interconnects. Impedance mismatches cause back reflection of a certain portion of the signal energy. The ratio of reflected signal relative to transmitted signal is called RL. The definition of characteristic impedance is either given as impedance [Ω] or as RL [dB], whatever is better suited for component.

In simplex operation, RL on a transmit path means a minor reduction of signal amplitude in transmit direction. Such losses are already included in the following.

— Output signal specification:

This covers amplitude reduction due to return losses inside the ECU, caused by an interface impedance mismatch to nominal differential characteristic impedance (100 Ω) of the standard measurement equipment.

— Attenuation requirements (see Table 17) for balanced media interconnects:

The measurement of attenuation inherently includes all losses. Therefore, it includes return losses caused by impedance mismatches within segments of a balanced media interconnect (channel) and by mismatches of the balanced media interconnects to nominal differential characteristic impedance (100 Ω) of the standard measurement equipment.

— Amplitude reduction due to return losses at receive interfaces (such as SP3), caused by mismatch of input impedance is included in the receive tolerance specification (see 11.1).

9.3.3.2   Electrical interconnect, characteristic impedance and RL

Table 18 specifies the balanced media interconnect characteristic impedance between SP2 and SP3.

Table 18 — Balanced media interconnect characteristic impedance and RL parameters

| Parameters	Condition	Symbol	Minimum	Typical	Maximum	Unit
Characteristic impedance of cable	Cd1[a]	Z_{0cable}	90	100	140	Ω
[a] Environmental conditions or mechanical stress being applied to the balanced media interconnect lead to parameter variations.						

9.3.3.3   PCB interfaces, characteristic impedance and RL

Balanced media interconnects are electrically connected to the balanced media transceivers on the PCB. Specification of SP2 already includes EBC output characteristic and potential losses due to board traces, passive components and board connector. SP3 represents signal characteristic at the end of a balanced media interconnect, terminated with the optimum value of 100 Ω. Potential signal degradation due to board traces, passive components and board connector between SP3 and BEC-input shall be considered additionally. The entity of board traces, passive components and board connector is summarized under the term analogue front end AFE. In some cases, the length of the electrical connection between device connector and the BEC/EBC might be long enough to adversely affect the signal integrity.

Table 19 specifies the PCB interface impedance and RL parameters.

Table 19 — PCB interface impedance and RL parameters

Parameters	Condition	Symbol	Minimum	Typical	Maximum	Unit
RL of ECU-Interface, measured at device connector	A, B, C, D C1[a] , C2[b], C3[c]	L_{RL-SP2} L_{RL_SP3}	---	---	≤ limit line	---
[a] Environmental conditions or mechanical stress lead to parameter variations. Refer to 10.1 and 11.3 for operating conditions.						
[b] The nominal characteristic impedance is 100 Ω.						
[c] The MNC shall provide test modes for RL evaluation.						
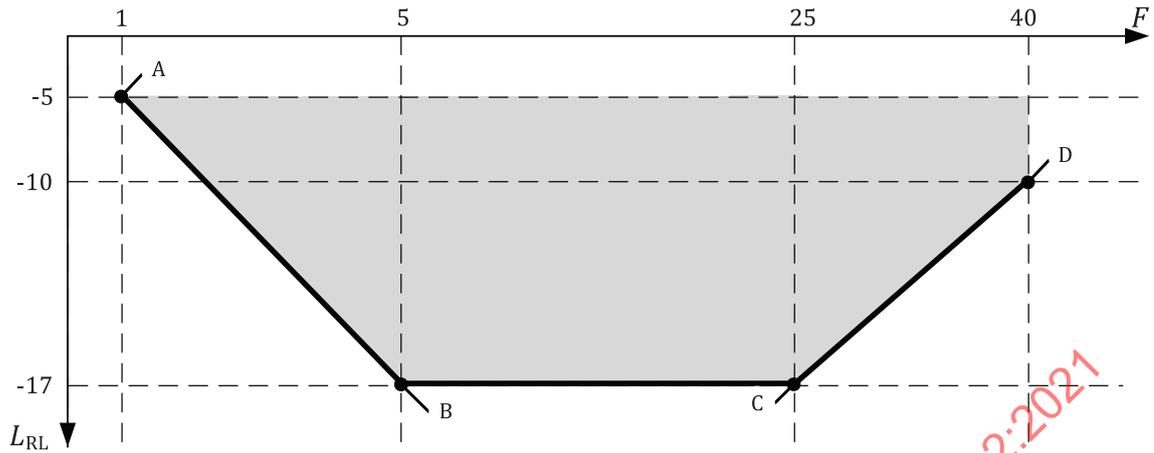
Key

A, B, C, and D	PCB interface impedance and RL parameters; see Table 20
F	frequency [MHz] logarithmic scale
L_{RL}	return loss [dB]

Figure 18 — PCB interface impedance and RL parameters – Limit line

Table 20 — PCB interface impedance and RL parameters – Limit line

Parameter [Key]	Frequency [MHz]	Return loss [dB]
A	1	-5
B	5	-17
C	25	-17
D	40	-10

9.4 SP3

The variations in the signal integrity at SP3 are mainly constrained by the definitions of SP2 link quality (see 9.2) and the balanced media interconnect attenuation requirements (see 9.3.2). Stimuli for SP3 can be calculated by filtering a signal representing an SP2 corner condition (shaped stress pattern, to form minimum/maximum PSD) using a filter with a transfer function specified in Table 21.

Further signal degradation at SP3 might occur due to amplitude noise coupled on the data-signal along the link. Amplitude noise reduces signal-to-noise ratio and may also cause jitter on the signal. Potential noise sources in general are EMC and crosstalk from neighbouring signals. Potential deterioration by EMC and crosstalk from neighbouring signals is not in the scope of this document.
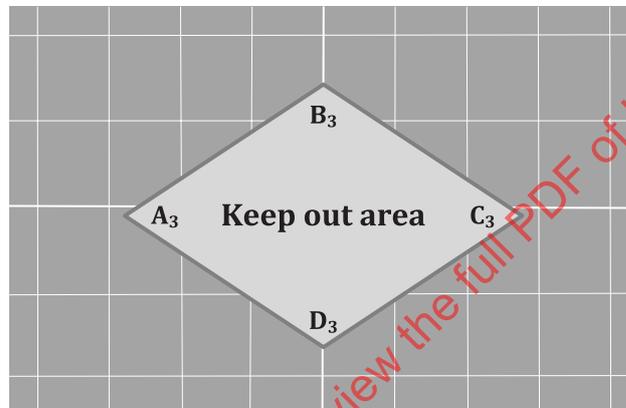
Table 21 defines the link quality parameters of SP3.

Table 21 — Link quality parameters of SP3

Link quality SP3	Condition	Symbol	Minimum	Typical	Maximum	Unit
RMS signal amplitude	Cd4[d], Cd6[f]	V_{RMS3}	260	---	---	mV
Transferred jitter (RMS)	Cd1[a]	J_{tr3}	---	---	190	ps
Eye mask (see Figure 19)	Cd2[b], Cd3[c], Cd5[e]	A_3 to D_3	---	---	---	---
[a] Use the jitter-filter specified in 8.2.2.
[b] Use the Golden PLL specified in 8.2.1.
[c] The DC offset is removed.
[d] The minimum value considers SP2 conditions and interconnect insertion loss.
[e] The mask amplitude parameters include tolerances for overshoot and ringing.
[f] SP3 is terminated with a nominal impedance of 100 Ω.

Figure 19 shows the link quality parameters of SP3 - Eye mask.

Key

A_3, B_3, C_3, and D_3 see Table 22

Figure 19 — Link quality parameters of SP3 - Eye mask

Table 22 — Link quality parameters of SP3 - Eye mask

Parameter [Key]	Amplitude [mV]	Timing [UI]
A_3	0	0,200
B_3	120	0,500
C_3	0	0,800
D_3	-120	0,500

10 Power-on and power-off

10.1 Frequency reference and power supply

The MOST device shall provide the following.

— Frequency reference for the MNC:

the frequency reference is typically a crystal-controlled oscillator or derivative. The requested accuracy is specified in Clause 12.

— Power supply for MNC, EBC and BEC:

  — continuous power supply: V_{CCCN}, with an operating range of 3,3 V ± 0,165 V. This power supply is used to power BEC (or BTR, see 10.3.2);

  — switched power supply: V_{CCSW}, with an operating range of 3,3 V ± 0,165 V, which shall be capable of being switched off. This power supply is used to power the MNC and EBC (or BTR, see 10.3.2).

— Power supply monitoring circuitry: the MOST device shall provide power supply monitoring circuitry for supervising V_{CCSW}, which is specified in 10.2. The MOST device shall connect the /RST inputs of the EBC (BTR) and the MNC.

If the BTR is powered by V_{CCCN} only (see 10.3.2), the /RST signal voltage shall remain below V_{CCSW}.

10.2 Power supply monitoring circuitry

The power supply monitoring circuitry shall do the following.

— Provide an active-low reset signal /RST that is a valid LVTTL (JESD8C) signal over the power supply range V_{VALID} specified in Table 23.

— Set the /RST signal to logic 1 when the power supply voltage ramps above the V_T. Switching from logic 0 to logic 1 shall be delayed by a minimum time of t_{D+} to allow the circuitry in the EBC to stabilize, the LVDS pins of the MNC to be driven, and the local frequency reference to stabilize. Although a maximum time for t_{D+} is not specified, an implicit maximum value exists due to the required start-up time.

— Set the /RST signal to logic 0 when the voltage drops below V_T. Switching from logic 1 to logic 0 shall occur within a time of t_{D-}.

Table 23 specifies the /RST signal parameters.

Table 23 — /RST signal generation

Parameter	Condition	Symbol	Minimum	Typical	Maximum	Unit
Supply range for valid logic levels	---	V_{VALID}	1	---	3,465	V
Logic switching threshold	---	V_T	2,970	---	---	V
Logic 0 to logic 1 time delay	---	t_{D+}	1	---	---	ms
Logic 1 to logic 0 time delay	---	t_{D-}	0	---	100	µs

10.3 Electrical transceiver EBC and BEC

10.3.1 General

Wake-up and shutdown methods of the MOST network require certain functionality to be built into the EBC and BEC of a balanced media transceiver.

10.3.2 BTR requirements

If a BTR has only one power domain (common power supply for EBC and BEC):

— it shall fulfil $I_{ccsleep}$ requirements defined in Table 25 during off-state with /RST signal set to logic 0, and

— it shall fulfil all the requirements for EBC and BEC, where all power supply related parameters (V_{EBC_OR}, V_{EBC_GR}, V_{EBC_OFF}, V_{BEC_OR}) are referred to the actual BTR power supply used.