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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 10: 150-Mbit/s coaxial physical layer

Véhicules routiers — Système de transport axé sur les médias —

Partie 10: Couche coaxiale physique à 150-Mbit/s

Reference number
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Foreword

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21806 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The Media Oriented Systems Transport (MOST) communication technology was initially developed at the end of the 1990s in order to support complex audio applications in cars. The MOST Cooperation was founded in 1998 with the goal to develop and enable the technology for the automotive industry. Today, MOST[1)] enables the transport of high quality of service (QoS) audio and video together with packet data and real-time control to support modern automotive multimedia and similar applications. MOST is a function-oriented communication technology to network a variety of multimedia devices comprising one or more MOST nodes.

Figure 1 shows a MOST network example.

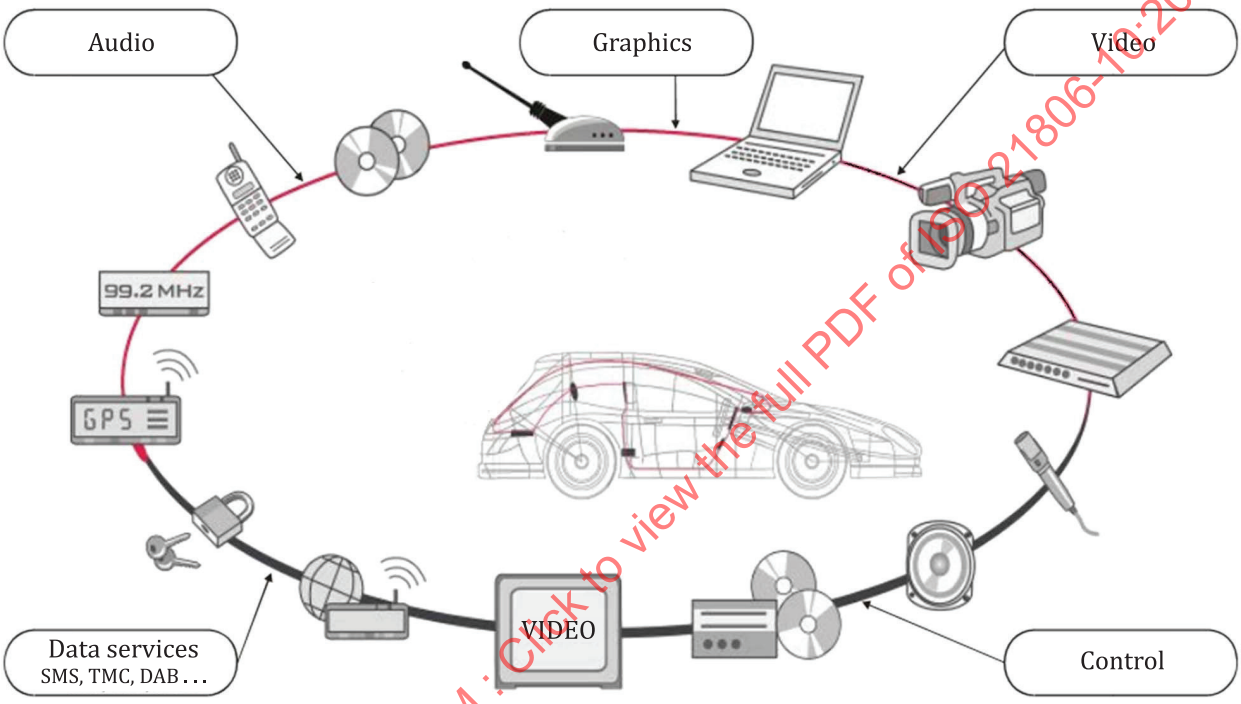

Figure 1 — MOST network example

The MOST communication technology provides:

— synchronous and isochronous streaming,

— small overhead for administrative communication control,

— a functional and hierarchical system model,

— API standardization through a function block (FBlock) framework,

— free partitioning of functionality to real devices,

— service discovery and notification, and

— flexibly scalable automotive-ready Ethernet communication according to ISO/IEC/IEEE 8802-3[2].

MOST is a synchronous time-division-multiplexing (TDM) network that transports different data types on separate channels at low latency. MOST supports different bit rates and physical layers. The network clock is provided with a continuous data signal.

1) MOST® is the registered trademark of Microchip Technology Inc. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO.

Within the synchronous base data signal, the content of multiple streaming connections and control data is transported. For streaming data connections, bandwidth is reserved to avoid interruptions, collisions, or delays in the transport of the data stream.

MOST specifies mechanisms for sending anisochronous, packet-based data in addition to control data and streaming data. The transmission of packet-based data is separated from the transmission of control data and streaming data. None of them interfere with each other.

A MOST network consists of devices that are connected to one common control channel and packet channel.

In summary, MOST is a network that has mechanisms to transport the various signals and data streams that occur in multimedia and infotainment systems.

The ISO Standards Maintenance Portal (https:/standards.iso.org/iso/) provides references to MOST specifications implemented in today's road vehicles because easy access via hyperlinks to these specifications is necessary. It references documents that are normative or informative for the MOST versions 4V0, 3V1, 3V0, and 2V5.

The ISO 21806 series has been established in order to specify requirements and recommendations for implementing the MOST communication technology into multimedia devices and to provide conformance test plans for implementing related test tools and test procedures.

To achieve this, the ISO 21806 series is based on the open systems interconnection (OSI) basic reference model in accordance with ISO/IEC 7498-1[1] and ISO/IEC 10731,[3] which structures communication systems into seven layers as shown in Figure 2. Stream transmission applications use a direct stream data interface (transparent) to the data link layer.

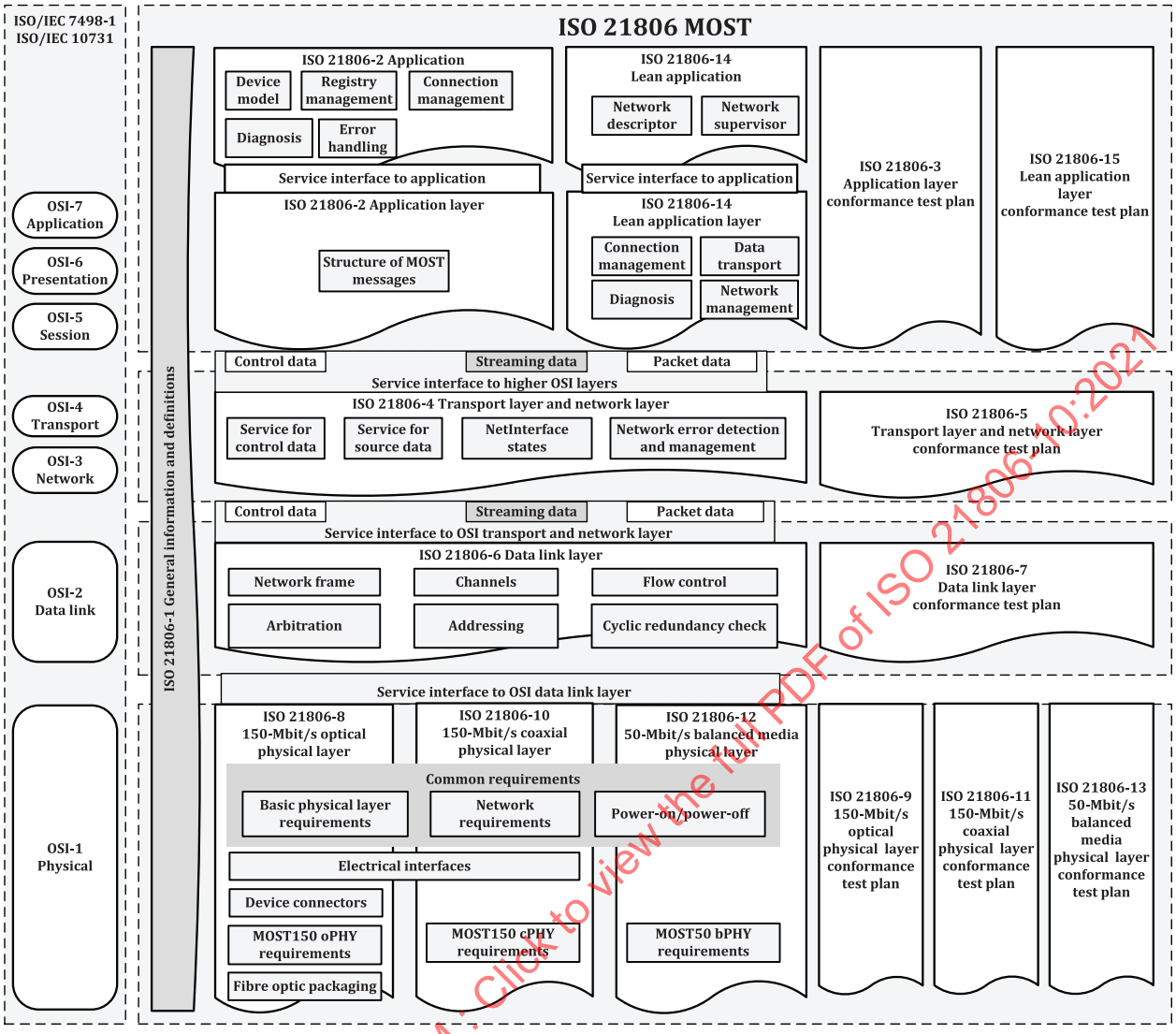

Figure 2 — The ISO 21806 series reference according to the OSI model

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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 10:
150-Mbit/s coaxial physical layer

1 Scope

This document specifies the 150-Mbit/s coaxial physical layer for MOST (MOST150 cPHY), a synchronous time-division-multiplexing network.

This document specifies the applicable constraints and defines interfaces and parameters, suitable for the development of products based on MOST150 cPHY. Such products include coaxial links, coaxial receivers, coaxial transmitters, electrical to coaxial converters, and coaxial to electrical converters.

This document also establishes basic measurement techniques and actual parameter values for MOST150 cPHY.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21806-1, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 1: General information and definitions*

No JEDEC JESD8C.01,[2] *Interface Standard for Nominal 3 V/3,3 V Supply Digital Integrated Circuits*

TIA/EIA-644-A-2001,[3] *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21806-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1
ECC
electrical to coaxial converter
MOST component that converts an electrical signal into a coaxial signal

2) Available at http://www.jedec.org/.

3) Available at https://wwwt.aonline.org/itandards/.

3.2
CEC
coaxial to electrical converter
MOST component that converts a coaxial signal into an electrical signal

4 Symbols and abbreviated terms

4.1 Symbols

---	empty table cell or feature undefined
A_C	attenuation conformance
A_{DC_loss}	DC attenuation
J_{tr}	transferred jitter (RMS)
L_{RL}	return loss
N_{BPF}	number of bits per frame
ρ_{BR}	bit rate
ρ_{Fs}	network frame rate
σ	standard deviation
T_A	ambient temperature
t_{MDT}	TimingMaster delay tolerance
t_{UI}	unit interval
V_{OH}	output high voltage
V_{OL}	output low voltage

4.2 Abbreviated terms

AC	alternating current
AFE	analogue frontend
BER	bit error rate
BR	bit rate
Cd[n]	condition
CEC	coaxial to electrical converter
cPHY	coaxial physical layer
CTR	coaxial transceiver
DC	direct current
DCA	DC adaptive

DDJ	data-dependent jitter
DLL	data link layer
DSV	digital sum value
ECC	electrical to coaxial converter
ECU	electronic control unit
EMC	electromagnetic compatibility
EMI	electromagnetic interference
LVDS	Low-Voltage Differential Signalling
MNC	MOST network controller
N/A	not applicable
PCB	printed circuit board
PDF	probability density function
PHY	physical layer
PLL	phase locked loop
RL	return loss
RMS	root mean square
Rx data	encoded digital bit stream being received
SP[n]	specification point [n]
Tx data	encoded digital bit stream being transmitted

5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[3].

6 Physical layer service interface to OSI data link layer

6.1 Overview

The physical layer (PHY) service interface specifies the abstract interface to the OSI data link layer (DLL), see ISO 21806-6[5].

6.2 Data type definitions

The data type `Enum` is defined as an 8-bit enumeration.

6.3 Event indications and action requests

6.3.1 P_EVENT.INDICATE

The PHY shall use `P_EVENT.INDICATE` to indicate the occurrence of an event to the DLL.

```
P_EVENT.INDICATE{
    PHY_Event
}
```

6.3.2 P_ACTION.REQUEST

`P_ACTION.REQUEST` shall trigger the execution of a request.

```
P_ACTION.REQUEST {
    PHY_Request
}
```

6.4 Parameters

6.4.1 PHY_Event

Table 1 specifies the `PHY_Event` parameter, which notifies the DLL about events.

Table 1 — Parameter passed from PHY to DLL

Parameter	Data type	Description

`PHY_Event`	`Enum {`
	`PHY_Output_Off,`
	`PHY_Network_Activity`
	`}`
		An event that is reported to the DLL.

Table 2 specifies the parameter values for the `PHY_Event Enum`.

Table 2 — PHY_Event Enum values

Enum value	Description
`PHY_Output_Off`	MNC transmit terminal is switched off.
`PHY_Network_Activity`	Network activity is detected at the MNC receive terminal.

6.4.2 PHY_Request

Table 3 specifies the `PHY_Request` parameter, which is passed from DLL to PHY.

Table 3 — Parameter passed from DLL to PHY

Parameter	Data type	Description

`PHY_Request`	`Enum {`
	`cmd_Output_Off,`
	`cmd_Output_On,`
	`cmd_Open_Bypass,`
	`}`
		A request from the DLL

Table 4 specifies the parameter values for the `PHY_Request Enum`.

Table 4 — PHY_Request Enum values

Enum value	Description
`cmd_Output_Off`	Switching off the MNC transmit terminal is requested. By default, it is off.
`cmd_Output_On`	Switching on the MNC transmit terminal is requested. By default, it is off.

Table 4 *(continued)*

Enum value	Description
`cmd_Open_Bypass`	Opening the bypass is requested. By default, the bypass is closed.

7 Basic physical layer requirements

7.1 Logic terminology

7.1.1 Single-ended low-voltage digital signals

For the parameters provided in JEDEC No. JESD8C.01, Table 5 defines the corresponding terms for single-ended signals used in this document. These terms are used to describe the logic states of signals /RST and STATUS.

Table 5 — Terms for single-ended signals

Term	Corresponding JEDEC parameter
Low	V_{OL} (output low voltage)
Logic 0	
High	V_{OH} (output high voltage)
Logic 1	

7.1.2 Differential LVDS signals

TIA/EIA-644-A-2001 uses the labels A and B for the device output terminals; this document uses P and N, respectively. Table 6 specifies the terms for LVDS signals. The terms correspond to the TIA/EIA-644-A-2001 specification.

Table 6 — Terms for LVDS signals

Term	Corresponding JEDEC parameter
Low	The P terminal shall be negative with respect to the N terminal for a binary 0 state.
Logic 0	
High	The P terminal shall be positive with respect to the N terminal for a binary 1 state.
Logic 1	

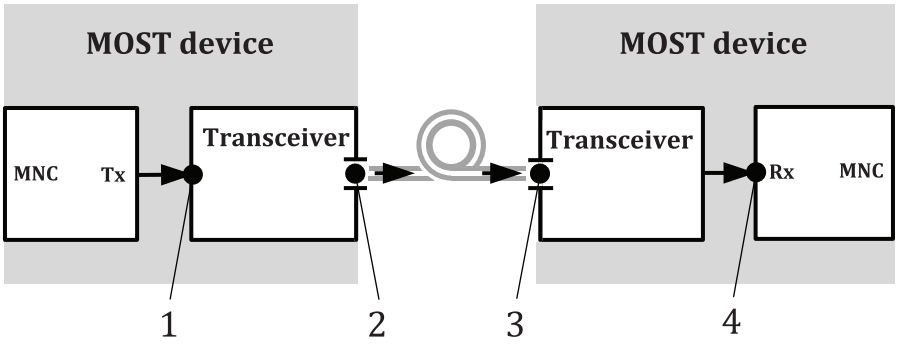
Since some of the MOST devices specified in this document use a tri-state LVDS interface, Table 7 specifies the terms for LVDS bus states.

Table 7 — Terms for LVDS bus states

Term	Corresponding TIA/EIA description
Disabled	The P and N terminals are in a high impedance state. If small leakage currents exist, they might cause an indeterminate voltage on the line/load.
Off	
Enabled	The P and the N terminals are driving the line/load. The outputs are at valid LVDS logic levels provided the input data is valid.
On	
Valid LVDS signal	Data or LVDS 0, according to LVDS voltage levels.

7.2 Specification points (SPs)

A physical connection of two MOST devices is called a link. Measurements are taken at specific locations along a link. These locations are called SPs. The location of the SPs is shown in Figure 3.



Key

1 SP1
2 SP2
3 SP3
4 SP4

Figure 3 — Location of SPs along a link

SPs define interfaces that are boundaries between a transmitting and a receiving MOST component. For each of those interfaces, a set of requirements and properties is defined (e.g. signal timing, signal amplitude, connector interface drawings). SP1 and SP4 are located between a MOST network controller (MNC) and the corresponding transceiver. SP2 and SP3 are located between transceivers and a wiring harness.

For MOST components that are located between two adjacent SPs, requirements and properties can be derived. The definitions of the second SP of the pair specify the component's output performance to be achieved, considering input conditions as defined in the first SP. For example, a transmit converter component specification can be derived from SP1 and SP2. Receive converter component requirements are covered by SP3 and SP4. Wiring harness requirements can be derived from SP2 and SP3.

In addition to the definitions of the SPs for a point-to-point link, this document defines requirements covering the stability of the MOST network. Examples are requirements regarding jitter transfer through MOST devices, jitter accumulation through the MOST network, and power state transitions.

The specified parameters in this document are minimum values to ensure functionality of the MOST network in a wide range of environmental conditions.

7.3 Phase variation

7.3.1 General

Data stream timing and distortion cause phase variation.

7.3.2 Wander

Wander consists of any phase variation from 0 Hz to 10 Hz. All active MOST components in the MOST network create wander. Wander is a function of the temperature drift and propagates from node to node. Typically, wander does not affect alignment jitter eye masks.

NOTE Wander might impact the TimingMaster.

7.3.3 Jitter

Jitter is any phase variation of frequencies above 10 Hz. Every MOST component and the transmission medium create jitter in the MOST network. Jitter is correlated or uncorrelated. The dominant jitter sources in the MOST network consist of PLL noise, link-induced DDJ, sensitivity-induced CEC noise,

crosstalk, or phenomena such as power supply coupling. Data scrambling is used to eliminate DDJ correlation between nodes.

There are two jitter categories as shown in Figure 4.

— Alignment jitter: jitter that affects the reception of data by degrading the receiver eye diagram with horizontal closure (influences eye diagram measurement); it has impact only on a link as data recovery is performed by the MNC.

— Transferred jitter: jitter that is accumulated over all links (does not influence eye diagram measurement); the TimingMaster jitter tolerance shall be determined accordingly.

As the jitter on the measured signal increases, the eye closes more and more. A keep-out mask is specified to detect possible error traces. If the eye does not hit the mask then data recovery is ensured. Mask design depends on the required receiver margin and the characteristics of the channel.

Figure 4 shows the phase variation measurements.

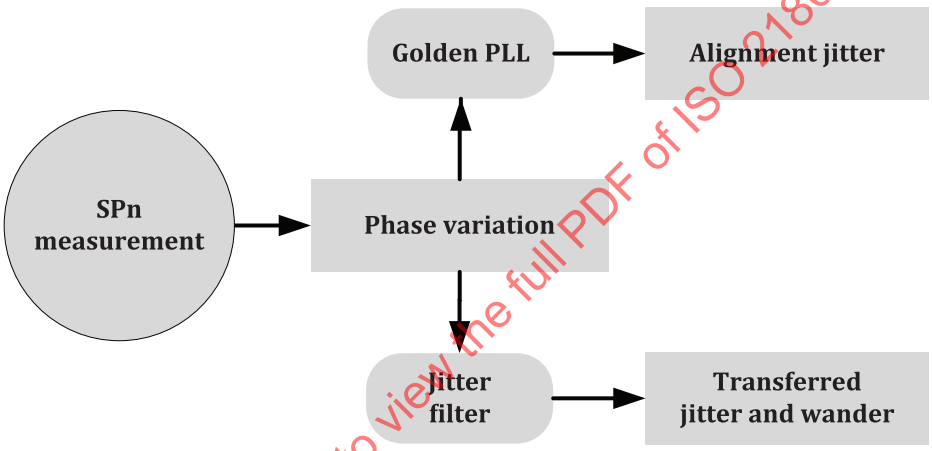


Figure 4 — Phase variation measurements

7.3.4 Clock recovery and reference clock

7.3.4.1 General

Phase variation can be measured directly on a data stream. To view alignment jitter and transferred jitter independently, special tools are required.

All MOST networks contain one device that implements the TimingMaster, which creates the reference clock. This clock is embedded within the data stream. All other MOST devices contain TimingSlaves that recover the clock from the data stream. Therefore, clock recovery is a basic functionality of an MNC. MOST components add phase variation to the data stream. This degrades the reference clock.

Receiver jitter tolerance and jitter transfer are basic operation properties of any MNC. Alignment jitter is measured by means of an eye diagram formed with a Golden PLL. Transferred jitter is measured with a jitter filter.

Figure 5 illustrates clock recovery and data recovery in an MNC. Therefore, there is a need for a Golden PLL model and a jitter filter model. Together they reflect the required jitter behaviour of an MNC.

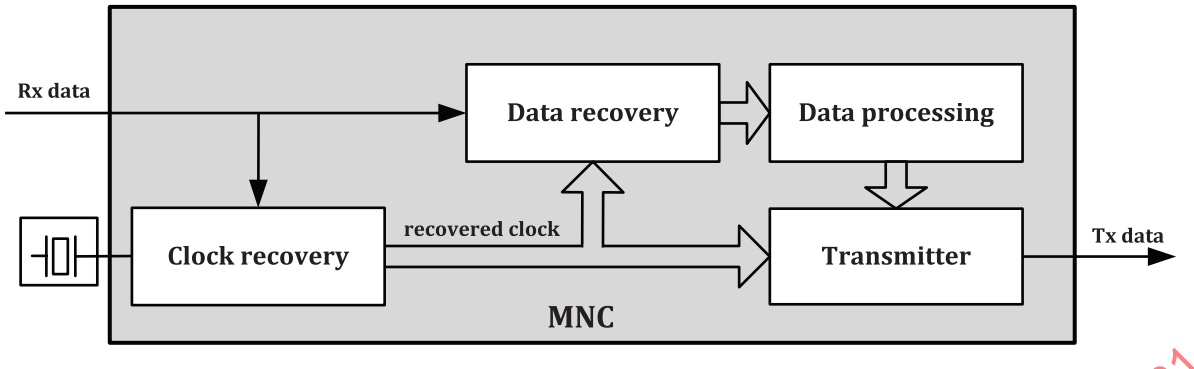


Figure 5 — Clock and data recovery example

7.3.4.2 Golden PLL

The Golden PLL is a simplified model which represents the behaviour of the MNC when jitter is applied to its input. A Golden PLL can be constructed out of hardware or software but shall obtain data from the SP and output a clock at the UI frequency for eye-diagram formation.

7.3.4.3 Jitter filter

The jitter filter is a simplified model which represents the worst-case MNC jitter transfer function. A jitter filter can be constructed out of hardware or software but shall obtain data from the SP and output the RMS value of the transferred jitter at the SP.

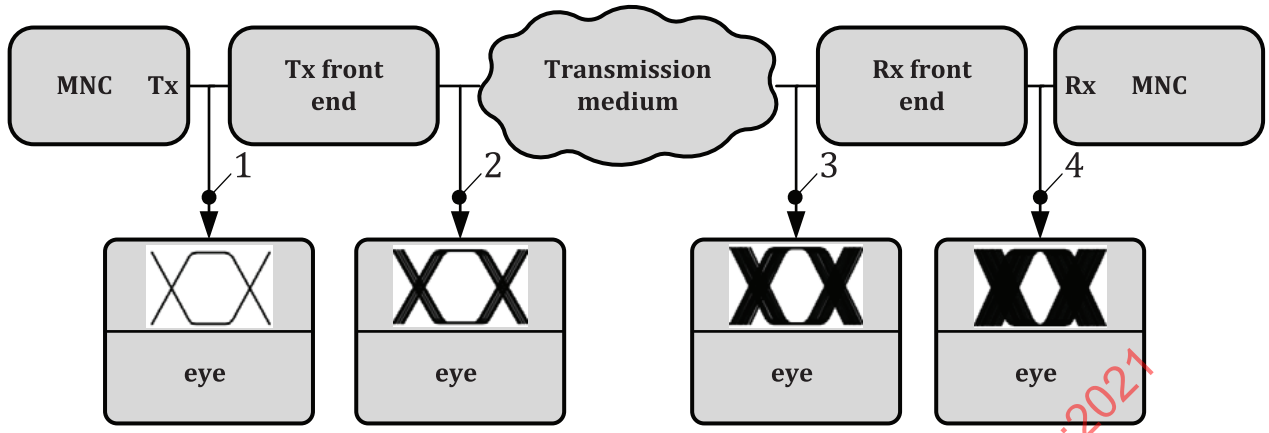
7.3.5 Link quality

7.3.5.1 General

Link quality describes the minimum performance of MOST components along a single link.

7.3.5.2 Alignment jitter

Link quality eye diagrams are used to specify and measure link operation and MOST network level performance. A jitter budget is created top down starting from SP4. The difference between the SPs gives the tolerable contribution of alignment jitter for the respective MOST component or transmission medium. As an example, link quality eyes can be required at every point along the link to allow each MOST component's alignment jitter contribution to be specified. Figure 6 shows an example of the eye diagrams that correspond to the SPs in a link.



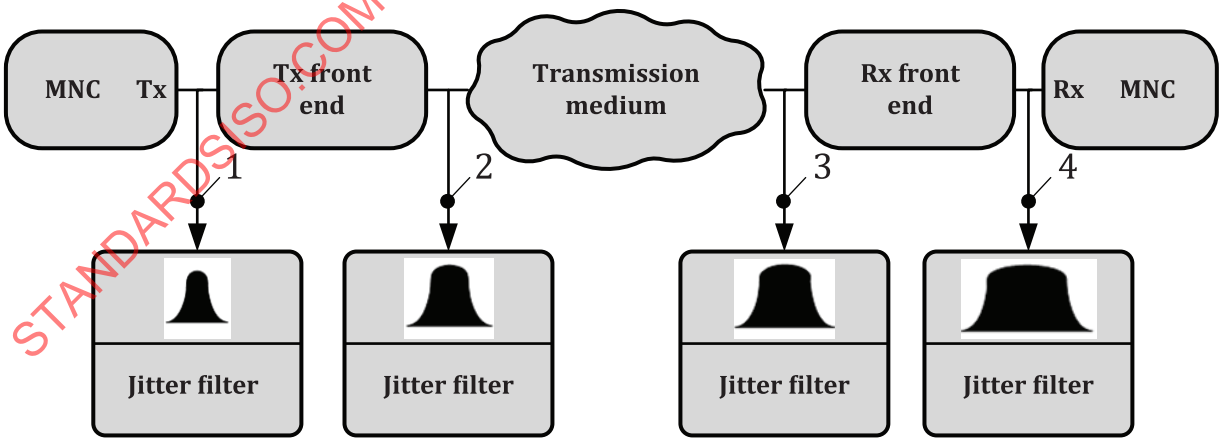
Key

1 SP1
2 SP2
3 SP3
4 SP4

Figure 6 — Illustration of eye diagrams at SPs in a link

7.3.5.3 Transferred jitter

A portion of every jitter source in the MOST network has some spectral content below the jitter filter bandwidth. Jitter passed by the filter accumulates in the following nodes. Transferred jitter from all sources combines to form accumulated jitter. In the network, starting with the first TimingSlave, accumulated jitter increases. Therefore, the total jitter at SP4 of the last MNC in the network consists of the total jitter generated in the final link and the accumulated jitter from all the links before. Transferred jitter is measured by filtering the phase variation at any SPn with a jitter filter. The RMS (standard deviation) of the output of this jitter filter is the amount of jitter contributed to accumulated jitter. Transferred jitter specifications are placed at every SP as shown in Figure 7.



Key

1 SP1
2 SP2
3 SP3
4 SP4

Figure 7 — Illustration of transferred jitter accumulation at various SPs in a link

7.3.6 MOST network quality

7.3.6.1 Receiver tolerance

Receiver tolerance describes the minimum alignment jitter tolerance of an MNC and the maximum tolerable alignment jitter that may occur at any place in the MOST network.

The minimum and maximum limits of the eye mask define the receiver tolerance. The closure of the eye mask originates from accumulated jitter in the MOST network. An MNC recovers all signals that fit into the SP4 receiver tolerance mask. A MOST device recovers all signals that satisfy the SP3 link quality requirements.

Figure 8 shows the typical SPs in a ring where the SP4 receiver tolerance limits can be applied as a test of MOST network performance.

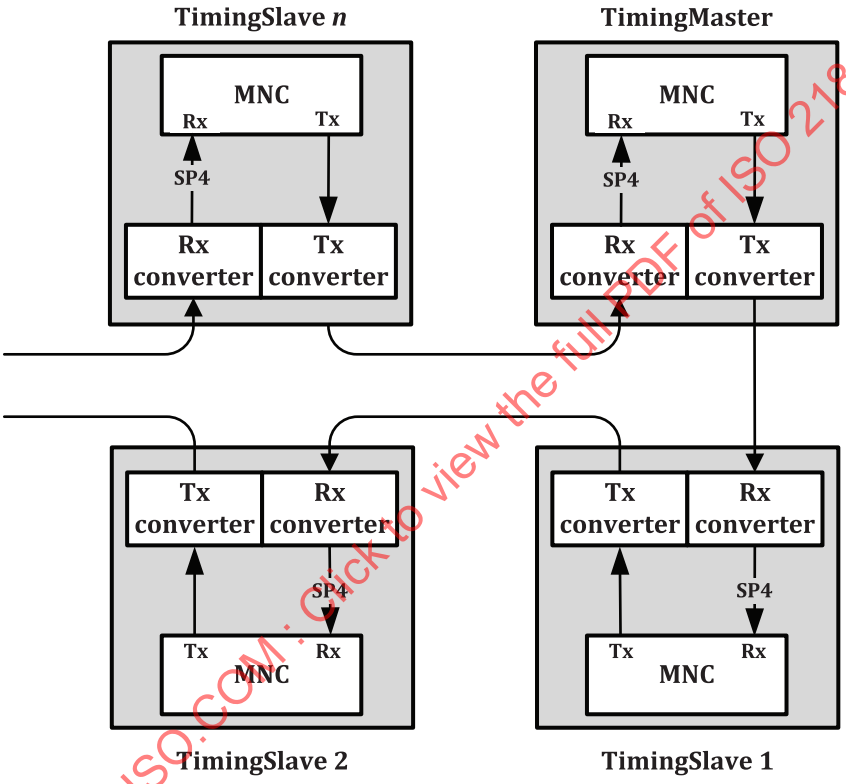


Figure 8 — Locations where receiver tolerance eye mask can be applied

7.3.6.2 TimingMaster delay tolerance

The MOST network stability is determined by the ability of the TimingMaster node to tolerate the accumulated delay present at the end of the ring. TimingMaster delay tolerance is the maximum amount of accumulated delay for an MNC that is configured as TimingMaster.

TimingMaster delay tolerance is tied to the delay, transferred jitter, transferred wander and maximum node count.

Formula (1) defines the minimum for the TimingMaster delay tolerance (t_{MDT}). The relevance of the different types of phase variation for the accumulated delay is shown in Table 8.

$$t_{MDT} \geq t_D(M) + \sum_{n=1}^{m-1} t_D(n) + \sum_{n=0}^{m-1} t_W(n) + t_{D\,Medium} + \alpha \times \sqrt{\sum_{n=0}^{m-1} [t_{TJ}(n)]^2} \quad (1)$$

where

t_{MDT} is the TimingMaster delay tolerance;

M is the position of the TimingMaster;

m is the number of nodes in the network;

n is the position of the node in the network;

$t_D(M)$ is the delay of the TimingMaster node caused by Rx and Tx converter;

$t_{D\ Medium}$ is the total delay caused by the medium;

α is a scaling factor that depends on the BER, see Table 8;

$t_D(n)$ is the delay of a TimingSlave node, see Table 8;

$t_W(n)$ is the wander (phase drift) of the node and link (peak-to-peak);

$t_{TJ}(n)$ is the transferred jitter of the node (i.e. α = 12, derived from ± 6 σ for BER = 10^{-9}).

Assumption:

t_W is correlated from node to node;

t_{TJ} is uncorrelated from node to node.

Table 8 shows the purpose of the MOST network delay and jitter parameters that are combined in Formula (1).

Table 8 — MOST network delay and jitter variables

Variable	Formula	Description
Delay of TimingMaster node	(2)	$t_D(M)$ is the delay caused by Rx and Tx converter of the TimingMaster node.
Delay of a TimingSlave node	(3)	A MOST network operates properly if the TimingMaster complies with this formula.
Accumulation of delay of TimingSlave nodes	(4)	t_{DS} is the delay caused by the (m - 1) TimingSlave nodes. The delay per node is determined by the contribution of Rx converter, MNC, and Tx converter.
Delay of the medium	$t_{D\ Medium}$	It is the total delay caused by the medium (e.g. depending on the length of the medium in use).
Accumulation of wander	(5)	t_{W_SUM} is the accumulated wander of all nodes. Due to the low-frequency characteristic of wander, either most or all of this phase variation is transferred by a PLL. Wander is generated by all active MOST components of the link and by the MNC chip. Wander is most commonly caused by variations in temperature. It shall be specified in the data sheet of each active MOST component.
Accumulation of transferred jitter	(6)	t_{TJ_SUM} is the accumulated transferred jitter of all nodes. Uncorrelated jitter sources add according to their variance. Scrambled data eliminates the correlation between DDJ on successive nodes. OEC noise and PLL noise sources are typically uncorrelated as well. This peak-to-peak number can be directly tied to a BER when the assumed jitter PDF is normal, e.g. α = 12 in case of ± 6 σ for BER = 10^{-9}.

$$t_D(M) = t_{D\,Rx}(M) + t_{D\,Tx}(M) \quad (2)$$

where

M is the position of the TimingMaster;

$t_{D}(M)$ is the delay of the node caused by Rx and Tx converter;

$t_{D\,Rx}(M)$ is the delay of the TimingMaster node caused by Rx converter;

$t_{D\,Tx}(M)$ is the delay of the TimingMaster node caused by Tx converter.

$$t_{D}(n) = t_{D\,Rx}(n) + t_{D\,MNC}(n) + t_{D\,Tx}(n) \tag{3}$$

where

n is the position of node in the network;

$t_{D}(n)$ is the delay of a TimingSlave node, see Table 8;

$t_{D\,Rx}(n)$ is the delay of the node n caused by Rx converter;

$t_{D\,MNC}(n)$ is the delay of the node n caused by MNC;

$t_{D\,Tx}(n)$ is the delay of the node n caused by Tx converter.

$$t_{DS} = \sum_{n=1}^{m-1} t_{D}(n) \tag{4}$$

where

t_{DS} is the accumulated delay of the TimingSlave nodes;

$t_{D}(n)$ is the delay of a TimingSlave node;

n is the position of node in the network;

m is the number of nodes in the network.

$$t_{W\_SUM} = \sum_{n=0}^{m-1} t_{W}(n) \tag{5}$$

where

t_{W_SUM} is the accumulated wander of all nodes;

$t_{W}(n)$ is the wander (phase drift) per node and link (peak-to-peak);

n is the position of node in the network;

m is the number of nodes in the network.

$$t_{TJ\_SUM} = \alpha \times \sqrt{\sum_{n=0}^{m-1} [t_{TJ}(n)]^2} \quad (6)$$

where

t_{TJ_SUM} is the accumulated transferred jitter of all nodes;

$t_{TJ}(n)$ is the transferred jitter per node (i.e. α = 12, derived from ± 6 σ for BER = 10^{-9});

n is the position of node in the network;

m is the number of nodes in the network.

8 MOST150 cPHY requirements

8.1 General MOST network parameters

8.1.1 MOST network coding

8.1.1.1 General

The following subclauses describe a technique of encoding digital data called DCA coding, which shall be used in MOST150 cPHY.

8.1.1.2 Pulse characteristics

The MOST150 cPHY signal is scrambled and encoded using DCA coding. Data pulses range from 2 UI to 6 UI, yielding five different pulse widths, as shown in Figure 9.

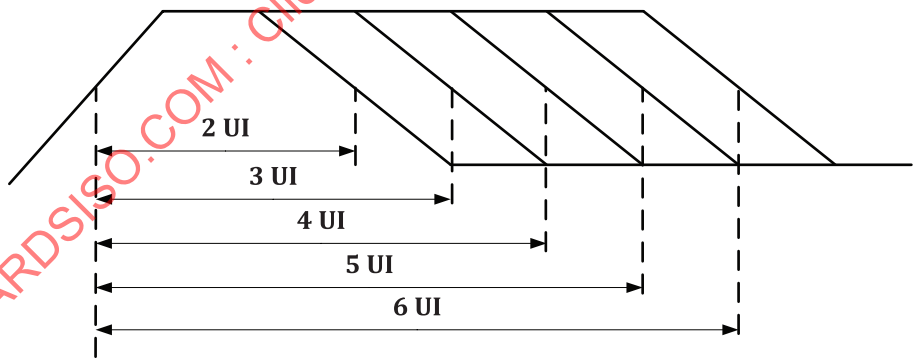


Figure 9 — Allowable pulse widths when using DCA coding

8.1.1.3 Unit interval definition

The unit interval (UI) width calculation is specified in Formula (7).

For MOST150 cPHY, there are 3 072 bits per frame (BPF). Using Formula (7) for a frame rate of 48 kHz results in a UI of 3,391 ns. A frame rate of 44,1 kHz has a UI of 3,691 ns.

$$t_{UI} = \frac{1}{\rho_{Fs} \times 2 \times N_{BPF}} \quad (7)$$

where

t_{UI} is the unit interval (UI);

ρ_{Fs} is the network frame rate;

N_{BPF} is the bits per frame.

8.1.1.4 DC balance

DCA coding ensures absence of DC. Short-term imbalances in offset occur during data transmission. These imbalances are tracked with a running total called the digital sum value (DSV). The DSV is calculated by incrementing the sum for every UI where the level is logic 1 and decrementing the sum for every UI where the level is logic 0. The calculation for DSV is illustrated in Figure 10.

Dynamic properties of DCA coding:

— the DSV is periodically driven to logic 0 at least once per frame;

— the range of DSV values in a valid DCA stream are {-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5};

— the shortest DCA period is 4 UI;

— the longest DCA period is 10 UI;

— the data stream shall have a period of 10 UI at least once per frame. These 10 UI periods can either be made of pulses that are 4 UI high/low with 6 UI low/high, 6 UI high/low with 4 UI low/high, or 5 UI high/low with 5 UI low/high.

Figure 10 shows the DSV calculation.

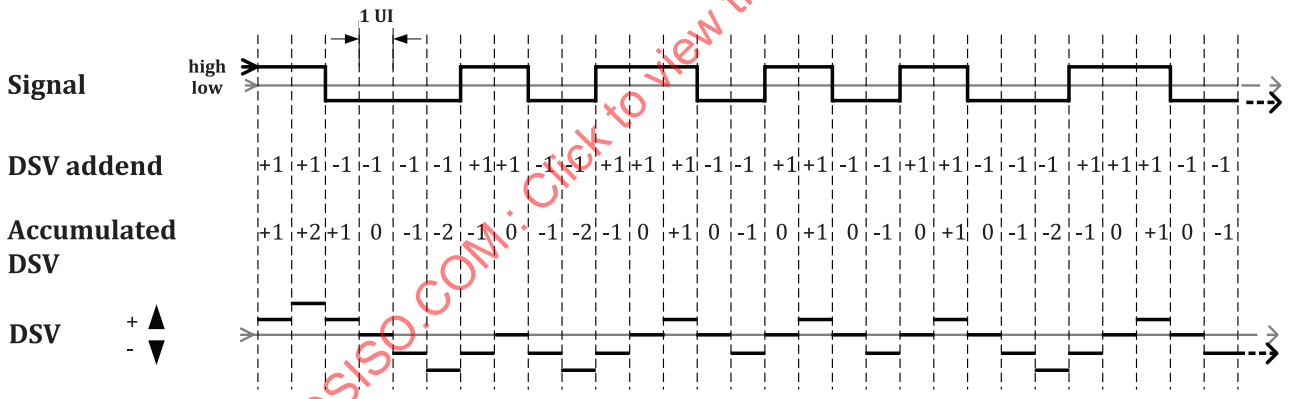


Figure 10 — DSV calculation

8.1.2 Link and interconnect type

The coaxial cables and the connectors shall be 50 Ω end terminated. Depending on the specific application, there are two interconnect types.

— Simplex (unidirectional) interconnect – the transmit and receive links are separate and unidirectional using two separate ports (device connectors) and cables.

— Duplex (bidirectional) interconnect – the transmit and receive links share the same cable using one port (device connector). Communication is full duplex. A coaxial transceiver (CTR - combination of an ECC and a CEC) is responsible for separating the transmit and receive signal components.

One of the following connector port types shall be used:

— transmit port (of a simplex interconnect);

— receive port (of a simplex interconnect);

— bi-directional port (of a duplex interconnect).

These ports shall be uniquely encoded to prevent accidental misconnections being made. All connectors shall conform to the electrical specifications as defined in 9.4. See Clause 13 for mechanical information and connector keying.

8.1.3 SP details

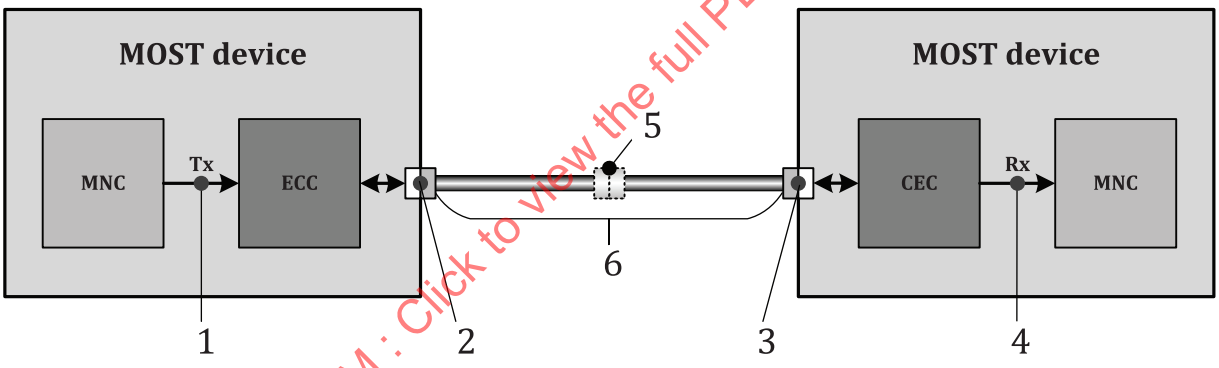
Table 9 defines the SP locations and interfaces.

Table 9 — SP locations and interfaces

SP	Location	Interface
SP1[a]	ECC electrical input pins at LVDS termination	LVDS
SP2[a]	Signal at transmit port of coaxial interface	analogue
SP3[a]	Signal at receive port of coaxial interface	analogue
SP4[a]	CEC electrical output pins at LVDS termination	LVDS

[a] See Figure 6.

Figure 11 shows the location of SPs.



Key

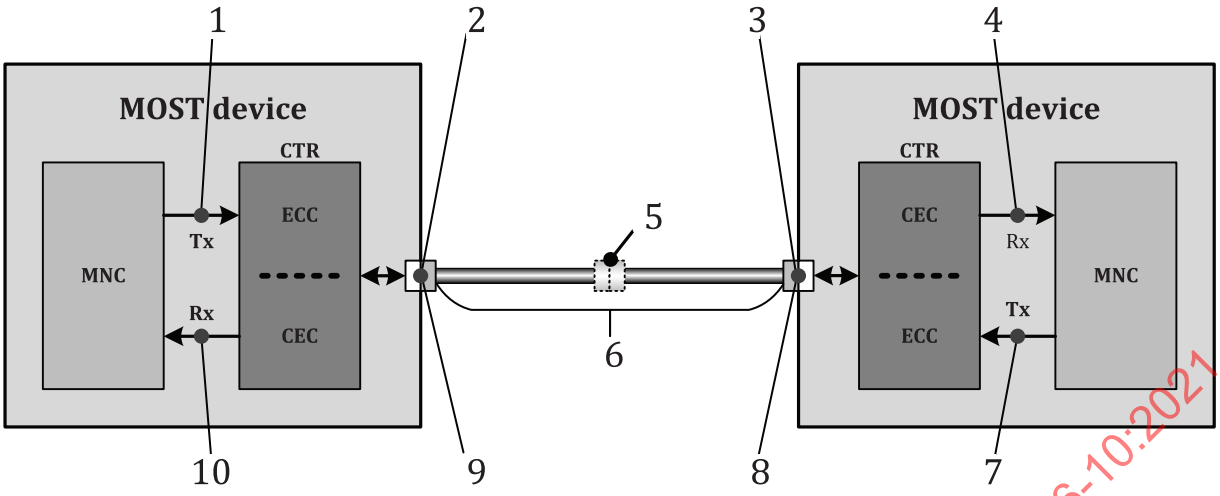
1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)

Figure 11 — Location of SPs for simplex interconnect

Viewed from one node, a duplex interconnect consists of two links – one transmit (or forward) and one receive (or reverse). In the duplex scenario, the two links shall be considered independently.

Figure 12 illustrates a duplex interconnect. SP1, SP2, SP3 and SP4 indicate the forward signal path. SP1*, SP2*, SP3* and SP4* indicate the reverse signal path.

The requirements for the forward and reverse signal paths are identical but the measurements are performed independently. A method to separate the forward and reverse components shall be utilised when measuring duplex interconnects.



Key

1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)
7 SP1*: reverse signal path
8 SP2*: reverse signal path
9 SP3*: reverse signal path
10 SP4*: reverse signal path

Figure 12 — Location of SPs for duplex interconnect

8.1.4 Analogue frontend

The section between transceiver pins and coaxial connector is called analogue frontend (AFE).

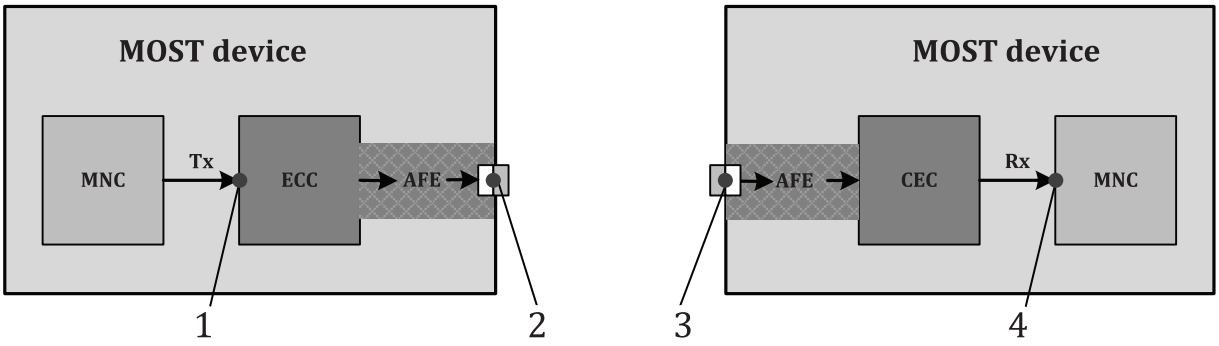
Suppliers of coaxial transceivers provide a connection scheme that meets the requirements for connection and layout of the transceivers with coaxial connector, including passive components. Performance criteria:

— for SP2 apply to ECC and AFE,

— for SP3 apply to the signal characteristic after passing the coaxial interconnect, and

— for SP4 apply to AFE and CEC.

Figure 13 shows the analogue frontend.



Key

1 SP1
2 SP2
3 SP3
4 SP4

Figure 13 — Analogue frontend

8.1.5 Integration of coaxial transceiver

Coaxial transceivers are either realized as standalone components or integrated in the MNC.

For standalone transceivers, connections between coaxial transceiver and MNC are formed as traces on the PCB (e.g. SP1 and SP4). Thus, coaxial transceivers and MNCs from different suppliers, adhering to the requirements for SP1 and SP4, can be used.

For integrated transceivers, the coaxial transceiver portion is connected with the MNC Rx section and the MNC Tx section. In consequence, there is no external SP1 and SP4. Suppliers of such integrated versions are solely responsible for their inherent SP1 and SP4 performance.

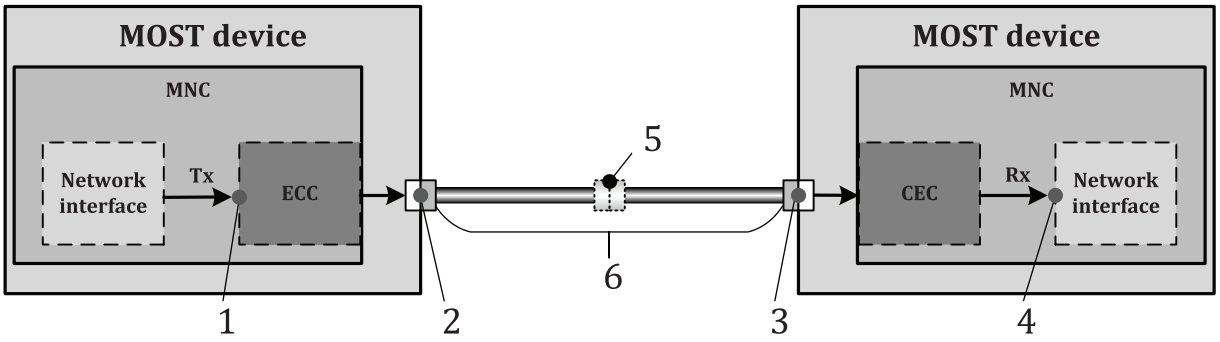
Table 10 defines the SP locations and interfaces for integrated coaxial transceivers.

Table 10 — SP locations and interfaces for integrated coaxial transceivers

SP	Location	Interface
SP2	Signal at transmit port of coaxial interface	analogue
SP3	Signal at receive port of coaxial interface	analogue

NOTE For special cases see Clause 15.

Figure 14 shows the location of SPs for simplex interconnect with integrated coaxial transceivers.

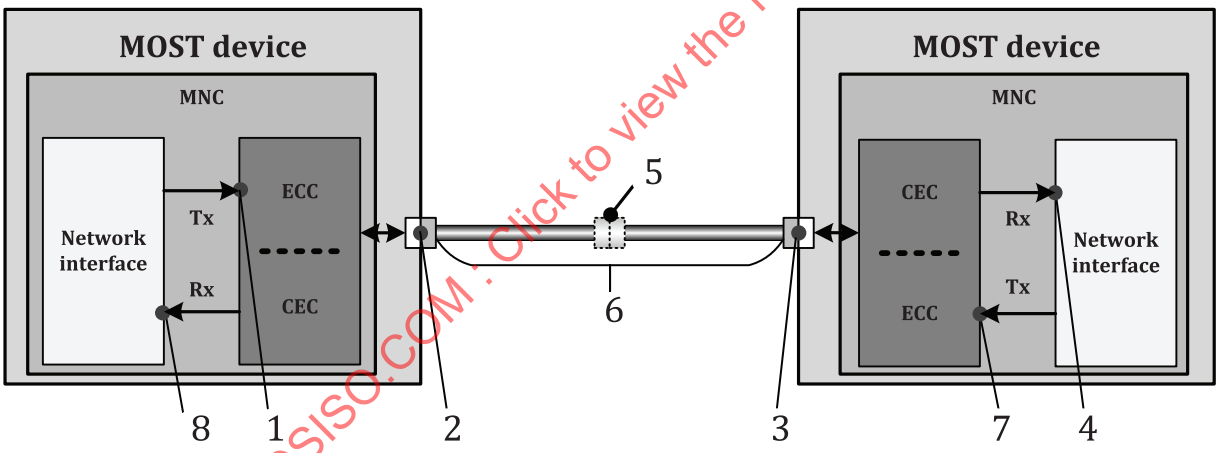


Key

1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)

Figure 14 — Location of SPs for simplex interconnect with integrated coaxial transceivers

Figure 15 shows the location of SPs for duplex interconnect with integrated coaxial transceivers.



Key

1 SP1
2 SP2
3 SP3
4 SP4
5 in-line connectors (optional)
6 50 Ω coaxial interconnect (including connectors)
7 SP1*: reverse signal path
8 SP4*: reverse signal path

Figure 15 — Location of SPs for duplex interconnect with integrated coaxial transceivers

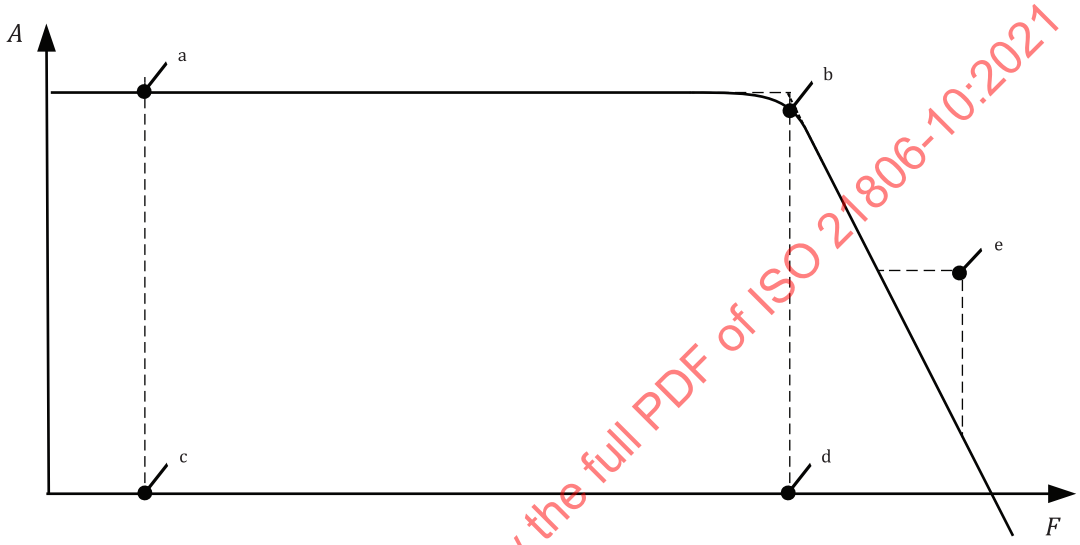
8.2 Models and measurement methods

8.2.1 Golden PLL

The Golden PLL determines the required worst-case jitter performance of an MNC and is used to form receiver eye diagrams. The positive edge of the signal shall trigger the Golden PLL. The transfer function is a low-pass filter with unity gain at 0 Hz.

NOTE For practicality of measurements, the transfer function is specified for 10 Hz and above.

Figure 16 shows the Golden PLL transfer function.



Key

a A_{P0}: amplitude point 0.
b A_{P1}: amplitude point 1.
c F_{P0}: frequency point 0.
d F_{P1}: frequency point 1.
e Slope.
A attenuation [dB]
F frequency [Hz], logarithmic scale

Figure 16 — Golden PLL transfer function

Table 11 specifies the Golden PLL parameters.

Table 11 — Golden PLL parameters

Parameter	Value	Unit
A_{P0}	0	dB
F_{P0}	10	Hz
A_{P1}	-3	dB
F_{P1}	125	kHz
Slope	-20	dB/dec

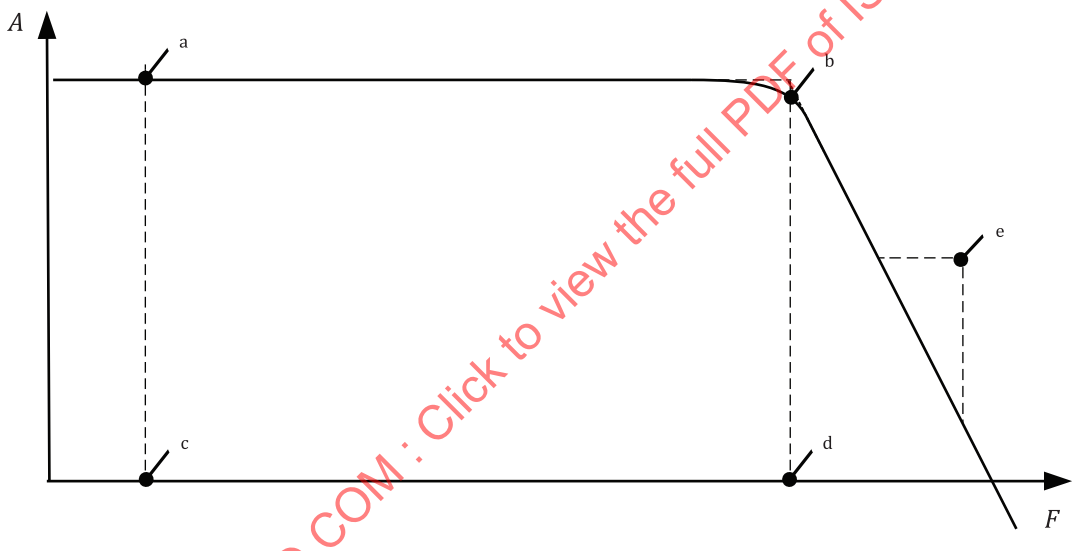
8.2.2 Jitter filter

The jitter filter determines the worst-case jitter transfer function of an MNC and is used to calculate transferred jitter along the link. The transfer function is a low-pass filter with unity gain at 0 Hz.

NOTE For practicality of measurements, the transfer function is specified for 10 Hz and above.

The jitter filter shall reference the positive edge of the signal.

Figure 17 shows the jitter filter response.



Key

a A_{J0}: amplitude point 0.
b A_{J1}: amplitude point 1.
c F_{J0}: frequency point 0.
d F_{J1}: frequency point 1.
e Slope.
A attenuation [dB]
F frequency [Hz], logarithmic scale

Figure 17 — Jitter filter response

Table 12 defines the jitter filter specifications.

Table 12 — Jitter filter specifications

Parameter	Value	Unit
A_{J0}	0	dB
F_{J0}	10	Hz
A_{J1}	-3	dB
F_{J1}	200	kHz
Slope	-20	dB/dec

8.2.3 Retimed bypass mode and stress pattern

The retimed bypass mode is a test mode for physical layer testing. In retimed bypass mode, the MNC shall refresh and forward the received signal.

The MOST150 cPHY stress pattern shall be used for:

— signal level detection,

— overshoot and undershoot, and

— all eye diagrams.

Table 13 defines the reference of the MOST150 cPHY stress pattern.

Table 13 — MOST150 cPHY stress pattern reference

Item	Item reference
Description code	MOST150 cPHY stress pattern
Filename	MOST150_Stress_Pattern-1v0.pat
Access location	ISO 21806-1:2020, Annex A
ZIP archive	MOST150_cPHY_Specification_1V0-0.zip

9 Link specifications

9.1 General

For jitter and pulse shape evaluation, this document specifies eye diagrams. A large eye opening indicates a signal with low jitter and distortion. The eye diagram is specified such that a valid signal does not overlap the eye mask. A signal that overlaps the eye mask does not meet the requirements. Signals with slow rise times, low amplitude, jitter, or pulse width variations are represented by closures in the eye diagram.

All MOST components along the link shall operate with a BER lower than 10^{-9}.

9.2 SP1

The signal at SP1 shall remain outside the keep-out areas of the eye mask. See 10.1, 11.3, and Clause 12 for operating conditions and interface specifications.

Table 14 specifies the link quality parameters of SP1.

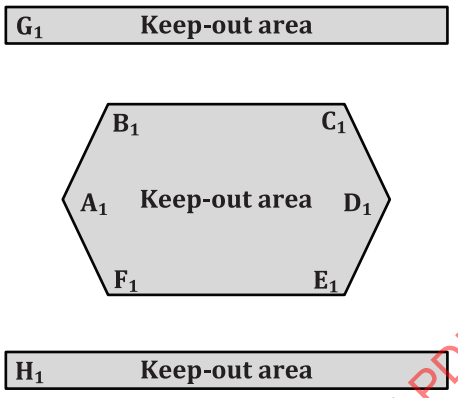
Table 14 — Link quality parameters of SP1

Link quality parameters of SP1	Condition	Symbol	Minimum	Typical	Maximum	Unit
Transferred jitter	Cd1[a]	J_{tr1}	---	---	50	ps
Eye mask (see Figure 18)	Cd2[b], Cd3[c]	A_1 to H_1	---	---	---	---

[a] Use the jitter filter as specified in 8.2.2.

[b] Use the Golden PLL as specified in 8.2.1.

[c] The signal shall comply with the minimum input signal amplitude specification, see 12.1.



Key

A_1 to H_1 see Table 15

Figure 18 — Link quality parameters of SP1 – Eye mask

Table 15 specifies the link quality parameters of SP1 - Eye mask.

Table 15 — Link quality parameters of SP1 - Eye mask

Parameter [Key]	Amplitude [mV]	Timing [UI]
A_1	0	0,075
B_1	+100	0,325
C_1	+100	0,675
D_1	0	0,925
E_1	-100	0,675
F_1	-100	0,325
G_1	+636	---
H_1	-636	---

9.3 SP2

The signal at SP2 shall meet the requirements in Table 16 and shall remain outside the keep-out area of the eye mask. Refer to 10.1, 11.3 and Clause 12 for operating conditions and interface specifications.

Table 16 — Link quality parameters of SP2

Link quality parameters of SP2	Condition	Symbol	Minimum	Typical	Maximum	Unit
Rise time	20 % to 80 %	t_{r2}	700	---	1 400	ps
Fall time	80 % to 20 %	t_{f2}	700	---	1 400	ps
Transferred jitter	Cd1[a]	J_{tr2}	---	---	112	ps
Steady-state amplitude	Cd4[d]	V_{ss2}	300	---	420	mV
Eye mask (see Figure 19)	Cd2[b], Cd3[c], Cd5[e]	A_2 to H_2	---	---	---	---

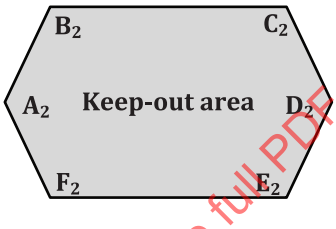
[a] Use the jitter filter specified in 8.2.2.

[b] Use the Golden PLL specified in 8.2.1.

[c] The DC offset is removed.

[d] The difference between high-state and low-state of bimodal waveform.

[e] The mask amplitude parameters include tolerances for overshoot and ringing.



Key

A_2 to F_2 see Table 17

Figure 19 — Link quality parameters of SP2 - Eye mask

Table 17 specifies the link quality parameters of SP2 - Eye mask.

Table 17 — Link quality parameters of SP2 - Eye mask

Parameter [Key]	Amplitude [mV]	Timing [UI]
A_2	0	0,150
B_2	125	0,400
C_2	125	0,600
D_2	0	0,850
E_2	-125	0,600
F_2	-125	0,400
G_2	235	---
H_2	-235	---

9.4 Coaxial link requirements

9.4.1 Coaxial interconnect, length and attenuation

The coaxial interconnect parameter requirements shall be the same for both simplex and duplex interconnects. The maximum coaxial interconnect length is specified in Table 18. This length includes the coaxial cables and the connectors (device and in-line). The number of in-line connectors is not limited as long as the interconnect conforms to the parameters specified in Table 18.

Table 18 — Coaxial interconnect attenuation parameters

Link quality parameters of SP2	Condition	Symbol	Minimum	Typical	Maximum	Unit
Coaxial interconnect length	Cd1[a]	l_{ci}	0	---	15	m
DC loss	Cd1[a]	A_{DC_loss}	0	---	0,5	dB
Skin effect loss	Cd1[a]	F_{skin}	$9{,}2 \times 10^6$	---	∞	Hz/dB^2
Attenuation conformance	Cd1[a], Cd2[b]	A_C	-1	---	1	dB

[a] Environmental conditions or mechanical stress being applied to the coaxial interconnect lead to parameter variations.

[b] F = 1 MHz to 450 MHz.

For signal integrity, the following loss parameters for coaxial cables and connectors are considered:

— connector insertion loss,

— DC resistance loss,

— skin effect loss,

— dielectric loss.

In the MOST150 cPHY frequency range of interest, dielectric and connector insertion losses, e.g. according to ISO 20860-1[4], are negligible. Therefore, it is sufficient to consider only DC resistance and skin effect losses of the coaxial cable as coaxial interconnect attenuation sources.

The amount of attenuation is mainly dependent on the length of the coaxial interconnect. For any given interconnect length and for any combination of cable segments and couplers in an interconnect, the DC resistance and skin effect losses have unique values.

For the MOST150 cPHY frequency range of interest, the theoretical transfer function of the coaxial interconnects is expressed with Formula (8) (coaxial cable transfer function versus frequency). Formula (8) consists of two terms; both of them are cable-length dependent (l). The first term of the formula represents the frequency dependent attenuation in [ratio/m], while the second term describes the phase over frequency in [rad/m].

$$H_{theo}(F) = 10^{-\left(\frac{A_{DC\_loss} + \sqrt{\frac{F}{F_{skin}}}}{20}\right) \times l} \times e^{-i \times \left(\frac{t_{lpd} \times F + \sqrt{\frac{F}{F_{skin}}}}{20\log_{10}(e)}\right) \times l} \quad (8)$$

where

H_{theo} is the theoretical complex transfer function for a coaxial cable;

A_{DC_loss} represents the DC attenuation;

F_{skin} represents skin effect losses;

t_{lpd} stands for linear phase delay and represents a constant propagation delay;

l is the length of the coaxial interconnect;

F is the frequency;

i is the imaginary unit.

The receiver circuitry in the CEC shall include an equalizer designed to compensate for attenuation. Variations in the coaxial interconnect characteristics, which do not follow the theoretical transfer

function above, cannot be compensated and degrade the CEC output signal. Therefore, the attenuation characteristic of a coaxial interconnect shall closely resemble that of an ideal coaxial cable.

Formula (9) expresses the attenuation versus frequency (in dB) for a coaxial interconnect of length l (within l_{ci}).

$$A(F) = -A_{DC\_loss} - \sqrt{\frac{F}{F_{skin}}} \tag{9}$$

where

A is the attenuation;

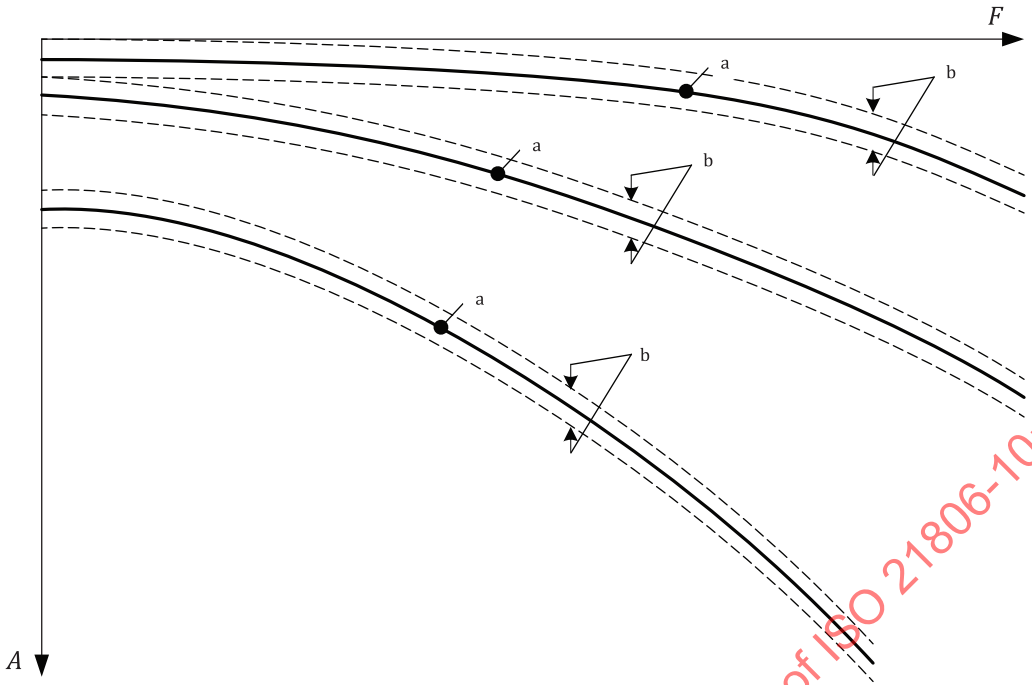
A_{DC_loss} represents the DC attenuation;

F_{skin} represents skin effect losses;

F is the frequency.

The resulting values of the parameters A_{DC_loss} and F_{skin} for a particular interconnect of length (l) are unique for exactly this configuration of cables. The resulting parameter values inherently consider the length of the particular interconnect. The parameters are derived from measured transfer characteristics (attenuation over frequency). The numerical values are determined using analytic or experimental (e.g. curve fitting) approaches; Clause 16 contains the description and an example. The resulting values for A_{DC_loss} and F_{skin} shall meet the range given in Table 18.

To put constraints on the coaxial interconnect variations, this document defines the attenuation conformance (A_C) parameter. A_C, as shown in Figure 20, specifies the maximum deviation from the theoretical cable transfer function Formula (8) for a given set of DC resistance and skin effect losses (as defined by the interconnect length and quality). The coaxial interconnect attenuation shall fit within the boundaries defined by the minimum and maximum values of parameter A_C.



Key

a Possible attenuation curves, based on different A_{DC_loss} and F_{skin}.

b A_C = ± 1 dB.

A attenuation

F frequency

Figure 20 — Attenuation conformance curves

Formula (8) allows to calculate the temporal impulse response, taking into consideration also the phase of the signal. The combination of infinite F_{skin} and zero A_{DC_loss} corresponds to a zero-length coaxial cable. The combination of finite F_{skin} and non-zero A_{DC_loss} corresponds to a coaxial cable with a non-zero length.

9.4.2 Characteristic impedance and return loss (L_{RL})

9.4.2.1 General

In 9.4.2.2 to 9.4.2.3 requirements are specified for characteristic impedance of components forming a coaxial link. Impedance mismatches cause reflection of some of the signal energy. The ratio of reflected signal to transmitted signal is called L_{RL}. The definition of characteristic impedance is either given as impedance [Ω] or as L_{RL} [dB], whatever is better suited for the component.

On a communication link, L_{RL} has different importance for simplex and duplex operation.

In simplex operation, L_{RL} on a transmit path means a minor reduction of signal amplitude in transmit direction. Such losses are already included in:

— SP2 output signal specification: this covers amplitude reduction due to L_{RL} inside the ECU;

— attenuation requirements (see Table 18) for coaxial interconnects: the measurement of attenuation inherently includes the respective L_{RL}.

Not covered are losses due to impedance mismatches at SP3, between coaxial interconnect and the PCB interface.

Crosstalk due to double reflections, as another possible form of signal degradation, is negligible for simplex.

For duplex, L_{RL} causes a minor reduction of signal amplitude in transmit direction. More important here is added noise due to reflections. Signal edges, generated on an ECC of a node, cause reflections when passing impedance mismatches. Multiple mismatches along that link cause multiple reflections, which overlay with each other. Such reflections overlay as crosstalk with the signal on the receive path, being sent from the opposite node. Therefore, the accumulation of relevant L_{RL} contributions along a link forms a crosstalk-signal, which compromises the data signal being sent to that node. Cable attenuation reduces the amplitude of reflections.

For duplex links, calculation of minimum CEC-input signal-quality shall consider losses along the coaxial interconnect as well as added crosstalk.

The mismatch of a load impedance Z_L to a source impedance Z_S results in a reflection coefficient as specified in Formula (10).

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{10}$$

where

Γ is the reflection coefficient;

Z_L is the load impedance;

Z_S is the source impedance.

The impedance values can be complex numbers. The magnitude of the reflection coefficient is given by Formula (11).

$$p = |\Gamma| \tag{11}$$

where

p is the magnitude of the reflection coefficient;

Γ is the reflection coefficient.

L_{RL} is expressed by Formula (12)

$$L_{RL} = -20 \times \log_{10}(p) \tag{12}$$

where

L_{RL} is the return loss, limits are given in the frequency range of 1 MHz to 450 MHz;

p is the magnitude of the reflection coefficient.

Formula (13) defines the worst-case accumulation of L_{RL} [dB] for impedance mismatches.

$$L_{RL\_acc} = -20 \times \log_{10}\left(10^{\left(\frac{-L_{RL\_a}}{20}\right)} + 10^{\left(\frac{-L_{RL\_b}}{20}\right)} + \ldots\right) \quad (13)$$

where

L_{RL_acc} is the return loss accumulation;

L_{RL_a} is the return loss for impedance mismatch *a*;

L_{RL_b} is the return loss for impedance mismatch *b*.

9.4.2.2 Coaxial interconnect, characteristic impedance and L_{RL}

Table 19 specifies the coaxial interconnect characteristic impedance and L_{RL} parameters. The end-to-end (SP2 to SP3) coaxial interconnect shall have L_{RL} as specified in Table 19.

Table 19 — Coaxial interconnect characteristic impedance and L_{RL} parameters

Parameters	Condition	Symbol	Minimum	Typical	Maximum	Unit
Return loss of harness-connectors and inline connectors	F= 1 MHz to 450 MHz Cd1[a], Cd2[b], Cd5[e], Cd6[f]	L_{RL_con}	--	---	15,6	dB
Return loss of coaxial interconnect	F = 1 MHz to 450 MHz Cd1[a], Cd3[c], Cd4[d], Cd5[e], Cd6[f]	$L_{RL\_intercon}$	---	---	-20	dB
Characteristic impedance of coaxial cable	Cd1[a], Cd2[b], Cd4[d], Cd7[g]	Z_{0cable}	47	50	53	Ω

[a] Environmental conditions or mechanical stress being applied to the coaxial interconnect lead to parameter variations. Refer to 10.1 and 11.3 for operating conditions.

[b] For simplex and duplex.

[c] For duplex only.

[d] Relevant for accumulated return loss.

[e] Measured using $t_{riseTDR}$ = 400 ps.

[f] Nominal characteristic impedance 50 Ω.

[g] See EN 50289-1-11:2002[9].

For duplex, the maximum number of cable segments within a coaxial interconnect is limited by the deviation of the cable pieces from the nominal characteristic impedance. The summation of mismatches in an interconnect shall result in a return loss, equal or less than specified for $L_{RL\_intercon}$.

9.4.2.3 PCB interfaces, characteristic impedance and return loss

Coaxial interconnects are electrically connected to the coaxial transceivers on the PCB. Specification of SP2 already includes ECC output characteristic and potential losses due to board traces, passive components and board connector. SP3 represents signal characteristic at the end of a coaxial interconnect, terminated with the optimum value of 50 Ω. Potential signal degradation due to board traces, passive components and board connector between SP3 and CEC-input shall be considered additionally. The combination of board traces, passive components, and board connector is called analogue front end (AFE). In some cases, the length of the electrical connection between device connector and the CEC/ECC could be long enough to adversely affect the signal integrity.

Table 20 specifies the PCB-interface impedance and L_{RL} parameters.

Table 20 — PCB-interface impedance and L_{RL} parameters

Parameters	Condition	Symbol	Minimum	Typical	Maximum	Unit
Return loss of ECU connector	F = 1 MHz to 450 MHz Cd1[a], Cd2[b], Cd3[c], Cd5[e], Cd6[f]	L_{RL_con}	---	---	-15,6	dB
For simplex: return loss of ECU interface, measured at device connector (see Figure 21)	---	L_{RL_SP2}	---	---	---	---
	A, B, C, D Cd1[a], Cd2[b], Cd5[e], Cd6[f]	L_{RL_SP3}			≤ limit line	---
For duplex: return loss of ECU interface, measured at device connector (see Figure 21)	A, B, C, D Cd1[a], Cd3[c], Cd4[d], Cd5[e], Cd6[f]	$L_{RL\_SP2\_SP3}$	---	---	≤ limit line	---

[a] Environmental conditions or mechanical stress being applied to the coaxial interconnect lead to parameter variations. Refer to 10.1 and 11.3 for operating conditions.

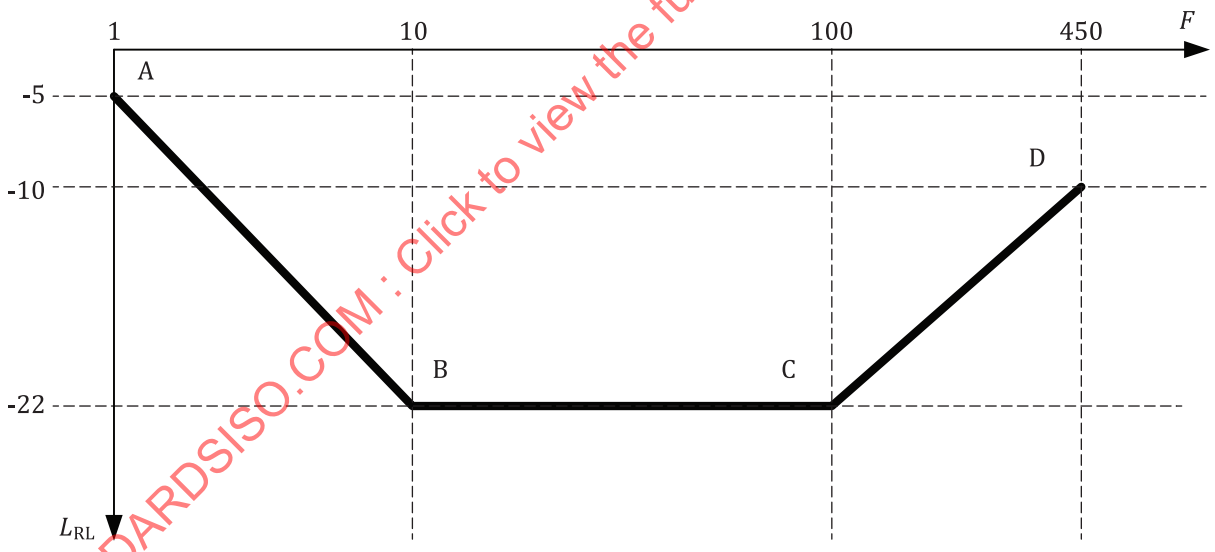
[b] For simplex only.

[c] For duplex only.

[d] Relevant for accumulated return loss.

[e] Measured using $t_{riseTDR}$ = 400 ps.

[f] Nominal characteristic impedance 50 Ω.



Key

F frequency [MHz]

L_{RL} return loss [dB]

A to D see Table 21

Figure 21 — PCB interface impedance and RL parameters – Limit line

Table 21 — PCB-interface impedance and return loss parameters – Limit line

Parameter [Key]	Frequency [MHz]	Return loss [dB]
A	1	-5
B	10	-22
C	100	-22
D	450	-10

9.5 SP3

The variations in the signal integrity at SP3 are mainly constrained by the definitions of SP2 link quality (see 9.3) and the coaxial interconnect attenuation requirements (see 9.4.1). Stimuli for SP3 can be calculated by filtering a signal representing an SP2 corner condition (minimum/maximum voltage amplitude V_{ss2}, minimum/maximum rise/fall time, etc.) using a filter with a transfer function given by Formula (8). The transfer function parameters A_{DC_loss} and F_{skin} shall be within the allowed range as specified in Table 18.

Further signal degradation at SP3 might occur due to amplitude noise coupled on the data-signal along the link. Amplitude noise reduces signal-to-noise ratio and might also cause jitter on the signal. Potential noise sources in general are EMC and crosstalk from neighbouring signals and reflections. Reflections are caused by impedance mismatches on the transmit link and are controlled by constraining component performances. Potential deterioration by EMC and crosstalk from neighbouring signals is not subject of this document.

Reduction of the noise budget on SP3 due to double reflections is negligible for simplex.

For duplex transmission, impedance mismatches might cause relevant reflections. Transitions of a downstream signal cause reflections, which accumulate over a link and add to the upstream data signal. A limitation for signal-to-noise ratio is inherently given by the specification of components return loss (see 9.4.2.2 and 9.4.2.3), the definition of accumulation of relevant return loss (see Formula (13)), and by the specification of maximum attenuation (see 9.4.1).

9.6 SP4

The signal at SP4 shall meet the requirements in Table 22 and shall remain outside the keep-out areas of the mask. Refer to 10.1, 11.3 and Clause 12 for operating conditions and interface standards.

Table 22 specifies the link quality parameters of SP4.

Table 22 — Link quality parameters of SP4

Link quality parameters of SP4	Condition	Symbol	Minimum	Typical	Maximum	Unit
Transferred jitter	Cd1[a]	J_{tr4}	---	---	230	ps
Eye mask (see Figure 22)	Cd2[b], Cd3[c], Cd4[d]	A_4 to H_4	---	---	---	---

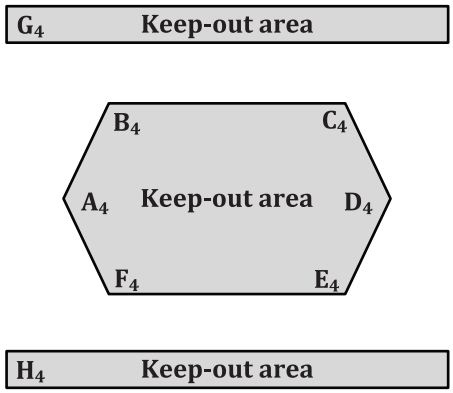
[a] Use the jitter filter specified in 8.2.2.

[b] Use the Golden PLL specified in 8.2.1.

[c] The mask parameters include tolerances for overshoot and ringing.

[d] The steady-state differential voltage shall not be less than that specified in TIA/EIA-644-A-2001.

Figure 22 specifies the link quality parameters of the SP4 eye mask.



Key

A_4 to H_4 see Table 23

Figure 22 — Link quality parameters of SP4 - Eye mask

Table 23 specifies the link quality parameters of SP4 - Eye mask.

Table 23 — Link quality parameters of SP4 - Eye mask

Parameter [Key]	Amplitude [mV]	Timing [UI]
A_4	0	0,275
B_4	+148	0,425
C_4	+148	0,575
D_4	0	0,725
E_4	-148	0,575
F_4	-148	0,425
G_4	+636	---
H_4	-636	---

10 Power-on and power-off

10.1 Frequency reference and power supply

The MOST device shall provide the following.

— Frequency reference:

The frequency reference is typically a crystal-controlled oscillator or derivative. The requested accuracy is specified in 12.2.

— Power supply for MNC, ECC and CEC:

— Continuous power supply: V_{CCCN}, with an operating range of 3,3 V ± 0,165 V. This power supply is used to power CEC (or CTR, see 10.3.2).

— Switched power supply: V_{CCSW}, with an operating range of 3,3 V ± 0,165 V, which shall be capable of being switched off. This power supply is used to power the MNC and ECC (or CTR, see 10.3.2).

— Power supply monitoring circuitry: the MOST device shall provide power supply monitoring circuitry for supervising V_{CCSW}, which is specified in 10.2. The MOST device shall connect the active-low reset signal /RST provided by the power supply monitoring circuitry to the /RST inputs of the ECC (CTR) and the MNC.

If the CTR is powered by V_{CCCN} only (see 10.3.2), the /RST signal voltage shall remain below V_{CCSW}.

10.2 Power supply monitoring circuitry

The power supply monitoring circuitry:

— shall provide an active-low reset signal /RST that is a valid LVTTL (JESD8C) signal over the power supply range V_{VALID} specified in Table 24.

— shall set the /RST signal to logic 1 when the power supply voltage ramps above V_T. Switching from logic 0 to logic 1 shall be delayed by a minimum time of t_{D+} to allow the circuitry in the ECC to stabilize, the LVDS pins of the MNC to be driven, and the local frequency reference to stabilize. Although a maximum time for t_{D+} is not specified, an implicit maximum value exists due to the required start-up time.

— shall set the /RST signal to logic 0 when the voltage drops below V_T. Switching from logic 1 to logic 0 shall occur within a time of t_{D-}.

Table 24 specifies the /RST signal parameters.

Table 24 — /RST signal parameters

Parameter	Condition	Symbol	Minimum	Typical	Maximum	Unit
Supply range for valid logic levels	---	V_{VALID}	1	---	3,465	V
Logic switching threshold	---	V_T	2,970	---	---	V
Logic 0 to logic 1 time delay	---	t_{D+}	1	---	---	ms
Logic 1 to logic 0 time delay	---	t_{D-}	0	---	100	µs

10.3 Coaxial transceiver ECC and CEC

10.3.1 General

Wake-up and shutdown methods of the MOST network require certain functionality to be built into the ECC and CEC of a coaxial transceiver.

10.3.2 CTR requirements

If a CTR has only one power domain (common power supply for ECC and CEC)

— it shall fulfil $I_{CCSLEEP}$ requirements defined in Table 26 during off-state with /RST signal set to logic 0 and

— it shall fulfil all the requirements for ECC and CEC, where all power supply related parameters (V_{ECCOR}, V_{ECCGR}, V_{ECCOFF}, V_{CECOR}) are referred to the actual CTR power supply used.

10.3.3 ECC requirements

The ECC functional requirements are listed below.

a) The ECC shall have an LVTTL (JESD8C) active-low reset input pin (/RST).

b) The ECC shall be capable of performing transition detection at its input. Transition detection is the ability to monitor the input frequency of the signal at SP1 and determine whether the frequency meets the specifications of F_{OFF1} or F_{ON1}.

c) The off-state for the ECC is defined as follows:

— the ECC shall not generate output transitions;

— the ECC shall perform transition detection at SP1 in order to check for a valid wake-up condition, defined as the input signal frequency being within F_{ON1}.

d) The on-state for the ECC is defined as follows:

— the ECC shall produce an output signal that is compliant with all the SP2 parameters defined in Table 16 when being driven by valid SP1 data;

— the ECC shall perform transition detection at SP1 in order to check for a valid shutdown condition, defined as the input signal frequency being within F_{OFF1}.

e) The ECC shall not generate any output, capable of waking up a following device, when being supplied with an operating voltage within V_{ECCOFF} regardless of the state of the SP1 and /RST inputs.

f) The ECC shall not generate any output transitions when the /RST input is logic 0.

g) When being supplied with an operating voltage within V_{ECCGR}, the internal circuitry of the ECC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+}.

h) When being supplied with an operating voltage within V_{ECCOR}, the ECC shall settle into operation defined as the on-state, within a time t_{ON2} when:

— the /RST signal is set to logic 1 and

— the frequency of the SP1 signal is within F_{ON1} (transition detection).

i) When being supplied with an operating voltage within V_{ECCGR}, the ECC shall be capable of performing transition detection and shall enter the off-state, within a time t_{OFF2} when:

— the /RST signal is set to logic 0 or

— the frequency of the SP1 signal is within F_{OFF1} (transition detection).

j) In the frequency range F_{ON1}, the ECC shall be in the on-state. In the frequency range F_{OFF1}, the ECC shall be in the off-state. The transition is performed between F_{OFF1} maximum and F_{ON1} minimum.

The ECC power state parameter requirements are summarized in Table 25. Refer to Figure 23 for more details.

Table 25 — ECC power state parameters

Parameter	Condition	Symbol	Minimum	Typical	Maximum	Unit
ECC operating voltage range	---	V_{ECCOR}	3,135	3,300	3,465	V
ECC glitch-safe voltage range	---	V_{ECCGR}	2,970	---	3,465	V
ECC off-state voltage range	---	V_{ECCOFF}	0	---	1	V
ECC on-state frequency range at SP1	Cd1[a]	F_{ON1}	12	---	73,743	MHz
ECC off-state frequency range at SP1	---	F_{OFF1}	0	---	10	kHz
ECC power-on delay	Cd2[b]	t_{ON2}	---	---	400	µs
ECC output settle	---	t_{OS2}	---	---	5	µs
ECC power-off delay	---	t_{OFF2}	---	---	2	µs

[a] Above this frequency, the ECC may remain in the on-state.

[b] t_{ON2} includes t_{OS2}.

Figure 23 shows the ECC timing diagram.

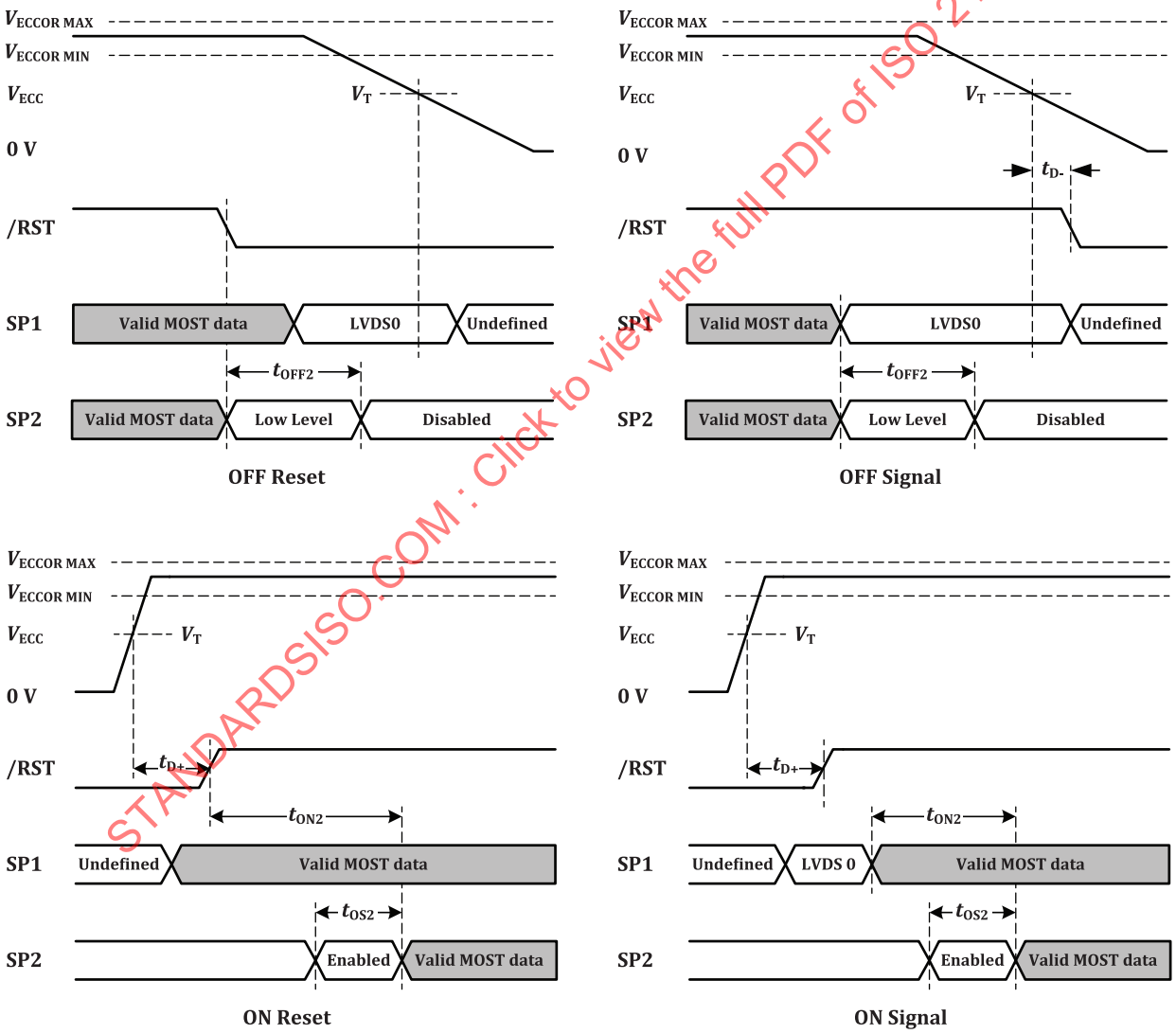


Figure 23 — ECC timing diagram

10.3.4 ECC power-on and power-off sequence

10.3.4.1 General

A typical power-on sequence and a typical power-off sequence for the ECC are described below. Figure 23 shows an ECC timing diagram. Valid MOST data is specified as follows:

— for SP1, valid MOST data shall be DCA encoded data according to the link quality parameters specified in Table 14 and the bit rate requirements specified in Table 31;

— for SP2, valid MOST data shall be DCA encoded data according to the link quality parameters specified in Table 16 and the bit rate requirements specified in Table 31.

10.3.4.2 Power-on sequence example scenario

The power-on sequence starts with the power supply voltage to the MNC and ECC ramping up. During the time at which the power supply voltage is not within the ECC's normal operating range, the /RST signal is set to logic 0 by the power supply monitoring circuitry to prevent edges from being generated at SP2. After the supply voltage reaches its normal operating level, the circuitry inside the MNC and ECC might not be stabilized. The power supply monitoring circuitry provides a delay from the time when the supply voltage reaches its normal operating value until /RST transitions to logic 1 so that the local frequency reference, MNC circuitry, and ECC circuitry have time to stabilize. Some time after the power supply reaches its typical value, the local frequency reference that provides the MNC with timing stabilizes, and valid LVDS logic levels are generated by the MNC at SP1. Once the proper frequency is detected at SP1, and /RST is logic 1, the ECC can then drive valid data on SP2 after an allowed short period of undefined data due to the AC-coupling between the output of the ECC and SP2. During this undefined data period the signal is balanced, making use of the DC-balancing of the DCA data signal.

10.3.4.3 Power-off sequence example scenario

The normal power-off sequence is initiated by SP1 data being driven to logic 0 by the MNC. The ECC detects this event using its internal transition detection circuit and disables the output by driving SP2 to the voltage range V_{ECCOFF} within the required time. The power supply to the ECC is shut down some time later. During the ramp down of the power supply, the /RST signal transitions to logic 0 before the ECC's power supply drops below the glitch-safe voltage range, preventing any glitches on the output at SP2. The /RST signal is valid down to the minimum of V_{VALID}. Below the minimum of V_{VALID}, the ECC is responsible for preventing any signal oscillations at SP2 regardless of the state of /RST.

10.3.5 CEC requirements

10.3.5.1 CEC functional requirements

The CEC functional requirements are listed below. These requirements are applicable for the CEC when being powered by an operating voltage in the range defined by *V*CECOR in Table 26.

a) The CEC shall provide an output pin (STATUS) in accordance with LVTTL (follow JEDEC No. JESD8C.01).

b) A CEC in the off-state:

— shall keep its STATUS logic 1, the SP4 bus disabled, and consume no more than the sleep current, $I_{CCSLEEP}$;

— shall monitor the amplitude and frequency at SP3.

c) A CEC in the on-state:

— shall keep its STATUS logic 0 and shall provide valid output data that meets all the SP4 specifications in Table 22 when receiving valid data at SP3;

— shall monitor the amplitude and frequency at SP3.

d) A CEC shall transition from the off-state to the on-state upon detecting valid wake-up conditions, defined as an SP3 signal with a frequency within F_{ON3} as specified in Table 26. The wake-up procedure has the following requirements:

— the CEC shall set the STATUS to logic 0 within time t_{STATF} after valid wake-up conditions are detected at SP3;

— the CEC shall enable the SP4 LVDS bus and produce a valid LVDS signal within time t_{LVDSV4} after setting STATUS to logic 0;

— the CEC shall enter the on-state within time t_{ON4} after the valid wake-up condition is detected.

e) A CEC in the on-state shall constantly monitor the input signal frequency and input amplitude. A CEC shall transition to the off-state upon detecting valid shutdown conditions. When the signal at SP3 has a frequency within F_{OFF3} as specified in Table 26 or an SP3 amplitude that is too low (see 9.3 and 9.4.1), the CEC shall transition to the off-state. The transition procedure to the off-state has the following requirements:

— the CEC shall force the signal at SP4 to LVDS 0 and set STATUS to logic 1 within a time t_{STATR} upon detecting valid shutdown conditions on SP3; additionally, the CEC shall maintain a valid LVDS signal during the detection phase;

— the CEC shall maintain its LVDS output at a logic 0 for a hold time of t_{LVDSH4} after STATUS transitions to logic 1;

— the CEC shall enter the off-state within time t_{OFF4} after the valid shutdown conditions occur.

f) While F_{ON3} defines the frequency range where the CEC shall be in on-state and F_{OFF3} defines the frequency range where the CEC shall be in off-state, the actual transition points are in the region between F_{OFF3} maximum and F_{ON3} minimum.

The CEC shall meet the requirements listed in Table 26. Refer to Figure 24 for more details.

10.3.5.2 CEC power state requirements

Table 26 specifies the CEC power state parameter requirements.

Table 26 — CEC power state parameters

CEC power state parameter		Condition	Symbol	Minimum	Typical	Maximum	Unit
Power-on	Frequency range of input at SP3 for on-state operation	Cd1[a]	F_{ON3}	12	---	73,743	MHz
	CEC power-on delay	Cd2[b]	t_{ON4}	---	---	9,7	ms
	Delay to STATUS falling	Cd3[c]	t_{STATF}	200	---	700	µs
	STATUS falling to LVDS valid	---	t_{LVDSV4}	---	---	100	µs
	CEC operating voltage range	---	V_{CECOR}	3,135	3,300	3,465	V
Power-off	Frequency range of input at SP3 for off-state operation	---	F_{OFF3}	0	---	10	kHz
	CEC power-off delay	Cd4[d]	t_{OFF4}	---	---	1	ms
	CEC LVDS hold time	---	t_{LVDSH4}	1	---	---	µs
	Delay to STATUS rising	Cd5[e], Cd6[f]	t_{STATR}	---	---	2	µs
		Cd5[e], Cd7[g]		---	---	7	µs
	Current consumption in the off-state	---	$I_{CCSLEEP}$	---	---	30	µA

a Above this frequency, the CEC may remain in the on-state.

b t_{ON4} is the sum of t_{STATF}, t_{LVDSV4} and an additional time required for SP4 to receive valid MOST data.

c It is the time from valid wake-up condition to STATUS logic 0, see 10.3.5.1 d).

d t_{OFF4} is the sum of t_{STATR} and t_{LVDSH4}.

e it is the time from detection of valid shutdown conditions at SP3 to STATUS logic 1, see 10.3.5.1 e).

f For stand-alone MOST transceivers.

g For integrated MOST transceivers.

Figure 24 shows the CEC timing diagram.

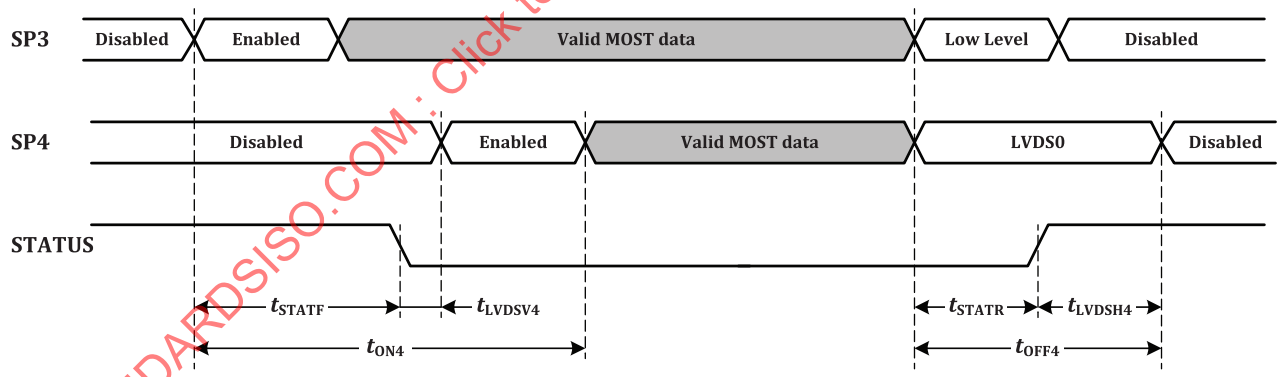


Figure 24 — CEC timing diagram

10.3.6 CEC power-on and power-off sequence

10.3.6.1 General

The typical sequences explained below provide a description of the timing shown in Figure 24. Initially it is assumed that the CEC is powered but it is in its off-state with STATUS logic 1 and the SP4 bus disabled. In Figure 24, valid MOST data is defined as follows:

— for SP3, valid MOST data shall be DCA encoded data according to the link quality parameters specified in 9.4.2.2 and the bit rate requirements specified in Table 31;

— for SP4, valid MOST data shall be DCA encoded data according to the link quality parameters specified in Table 22 and the bit rate requirements specified in Table 31.

10.3.6.2 Power-on sequence example scenario

A CEC that is in the off-state monitors the SP3 signal. The CEC verifies that the amplitude and signal frequency meet specifications before exiting the off-state. If valid wake-up conditions are present, the CEC sets STATUS to logic 0 and enables the SP4 LVDS bus. After a settling time, valid LVDS logic levels are present although valid MOST data may not be on the bus yet. After a short period, the CEC is on and valid MOST data is on the SP4 bus.

10.3.6.3 Power-off sequence example scenario

In the on-state, a CEC monitors the signal frequency at SP3. If the frequency does not meet specifications, the CEC begins transitioning to the off-state by setting the SP4 output to LVDS 0 and the STATUS to logic 1. The SP4 bus is then maintained at LVDS 0 for a hold time while STATUS is logic 1. After this hold time, the CEC disables the SP4 bus and enters the off-state.

11 MOST network requirements

11.1 SP4 receiver tolerance

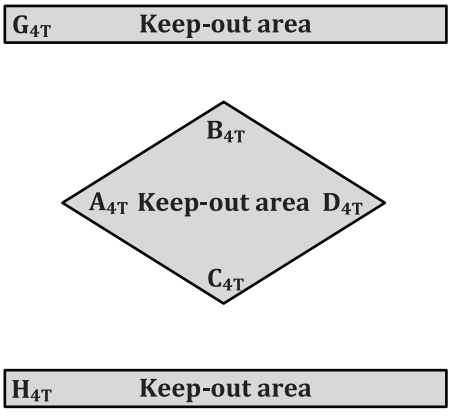
All MOST components along the link shall operate with a bit error rate (BER) lower than 10^{-9}. See 10.1, 11.3, and Clause 12 for operating conditions and interface standards.

Table 27 defines the receiver tolerance parameters of SP4.

Table 27 — Receiver tolerance parameters of SP4

Receiver tolerance SP4	Condition	Symbol	Minimum	Typical	Maximum	Unit
Eye mask (see Figure 25)	Cd1[a], Cd2[b], Cd3[c]	A_{4T} to H_{4T}	---	---	---	---
[a] Use the Golden PLL as specified in 8.2.1.						
[b] The difference between the SP4 eye mask and the SP4 receiver tolerance eye mask in the horizontal timing direction is due to accumulated jitter along the link.						
[c] Additional vertical closure on the mask is caused by the large amount of jitter present on the signal. The signal shall still comply with the LVDS specification regarding the minimum signal amplitude.						

Figure 25 shows the receiver tolerance parameters of SP4 - Eye mask.



Key

A_{4T} to H_{4T} see Table 28

Figure 25 — Receiver tolerance parameters of SP4 – Eye mask