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Road vehicles — In-vehicle Ethernet —

Part 6: Electrical 100-Mbit/s physical entity requirements and conformance test plan

Véhicules routiers — Ethernet embarqué —

Partie 6: Exigences et plan de tests de conformité de l'entité physique à 100-Mbit/s électrique

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT), see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21111 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The ISO 21111 series includes in-vehicle Ethernet requirements and test plans that are disseminated in other International Standards and complements them with additional test methods and requirements. The resulting requirement and test plans are structured in different documents following the Open Systems Interconnection (OSI) reference model and grouping the documents that depend on the physical media and bit rate used.

In general, the Ethernet requirements are specified in ISO/IEC/IEEE 8802-3. The ISO 21111 series provides supplemental specifications (e.g. wake-up, I/O functionality), which are required for in-vehicle Ethernet applications. In road vehicles, Ethernet networks are used for different purposes requiring different bit-rates. Currently, the ISO 21111 series specifies the 1-Gbit/s optical and 100-Mbit/s electrical physical layer.

The ISO 21111 series contains requirement specifications and test methods related to the in-vehicle Ethernet. This includes requirement specifications for physical layer entity (e.g. connectors, physical layer implementations) providers, device (e.g. electronic control units, gateway units) suppliers, and system (e.g. network systems) designers. Additionally, there are test methods specified for conformance testing and for interoperability testing.

Safety (electrical safety, protection, fire, etc.) and electromagnetic compatibility (EMC) requirements are out of the scope of the ISO 21111 series.

The structure of the specifications given in the ISO 21111 series complies with the Open Systems Interconnection (OSI) reference model is specified in ISO/IEC 7498-1[1] and ISO/IEC 10731[3].

ISO 21111-1 defines the terms which are used in this series of standards and provides an overview of the standards for in-vehicle Ethernet including the complementary relations to ISO/IEC/IEEE 8802-3 and the amendments, the document structure, type of physical entities, in-vehicle Ethernet specific functionalities, and so on.

ISO 21111-2 specifies the interface between reconciliation sublayer and physical entity including reduced gigabit media independent interface (RGMII), and the common physical entity wake-up and synchronised link sleep functionalities, independent from physical media and bit rate.

ISO 21111-3 specifies supplemental requirements to a physical layer capable of transmitting 1-Gbit/s over plastic optical fibre compliant with ISO/IEC/IEEE 8802-3, with specific application to communications inside road vehicles, and a test plan for physical entity conformance testing.

ISO 21111-4[3] specifies the optical components requirements and test methods for 1-Gbit/s optical in-vehicle Ethernet.

ISO 21111-5 specifies, for 1-Gbit/s optical in-vehicle Ethernet, requirements on the physical layer at system level, requirements on the interoperability test set-ups, the interoperability test plan that checks the requirements for the physical layer at system level, requirements on the device-level physical layer conformance test set-ups, and device-level physical layer conformance test plan that checks a set of requirements for the OSI physical layer that are relevant for device vendors.

This document specifies advanced features of an ISO/IEC/IEEE 8802-3 in-vehicle Ethernet physical layer (often also called transceiver), e.g. for diagnostic purposes for in-vehicle Ethernet physical layers. It specifies advanced physical layer features, wake-up and sleep features, physical layer test suite, physical layer control requirements and conformance test plan, physical sublayers test suite, and physical sublayers requirements and conformance test plan.

ISO 21111-7 specifies the implementation for ISO/IEC/IEEE 8802-3, which defines the interface implementation for automotive applications together with requirements on components used to realize this Bus Interface Network (BIN). ISO 21111-7 also defines further testing and system requirements for systems implemented according to the system specification. In addition, ISO 21111-7 defines the channels for tests of transceivers with a test wiring harness that simulates various electrical communication channels.

ISO 21111-8 specifies the transmission media, the channel performance, and the tests for an ISO/IEC/IEEE 8802-3 in-vehicle Ethernet.

ISO 21111-9 specifies the data link layer requirements and conformance test plan. It specifies the requirements and test plan for devices and systems with bridge functionality.

ISO 21111-10 specifies the application to session layer requirements and conformance test plan. It specifies the requirements and conformance test plan for devices and systems that include functionality related with OSI layers from 7 to 5.

ISO 21111-11 specifies the transport to network layer requirements and conformance test plan. It specifies the requirements and conformance test plan for devices and systems that include functionality related with OSI layers from 4 and 3.

Figure 1 shows the parts of the ISO 21111 series and the document structure.

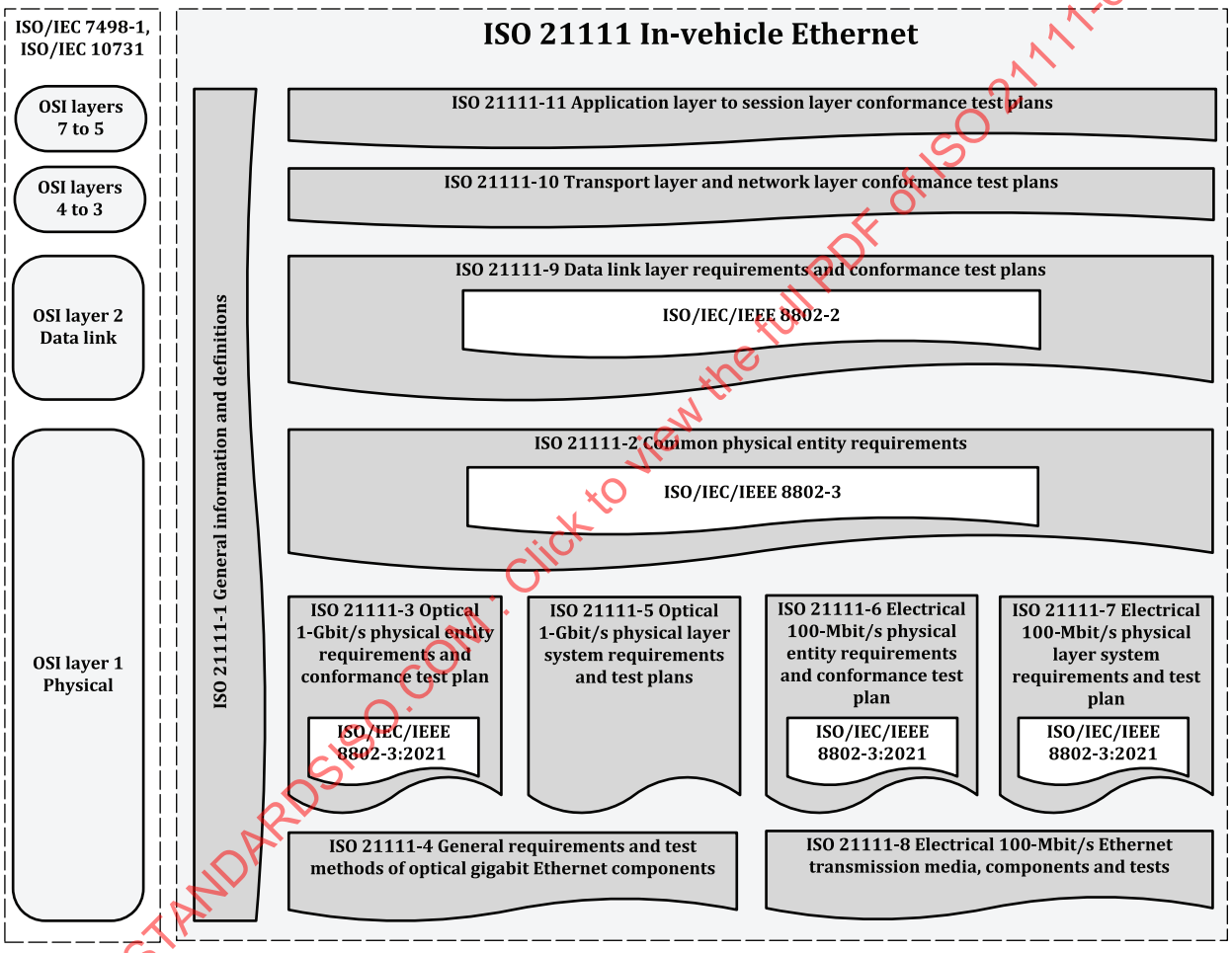


Figure 1 — In-vehicle Ethernet document reference according to OSI model

Road vehicles — In-vehicle Ethernet —

Part 6: Electrical 100-Mbit/s physical entity requirements and conformance test plan

1 Scope

This document specifies advanced features of an ISO/IEC/IEEE 8802-3 automotive Ethernet PHY (often also called transceiver), e.g. for diagnostic purposes for automotive Ethernet PHYs.

This document specifies:

— advanced PHY features;

— wake-up and sleep features;

— PHY test suite;

— PHY control IUT requirements and conformance test plan;

— PCS test suite;

— PCS IUT requirements and conformance test plan;

— PMA test suite; and

— PMA IUT requirements and conformance test plan.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 9646-1, *Information technology — Open Systems Interconnection — Conformance testing methodology and framework — Part 1: General concepts*

ISO 21111-1, *Road vehicles — In-vehicle Ethernet — Part 1: General information and definitions*

ISO 21111-2, *Road vehicles — In-vehicle Ethernet — Part 2: Common physical entity requirements*

ISO/IEC/IEEE 8802-3:2021, *Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks — Part 3: Standard for Ethernet*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21111-1, ISO/IEC 9646-1 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

3.1
automotive cable
balanced 100-Ω one pair cable having characteristics defined in ISO/IEC/IEEE 8802-3:2021, 96.7 physical layer specifications and management parameters for 100-Mbit/s operation over a single balanced twisted pair cable

3.2
short automotive cable
cable complying with *automotive cable* (3.1) used for test purposes and limited in length to reduce the amount of loss between the IUT transmitter and test and measurement equipment

3.3
PHY frame
normal data transmission consisting of SEND_N code groups defined in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.7 and which begins with a valid start-of-stream delimiter (SSD) and ends with a valid end-of-stream delimiter (ESD)

3.4
monitor
test system used to capture and decode the transmissions from the IUT

Note 1 to entry: See B.2.

4 Symbols and abbreviated terms

4.1 Symbols

–	empty table cell or feature undefined
L_{CL}	longitudinal conversion loss ($\frac{Sdc11}{Sdc22}$)
L_{CTL}	longitudinal conversion transmission loss
P_{SD}	power spectral density
T_{CL}	transverse conversion loss
T_{CTL}	transverse conversion transmission loss
X_2	binary wild card value representation

4.2 Abbreviated terms

ADC	analogue to digital converter
AFEXTDC	alien far end cross conversion loss common to differential
ANEXTDC	alien near end cross conversion loss common to differential
AWGN	additive white Gaussian noise
BER	bit error rate
BI_DA	bi-directional data signal pair A
COM	communication ready (status bit)
COR	polarity correct

CTC	conformance test case
CTP	conformance test plan
Cvt	convention
DCQ	dynamic channel quality
DD	defect distance
DET	polarity detection
DSP	digital signal processing
ECU	electronic control unit
GMII	gigabit media independent interface
HDD	harness defect detection
ICMP	Internet Control Message Protocol
IOL	interoperability laboratory
IUT	implementation under test
LCL	longitudinal conversion loss
LCTL	longitudinal conversion transmission loss
LFL	link failures and losses
LP	link partner
LPF	low-pass filter
LQ	link quality
LRT	local receiver time
LTT	link-training time
LU	link-up time
M	mandatory
MAC	media access control
MDC	management data clock
MDI	medium dependent interface
MII	media independent interface
MSE	mean square error
MSE_WC	mean square `error_worst-case`
O	optional
OS	OPEN/SHORT detection

PAM3	pulse amplitude modulation (3 level)
PCB	printed circuit board
PCS	physical coding sub-layer
PEC	pulse error correction
PHY	physical layer
pMSE	peak MSE
PLL	phase locked loop
POL	polarity (detection and correction)
PSAACRF	power sum attenuations to alien crosstalk ratio far end
PSANEXT	power sum alien near end crosstalk loss
PSD	power spectral density
RBW	resolution bandwidth
RGMII	reduced gigabit media independent interface
RRT	remote receiver time
SA	RF spectral analyser
SNR	signal to noise ratio
SQI	signal quality index
TDR	time domain reflectometer
TIE	time interval error
UI	unit interval
VBW	video bandwidth
VNA	RF network analyser

5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[2].

6 Wake-up and sleep features

6.1 Extension of physical coding sub-layer

This subclause describes the modification of the physical coding sub-layer of ISO/IEC/IEEE 8802-3:2021.

REQ	1.1 Wake-up and sleep features – Extension of physical coding sub-layer
Figure 2 specifies the state diagram of the power state machine, which implements the two-way handshake protocol.	

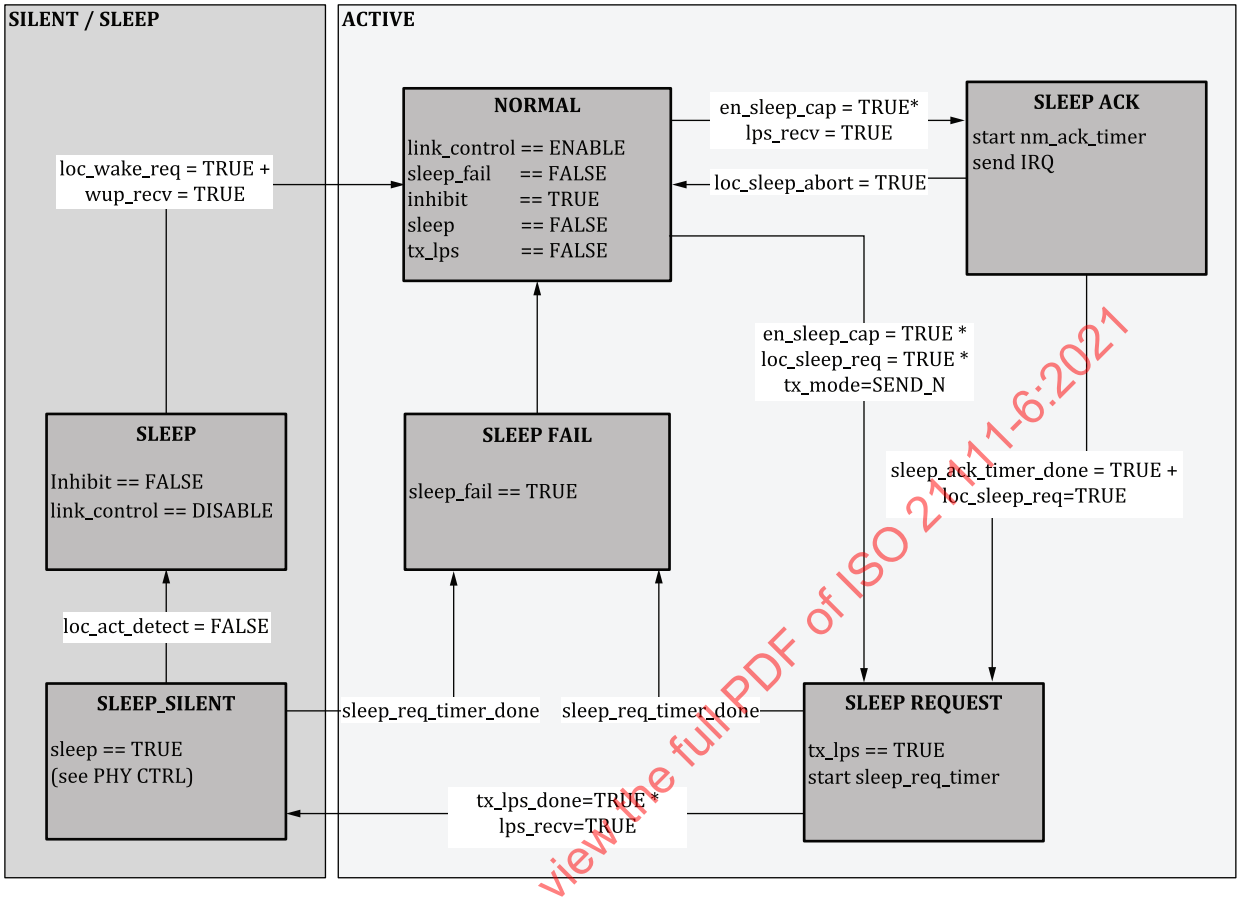


Figure 2 — Power sequencing ISO/IEC/IEEE 8802-3:2021

In case the link is up (`tx_mode = SEND_N`) and `Sleep.request` is asserted, the PHY enters the `Sleep.Request` state and sends LPS commands. The link partner receiving those LPS commands enters `SLEEP_ACK` state and starts `sleep_ack_timer`. If `loc_sleep_abort` is asserted, the sleep is aborted because of an incoming data message. If sleep reject is not done, the link partner enters `SLEEP_REQUEST` state and sends LPS commands. If the PHY detects that it sends and receives LPS commands, it transits to `SLEEP_SILENT` state and eventually to `SLEEP`. On the other hand, if the handshaking is not done before the `sleep_req_timer` timeout, the PHY enters `SLEEP_FAIL` and transits back to `SEND IDLE OR DATA` state.

The signalling of a Wakeup.request depends on the state of the link. If the link is up (`tx_mode = SEND_N`) the PHY transmits a WUR command over the active link during `IDLE` times. If the link is down (`tx_mode = SEND_N`) the PHY transmits a WUP pulse. If the link is not yet established (`!loc_rcvr_status`), for instance because the link is still in training (`tx_mode = SEND_I`), the link is first established, then a WUR command is sent.

REQ	1.2 Wake-up and sleep features – Selective wake-up forwarding mechanism
Multi-PHY devices (e.g. switches) shall implement a selective wake-up forwarding mechanism. If a multi-PHY device detects a `Wakeup.request` (either WUR or WUP) on one port, it shall be possible to forward the request to other PHYs of the device and to any other Single-PHY or Multi-PHY device.	

REQ	1.3 Wake-up and sleep features – Selective wake-up forwarding mechanism Single PHY device

Single-PHY devices shall implement a selective wake-up forwarding mechanism. If a Single-PHY device detects a Wakeup.request (either WUR or WUP), it shall be possible to forward the request to other Single-PHY or Multi-PHY devices.

REQ	1.4 Wake-up and sleep features – wake-up over a passive link (WUP) and active link (WUR)
It shall be possible to forward a wake-up over a passive link (WUP) as well as a wake-up over an active link (WUR) immediately to another port (or PHY).	

The `Wakeup.indicate` should be generated upon wake-up events. In case the link is down, this service primitive is generated upon the reception of WUP pulses (`wup_recv`) or if a local wake-up request (`loc_wake_req`) or a WUR is received (`wur_recv`). The implementation of the energy detection process is left to the PHY vendor.

REQ	1.5 Wake-up and sleep features – Energy detection
The energy detection process shall not take longer than 2 ms.	

REQ	1.6 Wake-up and sleep features – `IDLE` pattern on the link triggers the energy detection
It shall be ensured that any transmitted `IDLE` pattern on the link triggers the energy detection (`wup_recv = TRUE`).	

REQ	1.7 Wake-up and sleep features – PHY detects a wake-up request
If the PHY detects a wake-up request, while the sleep process has already been started, going into sleep shall be terminated and the wake-up shall be processed if possible.	

REQ	1.8 Wake-up and sleep features – Entering the SLEEP state
If the PHY detects a wake-up request while the transit into `SLEEP` state is irreversible, this wake-up request shall be stored and executed immediately upon entering the `SLEEP` state.	

No wakeup request should be lost.

6.2 Service primitives and interfaces

Figure 3 shows the ISO/IEC/IEEE 8802-3:2021 service primitives.

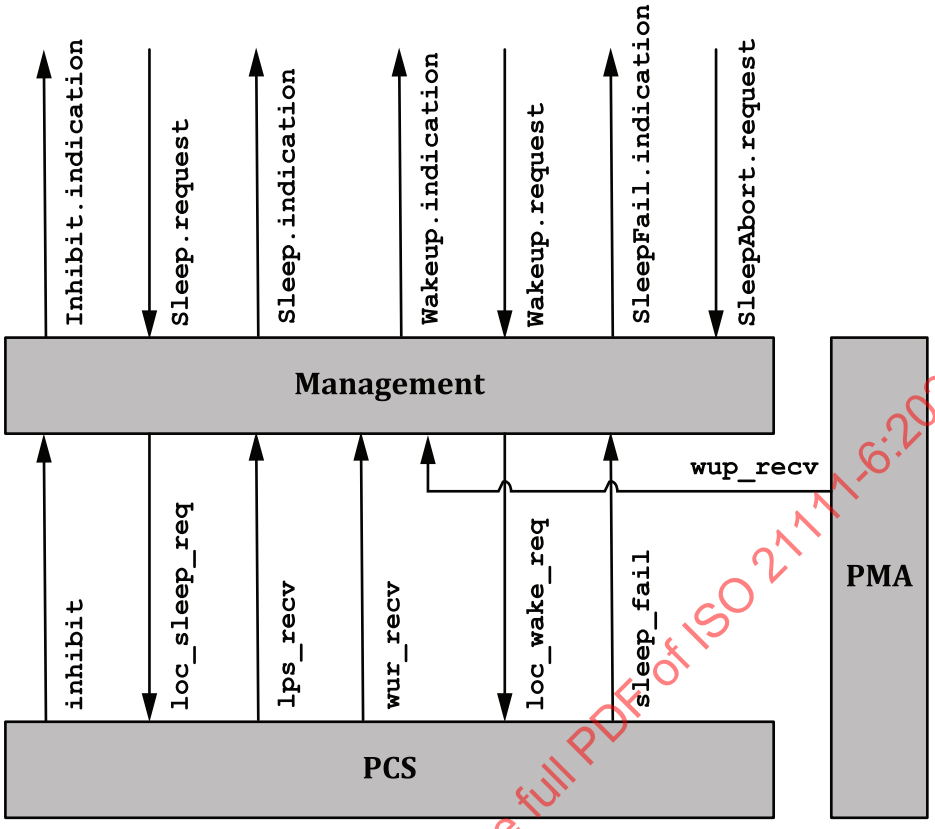


Figure 3 — ISO/IEC/IEEE 8802-3:2021 service primitives

REQ	1.9 Wake-up and sleep features – Mapping between this document and ISO 21111-2 service primitives
Table 1 specifies the mapping between this document and ISO 21111-2 service primitives which shall be followed.	

Table 1 — Mapping between this document and ISO 21111-2 service primitives

ISO 21111-6 (this document) service primitives	ISO 21111-2 service primitives
SleepConfig.request	PHY_ConfigSleepReject.request
Inhibit.indication	PHY_SleepStatus.indication
Sleep.request	PHY_LinkSleep.request
Sleep.indication	PHY_LinkSleepRequestEvent.indication
Wakeup.indication	PHY_WakeUp.indication
Wakeup.request	PHY_WakeUp.request
SleepFail.indication	PHY_LinkSleep.indication
SleepAbort.request	PHY_ LinkSleepRequestAbort.request

6.3 Power sequencing states

The following requirements specify power sequencing states.

REQ	1.10 Wake-up and sleep features – Power sequencing states
The power sequencing states NORMAL, SLEEP_ACK, SLEEP_REQ, SLEEP_SILENT, SLEEP_FAIL and SLEEP shall be implemented as specified in Figure 2.	

REQ	1.11 Wake-up and sleep features – NORMAL state
The NORMAL state shall be the substate of SEND IDLE OR DATA with normal data transmission. On entering NORMAL state, lps_recv and loc_sleep_abort shall be deasserted.	

REQ	1.12 Wake-up and sleep features – SLEEP_ACK state
The SLEEP_ACK state is also a substate of SEND IDLE OR DATA which allows a higher layer implicit acknowledgement during the time sleep_ack_timer. During SLEEP_ACK the sleep handshake can be aborted (loc_sleep_abort = TRUE) and the PHY transitions to NORMAL. The link partner senses the aborted sleep handshake (loc_sleep_abort = TRUE) and the PHY of the IUT transitions to NORMAL. When this happens the link partner sets sleep_req_timer_done and eventually transitions to SLEEP_FAIL.	

REQ	1.13 Wake-up and sleep features –SLEEP_REQ state
The SLEEP_REQ state is entered when the PHY is requested to enter SLEEP state over the LinkSleep.request primitive or after an implicit acknowledgement (sleep_ack_timer_done). In this state it is expected that the peer PHY also sends an LPS to acknowledge the flow. If the PHY has sent its own LPS command and also received LPS, then SLEEP_SILENT is entered. Otherwise the PHY enters SLEEP_FAIL after sleep_req_timer expires.	

REQ	1.14 Wake-up and sleep features – SLEEP_SILENT state
In SLEEP_SILENT the PHYs transmitter remains silent (tx_mode=SEND_Z) but the energy detection circuitry remains disabled to prevent spurious wup_recv glitches. This acts as a safeguard to prevent a mutual wake-up through LPS commands. SLEEP state is entered if both PHYs are silent (loc_act_detect = FALSE).	

REQ	1.15 Wake-up and sleep features – SLEEP_FAIL state
The SLEEP_FAIL state is entered if either one or both PHYs cannot finish handshaking before the sleep_req_timer timeout. The sleep flow is terminated and the PHYs go back to SEND IDLE OR DATA state.	

REQ	1.16 Wake-up and sleep features – SLEEP state
In SLEEP the transmitter shall be powered down and waits for a wake-up pulse or software wake-up.	

6.4 Command definitions

6.4.1 General

This document specifies three commands, which are used to request a power down and signal a wake-up over an active as well as a passive link.

6.4.2 Low power sleep (LPS)

LPS is encoded in the scrambler stream as specified in 6.5.

REQ	1.17 Wake-up and sleep features – Cmd – LPS

The LPS command shall be sent for a minimum of 64 bit.

The detection of an LPS command is left to the implementer. Aborting an LPS command may lead to sending less than 64 bit.

6.4.3 Wake-up request (WUR)

The WUR is encoded in the scrambler stream as specified in 6.4.

REQ	1.18 Wake-up and sleep features – Cmd – WUR
The WUR command shall be sent for a minimum of 64 bit.	

The detection of a WUR command is left to the implementer. Aborting a WUR command may lead to sending less than 64 bit. In addition, the maximum number of hops of a wake-up network is 4.

6.4.4 Wake-up pulse (WUP)

WUP are link-training codes transmitted on the network by a node in `tx_mode = SEND_I` or switch PHY to distribute the wake-up request over a link, which is down. The activity on the twisted-pair lines is detected by the partner PHY as a remote wake-up.

REQ	1.19 Wake-up and sleep features – Cmd – WUP
The wake-up pulse shall have a minimum duration of 1 ms ± 0,3 ms.	

REQ 1.18 allows reliable detection.

The energy detection of a WUP command is implementation-specific.

6.5 Generation of scrambling bits $Sdn[2:0]$

Commands are transmitted in the `IDLE` state of the PCS state machine. Therefore, the side stream scrambler is modified. The generation of $Sd_n[1:0]$ of ISO/IEC/IEEE 8802-3:2021 is modified. The bit $Sd_n[2]$ remains identical to ISO/IEC/IEEE 8802-3:2021.

The bit $Sd_n[1]$ is used to scramble the data bit $tx\_data_n[1]$ during data mode and to encode LPS otherwise. It is defined below.

IF $(tx\_enable_{n-3} = 1)$

$Sd_n[1] = (Sc_n[1] \wedge tx\_data_n[1])$

ELSE IF $((tx\_lps = TRUE) \ \& \ (loc\_wake\_req = FALSE) \ \& \ (tx\_mode = SEND\_N))$

$Sd_n[1] = Sc_n[1] \wedge 1$

ELSE

$Sd_n[1] = Sc_n[1]$

The bit $Sd_n[0]$ is used to scramble the data bit $tx\_data_n[0]$ during data mode and to encode WUR otherwise. It is defined below.

IF $(tx\_enable_{n-3} = 1)$

$Sd_n[0] = (Sc_n[0] \wedge tx\_data_n[0])$

ELSE IF $((tx\_lps = TRUE) \ \& \ (loc\_wake\_req = TRUE) \ \& \ (tx\_mode = SEND\_N))$

$Sd_n[0] = Sc_n[0] \wedge 1$

ELSE

$Sd_n[0] = Sc_n[0]$

6.6 PCS PHY control state diagram

Each variable shall have its own REQ statement with a reference to Figure 4.

REQ	1.20 Wake-up and sleep features – PCS PHY control state diagram
The PCS PHY control state machine, which implements parts of the power sequencing state machine, shall be implemented as specified in Figure 4.	

REQ	1.21 Wake-up and sleep features – PCS PHY control state diagram – Local activity detection signal
The variable `loc_act_detect` shall be set to `FALSE` if consecutive symbols of zeros were received; otherwise shall be set to `TRUE`. The value of `loc_act_detect` shall be set to `TRUE` (`FALSE`) within 1 µs (see Figure 4).	

REQ	1.22 Wake-up and sleep features – PCS PHY control state diagram – Low power sleep received
The variable `lps_recv` shall be set if the LPS command is entirely received (see Figure 4).	

REQ	1.23 Wake-up and sleep features – PCS PHY control state diagram – Wake-up request received
The variable `wur_recv` shall be set if the WUR command is entirely received (see Figure 4).	

REQ	1.24 Wake-up and sleep features – PCS PHY control state diagram – Wake-up pulse received
The variable `wup_recv` shall be set if the WUP pulses are sensed (see Figure 4).	

REQ	1.25 Wake-up and sleep features – PCS PHY control state diagram – Low power sleep transmitted
The variable `tx_lps` shall be set if the LPS bits are transmitted by the scrambler (see Figure 4).	

REQ	1.26 Wake-up and sleep features – PCS PHY control state diagram – Low power sleep transmitted done
The variable `tx_lps_done` shall be set if the LPS command is entirely sent (at least 64-bit) (see Figure 4).	

REQ	1.27 Wake-up and sleep features – PCS PHY control state diagram – Local sleep requested
The variable `loc_sleep_req` shall be set if a a sleep is requested by the local PHY (see Figure 4).	

REQ	1.28 Wake-up and sleep features – PCS PHY control state diagram – Local wake-up requested
The variable `loc_wake_req` shall be set if a wake-up is requested by the local PHY (see Figure 4).	

REQ	1.29 Wake-up and sleep features – PCS PHY control state diagram – Local sleep abort
The variable `loc_sleep_abort` shall be set if a remote sleep request is to be rejected while still in `SLEEP_ACK` state (see Figure 4).	

REQ	1.30 Wake-up and sleep features – PCS PHY control state diagram – Sleep fail
The variable `sleep_fail` shall be set if a sleep handshake is aborted by the link partner (see Figure 4).	

REQ	1.31 Wake-up and sleep features – PCS PHY control state diagram – Inhibit
The variable `inhibit` shall be set if the (external) power supply shutdown is inhibited (see Figure 4).	

REQ	1.32 Wake-up and sleep features – PCS PHY control state diagram – Sleep
The variable `sleep` shall be set by the power state machine to notify PHY CTRL to disable transmission (see Figure 4).	

REQ	1.33 Wake-up and sleep features – PCS PHY control state diagram – Enable sleep capability
The variable `en_sleep_cap` shall be set to `TRUE` when the IUT sleep capability is enabled and set to `FALSE` when the IUT sleep capability is not enabled (see Figure 4).	

REQ	1.34 Wake-up and sleep features – PCS PHY control state diagram – Wake-up timer
The IUT shall use the timer `wup_timer` to wait for reliable detection of a WUP pulse. The timer shall expire 1 ms ± 0,3 ms after being started (see Figure 4).	

REQ	1.35 Wake-up and sleep features – PCS PHY control state diagram – Sleep acknowledge timer
The timer `sleep_ack_timer` shall be used in `SLEEP_ACK` state to check whether NM decides to reject sleep flow on an incoming data message or not. The timer shall expire 8 ms ± 0,8 ms after being started (see Figure 4).	

REQ	1.36 Wake-up and sleep features – PCS PHY control state diagram – Sleep request timer
The timer `sleep_req_timer` shall be set-up in `SLEEP_REQ` to check if the handshaking is done by both PHYs. If the PHY does not enter `SLEEP` state before timeout, it enters `SLEEP_FAIL` state and back to `NORMAL`. The timer shall expire 16 ms ± 1,6 ms after being started (see Figure 4).	

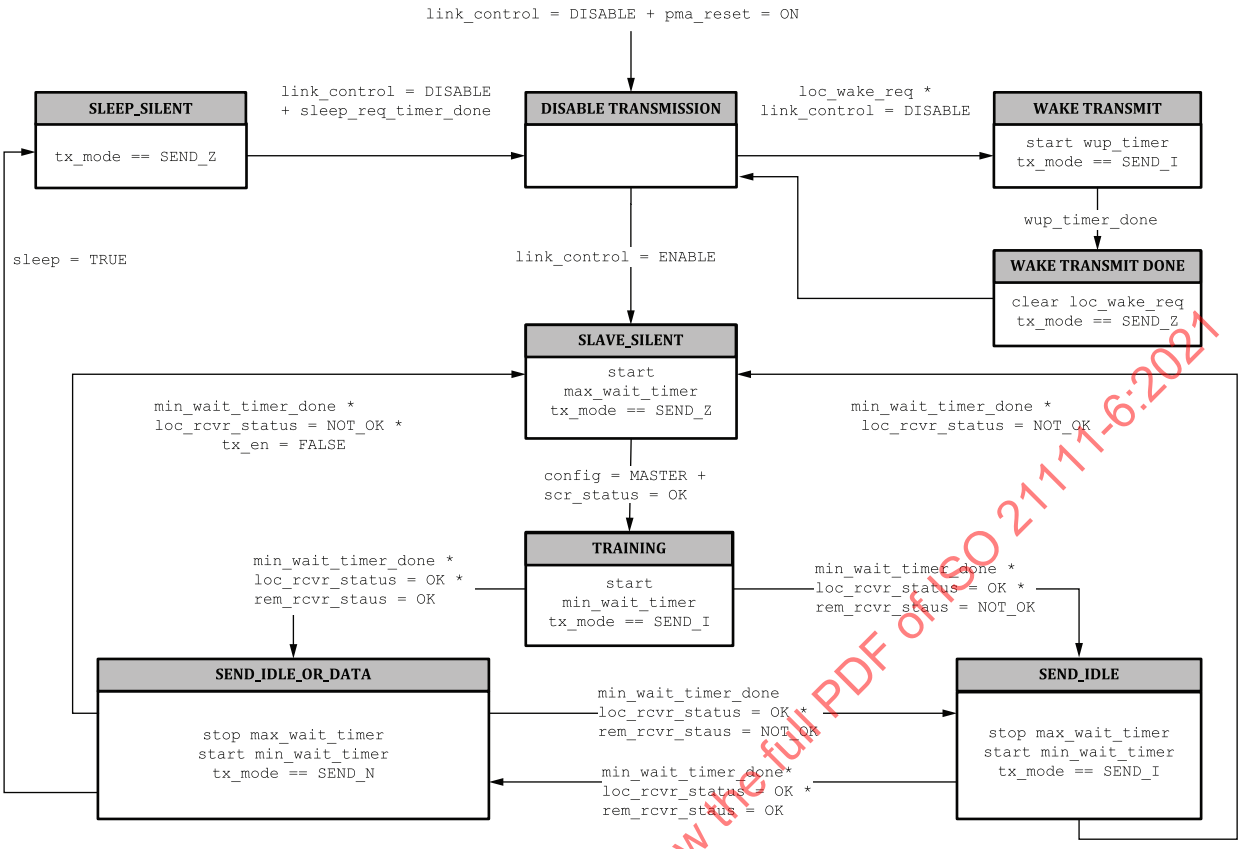


Figure 4 — PHY control state diagram to replace the ISO/IEC/IEEE 8802-3:2021 PHY control state diagram

7 CTP test system and CTC structure

7.1 General

The CTCs specified in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. CTCs are organized into groups, primarily in order to reduce set-up time in the lab environment. The different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the CTCs, where the first number indicates the subclause of Clause 96 of the ISO/IEC/IEEE 8802-3:2021 specification on which the CTP is based. The second and third numbers indicate the CTC's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections.

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

The references specify source material external to the test suite, including specific subsections pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned

in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

7.2 Test system set-up – Transmit test system

The test set-up consists of a test system and a system under test (SUT) connected via the physical medium. The test system implements an UT and a LT. The UT uses the test control protocol (Figure 5 key 2) or the UT point of control and observation (PCO) test system operator to control the LT. The LT supports the functionality required to test the OSI layer (Figure 5 key 5) of the IUT. The test system uses SUT-specific set-up parameters (Figure 5 key 1) for testing the communication with the IUT.

The control and measurement functionality is provided by direct logical access to the service interface (dashed line) (Figure 5 key 3) and the associated parameters of the OSI layer. The UT in the IUT (Figure 5 key 4) supports an equivalent part of the service interface (PCO) (dashed line) (Figure 5 key 3) and the associated parameters to control and measure the state(s) of IUT.

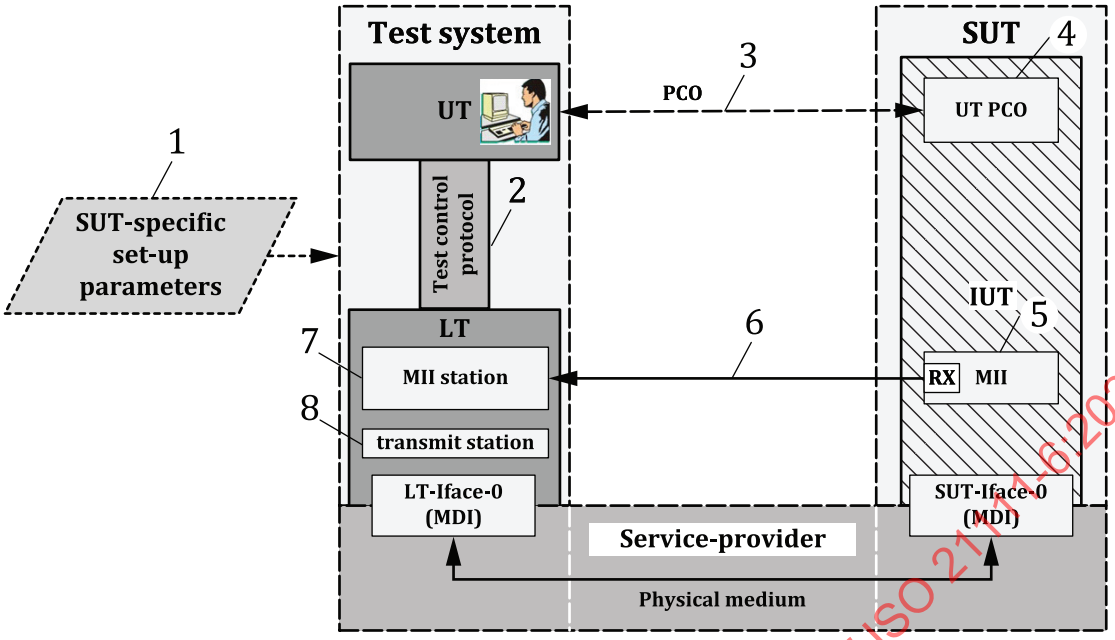
The UT PCO test system operator as part of the UT in the test system manipulates the service interface parameters of the OSI layers to fulfil the purpose of each conformance test case (CTC).

The MII station and the transmit station are part of the LT.

The purpose of the MII station (Figure 5 key 6) is to directly interact with the MII of the IUT (Figure 5 key 8); monitoring (Figure 5 key 5) the RX pins of the IUT MII (Figure 5 key 8), to verify that PHY frames received at the SUT-Iface-0 (MDI) are converted appropriately to bits recognizable by the MAC of the LT.

The purpose of the transmit station (Figure 5 key 7) is to act as a link partner with the IUT. The transmit station transmits ISO/IEC/IEEE 8802-3:2021 PAM3 encoding such that the IUT can achieve a link and receive ternary symbol sequences designed to stress the IUT implementation.

Figure 5 shows the transmit test system set-up.



Key

1 SUT-specific set-up parameters (node's electronic data sheet)
2 test control protocol
3 points of control and observation and abstract service primitives
4 UT PCO test system operator interface
5 IUT MII interface
6 monitoring of the RX pins of the IUT MII interface
7 MII station
8 transmit station (link partner of IUT)

Figure 5 — Test system set-up – Transmit test system

7.3 Test system set-up – Receive test system

The test set-up consists of a test system and a system under test (SUT) connected via the physical medium. The test system implements an UT and a LT. The UT uses the test control protocol (Figure 6 key 2) or the UT point of control and observation (PCO) test system operator to control the LT. The LT supports the functionality required to test the OSI layer (Figure 6 key 5) of the IUT. The test system uses SUT-specific set-up parameters (Figure 6 key 1) for testing the communication with the IUT.

The control and measurement functionality is provided by direct logical access to the service interface (dashed line) (Figure 6 key 3) and the associated parameters of the OSI layer. The UT in the IUT (Figure 6 key 4) supports and equivalent part of the service interface (PCO) (dashed line) (Figure 6 key 3) and the associated parameters to control and measure the state(s) of IUT.

The UT PCO test system operator as part of the UT in the test system manipulates the service interface parameters of the OSI layers to fulfil the purpose of each conformance test case (CTC).

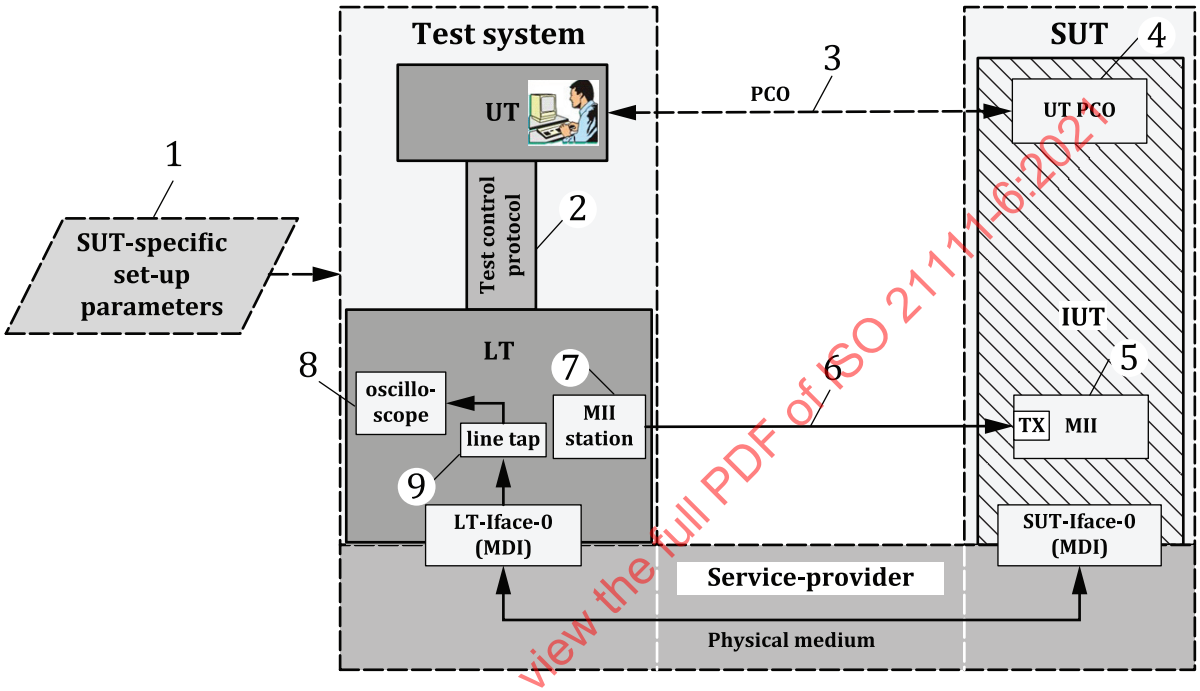
The MII station, line tap, and the oscilloscope are part of the LT.

The purpose of the MII station (Figure 6 key 7) is to directly interact (Figure 6 key 5) with the MII of the IUT; manipulating the TX pins of the IUT MII, to verify that the signals transmitted by the MII station of the LT are properly converted to PAM3 PHY frames transmitted by the IUT MDI via the SUT-Iface-0.

The purpose of the line tap (Figure 6 key 9) is to allow directional monitoring of the signalling from the physical medium. The receive signal from the LT-Iface-0 is then captured on the oscilloscope (Figure 6 key 7).

The purpose of the oscilloscope (Figure 6 key 8) is to measure the PAM3 signalling transmitted by the IUT MDI, allowing for capture and decoding of the ISO/IEC/IEEE 8802-3:2021 ternary symbols.

Figure 6 shows the receive test system set-up.



Key

1 SUT-specific set-up parameters (node's electronic data sheet)
2 test control protocol
3 points of control and observation and abstract service primitives
4 UT PCO test system operator interface
5 IUT MII interface
6 manipulation of IUT MII TX interface
7 MII station
8 oscilloscope measures the PAM3 signalling transmitted by the IUT MDI
9 line tap

Figure 6 — Test system set-up – Receive test system

7.4 CTC structure

CTCs are independent of one another. Each CTC checks the behaviour of the IUT for a particular purpose.

CTCs, which require variations of individual parameters, shall be repeated for each value of the parameter.

The CTC specifications are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Each CTC is specified according to a common CTC structure as shown in Table 2.

Table 2 — CTC structure

Item	Content
CTC # – Name	**CTC_x.y.z-a – CTC structure**
Purpose	The purpose is a brief statement outlining what the test attempts are to achieve. The test is written at the functional level.
Reference	The purpose of the reference is to specify source material external to the test suite, including any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.
Prerequisite	The purpose of the prerequisites is to specify the test hardware and/or software needed to perform the CTC. This is generally expressed in terms of minimum requirements. In some cases, specific equipment manufacturer/model information may be provided.
Set-up	The purpose of the set-up is to describe the initial configuration of the test environment. Small changes in the configuration should not be included here and are generally covered in the test procedure below.
Step	The test procedure includes the test description, which contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing and may be interspersed with observable results. Each test step shall have a numeric number in ascending order.
Iteration	The purpose of the test iterations is to include test procedure definitions, which are repeated more than once.
Expected response	The purpose of the expected response is to describe the expected results to be examined by the tester in order to verify that the IUT is operating. When multiple values for an observable are possible, this description provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.
Remark	The purpose of the remarks is to describe known issues with the test procedure, which can affect test results in certain situations. It can also refer the reader to test suite annexes and/or white papers that can provide more detail regarding these issues.

8 PHY – Control IUT conformance test plan (with MII access)

8.1 PHY – Group 1: PHY control and timers (with MII access)

8.1.1 Overview

The CTCs specified in 8.1 verify the PHY control and timers as specified in ISO/IEC/IEEE 8802-3:2021, 96.4.5. Refer to Annex A for additional low-level technical details about the PHY control test suite.

8.1.2 CTC_4.1.1 – PMA reset (with MII access)

The PMA reset function causes the transition to the `LINK DOWN` state and the IUT should set `link_status = FAIL`.

Table 3 specifies the CTC_4.1.1 – PMA reset (with MII access).

Table 3 — CTC_4.1.1 – PMA reset (with MII access)

Item	Content
CTC # – Name	CTC_4.1.1 – PMA reset (with MII access)
Purpose	This CTC verifies that the PMA initialises upon receipt of a reset request from the management entity.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.4.1 PMA reset function

Table 3 *(continued)*

Item	Content
Prerequisite	The UT shall have access to the PMA reset. The UT shall have access to the `link_status`[a]. The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap or to the test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall establish a valid link with the IUT. 3. The LT shall monitor the transmissions from the IUT and shall cause the management to request a PMA reset while simultaneously ceasing transmissions from the LT. 4. The UT shall configure the IUT as SLAVE. 5. The LT shall establish a valid link with the IUT. 6. The LT shall monitor the transmissions from the IUT and shall cause the management to request a PMA reset while simultaneously ceasing transmissions from the LT.
Iteration	Not applicable
Expected response	After step 3: The IUT stops transmitting with `tx_mode = SEND_N` and starts transmitting with `tx_mode = SEND_I`. The IUT sets `link_status = FAIL`. After step 6: The IUT stops transmitting. The IUT sets `link_status = FAIL`.
Remark	[a] The delay from the internal setting of `link_status` to the externally observable `link_status` signal shall be defined by the IUT supplier. If the ability to control the PMA reset request is not available, this CTC cannot be performed. If the `link_status` indication is not available, the expected response concerning `link_status = FAIL` cannot be completed. If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested. If it is not possible to synchronise asserting PMA reset and ceasing transmissions from the test system, ensure that the test system does not transmit a sequence that would cause the IUT to set `scr_status = OK` or `loc_rcvr_status = OK`.

8.1.3 CTC_4.1.2 – Value of `minwait_timer – minwait_timer` in `TRAINING` state (with MII access)

Table 4 specifies the CTC_4.1.2 – Case 1 – Value of `minwait_timer – minwait_timer` in `TRAINING` state (with MII access).

Table 4 — CTC_4.1.2 – Case 1 – Value of `minwait_timer – minwait_timer` in `TRAINING` state (with MII access)

Item	Content
CTC # – Name	CTC_4.1.2 – Case 1 – Value of `minwait_timer – minwait_timer` in `TRAINING` state (with MII access)
Purpose	This CTC verifies that the IUT implements correctly the `minwait_timer` of 1,8 µs ± 0,18 µs.
Reference	ISO/IEC/IEEE 8802-3:2021:

Table 4 *(continued)*

Item	Content
	— 96.4.7.2 timers; — Figure 96-18 PHY control state diagram; — Figure 96-19 link monitor state diagram.
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system (see Figure 5 key 7) and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. UT PCO test system operator shall configure the IUT as MASTER or as SLAVE. 2. The LT shall monitor the transmissions from the IUT and shall restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT establishes a link. 3. The LT shall start transmitting a valid training signal from the transmit station as soon as the IUT restarts the training process. If the IUT is a MASTER then the transmit test system should begin transmissions with `loc_rcvr_status = OK`. If the IUT is a SLAVE then the transmit test system should not set `loc_rcvr_status = OK` until after the IUT starts transmitting the idle training pattern. 4. The LT shall monitor how long the IUT sends the idle training pattern in the `TRAINING` state before transitioning to the `SEND IDLE OR DATA` state.
Iteration	a) REPEAT step 2 to step 4 with the IUT configured as MASTER, 10 times. b) REPEAT step 2 to step 4 with the IUT configured as SLAVE, 10 times.
Expected response	After step 4 iterations a): The IUT transmits the idle training pattern for 1,8 µs ± 0,18 µs. After step 4 iterations b): The IUT transmits the idle training pattern for 1,8 µs ± 0,18 µs.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested. It also cannot be performed, if the IUT needs longer than the `minwait_timer` to set the `loc_rcvr_status` to `TRUE`.

Table 5 specifies the CTC_4.1.2 – Case 2 – Value of `minwait_timer` – `minwait_timer` in `SEND IDLE OR DATA` state (with MII access).

Table 5 — CTC_4.1.2 – Case 2 – Value of `minwait_timer` – `minwait_timer` in `SEND IDLE` OR `DATA` state (with MII access)

Item	Content
CTC # – Name	CTC_4.1.2 – Case 2 – Value of `minwait_timer` – `minwait_timer` in `SEND IDLE OR DATA` state (with MII access)
Purpose	This CTC verifies that the IUT implements the `minwait_timer` of 1,8 µs and its tolerance.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.4.7.2 timers; — Figure 96-18 PHY control state diagram; — Figure 96-19 link monitor state diagram.
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.

Table 5 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall have the ability to configure the IUT as MASTER or SLAVE. 2. The LT shall monitor the transmissions from the IUT and shall restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall establish a valid link with the IUT, but shall stop transmitting as soon as the IUT transitions to `tx_mode = SEND_N`. 4. The LT shall monitor how long the IUT transmits with `tx_mode = SEND_N` before restarting training.
Iteration	a) REPEAT step 2 to step 4 with the IUT configured as MASTER, 10 times. b) REPEAT step 2 to step 4 with the IUT configured as SLAVE, 10 times.
Expected response	After step 4 iterations a): The IUT transmits with `tx_mode = SEND_N` for at least 1,62 µs and no more than 1 ms. After step 4 iterations b): The IUT transmits with `tx_mode = SEND_N` for at least 1,62 µs and no more than 1 ms.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration is tested. It also cannot be performed if the IUT needs longer than the `minwait_timer` to drop `loc_rcvr_status`.

Table 6 specifies the CTC_4.1.2 – Case 3 – Value of `minwait_timer` – `minwait_timer` between `SEND IDLE` to `SEND IDLE OR DATA` state (with MII access).

Table 6 — CTC_4.1.2 – Case 3 – Value of `minwait_timer – minwait_timer` between `SEND IDLE` to `SEND IDLE OR DATA` state (with MII access)

Item	Content
CTC # – Name	CTC_4.1.2 – Case 3 – Value of `minwait_timer` – `minwait_timer` between `SEND IDLE` to `SEND IDLE OR DATA` state (with MII access)
Purpose	This CTC verifies that the IUT implements the `minwait_timer` of 1,8 µs ± 0,18 µs while in the `SEND IDLE`.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.4.7.2 timers; — Figure 96-18 PHY control state diagram; — Figure 96-19 link monitor state diagram.
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.

Table 6 *(continued)*

Item	Content
Step	1. The UT shall configure the IUT as MASTER or SLAVE. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall establish a valid link with the IUT. 4. The UT shall instruct the LT to transmit with `tx_mode = SEND_I` with `loc_rcvr_status = OK`. 5. The UT shall instruct the LT to transmit with `loc_rcvr_status = NOT_OK` for less than `minwait_timer` as soon as the IUT begins transmitting with `tx_mode = SEND_N`. 6. As soon as the IUT begins transmitting with `tx_mode = SEND_I`, instruct the test system to transmit with `loc_rcvr_status = OK`. 7. The UT shall observe how long the IUT transmits with `tx_mode = SEND_I`.
Iteration	a) REPEAT step 2 to step 7 with the IUT configured as MASTER, 10 times. b) REPEAT step 2 to step 7 with the IUT configured as SLAVE, 10 times.
Expected response	After step 7 iterations a): The IUT transmits with `tx_mode = SEND_I` for 1,8 µs ± 0,18 µs. After step 7 iterations b): The IUT transmits with `tx_mode = SEND_I` for 1,8 µs ± 0,18 µs.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested. It also cannot be performed, if the IUT needs longer than the `minwait_timer` to set `rem_rcvr_status = TRUE`.

Table 7 specifies the CTC_4.1.2 – Case 4 – Value of `minwait_timer` – `minwait_timer` between `SEND IDLE OR DATA` to `SEND IDLE` state (with MII access).

Table 7 — CTC_4.1.2 – Case 4 – Value of `minwait_timer – minwait_timer` between `SEND IDLE OR DATA` to `SEND IDLE` state (with MII access)

Item	Content
CTC # – Name	CTC_4.1.2 – Case 4 – Value of `minwait_timer` – `minwait_timer` between `SEND IDLE OR DATA` to `SEND IDLE` state (with MII access)
Purpose	This CTC verifies that the IUT implements the `minwait_timer` of 1,8 µs ± 0,18 µs while in the `SEND IDLE OR DATA`.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.4.7.2 timers; — Figure 96-18 PHY control state diagram; — Figure 96-19 link monitor state diagram.
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.

Table 7 *(continued)*

Item	Content
Step	1. The UT shall configure the IUT as MASTER or SLAVE. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall establish a valid link with the IUT. 4. The UT shall instruct the LT to transmit with `tx_mode = SEND_I` with `loc_rcvr_status = NOT_OK`. 5. As soon as the IUT begins transmitting with `tx_mode = SEND_I`, the LT shall be instructed to transmit with `loc_rcvr_status = OK`. 6. The LT shall be instructed to transmit with `loc_rcvr_status = NOT_OK` as soon as the IUT begins transmitting with `tx_mode = SEND_N`. 7. The UT shall observe how long the IUT transmits with `tx_mode = SEND_N`.
Iteration	a) REPEAT step 2 to step 7 with the IUT configured as MASTER, 10 times. b) REPEAT step 2 to step 7 with the IUT configured as SLAVE, 10 times.
Expected response	After step 7 iterations a): The IUT transmits with `tx_mode = SEND_N` for 1,8 µs ± 0,18 µs. After step 7 iterations b): The IUT transmits with `tx_mode = SEND_N` for 1,8 µs ± 0,18 µs.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested. It also cannot be performed, if the IUT needs longer than the `minwait_timer` to drop `rem_rcvr_status`. Ambiguity between `SEND_I` and `SEND_N` code-groups may cause an additional error in the observed timer value. This error can be reduced by repeating the impacted test part until observing fewer ambiguous `SEND_I` and `SEND_N` code groups.

8.1.4 CTC_4.1.3 – Value of `maxwait_timer` (with MII access)

Table 8 specifies the CTC_4.1.3 – Value of `maxwait_timer` (with MII access).

Table 8 — CTC_4.1.3 – Value of maxwait_timer (with MII access)

Item	Content
CTC # – Name	CTC_4.1.3 – Value of `maxwait_timer` (with MII access)
Purpose	This CTC verifies that the IUT implements the `maxwait_timer` of 200 ms ± 2 ms.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.4.7.2 timers; — Figure 96-18 PHY control state diagram; — Figure 96-19 link monitor state diagram.
Prerequisite	The UT shall have access to the `link_status`[a]. The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.

Table 8 *(continued)*

Item	Content
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall establish a link and ensure that `link_status = OK`. 3. The LT shall monitor the transmissions and `link_status` from the IUT. 4. The LT shall stop transmitting signalling to the IUT. 5. Determine when the IUT sets `tx_mode ≠ SEND_N` and mark this as `TIME A`. 6. Determine when the IUT sets `link_status = FAIL` and mark this as `TIME B`. 7. The UT shall measure `max_wait_timer` as the difference between `TIME A` and `TIME B`. 8. The UT shall configure the IUT as SLAVE. 9. The LT shall establish a link and ensure that `link_status = OK`. 10. The LT shall monitor the transmissions and `link_status` from the IUT. 11. The LT shall stop transmitting signalling to the IUT. 12. Determine when the IUT sets `tx_mode ≠ SEND_N` and mark this as `TIME A`. 13. Determine when the IUT sets `link_status = FAIL` and mark this as `TIME B`. 14. The UT shall measure `max_wait_timer` as the difference between `TIME A` and `TIME B`.
Iteration	Not applicable
Expected response	After step 7: The IUT implements a `max_wait_timer` of 200 ms ± 2 ms when configured as MASTER. After step 14: The IUT implements a `max_wait_timer` of 200 ms ± 2 ms when configured as SLAVE.
Remark	[a] The delay from the internal setting of `link_status` to the externally observable `link_status` signal shall be defined by the IUT supplier. This CTC cannot be completed if access to `link_status` is not available. Also, some devices cannot be configured as MASTER or SLAVE, in which case only the supported configuration is tested.

8.1.5 CTC_4.1.4 – Value of `stabilize_timer` (with MII access)

Table 9 specifies the CTC_4.1.4 – Value of `stabilize_timer` (with MII access).

Table 9 — CTC_4.1.4 – Value of `stabilize_timer` (with MII access)

Item	Content
CTC # – Name	CTC_4.1.4 – Value of `stabilize_timer` (with MII access)
Purpose	This CTC verifies that the IUT implements the `stabilize_timer` of 1,8 µs ± 0,18 µs.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.4.7.2 timers; — Figure 96-18 PHY control state diagram; — Figure 96-19 link monitor state diagram.
Prerequisite	The UT shall have access to the `link_status`[a]. The UT shall have the ability to configure the IUT as MASTER or SLAVE.

Table 9 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER or SLAVE. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall start transmitting a valid training signal from the transmit station as soon as the IUT restarts the training process. 4. After the IUT sets `loc_rcvr_status = OK`, continue to send the valid signal for 0,36 µs, then stop transmitting. 5. The UT shall check the value of `link_status`.
Iteration	a) REPEAT step 2 to step 5, 1 time, with the IUT configured as MASTER and the test system configured as SLAVE, increasing the duration that the test system sends a valid signal in step 4 by 0,36 µs until the IUT reports `link_status = OK`. This is the value for `stabilize_timer`. b) REPEAT step 2 to step 5, 1 time, with the IUT configured as SLAVE and the test system configured as MASTER.
Expected response	After step 5 iteration a): LT expects the value of `stabilize_timer` to be 1,8 µs ± 0,18 µs when configured as MASTER. After step 5 iteration b): LT expects the value of `stabilize_timer` to be 1,8 µs ± 0,18 µs when configured as SLAVE.
Remark	[a] The delay from the internal setting of `link_status` to the externally observable `link_status` signal shall be defined by the IUT supplier. This CTC cannot be performed if real-time access to `link_status` is not available. Also, some devices cannot be configured as MASTER or SLAVE, in which case only the supported configuration is tested.

8.2 PHY – Group 2: PHY control state diagram (with MII access)

8.2.1 Overview

The CTCs specified in 8.2 verify the PHY control state diagram defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in ISO/IEC/IEEE 8802-3:2021, 96.4.5. Refer to Annex A for additional low-level technical details about the PHY control test suite.

8.2.2 CTC_4.2.1 – PHY control state diagram - `DISABLE TRANSMITTER` state (with MII access)

Table 10 specifies the CTC_4.2.1 – PHY control state diagram - `DISABLE TRANSMITTER` state (with MII access).

Table 10 — CTC_4.2.1 – PHY control state diagram - `DISABLE TRANSMITTER` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.1 – PHY control state diagram - `DISABLE TRANSMITTER` state (with MII access)
Purpose	This CTC verifies that the IUT disables the transmitter while in the `DISABLE TRANSMITTER` state.

Table 10 *(continued)*

Item	Content
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have access to the PMA reset. The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and cause the management to request a PMA reset. 3. The UT shall observe if the IUT disables the transmitter upon entering the `DISABLE TRANSMITTER` state. 4. The UT shall configure the IUT as SLAVE. 5. The LT shall monitor the transmissions from the IUT and cause the management to request a PMA reset. 6. The UT shall observe if the IUT disables the transmitter upon entering the `DISABLE TRANSMITTER` state.
Iteration	Not applicable
Expected response	After step 3: The IUT disables the transmitter upon entering the `DISABLE TRANSMITTER` state when configured as MASTER. After step 6: The IUT disables the transmitter upon entering the `DISABLE TRANSMITTER` state when configured as SLAVE.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested. It also cannot be performed, if the control of the PMA reset request is not available.

8.2.3 CTC_4.2.2 – PHY control state diagram - SLAVE SILENT state (with MII access)

Table 11 specifies the CTC_4.2.2 – PHY control state diagram - `SLAVE SILENT` state (with MII access).

Table 11 — CTC_4.2.2 – PHY control state diagram - `SLAVE SILENT` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.2 – PHY control state diagram - `SLAVE SILENT` state (with MII access)
Purpose	This CTC verifies that the IUT does not transmit while in the `SLAVE SILENT` state and that the IUT transitions out of this state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.

Table 11 *(continued)*

Item	Content
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT by sending invalid ternary codes after the IUT has established a link. 3. The LT shall observe that the IUT immediately transitions out of the `SLAVE SILENT` state without waiting for `scr_status = OK`. 4. The LT shall not immediately send a valid idle training pattern. 5. The LT shall send a valid idle training pattern and observe that the IUT begins transmitting a valid idle training pattern. 6. The UT shall configure the IUT as SLAVE. 7. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT by sending invalid ternary codes after the IUT has established a link. 8. The LT shall observe that the IUT immediately transitions out of the `SLAVE SILENT` state without waiting for `scr_status = OK`. 9. The LT shall not immediately send a valid idle training pattern. 10. The LT shall send a valid idle training pattern and observe that the IUT begins transmitting a valid idle training pattern.
Iteration	Not applicable
Expected response	After step 5: The IUT transitions out of the `SLAVE SILENT` state without waiting for `loc_rcvr_status = OK`. After step 10: The IUT does not transition out of the `SLAVE SILENT` state until it receives a valid idle training pattern.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested.

8.2.4 CTC_4.2.3 – PHY control state diagram – TRAINING state (with MII access)

The ISO/IEC/IEEE 8802-3:2021, Figure 96-18 PHY control state diagram states that the device remains in the `TRAINING` state until it has `loc_rcvr_status = OK` and `minwait_timer` has finished. If the link partner does not have `loc_rcvr_status = OK` then the device transits to the `SEND IDLE` state. If the link partner does have `loc_rcvr_status = OK` then the device transits to the `SEND IDLE OR DATA` state. The link partner's value for `rem_rcvr_status` is determined based on the scrambler sequence transmitter by the link partner.

Table 12 specifies the CTC_4.2.3 – Case 1 –PHY control state diagram – IUT remains in the `TRAINING` state (with MII access).

Table 12 — CTC_4.2.3 – Case 1 –PHY control state diagram – IUT remains in the `TRAINING` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.3 – Case 1 –PHY control state diagram – IUT remains in the `TRAINING` state (with MII access)
Purpose	This CTC verifies that the IUT remains in the `TRAINING` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.

Table 12 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall transmit a valid idle training pattern to the IUT, then the LT shall observe that the IUT continues to transmit a valid idle pattern with `tx_mode = SEND_I` and the scrambler for `loc_rcvr_status = NOT_OK`. 4. The UT shall configure the IUT as SLAVE. 5. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 6. The LT shall transmit a valid idle training pattern to the IUT, then stop transmitting as soon as the IUT begins transmitting. 7. The LT shall observe that the IUT does not exit the training state and continues transmitting a valid idle pattern with `tx_mode = SEND_I` and the scrambler for `loc_rcvr_status = NOT_OK`.
Iteration	Not applicable
Expected response	After step 3: The IUT continues transmitting a valid idle training pattern with `tx_mode = SEND_I` and `loc_rcvr_status = NOT_OK` when configured as MASTER. After step 7: The IUT continues transmitting a valid idle training pattern with `tx_mode = SEND_I` and `loc_rcvr_status = NOT_OK` when configured as SLAVE.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested.

Table 13 specifies the CTC_4.2.3 – Case 2 – PHY control state diagram – IUT transitions to the `SEND IDLE` state (with MII access).

Table 13 — CTC_4.2.3 – Case 2 – PHY control state diagram – IUT transitions to the `SEND IDLE` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.3 – Case 2 – PHY control state diagram – IUT transitions to the `SEND IDLE` state (with MII access)
Purpose	This CTC verifies that the IUT exits from the `TRAINING` state and transitions to the `SEND IDLE` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.

Table 13 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall transmit a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 4. The LT shall observe that the IUT continues transmitting with `tx_mode = SEND_I`. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall transmit a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 8. The LT shall observe that the IUT continues transmitting with `tx_mode = SEND_I`.
Iteration	Not applicable
Expected response	After step 4: The IUT continues transmitting a valid idle training pattern with `tx_mode = SEND_I` and `loc_rcvr_status = OK`. After step 8: The IUT continues transmitting a valid idle training pattern with `tx_mode = SEND_I` and `loc_rcvr_status = OK`.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested.

Table 14 specifies the CTC_4.2.3 – Case 3 – PHY control state diagram – IUT transitions to the `SEND IDLE OR DATA` state (with MII access).

Table 14 — CTC_4.2.3 – Case 3 – PHY control state diagram – IUT transitions to the `SEND IDLE OR DATA` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.3 – Case 3 – PHY control state diagram – IUT transitions to the `SEND IDLE OR DATA` state (with MII access)
Purpose	This CTC verifies that the IUT exits from the `TRAINING` state and transitions to the `SEND IDLE OR DATA` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE. The IUT shall have the ability to send and receive PHY frames. This can be accomplished through a loopback, responding to ICMP requests, or by forwarding traffic through two ports.

Table 14 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and the UT shall restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT establishes a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = OK`. 4. The LT shall observe that the IUT begins transmitting with `tx_mode = SEND_N` and is capable of sending and receiving PHY frames. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 8. The LT shall begin transmitting a valid idle training pattern with the scrambler for `loc_rcvr_status = OK` as soon as the IUT sets `scr_status = OK`. 9. The LT shall observe that the IUT begins transmitting with `tx_mode = SEND_N` and is capable of sending receiving PHY frames.
Iteration	Not applicable
Expected response	After step 4: The IUT begins transmitting with `tx_mode = SEND_N` and is capable of transmitting and receiving PHY frames when configured as MASTER. After step 9: The IUT begins transmitting with `tx_mode = SEND_N` and is capable of transmitting and receiving PHY frames when configured as SLAVE.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested. In step 9, the implementation may not allow to set `scr_status = OK` without also setting `loc_rcvr_status = OK` at the same time. In this case, the IUT transitions to the `SEND IDLE` state and this CTC cannot be performed.

8.2.5 CTC_4.2.4 – PHY control state diagram – SEND IDLE state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-18 PHY control state diagram states that the device remains in the `SEND IDLE` state while it has `loc_rcvr_status = OK` and `rem_rcvr_status = NOT_OK`. The IUT transits to the `SEND IDLE OR DATA` state once `rem_rcvr_status = OK` or to the `SLAVE SILENT` state if `loc_rcvr_status = NOT_OK`. The link partner's value for `loc_rcvr_status` is determined based on the scrambler sequence transmitter by the link partner.

Table 15 specifies the CTC_4.2.4 – Case 1 – PHY control state diagram – IUT remains in the `SEND IDLE` state (with MII access).

Table 15 — CTC_4.2.4 – Case 1 – PHY control state diagram – IUT remains in the SEND IDLE state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.4 – Case 1 – PHY control state diagram – IUT remains in the SEND IDLE state (with MII access)
Purpose	This CTC verifies that the IUT exits from the SEND IDLE state when the IUT remains in the SEND IDLE state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = NOT_OK. 4. The LT shall observe that the IUT continues transmitting a valid idle training pattern. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = NOT_OK. 8. The LT shall observe that the IUT continues transmitting a valid idle training pattern.
Iteration	Not applicable
Expected response	After step 4: The IUT as MASTER continues transmitting a valid idle training pattern with loc_rcvr_status = OK. After step 8: The IUT as SLAVE continues transmitting a valid idle training pattern with loc_rcvr_status = OK.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration is tested.

Table 16 specifies the CTC_4.2.4 – Case 2 – PHY control state diagram – IUT transitions to the SLAVE SILENT state (with MII access).

Table 16 — CTC_4.2.4 – Case 2 – PHY control state diagram – IUT transitions to the SLAVE SILENT state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.4 – Case 2 – PHY control state diagram – IUT transitions to the SLAVE SILENT state (with MII access)
Purpose	This CTC verifies that the IUT exits from the SEND IDLE state when the IUT transitions to the SLAVE SILENT state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram

Table 16 *(continued)*

Item	Content
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK` for at least `minwait_timer`. 4. The LT shall stop transmitting to the IUT. 5. The LT shall observe that the IUT transitions to the `SLAVE SILENT` state. 6. The UT shall configure the IUT as SLAVE. 7. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 8. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK` for at least `minwait_timer`. 9. The LT shall stop transmitting to the IUT. 10. The LT shall observe that the IUT transitions to the `SLAVE SILENT` state.
Iteration	Not applicable
Expected response	After step 5: The IUT as MASTER transmits with `tx_mode = SEND_I` for at least 3,24 µs and no more than 1 ms before transmitting with `tx_mode = SEND_Z` indicating a transition to the `SLAVE SILENT` state. After step 10: The IUT as SLAVE transmits with tx_mode = SEND_I for at least 3,24 µs and no more than 1 ms before transmitting with `tx_mode = SEND_Z` indicating a transition to the `SLAVE SILENT` state.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration is tested.

Table 17 specifies the CTC_4.2.4 – Case 3 – PHY control state diagram – IUT transitions in the `SEND IDLE OR DATA` state (with MII access).

Table 17 — CTC_4.2.4 – Case 3 – PHY control state diagram – IUT transitions in the `SEND IDLE OR DATA` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.4 – Case 3 – PHY control state diagram – IUT transitions in the `SEND IDLE OR DATA` state (with MII access)
Purpose	This CTC verifies that the IUT exits from the `SEND IDLE` state when the IUT transitions in the `SEND IDLE OR DATA` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram

Table 17 *(continued)*

Item	Content
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE. The IUT shall have the ability to send and receive PHY frames. This can be accomplished through a loopback, responding to ICMP requests, or by forwarding traffic through two ports.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK` for at least `minwait_timer`, then transmit with `loc_rcvr_status = OK`. 4. The LT shall observe that the IUT begins transmitting with `tx_mode = SEND_N` and is capable of sending and receiving PHY frames. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK` for at least `minwait_timer`, then transmit with `loc_rcvr_status = OK`. 8. The LT shall observe that the IUT begins transmitting with `tx_mode = SEND_N` and is capable of sending and receiving PHY frames.
Iteration	Not applicable
Expected response	After step 4: The IUT as MASTER begins transmitting with `tx_mode = SEND_N` and is capable of transmitting and receiving PHY frames when configured as MASTER. After step 8: The IUT as SLAVE begins transmitting with `tx_mode = SEND_N` and is capable of transmitting and receiving PHY frames when configured as SLAVE.
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration will be tested.

8.2.6 CTC_4.2.5 – PHY control state diagram – `SEND IDLE OR DATA` state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-18 PHY control state diagram states that the device remains in the `SEND IDLE OR DATA` state until it has `loc_rcvr_status = NOT_OK` and `TX_EN = FALSE`. The IUT transits to the `SLAVE SILENT` state if `loc_rcvr_status = NOT_OK` while `TX_EN = FALSE`. The IUT transits to the `SEND IDLE` state if `rem_rcvr_status = NOT_OK`.

Table 18 specifies the CTC_4.2.5 – Case 1 – PHY control state diagram – IUT exits from the `SEND IDLE OR DATA` state (with MII access).

Table 18 — CTC_4.2.5 – Case 1 – PHY control state diagram – IUT exits from the SEND IDLE OR DATA state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.5 –Case 1 – PHY control state diagram – IUT exits from the SEND IDLE OR DATA state (with MII access)
Purpose	This CTC verifies that the IUT exits from the SEND IDLE OR DATA state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE. The IUT shall have the ability to send and receive PHY frames. This can be accomplished through a loopback, responding to ICMP requests, or by forwarding traffic through two ports. The UT shall have the ability to access the MII test system.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = OK for at least minwait_timer. 4. The LT shall observe that the IUT establishes a valid link and begins receiving and transmitting PHY frames in loopback mode. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = NOT_OK. 8. The LT shall begin transmitting a valid idle training pattern with the scrambler for loc_rcvr_status = OK for at least minwait_timer as soon as the IUT sets scr_status = OK. 9. The LT shall observe that the IUT begins transmitting with tx_mode = SEND_N and begins receiving and transmitting PHY frames in loopback mode.
Iteration	Not applicable
Expected response	After step 4: The IUT establishes a valid link and begins receiving and transmitting PHY frames. After step 9: The IUT establishes a valid link and begins receiving and transmitting PHY frames.
Remark	---

Table 19 specifies the CTC_4.2.5 – Case 2 – PHY control state diagram – IUT transitions to the SLAVE SILENT state (with MII access).

Table 19 — CTC_4.2.5 – Case 2 – PHY control state diagram – IUT transitions to the SLAVE SILENT state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.5 – Case 2 – PHY control state diagram – IUT transitions to the SLAVE SILENT state (with MII access)
Purpose	This CTC verifies that the IUT exits from the SEND IDLE OR DATA state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = OK until the IUT sets tx_mode = SEND_N. 4. The LT shall stop transmitting to the IUT. 5. The LT shall observe that the IUT transitions to the SLAVE SILENT state. 6. The UT shall configure the IUT as SLAVE. 7. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 8. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = NOT_OK. 9. The LT shall begin transmitting a valid idle training pattern with the scrambler for loc_rcvr_status = OK until the IUT transitions from tx_mode = SEND_Z to tx_mode = SEND_I. 10. The LT shall stop transmitting to the IUT. 11. The LT shall observe that the IUT transitions to the SLAVE SILENT state.
Iteration	Not applicable
Expected response	After step 5: The IUT transitions to the SLAVE SILENT state within 1 ms. After step 11: The IUT transitions to the SLAVE SILENT state within 1 ms.
Remark	---

Table 20 specifies the CTC_4.2.5 – Case 3 – PHY control state diagram – IUT remains in the SEND IDLE OR DATA state while tx_enable = TRUE (with MII access).

Table 20 — CTC_4.2.5 – Case 3 – PHY control state diagram – IUT remains in the SEND IDLE OR DATA state while tx_enable = TRUE (with MII access)

Item	Content
CTC # – Name	CTC_4.2.5 – Case 3 – PHY control state diagram – IUT remains in the SEND IDLE OR DATA state while tx_enable = TRUE (with MII access)

Table 20 *(continued)*

Item	Content
Purpose	This CTC verifies that the IUT remains in the SEND IDLE OR DATA state while tx_enable = TRUE.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE. The UT shall have the ability to access the MII test system. This CTC shall be performed when the IUT transitions directly to SLAVE SILENT state as specified in CTC_4.2.5 – Case 2.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = OK for at least minwait_timer. 4. The LT shall force the IUT to set TX_EN = TRUE. 5. The LT shall stop transmitting to the IUT. 6. The LT shall observe that the IUT remains in the SEND IDLE OR DATA state. 7. The UT shall configure the IUT as SLAVE. 8. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 9. The LT shall send a valid idle training pattern to the IUT with the scrambler for loc_rcvr_status = NOT_OK. 10. The LT shall begin transmitting a valid idle training pattern with the scrambler for loc_rcvr_status = OK for at least minwait_timer as soon as the IUT sets scr_status = OK. 11. The LT shall force the IUT to set TX_EN = TRUE. 12. The LT shall stop transmitting to the IUT. 13. The LT shall observe that the IUT remains in the SEND IDLE OR DATA state.
Iteration	Not applicable
Expected response	After step 6: The IUT remains in the SEND IDLE OR DATA state. After step 13: The IUT remains in the SEND IDLE OR DATA state.
Remark	This CTC cannot be completed if access to the MII signals is not available. This CTC can also not be completed in the case where the IUT transitions to the SEND IDLE state and then to the SLAVE SILENT state. This is because loc_rcvr_status can take longer than minwait_timer to fall after transmissions to the IUT have ceased, and the transition tested in this CTC never occurs. Also, some devices cannot be configured as MASTER or SLAVE, in which case only the supported configuration is tested.

Table 21 specifies the CTC_4.2.5 – Case 4 – PHY control state diagram – IUT transitions to the SEND IDLE state (with MII access).

Table 21 — CTC_4.2.5 – Case 4 – PHY control state diagram – IUT transitions to the `SEND IDLE` state (with MII access)

Item	Content
CTC # – Name	CTC_4.2.5 – Case 4 – PHY control state diagram – IUT transitions to the `SEND IDLE` state (with MII access)
Purpose	This CTC verifies that the IUT transitions to the `SEND IDLE` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-18 – PHY control state diagram
Prerequisite	The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The IUT shall be configured as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = OK` until the IUT enters the `SEND IDLE` OR `DATA` state. 4. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 5. The LT shall observe that the IUT transitions to the `SEND IDLE` state. 6. The UT shall configure the IUT as SLAVE. 7. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 8. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 9. The LT shall begin transmitting a valid idle training pattern with the scrambler for `loc_rcvr_status = OK` for at least `minwait_timer` as soon as the IUT sets `scr_status = OK`. 10. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 11. The LT shall observe that the IUT transitions to the `SEND IDLE` state.
Iteration	Not applicable
Expected response	After step 5: The IUT transitions to the `SEND IDLE` state. After step 11: The IUT transitions to the `SEND IDLE` state.
Remark	---

8.3 PHY – Group 3: PHY link monitor state diagram (with MII access)

8.3.1 Overview

The CTCs specified in 8.3 verify the link monitor state diagram defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in ISO/IEC/IEEE 8802-3:2021, 96.4.5. Refer to Annex A for additional low-level technical details about the PHY control test suite.

8.3.2 CTC_4.3.1 – Link monitor state diagram – IUT does not enter the LINK OK state (with MII access)

Table 22 specifies the CTC_4.3.1 – Case 1 – Link monitor state diagram – IUT does not enter the `LINK OK` state (with MII access).

Table 22 — CTC_4.3.1 – Case 1 – Link monitor state diagram – IUT does not enter the LINK OK state (with MII access)

Item	Content
CTC # – Name	CTC_4.3.1 – Case 1 – Link monitor state diagram – IUT does not enter the `LINK OK` state (with MII access)
Purpose	This CTC verifies that the IUT implements the logic of the link monitor state diagram and does not enter the `LINK OK` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-19 link monitor state diagram
Prerequisite	The UT shall have the ability to access to the `link_status` signal. The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = OK`. The LT shall continue transmitting the valid idle training pattern until the IUT sets its `loc_rcvr_status = OK`, then the LT shall stop transmitting before `stabilize_timer` expires. 4. The LT shall observe that the IUT does not set `link_status = OK`. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 8. The LT shall begin transmitting a valid idle training pattern with the scrambler for `loc_rcvr_status = OK` as soon as the IUT sets `scr_status = OK`. The LT shall continue transmitting the valid idle training pattern until the IUT sets its `loc_rcvr_status = OK`, then the LT shall stop transmitting before `stabilize_timer` expires. 9. The LT shall observe that the IUT does not set `link_status = OK`.
Iteration	Not applicable
Expected response	After step 4: The IUT does not set `link_status = OK`. After step 9: The IUT does not set `link_status = OK`.
Remark	`stabilize_timer` cannot be verified if the IUT reaction time for the `loc_rcv_status` is longer than the `stabilize_timer`.

The ISO/IEC/IEEE 8802-3:2021 specification provides the link monitor state diagram. Devices shall not set `link_status = OK` until the `LINK UP` state.

Table 23 specifies the CTC_4.3.2 – Case 2 – Link monitor state diagram – IUT enters the `LINK OK` state (with MII access).

Table 23 — CTC_4.3.2 – Case 2 – Link monitor state diagram – IUT enters the LINK OK state (with MII access)

Item	Content
CTC # – Name	CTC_4.3.2 – Case 2 – Link monitor state diagram – IUT enters the `LINK OK` state (with MII access)
Purpose	This CTC verifies that the IUT implements the logic of the link monitor state diagram and enters the `LINK OK` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-19 link monitor state diagram
Prerequisite	The UT shall have the ability to access to the `link_status` signal. The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT by sending invalid ternary codes after the IUT has established a link. 3. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = OK` for at least `stabilize_timer`. 4. The LT shall observe that the IUT sets `link_status = OK`. 5. The UT shall configure the IUT as SLAVE. 6. The LT shall monitor the transmissions from the IUT and restart the training process on the IUT, either through management or by sending invalid ternary codes after the IUT has established a link. 7. The LT shall send a valid idle training pattern to the IUT with the scrambler for `loc_rcvr_status = NOT_OK`. 8. The LT shall begin transmitting a valid idle training pattern with the scrambler for `loc_rcvr_status = OK` as soon as the IUT sets `scr_status = OK`. The LT shall continue transmitting the valid idle training pattern until the IUT sets its `loc_rcvr_status = OK`, then the LT shall continue transmitting for at least `stabilize_timer`. 9. The LT shall observe that the IUT sets `link_status = OK`.
Iteration	Not applicable
Expected response	After step 4: The IUT sets `link_status = OK`. After step 9: The IUT sets `link_status = OK`.
Remark	`stabilize_timer` cannot be verified if the IUT reaction time for the `loc_rcv_status` is longer than the `stabilize_timer`.

Table 24 specifies the CTC_4.3.3 – Case 3 – Link monitor state diagram – IUT exits the `LINK OK` state (with MII access).

Table 24 — CTC_4.3.3 – Case 3 – Link monitor state diagram – IUT exits the LINK OK state (with MII access)

Item	Content
CTC # – Name	CTC_4.3.3 – Case 3 – Link monitor state diagram – IUT exits the `LINK OK` state (with MII access)
Purpose	This CTC verifies that the IUT implements the logic of the link monitor state diagram and exits the `LINK OK` state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-19 link monitor state diagram
Prerequisite	The UT shall have the ability to access to the `link_status` signal. The UT shall have the ability to configure the IUT as MASTER or SLAVE.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the ISO/IEC/IEEE 8802-3:2021 transmit test system and the ISO/IEC/IEEE 8802-3:2021 monitor test system. The IUT shall be powered on and shall be linked-up with the test system.
Step	1. The UT shall have the ability to configure the IUT as MASTER. 2. The LT shall monitor the transmissions from the IUT and `link_status`. 3. The LT shall establish a valid link with the IUT and The LT shall observe that the IUT sets `link_status = OK`. 4. The LT shall stop transmitting to the IUT. 5. The LT shall observe that the IUT sets `link_status = FAIL` after `maxwait_timer` expires. 6. The UT shall have the ability to configure the IUT as SLAVE. 7. The LT shall monitor the transmissions from the IUT and `link_status`. 8. The LT shall establish a valid link with the IUT and the LT shall observe that the IUT sets `link_status = OK`. 9. The LT shall stop transmitting to the IUT. 10. The LT shall observe that the IUT sets `link_status = FAIL` after `maxwait_timer` expires.
Iteration	Not applicable
Expected response	After step 5: The IUT sets `link_status = OK` then `link_status = FAIL`. After step 10: The IUT sets `link_status = OK` then `link_status = FAIL`.
Remark	`stabilize_timer` cannot be verified if the IUT reaction time for the `loc_rcv_status` is longer than the `stabilize_timer`.

9 PCS – IUT conformance test plan (with MII access)

9.1 PCS – Group 1: PCS transmit (with MII access)

9.1.1 Overview

The CTCs specified in 9.1 verify the PCS transmit defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in ISO/IEC/IEEE 8802-3:2021, 96.3.1 and 96.3.3.

9.1.2 CTC_3.1.1 – PCS signalling (with MII access)

The ISO/IEC/IEEE 8802-3:2021 PCS uses a combination of a 4B/3B conversion for MII data, side-stream scrambling and ternary symbols to encode the data for transmission on the line. In addition to the scrambler, there are additional functions performed on the data and idle streams to eliminate the correlation transmit data and to balance the power density.

Table 25 specifies the CTC_3.1.1 – PCS signalling (with MII access).

Table 25 — CTC_3.1.1 – PCS signalling (with MII access)

Item	Content
CTC # – Name	CTC_3.1.1 – PCS signalling (with MII access)
Purpose	This CTC verifies that the PCS performs the 4B/3B conversion, side-stream scrambling, and ternary symbol generation.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.3.3.1 4B/3B conversion; — 96.3.3.3.1 Side-stream scrambler polynomial; — 96.3.3.3.2 Generation of `Syn[2:0]`; — 96.3.3.3.3 Generation of `Scn[2:0]`; — 96.3.3.3.4 Generation of scrambled bits `Scn[2:0]`; — 96.3.3.3.5 Generation of ternary pair (TA_n, TB_n); — Table 96-1 Idle symbol mapping in training; — Table 96-2 Data symbols when `tx_mode = SEND_N`; — Table 96-3 Idle symbols when `tx_mode = SEND_N`.
Prerequisite	The UT shall be capable of capturing and decoding ternary symbols. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap. The IUT shall be powered on and shall be linked-up with the test system.

Table 25 *(continued)*

Item	Content
Step	1. The UT shall configure the IUT as MASTER and the link partner as SLAVE. 2. The LT shall monitor and decode the transmissions from the IUT while the IUT is in `tx_mode = SEND_I`. 3. The LT shall monitor and decode the transmissions from the IUT while the IUT is in `tx_mode = SEND_N` and `tx_enable = 1`. 4. The LT shall monitor and decode the transmissions from the IUT while the IUT is in `tx_mode = SEND_N` and `tx_enable = 0`. 5. The UT shall configure the IUT as SLAVE and the link partner as MASTER. 6. The LT shall monitor and decode the transmissions from the IUT while the IUT is in `tx_mode = SEND_I`. 7. The LT shall monitor and decode the transmissions from the IUT while the IUT is in `tx_mode = SEND_N` and `tx_enable = 1`. 8. The LT shall monitor and decode the transmissions from the IUT while the IUT is in `tx_mode = SEND_N` and `tx_enable = 0`.
Iteration	Not applicable
Expected response	After step 2: The transmissions follow the 4B/3B conversion specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.1 – 4B/3B conversion, the side-stream scrambler polynomial specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.1 – Side-stream scrambler polynomial for MASTER, the generation of `Sdn[2:0]` specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.4 – Generation of scrambled bits `Sdn[2:0]`, and the ternary symbol mapping defined in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.5 – Generation of ternary pair (TA_n, TB_n). After step 3: The transmissions follow the 4B/3B conversion specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.1 – 4B/3B conversion, the side-stream scrambler polynomial specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.1 – Side-stream scrambler polynomial for MASTER, the generation of `Sdn[2:0]` specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.4 – Generation of scrambled bits `Sdn[2:0]`, and the ternary symbol mapping defined in ISO/IEC/IEEE 8802-3:2021, Table 96-3 – Idle symbols when `tx_mode = SEND_N`. After step 4: The transmissions follow the 4B/3B conversion specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.1 – 4B/3B conversion, the side-stream scrambler polynomial specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.1 – Side-stream scrambler polynomial for MASTER, the generation of `Sdn[2:0]` specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.4 – Generation of scrambled bits `Sdn[2:0]`, and the ternary symbol mapping defined in ISO/IEC/IEEE 8802-3:2021, Table 96-3 – Idle symbols when `tx_mode = SEND_N`. After step 6: The transmissions follow the 4B/3B conversion specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.1 – 4B/3B conversion the side-stream scrambler polynomial specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.1 – Side-stream scrambler polynomial for SLAVE, the generation of `Sdn[2:0]` specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.4 – Generation of scrambled bits `Sdn[2:0]`, and the ternary symbol mapping defined in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.5 – Generation of ternary pair (TA_n, TB_n). After step 7: The transmissions follow the 4B/3B conversion specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.1 – 4B/3B conversion, the side-stream scrambler polynomial specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.1 – Side-stream scrambler polynomial for SLAVE, the generation of `Sdn[2:0]` specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.4 – Generation of scrambled bits `Sdn[2:0]`, and the ternary symbol mapping defined in ISO/IEC/IEEE 8802-3:2021, Table 96-2 – Data symbols when `tx_mode = SEND_N` and `tx_enable = 1`. After step 8: The transmissions follow the 4B/3B conversion specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.1 – 4B/3B conversion, the side-stream scrambler polynomial specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.1 – Side-stream scrambler polynomial for SLAVE, the generation of `Sdn[2:0]` specified in ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.3 – Generation of `Scn[2:0]`, and the ternary symbol mapping defined in ISO/IEC/IEEE 8802-3:2021, Table 96-3 – Idle symbols when `tx_mode = SEND_N`.

Table 25 *(continued)*

Item	Content
Remark	If the IUT is not configurable as MASTER or as SLAVE, then only the supported configuration is tested.

9.1.3 CTC_3.1.2 – PCS reset (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.1 – PCS reset function states that the PCS is reset upon power on or the receipt of a reset request from management entity. The PCS reset function causes the PCS transmit state diagram to transition to the `SEND IDLE` state and the side-stream scrambler to be reset.

Table 26 specifies the CTC_3.1.2 – PCS reset (with MII access).

Table 26 — CTC_3.1.2 – PCS reset (with MII access)

Item	Content
CTC # – Name	CTC_3.1.2 – PCS reset (with MII access)
Purpose	This CTC verifies that the PCS initialises upon receipt of a reset request from the management entity.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.1 PCS reset function
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames. The IUT shall provide access to the PCS reset.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The UT shall configure the IUT as MASTER. 2. The LT shall monitor and decode the transmissions from the IUT and cause the management to request a PCS reset. 3. The UT shall configure the IUT as SLAVE. 4. The LT shall monitor and decode the transmissions from the IUT and cause the management to request a PCS reset.
Iteration	Not applicable
Expected response	After step 2: The IUT transitions to the `SEND IDLE` state upon reception of a PCS reset request when configured as MASTER. The IUT resets the scrambler to a non-zero value upon reception of a PCS reset request when configured as MASTER. After step 4: The IUT transitions to the `SEND IDLE` state upon reception of a PCS reset request when configured as SLAVE. The IUT resets the scrambler to a non-zero value upon reception of a PCS reset request when configured as SLAVE.
Remark	If the ability to control the PCS reset request is not available, this CTC cannot be performed. Also, some devices cannot be configured as MASTER or SLAVE, in which case only the supported configuration is tested.

9.1.4 CTC_3.1.3 – PCS transmit proper SSD (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.3 – PCS transmit states that the PCS transmits 6 consecutive systems of `SSD` to the PMA upon assertion of `tx_enable`.

ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.5 – Generation of ternary symbol (TA_n, TB_n) states that this translates to ternary symbols of (0,0), (0,0), (0,0).

Table 27 specifies CTC_3.1.3 – PCS transmit proper SSD (with MII access).

Table 27 — CTC_3.1.3 – PCS transmit proper SSD (with MII access)

Item	Content
CTC # – Name	CTC_3.1.3 – PCS transmit proper SSD (with MII access)
Purpose	This CTC verifies that the PCS transmits the SSD upon assertion of tx_enable.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.3.3 PCS transmit; — 96.3.3.3.5 Generation of ternary pair (TA_n, TB_n).
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT shall monitor and decode the transmissions from the IUT as the IUT is sending PHY frames.
Iteration	Not applicable
Expected response	After step 1: The IUT transmits (0,0), (0,0), (0,0) at the beginning of every frame.
Remark	None

9.1.5 CTC_3.1.4 – PCS transmit proper ESD (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.3 – PCS transmit states that the PCS transmits 6 consecutive systems of ESD to the PMA upon de-assertion of tx_enable in the absence of transmit errors.

ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.5 – Generation of ternary symbol (TA_n, TB_n) states that this translates to ternary symbols of (0,0), (0,0), (1,1).

Table 28 specifies the CTC_3.1.4 – PCS transmit proper ESD (with MII access).

Table 28 — CTC_3.1.4 – PCS transmit proper ESD (with MII access)

Item	Content
CTC # – Name	CTC_3.1.4 – PCS transmit proper ESD (with MII access)
Purpose	This CTC verifies that the PCS transmits the ESD upon de-assertion of tx_enable in the absence of a transmit error.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.3.3 PCS transmit; — 96.3.3.3.5 Generation of ternary pair (TA_n, TB_n).

Table 28 *(continued)*

Item	Content
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT shall monitor and decode the transmissions from the IUT as the IUT is sending PHY frames.
Iteration	Not applicable
Expected response	After step 1: The IUT transmits (0,0), (0,0), (1,1) at the end of every frame that does not have transmit errors.
Remark	None

9.1.6 CTC_3.1.5 – PCS transmit ESD with tx_error (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.3 – PCS transmit states that the PCS transmits 6 consecutive systems of ESD_err to the PMA upon de-assertion of tx_enable in the presence of transmit errors.

ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.5 – Generation of ternary symbol (TA_n, TB_n) states that this translates to ternary symbols of (0,0), (0,0), (-1,-1).

Table 29 specifies the CTC_3.1.5 – PCS transmit ESD with tx_error (with MII access).

Table 29 — CTC_3.1.5 – PCS transmit ESD with tx_error (with MII access)

Item	Content
CTC # – Name	CTC_3.1.5 – PCS transmit ESD with tx_error (with MII access)
Purpose	This CTC verifies that the PCS transmits the ESD_err upon de-assertion of tx_enable in the presence of a transmit error.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.3.3 PCS transmit; — 96.3.3.3.5 Generation of ternary pair (TA_n, TB_n).
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames. The UT shall be capable of controlling the MII signals.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT shall monitor and decode the transmissions from the IUT as the IUT is sending PHY frames while causing the IUT to send transmit errors.
Iteration	Not applicable

Table 29 *(continued)*

Item	Content
Expected response	After step 1: The IUT transmits (0,0), (0,0), (-1,-1) at the end of every frame that has a transmit error.
Remark	It is not possible to perform this CTC if there is no method to force the IUT to transmit a frame with a transmit error. This can be accomplished through an MII test system if there is direct access to the MII.

9.1.7 CTC_3.1.6 – PCS transmission of stuff bits (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.3.1.2 – 4B/3B conversion for MII data states that the IUT shall append stuff bits at the end of every packet that is not a multiple of 3-bit in length.

Table 30 specifies the CTC_3.1.6 – PCS transmission of stuff bits (with MII access).

Table 30 — CTC_3.1.6 – PCS transmission of stuff bits (with MII access)

Item	Content
CTC # – Name	**CTC_3.1.6 – PCS transmission of stuff bits** (with MII access)
Purpose	This CTC verifies that the PCS inserts stuff bits during the 4B/3B conversion for MII data.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.1.2 4B/3B conversion for MII data
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. Monitor and decode the transmissions from the IUT as the IUT is sending PHY frames of several lengths that are a multiple of 3 (when including 8 bytes for preamble), including but not limited to 64 bytes and 67 bytes. 2. Monitor and decode the transmissions from the IUT as the IUT is sending PHY frames of several lengths that are 1 more than a multiple of 3 (when including 8 bytes for preamble), including but not limited to 66 bytes and 69 bytes. 3. Monitor and decode the transmissions from the IUT as the IUT is sending PHY frames of several lengths that are 2 more than a multiple of 3 (when including 8 bytes for preamble), including but not limited to 65 bytes and 68 bytes.
Iteration	Not applicable
Expected response	After step 1: The IUT does not transmit stuff bits. After step 2: The IUT transmits two stuff bits. After step 3: The IUT transmits one stuff bit.
Remark	None

9.1.8 CTC_3.1.7 – PCS `tx_error` (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.3 – PCS transmit states that the IUT shall set `tx_error = TRUE` if `tx_error_mii` is asserted during the packet period.

ISO/IEC/IEEE 8802-3:2021, 96.3.3 – PCS transmit and ISO/IEC/IEEE 8802-3:2021, Figure 96-6: 4B/3B MII signal conversion indicate that `tx_error = TRUE` is held until the IUT enters the `ERR ESD1 VECTOR` state.

Table 31 specifies the CTC_3.1.7 – PCS `tx_error` (with MII access).

Table 31 — CTC_3.1.7 – PCS `tx_error` (with MII access)

Item	Content
CTC # – Name	CTC_3.1.7 – PCS `tx_error` (with MII access)
Purpose	This CTC verifies that the PCS sets `tx_error` based on the value of `tx_error_mii` and `tx_enable_mii`.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.3.3 PCS transmit; — 96.3.3 Figure 96-6: 4B/3B MII signal conversion.
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames. The UT shall be capable of controlling the MII signals.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT and link partner shall be configured such that the IUT establishes a valid link while the MII test system is sending `TXD` = 0000_2, `TX_EN = FALSE`, and `TX_ER = FALSE`. 2. The LT shall instruct the MII test system to set `TXD` = 0101_2, `TX_EN = TRUE`, and `TX_ER = TRUE` for 1 clock cycle, then set `TXD` = 0101_2, `TX_EN = TRUE`, and `TX_ER = FALSE` for 5 clock cycles, and then set `TXD` = 0000_2, `TX_EN = FALSE`, and `TX_ER = FALSE` for at least 2 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set `TXD` = 0101_2, `TX_EN = TRUE`, and `TX_ER = FALSE` for 7 clock cycles, then set `TXD` = 0000_2, `TX_EN = TRUE`, and `TX_ER = TRUE` for 1 clock cycle, and then set `TXD` = 0000_2, `TX_EN = FALSE`, and `TX_ER = FALSE` for at least 3 clock cycles in step 2. b) REPEAT step 1 to step 3, except instruct the MII test system to set `TXD` = 0101_2, `TX_EN = TRUE`, and `TX_ER = FALSE` for 6 clock cycles, then set `TXD` = 0000_2, `TX_EN = FALSE`, and `TX_ER = TRUE` for at least 2 clock cycles in step 2. c) REPEAT step 1 to step 3, except instruct the MII test system to set `TXD` = 0000_2, `TX_EN = FALSE`, and `TX_ER = TRUE` for 1 clock cycle, then set `TXD` = 0101_2, `TX_EN = TRUE`, and `TX_ER = FALSE` for 6 clock cycles, and then set `TXD` = 0000_2, `TX_EN = FALSE`, and `TX_ER = FALSE` for at least 2 clock cycles in step 2.
Expected response	After step 3: After exiting the `TRANSMIT DATA` state, the IUT transmits `ERR ESD1, ESD2,` and `ERR ESD3`. After step 3 iteration a): After exiting the `TRANSMIT DATA` state, the IUT transmits `ESD1, ESD2,` and `ERR ESD3`. After step 3 iteration b): After exiting the `TRANSMIT DATA` state, the IUT transmits `ESD1, ESD2,` and `ESD3`. After step 3 iteration c): After exiting the `TRANSMIT DATA` state, the IUT transmits `ESD1, ESD2,` and `ESD3`.
Remark	None

9.2 PCS – Group 2: PCS transmit state diagram (with MII access)

9.2.1 Overview

The CTCs specified in 9.2 verify the PCS transmit state diagram defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in the ISO/IEC/IEEE 8802-3:2021, 96.3.3.2 specification.

9.2.2 CTC_3.2.1 – PCS transmit state diagram - SEND IDLE state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. The IUT should remain in the SEND IDLE state until tx_enable = TRUE.

Table 32 specifies the CTC_3.2.1 – PCS transmit state diagram - SEND IDLE state (with MII access).

Table 32 — CTC_3.2.1 – PCS transmit state diagram - SEND IDLE state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.1 – PCS transmit state diagram - SEND IDLE state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the SEND IDLE state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The LT shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The MII of the IUT shall be connected to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT shall be connected to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to send frame data on TXD while keeping TX_EN = FALSE. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TX_ER = TRUE in step 2. b) REPEAT step 1 to step 3, except instruct the MII test system to set TX_ER = FALSE and TX_EN = TRUE in step 2. c) REPEAT step 1 to step 3, except instruct the MII test system to set TX_ER = TRUE and TX_EN = TRUE in step 2.
Expected response	After step 2: The IUT remains in the SEND IDLE state. After step 3 iteration a): The IUT remains in the SEND IDLE state. After step 3 iteration b): The IUT transitions to the SSD1 VECTOR state and transmits SSD1. After step 3 iteration c): The IUT transitions to the SSD1 VECTOR state and transmits SSD1.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.3 CTC_3.2.2 – PCS transmit state diagram - SSD1 VECTOR and SSD2 VECTOR states (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram.

Table 33 specifies the CTC_3.2.2 – PCS transmit state diagram - SSD1 VECTOR and SSD2 VECTOR states (with MII access).

Table 33 — CTC_3.2.2 – PCS transmit state diagram - SSD1 VECTOR and SSD2 VECTOR states (with MII access)

Item	Content
CTC # – Name	CTC_3.2.2 – PCS transmit state diagram - SSD1 VECTOR and SSD2 VECTOR states (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the SSD1 VECTOR and SSD2 VECTOR states.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TX_EN = TRUE and TX_ER = FALSE for at least 3 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TX_EN = TRUE and TX_ER = TRUE for at least 3 clock cycles in step 2. b) REPEAT step 1 to step 3, except instruct the MII test system to set TX_EN = TRUE and TX_ER = FALSE for 1 clock cycle, and then set TX_EN = TRUE and TX_ER = TRUE for at least 2 clock cycles in step 2. c) REPEAT step 1 to step 3, except instruct the MII test system to set TX_EN = TRUE and TX_ER = FALSE for 1 clock cycle, then set TX_EN = FALSE and TX_ER = FALSE in step 2. d) REPEAT step 1 to step 3, instruct the MII test system to set TX_EN = TRUE and TX_ER = FALSE for 1 clock cycle, then set TX_EN = FALSE and TX_ER = TRUE in step 2.
Expected response	After step 2: The IUT transmits SSD1, SSD2, and SSD3. After step 3 iteration a): The IUT transmits SSD1, SSD2, and SSD3. After step 3 iteration b): The IUT transmits SSD1, SSD2, and SSD3. After step 3 iteration c): The IUT transmits SSD1, SSD2, and SSD3. After step 3 iteration d): The IUT transmits SSD1, SSD2, and SSD3.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.4 CTC_3.2.3 – PCS transmit state diagram - SSD3 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Once the IUT

enters the SSD3 VECTOR state, the IUT should transmit SSD3 and then transition to TRANSMIT_DATA, ERR ESD1 VECTOR, or ESD1 VECTOR.

Table 34 specifies the CTC_3.2.3 – PCS transmit state diagram - SSD3 VECTOR state (with MII access).

Table 34 — CTC_3.2.3 – PCS transmit state diagram - SSD3 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.3 – PCS transmit state diagram - SSD3 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the SSD3 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for at least 3 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0000_2, TX_EN = TRUE and TX_ER = FALSE for at least 3 clock cycles in step 2. b) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 2 clock cycles, and then set TX_EN = TRUE and TX_ER = TRUE for at least 1 clock cycle in step 2. c) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 2 clock cycles, then set TX_EN = FALSE and TX_ER = FALSE for at least 4 clock cycles in step 2. d) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 2 clock cycles, then set TX_EN = FALSE and TX_ER = FALSE for at least 4 clock cycles in step 2.
Expected response	After step 2: The IUT transmits SSD1 and SSD2, enters the SSD3 VECTOR state and transmit SSD3, and then enters the TRANSMIT DATA state and transmits the scrambled version of 010_2. After step 3 iteration a): The IUT transmits SSD1 and SSD2, enters the SSD3 VECTOR state and transmits SSD3, and then enters the TRANSMIT DATA state and transmits the scrambled version of 000_2. After step 3 iteration b): The IUT transmits SSD1 and SSD2, enters the SSD3 VECTOR state and transmits SSD3, and then enters the TRANSMIT DATA state and transmits the scrambled version of 010_2. After step 3 iteration c): The IUT transmits SSD1 and SSD2, enters the SSD3 VECTOR state and transmits SSD3, enters the ESD1 VECTOR state and transmits ESD1, and then transmits ESD2 and ESD3. After step 3 iteration d): The IUT transmits SSD1 and SSD2, enters the SSD3 VECTOR state and transmits SSD3, enters the ERR ESD1 VECTOR state and transmits ESD1, and then transmits ESD2 and ERR ESD3.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.5 CTC_3.2.4 – PCS transmit state diagram - TRANSMIT DATA state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Once the IUT enters the TRANSMIT DATA state, it should remain in this state and encode tx_data until TX_EN = FALSE.

Table 35 specifies the CTC_3.2.4 – PCS transmit state diagram - TRANSMIT DATA state (with MII access).

Table 35 — CTC_3.2.4 – PCS transmit state diagram - TRANSMIT DATA state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.4 – PCS transmit state diagram - TRANSMIT DATA state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the TRANSMIT DATA state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for at least 4 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0000_2, TX_EN = TRUE and TX_ER = FALSE for at least 4 clock cycles in step 2. b) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for at least 4 clock cycles in step 2. c) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 4 clock cycles, then set TX_EN = FALSE and TX_ER = FALSE for at least 3 clock cycles in step 2. d) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 4 clock cycles, then set TX_EN = FALSE and TX_ER = FALSE for at least 3 clock cycles in step 2.
Expected response	After step 3: The IUT transmits SSD1, SSD2, and SSD3, then enters the TRANSMIT DATA state and transmits the scrambled version of 010_2 and 101_2. After step 3 iteration a): The IUT transmits SSD1, SSD2, and SSD3, then enters the TRANSMIT DATA state and transmits the scrambled version of 000_2 and 000_2. After step 3 iteration b): The IUT transmits SSD1, SSD2, and SSD3, then enters the TRANSMIT DATA state and transmits the scrambled version of 010_2 and 101_2. After step 3 iteration c): The IUT transmits SSD1, SSD2, and SSD3, then enters the TRANSMIT DATA state and transmits the scrambled version of 010_2, 101_2, $0XX_2$, and then transmits ESD1, ESD2, and ESD3. The transmission of "$0XX_2$" represents a data bit of 0_2 and two stuff bits. After step 3 iteration d): The IUT transmits SSD1, SSD2, and SSD3, then enters the TRANSMIT DATA state and transmits the scrambled version of 010_2, 101_2, $0XX_2$, and then transmits ESD1, ESD2, and ERR ESD3. The transmission of $0XX_2$ represents a data bit of 0_2 and two stuff bits.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.6 CTC_3.2.5 – PCS transmit state diagram - ESD1 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Regardless of the transmissions on the MII, once the IUT enters the ESD1 VECTOR state the IUT should transmit ESD1, immediately transition to the ESD2 VECTOR state, and transmit ESD2.

Table 36 specifies the CTC_3.2.5 – PCS transmit state diagram - ESD1 VECTOR state (with MII access).

Table 36 — CTC_3.2.5 – PCS transmit state diagram - ESD1 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.5 – PCS transmit state diagram - ESD1 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the ESD1 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 6 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for at least 2 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 5 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for 1 clock cycle, and then set TX_EN = TRUE in step 2.
Expected response	After step 2: After exiting the TRANSMIT DATA state, the IUT transmits ESD1 followed by ESD2. After step 3 iteration a): After exiting the TRANSMIT DATA state, the IUT transmits ESD1 followed by ESD2.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.7 CTC_3.2.6 – PCS transmit state diagram - ESD2 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Regardless of the transmissions on the MII, once the IUT enters the ESD2 VECTOR state the IUT should transmit ESD2, immediately transition to the ESD3 VECTOR state, and transmit ESD3.

Table 37 specifies the CTC_3.2.6 – PCS transmit state diagram - ESD2 VECTOR state (with MII access).

Table 37 — CTC_3.2.6 – PCS transmit state diagram - ESD2 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.6 – PCS transmit state diagram - ESD2 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the ESD2 VECTOR state.

Table 37 *(continued)*

Item	Content
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 5 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for at least 2 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 6 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for 1 clock cycle, and then set TX_EN = TRUE in step 2.
Expected response	After step 2: After exiting the TRANSMIT DATA state, the IUT transmits ESD1, ESD2, and ESD3. After step 3 iteration a): After exiting the TRANSMIT DATA state, the IUT transmit ESD1, ESD2, and ESD3.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.8 CTC_3.2.7 – PCS transmit state diagram - ESD3 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Regardless of the transmissions on the MII, once the IUT enters the ESD3 VECTOR state the IUT should transmit ESD3, immediately transition to the SEND IDLE state, and transmit IDLE.

Table 38 specifies the CTC_3.2.7 – PCS transmit state diagram - ESD3 VECTOR state (with MII access).

Table 38 — CTC_3.2.7 – PCS transmit state diagram - ESD3 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.6 – PCS transmit state diagram - ESD2 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the ESD3 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.

Table 38 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = FALSE for 8 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for at least 3 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	Not applicable
Expected response	After step 2: After exiting the TRANSMIT DATA state, the IUT transmits ESD1, ESD2, ESD3, and idle symbols.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.9 CTC_3.2.8 – PCS transmit state diagram - ERR ESD1 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Regardless of the transmissions on the MII, once the IUT enters the ERR_ESD1 VECTOR state the IUT should transmit ESD1, immediately transition to the ERR ESD2 VECTOR state, and transmit ESD2.

Table 39 specifies the CTC_3.2.8 – PCS transmit state diagram - ERR ESD1 VECTOR state (with MII access).

Table 39 — CTC_3.2.8 – PCS transmit state diagram - ERR ESD1 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.8 – PCS transmit state diagram - ERR ESD1 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the ESD1 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 6 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for at least 2 clock cycles. 3. The LT shall monitor the transmissions from the IUT.

Table 39 *(continued)*

Item	Content
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 5 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for 1 clock cycle, and then set TX_EN = TRUE in step 2.
Expected response	After step 2: After exiting TRANSMIT DATA state, the IUT transmits ESD1, ESD2, and ERR ESD3. After step 3 iteration a): After exiting TRANSMIT DATA state, the IUT transmits ESD1, ESD2, and ERR ESD3.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.10 CTC_3.2.9 – PCS transmit state diagram - ERR ESD2 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Regardless of the transmissions on the MII, once the IUT enters the ERR ESD2 VECTOR state the IUT should transmit ESD2, immediately transition to the ERR ESD3 VECTOR state, and transmit ERR ESD3.

Table 40 specifies the CTC_3.2.9 – PCS transmit state diagram - ERR ESD2 VECTOR state (with MII access).

Table 40 — CTC_3.2.9 – PCS transmit state diagram - ERR ESD2 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.9 – PCS transmit state diagram - ERR ESD2 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the ERR ESD2 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2 Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 5 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for at least 2 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 6 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for 1 clock cycle, and then set TX_EN = TRUE in step 2.
Expected response	After step 2: After exiting the TRANSMIT DATA state, the IUT transmits ESD1, ESD2, and ERR ESD3. After step 3 iteration a): After exiting the TRANSMIT DATA state, the IUT transmits ESD1, ESD2, and ERR ESD3.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.2.11 CTC_3.2.10 – PCS transmit state diagram - ERR ESD3 VECTOR state (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS transmit state diagram. Regardless of the transmissions on the MII, once the IUT enters the ERR ESD3 VECTOR state the IUT should transmit ERR ESD3, immediately transition to the SEND IDLE state, and transmit IDLE.

Table 41 specifies the CTC_3.2.10 – PCS transmit state diagram - ERR ESD3 VECTOR state (with MII access).

Table 41 — CTC_3.2.10 – PCS transmit state diagram - ERR ESD3 VECTOR state (with MII access)

Item	Content
CTC # – Name	CTC_3.2.10 – PCS transmit state diagram - ERR ESD3 VECTOR state (with MII access)
Purpose	This CTC verifies that the IUT behaves while in the ERR ESD3 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.2, Figure 96-7 PCS transmit state diagram
Prerequisite	The LT shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The test system shall be capable of controlling the MII signals of the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). Connect the MII of the IUT to the MII test system and the ISO/IEC/IEEE 8802-3:2021 interface of the IUT to the link partner via the line tap.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link while the MII test system is sending TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE. 2. The LT shall instruct the MII test system to set TXD = 0101_2, TX_EN = TRUE, and TX_ER = TRUE for 8 clock cycles, then set TXD = 0000_2, TX_EN = FALSE, and TX_ER = FALSE for at least 3 clock cycles. 3. The LT shall monitor the transmissions from the IUT.
Iteration	Not applicable
Expected response	After step 2: After exiting the TRANSMIT DATA state, the IUT transmits ESD1, ESD2, ERR ESD3, and IDLE.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.3 PCS – Group 3: PCS receive (with MII access)

9.3.1 Overview

The CTCs specified in 9.3 verify the PCS receive defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in ISO/IEC/IEEE 8802-3:2021, 96.3.4.

9.3.2 CTC_3.3.1 – PCS receive signalling (with MII access)

This CTC is designed to ensure that the IUT decodes the ISO/IEC/IEEE 8802-3:2021 signalling during training, idle transmission, and data transmission.

Table 42 specifies the CTC_3.3.1 – PCS receive signalling (with MII access).

Table 42 — CTC_3.3.1 – PCS receive signalling (with MII access)

Item	Content
CTC # – Name	CTC_3.3.1 – PCS receive signalling (with MII access)
Purpose	This CTC verifies that the PCS decodes ISO/IEC/IEEE 8802-3:2021 signalling.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.4 PCS receive
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The UT shall configure the IUT as MASTER and the link partner as SLAVE. 2. The UT shall connect the IUT to a link partner and configure both devices to perform training and establish a link. Monitor the management indications from the IUT. 3. The UT shall connect the IUT to a link partner, establish a link, and configure the link partner to transmit valid PHY frames to the IUT. Monitor the management indications from the IUT. 4. The UT shall connect the IUT to a link partner, establish a link, and configure the link partner to transmit idle without PHY frames. Monitor the management indications from the IUT. 5. The UT shall configure the IUT as SLAVE and the link partner as MASTER. 6. The UT shall connect the IUT to a link partner and configure both devices to perform training and establish a link. Monitor the management indications from the IUT. 7. The UT shall connect the IUT to a link partner, establish a link, and configure the link partner to transmit valid PHY frames to the IUT. Monitor the management indications from the IUT. 8. The UT shall connect the IUT to a link partner, establish a link, and configure the link partner to transmit idle without PHY frames. Monitor the management indications from the IUT.
Iteration	Not applicable
Expected response	After step 2: The IUT accepts the idle pattern and establishes a link. After step 3: The IUT indicates link and receives PHY frames. After step 4: The IUT indicates reception of idle and maintain the link. After step 6: The IUT accepts the idle pattern and establish a link. After step 7: The IUT indicates link and should receive valid PHY frames. After step 8: The IUT indicates reception of idle and maintain the link.
Remark	None

9.3.3 CTC_3.3.2 – PCS automatic polarity detection (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.4.4 – PCS receive automatic polarity detection states that the IUT shall automatically detect the polarity of the received signal.

Table 43 specifies the CTC_3.3.2 – PCS automatic polarity detection (with MII access).

Table 43 — CTC_3.3.2 – PCS automatic polarity detection (with MII access)

Item	Content
CTC # – Name	CTC_3.3.2 – PCS automatic polarity detection (with MII access)
Purpose	This CTC verifies that the PCS detects polarity.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.4.4 PCS receive automatic polarity detection
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall support automatic polarity detection.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The UT shall connect the IUT to the link partner, transmit several PHY frames and observe that the link has been established. 2. The LT shall switch the polarity by reversing the pair connecting the IUT to the link partner and transmit several PHY frames and observe that the link has been established.
Iteration	Not applicable
Expected response	After step 2: The IUT establishes a link regardless of the receive polarity.
Remark	The IUT automatic polarity detection is an optional function. This CTC cannot be completed if the IUT does not implement automatic polarity detection.

9.3.4 CTC_3.3.3 – PCS receive SSD (with MII access)

The IUT should accept PHY frames with a valid SSD of (0,0), (0,0), (0,0).

Table 44 specifies the CTC_3.3.3 – PCS receive SSD (with MII access).

Table 44 — CTC_3.3.3 – PCS receive SSD (with MII access)

Item	Content
CTC # – Name	CTC_3.3.3 – PCS receive SSD (with MII access)
Purpose	This CTC verifies that the PCS accepts PHY frames with a valid SSD.
Reference	ISO/IEC/IEEE 8802-3:2021: — Figure 96-10 PCS receive state diagram; — 96.3.4.2 PCS receive symbol decoding.
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT shall transmit PHY frames with a valid SSD to the IUT while monitoring the IUT transmissions and counters.
Iteration	Not applicable

Table 44 *(continued)*

Item	Content
Expected response	After step 1: The IUT accepts all PHY frames.
Remark	None

9.3.5 CTC_3.3.4 – PCS receive ESD (with MII access)

The IUT should accept the frame with a valid ESD of (0,0), (0,0), (1,1).

Table 45 specifies the CTC_3.3.4 – PCS receive ESD (with MII access).

Table 45 — CTC_3.3.4 – PCS receive ESD (with MII access)

Item	Content
CTC # – Name	CTC_3.3.4 – PCS receive ESD (with MII access)
Purpose	This CTC verifies that the PCS accepts a frame with a valid ESD.
Reference	ISO/IEC/IEEE 8802-3:2021: — Figure 96-10 PCS receive state diagram; — 96.3.4.2 PCS receive symbol decoding.
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT shall transmit valid PHY frames to the IUT while monitoring the IUT transmissions and counters.
Iteration	Not applicable
Expected response	After step 1: The IUT accepts all PHY frames.
Remark	None

9.3.6 CTC_3.3.5 – PCS receive ERR ESD3 (with MII access)

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows that the IUT transitions to the RX_ERROR state and ISO/IEC/IEEE 8802-3:2021, 96.3.4.2 – PCS receive symbol decoding states that the IUT shall set pcs_rx_er = TRUE upon reception of ERR ESD3.

Table 46 specifies the CTC_3.3.5 – PCS receive ERR ESD3 (with MII access).

Table 46 — CTC_3.3.5 – PCS receive ERR ESD3 (with MII access)

Item	Content
CTC # – Name	CTC_3.3.4 – PCS receive ESD (with MII access)
Purpose	This CTC verifies that the PCS indicates reception of an error upon reception of ERR ESD3.
Reference	ISO/IEC/IEEE 8802-3:2021: — Figure 96-10 PCS receive state diagram; — 96.3.4.2 PCS receive symbol decoding.

Table 46 *(continued)*

Item	Content
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the test system via the line tap.
Step	1. The LT shall transmit a frame with `ERR ESD3` to the IUT while monitoring the IUT transmissions and counters.
Iteration	Not applicable
Expected response	After step 1: The IUT sets MII signal `RX_ER` to `TRUE`.
Remark	None

9.3.7 CTC_3.3.6 – PCS reception of stuff bits (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.4.2 – PCS receive symbol decoding states that the IUT shall discard stuff bits that are inserted during the 4B/3B transmit process.

Table 47 specifies the CTC_3.3.6 – PCS reception of stuff bits (with MII access).

Table 47 — CTC_3.3.6 – PCS reception of stuff bits (with MII access)

Item	Content
CTC # – Name	CTC_3.3.6 – PCS reception of stuff bits (with MII access)
Purpose	This CTC verifies that the PCS removes stuff bits during the 3B4B conversion for MII data.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.4.2 PCS receive symbol decoding
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order. The LT as a link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the link partner via the line tap.
Step	1. The LT shall transmit PHY frames of several lengths that are a multiple of 3 (when including 8 bytes for preamble), including but not limited to 64 bytes and 67 bytes, to the IUT while monitoring the IUT transmissions and counters. 2. The LT shall transmit PHY frames of several lengths that are 1 more than a multiple of 3 (when including 8 bytes for preamble), including but not limited to 66 bytes and 69 bytes, to the IUT while monitoring the IUT transmissions and counters. 3. The LT shall transmit PHY frames of several lengths that are 2 more than a multiple of 3 (when including 8 bytes for preamble), including but not limited to 65 bytes and 68 bytes, to the IUT while monitoring the IUT transmissions and counters.
Iteration	Not applicable
Expected response	After step 1: The IUT accepts all PHY frames.
Remark	None

9.3.8 CTC_3.3.7 – PCS de-interleave ternary pairs (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.10 – Generation of symbol sequence states that the IUT shall de-interleave the serial stream of ternary symbols as (TA_n, TB_n) or (TB_n, TA_n) to match the interleave order of the transmitter.

Table 48 specifies the CTC_3.3.7 – PCS de-interleave ternary pairs (with MII access).

Table 48 — CTC_3.3.7 – PCS de-interleave ternary pairs (with MII access)

Item	Content
CTC # – Name	CTC_3.3.7 – PCS de-interleave ternary pairs (with MII access)
Purpose	This CTC verifies that the PCS receiver de-interleaves the received ternary symbols in either ordering.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.3.3.3.10 Generation of symbol sequence
Prerequisite	The LT shall be capable of transmitting ternary symbols in either interleave order.
Set-up	The test system set-up shall be in accordance with Figure 5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The LT shall connect the IUT to the test system.
Step	1. The UT shall configure the LT to interleave the serial stream of ternary symbols as (TA_n, TB_n). 2. The UT shall connect the IUT to the LT, perform training, establish a link, and transmit PHY frames. The LT shall monitor the management indications from the IUT.
Iteration	a) REPEAT step 1 to step 2, but configure the LT to interleave the serial stream of ternary symbols as (TB_n, TA_n).
Expected response	After step 2: The IUT establishes a valid link and receives the transmitted PHY frames. After step 2 iteration a): The IUT establishes a valid link and receives the transmitted PHY frames.
Remark	None

9.4 PCS – Group 4: PCS receive state diagram (with MII access)

9.4.1 Overview

The CTCs specified in 9.4 verify the PCS receive state diagram defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in ISO/IEC/IEEE 8802-3:2021, 96.3.4.

9.4.2 CTC_3.4.1 – PCS receive state diagram (with MII access) - IDLE state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. The IUT should remain in the IDLE state while it is receiving idle.

Table 49 specifies the CTC_3.4.1 – PCS receive state diagram (with MII access) - IDLE state.

Table 49 — CTC_3.4.1 – PCS receive state diagram (with MII access) - IDLE state

Item	Content
CTC # – Name	CTC_3.4.1 – PCS receive state diagram (with MII access) - IDLE state
Purpose	This CTC verifies that the IUT behaves while in the IDLE state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.

Table 49 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending a valid idle. 2. The UT shall instruct the LT to send three SSD symbols. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 1 to step 3, except that the UT shall instruct the LT to send a ternary symbol that does not represent SSD1 or a valid idle code in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for two clock cycles, then RXD = $XXX1_2$ where X is determined by the test pattern sent from the LT transmit station. After step 3 iteration a): The IUT sets RX_ER = TRUE.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.3 CTC_3.4.2 – PCS receive state diagram (with MII access) - CHECK SSD2 state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT is in the CHECK SSD2 state, it should transition to the CHECK SSD3 state if it receives SSD2 or transition to the BAD SSD state if it receives anything else.

Table 50 specifies the CTC_3.4.2 – PCS receive state diagram (with MII access) - CHECK SSD2 state.

Table 50 — CTC_3.4.2 – PCS receive state diagram (with MII access) - CHECK SSD2 state

Item	Content
CTC # – Name	CTC_3.4.2 – PCS receive state diagram (with MII access) - CHECK SSD2 state
Purpose	This CTC verifies that the IUT behaves while in the CHECK SSD2 state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending a valid idle. 2. The UT shall instruct the LT to send three SSD symbols. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send SSD1 followed by a ternary symbol other than SSD2 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration a): The IUT sets RX_ER = TRUE.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.4 CTC_3.4.3 – PCS receive state diagram (with MII access) - CHECK SSD3 state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT is in the CHECK SSD3 state, it should transition to the SSD state if it receives SSD3 or transition to the BAD SSD state if it receives anything else.

Table 51 specifies the CTC_3.4.3 – PCS receive state diagram (with MII access) - CHECK SSD3 state.

Table 51 — CTC_3.4.3 – PCS receive state diagram (with MII access) - CHECK SSD3 state

Item	Content
CTC # – Name	CTC_3.4.3 – PCS receive state diagram (with MII access) - CHECK SSD3 state
Purpose	This CTC verifies that the IUT behaves while in the CHECK SSD3 state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send 2 SSD symbols followed by a ternary symbol other than SSD3 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration a): The IUT sets RX_ER = TRUE.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.5 CTC_3.4.4 – PCS receive state diagram (with MII access) - SSD state

The IUT is compatible with ISO/IEC/IEEE 8802-3:2021. Once the IUT enters the SSD state it should set the transition to the FIRST SSD state independent of the received content.

Table 52 specifies the CTC_3.4.4 – PCS receive state diagram (with MII access) - SSD state.

Table 52 — CTC_3.4.4 – PCS receive state diagram (with MII access) - SSD state

Item	Content
CTC # – Name	CTC_3.4.4 – PCS receive state diagram (with MII access) - SSD state
Purpose	This CTC verifies that the IUT behaves while in the SSD state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.

Table 52 *(continued)*

Item	Content
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols followed by a ternary symbol for 010_2. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except instruct LT to send three SSD symbols followed by a ternary symbol for data 000_2 in step 2. b) REPEAT step 2 to step 3, except instruct the LT to send three SSD symbols followed by the ternary symbol for SSD1 in step 2.
Expected response	After step 3: The IUT transitions to FIRST SSD and sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration a): The IUT transitions to FIRST SSD and sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration b): The IUT transitions to FIRST SSD and sets RX_DV = TRUE and RXD = 0101_2.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.6 CTC_3.4.5 – PCS receive state diagram (with MII access) - BAD SSD state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. The IUT enters the BAD SSD state upon reception of an error in the IDLE, CHECK SSD2, or CHECK SSD3 states. While in BAD SSD the IUT sets RX_ER = TRUE. The IUT waits for check_idle = TRUE to transition back to the IDLE state. The IUT should set check_idle = TRUE upon reception of 6 consecutive valid idle symbols.

Table 53 specifies the CTC_3.4.5 – PCS receive state diagram (with MII access) - BAD SSD state.

Table 53 — CTC_3.4.5 – PCS receive state diagram (with MII access) - BAD SSD state

Item	Content
CTC # – Name	CTC_3.4.5 – PCS receive state diagram (with MII access) - BAD SSD state
Purpose	This CTC verifies that the IUT behaves while in the BAD SSD state.
Reference	ISO/IEC/IEEE 8802-3:2021: — Figure 96-10 – PCS receive state diagram; — 96.3.4.1.1 Variables.
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send several ternary symbols that do not represent SSD or valid idle. 3. The LT shall monitor the MII transmissions from the IUT.

Table 53 *(continued)*

Item	Content
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send SSD followed by several ternary symbols that do not represent SSD or valid idle in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send 2 SSD symbols followed by several ternary symbols that do not represent SSD or valid idle in step 2. c) REPEAT step 2 to step 3, except instruct the test system to transmit a ternary symbol that does not represent SSD or valid idle, followed by 1 idle symbol and a valid frame in step 2. d) REPEAT iteration c), except send additional idle symbols before the frame until the IUT is observed to accept the frame. e) REPEAT iteration c) and d), except send an SSD symbol, 1 ternary symbol that does not represent SSD or valid idle, 1 idle symbol, and a valid frame in step 2. Increase the number of idle symbols until the IUT is observed to accept the frame in step 3. f) REPEAT iteration c) and d), except send 2 SSD symbols, 1 ternary symbol that does not represent SSD or valid idle, 1 idle symbol, and a valid frame in step 2. Increase the number of idle symbols until the IUT is observed to accept the frame in step 3.
Expected response	After step 2: The IUT sets RX_ER = TRUE while in the BAD SSD state. After step 3 iteration a): The IUT sets RX_ER = TRUE while in the BAD SSD state. After step 3 iteration b): The IUT sets RX_ER = TRUE while in the BAD SSD state. After step 3 iteration d): The IUT accepts the frame upon reception of 6 idle symbols after the non-SSD and non-idle symbol. After step 3 iteration e): The IUT accepts the frame upon reception of 6 idle symbols after the non-SSD and non-idle symbol. After step 3 iteration f): The IUT accepts the frame upon reception of 6 idle symbols after the non-SSD and non-idle symbol.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.7 CTC_3.4.6 – PCS receive state diagram (with MII access) - FIRST SSD state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Regardless of what is being received, once the IUT enters the FIRST SSD state it should set rx_data = 101_2 and transition to the SECOND SSD state.

Table 54 specifies the CTC_3.4.6 – PCS receive state diagram (with MII access) - FIRST SSD state.

Table 54 — CTC_3.4.6 – PCS receive state diagram (with MII access) - FIRST SSD state

Item	Content
CTC # – Name	CTC_3.4.6 – PCS receive state diagram (with MII access) - FIRST SSD state
Purpose	This CTC verifies that the IUT behaves while in the FIRST SSD state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.

Table 54 *(continued)*

Item	Content
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols followed by ternary symbols for 010_2 and 101_2. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols followed by the ternary symbols for 101_2 and 000_2 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols followed by the ternary symbols for 010_2 and SSD1 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.8 CTC_3.4.7 – PCS receive state diagram (with MII access) - SECOND SSD state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Regardless of what is being received, once the IUT enters the SECOND SSD state it should set rx_data = 010_2 and transition to the THIRD SSD state.

Table 55 specifies the CTC_3.4.7 – PCS receive state diagram (with MII access) - SECOND SSD state.

Table 55 — CTC_3.4.7 – PCS receive state diagram (with MII access) - SECOND SSD state

Item	Content
CTC # – Name	CTC_3.4.7 – PCS receive state diagram (with MII access) - SECOND SSD state
Purpose	This CTC verifies that the IUT behaves while in the SECOND SSD state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols, and then ternary symbols for 010_2, 101_2, and 010_2. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, and then ternary symbols for 010_2, 101_2, and 000_2 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, and then ternary symbols for 010_2, 101_2, and the ternary symbol for SSD1 in step 2.

Table 55 *(continued)*

Item	Content
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.9 CTC_3.4.8 – PCS receive state diagram (with MII access) - THIRD SSD state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT enters the THIRD SSD state it should set rx_data = 101_2 and transition to the CHECK ESD2 state if it receives ESD, or transition to the DATA state if it receives anything but ESD.

Table 56 specifies the CTC_3.4.8 – PCS receive state diagram (with MII access) - THIRD SSD state.

Table 56 — CTC_3.4.8 – PCS receive state diagram (with MII access) - THIRD SSD state

Item	Content
CTC # – Name	CTC_3.4.8 – PCS receive state diagram (with MII access) - THIRD SSD state
Purpose	This CTC verifies that the IUT behaves while in the THIRD SSD state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, and several ternary symbols representing data. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2 and 101_2, 010_2, and ESD1 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols and several ternary symbols for 000_2 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for six clock cycles and then transmits data. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2 for four clock cycles. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2 for two clock cycles, RXD = 0001_2 for one clock cycle, and then several clock cycles of RXD = 0000_2.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.10 CTC_3.4.9 – PCS receive state diagram (with MII access) - DATA state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT enters the DATA state, it should not exit until it receives ESD1.

Table 57 specifies the CTC_3.4.9 – PCS receive state diagram (with MII access) - DATA state.

Table 57 — CTC_3.4.9 – PCS receive state diagram (with MII access) - DATA state

Item	Content
CTC # – Name	CTC_3.4.9 – PCS receive state diagram (with MII access) - DATA state
Purpose	This CTC verifies that the IUT behaves while in the DATA state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, and several ternary symbols representing data, followed by ESD1. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, and ESD1 in step 2. b) REPEAT iteration a), sending additional data before the ESD1 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for 6 clock cycles and then transmits data, before setting RX_DV = FALSE and RXD = 0000_2. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles and transmits the data sent before the ESD.
Remark	In iteration b) the IUT cannot transmit 1 or 2 of the bits sent prior to the ESD because they can be received as stuff bits during the 3B4B conversion. This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.11 CTC_3.4.10 – PCS receive state diagram (with MII access) - CHECK ESD2 state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT enters the CHECK ESD2 state, it should transition to CHECK ESD3 upon reception of ESD2 or transition to BAD END if it receives anything other than ESD2.

Table 58 specifies the CTC_3.4.10 – PCS receive state diagram (with MII access) - CHECK ESD2 state.

Table 58 — CTC_3.4.10 – PCS receive state diagram (with MII access) - CHECK ESD2 state

Item	Content
CTC # – Name	CTC_3.4.10 – PCS receive state diagram (with MII access) - CHECK ESD2 state
Purpose	This CTC verifies that the IUT behaves while in the CHECK ESD2 state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.

Table 58 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, and several ternary symbols representing data, followed by ESD1, ESD2, and ESD3. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, and the ternary symbol for 000_2 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, and ESD3 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for 6 clock cycles and then transmits data, before setting RX_DV = FALSE and RXD = 0000_2. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles, and then sets RX_ER = TRUE. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles, and then sets RX_ER = TRUE.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.12 CTC_3.4.11 – PCS receive state diagram (with MII access) - CHECK ESD3 state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT enters the CHECK ESD3 state, it should transition to ESD upon reception of ESD3 or, RX ERROR upon reception of ERR ESD3, or BAD END if it receives anything else.

Table 59 specifies the CTC_3.4.11 – PCS receive state diagram (with MII access) - CHECK ESD3 state.

Table 59 — CTC_3.4.11 – PCS receive state diagram (with MII access) - CHECK ESD3 state

Item	Content
CTC # – Name	CTC_3.4.11 – PCS receive state diagram (with MII access) - CHECK ESD3 state
Purpose	This CTC verifies that the IUT behaves while in the CHECK ESD3 state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.

Table 59 *(continued)*

Item	Content
Step	1. The LT shall establish a valid link with the IUT. 2. The UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, and several ternary symbols representing data, followed by ESD1, ESD2, and ESD3. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, ESD2, and ERR ESD3 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, ESD2, and the ternary symbol for 000_2 in step 2. c) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, ESD2, ESD2, and ESD3 in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for 6 clock cycles and then transmits data, before setting RX_DV = FALSE and RXD = 0000_2. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 5 clock cycles, and then sets RX_ER = TRUE. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 5 clock cycles, and then sets RX_ER = TRUE. After step 3 iteration c): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 5 clock cycles, and then sets RX_ER = TRUE.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.13 CTC_3.4.12 – PCS receive state diagram (with MII access) – BAD ESD2 state

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT enters the BAD ESD2 state, it should set RX_ER = TRUE and transition to BAD END regardless of what is received.

Table 60 specifies the CTC_3.4.12 – PCS receive state diagram (with MII access) – BAD ESD2 state.

Table 60 — CTC_3.4.12 – PCS receive state diagram (with MII access) – BAD ESD2 state

Item	Content
CTC # – Name	CTC_3.4.12 – PCS receive state diagram (with MII access) – BAD ESD2 state
Purpose	This CTC verifies that the IUT behaves while in the BAD ESD2 state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.

Table 60 *(continued)*

Item	Content
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall istruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, and the ternary symbol for 000_2 twice. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, the ternary symbol for 000_2, and ESD3 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, the ternary symbol for 000_2, and SSD in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles, and then sets RX_ER = TRUE for 2 clock cycles. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles, and then sets RX_ER = TRUE for 2 clock cycles. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 4 clock cycles, and then sets RX_ER = TRUE for 2 clock cycles.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.4.14 CTC_3.4.13 – PCS receive state diagram (with MII access) - BAD END and RX ERROR states

ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the PCS receive state diagram. Once the IUT enters the BAD END or RX ERROR state, it should set RX_ER = TRUE and transition to IDLE regardless of what is received.

Table 61 specifies the CTC_3.4.13 – PCS receive state diagram (with MII access) - BAD END and RX ERROR states.

Table 61 — CTC_3.4.13 – PCS receive state diagram (with MII access) - BAD END and RX ERROR states

Item	Content
CTC # – Name	CTC_3.4.13 – PCS receive state diagram (with MII access) - BAD END and RX ERROR states
Purpose	This CTC verifies that the IUT behaves while in the BAD END or RX ERROR states.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-10 – PCS receive state diagram
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.
Set-up	The test system set-up shall be in accordance with Figure 6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, ESD2, and ERR ESD3. 3. The LT shall monitor the MII transmissions from the IUT.

Table 61 *(continued)*

Item	Content
Iteration	a) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, ESD2, and all ternary symbols that do not represent ESD3 or ERR ESD3 in step 2. b) REPEAT step 2 to step 3, except that the UT shall instruct the LT to send three SSD symbols, the ternary symbols for 010_2, 101_2, 010_2, 101_2, 010_2, ESD1, ESD2, and SSD in step 2.
Expected response	After step 2: The IUT sets RX_DV = TRUE and RXD = 0101_2 for 5 clock cycles, and then sets RX_ER = TRUE for one clock cycle. After step 3 iteration a): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 5 clock cycles, and then sets RX_ER = TRUE for one clock cycle. After step 3 iteration b): The IUT sets RX_DV = TRUE and RXD = 0101_2 for 5 clock cycles, and then sets RX_ER = TRUE for one clock cycle.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

9.5 PCS – Group 5: PCS JAB state diagram (with MII access)

9.5.1 Overview

The CTCs specified in 9.5 verify the JAB state diagram defined for ISO/IEC/IEEE 8802-3:2021 capable PHYs in ISO/IEC/IEEE 8802-3:2021, 96.3.4.

9.5.2 CTC_3.5.1 – PCS JAB state diagram (with MII access) - rcv_max_timer

ISO/IEC/IEEE 8802-3:2021, Figure 96-11 – JAB state diagram shows the valid transitions that an ISO/IEC/IEEE 8802-3:2021 device can take through the JAB state diagram. Once the IUT sets receiving = TRUE it enters the MONJAB state and starts the rcv_max_timer. Upon expiration of the timer, the IUT transitions to the JAB state, which causes the PCS receive state diagram to transition to the IDLE state. The value of rcv_max_timer should be within the range of 1,08 ms ± 54 µs.

This CTC is performed by sending a very large packet that is terminated with ESD1, ESD2, and ERR ESD3. If the frame is not long enough to cause a transition to the JAB state, then the PCS receive state diagram transitions to the RX ERROR state and sets pcs_rx_er = TRUE for one clock cycle while pcs_rx_dv = TRUE. If the frame is long enough to cause a transition to the JAB state, then the PCS receive state diagram transits directly to the IDLE state where it sets pcs_rx_dv = FALSE. The remaining frame data and/or ESD symbols causes a transition to the BAD SSD state where the IUT sets pcs_rx_er = TRUE while pcs_rx_dv = FALSE.

Table 62 specifies the CTC_3.5.1 – PCS JAB state diagram (with MII access) - rcv_max_timer.

Table 62 — CTC_3.5.1 – PCS JAB state diagram (with MII access) - rcv_max_timer

Item	Content
CTC # – Name	CTC_3.5.1 – PCS JAB state diagram (with MII access) - rcv_max_timer
Purpose	This CTC verifies that the IUT implements a rcv_max_timer of 1,08 ms ± 54 µs.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.3.4.4 PCS receive automatic polarity detection; — Figure 96-11 – JAB state diagram; — Figure 96-10 – PCS receive state diagram; — 96.3.4.1.3 Timer.
Prerequisite	The LT shall be capable of transmitting ternary symbols. The LT shall be capable of capturing the MII signals from the IUT.

Table 62 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure B.2. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the LT via the ISO/IEC/IEEE 8802-3:2021 and MII interfaces.
Step	1. The UT shall configure the LT such that the IUT establishes a valid link while the test system is sending valid idle. 2. The UT shall instruct the LT to send preamble and frame data for 1,026 ms, followed by `ESD1`, `ESD2`, and `ERR ESD3`. 3. The LT shall monitor the MII transmissions from the IUT.
Iteration	a) REPEAT step 2 to step 3, increasing the amount of data until the PCS receive state diagram transitions directly to the `IDLE` state.
Expected response	After step 3 iteration a): The IUT implements a `rcv_max_timer` within the range of 1,08 ms ± 54 µs.
Remark	This CTC cannot be performed if direct access to the IUT MII signals is not available.

10 PMA – IUT requirements and conformance test plan (with MII access)

10.1 PMA – Group 1: PMA electrical measurements (with MII access)

10.1.1 Overview

The CTCs specified in 10.1 verify the voltage parameters for capable PHY's defined in ISO/IEC/IEEE 8802-3:2021, Clause 5, the physical layer specifications and management parameters for 100 Mbit/s operation over a single balanced twisted pair cable.

10.1.2 CTC_5.1.1 – PMA maximum transmitter output droop (with MII access)

This CTC requires the IUT to operate in transmitter test mode 1. While in test mode 1, the IUT shall generate a sequence of at least 34 + 1 symbols followed by at least 34 - 1 symbols continually transmitted. Droop is calculated after measuring the peak voltage (V_{pk}) and the voltage 500 ns after the peak (V_{delay}). The droop is specified in ISO/IEC/IEEE 8802-3:2021, 96.5.4.1 - Transmitter output droop. This is performed on both, the positive and negative peaks of the waveform transmitted by test mode 1. The magnitude of the droop should be less than 45 %.

Table 63 specifies the CTC_5.1.1 – PMA maximum transmitter output droop (with MII access).

Table 63 — CTC_5.1.1 – PMA maximum transmitter output droop (with MII access)

Item	Content
CTC # – Name	CTC_5.1.1 – PMA maximum transmitter output droop (with MII access)
Purpose	This CTC verifies that the transmitter output level does not droop more than 45 % from the initial value.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.5.2 Test modes; — 96.5.3 Test fixtures; — 96.5.4.1 Transmitter output droop.

Table 63 *(continued)*

Item	Content
Prerequisite	The oscilloscope shall have the capability to measure the PAM3 signalling transmitted by the IUT MDI according to Figure C.3. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.3. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT so that it is operating in transmitter test mode 1. 2. The UT shall connect the BI_DA from the MDI to the test fixture 1. 3. The LT shall find the rising-edge initial peak voltage (V_{pk}) in the waveform. 4. The LT shall measure the amplitude of the waveform at 500 ns after the initial peak (V_{delay}) to find the droop voltage (V_d). 5. The LT shall compute the droop between V_{pk} and V_d.
Iteration	Not applicable
Expected response	After step 5: The maximum magnitude of both, the positive and negative droop, shall be less than 45 %.
Remark	For enhanced accuracy, repeat steps 3 to 5 multiple times.

10.1.3 CTC_5.1.2 – PMA transmitter distortion (with MII access)

In this CTC, the peak distortion is measured by capturing the test mode 4 waveform and finding the least mean squared error. The peak error between the ideal reference and the observed symbols is the peak transmitter distortion. ISO/IEC/IEEE 8802-3:2021, 96.5.4.2 - Transmitter distortion provides code for determining the peak distortion.

NOTE This code assumes that the disturber signal and the data acquisition clock of the oscilloscope are frequency-locked to the IUT `TX_TCLK`.

Table 64 specifies the CTC_5.1.2 – PMA transmitter distortion (with MII access).

Table 64 — CTC_5.1.2 – PMA transmitter distortion (with MII access)

Item	Content
CTC # – Name	CTC_5.1.2 – PMA transmitter distortion (with MII access)
Purpose	This CTC verifies that the distortion of the transmitter is within the conformance limits.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.5.2 Test modes; — 96.5.3 Test fixtures; — 96.5.4.2 Transmitter distortion.
Prerequisite	The high impedance differential probe shall be in accordance with C.2.2. The transmitter distortion adapter shall be in accordance with Figure C.2. The oscilloscope shall have the capability to measure the PAM3 signalling transmitted by the IUT MDI according to Figure C.5. The short automotive cable shall be in accordance with C.2.2.

Table 64 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure C.5. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT so that it is sourcing the transmitter test mode 4 waveform. 2. The UT shall configure the disturber source as specified in ISO/IEC/IEEE 8802-3:2021. 3. The UT shall connect the BI_DA from the MDI to test fixture 2. 4. The LT shall capture 2 ms of consecutive symbols in the test mode 4 waveform. 5. The LT shall process the capture using the code provided in ISO/IEC/IEEE 8802-3:2021 to calculate the peak distortion at 10 or more uniformly spaced phase offsets over 1 UI.
Iteration	Not applicable
Expected response	After step 5: The peak transmitter distortion should be less than 15 mV for all of the sampled phase offsets over 1 UI.
Remark	1. If the vertical resolution of the oscilloscope is less than 10-bit, then a low-pass filter is used during post-processing. The code provided in ISO/IEC/IEEE 8802-3:2021 includes such LPF. 2. If the TX_TCLK of the IUT is not accessible or the IUT does not have an external clock input, the test equipment is not able to synchronize internal sampling clocks. Because of this, phase offsets occur in the LT and measure distortion values are likely be greater than if the IUT's TX_TCLK is available.

10.1.4 CTC_5.1.3 – PMA transmitter timing jitter (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.2 - Test modes states that an ISO/IEC/IEEE 8802-3:2021 device shall implement 4 test modes. These test modes are provided to measure electrical characteristics and verify compliance. ISO/IEC/IEEE 8802-3:2021, 96.5.3 - Test fixtures specifies the test fixture to be used to perform the test. ISO/IEC/IEEE 8802-3:2021, 96.5.4.3 - Transmitter timing jitter provides a specification for the maximum allowable timing jitter for the transmitter.

Case 1 – MASTER transmitter timing jitter

When in test mode 2, the PHY transmits +1 symbols followed by -1 symbols continuously. In this mode, the transmitter output should be a 33 ⅓ MHz signal and the RMS TIE jitter measured at the PHY MDI output shall be less than 50 ps. The RMS TIE jitter is measured over an integration time interval of at least 1 ms.

Case 2 – SLAVE transmitter timing jitter

SLAVE transmitter timing jitter can only be performed when the IUTs TX_TCLK is exposed and accessible. For normal operation as the SLAVE, the IUTs reference clock is recovered from a compliant LP PHY operating as MASTER. The RMS TIE jitter of the SLAVE TX_TCLK shall not exceed 0,01 UI (150 ps).

Table 65 specifies the CTC_5.1.3 – PMA transmitter timing jitter (with MII access).

Table 65 — CTC_5.1.3 – PMA transmitter timing jitter (with MII access)

Item	Content
CTC # – Name	CTC_5.1.3 – PMA transmitter timing jitter (with MII access)
Purpose	This CTC verifies that the transmitter timing jitter of the PMA is within the conformance limits.
Reference	ISO/IEC/IEEE 8802-3:2021:

Table 65 *(continued)*

Item	Content
	— 96.5.2 Test modes; — 96.5.3 Test fixtures; — 96.5.4.3 Transmitter timing jitter.
Prerequisite	Case 1 MASTER: Test mode 2 at IUT Case 2 SLAVE: TX_TCLK access at IUT The oscilloscope shall have the capability to measure the PAM3 signalling transmitted by the IUT MDI according to Figure C.3. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.3. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	Case 1 – MASTER transmitter timing jitter 1. The UT shall configure the IUT so that it is operating in transmitter test mode 2. 2. The UT shall connect the BI_DA from the MDI to test fixture 1. 3. The LT shall capture at least 1 ms and process the capture to determine the RMS TIE jitter. Case 2 – SLAVE transmitter timing jitter 1. The UT shall configure the IUT so that it is operating in normal mode, forced to SLAVE. 2. The UT shall configure the LP so that it is operating in normal mode, forced to MASTER. 3. The UT shall connect the IUT TX_TCLK to the oscilloscope. 4. The LT shall establish a link between the IUT and the LP using a short automotive cable. 5. The LT shall capture at least 1 ms and process the capture of TX_TCLK to determine the RMS TIE jitter.
Iteration	Case 1: MASTER transmitter timing jitter a) For enhanced accuracy, repeat step 3 multiple times. Case 2: SLAVE transmitter timing jitter b) For enhanced accuracy, repeat step 4 multiple times.
Expected response	Case 1 – MASTER transmitter timing jitter After iteration a): The RMS TIE jitter measured at the MDI output should not exceed 50 ps. Case 2 – SLAVE transmitter timing After iteration b): The RMS TIE jitter of the SLAVE TX_TCLK should not exceed 0,01 UI (150 ps).
Remark	If the IUT does not provide access to the TX_TCLK, SLAVE jitter (case 2) testing cannot be performed as described in ISO/IEC/IEEE 8802-3:2021.

10.1.5 CTC_5.1.4 – PMA transmitter power spectral density (PSD) (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.2 - Test modes states that an ISO/IEC/IEEE 8802-3:2021 device shall implement 4 test modes. These test modes are provided to measure electrical characteristics and verify compliance. ISO/IEC/IEEE 8802-3:2021, 96.5.3 - Test fixtures specifies the test fixture to be used to perform the test. ISO/IEC/IEEE 8802-3:2021, 96.5.2 - Test modes specifies the operation of a device

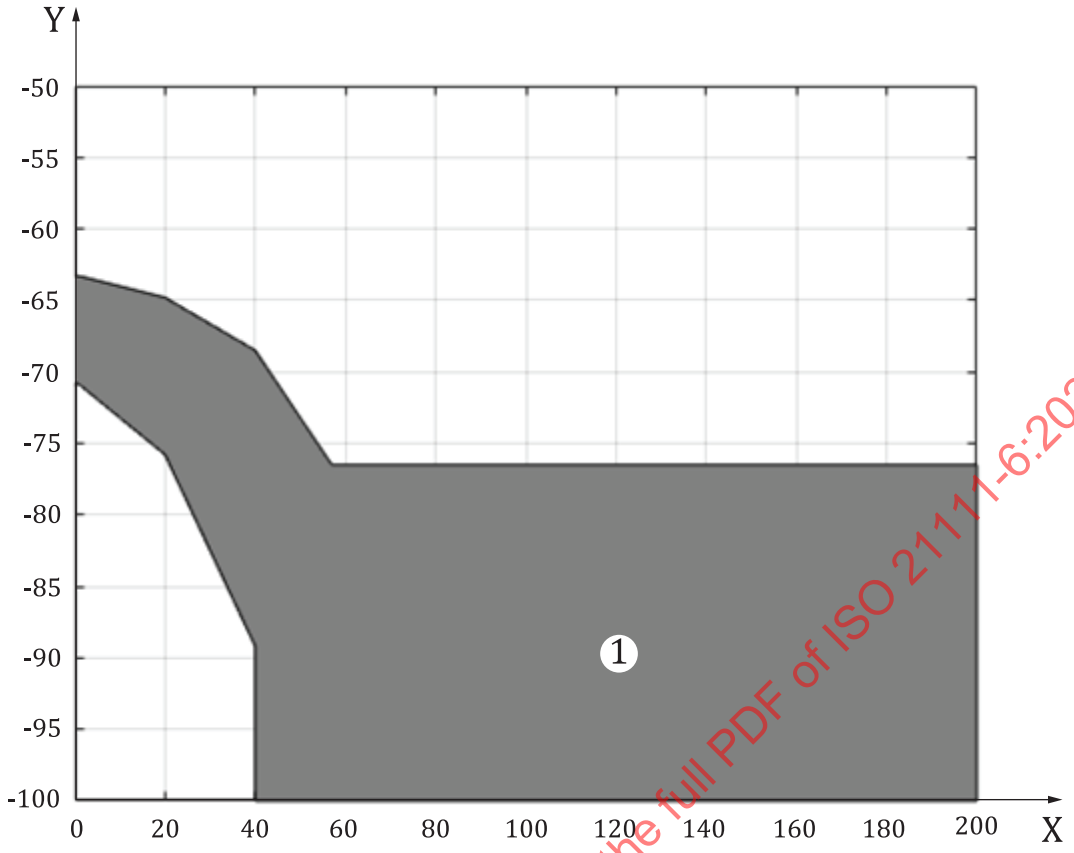
while in test mode 5, and ISO/IEC/IEEE 8802-3:2021, 96.5.4.4 - Transmitter power spectral density provides the transmitter PSD mask.

Table 66 specifies the CTC_5.1.4 – PMA transmitter power spectral density (PSD) (with MII access).

Table 66 — CTC_5.1.4 – PMA transmitter power spectral density (PSD) (with MII access)

Item	Content
CTC # – Name	CTC_5.1.4 – PMA transmitter power spectral density (PSD) (with MII access)
Purpose	This CTC verifies that the transmitter power spectral density is within the conformance limits.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.5.2 Test modes; — 96.5.3 Test fixtures; — 96.5.4.4 Transmitter power spectral density.
Prerequisite	The SA or oscilloscope shall support the spectral measurement capabilities. The balun (if necessary) shall be in accordance with C.1.4 and Figure C.6. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.6. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT so that it is operating in transmitter test mode 5. 2. The LT shall be connected to the MDI according to Figure C.6. 3. The UT shall configure the SA or oscilloscope settings: RBW = 10 kHz, VBW = 30 kHz, sweep time >60 s, detector = RMS. 4. The LT shall capture the spectrum of the transmitted test mode waveform using the SA or oscilloscope. 5. The UT shall compute the transmitter PSD.
Iteration	Not applicable
Expected response	After step 5: The PSD of the transmitter output while operating in test mode 5 fits within the transmitter PSD mask defined in ISO/IEC/IEEE 8802-3:2021, Figure 96–25 - PSD upper and lower limits.
Remark	None

Figure 7 shows the PMA transmitter power spectral density (PSD).



Key

X frequency in [MHz]

Y MDI return loss in [dBm/Hz]

1 compliant region

Figure 7 — PMA transmitter power spectral density (PSD)

10.1.6 CTC_5.1.5 – PMA transmit clock frequency (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.4.5 - Transmit clock frequency states that all ISO/IEC/IEEE 8802-3:2021 devices shall have a symbol transmission rate of 66 ⅔ MHz ± 100 ppm while operating in MASTER timing mode. This corresponds to a transmit clock of 66,660 3 MHz to 66,673 6 MHz. The reference clock used in this CTC is the one obtained in test CTC_5.1.3 – PMA transmitter timing jitter - Case 1. The frequency of this clock, extracted from the transmitted test mode 2 waveform, shall have a base frequency of 66 ⅔ MHz ± 100 ppm.

Table 67 specifies the CTC_5.1.5 – PMA transmit clock frequency (with MII access).

Table 67 — CTC_5.1.5 – PMA transmit clock frequency (with MII access)

Item	Content
CTC # – Name	CTC_5.1.5 – PMA transmit clock frequency (with MII access)
Purpose	This CTC verifies that the frequency of the transmit clock is within the conformance limits.
Reference	ISO/IEC/IEEE 8802-3:2021:

Table 67 *(continued)*

Item	Content
	— 96.5.2 Test modes; — 96.5.3 Test fixtures; — 96.5.4.5 Transmit clock frequency.
Prerequisite	The oscilloscope shall have the capability to measure the PAM3 signalling transmitted by the IUT MDI according to Figure C.3. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.3. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT so that it is operating in transmitter test mode 2. 2. The UT shall connect the BI_DA from the MDI to test fixture 1. 3. The LT shall use a narrow-bandwidth PLL to extract the clock frequency from the transmitted symbols. 4. For enhanced accuracy, repeat step 3 multiple times. 5. The UT shall measure the frequency of the transmit clock.
Iteration	Not applicable
Expected response	After step 5: The frequency of the IUT's transmit clock is between 66,660 3 MHz and 66,673 6 MHz.
Remark	None

10.1.7 CTC_5.1.6 – PMA MDI return loss (with MII access)

A compliant ISO/IEC/IEEE 8802-3:2021 device shall ideally have a differential characteristic impedance of 100 Ω. This is necessary to match the characteristic impedance of the automotive cabling. Any difference between these impedances results in a partial reflection of the transmitted signals. Return loss is a measure of the signal power that is reflected due to the impedance mismatch. ISO/IEC/IEEE 8802-3:2021, 96.8.2.1 – MDI return loss specifies the conformance limits for the reflected power measured at the MDI. The specification states that the return loss shall be maintained transmitting data or control symbols.

Table 68 specifies the CTC_5.1.6 – PMA MDI return loss (with MII access).

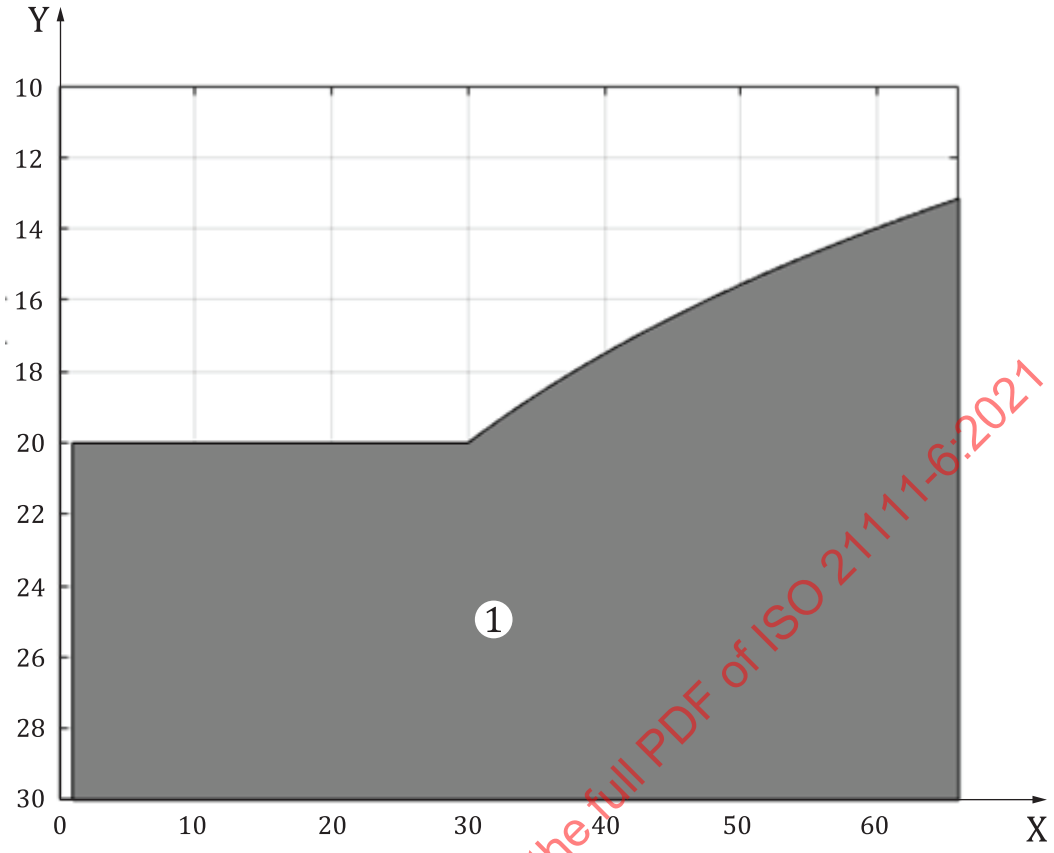
Table 68 — CTC_5.1.6 – PMA MDI return loss (with MII access)

Item	Content
CTC # – Name	CTC_5.1.6 – PMA MDI return loss
Purpose	This CTC measures the return loss at the MDI.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.8.2.1 MDI return loss

Table 68 *(continued)*

Item	Content
Prerequisite	IUT: Active transmitter The VNA or TDR with frequency domain capabilities or the oscilloscope with frequency domain capabilities shall be in accordance with C.1.4. The balun (if necessary) shall be in accordance with C.1.4 and Figure C.7. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.7. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT for SLAVE mode operation. 2. The LT shall calibrate the VNA (or TDR, or oscilloscope) to remove the effects of the test jig and connecting cable. 3. The UT shall connect the BI_DA from the MDI to the test equipment. 4. The UT shall measure the reflections at the MDI referenced to a 100 Ω characteristic impedance.
Iteration	Not applicable
Expected response	After step 4: The return loss measured at the MDI is at least 20 dB from 1 MHz to 30 MHz, and at least 20 – 20 × log10(F/30) dB from 30 MHz to 66 MHz when referenced to a characteristic impedance of 100 Ω, as shown in Figure 8.
Remark	None

Figure 8 shows the PMA MDI return loss.



Key

X frequency [MHz]

Y MDI return loss [dB]

1 compliant region

Figure 8 — PMA MDI return loss

10.1.8 CTC_5.1.7 – PMA MDI mode conversion loss (with MII access)

A compliant ISO/IEC/IEEE 8802-3:2021 device shall ideally have a differential characteristic impedance of 100 Ω. Mismatches in the positive and negative polarities of the MDI output introduce mode conversion. ISO/IEC/IEEE 8802-3:2021, 96.8.2.2 – MDI mode conversion loss specifies the conformance limits for the mode conversion measured at the MDI.

Table 69 specifies the CTC_5.1.7 – PMA MDI mode conversion loss (with MII access).

Table 69 — CTC_5.1.7 – PMA MDI mode conversion loss (with MII access)

Item	Content
CTC # – Name	CTC_5.1.7 – PMA MDI mode conversion loss (with MII access)
Purpose	This CTC verifies that the measurement of the mode conversion loss at the MDI meets the requirements stated in ISO/IEC/IEEE 8802-3:2021, 96.8.2.2.
Reference	ISO/IEC/IEEE 8802-3:2021, 96.8.2.2 MDI mode conversion loss

Table 69 *(continued)*

Item	Content
Prerequisite	The VNA or TDR with frequency domain capabilities or the oscilloscope with frequency domain capabilities shall be in accordance with C.1.4. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.7. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT for SLAVE mode operation. 2. The LT shall calibrate the VNA (or TDR, or oscilloscope) to remove the effects of the test jig and connecting cable. 3. The UT shall connect the BI_DA from the MDI to the test equipment. 4. The UT shall measure the mode conversion at the MDI referenced to a 100 Ω characteristic impedance.
Iteration	Not applicable
Expected response	After step 4: The mode conversion loss measured at the MDI meets a specified mask in Figure 9. The mask described in Figure 9 is modified from the definition provided in ISO/IEC/IEEE 8802-3:2021, 96.8.2.2 – MDI mode conversion loss. An equivalent formula is specified in Formula (1).
Remark	When measuring mode conversion loss, the impedance balance of the cabling and test fixtures in the test set-up is critical. Any fixtures used to connect the MDI of the IUT to the test equipment should have sufficient mode conversion loss margin compared to the MDI requirement. To achieve a high degree of reliability of measurement results it is recommended, that the test fixture mode conversion loss meet a specified mask when referenced to a characteristic impedance differential mode of 100 Ω and characteristic impedance common mode of 25 Ω, see Figure 10 and Formula (2).

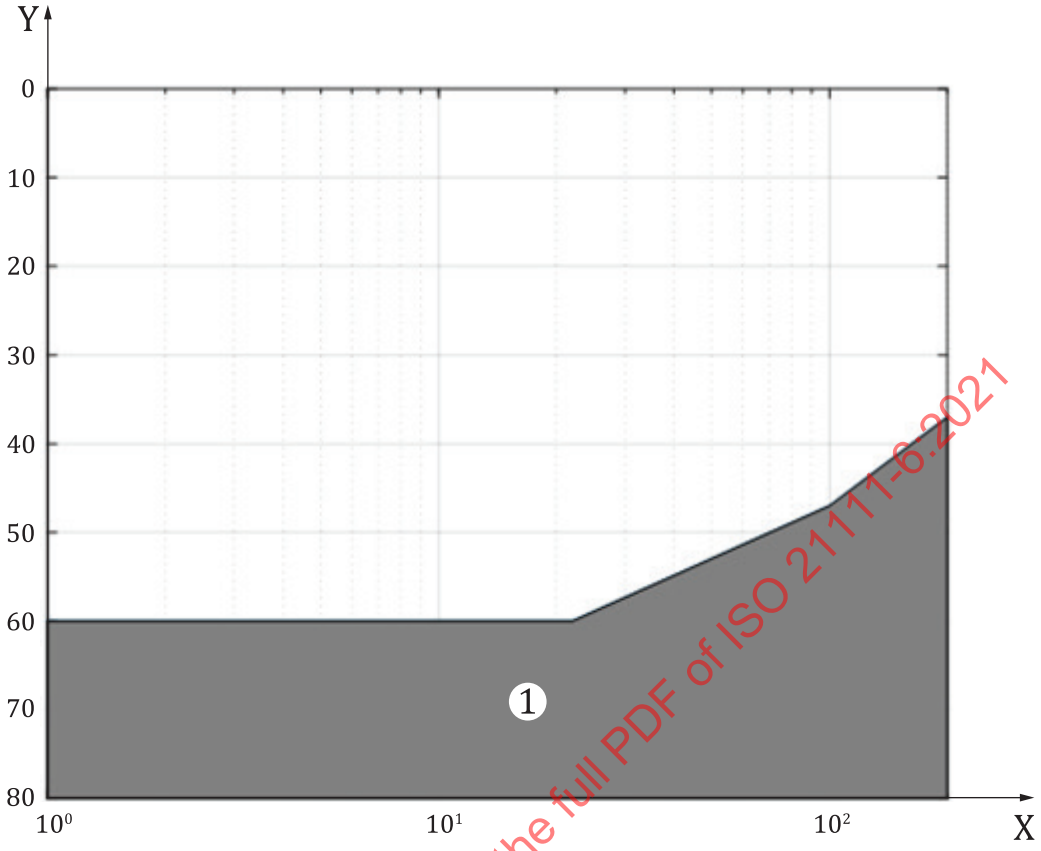
$$
\begin{aligned}
&\text{IF } F \geq 1) \text{ AND } (F < 22) \\
&\qquad T_{CL}(F) = 60 \\
&\text{ELSE IF } (F \geq 22) \text{ AND } (F < 100) \\
&\qquad T_{CL}(F) = 60 - \left(\frac{13}{\log_{10}\left(\frac{100}{22}\right)} \right) \times \log_{10}\left(\frac{F}{22}\right) \\
&\text{ELSE } (F \geq 100) \text{ AND } (F < 200) \\
&\qquad T_{CL}(F) = 47 - \left(\frac{10}{\log_{10}\left(\frac{200}{100}\right)} \right) \times \log_{10}\left(\frac{F}{100}\right)
\end{aligned}
\tag{1}
$$

where

F is the frequency, in MHz;

T_{CL} is the transverse conversion loss, in dB.

Figure 9 shows the PMA MDI mode conversion loss.



Key

X frequency [MHz]
Y MDI mode conversion loss [dB]
1 compliant region

Figure 9 — PMA MDI mode conversion loss

PMA MDI mode conversion loss test fixture

Formula (2) specifies the test fixture for the MDI mode conversion loss measurement.

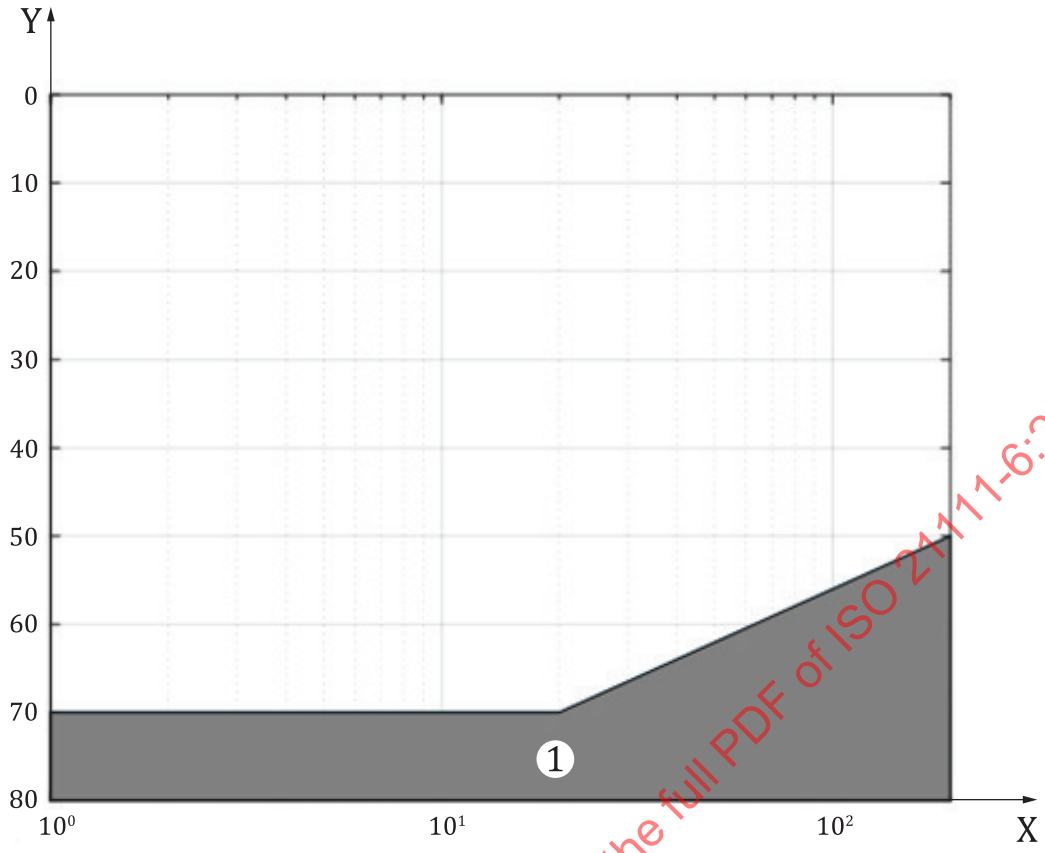
$$\begin{aligned} &\text{IF } (F \geq 1) \text{ AND } (F < 20) \\ &\quad T_{CL}(F) = 70 \\ &\text{ELSE } (F \geq 20) \text{ AND } (F < 200) \\ &\quad T_{CL}(F) = 70 - 20 \times \log_{10}\left(\frac{F}{20}\right) \end{aligned} \tag{2}$$

where

F is the frequency, in MHz;

T_{CL} is the transverse conversion loss, in dB.

Figure 10 shows the PMA MDI mode conversion loss test fixture.



Key

X frequency [MHz]

Y test fixture transverse conversion loss [dB]

1 compliant region

Figure 10 — PMA MDI mode conversion loss test fixture

10.1.9 CTC_5.1.8 – PMA transmitter peak differential output (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.6 – Transmitter peak differential output states that any ISO/IEC/IEEE 8802-3:2021 transmitter peak-to-peak differential amplitude shall be less than 2,2 × V_{PP} when measured with a 100 Ω termination. It also states that this is to be true for all transmit modes including SEND_I and SEND_N modes. This CTC could be performed when the IUT is configured as MASTER and in the TRAINING state of the PHY control state diagram. Test mode 5, as described in ISO/IEC/IEEE 8802-3:2021, 96.5.2 – Test modes, is labeled as normal operation at full power and is generated by transmitting random data through the same scrambling process as SEND_I. Either operating mode should be sufficient for this CTC and yield comparable results. Test fixture 1, specified in ISO/IEC/IEEE 8802-3:2021, 96.5.3 – Test fixtures, should be used to measure transmitter peak differential output.

Table 70 specifies the CTC_5.1.8 – PMA transmitter peak differential output (with MII access).

Table 70 — CTC_5.1.8 – PMA transmitter peak differential output (with MII access)

Item	Content
CTC # – Name	CTC_5.1.8 – PMA transmitter peak differential output (with MII access)
Purpose	This CTC verifies that the peak-to-peak differential amplitude does not exceed the specified amount.

Table 70 *(continued)*

Item	Content
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.5.2 Test modes; — 96.5.3 Test fixtures; — 96.5.6 Transmitter peak differential output.
Prerequisite	IUT: Active transmitter The oscilloscope shall have the capability of to measure the PAM3 signalling transmitted by the IUT MDI according to Figure C.3. The differential probe or the 2-pin to SMA adapter with a matched length of 50-Ω coaxial cables shall be in accordance with C.2.2. The short automotive cable shall be in accordance with C.2.2.
Set-up	The test system set-up shall be in accordance with Figure C.3. Refer to Annex C. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT so that it is operating as MASTER or operating in transmitter test mode 5. 2. The UT shall connect the BI_DA from the MDI to test fixture 1. 3. The UT shall measure the peak-to-peak amplitude of the waveform. 4. For enhanced accuracy, repeat step 3 multiple times.
Iteration	Not applicable
Expected response	After step 4: The maximum differential peak-to-peak amplitude of the waveform shall be less than 2,2 V_{PP}.
Remark	None

10.2 PMA – Group 2: PMA receive tests (with MII access)

10.2.1 Group 2 overview

The CTCs specified in 10.2 verify the integrity of the ISO/IEC/IEEE 8802-3:2021 PMA receiver through frame reception tests.

10.2.2 CTC_5.2.1 – PMA bit error rate verification (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.5.1 - Receiver differential input signals states that an ISO/IEC/IEEE 8802-3:2021 capable PHY shall not exceed a BER of less than 10^{-10}. The cables used for receiver BER testing are automotive cables, conformant to the characteristics described in ISO/IEC/IEEE 8802-3:2021, 96.7 – Link segment characteristics but representative of a worst-case channel. Channel characteristics of the worst-case channel are further discussed in C.3. Packet transmit and monitoring test systems are used to verify the BER of the IUT. If more than seven errors are observed in 3 × 1010_2 bit (about 2 470 000, which equals 1 518-byte packets), it can be concluded that the error rate is greater than 10^{-10} with less than a 5 % chance of error. If no errors are observed, it can be concluded that the BER is no more than 10^{-10} with less than a 5 % chance of error.

Table 71 specifies the CTC_5.2.1 – PMA bit error rate verification (with MII access).

Table 71 — CTC_5.2.1 – PMA bit error rate verification (with MII access)

Item	Content
CTC # – Name	CTC_5.2.1 – PMA bit error rate verification (with MII access)

Table 71 *(continued)*

Item	Content
Purpose	This CTC verifies that the IUT can maintain a BER of less than 10^{-10}.
Reference	ISO/IEC/IEEE 8802-3:2021: — 96.5.5.1 Receiver differential input signals; — 96.7 Link segment characteristics.
Prerequisite	The packet transmit/monitoring test system shall be in accordance with C.2.8. The automotive cables of varying lengths shall be in accordance with C.3.
Set-up	The test system set-up shall be in accordance with Figure C.9. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT as MASTER. 2. The UT shall connect the packet monitoring test system to the automotive cable. 3. The UT shall connect the IUT to the automotive cable. 4. The LT shall send 2 470 000 1 518-byte packets (for a 10^{-10} BER) and the monitor counts the number of packet errors.
Iteration	a) REPEAT step 4 for the remaining automotive cables, 1 time. b) REPEAT step 4 with the IUT configured as SLAVE, 1 time.
Expected response	After step 4 iteration a): The IUT maintains in a BER of less than 10^{-10} for all automotive cable lengths. After step 4 iteration b): The IUT maintains in a BER of less than 10^{-10} for all automotive cable lengths.
Remark	None

10.2.3 CTC_5.2.2 – PMA receiver frequency tolerance (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.5.2 - Receiver frequency tolerance states that an ISO/IEC/IEEE 8802-3:2021 capable PHY shall accept incoming data with the symbol rate of 66 ⅔ MHz ± 6 ⅔ kHz. This corresponds to a transmit clock of 66,660 3 MHz to 66,673 6 MHz. Please refer to CTC_5.2.1 – PMA bit error rate verification (10.2.2) for further details regarding the worst-case channel and packet analysis. The cables used for receiver frequency tolerance testing are automotive cables, conformant to the characteristics described in ISO/IEC/IEEE 8802-3:2021, 96.7 – Link segment characteristics but representative of a worst-case channel. Channel characteristics of the worst-case channel are further described in C.3.

Table 72 specifies the CTC_5.2.2 – PMA receiver frequency tolerance (with MII access).

Table 72 — CTC_5.2.2 – PMA receiver frequency tolerance (with MII access)

Item	Content
CTC # – Name	CTC_5.2.2 – PMA receiver frequency tolerance (with MII access)
Purpose	This CTC verifies that the IUT can accept incoming data with the symbol rate of 66 ⅔ MHz ± 6 ⅔ kHz.
Reference	C.3 and ISO/IEC/IEEE 8802-3:2021: — 96.5.5.2 Receiver frequency tolerance; — 96.7 Link segment characteristics.
Prerequisite	The packet transmit/monitoring test system shall be capable of a configurable transmit clock in accordance with C.2.8. The automotive cable representative of worst-case channel shall be in accordance with C.3.

Table 72 *(continued)*

Item	Content
Set-up	The test system set-up shall be in accordance with Figure C.9. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).
Step	1. The UT shall configure the IUT as SLAVE. 2. The UT shall connect the packet transmit/monitoring test system to the automotive cable. 3. The UT shall connect the IUT to the automotive cable. 4. The UT shall configure the packet transmit/monitoring test system to transmit data with a clock of 66,660 0 MHz. 5. The LT shall send 2 470 000 1 518-byte packets (for a 10^{-10} BER) and monitor the number of packet errors.
Iteration	a) REPEAT step 3 to step 5 using a transmit clock of 66,673 6 MHz.
Expected response	After step 5: The IUT maintains a BER of less than 10^{-10} when recovering a transmit clock of 66,660 0 MHz for all automotive cable lengths. After step 5 iteration a): The IUT maintains a BER of less than 10^{-10} when recovering a transmit clock of 66,673 3 MHz for all automotive cable lengths.
Remark	None

10.2.4 CTC_5.2.3 – PMA alien crosstalk noise rejection (with MII access)

ISO/IEC/IEEE 8802-3:2021, 96.5.5.3 – Alien crosstalk noise rejection specifies a test cable which uses a resistive network to inject crosstalk noise into the receive path of the IUT. ISO/IEC/IEEE 8802-3:2021, 96.5.5.3 – Alien crosstalk noise rejection goes on to state that an ISO/IEC/IEEE 8802-3:2021 capable PHY shall not exceed a BER of less than 10^{-10}, even with alien crosstalk noise present. The cables used for receiver frequency tolerance testing are automotive cables, conformant to the characteristics described in ISO/IEC/IEEE 8802-3:2021, 96.7 – Links characteristics but representative of a worst-case channel. Channel characteristics of the worst-case channel are further discussed in C.3.

Table 73 specifies the CTC_5.2.3 – PMA alien crosstalk noise rejection (with MII access).

Table 73 — CTC_5.2.3 – PMA alien crosstalk noise rejection (with MII access)

Item	Content
CTC # – Name	CTC_5.2.3 – PMA alien crosstalk noise rejection (with MII access)
Purpose	This CTC verifies that the IUT can maintain a bit error rate of less than 10^{-10} in the presence of a crosstalk noise source.
Reference	C.3 and ISO/IEC/IEEE 8802-3:2021: — 96.5.5.3 Alien crosstalk noise rejection; — 96.7 Links characteristics.
Prerequisite	The packet transmit/monitoring test system shall be capable of coupling crosstalk noise in accordance with C.2.9. The worst-case automotive crosstalk noise injection cable shall be in accordance with C.2.9 noise source injection.
Set-up	The test system set-up shall be in accordance with Figure C.10. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet).

Table 73 *(continued)*

Item	Content
Step	1. The UT shall configure the IUT as MASTER or SLAVE. 2. The UT shall connect the packet transmit/monitoring test system to the worst-case automotive crosstalk noise injection cable. 3. The UT shall connect the IUT to the worst-case automotive crosstalk noise injection cable. 4. The LT shall send 2 470 000 1 518-byte packets (for a 10^{-10} BER) and the monitor counts the number of packet errors.
Iteration	a) REPEAT step 2 to step 4 with the IUT configured as MASTER and using a Gaussian signal generator as the noise source, 1 time. b) REPEAT step 2 to step 4 with the IUT configured as SLAVE and using a Gaussian signal generator as the noise source, 1 time.
Expected response	After step a, b): The IUT shall maintain a BER of less than 10^{-10} when using the worst-case automotive crosstalk noise injection cable with a compliant ISO/IEC/IEEE 8802-3:2021 transmitter as the noise source. After step a, b): The IUT shall maintain a BER of less than 10^{-10} when using the worst-case automotive crosstalk noise injection cable with a Gaussian signal generator as the noise source.
Remark	None

Annex A
(informative)

PHY control – Test suite

A.1 PHY control – Additional information

A.1.1 PHY control – Overview

The PHY control test suite is intended to provide additional low-level technical details pertinent to specific tests defined in this test suite. The PHY control test suite cover topics that are beyond the scope of this document, but are specific to the methodologies used for performing the measurements covered in this test suite. This also includes details regarding a specific interpretation of this document (for the purposes of this test suite), in cases where a specification appears unclear or otherwise open to multiple interpretations.

A.1.2 PHY control – Scope

The PHY Control test suite is considered informative and pertains only to tests contained in this test suite.

A.2 PHY control – Test system set-up

A.2.1 PHY control – Purpose

The purpose of the test system set up is to provide the requirements of the test systems used during ISO/IEC/IEEE 8802-3:2021 PHY control testing.

A.2.2 PHY control – Discussion

Two test systems are required to perform all tests that are specified in this document. The ISO/IEC/IEEE 8802-3:2021 receive test system examines the transmissions from the IUT, and the ISO/IEC/IEEE 8802-3:2021 transmit test system transmits the necessary test patterns to test the receiver of the IUT. It is possible to combine both test systems into one set-up.

The ISO/IEC/IEEE 8802-3:2021 receive test system consists of an oscilloscope and software to capture and decode the transmissions from the IUT. The IUT connects to the test system through the line tap as specified in A.3. The software downloads the capture from the oscilloscope and decodes the ternary symbols, using knowledge of the ISO/IEC/IEEE 8802-3:2021 encoding, to create the MII data stream. The test set-up is shown in Figure A.1.

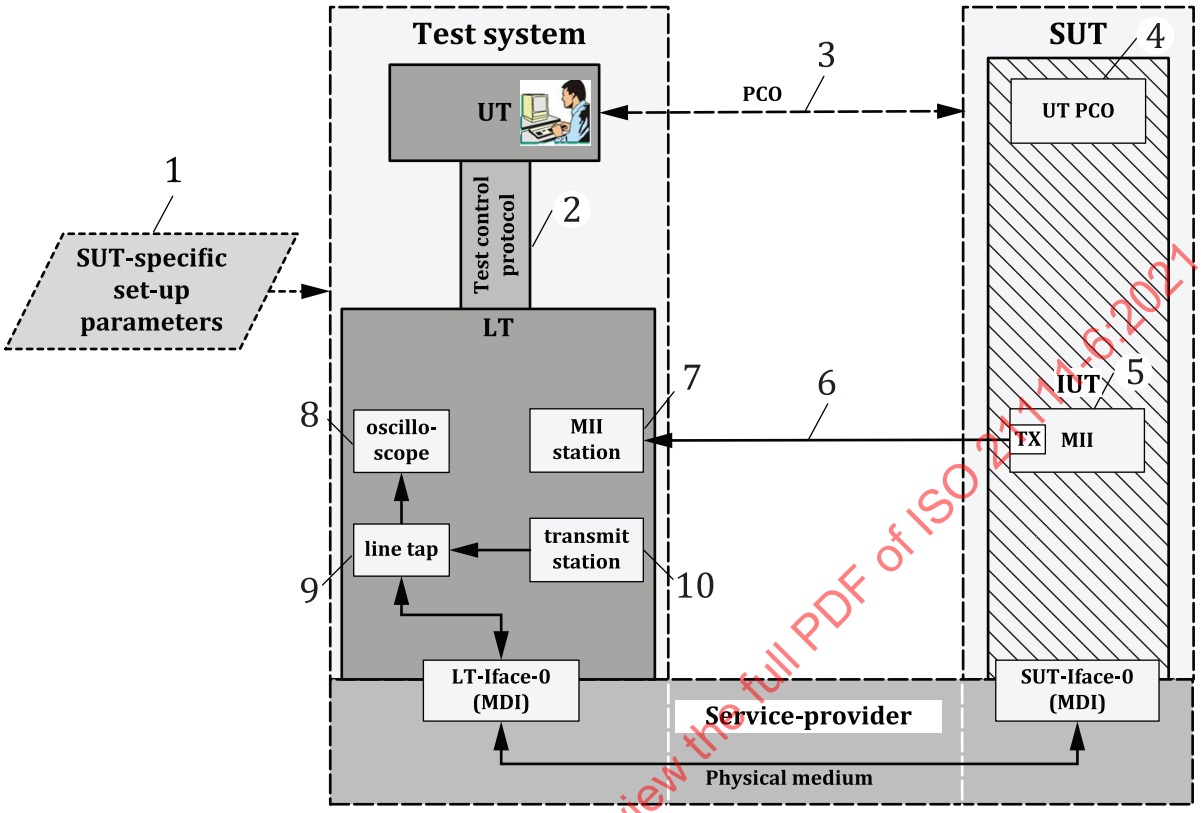
The MII station, transmit station, line tap, and the oscilloscope are part of the LT.

The purpose of the MII station (Figure A.1 key 7) is to directly interact with the MII of the IUT (Figure A.1 key 5), manipulating the TX pins of the IUT MII (Figure A.1 key 6) to verify that the signals transmitted by the MII station of the LT are properly converted to PAM3 PHY frames transmitted by the IUT MDI via the SUT-Iface-0.

The purpose of the line tap (Figure A.1 key 9) is to allow directional monitoring of the signalling from the physical medium. The receive signal from the LT-Iface-0 is then captured on the oscilloscope (Figure A.1 key 8).

The purpose of the oscilloscope (Figure A.1 key 8) is to measure the PAM3 signalling transmitted by the IUT MDI, allowing for capture and decoding of the ISO/IEC/IEEE 8802-3:2021 ternary symbols.

The MII test system is mandatory for some tests, while it can be replaced with higher OSI layers or a loopback in some tests, other solutions, such as an FPGA that can capture the ternary symbols, are possible. The test system does not modify or affect the transmissions from the IUT in any manner.



Key

1 SUT-specific set-up parameters (node's electronic data sheet)
2 test control protocol
3 points of control and observation and abstract service primitives
4 UT PCO test system operator interface
5 MII interface with TX
6 manipulation of IUT MII TX interface
7 MII station
8 oscilloscope
9 line tap
10 transmit station

Figure A.1 — ISO/IEC/IEEE 8802-3:2021 receive test system set-up

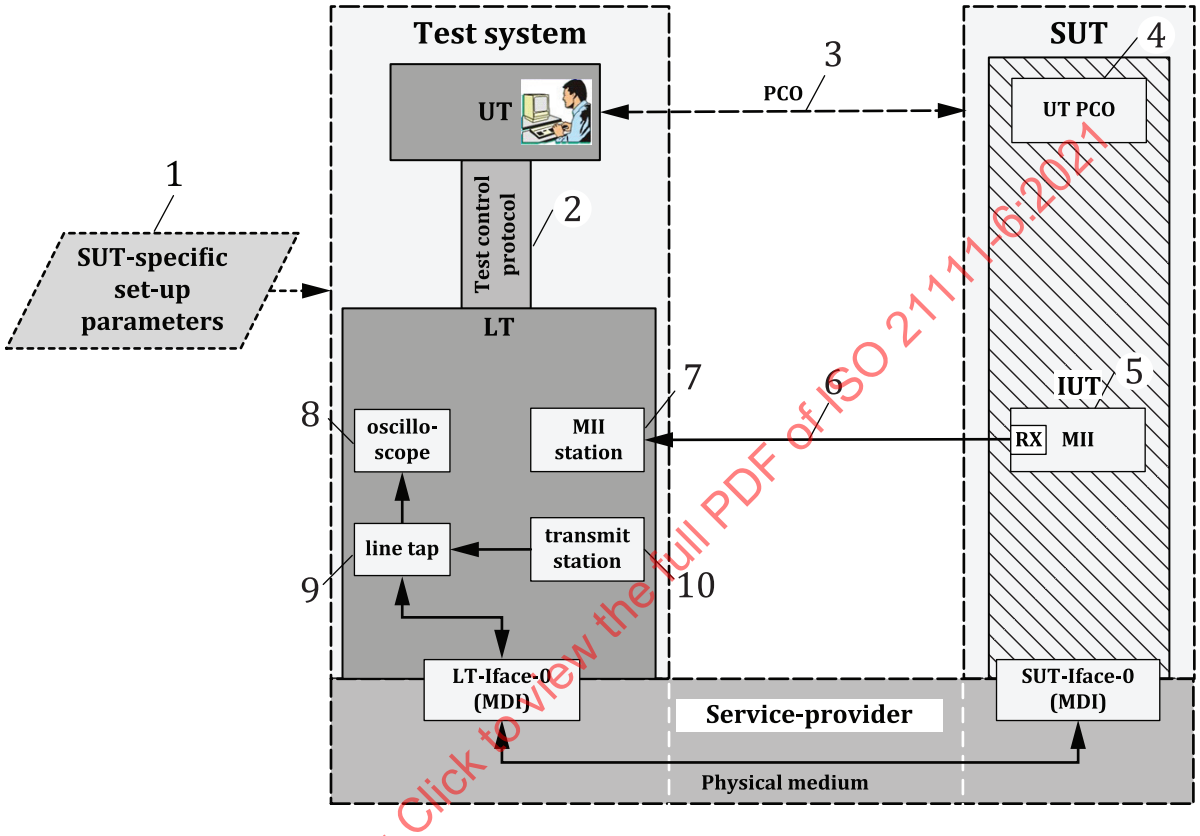
The ISO/IEC/IEEE 8802-3:2021 transmit test system consists of software and hardware that is capable of transmitting arbitrary ternary symbols to the IUT. The ability to send arbitrary sequences, such as invalid transitions of the PCS transmit state machine, is essential to test the receiver of the IUT. The test set-up is shown in Figure A.2.

The MII station, transmit station, line tap and the oscilloscope are part of the LT.

The purpose of the MII station (Figure A.2 key 7) is to directly interact with the MII of the IUT (Figure A.2 key 5), monitoring the RX pins of the IUT MII (Figure A.2 key 6) to verify that PHY frames received at the SUT-Iface-0 (MDI) are converted appropriately to bits recognizable by the MAC of the LT.

The purpose of the transmit station (Figure A.2 key 10) is to act as a link partner with the IUT. The transmit station transmits ISO/IEC/IEEE 8802-3:2021 PAM3 encoding such that the IUT can achieve a link and receive ternary symbol sequences designed to stress the IUT implementation.

The purpose of the line tap (Figure A.2 key 9) is to allow directional monitoring of the signalling from the physical medium. The receive signal from the LT-Iface-0 is then captured on the oscilloscope (Figure A.2 key 8).



Key

1 SUT-specific set-up parameters (node's electronic data sheet)
2 test control protocol
3 points of control and observation and abstract service primitives
4 UT PCO test system operator interface
5 MII interface
6 monitoring of the RX pins of the IUT MII interface
7 MII station
8 oscilloscope
9 line tap
10 transmit station

Figure A.2 — ISO/IEC/IEEE 8802-3:2021 transmit test system set-up

A.3 PHY control – Line tap

A.3.1 PHY control – Purpose

The purpose of the line tap is to connect the oscilloscope and to capture the transmissions from the IUT MDI.

A.3.2 PHY control – Discussion

The line tap fixture is used for collecting the necessary oscilloscope captures to perform this testing. Such a fixture is necessary to measure the IUT transmit signal while the IUT maintains a link with the link partner. The line tap can be constructed or implemented in several ways, for that reason a specific implementation is not specified in this document. Since the line tap is part of the test channel between the IUT and link partner, the only performance requirement is that the channel (including the line tap) meets the link-segment requirement of ISO/IEC/IEEE 8802-3:2021.

Annex B
(normative)

PCS – Test suite

B.1 PCS – Testing devices with MII access

B.1.1 PCS – Overview of CTCs that are possible with MII access

The PCS test suite is intended to provide additional low-level technical details pertinent to specific CTCs defined in this CTP. The CTP annexes often cover topics that are beyond the scope of this document, but are specific to the methodologies used for performing the measurements covered in this test suite. This may also include details regarding a specific interpretation of this document (for the purposes of this test suite), in cases where a specification may appear unclear or otherwise open to multiple interpretations.

B.1.2 PCS – Line tap

The line tap fixture is used for collecting the necessary oscilloscope captures to perform this testing. Such a fixture is necessary to measure the IUT transmit signal while the IUT maintains a link with the link partner. The line tap can be constructed or implemented in several ways, for that reason a specific implementation is not specified in this document. Since the line tap is part of the test channel between the IUT and link partner, the only performance requirement is that the channel (including the line tap) meets the link segment requirement of ISO/IEC/IEEE 8802-3:2021.

B.1.3 PCS – Test system set-up

Two test systems are required to perform all tests that are specified in this document. The ISO/IEC/IEEE 8802-3:2021 receive test system examines the transmissions from the IUT, and the ISO/IEC/IEEE 8802-3:2021 transmit test system transmits the necessary test patterns to test the receiver of the IUT. It is possible to combine both test systems into one set-up.

The ISO/IEC/IEEE 8802-3:2021 receive test system consists of an oscilloscope and software to capture and decode the transmissions from the IUT. The IUT connects to the test system through the line tap as specified in A.3. The software downloads the capture from the oscilloscope and decodes the ternary symbols, using knowledge of the ISO/IEC/IEEE 8802-3:2021 encoding, to create the MII data stream. The test set-up is shown in Figure B.1.

The MII station, line tap, and the oscilloscope are part of the LT.

The purpose of the MII station (Figure B.1 key 7) is to directly interact with the MII of the IUT (Figure B.1 key 5), manipulating the TX pins of the IUT MII (Figure B.1 key 6) to verify that the signals transmitted by the MII station of the LT are properly converted to PAM3 PHY frames transmitted by the IUT MDI via the SUT-Iface-0.

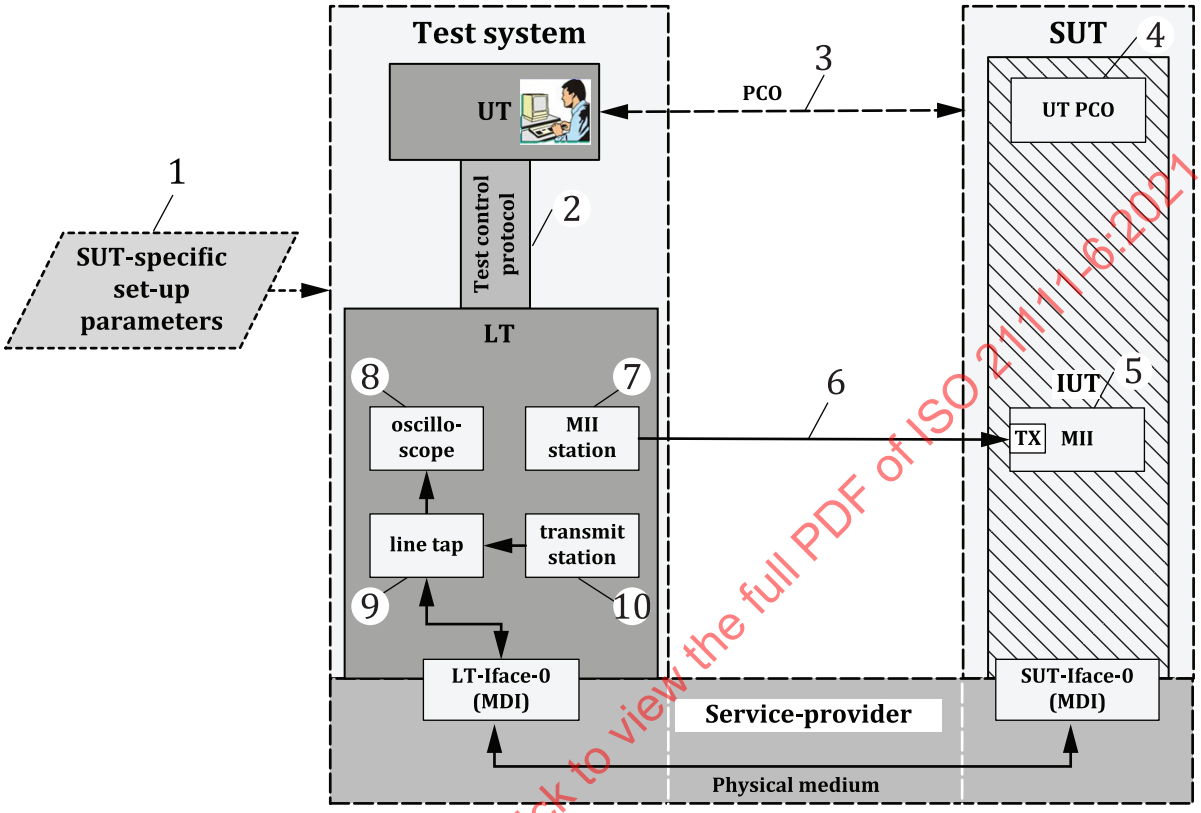
The MII station, transmit station, line tap and the oscilloscope are part of the LT.

The purpose of the transmit station (Figure B.1 key 10) is to act as a link partner with the IUT. The transmit station transmits ISO/IEC/IEEE 8802-3:2021 PAM3 encoding such that the IUT can achieve a link and receive ternary symbol sequences designed to stress the IUT implementation.

The purpose of the line tap (Figure B.1 key 9) is to allow directional monitoring of the signalling from the physical medium. The receive signal from the LT-Iface-0 is then captured on the oscilloscope (Figure B.1 key 8).

The purpose of the oscilloscope (Figure B.1 key 8) is to measure the PAM3 signalling transmitted by the IUT MDI, allowing for capture and decoding of the ISO/IEC/IEEE 8802-3:2021 ternary symbols.

The MII test system is mandatory for some tests, while it can be replaced with higher OSI layers or a loopback in some tests. Other solutions, such as an FPGA that can capture the ternary symbols, are possible.



Key

1 SUT-specific set-up parameters (node's electronic data sheet)
2 test control protocol
3 points of control and observation and abstract service primitives
4 UT PCO test system operator interface
5 IUT MII interface
6 manipulating the TX pins of the IUT MII interface
7 MII station
8 oscilloscope
9 line tap
10 transmit station

Figure B.1 — PCS – Receive test system set-up

The ISO/IEC/IEEE 8802-3:2021 transmit test system consists of software and hardware that is capable of transmitting arbitrary ternary symbols to the IUT. The ability to send arbitrary sequences, such as invalid transitions of the PCS transmit state machine, is essential to fully test the receiver of the IUT. The test set-up is shown in Figure B.2.

The MII station, transmit station, line tap and the oscilloscope are part of the LT.

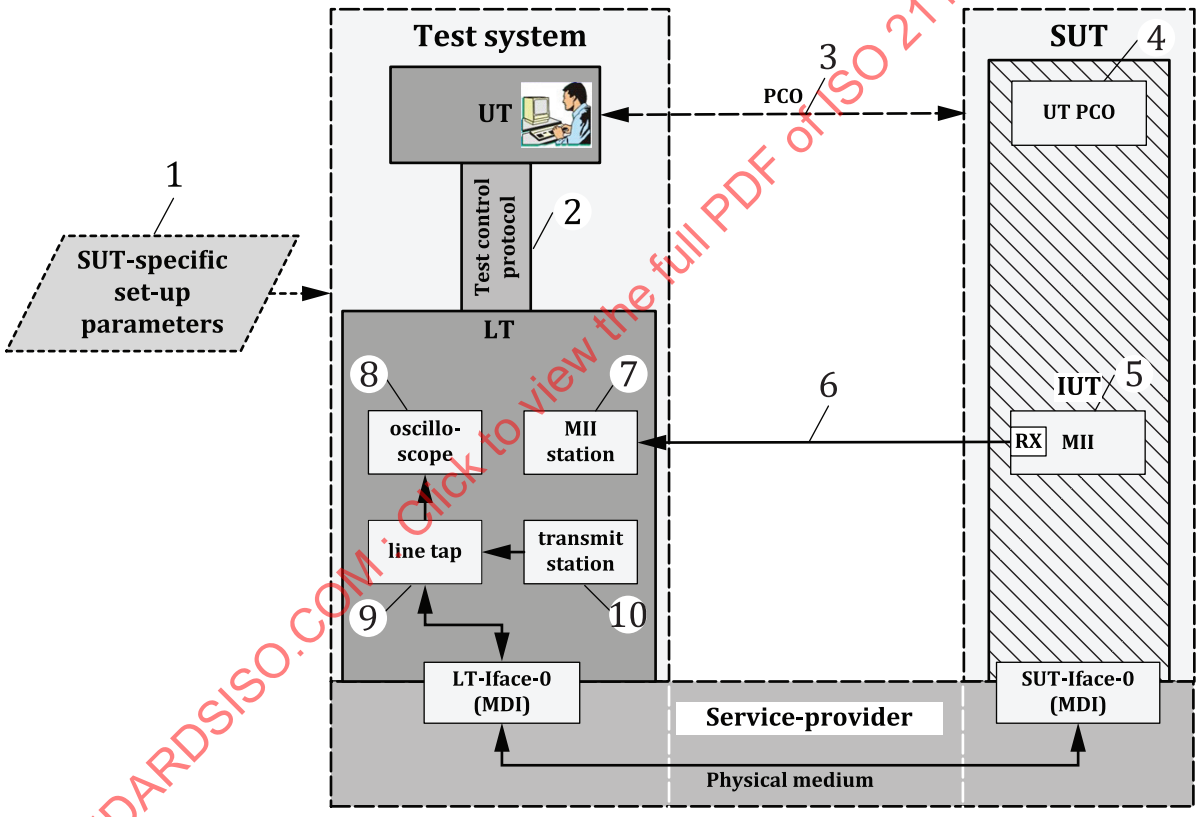
The purpose of the MII station (Figure B.2 key 7) is to directly interact with the MII of the IUT (Figure B.2 key 5), monitoring the RX pins of the IUT MII (Figure B.2 key 6) to verify that PHY frames received at the SUT-Iface-0 (MDI) are converted appropriately to bits recognizable by the MAC of the LT.

The purpose of the transmit station (Figure B.2 key 10) is to act as a link partner with the IUT. The transmit station transmits ISO/IEC/IEEE 8802-3:2021 PAM3 encoding such that the IUT can achieve a link and receive ternary symbol sequences designed to stress the IUT implementation.

The purpose of the line tap (Figure B.1 key 9) is to allow directional monitoring of the signalling from the physical medium. The receive signal from the LT-Iface-0 is then captured on the oscilloscope (Figure B.1 key 8).

The purpose of the oscilloscope (Figure B.1 key 8) is to measure the PAM3 signalling transmitted by the IUT MDI, allowing for capture and decoding of the ISO/IEC/IEEE 8802-3:2021 ternary symbols.

The MII test system is mandatory for some tests, while it can be replaced with higher OSI layers or a loopback in some tests.



Key

1 SUT-specific set-up parameters (node's electronic data sheet)
2 test control protocol
3 points of control and observation and abstract service primitives
4 UT PCO test system operator interface
5 IUT MII interface
6 monitoring of the RX pins of the IUT MII interface
7 MII station
8 oscilloscope
9 line tap
10 transmit station

Figure B.2 — PCS – Transmit test system set-up

B.2 PCS – Testing devices without MII access

B.2.1 PCS – Overview of CTCs that are possible without MII access

The number of CTCs that can be performed on a device without MII access is reduced. Typically, the only observation points are available packet counters or packets that are forwarded through another port on the IUT. The only transmissions available from the IUT are training, idle, and packets.

B.2.2 PCS – Group 1: PCS transmit CTCs that are possible without MII access

B.2.2.1 PCS – Group 1 overview

Table B.1 specifies the PCS transmit conformance tests that are possible without MII access.

Table B.1 — Group 1: PCS transmit CTCs that are possible without MII access

CTC # – Name	No modification required	Requires modification	Cannot be tested
CTC_3.1.1 – PCS signalling	all items of CTC	---	---
CTC_3.1.2 – PCS reset	all items of CTC	---	---
CTC_3.1.3 – PCS transmit proper `SSD`	all items of CTC	---	---
CTC_3.1.4 – PCS transmit proper `ESD`	all items of CTC	---	---
CTC_3.1.5 – PCS transmit `ESD` with `tx_error`	---	---	all items of CTC
CTC_3.1.6 – PCS transmission of stuff bits	all items of CTC	---	---
CTC_3.1.7 – PCS `tx_error`	---	---	all items of CTC

B.2.3 PCS – Group 2: PCS transmit state diagram CTCs that are possible without MII access

B.2.3.1 PCS – Group 2 overview

Table B.2 specifies the PCS transmit state diagram conformance tests that are possible without MII access.

Table B.2 — Group 2: PCS transmit state diagram CTCs that are possible without MII access

CTC # – Name	No modification required	Requires modification	Cannot be tested
CTC_3.2.1 – PCS transmit state diagram - `SEND IDLE` state	---	see Table B.3	---
CTC_3.2.2 – PCS transmit state diagram - `SSD1 VECTOR` and `SSD2 VECTOR` states	---	see Table B.4	---
CTC_3.2.3 – PCS transmit state diagram - `SSD3 VECTOR` state	---	see Table B.5	---
CTC_3.2.4 – PCS transmit state diagram - `TRANSMIT DATA` state	---	see Table B.6	---
CTC_3.2.5 – PCS transmit state diagram - `ESD1 VECTOR` state	---	see Table B.7	---
CTC_3.2.6 – PCS transmit state diagram - `ESD2 VECTOR` state	---	see Table B.8	---
CTC_3.2.7 – PCS transmit state diagram - `ESD3 VECTOR` state	---	see Table B.9	---
CTC_3.2.8 – PCS transmit state diagram - `ERR ESD1 VECTOR` state	---	---	all items of CTC

Table B.2 *(continued)*

CTC # – Name	No modification required	Requires modification	Cannot be tested
CTC_3.2.9 – PCS transmit state diagram - ERR ESD2 VECTOR state	---	---	all items of CTC
CTC_3.2.10 – PCS transmit state diagram - ERR ESD3 VECTOR state	---	---	all items of CTC

B.2.3.2 CTC_3.2.1 – PCS transmit state diagram (without MII access) - SEND IDLE state

Table B.3 specifies the CTC_3.2.1 - PCS transmit state diagram (without MII access) - SEND IDLE state.

Table B.3 — CTC_3.2.1 - PCS transmit state diagram (without MII access) - SEND IDLE state

Item	Content
CTC # – Name	CTC_3.2.1 – PCS transmit state diagram (without MII access) - SEND IDLE state
Purpose	This CTC verifies that the IUT behaves while in the SEND IDLE state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure B.2. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the transmit station and the monitor station.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link. 2. The LT shall instruct the IUT to transmit a valid packet. 3. The LT shall monitor the transmissions from the IUT.
Iteration	Not applicable
Expected response	After step 3: The IUT transmits valid SSD1.
Remark	Reduced test for SUT without MII access.

B.2.3.3 CTC_3.2.2 – PCS transmit state diagram (without MII access) - SSD1 VECTOR and SSD2 VECTOR states

Table B.4 specifies the CTC_3.2.2 - PCS transmit state diagram (without MII access) - SSD1 VECTOR and SSD2 VECTOR states.

Table B.4 — CTC_3.2.2 - PCS transmit state diagram (without MII access) - SSD1 VECTOR and SSD2 VECTOR states

Item	Content
CTC # – Name	CTC_3.2.2 – PCS transmit state diagram (without MII access) - SSD1 VECTOR and SSD2 VECTOR states
Purpose	This CTC verifies that the IUT behaves while in the SSD1 VECTOR and SSD2 VECTOR states.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram

Table B.4 *(continued)*

Item	Content
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure B.2. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the transmit station and the monitor station.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link. 2. The LT shall instruct the IUT to transmit a valid packet. 3. The LT shall monitor the transmissions from the IUT.
Iteration	Not applicable
Expected response	After step 3: The IUT transmits valid SSD1, SSD2, and SSD3.
Remark	Reduced test for SUT without MII access.

B.2.3.4 CTC_3.2.3 – PCS transmit state diagram (without MII access) - SSD3 VECTOR state

Table B.5 specifies the CTC_3.2.3 - PCS transmit state diagram (without MII access) - SSD3 VECTOR state.

Table B.5 — CTC_3.2.3 - PCS transmit state diagram (without MII access) - SSD3 VECTOR state

Item	Content
CTC # – Name	CTC_3.2.3 – PCS transmit state diagram (without MII access) - SSD3 VECTOR state
Purpose	This CTC verifies that the IUT behaves while in the SSD3 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure B.2. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the transmit station and the monitor station.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link. 2. The LT shall instruct the IUT to transmit a valid packet. 3. The LT shall monitor the transmissions from the IUT.
Iteration	Not applicable
Expected response	After step 3: The IUT transmits valid SSD3 and frame data.
Remark	Reduced test for SUT without MII access.

B.2.3.5 CTC_3.2.4 – PCS transmit state diagram (without MII access) - TRANSMIT DATA state

Table B.6 specifies the CTC_3.2.4 - PCS transmit state diagram (without MII access) - TRANSMIT DATA state.

Table B.6 — CTC_3.2.4 - PCS transmit state diagram (without MII access) - TRANSMIT DATA state

Item	Content
CTC # – Name	CTC_3.2.4 – PCS transmit state diagram (without MII access) - TRANSMIT DATA state
Purpose	This CTC verifies that the IUT behaves while in the TRANSMIT DATA state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure B.2. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the transmit station and the monitor station.
Step	1. The UT shall configure the LT and the link partner such that the IUT establishes a valid link. 2. The LT shall instruct the IUT to transmit a valid packet. 3. The LT shall monitor the transmissions from the IUT.
Iteration	Not applicable
Expected response	After step 3: The IUT transmits valid frame data and ESD.
Remark	Reduced test for SUT without MII access.

B.2.3.6 CTC_3.2.5 – PCS transmit state diagram (without MII access) - ESD1 VECTOR state

Table B.7 specifies the CTC_3.2.5 - PCS transmit state diagram (without MII access) - ESD1 VECTOR state.

Table B.7 — CTC_3.2.5 - PCS transmit state diagram (without MII access) - ESD1 VECTOR state

Item	Content
CTC # – Name	CTC_3.2.5 – PCS transmit state diagram (without MII access) - ESD1 VECTOR state
Purpose	This CTC verifies that the IUT behaves while in the ESD1 VECTOR state.
Reference	ISO/IEC/IEEE 8802-3:2021, Figure 96-7 – PCS transmit state diagram
Prerequisite	The test system shall be capable of capturing and decoding ternary symbols. The link partner shall follow ISO/IEC/IEEE 8802-3:2021. The LT's line tap shall allow the directional monitoring of the signalling to an oscilloscope. The IUT shall be capable of sending and receiving PHY frames.
Set-up	The test system set-up shall be in accordance with Figure B.2. The test system shall be parameterized in accordance with the SUT-specific set-up parameters (node's electronic data sheet). The UT shall connect the IUT to the transmit station and the monitor station.