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Road vehicles — In-vehicle Ethernet —

Part 3: Optical 1-Gbit/s physical entity requirements and conformance test plan

Véhicules routiers — Ethernet embarqué —

Partie 3: Exigences et plan d'essais de conformité de la couche physique optique à 1-Gbit/s

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT), see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21111 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The ISO 21111 series includes in-vehicle Ethernet requirements and test plans that are disseminated in other International Standards and complements them with additional test methods and requirements. The resulting requirement and test plans are structured in different documents following the Open Systems Interconnection (OSI) reference model and grouping the documents that depend on the physical media and bit rate used.

In general, the Ethernet requirements are specified in ISO/IEC/IEEE 8802-3. The ISO 21111 series provides supplemental specifications (e.g. wake-up, I/O functionality), which are required for in-vehicle Ethernet applications. In road vehicles, Ethernet networks are used for different purposes requiring different bit-rates. Currently, the ISO 21111 series specifies the 1-Gbit/s optical and 100-Mbit/s electrical physical layer.

The ISO 21111 series contains requirement specifications and test methods related to the in-vehicle Ethernet. This includes requirement specifications for physical layer entity (e.g. connectors, physical layer implementations) providers, device (e.g. electronic control units, gateway units) suppliers, and system (e.g. network systems) designers. Additionally, there are test methods specified for conformance testing and for interoperability testing.

Safety (electrical safety, protection, fire, etc.) and electromagnetic compatibility (EMC) requirements are out of the scope of the ISO 21111 series.

The structure of the specifications given in the ISO 21111 series complies with the Open Systems Interconnection (OSI) reference model specified in ISO/IEC 7498-1[1] and ISO/IEC 10731[5].

ISO 21111-1 defines the terms which are used in this series of standards and provides an overview of the standards for in-vehicle Ethernet including the complementary relations to ISO/IEC/IEEE 8802-3, the document structure, type of physical entities, in-vehicle Ethernet specific functionalities and so on.

ISO 21111-2 specifies the interface between reconciliation sublayer and physical entity including reduced gigabit media independent interface (RGMII), and the common physical entity wake-up and synchronized link sleep functionalities, independent from physical media and bit rate.

This document specifies supplemental requirements to a physical layer capable of transmitting 1-Gbit/s over plastic optical fibre compliant with ISO/IEC/IEEE 8802-3, with specific application to communications inside road vehicles, and a test plan for physical entity conformance testing.

ISO 21111-4 specifies the optical components requirements and test methods for 1-Gbit/s optical in-vehicle Ethernet.

ISO 21111-5 specifies, for 1-Gbit/s optical in-vehicle Ethernet, requirements on the physical layer at system level, requirements on the interoperability test set-ups, the interoperability test plan that checks the requirements for the physical layer at system level, requirements on the device-level physical layer conformance test set-ups, and device-level physical layer conformance test plan that checks a set of requirements for the OSI physical layer that are relevant for device vendors.

ISO 21111-6 specifies advanced features of an ISO/IEC/IEEE 8802-3 in-vehicle Ethernet physical layer (often also called transceiver), e.g. for diagnostic purposes for in-vehicle Ethernet physical layers. It specifies advanced physical layer features, wake-up and sleep features, physical layer test suite, physical layer control requirements and conformance test plan, physical sublayers test suite and physical sublayers requirements and conformance test plan.

ISO 21111-7 specifies the implementation for ISO/IEC/IEEE 8802-3:2017/Amd 1:2017, which defines the interface implementation for automotive applications together with requirements on components used to realize this Bus Interface Network (BIN). ISO 21111-7 also defines further testing and system requirements for systems implemented according to the system specification. In addition, ISO 21111-7 defines the channels for tests of transceivers with a test wiring harness that simulates various electrical communication channels.

ISO 21111-8 specifies the transmission media, the channel performance and the tests for ISO/IEC/IEEE 8802-3 in-vehicle Ethernet.

ISO 21111-9 specifies the data link layer requirements and conformance test plan. It specifies the requirements and test plan for devices and systems with bridge functionality.

ISO 21111-10 specifies the application to network layer requirements and test plan. It specifies the requirements and test plan for devices and systems that include functionality related with OSI layers from 3 to 7.

Figure 1 shows the parts of the ISO 21111 series and the document structure.

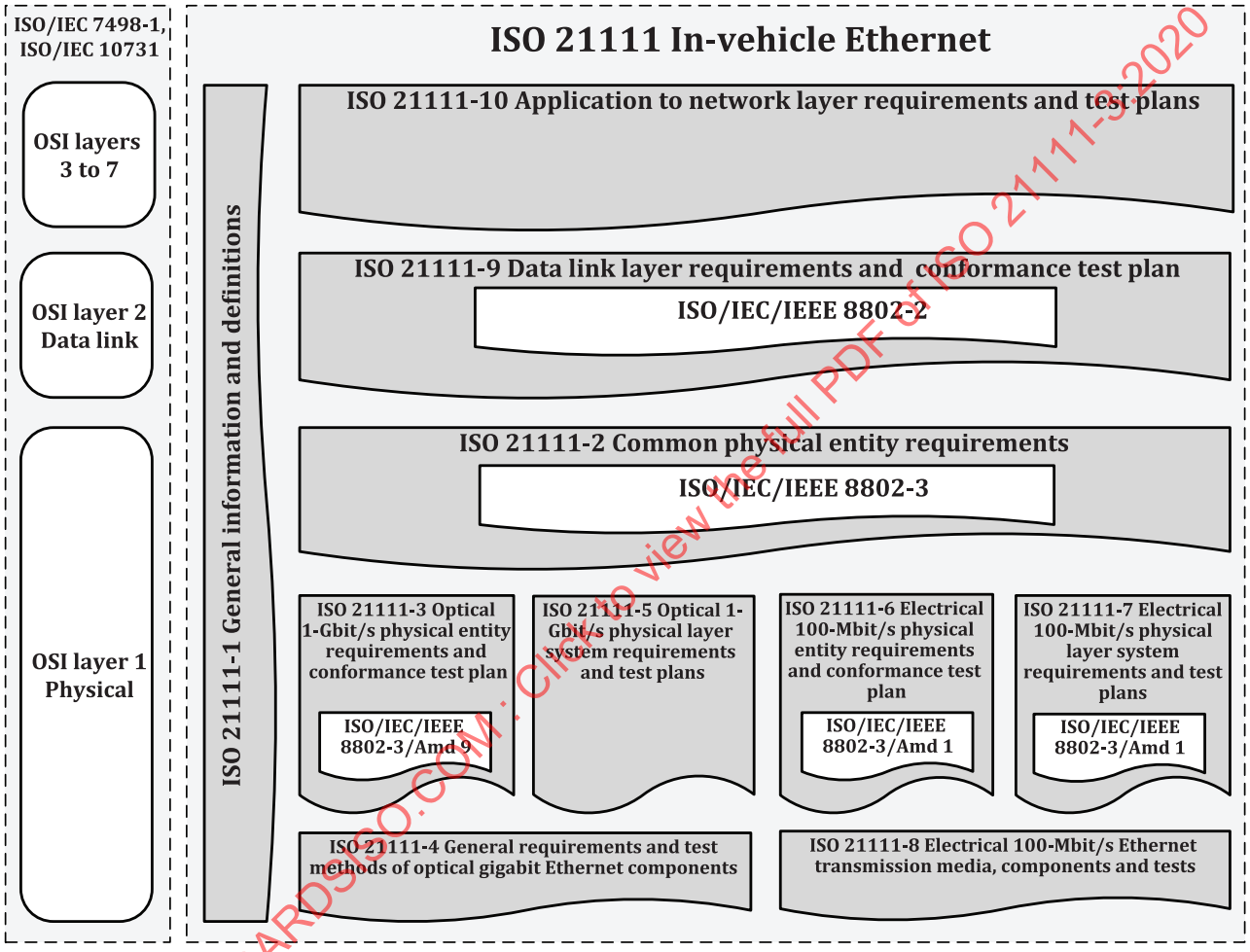


Figure 1 — In-vehicle Ethernet document reference according to the OSI model

Road vehicles — In-vehicle Ethernet —

Part 3: Optical 1-Gbit/s physical entity requirements and conformance test plan

1 Scope

This document provides supplemental specifications to a physical layer capable of transmitting 1 Gbit/s over plastic optical fibre compliant with ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, with specific application to communications inside road vehicles.

Additionally, there is a test plan specified for conformance testing. The test plan includes test cases to assure compliance of an IUT with the functionality specified in this document.

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 is considered indispensable for the application of this document.

The supplemental specifications include wake-up and synchronised link sleep functionality. The specification includes the sublayers, service interfaces, and state diagrams that support the functionality. The supplemental specifications are collected in protocol implementation conformance statement (PICS).

The requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 and in this document constitute the complete PICS that specifies the GEPOF physical entity functionality.

The optical component requirements and test methods for optical 1-Gbit/s transmission of in-vehicle Ethernet are not within the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21111-1[1], *Road vehicle — In-vehicle Ethernet — Part 1: General information and definitions*

ISO 21111-2:—[2], *Road vehicles — In-vehicle Ethernet — Part 2: Common medium-independent interface specifications*

ISO/IEC/IEEE 8802-3:2017, *Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements — Part 3: Standard for Ethernet*

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, *Physical layer specifications and management parameters for 1000 Mb/s operation over plastic optical fiber*

1) Under preparation. Stage at the time of publication: ISO/DIS 21111-1:2020.

2) Under preparation. Stage at the time of publication: ISO/DIS 21111-2:2020.

3 Terms and definitions

For the purposes of this document, the terms and definitions in ISO/IEC/IEEE 8802-3, ISO 21111-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1
neighbour GEPOF entities
two or more GEPOF entities embedded in the same device

3.2
GEPOF link partners
two GEPOF entities connected bi-directionally through POF

3.3
IEEE 802.3bv physical layer
physical layer compliant with 1000BASE-RHC

Note 1 to entry: 1000BASE-RHC is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 1.4.26c.

3.4
symbol
smallest unit of data transmission on the medium

Note 1 to entry: Symbols are specified in ISO/IEC/IEEE 8802-3:2017, 1.4.393 and in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.

3.5
transmit block
sequence of a fixed number of *symbols* (3.4) that encodes data from MAC layer and control information

Note 1 to entry: The transmit block is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.1.

3.6
transmit block generator
instrument that transmits and generates a *transmit block* (3.5) with controlled content

3.7
transmit block analyser
instrument that receives a *transmit block* (3.5) and processes the information contained in it

3.8
payload data sub-block
part of a *transmit block* (3.5) that encodes data from MAC layer

Note 1 to entry: The payload data sub-block is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.1.

4 Abbreviated terms

ACK	acknowledgement
AOP	average optical power
BCH	Bose, Ray-Chaudhuri, Hocquenghem
BER	bit error rate

CID	company identifier
CRC	cyclic check redundancy
EEE	energy-efficient Ethernet
ER	extinction ratio
FFME	fast forward management entity
GEPOF	gigabit Ethernet over plastic optical fibre
GMII	gigabit media independent interface
IUT	implementation under test
LPI	low power idle
LSB	least significant bit
LT	lower tester
MAC	medium access control
MDI	medium dependent interface
MDIO	management data input/output
MSB	most significant bit
OAM	operations, administration, and maintenance
OAMPDU	OAM protocol data unit
PCS	physical coding sublayer
PHD	physical header data
PHS	physical header sub-frame
PICS	protocol implementation conformance statement
PMA	physical medium attachment
PMD	physical medium dependent
POF	plastic optical fibre
RIN	reference input noise
RX	receiver
TX	transmitter
UT	upper tester
WUSME	wake-up and synchronised link sleep management entity

5 Wake-up and synchronised link sleep functionality

5.1 General

Figure 2 shows the functional block diagram of the GEPOF entity.

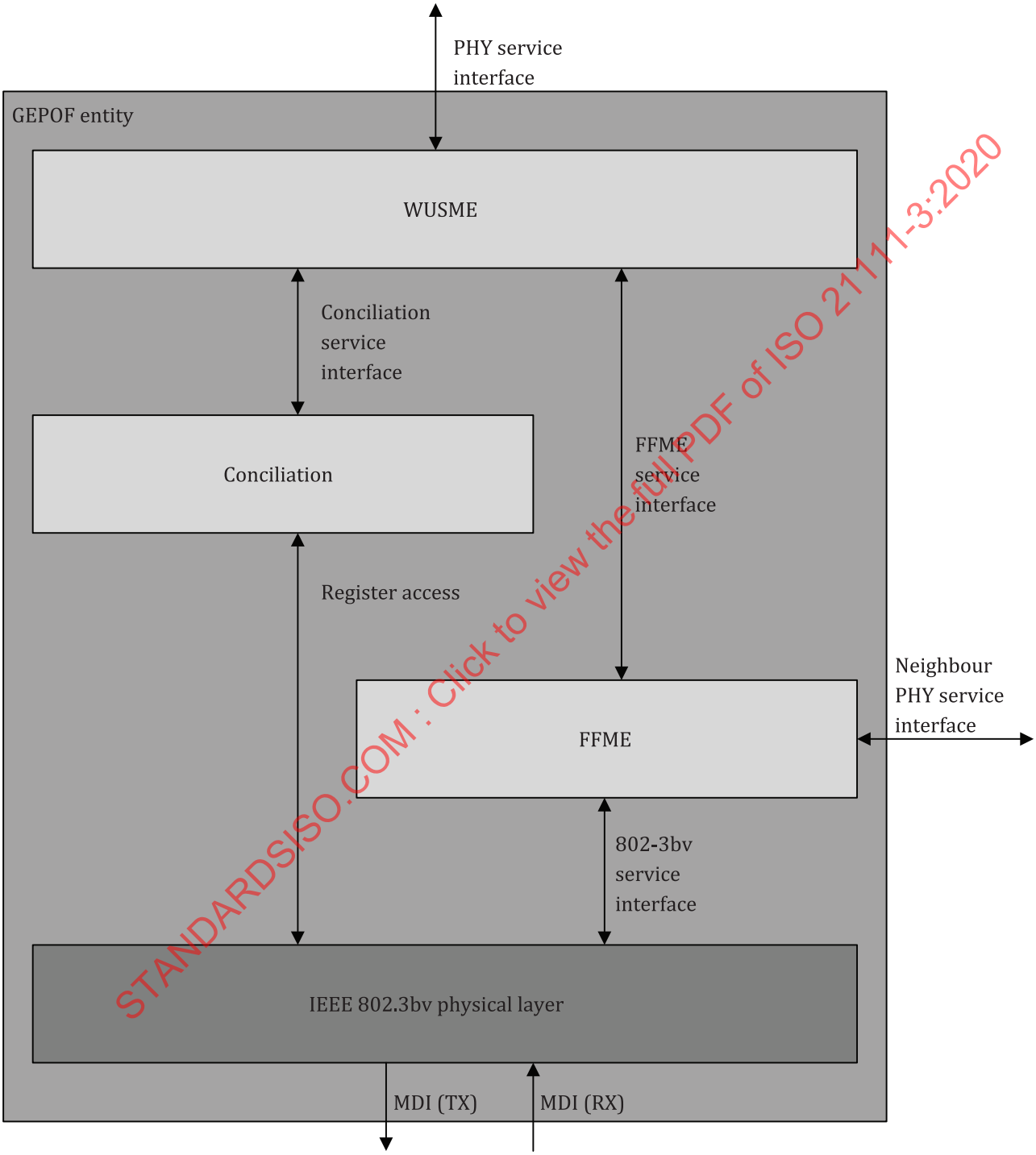


Figure 2 — GEPOF entity functional block diagram

WUSME sublayer shall communicate with the MAC layer over the PHY service interface specified in 5.2 and in ISO 21111-2:—, 6.8.

WUSME sublayer shall contain wake-up and synchronised link sleep algorithms as specified in ISO 21111-2:—, 6.4 and 6.5. This specification includes exchange of events that shall be encoded by using message exchange over the 1000BASE-H OAM channel specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.9 and the state diagrams specified in 5.7.

WUSME sublayer shall communicate with the conciliation sublayer over the conciliation service interface specified in 5.2.

WUSME sublayer shall communicate with FFME sublayer over the FFME service interface specified in 5.5.

FFME sublayer shall behave as the state diagram that controls the power state of the GEPOF entity specified in 5.8 and ISO 21111-2:—, 6.2.

FFME shall communicate with another FFME located inside neighbour GEPOF entity over the neighbour PHY service interface specified in 5.3 and in ISO 21111-2:—, 6.9.

FFME shall communicate with the IEEE 802.3bv physical layer over the 802-3bv service interface specified in 5.6.

The conciliation sublayer shall include the functions described in 5.9 that translate each of the conciliation service primitives into transactions over MDIO registers.

Bit naming and MDIO register numbering are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45. CID is specified in ISO/IEC/IEEE 8802-A:2015, 1.4.162.

The high logic level and low logic level for the MDIO registers are specified in ISO/IEC/IEEE 8802-3:2017, 22.4.

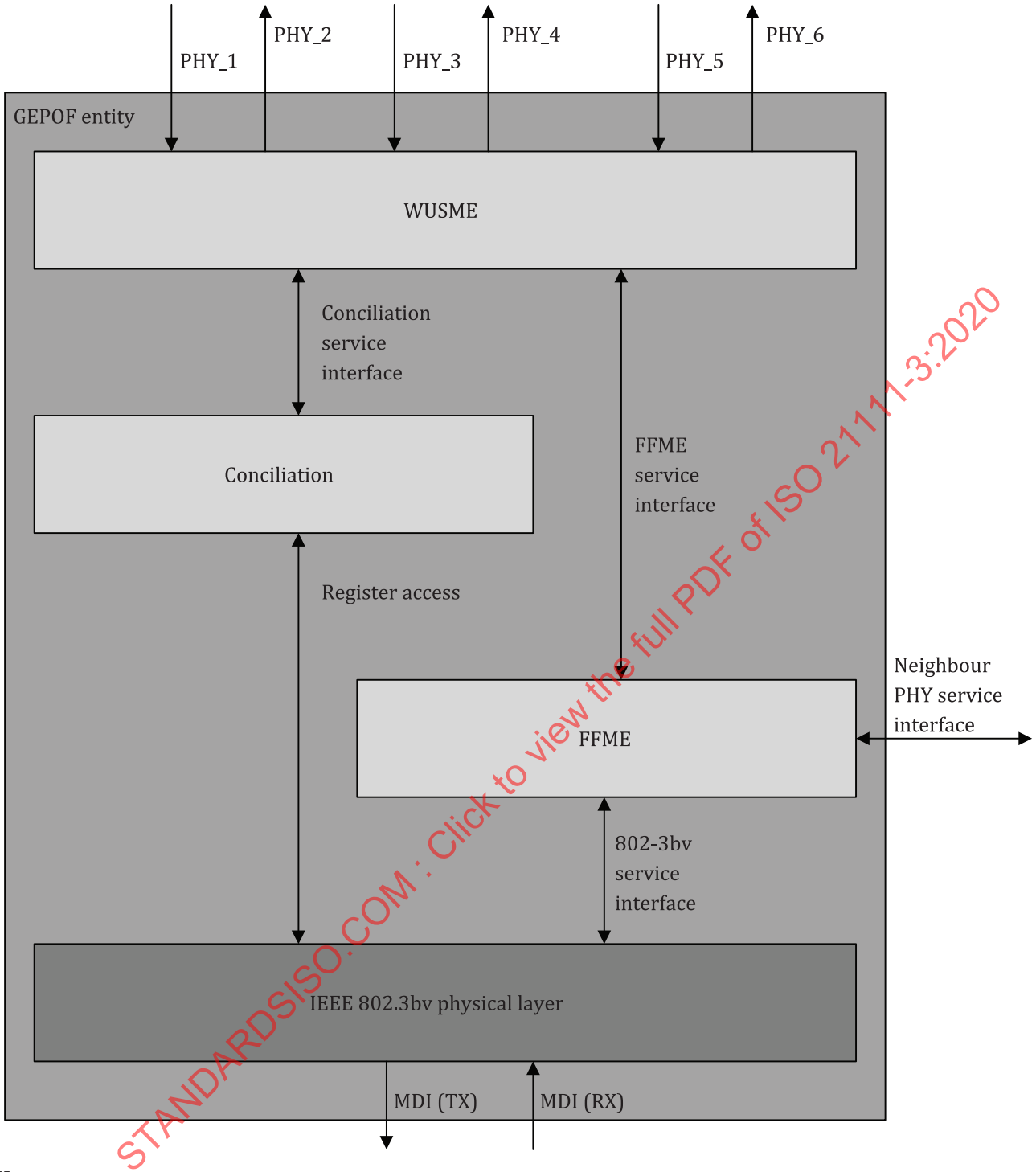
The value of the service primitive parameters follows a positive logic. TRUE corresponds to a high logic level and FALSE corresponds to a low logic level.

State diagrams in this document follow the notation specified in ISO/IEC/IEEE 8802-3:2017, 1.2.

5.2 PHY service interface for a GEPOF entity

The following specifies the mandatory service primitives of the PHY service interface as given in ISO 21111-2 that are required by a GEPOF entity.

Figure 3 shows the service primitives of the PHY service interface and the relationship with the GEPOF entity sublayers.



Key

PHY service interface

PHY_1: PHY_LinkSleep.request
PHY_2: PHY_LinkSleep.indication
PHY_3: PHY_WakeUp.request
PHY_4: PHY_WakeUp.indication
PHY_5: PHY_ConfigSleepReject.request
PHY_6: PHY_SleepStatus.indication

Figure 3 — PHY service interface

The PHY service interface comprises the following service primitives:

— PHY_LinkSleep.request (see ISO 21111-2:—, 6.8.1);

— PHY_LinkSleep.indication (see ISO 21111-2:—, 6.8.2);

— PHY_WakeUp.request (see ISO 21111-2:—, 6.8.3);

— PHY_WakeUp.indication (see ISO 21111-2:—, 6.8.4);

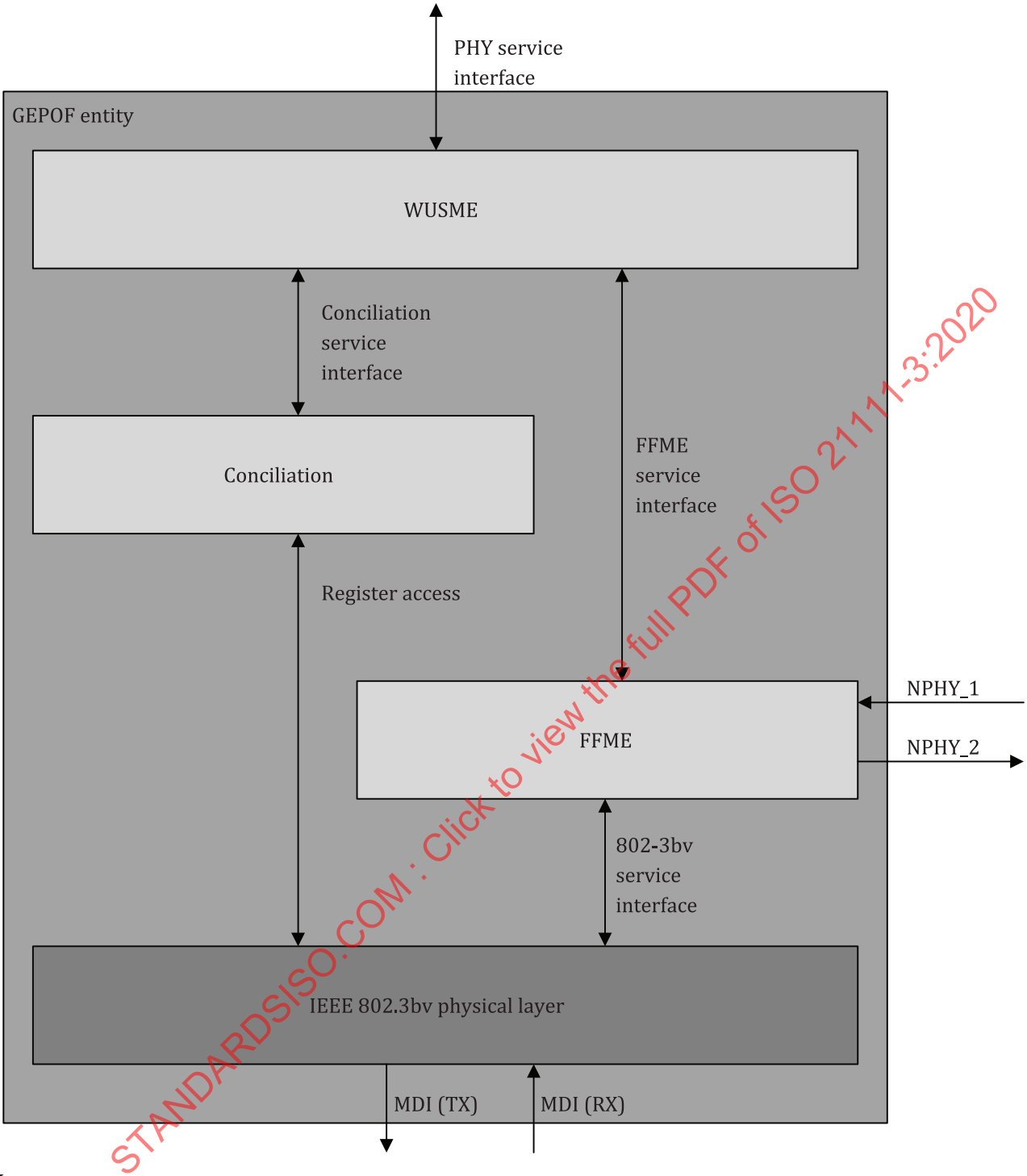
— PHY_ConfigSleepReject.request (see ISO 21111-2:—, 6.8.5);

— PHY_SleepStatus.indication (see ISO 21111-2:—, 6.8.6).

5.3 Neighbour PHY service interface for a GEPOF entity

The following specifies the mandatory service primitives of the neighbour PHY service interface as given in ISO 21111-2 that are required by a GEPOF entity.

Figure 4 shows the service primitives of the neighbour PHY service interface and the relationship with the GEPOF entity sublayers.



Key

Neigbour PHY service interface

NPHY_1: PHY_WakeUpForward.request

NPHY_2: PHY_WakeUpForward.indication

Figure 4 — Neighbour PHY service interface

The neighbour PHY service interface comprises the following service primitives:

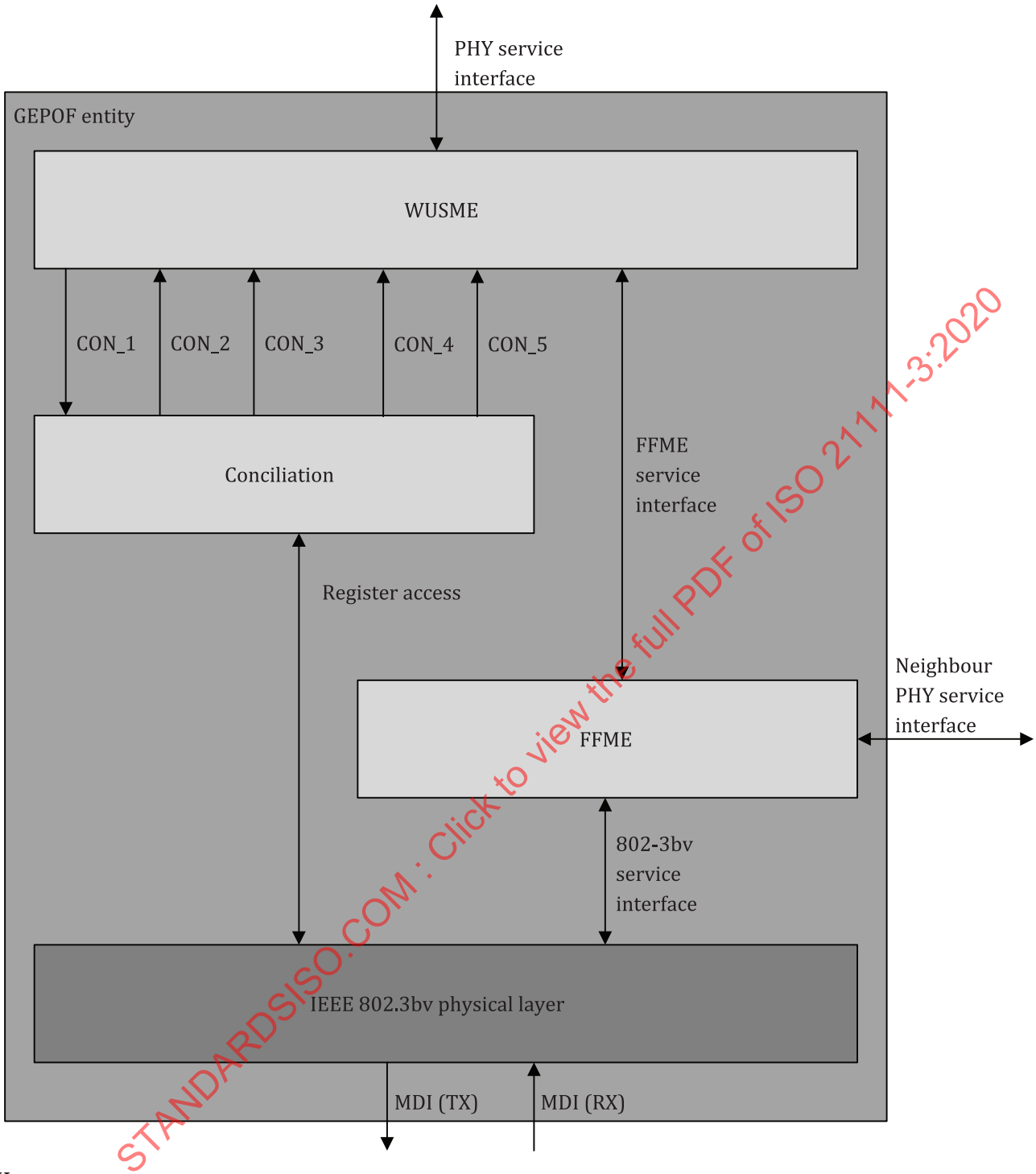
— NPHY_WakeUpForward.request (see ISO 21111-2:— , 6.9.1);

— NPHY_WakeUpForward.indication (see ISO 21111-2:— , 6.9.2).

5.4 Conciliation service interface

5.4.1 General

The following specifies the service primitives provided by the conciliation sublayer to the WUSME sublayer. Figure 5 shows the service primitives of the conciliation service interface and the relationship with the GEPOF entity sublayers.



Key

Conciliation service interface

CON_1: CON_WakeUpSleepPacket.request
CON_2: CON_WakeUpSleepPacket.indication
CON_3: CON_WakeUpSleepPacketACK.indication
CON_4: CON_SignalDetected.indication
CON_5: CON_OAMActive.indication

Figure 5 — Conciliation service interface

The conciliation service interface comprises the following service primitives:

— CON_WakeUpSleepPacket.request (see 5.4.2);

— CON_WakeUpSleepPacket.indication (see 5.4.3);

— CON_WakeUpSleepPacketACK.indication (see 5.4.4);

— CON_SignalDetected.indication (see 5.4.5);

— CON_OAMActive.indication (see 5.4.6).

5.4.2 CON_WakeUpSleepPacket.request

This service primitive is used to request to send a synchronised link sleep or wake-up event as specified in ISO 21111-2.

Table 1 specifies CON_WakeUpSleepPacket.request.

Table 1 — Specification of CON_WakeUpSleepPacket.request

Item	Description
Semantic	CON_WakeUpSleepPacket.request(c45_wu_sleep_pkt)
Parameters	The c45_wu_sleep_pkt parameter shall have one of the following values: — SLEEP; — SLEEP_ACK; — NO_SLEEP; — WAKE_UP.
Generation	CON_WakeUpSleepPacket.request shall be generated when the wu_sleep_pkt (see Table 10) variable is assigned to a value in the state diagram of Figure 8 or Figure 9. The value of the wu_sleep_pkt variable shall be copied to the c45_wu_sleep_pkt parameter.
Effect of receipt	A sequence of transactions over the IEEE 802.3bv physical layer registers depending on the c45_wu_sleep_pkt value shall be performed as described in 5.9.4.

5.4.3 CON_WakeUpSleepPacket.indication

This service primitive is used to indicate the reception of a synchronised link sleep or wake-up event as specified in ISO 21111-2.

Table 2 specifies CON_WakeUpSleepPacket.indication.

Table 2 — Specification of CON_WakeUpSleepPacket.indication

Item	Description
Semantic	CON_WakeUpSleepPacket.indication(wu_sleep_pkt_remote)
Parameters	The wu_sleep_pkt_remote parameter shall have one of the following values: — SLEEP; — SLEEP_ACK; — NO_SLEEP; — WAKE_UP.
Generation	CON_WakeUpSleepPacket.indication shall be generated when the conciliation sublayer receives a synchronised link sleep or wake-up packet (see 5.9.5).

Table 2 *(continued)*

Item	Description
Effect of receipt	The parameter wu_sleep_pkt_remote shall be copied to the WUSME variable wu_sleep_pkt_ind (see Table 10).

5.4.4 CON_WakeUpSleepPacketACK.indication

This service primitive is used to indicate the reception of an ACK of a previously sent synchronised link sleep or wake-up event from the IEEE 802.3bv physical layer.

Table 3 specifies CON_WakeUpSleepPacketACK.indication.

Table 3 — Specification of CON_WakeUpSleepPacketACK.indication

Item	Description
Semantic	CON_WakeUpSleepPacketACK.indication (void)
Parameters	None
Generation	CON_WakeUpSleepPacketACK.indication shall be generated when the transmission of a synchronised link sleep or wake-up event is acknowledged (see 5.9.6).
Effect of receipt	The variable wu_sleep_ack_ind (see Table 10) of WUSME sublayer (see 5.7.3.1) shall be set to TRUE.

5.4.5 CON_SignalDetected.indication

This service primitive is used to indicate the change in the content of the MDIO register 1.10.0 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-18.

Table 4 specifies CON_SignalDetected.indication.

Table 4 — Specification of CON_SignalDetected.indication

Item	Description
Semantic	CON_SignalDetected.indication (signal_detect_reg)
Parameters	The signal_detect_reg parameter shall have one of the following values: — TRUE: the MDIO register 1.10.0 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-18 of the IEEE 802.3bv physical layer is set to 1_2; — FALSE: the MDIO register 1.10.0 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-18 of the IEEE 802.3bv physical layer is set to 0_2.
Generation	CON_SignalDetected.indication shall be generated by the conciliation sublayer when the MDIO register 1.10.0 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-18 of the IEEE 802.3bv physical layer changes its value.
Effect of receipt	The parameter signal_detect_reg shall be copied to the WUSME variable signal_detect_reg (see Table 11).

5.4.6 CON_OAMActive.indication

This service primitive is used to indicate the change in the content of the MDIO register 3.519.13 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47d.3 when the MDIO register 3.518.1 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47c.3 is set to 1_2.

Table 5 specifies CON_OAMActive.indication.

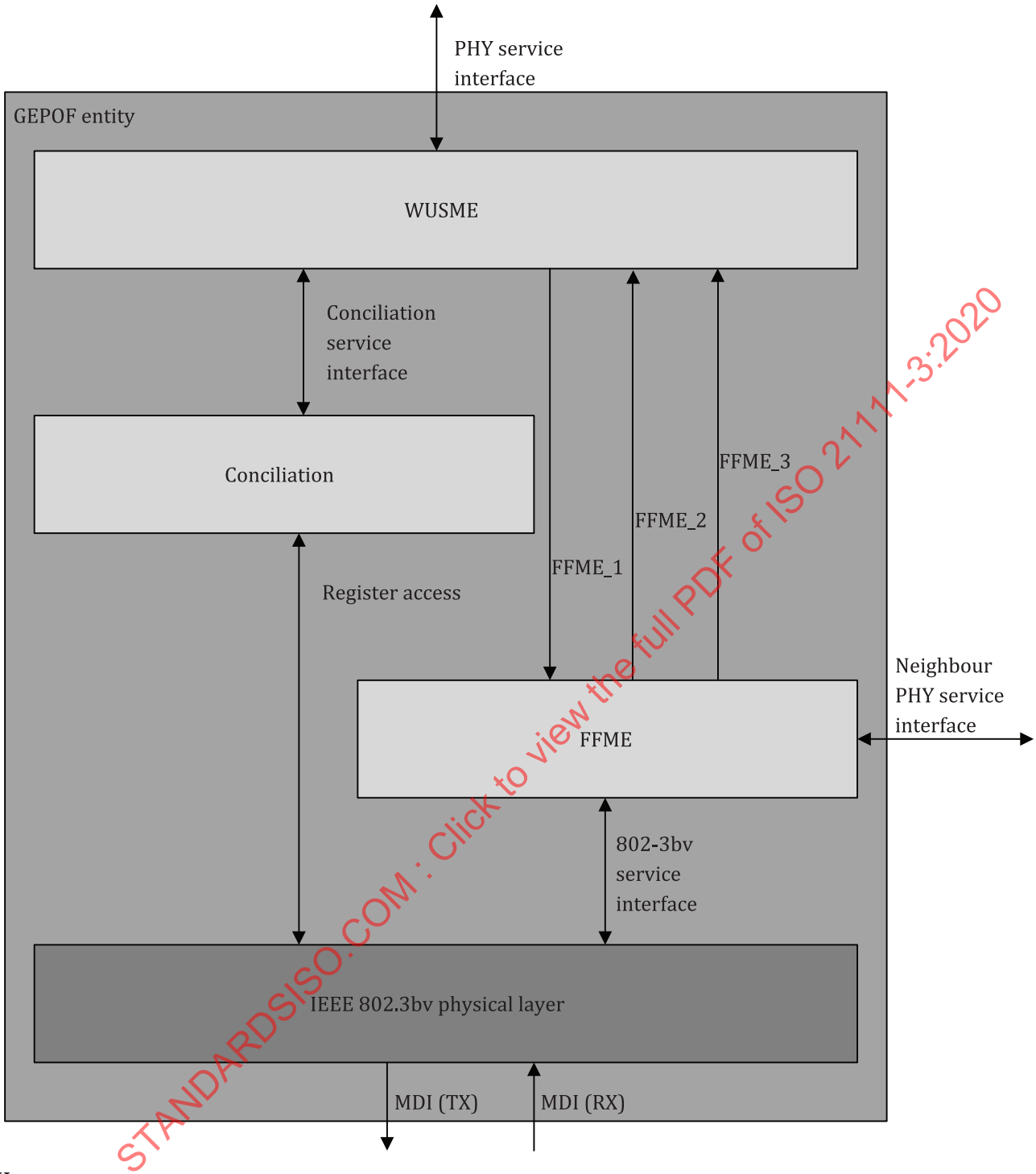
Table 5 — Specification of CON_OAMActive.indication

Item	Description
Semantic	CON_OAMActive.indication (oam_ch_active)
Parameters	The oam_ch_active parameter shall have one of the following values: — TRUE: the MDIO registers 3.518.1, 3.519.1, 3.519.3 and 3.519.10 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47c.3 and 45.2.3.47d are set to 1_2; — FALSE: any of the MDIO registers 3.518.1, 3.519.1, 3.519.3 and 3.519.10 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47c.3 and 45.2.3.47d is set to 0_2.
Generation	CON_OAMActive.indication shall be generated by the conciliation sublayer when the content of the MDIO register 3.519.10 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47d.6 changes its value and the MDIO register 3.518.1 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47c.3 is set to 1_2.
Effect of receipt	The parameter oam_ch_active shall be copied to the WUSME variable oam_ch_active (see Table 10).

5.5 FFME service interface

5.5.1 General

The following subclauses specify the service primitives provided by the FFME sublayer connected to the WUSME. Figure 6 shows the service primitives of the FFME service interface and the relationship with the GEPOF entity sublayers.



Key

FFME service interface

FFME_1: FFME_PowerDownStatus.request

FFME_2: FFME_PowerDownStatus.indication

FFME_3: FFME_WakeUp.indication

Figure 6 — FFME service interface

The FFME service interface comprises the following service primitives:

— FFME_PowerDownStatus.request (see 5.5.2);

— FFME_PowerDownStatus.indication (see 5.5.3);

— FFME_WakeUp.indication (see 5.5.4).

5.5.2 FFME_PowerDownStatus.request

This service primitive is used to request to the IEEE 802.3bv physical layer to enter or to leave the power-down state as specified in ISO/IEC/IEEE 8802-3:2017, 22.2.4.1.5.

Table 6 specifies FFME_PowerDownStatus.request.

Table 6 — Specification of FFME_PowerDownStatus.request

Item	Description
Semantic	FFME_PowerDownStatus.request (ffme_pd_status)
Parameters	The ffme_pd_status parameter shall have one of the following values: — TRUE: the WUSME sublayer requests to the IEEE 802.3bv physical layer to enter into the power-down state; — FALSE: the WUSME sublayer requests to the IEEE 802.3bv physical layer to leave the power-down state.
Generation	FFME_PowerDownStatus.request shall be generated when set_phy_pd_status (see Table 11) variable is assigned to a value as performed, for example in state diagram of Figure 9. The value of the set_phy_pd_status variable shall be copied to the ffme_pd_status parameter.
Effect of receipt	A transition in the FFME state diagram may be performed as described in Figure 10.

5.5.3 FFME_PowerDownStatus.indication

This service primitive is used to indicate if the FFME state diagram is in the Normal power state or not.

Table 7 specifies FFME_PowerDownStatus.indication.

Table 7 — Specification of FFME_PowerDownStatus.indication

Item	Description
Semantic	FFME_PowerDownStatus.indication (pd_status)
Parameters	The pd_status parameter shall have one of the two values: — TRUE: the FFME state diagram is not in the Normal power state; — FALSE: the FFME state diagram is in the Normal power state.
Generation	FFME_PowerDownStatus.indication shall be generated when a transition occurs from or to the Normal power state in the FFME state diagram (see Figure 10). The value of the pd_status variable (see Table 13) of the state diagram shall be copied to the pd_status parameter.
Effect of receipt	A transition in one of the WUSME state diagrams may be performed as specified in Figure 8 or Figure 9.

5.5.4 FFME_WakeUp.indication

This service primitive is used to indicate an assignation to TRUE of the ffme_wu_ind_gen variable of the FFME power state diagram (see Figure 10).

Table 8 specifies FFME_WakeUp.indication.

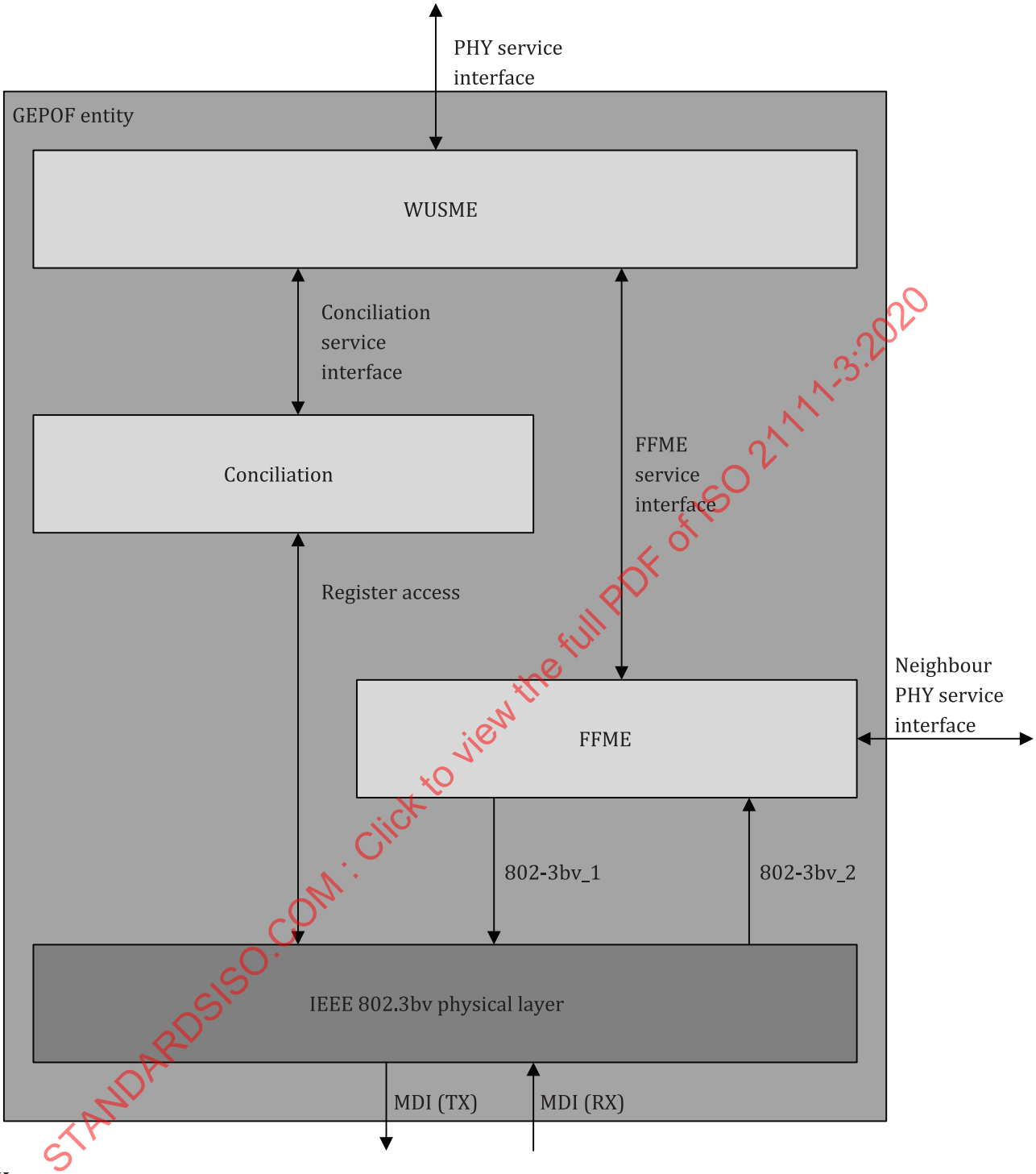
Table 8 — Specification of FFME_WakeUp.indication

Item	Description
Semantic	FFME_WakeUp.indication (void)
Parameters	None
Generation	FFME_WakeUp.indication shall be generated when ffme_wu_ind_gen variable is assigned to a TRUE value in the FFME state diagram (see Figure 10).
Effect of receipt	A transition in one of the WUSME state diagrams may be performed as specified in Figure 8 or Figure 9.

5.6 802-3bv service interface

5.6.1 General

The following specifies the service primitives provided by the IEEE 802.3bv physical layer and used by the FFME sublayer. Figure 7 shows the service primitives of the 802-3bv service interface and the relationship with the GEPOF entity sublayers.



Key

802-3bv service interface

802-3bv_1: 802-3bv_PowerDownStatus.request

802-3bv_2: 802-3bv_RXDETECT.indication

Figure 7 — 802-3bv service interface

The 802-3bv service interface comprises the following service primitives:

— 802-3bv_PowerDownStatus.request (see 5.6.2);

— 802-3bv_RXDETECT.indication (see 5.6.3).

5.6.2 802-3bv_PowerDownStatus.request

This service primitive is used to request a write operation in the MDIO register 1.0.11 specified in ISO/IEC/IEEE 8802-3:2017, 45.2.1.1.2 with the value defined by its parameter 802-3bv_pd_status.

Table 9 specifies 802-3bv_PowerDownStatus.request.

Table 9 — Specification of 802-3bv_PowerDownStatus.request

Item	Description
Semantic	802-3bv_PowerDownStatus.request (802-3bv_pd_status)
Parameters	The 802-3bv_pd_status parameter shall have one of the following values: — TRUE: the value to be written into the MDIO register 1.0.11 specified in ISO/IEC/IEEE 8802-3:2017, 45.2.1.1.2 is equal to 1_2; — FALSE: the value to be written into the MDIO register 1.0.11 specified in ISO/IEC/IEEE 8802-3:2017, 45.2.1.1.2 is equal to 0_2.
Generation	802-3bv_PowerDownStatus.request shall be generated when pd_status variable (see Table 13) is assigned to a value in the FFME state diagram (see Figure 10). The value of the pd_status variable shall be copied to the 802-3bv_pd_status.
Effect of receipt	A write operation in the MDIO register 1.0.11 specified in ISO/IEC/IEEE 8802-3:2017, 45.2.1.1.2 of the IEEE 802.3bv physical layer shall be performed with the value specified in the 802-3bv_pd_status parameter.

5.6.3 802-3bv_RXDETECT.indication

This service primitive is the same as PMD_RXDETECT.indication specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.1.5.

5.7 WUSME Sublayer

5.7.1 General

WUSME sublayer shall transit between the states shown in the state diagram specified in 5.7.2.2 and 5.7.3.2.

WUSME sublayer shall generate the PHY_SleepStatus.indication service primitive as specified in 5.7.4.

5.7.2 WUSME wake-up functionality

The WUSME wake-up functionality shall perform the event exchange between the GEPOF entity and its link partner for the wake-up algorithm specified in ISO 21111-2.

The WUSME wake-up functionality shall comply with the state diagram of Figure 8, and the associate state diagram variables specified in 5.7.2.1.

5.7.2.1 WUSME wake-up state diagram variables

Table 10 specifies the WUSME wake-up state diagram variables.

Table 10 — WUSME wake-up state diagram variables

Variable	Associated action	Value	Specification
wu_req	This variable reports the reception of a PHY_WakeUp.request service primitive (see ISO 21111-2:—, 6.8.3).	TRUE	A PHY_WakeUp.request is received and the wu_req variable shall be set to TRUE.
		FALSE	A PHY_WakeUp.request is not received and the wu_req variable shall be set to FALSE.
wu_ind	When this variable is assigned to TRUE, the WUSME sublayer generates a PHY_WakeUp.indication service primitive (see ISO 21111-2:—, 6.8.4).	TRUE	A PHY_WakeUp.indication shall be generated.
		FALSE	A PHY_WakeUp.indication shall not be generated.
wu_sleep_pkt	When this variable is assigned to a value, such value is copied into the parameter c45_wu_sleep_pkt of CON_WakeUpSleepPacket.request and the WUSME sublayer generates a CON_WakeUpSleepPacket.request service primitive (see 5.4.2).	SLEEP	The packet specified in the synchronised link sleep algorithm requested to be sent shall be of type SLEEP.
		SLEEP_ACK	The packet specified in the synchronised link sleep algorithm requested to be sent shall be of type SLEEP_ACK.
		NO_SLEEP	The packet specified in the synchronised link sleep algorithm requested to be sent shall be of type NO_SLEEP.
		WAKE_UP	The packet specified in the synchronised link sleep algorithm requested to be sent shall be of type WAKE_UP.
wu_sleep_ack_ind	This variable reports the reception of a CON_WakeUpSleepPacketACK.indication service primitive (see 5.4.4).	TRUE	A CON_WakeUpSleepPacketACK.indication is received and the variable WU_sleep_ack_ind shall be set to TRUE.
		FALSE	A CON_WakeUpSleepPacketACK.indication is not received and the variable wu_sleep_ack_ind shall be set to FALSE.
ffme_wu_ind	This variable reports the reception and presence of an FFME_WakeUp.indication service primitive (see 5.5.4).	TRUE	A FFME_WakeUp.indication is received and and the variable ffme_wu_ind shall be set to TRUE.
		FALSE	A FFME_WakeUp.indication is not received and the variable ffme_wu_ind shall be set to FALSE.
oam_ch_active	This variable stores the value of the oam_ch_active parameter of the last received CON_OAMActive.indication service primitive (see 5.4.6).	TRUE	The value of the oam_ch_active parameter of the last received CON_OAMActive.indication service primitive is TRUE and the variable oam_ch_active shall be set to TRUE.
		FALSE	The value of the oam_ch_active parameter of the last received CON_OAMActive.indication service primitive is FALSE and the variable oam_ch_active shall be set to FALSE.

Table 10 *(continued)*

Variable	Associated action	Value	Specification
wu_sleep_pkt_ind	This variable reports the value of the parameter wu_sleep_pkt_remote of a received CON_WakeUpSleepPacket.indication service primitive. Otherwise, the variable is set to FALSE (see 5.4.3).	SLEEP	A CON_WakeUpSleepPacket.indication service primitive is received and the parameter wu_sleep_pkt_remote is equal to SLEEP. Then the variable wu_sleep_pkt_ind shall be set to SLEEP.
		SLEEP_ACK	A CON_WakeUpSleepPacket.indication service primitive is received and the parameter wu_sleep_pkt_remote is equal to SLEEP_ACK. Then the variable wu_sleep_pkt_ind shall be set to SLEEP_ACK.
		NO_SLEEP	A CON_WakeUpSleepPacket.indication service primitive is received and the parameter wu_sleep_pkt_remote is equal to NO_SLEEP. Then the variable wu_sleep_pkt_ind shall be set to NO_SLEEP.
		WAKE_UP	A CON_WakeUpSleepPacket.indication service primitive is received and the parameter wu_sleep_pkt_remote is equal to WAKE_UP. Then the variable wu_sleep_pkt_ind shall be set to WAKE_UP.
		FALSE	A CON_WakeUpSleepPacket.indication service primitive is not received.

5.7.2.2 WUSME wake-up state diagram

WUSME wake-up functionality shall comply with the WUSME wake-up state diagram in Figure 8.

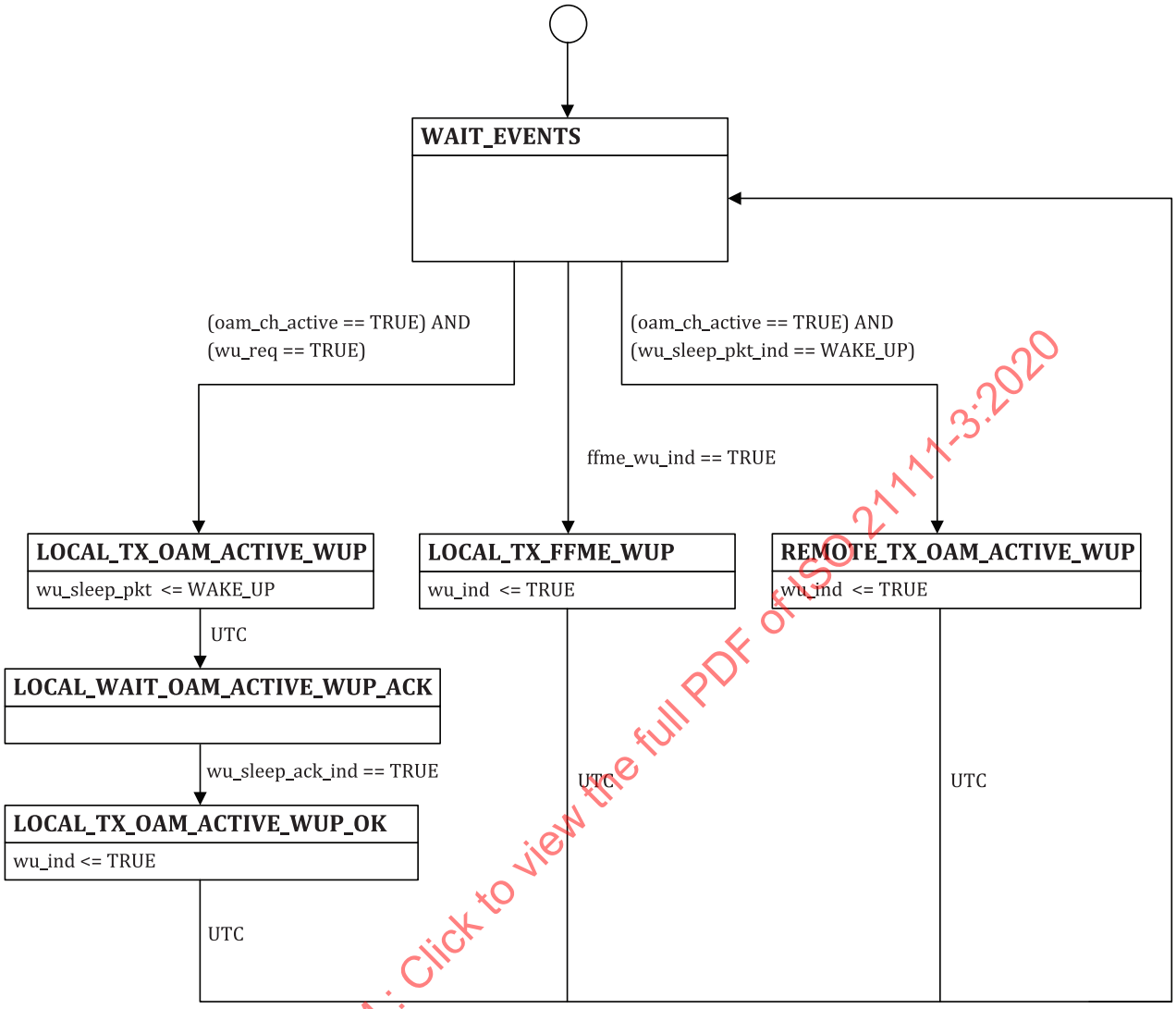


Figure 8 — WUSME wake-up state diagram

5.7.3 WUSME synchronised link sleep functionality

The WUSME synchronised link sleep functionality shall perform the event exchange between the GEPOF entity and its link partner for the synchronised link sleep algorithm specified in ISO 21111-2:—, 6.4.

The WUSME synchronised link sleep functionality shall comply with the synchronised link sleep state diagram in Figure 9, and the associate state diagram variables specified in 5.7.3.1.

5.7.3.1 WUSME synchronised link sleep state diagram variables

Table 11 specifies the WUSME synchronised link sleep state diagram variables not already specified in Table 10.

Table 11 — WUSME synchronised link sleep state diagram variables

Variable	Associated action	Value	Specification
sleep_reject	This variable stores the value of the mng_sleep_reject parameter of the last received PHY_ConfigSleepReject.request service primitive (see ISO 21111-2:—, 6.8.5).	TRUE	The value of the mng_sleep_reject parameter of the last received PHY_ConfigSleepReject.request service primitive is TRUE. Then the variable sleep_reject shall be set to TRUE.
		FALSE	The value of the mng_sleep_reject parameter of the last received PHY_ConfigSleepReject.request service primitive is FALSE. Then the variable sleep_reject shall be set to FALSE.
set_phy_pd_status	When this variable is assigned to a value, such value is copied into the parameter ffme_pd_status of FFME_PowerDownStatus.request and the WUSME sublayer generates an FFME_PowerDownStatus.request service primitive (see 5.5.2).	TRUE	The state diagram requests to the GEPOF entity to go to the sleep power state. An FFME_PowerDownStatus.request service primitive shall be generated.
		FALSE	The state diagram requests to the GEPOF entity to go to the Normal power state. An FFME_PowerDownStatus.request service primitive shall be generated.
link_sleep_success	When this variable is assigned to a value, such value is copied into the parameter link_sleep_success of PHY_LinkSleep.indication and the WUSME sublayer generates a PHY_LinkSleep.indication service primitive (see ISO 21111-2:—, 6.8.2).	TRUE	Synchronised link sleep algorithm is successful. A PHY_LinkSleep.indication service primitive shall be generated.
		FALSE	Synchronised link sleep algorithm is failed. A PHY_LinkSleep.indication service primitive shall be generated.
link_sleep_req	This variable reports the reception of a PHY_LinkSleep.request (see ISO 21111-2:—, 6.8.1).	TRUE	A PHY_LinkSleep.request is received and the variable link_sleep _req shall be set to TRUE.
		FALSE	A PHY_LinkSleep.request is not received and the variable link_sleep _req shall be set to FALSE.
signal_detect_reg	This variable stores the value of the signal_detect_reg parameter of the last received CON_SignalDetected.indication (see 5.4.5).	TRUE	The value of the signal_detect_reg parameter of the last received CON_SignalDetected.indication service primitive is TRUE. Then, the variable signal_detect_reg shall be set to TRUE.
		FALSE	The value of the signal_detect_reg parameter of the last received CON_SignalDetected.indication service primitive is FALSE. Then, the variable signal_detect_reg shall be set to FALSE.

5.7.3.2 WUSME synchronised link sleep state diagram

WUSME synchronised link sleep functionality shall comply with the WUSME synchronised link sleep state diagram in Figure 9.

NOTE The WAIT_EVENTS state is the same as the one specified in Figure 8.

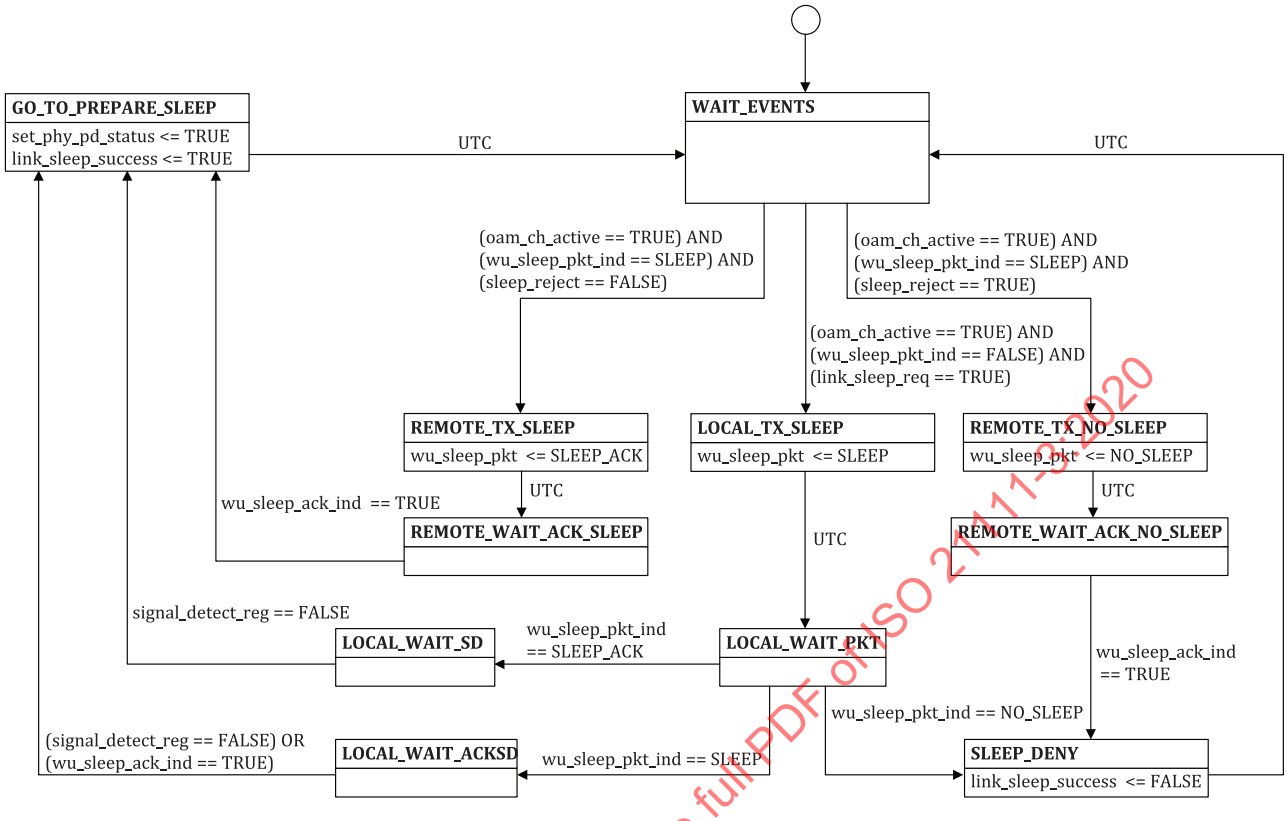


Figure 9 — WUSME synchronised link sleep state diagram

5.7.4 PHY_SleepStatus.indication generation

WUSME sublayer shall generate a PHY_SleepStatus.indication (see ISO 21111-2:—, 6.8.6) when it receives a FFME_PowerDownStatus.indication (see 5.5.3) or the variable power_off_entity changes its value (see Table 13).

The sleep_status parameter of PHY_SleepStatus.indication shall be determined from the pd_status parameter of FFME_PowerDownStatus.indication in accordance to Table 12.

Table 12 — PHY_SleepStatus.indication sleep_status parameter determination

pd_status parameter value	sleep_status parameter value
FALSE	NORMAL
TRUE	SLEEP

5.8 FFME sublayer

5.8.1 General

FFME sublayer shall transit between the states shown in the state diagram specified in 5.8.2.

5.8.2 FFME power state functionality

The FFME power state functionality shall perform the transitions between the power states specified in ISO 21111-2:—, 6.2.

The FFME power state functionality shall comply with the state diagram of Figure 10, and the associate state diagram variables specified in 5.8.2.1.

Sleep power state specified in ISO 21111-2:—, 6.2 is split in two FFME_power states: Prepare_sleep and Deep_sleep. Normal power state specified in ISO 21111-2:—, 6.2 is mapped into FFME_power state Normal.

5.8.2.1 FFME power state diagram variables

Table 13 specifies the FFME power state diagram variables.

Table 13 — FFME power state diagram variables

Variable	Associated action	Value	Specification
pd_status	When this variable is assigned to a value, such value is copied into the parameter pd_status of FFME_PowerDownStatus.indication and the FFME sublayer generates an FFME_PowerDownStatus.indication service primitive (see 5.5.3). Additionally, the value of this variable is also copied into the parameter 802-3bv_pd_status of 802-3bv_PowerDownStatus.request and the FFME sublayer generates an 802-3bv_PowerDownStatus.request service primitive (see 5.6.2).	TRUE	The IEEE 802.3bv physical layer is in power-down state. An FFME_PowerDownStatus.indication service primitive and an 802-3bv_PowerDownStatus.request service primitive shall be generated.
		FALSE	The IEEE 802.3bv physical layer is not in power-down state. An FFME_PowerDownStatus.indication service primitive and an 802-3bv_PowerDownStatus.request service primitive shall be generated.
power_off_entity	This variable changes when the power supply connected to the GEPOF entity goes to or from power off mode as specified in ISO 21111-2.	TRUE	The power supply connected to the GEPOF entity is in power-off mode. Then, the variable power_off_entity shall be set to TRUE.
		FALSE	The power supply connected to the GEPOF entity is not in power-off mode. Then, the variable power_off_entity shall be set to FALSE.
nphy_inh_sleep_req	This variable stores the value of the nphy_inh_sleep_req parameter of the last received NPHY_WakeUpForward.request (see ISO 21111-2:—, 6.9.1).	TRUE	The value of the nphy_inh_sleep_req parameter of the last received NPHY_WakeUpForward.request service primitive is TRUE. Then, the variable nphy_inh_sleep_req shall be set to TRUE.
		FALSE	The value of the nphy_inh_sleep_req parameter of the last received NPHY_WakeUpForward.request service primitive is FALSE. Then, the variable nphy_inh_sleep_req shall be set to FALSE.
power_state_is_normal	When the GEPOF entity enters or exits the Normal power status, the value of this variable is copied into the parameter power_state_is_normal of NPHY_WakeUpForward.indication and an NPHY_WakeUpForward.indication service primitive is generated (see ISO 21111-2:—, 6.9.2).	TRUE	The GEPOF entity is in the Normal power state. An NPHY_WakeUpForward.indication service primitive shall be generated.
		FALSE	The GEPOF entity is not in the Normal power state. An NPHY_WakeUpForward.indication service primitive shall be generated.
ffme_wu_ind_gen	When this variable is assigned to TRUE, the FFME sublayer generates an FFME_WakeUp.indication service primitive (see 5.4.2).	TRUE	An FFME_WakeUp.indication shall be generated.
		FALSE	An FFME_WakeUp.indication shall not be generated.

Table 13 *(continued)*

Variable	Associated action	Value	Specification
ffme_sd_ind	This variable stores the value of the signal_detect parameter of the last received 802-3bv_RXDETECT.indication (see 5.6.3).	TRUE	The value of the signal_detect parameter of the last received 802-3bv_RXDETECT.indication service primitive is OK. The meaning of OK for this parameter of the service primitive is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.1.5. Then, the variable ffme_sd_ind shall be set to TRUE.
		FALSE	The value of the signal_detect parameter of the last received 802-3bv_RXDETECT.indication is FAIL. The meaning of FAIL for this parameter of the service primitive is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.1.5. Then, the variable ffme_sd_ind shall be set to FALSE.
ffme_pd_status	This variable stores the value of the ffme_pd_status parameter of the last received FFME_PowerDownStatus.request (see 5.5.2).	TRUE	The value of the ffme_pd_status parameter of the last received FFME_PowerDownStatus.request was TRUE. Then, the variable ffme_pd_status shall be set to TRUE.
		FALSE	The value of the ffme_pd_status parameter of the last received FFME_PowerDownStatus.request was FALSE. Then, the variable ffme_pd_status shall be set to FALSE.

5.8.2.2 FFME power state diagram

FFME power state functionality shall comply with the FFME power state diagram in Figure 10.

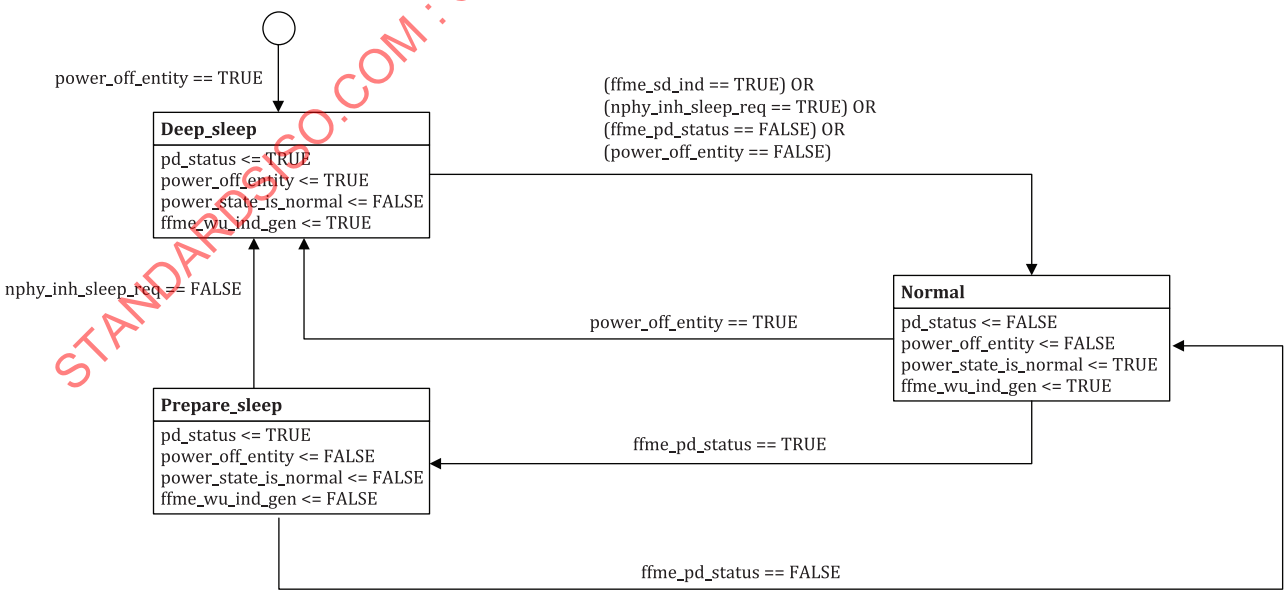


Figure 10 — FFME power state diagram

5.9 Conciliation sublayer

5.9.1 General

The conciliation sublayer shall implement the functions that generate the following conciliation service primitives:

— CON_WakeUpSleepPacket.indication (see 5.4.3);

— CON_WakeUpSleepPacketACK.indication (see 5.4.4);

— CON_SignalDetected.indication (see 5.4.5).

The information used to generate the service primitives shall be extracted from the MDIO registers specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

The conciliation sublayer shall also implement the functions that write the MDIO registers specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 when receiving the following conciliation service primitive:

— CON_WakeUpSleepPacket.request (see 5.4.2).

The conciliation sublayer and its service primitives use certain bits of the MDIO register 3.500. TXO_MSGT bit is the bit 12 of the MDIO register 3.500. TXO_MERT bit is the bit 13 of the MDIO register 3.500. TXO_REQ bit is the bit 15 of the MDIO register 3.500.

The conciliation sublayer implements also the CRC16 computation.

5.9.2 Conciliation sublayer variables

Table 14 specifies the conciliation sublayer variables.

Table 14 — Conciliation sublayer variables

Variable	Associated action	Value	Description
pkt_id	This variable stores the OAMPDU identifier (see ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 45-160a).	TRUE	The TXO_MSGT bit is equal to TXO_REQ when a CON_ WakeUpSleepPacket.request service primitive is received. Then, the variable pkt_id shall be set to TRUE.
		FALSE	The TXO_MSGT bit is different from TXO_REQ when a CON_ WakeUpSleepPacket.request service primitive is received. Then, the variable pkt_id shall be set to FALSE.

5.9.3 CRC16 computation

The OAMPDU is composed of a total of 140 bit. These 140 bit are the concatenation, from the LSB to the MSB, of the set of bits TXO_DATA0 to TXO_DATA8 in this order, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 45.2.3.47a.5, 115.3.4, and 115.9.

This subclause specifies how to compute a set of 16 bit for extra error detection capability from the 124 least significant bits of the OAMPDU. The computed set of 16 bit is called CRC16.

The generator polynomial is $(x + 1)\cdot(x^{15} + x^{14} + x^{13} + x^{11} + x^{9} + x^{8} + x^{5} + x + 1)$.

The CRC16 shall be computed from the 124 least significant bits of the OAMPDU and shall produce the same result as the implementation shown in Figure 11 and the procedure specified in this subclause. Each shift register element from S0 to S15 in Figure 11 stores one bit. The adders shall be one bit wide and module 2 (XOR).

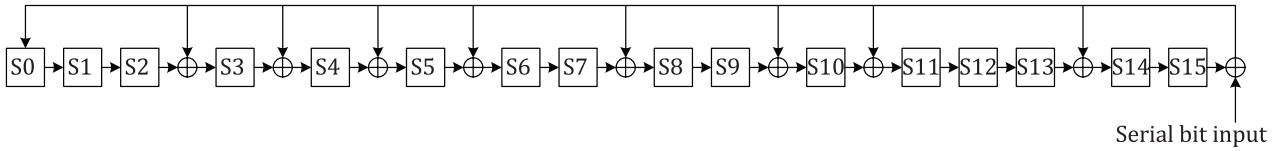


Figure 11 — CRC16 computation

The procedure to obtain CRC16 from the 124 least significant bits of the OAMPDU is the following:

1) The shift register elements from S0 to S15 shall be initialised with the value of 0000_{16} before the 124 least significant bits of the OAMPDU are introduced in the implementation of Figure 11.

2) The 124 least significant bits of the OAMPDU, starting with the LSB, are then used to compute the CRC16. The serial bit input of Figure 11 is set sequentially to each of the bit used to compute the CRC16. For each different bit in the serial bit input, a partial result of the computation is stored in each shift register element. For S0 the computation is always the feedback bit, computed as the XOR of the serial bit input and the bit stored in S15. For the rest of shift register elements, the partial result of the computation is one of the two possibilities:

   — the XOR of the bit stored in the left side shift register element and the feedback bit, or

   — the bit stored in the left side shift register.

3) After the 124 bit are serially processed, the 16 bit stored in the shift register elements from S15 to S0 in Figure 11 are the CRC16. The MSB of CRC16 is equal to the bit stored in S15 and the LSB of CRC16 is equal to the bit stored in S0.

5.9.4 Generating ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli from CON_WakeUpSleepPacket.request

The request to send a synchronised link sleep or wake-up event service primitive (CON_WakeUpSleepPacket.request) shall be implemented by performing the transmission of an OAMPDU following the steps specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.9.1.

The first 12 bit of the OAMPDU shall be the 12 most significant bits of the CID.

The following 128 user data bits of the OAMPDU shall be:

1) the 12 least significant bits of the CID, as specified in Table 15,

2) 4 bit set to zero,

4) the 16 bit of the protocol identifier for synchronised link sleep and wake-up protocol, as specified in Table 15,

5) the 16 bit of the packet type to transmit, as specified in Table 15, depending on the parameter c45_wu_sleep_pkt (see 5.4.2),

6) 64 bit set to zero, and

7) CRC16 computed using this OAMPDU as specified in 5.9.3.

5.9.5 Generating CON_WakeUpSleepPacket.indication from ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli

The conciliation sublayer shall generate a CON_WakeUpSleepPacket.indication service primitive after the reception of a packet specified in the synchronised link sleep algorithm.

The reception of a packet consists on the reception of an OAMPDU with a fixed content.

The sequence of ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli from IEEE 802.3bv physical layer that leads to the reception of an OAMPDU is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.9.3.

To generate a CON_WakeUpSleepPacket.indication service primitive the content of the received OAMPDU shall fulfil all the following requirements:

— the composed CID shall be the one specified in Table 15,

— the protocol identifier shall be equal to the one specified for synchronised link sleep and wake-up protocol (see Table 15),

— the packet type shall be one of the valid values specified in Table 15, and

— the CRC16 computed for this OAMPDU as specified in 5.9.3 matches with the CRC16 field of this OAMPDU.

When CON_WakeUpSleepPacket.indication is generated, its parameter wu_sleep_pkt_remote shall be set according to the received packet type of Table 15.

5.9.6 Generating CON_WakeUpSleepPacketACK.indication from ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli

The necessary sequence of ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli from an IEEE 802.3bv physical layer to generate CON_WakeUpSleepPacketACK.indication shall be the following:

1) wait until the value of TXO_MERT bit of MDIO register 3.500 and the value of the conciliation sublayer variable pkt_id are equal, and

2) then, CON_WakeUpSleepPacketACK.indication shall be generated.

CON_WakeUpSleepPacketACK.indication shall be present the time necessary to make a transition in any of the state diagrams specified in Figure 8 or Figure 9, or when TXO_MERT bit and the value of the conciliation sublayer pkt_id are the same.

5.9.7 Generating CON_SignalDetected.indication from ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli

The sequence of ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45 stimuli from an IEEE 802.3bv physical layer to generate CON_SignalDetected.indication shall be the following:

1) wait until the MDIO register 1.10.0 changes, and

2) then, CON_SignalDetected.indication shall be generated with its parameter signal_detect_reg equal to the value of the MDIO register 1.10.0.

CON_SignalDetected.indication shall be present the time necessary to make a transition in the state diagram specified in Figure 9.

5.9.8 Conciliation sublayer constants

Table 15 specifies the value of conciliation sublayer constants and the relationship with CON_WakeUpSleepPacket.indication parameter wu_sleep_pkt_remote.

Table 15 — Conciliation sublayer constants

Constant	Description	Value	Associated parameter	Associated parameter value
ISO TC22/SC31 CID	CID corresponding to ISO TC22/SC31	$BAF21C_{16}$	None	None
Protocol identifier for synchronised link sleep and wake-up	Value to identify a synchronised link sleep or wake-up packet specified in the synchronised link sleep algorithm	0001_{16}	None	None
SLEEP packet type	Value to identify a SLEEP packet specified in the synchronised link sleep algorithm	0000_{16}	wu_sleep_pkt_remote	SLEEP
NO_SLEEP packet type	Value to identify a NO_SLEEP packet specified in the synchronised link sleep algorithm	0001_{16}	wu_sleep_pkt_remote	NO_SLEEP
SLEEP_ACK packet type	Value to identify a SLEEP_ACK packet specified in the synchronised link sleep algorithm	0002_{16}	wu_sleep_pkt_remote	SLEEP_ACK
WAKE_UP packet type	Value to identify a WAKE_UP packet specified in the wake-up functionality (see 5.7.2)	0003_{16}	wu_sleep_pkt_remote	WAKE_UP

6 PICS proforma

6.1 General

The supplier of a protocol implementation that claims to conform to this document shall complete the following PICS proforma in addition to the one specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.14.

The convention used in the PICS proforma and the instructions for completing it are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 21.

6.2 Major capabilities/options

Table 16 speficies the major capabilities/options.

Table 16 — Wake-up and synchronised link sleep PICS. Major capabilities/options

Item	Feature	Clause	Value/Comment	Status	Support
*WUS	Wake-up and synchronised link sleep algorithms	Clause 5	Wake-up and synchronised link sleep algorithms comply with Clause 5.	O	Yes [ ] No [ ]

6.3 Wake-up and synchronised link sleep PICS items

Table 17 specifies the wake-up and synchronised link sleep PICS items

Table 17 — Wake-up and synchronised link sleep functionality PICS items

Item	Feature	Subclause	Value/Comment	Status	Support
WUS1	WUSME wake-up functionality	5.7.2	WUSME wake-up state diagram complies with Figure 8.	WUS:M	Yes [ ]
WUS2	WUSME synchronised link sleep functionality	5.7.3	WUSME synchronised link sleep state diagram complies with Figure 9.	WUS:M	Yes [ ]
WUS3	FFME power state functionality	5.8.2	FFME power state diagram complies with Figure 10.	WUS:M	Yes [ ]

Table 17 *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
WUS4	Time to complete synchronised link sleep algorithm	ISO 21111-2:—, 6.10.1	Time to complete synchronised link sleep algorithm shall be less than 50 ms.	WUS:M	Yes [ ]
WUS5	Time to complete wake-up algorithm when the physical entities involved in the algorithm are in the Normal power state	ISO 21111-2:—, 6.10.2	Time to complete wake-up algorithm shall be less than 2 ms.	WUS:M	Yes [ ]
WUS6	tWU_Link_Active	ISO 21111-2:—, 6.10.2.2	tWU_Link_Active shall be less than 2 ms.	WUS:M	Yes [ ]
WUS7	tWU_Link_Passive	ISO 21111-2:—, 6.10.2.3	tWU_Link_Passive shall be less than 2 ms.	WUS:M	Yes [ ]
WUS8	t_Powersupply_Stable	ISO 21111-2:—, 6.10.2.4	t_Powersupply_Stable shall be less than 5 ms.	WUS:M	Yes [ ]
WUS9	t_Initialisation	ISO 21111-2:—, 6.10.2.4	t_Initialisation shall be less than 10 ms.	WUS:M	Yes [ ]
WUS10	tWU_WakeIO	ISO 21111-2:—, 6.10.2.5	tWU_WakeIO shall be less than 1 ms.	WUS:M	Yes [ ]
WUS11	tWU_Forwarding	ISO 21111-2:—, 6.10.2.6	tWU_Forwarding shall be less than 1 ms.	WUS:M	Yes [ ]

7 Test plan

7.1 Test plan scope

The test plan specified in Clause 7 is designed to determine if a certain implementation of the GEPOF physical entity complies with the requirements specified in this document and in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

The complete list of the requirements is the collection of PICS in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.14 and in Clause 6 of this document.

All requirements in the complete list belong to the physical layer as specified in ISO 7498-1.

Bit naming and MDIO register numbering are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45. CID is specified in ISO/IEC/IEEE 8802-A:2015, 1.4.162.

The high logic level and low logic level for the MDIO registers are specified in ISO/IEC/IEEE 8802-3:2017, 22.4.

The valid values of the service primitive parameters specified in this document follow a positive logic. A value equal to TRUE corresponds to a high logic level and a value equal to FALSE corresponds to a low logic level.

The valid values of the header fields in the PHD follow a positive logic and are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-6. A value equal to OK corresponds to a high logic level and a value equal to NOT_OK corresponds to a low logic level.

Clause 7 specifies test cases that contain checks inside. The result of a check shall be OK only if the expected result for this concrete check is obtained. Otherwise, the result of the check shall be fail. The expected result is specified in each test case.

7.2 Test plan architecture

The ISO/IEC 9646 series specifies the methodology to check the conformance of protocol implementations to certain PICS. This methodology does not apply fully to physical layer protocols.

However, the test plan follows when possible the "OSI conformance testing general concepts" ISO/IEC 9646-1.

The test plan is restricted to the single party testing mode as specified in ISO/IEC 9646-1. The IUT is a GEPOF entity implementation for this test plan.

The generic test environment is described in Figure 12.

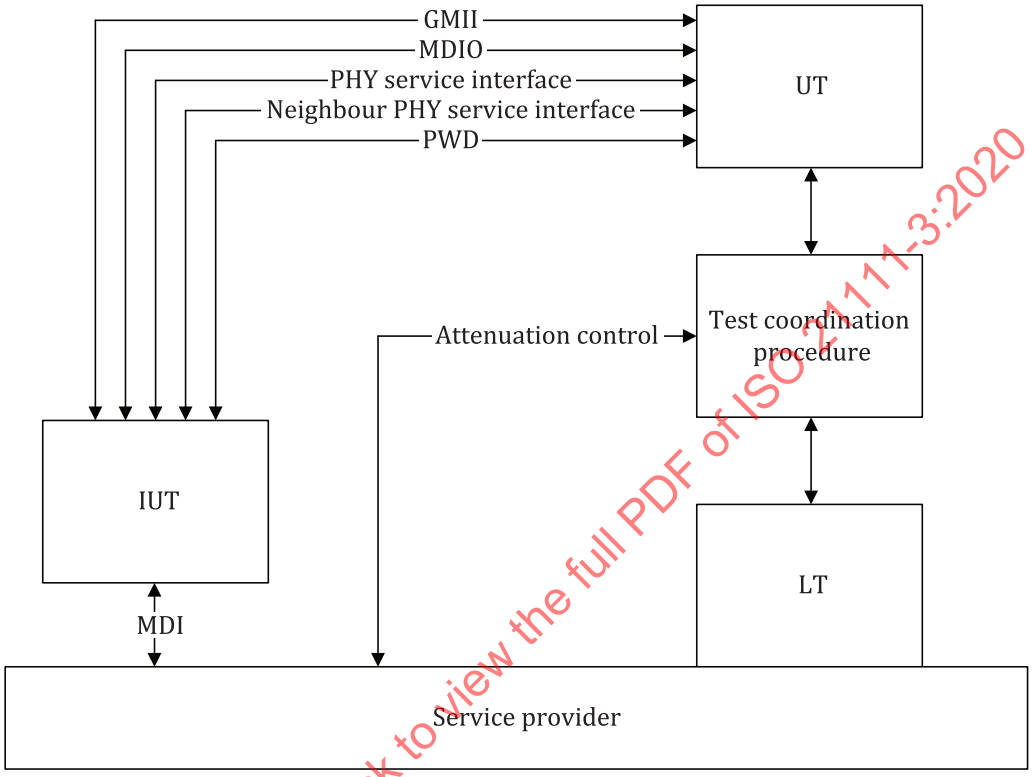


Figure 12 — Generic test environment

There are four interfaces that communicate the IUT with the UT:

— GMII as specified in ISO/IEC/IEEE 8802-3. The implementation of this interface for automotive Ethernet is specified in ISO 21111-2

— MDIO as specified in ISO/IEC/IEEE 8802-3:2017, Clauses 22, 35, and 45,

— PHY service interface, as specified in ISO 21111-2, and

— Neighbour PHY service interface, as specified in ISO 21111-2.

Additionally, the power source line PWD is also used as interface in this test plan.

The MDI standardized interface communicates the IUT with the physical medium. The MDI optical specifications are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018. The MDI is not an OSI protocol standard; therefore, the direct application of the ISO/IEC 9646 series' methodology is not possible.

Some PICS items require the measurement of several physical quantities such as AOP, frequency response or signal jitter.

The test environment used for the implementation of the test case involves four test functions:

— an LT operating as link partner of the IUT,

— an UT acting as user of the IUT,

— a test coordination procedure, running test case and granting test verdict, and

— a service provider that models the physical medium.

Each test case requires a particular implementation of the test environment defined as test setup. 7.6 specifies the test setups required by the test cases of this document.

Before test execution, the test coordination procedure configures IUT by means of the UT. The test coordination procedure configures also the service provider by selecting the optical attenuation required by the test case if needed by the test setup.

During test execution, a number of checks are performed by the test coordination procedure using the information obtained from the UT and LT. In some test cases these checks are required to be performed as measurements of physical quantities at test points inside the service provider. See ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-34 for test point specifications.

After test execution, the test coordination procedure grants the test verdict. The test verdict shall be "pass" only if all requirements listed in the observable results section of the test case are fulfilled. Otherwise, the test verdict shall be "failed".

The test case sections are specified in 7.4.

7.3 Test plan organization

The test cases are organized in groups of tests. Tests methods in the same group cover similar PICS.

The groups of tests are organized in blocks. Groups of tests in the same block share the same requirement level.

There are three blocks of groups of tests:

Block 1 contains all groups of tests that cover the GEPOF entity testing and loopback PICS items. The list of test cases in block 1 is specified in 7.5.1.

Block 2 contains all groups of tests that cover all the other mandatory GEPOF entity PICS items. The list of test cases in block 2 is specified in 7.5.2.

Block 3 contains all groups of tests that cover the optional GEPOF entity PICS items. The list of test cases in block 3 is specified in 7.5.3.

The order of execution of the test cases is strongly recommended to follow the same order as presented in this document.

The test case name is composed of the group of tests name in capital letters followed by a correlative test case number inside the group.

7.4 Test case sections

The test case specification consists of the following sections:

— purpose,

— test case references,

— test setup,

— discussion,

— test configuration,

— test procedure steps,

— observable results, and

— remarks.

The purpose is a brief statement outlining what the test case attempts to achieve.

The test case reference section specifies source material external to the test plan, including specific subsections pertinent to the test case definition, or any other references that might be helpful in understanding the test methodology and/or test results.

The test setup section specifies the instruments needed to perform the test case and how they are connected. The different test setups used in this document are specified in 7.6.

The discussion section covers the assumptions made in the design or implementation of the test case, as well as known limitations. Other items specific to the test case are covered here.

The test configuration section describes the initial configuration of the test environment. Small changes in the configuration shall not be included here and are generally covered in the test procedure steps section described in the paragraph below.

The test procedure steps section of the test case contains the systematic instructions in steps for carrying out the test. It provides a cookbook approach to testing and may be interspersed with observable results. The steps may consist of getting information from the IUT through the UT, set the instruments that compose the LT to perform some action or perform checks using the information obtained from the UT and LT among others. The test coordination procedure runs the test procedure steps and performs the checks that lead to the test verdict.

The observable results section lists the specific observables that shall be examined by the test coordination procedure in order to verify that the IUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail verdict for a particular test case is based on the successful (or unsuccessful) detection of a specific observable result. The test coordination procedure shall determine that the test case verdict is equal to "pass" only if all requirements listed in the observable results section are fulfilled.

The remarks section contains a description of known issues with the test case, which can affect test results in certain situations.

7.5 Test case reference tables

7.5.1 Block 1: test mode and loopback test cases

Table 18 specifies block 1 test cases.

Table 18 — Block 1: test modes and loopbacks test cases

Group	Test	Name	Description
Loopbacks	LBT_1	Loopback control	Verifies that the loopback mode selection is possible by using MDIO registers.
	LBT_2	GMII loopback	Verifies that the GMII loopback mode fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	LBT_3	PMD loopback	Verifies that the PMD service interface loopback mode fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	LBT_4	Line loopback	Verifies that the line loopback mode fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

Table 18 *(continued)*

Group	Test	Name	Description
Test modes	TMT_1	Test mode configuration general	Verifies that the configuration and general properties of test modes fulfil functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_2	Test mode 1 transmission	Verifies that the test mode 1 fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_3	Test mode 1 reception	Verifies that the test mode 1 fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_4	Test mode 2 transmission	Verifies that the pattern generated fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_5	Test mode 3 transmission	Verifies that the pattern generated fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_6	Test mode 4 transmission	Verifies that the pattern generated fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_7	Test mode 5 transmission	Verifies that the pattern generated fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	TMT_8	Test mode 6 transmission	Verifies that the pattern generated fulfils functionality specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.5.2 Block 2: PCS, PMA, PMD and MDI test cases

Table 19 specifies block 2 test cases.

Table 19 — Block 2: PCS, PMA, PMD and MDI test cases

Group	Test	Name	Description
PCS	PCST_1	PCS transmission signalling	Verifies that the IUT transmits a compliant transmit block structure as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	PCST_2	PCS transmission PHD	Verifies that the IUT transmits properly the PHD contents with the correct modulation, encoding, and position inside the transmit block as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	PCST_3	PCS transmission payload data	Verifies that the IUT transmits a compliant transmit block containing a fixed and known payload data.
	PCST_4	PCS reception header and payload data	Verifies that the IUT receives properly the PHD and payload data contents with the correct modulation, encoding, and position inside the transmit block.
	PCST_5	PCS transmission alignment	Verifies that the IUT sends properly using the PHD.TX.NEXT.PDB.OFFSET field in the PHD the information about the offset of the PCS measured from the beginning of the transmit block.
	PCST_6	PCS reception alignment	Verifies that the IUT receives properly using the PHD.TX.NEXT.PDB.OFFSET field in the PHD the information about the offset of the PCS measured from the beginning of the transmit block.

[a] Specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.13 is 6 500 bit-times not including delay in the POF cable and in the in-line connectors. A consideration of 1 ns per bit-time without taking additional channel delay is taken into account to reach the 6,5 µs requirement.

Table 19 *(continued)*

Group	Test	Name	Description
PMA	PMAT_1	Transmission PMA power scaling	Verifies that the IUT transmits a compliant transmit block and that each of the sub-blocks that compose it (pilot S1, pilot $S2_x$, and PHS_x) are correctly power scaled to generate symbols at the output of the PMA in such way that $-1 \leq x(t) < 1$.
	PMAT_2	THP transmission	Verifies that the payload data transmitted by the IUT is properly precoded using the Tomlinson-Harashima precoding and reset at the times specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1.
	PMAT_3	State diagrams – Transmit PHD commit point	Verifies that a change in the internal variable in the IUT that shall change the value of its associated PHD field is effectively reflected in the PHD transmitted over the first complete transmit block started after the internal variable change.
	PMAT_4	State diagrams – Receive PHD commit point	Verifies that a change in the internal variable in the IUT that shall change after receiving the value of its associated PHD field is effectively performed after PHS decoding of the received transmit block.
	PMAT_5	State diagrams – TX control	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.2 and Figure 115-22.
	PMAT_6	State diagrams – RX control	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.3 and Figure 115-23.
	PMAT_7	State diagrams – Link monitor	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.4 and Figure 115-24.
	PMAT_8	State diagrams – PHD monitor	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.5 and Figures 115-25, 115-26 and 115-27.
	PMAT_9	State diagrams – Adaptive THP TX	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.2 and Figure 115-28.
	PMAT_10	State diagrams – Adaptive THP request	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.3 and Figure 115-29.
	PMAT_11	State diagrams – Quality monitor state diagram	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.7.4 and Figure 115-30.

[a] Specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.13 is 6 500 bit-times not including delay in the POF cable and in the in-line connectors. A consideration of 1 ns per bit-time without taking additional channel delay is taken into account to reach the 6,5 µs requirement.

Table 19 *(continued)*

Group	Test	Name	Description
	PMAT_12	Synchronisation	Verifies that the IUT performs correctly the coarse and fine-tuning synchronisation with a transmitter that complies with the maximum clock deviation specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.2.
	PMAT_13	Equalization and BER measurement	Verifies that the IUT performs correctly the equalization algorithm that allows reaching the BER specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 when the system is designed for certain channel type specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.7.
PMD	PMDT_1	PMD transmit function – Electrical to optical	Verifies that the IUT performs correctly the PMD transmit function defined as the translation of electrical signals to optical signals. The test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3.
	PMDT_2	PMD transmit function – Power control	Verifies that the IUT turns on and off the optical power output in transmission by using the PMD_TXPWR.request as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.
	PMDT_3	PMD reception function – Optical to electrical	Verifies that the IUT converts the received optical power into electrical signal.
	PMDT_4	PMD reception function – Signal detection	Verifies that the IUT detects the presence of the optical signal at its input following the values given in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.4 and Table 115-7.
PMD/MDI	PMD_MDIT_1	Transmitter optical specifications – AOP	Verifies that the IUT fulfils the AOP required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_2	Transmitter optical specifications – ER	Verifies that the IUT fulfils the ER required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_3	Transmitter optical specifications – Centre wavelength	Verifies that the IUT fulfils the centre wavelength required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_4	Transmitter optical specifications – Spectral width	Verifies that the IUT fulfils the spectral width required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_5	Transmitter optical specifications – Rise time	Verifies that the IUT fulfils the rise time required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_6	Transmitter optical specifications – Fall time	Verifies that the IUT fulfils the fall time required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_7	Transmitter optical specifications – Signal overshoot	Verifies that the IUT fulfils the signal overshoot required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_8	Transmitter optical specifications – Positive output droop	Verifies that the IUT fulfils the positive output droop required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

[a] Specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.13 is 6 500 bit-times not including delay in the POF cable and in the in-line connectors. A consideration of 1 ns per bit-time without taking additional channel delay is taken into account to reach the 6,5 µs requirement.

Table 19 *(continued)*

Group	Test	Name	Description
	PMD_MDIT_9	Transmitter optical specifications – Negative output droop	Verifies that the IUT fulfils the negative output droop required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2
	PMD_MDIT_10	Transmitter optical specifications – Signal distortion	Verifies that the IUT fulfils the signal distortion (2nd, 3rd and 4th order harmonic and residual distortion), required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_11	Transmitter optical specifications – Relative intensity noise	Verifies that the IUT fulfils the relative intensity noise required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_12	Transmitter optical specifications – Transmitter off transition time	Verifies that the IUT reaches the AOP in transmission to be considered in transmission quiet mode in less than the off-transition time t_{OFF} specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.
	PMD_MDIT_13	Transmitter optical specifications – Transmitter on transition time	Verifies that the IUT reaches the AOP in transmission to be considered in transmission active operation in less than the on-transition time t_{ON} specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.
	PMD_MDIT_14	Transmitter optical specifications – Modal power distribution	Verifies that the IUT fulfils the modal power distribution required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_15	Transmitter optical specifications – Timing jitter	Verifies that the IUT fulfils the timing jitter required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.
	PMD_MDIT_16	Receiver optical specifications – AOP for a minimum BER	Verifies that the IUT fulfils the minimum and maximum AOP required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 and Table 115-10 measured in TP3 for all channel types specified for 1000BASE-RHC.
	PMD_MDIT_17	Receiver optical specifications – Damage threshold power	Verifies that the IUT fulfils the damage threshold power required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-10 Note a.
Delay	DLYT_1	Transmission plus reception delay	Verifies that the delay measured from the time when an bit pattern sequence sent over the IUT GMII transmission interface (GTX_CLK, TXD<7:0>, TX_EN and TX_ER in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3) to the time when the same bit pattern sequence is received, is lower than 6,5 µs, as specified[a] in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.13.

[a] Specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.13 is 6 500 bit-times not including delay in the POF cable and in the in-line connectors. A consideration of 1 ns per bit-time without taking additional channel delay is taken into account to reach the 6,5 µs requirement.

7.5.3 Block 3. EEE, OAM and wake-up and synchronised link sleep test cases

Table 20 specifies block 3 test cases.

Table 20 — Block 3. EEE, OAM and wake-up and synchronised link sleep test cases

Group	Test	Name	Description
EEE	EEET_1	Enter to LPI mode transmit operation	Verifies that the IUT enters properly into LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 and that the structure of the transmit block when entering the LPI mode matches the structure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-31.
	EEET_2	EEE capability exchange	Verifies that the IUT enters into LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 only when both, the link partner and the IUT, have the EEE capability activated, and it is properly announced in the IUT header.
	EEET_3	Loop test for LPI mode	Verifies that the IUT that enters into LPI mode continues the normal reception of GMII transactions when normal operation is resumed.
	EEET_4	Resume from LPI mode transmit operation	Verifies that the IUT resumes properly from LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 and that normal communication is possible after the resume from LPI mode.
OAM	OAMT_1	State diagrams – OAM transmit control	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.9.4.2 and Figure 115-42.
	OAMT_2	State diagrams – OAM receive control	Verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.9.4.3 and Figure 115-43.
	OAMT_3	Loop test for OAMPDU transmission and reception	Verifies that the IUT transmits and receives OAMPDUs.
Wake-up functionality and synchronised link sleep algorithm	WUST_1	WUSME synchronised link sleep state diagram – Synchronised link sleep ACK	Verifies that the IUT responds with a SLEEP_ACK packet to a synchronised link sleep requirement from its link partner.
	WUST_2	WUSME synchronised link sleep state diagram – SLEEP_ACK packet reception	Verifies that the IUT generates a synchronised link sleep requirement to its link partner and the response is a SLEEP_ACK packet.
	WUST_3	WUSME synchronised link sleep state diagram – SLEEP packet reception	Verifies that the IUT generates a synchronised link sleep requirement to its link partner and the response is a SLEEP packet.
	WUST_4	WUSME synchronised link sleep state diagram – Sleep rejection	Verifies that the IUT rejects a synchronised link sleep requirement from its link partner.
	WUST_5	WUSME wake-up state diagram	Verifies that the IUT transmits or receives packet specified in the synchronised link sleep algorithm with a request to perform a wake-up.

7.6 Test setups

7.6.1 General

A list of test setups and their description is specified in Table 21.

The name of each test setup is composed of the letters TS_ followed by a descriptive short name of the test setup.

Some of the test setups are already specified in the ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 specifications. In this case, a comment in the description field of Table 21 and a column in Table 22 are included.

Table 21 — Test setups and description

Test setup number	Test setup name	Description
1	TS_BASE	The IUT is connected over the GMII interface with a GMII station, and over MDIO interface with an MDIO station. Both stations are controlled by a test coordination procedure. The optical RX connector (MDI RX) of the IUT is connected with a transmit block generator (see 7.6.2). The optical TX connector (MDI TX) of the IUT is connected with a transmit block analyser. Both instruments are controlled by a test coordination procedure. Additionally, in each of the POF cables, an optical attenuator is introduced and programmed remotely by the test coordination procedure. POF cables fulfil the POF channel type II as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-38.
2	TS_EXTEND	This setup is the same as TS_BASE but adding two more measurement instruments. The first one is devoted to control using the exact time when the power supply is connected or disconnected to the IUT. The second one controls the wake I/O and detects and generates electrical signals as specified in ISO 21111-2.
3	TS_SIGPOW	The IUT is excited using a test mode with a known pattern. The optical signal power is physically analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3.
4	TS_AOPTX	The IUT is excited using a test mode with a known pattern. The optical signal AOP is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3.
5	TS_ER	The IUT is excited using a test mode with a known pattern. The optical signal ER is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.5.
6	TS_CW	The IUT is excited using a test mode with a known pattern. The optical signal centre wavelength is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.1 and IEC 61280-1-3.
7	TS_SW	The IUT is excited using a test mode with a known pattern. The optical signal spectral width is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.2 and IEC 61280-1-3.
8	TS_RT _FT	The IUT is excited using a test mode with a known pattern. The optical signal rise and falling time is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.4.
9	TS_OS	The IUT is excited using a test mode with a known pattern. The optical signal overshoot (OS) is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.6.
10	TS_NOD_POD	The IUT is excited using a test mode with a known pattern. The optical negative and positive output droop is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.7.
11	TS_DIST	The IUT is excited using a test mode with a known pattern. The optical signal distortion 2nd, 3rd, 4rd and residual harmonic distortion is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.8.
12	TS_RIN	The IUT is excited using a test mode with a known pattern. The optical transmitter relative intensity noise is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.10.
13	TS_MPD	The IUT is excited using a test mode with a known pattern. The modal power distribution is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.11.

Table 21 *(continued)*

Test setup number	Test setup name	Description
14	TS_TJ	The IUT is excited using a test mode with a known pattern. The timing jitter is analysed, without decodification of symbols. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.9.
15	TS_2LP	Two optically linked IUTs (a system composed of two link partners linked by an optical channel). One of them (transmitter) is set in a test mode. An instrument that sets a variable optical attenuation is inserted. Resulting optical signal with certain AOP is analysed and inserted in the link partner (reception) IUT. This test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 and 115.6.3.4.
16	TS_AOPRX	Equivalent to TS_EXTEND adding a controlled POF transfer function block in each of the links.
17	TS_LOOP	An IUT with MDI TX and MDI RX interfaces linked by a 1-m POF cable. The transfer function of this cable fulfils the POF channel type II as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-38.

Table 22 specifies the test cases associated with each test setup. The test cases are grouped by blocks.

Table 22 — Test setups and related test cases grouped to blocks

Test setup number	Test setup name	Block 1	Block 2	Block 3	Document where test setup is specified
1	TS_BASE	LBT_1	PCST_1	EEET_1	This document
		LBT_2	PCST_2	EEET_2	
		LBT_3	PCST_3	EEET_4	
		LBT_4	PCST_4	OAMT_1	
		TMT_1	PCST_5	OAMT_2	
		TMT_2	PCST_6		
		TMT_3	PMAT_1		
		TMT_4	PMAT_2		
		TMT_5	PMAT_3		
		TMT_6	PMAT_4		
		TMT_7	PMAT_5		
		TMT_8	PMAT_6		
			PMAT_7		
			PMAT_8		
			PMAT_9		
			PMAT_10		
			PMAT_11		
			PMAT_12		
			PMDT_3		
			PMDT_4		

Table 22 *(continued)*

Test setup number	Test setup name	Block 1	Block 2	Block 3	Document where test setup is specified
2	TS_EXTEND	None	None	WUST_1 WUST_2 WUST_3 WUST_4 WUST_5 PMD_MDIT_12 PMD_MDIT_13	This document
3	TS_SIGPOW	None	PMDT_1 PMDT_2	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3
4	TS_AOPTX	None	PMD_MDIT_1	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3
5	TS_ER	None	PMD_MDIT_2	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.5
6	TS_CW	None	PMD_MDIT_3	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.1
7	TS_SW	None	PMD_MDIT_4	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.2
8	TS_RT_FT	None	PMD_MDIT_5 PMD_MDIT_6	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.4
9	TS_OS	None	PMD_MDIT_7	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.6
10	TS_NOD_POD	None	PMD_MDIT_8 PMD_MDIT_9	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.7
11	TS_DIST	None	PMD_MDIT_10	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.8
12	TS_RIN	None	PMD_MDIT_11	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.10
13	TS_MPD	None	PMD_MDIT_14	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.11
14	TS_TJ	None	PMD_MDIT_15	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.9
15	TS_2LP	None	PMD_MDIT_16 PMD_MDIT_17	None	ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 and 115.6.3.4
16	TS_AOPRX	None	PMAT_13	None	This document

Table 22 *(continued)*

Test setup number	Test setup name	Block 1	Block 2	Block 3	Document where test setup is specified
17	TS_LOOP	None	DLYT_1	EEET_3 OAMT_3	This document

7.6.2 Test setup 1: TS_BASE

The elements that compose the test setup 1 are the following:

— The UT is composed of the following elements:

  — GMII station: instrument that transmits a bit pattern sequence with controlled content over a GMII interface.

  — MDIO station: instrument that translates test coordination procedure write or read operations on IUT registers into MDIO transactions.

— The LT is composed of the following elements:

  — Transmit block generator: instrument that transmits optically a transmit block with controlled content, both for control information and payload data. It shall use a reference light emitter that complies with ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 requirements. It shall precode the data payload contents using the coefficients stored in a local variable to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1c. The time when the transmit block is generated shall be controllable from the test coordination procedure.

  — Transmit block analyser: instrument that receives optically a transmit block and process it. That includes synchronisation, equalization and linearization of the communication channel. It also detects the presence of optical signal beyond the limits established in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018. It shall use a reference light receiver that complies with ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 requirements.

— The service provider that models the physical medium is composed of the following elements:

  — Optical attenuator: instrument that adds a controlled amount of attenuation to the optical channel. It is controlled by the test coordination procedure.

  — POF cables: four 1-m POF cables that shall fulfil the fibre optic channel type II as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-38.

— The test coordination procedure runs the test case and grants the test verdict.

The service provider frequency response up to 160 MHz when the optical attenuator is set to 0 dB shall be higher than −3 dB.

The service provider frequency response up to 160 MHz shall be flat with an allowed deviation of 0,5 dB around the mean.

The MDIO station of the UT shall perform at least two successful reads of MDIO registers within 100 µs.

The MDI RX port of the IUT is connected to the transmit block generator through a programmable optical attenuator that is controlled by the test coordination procedure. The transmit block generator is also controlled by the test coordination procedure that shall load the data to be transmitted and the time when the transmission shall start.

The MDI TX port of the IUT is connected to the transmit block analyser through a programmable optical attenuator that is controlled by the test coordination procedure. The transmit block analyser is also

controlled by the test coordination procedure that shall receive the analysed transmit block and the timing when the analysed transmit block arrives.

Figure 13 specifies test setup 1 TS_BASE.

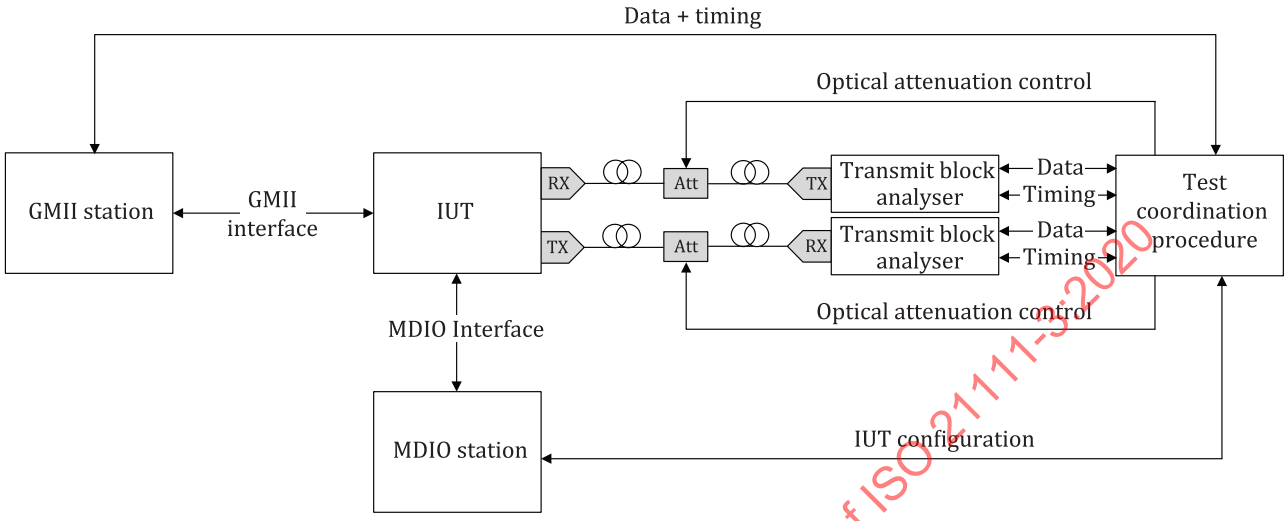


Figure 13 — Test setup 1: TS_BASE

The test coordination procedure controls the IUT configuration by means of the MDIO station and shall set any of the available loopback or test modes available. Moreover, the test coordination procedure can also control the GMII station to generate a fixed and controlled GMII transaction in the GMII interface.

7.6.3 Test setup 2: TS_EXTEND

The test setup 2 is specified as a superset of test setup 1 that includes two additional instruments into the UT:

— ON/OFF control: instrument that connects or disconnects the power supply to the IUT and annotates the time when the connection or disconnection occurs.

— Wake-up line detection: instrument that detects the time when a neighbour wake-up electrical signal is generated by the IUT as specified in ISO 21111-2. This instrument also generates a neighbour wake-up electrical signal to the IUT.

Both instruments are controlled by the test coordination procedure, and the exact time when the events take place shall be controlled in a precise manner.

The required connection among instruments for test setup 2 TS_EXTEND is specified in Figure 14.

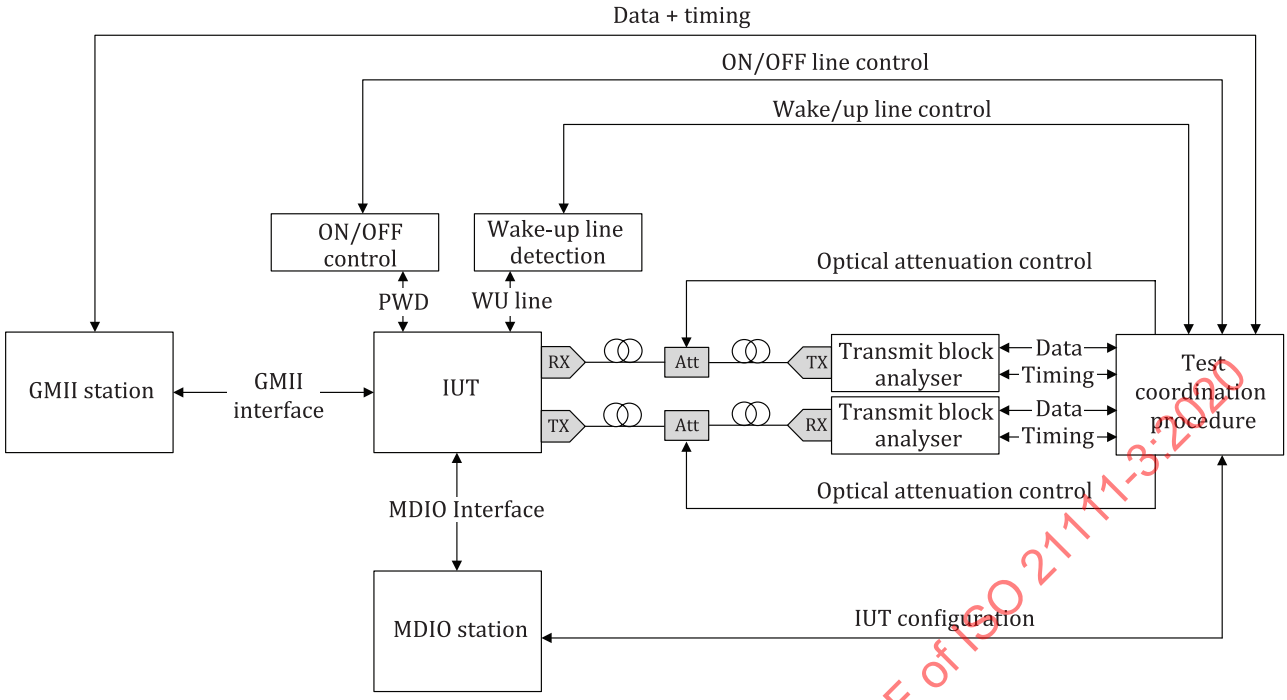


Figure 14 — Test setup 2: TS_EXTEND

7.6.4 Test setup 3: TS_SIGPOW

See Table 21.

7.6.5 Test setup 4: TS_AOPTX

See Table 21.

7.6.6 Test setup 5: TS_ER

See Table 21.

7.6.7 Test setup 6: TS_CW

See Table 21.

7.6.8 Test setup 7: TS_SW

See Table 21.

7.6.9 Test setup 8: TS_RT_FT

See Table 21.

7.6.10 Test setup 9: TS_OS

See Table 21.

7.6.11 Test setup 10: TS_NOD_POD

See Table 21.

7.6.12 Test setup 11: TS_DIST

See Table 21.

7.6.13 Test setup 12: TS_RIN

See Table 21.

7.6.14 Test setup 13: TS_MPD

See Table 21.

7.6.15 Test setup 14: TS_TJ

See Table 21.

7.6.16 Test setup 15: TS_2LP

See Table 21.

7.6.17 Test setup 16: TS_AOPRX

Test setup 16 TS_AOPRX is a variation of test setup 2 TS_EXTEND. It is specified in Figure 15.

There are four differences in the service provider compared to test setup 2 TS_EXTEND:

— The 1-m POF cable between the MDI transmission side of the IUT and the optical attenuator is substituted by a POF cable that shall have a flat attenuation in the frequency range from 0 MHz to 162,5 MHz with a maximum deviation of 0,1 dB.

— The 1-m POF cable between the optical attenuator and the reception side of the LT is substituted by a controlled POF transfer function element.

— The 1-m POF cable between the transmission side of the LT and the optical attenuator is substituted by a POF cable that shall have a flat attenuation in the frequency range from 0 MHz to 162,5 MHz with a maximum deviation of 0,1 dB.

— The 1-m POF cable between the optical attenuator and the MDI reception side of the IUT is substituted by a controlled POF transfer function element.

The normalized frequency response of the POF transfer function element shall depend on the channel type (I, II or III) as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.7 supported by the IUT.

The normalized frequency response of the POF transfer function block shall be based on the one specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-37 for channel type I, Figure 115-38 for channel type II and Figure 115-39 for channel type III.

The normalized frequency response of the POF transfer function block shall be always between the normalized frequency response specified for the IUT supported channel type and 0,2 dB more for the frequency range from 0 MHz to 162,5 MHz.

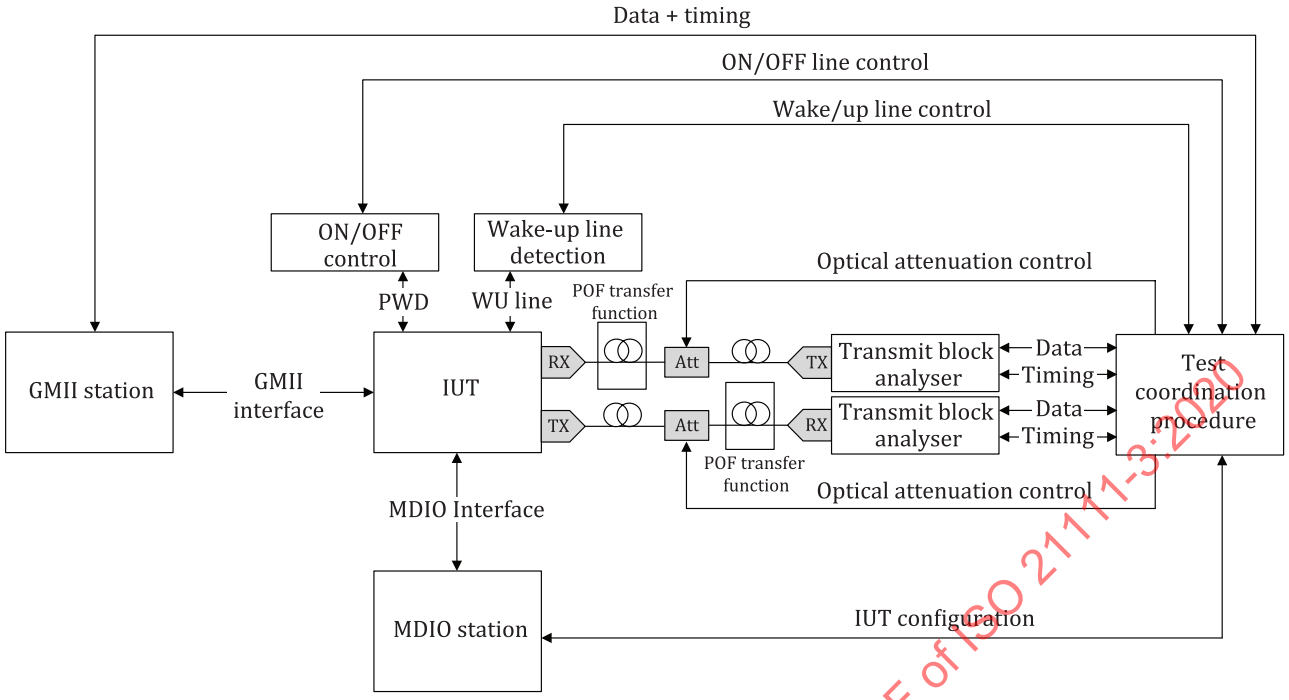


Figure 15 — Test setup 16: TS_AOPRX

7.6.18 Test setup 17: TS_LOOP

The service provider in this test setup is different from the one specified in test setup 1 TS_BASE.

MDI transmission and reception side of the IUT are connected by means of a 1-m POF cable that shall fulfil the fibre optic channel type II as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-38.

There is no LT in this test setup.

Test setup 17 TS_LOOP is specified in Figure 16.

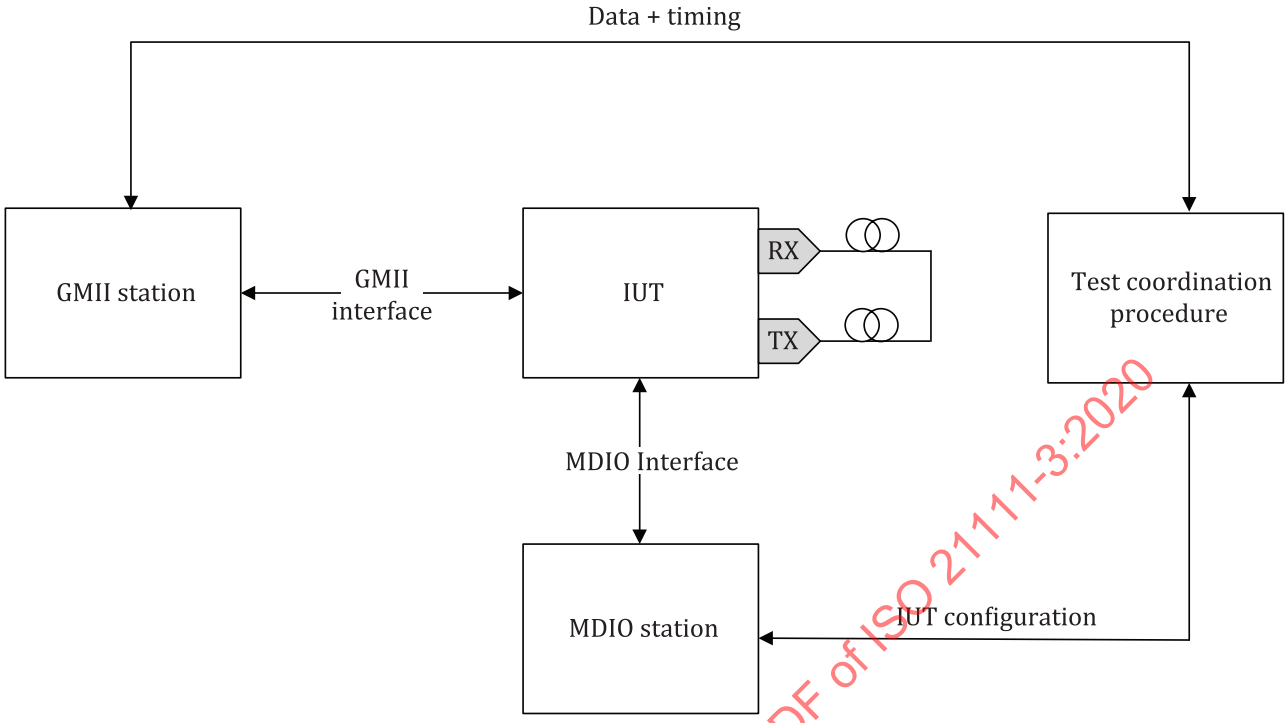


Figure 16 — Test setup 17: TS_LOOP

7.7 Block 1 test cases: test modes and loopbacks

7.7.1 General

7.7 specifies the test cases about test modes and loopbacks.

7.7.2 LBT_1: Loopback control

7.7.2.1 Purpose

This test case verifies that the loopback is configured by means of the MDIO and that the default value of the loopback registers is equal to 000_2.

7.7.2.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.10.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.2.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.2.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 specifies three different loopback modes that are configurable using bit 12 to bit 10 of the MDIO register 3.518.

7.7.2.5 Test configuration

Not applicable.

7.7.2.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
3) The test coordination procedure waits 100 ms.
4) The UT reads the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
5) The UT writes 001_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
6) The UT reads the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
7) The UT writes 010_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
8) The UT reads the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
9) The UT writes 011_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
10) The UT reads the MDIO register bit 12 to bit 10 of the MDIO register 3.518.

7.7.2.7 Observable results

— After step 4) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 000_2.
— After step 6) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 001_2.
— After step 8) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 010_2.
— After step 10) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 011_2.

7.7.2.8 Remarks

If the reset value of the bit 12 to bit 10 of the MDIO register 3.518 is different from 000_2, or the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.3 LBT_2: GMII loopback

7.7.3.1 Purpose

This test case verifies the GMII loopback in the IUT. Concretely it verifies that the same bit pattern sequence sent over the IUT GMII transmission interface (GTX_CLK, TXD<7:0>, TX_EN and TX_ER in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3) is received over the IUT GMII reception interface (RX_CLK, RXD<7:0>, RX_DV, RX_ER in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3). Additionally, this test case verifies also that every bit pattern sequence with error transmitted by the GMII Tx interface generates an error indication in the GMII Rx interface.

7.7.3.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.1.6.
— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.10.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.3.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.3.4 Discussion

This test case is specified based on the logical description of the GMII interface given in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018. The IUT may implement this interface by using one of the options given in ISO 21111-2. In this case, the stimuli and check data are modified accordingly.

7.7.3.5 Test configuration

Not applicable.

7.7.3.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 001_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

7) The UT captures the received GMII transactions.

8) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 64 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 64 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

9) The UT captures the received GMII transactions.

10) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$ but the last one, that are set to 00_{16} and GMII.TX_ER = 1, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA not

being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

11) The UT captures the received GMII transactions.

7.7.3.7 Observable results

— After step 3) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 001_2.

— After step 7) all the GMII received transactions are the same as the ones specified in step 6).

— After step 9) all the GMII received transactions are the same as the ones specified in step 8).

— After step 11) at least one of the GMII received transactions that compounds the bit pattern sequence sets the GMII.RX_ERR to 1_2.

7.7.3.8 Remarks

Check that the GMII interface cables are correctly attached.

Check that the GMII station is capable of generating individual transactions, both valid and erroneous.

7.7.4 LBT_3: PMD loopback

7.7.4.1 Purpose

This test case verifies the PMD loopback in the IUT. Concretely it verifies that the same bit pattern sequence sent over the IUT GMII transmission interface (GTX_CLK, TXD<7:0>, TX_EN and TX_ER in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3) is received over the IUT GMII reception interface (RX_CLK, RXD<7:0>, RX_DV, RX_ER in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3).

7.7.4.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.1.6.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.10.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.4.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.4.4 Discussion

The PMD loopback is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.10. This test case verifies that this loopback is working correctly, meaning that every bit pattern sequence sent over the GMII Tx interface is correctly received by the GMII Rx interface. Additionally, every bit pattern sequence with error transmitted by the GMII Tx interface generates an error indication in the GMII Rx interface.

7.7.4.5 Test configuration

Not applicable.

7.7.4.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 010_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT waits till the MDIO register bit 2 of the MDIO register 1.1 is set to 1_2.

7) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

8) The UT captures the received GMII transactions.

9) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 64 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 64 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

10) The UT captures the received GMII transactions.

11) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$ but the last one, that are set to 00_{16} and GMII.TX_ER = 1, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA not being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

12) The UT captures the received GMII transactions.

7.7.4.7 Observable results

— After step 3) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 010_2.

— After step 8) all the GMII received transactions are the same as the ones specified in step 7).

— After step 10) all the GMII received transactions are the same as the ones specified in step 9).

— After step 12) all the GMII received transactions are the same as the ones specified in step 11).

7.7.4.8 Remarks

Check that the GMII interface cables are correctly attached.

Check that the GMII station is capable of generating individual transactions, both valid and erroneous.

7.7.5 TMT_1: Test mode configuration general

7.7.5.1 Purpose

This test case verifies that the test mode is configured over the MDIO and that the default value of the test mode register is 000_2.

7.7.5.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.5.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.5.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5 specifies the different test modes.

7.7.5.5 Test configuration

Not applicable.

7.7.5.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 3.0.
3) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
5) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
6) The UT writes 010_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
7) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
8) The UT writes 011_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
9) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
10) The UT writes 100_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
11) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
12) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
13) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
14) The UT writes 110_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

15) The UT reads the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

7.7.5.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 000_2.

— After step 5) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 7) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 010_2.

— After step 9) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 011_2.

— After step 11) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 100_2.

— After step 13) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 15) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 110_2.

7.7.5.8 Remarks

If the reset value of the bit 15 to bit 13 of the MDIO register 3.518 is different from 000_2, or the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.6 TMT_2: Test mode 1 transmission

7.7.6.1 Purpose

This test case verifies that the IUT sets properly the test mode 1, and that the transmit block generated in this mode is the one expected.

7.7.6.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.6.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.6.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.1, the generated transmit block when IUT is configured in test mode 1 is equivalent to the transmission of a data payload set to zero, ignoring the inputs coming from the GMII interface. The 64B/65B encoder is not used in this test mode.

Rx binary scrambling is defined as the inverse function of the payload data binary scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2.

7.7.6.5 Test configuration

Not applicable.

7.7.6.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 3.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 3.0 is equal to 0_2.
6) The UT performs the link establishment using THP between IUT and transmit block analyser.
   i) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
   ii) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
      a) PHD.TX.NEXT.MODE is set to 0_2.
      b) PHD.RX.HDRSTATUS is set to OK.
      c) PHD.RX.RXLINKSTATUS is set to NOT_OK.
      d) PHD.TX.NEXT.THP.SETID is set to 0_2.
      e) PHD.RX.REQ.THP.SETID is set to 0_2.
   iii) The UT waits till a transmit block with header fields PHD.RX.HDRSTATUS set to OK and PHD.RX.REQ.THP.SETID equal to 1_2 is received by the transmit block analyser and captures it.
   iv) The test coordination procedure stores the value of the captured PHD.RX.REQ.THP.COEF[8:0] fields in the IUT_COEF_1 variable.
   v) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:
      a) PHD.TX.NEXT.MODE is set to 0_2.
      b) PHD.RX.HDRSTATUS is set to OK.
      c) PHD.RX.RXLINKSTATUS is set to NOT_OK.
      d) PHD.TX.NEXT.THP.SETID is set to 1_2.
      e) PHD.RX.REQ.THP.SETID is set to 0_2.
   vi) The UT waits till at least two transmit blocks with header fields with PHD.RX.HDRSTATUS set to OK and PHD.RX.LINKSTATUS set to OK are received by the transmit block analyser.
   vii) The UT waits till THP coefficients are calculated in the transmit block analyser with help from the test coordination procedure if necessary. The test coordination procedure stores them in the TBA_COEF variable.
   viii) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the

equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

a) PHD.TX.NEXT.MODE is set to 0_2.

b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to NOT_OK.

d) PHD.TX.NEXT.THP.SETID is set to 1_2.

e) PHD.RX.REQ.THP.SETID is set to 1_2.

f) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

ix) The UT waits till a transmit block with header fields with PHD.RX.HDRSTATUS set to OK, PHD.RX.LINKSTATUS set to OK and PHD.TX.REQ.NEXT.SETID equal to 1_2 is received by the transmit block analyser and captures it.

x) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

a) PHD.TX.NEXT.MODE is set to 0_2.

b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to OK.

d) PHD.TX.NEXT.THP.SETID is set to 1_2.

e) PHD.RX.REQ.THP.SETID is set to 1_2.

f) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

xi) The UT waits till the MDIO register bit 2 of the MDIO register 1.1 is set to 1_2.

7) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.6.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 7) all the captured payload data of the transmit block is equal to 0_2 after the Rx binary scrambling.

7.7.6.8 Remarks

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.7.7 TMT_4: Test mode 2 transmission

7.7.7.1 Purpose

This test case verifies that the IUT sets properly the test mode 2, and that the output of the IUT transmitter in this mode is the one expected.

7.7.7.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.7.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.7.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.2, the generated transmit block when IUT is configured in test mode 2 is equivalent to the transmission of a sequence of alternated symbols {+1} and {–1}, resulting into a square wave at 162,5 MHz.

7.7.7.5 Test configuration

Not applicable.

7.7.7.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 010_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.7.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 010_2.

— After step 6) the sequence received is equal to an alternation of {–1} and {1} symbols, resulting into a square wave at 162,5 MHz.

7.7.7.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.8 TMT_5: Test mode 3 transmission

7.7.8.1 Purpose

The test case verifies that the IUT sets properly the test mode 3, and that the output of the IUT transmitter in this mode is the one expected.

7.7.8.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.8.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.8.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.3, the generated transmit block when IUT is configured in test mode 3 is equivalent to the transmission of a sequence of ten symbols {+1} and ten symbols {–1}, resulting into a square wave at 16,25 MHz.

7.7.8.5 Test configuration

Not applicable.

7.7.8.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 011_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.8.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 011_2.

— After step 6) the sequence received is equal to an alternation of ten {+1} followed by ten {–1} symbols, resulting into a square wave at 16,25MHz.

7.7.8.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.9 TMT_6: Test mode 4 transmission

7.7.9.1 Purpose

The test case verifies that the IUT sets properly the test mode 4, and that the output of the IUT transmitter in this mode is the one expected.

7.7.9.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.9.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.9.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.4, the generated transmit block when IUT is configured in test mode 4 is equivalent to the transmission of two consecutive subsequences q_1 repeated 250 times and q_2 repeated 250 times. q_1 is a sequence of twenty symbols {+1} followed by ten symbols {−1}, and q_2 is a sequence of ten symbols {+1} followed by twenty symbols {−1}.

7.7.9.5 Test configuration

Not applicable.

7.7.9.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 100_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.9.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 100_2.

— After step 6) the sequence received is equal to the expected transmitted sequence in 7.7.9.4.

7.7.9.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.10 TMT_7: Test mode 5 transmission

7.7.10.1 Purpose

The test case verifies that the IUT sets properly the test mode 5, and that the output of the IUT transmitter in this mode is the one expected.

7.7.10.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.10.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.10.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.5, the generated transmit block when IUT is configured in test mode 5 is equivalent to the transmission of all symbols set to {0}.

7.7.10.5 Test configuration

Not applicable.

7.7.10.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.10.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 6) the sequence received is equal to the expected transmitted sequence in 7.7.10.4.

7.7.10.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.11 TMT_8: Test mode 6 transmission

7.7.11.1 Purpose

The test case verifies that the IUT sets properly the test mode 6, and that the output of the IUT transmitter in this mode is the one expected.

7.7.11.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.11.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.11.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.6, the generated transmit block when IUT is configured in test mode 5 is equivalent to the transmission of a scramble sequence specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.6.

7.7.11.5 Test configuration

Not applicable.

7.7.11.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 110_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.11.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 110_2.

— After step 6) the sequence received is equal to the expected transmitted sequence in 7.7.11.4.

7.7.11.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.7.12 TMT_3: Test mode 1 reception

7.7.12.1 Purpose

The test case verifies that the IUT receives properly the test mode 1, and that the state diagrams in the IUT are working properly.

7.7.12.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.12.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.12.4 Discussion

The test modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5. As specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.1, the generated transmit block that the IUT receives is equivalent to the transmission of a payload data set to zero.

7.7.12.5 Test configuration

Not applicable.

7.7.12.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 1_2.

   ii) PHD.RX.HDRSTATUS is set to OK.

   iii) PHD.RX.RXLINKSTATUS is set to OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 1_2.

   v) PHD.RX.REQ.THP.SETID is set to 1_2.

   vi) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

8) The UT reads MDIO register 3.522.

9) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero but a single bit equal to 1 precoded using the coefficients IUT_COEF_1 to perform

the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 1_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to OK.

iv) PHD.TX.NEXT.THP.SETID is set to 1_2.

v) PHD.RX.REQ.THP.SETID is set to 1_2.

vi) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

10) The UT reads MDIO register 3.522.

7.7.12.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the register 1.1, bit 2 is equal to 1_2.

— After step 8) the register 3.522 is equal to 0_2.

— After step 10) the register 3.522 is different from 0, increasing the value by one each transmit block received.

— After step 10) all GMII transactions are idle.

7.7.12.8 Remarks

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.7.13 LBT_4: Line loopback

7.7.13.1 Purpose

The test case verifies that the IUT operates in the line loopback mode.

7.7.13.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.10.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.7.13.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.7.13.4 Discussion

The loopback modes are specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018. In the line loopback mode, all data received is transmitted before the GMII interface, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3.

Rx binary scrambling is defined as the inverse function of the payload data binary scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2.

7.7.13.5 Test configuration

Not applicable.

7.7.13.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 011_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.
7) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.
8) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero but a single bit equal to 1 precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:
   i) PHD.TX.NEXT.MODE is set to 0_2.
   ii) PHD.RX.HDRSTATUS is set to OK.
   iii) PHD.RX.RXLINKSTATUS is set to OK.
   iv) PHD.TX.NEXT.THP.SETID is set to 1_2.
   v) PHD.RX.REQ.THP.SETID is set to 1_2.
   vi) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.
9) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

7.7.13.7 Observable results

— After step 3) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 011_2.
— After step 6) the register 1.1, bit 2 is equal to 1_2.
— After step 7) all the captured payload data of the transmit block is equal to 0_2 after the Rx binary scrambling.
— After step 9) all the captured payload data of the transmit block is equal to 0_2 but a single 1_2 after the Rx binary scrambling.

7.7.13.8 Remarks

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8 Block 2 test cases: Mandatory functionality

7.8.1 General

This subclause specifies the test cases covering the mandatory functionality of ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.2 PCST_1: PCS transmission signalling

7.8.2.1 Purpose

This test case verifies that the IUT transmits a compliant transmit block structure as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.2.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.2.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.2.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2 specifies the structure of the transmit block (see especially Figure 115-4). This test case verifies that the IUT generates a transmit block compliant with this specification, focusing on the structure of the pilot generation S1 and S2.

7.8.2.5 Test configuration

Not applicable.

7.8.2.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

7) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

   i) The test coordination procedure checks that the first 160 symbols of the transmit block compound a pilot S1 sub-block as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.1, in which the symbols are modulated using a PAM-2 scheme.

ii) The test coordination procedure checks that the following 7 904 symbols of the transmit block correspond to the expected transmitted symbols, resulting from the payload data binary scrambler, PAM-16 encoder and data symbol scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2, 115.2.4.3 and 115.2.4.4 respectively when input data is always zero. The symbols are PAM-16 modulated.

iii) The test coordination procedure checks that the following 160 symbols of the transmit block correspond to the first PHS sub-block of 14 PHS sub-blocks as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3. The test coordination procedure steps (2 × 7 904) + 160 symbols and gets the second PHS sub-block storing the 160 symbols starting at this point. The test coordination procedure repeats by stepping again (2 × 7 904) + 160 symbols up to get the 14^{th} PHS sub-block. Demodulate performing the inverse functions to the ones specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3 and check that the PHD CRC is correct.

iv) The test coordination procedure checks that the 160 symbols block starting at symbol 2 × (160 + 7 904) is identical to the 160 symbols starting from k × (160 + 7 904), with k equal to an integer in the range of 3 to 14.

v) The test coordination procedure checks that the 160 symbols block starting at symbol 2 × (160 + 7 904) compounds a pilot S2 sub-block as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.2, in which the symbols are modulated using a PAM-2 scheme.

7.8.2.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— The results of the check specified in step 7) are all OK.

7.8.2.8 Remarks

Check the MDIO cable connections.

7.8.3 PCST_2: PCS transmission PHD

7.8.3.1 Purpose

This test case verifies that the IUT transmits properly the PHD contents, with the correct modulation, encoding and position inside the transmit block.

7.8.3.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.3.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.3.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.1 specifies the transmit block structure, and specifies the PHS sub-blocks position and length inside the transmit block. In addition, ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3 describes how the PHD is encoded and scrambled to compose the symbols. Finally, in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4, the fields that compose the PHD are described.

This test case verifies that the IUT transmits properly the PHD with known contents. To validate the PHD, the test procedure steps go through the link establishment process, capturing and analysing the transmit blocks at each point. The test mode 1 is set to avoid any data coming from the GMII.

7.8.3.5 Test configuration

Not applicable.

7.8.3.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
3) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
4) The test coordination procedure waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
5) The UT performs the header lock part of the link establishment.
    i) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
    ii) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the PHD fields:
        a) PHD.TX.NEXT.MODE set to 0_2.
        b) PHD.RX.HDRSTATUS is set to OK.
        c) PHD.RX.RXLINKSTATUS is set to NOT_OK.
        d) PHD.TX.NEXT.THP.SETID is set to 0_2.
        e) PHD.RX.REQ.THP.SETID set to 0_2.
    iii) The UT waits till coarse and fine timing recovery is performed in the transmit block analyser as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.3.
    iv) The UT waits till MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.
    v) The UT waits till MDIO register bit 11 of the MDIO register 3.519 is equal to 1_2.
    vi) The UT waits till MDIO register bit 10 of the MDIO register 3.519 is equal to 1_2.
6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.
    i) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).
    ii) The test coordination procedure skips the following 7 904 symbols of the transmit block corresponding to the payload data symbols.

iii) The test coordination procedure checks that the following 160 symbols of the transmit block correspond to the first PHS sub-block of the total 14 PHS sub-blocks as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3. The test coordination procedure steps (2 × 7 904) + 160 symbols and gets the second PHS sub-block storing the 160 symbols starting at this point. The test coordination procedure repeats by stepping again (2 × 7 904) + 160 symbols up to get the 14^{th} PHS sub-block. Demodulate performing the inverse functions to the ones specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3 and check that the PHD CRC is correct. The test coordination procedure extracts the PHD as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-6.

iv) The test coordination procedure checks that PHD field PHD.TX.NEXT.MODE is equal to 1_2.

v) The test coordination procedure checks that PHD field PHD.TX.THP.SETID is equal to 0_2.

vi) The test coordination procedure checks that PHD field PHD.TX.NEXT.PDB.OFFSET is equal to 0_2.

vii) The test coordination procedure checks that PHD field PHD.RX.REQ.THP.COEF from [0] to [8] are equal to 0_2.

viii) The test coordination procedure checks that PHD field PHD.RX.LINKSTATUS is equal to NOT_OK.

ix) The test coordination procedure checks that PHD field PHD.RX.HDRSTATUS is equal to OK.

7) The test coordination procedure applies the THP coefficients calculated by the IUT in the transmit block generator.

i) The UT waits till a transmit block with header fields PHD.RX.HDRSTATUS set to OK and PHD.RX.REQ.THP.SETID equal to 1 is received by the transmit block analyser and captures it.

ii) The test coordination procedure stores the value of the captured PHD.RX.REQ.THP.COEF[8:0] fields in the IUT_COEF_1 variable.

iii) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

a) PHD.TX.NEXT.MODE is set to 0_2.

b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to NOT_OK.

d) PHD.TX.NEXT.THP.SETID is set to 1_2.

e) PHD.RX.REQ.THP.SETID is set to 0_2.

iv) The UT waits till at least two transmit blocks with header fields with PHD.RX.HDRSTATUS set to OK and PHD.RX.LINKSTATUS set to OK are received by the transmit block analyser.

8) The test coordination procedure calculates the THP coefficients in the transmission block analyser and ask the IUT to use them in the transmit blocks.

i) The UT waits till THP coefficients are calculated in the transmit block analyser with help from the test coordination procedure if necessary. The test coordination procedure stores them in the TBA_COEF variable.

ii) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

a) PHD.TX.NEXT.MODE is set to 0_2.

b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to NOT_OK.

d) PHD.TX.NEXT.THP.SETID is set to 1_2.

e) PHD.RX.REQ.THP.SETID is set to 1_2.

f) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

iii) The UT waits till a transmit block with header fields with PHD.RX.HDRSTATUS set to OK, PHD.RX.LINKSTATUS set to OK and PHD.TX.REQ.NEXT.SETID equal to 1_2 is received by the transmit block analyser and captures it.

iv) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

a) PHD.TX.NEXT.MODE is set to 0_2.

b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to OK.

d) PHD.TX.NEXT.THP.SETID is set to 1_2.

e) PHD.RX.REQ.THP.SETID is set to 1_2.

f) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

9) The UT waits till the MDIO register bit 2 of the MDIO register 1.1 is set to 1_2.

7.8.3.7 Observable results

— After step 2) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 5.iv) the value of the bit 12 of the MDIO register 3.518 is equal to 1_2.

— After step 5.v) the value of the bit 11 of the MDIO register 3.518 is equal to 1_2.

— After step 5.vi) the value of the bit 10 of the MDIO register 3.518 is equal to 1_2.

— The results of the check specified in step 6.iii) are all OK.

— The results of the check specified in step 6.iv) are all OK.

— The results of the check specified in step 6.v) are all OK.

— The results of the check specified in step 6.vi) are all OK.

— The results of the check specified in step 6.vii) are all OK.

— The results of the check specified in step 6.viii) are all OK.

— The results of the check specified in step 6.ix) are all OK.

— After step 9) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

7.8.3.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

Link margin cannot be enough to complete link establishment. Check all optical connections and the POF attenuation of the setup to be inside the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.4 PCST_3: Transmission PCS payload data

7.8.4.1 Purpose

This test case verifies that the IUT transmits a compliant transmit block containing a fixed and known payload data.

7.8.4.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.4.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.4.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2 specifies the structure of the transmit block. This test case verifies that the IUT generates a transmit block compliant with the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, with special focus on the contents of the payload data generated. Additionally, this test case also verifies the 64B/65B encoder and payload data BCH encoding as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.1.

7.8.4.5 Test configuration

Not applicable.

7.8.4.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 000_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes1 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT sets the GMII station to transmit idle status (GMII.RX_EN = 0_2).

7) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

8) The test coordination procedure obtains the lowest value of the PHD.TX.NEXT.PDB.OFFSET field from the transmit blocks transmitted by the IUT.

   i) The test coordination procedure gets all the 13 possible values of the PHD.TX.NEXT.PDB.OFFSET field from the transmit blocks transmitted by the IUT and received by the transmit block analyser.

   ii) The test coordination procedure stores the lowest value in the local variable DELTA_ZERO. The expected value is in the range from 0 to 4

9) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

   i) In a first stage, the test coordination procedure extracts the PHD.TX.NEXT.PDB.OFFSET field of the PHD specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4 from the PHS sub-blocks in the captured transmit block. If the content of the PHD.TX.NEXT.PDB.OFFSET field is different from 40+DELTA_ZERO, capture another one. If it is equal to 40+DELTA_ZERO, continue with the transmit block analyser going to ii).

   ii) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).

   iii) The test coordination procedure checks that the following 7 904 symbols of the transmit block correspond to the expected transmitted symbols, resulting from the payload data binary scrambler, PAM16 encoder and data symbol scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2, 115.2.4.3 and 115.2.4.4 respectively when input signal in the 64B/65B encoder is the one specified in 6). The first DELTA_ZERO bits of the transmit block payload data are not taken into account in the comparison.

   iv) The test coordination procedure steps 160 symbols of the transmit block and gets the following 7 904 symbols. Get the transmitted GMII transactions with the procedure specified in iii) and check that they correspond to idle transactions as expected.

   v) The test coordination procedure repeats step iv) 26 times to complete the transmit block decoding.

10) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

11) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

   i) In a first stage, the test coordination procedure extracts the PHD.TX.NEXT.PDB.OFFSET field of the PHD specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4 from the PHS sub-blocks in the captured transmit block. If the content of the PHD.TX.NEXT.PDB.OFFSET field is different from 40 + DELTA_ZERO, capture another one. If it is equal to 40+DELTA_ZERO, continue with the transmit block analyser going to ii).

   ii) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).

   iii) The test coordination procedure checks that the following 7 904 symbols of the transmit block correspond to the expected transmitted symbols, resulting from the payload data binary scrambler, PAM-16 encoder and data symbol scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2, 115.2.4.3 and 115.2.4.4 respectively when input signal in the 64B/65B encoder is the one specified in 10). The first DELTA_ZERO bits of the transmit block payload data are not taken into account in the comparison.

iv) The test coordination procedure steps 160 symbols of the transmit block and gets the following 7 904 symbols. Get the transmitted GMII transaction with the procedure specified in iii) and check that they are the expected values.

v) The test coordination procedure repeats step iv) 26 times to complete the transmit block decoding.

12) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$ but the last one, that is set to 00_{16} and GMII.TX_ER = 1, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA not being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

13) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

i) In a first stage, the test coordination procedure extracts the PHD.TX.NEXT.PDB.OFFSET field of the PHD specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4 from the PHS sub-blocks in the captured transmit block. If the content of the field is different from 40 + DELTA_ZERO, capture another one. If it is equal to 40 + DELTA_ZERO, continue with the transmit block analyser going to ii).

ii) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).

iii) The test coordination procedure checks that the following 7 904 symbols of the transmit block correspond to the expected transmitted symbols, resulting from the payload data binary scrambler, PAM-16 encoder and data symbol scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2, 115.2.4.3 and 115.2.4.4 respectively when input signal in the 64B/65B encoder is the one specified in 12). The first DELTA_ZERO bits of the transmit block payload data are not taken into account in the comparison.

iv) The test coordination procedure steps 160 symbols of the transmit block and gets the following 7 904 symbols. Get the transmitted GMII transaction with the procedure specified in iii) and check that at least one of the GMII received transactions that compounds the bit pattern sequence sets the GMII.RX_ERR to 1_2.

v) The test coordination procedure repeats step iv) 26 times to complete the transmit block decoding.

7.8.4.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 000_2.

— After step 7) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

— After step 5) vi) the value of the bit 10 of the MDIO register 3.518 is equal to 1_2.

— The results of the check specified in step 9) iii) are all OK.

— The results of the check specified in step 9) iv) are all OK.

— The results of the check specified in step 11) iii) are all OK.

— The results of the check specified in step 11) iv) are all OK.

— The results of the check specified in step 13) iii) are all OK.

— The results of the check specified in step 13) iv) are all OK.

7.8.4.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

Link margin cannot be enough to complete link establishment. Check all optical connections and the POF attenuation of the setup to be inside the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.5 PCST_4: PCS reception header and payload data

7.8.5.1 Purpose

This test case verifies that the IUT receives properly the PHD and payload data contents, with the correct modulation, encoding and position inside the transmit block.

7.8.5.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.10.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.5.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.5.4 Discussion

This test case verifies that the IUT receives properly a controlled content of PHD and payload data. The PHD received is checked indirectly, by reading the MDIO registers that change when a received PHD field is processed. I.e. when PHD.RX.HDRSTATUS goes from NOT_OK to OK, the IUT changes the bit 11 of MDIO register 3.519 from 0_2 to 1_2.

As the previous test cases are already performed and passed, the IUT PCS transmission is working properly. Then, the PMD interface level loopback mode is used to verify the reception side.

The test mode 1 (TS_BASE) is set to avoid any data coming from the GMII.

7.8.5.5 Test configuration

Not applicable.

7.8.5.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 010_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518 (PMD interface level loopback).

5) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

6) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

7) The UT performs the link establishment when IUT is in PMD loopback mode:

   i) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

   ii) The UT waits till the MDIO register 3.519 bit 12 is equal to 1_2.

   iii) The UT waits till the MDIO register 3.519 bit 11 is equal to 1_2.

   iv) The UT waits till the MDIO register 3.519 bit 10 is equal to 1_2.

   v) The UT waits till the MDIO register 3.519 bit 9 is equal to 1_2.

   vi) The UT waits till the MDIO register 3.519 bit 15 is equal to 1_2.

   vii) The UT waits till the MDIO register 3.519 bit 14 is equal to 1_2.

   viii) The UT waits till the MDIO register 3.519 bit 13 is equal to 1_2.

8) The test coordination procedure checks that the MDIO register 3.520 bit 7 to bit 0 represents a positive number with the fixed-point format specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.8.

9) The test coordination procedure checks that the MDIO register 3.521 bit 7 to bit 0 represents a positive number with the fixed-point format specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.8.

10) The test coordination procedure checks that the MDIO register 3.522 bit 15 to bit 0 are equal to 0_2.

7.8.5.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 4) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 010_2.

— After step 7) the value of the bit 15 to bit 9 of the MDIO register 3.519 is equal to 1111111_2.

— The results of the check specified in step 8) are all OK.

— The results of the check specified in step 9) are all OK.

— The results of the check specified in step 10) are all OK.

7.8.5.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.6 PCST_5: PCS transmission alignment

7.8.6.1 Purpose

This test case verifies that the IUT sends properly using the PHD.TX.NEXT.PDB.OFFSET field in the PHD the information about the offset of the PCS measured from the beginning of the transmit block.

7.8.6.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.1.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.6.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.6.4 Discussion

Because a transmit block does not contain an integer number of PDBs, in general the start of the transmit block payload data does not correspond to a PDB start. Upon reception start, the receiver uses the field PHD.TX.NEXT.PDB.OFFSET extracted from the previous received header to localize the start of the first complete PDB.

In order to avoid storing two consecutives transmit blocks in the transmit block analyser, the test case is based on the fact that the PHD.TX.NEXT.PDB.OFFSET in consecutive transmit blocks follows a known sequence derived of ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Equation 115-3.

7.8.6.5 Test configuration

Not applicable.

7.8.6.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

4) The test coordination procedure checks that the GMII station is transmitting idle transactions (TX_EN = 0_2; TX_ER = 0_2) to the IUT.

5) The test coordination procedure obtains the lowest value of the PHD.TX.NEXT.PDB.OFFSET field from the transmit blocks transmitted by the IUT.

   i) The test coordination procedure gets all the 13 possible values of the PHD.TX.NEXT.PDB.OFFSET field from the transmit blocks transmitted by the IUT and received by the transmit block analyser.

ii) The test coordination procedure stores the lowest value in the local variable DELTA_ZERO. The expected value is in the range from 0 to 4.

6) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

i) In a first stage, the test coordination procedure extracts the PHD.TX.NEXT.PDB.OFFSET field of the PHD specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4, from the PHS sub-blocks in the captured transmit block.

a) The test coordination procedure takes as reference the sequence SEQ(1:13) = [40 15 55 30 5 45 20 60 35 10 50 25 0] + DELTA_ZERO.

b) If the content of the field PHD.TX.NEXT.PDB.OFFSET is SEQ(k), the test coordination procedure takes the current transmission block offset CURR_OFFSET as SEQ(k-1) if k > 1, and SEQ(13) if k = 1.

ii) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).

iii) The test coordination procedure checks that the following 7 904 symbols of the transmit block correspond to the expected transmitted symbols, resulting from the payload data binary scrambler, PAM-16 encoder and data symbol scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2, 115.2.4.3 and 115.2.4.4 respectively when input signal in the 64B/65B encoder is the one specified in 3). The first CURR_OFFSET bits of the transmit block payload data is not taken into account in the comparison.

iv) The test coordination procedure skips 160 symbols of the transmit block and gets the following 7 904 symbols. Get the transmitted GMII transaction with the procedure specified in iii) and check that they are the expected values.

v) The test coordination procedure repeats step iv) 26 times to complete the transmit block decoding.

vi) The test coordination procedure marks CURR_OFFSET in the sequence SEQ as checked.

vii) If all CURR_OFFSET in the sequence SEQ is checked, the test coordination procedure finishes the test. If not, it returns to 6).

7.8.6.7 Observable results

— After step 6) all accumulated checks for all possible values of CURR_OFFSET are OK.

7.8.6.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.7 PCST_6: PCS reception alignment

7.8.7.1 Purpose

This test case verifies that the IUT receives properly, by using the PHD.TX.NEXT.PDB.OFFSET field in the PHD, the information about the offset of the PCS measured from the beginning of the transmit block. This test case verifies also the correct decoding procedure in the 64B/65B decoder

7.8.7.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.1.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.7.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.7.4 Discussion

Because a transmit block does not contain an integer number of PDBs, in general the start of the transmit block payload data does not correspond to a PDB start. Upon reception start, the receiver uses the field PHD.TX.NEXT.PDB.OFFSET extracted from the previous received header to localize the start of the first complete PDB.

To perform this test case the PMD interface level loopback is used and it is tested that control and data PDB types as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.1.1 are correctly received during at least 13 consecutive transmit blocks, which cover all possible values of the PHD.TX.NEXT.PDB.OFFSET header field.

7.8.7.5 Test configuration

Not applicable.

7.8.7.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 010_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518 (PMD interface level loopback).

4) The UT performs the link establishment when IUT is in PMD loopback mode as specified in 7) of 7.8.5.6.

5) The UT sets the GMII station to transmit idle status (GMII.RX_EN = 0_2).

6) The UT captures at least 141 120 GMII transactions in the reception of the GMII station.

7) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

8) The UT captures at least 141 120 GMII transactions in the reception of the GMII station.

9) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 64 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being

the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 64 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

10) The UT captures at least 141 120 GMII transactions in the reception of the GMII station.

11) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$ but the last one, that is set to 00_{16} and GMII.TX_ER = 1, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA not being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

12) The UT captures at least 141 120 GMII transactions in the reception of the GMII station.

7.8.7.7 Observable results

— After step 3) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 010_2.

— After step 4) the value of the bit 15 to bit 9 of the MDIO register 3.519 is equal to 1111111_2.

— After step 6) at least 141 120 of the GMII-captured transactions are the same as the ones specified in step 5).

— After step 8) at least 141 120 of the GMII-captured transactions are the same as the ones specified in step 7).

— After step 10) at least 141 120 of the GMII-captured transactions are the same as the ones specified in step 9).

— After step 12) at least 141 120 of the GMII-captured transactions are the same as the ones specified in step 11).

7.8.7.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.8 PMAT_1: Transmission PMA power scaling test

7.8.8.1 Purpose

This test case verifies that the IUT transmits an ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 compliant transmit block and each of the sub-blocks that compose it (pilot S1, pilot $S2_x$, and PHS_x) are correctly power scaled to generate symbols at the output of the PMA in such way that $-1 \leq x(t) < 1$.

7.8.8.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.1ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.8.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.8.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2 specifies the structure of the transmit block. This test case verifies that the IUT generates a transmit block compliant with the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, with special focus on the transmit power scaling. The test case verifies also that the different sections of the transmit block have the expected symbol range.

As the optical power is measured in TP2 after the PMD photonics, a relative calibration to the full scale equivalent to the symbols {–1} and {+1} at the output of PMA is performed. PMD photonics complies with the requirements in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

First the test mode 3 is programmed to calibrate in the transmit block analyser the expected levels of symbols {–1} and {+1}. Once calibrated, the test mode 1 is set and, after link establishment, symbols from pilot S1, pilot $S2_x$, PHD_x and payload data are collected in separate pools.

Once the required number of symbols is collected, a histogram of symbol levels is drawn for each pool and validated against the reference histogram built during the calibration stage of the test.

7.8.8.5 Test configuration

The POF cable length between optical PMD transmitter and optical PMD receiver shall be equal to 1 m. No optical attenuator shall be used in this test.

7.8.8.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 011_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518 (test mode 3).

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT captures at least 2 877 056 samples in the transmit block analyser. The samples are obtained by synchronising the amplitude capture at TP2 at the centre of each of the semiperiods of the generated square wave at 16,25 MHz. The test coordination procedure performs a histogram over the received amplitudes with maximum power $P_{1max} = (2 \times AOP_{max}) \times (ER_{max} / (ER_{max} + 1))$ and minimum power $P_{0min} = 2 \times (AOP_{min} / (ER_{max} + 1))$ and at least 100 bins. P_{1max}, P_{0min}, AOP_{max}, AOP_{min} and ER_{max} are expressed in linear units. AOP_{max}, AOP_{min} and ER_{max} are extracted from ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8 for 1000BASE-RHC. The test coordination procedure stores this histogram in the HIST_REF variable.

7) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

8) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

9) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

10) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

11) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

    i) The test coordination procedure selects from the first 160 symbols of the transmit block (pilot S1 sub-block), the 128 in the middle of the sequence, discarding the first and last 16 symbols. The test coordination procedure stores them in the pilot S1 sub-block pool.

    ii) The test coordination procedure stores the following 7 904 symbols of the transmit block in the payload data sub-block pool.

    iii) The test coordination procedure selects from the 160 symbols of the transmit block that corresponds to the PHS sub-block, the 128 in the middle of the sequence, discarding the first and last 16 symbols. The test coordination procedure stores them in the PHS sub-block pool.

    iv) The test coordination procedure stores the following 7 904 symbols of the transmit block in the payload data sub-block pool.

    v) The test coordination procedure selects from the following 160 symbols in the transmit block (pilot S2 sub-block), the 128 in the middle of the sequence, discarding the first and last 16 symbols. The test coordination procedure stores them in the pilot S2 sub-block pool.

    vi) The test coordination procedure returns to ii) till the captured transmit block is processed.

12) The test coordination procedure repeats step 11) till at least 13 transmit blocks are processed.

13) The test coordination procedure checks that the histogram with $P_{1\max}$ and $P_{0\min}$ with maximum and minimum power values respectively and 100 bins performed over the pilot S1 sub-block pool matches the HIST_REF histogram.

14) The test coordination procedure checks that the histogram with $P_{1\max}$ and $P_{0\min}$ with maximum and minimum power values respectively and 100 bins performed over the pilot S2 sub-block pool matches the HIST_REF normalized histogram.

15) The test coordination procedure checks that the histogram with $P_{1\max}$ and $P_{0\min}$ with maximum and minimum power values respectively and 100 bins performed over the PHS sub-block pool matches the HIST_REF normalized histogram.

16) The test coordination procedure checks that the histogram with $P_{1\max}$ and $P_{0\min}$ with maximum and minimum power values respectively and 100 bins performed over the payload data sub-block pool is a uniform distribution of 16 discrete values with extreme values matching the two most probable values in the HIST_REF histogram.

7.8.8.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 010_2.

— After step 7) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 10) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

— The result of the check specified in step 13) is OK.

— The result of the check specified in step 14) is OK.

— The result of the check specified in step 15) is OK.

— The result of the check specified in step 16) is OK.

7.8.8.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.9 PMAT_2: THP transmission

7.8.9.1 Purpose

This test case verifies that the payload data transmitted by the IUT is properly precoded using the Tomlinson-Harashima precoding and that the state of the feedback filter is reset in the points specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1. This test case also verifies that the update of the coefficients sent by the link partner in the IUT transmission is performed at the time points expected.

7.8.9.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.9.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.9.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 specifies the Tomlinson-Harashima precoding that is applied to the payload data symbols of the transmit block in transmission by using the coefficients received by the link partner. This test case verifies that the THP coefficients are calculated in the IUT only after the variable rcvr_hdr_lock specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.1 is set to 1_2.

This test case also verifies that ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Equations 115-19, 115-20 and 116-21 are properly applied to the transmit block payload data, by using the coefficients received by the IUT and calculated by the transmit block analyser.

7.8.9.5 Test configuration

The POF cable length between optical PMD transmitter and optical PMD receiver shall be equal to 1 m. No optical attenuator shall be used in this test.

7.8.9.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT writes the MDIO register bit 11 of the MDIO register 1.0 with 0_2.

7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to NOT_OK.

   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

   v) PHD.RX.REQ.THP.SETID is set to 0_2.

8) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

   i) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).

   ii) The test coordination procedure stores the optical power of the following 7 904 symbols of the transmit block in a pool called FIRST_PAYLOAD.

   iii) The test coordination procedure skips 160 symbols of the transmit block and store the optical power of the following 7 904 symbols in the FIRST_PAYLOAD pool.

   iv) The test coordination procedure repeats step iii) 26 times to complete the transmit block decoding.

   v) The test coordination procedure extracts the PHD.TX.REQ.THP.SETID field of the header specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4, from the physical header sub-blocks in the captured transmit block. The test coordination procedure checks that it is equal to 0_2.

9) The test coordination procedure repeats step 8) at least 13 times.

10) The test coordination procedure performs a histogram over the FIRST_PAYLOAD pool using at least 128 bins. The test coordination procedure checks that the histogram has 16 peaks that contain all the received symbols.

11) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

12) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

   i) The test coordination procedure skips the first 160 symbols of the transmit block (pilot S1 sub-block).

   ii) The test coordination procedure checks that the following 7 904 symbols of the transmit block correspond to the expected transmitted symbols, resulting from the payload data binary scrambler, PAM-16 encoder and data symbol scrambler specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.4.2, 115.2.4.3 and 115.2.4.4 respectively when input signal in the data scrambler is always zero.

   iii) The test coordination procedure stores the 7 904 symbols' optical power measured in ii) in a pool called SECOND_PAYLOAD.

   iv) The test coordination procedure skips 160 symbols of the transmit block and gets the following 7 904 symbols. Get the transmitted payload data with the procedure specified in ii) and check that they are the expected values, in this case, all the payload data equal to 0_2.

   v) The test coordination procedure repeats step iv) 26 times to complete the transmit block decoding.

13) The test coordination procedure repeats step 12) at least 13 times.

14) The test coordination procedure performs a histogram over the SECOND_PAYLOAD pool using at least 128 bins. The test coordination procedure checks that the histogram has a uniform distribution that contains all the received symbols.

15) The test coordination procedure checks that the SECOND_PAYLOAD pool is composed of at least 13 identical sequences of 7 904 symbols.

7.8.9.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 7) the value of the bit 12 of the MDIO register 3.519 is equal to 1_2.

— After step 7) the value of the bit 11 of the MDIO register 3.519 is equal to 0_2.

— The result of the check specified in step 8) is OK.

— The result of the check specified in step 10) is OK.

— After step 11) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

— The result of the check specified in step 12) is OK.

— The result of the check specified in step 14) is OK.

— The result of the check specified in step 15) is OK.

7.8.9.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.10 PMAT_3: State diagrams – Transmit PHD commit point

7.8.10.1 Purpose

This test case verifies that a change in one internal variable is reflected in the value of the corresponding PHD field. Moreover, the change is reflected in the first complete transmit block started after the internal variable change.

7.8.10.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.10.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.10.4 Discussion

There are internal variables in the IUT that are associated with certain PHD fields sent in the transmit block.

To isolate a case when an internal variable is changed and this change is reflected in an update in a PHD field, the test case uses the transition of the local variable loc_rcvr_hdr_lock, specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.1, from NOT_OK to OK, and its publication in the PHD field PHD.RX.HDRSTATUS.

The test mode 1 is set to avoid any data coming from the GMII.

7.8.10.5 Test configuration

Not applicable.

7.8.10.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
   i) PHD.TX.NEXT.MODE is set to 0_2.
   ii) PHD.RX.HDRSTATUS is set to OK.
   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
   v) PHD.RX.REQ.THP.SETID is set to 0_2.
7) At the same time that 6) is performed, the test coordination procedure starts monitoring MDIO register bit 12 of the MDIO register 3.519 till its value is 1_2. Then, the test coordination procedure resets to zero the t_delay internal timer and starts it.
8) The UT captures transmit blocks in the transmit block analyser till the PHD field PHD.RX.HDRSTATUS is set to 1_2. Then stops the t_delay internal timer.
9) The test coordination procedure checks that the t_delay timer value is less than 1,4 ms.
10) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero. Pilot and header symbols in the transmit block are set to zero symbols as specified in ISO/IEC/IEEE/8802-3:2017/Amd 9:2018, 115.3.3.1.

11) At the same time that 10) is performed, the test coordination procedure starts monitoring MDIO register bit 12 of the MDIO register 3.519 till its value is 0_2. Then, the test coordination procedure resets to zero the t_delay internal timer and starts it.

12) The UT captures transmit blocks in the transmit block analyser till the PHD field PHD.RX.HDRSTATUS is set to 0_2. Then stops the t_delay internal timer.

13) The test coordination procedure checks that the t_delay timer value is less than 1,4 ms.

7.8.10.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 7) the value of the bit 12 of the MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 9) are all OK.

— After step 11) the value of the bit 12 of the MDIO register 3.519 is equal to 0_2.

— The results of the check specified in step 13) are all OK.

7.8.10.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.11 PMAT_4: State diagrams – Receive PHD commit point

7.8.11.1 Purpose

This test case verifies that a change in the internal variable in the IUT associated with a PHD field is effectively performed after PHD decoding of the received transmit block.

7.8.11.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.11.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.11.4 Discussion

This test case isolates a situation when the reception of certain field in the PHD triggers an internal variable change. Concretely, this test case uses the transition of the local variable rem_rcvr_hdr_lock from NOT_OK to OK after the reception of a transmit block with PHD.RX.HDRSTATUS equal to OK.

The local variable rem_rcvr_hdr_lock is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.1.

The test mode 1 is set to avoid any data coming from the GMII.

7.8.11.5 Test configuration

Not applicable.

7.8.11.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
   i) PHD.TX.NEXT.MODE is set to 0_2.
   ii) PHD.RX.HDRSTATUS is set to NOT_OK.
   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
   v) PHD.RX.REQ.THP.SETID is set to 0_2.
7) The UT waits till the MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.
8) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
   i) PHD.TX.NEXT.MODE is set to 0_2.
   ii) PHD.RX.HDRSTATUS is set to OK.
   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
   v) PHD.RX.REQ.THP.SETID is set to 0_2.
9) When the last symbol of the first transmit block is transmitted, the test coordination procedure resets t_delay, a timer with resolution of at least 1 µs.
10) The UT monitors MDIO register bit 11 of the MDIO register 3.519 till its value is 1_2.
11) The test coordination procedure stops the t_delay and checks that the value is lower than 150 µs.

7.8.11.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.
— After step 7) bit 12 of MDIO register 3.519 is equal to 1_2.
— After step 10) bit 11 of MDIO register 3.519 is equal to 1_2.
— The results of the check specified in step 11) are all OK.

7.8.11.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.12 PMAT_5: State diagrams – TX control

7.8.12.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.2 and Figure 115-22.

7.8.12.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.12.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.12.4 Discussion

Some of the internal variables of the physical layer TX control state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

7.8.12.5 Test configuration

Not applicable.

7.8.12.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to OK.

   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

   v) PHD.RX.REQ.THP.SETID is set to 0_2.

4) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 64 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being

the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 64 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

5) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

6) The UT waits till the MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

7) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

8) The UT waits till the MDIO register bit 13 of the MDIO register 3.519 is equal to 1_2.

9) The UT captures the transmit block transmitted by the IUT in the transmit block analyser. Get the transmitted GMII transactions in the payload, and check that they comply with those specified in 4).

10) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

11) The UT reads the MDIO register bit 13 of the MDIO register 3.519 and check that is equal to 0_2.

12) The UT captures the transmit block transmitted by the IUT in the transmit block analyser.

    i) Get the transmitted GMII transactions in the payload data, and check that they are not the one specified in 4).

13) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

14) The UT waits till the MDIO register bit 13 of the MDIO register 3.519 is equal to 1_2.

15) The UT captures the transmit block transmitted by the IUT in the transmit block analyser. Get the transmitted GMII transactions in the payload data, and check that they comply with those specified in 4).

7.8.12.7 Observable results

— After step 5) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 6) the value of the bit 12 of the MDIO register 3.519 is equal to 1_2.

— After step 8) the value of the bit 13 of the MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 11) are all OK.

— The results of the check specified in step 12) are all OK.

— After step 14) the value of the bit 13 of the MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 15) are all OK.

7.8.12.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.13 PMAT_6: State diagrams – RX control

7.8.13.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.3 and Figure 115-23.

7.8.13.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.13.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.13.4 Discussion

Some of the internal variables of the RX control state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

This test case needs two MDIO registers reads per transmit block.

7.8.13.5 Test configuration

Not applicable.

7.8.13.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

4) The UT sets the GMII station to transmit idle status (GMII.RX_EN = 0_2).

5) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to NOT_OK.

   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

6) The UT monitors MDIO register bit 12 of the MDIO register 3.519 till its value is 1_2.

7) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 0_2.

8) The UT sets the transmit block generator to transmit continuously a transmit block with all symbols set to zeros, without any pilots nor header.

9) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.

10) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to NOT_OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

11) The UT monitors MDIO register bit 12 of the MDIO register 3.519 till its value is 1_2.

12) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 0_2.

13) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

14) The UT monitors MDIO register bit 10 of the MDIO register 3.519 till its value is 1_2.

15) The UT sets the transmit block generator to transmit continuously a transmit block with all symbols set to zeros, without any pilots nor header.

16) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.

17) The UT performs the THP coefficient calculation and transmission by the IUT to the transmit block analyser:

    i) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

    ii) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

        a) PHD.TX.NEXT.MODE is set to 0_2.

        b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to NOT_OK.

d) PHD.TX.NEXT.THP.SETID is set to 0_2.

e) PHD.RX.REQ.THP.SETID is set to 0_2.

iii) The UT waits till a transmit block with header fields PHD.RX.HDRSTATUS set to OK and PHD.RX.REQ.THP.SETID equal to 1_2 is received by the transmit block analyser and captures it.

iv) The test coordination procedure stores the value of the captured PHD.RX.REQ.THP.COEF[8:0] fields in the IUT_COEF_1 variable.

v) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

a) PHD.TX.NEXT.MODE is set to 0_2.

b) PHD.RX.HDRSTATUS is set to OK.

c) PHD.RX.RXLINKSTATUS is set to NOT_OK.

d) PHD.TX.NEXT.THP.SETID is set to 1_2.

e) PHD.RX.REQ.THP.SETID is set to 0_2.

vi) The UT waits till at least two transmit blocks with header fields with PHD.RX.HDRSTATUS set to OK and PHD.RX.LINKSTATUS set to OK are received by the transmit block analyser.

18) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 1_2.

19) The test coordination procedure checks that the received GMII transactions are all idle.

20) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to NOT_OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

21) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 0_2.

22) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

23) The test coordination procedure checks that the received GMII transactions are generally different from idle.

24) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to NOT_OK.

iii) PHD.RX.RXLINKSTATUS is set to OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

25) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 0_2.

26) The test coordination procedure checks that the received GMII transactions are all idle.

27) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

28) The test coordination procedure checks that the received GMII transactions are generally different from idle.

29) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

30) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 1_2.

31) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 0_2.

32) The test coordination procedure checks that the received GMII transactions are all idle.

7.8.13.7 Observable results

— After step 3) the value of the bit 1of the MDIO register 1.0 is equal to 0_2.

— After step 6) the value of the bit 12 of MDIO register 3.519 is equal to 1_2.

— After step 7) the value of the bit 11 of MDIO register 3.519 is equal to 0_2.

— After step 9) the value of the bit 12 of MDIO register 3.519 is equal to 0_2.

— After step 11) the value of the bit 12 of MDIO register 3.519 is equal to 1_2.

— After step 12) the value of the bit 11 of MDIO register 3.519 is equal to 0_2.

— After step 14) the value of the bit 10 of MDIO register 3.519 is equal to 1_2.

— After step 16) the value of the bit 12 of MDIO register 3.519 is equal to 0_2.

— After step 18) the value of the bit 9 of MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 19) are all OK.

— After step 21) the value of the bit 11 of MDIO register 3.519 is equal to 0_2.

— The results of the check specified in step 23) are all OK.

— After step 25) the value of the bit 11 of MDIO register 3.519 is equal to 0_2.

— The results of the check specified in step 26) are all OK.

— The results of the check specified in step 28) are all OK.

— After step 30) the value of the bit 11 of MDIO register 3.519 is equal to 1_2.

— After step 31) the value of the bit 13 of MDIO register 3.519 is equal to 0_2.

— The results of the check specified in step 32) are all OK.

7.8.13.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.14 PMAT_7: State diagrams – Link monitor

7.8.14.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.4 and Figure 115-24.

7.8.14.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.14.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.14.4 Discussion

Some of the internal variables of the link monitor state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

This test case needs two MDIO registers reads per transmit block.

7.8.14.5 Test configuration

Not applicable.

7.8.14.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

4) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to NOT_OK.

   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

   v) PHD.RX.REQ.THP.SETID is set to 0_2.

5) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 0_2.

6) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 0_2.

7) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.

8) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to OK.

   iii) PHD.RX.RXLINKSTATUS is set to OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

   v) PHD.RX.REQ.THP.SETID is set to 0_2.

9) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 0_2.

10) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 1_2.

11) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.

12) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to OK.

   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

   v) PHD.RX.REQ.THP.SETID is set to 0_2.

13) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 0_2.

14) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 0_2.

15) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.

16) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.

17) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 1_2.

18) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 1_2.

19) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 1_2.

20) The test coordination procedure stores the optical attenuation of the POF link ending at IUT receiver in the local variable RX_IUT_ATT.

21) The test coordination procedure increases the optical attenuation of the POF link ending at IUT receiver by 1 dB.

22) The test coordination procedure checks if the MDIO register bit 7 to bit 0 of the MDIO register 3.520 represents a negative number with the fixed-point format specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.8.

23) If the check result in 22) is OK, the test coordination procedure continues with 24). If not, it returns to 21).

24) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 0_2.

25) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 1_2.

26) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.

27) The test coordination procedure sets the optical attenuation of the POF link ending at IUT receiver to RX_IUT_ATT.

28) Wait 10 ms.

29) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 1_2.

30) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 1_2.

31) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 1_2.

32) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

33) The test coordination procedure checks that MDIO register bit 13 of the MDIO register 3.519 is equal to 0_2.

34) The test coordination procedure checks that MDIO register bit 14 of the MDIO register 3.519 is equal to 0_2.

35) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.

7.8.14.7 Observable results

— After step 3) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 5) the value of the bit 13 of MDIO register 3.519 is equal to 0_2.

— After step 6) the value of the bit 14 of MDIO register 3.519 is equal to 0_2.

— After step 7) the value of the bit 15 of MDIO register 3.519 is equal to 0_2.

— After step 9) the value of the bit 13 of MDIO register 3.519 is equal to 0_2.

— After step 10) the value of the bit 14 of MDIO register 3.519 is equal to 1_2.

— After step 11) the value of the bit 15 of MDIO register 3.519 is equal to 0_2.

— After step 13) the value of the bit 13 of MDIO register 3.519 is equal to 0_2.

— After step 14) the value of the bit 14 of MDIO register 3.519 is equal to 0_2.

— After step 15) the value of the bit 15 of MDIO register 3.519 is equal to 0_2.

— After step 17) the value of the bit 13 of MDIO register 3.519 is equal to 1_2.

— After step 18) the value of the bit 14 of MDIO register 3.519 is equal to 1_2.

— After step 19) the value of the bit 15 of MDIO register 3.519 is equal to 1_2.

— After step 24) the value of the bit 13 of MDIO register 3.519 is equal to 0_2.

— After step 25) the value of the bit 14 of MDIO register 3.519 is equal to 1_2.

— After step 26) the value of the bit 15 of MDIO register 3.519 is equal to 0_2.

— After step 29) the value of the bit 13 of MDIO register 3.519 is equal to 1_2.

— After step 30) the value of the bit 14 of MDIO register 3.519 is equal to 1_2.

— After step 31) the value of the bit 15 of MDIO register 3.519 is equal to 1_2.

— After step 33) the value of the bit 13 of MDIO register 3.519 is equal to 0_2.

— After step 34) the value of the bit 14 of MDIO register 3.519 is equal to 0_2.

— After step 35) the value of the bit 15 of MDIO register 3.519 is equal to 0_2.

7.8.14.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.15 PMAT_8: State diagrams – PHD monitor

7.8.15.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.5 and Figures 115-25, 115-26 and 115-27.

7.8.15.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.5.5.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.15.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.15.4 Discussion

Some of the internal variables of the PHD monitor state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

This test case needs two MDIO registers reads per transmit block.

7.8.15.5 Test configuration

Not applicable.

7.8.15.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

7) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.

8) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.

9) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to NOT_OK.

10) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to NOT_OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

11) The UT monitors MDIO register bit 12 of the MDIO register 3.519 till its value is 1_2.

12) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 0_2.

13) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.

14) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to OK.

15) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

16) The UT monitors MDIO register bit 11 of the MDIO register 3.519 till its value is 1_2.

17) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

18) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 1_2.

19) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to OK.

20) The UT sets the transmit block generator to transmit continuously a transmit block with all symbols set to zeros, without any pilots nor header.

21) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.

22) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to NOT_OK.

23) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

24) The UT monitors MDIO register bit 11 of the MDIO register 3.519 till its value is 1_2.

25) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

26) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 1_2.

27) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to OK.

28) The UT sets the transmit block generator to transmit a single transmit block with all symbols set to zero, except the subsections corresponding to pilots S1 and S2; followed by a continuous sequence of normal transmit blocks with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

29) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 1_2.

30) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

31) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 1_2.

32) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to OK.

33) The UT sets the transmit block generator to transmit two transmit block with all symbols set to zeros, but the subsections devoted to pilot transmission S1 and S2 followed by an infinite number of normal transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

34) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.

35) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.

36) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.HDRSTATUS is set to NOT_OK.

7.8.15.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The results of the check specified in step 7) are all OK.

— The results of the check specified in step 8) are all OK.

— The results of the check specified in step 9) are all OK.

— After step 11) the value of the bit 12 of the MDIO register 1.0 is equal to 1_2.

— The results of the check specified in step 12) are all OK.

— The results of the check specified in step 13) are all OK.

— The results of the check specified in step 14) are all OK.

— After step 16) the value of the bit 11 of the MDIO register 1.0 is equal to 1_2.

— The results of the check specified in step 17) are all OK.

— The results of the check specified in step 18) are all OK.

— The results of the check specified in step 19) are all OK.

— The results of the check specified in step 21) are all OK.

— The results of the check specified in step 22) are all OK.

— After step 24) the value of the bit 11 of the MDIO register 1.0 is equal to 1_2.

— The results of the check specified in step 25) are all OK.

— The results of the check specified in step 26) are all OK.

— The results of the check specified in step 27) are all OK.

— The results of the check specified in step 29) are all OK.

— The results of the check specified in step 30) are all OK.

— The results of the check specified in step 31) are all OK.

— The results of the check specified in step 32) are all OK.

— The results of the check specified in step 34) are all OK.

— The results of the check specified in step 35) are all OK.

— The results of the check specified in step 36) are all OK.

7.8.15.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.16 PMAT_9: State diagrams – Adaptive THP TX

7.8.16.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.2 and Figure 115-28.

7.8.16.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.16.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.16.4 Discussion

Some of the internal variables of the adaptive THP TX state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

This test case needs two MDIO registers reads per transmit block.

7.8.16.5 Test configuration

Not applicable.

7.8.16.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001$_2$ to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes the MDIO register bit 11 of the MDIO register 1.0 with 0_2.
7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
   i) PHD.TX.NEXT.MODE is set to 0_2.
   ii) PHD.RX.HDRSTATUS is set to NOT_OK.
   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

8) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.

9) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.TX.NEXT.SETID is set to 0_2.

10) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

11) The UT waits till THP coefficients are calculated in the transmit block analyser with help from the test coordination procedure if necessary. The test coordination procedure stores them in the TBA_COEF variable.

12) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 1_2.

vi) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF.

13) When the last symbol of the first transmit block is transmitted, capture the first two consecutive complete transmit blocks transmitted by the IUT in the transmit block analyser.

14) The test coordination procedure checks that the first captured transmit block has the PHD.TX.REQ.NEXT.SETID header field equal to 1_2.

15) The test coordination procedure checks that the first captured transmit block has not the payload data precoded with the TBA_COEF.

16) The test coordination procedure checks that the second captured transmit block has the PHD.TX.REQ.NEXT.SETID header field equal to 1_2.

17) The test coordination procedure checks that the second captured transmit block has the payload data precoded with the TBA_COEF.

18) The UT waits till THP coefficients are calculated in the transmit block analyser with help from the test coordination procedure if necessary. The test coordination procedure stores them in the TBA_COEF_2 variable.

19) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 2.

vi) PHD.RX.REQ.THP.COEF[8:0] is set to TBA_COEF_2.

20) When the last symbol of the first transmit block is transmitted, capture in the transmit block analyser the first two consecutive complete transmit blocks transmitted by the IUT.

21) The test coordination procedure checks that the first captured transmit block has the PHD.TX.REQ.NEXT.SETID header field equal to 2.

22) The test coordination procedure checks that the first captured transmit block has the payload data precoded with the TBA_COEF.

23) The test coordination procedure checks that the second captured transmit block has the PHD.TX.REQ.NEXT.SETID header field equal to 2.

24) The test coordination procedure checks that the second captured transmit block has the payload data precoded with the TBA_COEF_2.

7.8.16.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The results of the check specified in step 8) are all OK.

— The results of the check specified in step 9) are all OK.

— The results of the check specified in step 14) are all OK.

— The results of the check specified in step 15) are all OK.

— The results of the check specified in step 16) are all OK.

— The results of the check specified in step 17) are all OK.

— The results of the check specified in step 21) are all OK.

— The results of the check specified in step 22) are all OK.

— The results of the check specified in step 23) are all OK.

— The results of the check specified in step 24) are all OK.

7.8.16.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.17 PMAT_10: State diagrams – Adaptive THP request

7.8.17.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.3 and Figure 115-29.

7.8.17.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.17.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.17.4 Discussion

Some of the internal variables of the adaptive THP REQ state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

This test case needs two MDIO registers reads per transmit block.

7.8.17.5 Test configuration

Not applicable.

7.8.17.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
    i) PHD.TX.NEXT.MODE is set to 0_2.
    ii) PHD.RX.HDRSTATUS is set to NOT_OK.
    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

8) The UT monitors MDIO register bit 12 of the MDIO register 3.519 till its value is 1_2.

9) The test coordination procedure checks that MDIO register bit 11 of the MDIO register 3.519 is equal to 0_2.

10) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.

11) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 0_2.

12) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.REQ.THP.SETID is set to 0_2.

13) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

14) The UT monitors MDIO register bit 10 of the MDIO register 3.519 till its value is 1_2.

15) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 0_2.

16) The UT captures one transmit block in the transmit block analyser. The test coordination procedure checks if the PHD field PHD.RX.REQ.THP.SETID is set to 1_2.

17) If the check performed after 16) is OK, the test coordination procedure continues with next step. If not, it returns to 16).

18) The test coordination procedure checks that the PHD fields PHD.RX.REQ.THP.COEF[8:0] are set to values different from zero, and store then in the IUT_COEF_1 variable.

19) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 0_2.

20) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 1_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

21) When the last symbol of the first transmit block is transmitted, reset t_delay, a timer with resolution of at least 1 µs.

22) The UT monitors MDIO register bit 9 of the MDIO register 3.519 till its value is 1_2.

23) The test coordination procedure stops t_delay. The test coordination procedure checks that the value is lower than 1 042,116 9 µs and higher than 347,372 3 µs.

24) The UT captures one transmit block in the transmit block analyser. The test coordination procedure checks if the PHD field PHD.RX.REQ.THP.SETID is set to 2.

25) If the check performed after 24) is OK, the test coordination procedure continues with next step. If not, it returns to 26).

26) The test coordination procedure checks that the PHD fields PHD.RX.REQ.THP.COEF[8:0] are set to values different from zero, and store then in the IUT_COEF_2 variable.

27) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 1_2.

28) The UT captures one transmit block in the transmit block analyser. The test coordination procedure checks if the PHD field PHD.RX.REQ.THP.SETID is set to 3.

29) If the check performed after 29) is OK, the test coordination procedure continues with the next step. If not, it returns to 29).

30) The test coordination procedure checks that the PHD fields PHD.RX.REQ.THP.COEF[8:0] are set to values different from zero, and store then in the IUT_COEF_3 variable.

31) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 1_2.

32) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to NOT_OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 1_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

33) The UT monitors MDIO register bit 11 of the MDIO register 3.519 till its value is 0_2.

34) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

35) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.

36) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 0_2.

37) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.REQ.THP.SETID is set to 0_2.

7.8.17.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 8) the value of the bit 12 of MDIO register 3.518 is equal to 1_2.

— The results of the check specified in step 9) are all OK.

— The results of the check specified in step 10) are all OK.

— The results of the check specified in step 11) are all OK.

— The results of the check specified in step 12) are all OK.

— After step 14) the value of the bit 10 of MDIO register 3.518 is equal to 1_2.

— The results of the check specified in step 15) are all OK.

— The results of the check specified in step 17) are all OK.

— The results of the check specified in step 18) are all OK.

— The results of the check specified in step 19) are all OK.

— After step 22) the value of the bit 9 of MDIO register 3.518 is equal to 1_2.

— The results of the check specified in step 23) are all OK.

— The results of the check specified in step 25) are all OK.

— The results of the check specified in step 26) are all OK.

— The results of the check specified in step 27) are all OK.

— The results of the check specified in step 29) are all OK.

— The results of the check specified in step 30) are all OK.

— The results of the check specified in step 31) are all OK.

— After step 33) the value of the bit 11 of MDIO register 3.518 is equal to 0_2.

— The results of the check specified in step 34) are all OK.

— The results of the check specified in step 35) are all OK.

— The results of the check specified in step 36) are all OK.

— The results of the check specified in step 37) are all OK.

7.8.17.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.18 PMAT_11: State diagrams – Quality monitor state diagram

7.8.18.1 Purpose

This test case verifies that the IUT performs correctly the transitions of the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.7.4 and Figure 115-30.

7.8.18.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.7.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.18.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.18.4 Discussion

Some of the internal variables of the adaptive THP REQ state diagram are checked indirectly, by testing the expected behaviour in the system. Other stages and control variables are monitored via MDIO registers.

This test case needs two MDIO registers reads per transmit block.

In this test case the link reliability is controlled by means of the precoding coefficients. When the test case uses the correct precoding coefficients, the link is reliable. On the other hand, when the test case uses other precoding coefficients, the link is not reliable.

7.8.18.5 Test configuration

Not applicable.

7.8.18.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes the MDIO register bit 11 of the MDIO register 1.0 with 0_2.
7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
    i) PHD.TX.NEXT.MODE is set to 0_2.
    ii) PHD.RX.HDRSTATUS is set to NOT_OK.
    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
    v) PHD.RX.REQ.THP.SETID is set to 0_2.
8) The test coordination procedure checks that MDIO register bit 10 of the MDIO register 3.519 is equal to 0_2.
9) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.
10) The UT captures a transmit block in the transmit block analyser.
    i) The test coordination procedure checks that the PHD field PHD.RX.RXLINKSTATUS is set to 0_2.

ii) The test coordination procedure checks that the PHD field PHD.RX.RXLINKMARGIN is set to 80_{16}.

11) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

12) The UT captures one transmit block in the transmit block analyser. The test coordination procedure checks if the PHD field PHD.RX.REQ.THP.SETID is set to 1_2.

13) If the check performed after 12) is OK, the test coordination procedure continues with the next step. If not, it returns to 12).

14) The test coordination procedure checks that the PHD fields PHD.RX.REQ.THP.COEF[8:0] are set to values different from zero, and store then in the IUT_COEF_1 variable.

15) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero precoded using the coefficients IUT_COEF_1 to perform the equations in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.1.1 and with the following contents for the header fields:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 1_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

16) The UT monitors MDIO register bit 9 of the MDIO register 3.519 till its value is 1_2.

17) The UT captures one transmit block in the transmit block analyser. The test coordination procedure checks if the PHD field PHD.RX.RXLINKMARGIN is between 00_{16} and $7F_{16}$.

18) If the check performed after 16) is OK, the test coordination procedure continues with the next step. If not, it returns to 16).

19) The test coordination procedure checks that the PHD field PHD.RX.RXLINKSTATUS is OK in the last captured transmit block.

20) The UT monitors MDIO register bit 15 of the MDIO register 3.519 till its value is 1_2.

21) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero. Generate a set of random precoding coefficients and use them in the transmit block generator. The content of the transmit block header fields shall be the following:

i) PHD.TX.NEXT.MODE is set to 0_2.

ii) PHD.RX.HDRSTATUS is set to OK.

iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

iv) PHD.TX.NEXT.THP.SETID is set to 1_2.

v) PHD.RX.REQ.THP.SETID is set to 0_2.

22) The test coordination procedure checks that MDIO register bit 9 of the MDIO register 3.519 is equal to 1_2.

23) The UT captures one transmit block in the transmit block analyser. The test coordination procedure checks if the PHD field PHD.RX.RXLINKMARGIN represents a negative number with the fixed point format specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.8.

24) If the check performed after 23) is OK, the test coordination procedure continues with the next step. If not, it returns to 21).

25) The test coordination procedure checks that the PHD field PHD.RX.RXLINKSTATUS is NOT_OK in the last captured transmit block.

26) The test coordination procedure checks that MDIO register bit 15 of the MDIO register 3.519 is equal to 0_2.

7.8.18.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 1_2.

— The results of the check specified in step 8) are all OK.

— The results of the check specified in step 9) are all OK.

— The results of the check specified in step 10) are all OK.

— The results of the check specified in step 13) are all OK.

— The results of the check specified in step 14) are all OK.

— After step 16) the value of the bit 9 of the MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 18) are all OK.

— The results of the check specified in step 19) are all OK.

— After step 20) the value of the bit 15 of the MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 22) are all OK.

— The results of the check specified in step 24) are all OK.

— The results of the check specified in step 25) are all OK.

— The results of the check specified in step 26) are all OK.

7.8.18.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment, check all optical connections and the POF attenuation of the setup to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.19 PMAT_12: Synchronisation

7.8.19.1 Purpose

This test case verifies that the IUT performs correctly the coarse and fine synchronisation with a transmitter that complies with the maximum clock deviation specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.2.

7.8.19.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.19.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.19.4 Discussion

To check the correct synchronisation, the test first configures test setup 1 (TS_BASE) scheme when the same sampling clock is shared by all the blocks (IUT, transmit block generator and transmit block analyser), and is equal to the nominal one (325 MHz).

Under this situation, the test starts with a high attenuation and the synchronisation is not possible. Then, decreasing the attenuation, the test reaches the point in which the synchronisation is performed.

At this point, the test case gradually changes the sampling frequency of the IUT from the nominal one till 325 MHz + 32,5 kHz. Simultaneously, the sampling frequency in the transmit block generator is decreased at the same pace until it reaches 325 MHz – 32,5 kHz. The synchronisation is obtained in all the range of sampling frequencies.

The test case then gradually decreases the sampling frequency in the IUT from 325 MHz + 32,5 kHz until it reaches 325 MHz – 32,5 kHz. Simultaneously, the sampling frequency in the transmit block generator is increased at the same pace until it reaches 325 MHz +32,5 kHz.

The MDIO is used to access to variable s1_synch and rcvr_clock_lock.

This test case needs two MDIO registers reads per transmit block.

7.8.19.5 Test configuration

Not applicable.

7.8.19.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The test coordination procedure sets the optical attenuation of the POF link ending at IUT receiver to 14 dB.

4) The test coordination procedure sets clock input to IUT (CLOCK_IUT) to nominal sampling frequency (325 MHz).

5) The test coordination procedure sets clock input to transmit block generator (CLOCK_TBG) to nominal sampling frequency (325 MHz).

6) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

7) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

8) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

9) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

10) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

11) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.

12) Decrease optical attenuator in steps of 0,2 dB till MDIO register bit 12 of the MDIO register 3.519 is 1_2. Then, decrease optical attenuator in an additional step of 1 dB.

13) The test coordination procedure sets $k = 1$.

14) Change CLOCK_IUT to 325 MHz + (k × 3,25) kHz.

15) Change CLOCK_TBG to 325 MHz – (k × 3,25) kHz.

16) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 3.0.

17) The test coordination procedure waits 100 ms.

18) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

19) If $k < 10$, the test coordination procedure increases k by 1 and goes to 14). If not, it continues with 20).

20) Decrease k by 1.

21) Change CLOCK_IUT to 325 MHz + (k × 3,25) kHz.

22) Change CLOCK_TBG to 325 MHz – (k × 3,25) kHz.

23) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 3.0.

24) The test coordination procedure waits 100 ms.

25) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

26) If $k < -9$, finish the test. If not, go to 19).

7.8.19.7 Observable results

— After step 6) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 9) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The results of the check specified in step 11) are all OK.

— The results of the check specified in step 18) are all OK in all iterations.

— The results of the check specified in step 25) are all OK in all iterations.

7.8.19.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment before the test, check all optical connections and the POF attenuation of the setup without the optical attenuators to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 and requirements specified in 7.6.2.

7.8.20 PMAT_13: Equalization and BER measurement

7.8.20.1 Purpose

This test case verifies that the IUT performs correctly the equalization algorithm that allows reaching the BER specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 when the system is designed for certain channel type specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.7.

7.8.20.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.6.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.7.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.20.3 Test setup

The TS_AOPRX test setup (see 7.6.17) shall be used.

7.8.20.4 Discussion

This test case verifies that the IUT equalizes a channel with frequency response following the specifications in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.7.1 (Type I), 115.7.2 (Type II) or 115.7.3 (Type III).

The channel type (I, II or III) to be introduced in the test setup TS_AOPRX depends on the supported channel type claimed by the IUT.

In the case the IUT claims to be compliant with more than one channel type, this test case is performed for each of the channel types claimed.

The channel between transmit block generator and IUT are set as specified in 7.6.17 for the selected channel type.

Once the channel is equalized, a BER measurement is performed to check that the required quality level is reached by the link.

7.8.20.5 Test configuration

Not applicable.

7.8.20.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
   i) PHD.TX.NEXT.MODE is set to 0_2.
   ii) PHD.RX.HDRSTATUS is set to NOT_OK.
   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
   v) PHD.RX.REQ.THP.SETID is set to 0_2.
8) The UT reads bit 15 to bit 0 from the MDIO register 3.522.
9) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6.
10) The test coordination procedure sets the local variable ACC_LINK_MARGIN to 0. The test coordination procedure sets local variable $k = 1$.
11) The UT captures a transmit block in the transmit block analyser. The test coordination procedure adds the PHD field PHD.RX.RXLINKMARGIN to the previous value of the local variable ACC_LINK_MARGIN.
12) If $k = 128$, the test coordination procedure continues with step 13). If not, it sets $k = k + 1$ and goes to step 11).
13) The LT sets the optical attenuation of the POF link ending at IUT receiver to (ACC_LINK_MARGIN / 128) - 0,2 dB.
14) The UT captures a transmit block in the transmit block analyser. The test coordination procedure checks that the PHD field PHD.RX.RXLINKSTATUS is set to OK.
15) The UT reads bit 15 to bit 0 from the MDIO register 3.522. The test coordination procedure checks that is equal to 0000_{16}.
16) The test coordination procedure sets local variable $k = 1$.
17) The test coordination procedure waits 60 s.
18) The UT reads bit 15 to bit 0 from the MDIO register 3.521 and store then into the local variable CURR_LINK_MARGIN.

19) If CURR_LINK_MARGIN is not between 0,2 dB and 0,3 dB, the LT increases the optical attenuation of the POF link ending at IUT receiver by (CURR_LINK_MARGIN − 0,2 dB) and the test coordination procedure goes to step 18). Else, it continues with step 20).

20) If $k = 5\,744$, the test coordination procedure goes to step 21). Else, it sets $k = k + 1$ and goes to step 17).

21) The UT reads bit 15 to bit 0 from the MDIO register 3.522. The test coordination procedure checks that is less than or equal to 0023_{16} (35_{10}).

7.8.20.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 8) the value of the bit 15 to bit 0 of MDIO register 3.522 is equal to 0_2.

— After step 9) the value of the bit 13 of MDIO register 3.519 is equal to 1_2.

— The results of the check specified in step 14) are all OK.

— The results of the check specified in step 15) are all OK.

— The results of the check specified in step 21) are all OK.

7.8.20.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

If the link margin is not enough to complete link establishment before the test, check all optical connections and the POF attenuation of the setup without the optical attenuators to meet the channel requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.21 PMDT_1: PMD transmit function – Electrical to optical

7.8.21.1 Purpose

This test case verifies that the IUT performs correctly the PMD transmit function defined as the translation of electrical signals to optical signals. The test setup is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3.

7.8.21.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.21.3 Test setup

The TS_SIGPOW test setup (see 7.6.4, specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3) shall be used.

7.8.21.4 Discussion

Equation 115-30 from ISO/IEC/IEEE 8802-3:2017/Amd 9:2018 specifies the way the electrical signal is translated into optical signal. This test case verifies that the formula is fulfilled. Due to the test mode used in this test, the large area photodiode used to measure the AOP (as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3) measures the optical power in less than 61,5 ns.

7.8.21.5 Test configuration

Not applicable.

7.8.21.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 011_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518 (test mode 3).
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
7) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz.
8) The test coordination procedure stores the maximum optical power value in the local variable P_0 and the minimum optical power value in the local variable P_1.
9) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518 (test mode 5).
10) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
11) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
12) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
13) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz.
14) The test coordination procedure checks that the measured optical power is equal to $(P_0 + P_1) / 2$ at any point of the capture performed in the previous step.

7.8.21.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 011_2.
— After step 9) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.
— After step 14) the check result is OK.

7.8.21.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.22 PMDT_2: PMD transmit function – Power control

7.8.22.1 Purpose

This test case verifies that the IUT can turn on and off the optical power output in transmission by using the PMD_TXPWR.request. As this test case is independent of the optional LPI capability, the IUT is configured to be non-EEE capable.

7.8.22.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.22.3 Test setup

The TS_SIGPOW test setup (see 7.6.4) shall be used.

7.8.22.4 Discussion

PMD_TXPWR.request is generated (as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.1.3.2) whenever the tx_pwr variable changes its value. This event happens when a transition in the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4 Figure 115-32 leads to a state in which tx_pwr changes its previous value. As this test case is independent of optional features like LPI, the IUT is configured to be non-EEE capable. That is, the internal variable lpi_cap is always FALSE. This fact makes possible only to verify the transition from tx_pwr OFF to tx_pwr ON, as the transition of tx_pwr from ON to OFF is only possible in an IUT configured to be EEE capable.

7.8.22.5 Test configuration

The UT shall configure the IUT to be non-EEE capable.

7.8.22.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT reads bit 11 of the MDIO register 1.0.

4) The test coordination procedure checks that the content of bit 11 of the MDIO register 1.0 is 1_2.

5) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 0_2 or that the content of bit 0 of the MDIO register 3.519 is 0_2.

6) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz.

7) The test coordination procedure checks that the measured optical power is lower than AOP_{OFF} (as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8) in all the captures.

8) The UT writes 101_2 to the bit 15 to bit 13 of the MDIO register 3.518.

9) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

10) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

11) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

12) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz.

13) The test coordination procedure checks that the measured AOP matches into the margin specified by the maximum and minimum values of AOP at TP2 in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8 for 1000BASE-RHC and all available samples of the capture performed in the previous step.

7.8.22.7 Observable results

— The result of the check specified in step 4) is OK.

— The result of the check specified in step 6) is OK.

— The result of the check specified in step 8) is OK.

— After step 9) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 12) the value of the bit 11 of the MDIO register 1.0 is equal to 0.

— The result of the check specified in step 14) is OK.

7.8.22.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.23 PMDT_3: PMD receive function – Optical to electrical

7.8.23.1 Purpose

This test case verifies that the IUT converts the received optical power into electrical signal. Moreover, the test case verifies that the IUT controls the effect of optical power reaching the receiver depending on the value of variable rx_pwr as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.3.

7.8.23.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.23.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.23.4 Discussion

PMD_RXPWR.request is generated (as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.1.4.2) whenever the rx_pwr variable changes its value. This event happens when a transition in the state diagram specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4 Figure 115-33 leads to a state in which rx_pwr changes its previous value. As this test case is independent of optional features like EEE

capability, the IUT is configured to be non-EEE capable. That is, the internal variable lpi_cap is always FALSE. This fact makes possible only to verify the transition from rx_pwr OFF to rx_pwr ON, as the transition of rx_pwr from ON to OFF is only possible in an IUT configured to be EEE capable.

7.8.23.5 Test configuration

The UT shall configure the IUT to be non-EEE capable.

7.8.23.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT reads bit 11 of the MDIO register 1.0.
4) The test coordination procedure checks that the content of bit 11 of the MDIO register 1.0 is 1_2.
5) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 0_2 or that the content of bit 0 of the MDIO register 3.519 is 0_2.
6) The UT writes 001_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
7) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
8) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
9) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
    i) PHD.TX.NEXT.MODE is set to 0_2.
    ii) PHD.RX.HDRSTATUS is set to OK.
    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
    v) PHD.RX.REQ.THP.SETID is set to 0_2.
10) Wait the equivalent time to transmit 100 transmit blocks.
11) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 0_2.
12) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
13) Wait the equivalent time to transmit 100 transmit blocks.
14) The test coordination procedure checks that MDIO register bit 12 of the MDIO register 3.519 is equal to 1_2.

7.8.23.7 Observable results

— The result of the check specified in step 4) is OK.
— The result of the check specified in step 6) is OK.
— After step 7) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 001_2.
— The result of the check specified in step 12) is OK.

— The result of the check specified in step 15) is OK.

7.8.23.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.24 PMDT_4: PMD signal detect function

7.8.24.1 Purpose

This test case verifies that the IUT detects the presence of the optical signal at its input following the values given in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.4 and Table 115-7. For this test case, the UT configures the IUT to be non-EEE capable.

7.8.24.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.24.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.8.24.4 Discussion

The IUT detects the presence of optical signal when the AOP of the optical signal is in the range of the value given in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-7, second row. In this test, the internal value of the variable sd_inh (as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.3) is FALSE. In order to guarantee this, the IUT is configured to be not EEE capable (MDIO register 3.518 bit 0, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 45-160c set to 0_2, disable EEE ability).

7.8.24.5 Test configuration

IUT shall be configured to be non-EEE capable.

7.8.24.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT reads bit 11 of the MDIO register 1.0.

4) The test coordination procedure checks that the content of bit 11 of the MDIO register 1.0 is 1_2.

5) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 0_2 or that the content of bit 0 of the MDIO register 3.519 is 0_2.

6) The test coordination procedure sets the optical attenuator in the reception path of the IUT to a value that makes the AOP lower than -35 dBm at IUT TP3.

7) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

   i) PHD.TX.NEXT.MODE is set to 0_2.

   ii) PHD.RX.HDRSTATUS is set to OK.

   iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

   iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

   v) PHD.RX.REQ.THP.SETID is set to 0_2.

8) The UT reads the MDIO register 1.10 bit 0.

9) The test coordination procedure checks that the read value is 0_2.

10) The test coordination procedure sets the optical attenuator in the reception path of the IUT to a value that makes the AOP equal to a value in the range of -28,5 dBm to -28,9 dBm at IUT TP3.

11) The UT reads the MDIO register 1.10 bit 0.

12) The test coordination procedure checks that the read value is 1_2.

7.8.24.7 Observable results

— The result of the check specified in step 4) is OK.

— The result of the check specified in step 6) is OK.

— The result of the check specified in step 10) is OK.

— The result of the check specified in step 13) is OK.

7.8.24.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.25 PMD_MDIT_1: Transmitter optical specifications – AOP

7.8.25.1 Purpose

This test case verifies that the IUT fulfils the AOP required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2. The way the measurements are performed is already specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

7.8.25.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.25.3 Test setup

The TS_AOPTX test setup (see 7.6.5) shall be used.

7.8.25.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.25.5 Test configuration

Not applicable.

7.8.25.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.3 shall be fulfilled.

7.8.25.7 Observable results

The measured AOP value complies with the AOP requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.25.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.26 PMD_MDIT_2: Transmitter optical specifications – ER

7.8.26.1 Purpose

This test case verifies that the IUT fulfils the ER required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.26.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.26.3 Test setup

The TS_ER test setup (see 7.6.6) shall be used.

7.8.26.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.26.5 Test configuration

Not applicable.

7.8.26.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.5 shall be fulfilled.

7.8.26.7 Observable results

The measured ER value complies with the ER requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.26.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.27 PMD_MDIT_3: Transmitter optical specifications – Centre wavelength

7.8.27.1 Purpose

This test case verifies that the IUT fulfils the centre wavelength required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.27.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.27.3 Test setup

The TS_CW test setup (see 7.6.7) shall be used.

7.8.27.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.27.5 Test configuration

Not applicable.

7.8.27.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.1 shall be fulfilled.

7.8.27.7 Observable results

The measured centre wavelength value complies with the centre wavelength requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.27.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.28 PMD_MDIT_4: Transmitter optical specifications – Spectral width

7.8.28.1 Purpose

This test case verifies that the IUT fulfils the spectral width required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.28.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.28.3 Test setup

The TS_SW test setup (see 7.6.8) shall be used.

7.8.28.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.28.5 Test configuration

Not applicable.

7.8.28.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.2 shall be fulfilled.

7.8.28.7 Observable results

The measured spectral width value complies with the spectral width requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.28.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.29 PMD_MDIT_5: Transmitter optical specifications – Rise time

7.8.29.1 Purpose

This test case verifies that the IUT fulfils the rise time required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.29.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.29.3 Test setup

The TS_RT_FT test setup (see 7.6.9) shall be used.

7.8.29.4 Discussion

The method to measure the rise time fulfils the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 and fulfils the values specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

7.8.29.5 Test configuration

Not applicable.

7.8.29.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.4 shall be fulfilled.

7.8.29.7 Observable results

The measured rise time value complies with the rise time requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.29.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.30 PMD_MDIT_6: Transmitter optical specifications – Fall time

7.8.30.1 Purpose

This test case verifies that the IUT fulfils the fall time required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.30.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.30.3 Test setup

The TS_RT_FT test setup (see 7.6.9) shall be used.

7.8.30.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.30.5 Test configuration

Not applicable.

7.8.30.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.4 shall be fulfilled.

7.8.30.7 Observable results

The measured fall time value complies with the fall time requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.30.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.31 PMD_MDIT_7: Transmitter optical specifications – Signal overshoot

7.8.31.1 Purpose

This test case verifies that the IUT fulfils the signal overshoot required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.31.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.31.3 Test setup

The TS_OS test setup (see 7.6.10) shall be used.

7.8.31.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.31.5 Test configuration

Not applicable.

7.8.31.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.6 shall be fulfilled.

7.8.31.7 Observable results

The measured signal overshoot value complies with the signal overshoot requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.31.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.32 PMD_MDIT_8: Transmitter optical specifications – Positive output droop

7.8.32.1 Purpose

This test case verifies that the IUT fulfils the positive output droop required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.32.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.32.3 Test setup

The TS_NOD_POD test setup (see 7.6.11) shall be used.

7.8.32.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.32.5 Test configuration

Not applicable.

7.8.32.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.7 shall be fulfilled.

7.8.32.7 Observable results

The measured positive output droop value complies with the positive output droop requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8.

7.8.32.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.33 PMD_MDIT_9: Transmitter optical specifications – Negative output droop

7.8.33.1 Purpose

This test case verifies that the IUT fulfils the negative output droop required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.33.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.33.3 Test setup

The TS_NOD_POD test setup (see 7.6.11) shall be used.

7.8.33.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.33.5 Test configuration

Not applicable.

7.8.33.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.7 shall be fulfilled.

7.8.33.7 Observable results

The measured negative output droop value complies with the negative output droop requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.33.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.34 PMD_MDIT_10: Transmitter optical specifications – Signal distortion

7.8.34.1 Purpose

This test case verifies that the IUT fulfils the signal distortion (2nd, 3rd and 4th order harmonic and residual distortion) required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.34.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.34.3 Test setup

The TS_DIST test setup (see 7.6.12) shall be used.

7.8.34.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.34.5 Test configuration

Not applicable.

7.8.34.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.8 shall be fulfilled.

7.8.34.7 Observable results

The measured signal distortion (2^{nd}, 3^{rd} and 4^{th} order harmonic and residual distortion) value complies with the signal distortion (2^{nd}, 3^{rd} and 4^{th} order harmonic and residual distortion) requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8.

7.8.34.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.35 PMD_MDIT_11: Transmitter optical specifications – Relative intensity noise

7.8.35.1 Purpose

This test case verifies that the IUT fulfils the relative intensity noise required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.35.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.35.3 Test setup

The TS_RIN test setup (see 7.6.13) shall be used.

7.8.35.4 Discussion

The method to measure the relative intensity noise fulfils the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 and fulfils the values specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

7.8.35.5 Test configuration

Not applicable.

7.8.35.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.10 shall be fulfilled.

7.8.35.7 Observable results

The measured relative intensity noise value complies with the relative intensity noise requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.35.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.36 PMD_MDIT_12: Transmitter optical specifications – Transmitter off transition time

7.8.36.1 Purpose

This test case verifies that the IUT reaches the transmission quiet mode in less than the off-transition time t_{OFF}.

7.8.36.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.36.3 Test setup

The TS_EXTEND test setup (see 7.6.3) shall be used.

7.8.36.4 Discussion

The transmission quiet mode is defined as a mode in which the transmitter AOP is lower or equal to AOP_{OFF}, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.

The initial time is considered when the internal variable tx_pwr has a transition from ON to OFF.

The value of the off-transition time t_{OFF} is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.

For this test case, the UT configures the IUT to be EEE capable.

The time between the IUT commands by changing tx_pwr internal variable to switch off the MDI and the time when the AOP reaches the AOP_{OFF} value specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8 is less than the value established for t_{OFF} in the same table.

As the tx_pwr variable is not directly accessible, the test case establishes the link between the IUT and its link partner, and then the IUT enters into LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

At this point, a capture is performed by the transmit block analyser that includes the time when, after the transmission of 130 zeros as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.1, the AOP reaches the AOP_{OFF} value. Then, the test case measures the time from the AOP falls from the 90 % of the AOP_{ZEROS} value to the AOP reaches the AOP_{OFF} value.

All AOP values are measured at TP2.

AOP_{ZEROS} is defined as the AOP measured at TP2 when the transmitter sends a signal x(n) to the PMD equal to zero (see ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.3.1).

The time to be measured t_{OFF} is specified in Figure 17.

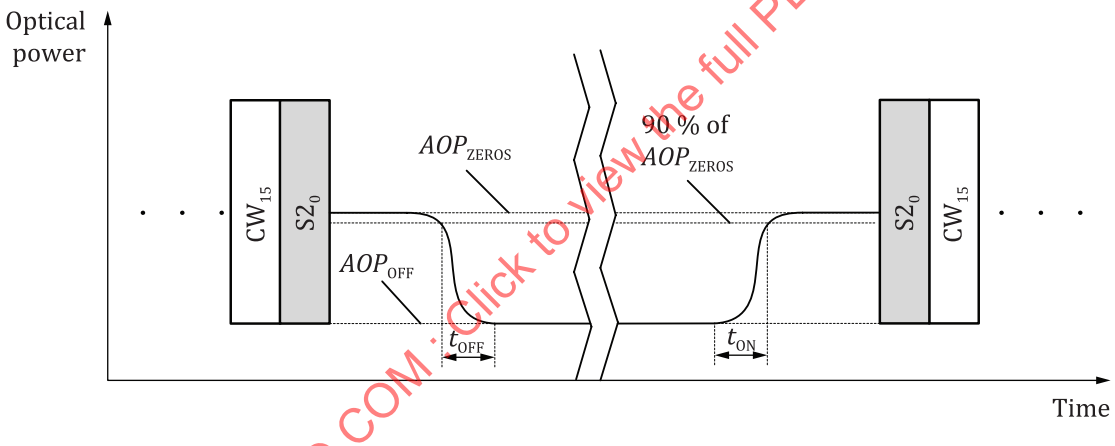


Figure 17 — t_{OFF} and t_{ON} specification for test cases PMD_MDIT_12 and PMD_MDIT_13

7.8.36.5 Test configuration

The UT shall configure the IUT to be EEE capable.

7.8.36.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

7) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz and stores the value in the local variable $AOP_{ZEROS.}$

8) The UT writes 000_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

9) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

10) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

11) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

12) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 1_2 and that the content of bit 0 of the MDIO register 3.519 is 1_2.

13) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to NOT_OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

    vi) PHD.CAP.LPI is set to 1_2.

14) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6. The transmit block generator is programmed to transmit the header fields with the content specified in step 6) of 7.7.6.6 and additionally setting PHD.CAP.LPI to 1_2.

15) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 1_2.

16) The UT sets the GMII station to perform an LPI assert in the GMII by setting GMII.TX_EN to 0, GMII.TX_ER to 1, GMII.TX_DATA to 10_{16} and GMII.CTRL to 10_2.

17) In the transmit block analyser, start capturing the signal from the event of reception of 130 consecutive symbols set to an AOP equal to AOP_{ZEROS}, with a relative tolerance of ±1 %. The capture includes at least 50 symbols.

18) The test coordination procedure calculates the value of t_{OFF} as the time when the signal AOP is the 90 % of AOP_{ZEROS} to the time the first captured symbol has an AOP equal to AOP_{OFF} (specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8). All AOP measurements are performed at TP2.

19) The test coordination procedure checks that the value of t_{OFF} is lower than the value specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.

7.8.36.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 8) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 000_2.

— After step 10) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The result of the check specified in step 12) is OK.

— The result of the check specified in step 15) is OK.

— The result of the check specified in step 19) is OK.

7.8.36.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.37 PMD_MDIT_13: Transmitter optical specifications – Transmitter on transition time

7.8.37.1 Purpose

This test case verifies that the IUT reaches the transmission active mode in less than the on-transition time t_{ON}.

7.8.37.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.2.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.2.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.37.3 Test setup

The TS_EXTEND test setup (see 7.6.3) shall be used.

7.8.37.4 Discussion

The transmission active mode is defined as a mode in which the transmitter AOP reaches the 90 % of AOP_{ZEROS}.

AOP_{ZEROS} is defined as the AOP measured at TP2 when the transmitter sends a signal x(n) to the PMD equal to zero (see ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.3.1).

The initial time is considered when the internal variable tx_pwr has a transition from OFF to ON.

The value of the off-transition time t_{ON} is specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.

For this test case, the UT configures the IUT to be EEE capable.

The time between the IUT commands by changing tx_pwr internal variable to switch on the MDI and the time when the AOP reaches the 90 % of AOP_{ZEROS} value is less than the value established for t_{ON} in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.

As the tx_pwr variable is not directly accessible, the test case establishes the link between the IUT and its link partner, and then the IUT enters into LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4. Then, the IUT returns to normal operation from the LPI mode.

At this point, a capture is performed by the transmit block analyser that includes the time when, after the transmission of 130 zeros as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.1, the transmission returns to active mode. Then, the test coordination procedure measures the time from the AOP at TP2 rise from the AOP_{OFF} value to the time when the AOP at TP2 reaches the 90 % of the AOP_{ZEROS} value.

All AOP values are measured at TP2.

Figure 17 specifies the time t_{ON}.

7.8.37.5 Test configuration

The UT shall configure the IUT to be EEE capable.

7.8.37.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0 with
7) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz and stores the value in the local variable AOP_{ZEROS}.
8) The UT writes 000_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
9) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
10) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
11) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
12) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 1_2 and that the content of bit 0 of the MDIO register 3.519 is 1_2.
13) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:
    i) PHD.TX.NEXT.MODE is set to 0_2.
    ii) PHD.RX.HDRSTATUS is set to NOT_OK.
    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.
    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.
    v) PHD.RX.REQ.THP.SETID is set to 0_2.
    vi) PHD.CAP.LPI is set to 1_2.
14) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6. The transmit block generator is programmed to transmit the header fields with the content specified in step 6) of 7.7.6.6 and additionally setting PHD.CAP.LPI to 1_2.
15) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 1_2.
16) The UT sets the GMII station to perform an LPI assert in the GMII by setting GMII.TX_EN to 0, GMII.TX_ER to 1, GMII.TX_DATA to 10_{16} and GMII.CTRL to 10_2.
17) The test coordination procedure waits 2 s.
18) The UT sets the GMII station to transmit continuously a bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two

values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

19) In the transmit block analyser, the UT starts capturing the signal from the event of reception of 130 consecutive symbols set to an AOP equal to AOP_{ZEROS}, with a relative tolerance of ±1 %. The capture includes at least a time equivalent to twice the t_{ON} specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8 before the event of reception of 130 consecutive symbols set to zero.

20) The test coordination procedure calculates the value of t_{ON} as the time when the signal starts to be higher than AOP_{OFF} to the time the first transmitted symbol has an AOP equal to the 90 % of AOP_{ZEROS}. All AOP measurements are performed at TP2.

21) The test coordination procedure checks that the value of t_{ON} is lower than the value specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8.

7.8.37.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 8) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 000_2.

— After step 11) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The result of the check specified in step 12) is OK.

— The result of the check specified in step 15) is OK.

— The result of the check specified in step 21) is OK.

7.8.37.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.38 PMD_MDIT_14: Transmitter optical specifications – Modal power distribution

7.8.38.1 Purpose

This test case verifies that the IUT fulfils the modal power distribution required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.38.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.38.3 Test setup

The TS_MPD test setup (see 7.6.14) shall be used.

7.8.38.4 Discussion

The method to measure the modal power distribution fulfils the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.11 and fulfils the values specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

7.8.38.5 Test configuration

Not applicable.

7.8.38.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.11 shall be fulfilled.

7.8.38.7 Observable results

The measured modal power distribution value complies with the modal power distribution requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-9.

7.8.38.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.39 PMD_MDIT_15: Transmitter optical specifications – Timing jitter

7.8.39.1 Purpose

This test case verifies that the IUT fulfils the timing jitter required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 and Table 115-8 measured in TP2.

7.8.39.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.39.3 Test setup

The TS_TJ test setup (see 7.6.15) shall be used.

7.8.39.4 Discussion

This test case performs the measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.9 to verify that the obtained value is compliant to ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.8.39.5 Test configuration

Not applicable.

7.8.39.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.9 shall be fulfilled.

7.8.39.7 Observable results

The measured timing jitter value complies with the timing jitter requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.1 Table 115-8.

7.8.39.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.40 PMD_MDIT_16: Receiver optical specifications – AOP for a minimum BER

7.8.40.1 Purpose

This test case verifies that the IUT fulfils the maximum allowable BER when the AOP at TP3 is in the range specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 and Table 115-10 for all channel types specified for 1000BASE-RHC. Receiver boundary conditions are also fulfilled as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.4.

7.8.40.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.40.3 Test setup

The TS_2LP test setup (see 7.6.16) shall be used.

7.8.40.4 Discussion

The method to measure the AOP measured at TP3 for all channel types specified for 1000BASE-RHC fulfils the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 and 115.6.3.4 and fulfils the values specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

For the minimum and maximum AOP at TP3 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-10 for the 1000BASE-RHC and the two fibre optic channels (type II and type III), the IEEE 802.3bv physical layer provides a BER less than 10^{-12} operating in test mode 1 as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

7.8.40.5 Test configuration

Not applicable.

7.8.40.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 shall be followed, taking into account the receiver boundary condition test specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.4.

7.8.40.7 Observable results

The measured minimum and maximum AOP complies with the minimum and maximum AOP requirements as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3 and Table 115-10 when the reliability of the link complies with the values given in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

7.8.40.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.41 PMD_MDIT_17: Receiver optical specifications – Damage threshold power

7.8.41.1 Purpose

This test case verifies that the IUT fulfils the damage threshold power required in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-10, Note a. Receiver boundary conditions are also fulfilled as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.4.

7.8.41.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.41.3 Test setup

The TS_2LP test setup (see 7.6.16) shall be used.

7.8.41.4 Discussion

The procedure to measure the damage threshold power (defined as the maximum AOP plus 1 dB) measured at TP3 fulfils the specification in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 and 115.6.3.4 and fulfils the values specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.3.

The IEEE 802.3bv physical layer tolerates, without damage, continuous exposure to the damage threshold power at TP3 specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-10.

7.8.41.5 Test configuration

Not applicable.

7.8.41.6 Test procedure steps

The measurement procedure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.4 shall be followed, taking into account the receiver boundary condition test specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.6.3.4.

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The test coordination procedure performs PMD_MDIT_16 test case specified in 7.8.40.
2) The test coordination procedure checks that the result of the test case is OK.
3) The test coordination procedure sets the AOP at TP3 to the damage threshold power during one hour.
4) The test coordination procedure performs PMD_MDIT_16 test case specified in 7.8.40.
5) The test coordination procedure checks that the result of the test case is OK.

7.8.41.7 Observable results

— The result of the check specified in step 2) is OK.

— The result of the check specified in step 5) is OK.

7.8.41.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.8.42 DLYT_1: Transmission plus reception delay

7.8.42.1 Purpose

This test case verifies the delay from the time when a bit pattern sequence sent over the IUT GMII transmission interface (GTX_CLK, TXD<7:0>, TX_EN and TX_ER in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-3) to the time when the same bit pattern sequence is received is lower than 6,5 µs.

7.8.42.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.13.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.8.42.3 Test setup

The TS_LOOP test setup (see 7.6.18) shall be used.

7.8.42.4 Discussion

ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115 to 13 specifies the maximum delay allowed for the addition of data transmission and reception time, measured when MDI (TX) and MDI (RX) interfaces are connected with each other in the same IUT. This test case verifies that this maximum delay is not reached.

7.8.42.5 Test configuration

Not applicable.

7.8.42.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 000_2 to the MDIO register bit 12 to bit 10 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

7) The UT waits till the MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2 (link status = OK).

8) The UT sets the GMII station to transmit a single bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA alternating between two values, being the first $5A_{16}$ and the second $A5_{16}$, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2.

9) Synchronously with the transmission of the first GMII transaction, the test coordination procedure resets to zero the t_delay internal timer and starts it.

10) The UT waits till the reception of the first GMII transaction that corresponds with the transmitter bit pattern sequence of step 8) by watching the GMII.RX_EN line.

11) The test coordination procedure stops the t_delay timer.

12) The test coordination procedure checks that the t_delay timer value is less than 6,5 µs.

7.8.42.7 Observable results

— After step 3) the value of the bit 12 to bit 10 of the MDIO register 3.518 is equal to 000_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 7) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

— The result of the check specified in step 12) is OK.

7.8.42.8 Remarks

Check that the GMII interface cables are correctly attached.

This test case requires that the GMII station is capable of a single bit pattern sequence. Check that the station used fulfils this feature.

7.9 Block 3 test cases: Optional functionality

7.9.1 General

This subclause specifies the test cases covering the optional functionality of ISO/IEC/IEEE 8802-3:2017/Amd 9:2018.

7.9.2 to 7.9.5 specify the test cases covering the optional EEE functionality.

7.9.6 to 7.9.8 specify the test cases covering the optional OAM channel functionality.

7.9.9 to 7.9.13 specify the test cases covering the optional wake-up and synchronised link sleep functionality.

7.9.2 EEET_1: Enter to LPI mode transmit operation

7.9.2.1 Purpose

This test case verifies that the IUT enters properly into LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 and that the structure of the transmit block when entering the LPI mode matches the structure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Figure 115-31.

7.9.2.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.9.2.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.9.2.4 Discussion

Several LPI-related requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 are tested.

First, the LPI mode is performed only if both the IUT and the link partner are LPI capable and this capability is announced in the CAP.LPI field of the physical header as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4 and Table 115-6.

The synchronisation between the assert LPI generated as a GMII transaction in the GMII transmission interface, and the moment when the LPI mode has its effect in the transmit block are checked in this test.

Finally, the correct structure of the transmit block once the LPI mode is activated is also checked, including the refresh periods.

AOP_{ZEROS} is defined as the AOP measured at TP2 when the transmitter sends a signal x(n) to the PMD equal to zero (see ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.3.1).

7.9.2.5 Test configuration

The UT shall configure the IUT to be EEE capable.

7.9.2.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

7) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz and stores the value in the local variable AOP_{ZEROS}.

8) The UT writes 000_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

9) The UT writes 1_2 to the MDIO register bit 0 of the MDIO register 3.518.

10) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 1_2 and that the content of bit 0 of the MDIO register 3.519 is 1_2.

11) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

12) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

13) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

14) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to NOT_OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

    vi) PHD.CAP.LPI is set to 1_2.

15) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6. The transmit block generator is programmed to transmit the header fields with the content specified in step 6) of 7.7.6.6 and additionally setting PHD.CAP.LPI to 1_2.

16) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 1_2.

17) The UT sets the GMII station to perform an LPI assert in the GMII by setting continuously GMII.TX_EN to 0, GMII.TX_ER to 1. GMII.TX_DATA to 10_{16} and GMII.CTRL to 10_2.

18) The UT captures the transmit block transmitted by the IUT in the transmit block analyser. The capture is triggered by the event of a transition between the measurement at TP2 of 130 symbols set to an AOP equal to AOP_{ZEROS}, with a relative tolerance of ±1 %, and the drop of the average output power to a value lower than AOP_{OFF}, specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8. The capture includes at least (2 × 160) + 130 symbols before the event that triggers the capture.

19) The test coordination procedure checks that in the obtained capture the 160 symbols before the transmission of the 130 contiguous symbols set to zero correspond to one of the three possibilities:

    i) A pilot S1 as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.1.

    ii) A pilot S2 as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.2.

    iii) A physical header as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3

20) The test coordination procedure checks that the AOP before the 160 symbols analysed in the previous step measured in at least 160 symbols is greater than AOP_{OFF}.

21) The test coordination procedure checks that after the trigger and during 7 644 symbols the AOP is lower than AOP_{OFF}.

22) The test coordination procedure checks that after 7 644 symbols from the trigger 130 symbols with an AOP equal to AOP_{ZEROS} follow.

23) The test coordination procedure checks that after 7 774 symbols from the trigger the following 160 symbols correspond to one of the three possibilities:

    i) A pilot S1 as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.1.

    ii) A pilot S2 as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2.2.

    iii) A physical header as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.3

24) The test coordination procedure checks that the 160 symbols detected in 23) follow the transmit block structure specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.2.2 taking into account the previously received 160 symbols of step 19).

25) The test coordination procedure checks that after 7 934 symbols from the trigger, 130 symbols with an AOP equal to AOP_{ZEROS} follow.

26) The test coordination procedure checks that after 8 064 symbols from the trigger, 7 644 symbols with an AOP is lower than AOP_{OFF} follow.

7.9.2.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 8) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 000_2.

— After step 12) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The result of the check specified in step 10) is OK.

— The result of the check specified in step 16) is OK.

— The result of the check specified in step 19) is OK.

— The result of the check specified in step 20) is OK.

— The result of the check specified in step 21) is OK.

— The result of the check specified in step 22) is OK.

— The result of the check specified in step 23) is OK.

— The result of the check specified in step 24) is OK.

— The result of the check specified in step 25) is OK.

— The result of the check specified in step 26) is OK.

7.9.2.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.9.3 EEET_2: EEE capability exchange

7.9.3.1 Purpose

This test case verifies that the IUT enters into LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 only when both, the link partner and the IUT, have active the EEE capability and it is properly announced in the IUT header.

7.9.3.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.9.3.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.9.3.4 Discussion

In the case that the EEE option is supported, the IUT enters into the LPI mode, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4, only when the link partner supports also the EEE option and it is properly announced in the correspondent header field as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4 and Table 115-6.

This test case covers the situation in which the link partner does not support (or does not announce) the LPI mode, and verifies the transparent transmission of LPI asserts in this case, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

7.9.3.5 Test configuration

The UT shall configure the IUT to be EEE capable.

7.9.3.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
7) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz and stores the value in the local variable AOP_{ZEROS}.
8) The UT writes 000_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.
9) The UT writes 1_2 to the MDIO register bit 0 of the MDIO register 3.518.

10) The test coordination procedure checks that the content of bit 0 of the MDIO register 3.518 is 1_2 and that the content of bit 0 of the MDIO register 3.519 is 1_2.

11) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

12) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

13) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

14) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to NOT_OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

    vi) PHD.CAP.LPI is set to 0_2.

15) The UT performs the link establishment using THP between IUT and transmit block analyser as in step 6) of 7.7.6.6. The transmit block generator are programmed to transmit the header fields with the content specified in step 6) of 7.7.6.6 and additionally setting PHD.CAP.LPI to 0_2.

16) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 0_2.

17) The UT sets the GMII station to perform an LPI assert in the GMII by setting continuously GMII. TX_EN to 0, GMII.TX_ER to 1, GMII.TX_DATA to 10_{16} and GMII.CTRL to 10_2.

18) The UT captures the transmit block transmitted by the IUT in the transmit block analyser. The capture is triggered by the event of a transition between the measurement at TP2 of 130 symbols set to an AOP equal to AOP_{ZEROS}, with a relative tolerance of ±1 %, and the drop of the average output power to a value lower than AOP_{OFF}, specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Table 115-8. The capture includes at least (2 × 160) + 130 symbols before the event that triggers the capture.

19) The test coordination procedure checks that the capture based on the trigger specified in 17) never occurs.

20) The UT sets the transmit block generator to transmit continuously a transmit block with payload data equal to zero and with the following contents for the header fields:

    i) PHD.TX.NEXT.MODE is set to 0_2.

    ii) PHD.RX.HDRSTATUS is set to NOT_OK.

    iii) PHD.RX.RXLINKSTATUS is set to NOT_OK.

    iv) PHD.TX.NEXT.THP.SETID is set to 0_2.

    v) PHD.RX.REQ.THP.SETID is set to 0_2.

    vi) PHD.CAP.LPI is set to 1_2.

21) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 1_2.

22) The UT captures the transmit block transmitted by the IUT in the transmit block analyser. The capture is triggered by the event of a transition between the measurement at TP2 of 130 symbols set to an AOP equal to AOP_{ZEROS}, with a relative tolerance of ±1 %, and the drop of the average output power to a value lower than AOP_{OFF}, specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018,

Table 115-8. The capture includes at least (2 × 160) + 130 symbols before the event that triggers the capture.

23) The test coordination procedure checks that the capture based on the trigger specified in 22) is performed.

24) The test coordination procedure checks that the PHD.CAP.LPI header field from the transmit block captured in step 22) is equal to 1.

7.9.3.7 Observable results

— After step 3) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 101_2.

— After step 6) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 8) the value of the bit 15 to bit 13 of the MDIO register 3.518 is equal to 000_2.

— The result of the check specified in step 10) is OK.

— After step 13) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— The result of the check specified in step 16) is OK.

— The result of the check specified in step 19) is OK.

— The result of the check specified in step 21) is OK.

— The result of the check specified in step 23) is OK.

— The result of the check specified in step 24) is OK.

7.9.3.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.9.4 EEET_3: Loop test for LPI mode

7.9.4.1 Purpose

This test case verifies that the IUT that enters into LPI mode continues the normal reception of GMII transactions when normal operation is resumed. Moreover, this test case checks that the assert LPI transactions are transparently transmitted independently of the value of the remote EEE ability bit located in bit 2 of the MDIO register 3.519.

7.9.4.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.9.4.3 Test setup

The TS_LOOP test setup (see 7.6.18) shall be used.

7.9.4.4 Discussion

When the EEE option is supported, the IUT enters into the LPI mode, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 and resumes normal mode after the LPI mode.

Independently of the value of the remote EEE ability bit located in bit 2 of the MDIO register 3.519, the LPI assert GMII transactions are transmitted transparently.

This test case uses an optical loopback to check that all GMII transactions both normal and LPI asserts are forwarded transparently.

The IUT can be configured to be EEE capable and non-EEE capable.

7.9.4.5 Test configuration

Not applicable.

7.9.4.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.
2) The test coordination procedure waits 100 ms.
3) The UT writes the MDIO register bit 0 of the MDIO register 3.518 with 0_2.
4) The UT writes 0_2 to the MDIO register bit 15 of the MDIO register 1.0.
5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.
6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.
7) The UT waits till the MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2.
8) The test coordination procedure checks that the GMII interface is transmitting idle transactions (TX_EN = 0_2; TX_ER = 0_2).
9) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 0_2.
10) The UT sets the GMII station to continuously transmit LPI assert by setting GMII.TX_EN to 0, GMII. TX_ER to 1, GMII.TX_DATA to 10_{16} and GMII.CTRL to 10_2.
11) The test coordination procedure checks that the GMII station receives LPI asserts as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.
12) The test coordination procedure sets the internal variable COUNTER to 00_{16}.
13) The UT sets the GMII station to transmit continuously bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with first GMII.TX_DATA being equal to COUNTER, the second (COUNTER + 1) module 256 and so on, reaching to the last that is (COUNTER + 1 517) module 256, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2. Each time a complete bit pattern sequence is transmitted, COUNTER is increased by 1.
14) The test coordination procedure checks that the GMII station receives continuously the bit pattern sequences transmitted by the GMIII station.
15) The UT writes 1_2 to the MDIO register bit 0 of the MDIO register 3.518.

16) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

17) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

18) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

19) The UT waits till the MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2.

20) The test coordination procedure checks that the GMII interface is transmitting idle transactions (TX_EN = 0_2; TX_ER = 0_2).

21) The test coordination procedure checks that the content of bit 2 of the MDIO register 3.519 is 1_2.

22) The UT sets the GMII station to perform an LPI assert in the transmission GMII by setting GMII. TX_EN to 0_2, GMII.TX_ER to 1_2. GMII.TX_DATA to 10_{16} and GMII.CTRL to 10_2.

23) The test coordination procedure checks that the GMII station receives LPI asserts.

24) The test coordination procedure sets the internal variable COUNTER to 00_{16}.

25) The UT sets the GMII station to transmit continuously bit pattern sequence consisting of a preamble (seven transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = 55_{16} followed by a transaction with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA = $D5_{16}$), 1 518 transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with first GMII.TX_DATA being equal to COUNTER, the second (COUNTER + 1) module 256 and so on, reaching to the last that is (COUNTER + 1 517) module 256, four transactions with GMII.TX_EN = 1_2 GMII.TX_ER = 0_2 with GMII.TX_DATA being the four octets resulting of the CRC calculation of the previous 1 518 octets as specified in ISO/IEC/IEEE 8802-3:2017, 3.29 and 12 idle transactions with GMII.TX_EN = 0_2. Each time a complete bit pattern sequence is transmitted, COUNTER is increased by 1.

26) The test coordination procedure checks that the GMII station receives continuously the same bit pattern sequences transmitted by the GMII station.

7.9.4.7 Observable results

— After step 3) the value of the bit 0 of the MDIO register 3.518 is equal to 0_2.

— After step 7) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

— The result of the check specified in step 8) is OK.

— The result of the check specified in step 9) is OK.

— The result of the check specified in step 11) is OK.

— The result of the check specified in step 14) is OK.

— After step 15) the value of the bit 0 of the MDIO register 3.518 is equal to 1_2.

— After step 18) the value of the bit 11 of the MDIO register 1.0 is equal to 0_2.

— After step 19) the value of the bit 2 of the MDIO register 1.1 is equal to 1_2.

— The result of the check specified in step 20) is OK.

— The result of the check specified in step 21) is OK.

— The result of the check specified in step 23) is OK.

— The result of the check specified in step 26) is OK.

7.9.4.8 Remarks

If the MDIO station cannot write correctly into the IUT, check the MDIO cable connections.

7.9.5 EEET_4: Resume from LPI mode transmit operation

7.9.5.1 Purpose

This test case verifies that the IUT resumes properly from LPI mode as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 and that normal communication of bit pattern sequences is possible after the resume from LPI mode.

7.9.5.2 Test case references

The following clauses and subclauses of the referred documents are relevant for this test case:

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.3.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 35.

— ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, Clause 45.

7.9.5.3 Test setup

The TS_BASE test setup (see 7.6.2) shall be used.

7.9.5.4 Discussion

When the EEE option is supported, the IUT resumes from the LPI mode, as specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4.

In this test, the synchronisation between the moment when the assert LPI generated as a GMII transaction in the GMII transmission interface is substituted by a normal GMII transaction, and the moment when the normal mode is resumed is checked. The requirements specified in ISO/IEC/IEEE 8802-3:2017/Amd 9:2018, 115.4 are also fulfilled.

7.9.5.5 Test configuration

The UT shall configure the IUT to be EEE capable.

7.9.5.6 Test procedure steps

The test coordination procedure by means of UT and LT shall perform the following test procedure steps:

1) The UT powers up the IUT.

2) The test coordination procedure waits 100 ms.

3) The UT writes 101_2 to the MDIO register bit 15 to bit 13 of the MDIO register 3.518.

4) The UT writes 1_2 to the MDIO register bit 15 of the MDIO register 1.0.

5) The UT waits till the MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

6) The UT writes 0_2 to the MDIO register bit 11 of the MDIO register 1.0.

7) The UT captures the measured optical power at TP2 during at least 250 ns with a sampling frequency of 325 MHz and stores the value in the local variable AOP_{ZEROS}.

