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Road vehicles — In-vehicle Ethernet —

Part 2: Common physical entity requirements

Véhicules routiers — Ethernet embarqué —

Partie 2: Exigences de l'entité physique commune

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21111 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The ISO 21111 series includes in-vehicle Ethernet requirements and test plans that are disseminated in other International Standards and complements them with additional test methods and requirements. The resulting requirement and test plans are structured in different documents following the Open Systems Interconnection (OSI) reference model and grouping the documents that depend on the physical media and bit rate used.

In general, the Ethernet requirements are specified in ISO/IEC/IEEE 8802-3. The ISO 21111 series provides supplemental specifications (e.g. wake-up, I/O functionality), which are required for in-vehicle Ethernet applications. In road vehicles, Ethernet networks are used for different purposes requiring different bit-rates. Currently, the ISO 21111 series specifies the 1-Gbit/s optical and 100-Mbit/s electrical physical layer.

The ISO 21111 series contains requirement specifications and test methods related to the in-vehicle Ethernet. This includes requirement specifications for physical layer entity (e.g. connectors, physical layer implementations) providers, device (e.g. electronic control units, gateway units) suppliers, and system (e.g. network systems) designers. Additionally, there are test methods specified for conformance testing and for interoperability testing.

Safety (electrical safety, protection, fire, etc.) and electromagnetic compatibility (EMC) requirements are out of the scope of the ISO 21111 series.

The structure of the specifications given in the ISO 21111 series complies with the Open Systems Interconnection (OSI) reference model specified in ISO/IEC 7498-1[1] and ISO/IEC 10731[5].

ISO 21111-1 defines the terms which are used in this series of standards and provides an overview of the standards for in-vehicle Ethernet including the complementary relations to ISO/IEC/IEEE 8802-3, the document structure, type of physical entities, in-vehicle Ethernet specific functionalities and so on.

ISO 21111-2 specifies the interface between reconciliation sublayer and physical entity including reduced gigabit media independent interface (RGMII), and the common physical entity wake-up and synchronised link sleep functionalities, independent from physical media and bit rate.

This document specifies supplemental requirements to a physical layer capable of transmitting 1-Gbit/s over plastic optical fibre compliant with ISO/IEC/IEEE 8802-3, with specific application to communications inside road vehicles, and a test plan for physical entity conformance testing.

ISO 21111-4 specifies the optical components requirements and test methods for 1-Gbit/s optical in-vehicle Ethernet.

ISO 21111-5 specifies, for 1-Gbit/s optical in-vehicle Ethernet, requirements on the physical layer at system level, requirements on the interoperability test set-ups, the interoperability test plan that checks the requirements for the physical layer at system level, requirements on the device-level physical layer conformance test set-ups, and device-level physical layer conformance test plan that checks a set of requirements for the OSI physical layer that are relevant for device vendors.

ISO 21111-6 specifies advanced features of an ISO/IEC/IEEE 8802-3 in-vehicle Ethernet physical layer (often also called transceiver), e.g. for diagnostic purposes for in-vehicle Ethernet physical layers. It specifies advanced physical layer features, wake-up and sleep features, physical layer test suite, physical layer control requirements and conformance test plan, physical sublayers test suite and physical sublayers requirements and conformance test plan.

ISO 21111-7 specifies the implementation for ISO/IEC/IEEE 8802-3:2017/Amd 1:2017, which defines the interface implementation for automotive applications together with requirements on components used to realize this Bus Interface Network (BIN). ISO 21111-7 also defines further testing and system requirements for systems implemented according to the system specification. In addition, ISO 21111-7 defines the channels for tests of transceivers with a test wiring harness that simulates various electrical communication channels.

ISO 21111-8 specifies the transmission media, the channel performance and the tests for ISO/IEC/IEEE 8802-3 in-vehicle Ethernet.

ISO 21111-9 specifies the data link layer requirements and conformance test plan. It specifies the requirements and test plan for devices and systems with bridge functionality.

ISO 21111-10 specifies the application to network layer requirements and test plan. It specifies the requirements and test plan for devices and systems that include functionality related with OSI layers from 3 to 7.

Figure 1 shows the parts of the ISO 21111 series and the document structure.

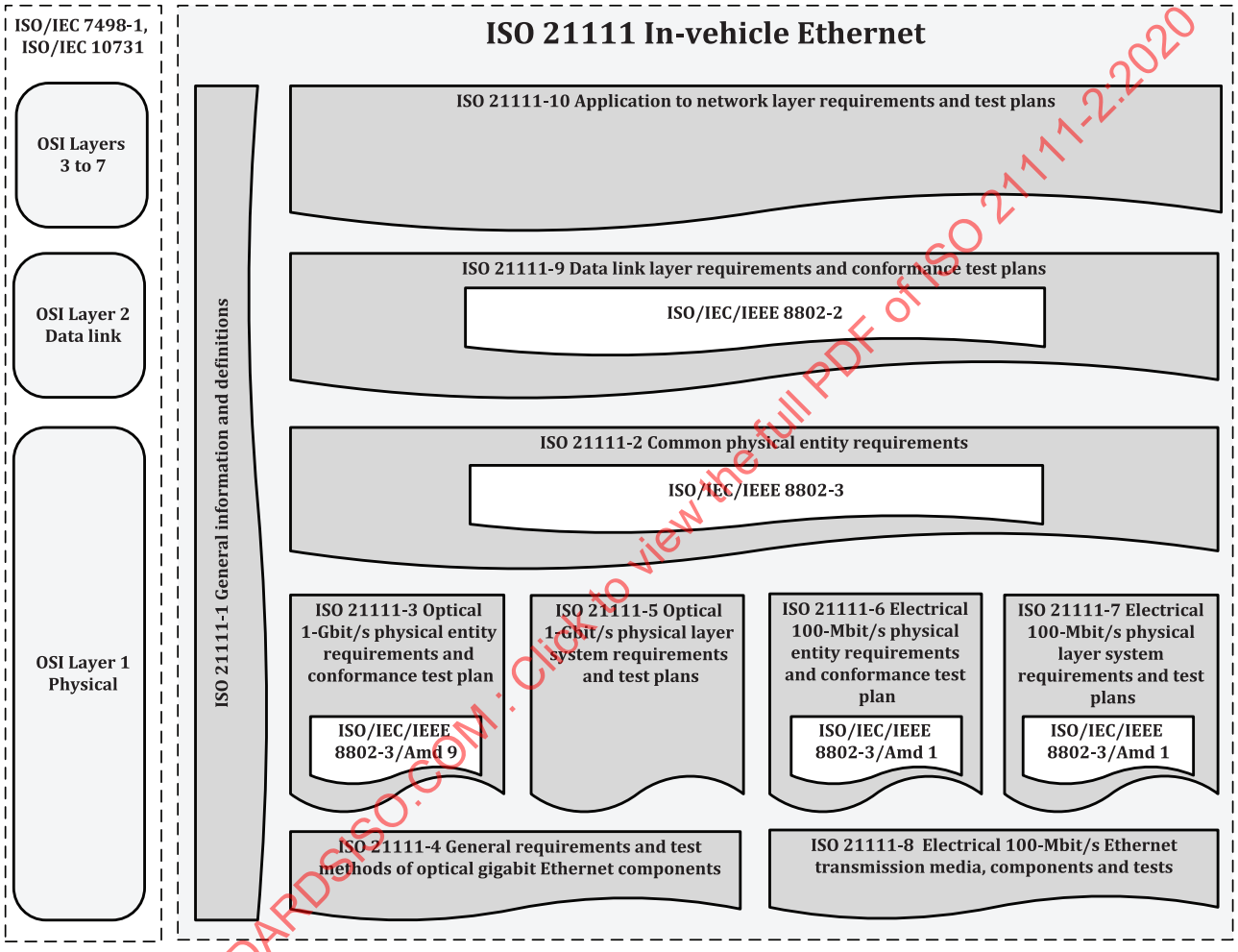

Figure 1 — In-vehicle Ethernet document reference according to the OSI model

Road vehicles — In-vehicle Ethernet —

Part 2:
Common physical entity requirements

1 Scope

This document specifies the following items to complement ISO/IEC /IEEE 8802-3:

— interface between reconciliation sublayer and physical entity including reduced gigabit media independent interface (RGMII);

— common physical entity wake-up and synchronised link sleep functionalities independent from physical media and transmission bit rate.

The optical and electrical component requirements and test methods for optical and electrical transmission of in-vehicle Ethernet are not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21111-1, *Road vehicles — In-vehicle Ethernet — Part 1: General information and definitions*

JEDEC – JESD8C.01:2006, *Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits*

JEDEC – JESD8-5A:2006, *2.5 V ± 0.2 V (Normal Range) and 1.8 V – 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*

JEDEC – JESD8-7A:1997, *1.8 V ± 0.15 V (Normal Range) and 1.2 V – 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21111-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1
double data rate
DDR
data transmission scheme, in which the data is transferred on both the rising and falling edges of the clock signal

3.2
event
piece of management information exchanged between a calling physical entity and a called physical entity

4 Abbreviated terms

DoD delay on destination

DoS delay on source

GMII gigabit media independent interface

I/O input and output

MAC media access control

MDC management data clock

MDIO management data input/output

MII media independent interface

N/A not applicable

PHY physical layer

RGMII reduced gigabit media independent interface

RTBI reduced ten-bit interface

RX receiver

TX transmitter

5 Media independent interfaces

5.1 General

ISO/IEC/IEEE 8802-3 specifies several speed-specific interfaces which are recommended for the communication between the reconciliation sub-layer and the PCS sub-layer. Two of the recommended interfaces are MII, used for10-Mbit/s and 100-Mbit/s capable physical entities, and GMII for 1-Gbit/s capable physical entities.

ISO/IEC/IEEE 8802-3:2017, Clause 22 specifies MII and ISO/IEC/IEEE 8802-3:2017, Clause 35 specifies GMII.

GMII signals, TXD and RXD, as specified in ISO/IEC/IEEE 8802-3:2017, Clause 35 are 8-bits wide. A direct mapping of the TXD or RXD 8-bits wide signals of the GMII interface into eight electrical lines is a drawback for some implementations. A mapping from GMII signals to a reduced set of electrical lines is specified in 5.2.

5.2 RGMII

5.2.1 General

The RGMII architecture (see Figure 2) is composed by the mapping of the GMII interface into a reduced set of signal lines, the reduced set of signal lines, and the de-mapping from the reduced set of signal lines into the GMII interface. In this subclause RGMII signal lines are the reduced set of signal lines in Figure 2.

The RGMII transmitter side adapter shall adapt the GMII signals to the RGMII signal lines in the reconciliation sub-layer side. The RGMII receiver side adapter shall adapt the RGMII signal lines to the GMII signals in the PCS sub-layer side.

5.2.2 specifies the RGMII signal lines. Each RGMII signal line is able to transmit an electrical signal. 5.2.3 specifies the RGMII electrical signal voltage levels and 5.2.4 specifies the RGMII electrical signal timing. 5.2.5 specifies how the GMII signals shall be mapped to the RGMII signal lines and vice versa.

All signals transmitted in an electrical signal line shall be conveyed with positive logic except if it is specified differently.

An electrical signal line shall be at logic high when it is at a voltage level greater than certain threshold. This threshold depends on the RGMII signal line nominal voltage.

An electrical signal line shall be at logic low when it is at a voltage level lower than certain threshold. This threshold depends on the RGMII signal line nominal voltage.

JEDEC - JESD8C.01:2006 shall be used for the thresholds for RGMII signal line voltage of 3,3 V.

JEDEC - JESD8-5A:2006 shall be used for the thresholds for RGMII signal line voltage of 2,5 V.

JEDEC - JESD8-7A:1997 shall be used for the thresholds for RGMII signal line voltage of 1,8 V.

5.2.2 RGMII signals

Figure 2 shows the architecture of the RGMII interface.

The RGMII is a full-duplex bidirectional interface and transfers data simultaneously in both directions. The RGMII connects the upper GMII and the lower GMII interfaces by means of adapters, which convert GMII signals to RGMII signals and vice versa.

The signals of each of the interfaces are grouped by the signal flow direction. The signals going in a downward direction in Figure 2 compose the transmit path, and the signals going in an upward direction compose the receive path. The transmitter side adapter is the signal source in the RGMII transmit path and the receiver side adapter is the signal source in the RGMII receive path.

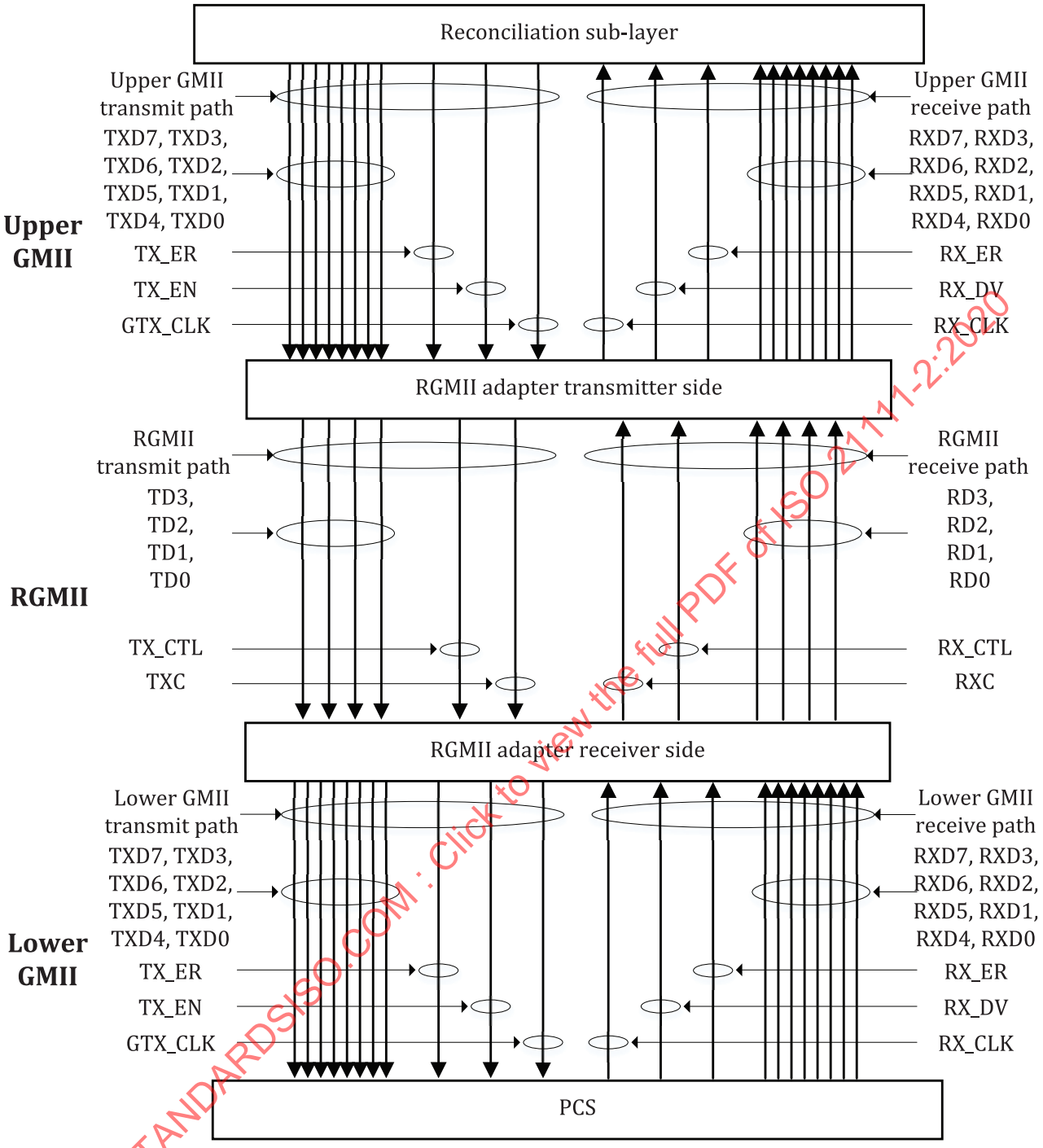

Figure 2 — RGMII architecture

Table 1 specifies the conversion of the GMII signals to the RGMII signals in the transmit path at the transmit side. The signals in the column "RGMII adapter internal signals" are only available inside the adapter and are used to convert the GMII signals. All GMII electrical signals are only valid during the rising edge of the GTX_CLK signal, whereas the RGMII adapter internal signals are valid during both edges of the A_TXC signal.

Table 1 — Conversion table for adapter at transmit side in transmit path

GMII signal	RGMII adapter internal signal		RGMII signal	Remark
	TXC rising edge	TXC falling edge		
GTX_CLK	A_TXC		TXC	N/A
TX_EN	A_TXEN	N/A	TX_CTL	A_TXEN=TX_EN
TX_ER	N/A	A_TXERR		A_TXERR=TX_EN xor TX_ER
TXD7	N/A	A_TD7	TD3	N/A
TXD6	N/A	A_TD6	TD2	N/A
TXD5	N/A	A_TD5	TD1	N/A
TXD4	N/A	A_TD4	TD0	N/A
TXD3	A_TD3	N/A	TD3	N/A
TXD2	A_TD2	N/A	TD2	N/A
TXD1	A_TD1	N/A	TD1	N/A
TXD0	A_TD0	N/A	TD0	N/A

Table 2 specifies the conversion of the RGMII signals to GMII signals in the transmit path at the receiver side. The signals in the column "RGMII adapter internal signal" are only available inside the adapter.

Table 2 — Conversion table for adapter at receiver side in transmit path

RGMII signal	RGMII adapter internal signal		GMII signal	Remark
	TXC rising edge	TXC falling edge		
TXC	A_TXC		GTX_CLK	N/A
TX_CTL	A_TXEN	N/A	TX_EN	TX_EN=A_TXEN
	N/A	A_TXERR	TX_ER	TX_ER=A_TXEN xor A_TXERR
TD3	A_TD3	N/A	TXD3	N/A
	N/A	A_TD7	TXD7	N/A
TD2	A_TD2	N/A	TXD2	N/A
	N/A	A_TD6	TXD6	N/A
TD1	A_TD1	N/A	TXD1	N/A
	N/A	A_TD5	TXD5	N/A
TD0	A_TD0	N/A	TXD0	N/A
	N/A	A_TD4	TXD4	N/A

Table 3 specifies the conversion of the GMII signals to RGMII signals in the receive path at the receiver side. The signals in the column "RGMII adapter internal signal" are only available inside the adapter.

Table 3 — Conversion table for adapter at receiver side in receive path

GMII signal	RGMII adapter internal signal		RGMII signal	Remark
	TXC rising edge	TXC falling edge		
RX_CLK	A_RXC		RX_CLK	N/A
RX_DV	A_RXDV	N/A	TX_CTL	A_RXDV=RX_DV
RX_ER	N/A	A_RXERR		A_RXERR=RX_DV xor RX_ER
RXD7	N/A	A_RD7	RD3	N/A
RXD6	N/A	A_RD6	RD2	N/A
RXD5	N/A	A_RD5	RD1	N/A
RXD4	N/A	A_RD4	RD0	N/A
RXD3	A_RD3	N/A	RD3	N/A

Table 3 *(continued)*

GMII signal	RGMII adapter internal signal		RGMII signal	Remark
	TXC rising edge	TXC falling edge		
RXD2	A_RD2	N/A	RD2	N/A
RXD1	A_RD1	N/A	RD1	N/A
RXD0	A_RD0	N/A	RD0	N/A

Table 4 specifies the conversion of the RGMII signals to GMII signals in the receive path at the transmitter side. The signals in the column "RGMII adapter internal signal" are only available inside the adapter.

Table 4 — Conversion table for adapter at transmitter side in receive path

RGMII signal	RGMII adapter internal signal		GMII signal	Remark
	TXC rising edge	TXC falling edge		
RXC	A_TXC		GTX_CLK	N/A
RX_CTL	A_RXDV	N/A	RX_DV	RX_DV=A_RXDV
	N/A	A_RXERR	RX_ER	RX_ER=A_RXDV xor A_RXERR
RD3	A_RD3	N/A	RXD3	N/A
	N/A	A_RD7	RXD7	N/A
RD2	A_RD2	N/A	RXD2	N/A
	N/A	A_RD6	RXD6	N/A
RD1	A_RD1	N/A	RXD1	N/A
	N/A	A_RD5	RXD5	N/A
RD0	A_RD0	N/A	RXD0	N/A
	N/A	A_RD4	RXD4	N/A

5.2.3 Electrical signal voltage level

Figure 3 specifies RGMII electrical signal voltage levels.

The RGMII electrical signal nominal voltage level of a RGMII signal line shall be at least one of these values: 1,8 V, 2,5 V or 3,3 V.

The 100 % value shown in Figure 3 is the RGMII electrical signal nominal voltage level of a RGMII signal line. All electrical signal voltage levels in this document are scaled with the RGMII electrical signal nominal voltage level.

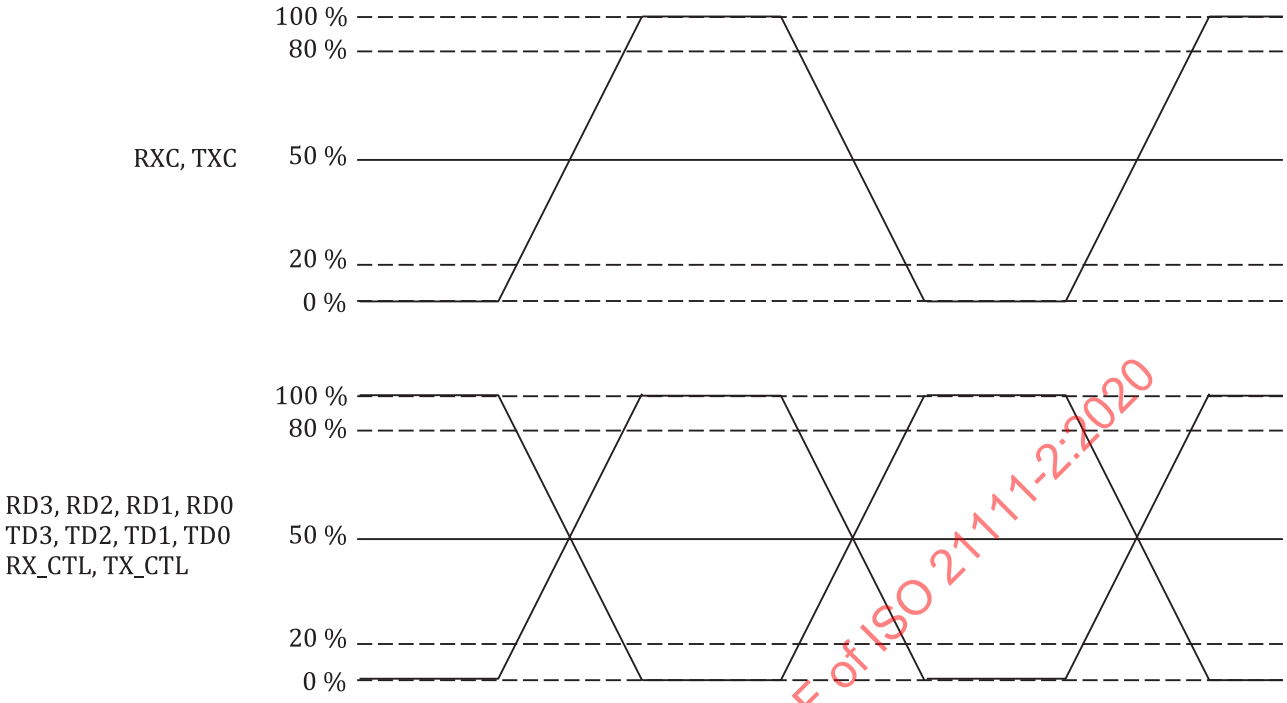

Figure 3 — RGMII electrical signal voltage level

5.2.4 Electrical signal timing

5.2.4.1 Signal delay mode

The electrical signals transmitted through the RGMII signal lines use the DDR data transfer scheme. The clock electrical signal is delayed with respect to the rest of the electrical signals transmitted in the data interface. This delay is defined as delay mismatch.

The electrical interconnection between source and destination of TX_CTL, TX_TD0 to TX_TD3 signal lines shall have a maximum delay mismatch of 150 ps. The electrical interconnection between source and destination of RX_CTL, RX_RD0 to RX_RD3 signal line shall have a maximum delay mismatch of 150 ps.

Depending on the electrical signal direction specified in Table 1, the source is either the RGMII reconciliation sub-layer side or the RGMII PCS sub-layer side, in the same way, the destination side is either the RGMII reconciliation sub-layer side or the RGMII PCS sub-layer side.

The RGMII shall support the following two signal delay modes.

— Delay on destination (DoD): all electrical signals in the data interface are transmitted edge aligned. The delay mismatch of the clock signal shall be accomplished by the destination side. The electrical signal parameters in DoD mode are specified in 5.2.4.2.

— Delay on source (DoS): the source side already provides the delay mismatch of the clock signal. The electrical signal parameters in DoS mode are specified in 5.2.4.3.

5.2.4.2 Electrical signal timing parameters in DoD mode

Figures 4 and 5, and Tables 5 and 6 define electrical signal timing in DoD mode.

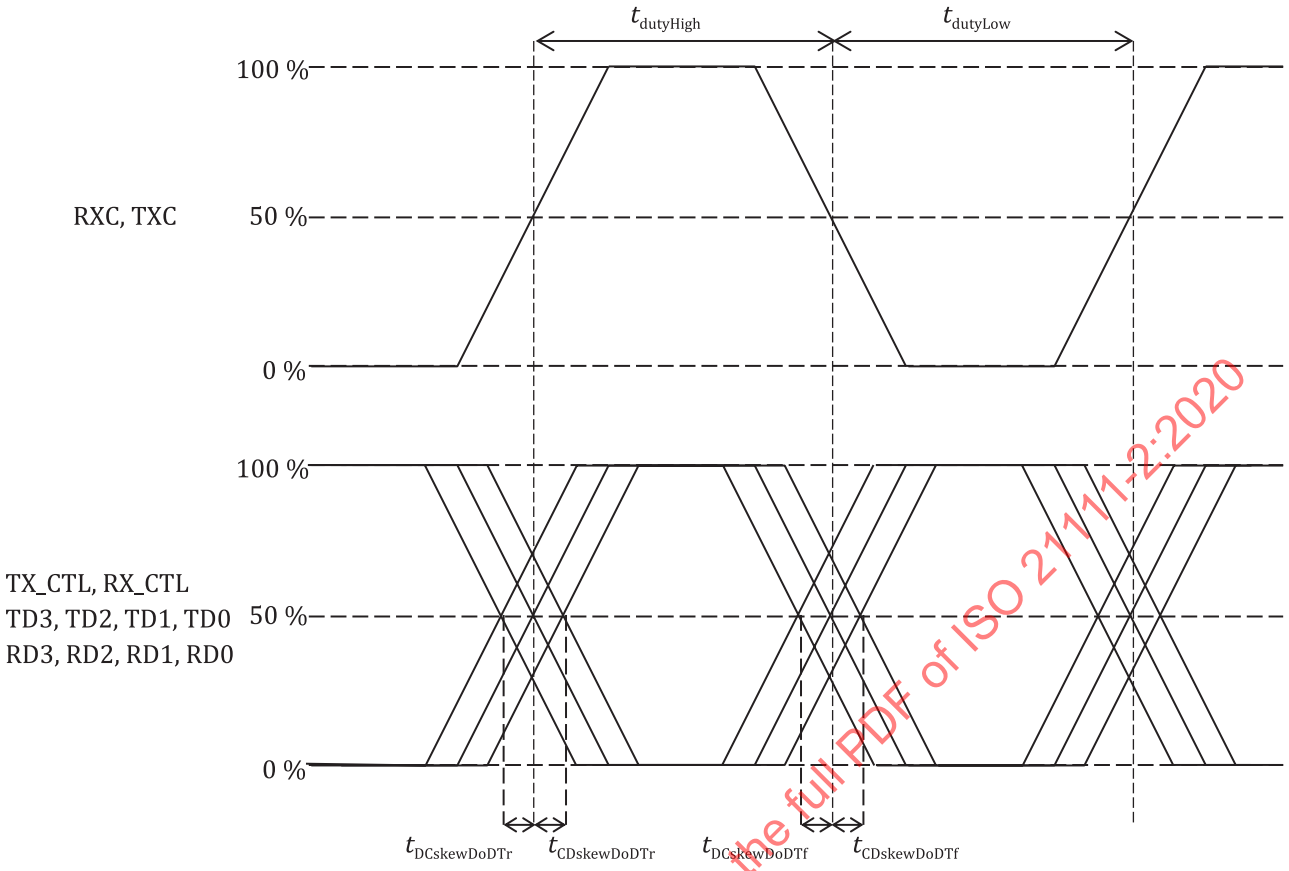

Figure 4 — Electrical signal timing parameters at source side in DoD mode

Table 5 — Duty cycle and skews at source side in DoD mode

Symbol	Parameter name	Minimum value (ns)	Maximum value (ns)
$t_{dutyHigh}$	clock duty cycle high minimum time	3,6	N/A
$t_{dutyLow}$	clock duty cycle low minimum time	3,6	N/A
$t_{DCskewDoDTr}$	data to clock skew in DoD mode at signal source rising edge	N/A	0,5
$t_{CDskewDoDTr}$	clock to data skew in DoD mode at signal source rising edge	N/A	0,5
$t_{DCskewDoDTf}$	data to clock skew in DoD mode at signal source falling edge	N/A	0,5
$t_{CDskewDoDTf}$	clock to data skew in DoD mode at signal source falling edge	N/A	0,5

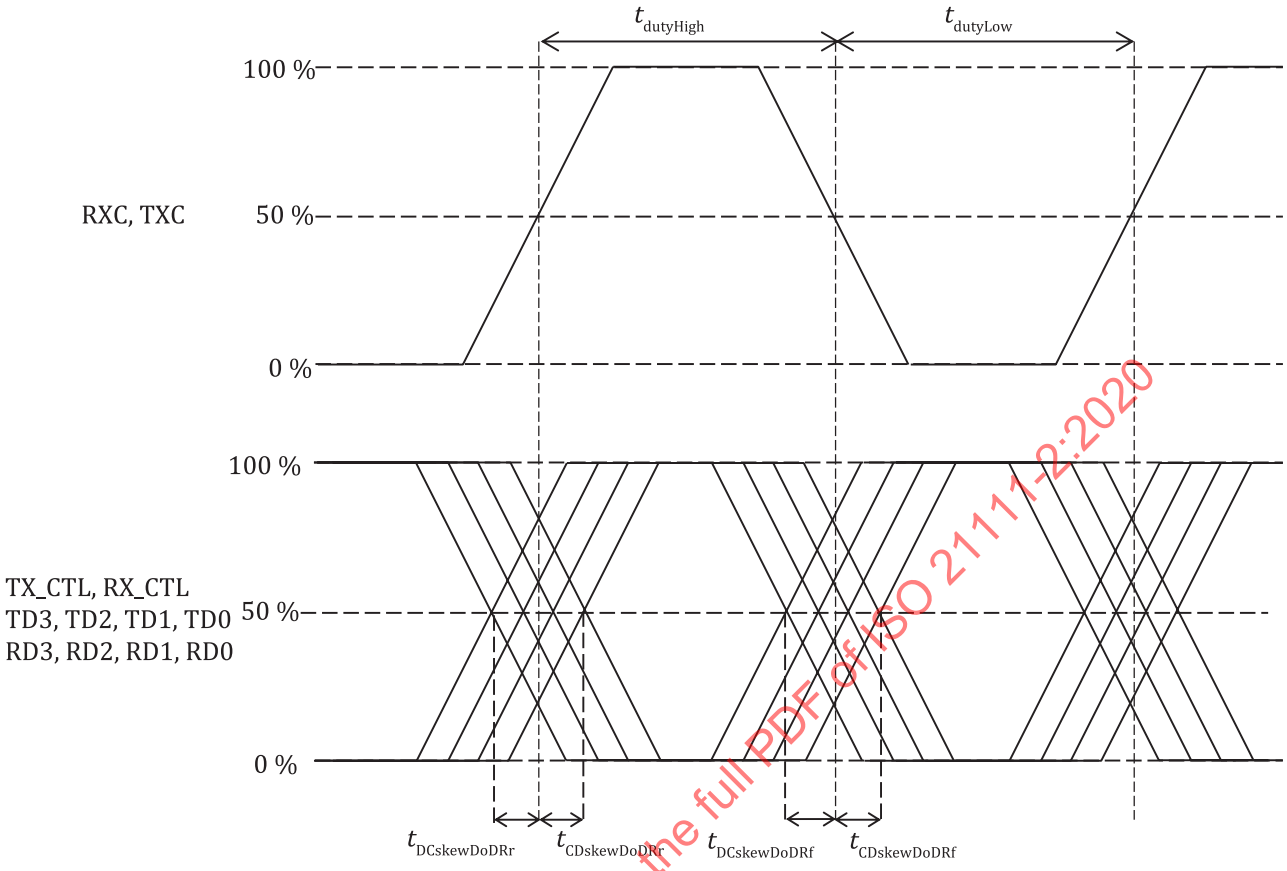

Figure 5 — Electrical signal timing and skews at destination side in DoD mode

Table 6 — Duty cycle and skews at destination side in DoD mode

Symbol	Parameter name	Minimum value (ns)	Maximum value (ns)
$t_{dutyHigh}$	clock duty cycle high minimum time	3,6	N/A
$t_{dutyLow}$	clock duty cycle low minimum time	3,6	N/A
$t_{DCskewDoDRr}$	data to clock skew in DoD mode at signal destination rising edge	N/A	0,65
$t_{CDskewDoDRr}$	clock to data skew in DoD mode at signal destination rising edge	N/A	0,65
$t_{DCskewDoDRf}$	data to clock skew in DoD mode at signal destination falling edge	N/A	0,65
$t_{CDskewDoDRf}$	clock to data skew in DoD mode at signal destination falling edge	N/A	0,65

5.2.4.3 Electrical signal timing parameters in DoS mode

Figures 6 and 7, and Tables 7 and 8 define electrical signal timing in DoS mode.

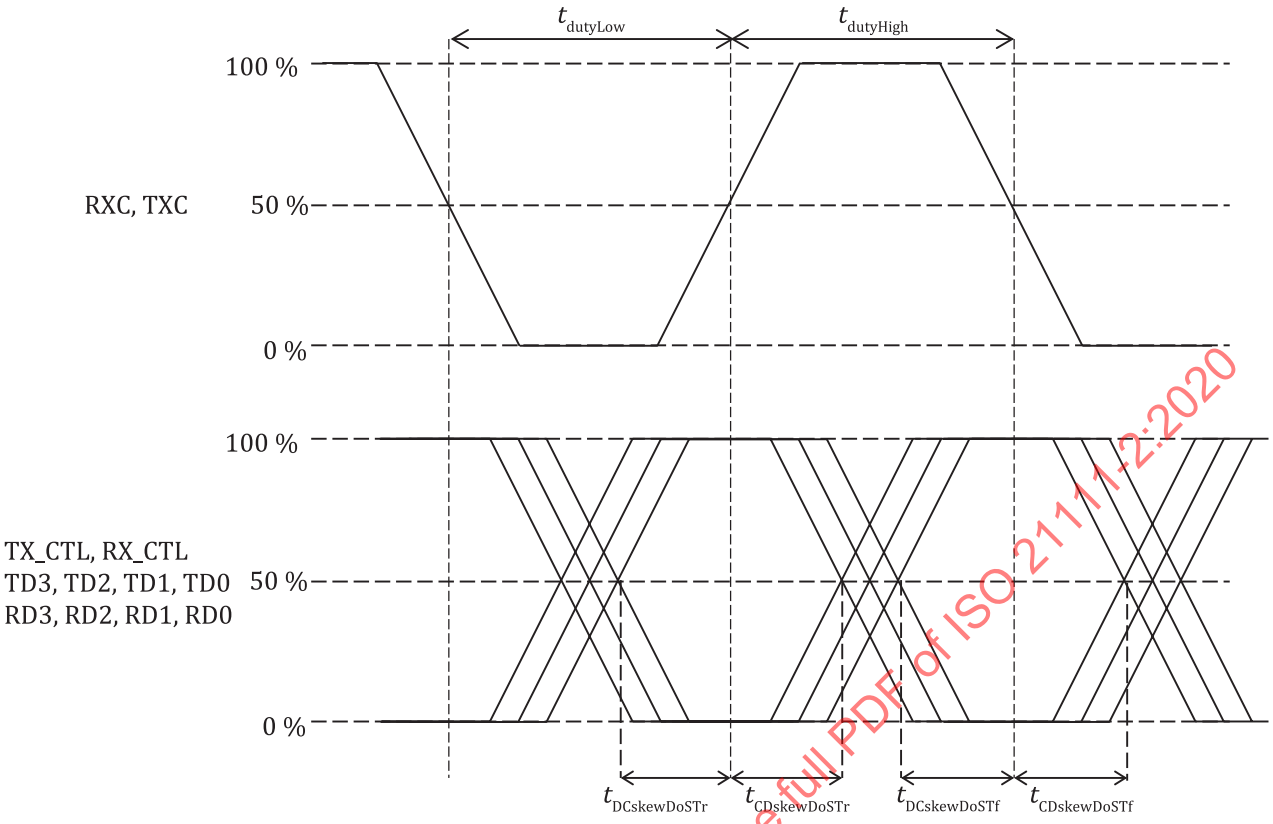

Figure 6 — Electrical signal timing parameters at source side in DoS mode

Table 7 — Duty cycle and skews at source side in DoS mode

Symbol	Parameter name	Minimum value (ns)	Maximum value (ns)
$t_{dutyHigh}$	clock duty cycle high minimum time	3,6	N/A
$t_{dutyLow}$	clock duty cycle low minimum time	3,6	N/A
$t_{DCskewDoSTr}$	data to clock skew in DoS mode at signal source rising edge	1,2	N/A
$t_{CDskewDoSTr}$	clock to data skew in DoS mode at signal source rising edge	1,2	N/A
$t_{DCskewDoSTf}$	data to clock skew in DoS mode at signal source falling edge	1,2	N/A
$t_{CDskewDoSTf}$	clock to data skew in DoS mode at signal source falling edge	1,2	N/A

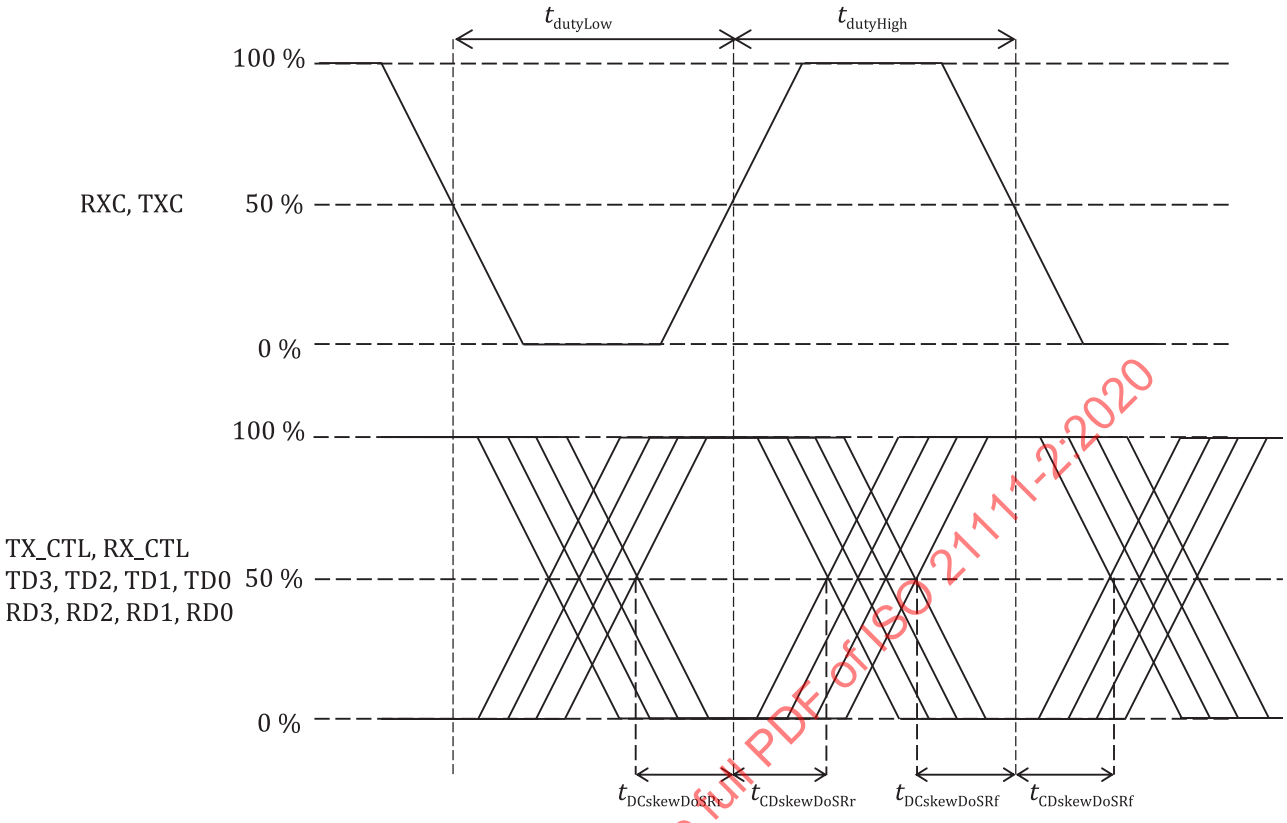

Figure 7 — Electrical signal timing parameters at destination side on DoS mode

Table 8 — Duty cycle and skews at destination side in DoS mode

Symbol	Parameter name	Minimum value (ns)	Maximum value (ns)
$t_{dutyHigh}$	clock duty cycle high minimum time	3,6	N/A
$t_{dutyLow}$	clock duty cycle low minimum time	3,6	N/A
$t_{DCskewDoSRr}$	data to clock skew in DoS mode at signal destination rising edge	1,05	N/A
$t_{CDskewDoSRr}$	clock to data skew in DoS mode at signal destination rising edge	1,05	N/A
$t_{DCskewDoSRf}$	data to clock skew in DoS mode at signal destination falling edge	1,05	N/A
$t_{CDskewDoSRf}$	clock to data skew in DoS mode at signal destination falling edge	1,05	N/A

5.2.4.4 General parameters

Table 9 specifies the other general RGMII parameters.

Table 9 — General RGMII parameters

Symbol	Parameter	Minimum value	Maximum value	Units	Remarks
tR_{max} [a]	maximum signal rise time	N/A	1	ns	from 20 % to 80 %
tF_{max} [a]	maximum signal fall time	N/A	1	ns	from 80 % to 20 %
[a] tR_{max} and tF_{max} are measured for a load of 5 pF at the source side.					

5.2.5 Mapping GMII signals into RGMII electrical signals

In this subclause the mapping of GMII signals into RGMII electrical signals that are transmitted by the RGMII signal lines is specified. The voltage of the RGMII data and control electrical signals is sampled in the rising and in the falling edge of the corresponding reference clock. This technique makes the number of electrical lines used for transmitting the data half, compared with a direct GMII mapping.

TXD<7:0>, TX_ER, TX_EN and TXC are GMII signals as defined in ISO/IEC/IEEE 8802-3:2017, Clause 35. Each of the bits that compose these signals is equal to a logical high or a logical low that is sampled when the TXC signal changes its logical status from logical low to logical high.

RXD<7:0>, RX_ER, RX_DV and RXC are also GMII signals as defined in ISO/IEC/IEEE 8802-3:2017, Clause 35. Each of the bits that compose these signals is equal to a logical high or a logical low that is sampled when the RXC signal changes its logical status from logical low to logical high.

Two variables are defined as:

— TXERR = TX_ER (XOR) TX_EN

— RXERR = RX_ER (XOR) RX_DV

Where (XOR) is the logical "exclusive or" function.

TXERR takes a new value when the TXC signal changes its logical status from logical low to logical high. RXERR takes a new value when the RXC signal changes its logical status from logical low to logical high.

The RGMII mapping functionality is specified as below.

The logical values in the bits TXD<3:0> shall be mapped into their corresponding voltage values of the RGMII signal lines TD3, TD2, TD1 and TD0 when the TXC signal changes its logical status from logical low to logical high. The logical values in the bits TXD<7:4> shall be mapped into their corresponding voltage values of the RGMII signal lines TD3, TD2, TD1 and TD0 when the TXC signal changes its logical status from logical high to logical low.

The logical values in the bits RXD<3:0> shall be mapped from their corresponding voltage values of the RGMII signal lines RD3, RD2, RD1 and RD0 when the RXC signal changes its logical status from logical low to logical high. The logical values in the bits RXD<7:4> shall be mapped from their corresponding voltage values of the RGMII signal lines RD3, RD2, RD1 and RD0 when the RXC signal changes its logical status from logical high to logical low.

The logical values in the bit TX_EN shall be mapped into their corresponding voltage values of the RGMII signal line TX_CTL when the TXC signal changes its logical status from logical low to logical high. The logical value in the variable TXERR shall be mapped into their corresponding voltage values of the RGMII signal line TX_CTL when the TXC signal changes its logical status from logical high to logical low.

The logical values in the bit RX_EN shall be mapped from their corresponding voltage values of the RGMII signal line RX_CTL when the RXC signal changes its logical status from logical low to logical high. The logical value in the variable RXERR shall be mapped from their corresponding voltage values of the RGMII signal line RX_CTL when the RXC signal changes its logical status from logical high to logical low.

6 Wake-up and synchronised link sleep functionality

6.1 General

This clause specifies service primitives, events, algorithms and state machine used to define the transition between the power states of a physical entity.

It also specifies timing requirements to complete the defined algorithms.

The requirements given in this clause are mandatory for physical entities compliant to the ISO 21111 series that implement a wake-up and synchronised link sleep functionality, independently of the signal bit rate or physical media used.

6.2 Power state, algorithms, and service interfaces

In the case of discrepancy between a figure specifying state machine and the specification in the text, the state machine prevails.

The value of the service primitive parameter and variables follows a positive logic, where TRUE corresponds to logical high and FALSE corresponds to logical low hereafter.

The physical entity has a variable that describe its power state:

— pd_status.

The pd_status variable indicates that the physical entity is in low-power consumption mode.

The physical entity power supply is the power supply that provides energy to the physical entity.

The physical entity power supply has a variable that describe its power state:

— power_off_entity.

The power_off_entity variable indicates that the physical entity power supply is in power off mode.

When the physical entity power supply is in power-off mode, it shall still provide enough current to enable the detection of a signal in the MDI (see 6.11).

The physical entity may control the power_off_entity variable.

The physical entity shall be in one of the two following power states:

— sleep, or

— normal.

The power state of the physical entity is defined by the value of pd_status variable.

The physical entity in sleep power state shall have its pd_status variable set to TRUE.

The physical entity in normal power state shall have its pd_status variable set to FALSE.

The physical entity in sleep power state shall be able to detect a wake signal at the MDI (see 6.11).

The state diagram of Figure 8 specifies the transitions between the power states of the physical entity.

In Figure 8 the presence of NPHY_Wakeup_Forward.request service primitive (see 6.9.1) with its parameter nphy_inh_sleep_req equal to TRUE is denoted as NPHY_Wakeup_Forward.request == TRUE.

Additionally, the presence of PHY_WakeUp.request service primitive (see 6.8.3) is denoted as PHY_WakeUp.request == TRUE.

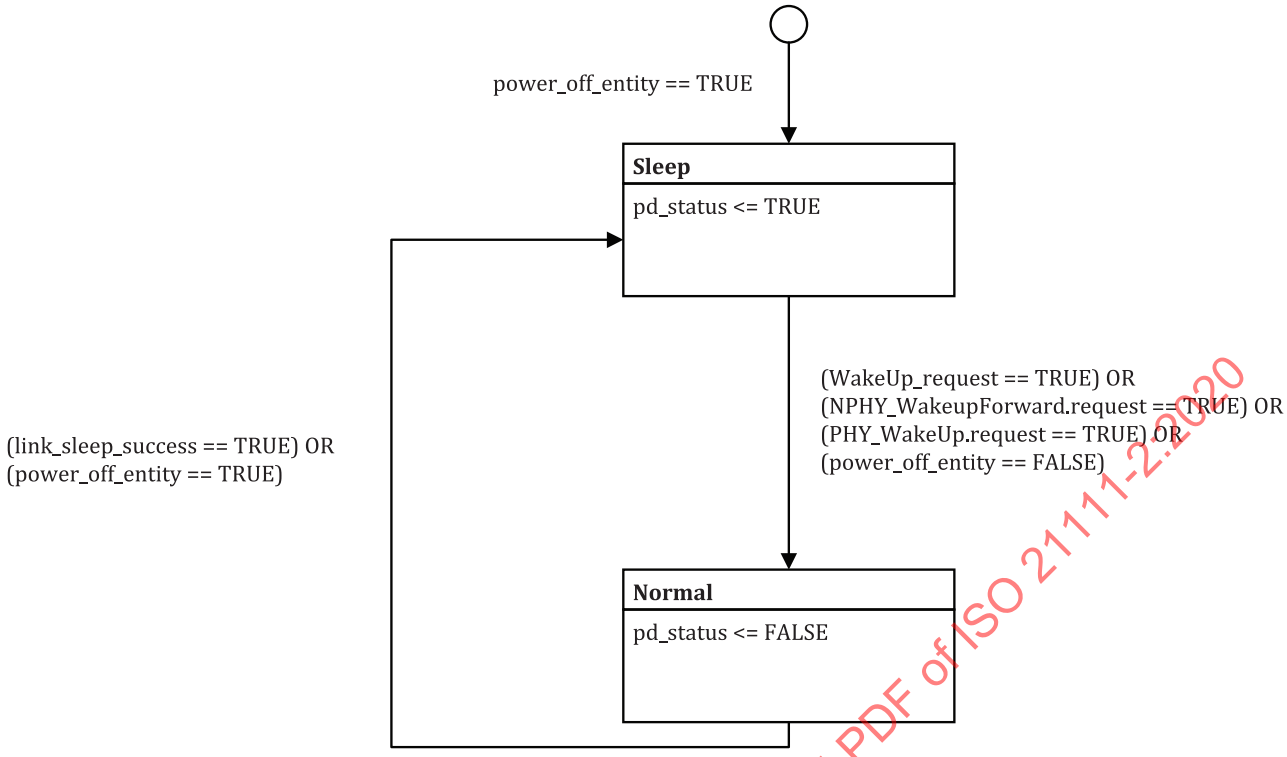

Figure 8 — Physical entity power state diagram

The physical entity shall support two algorithms for the transitions between the power states:

— synchronised link sleep algorithm, and

— wake-up algorithm.

The synchronised link sleep algorithm defines how to perform a synchronised transition from the normal power state to the sleep power state simultaneously in two physical entities which have an established link. One of two physical entities is a calling physical entity that starts the algorithms by instance of its MAC layer. The other is a called physical entity that starts the algorithms by instance of its link partner.

A configuration to refuse the request from the called physical entity to go to the sleep power state may be provided (see 6.4).

The wake-up algorithm defines how to perform a fast transition from sleep power state to normal power state of a called physical entity. The called physical entity may be a neighbour or a link partner (see 6.5).

Figure 9 specifies the physical entity service primitives that may be used by the wake-up and synchronised link sleep algorithms.

The service primitives are specified for all physical entities defined in the ISO 21111 series, independently of the signal bit rate or physical media used.

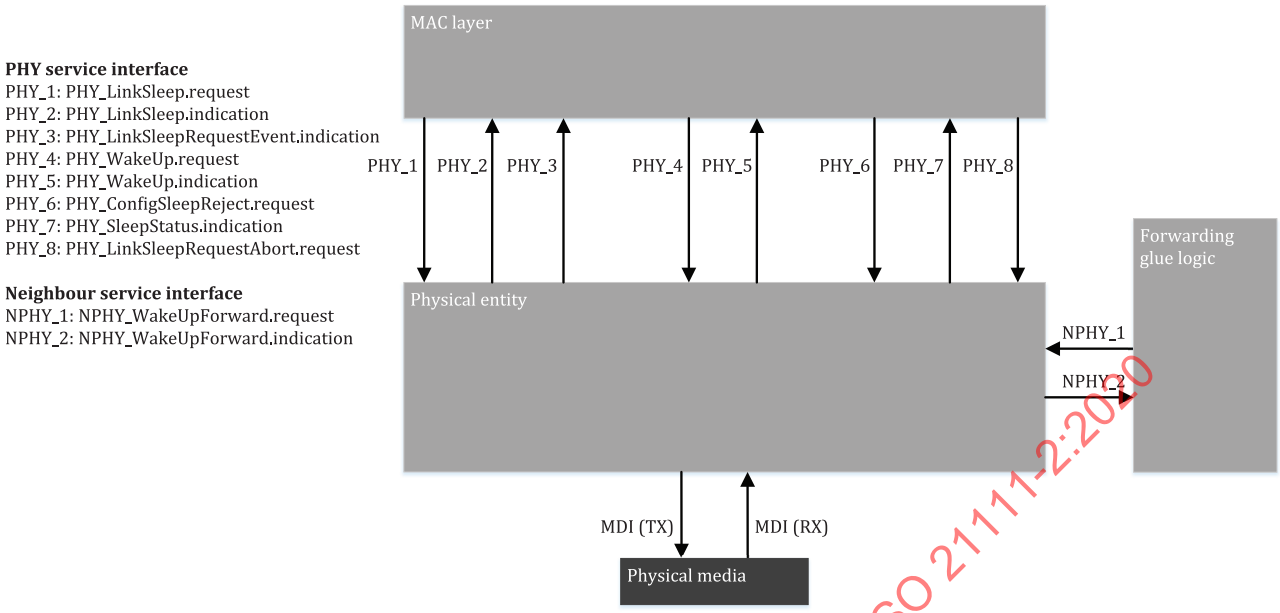

Figure 9 — Physical entity service primitives

Two service interfaces are defined:

a) PHY service interface is defined between a physical entity and MAC layer. The PHY service interface provides the following service primitives:

   — PHY_LinkSleep.request (see 6.8.1),

   — PHY_WakeUp.request (see 6.8.3),

   — PHY_WakeUp.indication (see 6.8.4), and

   — PHY_ConfigSleepReject.request (see 6.8.5).

   Additionally, the PHY service interface may provide the following service primitives:

   — PHY_LinkSleep.indication (see 6.8.2),

   — PHY_SleepStatus.indication (see 6.8.6),

   — PHY_LinkSleepRequestEvent.indication (see 6.8.7), and

   — PHY_LinkSleepRequestAbort.request (see 6.8.8).

b) Neighbour service interface is defined between physical entities that are neighbours, the neighbour service interface provides the following service primitives:

   — NPHY_WakeUpForward.request (see 6.9.1), and

   — NPHY_WakeUpForward.indication (see 6.9.2).

   Four events, which are transmitted between two physical entities in different devices, are defined:

   — LinkSleep_request,

   — LinkSleep_acknowledge,

   — LinkSleep_reject, and

   — WakeUp_request.

The events, service primitives and algorithms specification details depend on the bit rate and physical media used. They are specified in the following parts of the ISO 21111 series:

— ISO 21111-3 for 1 Gbit/s over plastic optical fibre and

— ISO 21111-6 for 100 Mbit/s over single twisted pair.

6.3 Neighbour physical entities

A device may include:

— one or more physical entities,

— one forwarding glue logic, and

— one wake I/O functional entity.

All physical entities in a device shall share the same power supply.

Two or more physical entities in the same device are defined as neighbour physical entities.

The forwarding glue logic is a functional entity that processes the NPHY_WakeUpForward.indication service primitives from the physical entities and the wake I/O functional entity to generate the NPHY_WakeUpForward.request service primitives to each of the physical entities and the wake I/O functional entity.

The wake I/O functional entity is specified in 6.6.

The forwarding glue logic functionality of NPHY_WakeUpForward.indication service primitives to generate the NPHY_WakeUpForward.request service primitives is not in the scope of this document.

The maximum timing delay from any NPHY_WakeUpForward.indication at the input of the forwarding glue logic to any NPHY_WakeUpForward.request generated by the forwarding glue logic is specified in 6.10.2.6.

An example of a device with two physical entities, a wake I/O functional entity and forwarding glue logic limited by dotted line is shown in Figure 10.

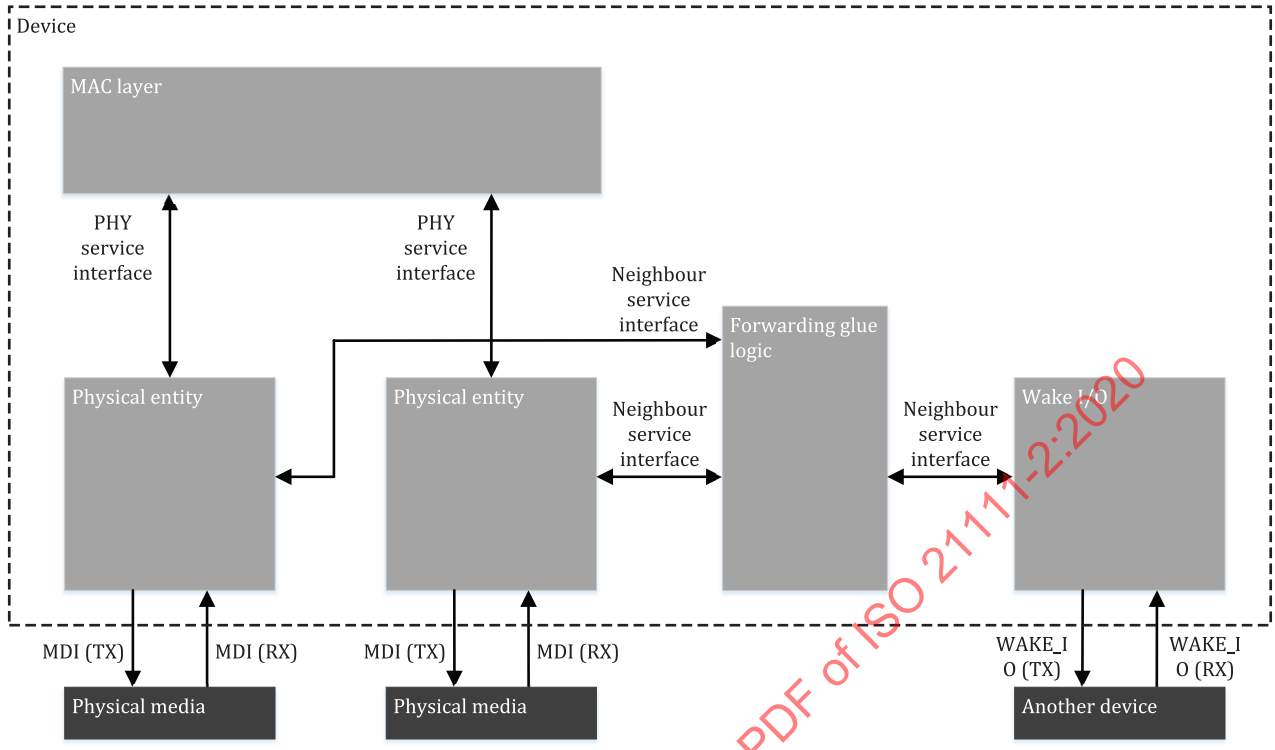

Figure 10 — Example of a device with two physical entities, wake I/O and forwarding glue logic

6.4 Synchronised link sleep algorithm

This subclause defines two events that the synchronised link sleep algorithm exchange between the calling physical entity and the called physical entity:

— successful synchronised link sleep event, and

— rejected synchronised link sleep event.

A successful synchronised link sleep exchange of events follows the next sequence:

1) the calling physical entity shall receive a PHY_LinkSleep.request service primitive from the MAC layer;

2) the calling physical entity shall generate a LinkSleep_request event that is transmitted to its link partner;

3) whenever a LinkSleep_request event is received, and the link partner is configured to not reject this request, the called physical entity shall respond to the calling physical entity with a LinkSleep_acknowledge event;

4) the link partner may generate the optional PHY_LinkSleepRequestEvent.indication service primitive and may allow its MAC layer aborting the sleep procedure. In case that the link partner MAC layer aborts the sleep procedure, the link partner shall not generate the LinkSleep_acknowledge event [see 3)];

5) when the LinkSleep_acknowledge event is received by the calling physical entity, and further media dependent optional conditions are fulfilled, the calling physical entity shall set its internal variable link_sleep_success to TRUE and may generate the PHY_LinkSleep.indication service primitive with the link_sleep_success parameter set to TRUE.

A rejected synchronised link sleep exchange of events follows the next sequence:

a) the calling physical entity shall receive a PHY_LinkSleep.request service primitive from the MAC layer;

b) the calling physical entity shall generate a LinkSleep_request event that is transmitted to its link partner;

c) if the link partner is configured to reject the LinkSleep_request event or the MAC layer of the link partner aborts the LinkSleep_request, the link partner shall respond to the calling physical entity with a LinkSleep_reject event, when the LinkSleep_request event is received;

d) in the case that the link partner implements the optional PHY_LinkSleepRequestEvent.indication service primitive, it shall be generated and sent to MAC layer of the link partner;

e) when the LinkSleep_reject event is received by the calling physical entity, the calling physical entity shall set its internal variable link_sleep_success to FALSE and shall generate the PHY_LinkSleep.indication service primitive with the link_sleep_success parameter set to FALSE.

A timeout of the LinkSleep_acknowledge event may be also interpreted as a valid LinkSleep_reject event.

6.5 Wake-up algorithm

When a transition from the sleep power state to the normal power state is produced, the physical entity shall generate the service primitive NPHY_WakeUpForward.indication with its parameter set to TRUE. Additionally, the physical entity shall generate and send to its link partner a WakeUp_request, except if it received the WakeUP_request from this link partner.

Additionally, when a WakeUp_request event is received from the link partner on an active link, the physical entity shall generate the service primitive NPHY_WakeUpForward.indication with its parameter set to TRUE.

When a transition from the normal power state to the sleep power state is produced, the physical entity shall generate the service primitive NPHY_WakeUpForward.indication with its parameter set to FALSE.

The transition from the sleep power state to the normal state is produced in the following cases, as specified in Figure 8:

— a WakeUp_request event is received from the link partner, or

— a NPHY_WakeUpForward.request with its parameter set to TRUE is received from the glue logic, or

— a PHY_WakeUp.request is received from the MAC layer.

6.6 Wake I/O block

The wake I/O block shall convert the presence of the incoming service primitive NPHY_WakeUpForward.request (see 6.9.1) into an electrical signal in the WAKE_IO (TX) interface.

When the incoming service primitive NPHY_WakeUpForward.request has its parameter equal to TRUE, the electrical signal generated in the WAKE_IO (TX) shall change from a low-voltage level to a high-voltage level and maintain such voltage level during 40 µs at minimum. Otherwise, the wake I/O functional entity shall not generate any electrical signal.

Additionally, the wake I/O functional entity shall convert an electrical signal consisting of a transition from low-voltage level followed by a high-voltage level with duration of more than 40 µs in the WAKE_IO (RX) interface into a service primitive NPHY_WakeUpForward.indication with its parameter set to TRUE (see 6.9.2).

An electrical signal consisting of a transition from low-voltage level followed by a high-voltage level with duration below 10 µs incoming to the WAKE_IO (RX) shall not generate an NPHY_WakeUpForward. indication with its parameter set to TRUE (see 6.9.2).

When the incoming service primitive NPHY_WakeUpForward.request has its parameter set to TRUE, the electrical signal generated in the WAKE_IO (TX) shall be a change from a low-voltage level to a high-voltage level and shall maintain such voltage level during 490 ms at minimum and 510 ms at a maximum. Then, the electrical signal shall return to the low-voltage level.

In this case, the wake I/O functional entity shall convert an electrical signal consisting of a transition from low-voltage level followed by a high-voltage level with duration between 20 ms and 500 ms in the WAKE_IO (RX) interface into a service primitive NPHY_WakeUpForward.indication with its parameter set to TRUE (see 6.9.2).

An electrical signal consisting of a transition from low-voltage level followed by a high-voltage level with duration below 10 ms incoming to the WAKE_IO (RX) shall not generate an NPHY_WakeUpForward. indication with its parameter set to TRUE (see 6.9.2).

NOTE 1 The electric voltage of the low and high-voltage levels defined in this subclause is out of the scope of this document.

NOTE 2 An inhibit pin (INH) for switching on the power supply is not in the scope of this document. Inhibit pins can be open-collector, active high.

6.7 Physical entity power state

6.7.1 Physical entity power state variables

The physical entity power state machine variables used in power state machine (see Figure 8) are specified in Table 10.

Table 10 — Physical entity power state machine variables

Variable	Description	Value	Remark
pd_status	Physical entity is in low-power consumption mode.	TRUE	The physical entity is in low-power consumption mode.
		FALSE	The physical entity is not in low-power consumption mode.
power_off_entity	Physical entity power supply is in power-off mode.	TRUE	The power supply connected to the physical entity is in power-off mode.
		FALSE	The power supply connected to the physical entity is not in power-off mode.
link_sleep_success	The synchronised link sleep exchange of events is successful. When a value is assigned to this variable, the value of the variable shall be copied into the parameter link_sleep_success of PHY_LinkSleep.indication and the service primitive shall be generated (see 6.8.2).	TRUE	Synchronised link sleep algorithm is successful (see 6.4).
		FALSE	Synchronised link sleep algorithm is failed (see 6.4).

6.8 PHY service interface

6.8.1 PHY_LinkSleep.request

PHY_LinkSleep.request requests a synchronous transition to the sleep power state of a physical entity and its link partner.

Table 11 specifies PHY_LinkSleep.request service primitive.

Table 11 — Specification of PHY_LinkSleep.request

Item	Description
Semantic	PHY_LinkSleep.request(void)
Parameters	None
Generation	The MAC layer shall generate a PHY_LinkSleep.request. It is present just at the time necessary to make a transition in the physical entity power state machine (Figure 10) in accordance with the synchronised link sleep algorithm (see 6.4).
Effect of receipt	The calling physical entity shall generate a LinkSleep_request to the link partner to initiate synchronised link sleep algorithm.

6.8.2 PHY_LinkSleep.indication

PHY_LinkSleep.indication indicates to the MAC layer whether a previous PHY_LinkSleep.request at the calling physical entity is successful or whether a PHY_LinkSleep.request from the link partner leads to a successful synchronous link sleep.

Table 12 specifies PHY_LinkSleep.indication service primitive.

Table 12 — Specification of PHY_LinkSleep.indication

Item	Description
Semantic	PHY_LinkSleep.indication(link_sleep_success)
Parameters	The link_sleep_success parameter shall have one of the following values: — TRUE: the previous PHY_LinkSleep.request (see 6.8.1) generated from upper layers or from a link partner is successful as described in 6.4; — FALSE: the previous PHY_LinkSleep.request (see 6.8.1) is not successful as described in 6.4.
Generation	The calling physical entity shall generate a PHY_LinkSleep.indication, when either the LinkSleep_acknowledge or the LinkSleep_reject is received from link partner.
Effect of receipt	MAC layer is informed about the success of previously requested synchronised link sleep.

6.8.3 PHY_WakeUp.request

PHY_WakeUp.request requests to wake up the physical entity and its link partner.

Table 13 specifies PHY_WakeUp.request service primitive.

Table 13 — Specification of PHY_WakeUp.request

Item	Description
Semantic	PHY_WakeUp.request(void)
Parameters	None
Generation	The data link layer shall generate a PHY_WakeUp.request. It is present just at the time necessary to make a transition in the state machine in accordance with the wake-up algorithm.
Effect of receipt	The physical entity which received a PHY_WakeUp.request shall generate a WakeUp_request in the wake-up algorithm.

6.8.4 PHY_WakeUp.indication

PHY_WakeUp.indication indicates to the MAC layer the reception of a WakeUp_request event.

Table 14 specifies PHY_WakeUp.indication service primitive.

Table 14 — Specification of PHY_WakeUp.indication

Item	Description
Semantic	PHY_WakeUp.indication(void)
Parameters	None
Generation	The physical entity shall generate a PHY_WakeUp.indication when the physical entity receives a WakeUp_request.
Effect of receipt	The MAC layer is informed about the reception of a WakeUp_request.

6.8.5 PHY_ConfigSleepReject.request

PHY_ConfigSleepReject.request configures if the physical entity accepts the LinkSleep_request from the link partner to make the transition to the sleep power state.

Table 15 specifies PHY_ConfigSleepReject.request service primitive.

Table 15 — Specification of PHY_ConfigSleepReject.request

Item	Description
Semantic	PHY_ConfigSleepReject.request (mng_sleep_reject)
Parameters	The mng_sleep_reject parameter shall have one of the following values: — TRUE: the physical entity shall reject or ignore any LinkSleep_request from the link partner to perform a synchronised link sleep; — FALSE: the physical entity shall accept any LinkSleep_request from the link partner to perform a synchronised link sleep.
Generation	The MAC layer shall generate a PHY_ConfigSleepReject.request.
Effect of receipt	The value of the mng_sleep_reject parameter may be copied to a calling physical entity variable and be used in the state machine in accordance with the synchronised link sleep algorithm.

6.8.6 PHY_SleepStatus.indication

PHY_SleepStatus.indication indicates to the MAC layer the power state of the physical entity as defined in 6.2.

Table 16 specifies PHY_SleepStatus.indication service primitive.

Table 16 — Specification of PHY_SleepStatus.indication

Item	Description
Semantic	PHY_SleepStatus.indication (sleep_status)
Parameters	The sleep_status parameter shall have one of the following values: — NORMAL: the physical entity is in the normal power state; — SLEEP: the physical entity is in the sleep power state.
Generation	PHY_SleepStatus.indication shall be generated by the physical entity when its power state changes.
Effect of receipt	The MAC layer is informed about the power state of the physical entity.

6.8.7 PHY_LinkSleepRequestEvent.indication

PHY_LinkSleepRequestEvent.indication indicates to the MAC layer whether a LinkSleep_request is received from its link partner.

Table 17 specifies PHY_LinkSleepRequestEvent.indication service primitive.

Table 17 — Specification of PHY_LinkSleepRequestEvent.indication

Item	Description
Semantic	PHY_LinkSleepRequestEvent.indication(void)
Parameters	None
Generation	The physical entity shall generate a PHY_LinkSleepRequestEvent.indication due to the reception of a LinkSleep_request from the link partner.
Effect of receipt	The MAC layer is informed about the reception of a LinkSleep_request from the link partner.

6.8.8 PHY_LinkSleepRequestAbort.request

PHY_LinkSleepRequestAbort.request aborts the current synchronised link sleep algorithm.

Table 18 specifies PHY_LinkSleepRequestAbort.request.

Table 18 — Specification of PHY_LinkSleepRequestAbort.request

Item	Description
Semantic	PHY_LinkSleepRequestAbort.request (void)
Parameters	None
Generation	The MAC layer shall generate PHY_LinkSleepRequestAbort.request.
Effect of receipt	The current synchronised link sleep algorithm is aborted and returns to the initial state.

6.9 Neighbour service interface

6.9.1 NPHY_WakeUpForward.request

This service primitive may be received from the forwarding glue logic that composes this service primitive from the NPHY_WakeUpForward.indication service primitive of the neighbour physical entities and from the wake I/O functional entity (see Figure 10).

Table 19 specifies NPHY_WakeUpForward.request service primitive.

Table 19 — Specification of NPHY_WakeUpForward.request

Item	Description
Semantic	NPHY_WakeUpForward.request(nphy_inh_sleep_req)
Parameters	The nphy_inh_sleep_req parameter shall have one of the following values: — TRUE: the physical entity shall not be able to make the transition from sleep prepare to sleep; — FALSE: the physical entity shall be able to make the transition from sleep prepare to sleep.
Generation	NPHY_WakeUpForward.request shall be generated by the forwarding glue logic that composes this service primitive from the NPHY_WakeUpForward.indication of the neighbour physical entities and the wake I/O functional entity.
Effect of receipt	The value of the nphy_inh_sleep_req parameter may be copied to a calling physical entity variable and be used in the power state diagram (see Figure 8) in accordance with the wake-up algorithm (see 6.5).

6.9.2 NPHY_WakeUpForward.indication

This service primitive may be generated by a physical entity and by a wake I/O functional entity to forward to its neighbours if its power state is the normal power state.

Table 20 specifies NPHY_WakeUpForward.indication service primitive.