INTERNATIONAL STANDARD

ISO 17987-8

First edition
2019-10

Road vehicles — Local Interconnect Network (LIN) —

Part 8: Electrical physical layer (EPL) specification: LIN over DC powerline (DC-LIN)

Véhicules routiers — Réseau Internet local (LIN) —

Partie 8: Spécification de couche physique électrique (EPL): LIN sur ligne d'alimentation en courant continu (DC-LIN)

Reference number
ISO 17987-8:2019(E)

ISO copyright office
CP 401 • Ch. de Blandonnet 8
CH-1214 Vernier, Geneva
Phone: +41 22 749 01 11
Fax: +41 22 749 09 47
Email: copyright@iso.org
Website: www.iso.org

Published in Switzerland

Contents

Page

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 17987 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user’s national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

ISO 17987 (all parts) specifies the use cases, communication protocol and physical layer requirements of an in-vehicle communication network called Local Interconnect Network (LIN).

The LIN protocol as proposed is an automotive-focused low speed UART-based network (Universal Asynchronous Receiver Transmitter). Some of the key characteristics of the LIN protocol are signal-based communication, schedule table-based frame transfer, master/slave communication with error detection, node configuration and diagnostic service transportation.

The LIN protocol is for low cost automotive control applications, for example door module and air conditioning systems. It serves as a communication infrastructure for low-speed control applications in vehicles by providing:

— signal-based communication to exchange information between applications in different nodes;

— bit rate support from 1 kbit/s to 20 kbit/s;

— deterministic schedule table-based frame communication;

— network management that wakes up and puts the LIN cluster into sleep mode in a controlled manner;

— status management that provides error handling and error signalling;

— transport layer that allows large amount of data to be transported (such as diagnostic services);

— specification of how to handle diagnostic services;

— electrical physical layer specifications;

— node description language describing properties of slave nodes;

— network description file describing behaviour of communication;

— application programmer's interface.

ISO 17987 (all parts) is based on the open systems interconnection (OSI) basic reference model as specified in ISO/IEC 7498-1 which structures communication systems into seven layers.

The OSI model structures data communication into seven layers called (top down) application layer (layer 7), presentation layer, session layer, transport layer, network layer, data link layer and physical layer (layer 1). A subset of these layers is used in ISO 17987 (all parts).

ISO 17987 (all parts) distinguishes between the services provided by a layer to the layer above it and the protocol used by the layer to send a message between the peer entities of that layer. The reason for this distinction is to make the services, especially the application layer services and the transport layer services, reusable also for other types of networks than LIN. In this way, the protocol is hidden from the service user and it is possible to change the protocol if special system requirements demand it.

ISO 17987 (all parts) provides all documents and references required to support the implementation of the requirements related to the following.

— ISO 17987-1: This part provides an overview of the ISO 17987 (all parts) and structure along with the use case definitions and a common set of resources (definitions, references) for use by all subsequent parts.

— ISO 17987-2: This part specifies the requirements related to the transport protocol and the network layer requirements to transport the PDU of a message between LIN nodes.

— ISO 17987-3: This part specifies the requirements for implementations of the LIN protocol on the logical level of abstraction. Hardware related properties are hidden in the defined constraints.

— ISO 17987-4: This part specifies the requirements for implementations of active hardware components which are necessary to interconnect the protocol implementation.

— ISO/TR 17987-5: This part specifies the LIN application programmers interface (API) and the node configuration and identification services. The node configuration and identification services are specified in the API and define how a slave node is configured and how a slave node uses the identification service.

— ISO 17987-6: This part specifies tests to check the conformance of the LIN protocol implementation according to ISO 17987-2 and ISO 17987-3. This comprises tests for the data link layer, the network layer and the transport layer.

— ISO 17987-7: This part specifies tests to check the conformance of the LIN electrical physical layer implementation (logical level of abstraction) according to ISO 17987-4.

— ISO 17987-8: This part specifies the requirements for implementations of the DC powerline electrical physical layer (EPL) for the LIN communications system as well as a conformance test plan for the EPL.

Road vehicles — Local Interconnect Network (LIN) —

Part 8: Electrical physical layer (EPL) specification: LIN over DC powerline (DC-LIN)

1 Scope

This document specifies an additional electrical physical layer (EPL) for the Local Interconnect Network (LIN) of the ISO 17987 series. It specifies the transmission over DC powerline without affecting the LIN higher layers, hereafter named DC-LIN.

The DC-LIN EPL uses a high-frequency modulated carrier to propagate UART bytes (byte-oriented) over the DC powerline.

This document specifies the electrical characteristics, the modulation method of the transmission, and how to impose the carrier signal on the DC powerlines.

The DC-LIN EPL supports bit rates of 9 615 bit/s, 10 417 bit/s, and 19 230 bit/s.

The DC-LIN EPL is applicable for a wide range of DC powerlines including 12-V and 24-V operations, allowing communicating between different DC powerlines via a coupling capacitor. A DC-LIN EPL interface to powerline example is described in Annex A.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 17987-4:2016, *Road vehicles — Local Interconnect Network (LIN) — Part 4: Electrical physical layer (EPL) specification 12 V/24 V*

ISO 17987-6, *Road vehicles — Local Interconnect Network (LIN) — Part 6: Protocol conformance test specification*

IEC 61000-4-2, *Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test*

3 Terms, definitions, symbols, and abbreviated terms

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1 Terms and definitions

3.1.1
BR_9_6K
DC-LIN EPL operating at nominal bit rate of 9 615 bit/s

3.1.2
BR_10K
DC-LIN EPL operating at nominal bit rate of 10 417 bit/s

3.1.3
BR_19_2K
DC-LIN EPL operating at nominal bit rate of 19 230 bit/s

3.1.4
byte field
byte that consists of one start bit, eight data bits, and one stop bit

3.1.5
byte field sync preamble
sequence of phase shifts at the beginning of EPL byte field modulation used for byte synchronization

3.1.6
carrier frequency
DC-LIN EPL center frequency that is altered (modulated) to transfer data

3.1.7
coupling capacitor
capacitor for blocking the DC powerline voltage to/from a DC-LIN EPL

3.1.8
DC-LIN EPL RX mode
mode that DC-LIN EPL de-asserts line-out and controls RXD according to signal at line-in

3.1.9
DC-LIN EPL TX mode
mode that DC-LIN EPL controls line-out according to logic state present at TXD

3.1.10
start bit
logic low ('0') of the first bit of a byte field

3.1.11
stop bit
logic high ('1') of the last bit of a byte field

3.2 Symbols and abbreviated terms

'0'	logical 0
'1'	logical 1
AC	alternate current
API	application programmers interface
B_{data_bit}	byte field data bit signalled on RXD at DC-LIN EPL receiver side
$B_{data\_bit\_local}$	byte field data bit signalled on RXD at DC-LIN EPL transmitter side

B_{del}	break delimiter signalled on RXD at DC-LIN EPL receiver side
B_{del_local}	break delimiter signalled on RXD at DC-LIN EPL transmitter side
$B_{err\_data\_bit\_local}$	byte field error data bit signalled on RXD at DC-LIN EPL transmitter side
$B_{fe\_stop\_bit}$	byte field frame error stop bit signalled on RXD at DC-LIN EPL receiver side
$B_{fe\_stop\_bit\_local}$	byte field frame error stop bit signalled on RXD at DC-LIN EPL transmitter side
$B_{fe\_del\_local}$	break field delimiter frame error signalled on RXD at DC-LIN EPL transmitter side
$B_{fe\_start\_bit\_local}$	byte field frame error start bit signalled on RXD at DC-LIN EPL transmitter side
BR	DC-LIN EPL operating bit rate
B_{start_bit}	byte field start bit signalled on RXD at DC-LIN EPL receiver side
$B_{start\_bit\_local}$	byte field start bit signalled on RXD at DC-LIN EPL transmitter side
B_{stop_bit}	byte field stop bit signalled on RXD at DC-LIN EPL receiver side
$B_{stop\_bit\_local}$	byte field stop bit signalled on RXD at DC-LIN EPL transmitter side
CB_{TX}	consecutive byte field transmission
CF_{max}	maximal number of carrier frequencies implemented in IUT transmit signal
DC	direct current
EPL	electrical physical layer
ESD	electrostatic discharge
fc_i	carrier frequency
FB_{TX}	first byte field transmission
I	in-phase signal component
IUT	implementation under test
bit/s	bit per second
LIN	Local Interconnect Network
line-in	modulated carrier signal input pin to the EPL from the DC powerline
line-out	modulated carrier signal output pin from the EPL to the DC powerline
LT	lower tester
L_{out_lev}	line-out sampled monitoring level
$L_{out\_thr\_lev}$	line-out monitoring peak threshold level
$L_{out\_err\_cond}$	line-out monitoring error condition
max.	maximum
min.	minimum

P_{byte_length} nominal length of modulated byte field in t_{BIT}

$P_{data\_bit\_len}$ nominal length of modulated byte field data bit

P_{data} data bit modulation phases

P_{dh_1} data bit ‘1’ 1st phase shift

P_{dh_2} data bit ‘1’ 2nd phase shift

P_{dh_3} data bit ‘1’ 3rd phase shift

P_{dl_1} data bit ‘0’ 1st phase shift

P_{dl_2} data bit ‘0’ 2nd phase shift

P_{dl_3} data bit ‘0’ 3rd phase shift

P_{ref_consec} reference phase of consecutive byte transmission

P_{ref_first} reference phase of the first byte transmission

P_{sync_p} sync preamble modulation phases

P_{sp_1} sync preamble 1st phase shift

P_{sp_2} sync preamble 2nd phase shift

P_{sp_3} sync preamble 3rd phase shift

P_{sp_4} sync preamble 4th phase shift

P_{sp_5} sync preamble 5th phase shift

P_{sp_6} sync preamble 6th phase shift

P_{sp_7} sync preamble 7th phase shift

P_{sp_8} sync preamble 8th phase shift

P_{sp_9} sync preamble 9th phase shift

P_{sp_10} sync preamble 10th phase shift

P_{sp_11} sync preamble 11th phase shift

P_{sp_12} sync preamble 12th phase shift

P_{sp_13} sync preamble 13th phase shift

P_{sp_14} sync preamble 14th phase shift

P_{sp_15} sync preamble 15th phase shift

P_{sp_16} sync preamble 16th phase shift

P_{sp_17} sync preamble 17th phase shift

P_{sp_18} sync preamble 18th phase shift

$P_{sync\_pre\_len}$ nominal length of modulated byte field sync preamble

Q	quadrature signal component
$\mathrm{R}_{\mathrm{rx\_mode}}$	DC-LIN EPL RX mode
$\mathrm{RX}_{\mathrm{err\_cond}}$	DC-LIN EPL RX node error condition
t_{BIT}	bit time
$t_{\mathrm{break\_field}}$	break field data bits ‘0’ length in t_{BIT}
$t_{\mathrm{l\_out\_mon\_l}}$	line-out monitoring active duration
$t_{\mathrm{l\_out\_mon\_samp}}$	line-out monitoring sample time
$t_{\mathrm{l\_out\_mon\_start}}$	start time of line-out monitoring
$t_{\mathrm{RX\_delay}}$	delay between transmitted byte field over to the DC powerline and the receiver reconstructed byte field from the DC powerline
$t_{\mathrm{RX\_delay\_local}}$	delay between transmitted byte field on TXD and the received byte field on RXD at a DC-LIN EPL node (locally)
$t_{\mathrm{rx\_proc\_max}}$	maximum process time at RX DC-LIN EPL side
$t_{\mathrm{rx\_proc\_min}}$	minimum process time at RX DC-LIN EPL side
$t_{\mathrm{SB\_TX}}$	start time of byte field sync preamble transmission on line-out
$\mathrm{T}_{\mathrm{tx\_mode}}$	DC-LIN EPL TX mode
$t_{\mathrm{txd\_min\_assert}}$	minimum TXD assert (‘0’) time without timeout event (deactivating $\mathrm{T}_{\mathrm{tx\_mode}}$)
$t_{\mathrm{txd\_min\_recover}}$	minimum TXD deassert (‘1’) time after timeout event ($\mathrm{T}_{\mathrm{tx\_mode}}$ remains deactivated)
$\overline{\mathrm{TXD}}$	logical inverted TXD (i.e. '0' becomes '1' and vice versa)
typ.	typical
UT	upper tester
Vpp	volt peak-to-peak
$V_{\mathrm{PWL\_max}}$	maximum rating for the DC powerline
φ	carrier phases
Δfc_i	carrier frequency resolution
°	degree

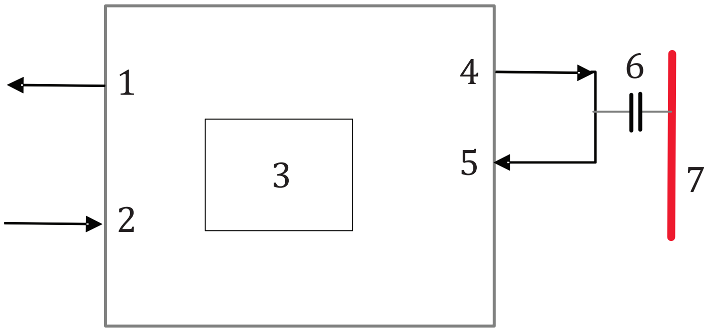
4 Electrical physical layer requirements

4.1 General

The DC-LIN EPL is the physical media access sub-layer, which links the data link layer as standardized in ISO 17987-3 and the DC powerlines (physical medium dependent sub-layer). Figure 1 depicts an example of a DC-LIN EPL. The EPL consists of a modem, which encodes the data from the data link layer into the modulated carrier signal that is coupled to the DC powerline. The modem also decodes the received data on the DC powerline and provides this to the data link layer at the receivers. Follow the DC-LIN EPL conformance test plan in Annex B.

The DC-LIN EPL transmitter encodes each byte field sent by the data link layer on TXD into a modulated carrier signal, which is transferred over the DC powerline. The modulation consists of a predefined combination of phase shifts according to the byte field modulation scheme specified in 4.2.2.

The DC-LIN EPL receiver decodes the received modulated byte from the DC powerline and signals it on RXD to the data link layer.



Key

1 RXD receive data pin
2 TXD transmit data pin
3 modem
4 line-out
5 line-in
6 coupling capacitor
7 DC powerline

Figure 1 — Example of a DC-LIN EPL

4.2 Transmitter characteristics

4.2.1 Transmit signal specification

The transmit signal shall be constructed as the sum of up to four (redundant) selectable modulated carrier frequencies.

The definition of the transmit signal is given in Formula (1).

Definition of the formula:

$$\text{Transmit signal} = \sum_{i=1}^{n} A \times \cos\left[\left(360° \times fc_i \times t\right) + \varphi(t)\right] \quad (1)$$

where

A is the gain amplitude of the carrier signal in volts;

t is the time in seconds;

fc_i is the selected carrier frequency;

$\varphi(t)$ is the carrier frequency phase; $\varphi(t)$ = 0°, 90°, 180°, 270°;

$\varphi(t)$ changes as a function of the byte field modulation scheme;

n is the maximal carrier frequency selection per transmit signal;

n = 1, 2, 3, 4.

Table 1 specifies the DC-LIN EPL carrier frequency.

Table 1 — Carrier frequency specification

Parameter	Description	Min.	Max.	Unit	Accuracy
fc_i	Carrier frequency band	5	30	MHz	±0,02 %
Δfc_i	Carrier frequency resolution	0,1	0,1	MHz	

In essence, $fc_i \in${5 MHz; 5,1 MHz; 5,2 MHz; ... 29,8 MHz; 29,9 MHz; 30 MHz}.

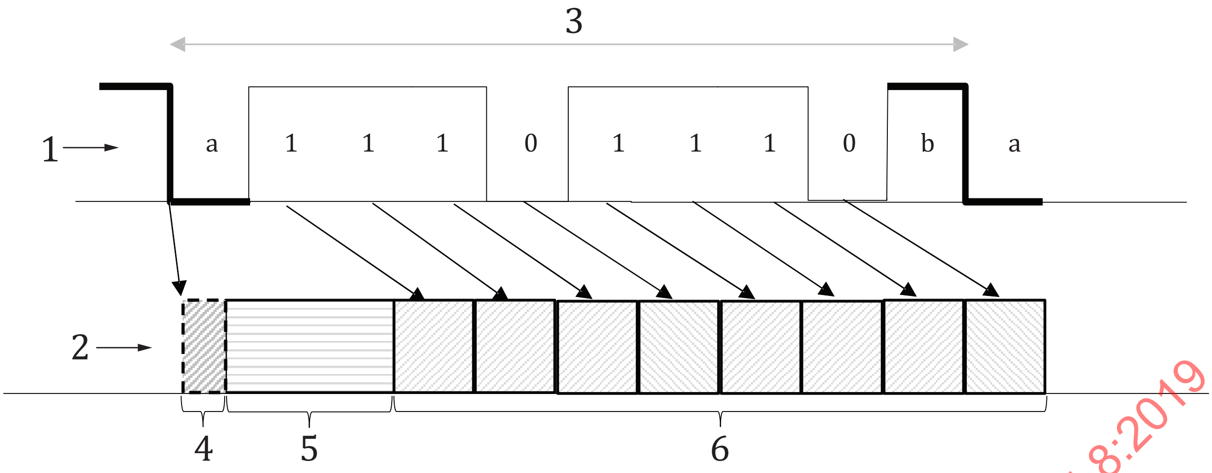
4.2.2 Byte field modulation scheme

4.2.2.1 Byte field modulation scheme structure

A byte field modulation scheme shall consist of a byte field sync preamble modulation (specified in 4.2.2.3) and a byte field data bit modulation (specified in 4.2.2.4). A first byte field modulation shall start with a dedicated reference phase (specified in 4.2.2.2).

A byte field start bit and stop bit shall not be included in a byte field modulation scheme. At receiving nodes, the DC-LIN EPL shall reconstruct both the start bit and stop bit artificially on RXD (see 4.4).

Figure 2 depicts a byte field modulation scheme structure.



Key

1 TXD DC-LIN node A

2 DC powerline

3 byte field

4 reference phase

5 byte field sync preamble

6 8 modulated data bits

[a] Start.

[b] Stop.

Figure 2 — Byte field modulation scheme structure

The byte field modulation scheme shall consist of a sequence of ±90° phase shifts while $L_{out\_err\_cond}$ is inactive (see 4.2.2.3 and 4.2.2.4).

While $L_{out\_err\_cond}$ is active, and only after completion of byte field sync preamble transmission, the transmit signal shall consist of no phase shifts (i.e. constant phase transmission) for the remaining field transmission time (see 4.5.3).

Figure 3 specifies the transmitting phases for 0°, 90°, 180°, and 270° [i.e. $\varphi(t)$].

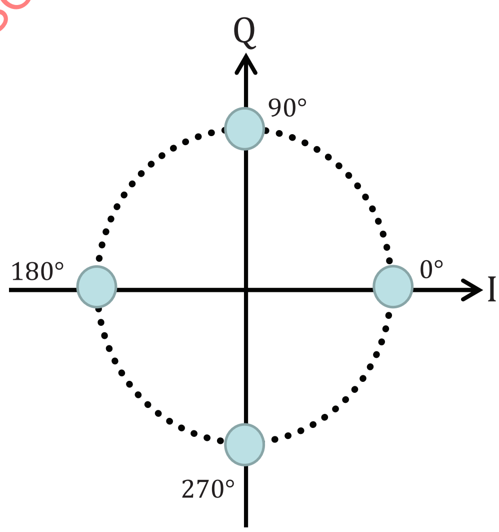


Figure 3 — Transmitter phase's definition

4.2.2.2 Reference phase

The DC-LIN EPL shall transmit a reference phase (P_{ref_first}) prior to the first phase transmission of a byte field sync preamble modulation.

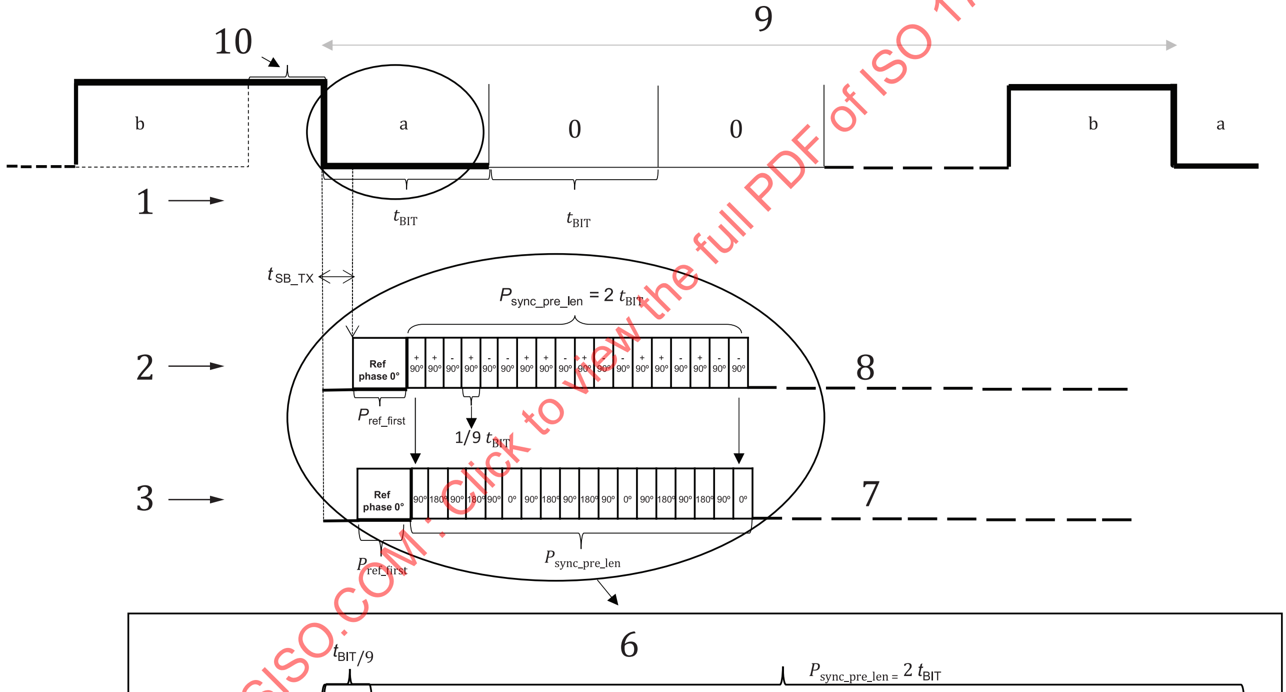
A first byte field transmission (FB_{TX}) shall be interpreted as a start of a byte field transmission by the data link layer with an inter-byte space longer than 1/3 t_{BIT}.

A consecutive byte field transmission (CB_{TX}) shall be interpreted as a start of a byte field transmission by the data link layer with an inter-byte space no longer than 1/3 t_{BIT}.

In the case of a FB_{TX}, a dedicated reference phase shall be transmitted (P_{ref_first}) as specified in Figure 4.

In the case of a CB_{TX} (i.e. not a FB_{TX}), the last phase of the previous byte field modulation transmission shall be used as the reference phase (P_{ref_consec}) of the next byte field sync preamble modulation (as specified in Figure 5).

Figure 4 shows an example of byte field sync preamble modulation of a first byte field transmission.



P_{sp_1}	P_{sp_2}	P_{sp_3}	P_{sp_4}	P_{sp_5}	P_{sp_6}	P_{sp_7}	P_{sp_8}	P_{sp_9}	P_{sp_10}	P_{sp_11}	P_{sp_12}	P_{sp_13}	P_{sp_14}	P_{sp_15}	P_{sp_16}	P_{sp_17}	P_{sp_18}
+ 90°	+ 90°	- 90°	+ 90°	- 90°	- 90°	+ 90°	+ 90°	- 90°	+ 90°	- 90°	- 90°	+ 90°	+ 90°	- 90°	+ 90°	- 90°	- 90°
90°	180°	90°	180°	90°	0°	90°	180°	90°	180°	90°	0°	90°	180°	90°	180°	90°	0°

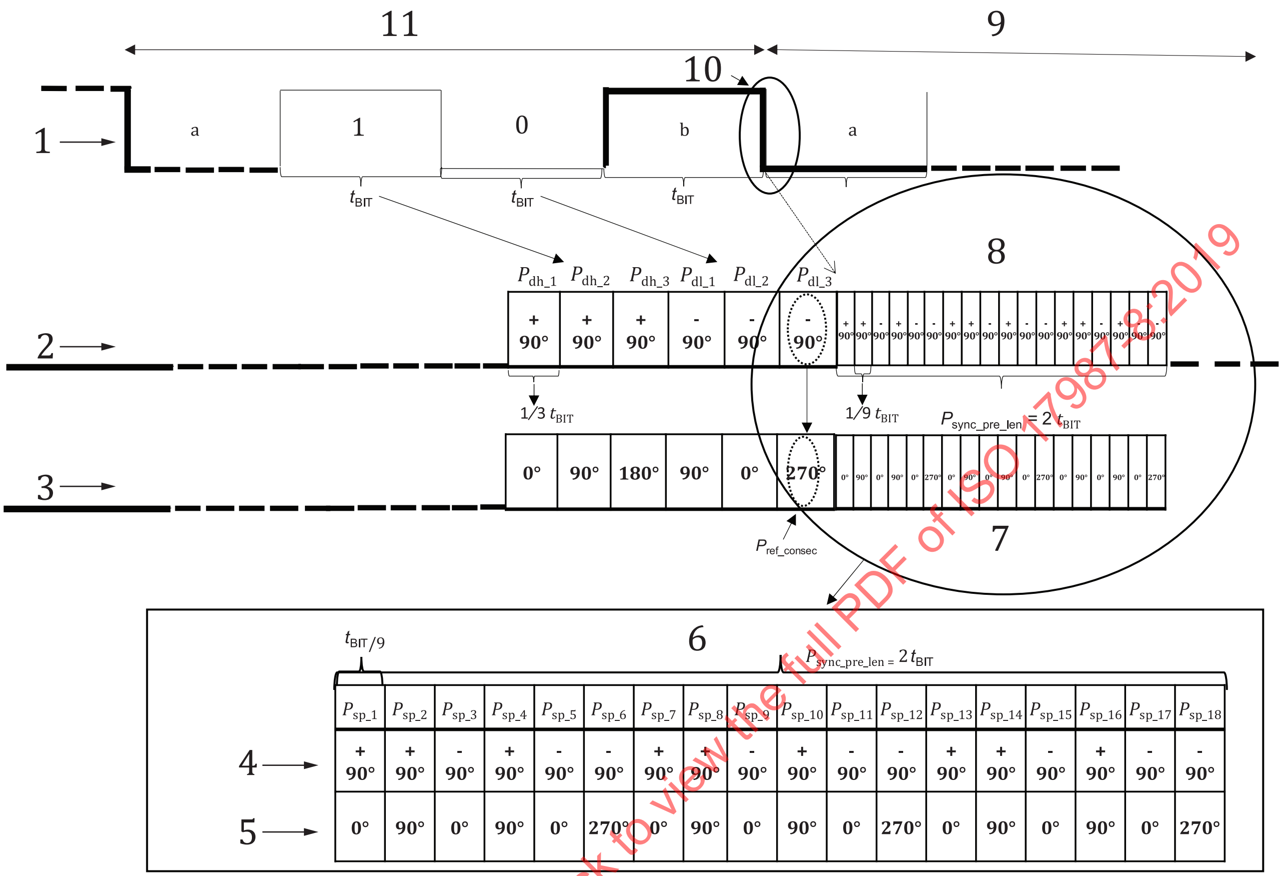
Key

1 TXD DC-LIN node A
2 DC powerline
3 TX phases
4 phase shifts
5 actual TX phases
6 byte field sync preamble
7 byte field sync preamble - actual TX phases
8 byte field sync preamble - phase shifts
9 DC-LIN first byte field transmission of node A
10 Inter-byte space > 1/3 t_{BIT}
a Start.
b Stop.

Figure 4 — Example of byte field sync preamble modulation of first byte field TX

Figure 5 shows an example of byte field sync preamble modulation of consecutive byte field transmissions.

P_{ref_consec} is the last phase of the previous byte field transmission.



Key

1 TXD DC-LIN node A
2 DC powerline
3 example of TX phases
4 phase shifts
5 example of TX phases
6 byte field sync preamble
7 byte field sync preamble – TX phases
8 byte field sync preamble – phase shifts
9 consecutive byte field transmission
10 Inter-byte space < 1/3 t_{BIT}
11 first byte field transmission
a Start.
b Stop.

Figure 5 — Example of byte field sync preamble modulation of consecutive byte field TX

Table 2 specifies the reference phase length and value.

Table 2 — Reference phase length and value definition

Parameter	Description	Phase	Min. phase length	Max. phase length	Unit
P_{ref_first}	Reference phase of a first byte field transmission (shown in Figure 4)	0°	2/9	1/3	t_{BIT}
P_{ref_consec}	Reference phase of a consecutive byte field transmission (shown in Figure 5)	Last byte field transmitted phase (0°/90°/180°/270°)	1/3	2/3	t_{BIT}

4.2.2.3 Byte field sync preamble modulation

Upon detection of falling edge of a start bit (t_{SB_TX}) from the data link layer, a byte field sync preamble modulation transmission shall start on line-out.

Table 3 specifies the start time of a byte field sync preamble transmission.

Table 3 — Start time of byte field sync preamble transmission definition

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SB_TX}	Start time of byte field sync preamble transmission on line-out (shown in Figure 4)	—	—	2/16	t_{BIT}

The byte field sync preamble modulation shall consist of 18 phase shifts.

The nominal length of modulated byte field sync preamble ($P_{sync\_pre\_len}$) is given in Formula (2).

Definition of the formula:

$$P_{sync\_pre\_len} = 2\ t_{BIT} \quad (2)$$

Table 4 specifies the byte field sync preamble phase shifts.

Table 4 — Byte field sync preamble phase shifts definition

Parameter	Description	Phase shift	Phase length
P_{sp_1}	Sync preamble 1st phase shift	+90°	1/9 t_{BIT} (shown in Figure 4 and Figure 5)
P_{sp_2}	Sync preamble 2nd phase shift	+90°	
P_{sp_3}	Sync preamble 3rd phase shift	−90°	
P_{sp_4}	Sync preamble 4th phase shift	+90°	
P_{sp_5}	Sync preamble 5th phase shift	−90°	
P_{sp_6}	Sync preamble 6th phase shift	−90°	
P_{sp_7}	Sync preamble 7th phase shift	+90°	
P_{sp_8}	Sync preamble 8th phase shift	+90°	
P_{sp_9}	Sync preamble 9th phase shift	−90°	
P_{sp_10}	Sync preamble 10th phase shift	+90°	
P_{sp_11}	Sync preamble 11th phase shift	−90°	
P_{sp_12}	Sync preamble 12th phase shift	−90°	
P_{sp_13}	Sync preamble 13th phase shift	+90°	
P_{sp_14}	Sync preamble 14th phase shift	+90°	
P_{sp_15}	Sync preamble 15th phase shift	−90°	
P_{sp_16}	Sync preamble 16th phase shift	+90°	
P_{sp_17}	Sync preamble 17th phase shift	−90°	
P_{sp_18}	Sync preamble 18th phase shift	−90°	

4.2.2.4 Byte field data bit modulation

Upon completion of the byte field sync preamble transmission period ($P_{sync\_pre\_len}$), the DC-LIN EPL shall transmit a byte field data bit modulation, bit-by-bit, for each one of the eight data bits transmitted from the data link layer.

The byte field data bit modulation shall consist of three phase shifts.

The nominal length of a modulated byte field data bit ($P_{data\_bit\_len}$) is given in Formula (3).

Definition of the formula:

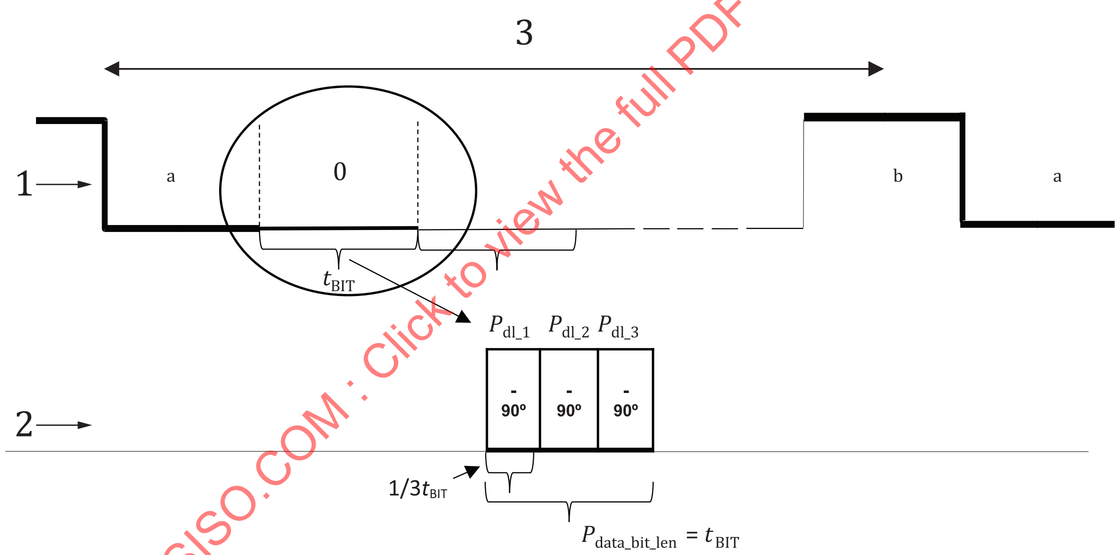
$$P_{data\_bit\_len} = 1\ t_{BIT} \quad (3)$$

Table 5 specifies the phase shift of the byte field data bit modulation.

Table 5 — Byte field data bit phase shift modulation definition

Data bit value	Parameter	Description	Phase shift	Phase length	Condition/ comment
1	P_{dh_1}	1st phase shift	+90°	1/3 t_{BIT}	$L_{out\_err\_cond}$ is inactive (see 4.5.3)
	P_{dh_2}	2nd phase shift	+90°		
	P_{dh_3}	3rd phase shift	+90°		
0	P_{dl_1}	1st phase shift	−90°		
	P_{dl_2}	2nd phase shift	−90°		
	P_{dl_3}	3rd phase shift	−90°		

Figure 6 shows a bit modulation example of data bit ‘0’.



Key

1 TXD

2 DC powerline

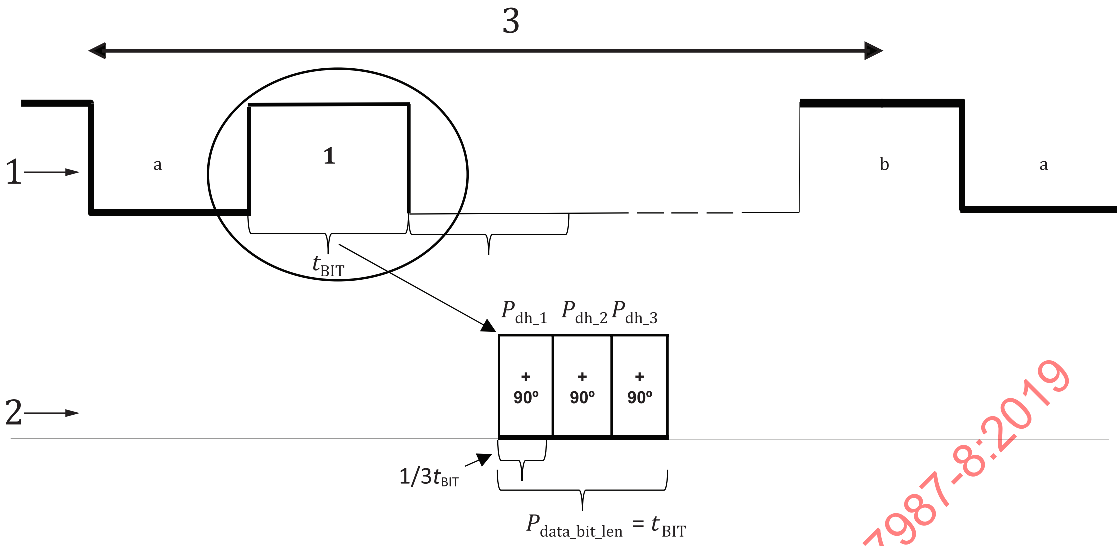
3 byte field

a Start.

b Stop.

Figure 6 — Example of bit ‘0’ modulation

Figure 7 shows a bit modulation example of data bit ‘1’.



Key

1 TXD
2 DC powerline
3 byte field
a Start.
b Stop.

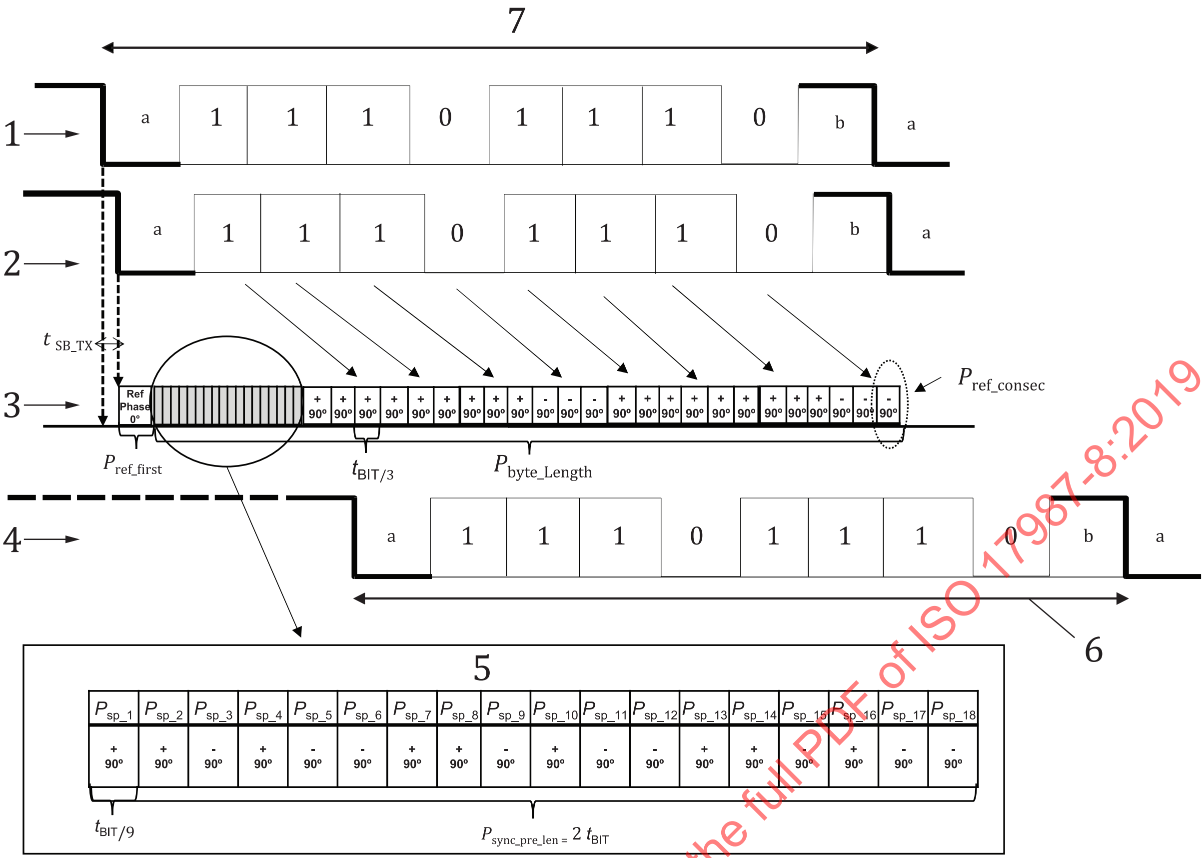
Figure 7 — Example of data bit '1' modulation

The nominal length of one modulated byte (P_{byte_length}) is given in Formula (4).

Definition of the formula:

$$P_{byte\_length} = P_{sync\_pre\_len} + 8 \times P_{data\_bit\_len} = 10\ t_{BIT} \quad (4)$$

Figure 8 shows an example of modulation scheme of data byte 01110111_2.



Key

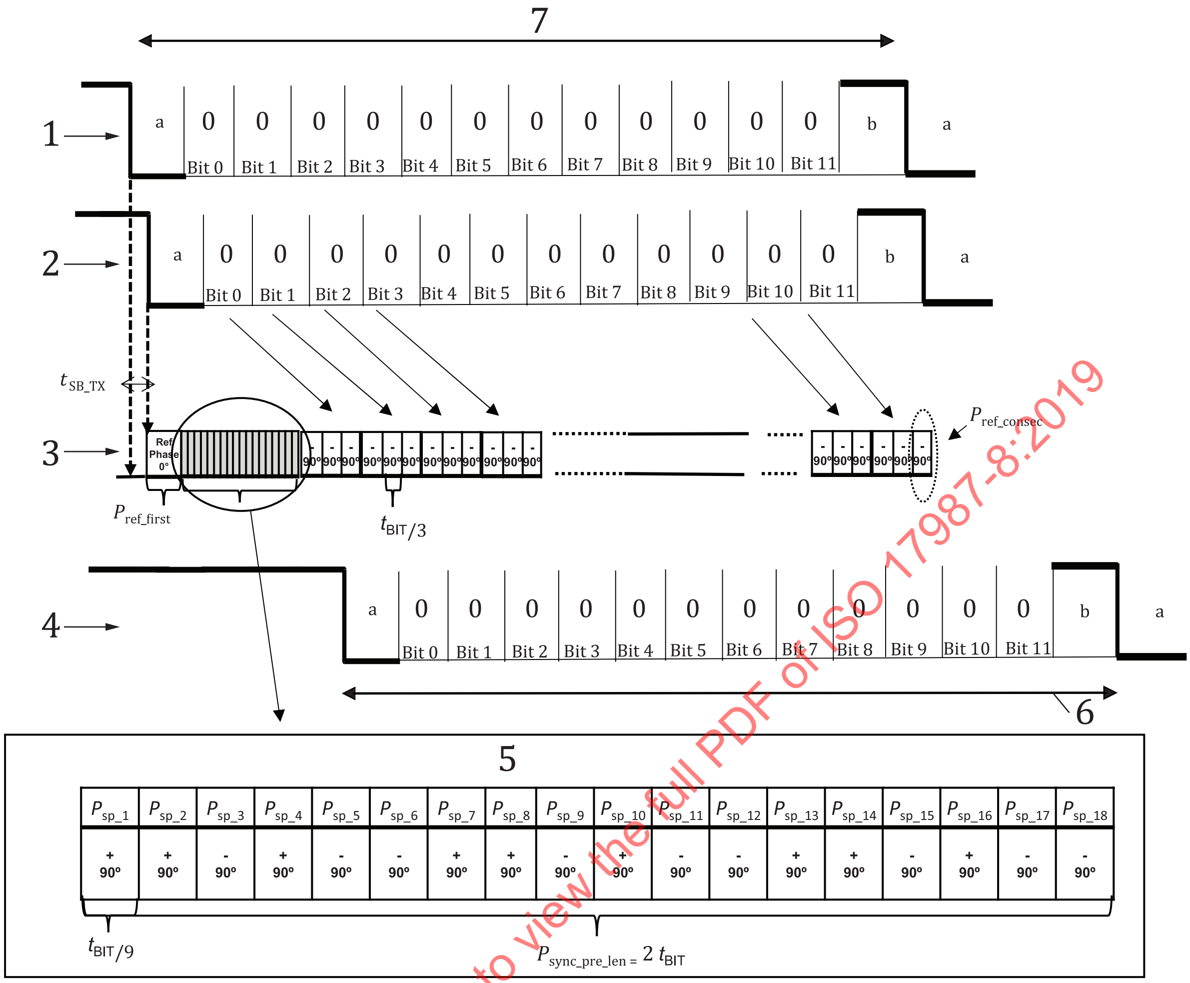
1 TXD DC-LIN node A
2 RXD DC-LIN node A
3 DC powerline
4 RXD DC-LIN node B
5 byte field sync preamble
6 DC-LIN byte field reception of node B
7 DC-LIN byte field transmission of node A
[a] Start.
[b] Stop.

Figure 8 — Example of a byte modulation scheme between a transmitting node A and receiving node B

4.2.3 Break field modulation scheme

The DC-LIN EPL shall transmit the break field over the DC powerline with the number of bits of the detected break field on TXD. The break field modulation scheme is the same as the byte field modulation scheme, but all data bits are ‘0’s.

Figure 9 shows an example of break field modulation transmission.



Key

1 TXD DC-LIN node A

2 RXD DC-LIN node A

3 DC powerline

4 RXD DC-LIN node B

5 byte field sync preamble

6 DC-LIN break field reception of node B

7 DC-LIN break field transmission of node A

a Start.

b Break delimiter.

Figure 9 — Example of a break field modulation transmission between a transmitting node A and receiving node B

4.2.4 Wake-up signal modulation scheme

The wake-up signal modulation is subject to the wake-up signal length on TXD (as specified in ISO 17987-2:2016, 5.3.1) and shall be transmitted either as a byte field modulation or as a break field modulation.

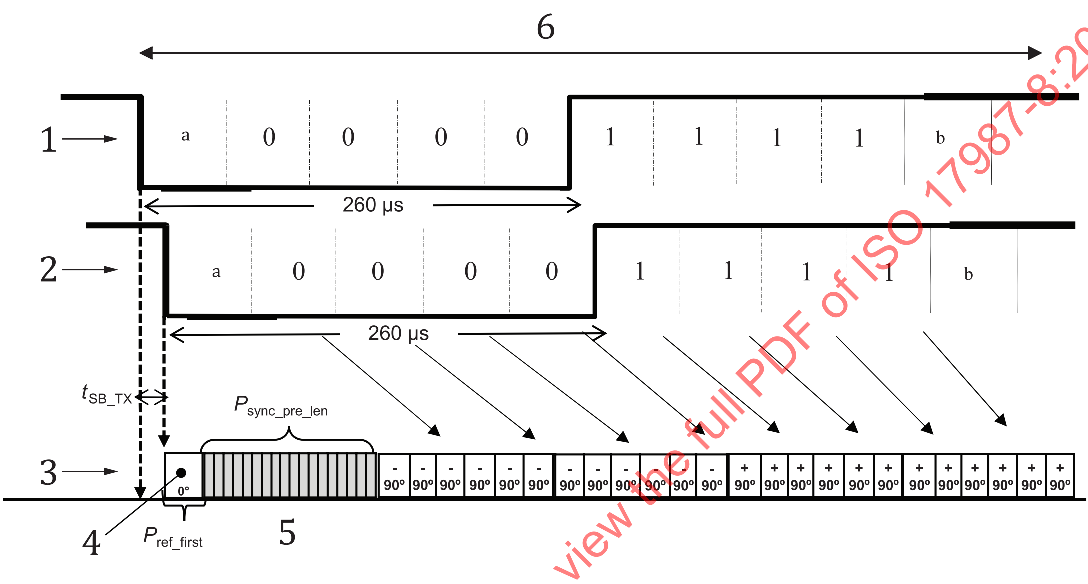
When the wake-up signal length on TXD is at least 10 t_{BIT} (i.e. a break field), the wake-up signal modulation shall be transmitted as a break field modulation scheme (see 4.2.3).

When the wake-up signal length on TXD is less than 10 t_{BIT}, the wake-up signal modulation shall be transmitted as a byte field modulation scheme (see 4.2.2.4) consisting of ‘0’ and ‘1’ data bit modulation (i.e. the wake-up signal is padded with ‘1’ data bit modulation to a complete byte field modulation transmission).

Figures 10, 11, and 12 show examples of a wake-up signal modulation transmission by a DC-LIN EPL that is set to BR_19_2K.

EXAMPLE Figure 10 depicts a wake-up signal with the length of 260 µs. The wake-up signal is encoded by the DC-LIN EPL to a start bit, four ‘0’ data bits, four ‘1’ data bits and a stop bit (i.e. $F0_{16}$).

The wake-up signal modulation is similar to a $F0_{16}$ byte field modulation.



Key

1 TXD wake-up signal DC-LIN node A

2 RXD wake-up signal DC-LIN node A

3 DC powerline

4 ref phase 0°

5 byte field sync preamble

6 DC-LIN wake-up signal transmission of node A

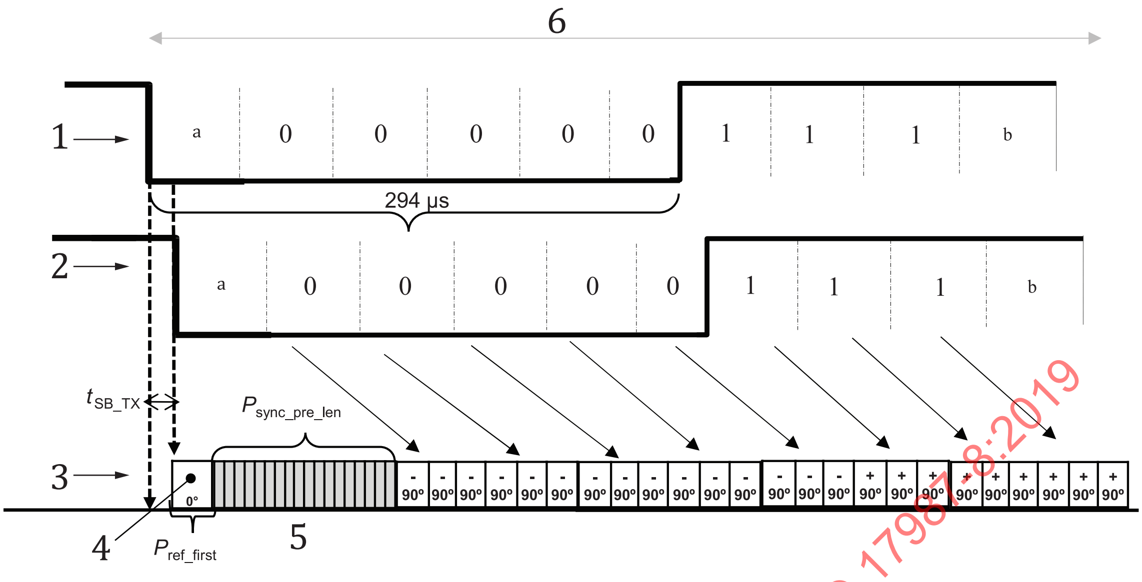
a Start.

b Stop.

Figure 10 — Example of a wake-up signal modulation similar to byte field modulation

EXAMPLE Figure 11 depicts a wake-up signal with the length of 294 µs. The wake-up signal is encoded by the DC-LIN EPL to a start bit, five ‘0’ data bits, three ‘1’ data bits and a stop bit (i.e. $E0_{16}$).

The wake-up signal modulation is similar to a $E0_{16}$ byte field modulation.



Key

1 TXD wake-up signal DC-LIN node A

2 RXD wake-up signal DC-LIN node A

3 DC powerline

4 ref phase 0°

5 byte field sync preamble

6 DC-LIN wake-up signal transmission of node A

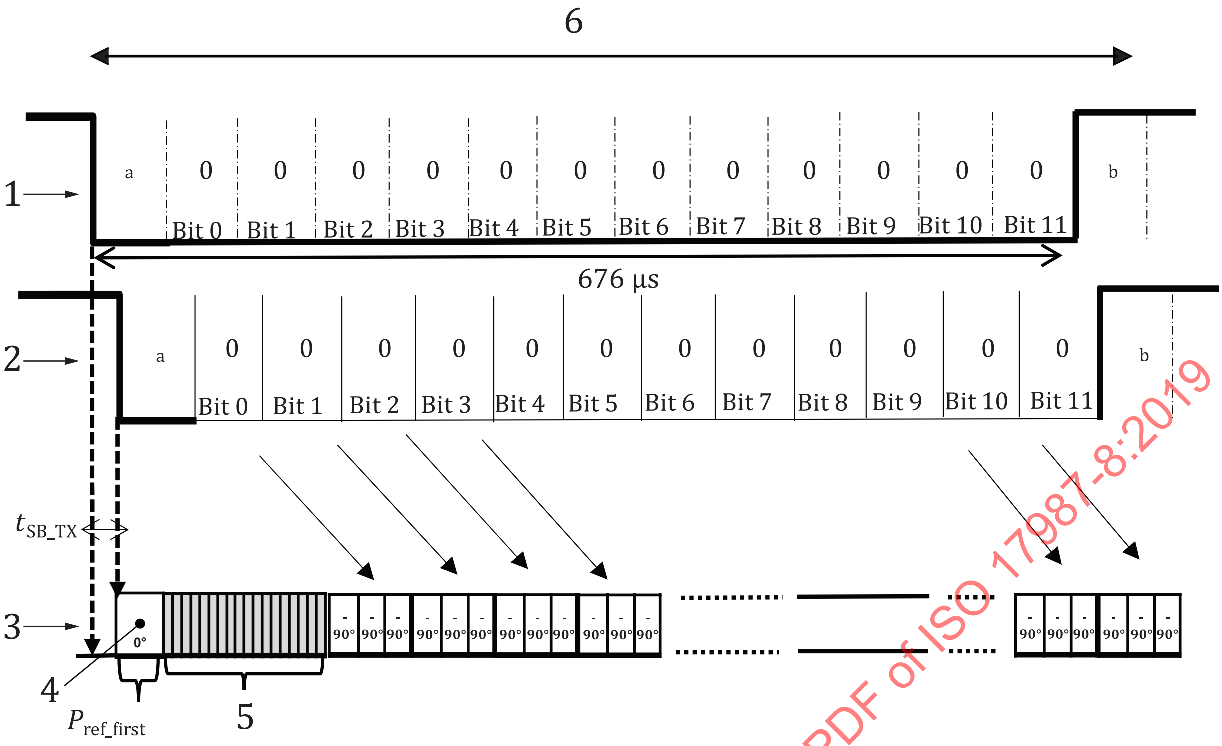
a Start.

b Stop.

Figure 11 — Example of a wake-up signal modulation similar to byte field modulation

EXAMPLE Figure 12 depicts a wake-up signal with the length of 676 µs. The wake-up signal is encoded by the DC-LIN EPL to a start bit, twelve '0' data bits and a stop bit (i.e. a break field).

The wake-up signal modulation is then similar to a break field modulation.



Key

1 TXD wake-up signal DC-LIN node A
2 RXD wake-up signal DC-LIN node A
3 DC powerline
4 ref phase 0°
5 byte field sync preamble
6 DC-LIN wake-up signal transmission of node A
[a] Start.
[b] Stop.

Figure 12 — Example of a wake-up signal modulation similar to break field modulation

4.3 Timing requirements

4.3.1 Bit rate tolerance

The bit rate tolerance describes the allowed deviation of the actual bit rate from the nominal bit rate for a DC-LIN EPL.

Table 6 specifies the bit rate tolerances for both master node and slave node DC-LIN EPL.

Table 6 — DC-LIN EPL bit rate tolerances

Bit rate	Deviation
BR_9_6K	<±0,5 %
BR_10K	<±0,5 %
BR_19_2K	<±0,5 %

The specified DC-LIN EPL bit rate deviation provides sufficient nominal bit rate, which is complying with EPL sync byte field quantization automatic bit rate detection as specified in ISO 17987-4:2016, 5.2.2, and with EPL bit rate deviation specified in ISO 17987-4:2016, 5.1.

4.3.2 Bit timing

The bit time is defined according to the selected bit rate (given in Table 6).

Calculation of a bit time is given in Formula (5).

Definition of the formula:

$$t_{BIT} = 1/(BR) \tag{5}$$

4.3.3 Bit sample timing

The bit sample timing on TXD shall apply the bit sampling timing specified in ISO 17987-4:2016, 5.2.3.

4.3.4 TXD assert timeout event

The minimum TXD assert ('0') time without timeout event is given in Formula (6).

Definition of the formula:

$$t_{txd\_min\_assert} = 6\ \text{ms} \tag{6}$$

The minimum TXD deassert ('1') time after timeout event (i.e. timeout recovery time) is given in Formula (7).

Definition of the formula:

$$t_{txd\_min\_recover} = 10\ t_{BIT} \tag{7}$$

Optionally, the DC-LIN EPL may detect a TXD assert timeout event when TXD assert time > $t_{txd\_min\_assert}$.

At the occurrence of TXD assert timeout event, the DC-LIN EPL's T_{tx_mode} may be deactivated until the next falling edge on TXD, which ocuurs after TXD deassert ('1') time > $t_{txd\_min\_recover}$.

4.3.5 Delay between transmitted byte field (DC-LIN node A) and received byte field (DC-LIN node A)

The delay between transmitted byte field on TXD and the received byte field on RXD at a DC-LIN EPL node (locally) ($t_{RX\_delay\_local}$) is given in Formula (8).

Definition of the formula:

$$t_{RX\_delay\_local} = t_{SB\_TX} \tag{8}$$

4.3.6 Delay between transmitted byte field (DC-LIN node A) and received byte field (DC-LIN node B)

The delay between the transmitted byte field, over to the DC powerline, and the receiver reconstructed byte field (t_{RX_delay}) is given in Table 7.

The maximum process time at RX DC-LIN EPL side is given in Formula (9).

Definition of the formula:

$$t_{rx\_proc\_max} = 6/9\ t_{BIT} \tag{9}$$

The minimum process time at RX DC-LIN EPL side is given in Formula (10).

Definition of the formula:

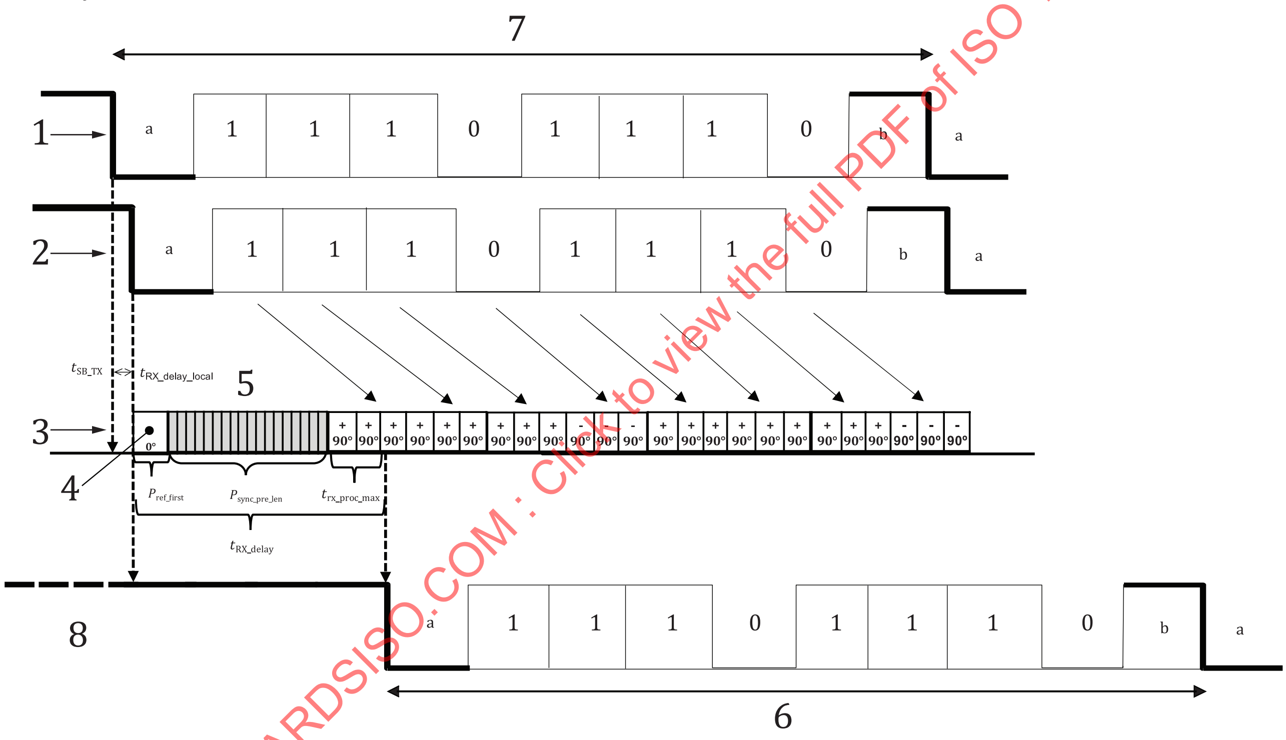
$$t_{rx\_proc\_min} = 2/9\ t_{BIT} \quad (10)$$

(The transmission delay on the DC powerline is negligible as compared to t_{BIT}, and hence not included in t_{RX_delay} calculation).

Table 7 — Delay between TXD (DC-LIN EPL node A) to RXD (DC-LIN EPL node B)

Parameter	Min.	Typ.	Max.	Unit	Condition / comment
t_{RX_delay}	22/9	—	25/8	t_{BIT}	$t_{RX\_delay\_max} = t_{SB\_TX}$ (2/16) + P_{ref_first} (3/9) + $P_{sync\_pre\_len}$ (18/9) + $t_{rx\_proc\_max}$ (6/9); $t_{RX\_delay\_min} = P_{ref\_first}$ (2/9) + $P_{sync\_pre\_len}$ (18/9) + $t_{rx\_proc\_min}$(2/9)

Figure 13 shows an example of a single byte field transmission, demonstrating the $t_{RX\_delay\_max}$, and $t_{RX\_delay\_local}$.



Key

1 TXD DC-LIN node A
2 RXD DC-LIN node A
3 DC powerline
4 ref phase 0°
5 byte field sync preamble
6 DC-LIN byte field reception of node B
7 DC-LIN byte field transmission of node A
8 RXD DC-LIN node B
a Start.
b Stop.

Figure 13 — Delay between TXD and RXD over the powerline between a transmitting node A and receiving node B

4.4 Receiver characteristics

At the receiver node side, the DC-LIN EPL (e.g. node B) shall decode a received byte/break field modulation from DC-LIN EPL (e.g. node A) into bits transferred on RXD to the data link layer (see Figures 8 and 9).

DC-LIN EPL RX node (e.g. node B) error condition (RX_{err_cond}) is defined active when decoding of the received modulation from DC-LIN EPL (e.g. node A) results in detection of no phase shifts for the duration of at least 1 t_{BIT}. RX_{err_cond} shall remain active for the remaining duration until completion of transmission $B_{fe\_stop\_bit}$ to the data link layer (see Table 8 and Figure 18).

Table 8 specifies RXD behaviour at receiver DC-LIN EPL node side.

If not otherwise stated, RXD logic level shall be set to ‘1’.

Table 8 — RXD behaviour at DC-LIN EPL receiver node side

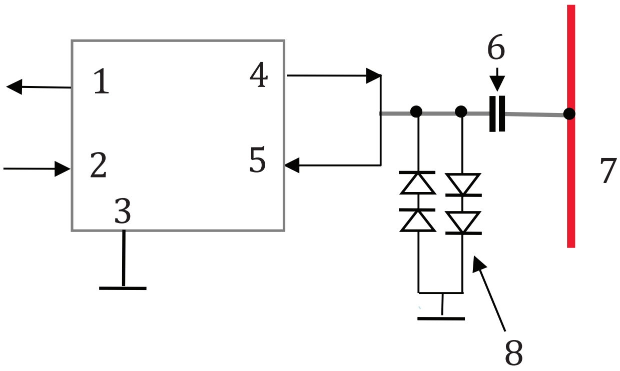
Parameter	RXD Logic level	Start time	Nominal bit length	Condition/comment
B_{start_bit}	Low (‘0’)	t_{RX_delay}	1 t_{BIT}	R_{rx_mode} is active
B_{data_bit}	Low (‘0’) when decoding bit modulation of data bit ‘0’ or High (‘1’) when decoding bit modulation of data bit ‘1’ or when RX_{err_cond} is active	t_{RX_delay} + 1 t_{BIT}	1 t_{BIT}	R_{rx_mode} is active The start time is defined for the first data bit (least significant bit), the rest of data bits are transmitted sequentially.
B_{stop_bit}	High (‘1’)	t_{RX_delay} + 9 t_{BIT}	1 t_{BIT}	R_{rx_mode} is active RX_{err_cond} is inactive Byte field receiving
$B_{fe\_stop\_bit}$	Low (‘0’)	t_{RX_delay} + 9 t_{BIT}	1 t_{BIT}	R_{rx_mode} is active RX_{err_cond} is active Byte field receiving
B_{del}	High (‘1’)	t_{RX_delay} +1 t_{BIT} + t_{break_field}	1 t_{BIT}	R_{rx_mode} is active RX_{err_cond} is inactive Break field receiving

4.5 Electrical parameters

4.5.1 General configuration — Coupling to the DC powerline

The coupling to the DC powerline may include a coupling capacitor and a protection network.

Figure 14 shows an example of a protection network using diodes.



Key

1 RXD receive data pin
2 TXD transmit data pin
3 GND
4 line-out
5 line-in
6 coupling capacitor
7 DC powerline
8 protection network

Figure 14 — Example of powerline coupling circuit with protection network

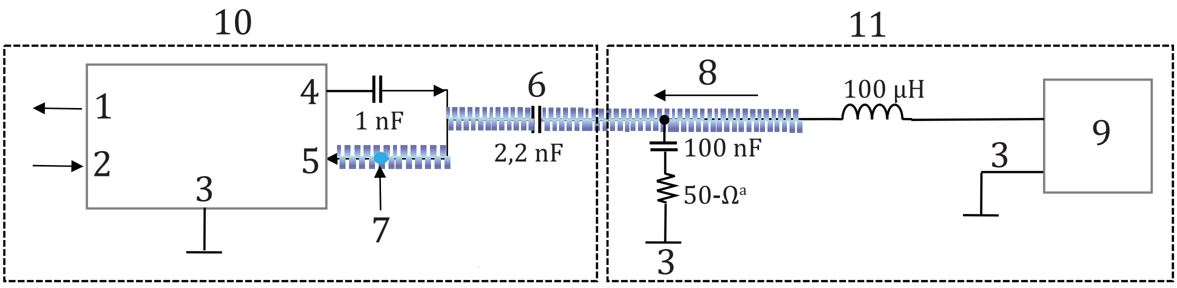
4.5.2 Signal specification

Table 9 specifies the electrical parameters of the DC-LIN EPL signal on the line-out and line-in.

Table 9 — Electrical parameters of the DC-LIN EPL

Symbol	Description	Min.	Typ.	Max.	Unit	Condition/comment
Line-in	Input voltage level at line-in pin	0,005	—	1,44	V	Volt peak-to-peak Measurement-point is between line-in and the coupling capacitor with 50-Ω load (shown in Figure 15).
	Line-in input impedance	5	—	—	kΩ	
Line-out	Output voltage level at line-out pin	0,96	1,2	1,44	V	Volt peak-to-peak Measurement-point is between line-in and the coupling capacitor with 50-Ω load (shown in Figure 16). T_{tx_mode} is active
	Output voltage level at line-out pin	0	—	0,1	V	Volt peak-to-peak Measurement-point is between line-in and the coupling capacitor with 50-Ω load (shown in Figure 16). T_{tx_mode} is inactive or low-power mode is active
	Line-out input impedance	100	—	—	kΩ	T_{tx_mode} is inactive or low-power mode is active

Figure 15 illustrates DC-LIN EPL line-in measure point test set-up.

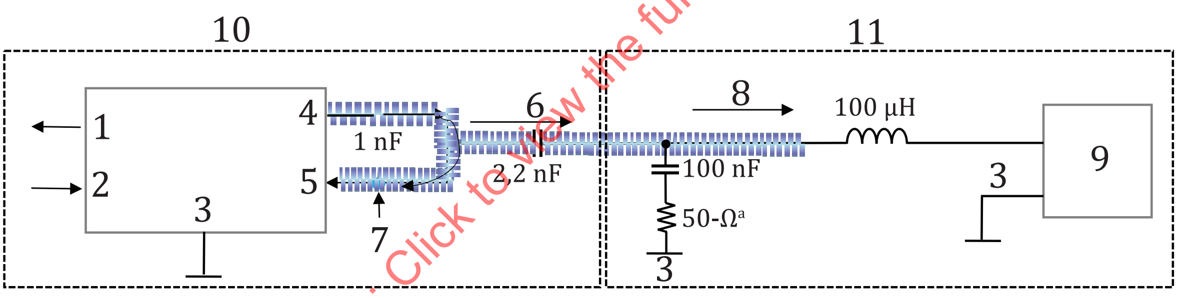


Key

1 RXD receive data pin
2 TXD transmit data pin
3 GND
4 line-out
5 line-in
6 coupling capacitor
7 RX signal level measure point
8 DC powerline
9 power supply
10 unit under test
11 test set-up
a Load.

Figure 15 — DC-LIN EPL line-in measurement-point: test set-up

Figure 16 illustrates DC-LIN EPL line-out measure point test set-up.



Key

1 RXD receive data pin
2 TXD transmit data pin
3 GND
4 line-out
5 line-in
6 coupling capacitor
7 TX signal level measure point
8 DC powerline
9 power supply
10 unit under test
11 test set-up
a Load.

Figure 16 — DC-LIN EPL line-out measurement-point: test set-up

4.5.3 Line-out monitoring

The DC-LIN EPL shall monitor its transmitted output level at line-out. The DC-LIN EPL line-out monitoring function shall provide an error indication on RXD to the data link layer in case the sampled line-out peak level is below $L_{out\_thr\_lev}$.

Table 10 specifies the line-out monitoring peak threshold level ($L_{out\_thr\_lev}$).

Table 10 — Line-out monitoring peak threshold level

Parameter	Description	Min.	Typ.	Max.	Unit
$L_{out\_thr\_lev}$	Line-out monitoring peak threshold level	25	—	50	mV

Start time of line-out monitoring ($t_{l\_out\_mon\_start}$) is given in Formula (11).

Definition of the formula:

$$t_{l\_out\_mon\_start} = t_{SB\_TX} \tag{11}$$

t_{SB_TX} is given in Table 3.

Line-out monitoring active duration ($t_{l\_out\_mon\_l}$) from t_{SB_TX} is given in Formula (12).

Definition of the formula:

$$t_{l\_out\_mon\_l} = 10\ t_{BIT} \tag{12}$$

The DC-LIN EPL shall sample the line-out level (L_{out_lev}) during line-out monitoring active duration at $t_{l\_out\_mon\_samp}$ for each detected bit on TXD (see Table 11). The sampled monitoring level shall be kept until next $t_{l\_out\_mon\_samp}$ (i.e. $t_{l\_out\_mon\_samp} + t_{BIT}$).

Table 11 specifies line-out monitoring sample time ($t_{l\_out\_mon\_samp}$) with respect to $t_{l\_out\_mon\_start}$.

Table 11 — Line-out monitoring sample time

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{l\_out\_mon\_samp}$	Line-out monitoring sample time	3/16	—	4/16	t_{BIT}

Line-out monitoring error condition ($L_{out\_err\_cond}$) is defined active when $L_{out\_lev} < L_{out\_thr\_lev}$, and shall stay active until completion of $t_{l\_out\_mon\_l}$. In case the transmit signal is constructed from more than one carrier frequency [i.e. $n > 1$, see Formula (1)], the $L_{out\_err\_cond}$ shall not be activated if at least one carrier frequency (e.g. c_2) out level is $\geq L_{out\_thr\_lev}$.

While $L_{out\_err\_cond}$ is active, and only after completion of byte field sync preamble transmission, the DC-LIN EPL shall change transmission from byte field modulation scheme to a constant phase (i.e. no phase shifts) transmission for the remaining transmission time (shown in Figure 18).

Table 12 specifies RXD behaviour at transmitter DC-LIN EPL node while TXD is active and according to L_{out_lev}.

If not otherwise stated, RXD logic level shall be set to '1'.

Table 12 — RXD behaviour at DC-LIN EPL transmitter node side

Parameter	RXD Logic level	Start time	Nominal bit length	Condition/comment
$B_{start\_bit\_local}$	Low ('0')	$t_{RX\_delay\_local}$	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is inactive ($L_{out\_lev} \geq L_{out\_thr\_lev}$)

Table 12 *(continued)*

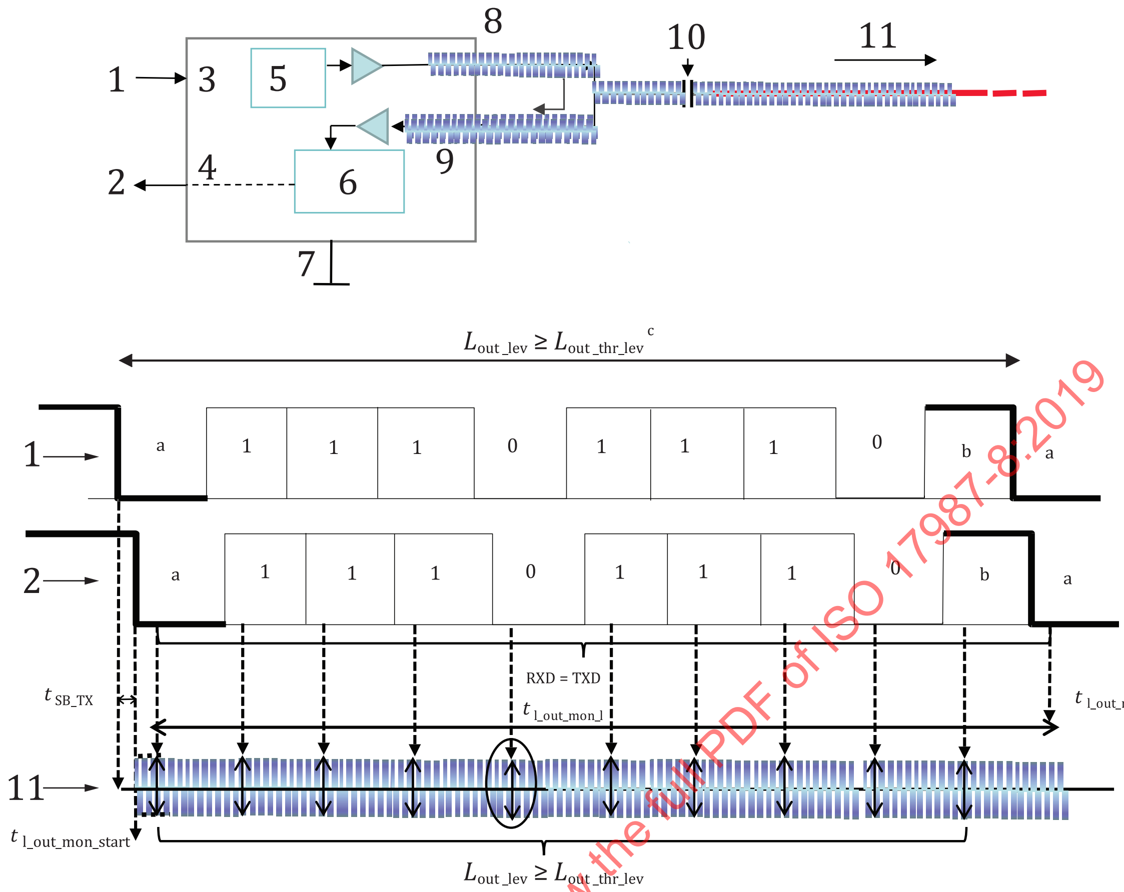
Parameter	RXD Logic level	Start time	Nominal bit length	Condition/comment
$B_{fe\_start\_bit\_local}$	High (‘1’)	$t_{l\_out\_mon\_samp}$	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is active ($L_{out\_lev} < L_{out\_thr\_lev}$) RXD indicates a start bit frame error to the data link layer.
$B_{data\_bit\_local}$	TXD	$t_{RX\_delay\_local}$ + 1 t_{BIT}	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is inactive ($L_{out\_lev} \geq L_{out\_thr\_lev}$) The start time is defined with respect to the first data bit (least significant bit), the other data bits are transmitted respectively with nominal bit length of 1 t_{BIT}.
$B_{err\_data\_bit\_local}$	$\overline{TXD}$	$t_{l\_out\_mon\_samp}$ + 1 t_{BIT}	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is active ($L_{out\_lev} < L_{out\_thr\_lev}$) The start time is defined with respect to the first data bit (least significant bit), the other data bits are transmitted respectively with nominal bit length of 1 t_{BIT}. RXD indicates an error to the data link layer.
$B_{stop\_bit\_local}$	High (‘1’)	$t_{RX\_delay\_local}$ + 9 t_{BIT}	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is inactive ($L_{out\_lev} \geq L_{out\_thr\_lev}$) Byte field transmission
$B_{fe\_stop\_bit\_local}$	Low (‘0’)	$t_{l\_out\_mon\_samp}$ + 9 t_{BIT}	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is active ($L_{out\_lev} < L_{out\_thr\_lev}$) The start time is defined with respect to $t_{l\_out\_mon\_samp}$ of start bit. Byte field transmission RXD indicates a stop bit frame error to the data link layer.
B_{del_local}	High (‘1’)	$t_{RX\_delay\_local}$ +1 t_{BIT} + t_{break_field}	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is inactive ($L_{out\_lev} \geq L_{out\_thr\_lev}$) Break field transmission

Table 12 *(continued)*

Parameter	RXD Logic level	Start time	Nominal bit length	Condition/comment
$B_{fe–del\_local}$	Low (‘0’)	$t_{l\_out\_mon\_samp}$ +1 t_{BIT} + t_{break_field}	1 t_{BIT}	T_{tx_mode} is active $L_{out\_err\_cond}$ is active (L_{out_lev} < $L_{out\_thr\_lev}$) The start time is defined with respect to $t_{l\_out\_mon\_samp}$ of start bit. Break field transmission. RXD indicates a break field delimiter frame error to the data link layer.

Figure 17 shows an example of line-out monitoring; where line-out level is not less than $L_{out\_thr\_lev}$ ($L_{out\_err\_cond}$ is inactive).

The data link layer of node A transmits a byte field on TXD. Node A DC-LIN EPL line-out monitoring is activated from t_{SB_TX} for the duration of $t_{L\_out\_mon\_l}$, where the line-out level (L_{out_lev}) is being sampled at $t_{l\_out\_mon\_samp}$ periodically every t_{BIT}.

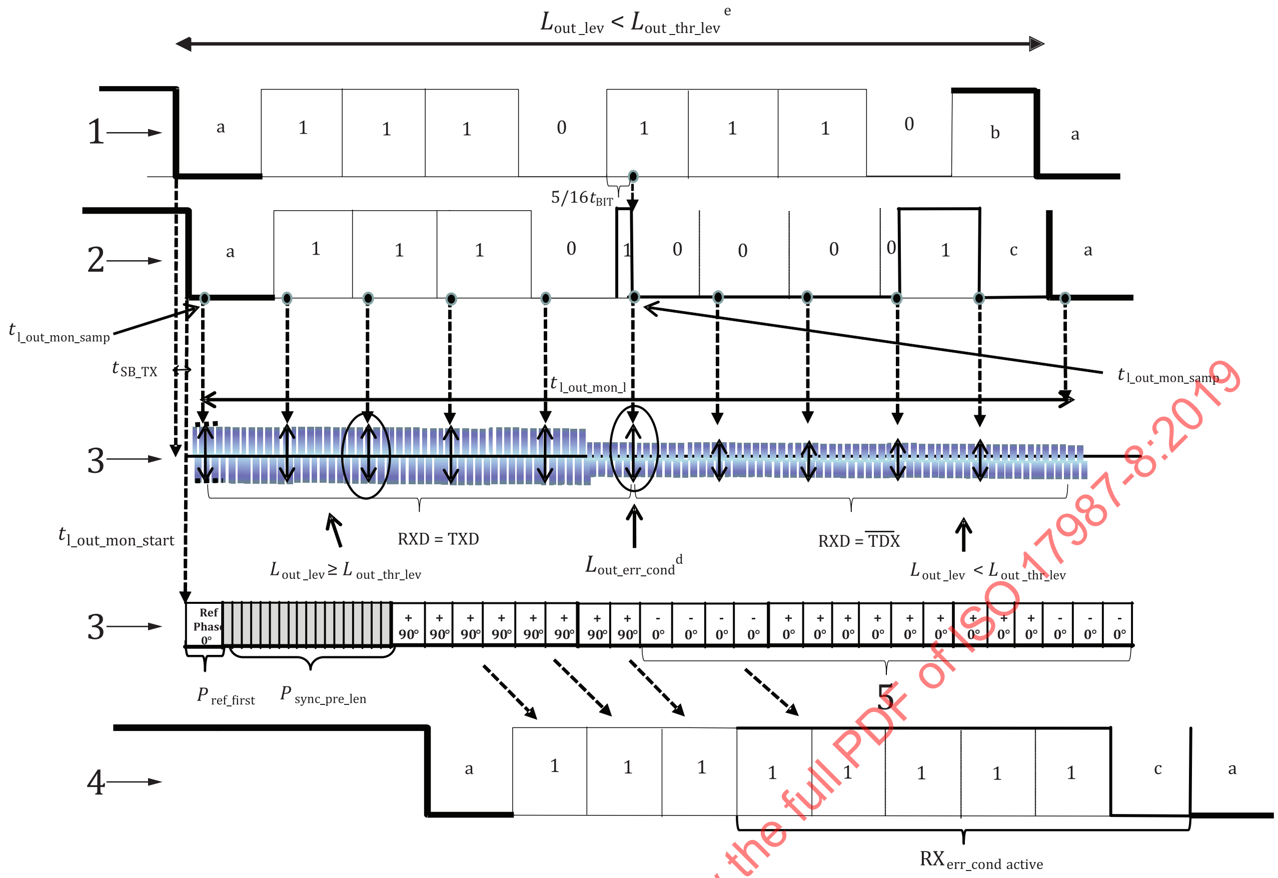


Key

1	TXD DC-LIN node A	8	line-out
2	RXD DC-LIN node A	9	line-in
3	TXD	10	coupling capacitor
4	RXD	11	DC powerline
5	modem	a	Start.
6	line-out monitoring logic	b	Stop.
7	GND	c	Line-out level is not less than the threshold level.

Figure 17 — Example of line-out monitoring: line-out level is not less than $L_{out\_thr\_lev}$

Figure 18 shows an example of line-out monitoring; where line-out level is lower than $L_{out\_thr\_lev}$ ($L_{out\_err\_cond}$ is active).



Key

1 TXD DC-LIN node A
2 RXD DC-LIN node A
3 DC powerline
4 RXD DC-LIN node B
5 no phase shifts
a Start.
b Stop.
c Stop bit frame error.
d Is triggered active.
e Line-out level is less than the threshold level.

Figure 18 — Example of line-out monitoring: line-out level is lower than $L_{out\_thr\_lev}$

4.5.4 ESD compliance

The DC-LIN EPL shall comply with requirements for protection against human body discharge according to IEC 61000-4-2. The minimum discharge voltage level shall be ±2 kV.

4.6 Communication in the presence of faults

Table 13 specifies the DC-LIN EPL behaviour in the presence of faults, in which there shall be no damage to the DC-LIN EPL.

Table 13 — DC-LIN EPL behaviour in the presence of faults

Description of fault	Communication behaviour
DC powerline becomes shorted to ground.	Data communication is not possible.
DC powerline is stuck in asserted state.	Data communication is not possible.
DC-LIN EPL's TXD is continuously asserted.	Data communication is not possible unless affected node has implemented TXD asserted timeout. functionality (see 4.3.4).
DC powerline is disconnected from power.	Remaining powered DC-LIN EPLs continue to communicate with no degradation.

Annex A
(informative)

DC-LIN EPL peripheral interface design considerations

An example for an interface between the DC-LIN EPL nodes and the DC powerline is shown in Figure A.1.

The example shows three DC-LIN EPL nodes connected to the DC powerline. To reduce the attenuation of the DC-LIN EPL carrier signal by filtering capacitors in power supplies, inductors or low-frequency ferrite beads are added in series to the power supply.

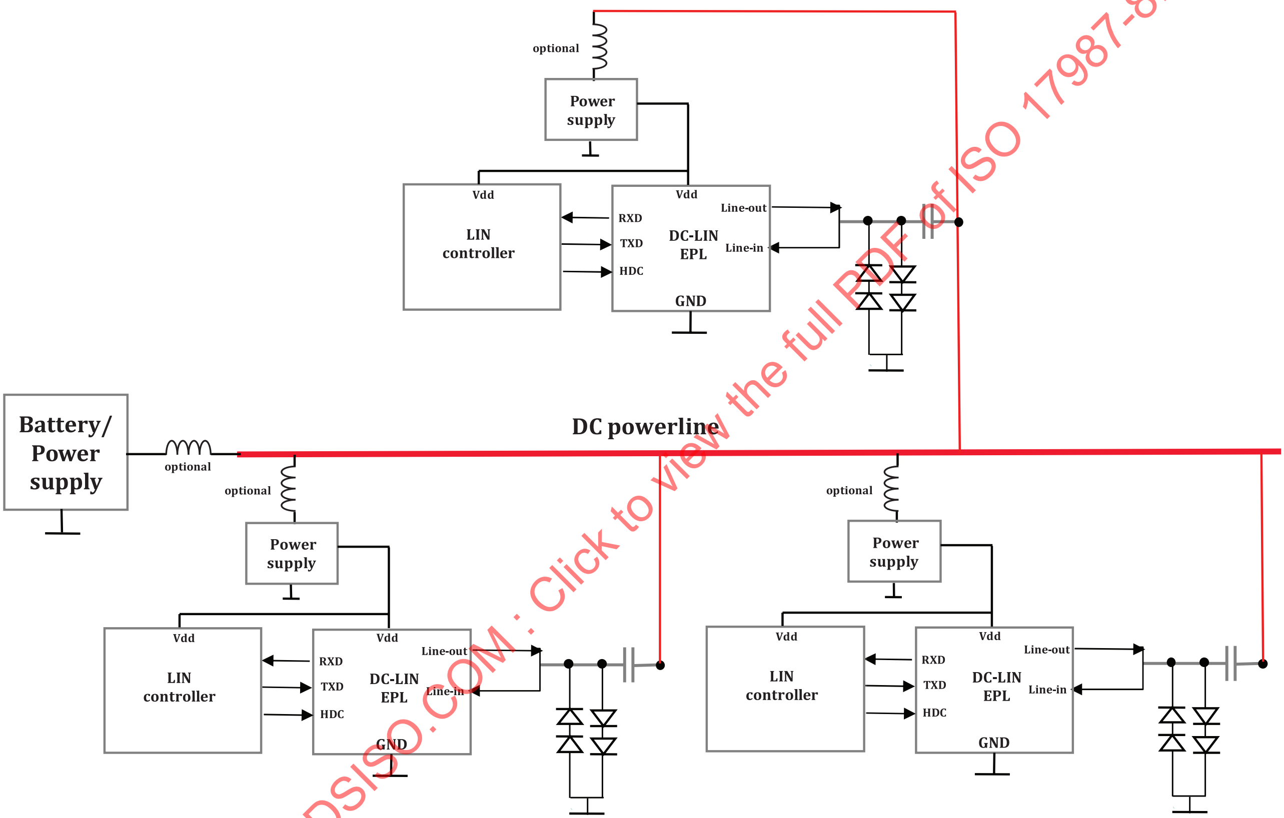


Figure A.1 — DC-LIN EPL coupling example

Annex B
(normative)

DC-LIN EPL conformance test plan

B.1 General

This annex specifies the DC-LIN EPL conformance test plan.

B.2 General test plan specification considerations

B.2.1 Test conditions

The tests shall be done at room temperature in a range of 15 °C to 35 °C.

B.2.2 Test case structure

In the description of each test case, it is specified, for which DC-LIN EPL type the test case is applicable, for master or slave node.

Each specification of a test case consists of nine parts.

- CTC # – Title
  - A common prefix for the conformance test case.
- Purpose
  - Brief statement outlining what the test case attempts to achieve.
- Reference
  - Defines the reference to this or other parts of the ISO 17987 series.
- Prerequisite
  - Defines the test set-up.
- Set-up
  - Defines the IUT configuration (see B.2.4.5).
- Step
  - Defines the test step/s for carrying out the test case.

  — If more than one step is defined in this field, the steps shall be executed in the order as they are stated in the document.

— Iteration

  — Defines the number of repetitions of test procedure test steps.

— Expected response

  — Defines the expected behaviour of the IUT when executing the test steps.

— Remark

  — Contains a description of known issues with the test case, which can affect test results in certain situations.

B.2.3 IUT general specification

IUT with RXD and TXD connectors available and line-in and line-out connector available is applicable for the DC-LIN EPL test cases specified in this document.

B.2.4 Test system requirements

B.2.4.1 Generation of LIN frames

The test system shall ensure the precision of the bit time of a master node as specified in this document.

B.2.4.2 Normal requirements for the test cases

For proper measurement and verification of tests pattern (see Table B.1), the test system shall use a minimum over sampling factor of 16; see Formula (B.1).

The definition of the sample resolution is given in Formula (B.1).

Definition of the formula:

$$\text{sample resolution} = t_{\text{BIT}} / 16 \quad \text{(B.1)}$$

B.2.4.3 Special requirements for bit timing testing

For proper measurement and verification of the bit timing tests, the test system shall measure with a minimum over sampling of 10 to the precision of a DC-LIN EPL bit rate deviation given in this document, Table 6; see Formula (B.2).

The definition of the bit time sample resolution is given in Formula (B.2).

Definition of the formula:

$$\text{bit time sample resolution} = t_{\text{BIT}} \times 0{,}000\,5 \quad \text{(B.2)}$$

B.2.4.4 Test system configuration

A detailed test system configuration is given under the test cases definitions. The test system shall be implemented in a way that the test cases can be performed as specified and reproducible.

B.2.4.5 General predefinitions for IUT configuration

B.2.4.5.1 General

Before executing a test case, some settings shall be done by LT concerning:

— the IUT initialization:

  — an initialization of the IUT shall be performed by the LT before each test case. To initialize the IUT a reset is carried out and thereafter the IUT shall be reconfigured;

— the IUT as master or slave node:

  — specifies to what state the IUT shall have been set before starting the execution of the test. If not otherwise defined, the IUT as master node T_{tx_mode} is active and the IUT as slave node R_{rx_mode} is active;

— the test pattern to be sent by the LT on TXD of the IUT or to stimulate the IUT line-in;

— the IUT bit rate configuration;

— the IUT transmit signal number of carrier frequencies;

— the IUT working carrier frequency configuration.

B.2.4.5.2 IUT TXD test pattern specification

Table B.1 specifies the test pattern to be sent on TXD of IUT in test cases.

Table B.1 — IUT TXD test pattern specification

Test pattern	Requirements for the test pattern
TST_BYTE_55	Single byte field 55_{16}
TST_BYTE_7A	Single byte field $7A_{16}$
TST_BYTE_65	Single byte field 65_{16}
TST_BYTE_5F	Single byte field $5F_{16}$
TST_BREAK_FIELD	Break field with length of 13 t_{BIT} and break delimiter of 1 t_{BIT}
TST_WAKEUP_SIGNAL_SHORT	Wake-up signal with length of 260 µs
TST_WAKEUP_SIGNAL_LONG	Wake-up signal with length of 4 992 µs

B.2.4.5.3 Transmit signal test pattern specification

The transmit signal test pattern shall comply with transmitter characteristics specified in this document (see 4.2, and its subclauses).

Table B.2 specifies the transmit signal test pattern to be sent over the powerline in test cases.

Table B.2 — Transmit signal test pattern specification

Test pattern	Requirements for the transmit signal test pattern	Transmit signal phases	Phase length	Remarks
TXS_S_BYTE_55	Single byte field modulation of byte field 55_{16}	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, and 0°.	1/3 t_{BIT}	P_{data}
TXS_BYTE_7A_CON-SEC_55	Two consecutive bytes field modulation. First byte field $7A_{16}$ with an inter-byte space no longer than 1/3 t_{BIT}, followed by byte field 55_{16}.	0°	1/3 t_{BIT}	P_{ref_first} of the first byte field
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p} of the first byte field
		90°, 180°, 270, 0°, 90°, 180°, 270°, 0°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 0°, 90°, 180°, 90°, 0°, 270°, 0°, 90°, and 180° (P_{ref_consec}).	1/3 t_{BIT}	P_{data} of the first byte field Last transmitted P_{data} is the P_{ref_consec} of the second byte field.
		270°, 0°, 270°, 0°, 270°, 180°, 270°, 0°, 270°, 0°, 270°, 180°, 270°, 0°, 270°, 0°, 270°, and 180°.	1/9 t_{BIT}	P_{sync_p} of the second byte field
		270°, 0°, 90°, 0°, 270°, 180°, 270°, 0°, 90°, 0°, 270°, 180°, 270°, 0°, 90°, 0°, 270°, 180°, 270°, 0°, 90°, 0°, 270°, and 180°.	1/3 t_{BIT}	P_{data} of the second byte field

Table B.2 *(continued)*

Test pattern	Requirements for the transmit signal test pattern	Transmit signal phases	Phase length	Remarks
TXS_BYTE_55_CONSEC_55_CONSEC_55	Three consecutive bytes field modulation of byte field 55_{16} with an inter-byte space no longer than 1/3 t_{BIT} between the first byte and the second byte, and with an inter-byte space longer than 1/3 t_{BIT} between the second byte and the third byte	0°	1/3 t_{BIT}	P_{ref_first} of the first byte field
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p} of the first byte field
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, and 0° (P_{ref_consec}).	1/3 t_{BIT}	P_{data} of the first byte field Last transmitted P_{data} is the P_{ref_consec} of the second byte field.
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p} of the second byte field
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, and 0°.	1/3 t_{BIT}	P_{data} of the second byte field
		0°	1/3 t_{BIT}	P_{ref_first} of the third byte field
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p} of the third byte field
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, and 0°.	1/3 t_{BIT}	P_{data} of the third byte field
TXS_S_BYTE_55_ERR_COND_N2	Single byte field modulation of byte field 55_{16} with $L_{out\_err\_cond}$ triggered at data bit 2.	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		90°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, and 0°.	1/3 t_{BIT}	P_{data}
TXS_S_BYTE_55_ERR_COND_N4	Single byte field modulation of byte field 55_{16} with $L_{out\_err\_cond}$ triggered at data bit 4.	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, and 0°.	1/3 t_{BIT}	P_{data}
TXS_S_BYTE_55_ERR_COND_N6	Single byte field modulation of byte field 55_{16} with $L_{out\_err\_cond}$ triggered at data bit 6.	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, 0°, and 0°.	1/3 t_{BIT}	P_{data}

Table B.2 *(continued)*

Test pattern	Requirements for the transmit signal test pattern	Transmit signal phases	Phase length	Remarks
TXS_S_BYTE_7A	Single byte field modulation of byte field $7A_{16}$	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		270°, 180°, 90°, 180°, 270°, 0°, 270°, 180°, 90°, 180°, 270°, 0°, 90°, 180°, 270°, 0°, 90°, 180°, 270°, 0°, 90°, 0°, 270°, and 180°	1/3 t_{BIT}	P_{data}
TXS_S_BYTE_65	Single byte field modulation of byte field 65_{16}	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 180°, 270°, 0°, 90°, 180°, 270°, 180°, 90°, and 0°.	1/3 t_{BIT}	P_{data}
TXS_S_BYTE_5F	Single byte field modulation of byte field $5F_{16}$	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		90°, 180°, 270°, 0°, 90°, 180°, 270°, 0°, 90°, 180°, 270°, 0°, 90°, 180°, 270°, 180°, 90°, 0°, 90°, 180°, 270°, 180°, 90°, and 0°.	1/3 t_{BIT}	P_{data}
TXS_BREAK_FIELD	Break field modulation with length of 13 t_{BIT}	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		270°, 180°, 90°, 0°, 270°, 180°,90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, and 0°.	1/3 t_{BIT}	P_{data} 12 data bit ‘0’
TXS_WAKEUP_SIGNAL_SHORT	Wake-up signal modulation with length of 260 µs	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°,90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 90°, 180°, ,270°, 0°, 90°, 180°, 270°, 0°, 90°, 180°, 270°, and 0°.	1/3 t_{BIT}	P_{data} 4 data bit ‘0’ 4 data bit ‘1’

Table B.2 *(continued)*

Test pattern	Requirements for the transmit signal test pattern	Transmit signal phases	Phase length	Remarks
TXS_WAKEUP_SIGNAL_LONG	Wake-up signal modulation with length of 4 992 µs	0°	1/3 t_{BIT}	P_{ref_first}
		90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, 0°, 90°, 180°, 90°, 180°, 90°, and 0°.	1/9 t_{BIT}	P_{sync_p}
		{270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, and 0°} Repeated 7 times followed by: 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, 270°, 180°, 90°, 0°, and 270°.	1/3 t_{BIT}	P_{data} 95 data bit ‘0’

B.2.4.5.4 Default delays for frame headers

If not otherwise specified, the delay between frame headers is specified in Table B.3.

Table B.3 — Default delays for frame headers

Bit rate	Delay
BR_19_2K	15 ms
BR_10K	20 ms
BR_9_6_K	20 ms

B.2.4.5.5 Default spaces between LIN frame fields

If not otherwise specified in the test cases, the inter-byte spaces between the header, the response field and the data fields are set to zero.

B.2.4.5.6 IUT default bit rate

The default bit rate is set to the highest bit rate that is specified by the specification of the IUT (i.e. BR_19_2K). Test cases with a different bit rate setting can only be performed when the required bit rate is in accordance with the specification of the IUT.

B.2.4.5.7 IUT default transmit signal number of carrier frequencies

If not specified otherwise in the test case, the default number of the IUT transmit signal carrier frequencies is set to 1.

CF_{max} is defined as the maximal number of carrier frequencies implemented in IUT transmit signal.

Test case specified with higher number of carrier frequencies setting can only be performed when the required number of carrier frequencies is in accordance with the specification and implementation of the IUT CF_{max}.

B.2.4.5.8 IUT default transmit signal carrier frequency

Table B.4 specifies the IUT default carrier frequencies configuration according to the IUT CF_{max} as specified in Table 1.

Table B.4 — IUT Default carrier frequencies configuration

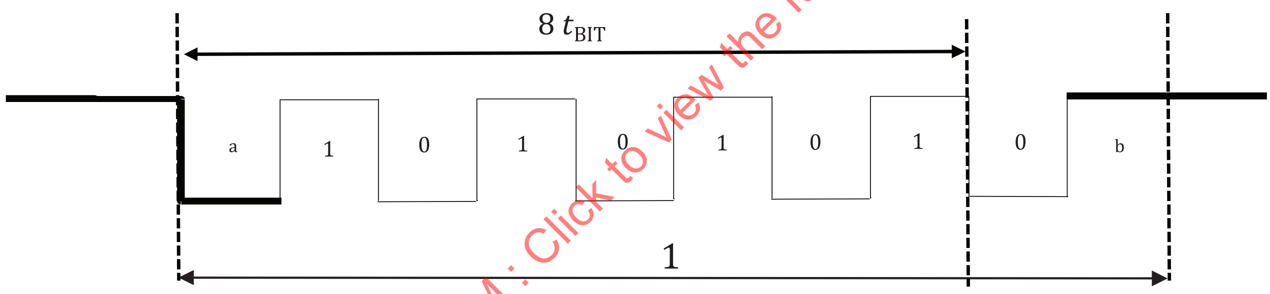
Number of transmit signal carriers (CF_{max})	Default carrier frequencies configuration	Unit
1	13	MHz
2	13 and 20	
3	13, 20 and 30	
4	5, 13, 20 and 30	

The maximal number of carrier frequencies (CF_{max}) constructing a DC-LIN EPL transmit signal is subject to the IUT implementation.

B.2.4.5.9 DC-LIN EPL TXD and RXD time measurements requirements

The time measurements of IUT TXD and RXD as master or slave node shall be done on TST_BYTE_55, between the start bit falling edge and the 5th falling edge, which is available in a distance of eight bit times. This allows a simple calculation of the basic bit time t_{BIT}.

Figure B.1 shows an example of TST_BYTE_55 byte field for time measurement.



Key

1 TST_BYTE_55

a Start.

b Stop.

Figure B.1 — Example of TST_BYTE_55 for time measurement

B.2.4.5.10 DC-LIN EPL line-out and line-in measurements requirements

Table B.5 specifies the line-out and line-in measurements requirements.

Table B.5 — Line-out and line-in measurements - Requirements

Measurement type	Minimum requirement
Carrier frequency	Oscilloscope: — 250 Mega samples/s — Rise time ≤ 3,5 ns — Bandwidth: 50 MHz — Voltage per division: 1 mV to 2 V
Phase length	
Phase shift value	

B.3 Transmitter characteristics timing

B.3.1 General

This subclause verifies if the DC-LIN EPL transmitter characteristics timing parameters of the IUT as master or slave node conform to the transmitter characteristics timing parameters that are specified in this document. The IUT is stimulated to transmit defined byte field/break field (lower tester) and the resulting behaviour is observed and compared with the expected behaviour (upper tester).

Figure B.2 depicts the test configuration of the test system 'Transmitter characteristics timing'.

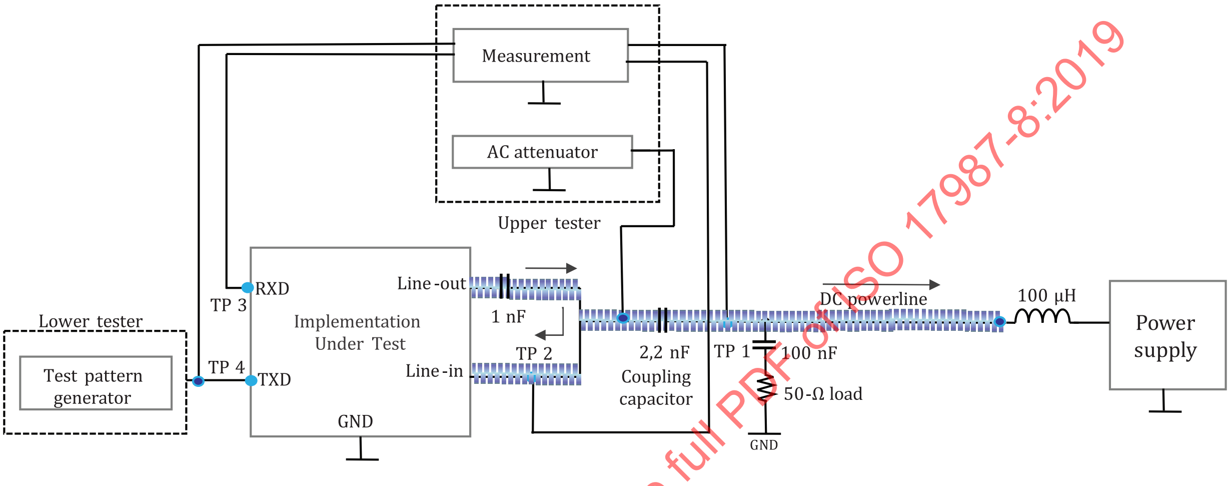


Figure B.2 — Test system: Transmitter characteristics timing

B.3.2 Transmit signal carrier frequencies

Table B.6 defines the test structure of CTC_TX_CHARC_1.

Table B.6 — Test structure of CTC_TX_CHARC_1

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_1 – Transmit signal carrier frequencies**
Purpose	This CTC verifies the correct carrier frequencies transmission, constructing the DC-LIN EPL transmit signal.
Reference	4.2.1
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 2 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 3 LT: Shall configure the IUT with CF_{max} transmit signal number of carrier frequencies (i.e. 1, 2, 3, or 4).
Step	1 LT: Shall send repeated TST_BYTE_55 on IUT TXD. 2 UT: Shall measure the corresponding carrier frequencies at TP 1 (see Figure B.2).
Iteration	Not applicable
Expected response	Step 2 The corresponding carrier frequencies measured at TP 1 (see Figure B.2) complies with Table 1 = OK.
Remark	—

B.3.3 Start time of byte field/s transmission

Table B.7 defines the test structure of CTC_TX_CHARC_2.

Table B.7 — Test structure of CTC_TX_CHARC_2

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_2 – Start time of byte field/s transmission**
Purpose	This CTC verifies that the start time of byte field/s transmission is according to t_{SB_TX}.
Reference	4.2.2.3 and 4.3.5
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 2 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 3 LT: Shall configure the IUT with CF_{max} transmit signal number of carrier frequencies (i.e. 1, 2, 3, or 4).
Step	1 LT: Shall send TST_BYTE_55 on IUT TXD. 2 UT: Shall measure the time from falling edge of start bit to IUT start of transmission at line-out at TP 1. 3 UT: Shall measure the time from falling edge of start bit to IUT falling edge of start bit at RXD at TP 3. 4 LT: Shall send two consecutive TST_BYTE_55 on IUT TXD with an inter-byte space no longer than 1/3 t_{BIT}. 5 UT: Shall measure the time from falling edge of start bit to IUT start of transmission at line-out at TP 1. 6 UT: Shall measure the time from falling edge of start bit to IUT falling edge of start bit at RXD at TP 3. 7 LT: Shall send three consecutive TST_BYTE_55 on IUT TXD with an inter-byte space no longer than 1/3 t_{BIT} between the first byte and the second byte, and with an inter-byte space longer than 1/3 t_{BIT} between the second byte and the third byte. 8 UT: Shall measure the time from falling edge of start bit to IUT start of transmission at line-out at TP 1. 9 UT: Shall measure the time from falling edge of start bit to IUT falling edge of start bit at RXD at TP 3.
Iteration	Not applicable
Expected response	Step 2 The time from falling edge of start bit to IUT start of transmission at line-out measured at TP 1 complies with t_{SB_TX} = OK. Step 3 The time from falling edge of start bit to IUT falling edge of start bit at RXD measured at TP 3 complies with $t_{RX\_delay\_local}$ = OK. Step 5 The time from falling edge of start bit to IUT start of transmission at line-out measured at TP 1 complies with t_{SB_TX} = OK. Step 6 The time from falling edge of start bit to IUT falling edge of start bit at RXD measured at TP 3 complies with $t_{RX\_delay\_local}$ = OK. Step 8 The time from falling edge of start bit to IUT start of transmission at line-out measured at TP 1 complies with t_{SB_TX} = OK. Step 9 The time from falling edge of start bit to IUT falling edge of start bit at RXD measured at TP 3 complies with $t_{RX\_delay\_local}$ = OK.
Remark	—

B.3.4 Length and value of reference phase

Table B.8 defines the test structure of CTC_TX_CHARC_3.

Table B.8 — Test structure of CTC_TX_CHARC_3

Item	Content	
CTC # – Title	**1.CTC_TX_CHARC_3 – Length and value of reference phase**	
Purpose	This CTC verifies the correct length and value of the reference phase.	
Reference	4.2.2.2	
Prerequisite	1	LT with the capability to stimulate, reset and configure the IUT.
	2	The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1	LT: Shall configure the IUT with default bit rate (see B.2.4.5.5).
	2	LT: Shall configure the IUT with default working carrier frequencies (see Table B.4).
	3	LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1	LT: Shall send TST_BYTE_55 on IUT TXD.
	2	UT: Shall measure the length and value of reference phase at TP 1.
	3	LT: Shall send TST_BYTE_7A on IUT TXD with an inter-byte space no longer than 1/3 t_{BIT}, followed by TST_BYTE_55.
	4	UT: Shall measure the length and value of first byte reference phase at TP 1.
	5	UT: Shall measure the length and value of second byte reference phase at TP 1.
	6	LT: Shall send three consecutive TST_BYTE_55 on IUT TXD with an inter-byte space no longer than 1/3 t_{BIT} between the first byte and the second byte, and with an inter-byte space longer than 1/3 t_{BIT} between the second byte and the third byte.
	7	UT: Shall measure the length and value of first byte reference phase at TP 1.
	8	UT: Shall measure the length and value of second byte reference phase at TP 1.
	9	UT: Shall measure the length and value of third byte reference phase at TP 1.
Iteration	Not applicable	
Expected response	Step 2	The length of reference phase measured at TP 1 complies with P_{ref_first} = OK, and the value of reference phase is 0° = OK.
	Step 4	The length of first byte reference phase measured at TP 1 complies with P_{ref_first} = OK, and the value of reference phase is 0° = OK.
	Step 5	The length of second byte reference phase measured at TP 1 complies with P_{ref_consec} = OK, and the value of reference phase is 180° = OK.
	Step 7	The length of first byte reference phase measured at TP 1 complies with P_{ref_first} = OK, and the value of reference phase is 0° = OK.
	Step 8	The length of second byte reference phase measured at TP 1 complies with P_{ref_consec} = OK, and the value of reference phase is 0° = OK.
	Step 9	The length of third byte reference phase measured at TP 1 complies with P_{ref_first} = OK, and the value of reference phase is 0° = OK.
Remark	—	

B.3.5 Length of byte field sync preamble phases

Table B.9 defines the test structure of CTC_TX_CHARC_4.

Table B.9 — Test structure of CTC_TX_CHARC_4

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_4 – Length of byte field sync preamble phases**
Purpose	This CTC verifies the correct length of the byte field sync preamble phases.
Reference	Table 4

Table B.9 *(continued)*

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_4 – Length of byte field sync preamble phases**
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 2 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 3 LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1 LT: Shall send TST_BYTE_55 on IUT TXD. 2 UT: Shall measure the length of each byte field sync preamble phases at TP 1.
Iteration	Not applicable
Expected response	Step 2 The length of each byte field sync preamble phases measured at TP 1 complies with Table 4 with tolerance of ±0,5 % = OK.
Remark	—

B.3.6 Values of byte field sync preamble phase shifts

Table B.10 defines the test structure of CTC_TX_CHARC_5.

Table B.10 — Test structure of CTC_TX_CHARC_5

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_5 – Values of byte field sync preamble phase shifts**
Purpose	This CTC verifies the correct values of the byte field sync preamble phase shifts.
Reference	Table 4
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 2 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 3 LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1 LT: Shall send TST_BYTE_55 on IUT TXD. 2 UT: Shall measure the value of byte field sync preamble phase shifts at TP 1.
Iteration	Not applicable
Expected response	Step 2 The value of byte field sync preamble phase shifts measured at TP 1 complies with Table 4 = OK.
Remark	—

B.3.7 Length of byte field data bit phases

Table B.11 defines the test structure of CTC_TX_CHARC_6.

Table B.11 — Test structure of CTC_TX_CHARC_6

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_6 – Length of byte field data bit phases**
Purpose	This CTC verifies the correct length of byte field data bit phases.
Reference	Table 5

Table B.11 *(continued)*

Item	Content	
CTC # – Title	**1.CTC_TX_CHARC_6 – Length of byte field data bit phases**	
Prerequisite	1	LT with the capability to stimulate, reset and configure the IUT.
	2	The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1	LT: Shall configure the IUT with default bit rate (see B.2.4.5.5).
	2	LT: Shall configure the IUT with default working carrier frequencies (see Table B.4).
	3	LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1	LT: Shall send TST_BYTE_55 on IUT TXD.
	2	UT: Shall measure the length of byte field data bit phases at TP 1.
Iteration	Not applicable	
Expected response	Step 2	The length of byte field data bit phases measured at TP 1 complies with Table 5 = OK.
Remark	—	

B.3.8 Value of byte field data bit phase shifts

Table B.12 defines the test structure of CTC_TX_CHARC_7.

Table B.12 — Test structure of CTC_TX_CHARC_7

Item	Content	
CTC # – Title	**1.CTC_TX_CHARC_7 – Value of byte field data bit phase shifts**	
Purpose	This CTC verifies the correct value of byte field data bit phase shifts.	
Reference	Table 5	
Prerequisite	1	LT with the capability to stimulate, reset and configure the IUT.
	2	The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1	LT: Shall configure the IUT with default bit rate (see B.2.4.5.5).
	2	LT: Shall configure the IUT with default working carrier frequencies (see Table B.4).
	3	LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1	LT: Shall send TST_BYTE_55 on IUT TXD.
	2	UT: Shall measure the value of byte field data bit phase shifts at TP 1.
	3	LT: Shall send TST_BYTE_7A on IUT TXD.
	4	UT: Shall measure the value of byte field data bit phase shifts at TP 1.
	5	LT: Shall send TST_BYTE_65 on IUT TXD.
	6	UT: Shall measure the value of byte field data bit phase shifts at TP 1.
	7	LT: Shall send TST_BYTE_5F on IUT TXD.
	8	UT: Shall measure the value of byte field data bit phase shifts at TP 1.
Iteration	Not applicable	
Expected response	Step 2	The value of byte field data bit phase shifts measured at TP 1 complies with Table 5 = OK.
	Step 4	The value of byte field data bit phase shifts measured at TP 1 complies with Table 5 = OK.
	Step 6	The value of byte field data bit phase shifts measured at TP 1 complies with Table 5 = OK.
	Step 8	The value of byte field data bit phase shifts measured at TP 1 complies with Table 5 = OK.

Table B.12 *(continued)*

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_7 – Value of byte field data bit phase shifts**
Remark	—

B.3.9 Length of break field phases

Table B.13 defines the test structure of CTC_TX_CHARC_8.

Table B.13 — Test structure of CTC_TX_CHARC_8

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_8 – Length of break field phases**
Purpose	This CTC verifies the correct length of break field phases.
Reference	4.2.3
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT as master node. 2 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 3 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 4 LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1 LT: Shall send TST_BREAK_FIELD on IUT TXD. 2 UT: Shall measure the length of break field phases at TP 1.
Iteration	Not applicable
Expected response	Step 2 The length of break field phases measured at TP 1 complies with as specified in 4.2.3 = OK.
Remark	—

B.3.10 Value of break field phase shifts

Table B.14 defines the test structure of CTC_TX_CHARC_9.

Table B.14 — Test structure of CTC_TX_CHARC_9

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_9 – Value of break field phase shifts.**
Purpose	This CTC verifies the correct value of break field phase shifts.
Reference	4.2.3
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT as master node. 2 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 3 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 4 LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1 LT: Shall send TST_BREAK_FIELD on IUT TXD. 2 UT: Shall measure the value of break field phase shifts at TP 1.
Iteration	Not applicable

Table B.14 *(continued)*

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_9 – Value of break field phase shifts.**
Expected response	Step 2 The value of break field phase shifts measured at TP 1 complies with as specified in 4.2.3 = OK.
Remark	—

B.3.11 Length of wake-up signal phases

Table B.15 defines the test structure of CTC_TX_CHARC_10.

Table B.15 — Test structure of CTC_TX_CHARC_10

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_10 – Length of wake-up signal phases**
Purpose	This CTC verifies the correct length of wake-up signal phases.
Reference	4.2.4
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).
Set-up	1 LT: Shall configure the IUT with default bit rate (see B.2.4.5.5). 2 LT: Shall configure the IUT with default working carrier frequencies (see Table B.4). 3 LT: Shall configure the IUT with default transmit signal number of carrier frequencies.
Step	1 LT: Shall send TST_WAKEUP_SIGNAL_SHORT on IUT TXD. 2 UT: Shall measure the length of wake-up signal phases at TP 1. 3 LT: Shall send TST_WAKEUP_SIGNAL_LONG on IUT TXD. 4 UT: Shall measure the length of wake-up signal phases at TP 1. 5 LT: Shall send TST_BREAK_FIELD on IUT TXD. 6 UT: Shall measure the length of wake-up signal phases at TP 1.
Iteration	Not applicable
Expected response	Step 2 The length of wake-up signal phases measured at TP 1 complies with as specified in 4.2.4 = OK. Step 4 The length of wake-up signal phases measured at TP 1 complies with as specified in 4.2.4 = OK. Step 6 The length of wake-up signal phases measured at TP 1 complies with as specified in 4.2.4 = OK.
Remark	—

B.3.12 Value of wake-up signal phase shifts

Table B.16 defines the test structure of CTC_TX_CHARC_11.

Table B.16 — Test structure of CTC_TX_CHARC_11

Item	Content
CTC # – Title	**1.CTC_TX_CHARC_11 – Value of wake-up signal phase shifts**
Purpose	This CTC verifies the correct value of wake-up signal phase shifts.
Reference	4.2.4
Prerequisite	1 LT with the capability to stimulate, reset and configure the IUT. 2 The UT is able to provide time measurement capabilities synchronised with the test step events (see Figure B.2).