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Road vehicles — Controller area network (CAN) —

Part 2: High-speed physical medium attachment (PMA) sublayer

Véhicules routiers — Gestionnaire de réseau de communication (CAN) —

Partie 2: Sous-couche de l'unité d'accès au support à haute vitesse (PMA)

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Foreword

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

This third edition cancels and replaces the second edition (ISO 11898-2:2016), which has been technically revised.

The main changes are as follows:

— Clause 5 is restructured, the parameters are categorized by static parameter and dynamic parameter;

— Table 13 with bit rates above 1 Mbit/s and up to 2 Mbit/s is in this edition Table 15 (parameter set A). Table 14 with bit rates above 2 Mbit/s and up to 5 Mbit/s is now Table 16 (parameter set B). The parameter set C (see Table 17 and Table 18) in this edition is newly introduced;

— Annex A in this edition is newly introduced; it specifies HS-PMAs with the SIC mode and the FAST mode. Annex B and Annex C in this edition are Annex A and Annex B in the previous edition. The content is unchanged.

A list of all parts in the ISO 11898 series can be found on the ISO website.

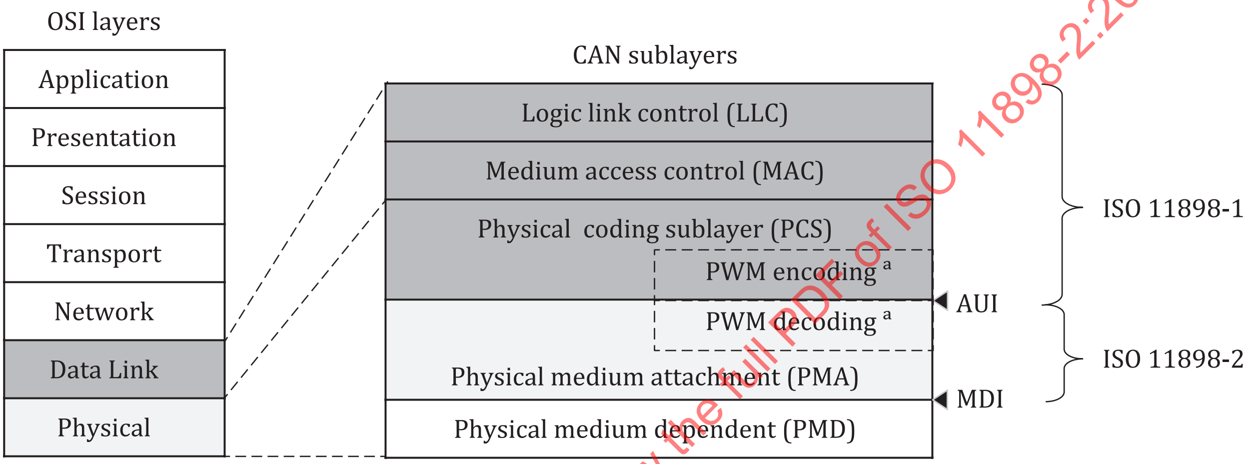
Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The ISO 11898 series provides requirement specifications for the CAN data link layer and physical layer. It is intended for chip implementers, e.g. ISO 11898-1 for CAN protocol controllers and this document for CAN transceivers. Related conformance test plans are given in the ISO 16845 series. The CAN data link layer models the open system interconnect (OSI) data link layer; it is internally subdivided into logic link control (LLC) and medium access control (MAC). ISO 11898-1 also specifies the CAN physical coding sublayer (PCS) by means of the attachment unit interface (AUI). Optionally, the PCS also provides the PWM encoding to be linked to a CAN SIC XL transceiver, which provides the PWM decoding.

The open system interconnect (OSI) layers above the data link layer (e.g. the network layer) are not specified in the ISO 11898 series.

Figure 1 shows the relation between the OSI layers and the CAN sublayers.



Key

AUI attachment unit interface

MDI medium dependent interface

[a] Only supported by CAN XL.

Figure 1 — CAN data link and physical sublayers relation to the OSI model

Road vehicles — Controller area network (CAN) —

Part 2: High-speed physical medium attachment (PMA) sublayer

1 Scope

This document specifies physical medium attachment (PMA) sublayers for the controller area network (CAN). This includes the high-speed (HS) PMA without and with low-power mode capability, without and with selective wake-up functionality. Additionally, this document specifies PMAs supporting the signal improvement capability (SIC) mode and the FAST mode in Annex A. The physical medium dependent (PMD) sublayer is not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7498-1, *Information technology — Open Systems Interconnection — Basic Reference Model: The Basic Model*

ISO 11898-1[1)], *Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC 7498-1, ISO 11898-1 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

3.1
active recessive
intermediate high-speed physical medium attachment (HS-PMA) output drive with a dedicated lower than nominal impedance at transitions from dominant state or level_0 state towards the *passive recessive* (3.14) state with a dedicated duration

3.2
attachment unit interface
AUI
interface between the *physical coding sublayer (PCS)* (3.15) and the *physical medium attachment (PMA)* (3.16) sublayer

3.3
bus
shared medium of any topology

1) Third edition under preparation. Stage at the time of publication: ISO/DIS 11898-1:2024.

3.4
bus state
state of the *medium dependent interface (MDI)* (3.11), which is dominant or recessive if the *physical medium attachment (PMA)* (3.16) sublayer is in arbitration mode, or is level_0 or level_1 otherwise

Note 1 to entry: The dominant state represents the logical 0 and the recessive state represents the logical 1. During simultaneous transmission of dominant and recessive bits, the resulting bus state is dominant. When no transmission is in progress, the *bus* (3.3) is idle. During idle time, it is in recessive state.

Note 2 to entry: The level_0 state represents the logical 0, and the level_1 state represents the logical 1.

3.5
CAN_H, CAN_L
pair of ports, where $V_{CAN\_H} - V_{CAN\_L}$ is positive at dominant *bus state* (3.4) and level_0 bus state

3.6
edge
difference in *bus states* (3.4) between two consecutive time quanta

3.7
FAST RX mode
mode in which the *physical medium attachment (PMA)* (3.16) sublayer drives the *bus state* (3.4) recessive and the receive thresholds are adjusted to distinguish between the bus states level_0 and level_1

3.8
FAST TX mode
mode in which the *physical medium attachment (PMA)* (3.16) sublayer drives the *bus states* (3.4) level_0 and level_1, which are not able to overwrite each other

3.9
legacy implementation
HS-PMA implementation compliant with previous ISO 11898-2 editions

3.10
low-power mode
mode in which the transceiver is not capable of transmitting or receiving frames, except for the purposes of determining if a WUP or WUF is being received

3.11
MDI
medium dependent interface
electrical interface consisting of CAN_H and CAN_L, that defines the signal transfer between the *physical medium dependent (PMD)* sublayer and the *physical medium attachment (PMA)* (3.16) sublayer

3.12
nominal bit time
duration of one bit in the arbitration phase

3.13
normal-power mode
mode in which the transceiver is capable of transmitting and receiving

3.14
passive recessive
final high-speed physical medium attachment (HS-PMA) output drive with nominal impedance, also known as recessive

3.15
physical coding sublayer
PCS
sublayer of the open system interconnect (OSI) physical layer that performs bit encoding/decoding and synchronization

3.16
physical medium attachment
PMA
sublayer of the open system interconnect (OSI) physical layer that converts physical signals into logical signals and vice versa

3.17
PWM decoding
PWMD
physical medium attachment (PMA) (3.16) sublayer function decoding the pulse-width modulation (PWM) bit streams into the non-return-to-zero (NRZ) bit streams

3.18
PWM encoding
PWME
physical coding sublayer (PCS) (3.15) function encoding the non-return-to-zero (NRZ) bit streams into the pulse-width modulation (PWM) bit streams

3.19
receiver
node that, while the *bus* (3.3) is not idle, is neither a *transmitter* (3.23) nor is it integrating

3.20
RXD
port of the *attachment unit interface (AUI)* (3.2) used to transmit the actual state of the physical medium, in binary format, to the *physical coding sublayer (PCS)* (3.15)

3.21
signal improvement capability
SIC
capability to suppress the ringing on the MDI

Note 1 to entry: It is as specified in the high-speed physical medium attachment (HS-PMA) implementation parameter set C in Table 14 and Table 17.

3.22
SIC mode
mode according to the high-speed physical medium attachment (HS-PMA) during the arbitration phase

Note 1 to entry: For PMA implementations, it is according to parameter set C or Annex A.

3.23
transmitter
node sending CAN frames

3.24
TXD
port of the *attachment unit interface (AUI)* (3.2) driven by the *physical coding sublayer (PCS)* (3.15) to control how the *physical medium attachment (PMA)* (3.16) influences the actual state of the physical medium

4 Abbreviated terms

For the purposes of this document, the symbols and abbreviated terms given in ISO 11898-1 and the following apply. If the definition of the term in this document is different from the definition in ISO 11898-1, this definition applies.

CAN controller area network

DLC data length code

ECU electronic control unit

EMC electromagnetic compatibility

ESD electro static discharge

GND ground

HS-PMA high-speed PMA

NRZ non-return-to-zero

OSI open layer system

PMD physical medium dependent

PN partial networking

PWM pulse width modulation

RF radio frequency

WUF wake-up frame

WUP wake-up pattern

5 HS-PMA function

5.1 Base requirements

The HS-PMA comprises one transmitter and one receiving entity. It shall be able to bias the connected physical medium, an electric two-wire cable, relative to a common ground. The transmitter entity shall drive a differential voltage between the CAN_H and CAN_L signals to signal a logical 0 (dominant) or shall not drive a differential voltage to signal a logical 1 (recessive) to be received by other nodes connected to the very same medium. These two signals are the interface to the PMD sublayer.

The HS-PMA shall provide an AUI to the physical coding sublayer as specified in ISO 11898-1. It comprises the TXD and RXD signals as well as the GND signal. The TXD signal receives from the physical coding sublayer the bit stream to be transmitted on the MDI. The RXD signal transmits to the physical coding sublayer the bit stream received from the MDI.

Implementations that comprise one or more HS-PMAs shall at least support the normal-power mode of operation. A low-power mode may be implemented.

Some of the items specified in the following depend on the operation mode of the (part of the) implementation, in which the HS-PMA is included.

Table 1 shows the possible combinations of HS-PMA operating modes and expected behaviour.

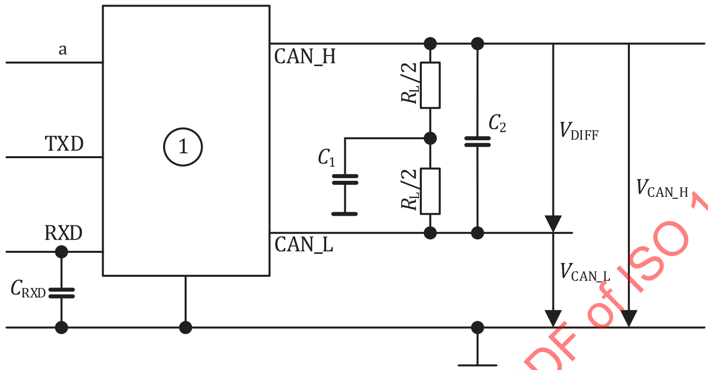
Table 1 — HS-PMA operating modes and expected behaviour

Operating mode	Bus-biasing behaviour	Transmitter behaviour
Normal-power mode	Bus biasing active	Dominant or recessive[a]
Low-power mode	Bus biasing active or inactive	Recessive
[a] Depends on input conditions as described in this document.		

Parameters given in Clause 5 shall be fulfilled throughout the operating temperature range and supply voltage range (if not explicitly specified for unpowered) as specified individually for every HS-PMA implementation.

5.2 HS-PMA test circuit

The outputs of the HS-PMA implementation to the CAN signals are called CAN_H and CAN_L, TXD is the transmit data input and RXD is the receive data output. Figure 2 shows the external circuit used to measure the specified voltage and current parameters. R_L represents the effective resistive load (bus load) for an HS-PMA implementation, when used in a network, and C_1 represents an optional split-termination capacitor. The values of R_L and C_1 vary for different parameters that the HS-PMA implementation needs to meet and are given as condition in the tables of related parameters.



Key

1	PMA implementation
V_{Diff}	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire
C_{RXD}	capacitive load on RXD
C_1	optional split-termination capacitor
C_2	differential capacitive load
R_L	differential load resistance
a	Power supply for the PMA implementation.

Figure 2 — HS-PMA test circuit

5.3 Static parameter

5.3.1 Maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Table 2 specifies upper and lower limit static voltages, which can be applied to CAN_H and CAN_L without causing damage, while V_{Diff} stays within in its own maximum rating range.

Table 2 — HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Parameter description	Notation	Value	
		Min. [V]	Max. [V]
Maximum rating	V_{Diff}[a]	−5,0	+10,0
General maximum rating	V_{CAN_H}, V_{CAN_L}	−27,0	+40,0
Optional: Extended maximum rating	V_{CAN_H}, V_{CAN_L}	−58,0	+58,0

[a] This is required regardless whether general or extended maximum rating for V_{CAN_H} and V_{CAN_L} is fulfilled.

Applies to HS-PMA implementation powered and unpowered conditions. Applies to transmit data input de-asserted and transmit data input (TXD) becomes asserted while CAN_H or/and CAN_L connected to a fixed voltage.

The maximum rating for V_{Diff} excludes that all combinations of V_{CAN_H} and V_{CAN_L} are compliant to this document. $V_{Diff} = V_{CAN\_H} - V_{CAN\_L}$, see Figure 2.

5.3.2 Recessive output characteristics, bus biasing active

Table 3 specifies the recessive output characteristics when bus biasing is active.

Table 3 — HS-PMA recessive output characteristics, bus biasing active

Parameter	Notation	Value		
		Min. [V]	Nom. [V]	Max. [V]
Single-ended output voltage on CAN_H [a]	V_{CAN_H}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_H [b]	$V_{CAN\_H\_rec}$	+2,137	+2,5	+2,887
Single-ended output voltage on CAN_L [a]	V_{CAN_L}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_L [b]	$V_{CAN\_L\_rec}$	+2,137	+2,5	+2,887
Differential output voltage	V_{Diff}	−0,5	0	+0,05

NOTE The requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential output voltage.

[a] Measurement setup according to Figure 2 (including implementations with selective wake-up function):

$R_L > 10^{10}$ Ω (not present)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

[b] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

5.3.3 Recessive output characteristics, bus biasing inactive

Table 4 specifies the recessive output characteristics when bus biasing is inactive.

Table 4 — HS-PMA recessive output characteristics, bus biasing inactive

Parameter	Notation	Value [a]		
		Min. [V]	Nom. [V]	Max. [V]
Single-ended output voltage on CAN_H	V_{CAN_H}	−0,1	0	+0,1
Single-ended output voltage on CAN_L	V_{CAN_L}	−0,1	0	+0,1
Differential output voltage	V_{Diff}	−0,2	0	+0,2

NOTE See 5.5.6 to determine when bias is inactive.

[a] Measurement setup according to Figure 2:

$R_L > 10^{10}$ Ω (not present)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

5.3.4 Dominant output characteristics

Table 5 specifies the output characteristics during dominant state. Figure 3 illustrates the voltage range for the dominant state.

Table 5 — HS-PMA dominant output characteristics

Parameter	Notation	Value [a]			Condition [b]
		Min. [V]	Nom. [V]	Max. [V]	
Single-ended voltage on CAN_H	V_{CAN_H}	+2,75	+3,5	+4,5	R_L = 50 Ω to 65 Ω
Single-ended voltage on CAN_L	V_{CAN_L}	+0,5	+1,5	+2,25	R_L = 50 Ω to 65 Ω
Differential voltage on normal bus load	V_{Diff}	+1,5	+2,0	+3,0	R_L = 50 Ω to 65 Ω
Differential voltage on effective resistance during arbitration	V_{Diff}	+1,5	Not defined	+5,0	R_L = 2 240 Ω (See NOTE)
Optional: Differential voltage on extended bus load range	V_{Diff}	+1,4	+2,0	+3,3	R_L = 45 Ω to 70 Ω

NOTE Assuming a maximum R_L of 70 Ω, this scenario covers a 32-node network (2 240 Ω/70 Ω = 32), 2 240 Ω is emulating a situation with up to 32 nodes transmitting dominant value simultaneously. In such case, the effective load resistance for single nodes decreases (a node does drive only a part of the nominal bus load).

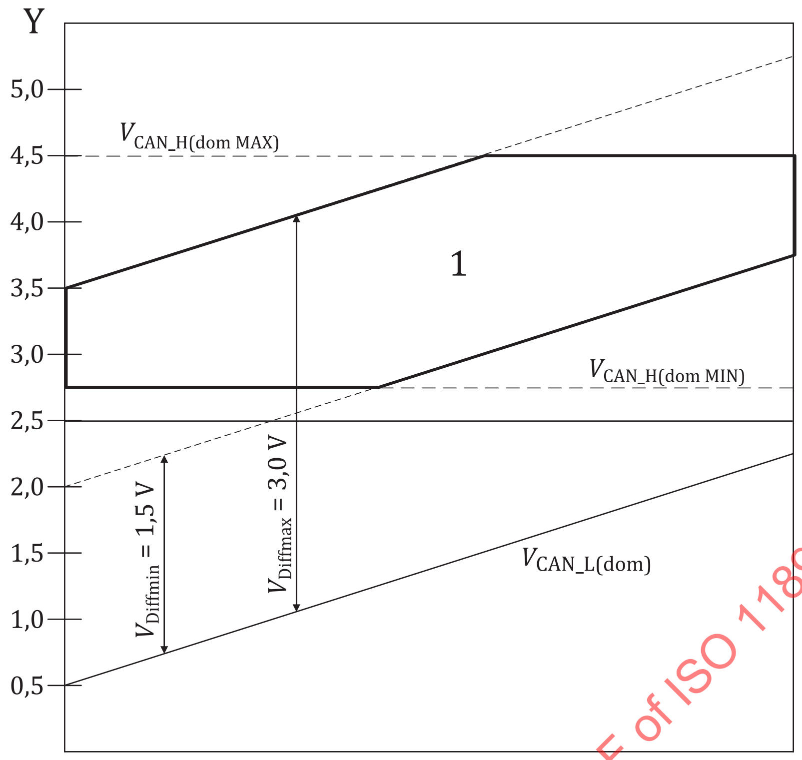
[a] Requirements given in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential voltage (see Figure 3).

[b] Measurement setup according to Figure 2:

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)



Key

Y	V_{CAN_H} and V_{CAN_L}
1	range of $V_{CAN\_H(dom)}$
V_{Diff}	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

Figure 3 — Voltage range of V_{CAN_H} during dominant state of CAN node, when V_{CAN_L} varies from minimum to maximum voltage level (50-Ω to 65-Ω bus-load condition)

5.3.5 Maximum driver output current

Table 6 specifies the maximum HS-PMA driver output current.

Table 6 — Maximum HS-PMA driver output current

Parameter	Notation	Value [a]		Condition
		Min. [mA]	Max. [mA]	
Absolute current on CAN_H	I_{CAN_H}	not specified	115	$-3\ V \le V_{CAN\_H} \le +18\ V$
Absolute current on CAN_L	I_{CAN_L}	not specified	115	$-3\ V \le V_{CAN\_L} \le +18\ V$

NOTE It is expected that the implementation does not stop driving its output dominant when the differential voltage between CAN_H and CAN_L is outside the limits given in the condition column. The minimum output current is implicitly specified in Table 5 and thus can be expected to be above 30 mA.

[a] Measurement setup according to Figure 2:

$R_L > 10^{10}$ Ω (not present)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

5.3.6 PMA static receiver input characteristics, bus biasing active and inactive

Table 7 specifies the voltage ranges for the HS-PMA static receiver in low-power mode, when the bus biasing is active.

Table 7 — HS-PMA static receiver input characteristics, bus biasing active

Parameter	Notation	Value [a]		Condition
		Min. [V]	Max. [V]	
Recessive state differential input voltage range	V_{Diff}	−3,0	+0,5	$-12{,}0\ V \leq V_{CAN\_L} \leq +12{,}0\ V$ $-12{,}0\ V \leq V_{CAN\_H} \leq +12{,}0\ V$
Dominant state differential input voltage range	V_{Diff}	+0,9	+8,0	$-12{,}0\ V \leq V_{CAN\_L} \leq +12{,}0\ V$ $12{,}0\ V \leq V_{CAN\_H} \leq +12{,}0\ V$

[a] Measurement setup according Figure 2:

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

NOTE A negative differential voltage can temporarily occur when the HS-PMA is connected to a medium in which common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage can temporarily occur when the HS-PMA is connected to a medium while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.

Table 8 specifies the the voltage ranges for the HS-PMA static receiver in low-power mode, when the bus biasing is inactive.

Table 8 — HS-PMA static receiver input characteristics, bus biasing inactive

Parameter	Notation	Value [a]		Condition
		Min. [V]	Max. [V]	
Recessive state differential input voltage range	V_{Diff}	−3,0	+0,4	$-12{,}0\ V \leq V_{CAN\_L} \leq +12{,}0\ V$ $-12{,}0\ V \leq V_{CAN\_H} \leq +12{,}0\ V$
Dominant state differential input voltage range	V_{Diff}	+1,15	+8,0	$-12{,}0\ V \leq V_{CAN\_L} \leq +12{,}0\ V$ $-12{,}0\ V \leq V_{CAN\_H} \leq +12{,}0\ V$

[a] Measurement setup according Figure 2:

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

NOTE A negative differential voltage can temporarily occur when the HS-PMA is connected to a medium in which common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage can temporarily occur when the HS-PMA is connected to a medium while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.

5.3.7 Receiver input resistance

Figure 4 shows an equivalent circuitry of the HS-PMA internal differential input resistance. Table 9 specifies the HS-PMA receiver input resistance parameter. Table 10 specifies the HS-PMA receiver input resistance matching parameters.

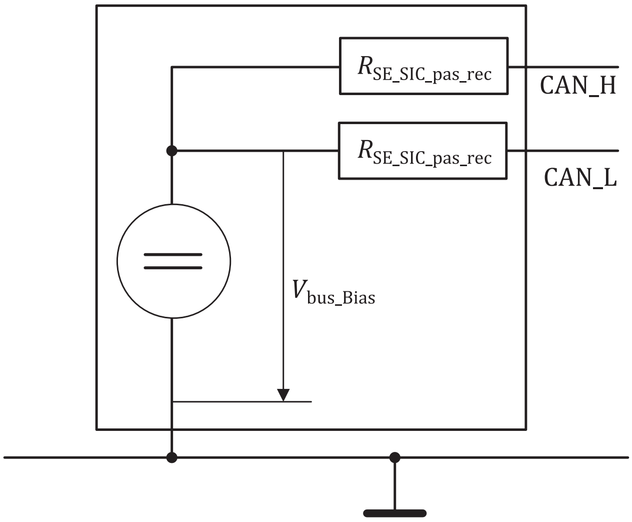


Figure 4 — Illustration of HS-PMA internal differential input resistance

Table 9 — HS-PMA receiver input resistance

Parameter	Notation	Value		Condition
		Min. [kΩ]	Max. [kΩ]	
Differential internal resistance	$R_{DIFF\_pas\_rec}$ [a]	12	100	$-2\text{ V} \leq V_{CAN\_L}$ $V_{CAN\_H} \leq +7\text{ V}$
Single-ended internal resistance	$R_{SE\_pas\_rec\_H}$ $R_{SE\_pas\_rec\_L}$	6	50	

[a] $R_{DIFF\_pas\_rec} = R_{SE\_pas\_rec\_H} + R_{SE\_pas\_rec\_L}$.

Table 10 — HS-PMA receiver input resistance matching

Parameter	Notation	Value		Condition
		Min.	Max.	
Matching[a] of internal resistance	m_R	−0,03	+0,03	V_{CAN_L}, V_{CAN_H}: +5 V

[a] The matching shall be calculated as $m_R = 2 \times (R_{SE\_H} - R_{SE\_L})/(R_{SE\_H} + R_{SE\_L})$.

5.3.8 Maximum leakage currents of CAN_H and CAN_L

An unpowered HS-PMA implementation shall not disturb the communication of other HS-PMAs that are connected to the same medium. Table 11 specifies the HS-PMA maximum leakage currents.

Table 11 — HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered

Parameter	Notation	Value	
		Min. [µA]	Max. [µA]
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	−10	+10

$V_{CAN\_H} = 5\text{ V}$, $V_{CAN\_L} = 5\text{ V}$, all supply inputs are connected to GND.
Positive currents are flowing into the implementation.

5.4 Dynamic parameter

5.4.1 Driver symmetry

In order to achieve a level of RF emission that is acceptably low, the transmitter shall meet the driver signal symmetry as specified in Table 12.

Table 12 — HS-PMA driver symmetry

Parameter	Notation	Value [c]		
		Min.	Nom.	Max.
Driver symmetry based on V_{CC} [a]	v_{sym_vcc}	+0,9	+1,0	+1,1
Driver symmetry based on V_{rec_sum} [b]	v_{sym_vrec}	+0,9	+1,0	+1,1

[a] $v_{sym\_vcc} = (V_{CAN\_H} + V_{CAN\_L})/V_{CC}$, with V_{CC} being the power supply of the transmitter

[b] $v_{sym\_vrec} = (V_{CAN\_H} + V_{CAN\_L})/V_{sum}$, without V_{CC} reference

$V_{rec\_sum} = V_{CAN\_H\_rec} + V_{CAN\_L\_rec}$

V_{sym_vcc} and V_{sym_vrec} shall be observed during dominant state and recessive state and also during the transition from dominant to recessive and vice versa, while TXD is stimulated by a square wave signal with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s) (HS-PMA in normal-power mode).

[c] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 4,7 nF (tolerance ≤ ± 5 %)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

5.4.2 Optional transmit dominant timeout

An implementation of an HS-PMA may limit the duration of dominant transmission in order not to prevent other CAN nodes from communication when the TXD input is permanently asserted. The HS-PMA implementation should implement a timeout. Table 13 recommends the optional HS-PMA transmit dominant timeout value range.

Table 13 — Optional HS-PMA transmit dominant timeout

Parameter	Notation	Value [a]	
		Min. [ms]	Max. [ms]
Transmit dominant timeout[a]	t_{dom}	0,8	10,0

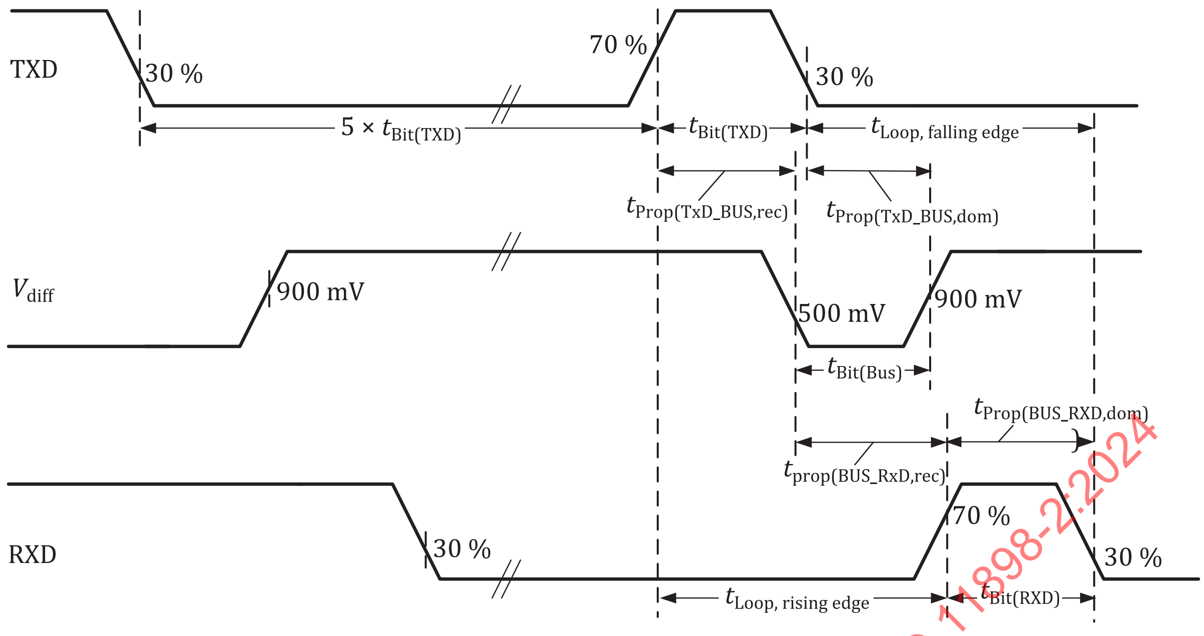
[a] A minimum value of 0,3 ms is accepted for legacy implementations.

NOTE There is a relation between the t_{dom} minimum value and the minimum bit rate. A t_{dom} minimum value of 0,8 ms accommodates 17 consecutive dominant bits at bit rates greater than or equal to 21,6 kbit/s and 36 consecutive dominant bits at bit rates greater than or equal to 45,8 kbit/s. The value 17 reflects PMA implementation attempts to send a dominant bit and every time sees a recessive level at the receive data input. The value 36 reflects six consecutive error frames when there is a bit error in the last bit of the first five attempts.

5.4.3 Transmitter and receiver timing behaviour

Figure 5 defines the HS-PMA implementation timing. Table 14 specifies the the HS-PMA implementation loop-delay requirements for parameter set A, parameter set B, and parameter set C. Table 15 specifies the HS-PMA implementation data signal timing requirements for parameter set A. Table 16 specifies the HS-PMA implementation data signal timing requirements for parameter set B. Table 17 and Table 18 specify HS-PMA implementation data signal timing requirements for parameter set C.

NOTE HS-PMA implementations with signal improvement capability developed prior to this document can refer to the CiA 601–4 specification.



Key

$t_{Bit(TXD)}$ nominal bit time of the bit rates the HS-PMA supports

Figure 5 — HS-PMA implementation timing definitions

Table 14 — HS-PMA implementation loop-delay requirement for parameter sets A, B and C

Parameter	Notation	Value [b]	
		Min. [ns]	**Max.** [ns]
Loop delay for parameter set A and parameter set B [a]	t_{Loop}	not specified	255
Loop delay for parameter set C [a]	t_{Loop}	not specified	190
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD\_BUS)}$	not specified	80
Propogation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS\_RXD)}$	not specified	110

[a] Time span from signal edge on TXD input to the next signal edge with the same polarity on RXD output, the maximum of delay of both signal edges is to be considered.

[b] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

Table 15 — HS-PMA implementation data signal timing requirements for parameter set A

Parameter	Notation	Value [d]	
		Min. [ns]	Max. [ns]
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$ [a]	−65	+30
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$ [b]	−100	+50
Receiver timing symmetry	$t_{\Delta REC}$ [c]	−65	+40

[a] $t_{\Delta Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TXD)}$

[b] $t_{\Delta Bit(RXD)} = t_{Bit(RXD)} - t_{Bit(TXD)}$

[c] $t_{\Delta Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

The requirements in this table apply concurrently. Therefore, not all combinations of $t_{\Delta Bit(Bus)}$ and $t_{\Delta Rec}$ are compliant with $t_{\Delta Bit(RXD)}$.

[d] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.

Table 16 — HS-PMA implementation data signal timing requirements for parameter set B

Parameter	Notation	Value [d]	
		Min. [ns]	Max. [ns]
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$ [a]	−45	+10
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$ [b]	−80	+20
Receiver timing symmetry variation	$t_{\Delta Rec}$ [c]	−45	+15

[a] $t_{\Delta Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TXD)}$

[b] $t_{\Delta Bit(RXD)} = t_{Bit(RXD)} - t_{Bit(TXD)}$

[c] $t_{\Delta Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

The requirements in this table apply concurrently. Therefore, not all combinations of $t_{\Delta Bit(Bus)}$ and $t_{\Delta Rec}$ are compliant with $t_{\Delta Bit(RXD)}$.

[d] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.

Table 17 — HS-PMA implementation data signal timing requirements for parameter set C

Parameter	Notation	Value [d]	
		Min. [ns]	Max. [ns]
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$ [a]	−10	+10
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$ [b]	−30	+20
Receiver timing symmetry variation	$t_{\Delta Rec}$ [c]	−20	+15

[a] $t_{\Delta Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TXD)}$

[b] $t_{\Delta Bit(RXD)} = t_{Bit(RXD)} - t_{Bit(TXD)}$

[c] $t_{\Delta Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

All requirements in this table apply concurrently. Therefore, not all combinations of $t_{\Delta Bit(Bus)}$ and $t_{\Delta Rec}$ are compliant with $t_{\Delta Bit(RXD)}$.

[d] Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ± 1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Table 18 specifies the HS-PMA implementation SIC timing and impedance for parameter set C.

Table 18 — HS-PMA implementation SIC timing and impedance for parameter set C

Parameter	Notation	Value		Condition
		Min.	Max.	
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF\_act\_rec}$	75 Ω	133 Ω	+2 V ≤ $V_{CAN\_H/L}$ ≤ V_{CC} −2 V, if R_{SE} fulfils $R_{SE\_act\_rec}$ otherwise −12 V ≤ $V_{CAN\_H/L}$ ≤ +12 V
Optional internal single-ended resistance	$R_{SE\_SIC\_act\_rec}$	37,5 Ω	66,5 Ω	+2 V ≤ $V_{CAN\_H/L}$ ≤ V_{CC} −2 V, if R_{SE} fulfils R_{SE_SIC} otherwise −12 V ≤ $V_{CAN\_H/L}$ ≤ V_{CC} +12 V
Start time of active signal improvement phase	$t_{act\_rec\_start}$	n.a.	120 ns	Measured from rising TXD edge with <5 ns slope at 50 % threshold
End time of active signal improvement phase	$t_{act\_rec\_end}$	355 ns	n.a.	
Start time of passive recessive phase	$t_{pas\_rec\_start}$	n.a.	530 ns	Measured from rising TXD edge with < 5 ns slope at 50 % threshold with R_{DIFF} ≥ min. R_{DIFF_REC} and R_{SE} ≥ min. R_{SE}.[a]

[a] Formerly specified in ISO 11898-2:2016, Table 10.

Figure 6 defines the SIC timing.

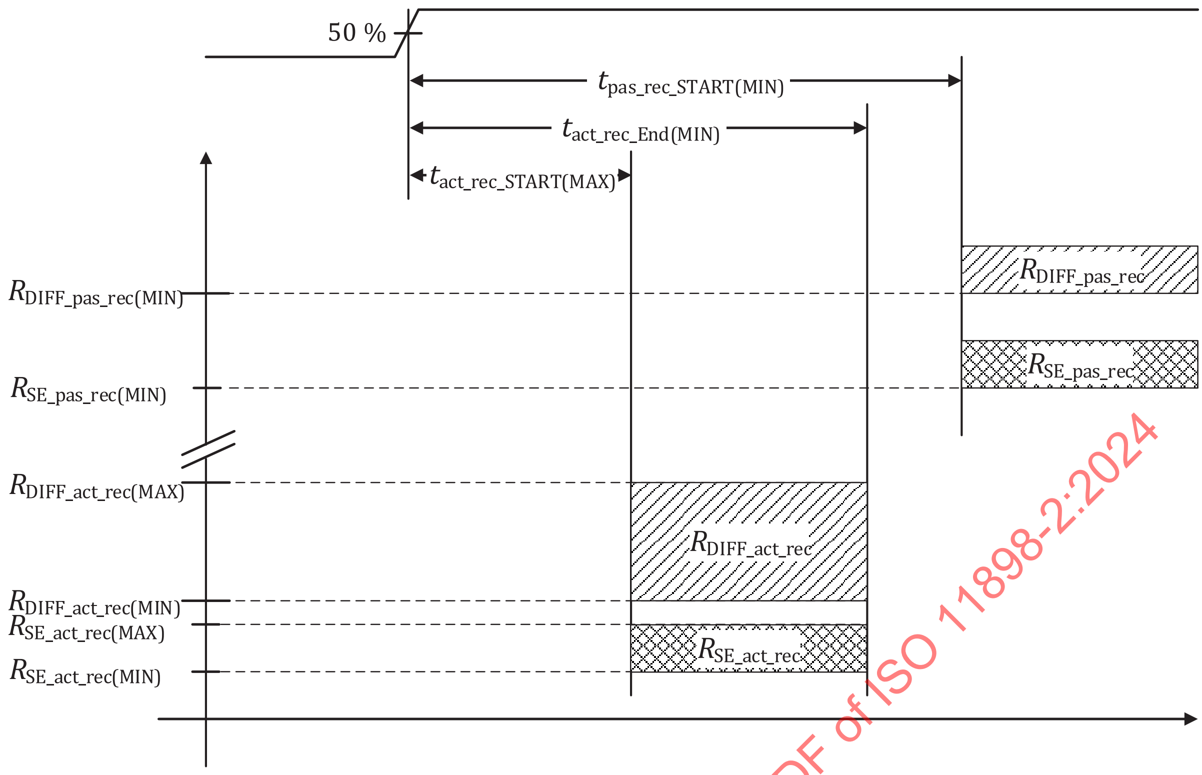


Figure 6 — SIC timing definitions

5.5 Wake-up from low-power mode

5.5.1 Wake-up procedures

When an implementation comprising one or more HS-PMAs implements a low-power mode, the HS-PMA can signal a wake-up event. Table 19 lists the wake-up procedures for defined types of HS-PMA implementations.

Table 19 — HS-PMA wake-up implementations

Type of HS-PMA implementation	Required wake-up mechanism
Without low-power mode	No wake-up
With low-power mode, but without selective wake-up	Either basic wake-up or wake-up pattern (WUP) wake-up
With selective wake-up	Selective wake-up frame (WUF) and wake-up pattern (WUP) wake-up

5.5.2 General requirement

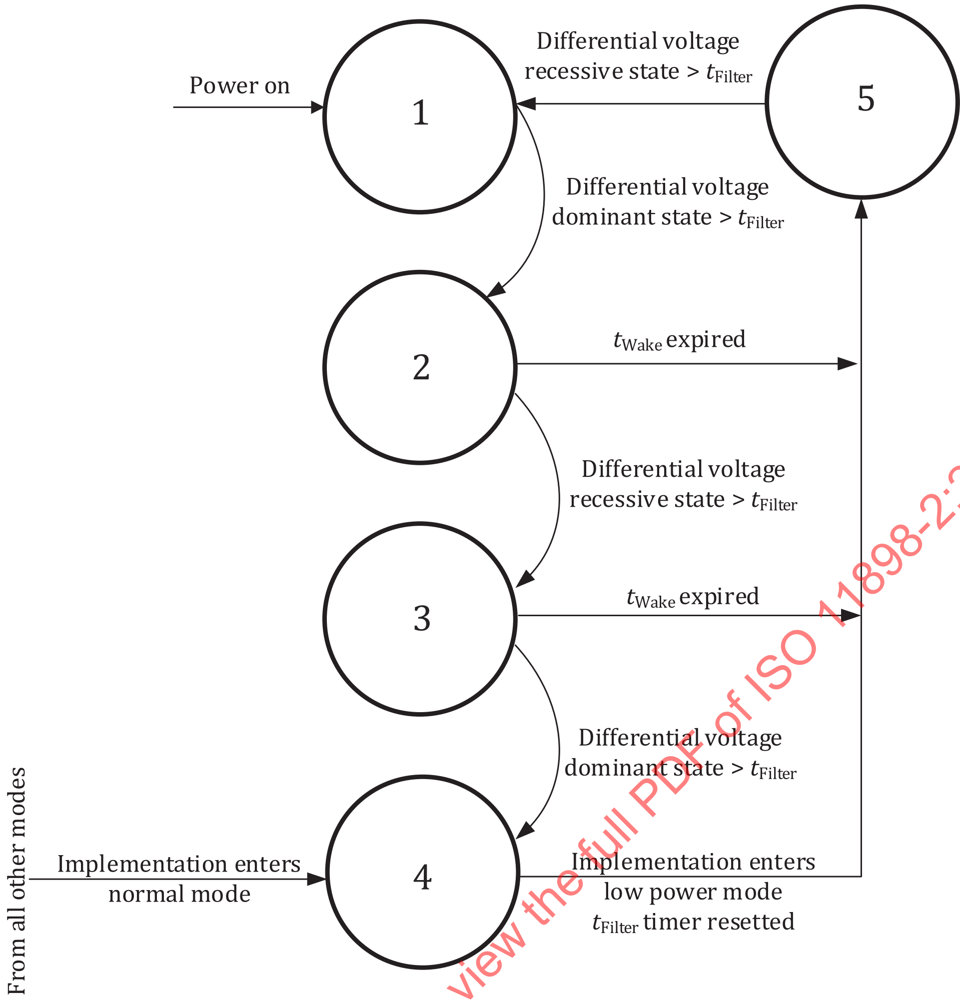
In case more than one wake-up procedure is implemented in an HS-PMA, the wake-up procedure to be used shall be configurable.

5.5.3 Basic wake-up

After having received a dominant state for the duration of at least t_{Filter}, the HS-PMA shall detect a wake-up.

5.5.4 Via wake-up pattern

Upon receiving two consecutive dominant states each for duration of at least t_{Filter}, separated by a recessive state with a duration of at least t_{Filter}, a wake-up event shall happen. This method is illustrated in Figure 7.



Key

1 INI state

2 state A

3 state B

4 state C: wake-up detected, entering this state shall signal the bus wake-up event

5 wait state

Figure 7 — Wake-up finite state machine

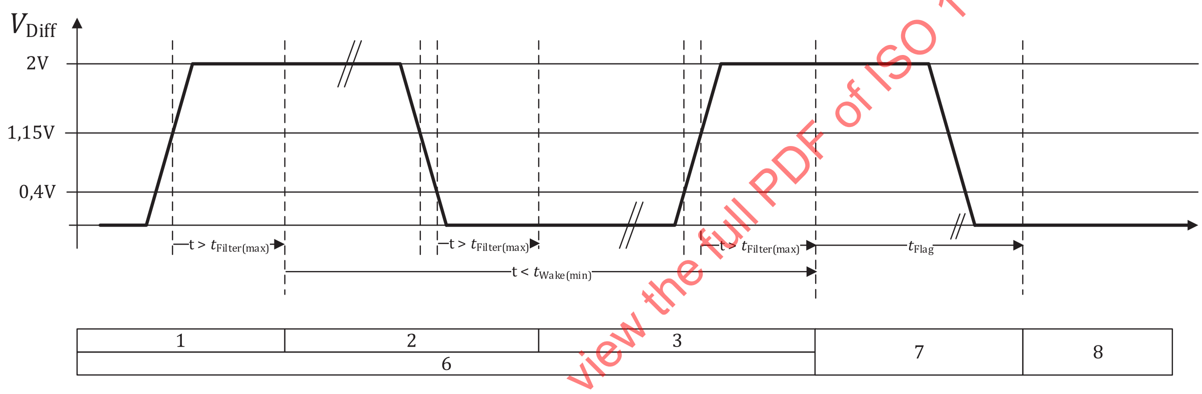
The finite state machine in Figure 7 specifies the wake-up behaviour for all operation modes. When entering state A the optional timer, t_{Wake}, shall be reset and when entering the Wait state the t_{Filter} timer shall be reset. Table 20 specifies the wake-up control timings and Figure 8 defines the wake-up reaction time.

Table 20 — PMA voltage wake-up control timings

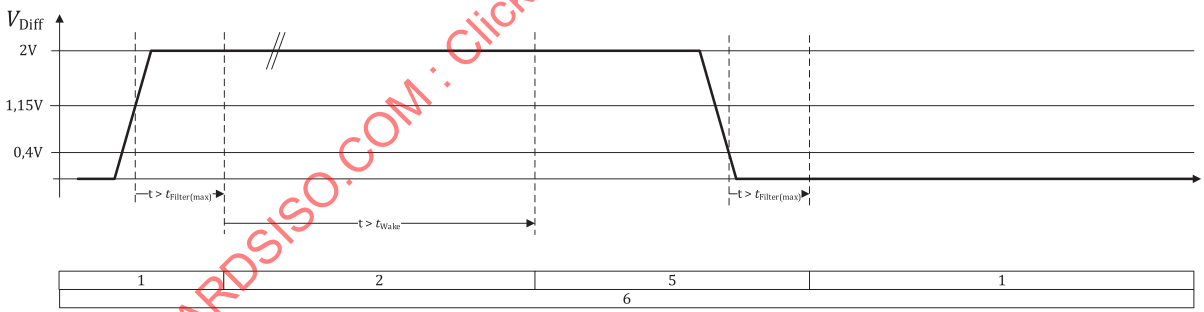
Parameter	Notation	Value		Condition
		Min. [µs]	Max. [µs]	
CAN activity filter time, long[a]	t_{Filter}	0,5	5,0	Bus voltages shall be as specified in Table 8.
CAN activity filter time, short[b]	t_{Filter}	0,15	1,8	Bus voltages shall be as specified in Table A.2.
Wake-up timeout	t_{Wake}	800,0	10 000,0	Optional timer
Wake-up pattern signalling	t_{Flag}	not defined	250,0	Measured from the completed wake-up pattern, see Figure 8

[a] Implementations do not need to meet this timing, in case the “CAN activity filter time, short” is met. It should be noted that the maximum filter time has an impact to the suitable wake-up pattern, especially at high bit rates. For example, in a 500-kbit/s network, a wake-up pattern shall carry at least three similar bit levels in a row in order to safely pass the wake-up filter. Shorter filter time implementations can increase the risk for unwanted bus wake-ups due to noise. The specified range is a compromise between robustness against unwanted wake-ups and freedom in frame selection.

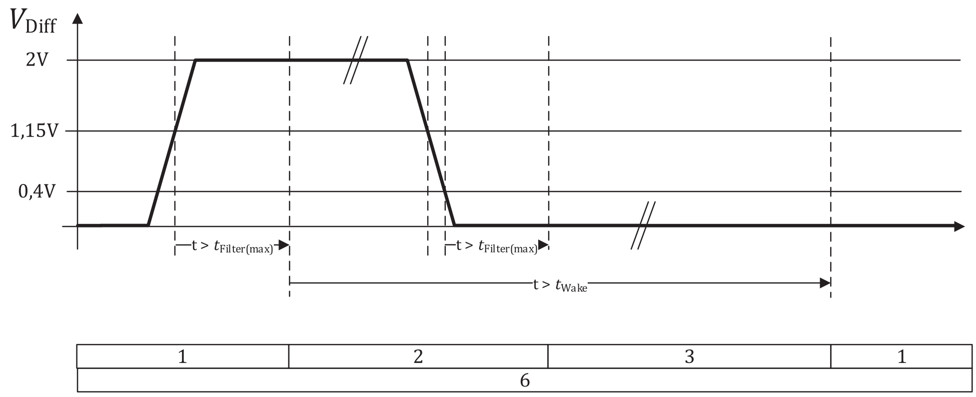
[b] Implementations do not need to meet this timing, in case the “CAN activity filter time, long” is met.



a) Correct wake-up pattern with PMA low-power mode



b) Incorrect wake-up pattern, dominant phase longer than t_{Wake}



c) Incorrect wake-up pattern, recessive phase longer than t_{Wake}

Key

1 INI state
2 in state A
3 in state B
4 in state C
5 in Wait state
6 in low-power mode
7 wake-up detected
8 wake-up flagged

Figure 8 — Wake-up reaction time, a) to c)

5.5.5 Selective wake-up

5.5.5.1 General

Upon detection of a wake-up frame (WUF), a wake-up event shall happen. Decoding of CAN frames in either classical base frame format (CBFF) or classical extended frame format (CEFF) and acceptance as a WUF is done by the HS-PMA. If enabled, decoding of CAN frames shall be possible in normal-power mode and low-power mode. The acceptance procedure is described in detail in the following subclauses.

After the bias reaction time, t_{Bias}, has elapsed, the implementation may ignore up to four (or up to eight when bit rate higher than 500 kbit/s) frames in CBFF and CEFF and shall not ignore any following frame in CBFF and CEFF.

In case of erroneous communication, the HS-PMA shall signal a wake-up upon or after an overflow of the internal error counter.

5.5.5.2 Behaviour during transitions between normal-power mode to low-power mode

If selective wake-up is enabled prior to the mode change and the HS-PMA is not anymore ignoring frames, decoding of CAN data frames and CAN remote frames shall also be supported during mode transitions, which have the frame detection functionality enabled. If the received frame is a valid WUF, the transceiver shall indicate a wake-up. If enabled, decoding of CAN data shall be possible in normal-power mode and low-power mode.

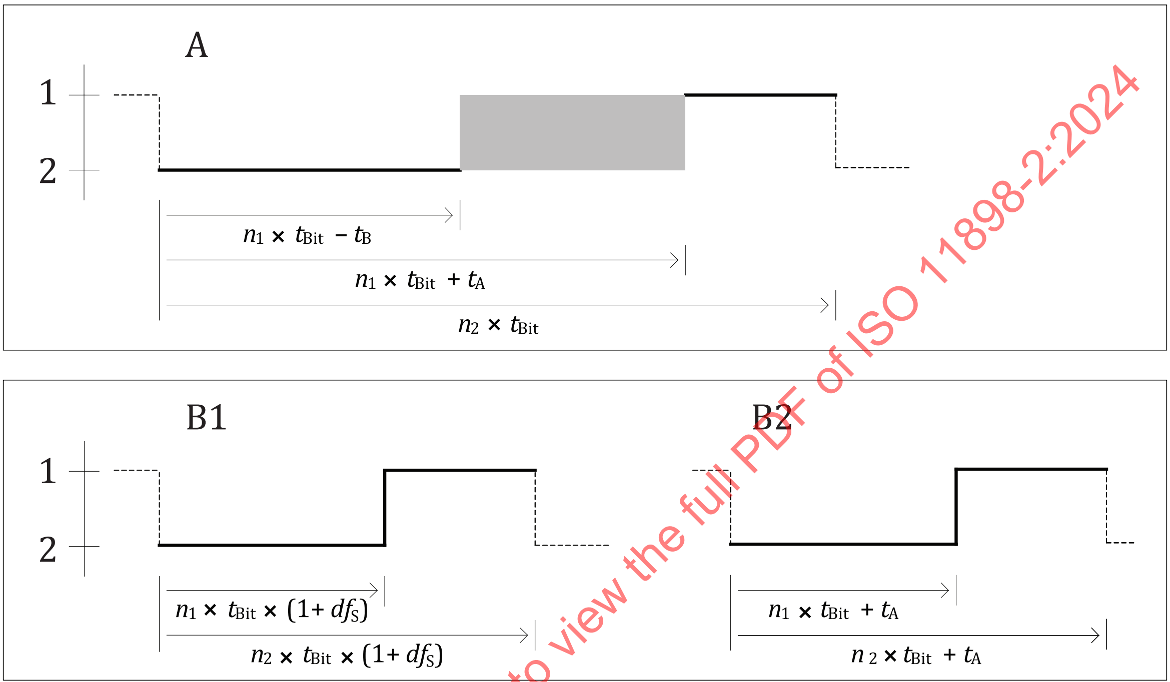
5.5.5.3 Bit decoding

A received classical CAN frame shall be decoded correctly when the timing of the differential voltage between CAN_H and CAN_L complies with one of the two following types of signals:

— the bit stream consists of multiple instances of the signal shape A (to handle ringing);

— the bit stream can be assembled out of multiple instances of the signal shape B1 and one instance of signal shape B2 (to handle sender clock tolerance and loss of arbitration).

These two types of signals are specified in Figure 9.



Key

1 recessive

2 dominant

n_1 number of consecutive dominant bits {1, 2, 3, 4, 5}

n_2 number of bits between two falling edges {2, 3, ..., 10}; $n_2 > n_1$

t_A $0 \leq t_A \leq 55$ % of t_{Bit} (implementation-specific higher maximum values for t_A are allowed)

t_B $0 \leq t_B \leq 5$ % of t_{Bit} (implementation-specific higher maximum values for t_B are allowed)

t_{Bit} nominal bit time

df_s transceivers according to this document shall tolerate sender clock frequency deviations up to at least 0,5 %

NOTE Often used values for t_{Bit} are 2 µs, 4 µs and 8 µs.

Figure 9 — Signal shape A and B of V_{Diff} for bit reception

Edges in the time span from "$n_1 \times t_{Bit} - t_B$" to "$n_1 \times t_{Bit} + t_A$" of signal shape A shall be ignored and shall not cause decoding errors.

5.5.5.4 Wake-up frame evaluation

If all of the following conditions are met, a valid classical CAN frame shall be accepted as a valid WUF.

a) The received frame is a classical CAN data frame when DLC matching [see c) in this subclause] is not disabled. The frame may also be a CAN remote frame when DLC matching is disabled.

b) The ID (as specified in ISO 11898-1:—[2], 6.6.11.2) of the received classical CAN frame is exactly matching a configured ID (in the HS-PMA implementation) in the relevant bit positions. The relevant bit positions are given by an ID-mask (in the HS-PMA implementation). This mechanism is illustrated in 5.5.5.7.

c) The DLC (as specified in ISO 11898-1:—, 6.6.11.3) of the received classical CAN data frame is exactly matching a configured DLC. This mechanism is illustrated in 5.5.5.8. This DLC matching condition may be disabled by configuration in the HS-PMA implementation.

d) When the DLC is greater than 0 and DLC matching is enabled, the data field (as specified in ISO 11898-1:—, 6.6.11.3) of the received frame has at least one bit set to 1 in a bit position, which corresponds to a bit set to 1 in the configured data mask. This mechanism is illustrated in 5.5.5.9.

e) A correct cyclic redundancy check (CRC) is received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:—, 6.6.11.5) is detected prior to the acknowledgement (ACK) slot. Figure 10 depicts the bits, which are considered as "don't care".

NOTE There is no requirement for the SRR bit to be received as dominant in CEFF to recognize the frame as a valid WUF.

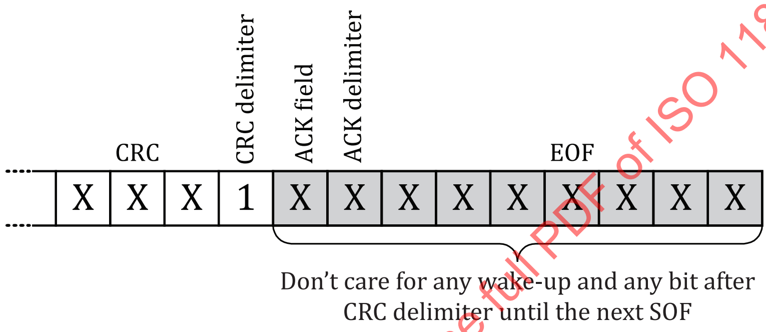


Figure 10 — Don't care bits for frame decoding

5.5.5.5 Frame error counter mechanism

Upon activating the selective wake-up function (e.g. by a connected host controller) and also on expiration of $t_{Silence}$, the counter for erroneous CAN frames shall be set to zero. The initial value of the counter is zero. This counter shall be incremented by one when a bit stuffing, CRC or CRC delimiter form error (according to ISO 11898-1) is detected. If a classical CAN frame is received, which is valid according to the definition in 5.5.5.4, and the counter is not zero, then the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field shall not increase the frame error counter.

On each increment or decrement of this counter, the decoder unit in the HS-PMA shall wait for n_{Bits_idle} recessive bits before considering a dominant bit as a start of frame. Figure 11 depicts the position of the mandatory start of frame (SOF) detection when a classical CAN frame was received and in case of an error scenario.

2) Third edition under preparation. Stage at the time of publication: ISO/DIS 11898-1:2024.

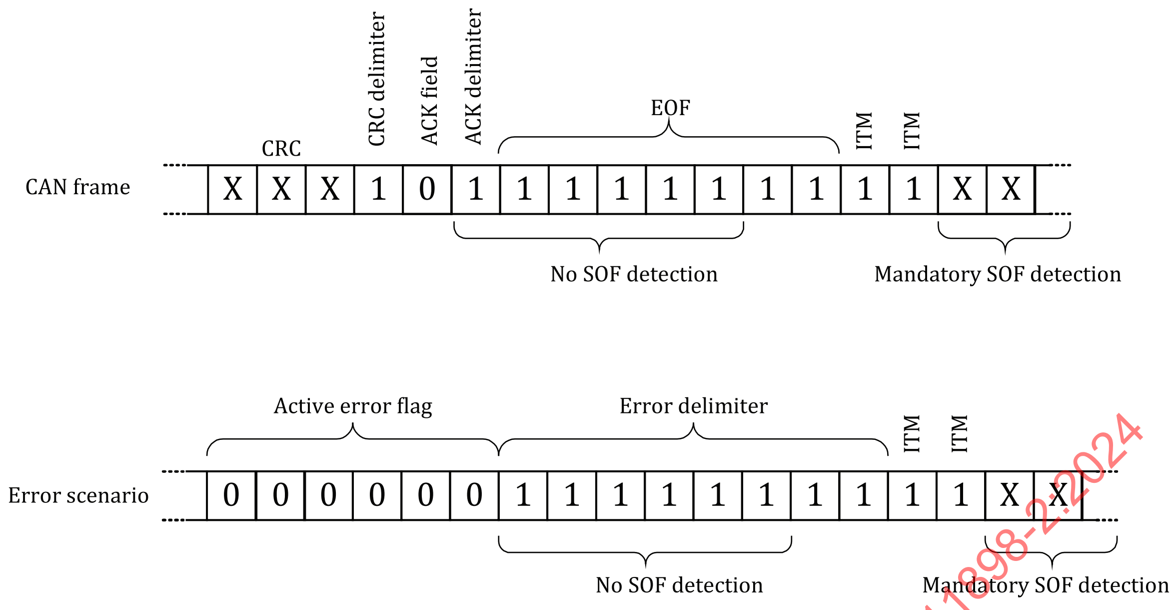


Figure 11 — Mandatory SOF detection after classical CAN frames and error scenarios

A wake-up shall be performed when the counter reaches the threshold value or upon the next received WUP. The default threshold value shall be 32, other values may be configured.

Up to four (or up to eight when bit rate > 500 kbit/s) consecutive classical CAN data frames and CAN remote frames that start after the bias reaction time, t_{Bias}, has elapsed can be either ignored (no error counter increase of failure) or judged as erroneous (error counter increase even in case of no error).

Receiving a frame in CEFF with non-nominal reserved bits (SRR, r0) shall not lead to an increase of the error counter.

5.5.5.6 Tolerance to CAN FD frames (optional)

After receiving a recessive FD format indicator (FDF) bit followed by a dominant res bit, the decoder unit in the HS-PMA shall wait for n_{Bits_Idle} recessive bits before considering a further dominant bit as a start of frame. Figure 11 depicts the position of the mandatory SOF detection when a CAN FD data frame is received and in case of an error scenario. Table 21 specifies the valid range for n_{Bits_Idle}.

Table 21 — Number of recessive bits before next SOF

Parameter	Notation	Value	
		Min.	Max.
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	6	10

The behaviour, when the FDF bit is received recessively and the following bit position is also received recessively, is outside the scope of this document.

One of the following bitfilter options shall be implemented to support different combinations of arbitration and data phase bit rates.

— Bitfilter option 1: a data phase bit rate less or equal to four times the arbitration bit rate or 2 Mbit/s, whichever is lower, shall be supported.

— Bitfilter option 2: a data bit rate less or equal to 10 times the arbitration bit rate or 5 Mbit/s, whichever is lower, shall be supported.

Dominant signals less than or equal to the minimum of $\rho_{Bitfilter}$ of the arbitration bit time in duration shall not be considered to be a valid bit and shall not restart the recessive bit counter. Dominant signals longer than or equal to maximum of $\rho_{Bitfilter}$ of the arbitration bit time in duration shall restart the recessive bit counter.

Table 22 specifies $\rho_{Bitfilter}$ depending on the chosen bitfilter option as percentage of the arbitration bit time.

Table 22 — Bitfilter in CAN FD data phase

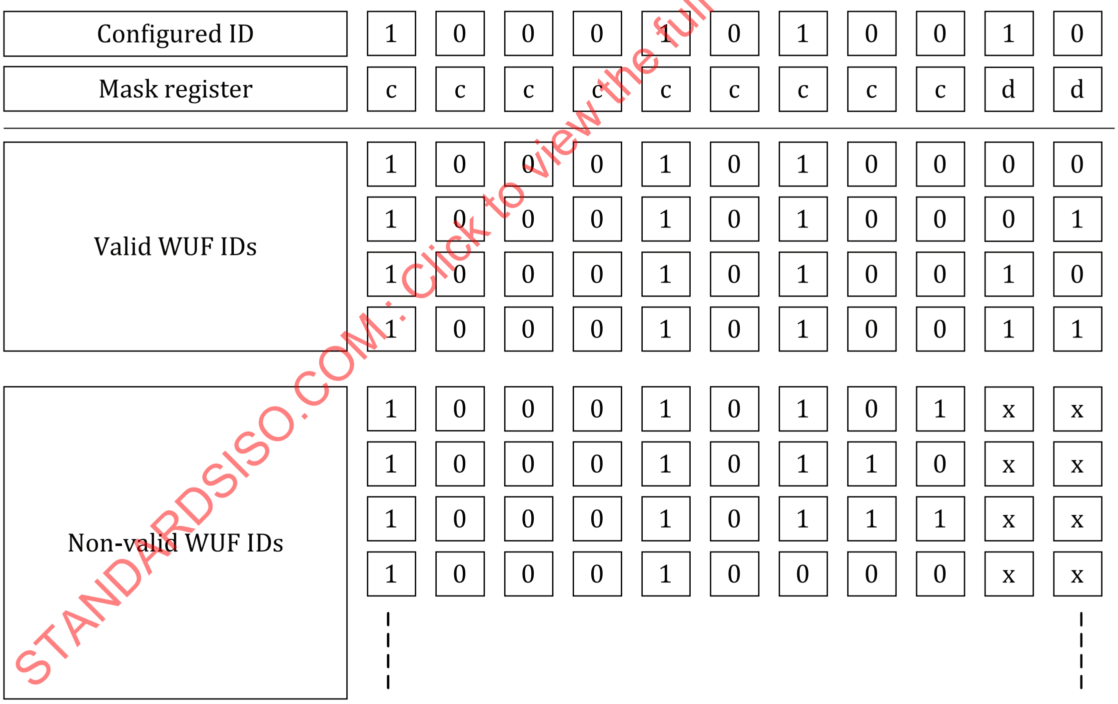
Parameter	Notation	Value	
		Min.	Max.
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter\_option1}$	5 %	17,5 %
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter\_option2}$	2,5 %	8,75 %

5.5.5.7 Wake-up frame ID evaluation

A CAN-ID mask mechanism shall be provided, in order to exclude ID-bits from the comparison. This mechanism shall support 11-bit and 29-bit identifiers. The IDE bit shall not be part of the ID mask, it shall be evaluated in both cases.

NOTE The user selects whether a WUF appears in CBFF or CEFF.

All masked ID-bits except "don't care" shall match exactly the configured ID-bits. If the masked ID-bits are configured as "don't care", then both "1" and "0" shall be accepted. The masking mechanism is implementation dependent. Figure 12 shows an example for valid WUF IDs corresponding to the ID-mask register.



Key

d don't care

c care

Figure 12 — Example for ID masking mechanism

5.5.5.8 Wake-up frame DLC evaluation

If the DLC matching condition is enabled, then a classical CAN frame can only be a valid WUF when the DLC of the received frame matches exactly the configured DLC.

If the DLC matching condition is disabled, then the DLC and data field are not evaluated, and a classical CAN frame is already a valid WUF when the identifier matches (see 5.5.5.7) and the CRC is correct.

5.5.5.9 Wake-up frame data field evaluation

If the DLC matching condition is enabled, then a classical CAN frame can only be a valid WUF if at least one logic 1 bit within the data field of the received WUF matches to a logic 1 bit of the data field within the configured WUF.

If the DLC matching condition is disabled, then the DLC and data field are not evaluated, and a classical CAN frame is already a valid WUF when the identifier matches (see 5.5.5.7) and the CRC is correct.

Figure 13 shows an example with a non-matching and a matching ID field.

		Byte 7	Byte 6	......	Byte 0
Configured data field		1 1 0 1 0 0 0 0	1 1 0 1 0 0 0 0	......	1 1 0 1 0 0 0 0
WUF data fields	matching	0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0	......	0 0 0 0 0 0 0 0
	none matching	0 0 0 0 0 1 1 1	0 0 0 0 0 1 1 1	......	0 0 0 0 0 1 1 1

Figure 13 — Example of the data field within a received classical CAN data frame

5.5.6 Bus biasing procedure

5.5.6.1 General requirements

The HS-PMA implementation with bus biasing functionality shall comply with the parameters given in Table 3 and Table 4.

When the HS-PMA implementation features a low-power mode and selective wake-up, automatic voltage biasing is required. For all other implementation, either normal biasing or automatic voltage biasing shall be implemented.

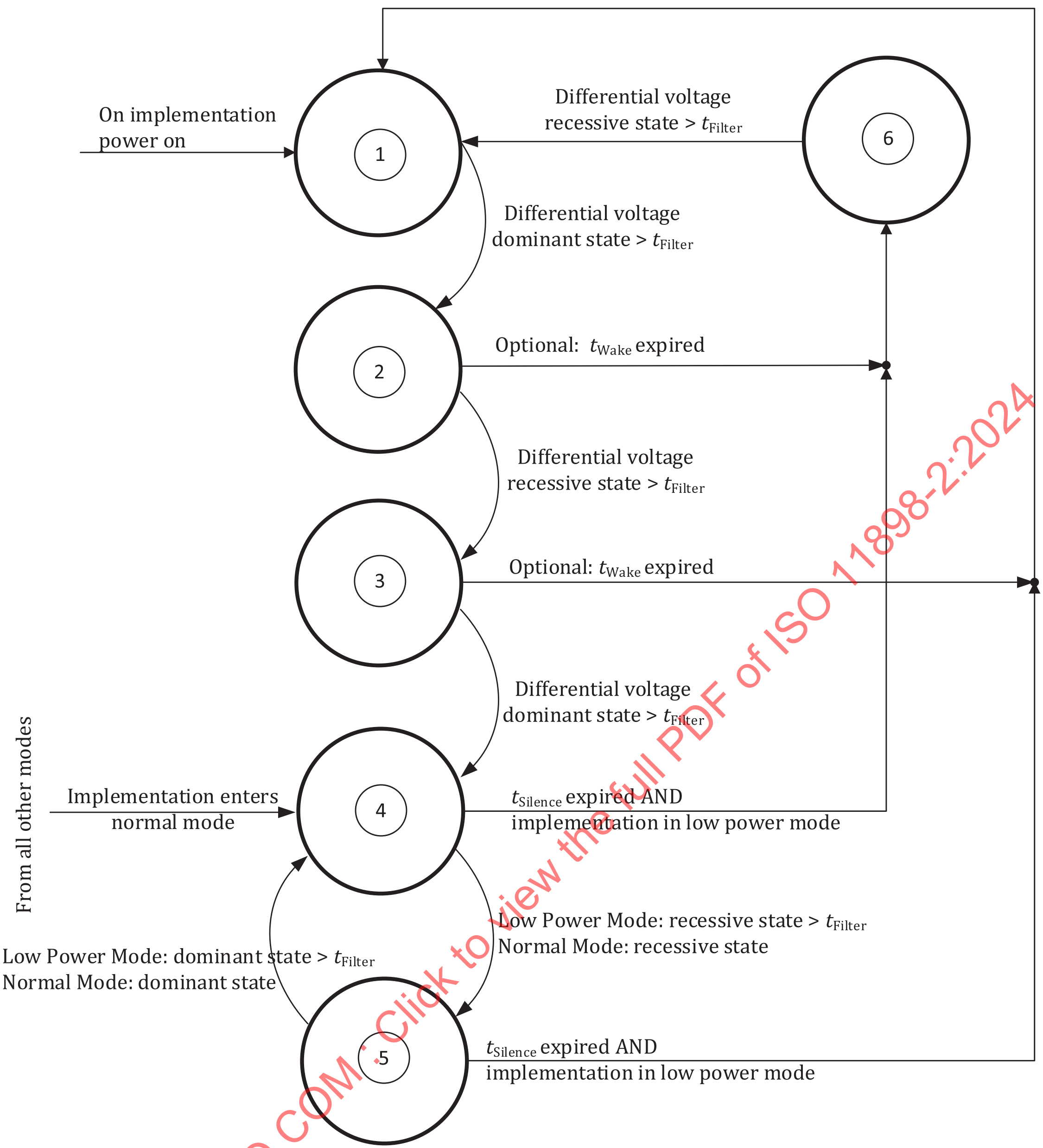
5.5.6.2 Normal biasing

Normal biasing means bus biasing is active in normal-power mode and inactive in low-power mode.

5.5.6.3 Automatic voltage biasing

Automatic voltage biasing means bus biasing is active in normal-power mode and is controlled by the differential voltage between CAN_H and CAN_L in low-power mode.

Figure 14 specifies the finite state machine for the bus biasing behaviour. When entering state A, the optional timer, t_{Wake}, shall be reset and restarted; when entering state C or D, the timer, $t_{Silence}$, shall be reset and restarted.



Key

1 Ini state; bus biasing is inactive

2 state A; bus biasing is inactive

3 state B; bus biasing is inactive

4 state C; bus biasing is active

5 state D; bus biasing is active

6 wait state; bus biasing is inactive

Figure 14 — Bus biasing control for automatic voltage biasing

Table 23 specifies the bus biasing control timings and Figure 15 the bias reaction time.

Table 23 — HS-PMA bus biasing control timings

Parameter	Notation	Value		Condition
		Min. [µs]	Max. [µs]	
Timeout for bus inactivity	$t_{Silence}$	0,6 × 10^{6}	1,2 × 10^{6}	Timer is reset and restarted when bus changes from dominant to recessive or vice versa.
Bus bias reaction time	t_{Bias}	Not defined	250,0	Measured from the start of a domin ant-recessive-dominant sequence (each phase 6 µs) until v_{sym} ≥ 0,1. See Figure 15 v_{sym} as defined in Table 12.

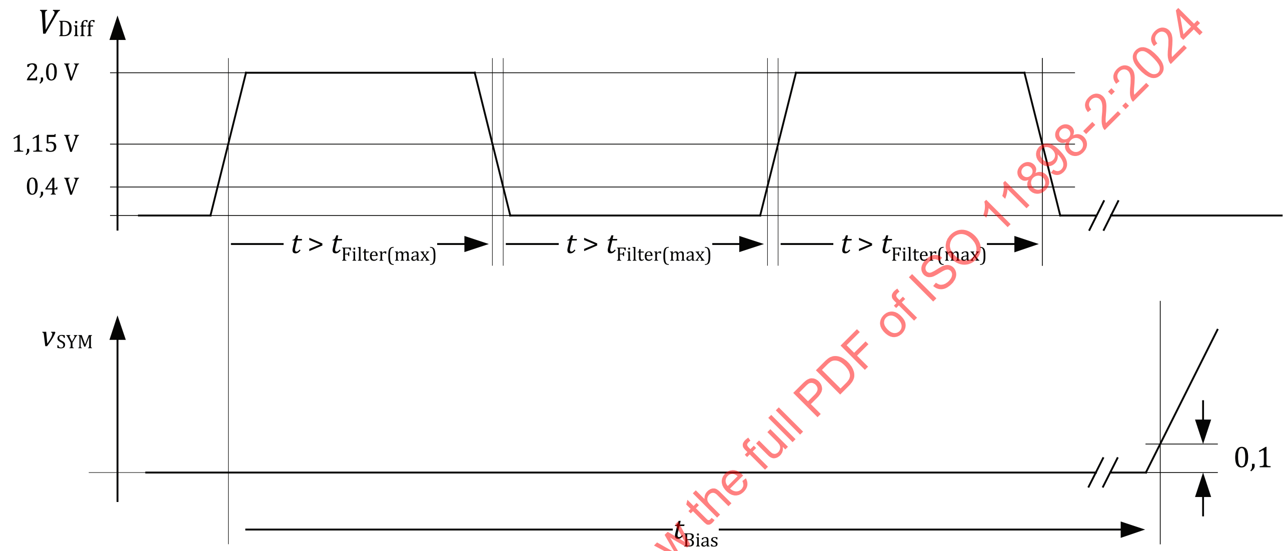


Figure 15 — Test signal definition for bias reaction time measurement

6 Conformance

A conformance test plan is not in the scope of this document.

Annex B provides an overview of optional features and implementation choices.

Annex A
(normative)

HS-PMA with SIC mode and FAST mode

A.1 Operating principle

During SIC mode the transmitter entity drives a differential voltage between the CAN_H and CAN_L signals to reflect a logical 0 (dominant) or drive another differential voltage to reflect a logical 1 (recessive). During the signal improvement time, the potential differential disturbances like reflections from the wiring harness are reduced. During FAST TX mode, the transmitter entity signals a logical 0 (level_0) or signals a logical 1 (level_1). During FAST RX mode, the transmitter entity signals a logical 1 (passive recessive). The signals on CAN_H and CAN_L are building the MDI towards the PMD sublayer.

The PMA provides the PWM decoding in accordance with the PWM encoding in the PCS as specified in ISO 11898-1.

Table A.1 shows the possible combinations of PMA operating modes and related states.

NOTE CiA 612–2 provides additional information about the PWM coding implementation.

Table A.1 — PMA operating modes and expected behaviour

Operating mode	Voltage biasing state	Transmitter state	Receiver state
SIC mode	Voltage biasing active	Dominant or recessive	Dominant or recessive
FAST TX mode	Voltage biasing active	level_1 or level_0	level_1 or level_0
FAST RX mode	Voltage biasing active	Passive recessive	level_1 or level_0

For the parameters that are not described in Annex A, the specification in Clause 5 applies.

A.2 Static parameter

A.2.1 Recessive output characteristics

Table A.2 specifies the passive/active recessive output characteristics when voltage biasing is active.

Table A.2 — PMA passive/active recessive output characteristics terminated, voltage biasing active

Parameter [a]	Notation	Value		
		Min. [V]	**Nom.** [V]	**Max.** [V]
Single-ended output voltage on CAN_H (based on supply reference voltage) [a]	V_{CAN_H}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_H [b]	$V_{CAN\_H\_rec}$	2,256	+2,5	+2,756
Single-ended output voltage on CAN_L (based on supply reference voltage) [a]	V_{CAN_L}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_L [b]	$V_{CAN\_L\_rec}$	+2,256	+2,5	+2,756
Differential output voltage	V_{Diff}	−0,5	0	+0,05

NOTE The requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential output voltage.

[a] Measurement setup according to Figure 2:

$R_L > 10^{10}$ Ω

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

[b] Measurement setup according to Figure 2:

Load condition in SIC mode: 45 Ω ≤ R_L ≤ 65 Ω (tolerance ≤ ± 1 %)

C_1 = 4,7 pF (tolerance ≤ ± 5 %)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

A.2.2 Output characteristics SIC mode and FAST TX mode

Table A.3 specifies the voltages that are required for the CAN_L signals.

Table A.3 — PMA dominant output characteristics during SIC mode

Parameter[a]	Notation	Value [a]		Condition
		Min. [V]	**Max.** [V]	
Single-ended voltage on CAN_H	V_{CAN_H}	3,0	4,26	R_L = 45 Ω to 65 Ω
Single-ended voltage on CAN_L	V_{CAN_L}	0,75	2,01	R_L = 45 Ω to 65 Ω
Differential voltage on normal differential load	V_{Diff}	1,5	3,0	R_L = 45 Ω to 65 Ω
Differential voltage on effective resistance during arbitration	V_{Diff}	as specified in 5.3.4		
Differential voltage on extended differential load range (optional)	V_{Diff}	1,5	3,3	R_L = 45 Ω to 70 Ω

[a] Measurement setup according to Figure 2:

R_L, see “Condition” column in this table

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

Table A.4 specifies the voltages that are required on the CAN_H signals.

Table A.4 — PMA output characteristics during FAST TX mode

Parameter[a]		Notation	Value [a]		Condition
			Min. [V]	**Max.** [V]	
Single-ended voltage on CAN_H	level_0	V_{CAN_H0}	+2,55	+3,51	R_L = 45 Ω to 60 Ω
	level_1	V_{CAN_H1}	+1,50	+2,46	
Single-ended voltage on CAN_L	level_0	V_{CAN_L0}	+1,50	+2,46	
	level_1	V_{CAN_L1}	+2,55	+3,51	
Differential voltage on normal differential load	level_0	V_{Diff0}	+0,60	+1,50	
	level_1	V_{Diff1}	−1,50	−0,60	

[a] Measurement setup according to Figure 2:

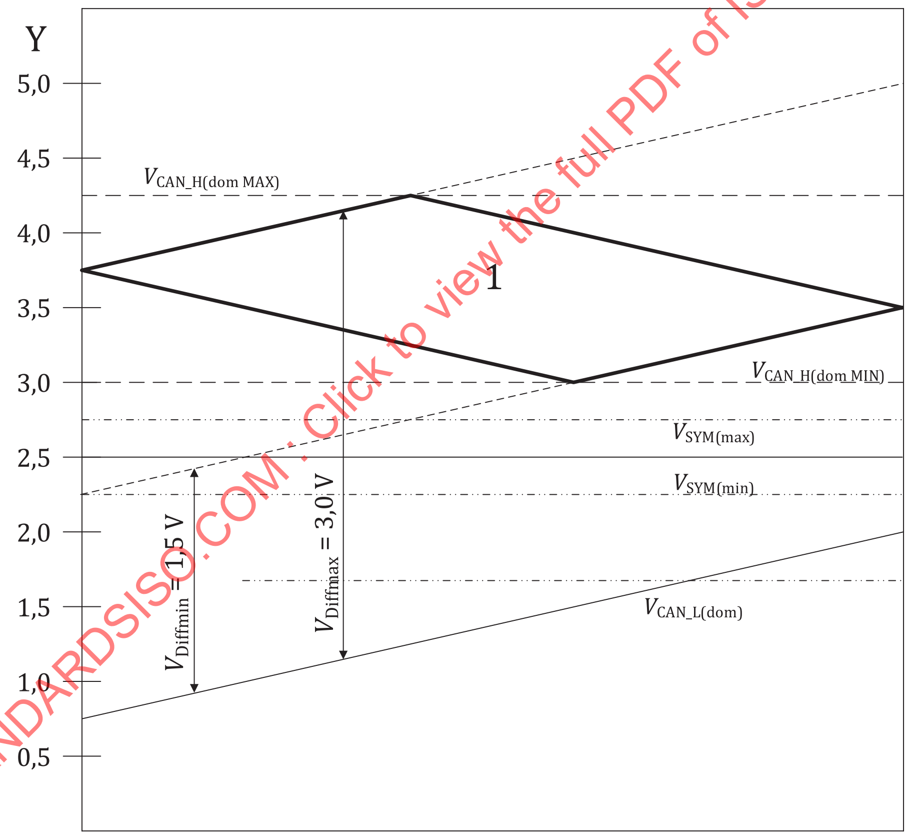
R_L, see "Condition" column in this table

C_1 = 0 pF (not present)

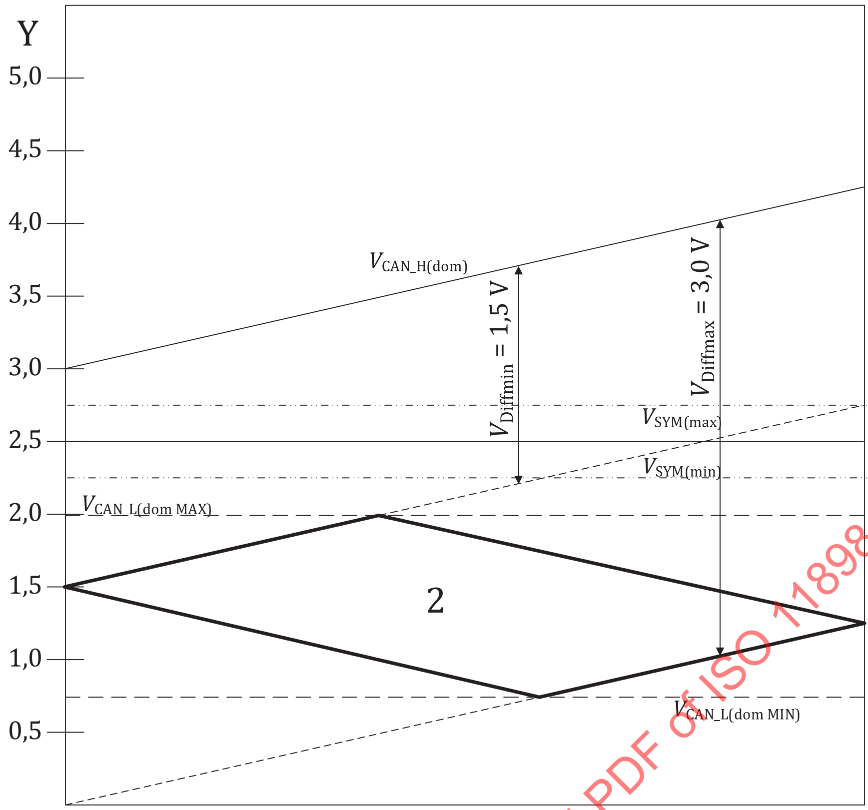
C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

Figure A.1 illustrates the voltage range for the dominant state during SIC mode. Figure A.2 illustrates the voltage range during FAST TX Mode.



a) Voltage range of V_{CAN_H} dominant while PMA is in SIC mode, when V_{CAN_L} varies from minimum to maximum voltage level (45-Ω to 65-Ω differential load condition)

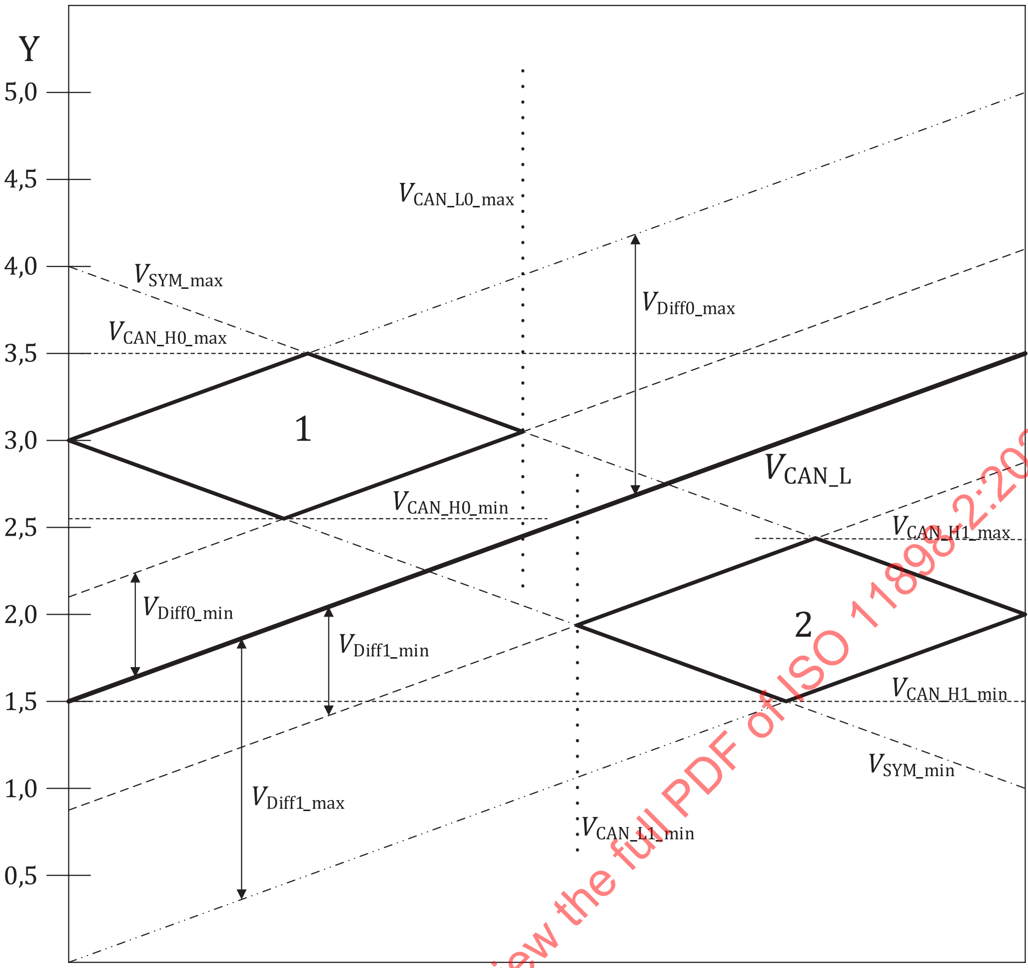


b) Voltage range of V_{CAN_L} dominant while PMA is in SIC mode, when V_{CAN_H} varies from minimum to maximum voltage level (45 Ω to 65 Ω differential load condition)

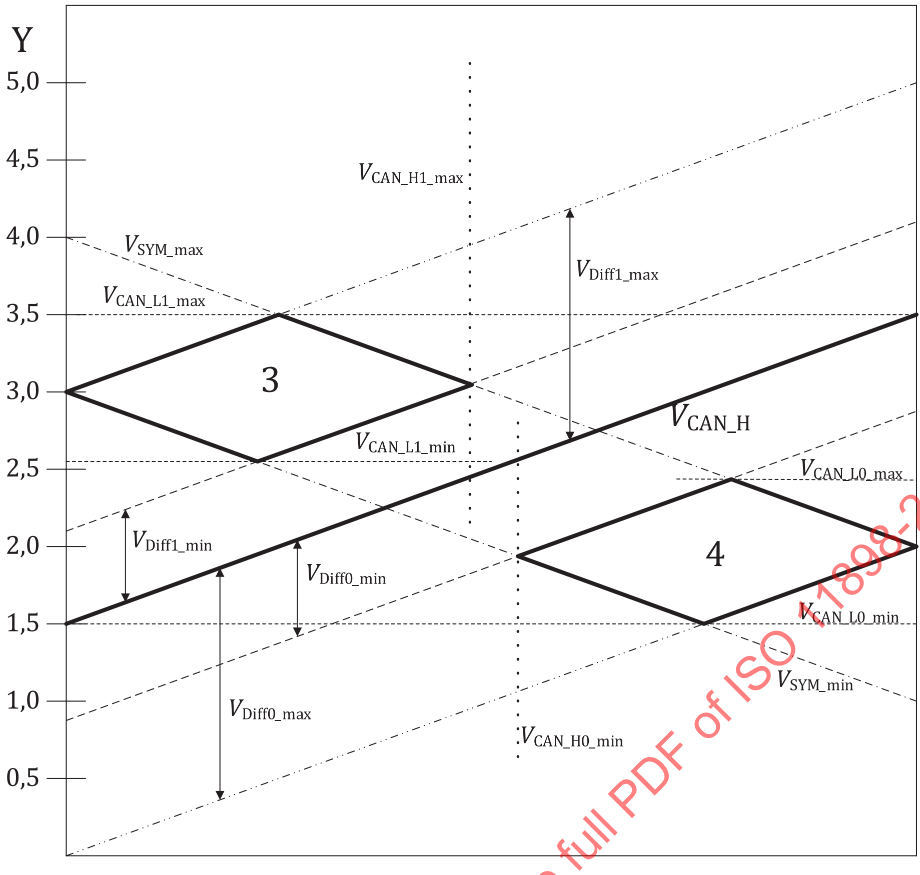
Key

1	range of V_{CAN_H} dominant
2	range of V_{CAN_L} dominant
V_{Diff}	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

Figure A.1 — Voltage range of V_{CAN_H} and V_{CAN_L} during dominant state while PMA is in SIC mode, when V_{CAN_L}, V_{CAN_H}, and Vcc vary from minimum to maximum voltage level (45 Ω to 65 Ω differential load condition)



a) Voltage range of VCAN_L0 and VCAN_L1 while PMA is in FAST TX mode, when VCAN_H0, VCAN_H1, and Vcc vary from minimum to maximum voltage level (45 Ω to 60 Ω differential load condition)



b) Voltage range of V_{CAN_H0} and V_{CAN_H1} while PMA is in FAST TX mode, when V_{CAN_L0}, V_{CAN_L1}, and V_{cc} vary from minimum to maximum voltage level (45 Ω to 60 Ω differential load condition)

Key

1	range of V_{CAN_H} level_0
2	range of V_{CAN_H} level_1
3	range of V_{CAN_L} level_0
4	range of V_{CAN_L} level_1
V_{Diff0}	differential voltage between CAN_H and CAN_L wires, level_0
V_{Diff1}	differential voltage between CAN_H and CAN_L wires, level_1
V_{CAN_H0}	single-ended voltage on CAN_H wire, level_0
V_{CAN_H1}	single-ended voltage on CAN_H wire, level_1
V_{CAN_L0}	single-ended voltage on CAN_L wire, level_0
V_{CAN_L1}	single-ended voltage on CAN_L wire, level_1

Figure A.2 — Voltage range of VCAN_L and VCAN_H while PMA is in FAST TX mode

A.2.3 PMA driver output current in FAST TX mode

Table A.5 specifies the PMA driver output current in FAST TX mode.

Table A.5 — PMA driver output current in FAST TX mode

Parameter[a]	Notation	Value (max.) [mA]	Condition
Absolute current on CAN_H	I_{CAN_H}	115	$-3\ V \leq V_{CAN\_H} \leq +18\ V$
Absolute current on CAN_L	I_{CAN_L}	115	$-3\ V \leq V_{CAN\_L} \leq +18\ V$

[a] Measurement setup according to Figure 2 with either V_{CAN_H} or V_{CAN_L} enforced to voltage levels as mentioned in the conditions by connection to an external voltage source.

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

A.2.4 Static receiver input characteristics, voltage biasing active, FAST RX mode or FAST TX mode

The receiver uses the transmitter output signals CAN_H and CAN_L as differential input. Table A.6 specifies the PMA static parameter input characteristics, voltage biasing active, FAST RX mode, and FAST TX mode parameters. This applies to the PMA implementation, when it is in FAST TX mode or FAST RX mode. The V_{Diff} differential input voltage ranges represent level_0 respectively level_1.

Table A.6 — PMA static receiver input characteristics, voltage biasing active, FAST RX mode or FAST TX mode

Parameter[a]	Notation	Value		Condition
		Min. [V]	Max. [V]	
Level_0 state differential input voltage range	V_{Diff}	+0,1	+8,0	$-12{,}0\ V \leq V_{CAN\_L}$, $V_{CAN\_H} \leq +12{,}0\ V$
Level_1 state differential input voltage range	V_{Diff}	−8,0	−0,1	

[a] Measurement setup according to Figure 2:

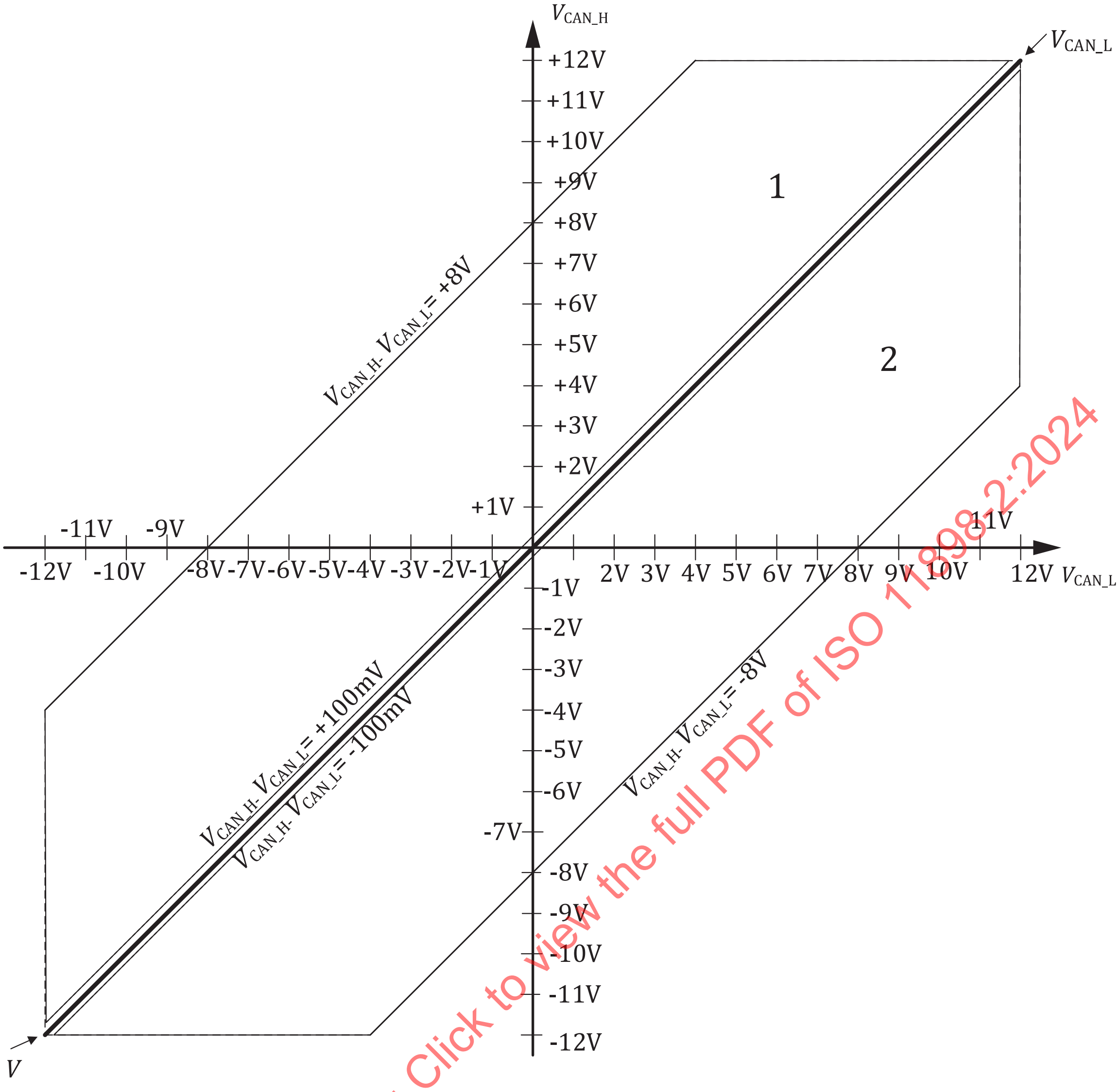
$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

Figure A.3 illustrates Table A.6.



Key

1	range of V_{CAN_H} RXD = 0
2	range of V_{CAN_H} RXD = 1
$V_{Diff} = V_{CAN\_H} - V_{CAN\_L}$	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

Figure A.3 — PMA static receiver input characteristics, voltage biasing active, PMA in FAST RX mode or FAST TX mode (condition −12,0 V ≤ V_{CAN_L}, V_{CAN_H} ≤ +12,0 V, +4,75 V ≤ Vcc ≤ +5,25 V)

A.2.5 Out-of-bounds (OOB) comparator

The OOB comparator uses the signals CAN_H and CAN_L as differential input. Figure A.4 specifies how the OOB and the comparator signals are linked with the RXD in SIC mode. The "&" (AND) gate is illustrating the logical function, how the OOB signal is merged into the RXD line for the CAN XL use case with FAST level schemes when the PMA implementation is in SIC mode as a receiving node.

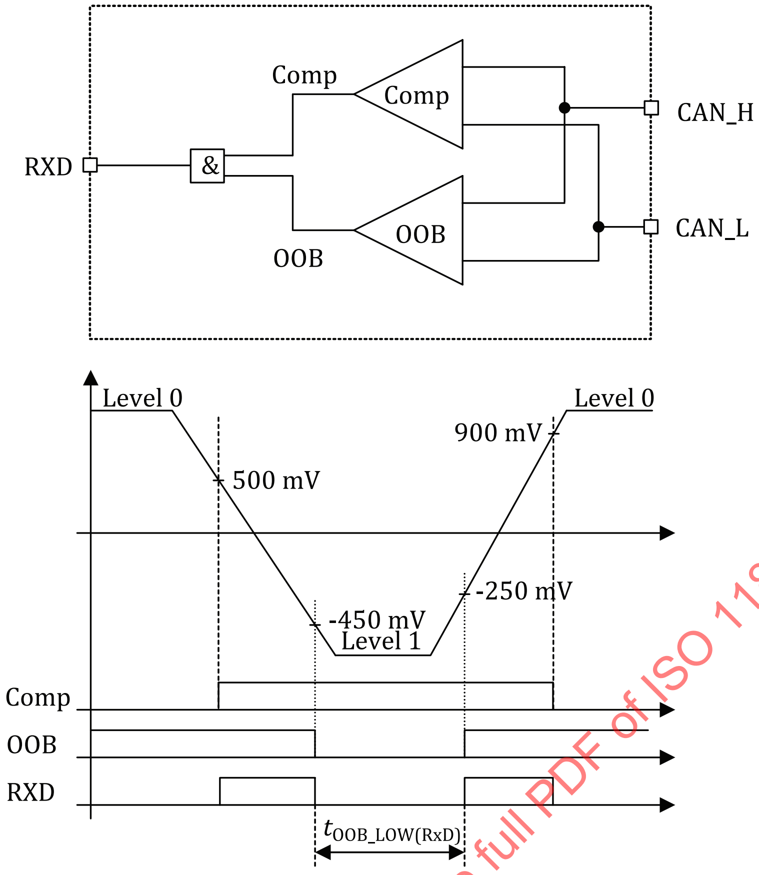


Figure A.4 — OOB and comparator signals when RXD is in SIC mode

Table A.7 specifies the OOB high state and OOB low state differential input voltage ranges, when the PMA implementation is in SIC mode and voltage biasing is active.

Table A.7 — PMA static OOB input characteristics (voltage biasing active; SIC mode)

Parameter[a]	Notation	Value		Condition
		Min. [V]	**Max.** [V]	
Low state differential input voltage range	V_{Diff}	−8,0	−0,45	$-12\ V \le V_{CAN\_L}, V_{CAN\_H} \le +12\ V$
High state differential input voltage range	V_{Diff}	−0,25	+8,0	

[a] Measurement setup according to Figure 2:

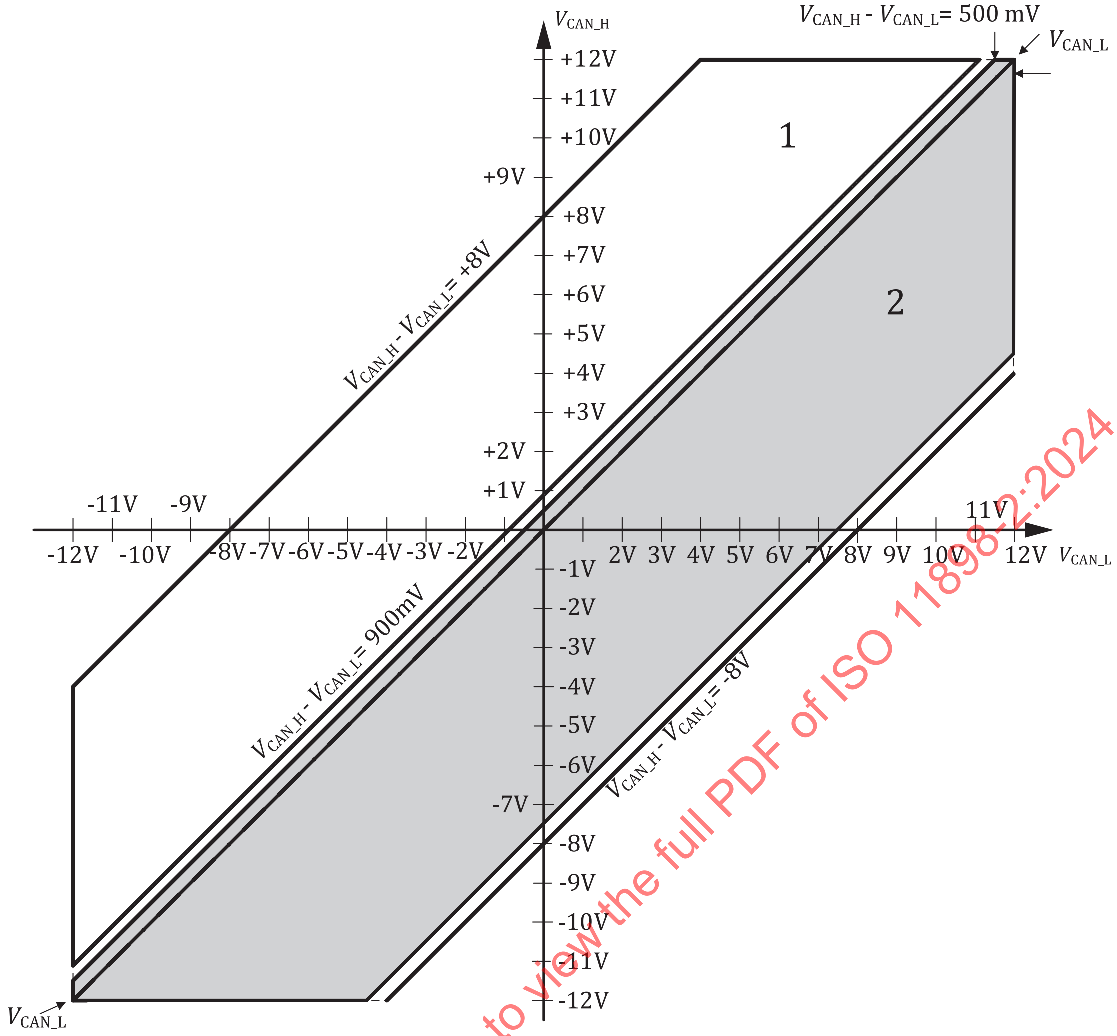
$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0$ pF (not present)

$C_2 = 0$ pF (not present)

$C_{RXD} = 0$ pF (not present)

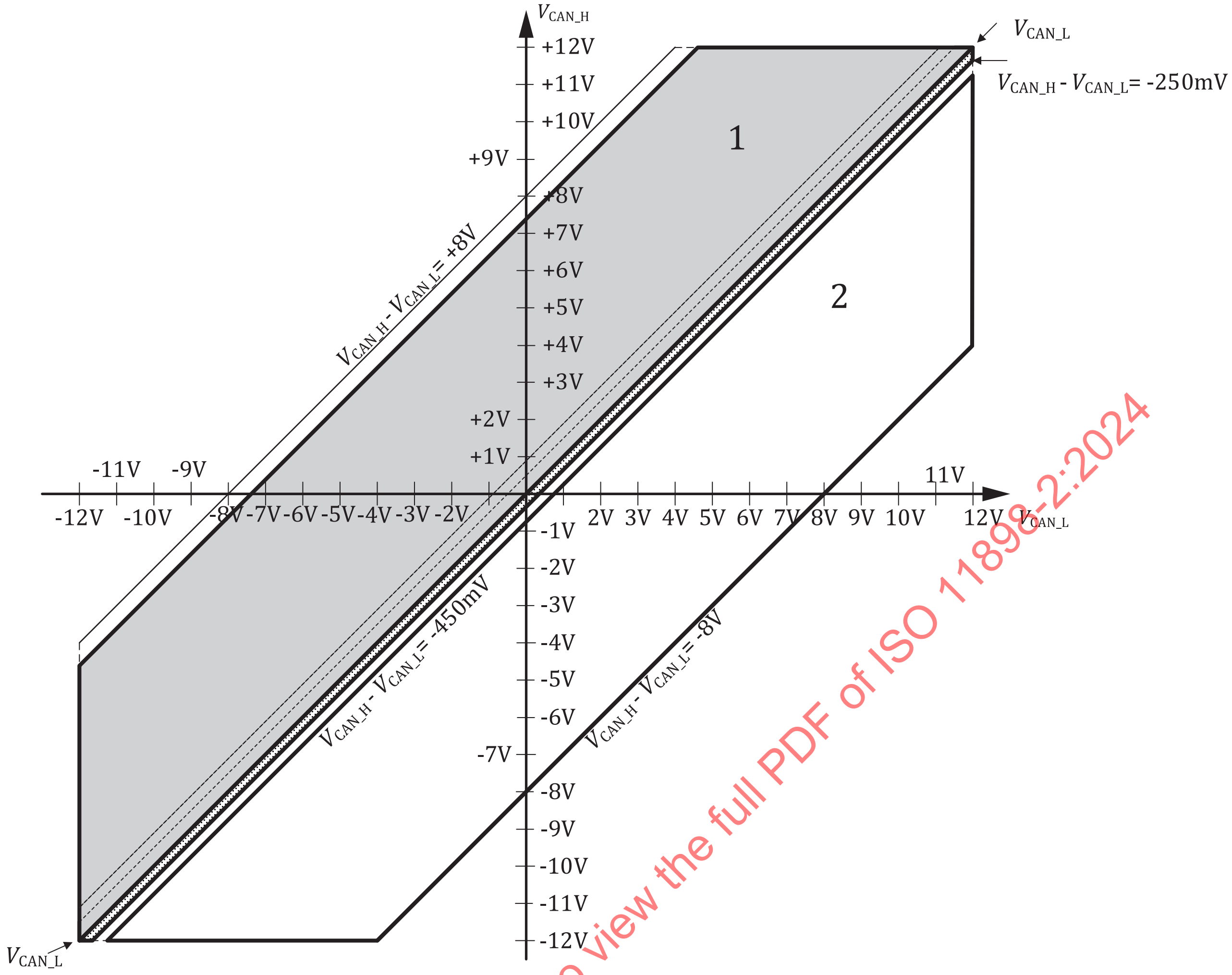
Figure A.5 illustrates the PMA static comparator receiver input characteristics (voltage biasing active, SIC mode). Figure A.6 illustrates the PMA static OOB receiver input characteristics (voltage biasing active, SIC mode). Figure A.7 illutrates the PMA static comparator and the OOB receiver input characteristics (voltage biasing active; SIC mode).



Key

1	range of V_{CAN_H}, RXD = 0
2	range of V_{CAN_H}, comparator output = 1
$V_{Diff} = V_{CAN\_H} - V_{CAN\_L}$	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

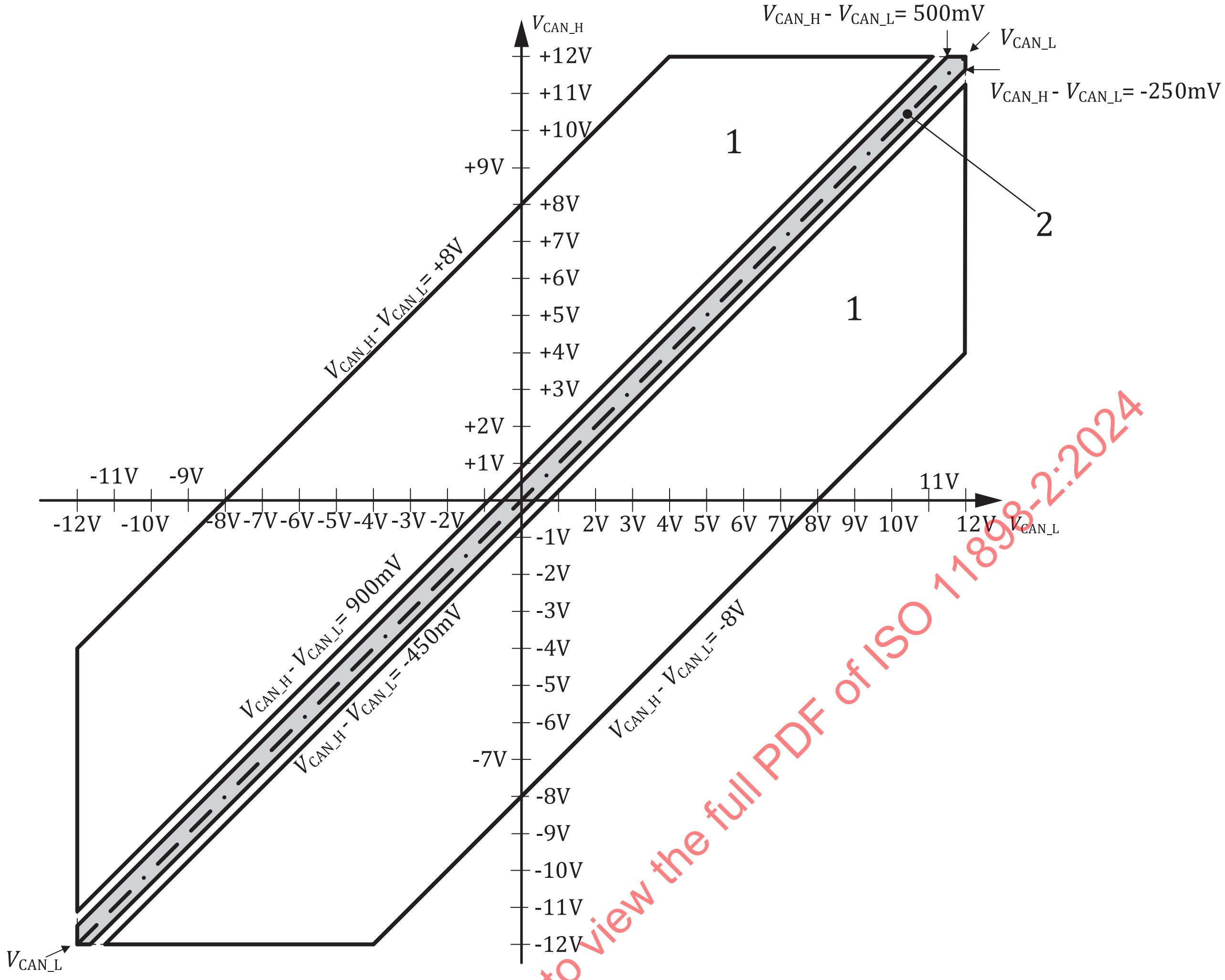
Figure A.5 — PMA static comparator receiver input characteristics (voltage biasing active; SIC mode; conditions: −12,0 V ≤ V_{CAN_L}, V_{CAN_H} ≤ +12,0 V, +4,75 V ≤ V_{cc} ≤ +5,25 V)



Key

1	range of V_{CAN_H}, OOB output = 1
2	range of V_{CAN_H}, OOB output = 0
$V_{Diff} = V_{CAN\_H} - V_{CAN\_L}$	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

Figure A.6 — PMA static OOB receiver input characteristics (voltage biasing active; SIC mode; conditions: −12,0 V ≤ V_{CAN_L}, V_{CAN_H} ≤ +12,0 V, +4,75 V ≤ V_{cc} ≤ +5,25 V)



Key

1	range of V_{CAN_H}, RXD = 0
2	range of V_{CAN_H}, RXD = 1
$V_{Diff} = V_{CAN\_H} - V_{CAN\_L}$	differential voltage between CAN_H and CAN_L wires
V_{CAN_H}	single-ended voltage on CAN_H wire
V_{CAN_L}	single-ended voltage on CAN_L wire

Figure A.7 — PMA static comparator and OOB receiver input characteristics, voltage biasing active, SIC mode (condition −12,0 V ≤ V_{CAN_L}, V_{CAN_H} ≤ +12,0 V, +4,75 V ≤ V_{cc} ≤ +5,25 V)

A.2.6 TXD input signal characteristic (normal-power mode)

The TXD signal input characteristic shall be applied to PMA implementations only if PMA implementations provide this input signal as a physically available signal. Figure A.8 specifies the TXD input circuitry.

The TXD input of the PMA implementation shall provide a symmetrical input impedance, which follows the input voltage level through a repeater functionality in normal-power mode. In case the TXD input level rises above the threshold $V_{(TXD)Thresh}$ as specified Table A.8, a pull-up behaviour towards the interface supply rail V_{IO} shall become active. In case the TXD input level falls below the threshold $V_{(TXD)Thresh}$ as specified in Table A.8, a pull-down behaviour towards GND shall become active. V_{IO} may be equal to V_{CC} and shall be assigned to the interface supply rail of the connected driving device (e.g. the CAN protocol controller that implements the DLL). The PMA implementation shall have an input impedance as specified in Table A.8. Furthermore, the input impedance shall meet the requirement specified in Table A.8.

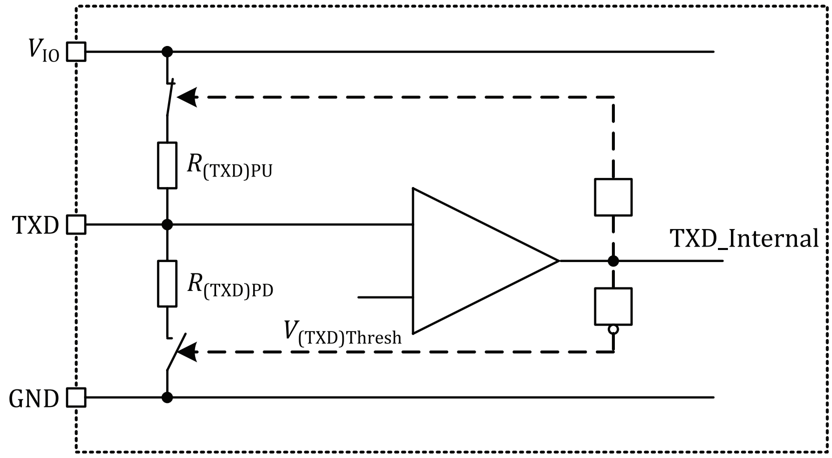


Figure A.8 — TXD input circuitry

Table A.8 — PMA TXD input characteristics

Parameter	Notation	Value		Remark
		Min.	Max.	
TXD input threshold voltage	$V_{(TXD)Thresh}$	0,95 (V_{IO}/2) V	1,05 (V_{IO}/2) V	Within V_{IO} specification range In this range the detection changes from low to high or vice versa.
TXD input low voltage range	$V_{(TXD)Low}$	GND	$V_{(TXD)Thresh\_min}$	Within V_{IO} specification range In this range the TXD input level is detected as low. The min value can be below GND in accordance with the PMA implementations.
TXD input high voltage range	$V_{(TXD)High}$	$V_{(TXD)Thresh\_max}$	V_{IO}	Within V_{IO} specification range In this range the TXD input level is detected as high. The max value can be above V_{IO} in accordance with the PMA implementations.
Pull-up and pull-down impedance	$R_{(TXD)PU}$ $R_{(TXD)PD}$	20 kΩ	80 kΩ	Within V_{IO} specification range
Pull-up and pull-down impedance matching [a]	$m_{R(TXD)}$	−0,05	+0,05	Within V_{IO} specification range

[a] The matching shall be calculated as $m_{R(TXD)} = 2 \times (R_{(TXD)PU} - R_{(TXD)PD}) / (R_{(TXD)PU} + R_{(TXD)PD})$.

A.3 Dynamic parameter

A.3.1 PMA driver symmetry FAST TX mode

In order to achieve a level of the RF emission that is acceptably low, the transmitter shall meet the driver signal symmetry in SIC mode and in FAST TX mode as specified in Table A.9.

Table A.9 — PMA driver symmetry

Parameter[a]	Notation	Value [b]	
		Min.	Max.
Driver symmetry[a]	v_{sym}	0,95	1,05

[a] $v_{sym} = (V_{CAN\_H} + V_{CAN\_L})/V_{rec}$,

$V_{rec} = V_{CAN\_H\_rec} + V_{CAN\_L\_rec}$

[b] Measurement setup according to Figure 2:

Load condition in SIC mode: 45 Ω ≤ R_L ≤ 65 Ω

Load condition in FAST RX mode or FAST TX mode: 45 Ω ≤ R_L ≤ 60 Ω

C_1 = 4,7 nF (tolerance ≤ ± 5 %)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

A.3.2 PMA transmit timeout SIC mode

In SIC mode the PMA implementation shall limit the duration of dominant transmission as specified in Table A.10, in order to prevent a permanent dominant clamping condition when the TXD input is permanently asserted.

Table A.10 — PMA transmit timeout

Parameter	Notation	Value	
		Min. [ms]	Max. [ms]
Transmit dominant timeout	t_{dom}	0,80	6,0

A.3.3 Transmitter, receiver and OOB timing behaviour

The timing parameters specified in Table A.11, Table A.12, Table A.13, and Table A.14 shall be measured at the RXD output and the TXD input of the PMA implementation as well as on the differential voltage between CAN_H and CAN_L. Table A.11 specifies the loop delay requirement for SIC mode. Table A.12 and Table A.13 specify the data signal timing requirements during SIC mode and during FAST RX or FAST TX Mode. Table A.14 specifies the propagation delay symmetry requirements during mode transition.

For the impedance specification see Table 9.

For measuring the timing in the signal traces, Figure A.9 specifies the timing diagram during SIC mode; Figure A.10 illustrates the timing diagram during FAST TX mode and PWM driven; Figure A.11 illustrates the PMA OOB implementation timing diagram during SIC mode and PWM driven; Figure A.12 illustrates the timing diagram in the transition from SIC mode to FAST TX mode; Figure A.13 illustrates the timing diagram in the transition from FAST TX mode to SIC mode; Figure A.14 illustrates the SIC mode time after FAST RX detection; Figure A.15 illustrates the propagation delay symmetry in the mode transition.

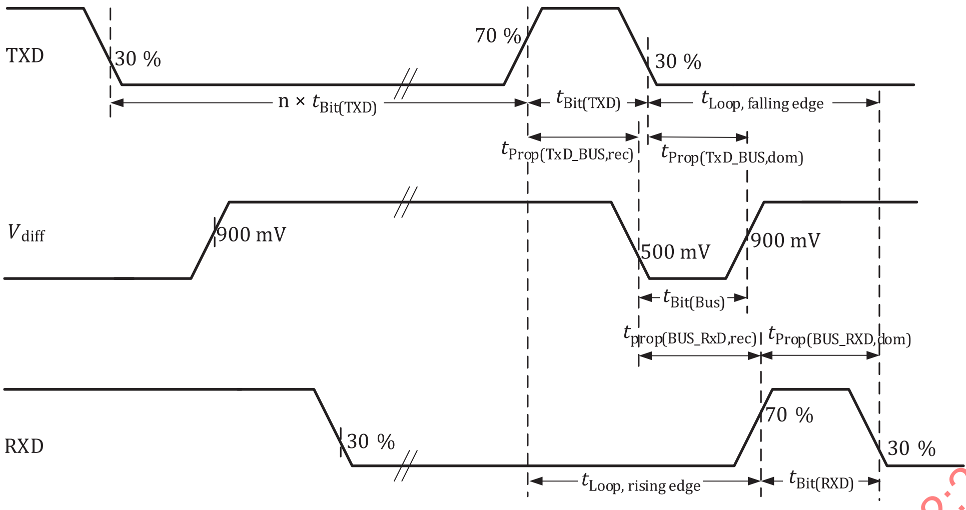
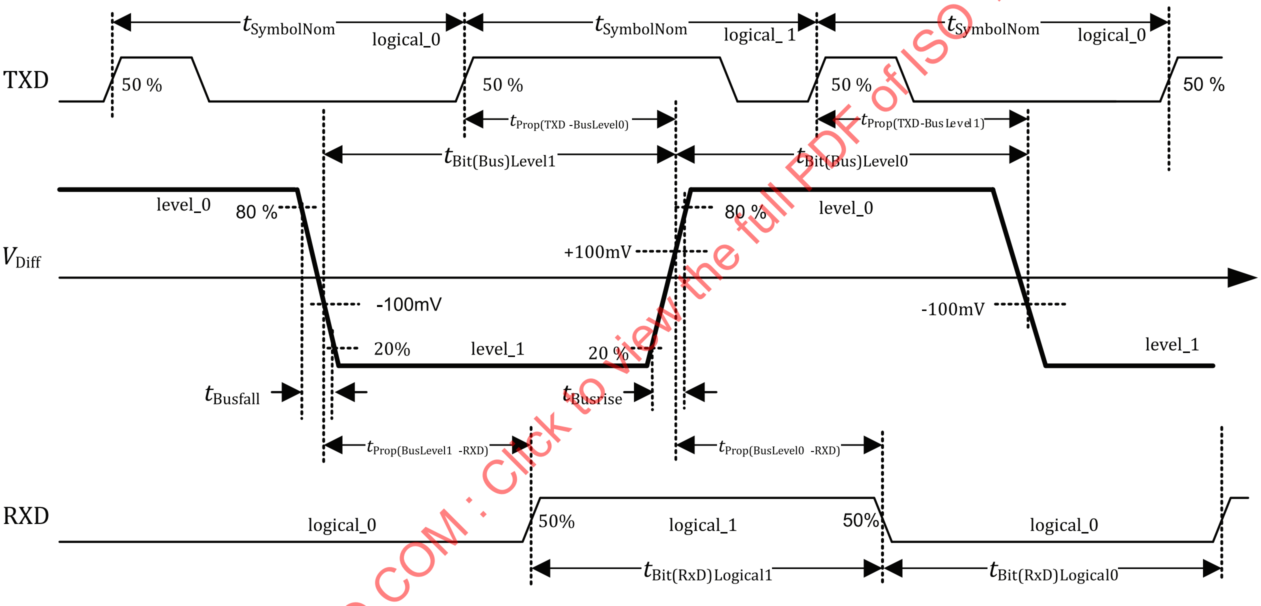
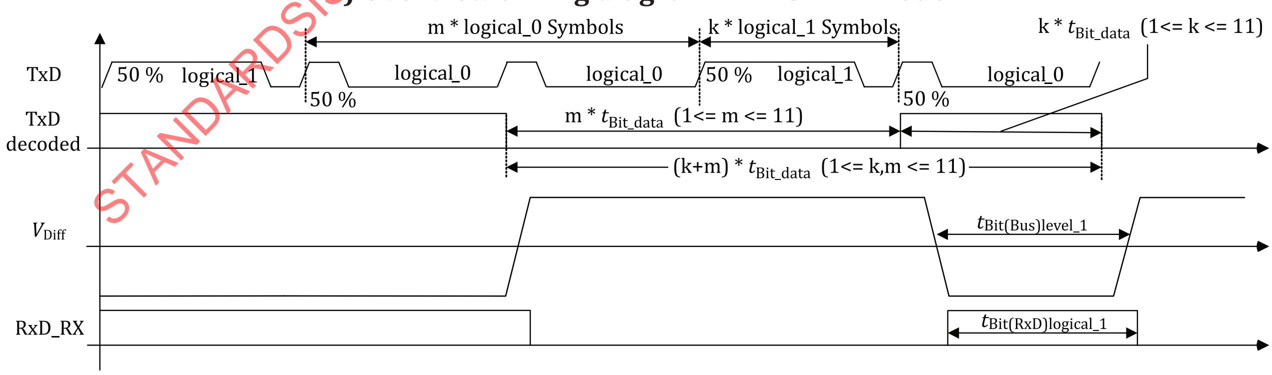


Figure A.9 — PMA implementation timing diagram, during SIC mode



a) Overview timing diagram in FAST TX mode



b) Symmetry of level_1 timing diagram in FAST TX mode

Figure A.10 — PMA implementation timing diagram, during FAST TX mode, PWM driven

The delay from TXD to the CAN_H and CAN_L in FAST TX Mode as shown in Figure A.10 a) shall be measured from the rising TXD edge of the PWM symbol forcing the according level change on CAN_H and CAN_L.

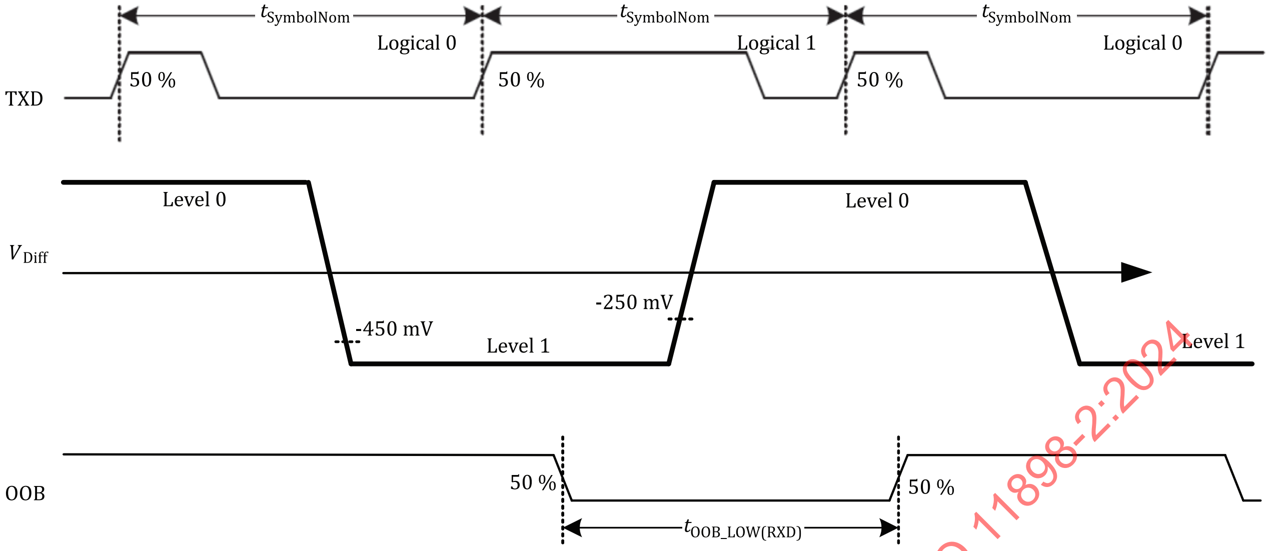


Figure A.11 — PMA OOB implementation timing diagram, during SIC mode, PWM driven

NOTE Figure A.11 illustrates the timing behaviour on RXD of a receive node in SIC mode while another node is sending in FAST TX mode. Eventually, the OOB comparator output signal is not physically available to the outside of a transceiver. Therefore, Figure A.11 illustrates the transceiver internal OOB signal and how it is reflected later in length on the RXD pin of a receiving node in SIC mode.

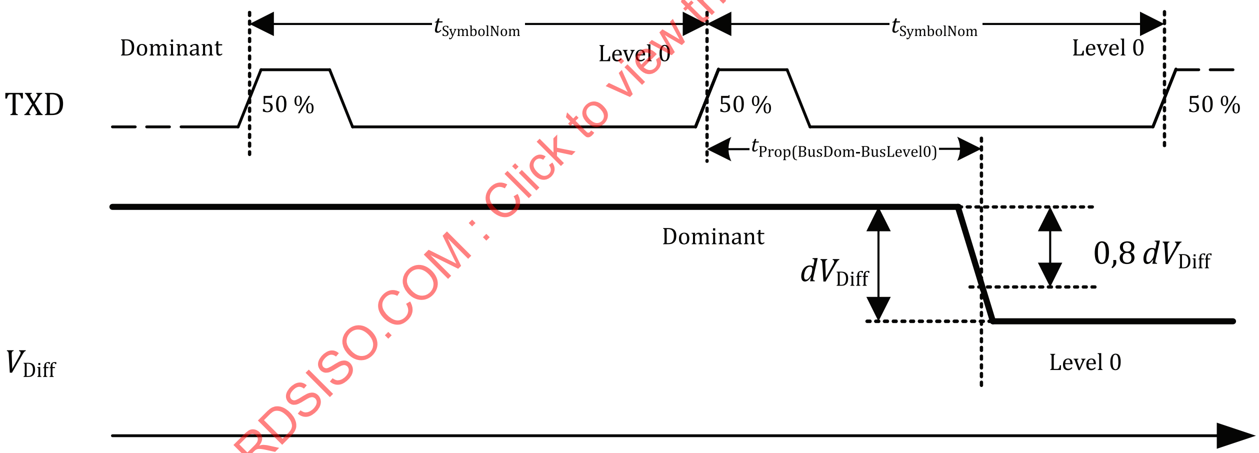
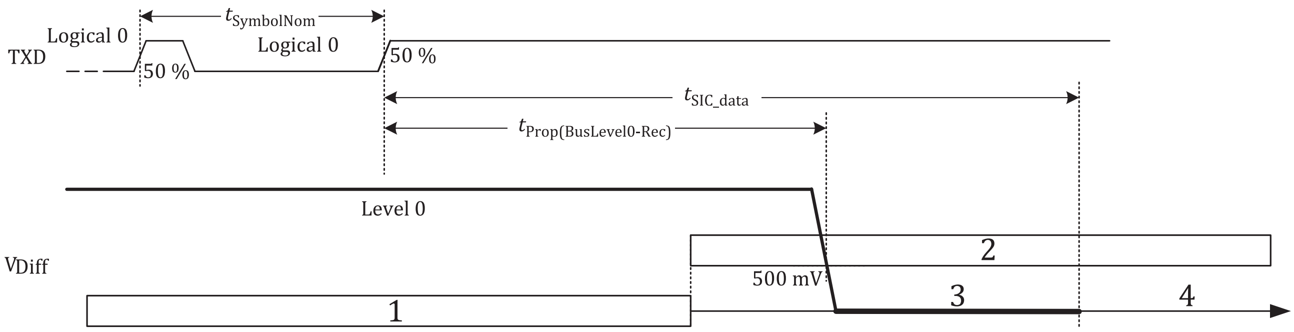


Figure A.12 — PMA implementation timing diagram, transition SIC mode to FAST TX mode, PWM driven



Key

1 receiver threshold range FAST mode

2 receiver threshold range SIC mode

3 active recessive

4 passive recessive

Figure A.13 — PMA implementation timing diagram, transition FAST TX mode to SIC mode, PWM driven

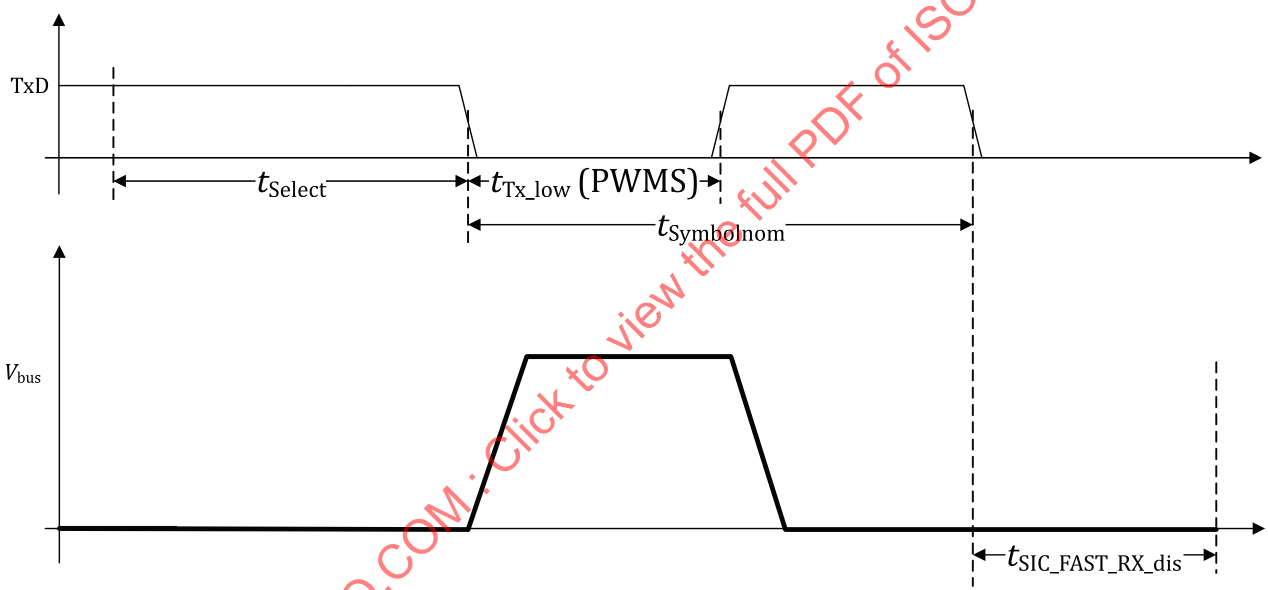


Figure A.14 — PMA implementation timing diagram, SIC mode time after FAST RX detection

Table A.11 — PMA implementation loop delay requirement for SIC mode

Parameter[b]	Notation	Value	
		Min. [ns]	**Max.** [ns]
Loop delay[a]	t_{Loop}	not defined	190

[a] Time span from signal edge on TXD input to the corresponding signal edge with the same polarity on RXD output; the maximum delay of both signal edges is to be considered.

[b] Measurement setup according to Figure 2:

$45\ \Omega \leq R_L \leq 65\ \Omega$

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ± 1 %)

C_{RXD} = 15 pF (tolerance ≤ ± 1 %)

Table A.12 — PMA implementation data signal timing requirements, during SIC mode

Parameter[a]	Notation	Value		Remark
		Min. [ns]	Max. [ns]	
Signal improvement time	t_{SIC}	+300	+530	Time from rising edge of the TXD signal to the end of the signal improvement phase
Transmitted bit width variation	$t_{\Delta Bit(Bus)}$	−10	+10	Bus recessive bit length variation relative to TXD bit length, see Figure A.9 $t_{\Delta Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TXD)}$
Received bit width variation	$t_{\Delta Bit(RXD)}$	−30	+20	RXD recessive bit length variation relative to TXD bit length, see Figure A.9 $t_{\Delta Bit(RXD)} = t_{Bit(RXD)} - t_{Bit(TXD)}$
Receiver timing symmetry	$t_{\Delta REC}$	−20	+15	RXD recessive bit length variation relative to bus bit length, see Figure A.9 $t_{\Delta REC} = t_{Bit(RXD)} - t_{Bit(Bus)}$
Propagation delay from TXD logical 0 to bus dominant	$t_{Prop(TXD-BusDom)}$	not defined	+80	See Figure A.9
Propagation delay from TXD logical 1 to bus recessive	$t_{Prop(TXD-BusRec)}$	not defined	+80	See Figure A.9
Propagation delay of the receiver from bus to RXD logical 0	$t_{Prop(BusDom-RXD)}$	not defined	+110	See Figure A.9
Propagation delay of the receiver from bus to RXD logical 1	$t_{Prop(BusRec-RXD)}$	not defined	+110	See Figure A.9
RXD low pulse width during fast data traffic[b], at the bit rate 10 Mbit/s	$t_{OOB\_LOW\,(RXD)}$	+30	not defined	$t_{Bit(TXD)}$ = 100 ns see Figure A.11
RXD low pulse width during fast data traffic[b], at the bit rate 20 Mbit/s	$t_{OOB\_LOW\,(RXD)}$	+15	not defined	$t_{Bit(TXD)}$ = 50 ns see Figure A.11

[a] Measurement setup according to Figure 2:
$45\ \Omega \le R_L \le 65\ \Omega$
$C_1 = 0$ pF (not present)
$C_2 = 100$ pF (tolerance ≤ ± 1 %)
$C_{RXD} = 15$ pF (tolerance ≤ ± 1 %)
Measurement according to Figure A.9:
The input signal on TXD shall have rising times (10 % to 90 %) and fall times (90 % to 10 %) of less than 10 ns with n = 1 to 5.

[b] Measured through FAST TX mode sending with associated data bit rate while accessing the OOB comparator through a dedicated test mode (semiconductor-manufacturer specific).
Measurement setup according to Figure 2 for FAST TX mode:
$4{,}75\ V \le V_{CC} \le 5{,}25\ V$
$45\ \Omega \le R_L \le 60\ \Omega$
$C_1 = 0$ pF
$C_2 = 25$ pF
$C_{RXD} = 15$ pF

Table A.13 — PMA implementation data signal timing requirements, during FAST RX mode or FAST TX mode

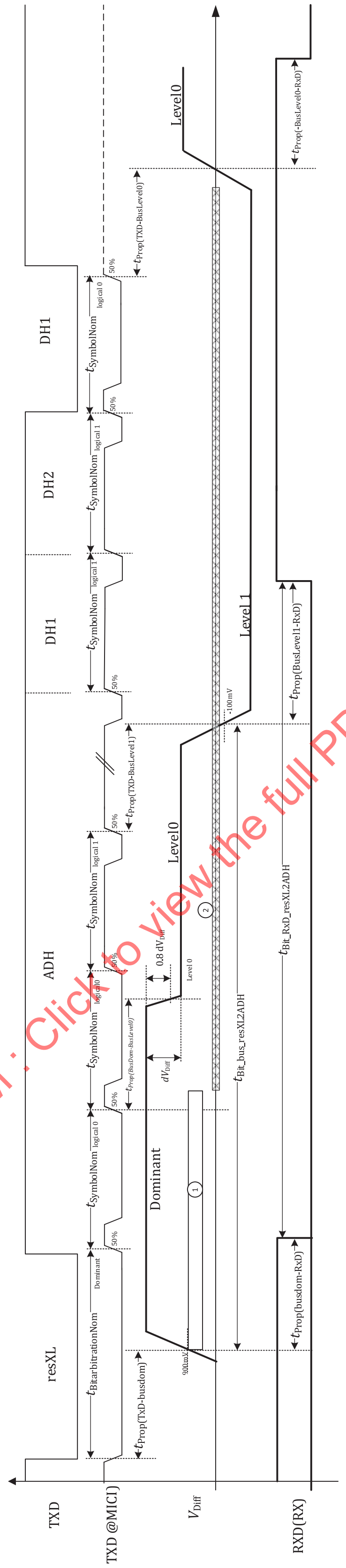
Parameter[a]	Notation	Min. [ns]	Max. [ns]	Remark
Signal improvement time in FAST TX Mode	t_{SIC_data}	not defined	+775	Time from rising edge of TXD symbol to the end of the signal improvement phase, see Figure A.13
SIC mode time after FAST RX detection	$t_{SIC\_Fast\_RXD\_Dis}$	not defined	+80	Time starting with the second falling edge that is used for PWM detection see Figure A.14
Transmitted level_1 bit width variation in FAST TX Mode	$t_{\Delta Bit(Bus)Level1}$	−5	+5	Bus level_1 bit length variation relative to TXD t_{Bit_data} length, see Figure A.10 b) $t_{\Delta Bit(Bus)Level1} = t_{Bit(Bus)Level1} - k * t_{Bit\_data}$
Received logical 1 bit width variation in FAST TX Mode	$t_{\Delta Bit(RxD)Logical1}$	−10	+10	RXD logical 1 bit length variation relative to TXD t_{Bit_data} length, see Figure A.10 b) $t_{\Delta Bit(RxD)Logical1} = t_{Bit(RXD)Logical1} - k * t_{Bit\_data}$
Logical 1 receiver timing symmetry in FAST RX Mode	$t_{\Delta REC\_Logical1}$	−5	+5	RXD logical 1 bit length variation relative to bus level_1 bit length, see Figure A.10 b) $t_{\Delta REC\_Logical1} = t_{Bit(RXD)Logical1} - t_{Bit(Bus)Level1}$
Propagation delay from mode change to bus level_0	$t_{Prop(BusDom\text{-}BusLevel0)}$	not defined	+80	See Figure A.12
Propagation delay from mode change to bus recessive in FAST TX and FAST RX Mode	$t_{Prop(BusLevel0\text{-}Rec)}$	not defined	+325	See Figure A.13
Propagation delay from TXD logical 0 to bus level_0	$t_{Prop(TXD\text{-}BusLevel0)}$	not defined	+80	See Figure A.10 a)
Propagation delay from TXD logical 1 to bus level_1	$t_{Prop(TXD\text{-}BusLevel1)}$	not defined	+80	See Figure A.10 a)
Propagation delay from bus level_0 to RXD logical 0	$t_{Prop(BusLevel0\text{-}RXD)}$	not defined	+110	See Figure A.10 a)
Propagation delay from bus level_1 to RXD logical 1	$t_{Prop(BusLevel1\text{-}RXD)}$	not defined	+110	See Figure A.10 a)
Fall time V_{Diff}	$t_{Busfall}$	+6	+20	See Figure A.10 a)
Rise time V_{Diff}	$t_{Busrise}$	+6	+20	See Figure A.10 a)

[a] Measurement setup according to Figure 2:
$45\ \Omega \le R_L \le 60\ \Omega$
$C_1 = 0$ pF (not present)
$C_2 = 25$ pF (tolerance ≤ ± 1 %)
$C_{RXD} = 15$ pF (tolerance ≤ ± 1 %)

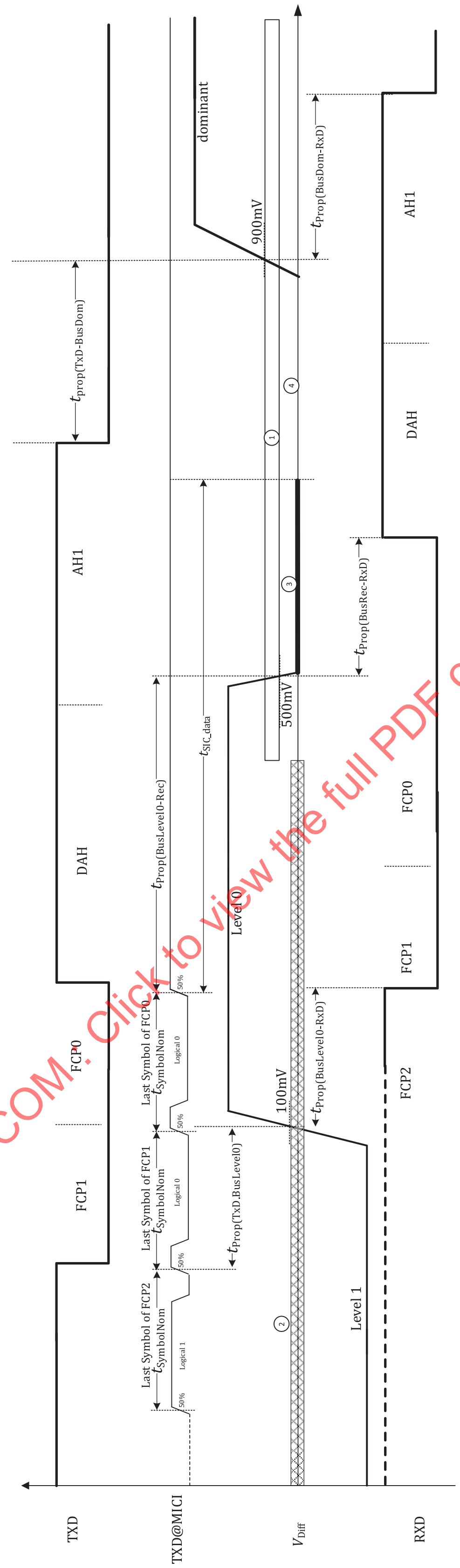
Table A.14 — PMA implementation propagation delay symmetry requirements, during mode transition

Parameter[a]	Notation	Min. [ns]	Max. [ns]	Remark
Transmitter propagation delay symmetry ADS/DAS	$t_{\Delta Bit(Bus)ADS/DAS}$	−30	+30	see Figure A.15 $t_{\Delta Bit(Bus)ADS/DAS} = t_{Prop(TXD\text{-}BusDom)} - t_{Prop(TXD\text{-}BusLevel0)}$
Receiver propagation delay symmetry ADS/DAS	$t_{\Delta Bit(RXD)ADS/DAS}$	−20	+20	see Figure A.15 $t_{\Delta Bit(RXD)ADS/DAS} = t_{Prop(BusDom\text{-}RXD)} - t_{Prop(BusLevel0\text{-}RXD)}$

[a] Measurement setup according to Figure 2:
$4{,}75\ V \le V_{CC} \le 5{,}25\ V$
$45\ \Omega \le R_L \le 60\ \Omega$
$C_1 = 0$ pF
$C_2 = 25$ pF
$C_{RXD} = 15$ pF



a) Transition SIC mode to FAST TX mode PWM driven



b) Transition FAST TX mode to SIC mode

Key

1 receiver threshold range SIC mode

2 receiver threshold range FAST mode

3 active recessive

4 passive recessive

Figure A.15 — PMA implementation propagation delay symmetry

A.3.4 PMA mode selection and decoding

The PMA mode selection shall be available through a PWM-coded TXD input signal. Similar edges of the TXD signal with a period time of shorter than $t_{SymbolNom}$ shall switch the mode of the PMA towards FAST RX mode or FAST TX mode.

Consecutive TXD signal period times (logical 0 or logical 1) longer than $t_{FastToSIC}$ during FAST RX mode or FAST TX mode shall switch the mode of the PMA towards the SIC mode.

The PMA shall provide the following behaviours:

1) FAST TX mode (for the sending node);

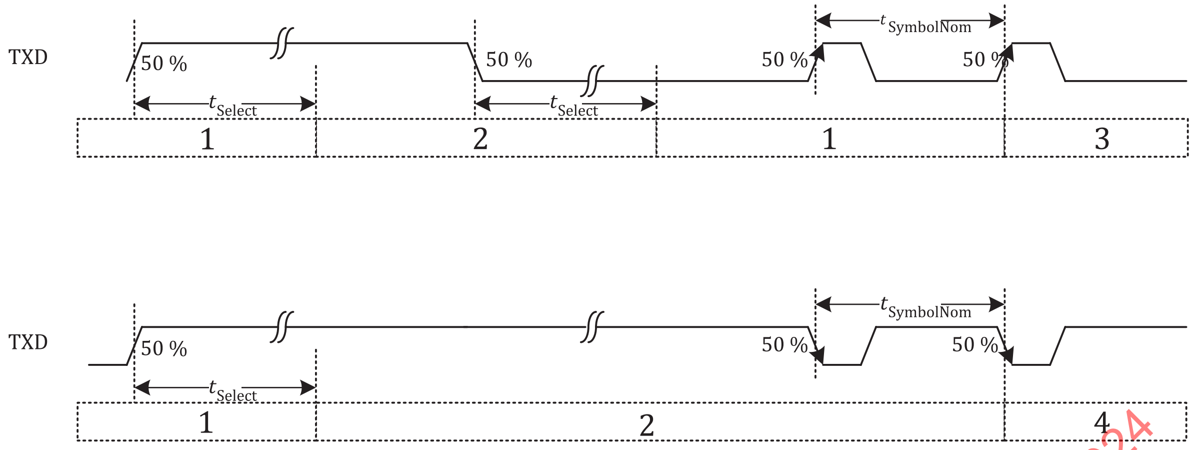
2) FAST RX mode (for all receiving nodes).

The PMA shall distinguish the required behaviour based on the last received bit level on pin TXD without PWM encoding. FAST TX mode shall be preselected, if there is a consecutive logical 0 on pin TXD detected for t_{Select}. FAST RX shall be preselected, if there is a consecutive logical 1 on pin TXD detected for t_{Select}. Based on the preselected mode the PMA shall execute the mode transition with the first detected PWM symbol. Table A.15 specifies the timing requirements of the PMA mode selection. Figure A.16 specifies the PMA mode selection through PWM symbols.

Table A.15 — PMA mode selection timing requirements

Parameter	Notation	Min. [ns]	Max. [ns]	Remark
PWM symbol acceptance length[a]	$t_{SymbolNom}$	45	205	Time between two rising edges on TXD if FAST TX mode is preselected. Time between two falling edges on TXD if FAST RX mode is preselected. PMA implementations can support shorter $t_{SymbolNom}$ periods than 45 ns.
FAST to SIC mode switching time [a]	$t_{FastToSIC}$	210	245	Time after last symbol edge on TXD
PWM ratio detected as logical_0 FAST TX	$t_{Logical\_0\_Tx}$	t_{Decode}	0,5 * $t_{SymbolNom}$ - t_{Decode}	PWM ratio detected as logical_0 in FAST TX mode
PWM ratio detected as logical_1 FAST TX	$t_{Logical\_1\_Tx}$	0,5 * $t_{SymbolNom}$ + t_{Decode}	$t_{SymbolNom}$ - t_{Decode}	PWM ratio detected as logical_1 in FAST TX mode
PWM ratio detected FAST RX	$t_{Logical\_Rx}$	t_{Decode}	$t_{SymbolNom}$ - t_{Decode}	PWM ratio detected in FAST RX mode
Mode pre-selection time	t_{Select}	500	980	Consecutive received bit level time for preselection of the required FAST RX mode or FAST TX mode.
PWM detection resolution	t_{Decode}	Not defined	5	Granularity of TXD symbol decoding

[a] Up to 205 ns, it reads as PWM-coded signals and starting from 250 ns the signals are NRZ-coded (8 Mbit/s).



Key

1 FAST TX mode pre-selection

2 FAST RX mode pre-selection

3 FAST TX mode level_0

4 FAST RX mode

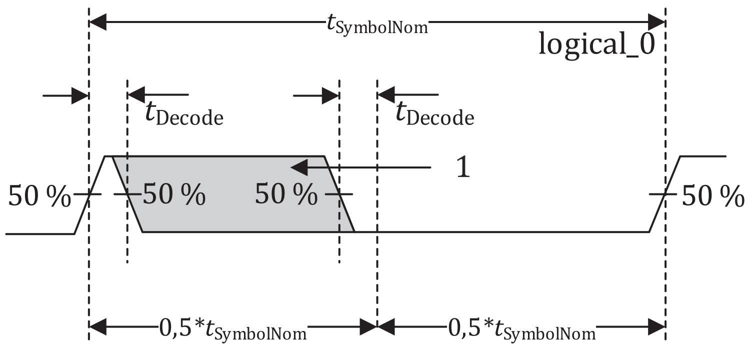
Figure A.16 — Mode selection through PWM

As specified in Figure A.16, if FAST RX mode is preselected, the PMA shall detect the PWM signal based on falling edges on the TXD signal; if FAST TX mode is preselected, the PMA shall detect PWM signals based on rising edges on the TXD signal.

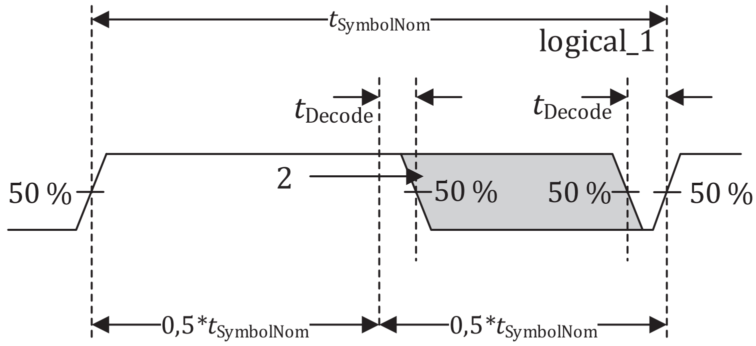
The high to low ratio of consecutive TXD symbols between two rising edges shall be used during FAST TX Mode to distinguish between level_0 and level_1.

In case the TXD signal between two rising edges is logical 1 for more than 50 % of $t_{SymbolNom}$, the PMA in FAST TX mode outputs a level_1 signal with the detected rising edge. In case the TXD signal between two rising edges is logical 0 for more than 50 % of $t_{SymbolNom}$, the PMA in FAST TX mode outputs a level_0 signal with the detected rising edge.

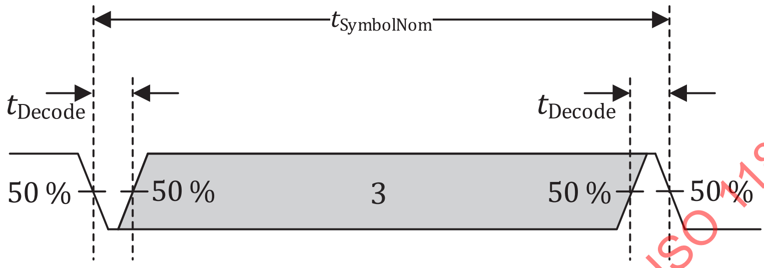
The PMA shall detect and decode PWM symbols from the TXD signal with a PWM detection resolution t_{Decode} as specified in Table A.15. Figure A.17 specifies the worst-cases how to decode the PWM symbols correctly. If FAST TX mode is preselected or during FAST TX mode a PWM duration between t_{Decode} and 0,5 × $t_{SymbolNom}$ - t_{Decode} shall be detected as logical 0 and cause a level_0 on the bus as specified in Figure A.17 a). If FAST TX mode is preselected or during FAST TX mode a PWM duration between 0,5 × $t_{SymbolNom}$ - t_{Decode} shall be detected as logical 1 and cause a level_1 on the bus as specified in Figure A.17 b). If FAST RX mode is preselected or during FAST RX mode a PWM duration between t_{Decode} and $t_{SymbolNom}$ - t_{Decode} shall be detected as valid symbol as specified in Figure A.17 c). The PWM symbol has no logical value, because any PWM symbol is allowed for the receiving node.



a) Transmitting PMA worst-case level_0 PWM symbol to be decoded



b) Transmitting PMA worst-case level_1 PWM symbol to be decoded



c) Receiving PMA worst-case PWM symbol

Key

1 detection area of logical_0

2 detection area of logical_1

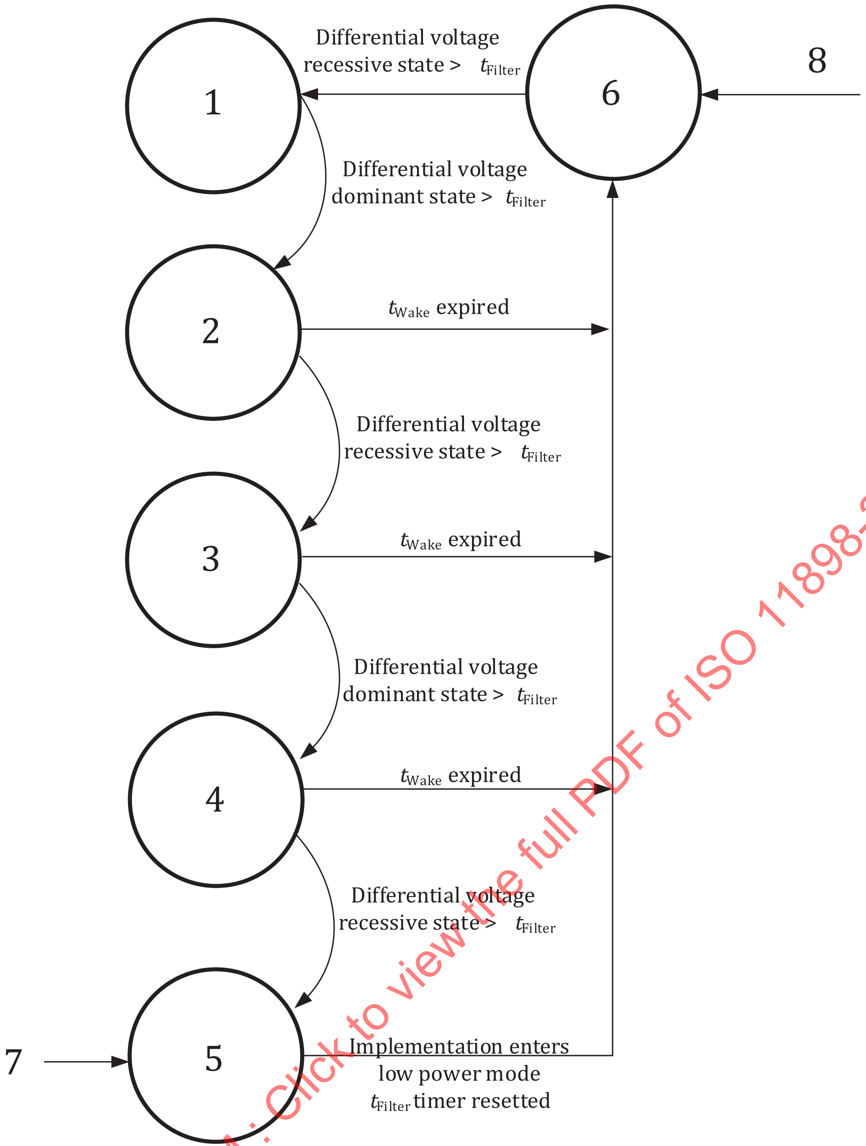
3 detection area

Figure A.17 — Worst-case level_0 and level_1 PWM symbol to be decoded

A.4 Wake-up from low-power mode

A.4.1 Via wake-up pattern

Upon receiving two consecutive dominant states each for duration of at least t_{Filter}, separated by a recessive state of at least t_{Filter} and followed by a recessive state with duration of at least t_{Filter}, a wake-up event shall be signalled. The bus biasing can be activated.



Key

1 INI state: no wake-up detected

2 state A: no wake-up detected

3 state B: no wake-up detected

4 state C: no wake-up detected

5 state D: wake-up detected – entering this state shall signal the bus wake-up event and may turn on the bias through implementation-specific measures

6 wait state

7 transition from other nodes; PMA implementation enters normal mode

8 power on

Figure A.18 — Wake-up pattern

The finite state machine in Figure A.18 specifies the voltage wake-up behaviour for all operation modes.

When entering state A, the optional timer t_{Wake} shall be reset and restarted.

Table A.16 specifies the voltage wake-up control timings. Figure A.19 illustrates the test signal definition for bus wake-up reaction time measurement. Figure A.20 illustrates the test signal definition for extended