

INTERNATIONAL
STANDARD

ISO
10483-2

First edition
1996-02-01

**Road vehicles — Intelligent power
switches —**

Part 2:

Low-side intelligent power switch

*Véhicules routiers — Sectionneurs de puissance intelligents —
Partie 2: Sectionneur de puissance intelligent en version d'aval*



Reference number
ISO 10483-2:1996(E)

Contents

	Page
1 Scope	1
2 Normative references	1
3 Definitions	1
4 Functioning	3
5 Electrical specifications	6
6 Test methods	10

STANDARDSISO.COM : Click to view the full PDF of ISO 10483-2:1996

© ISO 1996

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

International Organization for Standardization
Case Postale 56 • CH-1211 Genève 20 • Switzerland

Printed in Switzerland

Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

Draft International Standards adopted by the technical committees are circulated to the member bodies for voting. Publication as an International Standard requires approval by at least 75 % of the member bodies casting a vote.

International Standard ISO 10483-2 was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 3, *Electrical and electronic equipment*.

ISO 10483 consists of the following parts, under the general title *Road vehicles — Intelligent power switches*:

- Part 1: *High-side intelligent power switch*
- Part 2: *Low-side intelligent power switch*

This page intentionally left blank

STANDARDSISO.COM : Click to view the full PDF of ISO 10483-2:1996

Road vehicles — Intelligent power switches —

Part 2:

Low-side intelligent power switch

1 Scope

This part of ISO 10483 specifies the minimum requirements for 12 V and 24 V body system low-side intelligent power switches (LSIPS). These switches are intended primarily for automotive applications (for example, lamps, motors, relays, etc.).

The numerical values in parentheses refer to 24 V nominal vehicle supply voltage systems.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this part of ISO 10483. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this part of ISO 10483 are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO 7637-1:1990, *Road vehicles — Electrical disturbance by conduction and coupling — Part 1: Passenger cars and light commercial vehicles with nominal 12 V supply voltage — Electrical transient conduction along supply lines only.*

ISO 7637-2:1990, *Road vehicles — Electrical disturbance by conduction and coupling — Part 2: Commercial vehicles with nominal 24 V supply voltage — Electrical transient conduction along supply lines only.*

ISO 10483-1:1993, *Road vehicles — Intelligent power switches — Part 1: High-side intelligent power switch.*

3 Definitions

For the purposes of this part of ISO 10483, the following definitions apply.

3.1 intelligent power switch (IPS): Single solid-state on/off switch with

- self-protection;
- functional status information;
- positive logic level input.

3.2 low-side intelligent power switch (LSIPS): Single solid-state on/off switch where the switching part of the IPS is between ground and the load, and with

- self protection and automatic recovery;
- functional status information;
- positive logic level input.

3.2.1 battery-connected LSIPS (LSIPS-B): LSIPS where the control supply pin is connected to the load supply.

3.2.2 regulated control supply LSIPS (LSIPS-R): LSIPS where the control supply pin is connected to a separate control supply.

3.3 control supply voltage, V_{cs} : Voltage which supplies the control part of the LSIPS.

3.4 nominal current, I_{nom} : Current which produces a voltage drop of 0,5 V (0,5 V) across the load pin and the ground pin, at 85 °C case temperature and at a load supply voltage of 13 V (26 V).

NOTE 1 The nominal current is defined only for a consistent comparison between devices from different sources. In use the voltage drop will depend on the application.

3.5 maximum continuous current, I_{max} : Maximum current which does not activate self-protection at 85 °C case temperature, a load supply voltage of 13 V (26 V) and at the nominal voltage of the control supply.

3.6 maximum control current, I_{CM} : Maximum control current over the full range of temperature and voltage, and at maximum continuous current, I_{max} .

3.7 overcurrent, I_{ov} : Minimum value of load current which causes the LSIPS to change from its normal function to a current-limited mode of operation.

3.8 on resistance, R_{on} : Resistance of the device at nominal current conditions.

3.9 maximum continuous voltage, V_{14C} : Maximum continuous supply voltage at the load pin which does not destroy the switch over the total range of temperature in free air conditions [ISO 10483-1:1993, definition 3.3] with the input pin grounded, and over the total range of control supply voltage.

3.10 control breakdown voltage, V_{CBR} : Maximum continuous control supply voltage which does not destroy the switch over the total range of temperature in free air conditions and in an input and load condition.

3.11 supply quiescent current, I_{sq} : Total supply current (to the ground pin) when the load is short-circuited, the status output is an open circuit and the input is grounded.

3.12 open load condition: Condition when the load current is less than the threshold current, I_{ol} , which is between 10 % of the nominal current and 5 mA.

3.13 overload condition: Condition when the switch is in a self-protected state.

3.14 thermal protection: Ability of the LSIPS to protect itself against over-temperature by switching off the load current.

3.15 inductive load at nominal current, L_{nom} : Maximum inductance in series with a nominal resistance specified in 6.1.2 which can be driven without a freewheel diode.

3.16 inductive load at maximum current, L_{max} : Maximum inductance in series with the minimum resistance specified in 6.1.2 which can be driven without a freewheel diode.

3.17 propagation delay time for the open load, t_{pol} : Time between the falling edge of the input signal and rising edge of the status signal in the case of a permanent open load.

3.18 propagation delay time for overload, t_{povl} : Time between the falling edge of the input signal and rising edge of the status signal in the case of an overload.

3.19 nominal load pin clamping voltage, V_{ncv} : Voltage measured at the load pin after switching off its nominal current, I_{nom} , in an inductive load, defined in 3.15.

3.20 load pin clamping threshold voltage, V_{thcv} : Load pin voltage at which the LSIPS sinks 1 % of the nominal current or 5 mA, whichever is greater.

4 Functioning

4.1 Overview

The LSIPS has two main functions:

- a) the switching function;
- b) the overcurrent protection of the switch and an indication with a single status bit information of the state of the load and of the switch.

The switch may internally clamp over voltages resulting from switching of an inductive load. Clamp capabilities shall be specified by semiconductor manufacturers.

A LSIPS is a five-pin component as shown in figure 1 a) and 1 b).

4.1.1 Battery connected control supply LSIPS-B

See figure 1 a).

4.1.2 Regulated control supply LSIPS-R

See figure 1 b).

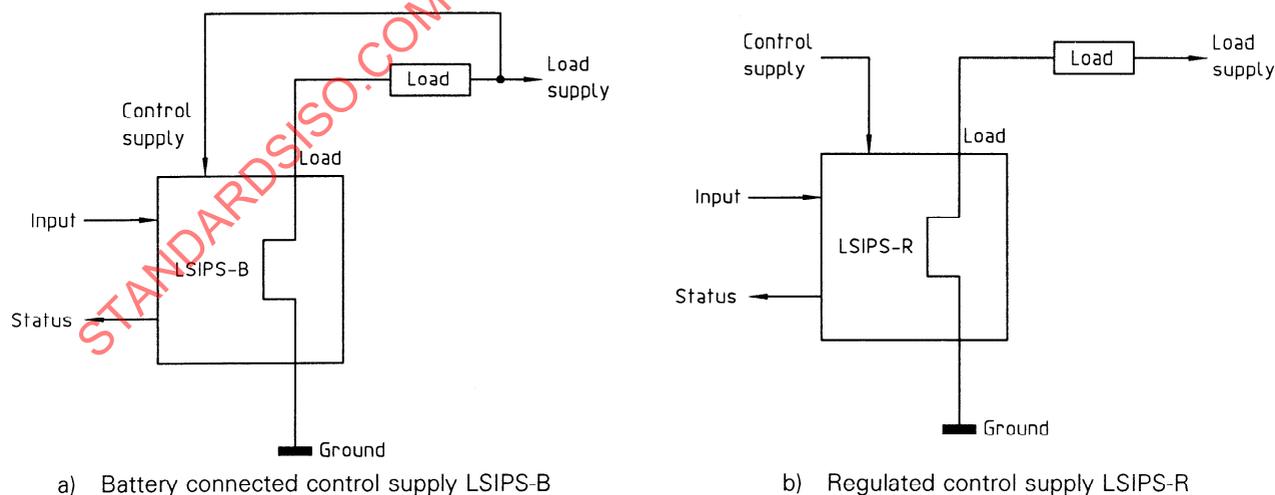


Figure 1 — Control supply

4.2 Input functionality

A logic level "0" on the input ensures that the switch is in the off state, except during clamping, and a logic level "1" on the input ensures that the switch is in the on state, except in overload conditions. When the input is not connected, the switch shall be in the off state.

4.3 Status functionality

4.3.1 General requirements

When the input is at the logic level "1", the status bit indicates with a logic level "0":

- open circuit of the load;
- overload.

Otherwise the status bit is at logic level "1".

A logic level "1" of the status output corresponds to a high impedance between status output and ground, and a logic level "0" of the status output corresponds to a low impedance between status output and ground.

4.3.2 Status strategy

4.3.2.1 Open load condition

The open load condition is indicated by a logic "0" on the status pin if the open load condition is present for a time exceeding t_1 ($1 \text{ ms} < t_1 < 10 \text{ ms}$). (See 4.3.3.)

The status signal will return to logic "1" if the open load condition disappears for a time exceeding t_1 .

4.3.2.2 Overload condition

An overload condition is indicated by a logic "0" on the status pin as soon as the LSIPS is in a self-protected state.

4.3.2.3 Discrimination between overload and open load

4.3.2.3.1 With external components

With external components it is possible to use the output of the status pin in conjunction with other information to differentiate between open load and overload.

In this case t_{pol} and t_{povl} are of the same order of magnitude.

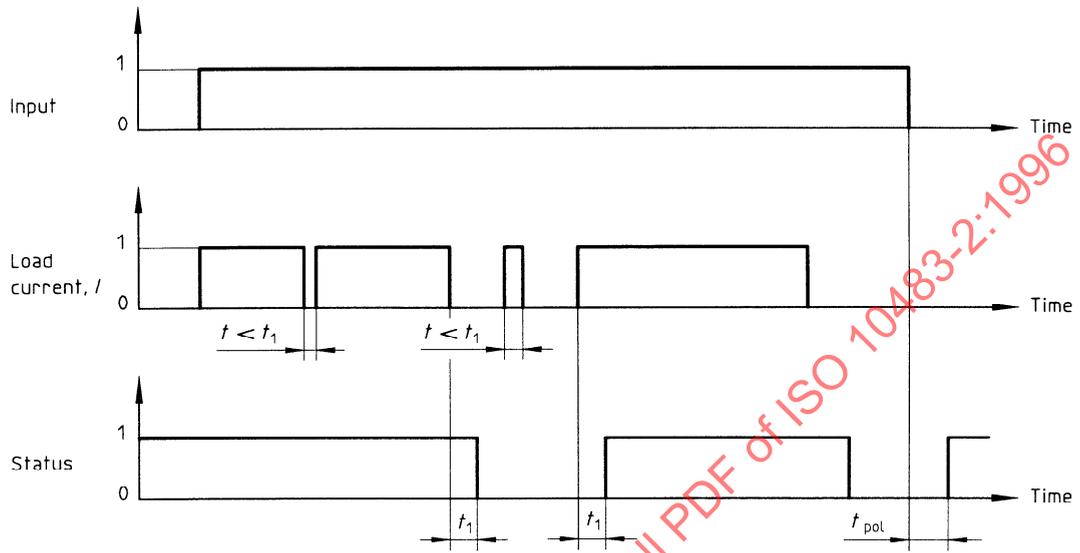
4.3.2.3.2 Internally

If a feature is implemented within the device in order to distinguish between overload and open load, it should be by means of an increase of t_{pol} .

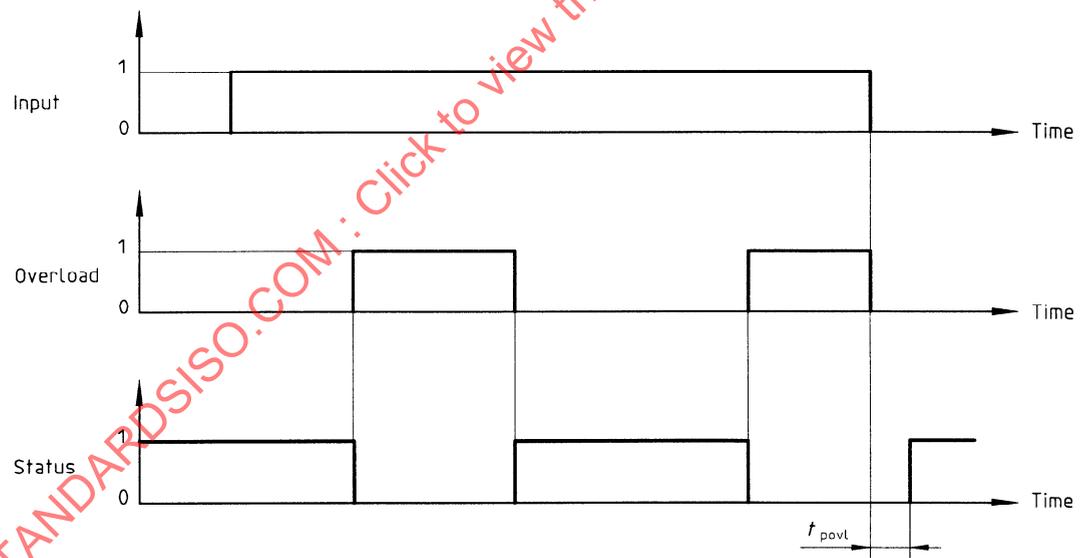
In this case t_{pol} shall exceed t_{povl} .

4.3.3 Description of status information

See figure 2.



a) Open load



b) Overload

Figure 2 — Status information

4.4 Overcurrent

The overcurrent is the current level where a protection of the LSIPS by current limitation is activated in the switch.

The current depends on the load and for that reason the graph in figure 3 defines this value as a function of the type of load, where the overcurrent is in the unshaded part of the curve.

EXAMPLES

- For a lamp requiring a 6 A LSIPS, the minimum current limitation shall exceed 30 A for response time problem ($k = 5$).
- For a d.c. motor requiring a 20 A LSIPS, the minimum current limitation shall exceed 40 A to ensure surge response ($k = 2$).

An implication of the concept of overcurrent is that, when the device is switching the load models defined in 5.3, the output will not operate in a chopping mode, and the status pin will not indicate an overload.

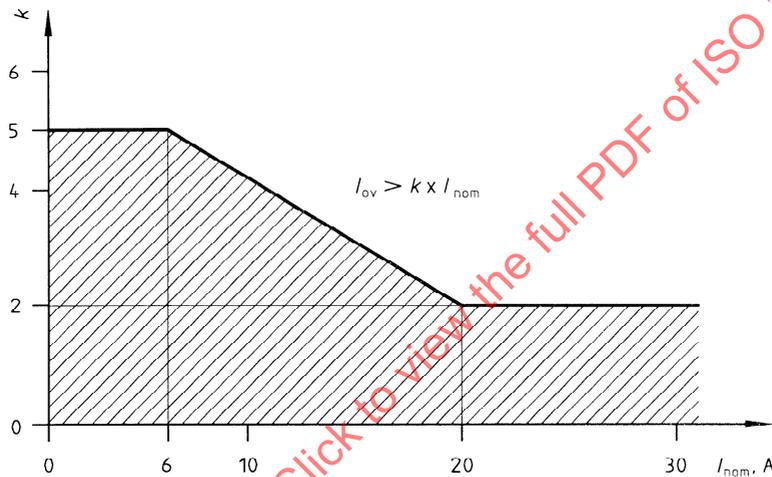


Figure 3 — Overcurrent

4.5 Failure mode

In the case of disconnection of the load supply pin, or the input pin, the device shall turn off.

In the case of disconnection of the ground pin, the semiconductor manufacturer shall specify the behaviour of the LSIPS.

5 Electrical specifications

5.1 Supply voltage range

5.1.1 For LSIPS-B

See table 1.

Table 1 — Supply voltage range for LSIPS-B

Voltage range V	Justification	Comments
≥ 50(75)	Spurious spikes (see ISO 7637-1 and ISO 7637-2)	The LSIPS should be capable of being protected by external devices
30 to 50 (40 to 75)	Spurious spikes	
30 to 40 (40 to 60)	Clamped load dump	Protection of the switch takes priority over functionality
22 to 30	Spurious spikes	Operation ensured in a degraded mode (on resistance)
16 to 22 (32 to 40)	Jump start or regulator degraded	Operation to nominal design specification
10,5 to 16 (20 to 32)	Normal operation condition	Operation to nominal design specification
8 to 10,5 (12 to 20)	Alternator degraded	Operation ensured in a degraded mode (on resistance)
6 to 8 (6 to 12)	Starting phase gasoline engine	Operation ensured in a degraded mode (on resistance)
0 to 6 (0 to 6)	Starting phase diesel engine	Capability to be switched off and to stay in off state when the input goes low
Negative	Negative peaks (see ISO 7637-1 and ISO 7637-2) or inverted battery	The LSIPS should be capable of being protected by external devices

5.1.2 For LSIPS-R**5.1.2.1 Load supply voltage range**

See table 2.

Table 2 — Load supply voltage range for LSIPS-R

Voltage range V	Justification	Comments
≥ 50(75)	Spurious spikes (see ISO 7637-1 and ISO 7637-2)	The LSIPS should be capable of being protected by external means
30 to 50 (40 to 75)	Spurious spikes	Protection of the switch takes priority over functionality
30 to 40 (40 to 60)	Clamped load dump	
22 to 30	Spurious spikes	R_{on} varies with control voltage
16 to 22 (32 to 40)	Jump start or regulator degraded	
10,5 to 16 (20 to 32)	Normal operation condition	
8 to 10,5 (12 to 20)	Alternator degraded	
6 to 8 (6 to 12)	Starting phase gasoline engine	R_{on} varies with control voltage. Capability to be switched off and to stay in off state when the input goes low
0 to 6 (0 to 6)	Starting phase diesel engine	
Negative	Negative peaks (see ISO 7637-1 and ISO 7637-2) or inverted battery	The LSIPS should be capable of being protected by external devices

5.1.2.2 Control supply voltage range

See table 3.

Table 3 — Control supply voltage range for LSIPS-R

	Control voltage range	Condition
Regulated control supply	4,5 V to 16 V	Operation to nominal specification
	0 to 4,5 V	Capability to be switched off and to stay in off state when the input goes low. $I_{sq} \leq 50 \mu\text{A}$

5.1.3 Nominal load pin clamping voltage

The clamping voltage of the load pin shall exceed 40 V for 12 V applications and exceed 60 V for 24 V applications.

5.1.4 Load pin clamping threshold voltage

The load pin clamping threshold shall exceed 22 V (40 V).

5.2 Case temperature

The LSIPS shall be fully functional in the temperature range of

$$-40 \text{ }^{\circ}\text{C} \leq t_{\text{case}} \leq 125 \text{ }^{\circ}\text{C}$$

but some parameters may vary, as for instance the switching current or the on resistance.

5.3 Input characteristics

The temperature range shall be as in 5.2.

5.3.1 Triggering levels

The triggering levels shall be as in table 4.

Table 4 — Triggering levels

Values in volts

Triggering level	Voltage	
	min.	max.
V_{t-}	0,8	—
V_{t+}	—	2
Hysteresis (V_{t+}) - (V_{t-})	0,5	—

5.3.2 Pull-down input impedance

The pull-down input impedance shall be between 10 k Ω and 50 k Ω .

5.4 Status output characteristics

The status output type shall be an open drain or an open collector, and shall show the following characteristics with the temperature range as specified in 5.2:

- a) maximum output voltage of 0,4 V at logic level "0" and a sink current of 1,5 mA;
- b) minimum clamp voltage of 5,5 V at a status leakage current below 0,1 mA.

5.5 Supply quiescent current, I_{sq}

The supply quiescent current shall be below 50 μ A at 13 V (26 V) load supply voltage and nominal control supply voltage, and shall be measured at a case temperature of (23 ± 5) °C.

5.6 Switching characteristics

The switching characteristics at normal and short-circuit operation shall be as given in table 5, when measured as specified in 6.4.

Table 5 — Switching characteristics

Switching mode	dI/dt in LSIPS	
	Normal operation	Short-circuit operation
	A/ μ s	A/ μ s
Switching on	< 0,5	< 1
Switching off	< 3	< 3

5.7 Variation of R_{on} versus voltages

5.7.1 Variation of R_{on} for LSIPS connected to the battery (control pin)

The variation of the on resistance shall meet the specification of figure 4 referring to measurements at nominal current with a resistive load, and at a case temperature of 85 °C.

5.7.2 Variation of R_{on} versus control supply voltage for LSIPS-R

R_{on} shall not exceed the value specified in 3.7 at control supply voltage between 4,5 V and 16 V.

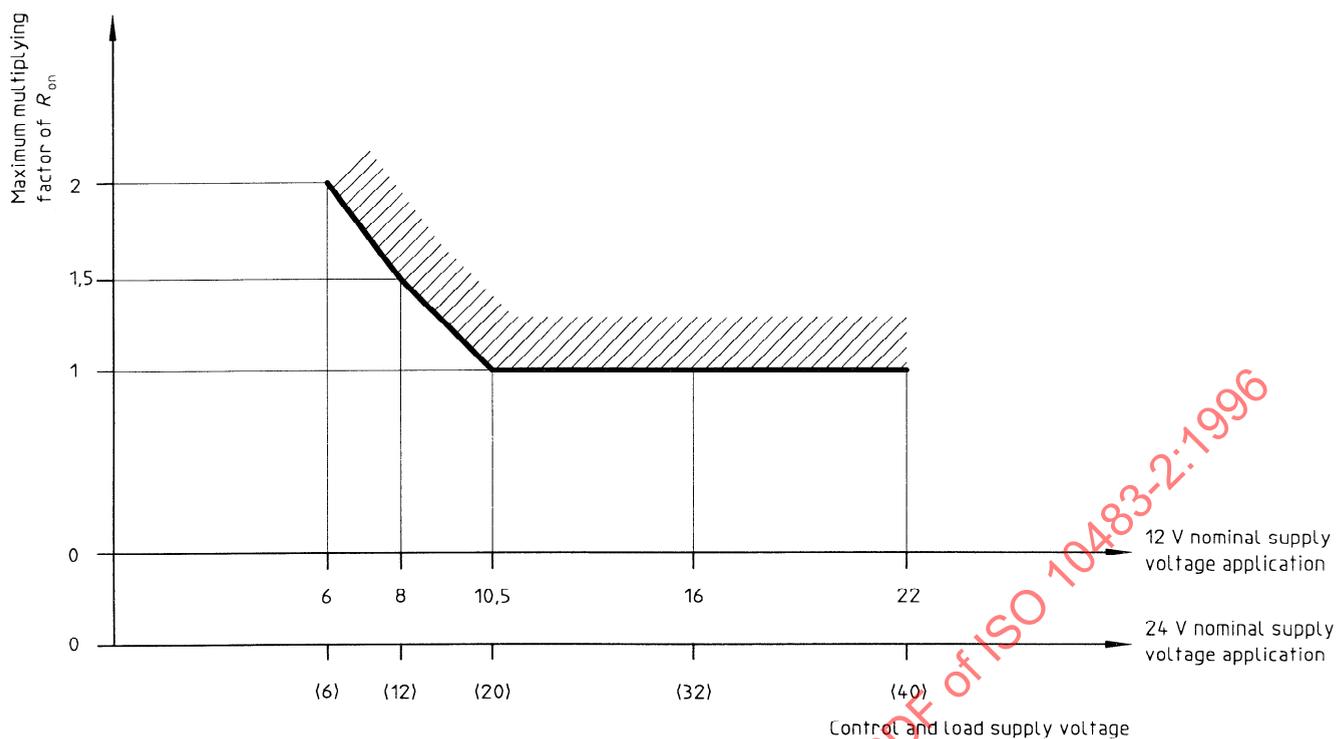


Figure 4 — Variation of R_{on} for LSIPS connected to battery

5.8 Packaging (five pins)

5.8.1 Package 1

If TO 220 or TO 218 packages are used, the pin allocation shall be as in table 6.

5.8.2 Package 2

If TO 220 or TO 218 ground case packages are used, the pin allocation shall be as in table 6.

Table 6 — Packaging

Pin number	Pin allocation of	
	Package 1	Package 2
1	Input	
2	Status	
3	Load	Ground
4	Control supply	
5	Ground	Load

6 Test methods

6.1 Load models

The purpose of these load models is to test switching behaviour (dI/dt , thermal behaviour, etc.). The values specified refer to an ambient temperature of $(23 \pm 5) ^\circ\text{C}$.

6.1.1 Bulb model

See figure 5 and table 7.

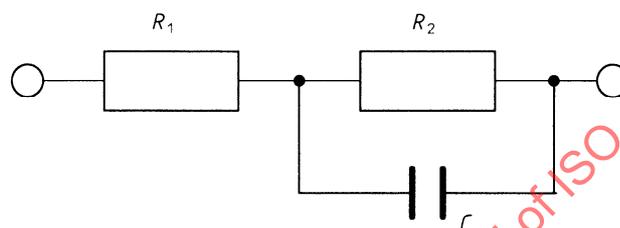


Figure 5 — Bulb model

Table 7 — Bulb model characteristics

Bulb power W	Resistance		Capacitance
	R_1 Ω	R_2 Ω	C $\mu\text{F}^1)$
55/65 (70/75)	0,17 (0,6)	2,3 (9)	33 000 (5 200)
21	0,6 (1,9)	6,2 (27)	3 200 (1 000)
5	2,4 (10)	27 (110)	400 (250)

1) The equivalent series resistance of the capacitor shall be less than 10 m Ω .

6.1.2 Inductive load model

See figure 6 and table 8.

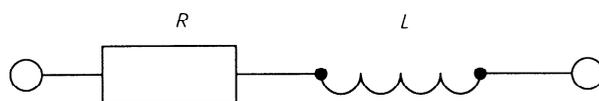


Figure 6 — Inductive load model

Table 8 — Inductive load model

Test	R ¹⁾ Ω	L
at I_{nom}	$13 \text{ V}/I_{\text{nom}}$ ($26 \text{ V}/I_{\text{nom}}$)	To be specified by the semiconductor manufacturer
at I_{max}	$13 \text{ V}/I_{\text{max}}$ ($26 \text{ V}/I_{\text{max}}$)	
1) I_{nom} and I_{max} are expressed in amperes.		

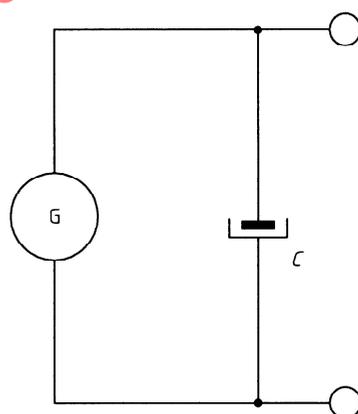
6.1.3 Short-circuit model

The short-circuit model shall consist of a resistor smaller than 10 m Ω .

6.2 Supply characteristics

6.2.1 Load supply characteristics

The load supply characteristics shall be as given in figure 7.



$C = 100\,000 \mu\text{F}$ with an equivalent series resistance $< 10 \text{ m}\Omega$

G is the power supply generator with a current of min. 50 A, and an internal impedance of

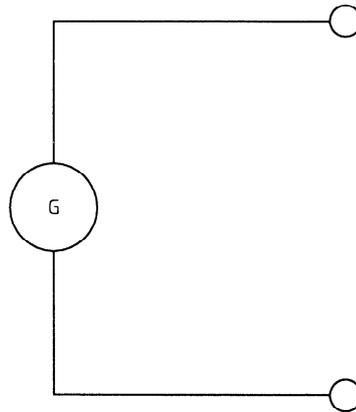
$< 1 \text{ m}\Omega$ for $f < 100 \text{ Hz}$;

$< 10 \text{ m}\Omega$ for $100 \text{ Hz} < f < 1 \text{ kHz}$.

Figure 7 — Load supply characteristics

6.2.2 Control supply characteristics

The control supply characteristics shall be as given in figure 8.



G is the power supply generator with a current of min. 1 A, and an internal impedance of
5 m Ω for $f = 100$ Hz;
50 m Ω for $f = 1$ kHz.

Figure 8 — Control supply characteristics

6.3 Short-circuit test

After the short-circuit test, LSIPS tested shall remain within its specifications.

6.3.1 Test circuits

The circuit for LSIPS-B shall be as in figure 9 a) and for LSIPS-R as in figure 9 b).

STANDARDSISO.COM · Click to view the full PDF of ISO 10483-2:1996

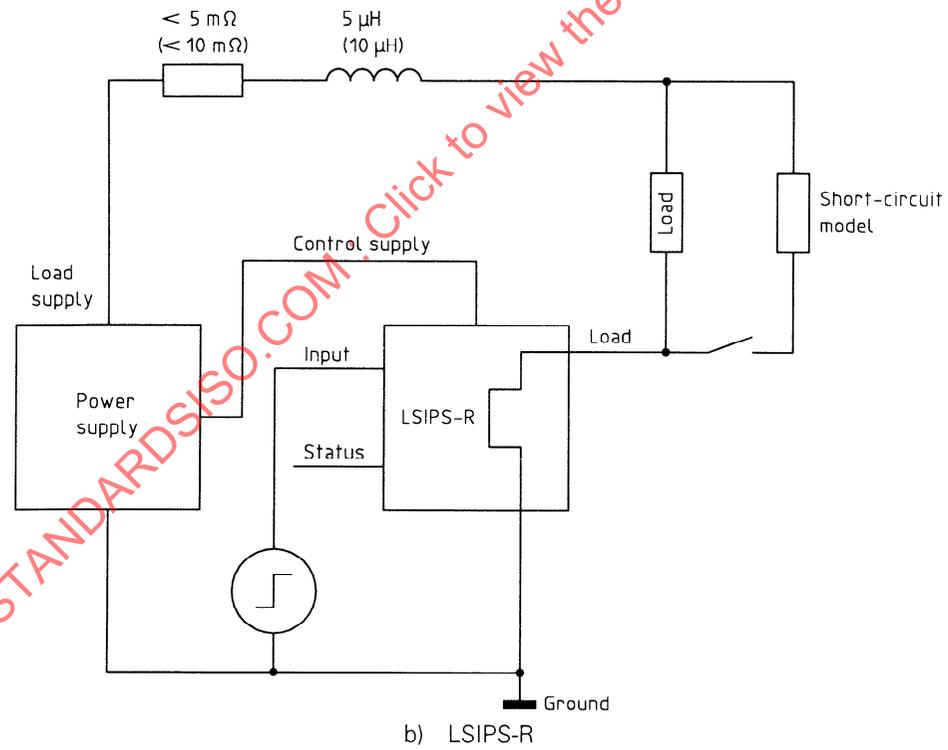
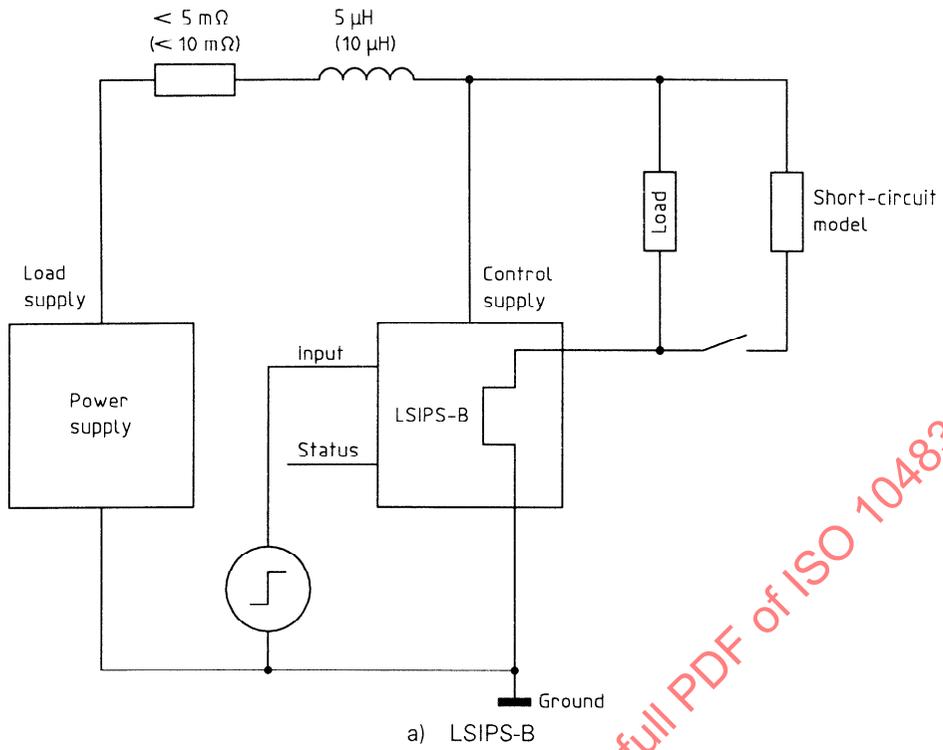


Figure 9 — Short-circuit test

6.3.2 Test conditions

The test conditions shall be as follows:

- load supply voltage: 13 V (26 V);
- load supply: as in 6.2;
- minimum test duration: 1 min;
- temperature: ambient temperature of (23 ± 5) °C at free air condition;
- control supply voltage: 5 V for LSIPS-R and 13 V (26 V) for LSIPS-B.

The short-circuit can occur before or after switching on.

6.4 Switching test

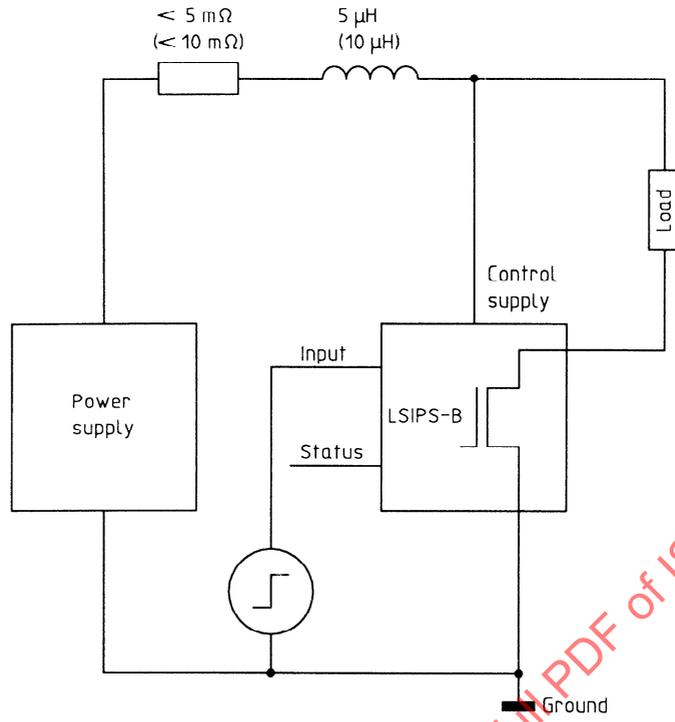
The device tested shall remain within its specification after the following tests.

The highest value of dI/dt measured shall be taken into consideration at the switching test during normal operation, see 6.4.2.

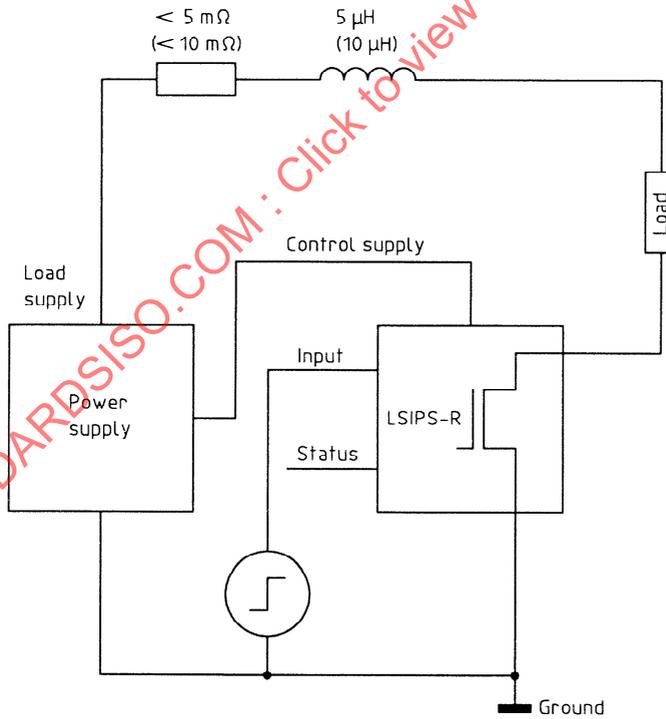
6.4.1 Switching test circuits

The circuit for LSIPS-B shall be as in figure 10 a) and for LSIPS-R as in figure 10 b).

STANDARDSISO.COM : Click to view the full PDF of ISO 10483-2:1996



a) LSIPS-B



b) LSIPS-R

Figure 10 — Switching test circuit

6.4.2 Switching test conditions during normal operation

The switching test conditions during normal operation shall be as follows:

- load supply: 13 V (26 V);
- load supply conditions: as in 6.2;
- load model: bulb model or resistance $R = 13V/I_{nom}$ (26 V/ I_{nom});
- temperature: ambient temperature of (23 ± 5) °C at free air condition.

6.4.3 Switching test conditions during a short-circuit

The switching test conditions during a short-circuit shall be as follows:

- load supply: 13 V (26 V);
- load supply conditions: as in 6.2;
- load model: short-circuit model as in 6.1.3;
- temperature: ambient temperature of (23 ± 5) °C at free air condition.

6.4.4 Switching test conditions with inductive load

The switching test conditions with inductive load shall be as follows:

- load supply: 13 V (26 V);
- load supply conditions: as in 6.2;
- load model: inductive load model as in 6.1.2;
- temperature: $t_{case} = 85$ °C.

6.4.4.1 Test at nominal current

- Frequency: 1 Hz;
- "On" time t_{on} : $(L/R \times 5) \pm 10$ %;
- duration: 1 min

6.4.4.2 Test at maximum current

- Frequency: 1 Hz;
- "On" time t_{on} : $(L/R \times 5) \pm 10$ %;
- duration: 1 min

6.5 Determination of the maximum continuous current

The determination of the maximum continuous current shall be carried out at the following measuring conditions:

- load supply voltage: 13 V (26 V);
- load supply conditions: as in 6.2;

- control supply characteristic: 5 V for LSIPS-R and 13 V (26 V) for LSIPS-B;
- heat sink temperature: adjusted to maintain $t_{\text{case}} = 85 \text{ }^{\circ}\text{C}$.

To maintain equilibrium the current is slowly increased to the point where the thermal protection operates. The procedure is then repeated at a point just below the protection threshold, and the current and voltage drop are measured.

The current measured is the maximum continuous current.

6.6 Determination of the nominal current

The determination of the nominal current shall be carried out at the following measuring conditions:

- load supply voltage: 13 V (26 V);
- load supply conditions: as in 6.2;
- heat sink temperature: adjusted to maintain $t_{\text{case}} = 85 \text{ }^{\circ}\text{C}$.

The current shall be adjusted to cause a voltage drop of 0,5 V measured across the switch.

The then measured current is the nominal current.

6.7 Measurement of the status propagation delay time

The measurement shall be carried out as shown in figure 11, and at the following measuring conditions:

- load supply voltage: 13 V (26 V);
- load supply conditions: as in 6.2;
- test circuits: as in 6.7.1 and 6.7.2.

STANDARDSISO.COM : Click to view the full PDF of ISO 10483-2:1996

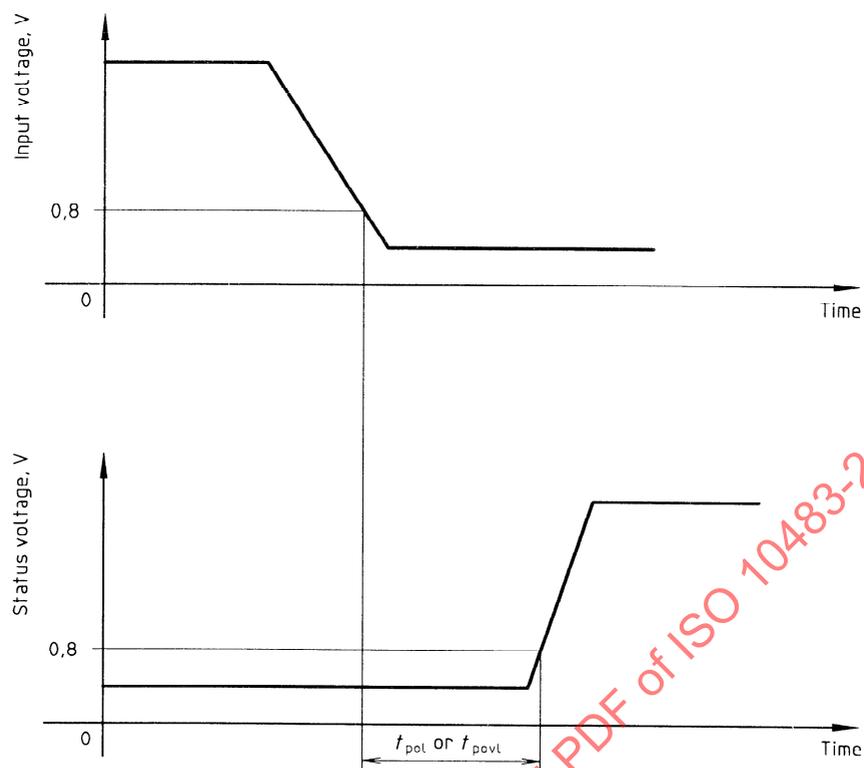
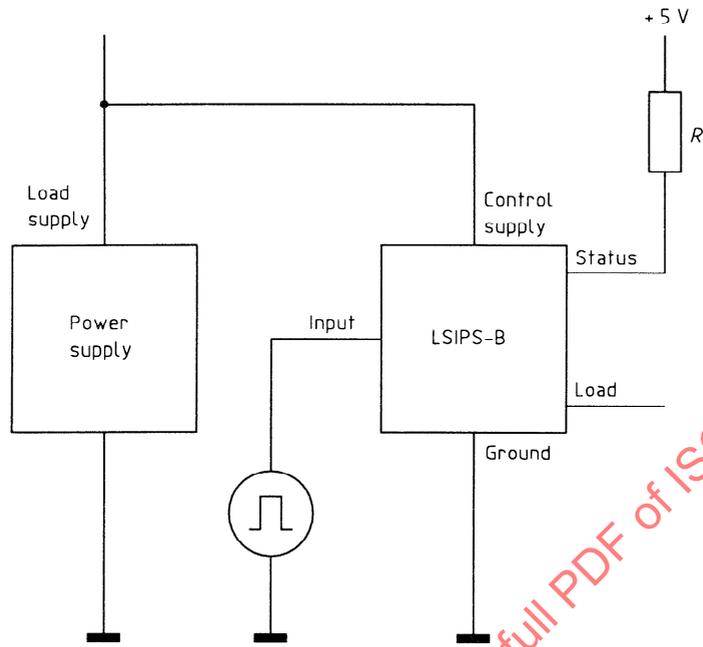


Figure 11 — Propagation delay time measurement

STANDARDSISO.COM : Click to view the full PDF of ISO 10483-2:1996

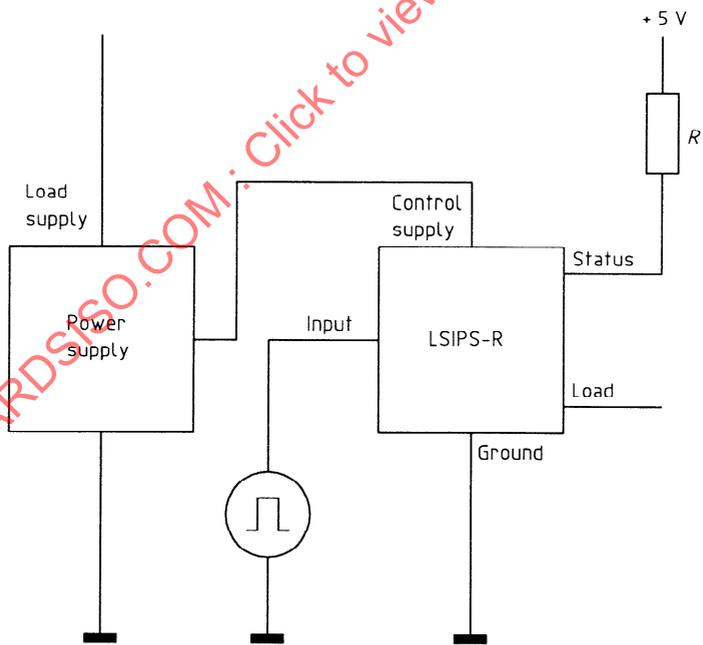
6.7.1 Status test circuit for open load

The test circuit shall be as in figure 12 a) or 12 b) as appropriate.



$R = 3\ 125\ \Omega$

a) LSIPS-B



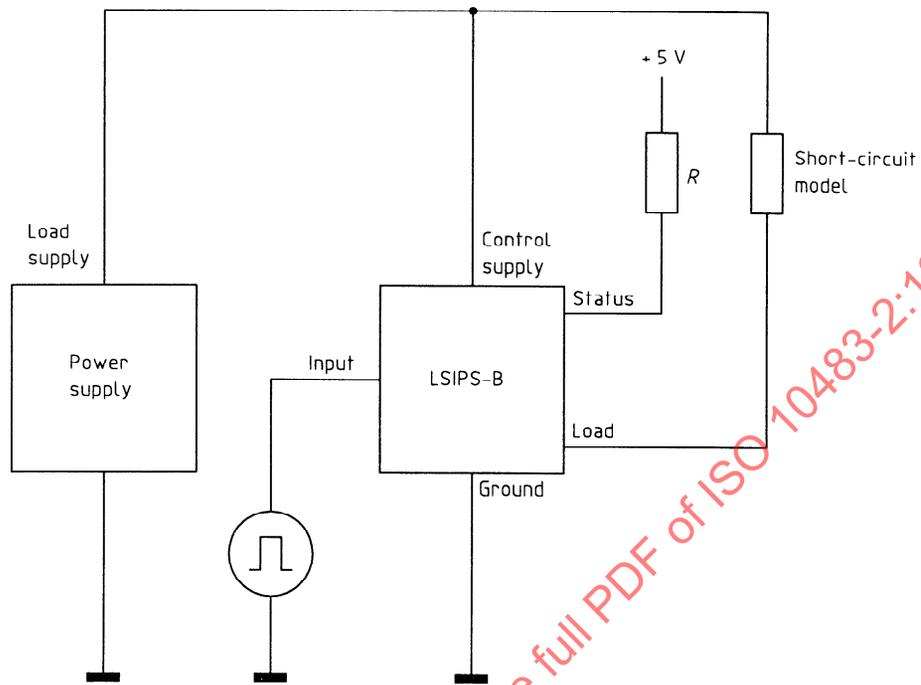
$R = 3\ 125\ \Omega$

b) LSIPS-R

Figure 12 — Status test circuit

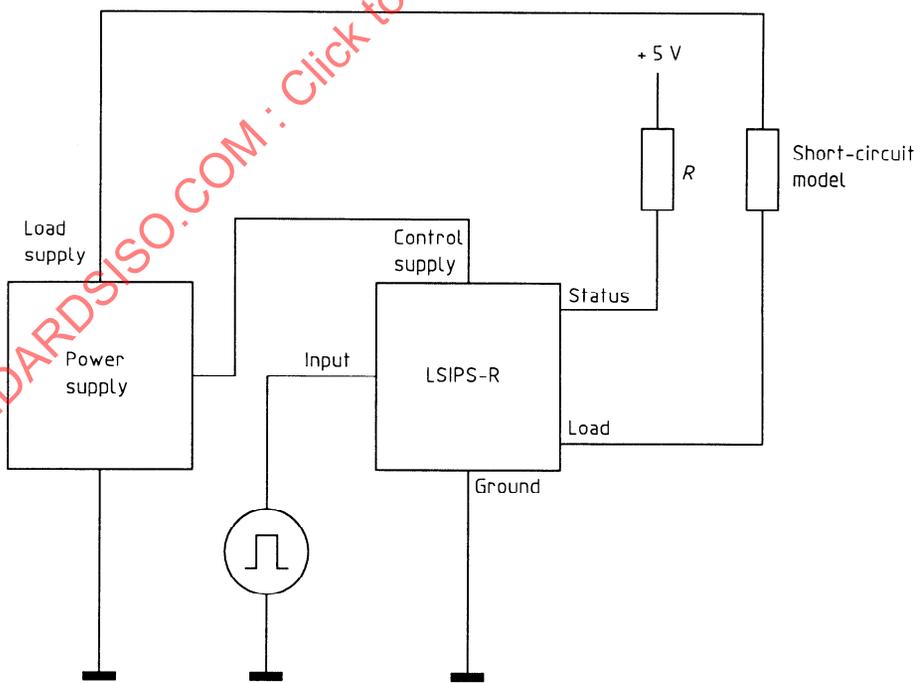
6.7.2 Status test circuit for overload

The test circuit shall be as in figure 13 a) or 13 b) as appropriate.



$R = 3\ 125\ \Omega$

a) LSIPS-B



$R = 3\ 125\ \Omega$

b) LSIPS-R

Figure 13 — Status test circuit