TECHNICAL REPORT

# ISO/IEC TR 10091

First edition
1995-02-01



# Information technology — Technical aspects of 130 mm optical disk cartridge write-once recording format

*Technologies de l'information — Aspects techniques relatifs au format d'enregistrement pour les cartouches de disque optique de diamètre* 130 mm, *non réinscriptible*

Reference number
ISO/IEC TR 10091:1995(E)

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# Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

The main task of technical committees is to prepare International Standards, but in exceptional circumstances a technical committee may propose the publication of a Technical Report of one of the following types:

— type 1, when the required support cannot be obtained for the publication of an International Standard, despite repeated efforts;

— type 2, when the subject is still under technical development or where for any other reason there is the future but not immediate possibility of an agreement on an International Standard;

— type 3, when a technical committee has collected data of a different kind from that which is normally published as an International Standard ("state of the art", for example).

Technical Reports of types 1 and 2 are subject to review within three years of publication, to decide whether they can be transformed into International Standards. Technical Reports of type 3 do not necessarily have to be reviewed until the data they provide are considered to be no longer valid or useful.

ISO/IEC TR 10091, which is a Technical Report of type 3, was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology,* Subcommittee SC 23, *Optical disk cartridges for information interchange*.

# Information technology — Technical aspects of 130 mm optical disk cartridge write-once recording format

## Section 1 - General

### 1 Scope

This Technical Report is a complement to ISO/IEC 9171-2 for the Type A and B formats.

This Technical Report covers the figures that characterize each format, the relationship between these figures, and the technological background used to reach decisions concerning the formats; in addition it gives some examples of implementation.

### 2 References

ISO/IEC 9171-1:1990, *Information technology -130mm optical disk cartridge, write once, for information interchange - Part 1: Unrecorded optical disk cartridge*

ISO/IEC 9171-2:1990, *Information technology -130mm optical disk cartridge, write once, for information interchange - Part 2: Recording format*

### 3 Recording area and control track

The recording area and control tracks are divided as given in table 1. The dimensions are for reference only, they are nominal positions (see ISO/IEC 9171-2 clause 4).

**Table 1 - Formatted Zone**

| | |
|---|---|
| -Reflective Zone | 27,00 mm to 29,00 mm |
| -Control Track PEP Zone | 29,00 mm to 29,50 mm |
| -Transition Zone for SFP | 29,50 mm to 29,52 mm |
| -Inner Control Track SFP Zone | 29,52 mm to 29,70 mm |
| -Inner Manufacturer Zone | 29,70 mm to 30,00 mm |
| -Guard Band | 29,70 mm to 29,80 mm |
| -Manufacturer Test Zone | 29,80 mm to 29,90 mm |
| -Guard Band | 29,90 mm to 30,00 mm |
| -User Zone | 30,00 mm to 60,00 mm |
| -Outer Manufacture Zone | 60,00 mm to 60,15 mm |
| -Outer Control Track SFP Zone | 60,15 mm to 60,50 mm (maximum) |
| -Lead-Out Zone | 60,50 mm to 61,00 mm |

The inner radius of the Formatted Zone shall be at least 27,0 mm to avoid interference with the Clamping Zone.

The format of the Reflective Zone is not specified but it shall have the same reflective recording layer as the rest of the Recording Zone. Servo information (grooves or pits) is not required in the Reflective Zone.

The width of the PEP Zone is determined by the requirements for the accuracy of the drive head positioning system. The width of 0,5 mm for the PEP Zone is sufficient for stable operation of the drive actuator mechanism. Since grooves are not required in the PEP Zone, the track pitch may be changed to make it easier to read out the PEP without using a tracking servo.

A Transition Zone for SFP is provided to enable the optical head to move from the PEP Zone to the SFP Zone, which requires a period for changing the translation mode of the optical head at the transition point from the PEP Zone to the SFP Zone in the mastering process. The Transition Zone for the SFP Zone can be an unrecorded area.

Considering the accuracy of control of the media mastering equipment, the starting position of the outer SFP is to be determined relative to the starting position of the inner control track and the tolerance built-up over the mastered area.

Within the Manufacturer Test Zone, it is recommended to have the same header format as that of the User Zone.

There shall be no pre-recorded information on tracks between 60,50 mm and 61,00 mm.

## 4 Physical control track format

There are two recording methods for the control track information to be placed into three different areas (PEP Zone, Inner and Outer SFP Zones). The first method shall be used for the PEP (Phase Encoded Part) and the second method for the SFP (Standard Format Part).

The PEP is recorded at the innermost radius and is recorded independently of the format (A or B) chosen for the rest of the disk. This common PEP recording method allows a drive that is set up for either format A or format B to read the PEP information. The PEP is intended to be read without requiring that servo tracking be established by the drive.

The SFP Zones must be recorded in the same format as the rest of the disk (either format A or format B). It contains additional information plus a duplication of the information in the PEP, so there is no requirement that the PEP be read by every drive.

### 4.1 General aspects

The control track areas provide information about the media that may be used to optimize the read and write characteristics of the drive.

The innermost recorded zone, PEP, is recorded using low frequency phase encoded modulation, which can be read independently of the characteristics of the servo method of the drive.

To facilitate drive compatibility with various media types, there is a hierarchy of information supplied, beginning with the cartridge. The cartridge identifier sensor holes supply information to read the PEP. The PEP supplies enough information to read the SFP, and the SFP supplies information to optimize write and read operations on user data. A drive can then be adjusted by using each source of information in turn leading to the ability to read and/or write user data with optimal efficiency.

The number of sectors per track in the SFP area equals the number of sectors per track at track No. 0. The outer SFP area begins at track No. N+96 where N is the track number of the last track of the User Zone, and continues until radius 60,5 mm.

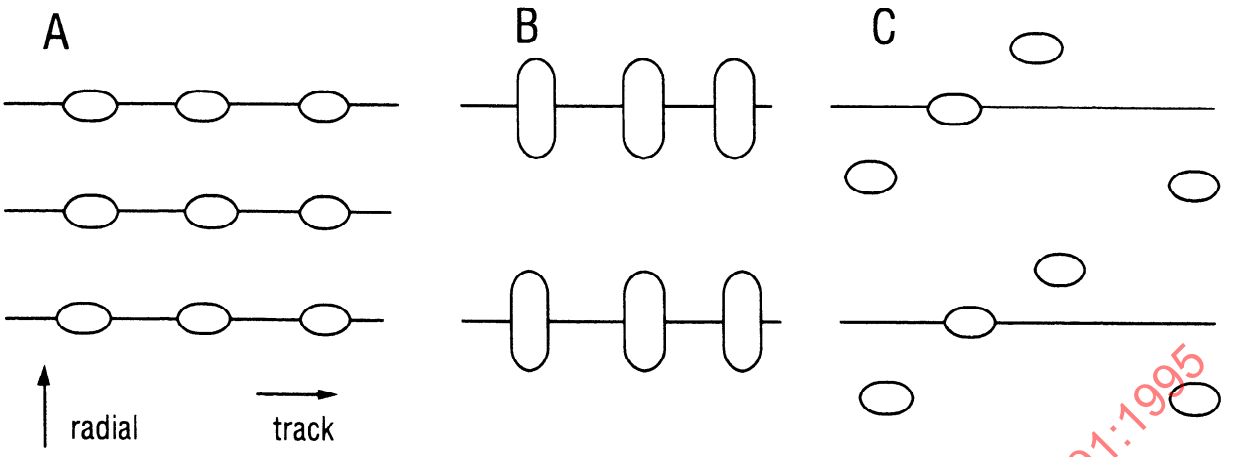
### 4.2 Phase Encoded Part (PEP)

The maximum power applied to the media to read the PEP Zone of the Control Track shall not exceed 0,50 mW.

The low density of the PEP allows a high tolerance for media defects and permits decoding the information with a microprocessor instead of a dedicated circuit. The loss of cross-track signal is limited in the PEP area in order to allow off-track reading. Three methods to reduce the loss of cross-track signal are given in figure 1.

Taking into consideration the various methods, the loss of cross-track signal is defined as the maximum amplitude of the read signal from channel one from three successive marks on the media, divided by the minimum amplitude of the read signal from one revolution of the media (ignoring any effects from defective areas on the media).

This cross track ratio shall not exceed 2,0.




legend:

A : small track pit pattern

B : wide pit pattern

C : wobble pit pattern

**Figure 1 - Example of pit recording in PEP**

The recording sequence throughout the International Standard shall be MSB (most significant bit) first and from byte 0 to byte n.

The PEP Control Track information in bytes 0 to 9 and byte 18 is mandatory for optical disks in order to conform to the International Standard.

The bit assignment of the PEP is summarized in table 2. In order to show correct bit assignment, the following example is given:

In 4/15 modulation bit 2 in byte 0 must be a ONE.

The definition of the lowest value for the amplitude of Pre-formatted data in byte 4 is as follows;

The lowest value in the type A format will be obtained by the recorded data pattern (33). The lowest value in the type B format is obtained by the pattern (C0). All signal levels should be measured at the Inner SFP Zone.

**Table 2 - PEP summary**

PEP Sector Data field summary

| Byte | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Format | 0 | 0 | 0 | 0 | Modulation Code | | |
| 1 | 0 | ECC TYPE | | | 0 | Number of User bytes | | |
| 2 | Number of sectors in track No.0 | | | | | | | |
| 3 | Baseline reflectance at 825nm wavelength | | | | | | | |
| 4 | L or G | Amplitude and polarity of pre-formatted data | | | | | | |
| 5 | Amplitude and polarity of user recorded data | | | | | | | |
| 6 | Max read power for SFP Zone at 825nm and 30Hz rotation | | | | | | | |
| 7 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 8 | Starting track address of Outer SFP Zone, (MSB) | | | | | | | |
| 9 | Starting track address of Outer SFP Zone, (LSB) | | | | | | | |
| 10 | Reserved, (FF) | | | | | | | |
| 11 | Reserved, (FF) | | | | | | | |
| 12 | Reserved, (FF) | | | | | | | |
| 13 | Reserved, (FF) | | | | | | | |
| 14 | NOT SPECIFIED (Ignored in interchange) | | | | | | | |
| 15 | NOT SPECIFIED (Ignored in interchange) | | | | | | | |
| 16 | NOT SPECIFIED (Ignored in interchange) | | | | | | | |
| 17 | NOT SPECIFIED (Ignored in interchange) | | | | | | | |
| 18 | CRC, (Covers bytes 0-17) | | | | | | | |

### 4.3 Standard Formatted Part (SFP)

The type of mark used for the SFP is a phase pit, and the recording format is identical with that of the Users Data area. Only the first 512 bytes in a sector are used for recording the SFP data. If a 1024 byte sector is used, the remaining 512 bytes are recorded as (FF). All unused bytes in the SFP shall be recorded as (FF).

## Section 2 : Type A format

## 5 CCS

The continuous servo tracking format, also called the Continuous Composite Servo, (CCS) tracking format, is explained in this section. The Type A format is based on a CCS tracking method (see ISO/IEC 9171-2 clause 5).

## 6 Track Format

In the push-pull tracking and signal detection scheme, d.c. and low frequency component offsets caused by disk skew and non-concentric tracking must be compensated for, including worst case end-of-life conditions. To resolve these problems, a low frequency tracking offset correction scheme may be used. This correction scheme is not always necessary, but it is required in case of large amounts of tilt, as may happen at the end-of-life of media.

## 7 Sector Format

The Sector Format consists of the following fields:

(1) Sector Mark
(2) VFO1, VFO2, VFO3
(3) Address Mark
(4) ID field
(5) Postamble
(6) Offset detection flag
(7) Gap
(8) Flag
(9) ALPC area
(10) Sync
(11) Data field
(12) Resync
(13) Buffer

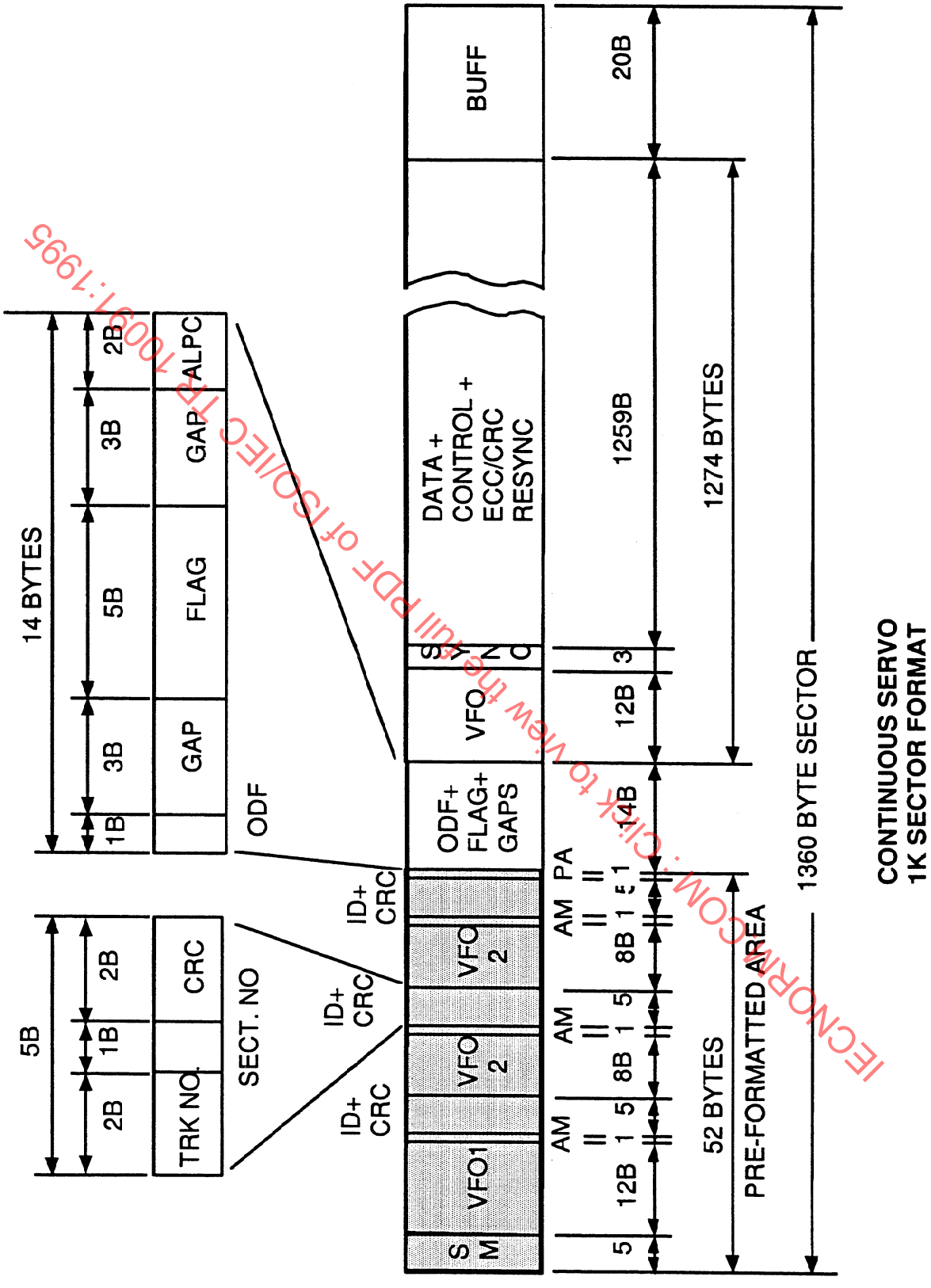
A sector for 1 024 user bytes consists of 52 bytes for the preformatted header area, 14 bytes for flag, gap, ALPC and ODF field, 1274 bytes for the data and other fields and 20 bytes for the buffer.

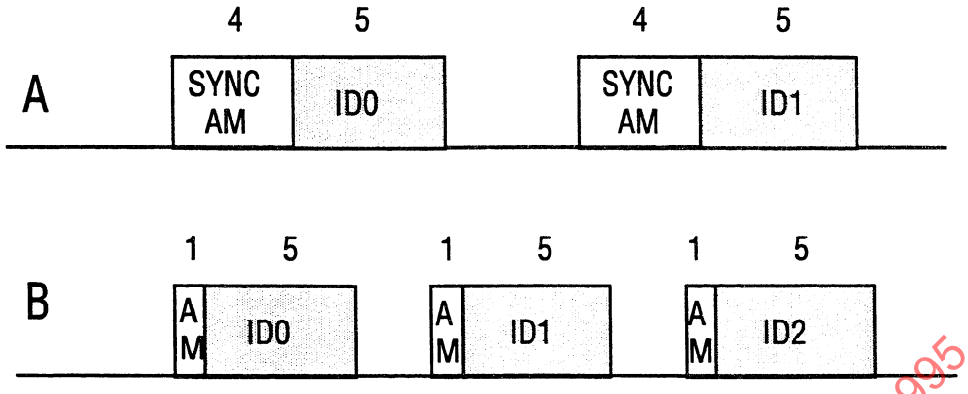
The Resync field is not a discrete field, but instead, a series of special byte patterns inserted into the Data Field to protect the data from loss due to defects and subsequent loss of byte framing by the read channel.

Each ID field has a Variable Frequency Ocilator (VFO) pattern, an Address Mark (AM) pattern and Identifier (ID) information. The sector layout is shown in table 3.

By applying three redundant ID fields, reliable ID detection can be achieved when defects are present. Experimental data used to validate the use of three ID fields is included in the annexes (especially see annex A).

Table 3 - Sector field functions






| | Robustness for timing detection | | | Address robustness | TOTAL |
|---|---|---|---|---|---|
| | random | burst | efficiency | | |
| A | very strong | weaker | good | weak | good |
| B | strong | strong | better | strong | very good |

NOTE

A: 2 ID fields of 4 byte of Sync/AM

B: 3 ID fields of 1 byte of AM

**Figure 2 - Comparison of robustness between two different header formats**

## 7.1 Sector Mark

**Functions**

The purpose of the Sector Mark (SM) is to reliably provide a timing window to begin synchronization of the read channel. It is distinguished from address data or user data by its unique channel bit pattern and can be detected without recourse to a PLL.

**Characteristics of the Pattern**

The pattern does not exist in data and can be detected by a simple timing comparison. The detection of the redundant 3 and 5 channel bit time long pits is reasonably robust to the effects of short burst defects.

**Example of a Detecting Circuit**

Figure 3 shows an example of an SM detecting circuit, and figure 4 shows its action. The signal from the media passes an amplifier and is converted to a pulse width signal by a binarization circuit. A serial-to-parallel conversion circuit along with a time comparison outputs each pulse value at a fixed level. These parallel output signals are compared by majority logic.

As can be seen in figure 4, at most one signal pattern at a time is detected as ONE at time 0. Therefore, identifying the patterns to equal an SM requires more than two ONEs. An SM can be detected even if two output signals are missed. Since the minimum detection criteria is 3 out of 5 pulses, it is highly unlikely that a combination of defects would occur to give a false detection, and it is also unlikely a defect would destroy 3 out of the 5 patterns to cause a missed detection.

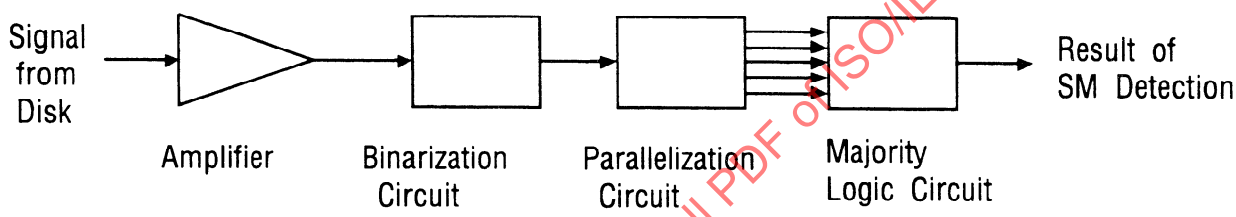



**Figure 3 - SM detecting circuit**

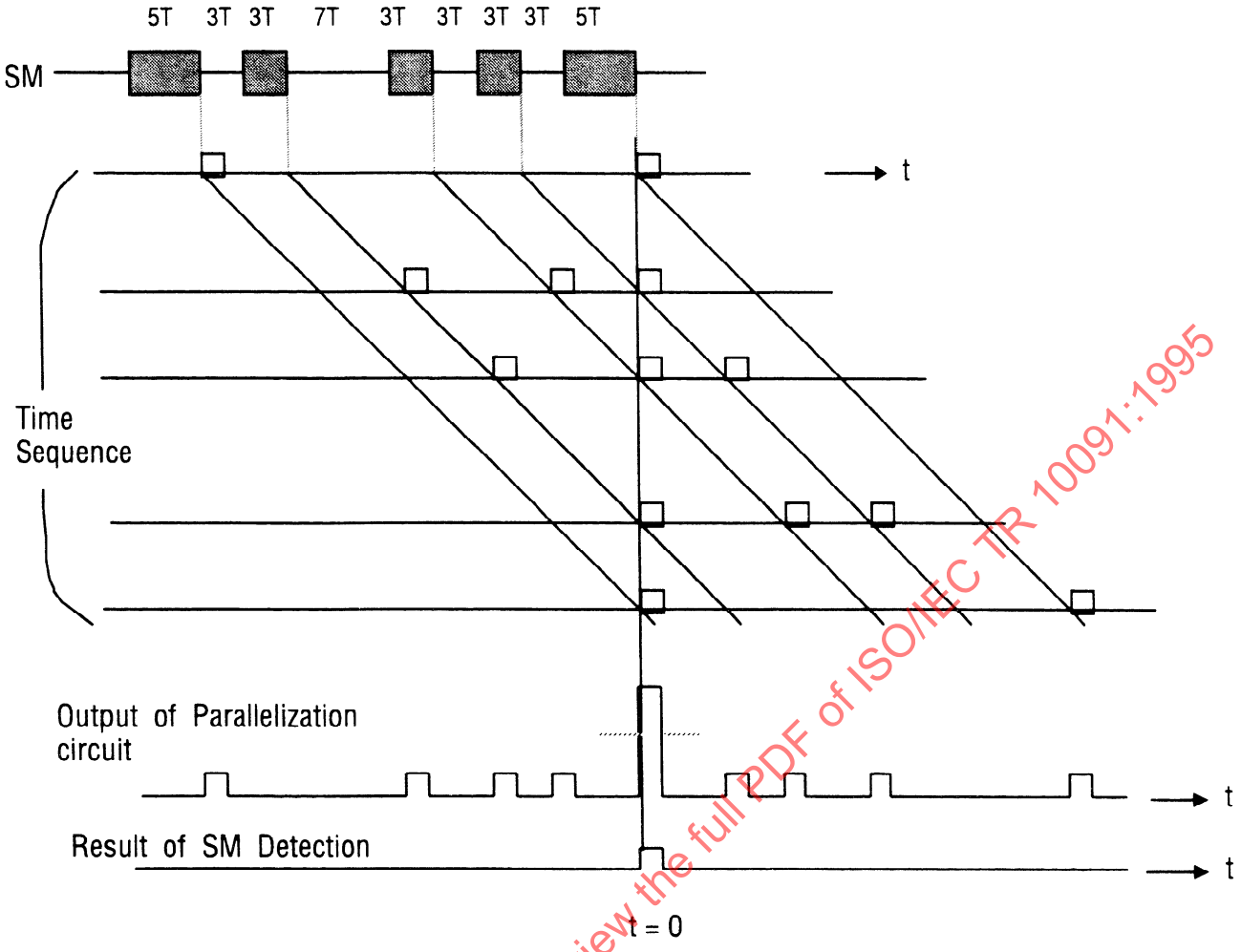



**Figure 4 - SM detecting action**

## 7.2 VFO Areas

**Functions**

VFO fields are not equal in length or pattern (figure 5) for several reasons. VFO1 has the functions to both stabilize the AGC (automatic gain control) and to stabilize the PLL (phase-locked loop) on the clock of the signal from the disk.

VFO2 stabilizes the PLL. As the AGC is assumed to have been stabilized already, the length of VFO2 is shorter than that of VFO1.

VFO3 stabilizes the AGC for the written data field and also stabilizes the PLL. For AGC stabilization it is assumed that a Channel bit stream from 0 to 80 Channel bits in length is necessary depending upon the circuit or method used.

**Characteristics of the pattern**

It is the most dense Channel bit pattern which is suitable to perform the above mentioned functions. The field size when entering the VFO area from a region of unknown or unpredictable signal is 192 Channel bits, while that for the VFO preceding ID1 and ID2 is 136 Channel bits. Since there is no gap proceeding the second and third ID fields, it is assumed that enough information remains in the preceding field to establish the AGC level of the PLL. This leaves 136 Channel bit times for the PLL to establish phase-frequency lock on the data stream.

Two VFO patterns prior to ID1 and ID2 are needed in order to allow the last byte of CRC to achieve closure. The patterns are

"100100100.....010010" and "000100100.....010010".

Notice that the VFO fields always end in the same Channel bit pattern just before the Address Mark. The choice of initial pattern for VFO2 depends on the content of the last byte of CRC in the preceding ID field. The use of these patterns avoids the necessity of having a gap between the end of an ID field and the beginning of the next VFO field.

**Detecting Circuit**

Typical AGC and PLL circuits can be used. No attempt is made here to define such circuits, as ample information already exists. However, it is recommended to add a circuit similar to that in figure 6 to make the PLL more stable. Its purpose is to detect the frequency difference between the master clock and the read clock. When the difference reaches a specified criterion (3% to 4%), it reestablishes the read clock using the master clock, then resumes reading. Thus, if the PLL looses frequency synchronization due to a large burst error, reliable PLL operation can still be expected again after the defective area has passed.

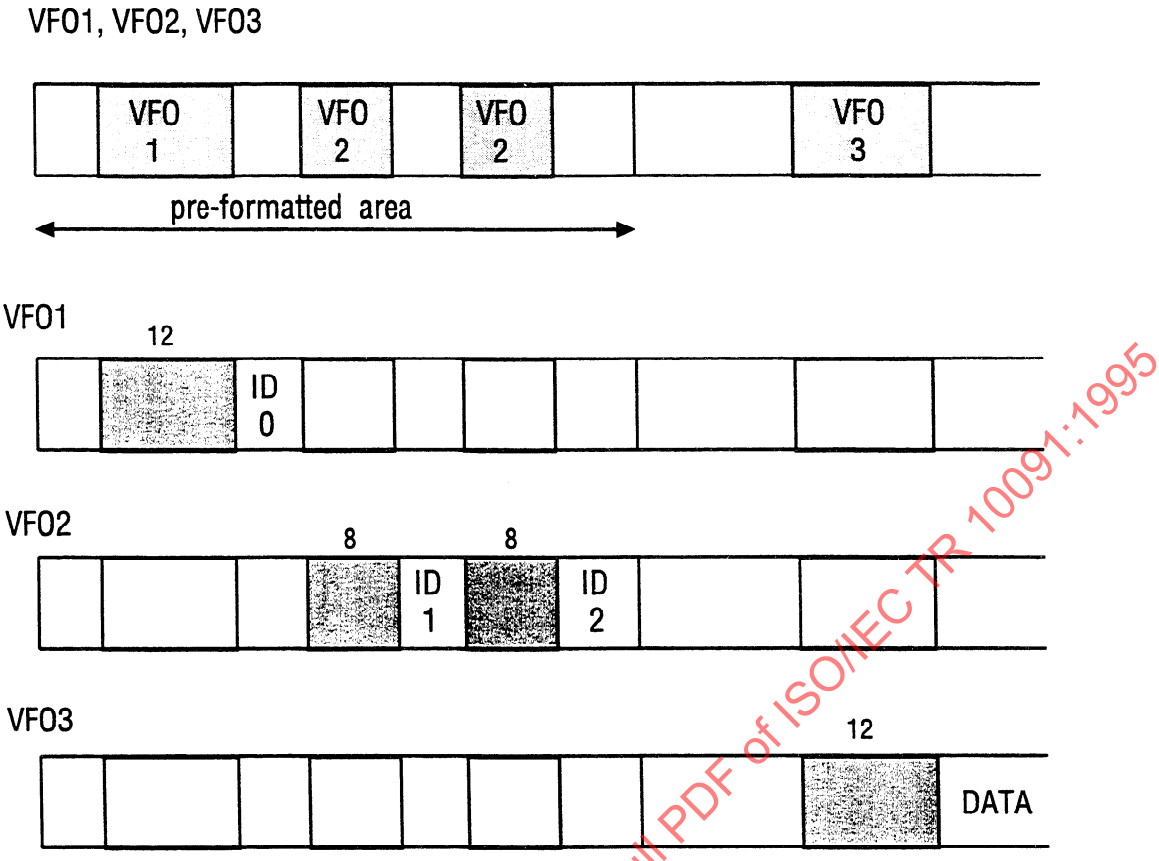
**Comment on the length of the VFO**

Pull-in times for phase-locked loop (PLL) circuitry used in production model of optical disk drives have been measured as follows;

Company A : about 4,5 μs (48 Channel bits),
Company B : about 9 μs (96 Channel bits) in the worst case.

Therefore the length of the VFO region should not be less than 96 Channel bits. A VFO region of 136 Channel bits should be long enough for pull-in of the PLL. An experimental circuit was used for measuring the pull-in time similar to that shown in figure 6. The circuit was modified from what would be used in a production drive by reducing the allowed time for acquisition by 50%. This means that this PLL is less stable than the production version. The signals shown in figure 7 show that the pull-in response was sufficiently stable. The upper trace shows the switching signal which moves between 10,5 MHz and 10 MHz. The figure shows that the pull-in for the VFO was completed within 3 μsec (32 Channel bits).

This demonstrates that it is possible to design a PLL circuit whose pull-in time is shorter than 136 Channel bits and is still stable.




NOTE – There are data on readability of ID's in the following case (ID) (see annex A)

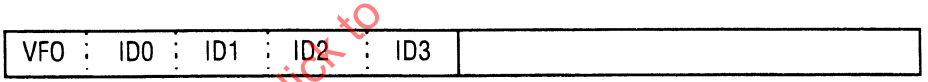



**Figure 5 - VFO fields**

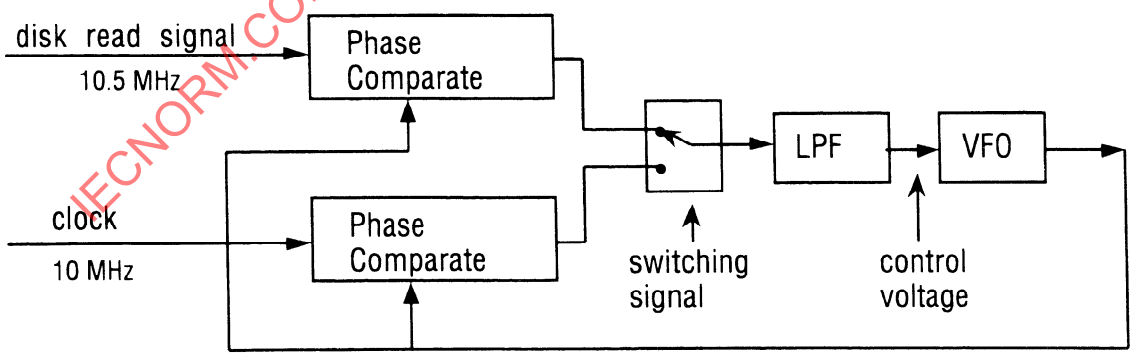



**Figure 6 - Block diagram**

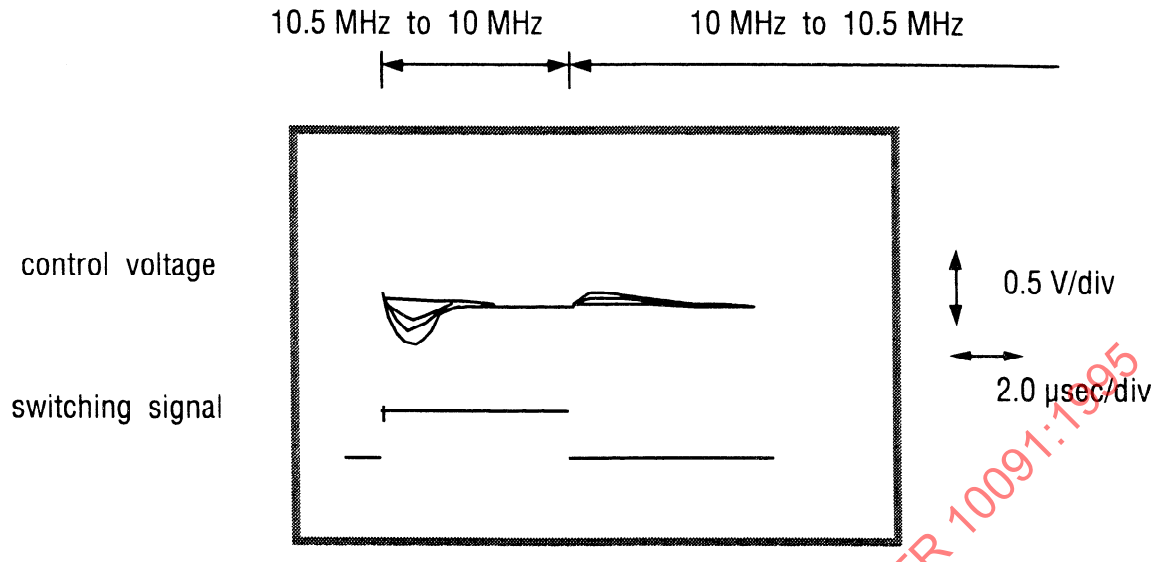



**Figure 7 - Observed pull-in response of PLL**

## 7.3 Address Mark

**Functions**

The purpose of the Address Mark (AM) is to detect the head of each ID field.

**Characteristics of the Pattern**

With the redundancy provided by three ID fields, it was not necessary to continue with another Sync Mark in front of each ID field as once proposed. The Address Mark is a special pattern, not found in RLL (2,7) data, and is a run length violation for RLL (2,7) encoding.

**Example of Detection Circuit**

An example of a detection scheme is shown in figure 8. Both AM and SM detection may use similar circuits.

## 7.4 ID field

**Functions**

The purpose of the ID field is to identify the track number and the sector number.

The ID field consists of 4 sub-parts; a track number, an ID number (to identify the field as ID-1, ID-2 or ID-3), a sector number, and a CRC. A successful ID field detection is when all of the 4 sub-parts and the preceding AM (6 bytes total) are detected correctly in one read pass.

**Characteristics of the Pattern**

Reliable reading of ID information and bit and byte timing are achieved by the 3 IDs. Since the AM has an irregular pattern which does not exist in any other area, the ID can be detected using it independently even if the SM fails to be detected.

Accurate bit timing in the sector can be set by using the ID number and CRC OK signal (explained later). This is especially helpful if the SM happens to be missed due to an unusual burst error.

**Example of Detection Circuit**

Figure 8 shows an example of an ID detecting circuit, and figure 9 shows its timing. The sector-timing counter starts when an SM is detected and the count indicates the Channel bit position within the sector. The AM detector detects the AM by pattern matching, using the signal from the disk in a shift register.

The CRC circuit starts when an AM is detected and gets as input the track number, the ID number, the sector number, and the CRC bytes read from the disk. It generates a CRC OK signal if the data plus the CRC bytes result in a zero residual.

The timing counter is readjusted by using both the CRC OK signal and the ID number. If the SM has not been detected, the sector timing counter can start by using the CRC OK signal and the ID number.

At the detection of an SM the PLL has not yet locked and the detecting window is rather large. There may exist an error of 1 or 2 Channel bits, but the correct Channel bit timing can usually be obtained by the first CRC OK signal.

The ID information is recorded 3 times and read data recovery is possible if at least one of the 3 ID's is detected. This means the format can stand a burst error of 320 Channel bits in length. A disk which has manufacturing defects over 100 µm (192 Channel bits) can be easily detected and eliminated before shipping. For write operations, it is recommended that at least 2 ID fields be detected properly. This should give sufficient margin for aging.

**Residual Polynomial of CRC**

The CRC calculation is done with the registers initially preset to all ONEs. Refer to ISO/IEC 9171 for the generating polynomial.

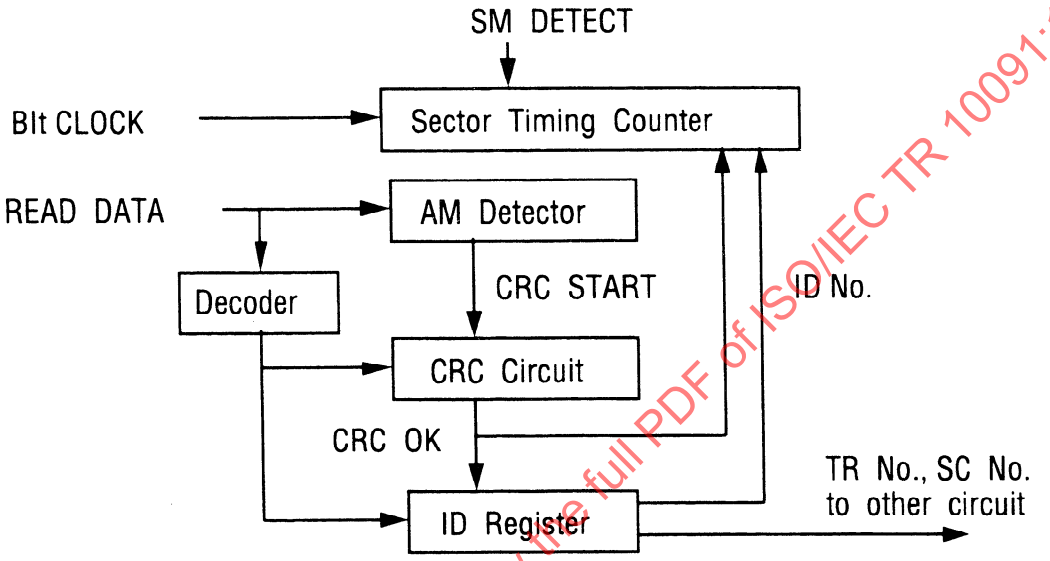
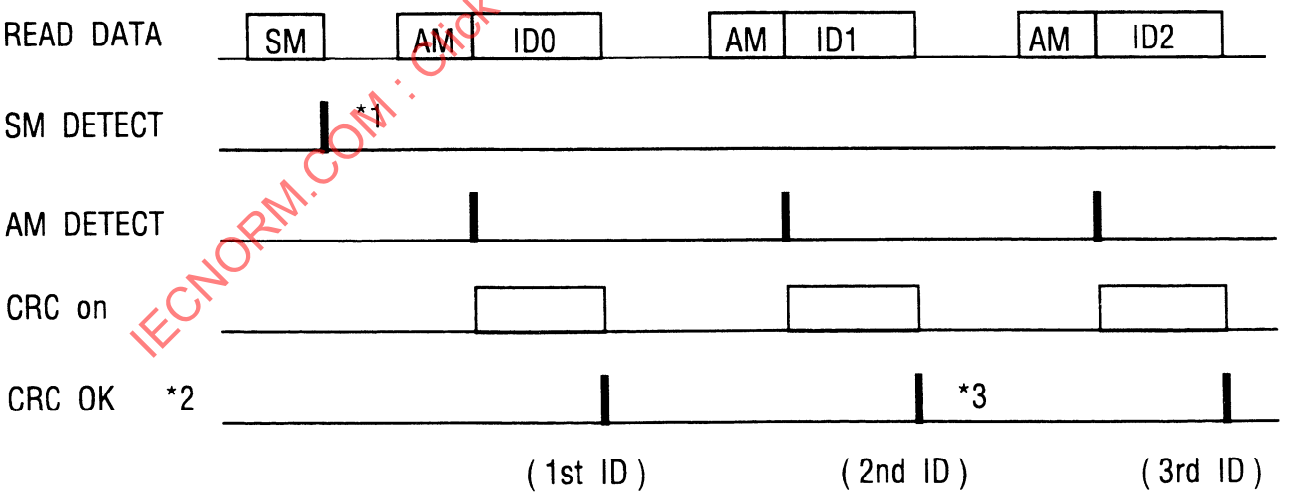



**Figure 8 - ID detecting circuit**




*1 Sector Timing Counter starts
*2 Readjust the Sector Timing Counter
*3 If an error is detected then CRC OK is suppressed

**Figure 9 - ID detecting timing chart**

### 7.5 Offset Detection Flag (ODF)

ODF Marks (also known as Mirror Marks, or Mirror Flags) are areas of the media with no grooves or recorded information for the length of 16 Channel bits.

Some of the basic principles of track offset signal detection are shown in figure 10. ODF marks are independent of the recording method and may be selectively used for offset correction according to the amount of disk skew, and the tracking accuracy required.

In some cases, offset correction would be applied only to tracking for data recovery. In other cases, offset detection would be used only for the detection of the allowable offset signal for write operation, thus providing protection from writing in the wrong area. These ODF marks will not have any adverse effects on the continuous tracking signals even if they are not used for offset correction. The short duration of the marks make their presence completely compatible with the classic CCS pregroove format. Moreover, no additional area is required for the ODF area. The use of the marks is left to the drive designer's choice.

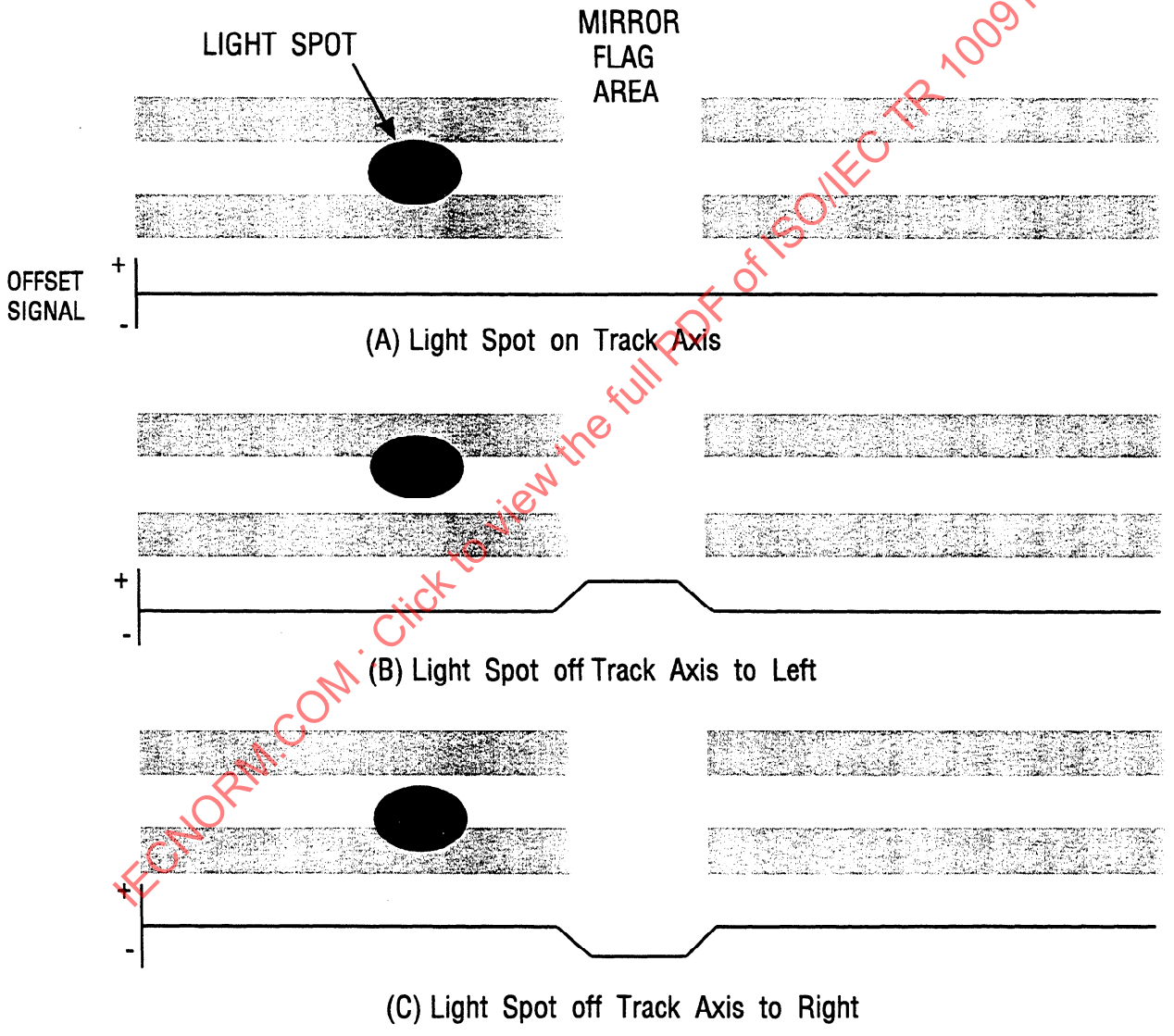



**Figure 10 - Generation of track offset signal**

### 7.6 Gap

A gap consists of an un-written area of 48 Channel bits on either side of the FLAG field to absorb the time fluctuation of flag writing.

## 7.7 Flag

**Functions**

A flag allows a micro processor to make a fast decision as to the status of the sector, without having to read the entire sector and to attempt an ECC correction. The flag is written after the data area write operation has been completed successfully. The Flag field is required to be written in any media conforming to the International Standard.

**Characteristics of the pattern**

It is the shortest pattern with the most resistance to defects that allows the controller to distinguish whether data has been previously written or not. Considering the best correct detection possibility and the overhead, a length of 80 Channel bits was chosen. The pattern begins with the first bit of the field and continues without reset for all 80 bit times.

**Examples of Detection Circuit**

Synchronization of the PLL is not required for the detection of the flag. The detection circuit is similar to the one used for AM detection. A pattern matching method was adopted using a 6 out of 16 match with the following pattern:

100100100100100100.... (18 Channel code bits)

The write flag mark is recognized as active if this 18 bit pattern is found anywhere within the 80 bit length of the write flag field.

Use of the flag byte gives sufficient security against a mistaken write command that would write new data over old data.

The probability for false detection of this pattern is extremely low, since it would happen only when the corresponding 6 bits are exactly duplicated by a defect.

## 7.8 ALPC

**Functions**

The Auto Laser Power Control (ALPC) is an area which allows for a reliable measurement of the output power of the laser diode (LD). An arbitrary test pulse pattern can be written in this area to adjust the laser power. During this test recording period the optimum writing current level can be obtained.

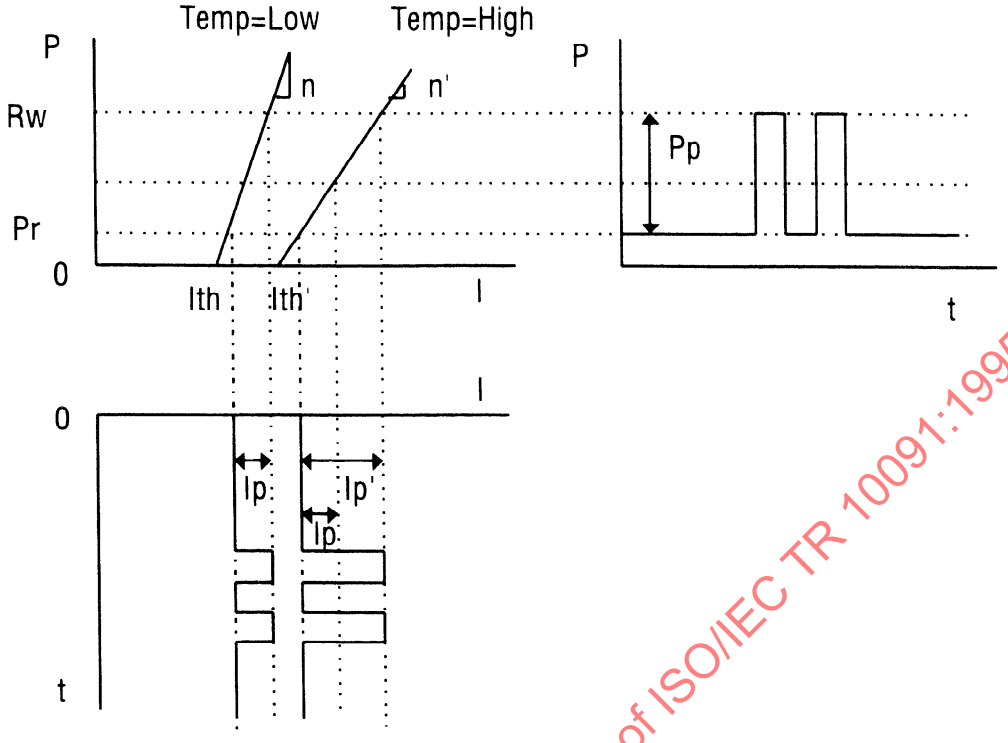
The optimum write current level would be set before the data field is written.

The laser power adjustment is carried out by a microprocessor in the drive. No special operation is needed by the controller or the host computer.

**Necessity of ALPC area**

Figure 11 shows the relation between drive current ($I$) and output power ($P$) of a typical laser diode. Its threshold current, $I_{th}$ and differential efficiency, $n$ vary as a function of its temperature. The temperature rise causes an increase in $I_{th}$ and a decrease of $n$. Moreover, $I_{th}$ becomes larger and $n$ smaller after aging.

While reading, the output power of the LD is kept constant by feedback control using monitored output power. During the writing period the additional drive current, $I_p$ needed to output the required pulse power, $P_p$ is inversely proportional to $n$, so some compensation is required.




NOTE

Pr : read power
Pw: write power
Pp: write pulse power
Ith: threshold current
Ip : write pulse drive current
n : differential efficiency

**Figure 11 - Characteristics of laser diodes**



## 7.9 Sync

**Functions**

The purpose of the Sync field is to establish the bit and byte synchronization timing for the data field.

**Characteristics of the pattern**

As can be seen in figure 12, the autocorrelation function of the proposed pattern has a sharp peak point only at the correct sync timing, and has a small value elsewhere. Moreover, majority logic tolerates some errors due to the redundancy of the pattern.

**Examples of detection circuit**

Figure 13 shows an example of a detecting circuit. Signals from the disk are fed into a shift register, then the output of the shift register enters a decoder, and is decoded by block. Each block is one of *n* partitions of the normal pattern.

The majority logic recognizes Sync if it detects more than *m* signals out of *n* decoded signals. For example, let $n$= 12 and $m$=8, and assume that four block errors are present. Given that the condition $m>6$ will occur only at $t$=0 (because the majority logic can detect 8 out of the 12 possible decodes signals only in the neighborhood of $t$=0 (see figure 12)), then Sync will be detected correctly even with errors present

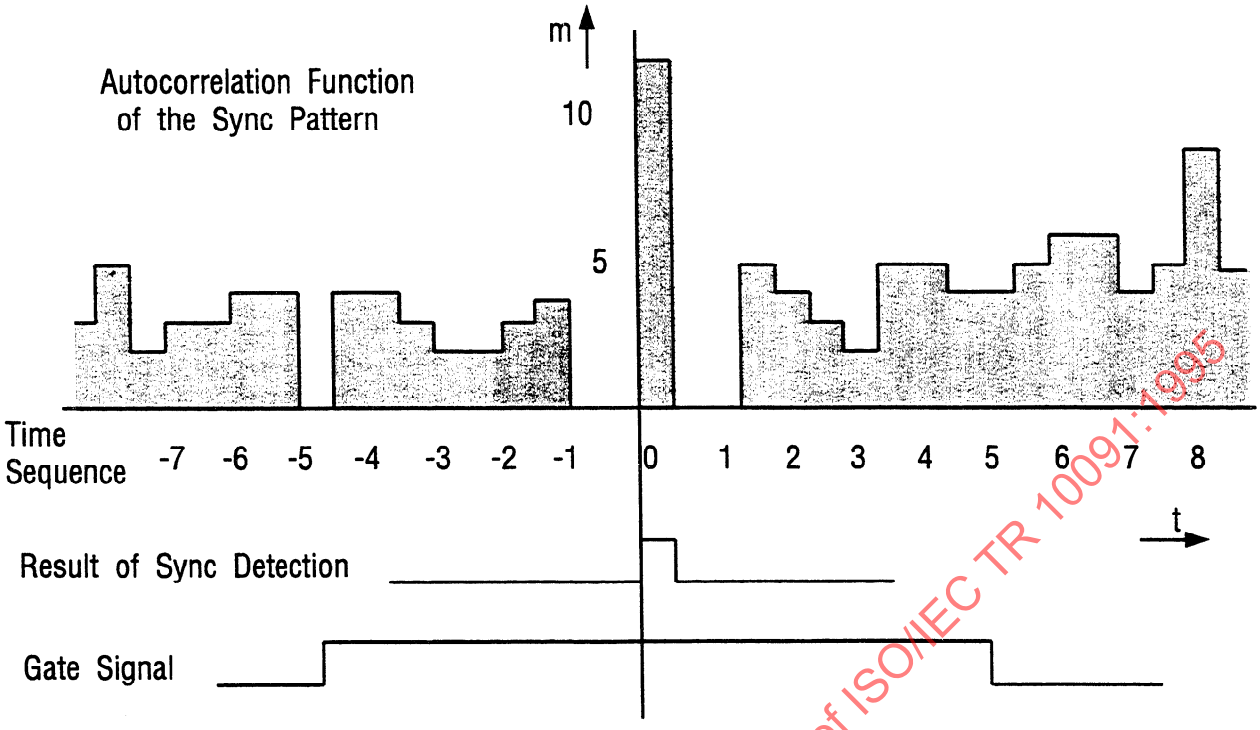



**Figure 12 - Timing chart of Sync detection**

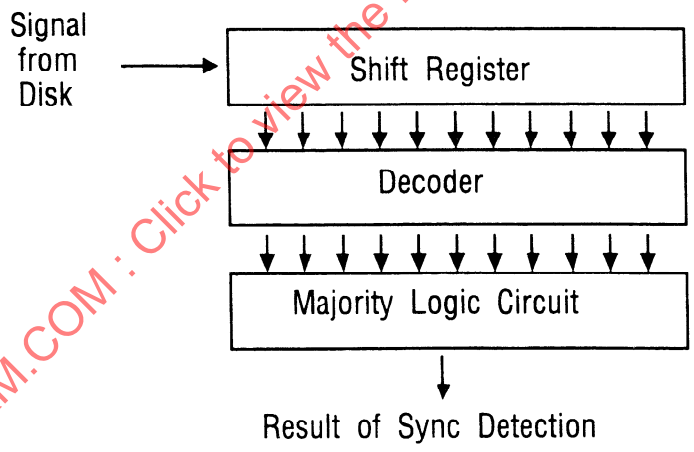



**Figure 13 - Sync detecting circuit**



### 7.10 Data field

The Data field consists of 1024 bytes (512 optional) of user data and 164 bytes of CRC and ECC information and 59 bytes of Resync information, plus 12 bytes of defect management pointers.

The defect management pointers within the data field consist of 12 bytes divided into three 4-byte pointers of address information used for bad block mapping and error recovery. If the sector is a primary sector (not a spare sector) then the three pointers contain the following information:

P1 = Self-address (this sector)

P2 = Address of the first sector of the current replacement group of sectors.

P3 = A duplicate of P2

If the sector is a spare (replacement) sector, then the pointer will have the following information recorded when it is written as a replacement for a defective Primary sector:

P1 = Self-address, (this sector)

P2 = Address of the original defective sector (backwards pointer)

P3 = A duplicate of P2

See table 4 for pointer configuration.

**Table 4 - Defect Management Pointer information**

| First Byte | Second Byte | Third Byte | Fourth Byte |
|---|---|---|---|
| Track MSB | Track LSB | Sector Number | Reserved(FF) |

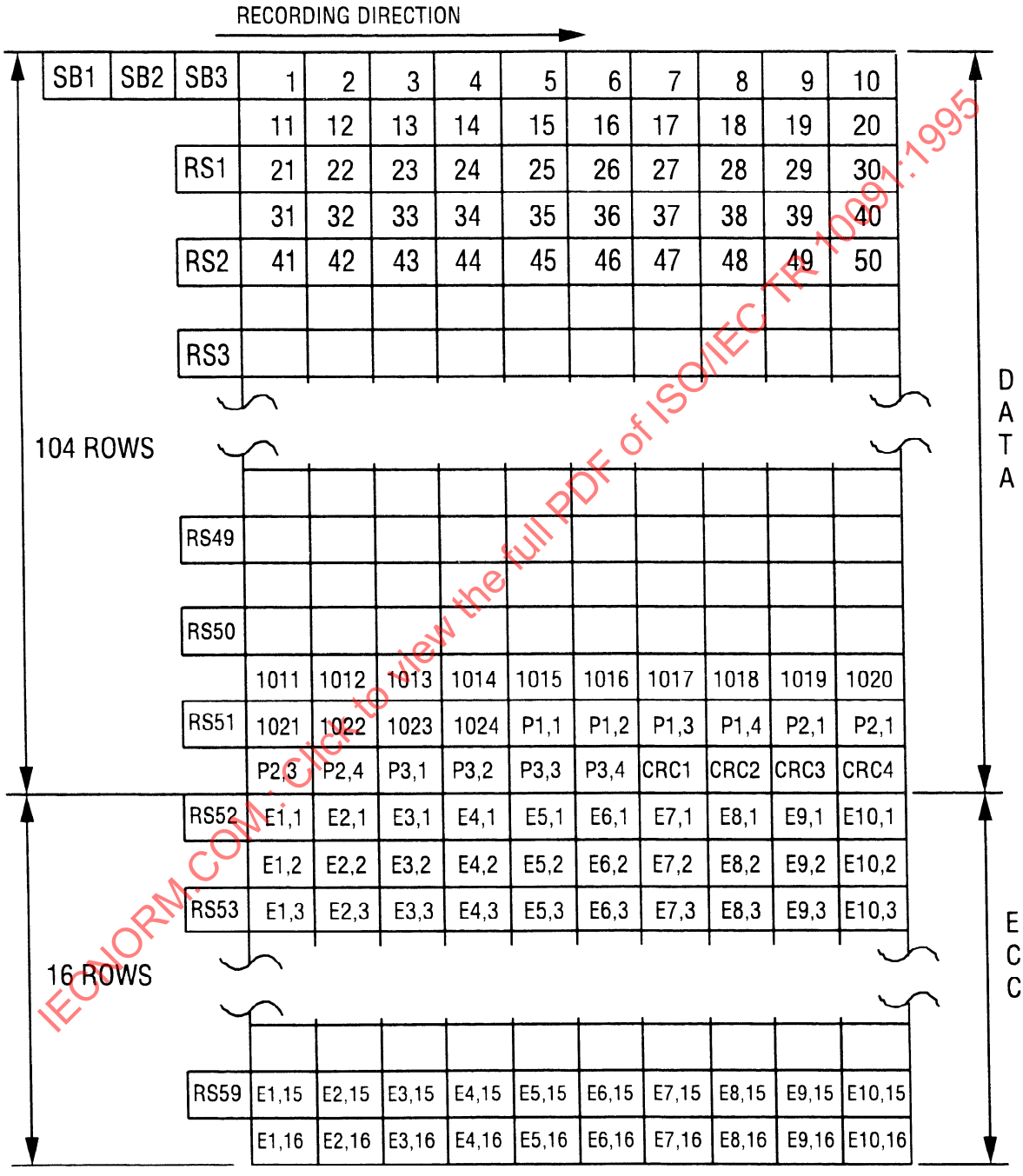



**Figure 14 - Continuous servo data block configuration**

(1 024 byte sector format, ECC with 10-way interleave)

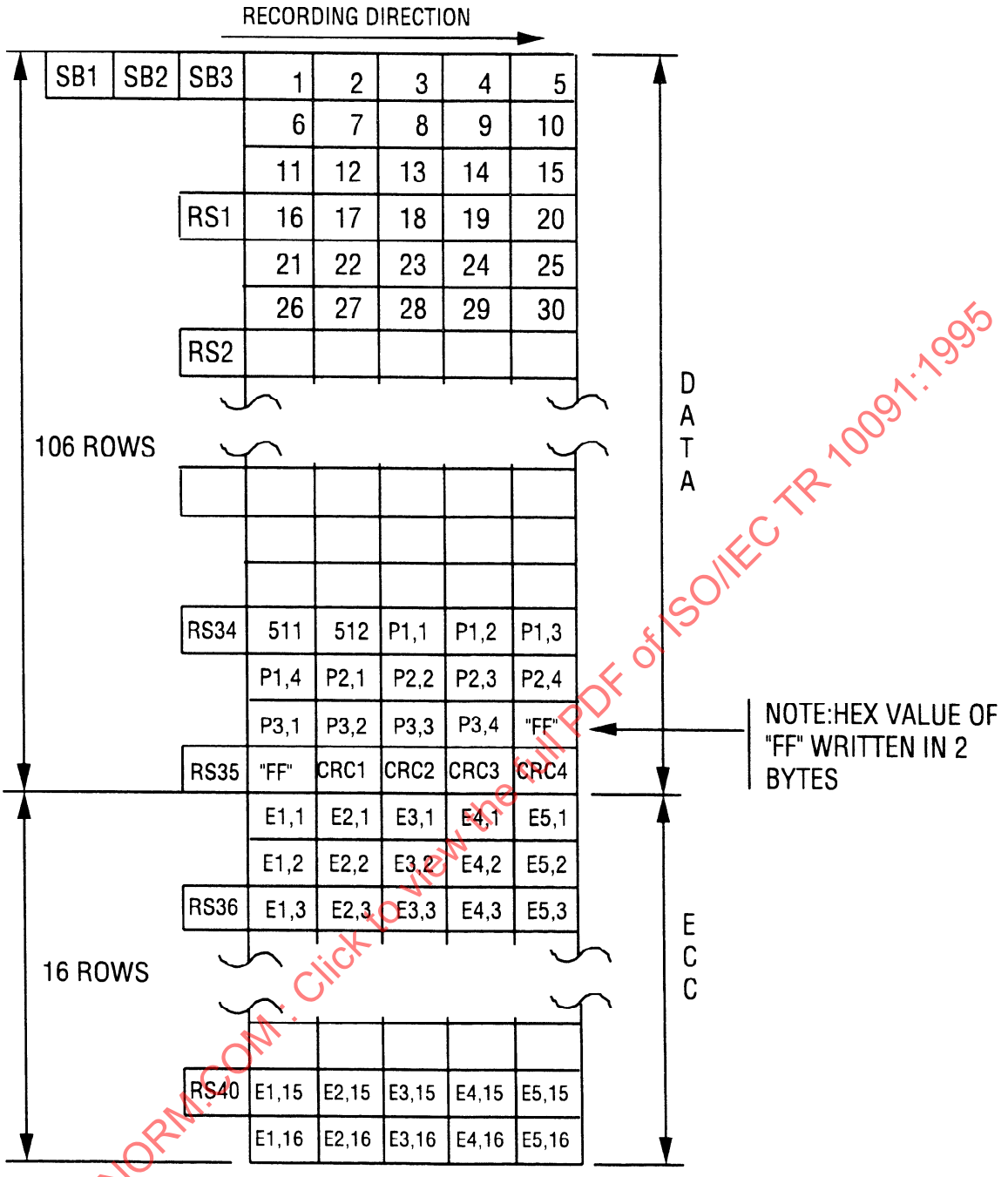





**Figure 15 - Continuous servo data block configuration**

(512 byte sector format, ECC with 5-way interleave)

## 7.11 Resync

**Functions**

The primary purpose of the Resync field is to prevent error propagation after a burst error. Detection of the Resync pattern sets the byte timing window, thus preventing bit slip propagation after a defect.

The Resync field prevents the loss of byte synchronization when the VFO rides through defects within a Data field and can be used to recover data even if the Sync pattern is missed.

The position of Resync field within the Data field was chosen to use the smallest amount of overhead while still giving good protection. Loss or failure to detect one Resync will not result in too many bytes to correct in any single ECC interleave. One

Resync failure could result in 40 bytes in error (4 bytes per interleave), which would be the worst case for a 1024 byte sector. The ECC can easily correct for this type of error.

Loss of two Resync fields can still be corrected, but this type of error begins to approach the limits of the ECC. It is not recommended to attempt error correction if three or more Resync bytes are lost.

A secondary use of the Resync field is to compensate for the loss of the Data field Sync Mark. Since Resync is a 16 channel bit patten, a defect could look similar to the Resync pattern. To avoid this problem, gating signal is used to insure that the detection of Resync is only allowed at specific time intervals. This reduces the probability of false detection to a very low value. The timing for the Resync gate can be established during the ID fields or even during the previous sector.

With the Resync timing gate established, it may be possible to recover data from a field when Sync is not detected. If VFO lock and AGC levels can be established within 2 Resync marks, the data can be recovered by use of ECC correction on the first portion of the field. The use of this method depends on the VFO design.

**Characteristics of the Pattern**

The Resync has a sharp correlation peak when a proper detection circuit is used. It is an irregular pattern of the RLL (2,7,) code, not found in data yet not an RLL (2,7) violation.

**Examples of Detecting Circuit**

The detecting circuit is almost the same as that for Sync Mark (see figure 6).

### 7.12 Buffer

**Functions**

Motor speed tolerances and mechanical tolerances require some reservation of space at the end of each sector to prevent the overrun of one sector into another, when different sectors are written by different drives at different times.

**Allocation of 20 bytes of the Buffer**

| Item | Tolerance | Bytes Used |
|---|---|---|
| - rotational jitter | $10^{-3} > 0,1\%$ | (1,4 bytes) |
| - eccentricity, mechanical oscillation | 200µm > 10µs > 0,3% | (4,2 bytes) |
| - imperfection of the disk | 2µs > 0,003% | (negligible) |
| **Totals** | **0,4%** | **(5,6 bytes)** |

Allowing for a worst case of 1%, 14 bytes should be reserved to absorb these time fluctuations.

Another 6 bytes are allocated for time which may be necessary for electronics and software to prepare to read and write the next sector. In addition, the time of the first 17 bytes (5 bytes of SM and 12 bytes of VFO) in the next sector can also be used for software processing if needed.

**Modification of the length of the Buffer**

In the case of the optional 512 byte format, the length of the Buffer field is modified slightly to make the timing rate the same as that of the 1024-bytes format. The average length for each Buffer is 14,81 bytes, thus 15 bytes are used.

### 7.13 Delete pattern (Optional)

**Functions**

A delete pattern is not defined in ISO/IEC 9171, but a specific pattern is recommended. This pattern should be written over the data in the sector to be deleted.

**The proposed pattern**

Pits of the length of 5T (T is 1 Channel bit time length) are recorded over the data at an equal separation distance of 30T (see figure 16).

A read signal and track error signal from a deleted sector are shown in figure 16. It shows that the delete pattern does not affect the tracking. The signals are expanded on the time axis in figure 16. The recorded data are blacked out over the marked area of delete pattern. The digitalized signal is shown in figure 16. The marked area can be detected with good reliability.

**Examples of detecting circuit**

This pattern should be recognized by the controller. The drive designer chooses a suitable method. For example, count the number of 5T pattern marked areas in a sector. When this number is over the predetermined value, the sector shall be considered as a deleted sector.

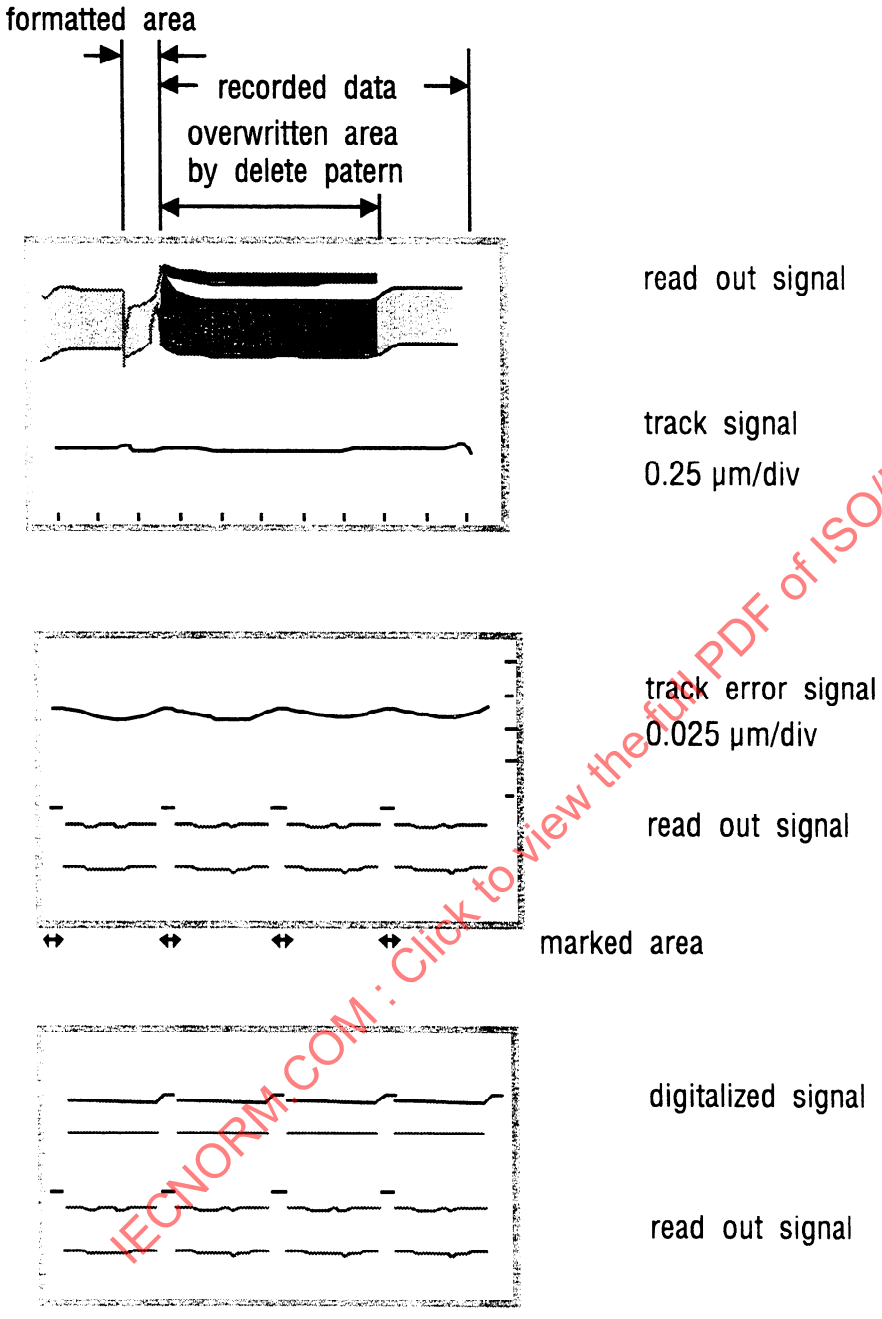



**Figure 16 - Delete pattern**



## 8 Error detection and correction

Please refer to ISO/IEC 9171 for a complete description of the defect management procedures.

## 9 Modulation method

**Recording method**

(2,7) modulation code (see table 5)

Pit position recording (see figure 17)

Peak detection

**Advantages**

a) code is self-clocking

b) The density ratio of (2,7) code is larger than other codes (see figure 18). This results in a higher bit density

c) The error propagation of the (2,7) code is small. It is limited to four bits. Burst error propagation is limited by use of a one-byte Resync mark throughout the data field.

d) The (2,7) code is well known and "field proven" with a large number of products.

e) Laser power fluctuations and inhomogeneities of the sensitive layer of the disk will have a small influence on signal jitter in pit position recording using peak detection, compared with edge detection methods.

The recording method is mark position recording. The centre or the mark is all that determines the presence of a Channel bit.

**Table 5 - RLL (2,7) Code Conversion**

| Input bits | RLL 2,7 Channel bits |
|---|---|
| 10 | 0100 |
| 010 | 100100 |
| 0010 | 00100100 |
| 11 | 1000 |
| 011 | 001000 |
| 0011 | 00001000 |
| 000 | 000100 |

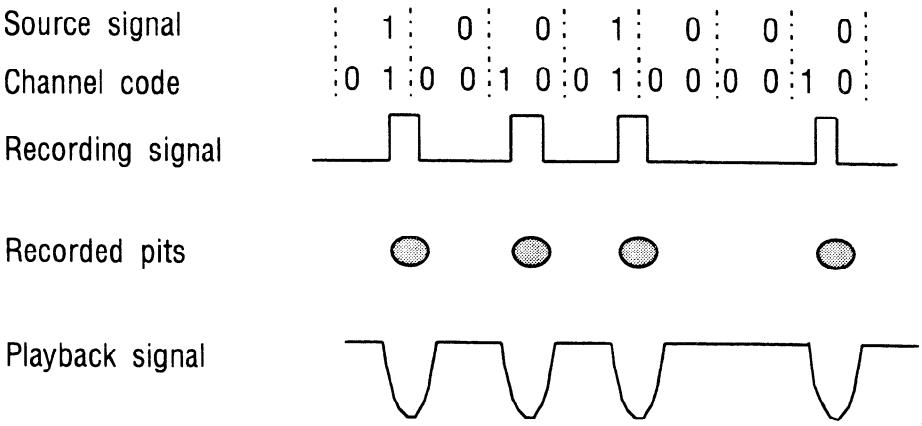
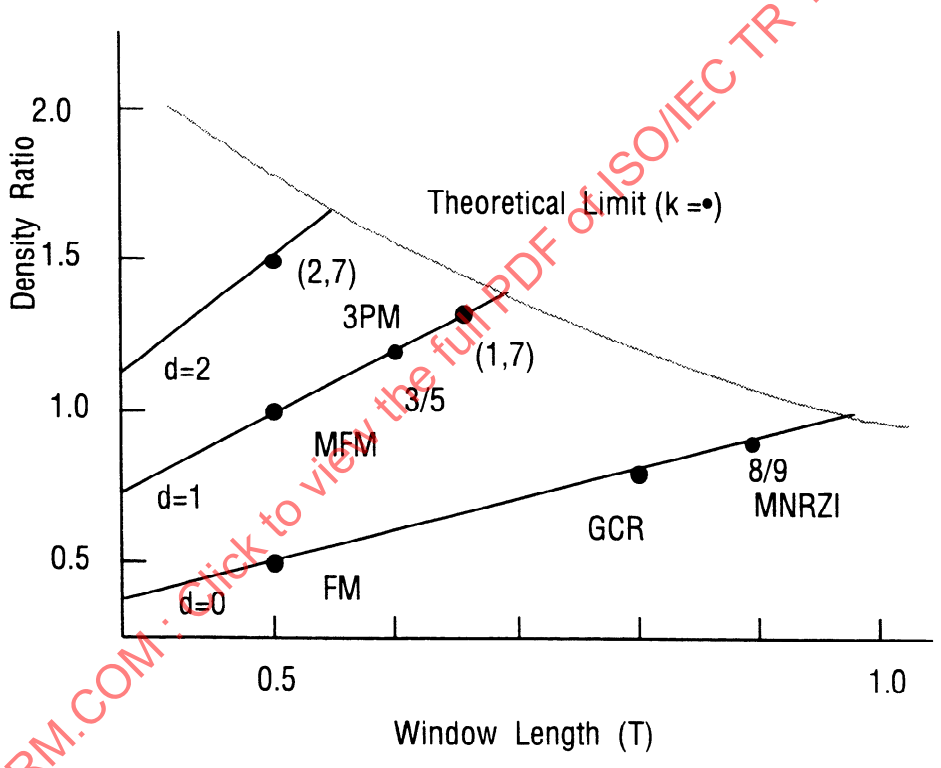



**Figure 17 - Schematic diagram of pit position recording**




NOTE

d: minimum number of 0s between successive is
k: maximum number of 0s between successive is
T: data bit period
m/n: modulation code rate
(m/n)(d+1)T: density ratio

**Figure 18 - Density ratio and window length of typical modulation code**

# Section 3 - Type B format

## 10 Sampled Servo

The Sampled Servo tracking format is explained in this section. The Type B format is based on a sampled servo tracking method (see ISO/IEC 9171-2 clause 6).

## 11 Prerecorded signal properties

Prerecorded signal properties are specified in the section 6.1.2 of ISO/IEC 9171-2. In this section,an example for setup of a disk mastering system is shown. The parameters required to be measured and the simulated results are also shown to confirm the specified values.

### 11.1 Schematic diagram of the disk mastering system

Figure 19 shows a schematic diagram for configuration of a disk mastering system. A simple single beam optical system with a high speed optical beam deflector is used to fabricate wobbled marks and a high speed optical modulator to fabricate clock marks or header marks as required. As the position of the clock marks is a critical parameter for the sampled format disk system stability, an accurate and stable disk rotation mechanism is required.

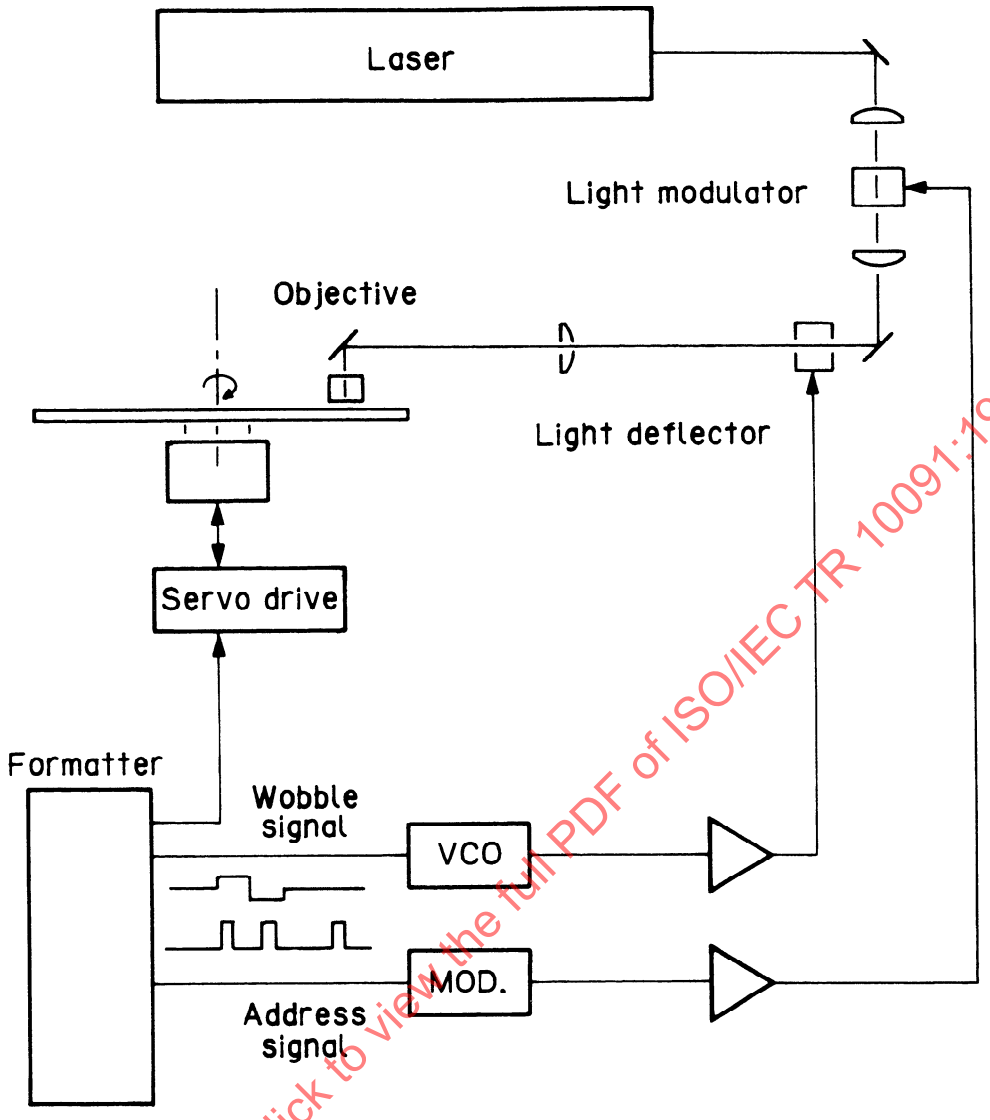



**Figure 19 - A schematic diagram of the mastering system for the sampled formatted disk**

## 11.2 Signal amplitude of the prerecorded signal

The prerecorded signal amplitude is specified as a fraction of the signal obtained from an unrecorded area:

$0,4 < I_p/I_o$

$I_p$ is a prerecorded signal and $I_o$ is a signal obtained from an unrecorded area (see figure 20). The range of full width at half maximum amplitude (FWHM) is specified as follows:

FWHM < 2,3 x channel bit length

For a stable clock recovery, the value of $I_p/I_o$ should be as large as possible while FWHM should be less than 2,3 times the channel bit length. The value of $I_p/I_o$ can be varied by enlarging the length of the prerecorded mark. A simulated result of the FWHM at the innermost radius of the user area is shown in figure 21. The profile of the read-out spot is indicated in the same figure. The result shows that the length of the mark can be longer than the channel bit length, while the FWHM is less than 2,3 times the channel bit length.

The optical parameters of the optics used for the calculation was as follows:

| | |
|---|---|
| $\lambda$ | = 825 nm |
| $\lambda$/NA | = 1,59 µm |
| R/W(tan.) | = 0,8 (tangential direction) |
| R/W(rad.) | = 1,0 (radial direction) |

The maximum allowable mark length at the most inner radius was ~ 0,8 µm and the corresponding $I_p/I_o$ was ~0,8.

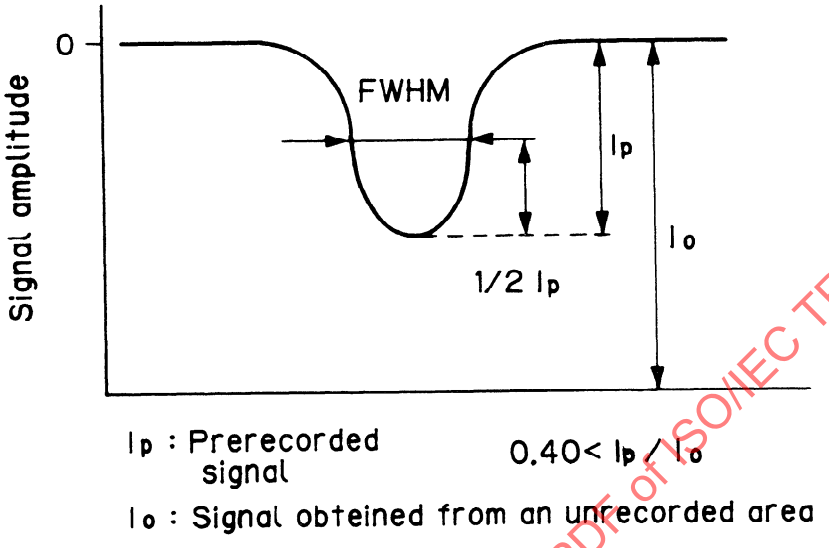



**Figure 20 - The definition for the amplitude of a prerecorded signal**

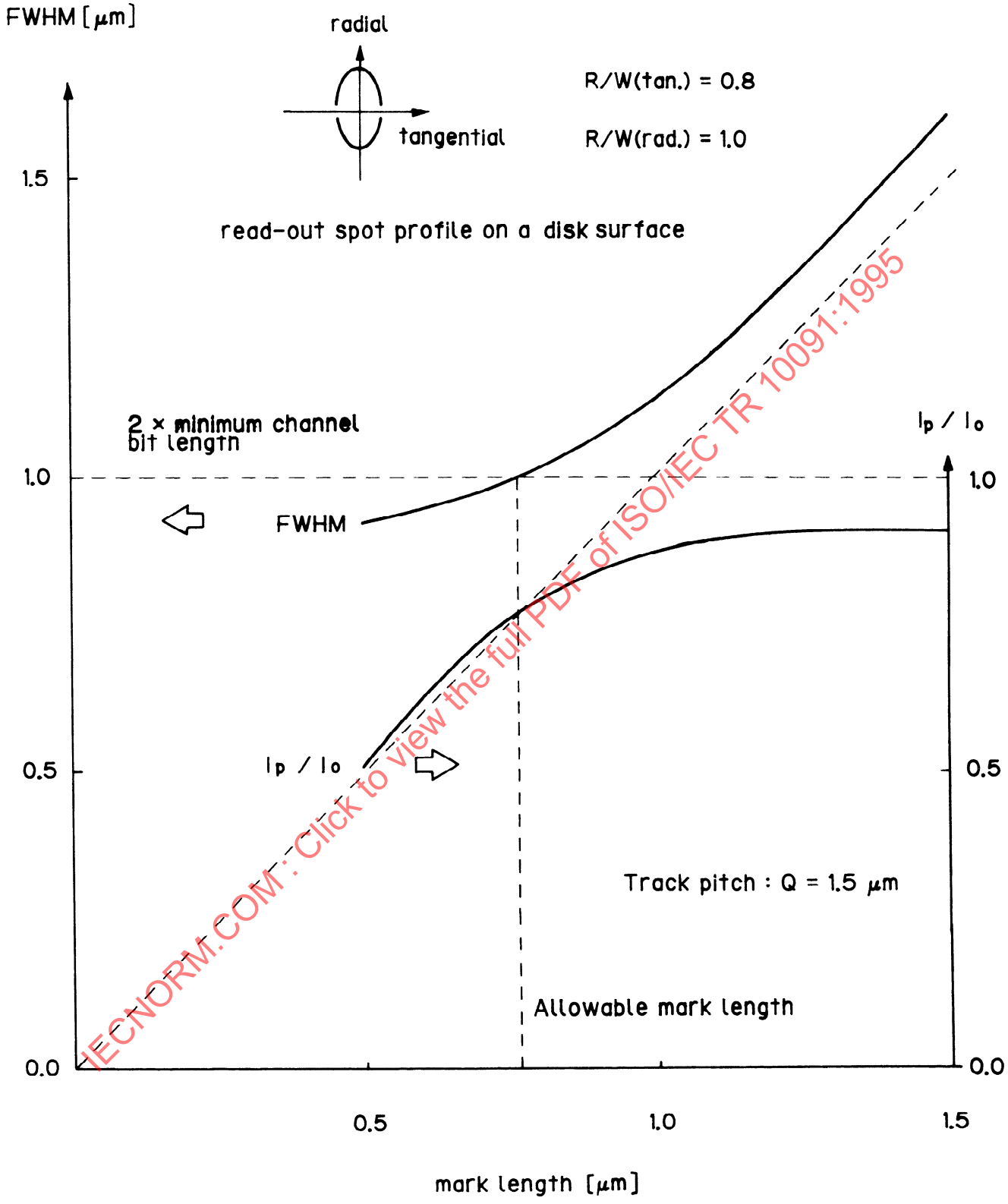





**Figure 21 - The full width at half maximum amplitude (FWHM) vs. mark length**

## 11.3 Tracking error signal

**The allowable amplitude difference between two wobble marks**

The average signal amplitude of the first wobble mark $I_f$ and that of the second wobble mark $I_s$ shall be identical within 5% while tracking at track centre:

$$|I_f - I_s|_{centre} / I_o < 0,05$$

This specification determines the allowable difference between two wobble marks. As shown in figure 22, an off-centring of the beam spot will be less than 0,05 mm if the difference between two wobble marks is as determined above.

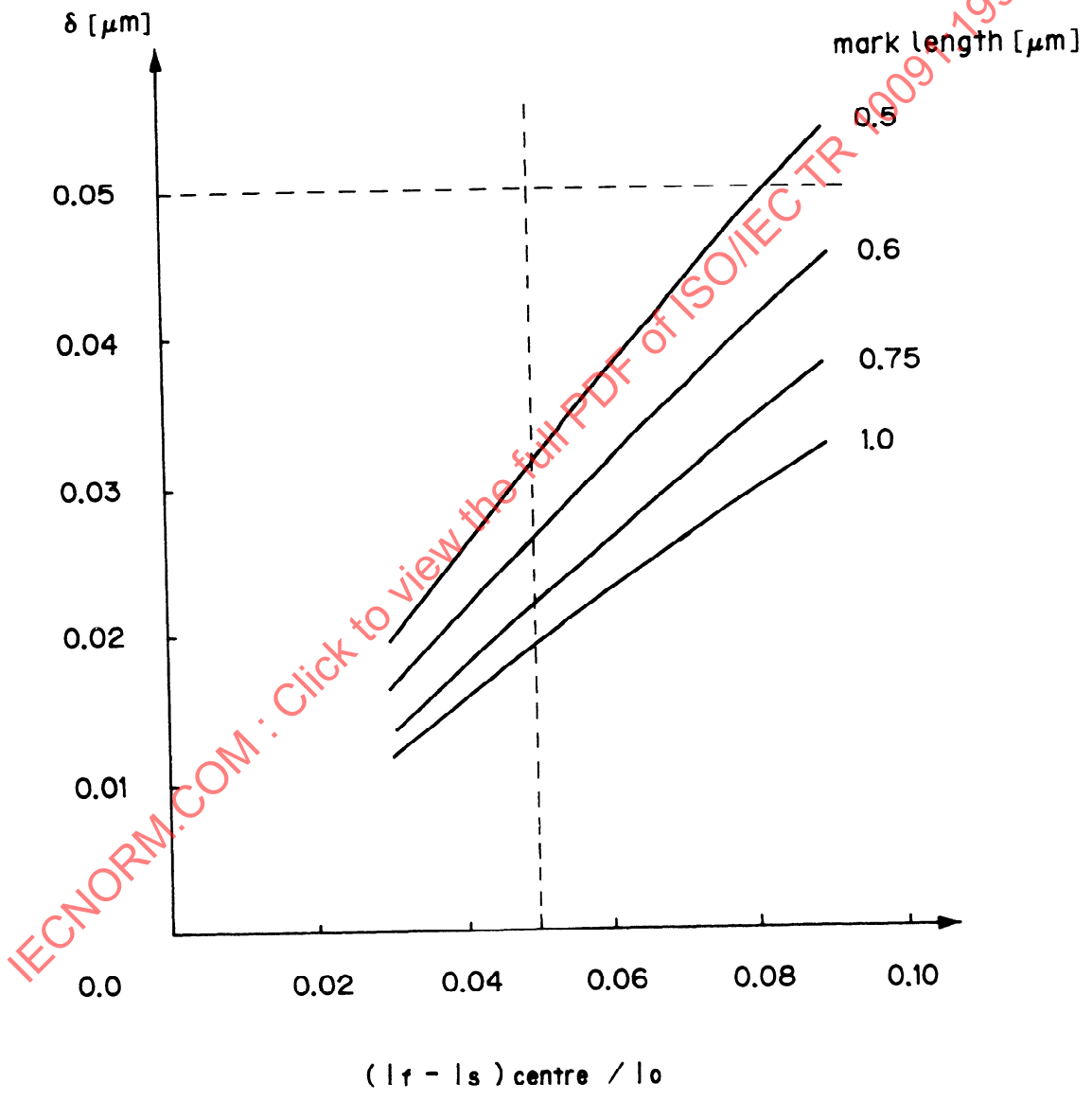





**Figure 22 - Off-centring of the beam spot δ plotted against the difference between two wobble marks**

**The amplitude of tracking error signal**

The average signal amplitude of the first wobble mark $I_f$ and that of the second wobble mark $I_s$ shall be within 0,15 ± 0,05 of each other while tracking with 0,1 mm offset relative to the track centre:

$$|I_f - I_s|_{0,1mm} / I_o = 0,15 \pm 0,05$$

This specification determines the amplitude of the tracking error signal at a specific off-centring value. The tracking error signal can be expressed as a function of off-centring.

$$(I_f - I_s)/I_o = A \times \sin(2\pi\Delta\varepsilon)$$

$\Delta\varepsilon$ : off-centring/track pitch

Here, A is the maximum amplitude when the displacement of the wobble mark from the track centre is 1/4 track pitch. $\Delta\varepsilon$ is an off-centring as a fraction of the track pitch (see figure 23). If the beam spot is tracking on 0,1 µm off-centred trajectory, the tracking error signal is,

$$(I_f - I_s)/I_o = A \times \sin(2\pi \times 0,1\ \mu m/1,5\ \mu m) = 0,407 \times A$$

Therefore, the measured amplitude should be

$$0,25 < A < 0,49$$

Figure 24 shows that while the prerecorded mark length was in the range of 0,5 ~ 1,0 µm, both the tracking error amplitude A and the prerecorded signal amplitude were within the specified range mentioned above.



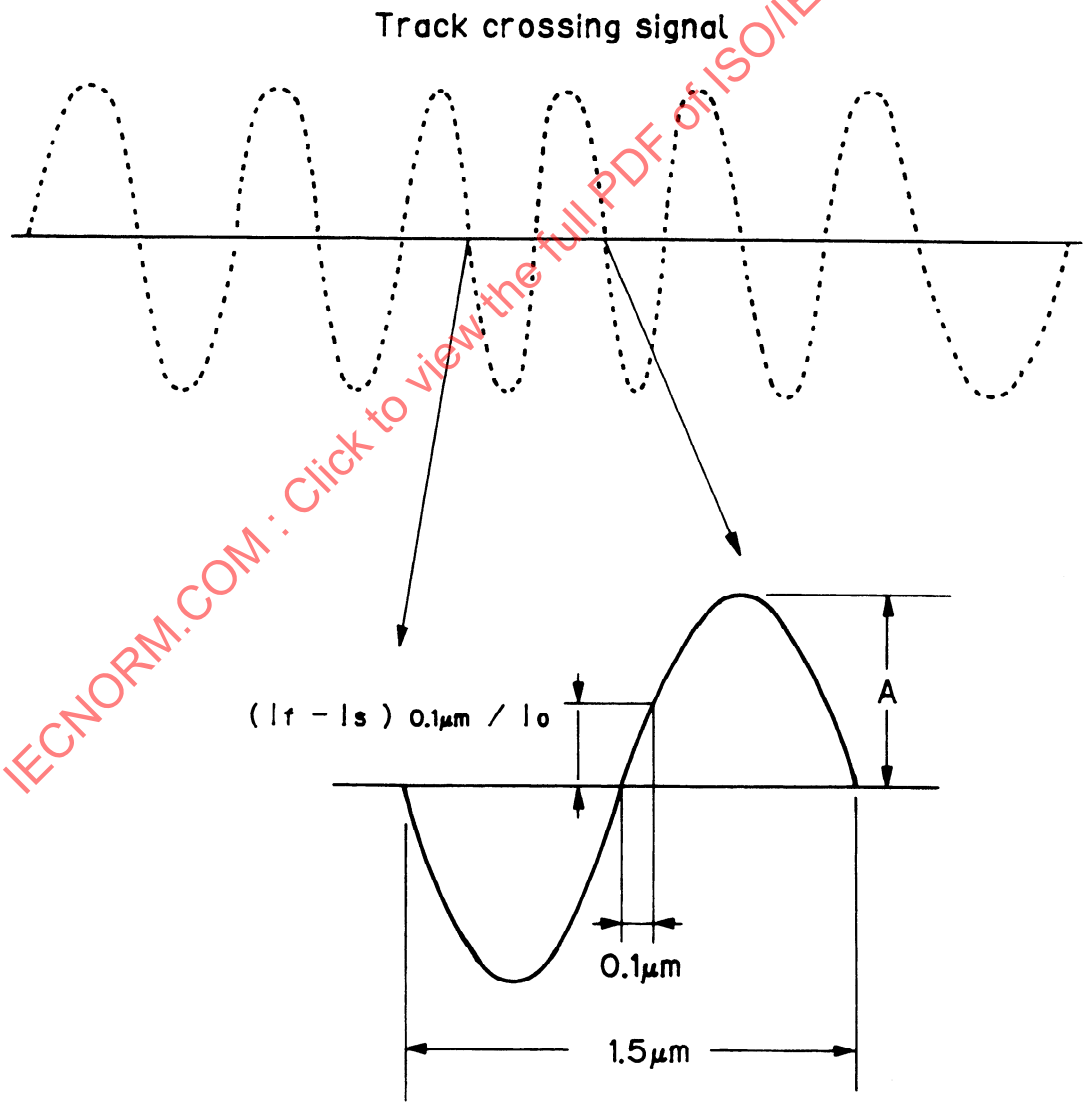
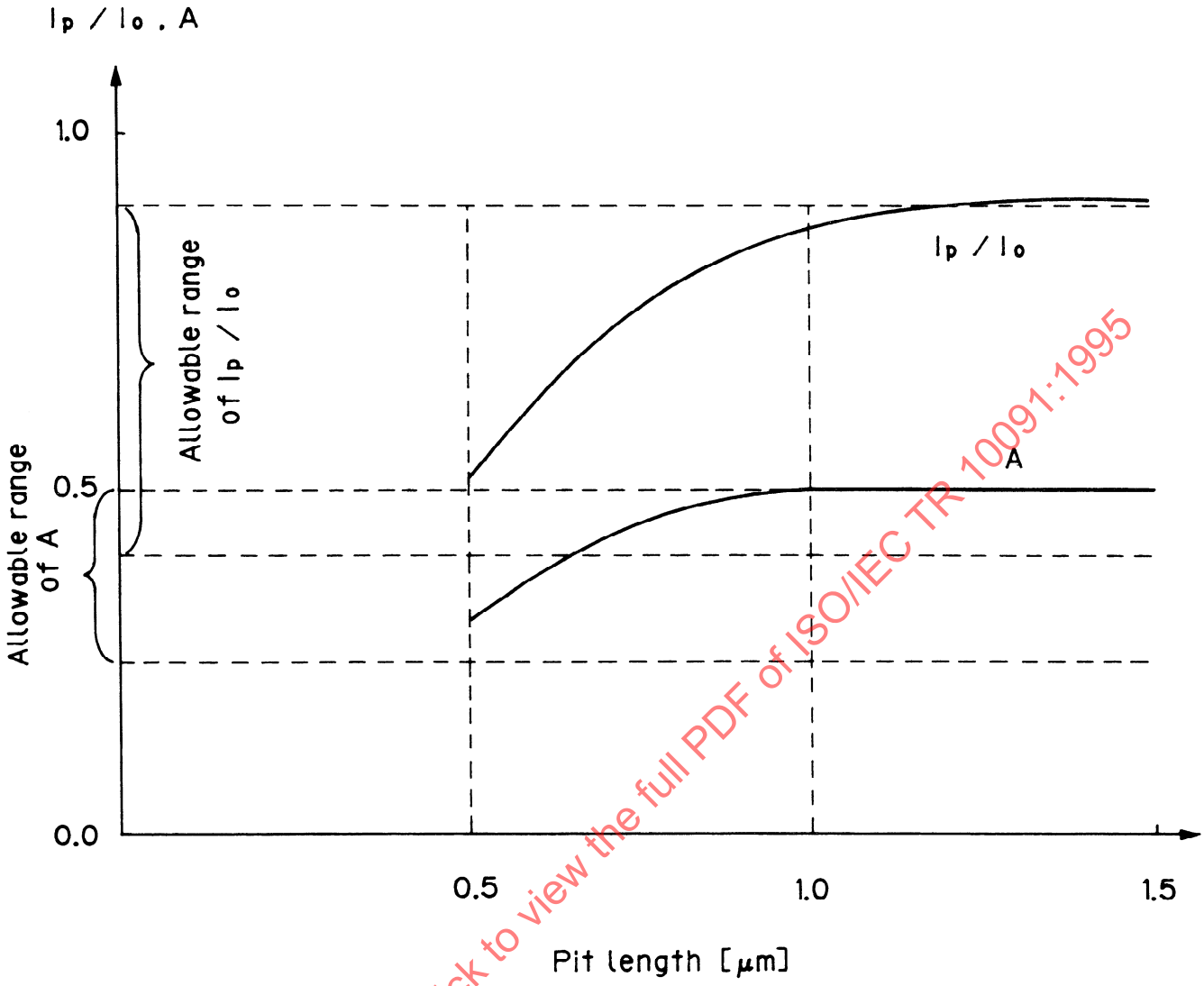



**Figure 23 - Tracking error signal normalized by Io**




A : Maximum amplitude of tracking error signal for a given mark length

Ip / Io : Prerecorded signal amplitude

Optical parameters: R/W(tan.) = 0,8, R/W(rad.) = 1,0, λ = 825 nm, λ/NA = 1,59 μm

**Figure 24 - Prerecorded signal amplitude Ip / Io and tracking error signal amplitude A vs mark length**



### 11.4 Wobble marks

It is prescribed that the wobble marks should be located approximately 1/4 track pitch off the track centre. Figure 25 plots the tracking error signals varying the location of the wobble marks. Suppose that Δq is the wobble mark displacement expressed as a fraction of the track pitch, then the maximum amplitude of the racking error signal can be expressed as a function of the displacement.

$$A(\Delta q) = B \times \sin(2\pi\Delta q)$$

Here, B can be calculated by using the above equation, where A is a value at a certain pit length in figure 24 and Δq = 1/4. Therefore, the tracking error signal will be:

$$(I_f - I_s)/I_o = A(\Delta q) \times \sin(2\pi\Delta\varepsilon)$$

$$= B \times \sin(2\pi\Delta q) \times \sin(2\pi\Delta\varepsilon)$$

If the wobble mark displacement is larger than 2/16 track pitch, the tracking error signal amplitude A (Δq) is also larger than the specified lower limit 0,25, even when the mark length was 0,5 μm. Therefore, the tolerable fluctuation of the displacement can be ± 2/16 track pitch.

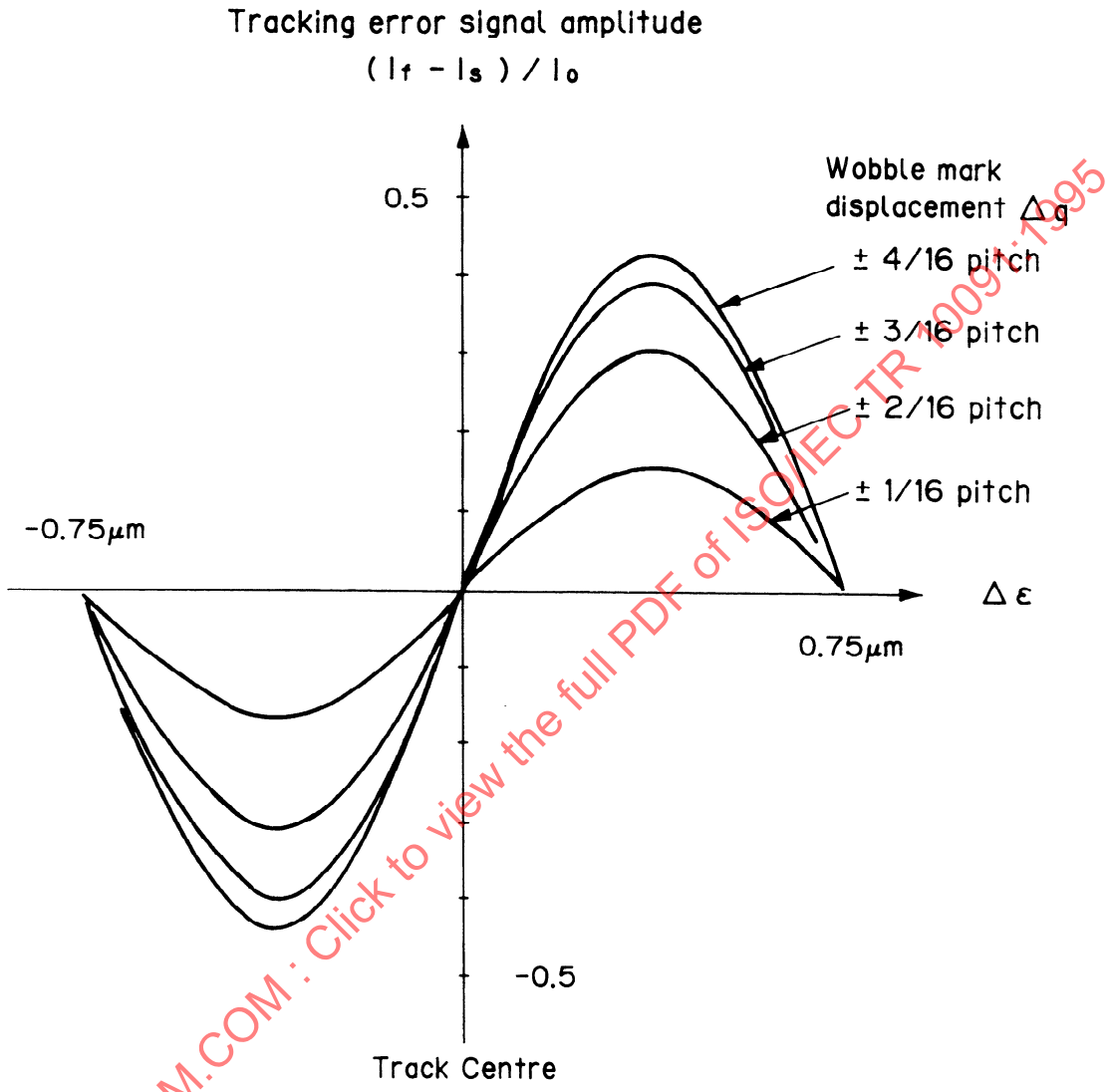





**Figure 25 - Tracking error signal vs wobble mark displacement from the track centre**

## 11.5 Clock mark

The clock mark on the disk should be positioned accurately. Here, an example of measuring the clock mark position displacement is shown. The results of the measurements on a replicated disk using the given method are also described.

**Measurement**

Figure 26 shows a block diagram of the mark position displacement measurement system. The system is composed of a disk drive where the clock is generated from a sampled formatted disk and a circuit which processes the voltage-controlled oscillator (VCO) drive signal. A waveform digitizer and a computer to calculate the mark position displacements is also introduced. The parameters of the phase-locked loop (PLL) circuit of the system with 1800 rpm disk rotation and 11,1 MHz clock rate are as follows:

natural angular frequency : $\omega_n$ = 16 k (rad/sec)

damping factor : $\zeta = 0,7$

The drive signal of the VCO in the PLL indicates the derivative of the mark position displacement of the measured disk. After integrating the signal, a waveform indicating the mark position displacement is obtained. The waveform is digitized and stored in the computer. A fast fourier transformation (FFT) is applied to the waveform to obtain a mark position displacement spectrum. The obtained amplitude of the spectrum is corrected using factors for each circuitry. Finally, the actual mark position displacement spectrum can be obtained.

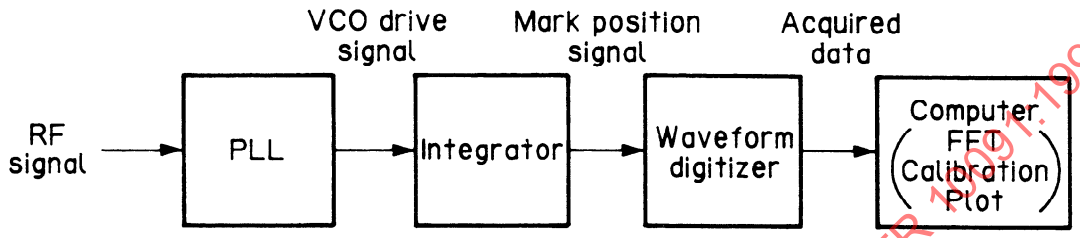



**Figure 26 - Block diagram of the mark position displacement measurement system**

Results

Figure 27 shows a measured mark position displacement spectrum of a polycarbonate replicated disk at inner track –33 mm from the disk centre – and figure 28 also shows the mark position displacement at outer track – 59 mm from the disk center – using the method mentioned above. The base line – 0 dB of the figures is set to be ± 1/90 channel clock width (± 1 ns at 1800 rpm). When cutoff frequency of the PLL loop is 2,5 kHz, the clock jitter can be plotted by the line having a gradient of -40 dB/decade as shown in the figures.

The amount of eccentricity can be measured independently, by counting the traversed tracks with the optical head in a tracking-off state. The peak height of the 30 Hz component of the spectrum should be consistent with the measured eccentricity.

As can be seen in the figures, clock jitter is suppressed below ± 1 ns both at the inner and outer track. The above result shows that the replicated disks can be fabricated having enough accuracy to guarantee the in-track mark position displacement less than 1/30 channel bit at high frequency.

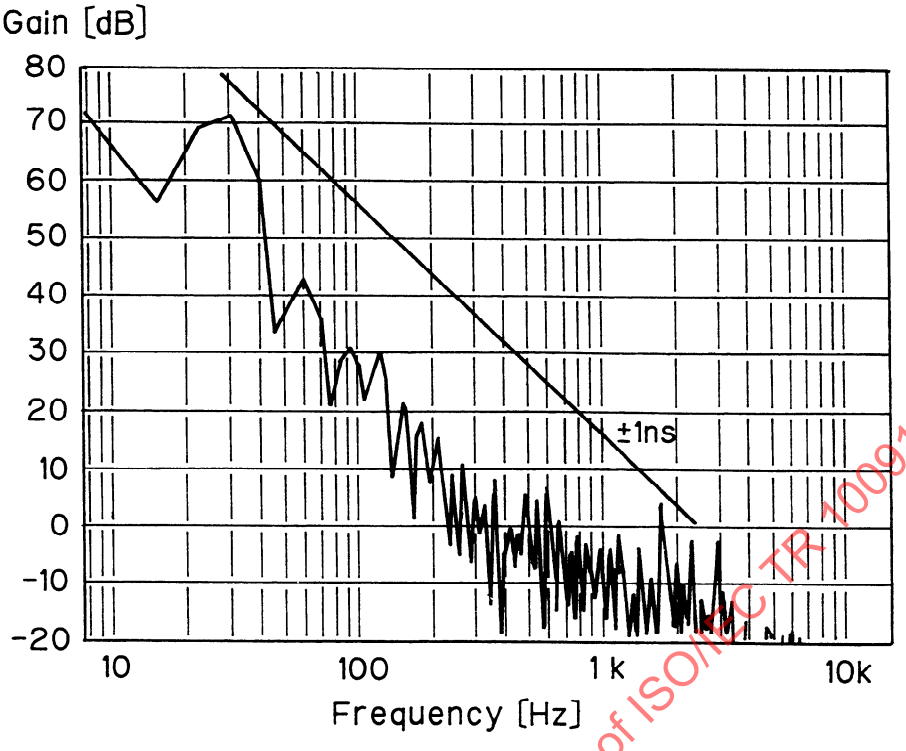



**Figure 27 - Mark position displacement spectrum of inner track (r = 33 mm)**

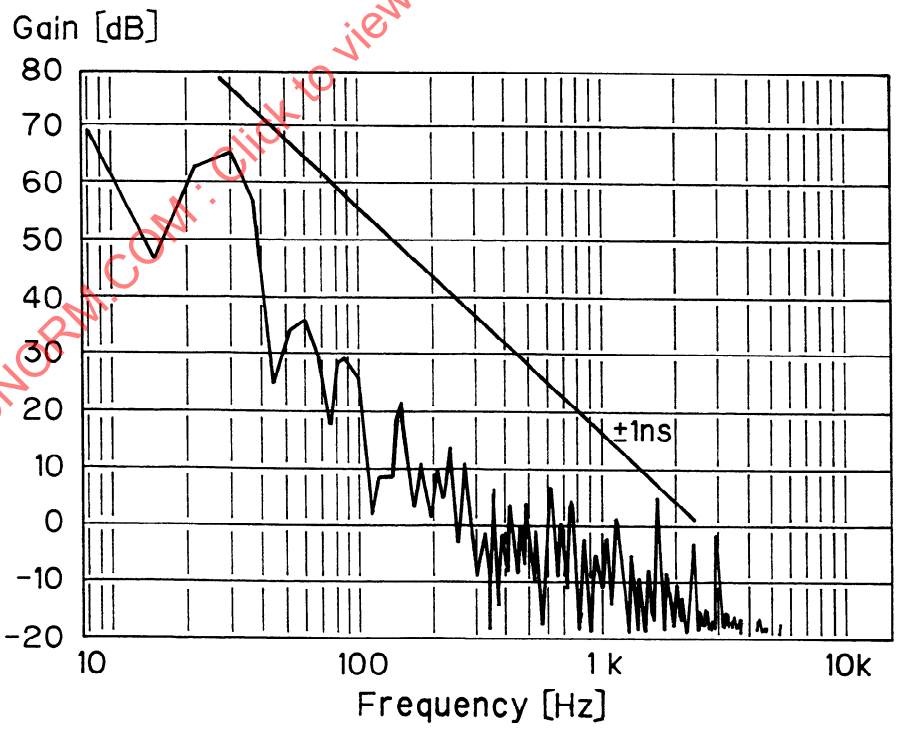



**Figure 28 - Mark position displcement spectrum at outer track (r = 59 mm)**

# 12 Sector header

## 12.1 Sector header format

Each sector has its first 16 data (non-servo) bytes assigned as header area. The first 7 bytes of this area are prerecorded and consist of,(sequentially) sync mark, sector number, most significant byte (MSB) of track number, least significant byte (LSB) of track number, complement of track LSB, complement of track MSB and complement of track LSB. The last 9 bytes of the area are not prerecorded. Six are reserved (non-assigned) and the very last 3 are assigned as laser power control field. As anything can be written in the laser power control field, specific information should not be expected during a read in this field. The header structure is given in figure 29.

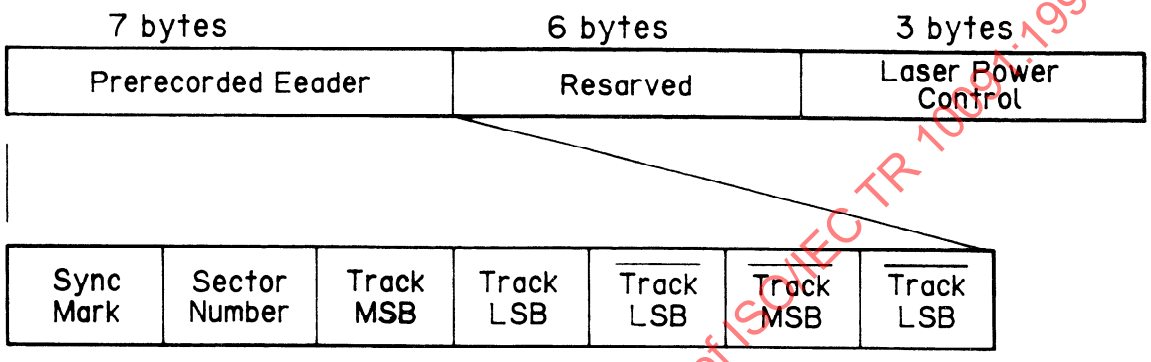



**Figure 29 - Header structure**

## 12.2 Functionality of each part in the sector header

– The sync mark is an unique byte, used to achieve sector synchronization.

– The sector number identifies consecutive sectors on a track.

– The track number (MSB, LSB) identifies the track.

– The track number complements either LSB, MSB or MSB, LSB, following the track number provide a simple protection against defects.

– Further protection of track and sector number is derived from the repetition of the headers on a track ("running check" method).

– The reason for having a LSB and a LSB-bar of the track address close together is to make it possible to read headers during a seek (see figure 30). With the proposed sampled format, even though a beam is crossing the tracks, data can be read when the track crossing speed is not higher than crossing a track within a data byte. If a beam traces at least two data bytes to cross a track, the traced two bytes can be read. Using this capability, a set of track addresses LSB and LSB-bar can be read during seek. Just adding the LSB and LSB-bar in binary numbers, the LSB address validity can be determined. The MSB of the track can be read at almost any time, because blocks of 256 tracks have the same MSB.

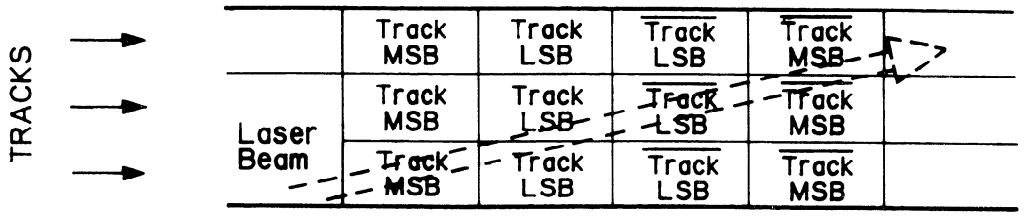



**Figure 30 - Reading an address during seek**

### 12.3 Reliability of the header information

The reliability of the header format is, to a large extent, derived from its repetition. The different features, however, have different dependences on error rates and are, therefore, described separately below (see figure 31). Throughout the following description, it should be kept in mind that the drive is in byte sync with the media, which guarantees very accurate knowledge about the circumferential location of the light spot at all times (i.e. both during regular tracking and seeks).

– The sync mark, in principle, has to be detected correctly only once to achieve correct sector synchronization. If the random byte error rate of the media equals P, the probability of finding a single sync mark in error equals P and the probability of misdetecting any bytes as a sync mark equals P/256. Hence, the probability of mistaking any byte in a sector for the sync mark equals 43 x 16 x P/256 = 2,7P. Therefore, at start-up of the drive or at any time sync loss is suspected, it is required to execute a check of the correct repetition (once every 43 x 18 = 744 bytes) of the sync mark. In a three sector long search for at least two mutually correctly located sync marks without any other mislocated ones, the probability of not detecting the sequence equals approximately $22P^2$, and the probability for incorrectly detecting a sequence equals approximately 2,7P x 2P/256 x $P^2$ = 2 x $10^{-2}p^4$. A similar four sector long search for at least three mutually correctly located sync marks without any other mislocated ones, the probability of not detecting equals approximately $43P^2$, and the probability of incorrectly detecting equals approximately $10^{-4}$x $P^6$. Other types of search and/or a running check of the sync mark are up to the drive design.

– The sector number location is well known, once sector synchronization has been achieved. Hence, error probabilities for similar checks, as mentioned above on the correct sector number sequence, are somewhat different. Also, because only 32 specific bytes are used as sector numbers, the probability of misdetecting a sector number is 32P/256 = P/8. A three out of four majority vote on the sector number sequence results in a probability of non-detection of approximately $6P^2$ and a probability of incorrectly detecting of approximately 2 x $10^{-5}P^3$. Other check schemes can be easily assessed in a similar way.

– The track address (both MSB and LSB) has some internal protection through the addition of its complement. The doubling up of the LSB complement is related to the limited probability of error correlation in adjacent bytes and allows for somewhat more reliable error checks if so desired. In the following, only random byte errors will be considered. The probability of finding an error in an M/LSB after a check with its complement is 2P, the probability of not detecting an error equals approximately $P^2/128$. A 2 out of 3 majority vote system in consecutive headers results in a probability of not detecting a correct M/LSB of $12P^2$ and a probability of incorrectly detecting a M/LSB of 7 x $10^{-7}p^4$. A 3 out of 4 majority vote system gives probabilities of $24P^2$ and 6 x $10^{-11}p^5$, respectively.

– During seeks, the probability of correctly detecting a track LSB is greatly reduced relative to the disk byte error rate. Preliminary measurements show 2P = 7% for seek velocities lower than 0,15 m/s and 2P = 40% for velocities over 0,15 m/s. Application of the 2 out of 3 majority vote system on detection of the LSB, results in a not detected percentage of 1,4% and an incorrectly detected probability of $10^{-12}$ for low seek velocities (< 0,15 m/s). Even at high seek velocities, using this majority vote system still results in 30% not detected LSB and $10^{-7}$ probability of incorrectly detected LSB.

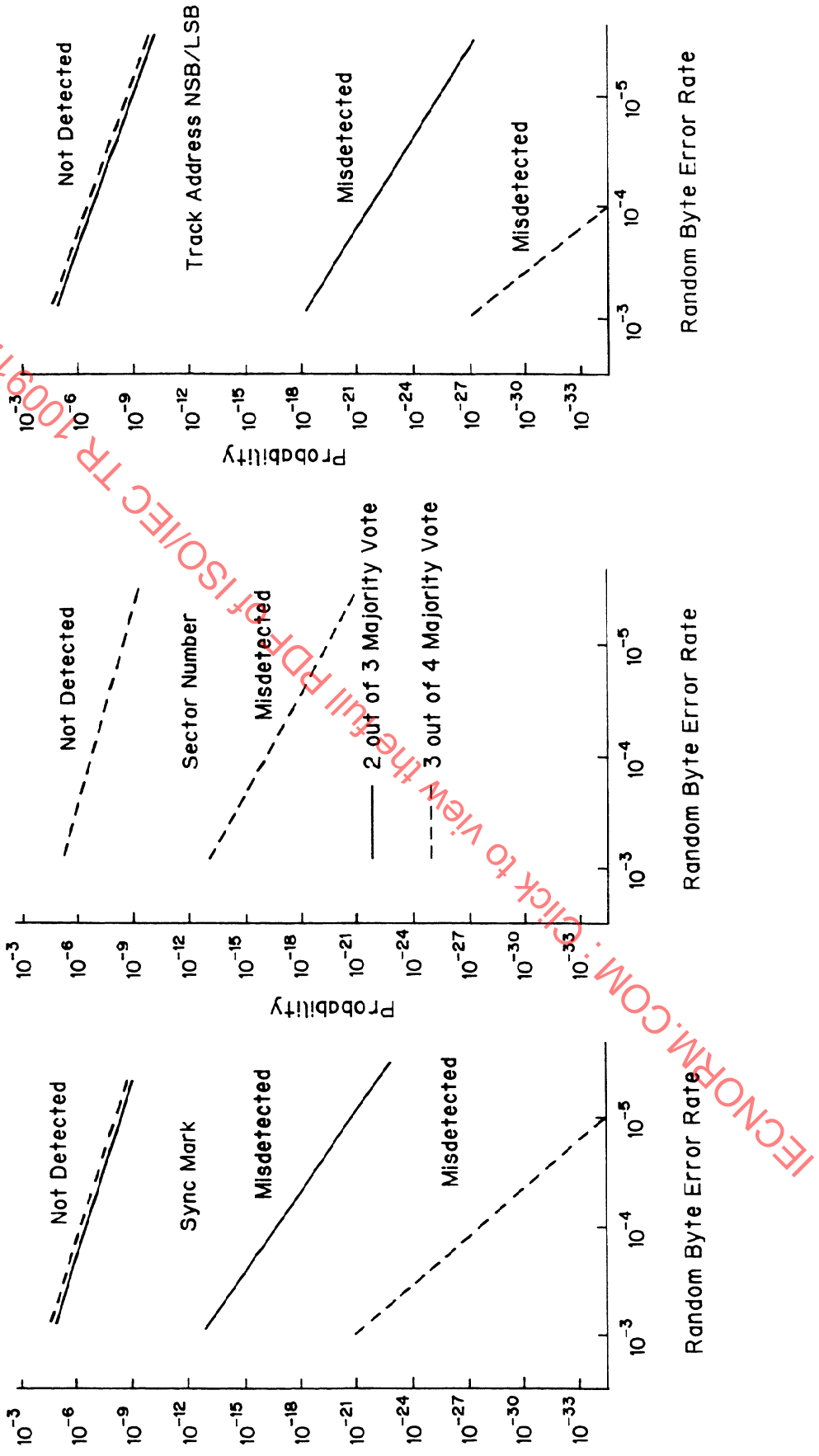



**Figure 31 - Reliability of header information**

## 13 Error detection and correction

**Polynomial**

$$P(x) = X^8 + X^4 + X^3 + X^2 + 1$$

**Error correction code type**

C1: (48, 44) Reed-Solomon code

C2: (14, 12) Reed-Solomon code

Product code (C1 x C2)

### 13.1 Error correction capability

**L-M model**

$$R(x) = [1 + x/L(M-1)]^{-M}$$

R(x) : Probability of a physical error = defect rate ($x \geq d$)

d : physical error length = defect length (bit)

L : mean defect length

M : arbitrary fitting parameter

An example of defect rate vs. defect length is shown in figure 32. The applied values to the parameters L and M are as follows:

L = 3,1 M = 1,65

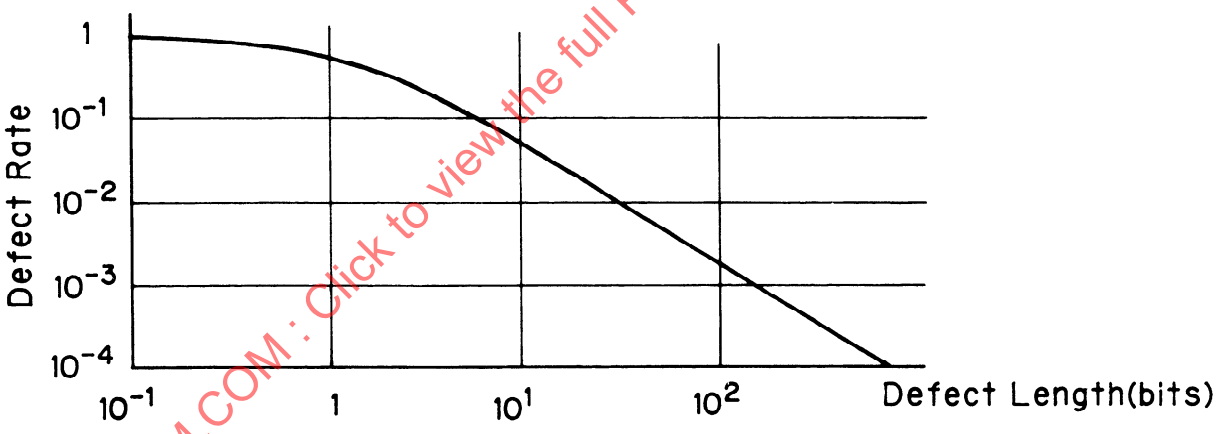



**Figure 32 - Defect rate vs defect length (bits) in L-M model**



**Derivation of Bytes Error Rate from L-M Model**

Definitions: P : error event rate/bit,

$P_{NS}$ : probability of N (or more than N) successive error bytes,

a : error propagation length (bits).

$$P_S = P_{1S} = 8P + \int P \cdot R(x)dx + aP$$

$$P_{2S} = \int P \cdot R(x)dx + aP$$

....

.

.

$$P_{NS} = \int P \cdot R\{x + 8(N - 2) - a\}dx$$

(N≥3)

The following are the results applying the L-M model to the above formulas.

$P_S = (8 + L + a)P$

$P_{2S} = (L + a)P$

.

.

.

$P_{NS} = LP\{1 + [8(N - 2) - a]/[L(M - 1)]\}^{-M+1}$

In 4/15 modulation, a = 0

**Derivation of Error Correctability (Error event rate/sector)**

a) Random errors

$${}_{14}C_3 \times 3 \times {}_{48}C_4 \times 44 \times {}_4C_2 \times P_S{}^{10} = 5.61 \times 10^{10} P_S{}^{10}$$

The assumed error pattern is shown in figure 33.

b) Medium (short) burst errors.

$${}_{14}C_3 \times 3 \times 44 \times {}_4C_2 \times P_{4S}{}^2 \times P_{5S} = 1092 \times P_{4S}{}^2 \times P_{5S}$$

The assumed error pattern is shown in figure 34.

c) Burst errors

$$(48 - 6 - 2) \times 12 \times P_{93S} = 480 \times P_{93S} (+ 12 \times P_{94S} + \cdots)$$



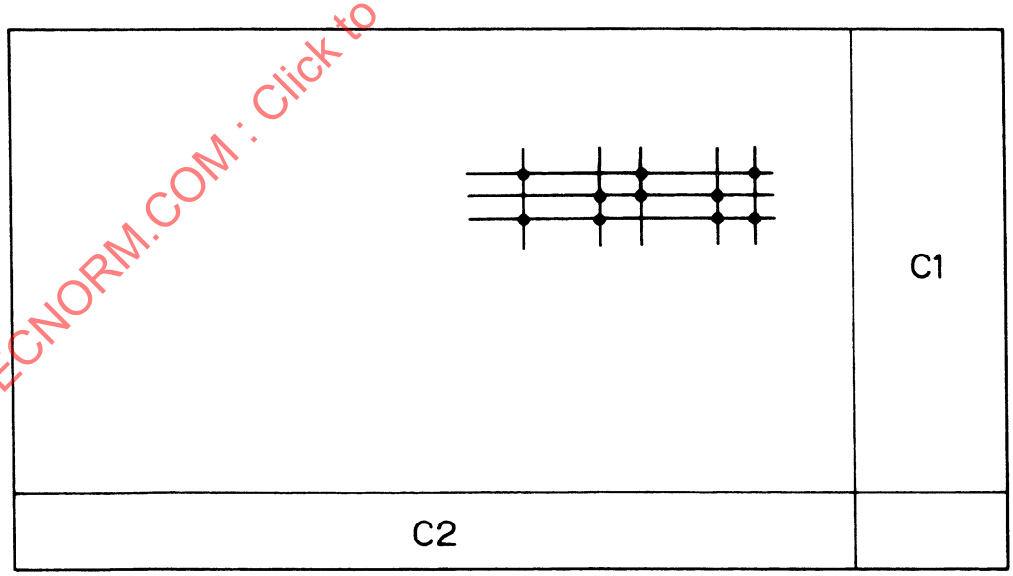



**Figure 33 - Assumed pattern of random errors**

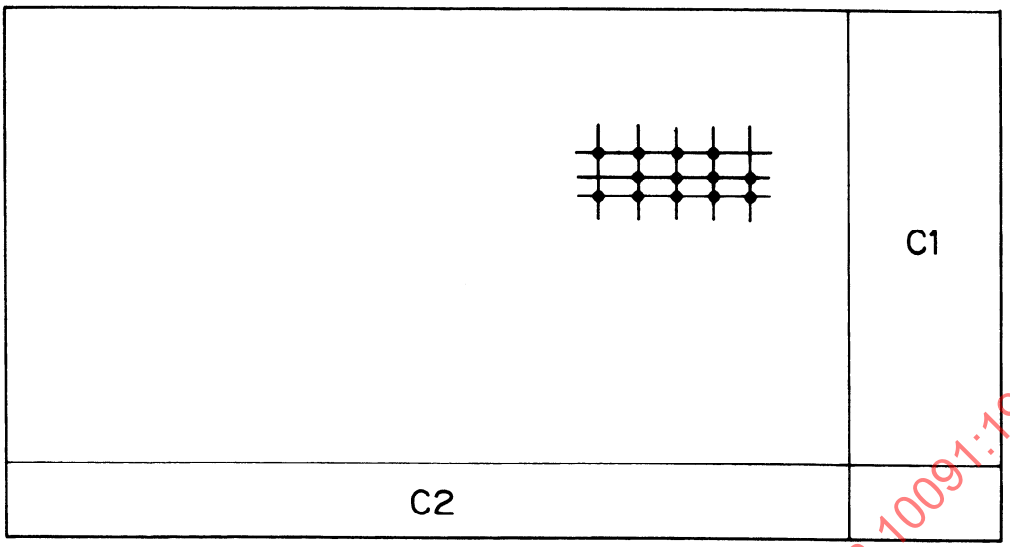



**Figure 34 - Assumed pattern of short burst errors**

Then, the sector error rate is expressed as follows:

$$\text{Sector error rate} = 5{,}61 \times 10^{10} \times P_S{}^{10} + 1{,}09 \times 10^{3} \times P_{4S}{}^{2} \times P_{5S} + 4{,}80 \times 10^{2} \times P_{93S} + 12 \times \prod_{i=94}^{99} P_{is} + 11 \times \prod_{i=100}^{101} P_{is}$$ (see figure 35)

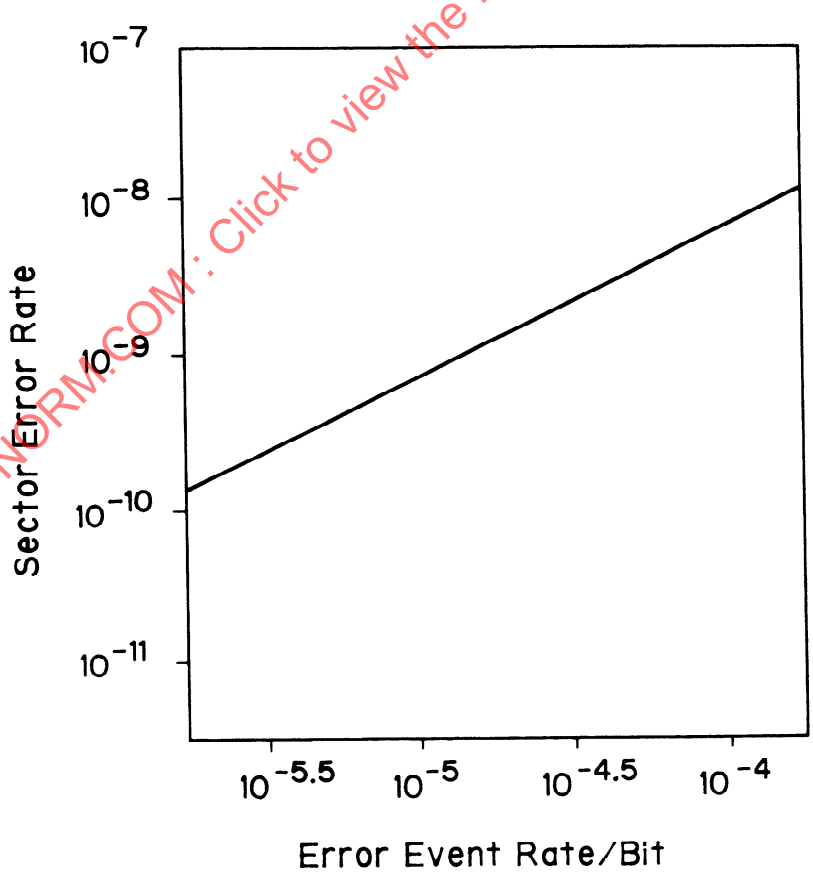



**Figure 35 - Sector error rate plotted against error event rate/bit**

### 13.2 Estimated chip size of the LSI for EDAC

Estimated size of the EDAC LSI will be approximately 5000 gates. The functions of the LSI are generating C1, C2 parity codes and also check codes (CRC). Errors can be corrected through single path of C1, C2 series and data can also be checked by the check code.

### 13.3 Correction time

The correction time of the EDAC LSI will be <230 µsec per sector under the following conditions.

C1 : 2 Bytes correction or 4 bytes erasure correction,

C2 : 1 Byte correction or 2 bytes erasure correction,

(single series of C1 and C2),

LSI clock : 6 MHz.

## 14 4/15 Modulation and differential detection

### 14.1 Modulation coding

**Key features of the modulation coding**

The 4/15 code is d.c. free. The power density spectrum of the code is zero at frequency zero. The code allows demodulation by differential detection. This demodulation technique has a performance that approaches maximum likelihood decoding. The details are explained below. The code also has a null in its power density spectrum at the clock frequency. This allows for clock generation by means of a buried in-track clock frequency, as well as other more conventional clock generation techniques.

The code requires only 4 written marks per byte.

The code has an equal number of marks (holes in an ablative recording material) written on odd (2) and on even (2) positions in a code word.

The code adheres to the "distance = 2" rule. This means that between strings of consecutive marks (nodes) at least two positions are left open. This rule minimizes intersymbol interference and results in a higher effective bit density. In order to satisfy this rule for the concatenation of code words, the last position in the code word is always empty.

**Recording code**

The 4/15 recording code maps 1 byte of user data onto 15 channel bits using 4 written marks. The symbols in the 4/15 code are constructed in such a way that the most and least significant 4 bits of a byte of user data are generated independent from each other, except when one of these 4-bit bytes is equal to F (hexadecimal notation). Tables 6 and 7 show the 4/15 symbols for the user data.

There are 30 combinations which fulfill the modulation rules reserved for possible special functions. The 4/15 symbols for special functions are shown in table 8.

**Table 6 - 4/15 recorded symbols for the least significant 4 bits of a user data byte**

| LSB | Mark positions | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| (0) | x | | | | x | | | | | | | | | | |
| (1) | x | | | | | | x | | | | | | | | |
| (2) | x | | | | | | | | x | | | | | | |
| (3) | x | | | | | | | | | | x | | | | |
| (4) | x | | | | | | | | | | | | x | | |
| (5) | | | x | | | | x | | | | | | | | |
| (6) | | | x | | | | | | x | | | | | | |
| (7) | | | x | | | | | | | | x | | | | |
| (8) | | | x | | | | | | | | | | x | | |
| (9) | | | | | x | | | | x | | | | | | |
| (A) | | | | | x | | | | | | x | | | | |
| (B) | | | | | x | | | | | | | | x | | |
| (C) | | | | | | | x | | | | x | | | | |
| (D) | | | | | | | x | | | | | | x | | |
| (E) | | | | | | | | | x | | | | x | | |

| MSB | LSB | Mark positions | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| (0) | (F) | x | x | x | | | x | | | | | | | | | |
| (1) | (F) | x | x | x | | | | | x | | | | | | | |
| (2) | (F) | x | x | x | | | | | | | x | | | | | |
| (3) | (F) | x | x | x | | | | | | | | | x | | | |
| (4) | (F) | x | x | x | | | | | | | | | | | x | |
| (5) | (F) | | | x | x | x | | | x | | | | | | | |
| (6) | (F) | | | x | x | x | | | | | x | | | | | |
| (7) | (F) | | | x | x | x | | | | | | | x | | | |
| (8) | (F) | | | x | x | x | | | | | | | | | x | |
| (9) | (F) | | | | | x | x | x | | | x | | | | | |
| (A) | (F) | | | | | x | x | x | | | | | x | | | |
| (B) | (F) | | | | | x | x | x | | | | | | | x | |
| (C) | (F) | | | | | | | x | x | x | | | x | | | |
| (D) | (F) | | | | | | | x | x | x | | | | | x | |
| (E) | (F) | | | | | | | | | x | x | x | | | x | |
| (F) | (F) | | | | | | | | x | x | x | | | x | | |

**Table 7 - 4/15 recorded symbols for the most significant 4 bits of a user data byte**

| MSB | Mark positions | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| (0) | | x | | | | x | | | | | | | | | |
| (1) | | x | | | | | | x | | | | | | | |
| (2) | | x | | | | | | | | x | | | | | |
| (3) | | x | | | | | | | | | | x | | | |
| (4) | | x | | | | | | | | | | | | x | |
| (5) | | | | x | | | | x | | | | | | | |
| (6) | | | | x | | | | | | x | | | | | |
| (7) | | | | x | | | | | | | | x | | | |
| (8) | | | | x | | | | | | | | | | x | |
| (9) | | | | | | x | | | | x | | | | | |
| (A) | | | | | | x | | | | | | x | | | |
| (B) | | | | | | x | | | | | | | | x | |
| (C) | | | | | | | | x | | | | x | | | |
| (D) | | | | | | | | x | | | | | | x | |
| (E) | | | | | | | | | | x | | | | x | |

| MSB | LSB | Mark positions | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| (F) | (0) | x | | | x | x | x | | | | | | | | | |
| (F) | (1) | x | | | | | x | x | x | | | | | | | |
| (F) | (2) | x | | | | | | | x | x | x | | | | | |
| (F) | (3) | x | | | | | | | | | x | x | x | | | |
| (F) | (4) | x | | | | | | | | | | | x | x | x | |
| (F) | (5) | | | x | | | x | x | x | | | | | | | |
| (F) | (6) | | | x | | | | | x | x | x | | | | | |
| (F) | (7) | | | x | | | | | | | x | x | x | | | |
| (F) | (8) | | | x | | | | | | | | | x | x | x | |
| (F) | (9) | | | | | x | | | x | x | x | | | | | |
| (F) | (A) | | | | | x | | | | | x | x | x | | | |
| (F) | (B) | | | | | x | | | | | | | x | x | x | |
| (F) | (C) | | | | | | | x | | | x | x | x | | | |
| (F) | (D) | | | | | | | x | | | | | x | x | x | |
| (F) | (E) | | | | | | | | | x | | | x | x | x | |
| (F) | (F) | | | | | | | | x | x | x | | | x | | |

**Table 8 - 4/15 recorded symbols reserved for special functions**

| FLAG | MSB | LSB | Mark positions | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| M | (0) | (F) | | x | | | x | x | x | | | | | | | | |
| M | (1) | (F) | | x | | | | | x | x | x | | | | | | |
| M | (2) | (F) | | x | | | | | | | x | x | x | | | | |
| M | (3) | (F) | | x | | | | | | | | | x | x | x | | |
| M | (5) | (F) | | | | x | | | x | x | x | | | | | | |
| M | (6) | (F) | | | | x | | | | | x | x | x | | | | |
| M | (7) | (F) | | | | x | | | | | | | x | x | x | | |
| M | (9) | (F) | | | | | | x | | | x | x | x | | | | |
| M | (A) | (F) | | | | | | x | | | | | x | x | x | | |
| M | (C) | (F) | | | | | | | | x | | | x | x | x | | |
| M | (F) | (5) | | x | x | x | | | x | | | | | | | | |
| M | (F) | (6) | | x | x | x | | | | | x | | | | | | |
| M | (F) | (7) | | x | x | x | | | | | | | x | | | | |
| M | (F) | (8) | | x | x | x | | | | | | | | | x | | |
| M | (F) | (9) | | | | x | x | x | | | x | | | | | | |
| M | (F) | (A) | | | | x | x | x | | | | | x | | | | |
| M | (F) | (B) | | | | x | x | x | | | | | | | x | | |
| M | (F) | (C) | | | | | | x | x | x | | | x | | | | |
| M | (F) | (D) | | | | | | x | x | x | | | | | x | | |
| M | (0) | (0) | x | x | x | x | | | | | | | | | | | |
| M | (1) | (1) | | x | x | x | x | | | | | | | | | | |
| M | (2) | (2) | | | x | x | x | x | | | | | | | | | |
| M | (3) | (3) | | | | x | x | x | x | | | | | | | | |
| M | (4) | (4) | | | | | x | x | x | x | | | | | | | |
| M | (5) | (5) | | | | | | x | x | x | x | | | | | | |
| M | (6) | (6) | | | | | | | x | x | x | x | | | | | |
| M | (7) | (7) | | | | | | | | x | x | x | x | | | | |
| M | (8) | (8) | | | | | | | | | x | x | x | x | | | |
| M | (9) | (9) | | | | | | | | | | x | x | x | x | | |
| M | (A) | (A) | | | | | | | | | | | x | x | x | x | |



## 14.2 Differential detection

### Introduction

There are basically two classes of techniques used in the decoding of recorded information: threshold detection and differential detection. The 4/15 modulation rules allows the use of differential detection. In this section, we will describe the basic principles of the differential detection method, and clarify some of its advantages.

### Channel properties

First, we would like to emphasize the differences in channel properties of recordable media and read only media. For example, the compact disk is a read only system. The information is read with a constant linear velocity (CLV). This limits the variation in the read-out waveform to a minimum. Furthermore, the CD-channel is a symmetrical channel, i.e. pits and lands are on the average of equal length. Figure 36 shows typical waveforms.

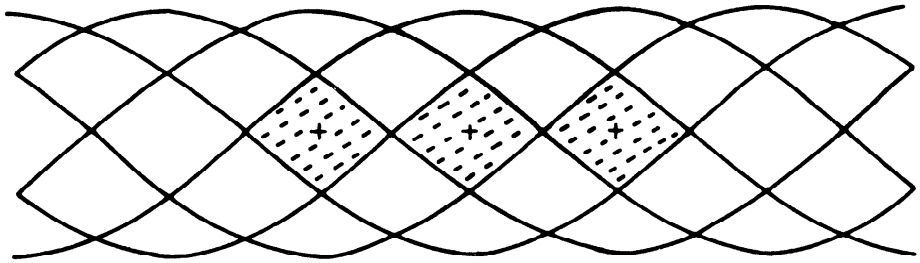


**Figure 36 - Typical waveforms of the CD-channel**

In contrast, in recordable systems, a constant angular velocity (CAV) is required in order to achieve low access times. This means a radius-dependent effect size, and a radius-dependent read-out waveform. Also, the channel is mostly asymmetrical (circular effect which overlaps the adjacent blank location), leading to an asymmetrical read-out waveform.

Moreover, the data is often recorded in between prerecorded (stamped) headers which may have different channel characteristics, and consequently, different read-out waveform compared to the written data. These headers are preferably digitized by the same circuitry.

Additional variations are also introduced by the requirements of data interchangeability. The drive shall be able to read different media where the optical mark may be represented by a hole, a pit, a bubble, or any of a number of possible alternate effects.

These variations and asymmetries of the digital optical recording channel greatly complicate the digitizing and also the clock recovery process.

**Principles of threshold detection**

Threshold detection is a commonly used digitizing technique in telecommunication and magnetic recording. It is also used in CD drives. Figure 37 shows the basic approach.

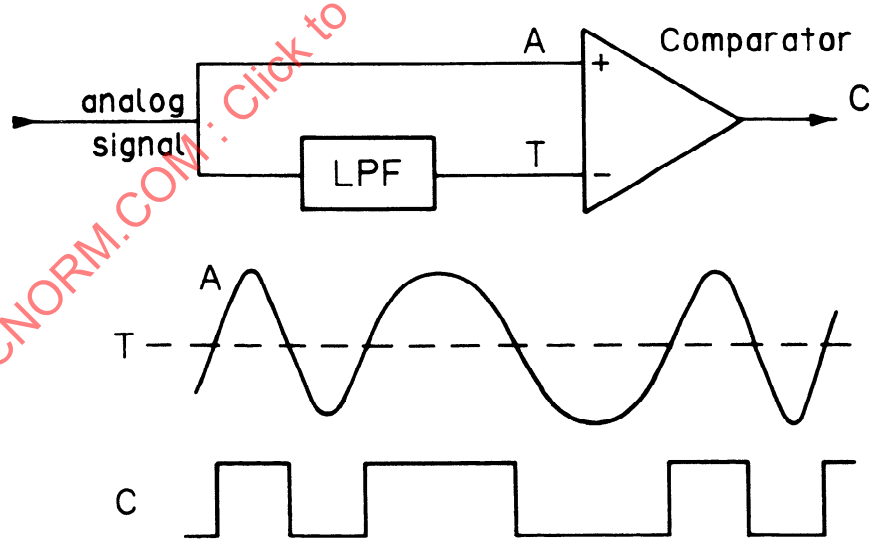



**Figure 37 - Schematic diagram of simple threshold detection**

This straight-forward system works very well with symmetrical channels like those in a CD drive. The time constant of the lowpass filter can be chosen such that the threshold tracks relatively slow d.c. - variations in the input signal. Clock information is usually retrieved from the edges in signal C.

With asymmetrical, but stable, channels (e.g. ablative recording with CLV) it becomes a little more complex. Figure 38 shows how — with two peak detectors — one can derive a good threshold and achieve a reliable digitizer.

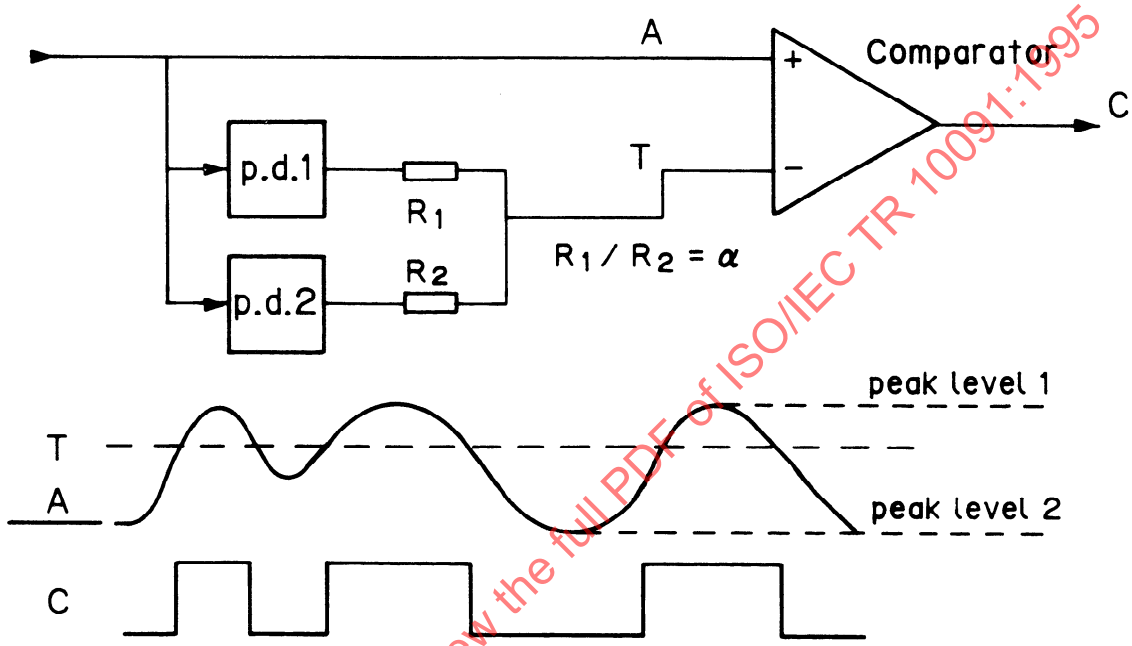



**Figure 38 - Schematic diagram of improved threshold detection**

If we project all channel locations on top of each another, the picture of figure 39 appears. Here we see a so-called EYE-PATTERN. The dashed area indicates the amplitude and phase margin.

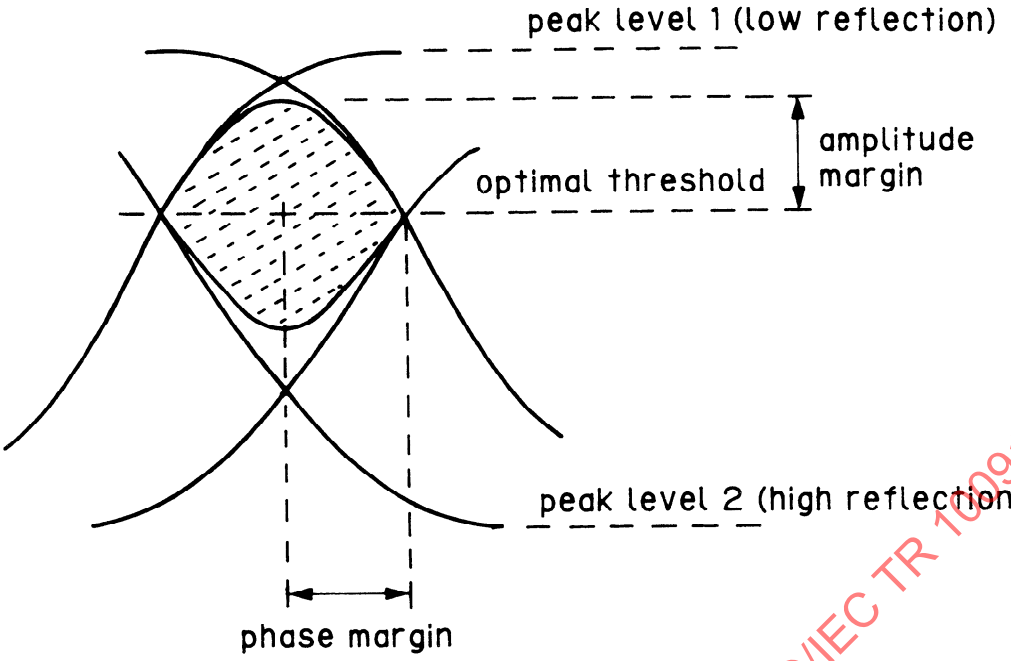



**Figure 39 - The amplitude and phase margin of the eye pattern**

For asymmetrical channels with variable characteristics, such as in CAV-recordable systems, the approach of figure 38 is insufficient since the eye-pattern varies with radius as is shown in figure 40.

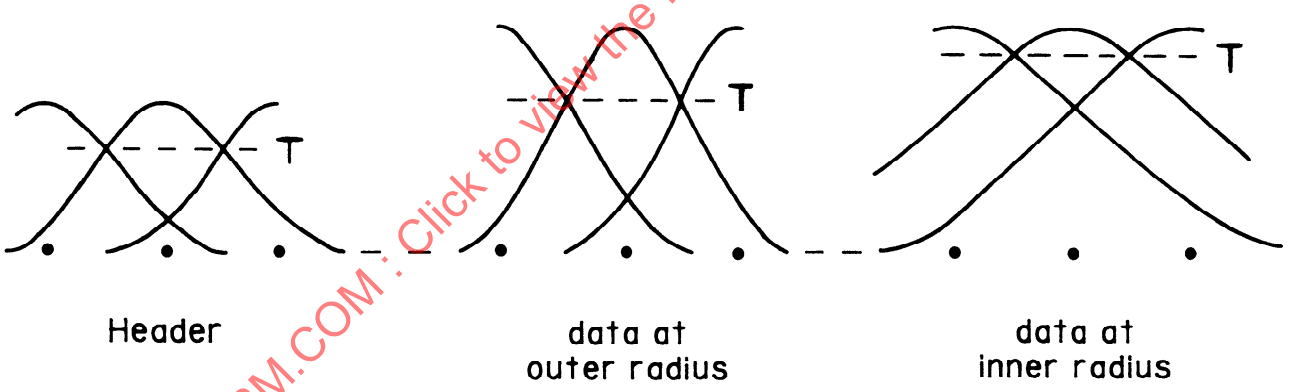



**Figure 40 - Variations of eye patterns with locations of information pit**

So we need an adjustable threshold for the different radii. The use of analog/digital - and digital/analog converters, controlled by a microprocessor may be a good solution, provided that the waveform for each radius is reproducible under all conditions.

**Principles of differential detection**

Differential detection can be applied to any block-code with a fixed number of marks per block (m out of 1). Basically, differential detection determines the locations of the marks by comparing the signal amplitudes of all locations within each block. The m locations with the most extreme amplitudes are assumed to be the mark locations. These mark locations are then converted into data words. Therefore, characteristics of the differential detection are:

- It does not required an external reference from the past. In fact, there is no threshold at all.
- It automatically optimizes the amplitude margin.

This is illustrated in figure 41.

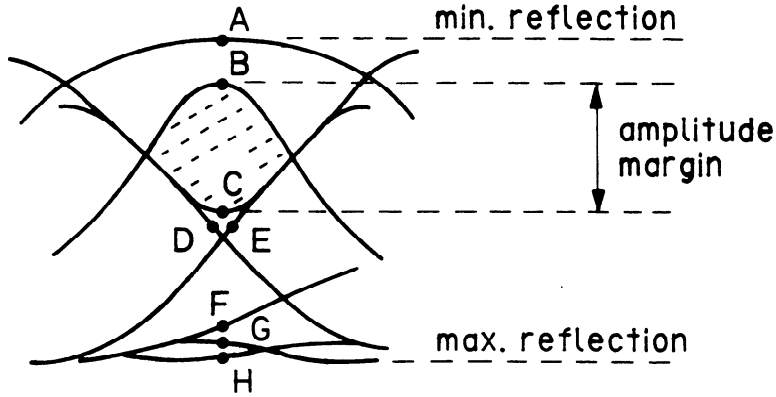



**Figure 41 - Amplitude margin of differential detection**

The samples A through H are compared with each other, after which A and B are found to be the two extremes. This may be maximum or minimum, depending on the polarity of the marks. The distance B-C is the worst-case amplitude margin, but it is still about twice as high as the threshold detection margin. The results is that this digitizer is very insensitive to reflection variations and effect-amplitude variations, and, it increases the amplitude margin by a factor of two. The performance of differential detection approaches the theoretical optimum achievable by maximum likelihood decoding.

**Some detection problems**

Figure 42 shows a distortion that has been observed occasionally. This distortion can be caused, for example, by dust particles on the entrance surface of the media.

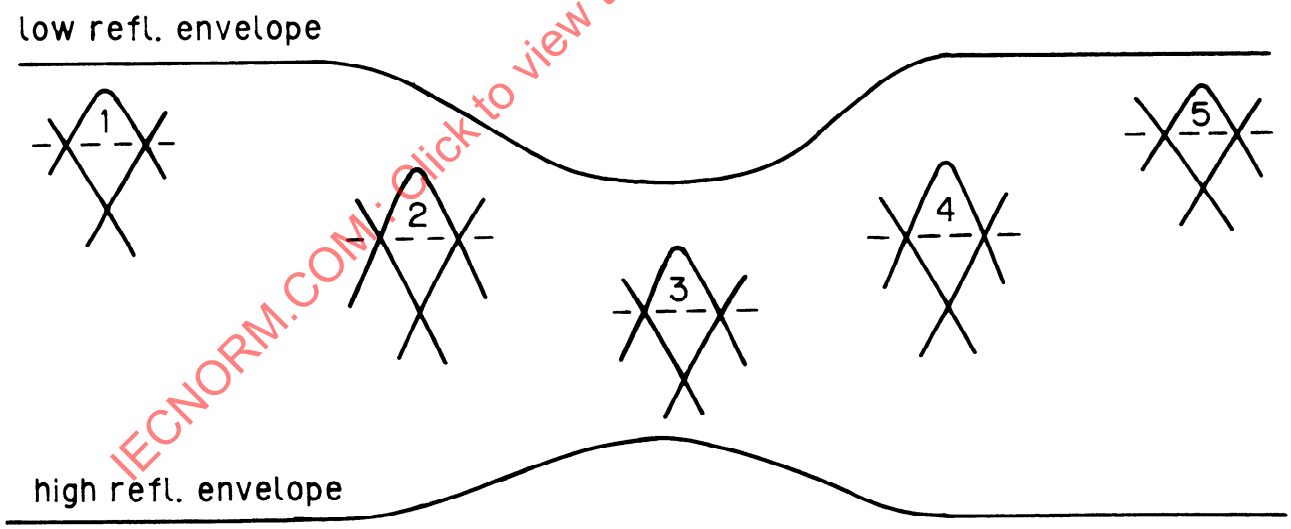



**Figure 42 - Effects of distorted signals on detection capability**

Locally the reflection decreases while the required write power increases. The holes (or other effects) become smaller and the detection eye changes from 1 through 5.

For differential detection this presents no problem. The extremes are always found as long as they exceed the noise peaks.

With threshold detection it is, in principle, possible to let the threshold track the peak levels within a certain bandwidth, but the problem here is that the optimum threshold for 1 is at 80%, optimum threshold for 2 is at 65% and optimum threshold for 3 is 50% of the peak-peak value. In fact the optimum threshold is very unpredictable and data errors are very likely.

Another problem for threshold detection is the transition from blank sectors to recorded sectors. How do we set the threshold to start with?

The first thought is probably to derive a threshold from the sector headers or servo areas. But the amplitude relation of stamped and recorded information is seldom well defined and for some media may even be of opposite polarity.

And, last but not least, there is the problem of birefringence in plastic substrates. Birefringence variations cause considerable variations in the read signal, with serious consequences for the derivation of a suitable threshold. Differential detection is substantially less sensitive to these variations.

**Compatibility towards a variety of sensitive layers**

The future will probably bring a large variety of sensitive layers, including different kinds of rewritable. It is desirable to develop drives which can be adapted to accept many different kinds of media, perhaps with some programmable adjustments. The number of adjustments, however, should be limited to a minimum. For reading the data, differential detection offers a solution with only one adjustment: the polarity of the read signal.

However, with threshold detection the drive shall adjust, not only the polarity, but also the threshold percentage for each different sensitive layer, and, in CAV applications, also the threshold percentage for various radii. It may even be necessary to adjust the threshold for stamped information separately. The question then arises: How are we going to deliver this information to the drive?

Even if such a wide compatibility is not required, it is still an advantage if we do not have to go through a redevelopment of the read-channel for each new media technology like phase-change or magneto-optic.

Differential detection maintains its advantages independent on layer or substrate.

**Advantages of differential detection**

Differential detection is a very flexible digitizer, which may be applied to a certain class of block codes. Differential detection is a highly preferred digitizer if compatibility to various channel characteristics (CLV/CAV, ablative/non-ablative/rewritable) is desired.

Differential detection offers compatibility with a minimum amount of adjustments regarding reading: one polarity switch.

Differential detection increases the amplitude-margin by a factor of two over threshold detection.

## 14.3 Implementation

A number of approaches are possible.

Figure 43 shows a straight forward approach. The analog signal is delayed through 6 equal delay units (these may be delay-lines, bucket-bridges, sample & holds etc.). The delay-time is equal to the duration of two channel-bits. At some point in time, the 7 odd locations of one code word are available at the inputs of the voltage comparators. At that instant, the decoder (conversion table) converts the compare results to least significant 4 bits. One channel-bit period later, the 4 most significant data bits are derived from the 7 even locations in the same way. There is one special case: if the least significant 4 bits were decoded as E, and the even extremes are at location 8 and 10, then the data byte should be hex 'FF'. Note that location 15 is completely ignored.

This approach allows for very high data rates since no "decision feedback" is required. The drawback of this approach is the large number of delay-units and comparators.

A second approach does the comparisons on the fly, and only stores those signal values, together with their location numbers, which may eventually be the extremes. This requires some decision feedback logic, but uses significantly fewer storage devices and comparators.

Figure 44 shows the block diagram. The fast analog to digital converter on the left of the diagram converts the analog signal into binary words (6 bit words result in a resolution of 1.6%), synchronized with the channel bit locations. From here, the odd and even samples are separated and processed in two parallel channels (upper and lower part of the block diagram). The common location counter counts the locations within the code word.

As an example, let us take the read signal of figure 45. First the odd channel bits:

The amplitude of location 1 is always stored in register L, that of location 3, always in register M. The two location registers on the right now contain a 1 and a 3. Unit S compares register L to register M and passes the lowest value to comparator Z. In this case, the amplitude of location 1 is the lowest, so register L appears at input B of comparator Z. Next, the amplitude of location 5 is applied to input A of comparator Z. As this new value is higher than the location 1 value, which was stored in register L, the content of register L is now replaced by the value of location 5. At the same time, the corresponding location-register is updated and now contains a '5' instead of '1'.

Since the value of location 3 in register M is still higher than the value of location 5 in register L, unit S passes register L to comparator Z. Next the amplitude of location 7 appears at input A of comparator Z. As this value is slightly lower than the value at input B (coming from register L), no replacement and update will take place. The same applies to locations 9 and 11.

Finally, the amplitude of location 13 is compared to the amplitude of location 5. This time, the new value is higher and register L is replaced with the new value from location 13. At the same time, the corresponding location register is updated. Now the location registers contain 13 and 3.

A simple conversion table translates this information to the 4 least significant bits of a byte. According to table 5, effect positions of 3 and 13 result in a least significant 4 bits of hex '8'.

In the same way, the even locations are processed. The two highest values are found at location 6 and 12, which according to table 6, results in a most significant 4 bits of hex 'A'.

This approach does all signal processing digitally (apart from the A/D converter) thus, it is very suitable for integration into a gate array and may be easily combined with other drive control logic.

An alternative without A/D converter is shown in figure 46.

Signal processing is done in a similar way as described above, but amplitude storage is now done by means of Sample & Hold's and analog voltage comparators are used to determine the extremes.

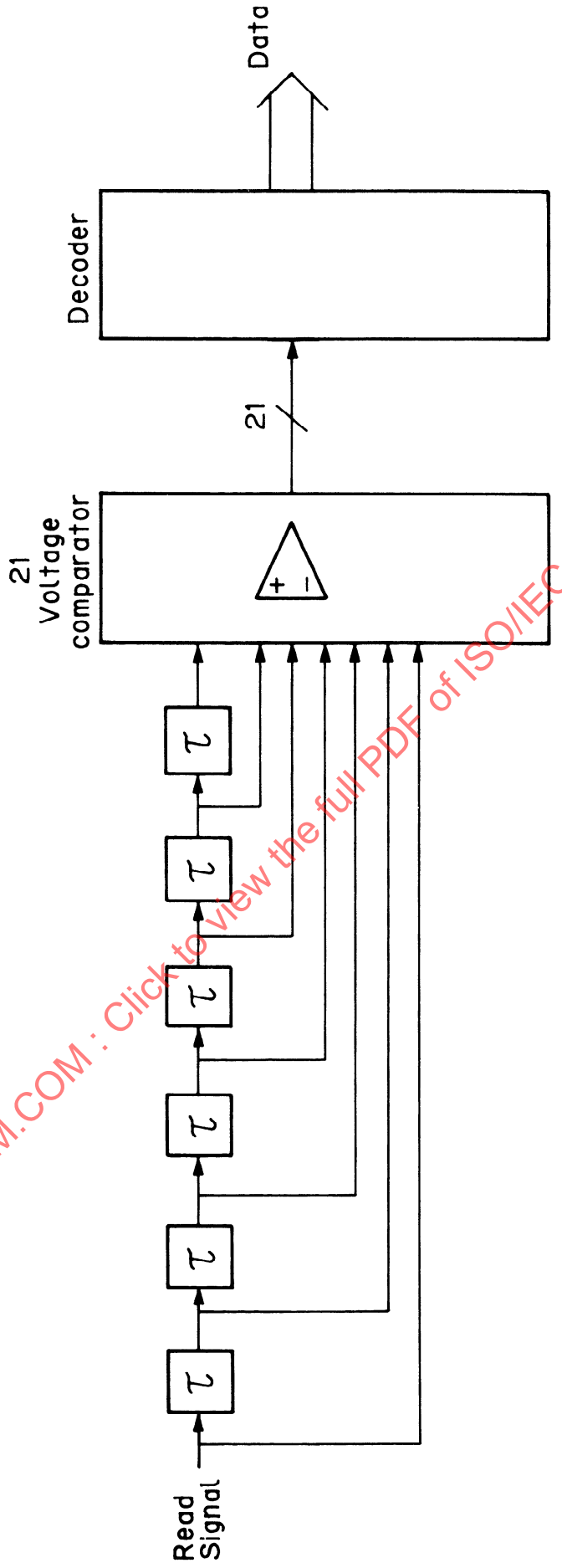





**Figure 43 - The first example of 4/15 decoder, a straight forward approach**

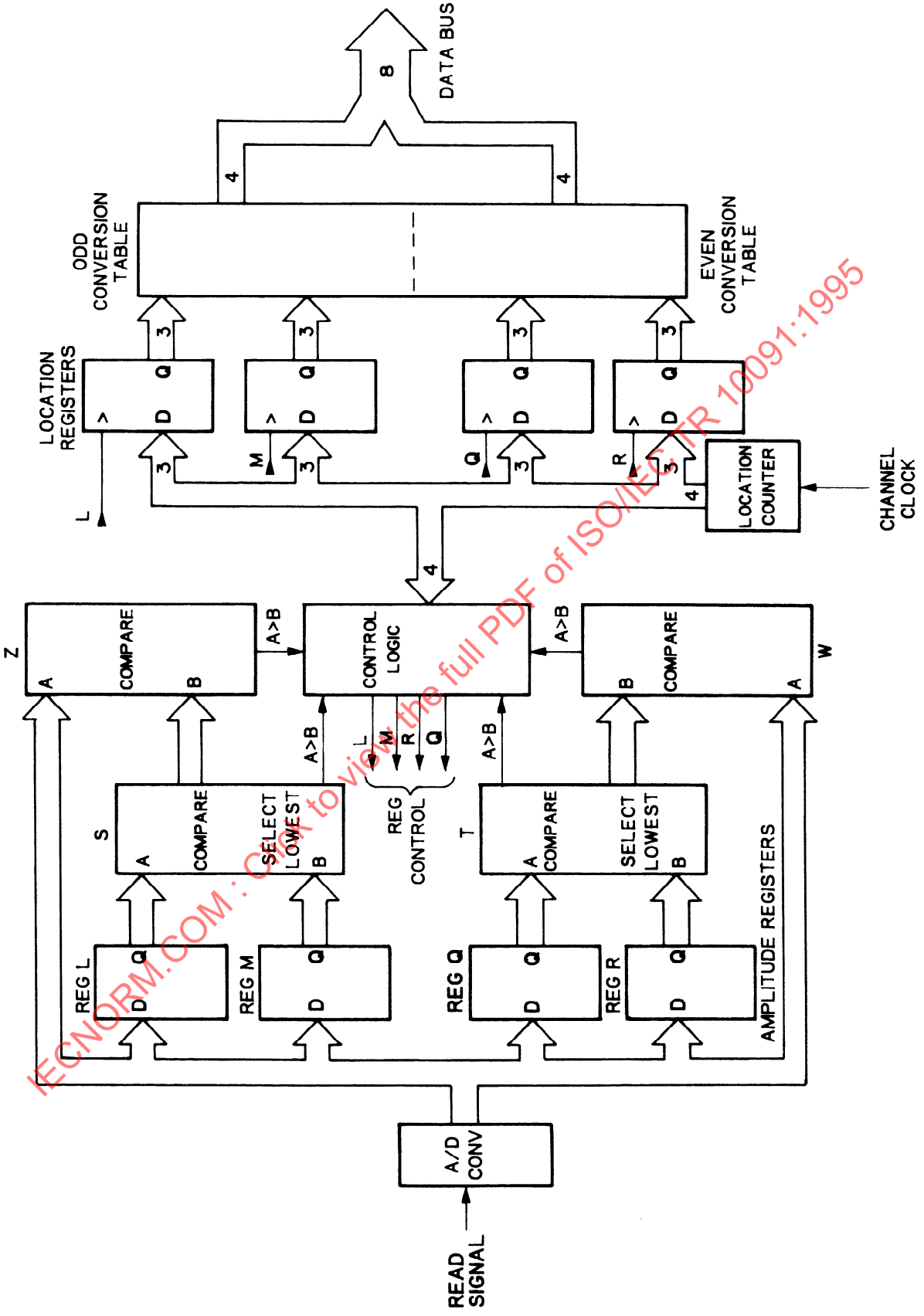





**Figure 44 - The second example of 4/15 decoder**