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**Telecommunications and exchange  
between information technology  
systems — Requirements for local and  
metropolitan area networks —**

**Part 3:  
Standard for Ethernet**

**AMENDMENT 2: Physical layer and  
management parameters for power over  
Ethernet over 4 pairs**

*Télécommunications et échange entre systèmes informatiques —  
Exigences pour les réseaux locaux et métropolitains —*

*Partie 3: Norme pour Ethernet*

*AMENDEMENT 2: Couche physique et paramètres de gestion pour la  
puissance par ethernet sur 4 paires*





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# **IEEE Standard for Ethernet**

## **Amendment 2: Physical Layer and Management Parameters for Power over Ethernet over 4 Pairs**

Sponsor

**LAN/MAN Standards Committee  
of the  
IEEE Computer Society**

Approved 27 September 2018

**IEEE-SA Standards Board**

**Abstract:** The maximum Powered Device (PD) power available is increased by this amendment to IEEE Std 802.3-2018 by utilizing all four pairs in the specified structured wiring plant. This represents a substantial change to the capabilities of Ethernet with standardized power. The power classification information exchanged during negotiation is extended to allow meaningful power management capability. These enhancements solve the problem of higher power and more efficient standardized Power over Ethernet (PoE) delivery systems.

**Keywords:** amendment, DTE power via MDI, Ethernet, IEEE 802.3™, IEEE 802.3bt™, PoE, Power over Ethernet

*This standard is dedicated to the memory  
of our friend and colleague Martin Patoka.*

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## Introduction

This introduction is not part of IEEE Std 802.3bt-2018, IEEE Standard for Ethernet—Amendment 2: Physical Layer and Management Parameters for Power over Ethernet over 4 Pairs.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of publication for IEEE Std 802.3bt-2018, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines

services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

#### IEEE Std 802.3cb™-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

#### IEEE Std 802.3bt-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

A companion document, IEEE Std 802.3.1, describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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# IEEE Standard for Ethernet

## Amendment 2: Physical Layer and Management Parameters for Power over Ethernet over 4 Pairs

[This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018.]

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in **bold italic**. Four editing instructions are used: change, delete, insert, and replace. **Change** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). **Delete** removes existing material. **Insert** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. **Replace** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.<sup>1</sup>

<sup>1</sup> Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

## 1. Introduction

### 1.3 Normative references

*Insert the following reference into 1.3 in alphanumeric order:*

ANSI/TIA-568.0-D, Generic Telecommunications Cabling for Customer Premises.<sup>2</sup>

### 1.4 Definitions

*Insert the following new term and definition, 1.4.139a, after 1.4.139 “agile device”:*

**1.4.139a ampacity:** The maximum current, in ampere, that a conductor can carry continuously under the conditions of use without exceeding its temperature rating.

*Insert the following new term and definition, 1.4.236a, after 1.4.236 “dual duplex”:*

**1.4.236a dual-signature PD:** A PD that has independent detection signatures, class signatures, and maintain power signatures on each pairset. (See IEEE Std 802.3, Clause 145.)

*Insert the following new term and definition, 1.4.287a, after 1.4.287 “Idle mode”:*

**1.4.287a IEEE 802.3 Power over Ethernet (IEEE 802.3 PoE):** A system consisting of one PSE and one PD that provides power across balanced twisted-pair cabling. (See IEEE Std 802.3, Clause 33 and Clause 145.)

*Change 1.4.308 as follows:*

**1.4.308 link section:** ~~The point-to-point medium connection between the active PSE Power Interface (PI) and the PD PI.~~ The portion of the link between the PSE Power Interface (PI) and the PD PI.

*Insert the following new term and definition, 1.4.374a, after 1.4.374 “page”:*

**1.4.374a pairset:** Either of the two valid 4-conductor connections, Alternative A or Alternative B, as listed in IEEE Std 802.3, 145.2.4. The PSE Alternative A and Alternative B connections are referred to as Mode A and Mode B, respectively, at the PD.

*Change 1.4.407 as follows:*

**1.4.407 Power Sourcing Equipment (PSE):** ~~A DTE or midspan device that provides the power to a single link section. PSEs are defined for use with two different types of balanced twisted pair PHYs. When used with 2 or 4 pair balanced twisted pair (BASE-T) PHYs, (see IEEE Std 802.3, Clause 33), DTE powering is intended to provide a single 10BASE-T, 100BASE-TX, or 1000BASE-T device with a unified interface for both the data it requires and the power to process these data. When used with single balanced twisted pair (BASE-T1) PHYs (see IEEE Std 802.3, Clause 104), DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the data it requires and the power to process these data. A PSE used with balanced single twisted pair PHYs is also referred to as a PoDL PSE. A DTE or midspan device that provides power to a single link section, which may also carry data (for 2 or~~

<sup>2</sup> ANSI/TIA publications are available from the IHS Standards Store (<http://global.ihs.com/>) or from the Telecommunications Industry Association (<http://www.tiaonline.org>).

4 pair systems, see IEEE Std 802.3, Clause 33 and Clause 145; for single pair systems, see IEEE Std 802.3, Clause 104).

*Insert the following new term and definition, 1.4.453a, after 1.4.453 “single-port device”:*

**1.4.453a single-signature PD:** A PD that simultaneously shares the same detection signature, class signature, and maintain power signature between both pairs. (See IEEE Std 802.3, Clause 145.)

*Change 1.4.488, 1.4.489, 1.4.490, and 1.4.491 as follows:*

**1.4.488 Type 1 PD:** A PD that ~~provides a Class 0, 1, 2, or 3 signature requests Class 0 to Class 3 during Physical Layer classification, and that is not a PoDL PD.~~ (See IEEE Std 802.3, Clause 33.)

**1.4.489 Type 1 PSE:** A PSE that ~~supports only a Type 1 PD Class 0 to Class 3 power levels and provides power over 2 pairs.~~ (See IEEE Std 802.3, Clause 33.)

**1.4.490 Type 2 PD:** A PD that ~~provides a Class 4 signature during Physical Layer classification, understands 2-Event classification, and is capable of Data Link Layer classification requests Class 4 during Physical Layer classification, supports 2-Event Classification, and supports Data Link Layer classification.~~ (See IEEE Std 802.3, Clause 33.)

**1.4.491 Type 2 PSE:** A PSE that ~~supports both a Type 1 and a Type 2 PD Class 0 to Class 4 power levels and provides power over 2 pairs.~~ (See IEEE Std 802.3, Clause 33.)

*Insert the following new terms and definitions, 1.4.491a to 1.4.491d, after 1.4.491 “Type 2 PSE”:*

**1.4.491a Type 3 PD:** A single-signature PD that requests Class 1 to Class 6, or a dual-signature PD that requests Class 1 to Class 4 on both Modes, during Physical Layer classification. Additionally, the PD implements Multiple-Event classification and accepts power on both Modes simultaneously. (See IEEE Std 802.3, Clause 145.)

**1.4.491b Type 3 PSE:** A PSE that supports up to Class 6 power levels, supports short MPS, and may support 4-pair power. (See IEEE Std 802.3, Clause 145.)

**1.4.491c Type 4 PD:** A single-signature PD that requests Class 7 or Class 8, or a dual-signature PD that request Class 5 on at least one Mode, during Physical Layer classification. Additionally, the PD implements Multiple-Event classification, is capable of Data Link Layer classification, and accepts power on both Modes simultaneously. (See IEEE Std 802.3, Clause 145.)

**1.4.491d Type 4 PSE:** A PSE that supports at least Class 7 power levels, in addition to lower PD Classes, short MPS, and 4-pair power. (See IEEE Std 802.3, Clause 145.)

*Delete the definitions for  $I_{Port}$  (1.4.294),  $V_{PD}$  (1.4.502), and  $V_{PSE}$  (1.4.503).*

## 1.5 Abbreviations

*Insert the following new abbreviation into 1.5 in alphabetic order:*

PoE      Power over Ethernet

## 14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T including type 10BASE-Te

### 14.3 MAU electrical specifications

#### 14.3.1 MAU-to-MDI interface characteristics

##### 14.3.1.1 Isolation requirement

*Change the first paragraph of 14.3.1.1 as follows:*

A MAU with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

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## 25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

### 25.4 Specific requirements and exceptions

#### 25.4.5 Change to 9.1.7, “Worst case droop of transformer”

*Change 25.4.5 as follows:*

A 100BASE-TX receiver in a Type 2, Type 3, or Type 4 Endpoint PSE or Type 2, Type 3, or Type 4 PD (see Clause 33 and Clause 145) shall meet the requirements of 25.4.7. A 100BASE-TX transmitter in a Type 2 Endpoint PSE or Type 2 PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD; or meet the requirements of 25.4.5.1. A 100BASE-TX transmitter in a Type 3 or Type 4 Endpoint PSE or Type 3 or Type 4 PD shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or meet the requirements of 25.4.5.1.

#### 25.4.6 Replacement of 8.4.1, “UTP isolation requirements”

*Change the first paragraph of 25.4.6 as follows:*

A PMD with a MDI that is a PI (see 33.1.3 and 145.1.3) shall meet the isolation requirements defined in 33.4.1 and 145.4.1.

#### 25.4.7 Addition to 10.1, “Receiver”

*Change 25.4.7 as follows:*

Differential voltage signals generated by a remote transmitter that meets the specifications of Clause 25; passed through a link specified in 25.4.8; and received at the MDI of a 100BASE-TX PMD in a Type 2, Type 3, or Type 4 Endpoint PSE or a Type 2, Type 3, or Type 4 PD shall be translated into one of the PMD\_UNITDATA.indicate messages with a bit error ratio less than  $10^{-9}$  after link reset completion.

**25.6 Protocol implementation conformance statement (PICS) proforma for Clause 25,  
Physical Medium Dependent (PMD) sublayer and baseband medium, type  
100BASE-TX<sup>3</sup>**

**25.6.3 Major capabilities/options**

*Change the title of 25.6.3.1 as follows:*

**25.6.3.1 ~~DTE Power via MDI~~ Power over Ethernet major capabilities/options**

**25.6.4 PICS proforma tables for the Physical Medium Dependent (PMD) sublayer and  
baseband medium, type 100BASE-TX**

*Change the title of 25.6.4.4 as follows:*

**25.6.4.4 ~~DTE Power via MDI~~ Power over Ethernet compliance**

<sup>3</sup> Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

## 30. Management

### 30.2 Managed objects

#### 30.2.2 Overview of managed objects

##### 30.2.2.1 Text description of managed objects

Delete entry “oPD” and its description (“The managed object ... PSE system.”) in 30.2.2.1.

##### 30.2.3 Containment

Replace Figure 30-4 as follows (oPD object deleted):

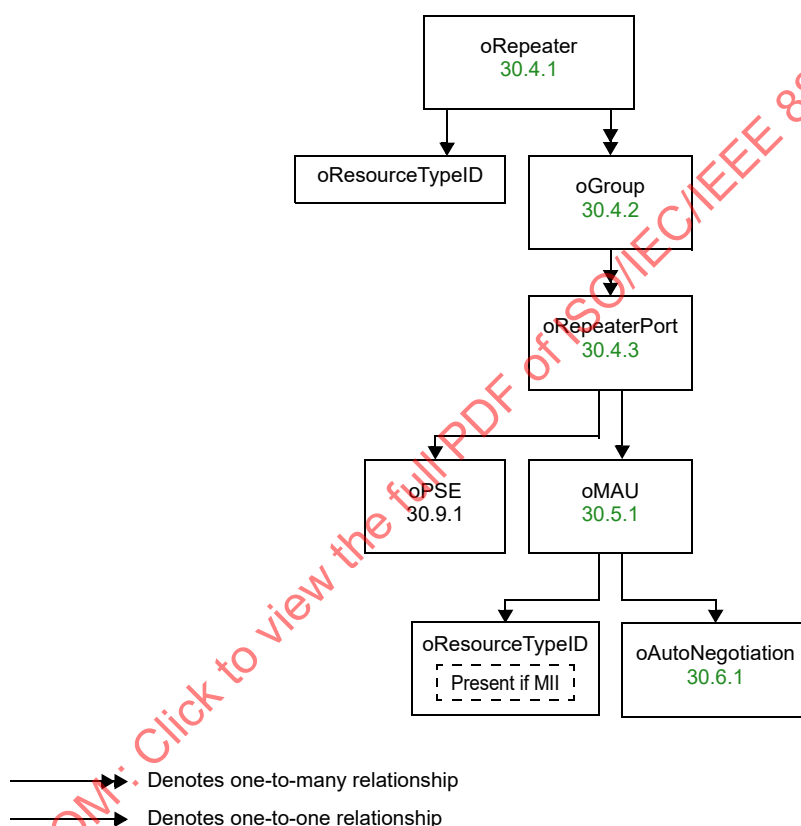


Figure 30-4—Repeater entity relationship diagram

*Change Table 30-4 as follows:*

|                                                 |                  |            |          |                               |                                    |                                     |                              |
|-------------------------------------------------|------------------|------------|----------|-------------------------------|------------------------------------|-------------------------------------|------------------------------|
|                                                 |                  |            |          | PSE Basic Package (mandatory) | PSE Recommended Package (optional) | Midsan Basic Capability (mandatory) | PD-Basic-Package (mandatory) |
| <b>oResourceTypeID managed object</b>           |                  |            |          |                               |                                    |                                     |                              |
| aResourceTypeIDName                             | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| aResourceInfo                                   | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| <b>oMidSpan managed object class (30.10.1)</b>  |                  |            |          |                               |                                    |                                     |                              |
| aMidSpanID                                      | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| aMidSpanPSEGroupCapacity                        | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| aMidSpanPSEGroupMap                             | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| nMidSpanPSEGroupMapChange                       | NOTIFICATION     |            |          |                               | X                                  |                                     |                              |
| <b>oPSEGroup managed object class (30.10.2)</b> |                  |            |          |                               |                                    |                                     |                              |
| aPSEGroupID                                     | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| aPSECapacity                                    | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| aPSEMap                                         | ATTRIBUTE        | GET        |          |                               | X                                  |                                     |                              |
| nPSEMapChange                                   | NOTIFICATION     |            |          |                               | X                                  |                                     |                              |
| <b>oPSE managed object class (30.9.1)</b>       |                  |            |          |                               |                                    |                                     |                              |
| aPSEID                                          | ATTRIBUTE        | GET        | X        |                               |                                    |                                     |                              |
| aPSEAdminState                                  | ATTRIBUTE        | GET        | X        |                               |                                    |                                     |                              |
| aPSEPowerPairsControlAbility                    | ATTRIBUTE        | GET        | X        |                               |                                    |                                     |                              |
| aPSEPowerPairs                                  | ATTRIBUTE        | GET-SET    | X        |                               |                                    |                                     |                              |
| aPSEPowerDetectionStatus                        | ATTRIBUTE        | GET        | X        |                               |                                    |                                     |                              |
| <u>aPSEPowerDetectionStatusA</u>                | <u>ATTRIBUTE</u> | <u>GET</u> | <u>X</u> |                               |                                    |                                     |                              |
| <u>aPSEPowerDetectionStatusB</u>                | <u>ATTRIBUTE</u> | <u>GET</u> | <u>X</u> |                               |                                    |                                     |                              |
| aPSEPowerClassification                         | ATTRIBUTE        | GET        |          | X                             |                                    |                                     |                              |
| <u>aPSEPowerClassificationA</u>                 | <u>ATTRIBUTE</u> | <u>GET</u> |          | <u>X</u>                      |                                    |                                     |                              |
| <u>aPSEPowerClassificationB</u>                 | <u>ATTRIBUTE</u> | <u>GET</u> |          | <u>X</u>                      |                                    |                                     |                              |
| aPSEInvalidSignatureCounter                     | ATTRIBUTE        | GET        |          | X                             |                                    |                                     |                              |
| <u>aPSEInvalidSignatureCounterA</u>             | <u>ATTRIBUTE</u> | <u>GET</u> |          | <u>X</u>                      |                                    |                                     |                              |
| <u>aPSEInvalidSignatureCounterB</u>             | <u>ATTRIBUTE</u> | <u>GET</u> |          | <u>X</u>                      |                                    |                                     |                              |
| aPSEPowerDeniedCounter                          | ATTRIBUTE        | GET        |          | X                             |                                    |                                     |                              |

Table 30–4—DTE Power via MDI capabilities (*continued*)

|                                         |           |     |  | PSE Basic Package (mandatory) | PSE Recommended Package (optional) | Midspan Basic Capability (mandatory) | PD Basic Package (mandatory) |
|-----------------------------------------|-----------|-----|--|-------------------------------|------------------------------------|--------------------------------------|------------------------------|
| aPSEPowerDeniedCounterA                 | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEPowerDeniedCounterB                 | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEOverLoadCounter                     | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEOverLoadCounterA                    | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEOverLoadCounterB                    | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEShortCounter                        | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEMPSAbsentCounter                    | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEMPSAbsentCounterA                   | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEMPSAbsentCounterB                   | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| acPSEAdminControl                       | ACTION    |     |  | X                             |                                    |                                      |                              |
| aPSEActualPower                         | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSEPowerAccuracy                       | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| aPSECumulativeEnergy                    | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |
| <b>PD managed object class (30.9.2)</b> |           |     |  |                               |                                    |                                      |                              |
| aPDID                                   | ATTRIBUTE | GET |  |                               |                                    |                                      | X                            |
| <b>Common Attributes Template</b>       |           |     |  |                               |                                    |                                      |                              |
| aCMCounter                              | ATTRIBUTE | GET |  | X                             |                                    |                                      |                              |

### Table 30-7—LLDP capabilities

[illegible]

Table 30–7—LLDP capabilities (continued)

|                                      |           |     | LLDP Basic Package (mandatory) | LLDP MAC/PHY Configuration/Status Local Package (conditional) | LLDP MAC/PHY Configuration/Status Remote Package (conditional) | LLDP Power via MDI Local Package (conditional) | LLDP Power via MDI Remote Package (conditional) | LLDP Power via MDI Measurements Local Package (conditional) | LLDP Power via MDI Measurements Remote Package (conditional) | LLDP Link Aggregation Local Package (conditional) | LLDP Link Aggregation Remote Package (conditional) | LLDP Maximum Frame Size Local Package (conditional) | LLDP Maximum Frame Size Remote Package (conditional) | LLDP EEE Local Package (optional) | LLDP EEE Remote Package (optional) |
|--------------------------------------|-----------|-----|--------------------------------|---------------------------------------------------------------|----------------------------------------------------------------|------------------------------------------------|-------------------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------|----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|-----------------------------------|------------------------------------|
| aLldpXdot3LocPSEAllocatedPowerValueB | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPSEPoweringStatus       | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPDPoweredStatus         | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerpairsExt           | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPDLoad                  | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerClassExtA          | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerClassExtB          | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerClassExt           | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerTypeExt            | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPD4PID                  | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPSEMaxAvailPower        | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPSEAutoclassSupport     | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocAutoclassCompleted      | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocAutoclassRequest        | ATTRIBUTE | SET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerDownRequest        | ATTRIBUTE | SET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerDownTime           | ATTRIBUTE | SET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasVoltageSupport      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasCurrentSupport      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasPowerSupport        | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasEnergySupport       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasurementSource       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasVoltageRequest      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasCurrentRequest      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasPowerRequest        | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasEnergyRequest       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasVoltageValid        | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasCurrentValid        | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |

Table 30–7—LLDP capabilities (continued)

|                                         |           |     | LLDP Basic Package (mandatory) | LLDP MAC/PHY Configuration/Status Local Package (conditional) | LLDP MAC/PHY Configuration/Status Remote Package (conditional) | LLDP Power via MDI Local Package (conditional) | LLDP Power via MDI Remote Package (conditional) | LLDP Power via MDI Measurements Local Package (conditional) | LLDP Power via MDI Measurements Remote Package (conditional) | LLDP Link Aggregation Local Package (conditional) | LLDP Link Aggregation Remote Package (conditional) | LLDP Maximum Frame Size Local Package (conditional) | LLDP Maximum Frame Size Remote Package (conditional) | LLDP EEE Local Package (optional) | LLDP EEE Remote Package (optional) |
|-----------------------------------------|-----------|-----|--------------------------------|---------------------------------------------------------------|----------------------------------------------------------------|------------------------------------------------|-------------------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------|----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|-----------------------------------|------------------------------------|
| aLldpXdot3LocMeasPowerValid             | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasEnergyValid            | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasVoltageUncertainty     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasCurrentUncertainty     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasPowerUncertainty       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocMeasEnergyUncertainty      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocVoltageMeasurement         | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocCurrentMeasurement         | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPowerMeasurement           | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocEnergyMeasurement          | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocPSEPowerPriceIndex         | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                | X                                               |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocResponseTime               | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocReady                      | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocReducedOperationPowerValue | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3LocTxTwSys                    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocTxTwSysEcho                | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocRxTwSys                    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocRxTwSysEcho                | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocFbTwSys                    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3TxDllReady                    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3RxDllReady                    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocDllEnabled                 | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocTxFw                       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocTxFwEcho                   | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocRxFw                       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |
| aLldpXdot3LocRxFwEcho                   | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      | X                                 |                                    |

**Table 30–7—LLDP capabilities (continued)**

[illegible]

Table 30–7—LLDP capabilities (continued)

|                                            |           |     | LLDP Basic Package (mandatory) | LLDP MAC/PHY Configuration/Status Local Package (conditional) | LLDP MAC/PHY Configuration/Status Remote Package (conditional) | LLDP Power via MDI Local Package (conditional) | LLDP Power via MDI Remote Package (conditional) | LLDP Power via MDI Measurements Local Package (conditional) | LLDP Power via MDI Measurements Remote Package (conditional) | LLDP Link Aggregation Local Package (conditional) | LLDP Link Aggregation Remote Package (conditional) | LLDP Maximum Frame Size Local Package (conditional) | LLDP Maximum Frame Size Remote Package (conditional) | LLDP EEE Local Package (optional) | LLDP EEE Remote Package (optional) |
|--------------------------------------------|-----------|-----|--------------------------------|---------------------------------------------------------------|----------------------------------------------------------------|------------------------------------------------|-------------------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------|----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|-----------------------------------|------------------------------------|
| <u>aLldpXdot3RemPowerClassExtA</u>         | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPowerClassExtB</u>         | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPowerClassExt</u>          | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPowerTypeExt</u>           | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPD4PID</u>                 | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPSEMaxAvailPower</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPSEAutoclassSupport</u>    | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemAutoclassCompleted</u>     | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemAutoclassRequest</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPowerDownRequest</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPowerDownTime</u>          | ATTRIBUTE | GET |                                |                                                               |                                                                | X                                              |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasVoltageSupport</u>     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasCurrentSupport</u>     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasPowerSupport</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasEnergySupport</u>      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasurementSource</u>      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasVoltageRequest</u>     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasCurrentRequest</u>     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasPowerRequest</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasEnergyRequest</u>      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasVoltageValid</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasCurrentValid</u>       | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasPowerValid</u>         | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasEnergyValid</u>        | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasVoltageUncertainty</u> | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasCurrentUncertainty</u> | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemMeasPowerUncertainty</u>   | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |

Table 30–7—LLDP capabilities (continued)

|                                           |           |     | LLDP Basic Package (mandatory) | LLDP MAC/PHY Configuration/Status Local Package (conditional) | LLDP MAC/PHY Configuration/Status Remote Package (conditional) | LLDP Power via MDI Local Package (conditional) | LLDP Power via MDI Remote Package (conditional) | LLDP Power via MDI Measurements Local Package (conditional) | LLDP Power via MDI Measurements Remote Package (conditional) | LLDP Link Aggregation Local Package (conditional) | LLDP Link Aggregation Remote Package (conditional) | LLDP Maximum Frame Size Local Package (conditional) | LLDP Maximum Frame Size Remote Package (conditional) | LLDP EEE Local Package (optional) | LLDP EEE Remote Package (optional) |
|-------------------------------------------|-----------|-----|--------------------------------|---------------------------------------------------------------|----------------------------------------------------------------|------------------------------------------------|-------------------------------------------------|-------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------|----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|-----------------------------------|------------------------------------|
| <u>aLldpXdot3RemMeasEnergyUncertainty</u> | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemVoltageMeasurement</u>    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemCurrentMeasurement</u>    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPowerMeasurement</u>      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemEnergyMeasurement</u>     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| <u>aLldpXdot3RemPSEPowerPriceIndex</u>    | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 | X                                                           |                                                              |                                                   |                                                    |                                                     |                                                      |                                   |                                    |
| aLldpXdot3RemTxTwSys                      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemTxTwSysEcho                  | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemRxTwSys                      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemRxTwSysEcho                  | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemFbTwSys                      | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemTxFw                         | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemTxFwEcho                     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemRxFw                         | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |
| aLldpXdot3RemRxFwEcho                     | ATTRIBUTE | GET |                                |                                                               |                                                                |                                                |                                                 |                                                             |                                                              |                                                   |                                                    |                                                     |                                                      |                                   | X                                  |

Change the title of 30.9 as follows:

## 30.9 Management for ~~DTE Power via MDI~~ Power over Ethernet

### 30.9.1 PSE managed object class

#### 30.9.1.1 PSE attributes

Change 30.9.1.1.2 through 30.9.1.1.5 as follows:

##### 30.9.1.1.2 aPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|          |                        |
|----------|------------------------|
| enabled  | PSE functions enabled  |
| disabled | PSE functions disabled |

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational state of the PSE functions. An interface which can provide the PSE functions specified in Clause 33 will be enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled”, the interface will act as it would if it had no PSE function. The operational state of the PSE function can be changed using the acPSEAdminControl action. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Enable bit specified in 33.5.1.1.6.;

##### 30.9.1.1.3 aPSEPowerPairsControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

Indicates the ability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. When “true”, the PSE Pinout Alternative used can be controlled through the aSectionSESS-aPSEPowerPairs attribute. When “false”, the PSE Pinout Alternative used cannot be controlled through the aSectionSESS-aPSEPowerPairs attribute. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control Ability bit specified in 33.5.1.2.12;

##### 30.9.1.1.4 aPSEPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|             |                                                   |
|-------------|---------------------------------------------------|
| signal      | PSE Pinout Alternative A                          |
| spare       | PSE Pinout Alternative B                          |
| <u>both</u> | <u>PSE Pinout Alternative A and Alternative B</u> |

BEHAVIOUR DEFINED AS:

A read-write value that identifies the supported PSE Pinout Alternative specified in 33.2.3 and 145.2.4. A GET operation returns the PSE Pinout Alternative in use. A SET operation changes the PSE Pinout Alternative used to the indicated value only if the attribute aSectionSESThreshold is “true”. If the attribute aPSEPowerPairsControlAbility is “true”, a SET operation will cause the

PSE functions to be disabled, the PSE Pinout Alternative used to be changed to the value indicated if supported, and then the PSE functions to be enabled. If the attribute aSectionSESThreshold-aPSEPowerPairsControlAbility is “false”, a SET operation has no effect.

The enumeration “signal” indicates that PSE Pinout Alternative A is used for PD detection and power. The enumeration “spare” indicates that PSE Pinout Alternative B is used for PD detection and power. The enumeration “both” indicates that the PSE Pinout uses both Alternative A and Alternative B for detection and power. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control bits specified in 33.5.1.1.4.;

### 30.9.1.1.5 aPSEPowerDetectionStatus

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                 |                                            |
|-----------------|--------------------------------------------|
| disabled        | PSE disabled                               |
| searching       | PSE searching                              |
| deliveringPower | PSE delivering power                       |
| test            | PSE test mode                              |
| fault           | PSE fault detected                         |
| otherFault      | PSE implementation specific fault detected |

#### BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.5 and 145.2.6.

The enumeration “disabled” indicates that the PSE State diagram (Figure 33–9 or Figure 145–13) is in the state DISABLED. The enumeration “deliveringPower” indicates that the PSE State diagram is in the state POWER\_ON. The enumeration “test” indicates that the PSE State diagram is in the state TEST\_MODE. The enumeration “fault” indicates that the PSE State diagram is in the state TEST\_ERROR. The enumeration “otherFault” indicates that the PSE State diagram is in the state IDLE due to the variable error\_condition = ~~true~~ TRUE. The enumeration “searching” indicates the PSE State diagram is in a state other than those listed above. Type 3 and Type 4 PSEs do not use the values “test” or “fault”. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.5.1.2.11.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPower” enumeration as the PSE state diagram will enter and then quickly exit the POWER\_ON state if a short-circuit or overcurrent condition is present when power is first applied.;

*Insert the following new subclauses, 30.9.1.1.5a and 30.9.1.1.5b, after 30.9.1.1.5:*

### 30.9.1.1.5a aPSEPowerDetectionStatusA

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                     |                      |
|---------------------|----------------------|
| searchingAltA       | PSE searching        |
| deliveringPowerAltA | PSE delivering power |
| faultAltA           | PSE fault detected   |

#### BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 145.2.6.

The enumeration “deliveringPowerAltA” indicates that the PSE State diagram is in the state POWER\_ON\_PRI if alt\_pri=‘a’ or the state POWER\_ON\_SEC if alt\_pri=‘b’. The enumeration “faultAltA” indicates that the PSE State diagram is in the state IDLE\_PRI if alt\_pri=‘a’ or the state IDLE\_SEC if alt\_pri=‘b’ due to the variable error\_condition\_pri = TRUE (if alt\_pri=‘a’) or error\_condition\_sec = TRUE (if alt\_pri=‘b’). The enumeration “searchingAltA” indicates the PSE State diagram is in a state other than those listed above.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPowerAltA” enumeration as the PSE state diagram will enter and then quickly exit the POWER\_ON\_PRI (if alt\_pri=‘a’) state or the POWER\_ON\_SEC (if alt\_pri=‘b’) state if a short-circuit or overcurrent condition is present when power is first applied.;

### 30.9.1.1.5b aPSEPowerDetectionStatusB

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                     |                      |
|---------------------|----------------------|
| searchingAltB       | PSE searching        |
| deliveringPowerAltB | PSE delivering power |
| faultAltB           | PSE fault detected   |

#### BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 145.2.6.

The enumeration “deliveringPowerAltB” indicates that the PSE State diagram is in the state POWER\_ON\_SEC if alt\_pri=‘a’ or the state POWER\_ON\_PRI if alt\_pri=‘b’. The enumeration “faultAltB” indicates that the PSE State diagram is in the state IDLE\_SEC if alt\_pri=‘a’ or the state IDLE\_PRI if alt\_pri=‘b’ due to the variable error\_condition\_sec = TRUE (if alt\_pri=‘a’) or error\_condition\_pri = TRUE (if alt\_pri=‘b’). The enumeration “searchingAltB” indicates the PSE State diagram is in a state other than those listed above.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPowerAltB” enumeration as the PSE state diagram will enter and then quickly exit the POWER\_ON\_SEC (if alt\_pri=‘a’) state or the POWER\_ON\_PRI (if alt\_pri=‘b’) state if a short-circuit or overcurrent condition is present when power is first applied.;

*Change 30.9.1.1.6 as follows:*

### 30.9.1.1.6 aPSEPowerClassification

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|               |                   |
|---------------|-------------------|
| class0        | Class 0 PD        |
| class1        | Class 1 PD        |
| class2        | Class 2 PD        |
| class3        | Class 3 PD        |
| class4        | Class 4 PD        |
| <u>class5</u> | <u>Class 5 PD</u> |
| <u>class6</u> | <u>Class 6 PD</u> |
| <u>class7</u> | <u>Class 7 PD</u> |
| <u>class8</u> | <u>Class 8 PD</u> |

## BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected PD as specified in [33.2.6.1](#) and [145.2.8.1](#).

This value is only valid while a PD is being powered, that is the attribute ~~aLineSESThreshold~~ ~~aPSEPowerDetectionStatus~~ reporting the enumeration “deliveringPower”. For Type 1 or Type 2 PSEs, if a [Clause 22](#) MII or [Clause 35](#) GMII is present, then this will map to the PD Class bits specified in [33.5.1.2.10](#);

*Insert the following new subclauses, 30.9.1.1.6a and 30.9.1.1.6b, after 30.9.1.1.6:*

**30.9.1.1.6a aPSEPowerClassificationA**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|        |            |
|--------|------------|
| class1 | Class 1 PD |
| class2 | Class 2 PD |
| class3 | Class 3 PD |
| class4 | Class 4 PD |
| class5 | Class 5 PD |

## BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected dual-signature PD as specified in [145.2.8.1](#).

This value is only valid while a PD is being powered, that is the attribute ~~aPSEPowerDetectionStatusA~~ reporting the enumeration “deliveringPowerAltA”;

**30.9.1.1.6b aPSEPowerClassificationB**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|        |            |
|--------|------------|
| class1 | Class 1 PD |
| class2 | Class 2 PD |
| class3 | Class 3 PD |
| class4 | Class 4 PD |
| class5 | Class 5 PD |

## BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected dual-signature PD as specified in [145.2.8.1](#).

This value is only valid while a PD is being powered, that is the attribute ~~aPSEPowerDetectionStatusB~~ reporting the enumeration “deliveringPowerAltB”;

*Change 30.9.1.1.7 as follows:*

#### 30.9.1.1.7 aPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the Type 1 and Type 2 PSE state diagram (Figure 33–9) enters the state SIGNATURE\_INVALID. This counter is not defined for Type 3 and Type 4 PSEs. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.5.1.2.6.;

*Insert the following new subclauses, 30.9.1.1.7a and 30.9.1.1.7b, after 30.9.1.1.7:*

#### 30.9.1.1.7a aPSEInvalidSignatureCounterA

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the do\_detect\_pri or do\_detect\_sec function in Figure 145–13, Figure 145–15, and Figure 145–16, whichever corresponds to Alternative A depending on the value of alt\_pri, returns ‘invalid’.

#### 30.9.1.1.7b aPSEInvalidSignatureCounterB

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the do\_detect\_pri or do\_detect\_sec function in Figure 145–13, Figure 145–15, and Figure 145–16, whichever corresponds to Alternative B depending on the value of alt\_pri, returns ‘invalid’.

*Change 30.9.1.1.8 as follows:*

#### 30.9.1.1.8 aPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9 and Figure 145–13) enters the state POWER\_DENIED. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.5.1.2.4.;

*Insert the following new subclauses, 30.9.1.1.8a and 30.9.1.1.8b, after 30.9.1.1.8:*

#### **30.9.1.1.8a aPSEPowerDeniedCounterA**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state POWER\_DENIED\_PRI if alt\_pri='a' or enters the state POWER\_DENIED\_SEC if alt\_pri='b';

#### **30.9.1.1.8b aPSEPowerDeniedCounterB**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state POWER\_DENIED\_SEC if alt\_pri='a' or enters the state POWER\_DENIED\_PRI if alt\_pri='b';

*Change 30.9.1.1.9 as follows:*

#### **30.9.1.1.9 aPSEOverLoadCounter**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9 and Figure 145–13) enters the state ~~ERROR\_DELAY\_OVER~~ ERROR\_DELAY. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.5.1.2.8.;

*Insert the following new subclause, 30.9.1.1.9a, after 30.9.1.1.9:*

#### **30.9.1.1.9a aPSEOverLoadCounterA**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state ERROR\_DELAY\_PRI if alt\_pri='a' or enters the state ERROR\_DELAY\_SEC if alt\_pri='b';

*Change 30.9.1.1.10 as follows:*

#### **30.9.1.1.10 ~~aPSEShortCounter~~ aPSEOverLoadCounterB**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

~~This counter is incremented when the PSE state diagram (Figure 33–9) enters the state ERROR\_DELAY\_SHORT. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Short Circuit bit specified in 33.5.1.2.7.;~~

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state ERROR\_DELAY\_SEC if alt\_pri='a' or enters the state ERROR\_DELAY\_PRI if alt\_pri='b'.

*Change 30.9.1.1.11 as follows:*

#### **30.9.1.1.11 aPSEMPSAbsentCounter**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9 and Figure 145–13) transitions directly from the state POWER\_ON to the state IDLE due to tmpdo\_timer\_done being asserted. For Type 1 or Type 2 PSEs. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.5.1.2.9.;

*Insert the following new subclauses, 30.9.1.1.11a and 30.9.1.1.11b, after 30.9.1.1.11:*

#### **30.9.1.1.11a aPSEMPSAbsentCounterA**

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) transitions directly from the state POWER\_ON\_PRI to the state IDLE\_PRI due to mpdo\_timer\_pri\_done being asserted if alt\_pri='a' or transitions directly from the state POWER\_ON\_SEC to the state IDLE\_SEC due to mpdo\_timer\_sec\_done being asserted if alt\_pri='b'.

### 30.9.1.1.11b aPSEMPSAbsentCounterB

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) transitions directly from the state POWER\_ON\_SEC to the state IDLE\_SEC due to mpdo\_timer\_sec\_done being asserted if alt\_pri='a' or transitions directly from the state POWER\_ON\_PRI to the state IDLE\_PRI due to mpdo\_timer\_pri\_done being asserted if alt\_pri='b'.;

### 30.9.1.2 PSE actions

*Change 30.9.1.2.1 as follows:*

#### 30.9.1.2.1 acPSEAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as ~~aSectionStatus~~ aPSEAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to alter ~~aSectionStatus~~ aPSEAdminState.;

*Delete 30.9.2 “PD managed object class” and its subclauses in their entirety.*

## 30.12 Layer Management for Link Layer Discovery Protocol (LLDP)

### 30.12.2 LLDP Local System Group managed object class

#### 30.12.2.1 LLDP Local System Group attributes

*Change 30.12.2.1.6 through 30.12.2.1.10 as follows:*

##### 30.12.2.1.6 aLldpXdot3LocPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

For a PSE, this attribute contains a ~~A~~ read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the local system. For a PD, the value of this attribute is undefined.;

##### 30.12.2.1.7 aLldpXdot3LocPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

## BEHAVIOUR DEFINED AS:

For a PSE, this attribute contains a read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the local system. For a PD, the value of this attribute is undefined.

**30.12.2.1.8 aLdpXdot3LocPowerPairControllable**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BOOLEAN

## BEHAVIOUR DEFINED AS:

A read-only Boolean value derived from the value of pethPsePortPowerPairsControlAbility object (defined in IETF RFC 3621) and used to indicate whether the pair selection can be controlled on the given port associated with the local system.

A read-only Boolean value used to indicate the ability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. For a PSE, this attribute contains the value of the aPSEPowerPairsControlAbility attribute (see 30.9.1.1.3). For a PD, the contents of this attribute are undefined.

**30.12.2.1.9 aLdpXdot3LocPowerPairs**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

The same as used for aPSEPowerPairs

An ENUMERATED value list that has the following entries:

|               |                                 |
|---------------|---------------------------------|
| <u>signal</u> | <u>PSE Pinout Alternative A</u> |
| <u>spare</u>  | <u>PSE Pinout Alternative B</u> |

## BEHAVIOUR DEFINED AS:

A read-only value that contains the value of the pethPsePortPowerPairs object (defined in IETF RFC 3621) which is associated with the given port on the local system.

A read-only value that identifies the PSE Pinout Alternative (see 33.2.3 and 145.2.4) in use for detecting and supplying power to the PD. For a PSE, this attribute contains a value derived from the aPSEPowerPairs attribute (see 30.9.1.1.4). For a PD, the contents of this attribute are undefined. A Type 3 or Type 4 PSE detecting or supplying power on both PSE Pinout Alternatives may return either PSE Pinout Alternative as this configuration is communicated through the aLdpXdot3LocPowerPairsExt attribute. A Type 3 or Type 4 PSE supplying power on only one PSE Pinout Alternative returns that PSE Pinout Alternative. For a PD, the contents of this attribute are undefined.

**30.12.2.1.10 aLdpXdot3LocPowerClass**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

The same as used for aPSEPowerClassification

An ENUMERATED value list that has the following entries:

|               |                   |
|---------------|-------------------|
| <u>class0</u> | <u>Class 0 PD</u> |
| <u>class1</u> | <u>Class 1 PD</u> |
| <u>class2</u> | <u>Class 2 PD</u> |
| <u>class3</u> | <u>Class 3 PD</u> |
| <u>class4</u> | <u>Class 4 PD</u> |

## BEHAVIOUR DEFINED AS:

~~A read-only value that contains the value of the `pathPsePortPowerClassifications` object (defined in IETF RFC 3621) which is associated with the given port on the local system.;~~  
A read-only value that indicates the requested Class of the PD as specified in 33.2.6 and 145.2.8. This attribute returns an enumeration of “class4” for a PD of Class 4 or higher as such PD Classes are identified through the `aLldpXdot3LocPowerClassExt` attribute.;

*Change 30.12.2.1.14 as follows:*

**30.12.2.1.14 aLldpXdot3LocPowerType**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

## BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or ~~Type 2 greater than Type 1~~. The first bit indicates Type 1 or ~~Type 2 greater than Type 1~~. The second bit indicates PSE or PD. A PSE ~~shall~~ sets this bit to indicate a PSE. A PD ~~shall~~ sets this bit to indicate a PD. See also `aLldpXdot3LocPowerTypeExt`.;

*Change 30.12.2.1.17 as follows:*

**30.12.2.1.17 aLldpXdot3LocPDRequestedPowerValue**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value in units of 0.1 W. For a PD, it is the power value that the PD has currently requested from the remote system. The PD requested power value is the maximum input average power the PD ever draws under this power allocation if accepted. For a PSE, it is the power value that the PSE ~~mirrors-echoes~~ back to the remote system. This is the PD requested power value that was used by the PSE to compute the power it has currently allocated to the remote system. ~~The PD requested power value is encoded according to Equation (79-1), where X is the decimal value of aLldpXdot3LocPDRequestedPowerValue.;~~

*Insert the following new subclauses, 30.12.2.1.17a and 30.12.2.1.17b, after 30.12.2.1.17:*

**30.12.2.1.17a aLldpXdot3LocPDRequestedPowerValueA**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value for the Mode A pairset in units of 0.1 W. For a PD, it is the power value that the PD has currently requested from the remote system for the Mode A pairset. For a PSE, it is the power value for the Alternative A pairset that the PSE echoes back to the remote system.;

**30.12.2.1.17b aLldpXdot3LocPDRequestedPowerValueB**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value for the Mode B pairset in units of 0.1 W. For a PD, it is the power value that the PD has currently requested from the remote system for the Mode B pairset. For a PSE, it is the power value for the Alternative B pairset that the PSE echoes back to the remote system.;

*Change 30.12.2.1.18 as follows:***30.12.2.1.18 aLldpXdot3LocPSEAllocatedPowerValue**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value in units of 0.1 W. For a PSE, it is the power value that the PSE has currently allocated to the remote system. The PSE allocated power value is the maximum input average power that the PSE wants the PD to ever draw under this allocation if it is accepted. For a PD, it is the power value that the PD ~~mirrors-echoed~~ back to the remote system. ~~This is the PSE allocated power value that was used by the PD to compute the power that it has currently requested from the remote system. The PSE allocated power value is encoded according to Equation (79-2), where X is the decimal value of~~ aLldpXdot3LocPSEAllocatedPowerValue.;

*Insert the following new subclauses, 30.12.2.1.18a through 30.12.2.1.18am, after 30.12.2.1.18:***30.12.2.1.18a aLldpXdot3LocPSEAllocatedPowerValueA**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value for the Alternative A pairset in units of 0.1 W. For a PSE, it is the power value for the Alternative A pairset that the PSE has currently allocated to the remote system. For a PD, it is the power value for the Mode A pairset that the PD echoes back to the remote system.;

**30.12.2.1.18b aLldpXdot3LocPSEAllocatedPowerValueB**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value for the Alternative B pairset in units of 0.1 W. For a PSE, it is the power value for the Alternative B pairset that the PSE has currently

allocated to the remote system. For a PD, it is the power value for the Mode B pairset that the PD echoes back to the remote system.;

#### 30.12.2.1.18c aLldpXdot3LocPSEPoweringStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                |                                       |
|----------------|---------------------------------------|
| 4PdualsigPD    | 4-pair powering a dual-signature PD   |
| 4Psingle sigPD | 4-pair powering a single-signature PD |
| 2P             | 2-pair powering                       |

BEHAVIOUR DEFINED AS:

A read only value that indicates the powering status of the PSE. For a PD, the contents of this attribute are undefined.;

#### 30.12.2.1.18d aLldpXdot3LocPDPoweredStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|              |                                  |
|--------------|----------------------------------|
| 4PdualsigPD  | 4-pair powered dual-signature PD |
| 2PdualsigPD  | 2-pair powered dual-signature PD |
| single sigPD | powered single-signature PD      |

BEHAVIOUR DEFINED AS:

A read only value that indicates the powering status of the PD. For a PSE, the contents of this attribute are undefined.;

#### 30.12.2.1.18e aLldpXdot3LocPowerPairsExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|      |                   |
|------|-------------------|
| altA | Alternative A     |
| altB | Alternative B     |
| both | Both Alternatives |

BEHAVIOUR DEFINED AS:

A read-only value that identifies the supported PSE Pinout Alternative specified in 145.2.4. For a PSE, this attribute contains the value of the aPSEPowerPairs attribute (see 30.9.1.1.4). For a PD, the contents of this attribute are undefined.;

#### 30.12.2.1.18f aLldpXdot3LocPowerClassExtA

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|            |                                        |
|------------|----------------------------------------|
| single sig | Single-signature PD or 2-pair only PSE |
| class1     | Class 1                                |
| class2     | Class 2                                |
| class3     | Class 3                                |

|        |         |
|--------|---------|
| class4 | Class 4 |
| class5 | Class 5 |

**BEHAVIOUR DEFINED AS:**

For a dual-signature PD, a read-only value that indicates the requested Class for Mode A during Physical Layer Classification (see 145.3.6). For a single-signature PD, a read-only value set to 'singlesig'.

For a PSE connected to a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode A (see 145.2.8). For a PSE connected to a single-signature PD or a PSE that operates only in 2-pair mode, a read-only value set to 'singlesig';

**30.12.2.1.18g aLldpXdot3LocPowerClassExtB****ATTRIBUTE****APPROPRIATE SYNTAX:**

An ENUMERATED VALUE that has one of the following entries:

|           |                                        |
|-----------|----------------------------------------|
| singlesig | Single-signature PD or 2-pair only PSE |
| class1    | Class 1                                |
| class2    | Class 2                                |
| class3    | Class 3                                |
| class4    | Class 4                                |
| class5    | Class 5                                |

**BEHAVIOUR DEFINED AS:**

For a dual-signature PD, a read-only value that indicates the requested Class for Mode B during Physical Layer Classification (see 145.3.6). For a single-signature PD, a read-only value set to 'singlesig'.

For a PSE connected to a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode B (see 145.2.8). For a PSE connected to a single-signature PD or a PSE that operates only in 2-pair mode, a read-only value set to 'singlesig';

**30.12.2.1.18h aLldpXdot3LocPowerClassExt****ATTRIBUTE****APPROPRIATE SYNTAX:**

An ENUMERATED VALUE that has one of the following entries:

|         |                   |
|---------|-------------------|
| dualsig | Dual-signature PD |
| class1  | Class 1           |
| class2  | Class 2           |
| class3  | Class 3           |
| class4  | Class 4           |
| class5  | Class 5           |
| class6  | Class 6           |
| class7  | Class 7           |
| class8  | Class 8           |

**BEHAVIOUR DEFINED AS:**

For a single-signature PD, a read-only value that indicates the requested Class during Physical Layer Classification (see 145.3.6). For a dual-signature PD, a read-only value set to 'dualsig'.

For a PSE connected to a single-signature PD or a PSE that operates only in 2-pair mode, a read-only value that indicates the currently assigned Class (see 145.2.8). For a PSE connected to a dual-signature PD, a read-only value set to 'dualsig';

#### 30.12.2.1.18i aLldpXdot3LocPowerTypeExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                  |                            |
|------------------|----------------------------|
| type4dualsigPD   | Type 4 dual-signature PD   |
| type4singlesigPD | Type 4 single-signature PD |
| type3dualsigPD   | Type 3 dual-signature PD   |
| type3singlesigPD | Type 3 single-signature PD |
| type4PSE         | Type 4 PSE                 |
| type3PSE         | Type 3 PSE                 |

BEHAVIOUR DEFINED AS:

A read-only attribute that returns a value to indicate if the local system is a Type 3 or Type 4 PSE or PD and, in the case of a Type 3 or Type 4 PD, if it is a single-signature PD or a dual-signature PD.;

#### 30.12.2.1.18j aLldpXdot3LocPDLoad

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

For a dual-signature PD, a GET attribute that returns whether the load of a dual-signature PD is electrically isolated, as defined in 79.3.2.6d.2. For a single-signature PD or a PSE, the value of this attribute is FALSE.;

#### 30.12.2.1.18k aLldpXdot3LocPD4PID

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean attribute indicating whether the local PD system supports powering of both PD Modes.;

#### 30.12.2.1.18l aLldpXdot3LocPSEMaxAvailPower

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the local PSE maximum available power value in units of 0.1 W.;

#### 30.12.2.1.18m aLldpXdot3LocPSEAutoclassSupport

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A read-only attribute that returns a bit string indicating whether the local PSE system supports Autoclass.;

**30.12.2.1.18n aLldpXdot3LocAutoclassCompleted**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A read-only attribute that returns a bit string indicating whether the local PSE system has completed the Autoclass measurement.;

**30.12.2.1.18o aLldpXdot3LocAutoclassRequest**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A read-only attribute that returns a bit string indicating whether the local PD system is requesting an Autoclass measurement and power budget adjustment.;

**30.12.2.1.18p aLldpXdot3LocPowerDownRequest**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A SET attribute that indicates the local PD system is requesting a power down when the value is 0x1D.;

**30.12.2.1.18q aLldpXdot3LocPowerDownTime**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A SET attribute that indicates the number of seconds the PD requests to stay powered off. A value of zero indicates an indefinite amount of time.;

**30.12.2.1.18r aLldpXdot3LocMeasVoltageSupport**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is capable of providing a voltage measurement.;

**30.12.2.1.18s aLldpXdot3LocMeasCurrentSupport**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is capable of providing a current measurement.;

**30.12.2.1.18t aLldpXdot3LocMeasPowerSupport**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is capable of providing a power measurement.;

**30.12.2.1.18u aLldpXdot3LocMeasEnergySupport**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is capable of providing an energy measurement.;

**30.12.2.1.18v aLldpXdot3LocMeasurementSource**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A SET attribute value that indicates to local device on which Alternative or Mode the measurement is to be taken.;

**30.12.2.1.18w aLldpXdot3LocMeasVoltageRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is requesting a voltage measurement from the remote device.;

**30.12.2.1.18x aLldpXdot3LocMeasCurrentRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is requesting a current measurement from the remote device.;

**30.12.2.1.18y aLldpXdot3LocMeasPowerRequest**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is requesting a power measurement from the remote device.;

**30.12.2.1.18z aLldpXdot3LocMeasEnergyRequest**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device is requesting an energy measurement from the remote device.;

**30.12.2.1.18aa aLldpXdot3LocMeasVoltageValid**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device's voltage measurement is valid.;

**30.12.2.1.18ab aLldpXdot3LocMeasCurrentValid**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device's current measurement is valid.;

**30.12.2.1.18ac aLldpXdot3LocMeasPowerValid**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device's power measurement is valid.;

**30.12.2.1.18ad aLdpXdot3LocMeasEnergyValid**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the local device's energy measurement is valid.;

**30.12.2.1.18ae aLdpXdot3LocMeasVoltageUncertainty**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the device's voltage measurement. See Table 79–8a.;

**30.12.2.1.18af aLdpXdot3LocMeasCurrentUncertainty**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the device's current measurement. See Table 79–8a.;

**30.12.2.1.18ag aLdpXdot3LocMeasPowerUncertainty**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the device's power measurement. See Table 79–8a.;

**30.12.2.1.18ah aLdpXdot3LocMeasEnergyUncertainty**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the device's energy measurement. See Table 79–8a.;

**30.12.2.1.18ai aLldpXdot3LocVoltageMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured device voltage. See Table 79–8a.;

**30.12.2.1.18aj aLldpXdot3LocCurrentMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured device current. See Table 79–8a.;

**30.12.2.1.18ak aLldpXdot3LocPowerMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured device power. See Table 79–8a.;

**30.12.2.1.18al aLldpXdot3LocEnergyMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured device energy. See Table 79–8a.;

**30.12.2.1.18am aLldpXdot3LocPSEPowerPriceIndex**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns an index of the price of power being sourced by the PSE. For a PD, this value is undefined.;

**Delete 30.12.2.1.21 “aLldpXdot3LocReducedOperationPowerValue.”**

### 30.12.3 LLDP Remote System Group managed object class

#### 30.12.3.1 LLDP Remote System Group attributes

*Change 30.12.3.1.6 through 30.12.3.1.10 as follows:*

##### 30.12.3.1.6 aLldpXdot3RemPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

This attribute contains a read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the remote PSE system. When the remote system is a PD, the value of this attribute is undefined.;

##### 30.12.3.1.7 aLldpXdot3RemPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

This attribute contains a read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the remote PSE system. When the remote system is a PD, the value of this attribute is undefined.;

##### 30.12.3.1.8 aLldpXdot3RemPowerPairControllable

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

~~A read-only Boolean value is derived from the value of pethPsePortPowerPairsControlAbility object (defined in IETF RFC 3621) and is used to indicate whether the pair selection can be controlled on the given port associated with the remote system.;~~  
A read-only Boolean value used to indicate the ability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power on the given port on the remote system. For a PD, this attribute contains the value of the aPSEPowerPairsControlAbility attribute (see 30.9.1.1.3) on the given port on the remote system. For a PSE, the contents of this attribute are undefined.;

##### 30.12.3.1.9 aLldpXdot3RemPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

~~The same as used for aPSEPowerPairs~~

An ENUMERATED value list that has the following entries:

|               |                                 |
|---------------|---------------------------------|
| <u>signal</u> | <u>PSE Pinout Alternative A</u> |
| <u>spare</u>  | <u>PSE Pinout Alternative B</u> |

## BEHAVIOUR DEFINED AS:

~~A read-only value that contains the value of the pethPsePortPowerPairs object (defined in IETF RFC 3621) which is associated with the given port on the remote system.;~~

A read-only value that identifies the supported PSE Pinout Alternative (see 33.2.3 and 145.2.4) in use for supplying power to the PD on the given port on the remote system. For a PD, this attribute contains a value derived from the aPSEPowerPairs attribute (see 30.9.1.1.4) on the given port on the remote system. For a PSE, the contents of this attribute are undefined. When the remote system is a Type 3 or Type 4 PSE supplying power on both PSE Pinout Alternatives, the value of this attribute can indicate either pinout. If the aLldpXdot3RemPowerPairsExt attribute is available, it will report this configuration.;

**30.12.3.1.10 aLldpXdot3RemPowerClass**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

~~The same as used for aPSEPowerClassification~~

An ENUMERATED value list that has the following entries:

|               |                   |
|---------------|-------------------|
| <u>class0</u> | <u>Class 0 PD</u> |
| <u>class1</u> | <u>Class 1 PD</u> |
| <u>class2</u> | <u>Class 2 PD</u> |
| <u>class3</u> | <u>Class 3 PD</u> |
| <u>class4</u> | <u>Class 4 PD</u> |

## BEHAVIOUR DEFINED AS:

~~A read-only value that contains the value of the pethPsePortPowerClassifications object (defined in IETF RFC 3621) which is associated with the given port on the remote system.;~~

A read-only value that identifies the requested Class of the PD as specified in 33.2.6 and 145.2.8 on the given port on the remote system. This attribute will return an enumeration of “class4” for a PD of Class 4 or higher as such PD Classes are identified through the aLldpXdot3RemPowerClassExt attribute.;

*Change 30.12.3.1.14 as follows:*

**30.12.3.1.14 aLldpXdot3RemPowerType**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

## BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1 or Type 2 greater than Type 1. The first bit indicates Type 1 or Type 2 greater than Type 1. The second bit indicates PSE or PD. See also aLldpXdot3RemPowerTypeExt.;

*Change 30.12.3.1.17 as follows:*

**30.12.3.1.17 aLldpXdot3RemPDRrequestedPowerValue**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value that was used by the remote system to compute the power value that ~~is it~~ has currently allocated to the PD. For a PSE, it is the PD requested power value received from the remote system. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17). For a PD, it is the mirrored copy of the requested power field echoed back by the remote PSE.;

*Insert the following new subclauses, 30.12.3.1.17a and 30.12.3.1.17b, after 30.12.3.1.17:*

**30.12.3.1.17a aLldpXdot3RemPDRequestedPowerValueA**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value for the Mode A pairset that was used by the remote system to compute the power value that it has currently allocated to the PD. For a PSE, it is the PD requested power value for the Alternative A pairset received from the remote system. For a PD, it is the PD requested power value for the Alternative A pairset that the PSE echoes back to the remote system. The definition and encoding of PD requested power value for the Mode A pairset is the same as described in aLldpXdot3LocPDRequestedPowerValueA (30.12.2.1.17a).;

**30.12.3.1.17b aLldpXdot3RemPDRequestedPowerValueB**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value for the Mode B pairset that was used by the remote system to compute the power value that it has currently allocated to the PD. For a PSE, it is the PD requested power value for the Alternative B pairset received from the remote system. For a PD, it is the PD requested power value for the Alternative B pairset that the PSE echoes back to the remote system. The definition and encoding of PD requested power value for the Mode B pairset is the same as described in aLldpXdot3LocPDRequestedPowerValueB (30.12.2.1.17b).;

*Change 30.12.3.1.18 as follows:*

**30.12.3.1.18 aLldpXdot3RemPSEAllocatedPowerValue**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value received from the remote system. For a PSE, it is the PSE allocated power value that ~~was used by the remote system to compute the power value that it has currently requested from the PSE~~ was echoed back by the remote PD. For a PD, it is the PSE allocated power value received from the remote system. The definition and

encoding of PSE allocated power value is the same as described in  
aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18).;

*Insert the following new subclauses, 30.12.3.1.18a through 30.12.3.1.18am, after 30.12.3.1.18:*

#### **30.12.3.1.18a aLldpXdot3RemPSEAllocatedPowerValueA**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value for the Alternative A pairset received from the remote system. For a PSE, it is the PSE allocated power value for the Alternative A pairset that was echoed back by the remote PD. For a PD, it is the PSE allocated power value for the Mode A pairset received from the remote system. The definition and encoding of PSE allocated power value for the Alternative A pairset is the same as described in aLldpXdot3LocPSEAllocatedPowerValueA (30.12.2.1.18a).;

#### **30.12.3.1.18b aLldpXdot3RemPSEAllocatedPowerValueB**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value for the Alternative B pairset received from the remote system. For a PSE, it is the PSE allocated power value for the Alternative B pairset that was echoed back by the remote PD. For a PD, it is the PSE allocated power value for the Mode B pairset received from the remote system. The definition and encoding of PSE allocated power value for the Alternative B pairset is the same as described in aLldpXdot3LocPSEAllocatedPowerValueB (30.12.2.1.18b).;

#### **30.12.3.1.18c aLldpXdot3RemPSEPoweringStatus**

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                |                                       |
|----------------|---------------------------------------|
| 4PdualsigPD    | 4-pair powering a dual-signature PD   |
| 4Psingle sigPD | 4-pair powering a single-signature PD |
| 2P             | 2-pair powering                       |

BEHAVIOUR DEFINED AS:

A read only value that indicates the powering status of the remote PSE. For a PSE, the contents of this attribute are undefined.;

#### **30.12.3.1.18d aLldpXdot3RemPDPoweredStatus**

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|             |                                  |
|-------------|----------------------------------|
| 4PdualsigPD | 4-pair powered dual-signature PD |
|-------------|----------------------------------|

|             |                                  |
|-------------|----------------------------------|
| 2PdualsigPD | 2-pair powered dual-signature PD |
| singlesigPD | powered single-signature PD      |

**BEHAVIOUR DEFINED AS:**

A read only value that indicates the powering status of the remote PD. For a PD, the contents of this attribute are undefined.;

**30.12.3.1.18e aLldpXdot3RemPowerPairsExt****ATTRIBUTE****APPROPRIATE SYNTAX:**

An ENUMERATED VALUE that has one of the following entries:

|      |                   |
|------|-------------------|
| altA | Alternative A     |
| altB | Alternative B     |
| both | Both Alternatives |

**BEHAVIOUR DEFINED AS:**

A read-only value that identifies the supported PSE Pinout Alternative specified in 145.2.4. For a PD, this attribute contains the value of the aPSEPowerPairs attribute (see 30.9.1.1.4) as sent by the remote PSE. For a PSE, the contents of this attribute are undefined.;

**30.12.3.1.18f aLldpXdot3RemPowerClassExtA****ATTRIBUTE**

An ENUMERATED VALUE that has one of the following entries:

|           |                                        |
|-----------|----------------------------------------|
| singlesig | Single-signature PD or 2-pair only PSE |
| class1    | Class 1                                |
| class2    | Class 2                                |
| class3    | Class 3                                |
| class4    | Class 4                                |
| class5    | Class 5                                |

**BEHAVIOUR DEFINED AS:**

For a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode A by the remote 4-pair PSE. For a single-signature PD or a dual-signature PD connected to a 2-pair only PSE, a read-only value set to 'singlesig' by the remote PSE. For a PSE connected to a dual-signature PD, a read-only value that indicates the requested Class for Mode A during Physical Layer classification (see 145.2.8) by the remote PD. For a PSE connected to a single-signature PD, a read-only value set to 'singlesig' by the remote PD.;

**30.12.3.1.18g aLldpXdot3RemPowerClassExtB****ATTRIBUTE**

An ENUMERATED VALUE that has one of the following entries:

|           |                                        |
|-----------|----------------------------------------|
| singlesig | Single-signature PD or 2-pair only PSE |
| class1    | Class 1                                |
| class2    | Class 2                                |
| class3    | Class 3                                |
| class4    | Class 4                                |
| class5    | Class 5                                |

**BEHAVIOUR DEFINED AS:**

For a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode B by the remote 4-pair PSE. For a single-signature PD or a dual-signature PD connected to a 2-pair

only PSE, a read-only value set to 'singlesig' by the remote PSE. For a PSE connected to a dual-signature PD, a read-only value that indicates the requested Class for Mode B during Physical Layer classification (see 145.2.8) by the remote PD. For a PSE connected to a single-signature PD, a read-only value set to 'singlesig' by the remote PD.;

### 30.12.3.1.18h aLldpXdot3RemPowerClassExt

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|         |                   |
|---------|-------------------|
| dualsig | Dual-signature PD |
| class1  | Class 1           |
| class2  | Class 2           |
| class3  | Class 3           |
| class4  | Class 4           |
| class5  | Class 5           |
| class6  | Class 6           |
| class7  | Class 7           |
| class8  | Class 8           |

#### BEHAVIOUR DEFINED AS:

For a single-signature PD or a dual-signature PD connected to a 2-pair only PSE, a read-only value that indicates the currently assigned Class by the remote PSE. For a dual-signature PD connected to a 4-pair capable PSE, a read-only value set to 'dualsig' by the remote PSE. For a PSE connected to a single-signature PD, a read-only value that indicates the requested Class during Physical Layer classification (see 145.2.8) by the remote PD. For a PSE connected to a dual-signature PD, a read-only value set to 'dualsig' by the remote PD.;

### 30.12.3.1.18i aLldpXdot3RemPowerTypeExt

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

|                  |                            |
|------------------|----------------------------|
| type4dualsigPD   | Type 4 dual-signature PD   |
| type4singlesigPD | Type 4 single-signature PD |
| type3dualsigPD   | Type 3 dual-signature PD   |
| type3singlesigPD | Type 3 single-signature PD |
| type4PSE         | Type 4 PSE                 |
| type3PSE         | Type 3 PSE                 |

#### BEHAVIOUR DEFINED AS:

A read-only attribute that returns a value to indicate if the remote system is a Type 3 or Type 4 PSE or PD and, in the case of a Type 3 or Type 4 PD, if it is a single-signature PD or dual-signature PD.;

### 30.12.3.1.18j aLldpXdot3RemPDLoad

#### ATTRIBUTE

#### APPROPRIATE SYNTAX:

BOOLEAN

#### BEHAVIOUR DEFINED AS:

For a PSE, a GET attribute that returns whether the load of the remote dual-signature PD is electrically isolated, as defined in 79.3.2.6d.2. For a PD, this attribute is set to FALSE.;

**30.12.3.1.18k aLldpXdot3RemPD4PID**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean attribute indicating whether the remote PD system supports powering of both PD Modes.;

**30.12.3.1.18l aLldpXdot3RemPSEMaxAvailPower**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the remote PSE maximum available power value in units of 0.1 W.;

**30.12.3.1.18m aLldpXdot3RemPSEAutoclassSupport**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean attribute indicating whether the remote PSE system supports Autoclass.;

**30.12.3.1.18n aLldpXdot3RemAutoclassCompleted**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean attribute indicating whether the remote PSE system has completed the Autoclass measurement.;

**30.12.3.1.18o aLldpXdot3RemAutoclassRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean attribute indicating whether the remote PD system is requesting an Autoclass measurement.;

**30.12.3.1.18p aLldpXdot3RemPowerDownRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A read-only attribute that indicates the remote PD system is requesting a power down when the value is 0x1D.;

**30.12.3.1.18q aLldpXdot3RemPowerDownTime**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

INTEGER

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates the number of seconds the remote PD requests to stay powered off.

A value of zero indicates an indefinite amount of time.;

**30.12.3.1.18r aLldpXdot3RemMeasVoltageSupport**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BOOLEAN

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates if the remote device is capable of providing a voltage measurement.;

**30.12.3.1.18s aLldpXdot3RemMeasCurrentSupport**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BOOLEAN

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates if the remote device is capable of providing a current measurement.;

**30.12.3.1.18t aLldpXdot3RemMeasPowerSupport**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BOOLEAN

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates if the remote device is capable of providing a power measurement.;

**30.12.3.1.18u aLldpXdot3RemMeasEnergySupport**

## ATTRIBUTE

## APPROPRIATE SYNTAX:

BOOLEAN

## BEHAVIOUR DEFINED AS:

A GET attribute that indicates if the remote device is capable of providing an energy measurement.;

**30.12.3.1.18v aLldpXdot3RemMeasurementSource**

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A SET attribute value that indicates on which Alternative or Mode the measurement was taken by the remote device.;

**30.12.3.1.18w aLldpXdot3RemMeasVoltageRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting a voltage measurement from the local device.;

**30.12.3.1.18x aLldpXdot3RemMeasCurrentRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting a current measurement from the local device.;

**30.12.3.1.18y aLldpXdot3RemMeasPowerRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting a power measurement from the local device.;

**30.12.3.1.18z aLldpXdot3RemMeasEnergyRequest**

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting an energy measurement from the local device.;

#### 30.12.3.1.18aa aLldpXdot3RemMeasVoltageValid

ATTRIBUTE

APPROPRIATE SYNTAX:  
BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device's voltage measurement is valid.;

#### 30.12.3.1.18ab aLldpXdot3RemMeasCurrentValid

ATTRIBUTE

APPROPRIATE SYNTAX:  
BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device's current measurement is valid.;

#### 30.12.3.1.18ac aLldpXdot3RemMeasPowerValid

ATTRIBUTE

APPROPRIATE SYNTAX:  
BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device's power measurement is valid.;

#### 30.12.3.1.18ad aLldpXdot3RemMeasEnergyValid

ATTRIBUTE

APPROPRIATE SYNTAX:  
BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device's energy measurement is valid.;

#### 30.12.3.1.18ae aLldpXdot3RemMeasVoltageUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the remote device's voltage measurement. See Table 79–8a.;

#### 30.12.3.1.18af aLldpXdot3RemMeasCurrentUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the remote device's current measurement. See Table 79–8a.;

**30.12.3.1.18ag aLldpXdot3RemMeasPowerUncertainty**

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the remote device's power measurement. See Table 79–8a.;

**30.12.3.1.18ah aLldpXdot3RemMeasEnergyUncertainty**

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor  $k = 2$ ) for the remote device's energy measurement. See Table 79–8a.;

**30.12.3.1.18ai aLldpXdot3RemVoltageMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device voltage. See Table 79–8a.;

**30.12.3.1.18aj aLldpXdot3RemCurrentMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device current. See Table 79–8a.;

**30.12.3.1.18ak aLldpXdot3RemPowerMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:  
INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device power. See Table 79–8a.;

**30.12.3.1.18a1 aLldpXdot3RemEnergyMeasurement**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device energy. See Table 79–8a.;

**30.12.3.1.18am aLldpXdot3RemPSEPowerPriceIndex**

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns an index of the price of power being sourced by the remote PSE. For a PSE, this value is undefined.;

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*Change the title of Clause 33 as follows:*

### **33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI) Power over Ethernet over 2 Pairs**

#### **33.1 Overview**

*Insert the following paragraph after the first paragraph (“This clause defines ....”) in 33.1:*

This clause specifies Type 1 and Type 2 devices. References to PSEs and PDs without a Type qualifier refer to Type 1 and Type 2 devices. See Clause 145 for the specification of Type 3 and Type 4 devices.

*Change the first sentence in the now third paragraph of 33.1 as follows:*

~~DTE powering~~ Power over Ethernet is intended to provide a 10BASE-T, 100BASE-TX, ~~or~~ 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a single interface to both the data it requires and the power to process this data.

#### **33.1.1 Objectives**

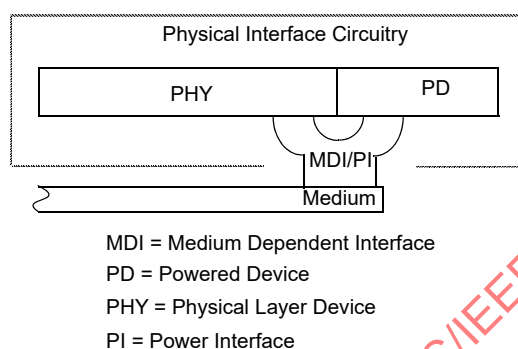
*Change item c) and item d) in 33.1.1 as follows:*

- c) *Compatibility*—Clause 33 utilizes the MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification. Type 1 operation adds no significant requirements to the cabling. Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling and a derating of the cabling maximum ambient operating temperature. ~~The clause does not address the operation of 10GBASE-T. For 10GBASE-T operation, the channel model specified in Clause 55 needs to be met without regard to DTE Power via MDI presence or operation.~~
- d) *Simplicity*—The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, ~~or~~ 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T.

*Change the title and first two paragraphs of 33.1.3 and the titles of Figure 33–1, Figure 33–2, and Figure 33–3 as follows:*

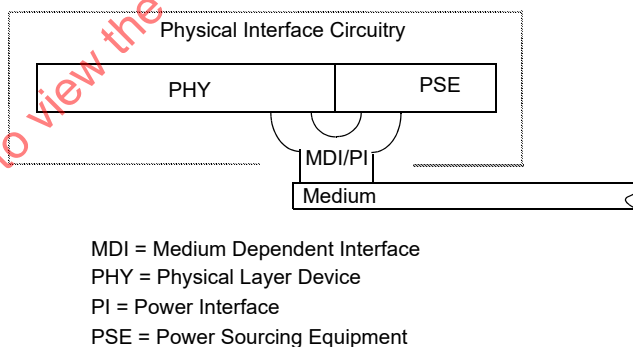
### 33.1.3 Relationship of ~~DTE Power via MDI~~ Power over Ethernet to the IEEE 802.3 Architecture

~~DTE Power via MDI~~ Power over Ethernet comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 33–1 depicts the positioning of ~~DTE Power via MDI~~ Power over Ethernet (PoE) in the case of the PD.

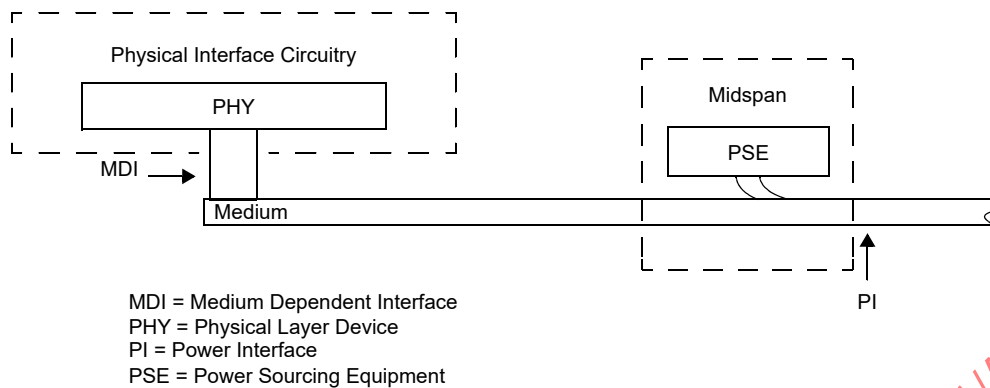


**Figure 33–1—~~DTE Power via MDI~~ PoE powered device relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model**

Figure 33–2 and Figure 33–3 depict the positioning of ~~DTE Power via MDI~~ Power over Ethernet in the cases of the Endpoint PSE and the Midspan PSE, respectively.



**Figure 33–2—~~DTE Power via MDI~~ PoE Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model**



**Figure 33–3—~~DTE Power via MDI PoE~~ Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model**

### 33.2 Power sourcing equipment (PSE)

#### 33.2.1 PSE location

*Change the last paragraph of 33.2.1 as follows:*

The PSEs can be specification is designed to be compatible with any of the following: 10BASE-T, 100BASE-TX, and/or 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T. PSEs may support either Alternative A, Alternative B, or both.

#### 33.2.2 Midspan PSE types

*Change the first paragraph of 33.2.2 as follows:*

There are ~~two types~~ several variants of Midspan PSEs defined:-

*Insert the following new variant descriptions after the “1000BASE-T Midspan PSE” description in 33.2.2:*

##### 2.5GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T and 2.5GBASE-T operation and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

##### 5GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, and 5GBASE-T operation and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

##### 10GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T operation and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

*Change the titles of Figure 33-5 and Figure 33-7 as follows:*

**Figure 33–5—1000/2.5G/5G/10GBASE-T Endpoint PSE location overview**

**Figure 33–7—1000/2.5G/5G/10GBASE-T Midspan PSE location overview**

### 33.3 Powered devices (PDs)

#### 33.3.1 PD PI

*Change the note in 33.3.1 as follows:*

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this clause standard. A PD may indicate the ability to accept power on both pairsets from a Clause 145 PSE using TLV variable PD 4PID; see 79.3.2.4.2a.

### 33.4 Additional electrical specifications

*Change 33.4 as follows:*

This clause defines additional electrical specifications for both the PSE and PD. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 33.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX, ~~and~~ 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T PHYs.

#### 33.4.2 Fault tolerance

*Change the first paragraph of 33.4.2 as follows:*

Each wire pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, ~~and~~ 40.8.3.4, 55.8.2.3, and 126.8.2.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

#### 33.4.3 Impedance balance

*Change the first paragraph of 33.4.3, including the deletion of Equation (33-15) and Equation (33-16), as follows:*

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed the limits in Table 33-19a for all supported PHY speeds.

$$\left\{ 29.0 - 17.0 \times \log_{10} \left( \frac{f}{10.0} \right) \right\} \text{ dB} \quad (33-15)$$

where

$f$  is the frequency in MHz from 1.00 MHz to 20.0 MHz for a 10 Mb/s MAU

$$\left\{ 34.0 - 19.2 \times \log_{10} \left( \frac{f}{50.0} \right) \right\} \text{ dB} \quad (33-16)$$

where

$f$  is the frequency in MHz from 1.00 MHz to 100. MHz for a 100 Mb/s or greater PHY

*Insert Table 33-19a into 33.4.3 after the first paragraph:*

**Table 33-19a—Impedance balance limits for supported speeds**

| Supported speed           | Impedance balance limit (dB)       | Frequency range          |
|---------------------------|------------------------------------|--------------------------|
| 10 Mb/s MAU               | $29 - 17 \times \log_{10}(f/10)$   | $1 \leq f \leq 20$ MHz   |
| 100 Mb/s or 1000 Mb/s PHY | $34 - 19.2 \times \log_{10}(f/50)$ | $1 \leq f \leq 100$ MHz  |
| 2.5 Gb/s PHY              | 48                                 | $1 \leq f < 10$ MHz      |
|                           | $48 - 20 \times \log_{10}(f/10)$   | $10 \leq f < 20$ MHz     |
|                           | $42 - 15 \times \log_{10}(f/20)$   | $20 \leq f \leq 125$ MHz |
| 5 Gb/s PHY                | 48                                 | $1 \leq f < 30$ MHz      |
|                           | $44 - 19.2 \times \log_{10}(f/50)$ | $30 \leq f \leq 250$ MHz |
| 10 Gb/s PHY               | 48                                 | $1 \leq f < 30$ MHz      |
|                           | $44 - 19.2 \times \log_{10}(f/50)$ | $30 \leq f \leq 500$ MHz |

#### 33.4.4 Common-mode output voltage

*Change the first paragraph of 33.4.4 as follows:*

The magnitude of the common-mode AC output voltage measured according to Figure 33-21 and Figure 33-22 at the transmit PI while transmitting data and with power applied,  $E_{\text{cm\_out}}$ , shall not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater. The frequency of the measurement shall be from 1 MHz to 100 MHz, the values in Table 33-19b while operating at the specified speed, when measured over the specified bandwidth.

*Insert Table 33-19b into 33.4.4 after Figure 33-22:*

**Table 33-19b—Common-mode output voltage for given operating speed**

| Operating speed           | Common-mode output voltage ( $E_{\text{cm\_out}}$ ) | Measurement bandwidth   |
|---------------------------|-----------------------------------------------------|-------------------------|
| 10 Mb/s MAU               | 50 mV peak                                          | $1 \leq f \leq 100$ MHz |
| 100 Mb/s or 1000 Mb/s PHY | 50 mV <sub>pp</sub>                                 | $1 \leq f \leq 100$ MHz |
| 2.5 Gb/s PHY              | 50 mV <sub>pp</sub>                                 | $1 \leq f \leq 100$ MHz |
| 5 Gb/s PHY                | 50 mV <sub>pp</sub>                                 | $1 \leq f \leq 250$ MHz |
| 10 Gb/s PHY               | 50 mV <sub>pp</sub>                                 | $1 \leq f \leq 500$ MHz |

### 33.4.6 Differential noise voltage

*Change 33.4.6 as follows:*

~~The~~ For 10/100/1000 Mb/s, the coupled noise,  $E_{d \text{ out}}$  in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4, item 1) and item 2).

For 2.5GBASE-T, 5GBASE-T, or 10GBASE-T, the coupled noise,  $E_{d \text{ out}}$  in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1 mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T under the conditions specified in 33.4.4, item 1) and item 2).

### 33.4.7 Return loss

*Change 33.4.7 as follows:*

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI INCITS 263-1995 for a 100 Mb/s PHY, and in 40.8.3.1 for a 1000 Mb/s PHY, in 126.8.2.2 for a 2.5 Gb/s or 5 Gb/s PHY, and in 55.8.2.1 for a 10 Gb/s PHY. In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75  $\Omega$ . The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

### 33.4.9 Midspan PSE device additional requirements

*Change the third paragraph of 33.4.9 as follows:*

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

- a) If the existing FD configuration is of the “Interconnect model” type, the Midspan PSE can be added, provided it does not increase the length-insertion loss of the resulting “channel” to more than that specified for the same Class or category 100 m channel as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.
- b) If the existing FD configuration is of the “Cross-connect model” type, the Midspan PSE can ~~needs to be~~ installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the length-insertion loss of the resulting “channel” to more than that specified for the same Class or category 100 m channel as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.
- c) For a 10GBASE-T midspan PSE, in meeting either of the above requirements, the Midspan PSE may be substituted for up to two connection pairs in the FD.

*Change 33.4.9.1 and 33.4.9.1.1 through 33.4.9.1.3 as follows:*

#### 33.4.9.1 “Connector” or “telecom outlet” Midspan PSE device transmission requirements

The Midspan PSE equipment to be inserted as “connector” or “telecom outlet” shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO 11801:2002 or ANSI/TIA-568-C.2 for connecting hardware.

There are ~~four types~~ five variants of Midspan PSEs defined with respect to transmission requirements:

- 1) 10BASE-T/100BASE-TX connector ~~or telecom outlet~~ Midspan PSE
- 2) ~~10BASE-T/100BASE-TX work area or equipment cable~~ Midspan PSE
- 3) 1000BASE-T connector ~~or telecom outlet~~ Midspan PSE
- 4) ~~1000BASE-T work area or equipment cable~~ Midspan PSE
- 3) 2.5GBASE-T connector Midspan PSE
- 4) 5GBASE-T connector Midspan PSE
- 5) 10GBASE-T connector Midspan PSE

### 33.4.9.1.1 Near End Crosstalk (NEXT)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. For operation with 1000BASE-T and lower rates, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, For operation with 5GBASE-T and lower rates, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXT_{conn}\}_{dB} \geq 40.0 - 20.0 \times \log_{10}\left(\frac{f}{100}\right) \quad (33-18)$$

where

$NEXT_{conn}$  is the Near End Crosstalk loss  
 $f$  is the frequency expressed in MHz

For 2.5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18a) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18a) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For operation with 2.5GBASE-T and 5GBASE-T, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXT_{conn}\}_{dB} \geq 43 - 20 \times \log_{10}\left(\frac{f}{100}\right) \quad (33-18a)$$

where

$NEXT_{conn}$  is the Near End Crosstalk loss  
 $f$  is the frequency expressed in MHz

For 10GBASE-T operation, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18b) when measured for the transmit and receive pairs from 1 MHz to 500 MHz. However, for frequencies that correspond to calculated values greater than 75 dB, the requirement reverts to the minimum requirement of 75 dB.

$$\{NEXT_{conn}\}_{dB} \leq \left\{ \begin{array}{ll} 54 - 20 \times \log_{10}\left(\frac{f}{100}\right) & \text{for } (1 \leq f \leq 250) \\ 46.04 - 40 \times \log_{10}\left(\frac{f}{250}\right) & \text{for } (250 < f \leq 500) \end{array} \right\}_{dB} \quad (33-18b)$$

where

$NEXT_{conn}$  is the Near End Crosstalk loss in dB  
 $f$  is the frequency expressed in MHz

**33.4.9.1.2 Insertion loss**

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. For other than 5GBASE-T or 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, for 5GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB. For 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured from the transmit and receive pairs from 1 MHz to 500 MHz.

$$\{IL_{conn}\}_{dB} \leq 0.040 \times \sqrt{f} \quad (33-19)$$

where

$IL_{conn}$  is the insertion loss  
 $f$  is the frequency expressed in MHz

**33.4.9.1.3 Return loss**

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 33–20 ~~when measured for the transmit and receive pairs from 1 MHz to 100 MHz.~~

**Table 33–20—Connector return loss**

| Midspan PSE variant      | Frequency                        | Return loss                              |
|--------------------------|----------------------------------|------------------------------------------|
| <u>10/100/1000BASE-T</u> | <u>1 MHz ≤ f &lt; 20 MHz</u>     | <u>23 dB</u>                             |
|                          | <u>20 MHz ≤ f ≤ 100 MHz</u>      | <u>14 dB</u>                             |
| <u>2.5GBASE-T</u>        | <u>1 MHz ≤ f &lt; 31.5 MHz</u>   | <u>30 dB</u>                             |
|                          | <u>31.5 MHz ≤ f &lt; 100 MHz</u> | <u>20 – 20 log<sub>10</sub>(f / 100)</u> |
| <u>5GBASE-T</u>          | <u>1 MHz ≤ f &lt; 31.5 MHz</u>   | <u>30 dB</u>                             |
|                          | <u>31.5 MHz ≤ f ≤ 250 MHz</u>    | <u>20 – 20 log<sub>10</sub>(f / 100)</u> |
| <u>10GBASE-T</u>         | <u>1 MHz ≤ f &lt; 79 MHz</u>     | <u>30 dB</u>                             |
|                          | <u>79 MHz ≤ f ≤ 500 MHz</u>      | <u>28 – 20 log<sub>10</sub>(f / 100)</u> |

*Change the subclause number, title, and text of 33.4.9.1.4 as follows:*

**33.4.9.1a ~~33.4.9.1.4~~ Work area or equipment cable Cord Midspan PSE**

Replacing the work area or equipment cable with a cable that includes a Midspan PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a ~~Category 5–(jumper) cord as specified in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2~~ for insertion loss, NEXT, and return loss for the transmit and receive pairs, as shown in Table 33–20a.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

- 1) 10BASE-T/100BASE-TX cord Midspan PSE
- 2) 1000BASE-T cord Midspan PSE
- 3) 2.5GBASE-T cord Midspan PSE
- 4) 5GBASE-T cord Midspan PSE
- 5) 10GBASE-T cord Midspan PSE

*Insert Table 33-20a into 33.4.9.1a after the second paragraph:*

**Table 33-20a—Cord specifications for use with Midspan PSEs**

| Highest PHY rate supported | Cord specification                                           | Frequency range                           |
|----------------------------|--------------------------------------------------------------|-------------------------------------------|
| Up to 1000BASE-T           | Category 5 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-A:1995 | $1\text{ MHz} \leq f \leq 100\text{ MHz}$ |
| Up to 2.5GBASE-T           | Category 5e cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2   | $1\text{ MHz} \leq f \leq 100\text{ MHz}$ |
| Up to 5GBASE-T             | Category 6 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2    | $1\text{ MHz} \leq f \leq 250\text{ MHz}$ |
| Up to 10GBASE-T            | Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2      | $1\text{ MHz} \leq f \leq 500\text{ MHz}$ |

*Insert the following new subclauses (33.4.9.1a.1, 33.4.9.1a.2, and 33.4.9.1b with its subclauses) after 33.4.9.1a:*

#### **33.4.9.1a.1 Maximum link delay**

The propagation delay contribution of the Midspan PSE device shall not exceed 2.5 ns from 1 MHz to the highest referenced frequency.

#### **33.4.9.1a.2 Maximum link delay skew**

The propagation delay skew of the Midspan PSE device shall not exceed 1.25 ns from 1 MHz to the highest referenced frequency.

#### **33.4.9.1b Coupling parameters between link segments**

Midspan PSEs intended for operation with 2.5G/5G/10GBASE-T (variants 3 through 5 in 33.4.9.1 and 33.4.9.1a) are additionally required to meet the following parameters for coupling signals between ports relating to different link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To bound the total alien NEXT loss and alien FEXT loss coupled between link segments, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss are specified.

**33.4.9.1b.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss**

PSANEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using Equation (33–19a). For other than 5GBASE-T or 10GBASE-T operation, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19a) from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19a) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19a) from 1 MHz to 500 MHz. When the computed PSANEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

$$\text{PSANEXT Loss} = 70.5 - 20\log_{10}(f/100) \quad (33-19a)$$

**33.4.9.1b.2 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss**

PSAFEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using Equation (33–19b). For other than 5GBASE-T or 10GBASE-T operation, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19b) from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19b) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19b) from 1 MHz to 500 MHz. When the computed PSAFEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

$$\text{PSAFEXT Loss} = 67 - 20\log_{10}(f/100) \quad (33-19b)$$

**33.6 Data Link Layer classification****33.6.3 Power control state diagrams****33.6.3.3 Variables**

*Change the second paragraph of the following definitions in 33.6.3.3 as shown:*

MirroredPDRequestedPowerValue

The copy ....

Values: 0 through 255

MirroredPSEAllocatedPowerValue

The copy ....

Values: 0 through 255

PDRequestedPowerValueEcho

This variable ....

Values: 0 through 255

PDRequestedPowerValue

Integer that ....

Values: 0 through PD\_DLLMAX\_VALUE

PSEAllocatedPowerValue

Integer that ....

Values: 0 through 255

PSEAllocatedPowerValueEcho

This variable ....

Values: 0 through 255

*Change the last paragraph of 33.6.3.3 as follows:*

A summary cross-references between the ~~DTE Power via MDI Power over Ethernet~~ classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in [Table 33–23](#).

*Change the title of 33.8 as follows:*

### **33.8 Protocol implementation conformance statement (PICS) proforma for Clause 33, ~~DTE Power via MDI Power over Ethernet over 2 Pairs~~<sup>4</sup>**

#### **33.8.1 Introduction**

*Change the first paragraph of 33.8.1 as follows:*

The supplier of a protocol implementation that is claimed to conform to Clause 33, ~~DTE Power via MDI Power over Ethernet over 2 Pairs~~, shall complete the following protocol implementation conformance statement (PICS) proforma.

#### **33.8.2 Identification**

##### **33.8.2.2 Protocol summary**

*Change 33.8.2.2 as follows:*

|                                                                                                                                                                                     |                                                                                                 |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| Identification of protocol standard                                                                                                                                                 | IEEE Std 802.3bt-2018, Clause 33, <del>DTE Power via MDI Power over Ethernet over 2 Pairs</del> |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS                                                                     |                                                                                                 |
| Have any Exception items been required? No [ ] Yes [ ]<br>(See <a href="#">Clause 21</a> ; the answer Yes means that the implementation does not conform to IEEE Std 802.3bt-2018.) |                                                                                                 |
| Date of Statement                                                                                                                                                                   |                                                                                                 |

<sup>4</sup>Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Change the title of 33.8.3 as follows:

### 33.8.3 PICS proforma tables for ~~DTE Power via MDI~~ **Power over Ethernet over 2 Pairs**

#### 33.8.3.4 Electrical specifications applicable to the PSE and PD

Change the following table rows in 33.8.3.4 as shown (note that unchanged rows are not shown):

| Item  | Feature                                                                           | Subclause | Value/Comment                                                                                                                                                                                                                     | Status | Support |
|-------|-----------------------------------------------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------|
| EL13  | Common-mode to differential-mode impedance balance for transmit and receive pairs | 33.4.3    | <del>Exceeds Equation (33–15) for 10 Mb/s PHYs and Equation (33–16) for 100 Mb/s or greater PHYs</del><br>Exceeds value in Table 33–19a for all supported PHY speeds.                                                             | M      | Yes [ ] |
| EL14  | Common-mode AC output voltage                                                     | 33.4.4    | <del>Magnitude while transmitting data and with power applied does not exceed 50 mV peak when operating at 10 Mb/s and 50 mV peak-to-peak when operating at 100 Mb/s or greater</del><br>Not to exceed the values in Table 33–19b | M      | Yes [ ] |
| EL15  | <del>Frequency range for common-mode AC output voltage measurement</del>          | 33.4.4    | From 1 MHz to 100 MHz                                                                                                                                                                                                             | M      | Yes [ ] |
| EL17a | Coupled noise $E_{d\_out}$                                                        | 33.4.6    | Not to exceed 10 mV peak-to-peak in the band from 1 MHz to 10 MHz                                                                                                                                                                 | M      | Yes [ ] |
| EL17b | Coupled noise $E_{d\_out}$                                                        | 33.4.6    | Not to exceed 10 mV peak-to-peak in the band from 10 MHz to 100 MHz (for 2.5GBASE-T), 10 MHz to 250 MHz (for 5GBASE-T), and 10 MHz to 500 MHz (for 10GBASE-T) under the conditions specified in 33.4.4.                           | M      | Yes [ ] |

## 40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

### 40.6 PMA electrical specifications

#### 40.6.1 PMA-to-MDI interface tests

##### 40.6.1.1 Isolation requirement

*Change the first paragraph of 40.6.1.1 as follows:*

A PHY with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

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## 55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

### 55.5 PMA electrical specifications

#### 55.5.1 Isolation requirement

*Change 55.5.1 as follows:*

A PHY with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

~~The A PHY with a MDI that is not a PI shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall withstand at least one of the following electrical strength tests:~~

- a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.2.2 of IEC 60950-1:2001.
- b) 2250 V dc for 60 s, applied as specified in Section 5.2.2 of IEC 60950-1:2001.
- c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses is 1.2/50  $\mu$ s (1.2  $\mu$ s virtual front time, 50  $\mu$ s virtual time or half value), as defined in Annex N of IEC 60950-1:2001.

There shall be no insulation breakdown, as defined in Section 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 M $\Omega$ , measured at 500 V dc.

## 79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements

### 79.1 Overview

#### 79.1.1 IEEE 802.3 LLDP frame format

##### 79.1.1.3 Length/Type field

*Change 79.1.1.3 as follows:*

The Length/Type field of an IEEE 802.3 LLDP frame is a 2-octet field that contains ~~0x88CC, the hexadecimal value: 88-CC~~. This value carries the Type interpretation (see 3.2.6), and has been universally assigned for LLDP.

### 79.3 IEEE 802.3 Organizationally Specific TLVs

*Change Table 79-1 as follows:*

**Table 79–1—IEEE 802.3 Organizationally Specific TLVs**

| IEEE 802.3 subtype | TLV name                                   | Subclause reference |
|--------------------|--------------------------------------------|---------------------|
| 1                  | MAC/PHY Configuration/Status               | 79.3.1              |
| 2                  | Power Via Medium Dependent Interface (MDI) | 79.3.2              |
| 3                  | Link Aggregation (deprecated)              | 79.3.3              |
| 4                  | Maximum Frame Size                         | 79.3.4              |
| 5                  | Energy-Efficient Ethernet                  | 79.3.5              |
| 6                  | EEE fast wake                              | 79.3.6              |
| 7                  | Additional Ethernet Capabilities           | 79.3.7              |
| 8                  | Power Via MDI Measurements                 | 79.3.8              |
| 9 to 255           | Reserved                                   | —                   |

#### 79.3.2 Power Via MDI TLV

*Change the text of 79.3.2 as follows:*

Clause 33 and Clause 145 defines two optional power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the same generic cabling as used for data transmission. The Power Via MDI TLV allows network management to advertise and discover the Power over Ethernet MDI power support capabilities of the sending IEEE 802.3 LAN station. This TLV is also required to perform Data Link Layer classification as defined in 33.6 and 145.5. Figure 79–3 shows the format of this TLV.

The TLV shown in Figure 79–3 is a revision of the legacy Power via MDI TLV originally defined in IEEE Std 802.1AB-2016 Annex F.3. The legacy TLV had only the first three fields of the TLV shown in the figure. These three fields enable discovery and advertisement of MDI power support capabilities. The newly added fields provide Data Link Layer classification capabilities. The revised TLV can be used by the PSE only when it is supplying power to a PI encompassed within an MDI and by the PD only when it is drawing

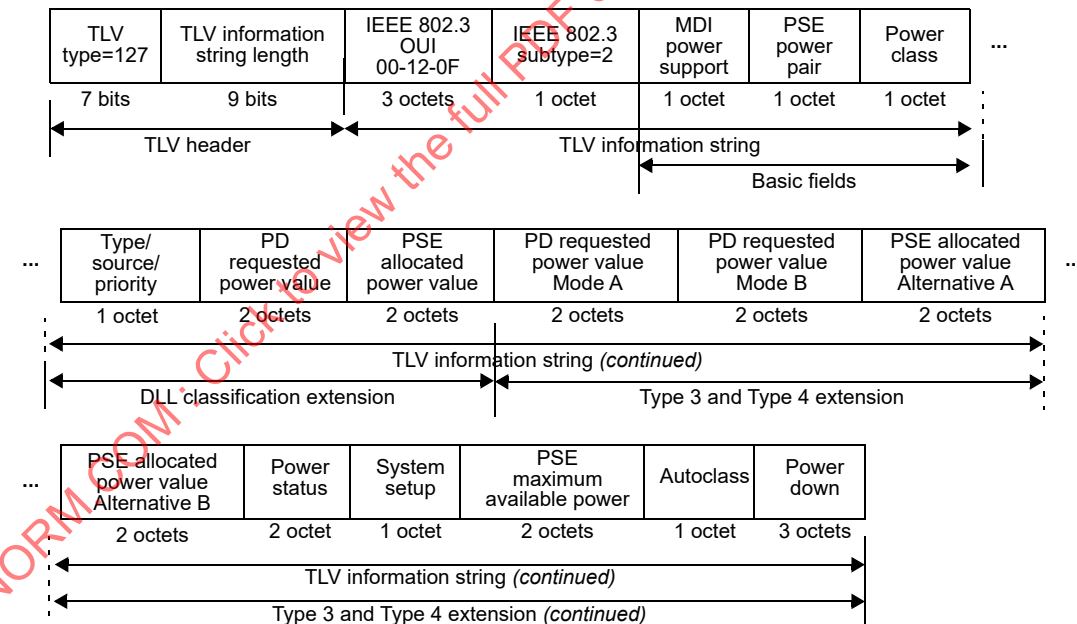
power from the PI. Power entities may continue to use the legacy TLV prior to supplying/drawing power to/from the PI. If the power entity implements Data Link Layer classification, it shall use the Power via MDI TLV shown in Figure 79-3 after the PI has been powered.

The Power via MDI TLV shown in Figure 79-3 was originally defined in IEEE Std 802.1AB-2005 Annex G.3. This original TLV supported only the first three fields of Figure 79-3, labeled basic fields, enabling discovery and advertisement of Power via MDI capabilities. The Power via MDI TLV was revised by IEEE Std 802.3at-2009 to add a further three fields, labeled DLL classification extension, to provide Data Link Layer (DLL) classification capabilities. The Power via MDI TLV was revised again by IEEE Std 802.3bt-2018 to add a further nine fields, labeled Type 3 and Type 4 extension, to support additional capabilities offered by Type 3 and Type 4 PSEs and PDs.

Power entities may continue to use the Power Via MDI TLV basic fields shown in Figure 79-3 prior to supplying/drawing power to/from the Power Interface (PI), as defined in 1.4.406. The DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79-3 shall not be sent by the PSE unless it is supplying power to a PI encompassed within an MDI and by the PD unless it is drawing power from the PI.

If a Type 1 or Type 2 power entity implements Data Link Layer classification, it shall support the Power Via MDI TLV DLL classification extension fields shown in Figure 79-3 after the PI has been powered. If a Type 3 or Type 4 power entity implements Data Link Layer classification, it shall support both the DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79-3 after the PI has been powered. Type 1 and Type 2 devices shall not include the Type 3 and Type 4 extension fields in the transmitted Power via MDI TLV.

Replace Figure 79-3 with the following:



The TLV information string length is

- Basic fields: 7 octets
- Basic fields and DLL classification extension: 12 octets
- Basic fields, DLL classification extension, and Type 3 and Type 4 extension: 29 octets

Figure 79-3—Power Via MDI TLV format

**79.3.2.1 MDI power support**

*Change Table 79-3 as follows:*

**Table 79-3—MDI power capabilities/status support field**

| Bit | Function                            | Value/meaning                                                                    | <del>IETF RFC 3621 object reference</del>     |
|-----|-------------------------------------|----------------------------------------------------------------------------------|-----------------------------------------------|
| 7:4 | Reserved for future standardization | —                                                                                | —                                             |
| 3   | PSE pairs control ability           | 1 = pair selection can be controlled<br>0 = pair selection can not be controlled | <del>pethPsePortPowerPairControlAbility</del> |
| 2   | PSE MDI power state                 | 1 = enabled<br>0 = disabled                                                      | <del>pethPsePortAdminEnable</del>             |
| 1   | PSE MDI power support               | 1 = supported<br>0 = not supported                                               | <del>See Note 2 and Note 3</del>              |
| 0   | Port class                          | 1 = PSE<br>0 = PD                                                                | <del>See Note 1</del>                         |

~~NOTE 1—Port class information is implied by the support of the PSE or PD groups.~~

~~NOTE 2—MDI power support information is implied by support of IETF RFC 3621.~~

~~NOTE 3—If bit 1 is zero, bit 2 has no meaning.~~

*Insert the following new subclauses, 79.3.2.1.1 through 79.3.2.1.4, after 79.3.2.1:*

**79.3.2.1.1 Port class**

The ‘Port class’ field transmitted shall indicate if the port is a PSE or a PD.

**79.3.2.1.2 PSE MDI power support**

The ‘PSE MDI power support’ field transmitted by a PSE shall indicate if MDI power is supported. The value of the ‘PSE MDI power support’ field transmitted by a PD is undefined.

**79.3.2.1.3 PSE MDI power state**

The ‘PSE MDI power state’ field transmitted by a PSE shall indicate if the PSE function is enabled or disabled. When disabled all PSE functions are disabled and behavior is as if there was no PSE functionality. The value of the ‘PSE MDI power state’ field transmitted by a PD is undefined.

**79.3.2.1.4 PSE pairs control ability**

The ‘PSE pairs control ability’ field transmitted by a PSE shall indicate if the PSE has the capability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. The value of the ‘PSE pairs control ability’ field transmitted by a PD is undefined.

### 79.3.2.2 PSE power pair

*Change the text of 79.3.2.2 as follows:*

~~The PSE power pair field shall contain an integer value as defined by the pethPsePortPowerPairs object in IETF RFC 3621.~~

The ‘PSE power pair’ field transmitted by a PSE shall contain an integer value as defined in Table 79–3a based on aPSEPowerPairs (see 30.9.1.1.4). A Type 3 or Type 4 PSE that is supplying power on a single pairset shall use the value that defines that pairset. Either pairset may be indicated when a PSE is detecting or supplying power on both pairsets. The ‘PSE power status value’ field defined in 79.3.2.6c indicates when a PSE is supplying power on both pairsets. The value of the ‘PSE power pair’ field transmitted by a PD is undefined.

*Insert Table 79-3a at the end of 79.3.2.2:*

**Table 79–3a—PSE power pair field**

| Value | Meaning | Alternative   |
|-------|---------|---------------|
| 1     | signal  | Alternative A |
| 2     | spare   | Alternative B |

### 79.3.2.3 Power class

*Change the text of 79.3.2.3 as follows:*

~~The power class field shall contain an integer value as defined by the pethPsePortPowerClassifications object in IETF RFC 3621.~~

The ‘Power class’ field transmitted by a PSE shall contain an integer value as defined in Table 79–3b based on aPSEPowerClassification (see 30.9.1.1.6). Class 4 and above is indicated with the same value in this field. Class 5 and above is communicated by the ‘Power Class ext’ field defined in 79.3.2.6c.6. The ‘Power class’ field transmitted by a PD is undefined.

*Insert Table 79-3b at the end of 79.3.2.3:*

**Table 79–3b—Power class field**

| Value | Meaning              |
|-------|----------------------|
| 1     | Class 0 PD           |
| 2     | Class 1 PD           |
| 3     | Class 2 PD           |
| 4     | Class 3 PD           |
| 5     | Class 4 and above PD |

Change 79.3.2.4 as follows:

#### 79.3.2.4 Requested ~~p~~Power type/source/priority

The ~~power~~ 'Power type/source/priority' field shall contain a bit-map of the Power type, source, and priority defined in Table 79-4 and is reported for the device generating the TLV.

Table 79-4—Power type/source/priority field

| Bit | Function                    | Value/meaning                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | <del>p</del> Power type     | $\begin{array}{cc} 7 & 6 \\ 1 & 1 = \text{Type 1 PD} \\ 1 & 0 = \text{Type 1 PSE} \\ 0 & 1 = \text{Type 2 PD} \\ 0 & 0 = \text{Type 2 PSE} \end{array}$                                                                                                                                                                                                                                               |
| 5:4 | <del>p</del> Power source   | <p>Where <del>p</del>Power type = PD</p> $\begin{array}{cc} 5 & 4 \\ 1 & 1 = \text{PSE and local} \\ 1 & 0 = \text{Reserved} \\ 0 & 1 = \text{PSE} \\ 0 & 0 = \text{Unknown} \end{array}$ <p>Where <del>p</del>Power type = PSE</p> $\begin{array}{cc} 5 & 4 \\ 1 & 1 = \text{Reserved} \\ 1 & 0 = \text{Backup source} \\ 0 & 1 = \text{Primary power source} \\ 0 & 0 = \text{Unknown} \end{array}$ |
| 3:2 | Reserved                    | Transmit as zero, ignore on receive                                                                                                                                                                                                                                                                                                                                                                   |
| 2   | <u>PD 4PID</u>              | <u>1 = PD supports powering of both Modes simultaneously</u><br><u>0 = PD does not support powering of both Modes simultaneously</u>                                                                                                                                                                                                                                                                  |
| 1:0 | <del>p</del> Power priority | $\begin{array}{cc} 1 & 0 \\ 1 & 1 = \text{low} \\ 1 & 0 = \text{high} \\ 0 & 1 = \text{critical} \\ 0 & 0 = \text{unknown (default)} \end{array}$                                                                                                                                                                                                                                                     |

#### 79.3.2.4.1 Power type

Change 79.3.2.4.1 as follows:

This field shall be set according to Table 79-4. Type 3 or Type 4 PSEs shall set this field to the value corresponding with Type 2 PSEs. Type 3 or Type 4 PDs shall set this field to the value corresponding with Type 2 PDs.

Insert the following new subclause, 79.3.2.4.2a, after 79.3.2.4.2:

#### 79.3.2.4.2a PD 4PID

This field shall be set according to Table 79-4 when the Power type is PD to indicate whether the PD supports powering of both Modes simultaneously. This field shall be set to '0' when the Power type is PSE.

**79.3.2.5 PD requested power value***Change 79.3.2.5 as follows:*

The ‘PD requested power value’ field shall contain the PD’s requested power value defined in Table 79–5.  
See 33.6.3.3 and Table 145–42 for permitted value ranges.

**Table 79–5—PD requested power value field**

| Bit  | Function                 | Value/meaning                                                                                                                                                        |
|------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PD requested power value | <del>Power = 0.1 × (decimal value of bits) Watts.</del><br><u>Power expressed in units of 0.1 W.</u><br>Valid values for these bits are decimal 1–0 through 255–999. |

The PD requested power value is encoded according to Equation (79–1).

$$Power = \{0.1 \times X\}_W \quad (79-1)$$

where

*Power* is the effective requested PD power value

*X* is the decimal value of the power value field, bits 15:0

“PD requested power value” is the maximum input average power (see 33.3.7.2 and 145.3.8.2) the PD wants to draw is requesting. “PD requested power value” is the power value at the input to the PD’s PI. A value higher than 713 requires the PSE to support a power level higher than  $P_{Class\_PD}$  at the PD PI. See 145.2.8 and 145.3.8.2.

**79.3.2.6 PSE allocated power value***Change 79.3.2.6 as follows:*

The ‘PSE allocated power value’ field shall contain the PSE’s allocated power value defined in Table 79–6.  
See 33.6.3.3 and Table 145–41 for permitted value ranges.

**Table 79–6—PSE allocated power value field**

| Bit  | Function                  | Value/meaning                                                                                                                                                        |
|------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PSE allocated power value | <del>Power = 0.1 × (decimal value of bits) Watts.</del><br><u>Power expressed in units of 0.1 W.</u><br>Valid values for these bits are decimal 1–0 through 255–999. |

The PSE allocated power value is encoded according to Equation (79–2).

$$Power = \{0.1 \times X\}_W \quad (79-2)$$

where

*Power* is the effective allocated PSE power value

*X* is the decimal value of the power value field, bits 15:0

“PSE allocated power value” is the maximum input average power (see 33.3.7.2 and 145.3.8.2) the PSE expects the PD to draw. “PSE allocated power value” is the power at the input to the PD’s PI. The PSE uses this value to compute  $P_{Class}$  defined in 33.2.6 and 145.2.8. A value higher than 713 indicates that the PSE is capable of supporting a power level beyond  $P_{Class\_PD}$  at the PD PI. This may require an output power level higher than  $P_{Type\_min}$ . See 145.2.8.

*Insert the following new subclauses, 79.3.2.6a through 79.3.2.6g with their subclauses, after 79.3.2.6:*

#### 79.3.2.6a Dual-signature PD requested power value for Mode A and Mode B

The ‘PD requested power value Mode A’ field and ‘PD requested power value Mode B’ field shall contain the PD requested power value defined in Table 79–6a for Mode A and in Table 79–6b for Mode B of a dual-signature PD.

**Table 79–6a—PD requested power value Mode A field**

| Bit  | Function                                           | Value/meaning                                                                                |
|------|----------------------------------------------------|----------------------------------------------------------------------------------------------|
| 15:0 | Dual-signature PD requested power value for Mode A | Power expressed in units of 0.1 W.<br>Valid values for these bits are decimal 0 through 499. |

**Table 79–6b—PD requested power value Mode B field**

| Bit  | Function                                           | Value/meaning                                                                                |
|------|----------------------------------------------------|----------------------------------------------------------------------------------------------|
| 15:0 | Dual-signature PD requested power value for Mode B | Power expressed in units of 0.1 W.<br>Valid values for these bits are decimal 0 through 499. |

The ‘PD requested power value Mode A’ field and ‘PD requested power value Mode B’ field are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

#### 79.3.2.6b PSE allocated power value Alternative A and Alternative B

The ‘PSE allocated power value Alternative A’ field and the ‘PSE allocated power value Alternative B’ field shall contain the values in Table 79–6c and Table 79–6d for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.

**Table 79–6c—PSE allocated power value Alternative A field**

| Bit  | Function                                    | Value/meaning                                                                                |
|------|---------------------------------------------|----------------------------------------------------------------------------------------------|
| 15:0 | PSE allocated power value for Alternative A | Power expressed in units of 0.1 W.<br>Valid values for these bits are decimal 0 through 499. |

**Table 79–6d—PSE allocated power value Alternative B field**

| Bit  | Function                                    | Value/meaning                                                                                |
|------|---------------------------------------------|----------------------------------------------------------------------------------------------|
| 15:0 | PSE allocated power value for Alternative B | Power expressed in units of 0.1 W.<br>Valid values for these bits are decimal 0 through 499. |

The ‘PSE allocated power value Alternative A’ and ‘PSE allocated power value Alternative B’ fields are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives when the PSE provides power over 4-pair. These fields are the power levels at the dual-signature PD PI. The PSE uses these values to compute  $P_{\text{Class-2P}}$  as defined in 145.2.8.

### 79.3.2.6c Power status

The ‘Power status’ field contains the PSE's bit-map of the PSE power pair and PSE or PD power class, defined in Table 79–6e, and is reported for the device generating the TLV.

**Table 79–6e—Power status field**

| Bit   | Function                              | Value/meaning                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | PSE powering status                   | $\begin{array}{cc} \underline{15} & \underline{14} \\ 1 & 1 = 4\text{-pair powering dual-signature PD} \\ 1 & 0 = 4\text{-pair powering single-signature PD} \\ 0 & 1 = 2\text{-pair powering} \\ 0 & 0 = \text{Reserved/Ignore} \end{array}$                                                                                                                                 |
| 13:12 | PD powered status                     | $\begin{array}{cc} \underline{13} & \underline{12} \\ 1 & 1 = 4\text{-pair powered dual-signature PD} \\ 1 & 0 = 2\text{-pair powered dual-signature PD} \\ 0 & 1 = \text{Powered single-signature PD} \\ 0 & 0 = \text{Reserved/Ignore} \end{array}$                                                                                                                         |
| 11:10 | PSE power pairs ext                   | $\begin{array}{cc} \underline{11} & \underline{10} \\ 1 & 1 = \text{Both Alternatives} \\ 1 & 0 = \text{Alternative B} \\ 0 & 1 = \text{Alternative A} \\ 0 & 0 = \text{Reserved/Ignore} \end{array}$                                                                                                                                                                         |
| 9:7   | Dual-signature power Class ext Mode A | $\begin{array}{ccc} \underline{9} & \underline{8} & \underline{7} \\ 1 & 1 & 1 = \text{Single-signature PD or 2-pair only PSE} \\ 1 & 1 & 0 = \text{Reserved/Ignore} \\ 1 & 0 & 1 = \text{Class 5} \\ 1 & 0 & 0 = \text{Class 4} \\ 0 & 1 & 1 = \text{Class 3} \\ 0 & 1 & 0 = \text{Class 2} \\ 0 & 0 & 1 = \text{Class 1} \\ 0 & 0 & 0 = \text{Reserved/Ignore} \end{array}$ |
| 6:4   | Dual-signature power Class ext Mode B | $\begin{array}{ccc} \underline{6} & \underline{5} & \underline{4} \\ 1 & 1 & 1 = \text{Single-signature PD or 2-pair only PSE} \\ 1 & 1 & 0 = \text{Reserved/Ignore} \\ 1 & 0 & 1 = \text{Class 5} \\ 1 & 0 & 0 = \text{Class 4} \\ 0 & 1 & 1 = \text{Class 3} \\ 0 & 1 & 0 = \text{Class 2} \\ 0 & 0 & 1 = \text{Class 1} \\ 0 & 0 & 0 = \text{Reserved/Ignore} \end{array}$ |

**Table 79–6e—Power status field (continued)**

| Bit | Function        | Value/meaning                                                                    |
|-----|-----------------|----------------------------------------------------------------------------------|
| 3:0 | Power Class ext | $\begin{matrix} 3 & 2 & 1 & 0 \\ 1 & 1 & 1 & 1 \end{matrix}$ = Dual-signature PD |
|     |                 | $\begin{matrix} 1 & 1 & 1 & 0 \end{matrix}$ = Reserved/Ignore                    |
|     |                 | $\begin{matrix} 1 & 1 & 0 & 1 \end{matrix}$ = Reserved/Ignore                    |
|     |                 | $\begin{matrix} 1 & 1 & 0 & 0 \end{matrix}$ = Reserved/Ignore                    |
|     |                 | $\begin{matrix} 1 & 0 & 1 & 1 \end{matrix}$ = Reserved/Ignore                    |
|     |                 | $\begin{matrix} 1 & 0 & 1 & 0 \end{matrix}$ = Reserved/Ignore                    |
|     |                 | $\begin{matrix} 1 & 0 & 0 & 1 \end{matrix}$ = Reserved/Ignore                    |
|     |                 | $\begin{matrix} 1 & 0 & 0 & 0 \end{matrix}$ = Class 8                            |
|     |                 | $\begin{matrix} 0 & 1 & 1 & 1 \end{matrix}$ = Class 7                            |
|     |                 | $\begin{matrix} 0 & 1 & 1 & 0 \end{matrix}$ = Class 6                            |
|     |                 | $\begin{matrix} 0 & 1 & 0 & 1 \end{matrix}$ = Class 5                            |
|     |                 | $\begin{matrix} 0 & 1 & 0 & 0 \end{matrix}$ = Class 4                            |
|     |                 | $\begin{matrix} 0 & 0 & 1 & 1 \end{matrix}$ = Class 3                            |
|     |                 | $\begin{matrix} 0 & 0 & 1 & 0 \end{matrix}$ = Class 2                            |
|     |                 | $\begin{matrix} 0 & 0 & 0 & 1 \end{matrix}$ = Class 1                            |
|     |                 | $\begin{matrix} 0 & 0 & 0 & 0 \end{matrix}$ = Reserved/Ignore                    |

**79.3.2.6c.1 PSE powering status**

The ‘PSE powering status’ field is used to indicate the existing powering configuration as shown in Table 145–41 and thus to indicate that the PSE is using the ‘PSE allocated power value’ field or is using the ‘PSE allocated power value Alternative A’ field and ‘PSE allocated power value Alternative B’ field as specified in Table 79–6c and Table 79–6d. A PSE shall set this field according to the current powering status as defined in Table 79–6e. A PD shall set the field to 0.

**79.3.2.6c.2 PD powered status**

The ‘PD powered status’ field is used to indicate the existing powered configuration of the PD as shown in Table 145–42 and thus to indicate that the PD is using the ‘PD requested power value’ field or is using the ‘PD requested power value Mode A’ field and the ‘PD requested power value Mode B’ field as specified in Table 79–6a and Table 79–6b. A PD shall set this field according to its signature configuration and the current powering status as defined in Table 79–6e. A PSE shall set the field to 0.

**79.3.2.6c.3 PSE power pairs ext**

The ‘PSE power pairs ext’ field shall contain the powering status of the PSE, as defined in Table 79–6e. A PD shall set the field to 0.

**79.3.2.6c.4 Dual-signature power Class ext Mode A**

A single-signature PD shall set this field to value 7. A dual-signature PD shall set this field per its requested Class on Mode A defined in 145.3.6. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to value 7. A PSE connected to a dual-signature PD shall set this field to the PSEs assigned Class for Alternative A as defined in 145.2.8.

**79.3.2.6c.5 Dual-signature power Class ext Mode B**

A single-signature PD shall set this field to value 7. A dual-signature PD shall set this field per its requested Class on Mode B defined in 145.3.6. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to value 7. A PSE connected to a dual-signature PD shall set this field to the PSEs assigned Class for Alternative B as defined in 145.2.8.

**79.3.2.6c.6 Power Class ext**

A single-signature PD shall set this field per its requested Class as defined in 145.3.6. A dual-signature PD shall set this field to value 15. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to the PSEs assigned Class as defined in 145.2.8. A PSE connected to a dual-signature PD shall set this field to value 15.

**79.3.2.6d System setup**

The ‘System setup’ field shall contain the device bit-map of the Power Type ext and PD Load defined in Table 79–6f and is reported for the device generating the TLV.

**Table 79–6f—System setup field**

| Bit           | Function       | Value/meaning                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                              |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
|---------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|---------------|---------------|---------------------|---|---|---|---------------------|---|---|---|----------------------------|---|---|---|------------------------------|---|---|---|----------------------------|---|---|---|------------------------------|---|---|---|--------------|---|---|---|--------------|
| 7:4           | Reserved       | Transmit as zero. Ignore on receive.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                              |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 3:1           | Power Type ext | <table><tr><td><math>\frac{3}{1}</math></td><td><math>\frac{2}{1}</math></td><td><math>\frac{1}{1}</math></td><td>= Reserved / ignore</td></tr><tr><td>1</td><td>1</td><td>0</td><td>= Reserved / ignore</td></tr><tr><td>1</td><td>0</td><td>1</td><td>= Type 4 dual-signature PD</td></tr><tr><td>1</td><td>0</td><td>0</td><td>= Type 4 single-signature PD</td></tr><tr><td>0</td><td>1</td><td>1</td><td>= Type 3 dual-signature PD</td></tr><tr><td>0</td><td>1</td><td>0</td><td>= Type 3 single-signature PD</td></tr><tr><td>0</td><td>0</td><td>1</td><td>= Type 4 PSE</td></tr><tr><td>0</td><td>0</td><td>0</td><td>= Type 3 PSE</td></tr></table> | $\frac{3}{1}$                | $\frac{2}{1}$ | $\frac{1}{1}$ | = Reserved / ignore | 1 | 1 | 0 | = Reserved / ignore | 1 | 0 | 1 | = Type 4 dual-signature PD | 1 | 0 | 0 | = Type 4 single-signature PD | 0 | 1 | 1 | = Type 3 dual-signature PD | 0 | 1 | 0 | = Type 3 single-signature PD | 0 | 0 | 1 | = Type 4 PSE | 0 | 0 | 0 | = Type 3 PSE |
| $\frac{3}{1}$ | $\frac{2}{1}$  | $\frac{1}{1}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | = Reserved / ignore          |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 1             | 1              | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Reserved / ignore          |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 1             | 0              | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Type 4 dual-signature PD   |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 1             | 0              | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Type 4 single-signature PD |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 0             | 1              | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Type 3 dual-signature PD   |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 0             | 1              | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Type 3 single-signature PD |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 0             | 0              | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Type 4 PSE                 |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 0             | 0              | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | = Type 3 PSE                 |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |
| 0             | PD Load        | <p>1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated.</p> <p>0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                      |                              |               |               |                     |   |   |   |                     |   |   |   |                            |   |   |   |                              |   |   |   |                            |   |   |   |                              |   |   |   |              |   |   |   |              |

**79.3.2.6d.1 Power Type ext**

This field shall be set according to Table 79–6f.

**79.3.2.6d.2 PD Load**

This field shall be set according to Table 79–6f when the Power type is PD. This field shall be set to 0 when the Power type is PSE. See 145.4.1 for details.

**79.3.2.6e PSE maximum available power value**

The ‘PSE maximum available power value’ field shall contain the highest power the PSE can grant as defined in Table 79–6g. The PSE sets the value of this field taking available power budget and hardware capabilities into account. When connected to a dual-signature PD this value refers to the total amount of

power available at the PI, even though power is allocated separately on a per pairset basis. A PD shall set this field to 0.

**Table 79–6g—PSE maximum available power value field**

| Bit  | Function                          | Value/meaning                                                                        |
|------|-----------------------------------|--------------------------------------------------------------------------------------|
| 15:0 | PSE maximum available power value | Power expressed in units of 0.1 W.<br>Valid values for these bits are 1 through 999. |

### 79.3.2.6f Autoclass

The ‘Autoclass’ field shall contain the bits defined in Table 79–6h to control Autoclass. See 145.2.8.2 and 145.3.6.2 for details on Autoclass. Using the ‘Autoclass’ field to trigger a new Autoclass measurement allows a PD to change maximum power consumption.

**Table 79–6h—Autoclass field**

| Bit | Function              | Value/meaning                                                    |
|-----|-----------------------|------------------------------------------------------------------|
| 7:3 | Reserved              | Transmit as zero. Ignore on receive.                             |
| 2   | PSE Autoclass support | 1 = PSE supports Autoclass<br>0 = PSE does not support Autoclass |
| 1   | Autoclass completed   | 1 = Autoclass measurement completed<br>0 = Autoclass idle        |
| 0   | Autoclass request     | 1 = PD requests Autoclass measurement<br>0 = Autoclass idle      |

#### 79.3.2.6f.1 PSE Autoclass support

When the Power type is PSE, this field shall be set to indicate if the PSE supports Autoclass over DLL according to Table 79–6h. When the Power type is PD, this field shall be set to 0.

#### 79.3.2.6f.2 Autoclass completed

When the Power type is PSE, this field shall be set to indicate that the PSE has concluded the Autoclass measurement. This happens after a request for Autoclass is made by the PD using the ‘Autoclass request’ field defined in Table 79–6h. When the Power type is PD, this field shall be set to 0.

#### 79.3.2.6f.3 Autoclass request

When the Power type is PD, this field may be set to 1 to request a Autoclass measurement by the PSE. The PD sets this field when it is in a state where it consumes its maximum amount of power. In all other cases, the PD sets this field to 0. When the Power type is PSE, this field shall be set to 0.

**79.3.2.6g Power down**

The ‘Power down’ field shall contain the bits defined in Table 79–6i. The ‘Power down’ field allows the PD to request power delivery to be terminated, either indefinitely or for a certain period of time.

**Table 79–6i—Power down field**

| Bit   | Function           | Value/meaning                                                                                                                                                   |
|-------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:18 | Power down request | Value = 0x1D requests a power down.<br>Any other value is ignored.                                                                                              |
| 17:0  | Power down time    | The amount of time in seconds the PD requests to be unpowered.<br>A value of zero means to remain unpowered indefinitely.<br>Valid values are 0 through 262143. |

**79.3.2.6g.1 Power down request**

When the Power type is PD, this field may be set to 0x1D to indicate a request for power down. If power is to be maintained, the field shall be set to 0. When the Power type is PSE, this field shall be set to 0.

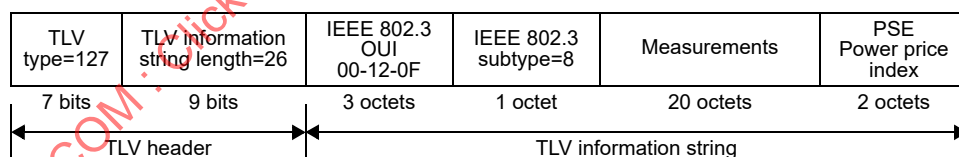
**79.3.2.6g.2 Power down time**

This field controls the amount of time in seconds the PD is requesting to be unpowered. When the Power type is PD, this field shall be set per the description in Table 79–6i. When the Power type is PSE, this field shall be set to 0.

*Insert the following new subclause, 79.3.8 with its subclauses, after 79.3.7.2:*

**79.3.8 Power via MDI Measurements TLV**

Clause 33 and Clause 145 define two optional power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the same generic cabling as used for data transmission. The Power Via MDI Measurement TLV allows network management to read electrical measurement data from the sending IEEE 802.3 LAN station. Figure 79–9 shows the format of this TLV.

**Figure 79–9—Power Via MDI Measurements TLV format for Type 3 and Type 4****79.3.8.1 Measurements**

This field shall be set according to Table 79–8a.

The ‘Voltage measurement’ field carries the measured voltage value at the PI, the ‘Current measurement’ field carries the measured current value at the PI, the ‘Power measurement’ field carries the measured power value at the PI, and the ‘Energy measurement’ field carries the measured energy consumption value at the PI, as defined in Table 79–8a.

Measurement values (voltage, current, power, or energy) shall be set to 0 in case the corresponding request bit is 0. If a device does not support a particular measurement, the corresponding measurement value shall be set to 0.

**Table 79–8a—Measurements**

| Bit     | Function                  | Value/meaning                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 159     | Voltage support           | 1 = Device supports voltage measurement<br>0 = Device does not support voltage measurement                                                                                                                                                                                                                                                                                                    |
| 158     | Current support           | 1 = Device supports current measurement<br>0 = Device does not support current measurement                                                                                                                                                                                                                                                                                                    |
| 157     | Power support             | 1 = Device supports power measurement<br>0 = Device does not support power measurement                                                                                                                                                                                                                                                                                                        |
| 156     | Energy support            | 1 = Device supports energy measurement<br>0 = Device does not support energy measurement                                                                                                                                                                                                                                                                                                      |
| 155:154 | Reserved                  |                                                                                                                                                                                                                                                                                                                                                                                               |
| 153:152 | Measurement source        | Determine where the measurement is to be taken.<br><div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <u>153</u><br/>0<br/>0<br/>1<br/>1 </div> <div style="text-align: center;"> <u>152</u><br/>0<br/>1<br/>0<br/>1 </div> <div> No request<br/> Pairset Alternative A / Mode A<br/> Pairset Alternative B / Mode B<br/> Port total </div> </div> |
| 151     | Voltage request           | 1 = Request for voltage measurement<br>0 = No request for voltage measurement                                                                                                                                                                                                                                                                                                                 |
| 150     | Current request           | 1 = Request for current measurement<br>0 = No request for current measurement                                                                                                                                                                                                                                                                                                                 |
| 149     | Power request             | 1 = Request for power measurement<br>0 = No request for power measurement                                                                                                                                                                                                                                                                                                                     |
| 148     | Energy request            | 1 = Request for energy measurement<br>0 = No request for energy measurement                                                                                                                                                                                                                                                                                                                   |
| 147     | Voltage measurement valid | 1 = Voltage measurement field contains valid data<br>0 = Voltage measurement disabled                                                                                                                                                                                                                                                                                                         |
| 146     | Current measurement valid | 1 = Current measurement field contains valid data<br>0 = Current measurement disabled                                                                                                                                                                                                                                                                                                         |
| 145     | Power measurement valid   | 1 = Power measurement field contains valid data<br>0 = Power measurement disabled                                                                                                                                                                                                                                                                                                             |
| 144     | Energy measurement valid  | 1 = Energy measurement field contains valid data<br>0 = Energy measurement disabled                                                                                                                                                                                                                                                                                                           |
| 143:128 | Voltage uncertainty       | Expanded uncertainty (coverage factor $k = 2$ ) for the voltage measurement, expressed in units of 1 mV.<br>Valid values are 1 through 65000.                                                                                                                                                                                                                                                 |
| 127:112 | Current uncertainty       | Expanded uncertainty (coverage factor $k = 2$ ) for the current measurement, expressed in units of 0.1 mA.<br>Valid values are 1 through 65000.                                                                                                                                                                                                                                               |

Table 79–8a—Measurements (continued)

| Bit    | Function            | Value/meaning                                                                                                                                                                                                                           |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 111:96 | Power uncertainty   | Expanded uncertainty (coverage factor $k = 2$ ) for the power measurement, expressed in units of 10 mW.<br>Valid values are 1 through 65000.                                                                                            |
| 95:80  | Energy uncertainty  | Expanded uncertainty (coverage factor $k = 2$ ) for the energy measurement, expressed in units of 0.1 kJ.<br>Valid values are 1 through 65000.                                                                                          |
| 79:64  | Voltage measurement | $V_{\text{Port\_PD-2P}}$ expressed in units of 1 mV. When the Measurement source is set to 'Port total' this field contains the measurement of the pairset with the highest voltage.<br>Valid values are 0 through 65000 <sup>a</sup> . |
| 63:48  | Current measurement | $I_{\text{Port}}$ or $I_{\text{Port-2P}}$ expressed in units of 0.1 mA.<br>Valid values are 0 through 20000.                                                                                                                            |
| 47:32  | Power measurement   | Power sourced or drawn expressed in units of 10 mW.<br>Valid values are 0 through 10000.                                                                                                                                                |
| 31:0   | Energy measurement  | Energy consumed at the port or pairset expressed in units of 0.1 kJ since power on.<br>Valid values are 0 through 4294967295.                                                                                                           |

<sup>a</sup> The valid range of this field extends beyond the allowed operating range of  $V_{\text{Port\_PD-2P}}$ ; see 33.3.8.1 and 145.3.8.1.

### 79.3.8.2 PSE power price index

The 'PSE power price index' field shall contain an index of the current price of electricity compared to what the PSE considers the nominal electricity price. The determination of the nominal electricity price is implementation dependent. The field is encoded as defined in Equation (79–1). The PSE sets the value of this field taking the availability of power from any external and internal resources, and the relative supply and demand balance, into account. A value of 0xFFFF means that no power price index is available.

$$K_{\text{PPI}} = \left( \frac{(\text{Power price index} + 10046) \times 2.512}{75046} \right)^5 \quad (79-1)$$

where

$K_{\text{PPI}}$  is the power price index expressed as a factor ranging from 0.0004 to 100 times the nominal price  
Power price index is the value of the 'Power price index' field defined in Table 79–8b

Table 79–8b—Power price index

| Bit  | Function          | Value/meaning                                                                          |
|------|-------------------|----------------------------------------------------------------------------------------|
| 15:0 | Power price index | Valid values for these bits are decimal 0 through 65000, and hexadecimal value 0xFFFF. |

**79.3.8.3 Power Via MDI Measurements TLV usage rules**

An LLDPDU should contain no more than one Power Via MDI Measurements TLV.

**79.4 IEEE 802.3 Organizationally Specific TLV selection management****79.4.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references**

*Insert the following new rows into Table 79-10 at the end of the “Power via MDI” TLV name group:*

**Table 79-10—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references**

| TLV name      | TLV variable                            | LLDP Local System Group managed object class attribute |
|---------------|-----------------------------------------|--------------------------------------------------------|
| Power via MDI | PD requested power value Mode A         | aLldpXdot3LocPDRequestedPowerValueA                    |
|               | PD requested power value Mode B         | aLldpXdot3LocPDRequestedPowerValueB                    |
|               | PSE allocated power value Alternative A | aLldpXdot3LocPSEAllocatedPowerValueA                   |
|               | PSE allocated power value Alternative B | aLldpXdot3LocPSEAllocatedPowerValueB                   |
|               | PSE powering status                     | aLldpXdot3LocPSEPoweringStatus                         |
|               | PD powered status                       | aLldpXdot3LocPDPoweredStatus                           |
|               | PSE power pairs ext                     | aLldpXdot3LocPowerPairsExt                             |
|               | Dual-signature power Class ext Mode A   | aLldpXdot3LocPowerClassExtA                            |
|               | Dual-signature power Class ext Mode B   | aLldpXdot3LocPowerClassExtB                            |
|               | Power class ext                         | aLldpXdot3LocPowerClassExt                             |
|               | Power Type ext                          | aLldpXdot3LocPowerTypeExt                              |
|               | PD 4PID                                 | aLldpXdot3LocPD4PID                                    |
|               | PD Load                                 | aLldpXdot3LocPDLLoad                                   |
|               | PSE maximum available power value       | aLldpXdot3LocPSEMaxAvailPower                          |
|               | PSE Autoclass support                   | aLldpXdot3LocPSEAutoclassSupport                       |
|               | Autoclass completed                     | aLldpXdot3LocAutoclassCompleted                        |
|               | Autoclass request                       | aLldpXdot3LocAutoclassRequest                          |
|               | Power down request                      | aLldpXdot3LocPowerDownRequest                          |
|               | Power down time                         | aLldpXdot3LocPowerDownTime                             |

*Insert the following new TLV name group into Table 79-10 after the “Power via MDI” TLV name group (and before the “Link Aggregation (deprecated)” row):*

**Table 79–10—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references (continued)**

| TLV name                   | TLV variable              | LLDP Local System Group managed object class attribute |
|----------------------------|---------------------------|--------------------------------------------------------|
| Power via MDI Measurements | Voltage support           | aLldpXdot3LocMeasVoltageSupport                        |
|                            | Current support           | aLldpXdot3LocMeasCurrentSupport                        |
|                            | Power support             | aLldpXdot3LocMeasPowerSupport                          |
|                            | Energy support            | aLldpXdot3LocMeasEnergySupport                         |
|                            | Measurement source        | aLldpXdot3LocMeasurementSource                         |
|                            | Voltage request           | aLldpXdot3LocMeasVoltageRequest                        |
|                            | Current request           | aLldpXdot3LocMeasCurrentRequest                        |
|                            | Power request             | aLldpXdot3LocMeasPowerRequest                          |
|                            | Energy request            | aLldpXdot3LocMeasEnergyRequest                         |
|                            | Voltage measurement valid | aLldpXdot3LocMeasVoltageValid                          |
|                            | Current measurement valid | aLldpXdot3LocMeasCurrentValid                          |
|                            | Power measurement valid   | aLldpXdot3LocMeasPowerValid                            |
|                            | Energy measurement valid  | aLldpXdot3LocMeasEnergyValid                           |
|                            | Voltage uncertainty       | aLldpXdot3LocMeasVoltageUncertainty                    |
|                            | Current uncertainty       | aLldpXdot3LocMeasCurrentUncertainty                    |
|                            | Power uncertainty         | aLldpXdot3LocMeasPowerUncertainty                      |
|                            | Energy uncertainty        | aLldpXdot3LocMeasEnergyUncertainty                     |
|                            | Voltage measurement       | aLldpXdot3LocVoltageMeasurement                        |
|                            | Current measurement       | aLldpXdot3LocCurrentMeasurement                        |
|                            | Power measurement         | aLldpXdot3LocPowerMeasurement                          |
|                            | Energy measurement        | aLldpXdot3LocEnergyMeasurement                         |
|                            | PSE Power price index     | aLldpXdot3LocPSEPowerPriceIndex                        |

*Insert the following new rows into Table 79-11 at the end of the “Power via MDI” TLV name group:*

**Table 79–11—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references**

| TLV name      | TLV variable                            | LLDP Remote System Group managed object class attribute |
|---------------|-----------------------------------------|---------------------------------------------------------|
| Power via MDI | PD requested power value Mode A         | aLldpXdot3RemPDRequestedPowerValueA                     |
|               | PD requested power value Mode B         | aLldpXdot3RemPDRequestedPowerValueB                     |
|               | PSE allocated power value Alternative A | aLldpXdot3RemPSEAllocatedPowerValueA                    |
|               | PSE allocated power value Alternative B | aLldpXdot3RemPSEAllocatedPowerValueB                    |
|               | PSE powering status                     | aLldpXdot3RemPSEPoweringStatus                          |
|               | PD powered status                       | aLldpXdot3RemPDPoweredStatus                            |
|               | PSE power pairs ext                     | aLldpXdot3RemPowerPairsExt                              |
|               | Dual-signature power Class ext Mode A   | aLldpXdot3RemPowerClassExtA                             |
|               | Dual-signature power Class ext Mode B   | aLldpXdot3RemPowerClassExtB                             |
|               | Power class ext                         | aLldpXdot3RemPowerClassExt                              |
|               | Power Type ext                          | aLldpXdot3RemPowerTypeExt                               |
|               | PD 4PID                                 | aLldpXdot3RemPD4PID                                     |
|               | PD Load                                 | aLldpXdot3RemPDLoad                                     |
|               | PSE maximum available power value       | aLldpXdot3RemPSEMaxAvailPower                           |
|               | PSE Autoclass support                   | aLldpXdot3RemPSEAutoclassSupport                        |
|               | Autoclass completed                     | aLldpXdot3RemAutoclassCompleted                         |
|               | Autoclass request                       | aLldpXdot3RemAutoclassRequest                           |
|               | Power down request                      | aLldpXdot3RemPowerDownRequest                           |
|               | Power down time                         | aLldpXdot3RemPowerDownTime                              |

*Insert the following new TLV name group into Table 79-11 after the “Power via MDI” TLV name group (and before the “Link Aggregation (deprecated)” row):*

**Table 79–11—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references (*continued*)**

| TLV name                   | TLV variable              | LLDP Remote System Group managed object class attribute |
|----------------------------|---------------------------|---------------------------------------------------------|
| Power via MDI Measurements | Voltage support           | aLldpXdot3RemMeasVoltageSupport                         |
|                            | Current support           | aLldpXdot3RemMeasCurrentSupport                         |
|                            | Power support             | aLldpXdot3RemMeasPowerSupport                           |
|                            | Energy support            | aLldpXdot3RemMeasEnergySupport                          |
|                            | Measurement source        | aLldpXdot3RemMeasurementSource                          |
|                            | Voltage request           | aLldpXdot3RemMeasVoltageRequest                         |
|                            | Current request           | aLldpXdot3RemMeasCurrentRequest                         |
|                            | Power request             | aLldpXdot3RemMeasPowerRequest                           |
|                            | Energy request            | aLldpXdot3RemMeasEnergyRequest                          |
|                            | Voltage measurement valid | aLldpXdot3RemMeasVoltageValid                           |
|                            | Current measurement valid | aLldpXdot3RemMeasCurrentValid                           |
|                            | Power measurement valid   | aLldpXdot3RemMeasPowerValid                             |
|                            | Energy measurement valid  | aLldpXdot3RemMeasEnergyValid                            |
|                            | Voltage uncertainty       | aLldpXdot3RemMeasVoltageUncertainty                     |
|                            | Current uncertainty       | aLldpXdot3RemMeasCurrentUncertainty                     |
|                            | Power uncertainty         | aLldpXdot3RemMeasPowerUncertainty                       |
|                            | Energy uncertainty        | aLldpXdot3RemMeasEnergyUncertainty                      |
|                            | Voltage measurement       | aLldpXdot3RemVoltageMeasurement                         |
|                            | Current measurement       | aLldpXdot3RemCurrentMeasurement                         |
|                            | Power measurement         | aLldpXdot3RemPowerMeasurement                           |
|                            | Energy measurement        | aLldpXdot3RemEnergyMeasurement                          |
|                            | PSE Power price index     | aLldpXdot3RemPSEPowerPriceIndex                         |

### 79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements<sup>5</sup>

#### 79.5.3 Major capabilities/options

Change 79.5.3 as follows:

| Item  | Feature                                | Subclause | Value/Comment  | Status | Support                                                     |
|-------|----------------------------------------|-----------|----------------|--------|-------------------------------------------------------------|
| *MP   | MAC/PHY Configuration/Status TLV       | 79.3.1    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *PV   | Power Via MDI TLV                      | 79.3.2    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *PT12 | Device is a Type 1 or Type 2 PSE or PD | 79.3.2    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *PT34 | Device is a Type 3 or Type 4 PSE or PD | 79.3.2    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *LA   | Link Aggregation TLV                   | 79.3.3    | TLV deprecated | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *FS   | Maximum Frame Size TLV                 | 79.3.4    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *EE   | EEE TLV                                | 79.3.5    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *EEFW | EEE Fast Wake TLV                      | 79.3.6    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *AE   | Additional Ethernet Capabilities TLV   | 79.3.7    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |
| *PM   | Power via MDI Measurements TLV         | 79.3.8    |                | O      | Yes <input type="checkbox"/><br>No <input type="checkbox"/> |

<sup>5</sup>Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

### 79.5.8 Power Via MDI TLV

Delete the entire Power via MDI TLV PICS table and insert the following new table in 79.5.8:

| Item  | Feature                                                                               | Subclause  | Value/Comment                                                                                                                                               | Status    | Support            |
|-------|---------------------------------------------------------------------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|
| PVT1  | Not send DLL classification or Type 3 and Type 4 extension fields                     | 79.3.2     | Unless supplying or drawing power from the PI                                                                                                               | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT2  | Type 1 or Type 2 power entity DLL classification extension fields                     | 79.3.2     | Support the Power Via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered                                        | PV*PT12:M | Yes [ ]<br>N/A [ ] |
| PVT3  | Type 3 or Type 4 power entity DLL classification extension fields                     | 79.3.2     | Support the Power Via MDI TLV DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT4  | Not support Type 3 and Type 4 power entity DLL Classification                         | 79.3.2     | Not include the Type 3 and Type 4 extension fields in Power via MDI TLVs                                                                                    | PV*PT12:M | Yes [ ]<br>N/A [ ] |
| PVT5  | ‘Port class’ field                                                                    | 79.3.2.1.1 | Indicates if the port is a PSE or a PD when transmitted                                                                                                     | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT6  | ‘PSE MDI power support’ field                                                         | 79.3.2.1.2 | Indicates if MDI power is supported                                                                                                                         | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT7  | ‘PSE MDI power state’ field                                                           | 79.3.2.1.3 | Indicates if the PSE function is enabled or disabled                                                                                                        | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT8  | ‘PSE pairs control ability’ field                                                     | 79.3.2.1.4 | Indicates if the PSE has the capability to control which PSE Pinout Alternative is used for PD detection and power                                          | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT9  | ‘PSE power pair’ field                                                                | 79.3.2.2   | Integer value as defined in Table 79–3a based on aPSEPowerPairs (30.9.1.1.4)                                                                                | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT10 | ‘PSE power pair’ field for Type 3 or Type 4 PSEs furnishing power on a single pairset | 79.3.2.2   | To use value that defines that pairset                                                                                                                      | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT11 | ‘Power class’ field                                                                   | 79.3.2.3   | Integer value as defined in Table 79–3b by the aPsePortPowerClassification (30.9.1.1.6)                                                                     | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT12 | ‘Power type/source/priority’ field                                                    | 79.3.2.4   | Contains a bit-map of the Power type, source, and priority defined in Table 79–4                                                                            | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT13 | ‘Power type’ field                                                                    | 79.3.2.4.1 | Set according to Table 79–4                                                                                                                                 | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT14 | ‘Power type’ field for Type 3 or Type 4 PSEs                                          | 79.3.2.4.1 | Set to the value corresponding with Type 2 PSEs                                                                                                             | PV*PT34:M | Yes [ ]<br>N/A [ ] |

| Item  | Feature                                                                                                       | Subclause   | Value/Comment                                                                                         | Status    | Support            |
|-------|---------------------------------------------------------------------------------------------------------------|-------------|-------------------------------------------------------------------------------------------------------|-----------|--------------------|
| PVT15 | ‘Power type’ field for Type 3 or Type 4 PDs                                                                   | 79.3.2.4.1  | Set to the value corresponding with Type 2 PDs                                                        | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT16 | ‘PD 4PID’ field when Power type is PD                                                                         | 79.3.2.4.2a | Set according to Table 79–4 to indicate whether the PD supports powering of both Modes simultaneously | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT17 | ‘PD 4PID’ field when Power type is PSE                                                                        | 79.3.2.4.2a | Set to ‘0’                                                                                            | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT18 | ‘PD requested power value’ field                                                                              | 79.3.2.5    | Contains the PD’s requested power value defined in Table 79–5                                         | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT19 | ‘PSE allocated power value’ field                                                                             | 79.3.2.6    | Contains the PSE’s allocated power value defined in Table 79–6                                        | PV:M      | Yes [ ]<br>N/A [ ] |
| PVT20 | ‘PD requested power Mode A’ field and ‘PD requested power Mode B’ field                                       | 79.3.2.6a   | Contains the PD’s requested power value defined in Table 79–6a for Mode A and Table 79–6b for Mode B  | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT21 | ‘PSE allocated power Alternative A’ field and ‘PSE allocated power Alternative B’ field                       | 79.3.2.6b   | Contains the values in Table 79–6c and Table 79–6d                                                    | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT22 | ‘PSE powering status’ field for PSEs                                                                          | 79.3.2.6c.1 | Set to the current powering status as defined in Table 79–6e                                          | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT23 | ‘PSE powering status’ field for PDs                                                                           | 79.3.2.6c.1 | Set to ‘0’                                                                                            | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT24 | ‘PD powered status’ field for PDs                                                                             | 79.3.2.6c.2 | Set to the current powered status as defined in Table 79–6e                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT25 | ‘PD powered status’ field for PSEs                                                                            | 79.3.2.6c.2 | Set to ‘0’                                                                                            | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT26 | ‘PSE power pairs ext’ field for PSEs                                                                          | 79.3.2.6c.3 | Contain powering status of the PSE as defined in Table 79–6e                                          | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT27 | ‘PSE power pairs ext’ field for PDs                                                                           | 79.3.2.6c.3 | Set to ‘0’                                                                                            | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT28 | ‘Dual-signature power Class ext Mode A’ field for single-signature PDs                                        | 79.3.2.6c.4 | Set to ‘7’                                                                                            | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT29 | ‘Dual-signature power Class ext Mode A’ field for dual-signature PDs                                          | 79.3.2.6c.4 | Set to the requested Class (see 145.3.6) for Mode A                                                   | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT30 | ‘Dual-signature power Class ext Mode A’ field for 2-pair only PSEs or PSEs connected to a single-signature PD | 79.3.2.6c.4 | Set to ‘7’                                                                                            | PV*PT34:M | Yes [ ]<br>N/A [ ] |

| Item  | Feature                                                                                                       | Subclause   | Value/Comment                                                                        | Status    | Support            |
|-------|---------------------------------------------------------------------------------------------------------------|-------------|--------------------------------------------------------------------------------------|-----------|--------------------|
| PVT31 | ‘Dual-signature power Class ext Mode A’ field for PSEs connected to a dual-signature PD                       | 79.3.2.6c.4 | Set to the assigned Class (see 145.2.8) for Mode A                                   | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT32 | ‘Dual-signature power Class ext Mode B’ field for single-signature PDs                                        | 79.3.2.6c.5 | Set to ‘7’                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT33 | ‘Dual-signature power Class ext Mode B’ field for dual-signature PDs                                          | 79.3.2.6c.5 | Set to the requested Class (see 145.3.6) for Mode B                                  | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT34 | ‘Dual-signature power Class ext Mode B’ field for 2-pair only PSEs or PSEs connected to a single-signature PD | 79.3.2.6c.5 | Set to ‘7’                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT35 | ‘Dual-signature power Class ext Mode B’ field for PSEs connected to a dual-signature PD                       | 79.3.2.6c.5 | Set to the assigned Class (see 145.2.8) for Mode B                                   | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT36 | ‘Power Class ext’ field for single-signature PDs                                                              | 79.3.2.6c.6 | Set to the requested Class (see 145.3.6)                                             | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT37 | ‘Power Class ext’ field for dual-signature PDs                                                                | 79.3.2.6c.6 | Set to ‘7’                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT38 | ‘Dual-signature power Class ext Mode B’ field for 2-pair only PSEs or PSEs connected to a single-signature PD | 79.3.2.6c.6 | Set to the assigned Class (see 145.2.8)                                              | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT39 | ‘Dual-signature power Class ext Mode B’ field for PSEs connected to a dual-signature PD                       | 79.3.2.6c.6 | Set to ‘7’                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT40 | ‘System setup’ field                                                                                          | 79.3.2.6d   | Contains the device bit-map of the Power Type ext and PD Load defined in Table 79–6f | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT41 | ‘Power type ext’ field                                                                                        | 79.3.2.6d.1 | Set according to Table 79–6f                                                         | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT42 | ‘PD Load’ field when ‘Power type’ is PD                                                                       | 79.3.2.6d.2 | Set according to Table 79–6f                                                         | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT43 | ‘PD Load’ field when ‘Power type’ is PSE                                                                      | 79.3.2.6d.2 | Set to ‘0’                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT44 | ‘PSE maximum available power value’ field                                                                     | 79.3.2.6e   | Contains the highest power the PSE can grant as defined in Table 79–6g               | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT45 | ‘PSE maximum available power value’ field for PDs                                                             | 79.3.2.6e   | Set to ‘0’                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT46 | ‘Autoclass’ field                                                                                             | 79.3.2.6f   | Contains the bits defined in Table 79–6h                                             | PV*PT34:M | Yes [ ]<br>N/A [ ] |

| Item  | Feature                                                                          | Subclause   | Value/Comment                                                                   | Status    | Support            |
|-------|----------------------------------------------------------------------------------|-------------|---------------------------------------------------------------------------------|-----------|--------------------|
| PVT47 | ‘PSE Autoclass support’ field when ‘Power type’ is PSE                           | 79.3.2.6f.1 | Set to indicate if the PSE supports Autoclass over DLL according to Table 79–6h | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT48 | ‘PSE Autoclass support’ field when ‘Power type’ is PD                            | 79.3.2.6f.1 | Set to ‘0’                                                                      | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT49 | ‘Autoclass completed’ field when ‘Power type’ is PSE                             | 79.3.2.6f.2 | Set to indicate that the PSE has concluded the Autoclass measurement            | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT50 | ‘Autoclass completed’ field when ‘Power type’ is PD                              | 79.3.2.6f.2 | Set to ‘0’                                                                      | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT51 | ‘Autoclass request’ field when ‘Power type’ is PSE                               | 79.3.2.6f.3 | Set to 0’0                                                                      | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT52 | ‘Power down’ field                                                               | 79.3.2.6g   | Contains the bits defined in Table 79–6i                                        | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT53 | ‘Power down request’ field when ‘Power type’ is PD and power is to be maintained | 79.3.2.6g.1 | Set to ‘0’                                                                      | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT54 | ‘Power down request’ field when ‘Power type’ is PSE                              | 79.3.2.6g.1 | Set to ‘0’                                                                      | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT55 | ‘Power down time’ field when ‘Power type’ is PD                                  | 79.3.2.6g.2 | Set per the description in Table 79–6i                                          | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PVT56 | ‘Power down time’ field when ‘Power type’ is PSE                                 | 79.3.2.6g.2 | Set to ‘0’                                                                      | PV*PT34:M | Yes [ ]<br>N/A [ ] |

*Insert the following new subclause, 79.5.12, after 79.5.11:*

#### **79.5.12 Power via MDI Measurements TLV**

| Item | Feature                                                                | Subclause | Value/Comment                                                                                                          | Status    | Support            |
|------|------------------------------------------------------------------------|-----------|------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|
| PMT1 | ‘Measurements’ field                                                   | 79.3.8.1  | Set according to Table 79–8a                                                                                           | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PMT2 | Measurement values (voltage, current, power, or energy)                | 79.3.8.1  | Set to ‘0’ in case the corresponding request bit is ‘0’                                                                | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PMT3 | No support for Measurement values (voltage, current, power, or energy) | 79.3.8.1  | Value that is not supported set to ‘0’                                                                                 | PV*PT34:M | Yes [ ]<br>N/A [ ] |
| PMT4 | ‘PSE power price index’ field                                          | 79.3.8.2  | Contains an index of the current price of electricity compared to what the PSE considers the nominal electricity price | PV*PT34:M | Yes [ ]<br>N/A [ ] |

**126. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 2.5GBASE-T and 5GBASE-T****126.5 PMA electrical specifications****126.5.1 Isolation requirement**

*Change 126.5.1 as follows:*

A PHY with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

~~The A PHY with a MDI that is not a PI shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall withstand at least one of the following electrical strength tests:~~

- a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.2.2 of IEC 60950-1:2001.
- b) 2250 V dc for 60 s, applied as specified in Section 5.2.2 of IEC 60950-1:2001.
- c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses is 1.2/50  $\mu$ s (1.2  $\mu$ s virtual front time, 50  $\mu$ s virtual time or half value), as defined in Annex N of IEC 60950-1:2001.

There shall be no insulation breakdown, as defined in Section 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 M $\Omega$ , measured at 500 V dc.

*Insert new Clause 145 after Clause 130 (Clause 131 to Clause 144 are reserved for future amendments):*

## 145. Power over Ethernet

### 145.1 Overview

This clause defines the functional and electrical characteristics of an enhanced Power over Ethernet (PoE) system. The original PoE system is defined in Clause 33. Clause 145 includes the capability to provide power over 4 pairs while maintaining compatibility with equipment designed in accordance with Clause 33.

A PoE system consists of three separately specified major elements. They are the power supply, a non-data entity which is called the Power Sourcing Equipment (PSE), the powered load, another non-data entity which is called the Powered Device (PD), and the standards based, balanced, twisted-pair cabling connecting the two.

The cabling portion of the system is defined as the link section. The link section shares use of the cabling with the link segment used for data transmission. The PSE is normally an element of the powering DTE but may, instead, be located within the cabling portion of the system. PSEs located within the cabling portion of the system are called Midspan PSEs, or simply Midspans. The PD is an element of the powered DTE.

The system specified here is for use with IEEE 802.3 MAUs connected by 4-pair twisted pair cabling that have been qualified as being compatible with this clause. Those MAUs are defined in Clause 14 and the PHYs are defined in Clause 25, Clause 40, Clause 55, and Clause 126. Use in other environments is outside the scope of this standard. Power over Ethernet allows devices to supply / use power using the same generic cabling as is used for data transmission.

PSEs and PDs are categorized by Type. This clause specifies Type 3 and Type 4 devices as well as their interaction with Type 1 and Type 2 devices. References in this clause to PSEs and PDs without a Type qualifier refer exclusively to Type 3 and Type 4 devices. See Clause 33 for the specification of Type 1 and Type 2 devices.

Power over Ethernet is intended to provide a 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a single cabling interface for both data and power. This clause specifies the following:

- a) A PSE to add power to the 100  $\Omega$  balanced cabling system
- b) The characteristics of a PD's load on the PSE and the structured cabling
- c) A protocol allowing the detection of a PD that requests power from a PSE
- d) Methods to classify a PD based on its power needs
- e) A method for a connected PSE and PD to dynamically negotiate power
- f) A method for scaling supplied power back to the detect level when power is no longer requested or required

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100  $\Omega$  balanced cabling system, and the possible consequences of applying power to such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is not point-to-point, resulting in unpredictable performance and possibly damaged equipment.

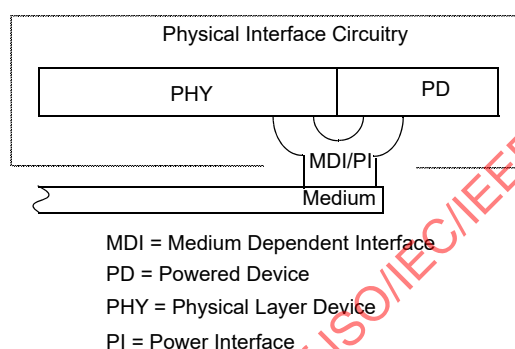
This clause differentiates between the two ends of the powered portion of the link, i.e. the link section, defining the PSE and the PD as separate but related devices.

### 145.1.1 Compatibility considerations

The requirements in this Clause are designed such that PSEs and PDs that meet these requirements are compatible at their respective Power Interfaces (PIs). Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

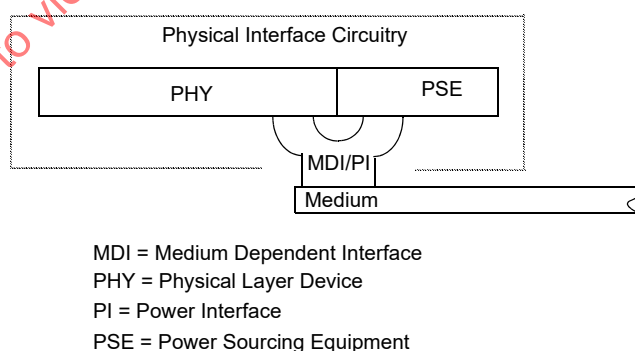
### 145.1.2 Relationship of Power over Ethernet to the IEEE 802.3 Architecture

Power over Ethernet comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 145–1 depicts the positioning of PoE in the case of the PD.



**Figure 145–1—Power over Ethernet powered device relationship to the physical interface circuitry and the IEEE 802.3 Ethernet LAN model**

Figure 145–2 and Figure 145–3 depict the positioning of PoE in the cases of the Endpoint PSE and the Midspan PSE, respectively.

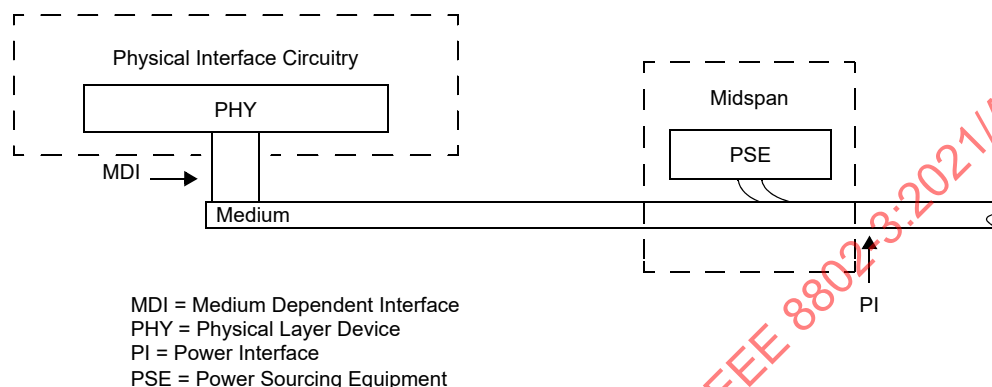


**Figure 145–2—Power over Ethernet Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 Ethernet LAN model**

The Power Interface (PI) is the mechanical and electrical interface between the PSE or PD and the transmission medium as defined in 1.4.406.

In an Endpoint PSE and in a PD, the PI is the MDI as defined in 1.4.324.

In the case of a Midspan PSE, the PI is physically separate from the MDI and is contained within the cabling portion of the data transmission system.



**Figure 145-3—Power over Ethernet Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 Ethernet LAN model**

### 145.1.3 System parameters

A valid power system consists only of a single PSE sourcing power, a single PD, and the link section connecting them. The PSE and PD can each be of a Type defined in Clause 33 or Clause 145, in any combination. The power system has certain basic parameters defined according to Table 145-1. See 33.1.4 for these parameters as applicable to Type 1 and Type 2 devices. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 145.2 and 145.3.

**Table 145-1—System parameters**

| PSE Type                                                                                                                                                                                                                                                  | Nominal highest current per pair (I <sub>Cable</sub> , A) | Number of powered pairs | Channel pairset maximum DC loop resistance (R <sub>Ch</sub> , Ω) | Minimum cabling type                                                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|-------------------------|------------------------------------------------------------------|---------------------------------------------------------------------|
| Type 3                                                                                                                                                                                                                                                    | 0.6                                                       | 2 or 4                  | 12.5                                                             | Class D (ISO/IEC11801:1995) or Category 5 (ANSI/EIA/TIA-568-A:1995) |
| Type 4                                                                                                                                                                                                                                                    | 0.6                                                       | 2                       | 12.5                                                             |                                                                     |
|                                                                                                                                                                                                                                                           | 0.96                                                      | 4                       | 12.5                                                             |                                                                     |
| NOTE—The current on the pairs may be impacted by pair-to-pair system resistance unbalance. See 145.2.10.6.1. For additional information on pair-to-pair resistance unbalance in structured cabling systems, see TIA TSB-184-A [Bx2] and ISO/IEC TS 29125. |                                                           |                         |                                                                  |                                                                     |

$I_{\text{Cable}}$ , specified in Table 145–1, is the current on one twisted pair in the balanced twisted-pair cable. When power is delivered over 2 pairs, two twisted pairs are required to source  $I_{\text{Cable}}$ , one carrying (+  $I_{\text{Cable}}$ ) and one carrying (–  $I_{\text{Cable}}$ ), from the perspective of the PI.

When power is delivered over 4 pairs, four twisted pairs are required to source  $2 \times I_{\text{Cable}}$ , two each carrying a nominal current (+  $I_{\text{Cable}}$ ) and two each carrying a nominal current (–  $I_{\text{Cable}}$ ), from the perspective of the PI. Greater than Class 4 power delivery requires 4 pairs.

$I_{\text{Cable}}$  is the highest nominal current on a pair for a system without pair-to-pair current unbalance. When power is provided over 4 pairs, the current may be unbalanced, causing one pair to have a higher current than  $I_{\text{Cable}}$ , while the other pair of the same polarity carries a corresponding lower current than  $I_{\text{Cable}}$ . The maximum nominal total 4-pair current is twice the value of  $I_{\text{Cable}}$ . See TIA TSB-184-A [Bx2] and ISO/IEC TS 29125 for additional information on pair-to-pair resistance unbalance.

The cable references use “DC loop resistance,” which refers to two single conductors in series. This clause uses “pairset DC loop resistance” ( $R_{\text{Ch}}$ ), which refers to two pairs in series. Therefore,  $R_{\text{Ch}}$  is related to, but not equivalent to, the “DC loop resistance” called out in the cable references. In addition to  $I_{\text{Cable}}$ , the requirements of this clause reference the total current and the per pairset current, which are described here.

$I_{\text{Port}}$  is the total current on both pairs with the same polarity and is defined in Equation (145–7).

$I_{\text{Port-2P}}$  is the current on the negative pair of a pairset and is derived from  $I_{\text{Port-2P-pri}}$  and  $I_{\text{Port-2P-sec}}$  in Equation (145–5).

Pairset current is the current on the negative pair associated with a given pairset. Note that the positive pair and the negative pair of a pairset may carry a different amount of current, caused by the independent pair-to-pair current unbalance in the positive pairs, and in the negative pairs, when the system is providing power over more than 2 pairs.

2-pair mode refers to power delivery using either one pair at positive  $V_{\text{PSE}}$  and one at negative  $V_{\text{PSE}}$ , or to using two pairs at positive  $V_{\text{PSE}}$  and one at negative  $V_{\text{PSE}}$ .

4-pair mode refers to power delivery using two pairs at positive  $V_{\text{PSE}}$  and two at negative  $V_{\text{PSE}}$ .

$R_{\text{Ch}}$  is the maximum pairset DC loop resistance, as defined in Table 145–1.

$R_{\text{Chan}}$  is the actual DC resistance from the PSE PI to the PD PI and back.  $R_{\text{Chan}}$  has a maximum value of  $R_{\text{Ch}} / 2$  when operating in 4-pair mode.  $R_{\text{Chan}}$  has a maximum value of  $R_{\text{Ch}}$  when operating in 2-pair mode.

$R_{\text{Chan-2P}}$  is the actual pairset DC resistance from the PSE PI to the PD PI and back.  $R_{\text{Chan-2P}}$  has a maximum value of  $R_{\text{Ch}}$ .

$V_{PD}$  is the voltage at the PD PI. For a single-signature PD,  $V_{PD}$  is measured between any positive conductor of a pairset and any negative conductor of the corresponding pairset, for the pairset with the highest voltage. For a dual-signature PD,  $V_{PD}$  is measured between any positive conductor of a pairset and any negative conductor of the corresponding pairset, for the given Mode.

$V_{PSE}$  is the voltage at the PSE PI. When connected to a single-signature PD and operating in 4-pair mode,  $V_{PSE}$  is measured between any positive conductor and any negative conductor. When connected to a dual-signature PD, when operating in 2-pair mode, or when the PD signature configuration has not yet been identified,  $V_{PSE}$  is measured between any positive conductor of the pairset and any negative conductor of the corresponding pairset, for the given Alternative.

#### 145.1.4 Cabling requirements

Class D or better cabling as specified in ISO/IEC 11801:1995, with the additional requirement that the channel DC loop resistance is 25  $\Omega$  or less, is required to support operation as specified in this Clause. These requirements are also met by Class D or better cabling as specified by ISO/IEC 11801:2002, Category 5e or better cable and components as specified in ANSI/TIA-568-C.2, or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995.

Cable ambient operating temperature guidelines for Type 3 and Type 4 operation are provided in ISO/IEC TS 29125 [B48]<sup>6</sup> and TIA TSB-184A [Bx2]. For Type 3 and Type 4 PoE systems, managing the temperature rise can require a reduction in the maximum number of cables bundled. See ISO/IEC TS 29125, TIA TSB-184-A, as well as applicable local codes and regulations, e.g., the National Electrical Code® (NEC®) (NFPA 70®, 2017 Edition) [Bx1], for more information.

Planning considerations for PoE systems are provided in ISO/IEC CD 14763-2 supported by the information in ISO/IEC TS 29125 and TIA TSB-184-A, as well as applicable local codes and regulations.

Within Clause 145 and its annexes, the term link section refers to the point-to-point medium connection between two and only two active Power Interfaces (PIs). Type 3 and Type 4 operation requires link sections to comply with the intra-pair resistance unbalance requirements for twisted-pair cabling as specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2. Refer to Annex 145A for more information including the requirements for pair-to-pair resistance unbalance when operating over 4 pairs.

<sup>6</sup>The numbers in brackets correspond to those of the bibliography in Annex A.

## 145.2 Power sourcing equipment (PSE)

The PSE is the portion of the end station or midspan equipment that provides the power to a single PD. The PSE's main functions are as follows:

- To search the link section for a PD
- To supply power to the detected PD through the link section
- To monitor the power on the link section
- To remove power when no longer requested or required, returning to the searching state

An unplugged link section is one instance when power is no longer required.

In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD.

A PSE is electrically specified at the point of the physical connection to the cabling.

Additional electrical specifications that apply to the PSE are specified in 145.4.

### 145.2.1 PSE Type descriptions

A PSE can be categorized as either a Type 1, Type 2, Type 3 or Type 4 PSE. See 33.2 for the specification of Type 1 and Type 2 PSEs.

Type 1, Type 2, Type 3, and Type 4 PSEs interoperate with Type 1, Type 2, Type 3, and Type 4 PDs, subject to power limitations. See 145.2.8.

Table 145–2 summarizes the supported parameters of Type 3 and Type 4 PSEs. The PSE Type can only change when the PSE state diagram (Figure 145–13) is in IDLE.

**Table 145–2—PSE supported parameters**

| PSE Type | Supports 4-pair power | Highest Class supported <sup>a</sup> | Short MPS support <sup>b</sup> | Physical Layer classification <sup>a</sup> | Data Link Layer classification <sup>a</sup> | Autoclass <sup>c</sup> |
|----------|-----------------------|--------------------------------------|--------------------------------|--------------------------------------------|---------------------------------------------|------------------------|
| Type 3   | No / Yes              | 1 to 4                               | Yes                            | Multiple-Event                             | Optional                                    | Optional               |
|          | Yes                   | 1 to 6                               |                                |                                            |                                             |                        |
| Type 4   | Yes                   | 7 to 8                               |                                |                                            |                                             |                        |

<sup>a</sup> See 145.2.8, Table 145–11 and Table 145–12.

<sup>b</sup> See 145.2.12.

<sup>c</sup> See 145.2.8.2 and 145.3.6.2.

### 145.2.2 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an “Endpoint PSE”. A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a “Midspan PSE”. The requirements of this document apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. The location of various Endpoint and Midspan PSEs are illustrated in Figure 145–4 to Figure 145–11.

PSEs can be compatible with any of the following: 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T.

### 145.2.3 Midspan PSE variants

There are several variants of Midspan PSEs defined.

#### 10BASE-T/100BASE-TX Midspan PSE:

A Midspan PSE that results in a link that can support only 10BASE-T and 100BASE-TX operation (see Figure 145–8 and Figure 145–10). Note that this limitation is due to the presence of the Midspan PSE whether it is supplying power or not.

#### 1000BASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see Figure 145–9 and Figure 145–11).

#### 2.5GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T and 2.5GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 145–9 and Figure 145–11).

#### 5GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, and 5GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 145–9 and Figure 145–11).

#### 10GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 145–9 and Figure 145–11).

NOTE—See 145.4.9.3 for Alternative A Midspan PSEs.

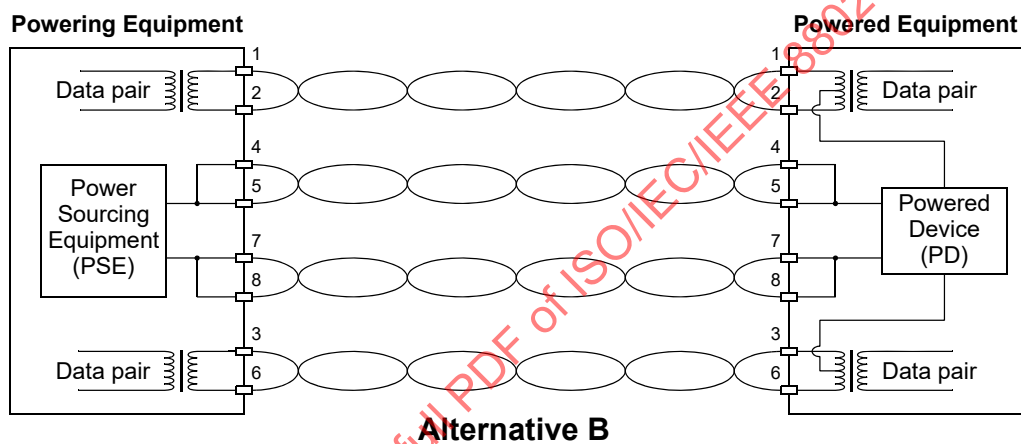
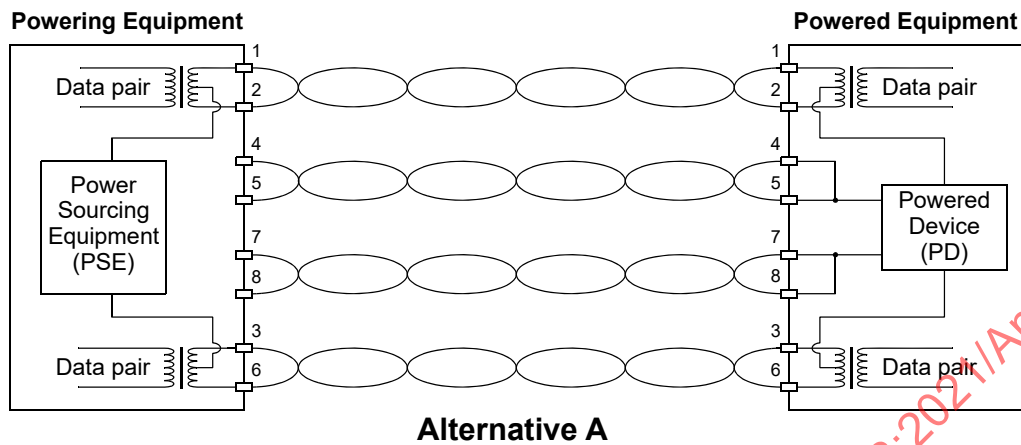


Figure 145-4—10BASE-T/100BASE-TX 2-pair Endpoint PSE location overview

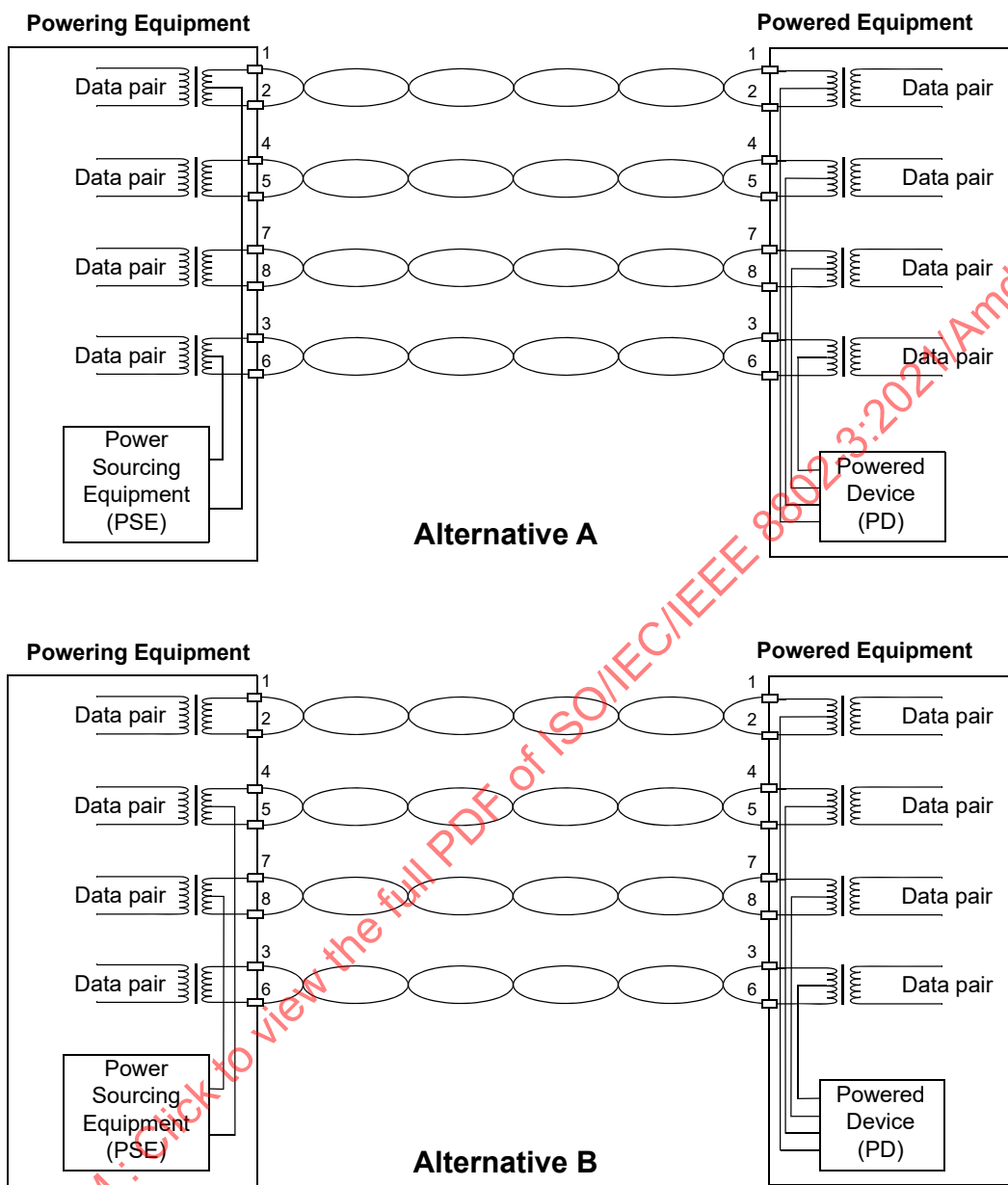


Figure 145-5—1000/2.5G/5G/10GBASE-T 2-pair Endpoint PSE location overview

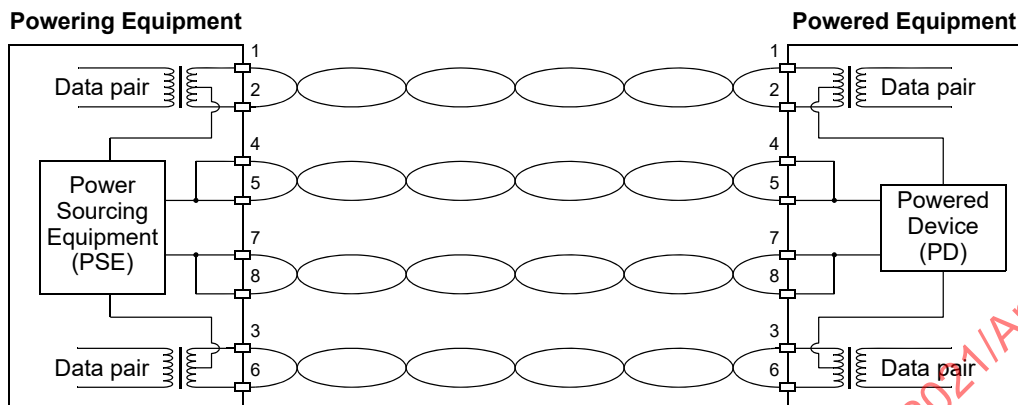


Figure 145-6—10BASE-T/100BASE-TX 4-pair Endpoint PSE location overview

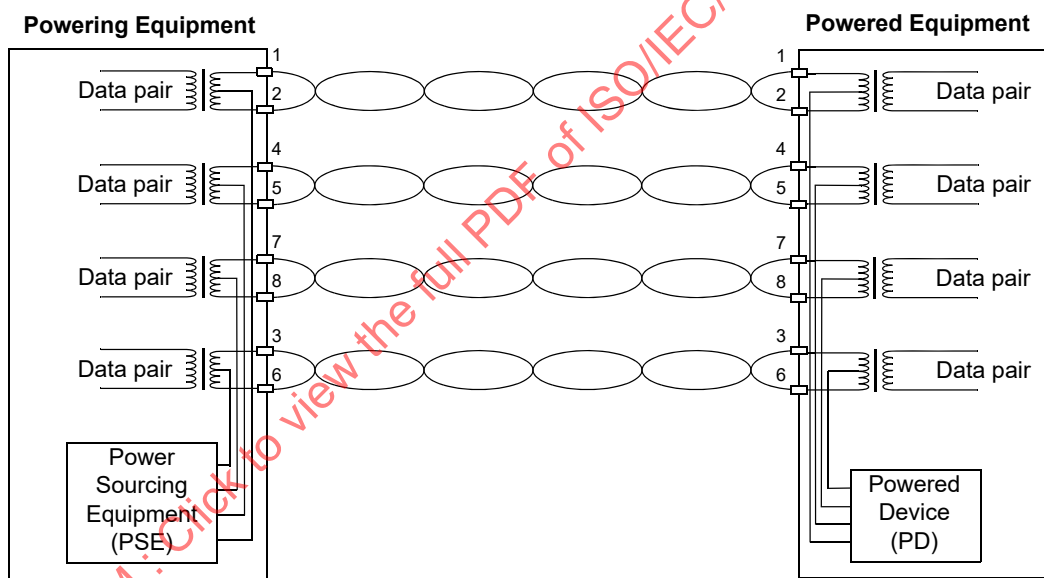


Figure 145-7—1000/2.5G/5G/10GBASE-T 4-pair Endpoint PSE location overview

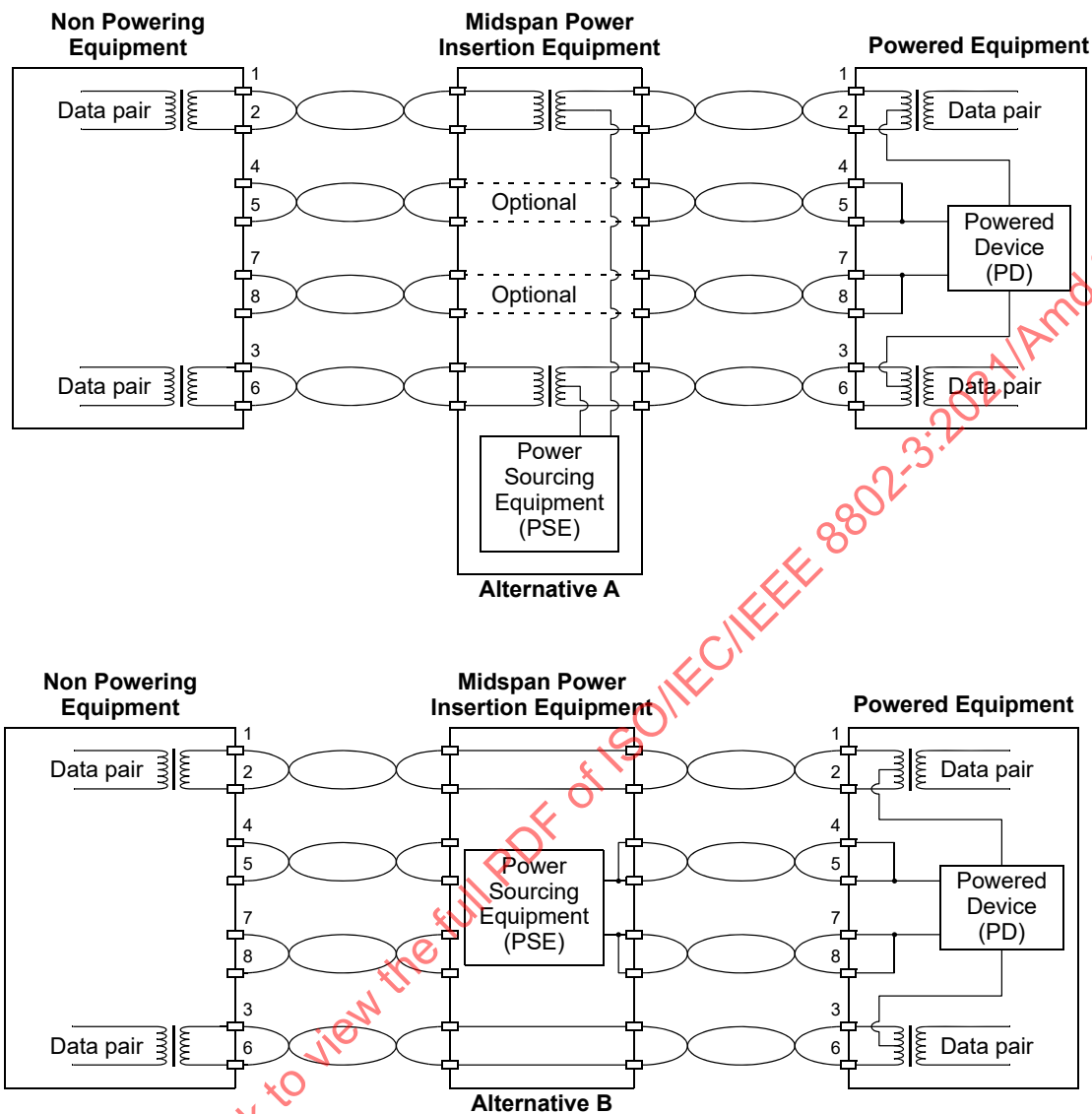


Figure 145-8—10BASE-T/100BASE-TX 2-pair Midspan PSE location overview

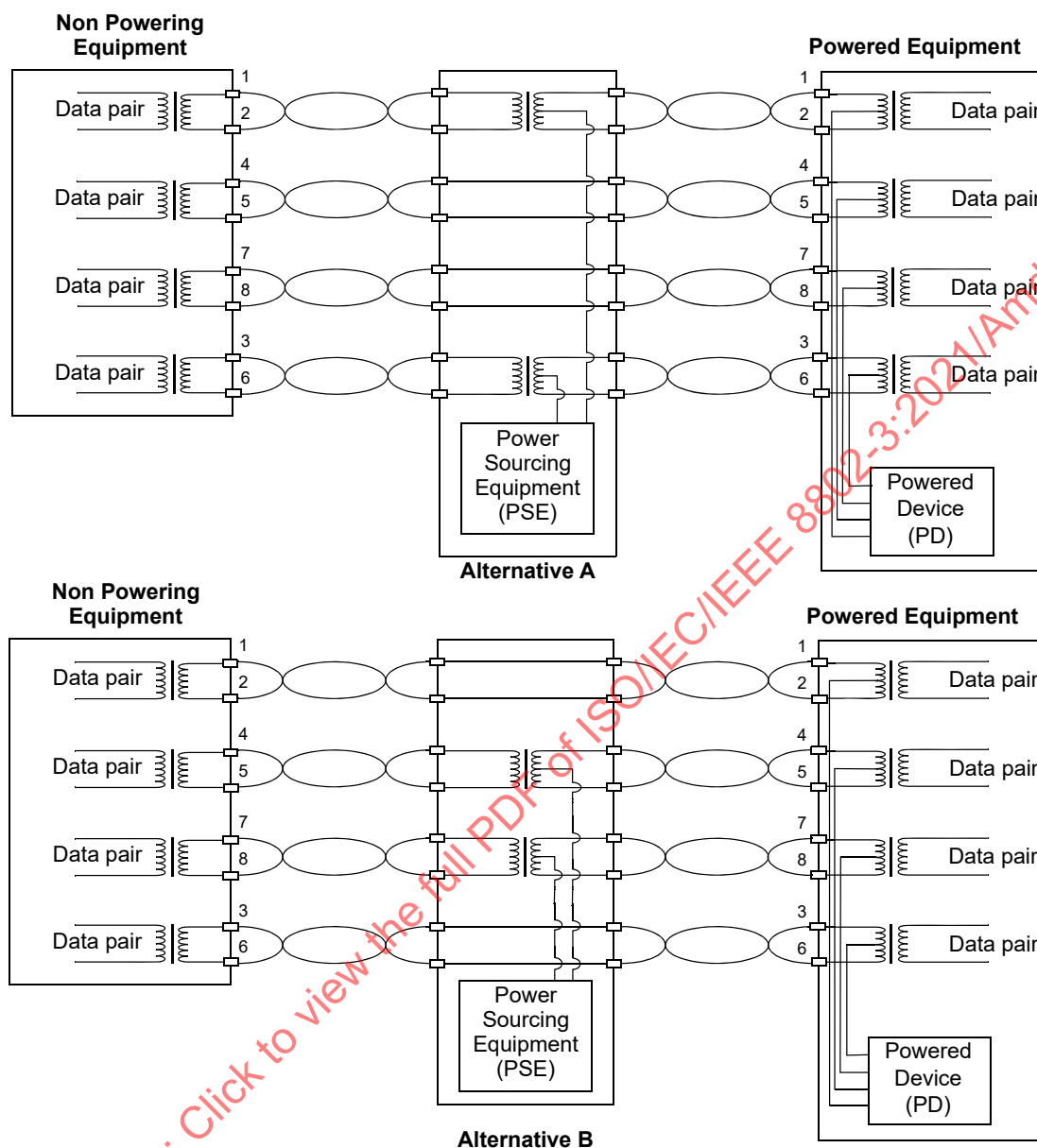


Figure 145-9—1000BASE-T, 2.5G, 5G, or 10GBASE-T 2-pair Midspan PSE location overview

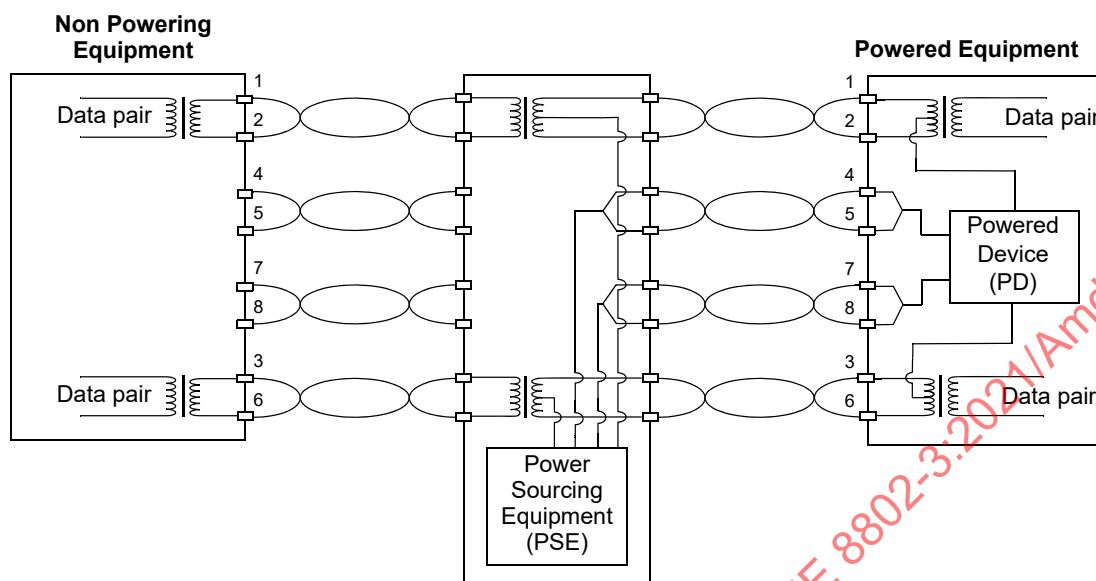


Figure 145-10—10BASE-T/100BASE-TX 4-pair Midspan PSE location overview

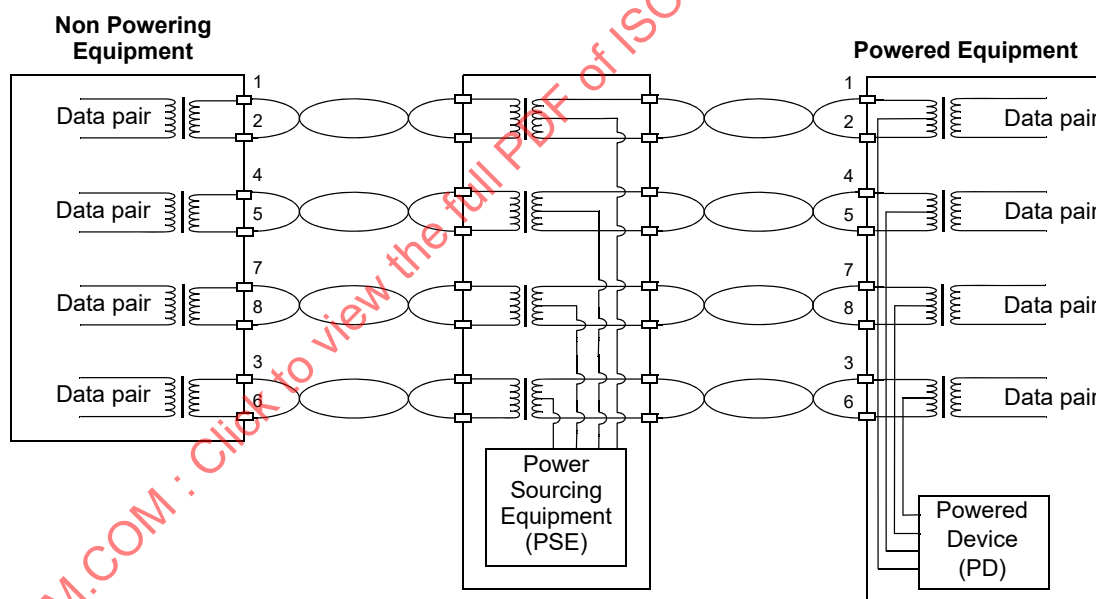


Figure 145-11—1000BASE-T, 2.5G, 5G, or 10GBASE-T 4-pair Midspan PSE location overview

#### 145.2.4 PSE PI

A PSE device may provide power via one or both of the two valid four-conductor connections, named pairsets. A pairset consists of a pair at the positive  $V_{PSE}$  and a pair at the negative  $V_{PSE}$ . The two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 145–12, in conjunction with Table 145–3, illustrates the pairsets, which for PSEs are named Alternative A and Alternative B.

PSEs are required to switch the negative pairs, and may switch the positive pairs as defined in 145.4.1.1. This may lead to both positive pairs providing current in 2-pair mode.

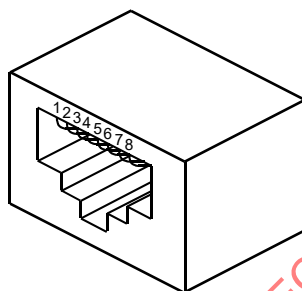


Figure 145–12—PD and PSE eight-pin modular jack

Table 145–3—PSE Pinout Alternatives

| Conductor | Alternative A (MDI-X) | Alternative A (MDI) | Alternative B(X)   | Alternative B(S)   |
|-----------|-----------------------|---------------------|--------------------|--------------------|
| 1         | Negative $V_{PSE}$    | Positive $V_{PSE}$  | —                  | —                  |
| 2         | Negative $V_{PSE}$    | Positive $V_{PSE}$  | —                  | —                  |
| 3         | Positive $V_{PSE}$    | Negative $V_{PSE}$  | —                  | —                  |
| 4         | —                     | —                   | Negative $V_{PSE}$ | Positive $V_{PSE}$ |
| 5         | —                     | —                   | Negative $V_{PSE}$ | Positive $V_{PSE}$ |
| 6         | Positive $V_{PSE}$    | Negative $V_{PSE}$  | —                  | —                  |
| 7         | —                     | —                   | Positive $V_{PSE}$ | Negative $V_{PSE}$ |
| 8         | —                     | —                   | Positive $V_{PSE}$ | Negative $V_{PSE}$ |

PSEs shall use only the permitted polarity configurations associated with Alternative A and Alternative B listed in Table 145–4 corresponding with their Type. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

**Table 145–4—Permitted Pinout Alternatives per Type**

| PSE Type | Alternative A (MDI-X) | Alternative A (MDI) | Alternative B(X) | Alternative B(S) |
|----------|-----------------------|---------------------|------------------|------------------|
| Type 3   | Yes                   | Yes                 | Yes              | Yes              |
| Type 4   | Yes                   | No                  | No               | Yes              |

Type 3 PSEs shall implement Alternative A, Alternative B, or both. Type 3 PSEs providing Class 5 or Class 6 power levels and Type 4 PSEs shall implement Alternative A and Alternative B. PSEs may operate simultaneously on both Alternatives, when the requirements of 145.2.9 are met.

The PSE specifications related to current apply on the negative pair or pairs unless otherwise noted.

#### 145.2.5 PSE state diagrams

PSEs shall provide the behavior of the state diagrams shown in Figure 145–13 to Figure 145–18.

##### 145.2.5.1 State diagram overview and timing

If power is to be applied, the PSE turns on power after a valid detection in less than  $T_{\text{pon}}$  as defined in Table 145–16. If the PSE cannot supply power within  $T_{\text{pon}}$ , it initiates and successfully completes a new detection cycle before applying power. See 145.2.10.14 for details.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 145.2.2), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE shall back off for at least  $T_{\text{dbo}}$  as defined in Table 145–16 before attempting another detection, except in the case of an open circuit as defined in 145.2.6.5. During this backoff, the PSE shall not apply a voltage greater than  $V_{\text{Off}}$  to the PI. See 145.2.6.5 for more information on Alternative B detection backoff requirements.

If a PSE performing detection using Alternative A detects an invalid detection signature, it should complete a second detection in less than  $T_{\text{dbo}}$  after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid detection signature.

Connection Check timing requirements are specified in Table 145–10. Detection and power turn-on timing requirements are specified in Table 145–16. Classification timing requirements are specified in Table 145–14. Autoclass timing requirements are specified in Table 145–15.

In the state diagram, each Alternative serves a distinct role during 4-pair operation. In any implementation, the roles of the Alternatives shall be established in IDLE and be maintained in every other state. In the state diagram, the roles of the Alternatives are named Primary Alternative and Secondary Alternative.

NOTE—During 4-pair operation, it may be necessary to swap the roles of Alternative A and Alternative B in IDLE in order to detect a PD.

The state diagram consists of multiple state diagrams that operate concurrently. Depending on the connected PD being identified as single-signature or dual-signature, the state diagram operates in a different manner. The top level state diagram consists of Figure 145–13.

If the connected PD is identified as dual-signature, the top level state diagram will proceed to SISM START and remain in that state, at which point the semi-independent state diagrams for the Primary and Secondary Alternative become active. The dual-signature semi-independent state diagram is defined in Figure 145–15 and Figure 145–16 for the Primary and Secondary Alternative respectively.

Monitoring of MPS is described by the state diagrams in Figure 145–17 and Figure 145–18.

#### 145.2.5.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5. In addition a precedence order for operators is established in Table 145–5. Operators of equal precedence are evaluated left-to-right. Operator precedence in qualifiers is a local convention for this clause.

**Table 145–5—State diagram operators in order of precedence (highest to lowest)**

| Operator         | Meaning                                                                                      |
|------------------|----------------------------------------------------------------------------------------------|
| ()               | Indicates precedence                                                                         |
| <, ≤, >, ≥, =, ≠ | Less than, less than or equal to, greater than, greater than or equal to, equals, not equals |
| !                | Boolean NOT                                                                                  |
| *                | Boolean AND                                                                                  |
| ^                | Boolean XOR                                                                                  |
| +                | Boolean OR                                                                                   |
| ←=               | Assignment operator                                                                          |

Some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

State diagrams may span over multiple pages. Arcs between states located on a different page within the same state diagram are drawn using a label containing the destination state's name at the originating state. An empty label is used at the destination state to indicate that there exists an entry, or entries, from another state.

### 145.2.5.3 Constants

#### CC\_DET\_SEQ

A constant indicating the sequence in which the PSE performs connection check and detection. See Annex 145B for timing diagrams.

Values:

- 0: Connection Check is followed by staggered detection for a single-signature PD and parallel or staggered detection for a dual-signature PD.
- 1: Detection on a pairset is followed by connection check and then detection on the other pairset for a single-signature PD and parallel or staggered (starting with first pairset) detection for a dual-signature PD.
- 2: Connection check and detection on both pairsets are performed within a single  $T_{det}$  window.
- 3: Connection check is followed by staggered detection.

Parallel detection refers to detection on both pairsets being performed in the same  $T_{det}$  time period. Staggered detection refers to detection on both pairsets being performed in a different  $T_{det}$  cycle.

### 145.2.5.4 Variables

#### alt\_done\_pri

A variable used to coordinate the main single-signature state diagram with the semi-independent dual-signature state diagram for the Primary Alternative.

Values:

- FALSE: The semi-independent state diagram is not ready to return to IDLE within the single-signature state diagram.
- TRUE: The semi-independent state diagram is ready to return to IDLE within the single-signature state diagram.

#### alt\_done\_sec

A variable used to coordinate the main single-signature state diagram with the semi-independent dual-signature state diagram for the Secondary Alternative.

Values:

- FALSE: The semi-independent state diagram is not ready to return to IDLE within the single-signature state diagram.
- TRUE: The semi-independent state diagram is ready to return to IDLE within the single-signature state diagram.

#### alt\_pri

A variable used to select which Alternative assumes the role of Primary Alternative in the state diagram.

Values:

- a: Alternative A assumes the role of Primary Alternative. When operating over 4 pairs, Alternative B assumes the role of Secondary Alternative.
- b: Alternative B assumes the role of Primary Alternative. When operating over 4 pairs, Alternative A assumes the role of Secondary Alternative.

#### alt\_pwrd\_pri

A variable that controls the circuitry that the PSE uses to power the PD over the Alternative that has been assigned as Primary.

Values:

- FALSE: The circuitry that applies operating voltage to the Primary Alternative is disabled.
- TRUE: The circuitry that applies operating voltage to the Primary Alternative is enabled.

#### alt\_pwrd\_sec

A variable that controls the circuitry that the PSE uses to power the PD over the Alternative that has been assigned as Secondary.

## Values:

- FALSE: The circuitry that applies operating voltage to the Secondary Alternative is disabled.
- TRUE: The circuitry that applies operating voltage to the Secondary Alternative is enabled.

## autoclass\_enable

A variable indicating that the PSE is enabled to check if the PD is requesting Autoclass via Physical Layer classification; see 145.2.8.2 and 145.3.6.2.

## Values:

- FALSE: Autoclass is disabled in the PSE.
- TRUE: Autoclass is enabled in the PSE.

## class\_4PID\_mult\_events\_pri

A variable indicating if the PSE generates 3 class events on the Primary Alternative to determine if a dual-signature PD is a candidate for 4-pair power.

## Values:

- FALSE: The PSE does not need to generate 3 class events to determine if the PD is a candidate for 4-pair power.
- TRUE: The PSE generates at least 3 class events to determine if the PD is a candidate for 4-pair power.

## class\_4PID\_mult\_events\_sec

A variable indicating if the PSE generates 3 class events on the Secondary Alternative to determine if a dual-signature PD is a candidate for 4-pair power.

## Values:

- FALSE: The PSE does not need to generate 3 class events to determine if the PD is a candidate for 4-pair power.
- TRUE: The PSE generates at least 3 class events to determine if the PD is a candidate for 4-pair power.

## det\_once\_sec

This variable indicates if the PSE has probed the Secondary Alternative at least once following exit from ENTRY\_SEC.

## Values:

- FALSE: The PSE has not probed the Secondary Alternative since entering the Secondary Alternative state diagram.
- TRUE: The PSE has probed the Secondary Alternative at least once since entering the Secondary Alternative state diagram.

## det\_start\_pri

A variable that indicates to the Secondary Alternative that the Primary Alternative is between START\_DETECT and POWER\_UP.

## Values:

- FALSE: The Primary Alternative is not between START\_DETECT and POWER\_UP.
- TRUE: The Primary Alternative is between START\_DETECT and POWER\_UP.

## det\_start\_sec

A variable that indicates to the Primary Alternative that the Secondary Alternative is between START\_DETECT and POWER\_UP.

## Values:

- FALSE: The Secondary Alternative is not between START\_DETECT and POWER\_UP.
- TRUE: The Secondary Alternative is between START\_DETECT and POWER\_UP.

## det\_temp

A variable that indicates whether a 4-pair PSE has completed detection on one and only one Alternative or if the PSE has completed detection on neither or both Alternatives.

## Values:

- both\_neither: The PSE has completed detection on both Alternatives or neither Alternatives.
- only\_one: The PSE has completed detection on only one Alternative.

**error\_condition**

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145–16 and that require the PSE not to source power. This variable may be set by the PSE at any time.

Values:

- FALSE: No fault indication.  
TRUE: A fault indication exists.

**error\_condition\_pri**

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145–16 and that require the PSE not to source power over the Primary Alternative. This variable may be set by the PSE at any time.

Values:

- FALSE: No fault indication.  
TRUE: A fault indication exists.

**error\_condition\_sec**

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145–16 and that require the PSE not to source power over the Secondary Alternative. This variable may be set by the PSE at any time.

Values:

- FALSE: No fault indication.  
TRUE: A fault indication exists.

**error\_pri**

Alias for the following terms: short\_det\_pri + ovld\_det\_pri + option\_vport\_lim\_pri.

**error\_sec**

Alias for the following terms: short\_det\_sec + ovld\_det\_sec + option\_vport\_lim\_sec.

**iclass\_lim\_det**

A variable indicating if any  $I_{Class}$  measured by the PSE during do\_classification is invalid or equal to or greater than  $I_{Class\_LIM\ min}$  as defined in Table 145–14. This variable is set per this description.

Values:

- FALSE: Measured  $I_{Class}$  is not invalid or is less than  $I_{Class\_LIM\ min}$  during do\_classification or this function is not active.  
TRUE: Measured  $I_{Class}$  is invalid or equal to or greater than  $I_{Class\_LIM\ min}$  during do\_classification.

**iclass\_lim\_det\_pri**

A variable indicating if any  $I_{Class}$  measured by the PSE over the Primary Alternative during do\_classification\_pri is invalid or equal to or greater than  $I_{Class\_LIM\ min}$  as defined in Table 145–14. This variable is set per this description.

Values:

- FALSE: Measured  $I_{Class}$  over the Primary Alternative is not invalid or is less than  $I_{Class\_LIM\ min}$  during do\_classification\_pri or this function is not active.  
TRUE: Measured  $I_{Class}$  over the Primary Alternative is invalid or equal to or greater than  $I_{Class\_LIM\ min}$  during do\_classification\_pri.

**iclass\_lim\_det\_sec**

A variable indicating if any  $I_{Class}$  measured by the PSE over the Secondary Alternative during do\_classification\_sec is invalid or equal to or greater than  $I_{Class\_LIM\ min}$  as defined in Table 145–14. This variable is set per this description.

Values:

- FALSE: Measured  $I_{Class}$  over the Secondary Alternative is not invalid or is less than  $I_{Class\_LIM\ min}$  during do\_classification\_sec or this function is not active.

TRUE: Measured  $I_{Class}$  over the Secondary Alternative is invalid or equal to or greater than  $I_{Class\_LIM}$  min during `do_classification_sec`.

#### MirroredPDAutoclassRequest

A variable output by the PSE power control state diagram that indicates whether the PSE has received an Autoclass measurement request from the PD via the Data Link Layer. See 145.5. This variable is assigned through Table 145–38.

Values:

FALSE: The PSE has not received an Autoclass measurement request from PD.  
TRUE: The PSE has received an Autoclass measurement request from PD.

#### mps\_valid

The PSE monitors the Maintain Power Signature (MPS, see 145.2.12). This variable indicates the presence or absence of a valid MPS, when the connected PD is a single-signature PD, or the PSE is operating in 2-pair mode. This variable is set per this description.

Values:

FALSE: MPS is absent.  
TRUE: MPS is present.

#### mps\_valid\_pri

The PSE monitors the Maintain Power Signature (MPS, see 145.2.12) on the Primary Alternative. This variable indicates the presence or absence of a valid MPS on the Primary Alternative, when the connected PD is a dual-signature PD. This variable is set per this description.

Values:

FALSE: MPS is absent.  
TRUE: MPS is present.

#### mps\_valid\_sec

The PSE monitors the Maintain Power Signature (MPS, see 145.2.12) on the Secondary Alternative. This variable indicates the presence or absence of a valid MPS on the Secondary Alternative, when the connected PD is a dual-signature PD. This variable is set per this description.

Values:

FALSE: MPS is absent.  
TRUE: MPS is present.

#### option\_2ev

This variable indicates if PSE will generate 2 or 3 class events when `pse_avail_pwr` is 4.

Values:

FALSE: The PSE is not restricted to 2 class events when `pse_avail_pwr` is 4.  
TRUE: The PSE is restricted to 2 class events when `pse_avail_pwr` is 4.

#### option\_class\_probe

This variable indicates if the PSE should determine the PD requested Class via the `do_class_probe` function. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying  $V_{Reset}$  for at least  $T_{Reset}$  to the PI (see Table 145–14), followed by a normal classification procedure.

Values:

FALSE: The PSE will not probe for the PD requested Class.  
TRUE: The PSE probes for the PD requested Class.

#### option\_class\_probe\_pri

This variable indicates if the PSE should determine the PD requested Class on the Primary Alternative via the `do_class_probe_pri` function. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying  $V_{Reset}$  for at least  $T_{Reset}$  to the Primary Alternative (see Table 145–14).

Values:

FALSE: The PSE will not probe for the PD requested Class.  
TRUE: The PSE probes for the PD requested Class.

**option\_class\_probe\_sec**

This variable indicates if the PSE should determine the PD requested Class on the Secondary Alternative via the `do_class_probe_sec` function. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying  $V_{Reset}$  for at least  $T_{Reset}$  to the Secondary Alternative (see Table 145–14).

Values:

- FALSE: The PSE will not probe for the PD requested Class.
- TRUE: The PSE probes for the PD requested Class.

**option\_detect\_ted**

This variable indicates if detection can be performed by the PSE during the `ted_timer` interval.

Values:

- FALSE: Do not perform detection during `ted_timer` interval.
- TRUE: Perform detection during `ted_timer` interval.

**option\_detect\_ted\_pri**

This variable indicates if detection can be performed by the PSE on the Primary Alternative during the `ted_timer_pri` interval.

Values:

- FALSE: Do not perform detection during `ted_timer_pri` interval.
- TRUE: Perform detection during `ted_timer_pri` interval.

**option\_detect\_ted\_sec**

This variable indicates if detection can be performed by the PSE on the Secondary Alternative during the `ted_timer_sec` interval.

Values:

- FALSE: Do not perform detection during `ted_timer_sec` interval.
- TRUE: Perform detection during `ted_timer_sec` interval.

**option\_probe\_alt\_sec**

This variable indicates if the PSE will continue to detect and conditionally perform Physical Layer classification on the Secondary Alternative in the event power is not applied to the Primary Alternative.

Values:

- FALSE: PSE does not probe the Secondary Alternative if power is not applied to the Primary Alternative.
- TRUE: PSE does probe the Secondary Alternative if power is not applied to the Primary Alternative.

**option\_vport\_lim\_pri**

This variable indicates if  $V_{PSE}$  on the Primary Alternative is out of the operating range during normal operating state. This variable is set per this description.

Values:

- FALSE:  $V_{PSE}$  on the Primary Alternative is within the  $V_{Port\_PSE-2P}$  operating range as defined in Table 145–16 or the PSE does not implement this option.
- TRUE:  $V_{PSE}$  on the Primary Alternative is outside of the  $V_{Port\_PSE-2P}$  operating range as defined in Table 145–16.

**option\_vport\_lim\_sec**

This variable indicates if  $V_{PSE}$  on the Secondary Alternative is out of the operating range during normal operating state. This variable is set per this description.

Values:

- FALSE:  $V_{PSE}$  on the Secondary Alternative is within the  $V_{Port\_PSE-2P}$  operating range as defined in Table 145–16 or the PSE does not implement this option.
- TRUE:  $V_{PSE}$  on the Secondary Alternative is outside of the  $V_{Port\_PSE-2P}$  operating range as defined in Table 145–16.

**ovld\_det\_pri**

A variable indicating if the PSE output current has been in an overload condition on the Primary Alternative; see 145.2.10.8. This variable is set per this description.

## Values:

- FALSE: The PSE has not detected an overload condition on the Primary Alternative.  
 TRUE: The PSE has detected an overload condition on the Primary Alternative.

**ovld\_det\_sec**

A variable indicating if the PSE output current has been in an overload condition on the Secondary Alternative; see 145.2.10.8. This variable is set per this description.

## Values:

- FALSE: The PSE has not detected an overload condition on the Secondary Alternative.  
 TRUE: The PSE has detected an overload condition on the Secondary Alternative.

**pd\_4pair\_cand**

This variable is used by the PSE to indicate that a connected PD is a candidate to receive power on both Modes. This variable is a function of the results of detection, connection check, Physical Layer classification, and PD 4PID; see 145.2.9.

## Values:

- FALSE: The PD is not a candidate to receive power on both Modes.  
 TRUE: The PD is a candidate to receive power on both Modes.

**pd\_cls\_4PID\_pri**

This variable indicates that the Type of the dual-signature PD has been established on the Primary Alternative by Physical Layer classification.

## Values:

- FALSE: The PD is not a candidate for 4-pair power or the PSE has not used Physical Layer classification to determine the PD Type.  
 TRUE: The PD is a candidate for 4-pair power and has been identified as a Type 3 or Type 4 PD, see Table 145–27.

**pd\_cls\_4PID\_sec**

This variable indicates that the Type of the dual-signature PD has been established on the Secondary Alternative by Physical Layer classification.

## Values:

- FALSE: The PD is not a candidate for 4-pair power or the PSE has not used Physical Layer classification to determine the PD Type.  
 TRUE: The PD is a candidate for 4-pair power and has been identified as a Type 3 or Type 4 PD, see Table 145–27.

**pd\_req\_pwr**

The variable indicates the PD requested Class. When a PD requests a higher Class than a PSE can support, the PSE assigns the PD to Class 3, Class 4, or Class 6, whichever is the highest Class it can support. If pse\_avail\_pwr is less than 4 and option\_class\_probe is FALSE, this variable may not contain the PD requested Class; do\_class\_probe also returns this variable.

## Values:

- 0: Class 0  
 1: Class 1  
 2: Class 2  
 3: Class 3  
 4: Class 4  
 5: Class 5  
 6: Class 6  
 7: Class 7  
 8: Class 8

**power\_available**

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 145.2.8. This variable may be set by the PSE at any time.

Values:

- FALSE: PSE is no longer capable of sourcing power to a PD.
- TRUE: PSE is capable to continue to source power to a PD.

**power\_available\_pri**

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power on the Primary Alternative to support the attached PD. Sufficient power is defined by classification; see 145.2.8. This variable may be set by the PSE at any time.

Values:

- FALSE: PSE is no longer capable of sourcing power on the Primary Alternative.
- TRUE: PSE is capable to continue to source power on the Primary Alternative.

**power\_available\_sec**

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power on the Secondary Alternative to support the attached PD. Sufficient power is defined by classification; see 145.2.8. This variable may be set by the PSE at any time.

Values:

- FALSE: PSE is no longer capable of sourcing power on the Secondary Alternative.
- TRUE: PSE is capable to continue to source power on the Secondary Alternative.

**pse\_allocated\_pwr**

A variable that indicates the Class that has been assigned to the PD.

Values:

- 0: No power has been assigned to the PD
- 1: Class 1
- 2: Class 2
- 3: Class 3
- 4: Class 4
- 5: Class 5
- 6: Class 6
- 7: Class 7
- 8: Class 8

**pse\_alternative**

This variable indicates which Pinout Alternative the PSE uses to apply power to the PI (see Table 145–3).

Values:

- a: The PSE uses PSE pinout Alternative A.
- b: The PSE uses PSE pinout Alternative B.
- both: The PSE uses both Alternative A and Alternative B.

**pse\_avail\_pwr**

This variable indicates the highest Class the PSE may assign to the PD by Physical Layer classification. The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

- 1: Class 1
- 2: Class 2
- 3: Class 3
- 4: Class 4
- 5: Class 5
- 6: Class 6

7: Class 7  
 8: Class 8

**pse\_avail\_pwr\_pri**

This variable indicates the highest Class the PSE may assign to the PD by Physical Layer classification on the Primary Alternative. The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

1: Class 1  
 2: Class 2  
 3: Class 3  
 4: Class 4  
 5: Class 5

**pse\_avail\_pwr\_sec**

This variable indicates the highest Class the PSE may assign to the PD by Physical Layer classification on the Secondary Alternative. The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

1: Class 1  
 2: Class 2  
 3: Class 3  
 4: Class 4  
 5: Class 5

**pse\_dll\_capable**

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 145.5 for a description of Data Link Layer functionality. A variable that is set in an implementation-dependent manner.

Values:

FALSE: The PSE's Data Link Layer classification capability is not enabled.  
 TRUE: The PSE's Data Link Layer classification capability is enabled.

**pse\_dll\_enable**

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 145.5.

Values:

FALSE: Data Link Layer classification is not enabled.  
 TRUE: Data Link Layer classification is enabled.

**pse\_dll\_ready**

An implementation-specific variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20). This variable may be set by the PSE at any time.

Values:

FALSE: Data Link Layer classification has not completed initialization.  
 TRUE: Data Link Layer classification has completed initialization.

**pse\_enable**

A variable that selects PSE operation. This variable may be set by the PSE at any time.

Values:

disable: All PSE functions disabled (behavior is as if there was no PSE functionality).  
 enable: Normal PSE operation.

**pse\_power\_update**

A variable that is set when the PSEAllocatedPowerValue in the DLL state diagram in Figure 145–40 has been updated. This variable may be set by the PSE at any time.

Values:

FALSE: The value of PSEAllocatedPowerValue has not changed.  
 TRUE: The value of PSEAllocatedPowerValue has changed.

pse\_power\_update\_pri

A variable that is set when the PSEAllocatedPowerValue\_alt(X) in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated, where X is the Primary Alternative. This variable may be set by the PSE at any time.

Values:

- FALSE: The value of PSEAllocatedPowerValue\_alt(X) has not changed.
- TRUE: The value of PSEAllocatedPowerValue\_alt(X) has changed.

pse\_power\_update\_sec

A variable that is set when the PSEAllocatedPowerValue\_alt(X) in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated, where X is the Secondary Alternative. This variable may be set by the PSE at any time.

Values:

- FALSE: The value of PSEAllocatedPowerValue\_alt(X) has not changed.
- TRUE: The value of PSEAllocatedPowerValue\_alt(X) has changed.

pse\_ready

Variable that is asserted in an implementation-dependent manner to probe the link segment. This variable may be set by the PSE at any time.

Values:

- FALSE: PSE is not ready to probe the link segment.
- TRUE: PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid detection signature is detected due to the delay it introduces between detection attempts (see 145.2.5.1).

pse\_reset

Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality. This variable is set per this description.

Values:

- FALSE: Do not reset the PSE state diagram.
- TRUE: Reset the PSE state diagram.

pse\_reset\_pri

Controls the resetting of the PSE state diagram on Primary Alternative. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE Primary Alternative functionality. This variable is set per this description.

Values:

- FALSE: Do not reset the PSE state diagram.
- TRUE: Reset the PSE state diagram.

pse\_reset\_sec

Controls the resetting of the PSE state diagram on Secondary Alternative. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE Secondary Alternative functionality. This variable is set per this description.

Values:

- FALSE: Do not reset the PSE state diagram.
- TRUE: Reset the PSE state diagram.

pse\_ss\_mode

A variable that controls whether the PSE provides power over 2 pair or 4 pair to a single-signature PD assigned to Class 1 through Class 4. This variable may be set by the PSE at any time.

- 0: Single-signature PD is powered over 2 pair.
- 1: Single-signature PD is powered over 4 pair.

**pse\_ss\_mode\_update**

A variable that is used to cause the PSE to re-evaluate the value of `pse_ss_mode` when it is in `POWER_ON`. This variable may be set by the PSE at any time.

Values:

- FALSE: `pse_ss_mode` is not re-evaluated.
- TRUE: `pse_ss_mode` will be re-evaluated.

**pwr\_app\_pri**

A variable indicating that the PSE has begun steady state operation on the Primary Alternative by having asserted `alt_pwrd_pri`, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the `POWER_UP` requirements of 145.2.10.7. This variable is set per this description.

Values:

- FALSE: The PSE is either not applying power or has begun applying power but is still in `POWER_UP` on the Primary Alternative.
- TRUE: The PSE has begun steady state operation on the Primary Alternative.

**pwr\_app\_sec**

A variable indicating that the PSE has begun steady state operation on the Secondary Alternative by having asserted `alt_pwrd_sec`, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the `POWER_UP` requirements of 145.2.10.7. This variable is set per this description.

Values:

- FALSE: The PSE is either not applying power or has begun applying power but is still in `POWER_UP` on the Secondary Alternative.
- TRUE: The PSE has begun steady state operation on the Secondary Alternative.

**semi\_pwr\_en**

A variable indicating if, in the case of a single-signature PD, the PSE uses the method consisting of turning off only the pairset on which a short-circuit, overload or out of range  $V_{PSE}$  is detected.

Values:

- TRUE: Only the pairset with the fault condition is turned off.
- FALSE: Both pairsets are turned off if there is a fault on one pairset.

**short\_det\_pri**

A variable indicating if the PSE output current has been in a short circuit condition on the Primary Alternative. This variable is set per this description. See 145.2.10.9.

Values:

- FALSE: The PSE has not detected a short circuit condition on the Primary Alternative.
- TRUE: The PSE has detected a short circuit condition on the Primary Alternative.

**short\_det\_sec**

A variable indicating if the PSE output current has been in a short circuit condition on the Secondary Alternative. This variable is set per this description. See 145.2.10.9.

Values:

- FALSE: The PSE has not detected a short circuit condition on the Secondary Alternative.
- TRUE: The PSE has detected a short circuit condition on the Secondary Alternative.

**sism**

A variable used by the single-signature state diagram to initiate the semi-independent dual-signature state diagrams.

Values:

- FALSE: Single-signature state diagram has control of the Alternatives.
- TRUE: Single-signature state diagram has passed control of the Alternatives to the semi-independent dual-signature state diagrams.

**temp\_var**

A variable used to store the previous value of the variable `pd_class_sig`.

**temp\_var\_pri**

A variable used to store the previous value of the variable `pd_class_sig_pri` for the Primary Alternative.

temp\_var\_sec

A variable used to store the previous value of the variable pd\_class\_sig\_sec for the Secondary Alternative.

PSEs shall set pse\_avail\_pwr, pse\_avail\_pwr\_pri, and pse\_avail\_pwr\_sec from the range in Table 145–6.

**Table 145–6—Allowed Type 3 and Type 4 PSE permutations for pse\_avail\_pwr**

| PSE Type | pse_avail_pwr | pse_avail_pwr_pri, pse_avail_pwr_sec |
|----------|---------------|--------------------------------------|
| Type 3   | 1 to 6        | 1 to 4                               |
| Type 4   | 1 to 8        | 1 to 5                               |

#### 145.2.5.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop  $x$ \_timer” is asserted.

tauto\_pse1\_timer

A timer used to delay Autoclass power measurement following transition into POWER\_ON; see  $T_{\text{AUTO\_PSE1}}$  in Table 145–15.

tauto\_pse2\_timer

A timer used to limit Autoclass power measurement following transition into POWER\_ON; see  $T_{\text{AUTO\_PSE2}}$  in Table 145–15.

tcc2det\_timer

A timer used to limit the time between connection check and detection when CC\_DET\_SEQ = 0 or CC\_DET\_SEQ = 3. See  $T_{\text{cc2det}}$  in Table 145–10.

tcev\_timer

A timer used to limit the second through fifth class event time in Multiple-Event classification; see  $T_{\text{CEV}}$  in Table 145–14.

tcev\_timer\_pri

A timer used to limit the second through fourth class event time in Multiple-Event classification on the Primary Alternative; see  $T_{\text{CEV}}$  in Table 145–14.

tcev\_timer\_sec

A timer used to limit the second through fourth class event time in Multiple-Event classification on the Secondary Alternative; see  $T_{\text{CEV}}$  in Table 145–14.

tclass\_acs\_timer

A timer used to indicate when the PSE may measure the class current during the first long class event, to check if the PD is requesting Autoclass. See  $T_{\text{Class\_ACS}}$  in Table 145–14.

tclass\_reset\_timer

A timer used to limit the classification reset time; See  $T_{\text{Reset}}$  in Table 145–14.

tclass\_reset\_timer\_pri

A timer used to limit the classification reset time on the Primary Alternative; see  $T_{\text{Reset}}$  in Table 145–14.

tclass\_reset\_timer\_sec

A timer used to limit the classification reset time on the Secondary Alternative; see  $T_{\text{Reset}}$  in Table 145–14.

- tdbo\_timer**  
 A timer used to regulate backoff upon detection of an invalid detection signature; see  $T_{dbo}$  in Table 145–16.
- tdet\_timer**  
 A timer used to limit an attempt to detect a PD; see  $T_{det}$  in Table 145–16.
- tdet\_timer\_pri**  
 A timer used to limit an attempt to detect a PD on the Primary Alternative; see  $T_{det}$  in Table 145–16.
- tdet\_timer\_sec**  
 A timer used to limit an attempt to detect a PD on the Secondary Alternative; see  $T_{det}$  in Table 145–16.
- tdet2det\_timer**  
 A timer used to limit the time between the completion of a detection on one pairset and the beginning of a detection on the other; see  $T_{det2det}$  in Table 145–10.
- ted\_timer**  
 A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see  $T_{ed}$  in Table 145–16. The default state of this timer is `ted_timer_done`.
- ted\_timer\_pri**  
 A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal from the Primary Alternative; see  $T_{ed}$  in Table 145–16. The default state of this timer is `ted_timer_pri_done`.
- ted\_timer\_sec**  
 A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal from the Secondary Alternative; see  $T_{ed}$  in Table 145–16. The default state of this timer is `ted_timer_sec_done`.
- tinrush\_timer\_pri**  
 A timer used to monitor the duration of the inrush event on the Primary Alternative; see  $T_{Inrush}$  in Table 145–16.
- tinrush\_timer\_sec**  
 A timer used to monitor the duration of the inrush event on the Secondary Alternative; see  $T_{Inrush}$  in Table 145–16.
- tlce\_timer**  
 A timer used to limit the first class event time in Multiple-Event classification; see  $T_{LCE}$  in Table 145–14.
- tlce\_timer\_pri**  
 A timer used to limit the first class event time in Multiple-Event classification on the Primary Alternative; see  $T_{LCE}$  in Table 145–14.
- tlce\_timer\_sec**  
 A timer used to limit the first class event time in Multiple-Event classification on the Secondary Alternative; see  $T_{LCE}$  in Table 145–14.
- tme1\_timer**  
 A timer used to limit mark event times for all but the last mark event time during Multiple-Event classification; see  $T_{ME1}$  in Table 145–14.
- tme1\_timer\_pri**  
 A timer used to limit mark event times for all but the last mark event time during Multiple-Event classification on the Primary Alternative; see  $T_{ME1}$  in Table 145–14.
- tme1\_timer\_sec**  
 A timer used to limit mark event times for all but the last mark event time during Multiple-Event classification on the Secondary Alternative; see  $T_{ME1}$  in Table 145–14.

tme2\_timer

A timer used to limit the final mark event time in Multiple-Event classification; see  $T_{ME2}$  in Table 145–14.

tme2\_timer\_pri

A timer used to limit the final mark event time in Multiple-Event classification on the Primary Alternative; see  $T_{ME2}$  in Table 145–14.

tme2\_timer\_sec

A timer used to limit the final mark event time in Multiple-Event classification on the Secondary Alternative; see  $T_{ME2}$  in Table 145–14

tmpdo\_timer

A timer used to monitor the dropout of the MPS; see  $T_{MPDO}$  in Table 145–16.

tmpdo\_timer\_pri

A timer used to monitor the dropout of the MPS on the Primary Alternative; see  $T_{MPDO}$  in Table 145–16.

tmpdo\_timer\_sec

A timer used to monitor the dropout of the MPS on the Secondary Alternative; see  $T_{MPDO}$  in Table 145–16.

tpon\_timer

A timer used to limit the time for power turn-on; see  $T_{pon}$  in Table 145–16.

tpon\_timer\_pri

A timer used to limit the time on the Primary Alternative for power turn-on; see  $T_{pon}$  in Table 145–16.

tpon\_timer\_sec

A timer used to limit the time on the Secondary Alternative for power turn-on; see  $T_{pon}$  in Table 145–16.

#### 145.2.5.6 Functions

The variable formed by the function name appended with “\_done” is used to indicate when the function has completed. This variable is set to FALSE when the function is called and is set to TRUE once the function is complete and its output variables are valid.

do\_autoclass\_measure

This function measures  $P_{Autoclass}$  as defined in 145.2.8.2.

do\_autoclassification

This function returns the following variable:

pd\_autoclass: This variable indicates whether the PD requests Autoclass during Physical Layer classification. pd\_autoclass is set to True when a class signature of ‘0’ is detected during the  $T_{Class\_ACS}$  window, as defined in Table 145–14, otherwise it is set to False.

Values:

|        |                                    |
|--------|------------------------------------|
| FALSE: | The PD does not request Autoclass. |
| TRUE:  | The PD requests Autoclass.         |

do\_class\_probe

This function discovers the PD requested Class by producing a number of class events. The class events produced are limited to CLASS\_EV1\_LCE to MARK\_EV3. The tlce\_timer in CLASS\_EV1\_LCE may be replaced with the tcev\_timer to allow abbreviated class timing duration. This function returns the following variable:

pd\_req\_pwr: See pd\_req\_pwr in 145.2.5.4.

**do\_class\_probe\_pri**

This function discovers the PD requested Class by producing a number of class events on the Primary Alternative. The class events produced are limited to CLASS\_EV1\_LCE\_PRI to MARK\_EV3\_PRI. The tlce\_timer\_pri in CLASS\_EV1\_LCE\_PRI may be replaced with the tcev\_timer\_pri to allow abbreviated class timing duration. This function returns the following variables:

pd\_req\_pwr\_pri: See do\_classification\_pri function.

pd\_cls\_4PID\_pri: See pd\_cls\_4PID\_pri in 145.2.5.4.

**do\_class\_probe\_sec**

This function discovers the PD requested Class by producing a number of class events on the Secondary Alternative. The class events produced are limited to CLASS\_EV1\_LCE\_SEC to MARK\_EV3\_SEC. The tlce\_timer\_sec in CLASS\_EV1\_LCE\_SEC may be replaced with the tcev\_timer\_sec to allow abbreviated class timing duration. This function returns the following variables:

pd\_req\_pwr\_sec: See do\_classification\_sec function.

pd\_cls\_4PID\_sec: See pd\_cls\_4PID\_sec in 145.2.5.4.

**do\_class\_reset**

This function produces the classification reset voltage; See  $V_{Reset}$  in Table 145–14. This function does not return any variables.

**do\_class\_reset\_pri**

This function produces the classification reset voltage on the Primary Alternative; See  $V_{Reset}$  in Table 145–14. This function does not return any variables.

**do\_class\_reset\_sec**

This function produces the classification reset voltage on the Secondary Alternative; See  $V_{Reset}$  in Table 145–14. This function does not return any variables.

**do\_classification**

This function produces the classification event voltage and determines the PD's class signature. This function returns the following variable:

pd\_class\_sig: The PD class signature seen on the negative pair or pairs during the most recent class event; see Table 145–13 and 145.2.8.

Values:

- 0: class signature 0
- 1: class signature 1
- 2: class signature 2
- 3: class signature 3
- 4: class signature 4

**do\_classification\_pri**

This function produces the classification event voltage and determines the PD's class signature for the Primary Alternative. This function returns the following variables for the Primary Alternative:

**pd\_req\_pwr\_pri:** This variable indicates the PD requested Class. When a PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support. See 145.2.8. The returned value is based on all previous **do\_classification\_pri** function calls since the last time in **DETECT\_EVAL\_PRI** or **CLASS\_RESET\_PRI**. See Table 145–27 for a determination of the PD requested Class.

Values:

|    |         |
|----|---------|
| 1: | Class 1 |
| 2: | Class 2 |
| 3: | Class 3 |
| 4: | Class 4 |
| 5: | Class 5 |

**pse\_allocated\_pwr\_pri:** This variable indicates the Class assigned to the PD for the Primary Alternative. The returned value is based on all previous **do\_classification\_pri** function calls since the last time in **DETECT\_EVAL\_PRI** or **CLASS\_RESET\_PRI**. See Table 145–11 for a determination of the PSE assigned Class.

Values:

|    |         |
|----|---------|
| 1: | Class 1 |
| 2: | Class 2 |
| 3: | Class 3 |
| 4: | Class 4 |
| 5: | Class 5 |

**pd\_class\_sig\_pri:** The PD class signature seen on the negative pair associated with the Primary Alternative during the most recent class event; see Table 145–13 and 145.2.8.

Values:

|    |                   |
|----|-------------------|
| 0: | class signature 0 |
| 1: | class signature 1 |
| 2: | class signature 2 |
| 3: | class signature 3 |
| 4: | class signature 4 |

**do\_classification\_sec**

This function produces the classification event voltage and determines the PD's class signature for the Secondary Alternative. This function returns the following variables for the Secondary Alternative:

**pd\_req\_pwr\_sec:** This variable indicates the PD requested Class. When a PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support. See 145.2.8. The returned value is based on all previous **do\_classification\_sec** function calls since the last time in **DETECT\_EVAL\_SEC** or **CLASS\_RESET\_SEC**. See Table 145–27 for a determination of the PD requested Class.

Values:

|    |         |
|----|---------|
| 1: | Class 1 |
| 2: | Class 2 |
| 3: | Class 3 |
| 4: | Class 4 |
| 5: | Class 5 |

**pse\_allocated\_pwr\_sec:** This variable indicates the Class assigned to the PD for the Secondary Alternative. The returned value is based on all previous **do\_classification\_sec** function calls since the last time in **DETECT\_EVAL\_SEC** or **CLASS\_RESET\_SEC**. See Table 145–11 for a determination of the PSE assigned Class.

Values:

|    |         |
|----|---------|
| 1: | Class 1 |
| 2: | Class 2 |
| 3: | Class 3 |
| 4: | Class 4 |
| 5: | Class 5 |

**pd\_class\_sig\_sec:** The PD class signature seen on the negative pair associated with the Secondary Alternative during the most recent class event; see Table 145–13 and 145.2.8.

Values:

|    |                   |
|----|-------------------|
| 0: | class signature 0 |
| 1: | class signature 1 |
| 2: | class signature 2 |
| 3: | class signature 3 |
| 4: | class signature 4 |

**do\_cxn\_chk**

This function initiates the Connection Check as defined in 145.2.7. This function returns the following variable:

**sig\_type:** This variable indicates the PD signature configuration connected to the PI, with respect to 4-pair operation.

Values:

|          |                                                                                                                                          |
|----------|------------------------------------------------------------------------------------------------------------------------------------------|
| invalid: | Neither a single-signature nor a dual-signature configuration has been found. This includes an open circuit condition on either pairset. |
| single:  | The PSE has determined there is a single-signature PD configuration connected to the PI.                                                 |
| dual:    | The PSE has determined there is a dual-signature PD configuration connected to the PI.                                                   |

**do\_detect\_pri**

This function returns the following variables (see 145.2.6):

**sig\_pri:** This variable indicates the presence or absence of a valid PD detection signature on the Primary Alternative.

Values:

|               |                                                                            |
|---------------|----------------------------------------------------------------------------|
| open_circuit: | The PSE has detected an open circuit.                                      |
| valid:        | The PSE has detected a valid PD detection signature.                       |
| invalid:      | Neither an open circuit nor a valid PD detection signature has been found. |

**do\_detect\_sec**

This function returns the following variables (see 145.2.6):

**sig\_sec:** This variable indicates the presence or absence of a valid PD detection signature on the Secondary Alternative.

Values:

|               |                                                                            |
|---------------|----------------------------------------------------------------------------|
| open_circuit: | The PSE has detected an open circuit.                                      |
| valid:        | The PSE has detected a valid PD detection signature.                       |
| invalid:      | Neither an open circuit nor a valid PD detection signature has been found. |

do\_initialize

This function returns the following variables (see 145.2.5.4):

alt\_pri  
autoclass\_enable  
class\_4PID\_mult\_events\_pri  
class\_4PID\_mult\_events\_sec  
option\_2ev  
option\_class\_probe  
option\_class\_probe\_pri  
option\_class\_probe\_sec  
option\_detect\_ted  
option\_detect\_ted\_pri  
option\_detect\_ted\_sec  
option\_probe\_alt\_sec  
pse\_alternative  
pse\_avail\_pwr  
pse\_avail\_pwr\_pri  
pse\_avail\_pwr\_sec  
pse\_dll\_capable  
semi\_pwr\_en

do\_mark

This function produces the classification mark event voltage. This function does not return any variables.

do\_mark\_pri

This function produces the classification mark event voltage on the Primary Alternative. This function does not return any variables.

do\_mark\_sec

This function produces the classification mark event voltage on the Secondary Alternative. This function does not return any variables.

do\_update\_pse\_allocated\_pwr

A function that updates the pse\_allocated\_pwr based on the value of PSEAllocatedPowerValue as defined in Table 145–12. This function returns the following variable:

pse\_allocated\_pwr: See pse\_allocated\_pwr in 145.2.5.4.

do\_update\_pse\_allocated\_pwr\_pri

A function that updates the pse\_allocated\_pwr\_pri value based on the value of PSEAllocatedPowerValue\_alt(X) as defined in Table 145–12. This function returns the following variable:

pse\_allocated\_pwr\_pri: See pse\_allocated\_pwr\_pri in 145.2.5.4.

do\_update\_pse\_allocated\_pwr\_sec

A function that updates the pse\_allocated\_pwr\_sec value based on the value of PSEAllocatedPowerValue\_alt(X) as defined in Table 145–12. This function returns the following variable:

pse\_allocated\_pwr\_sec: See pse\_allocated\_pwr\_sec in 145.2.5.4.

## 145.2.5.7 State diagrams

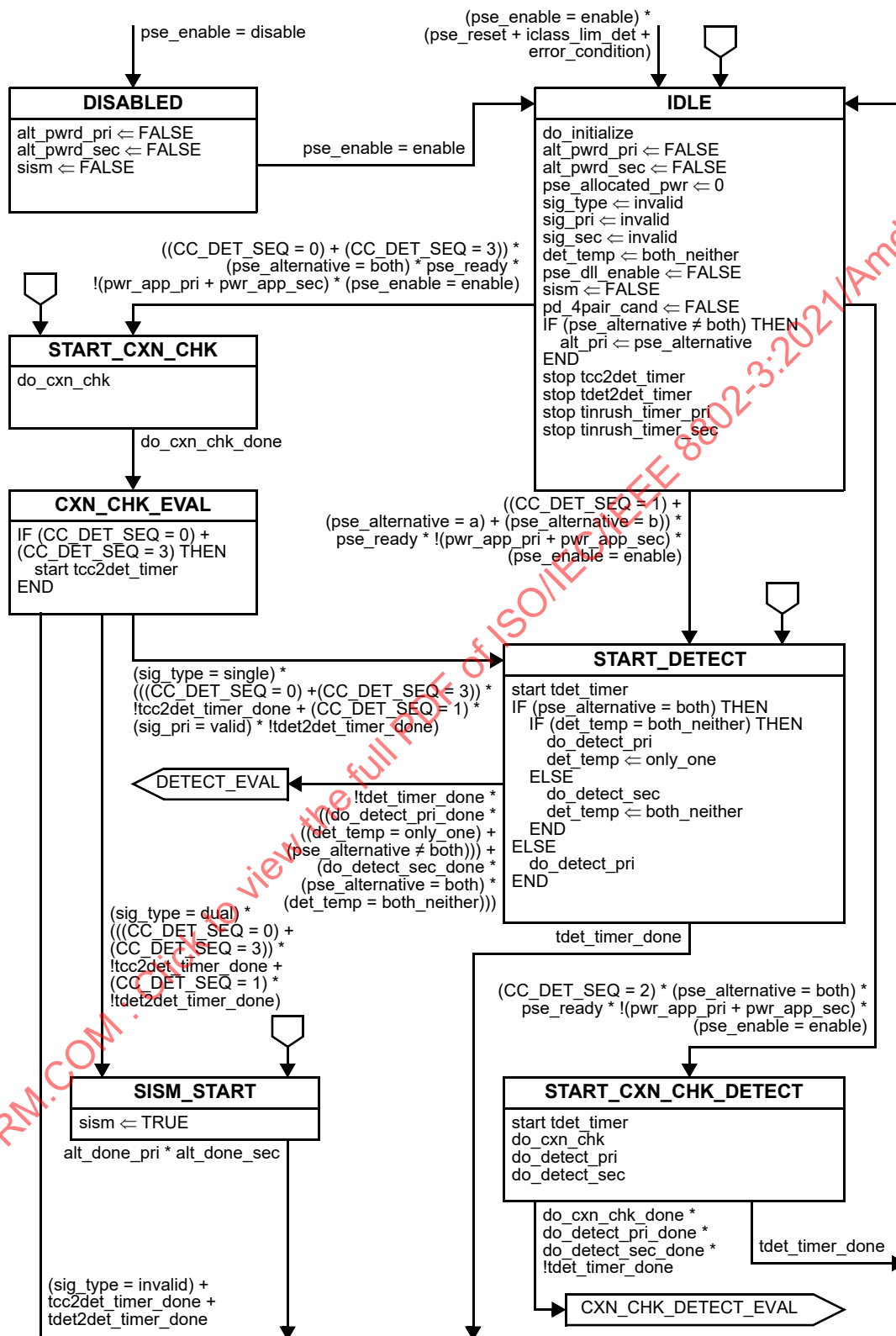


Figure 145–13—Top level PSE state diagram

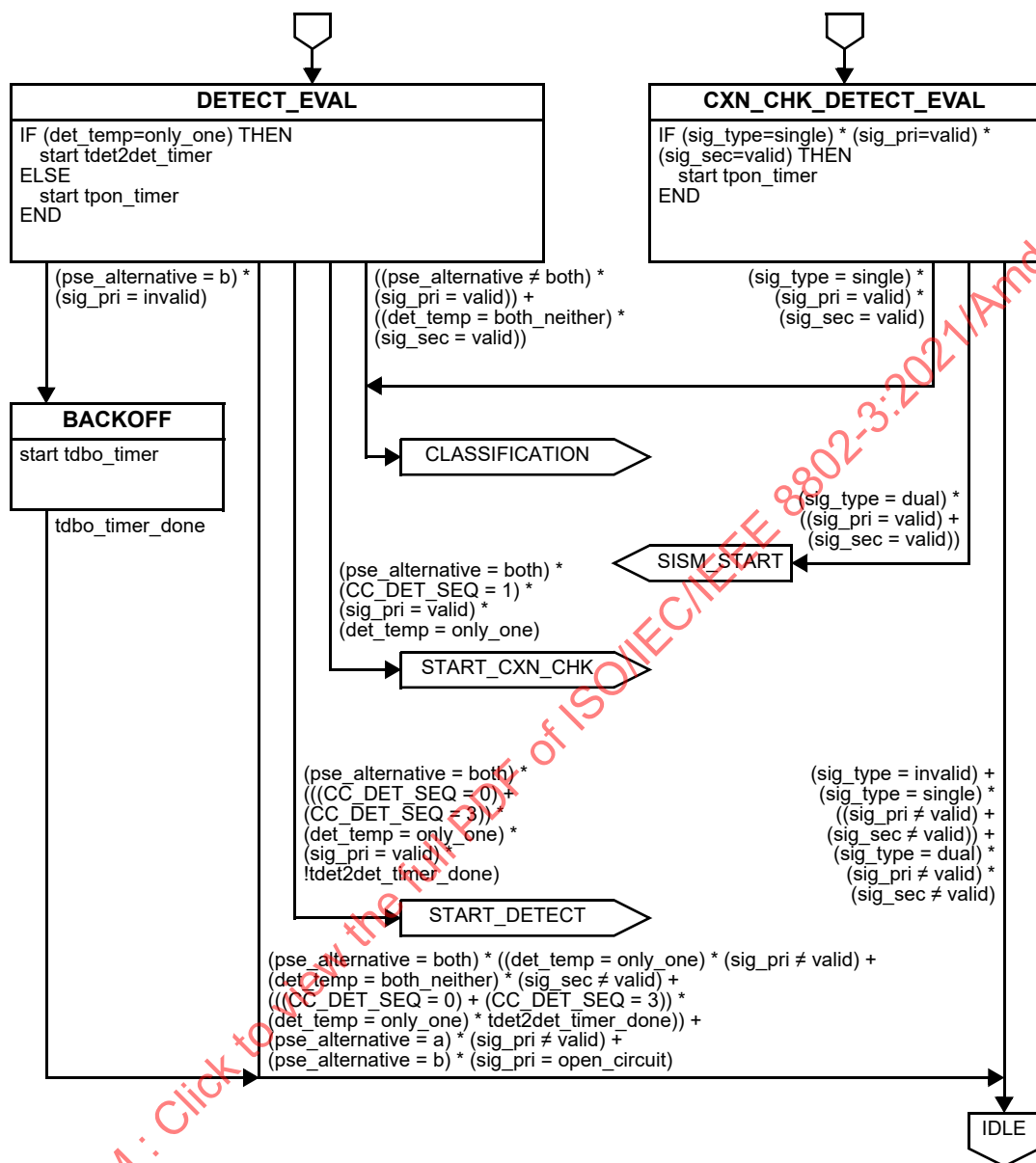


Figure 145–13—Top level PSE state diagram (continued)

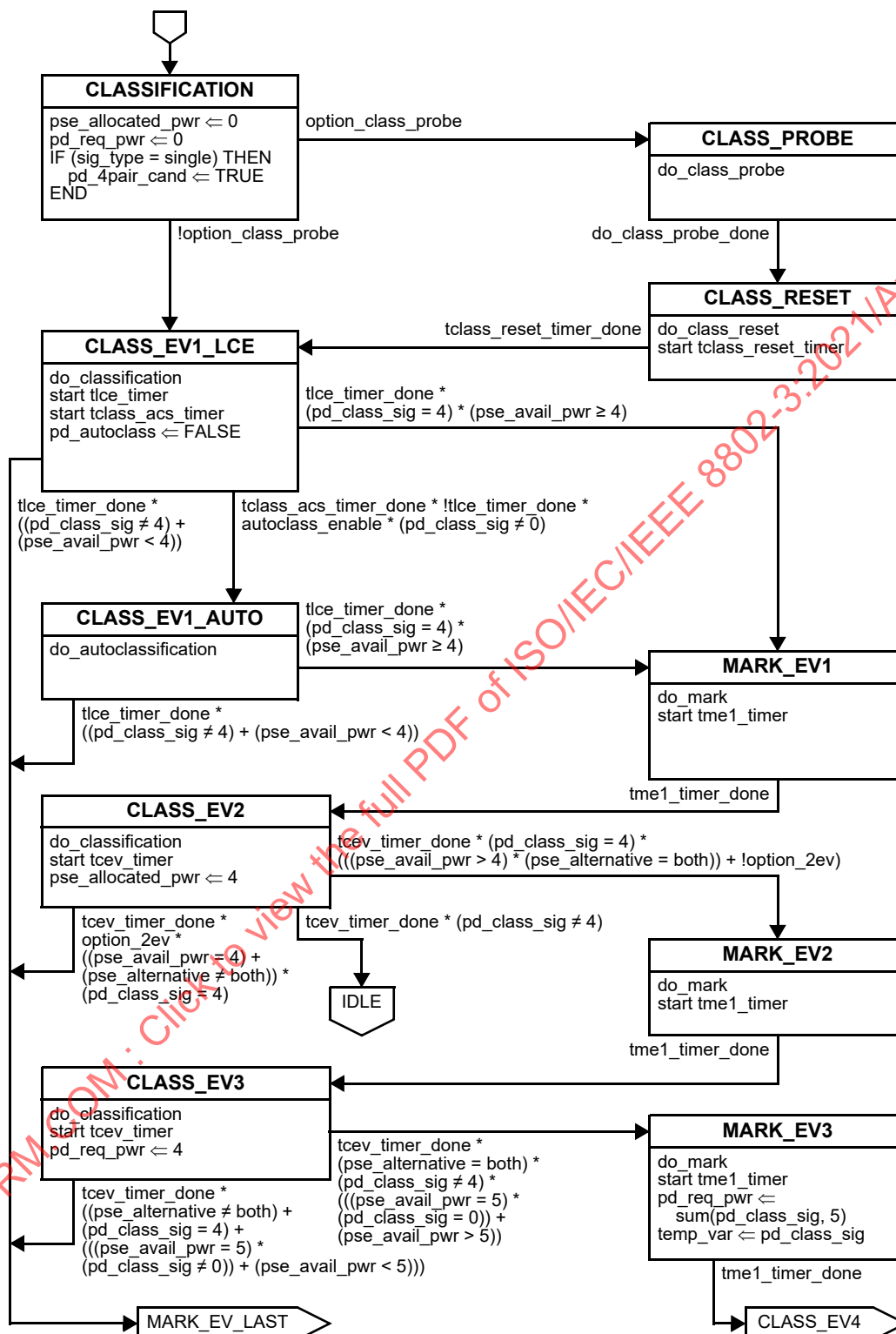


Figure 145-13—Top level PSE state diagram (continued)

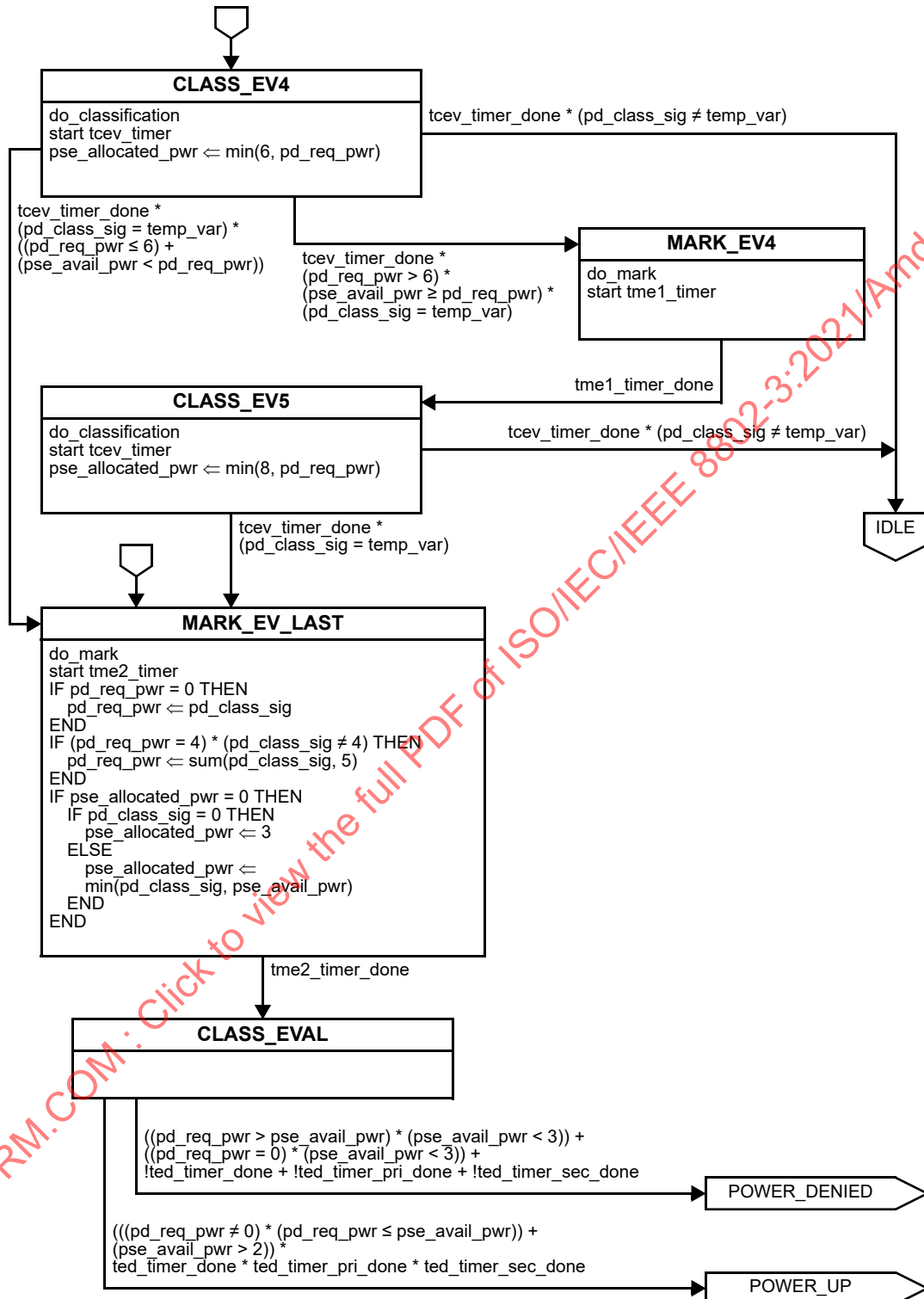


Figure 145–13—Top level PSE state diagram (continued)

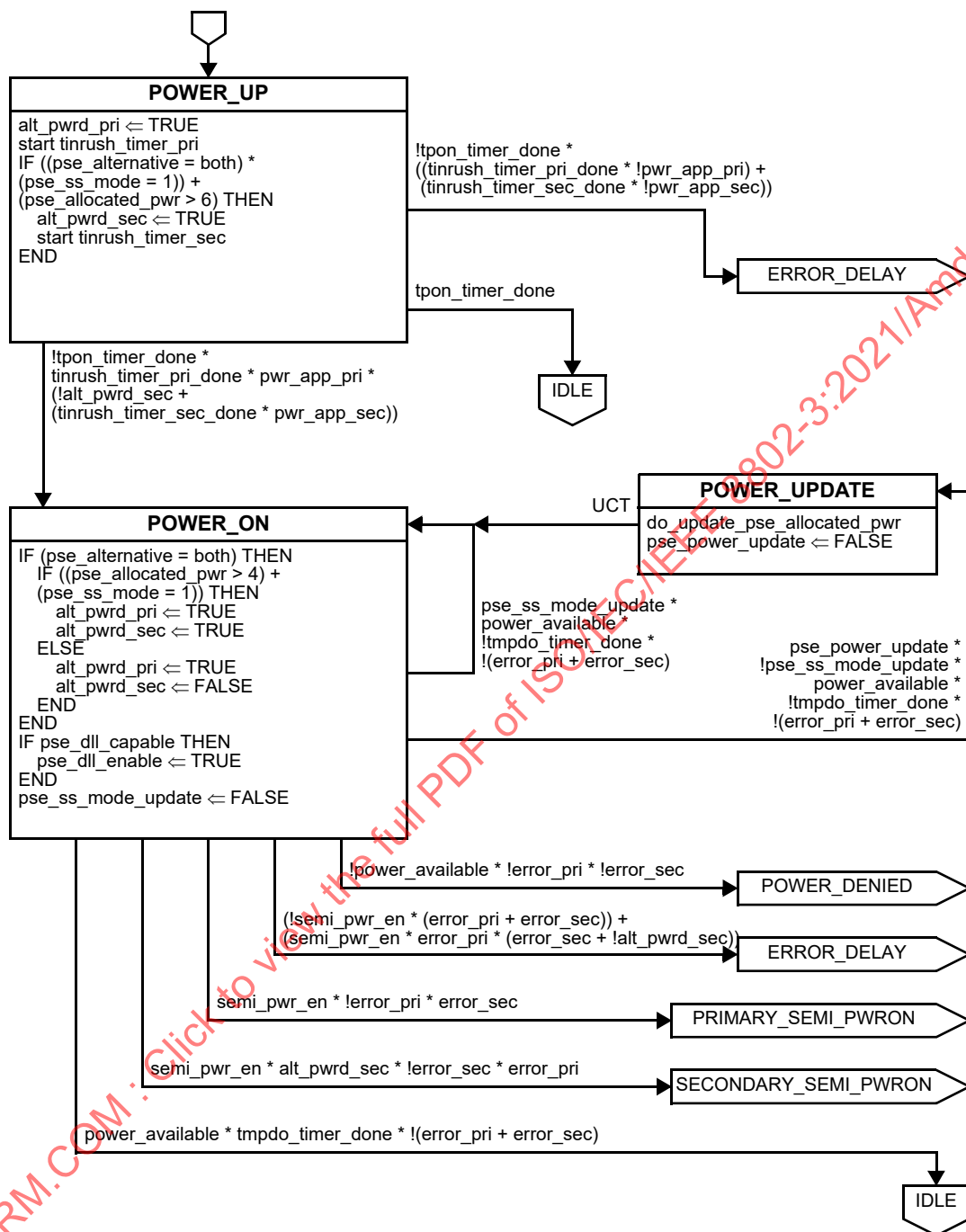


Figure 145–13—Top level PSE state diagram (continued)

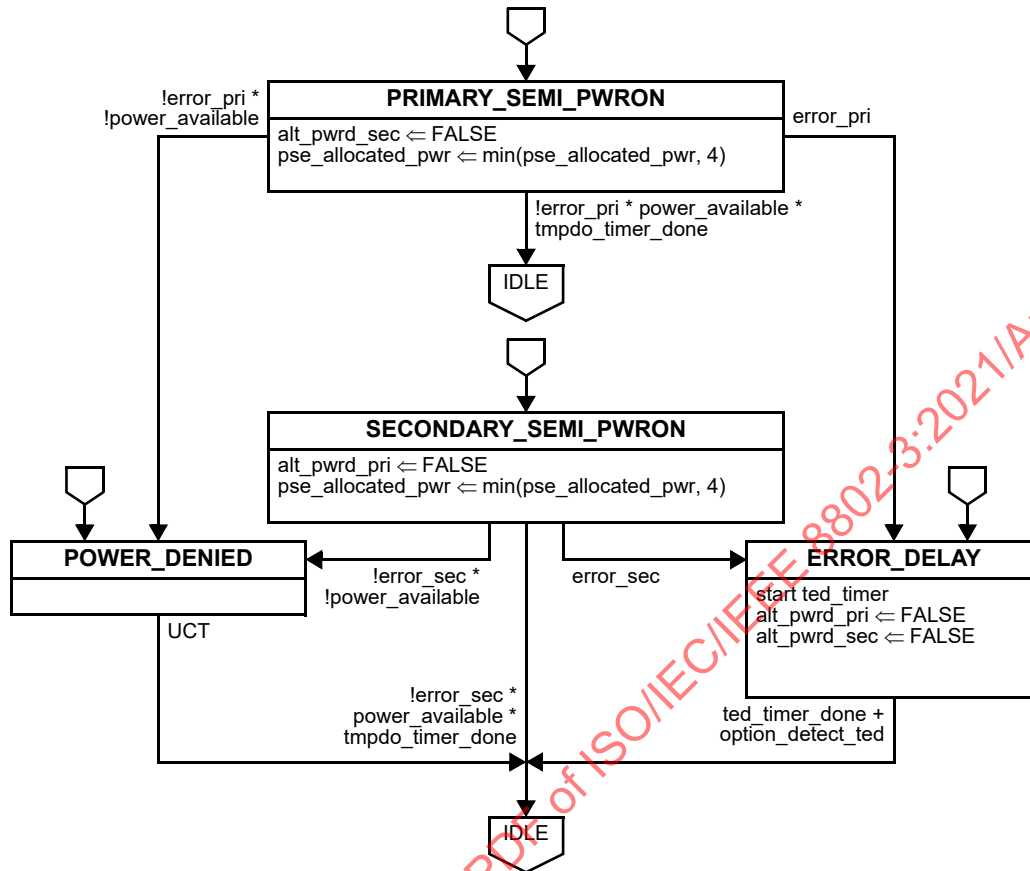


Figure 145-13—Top level PSE state diagram (continued)

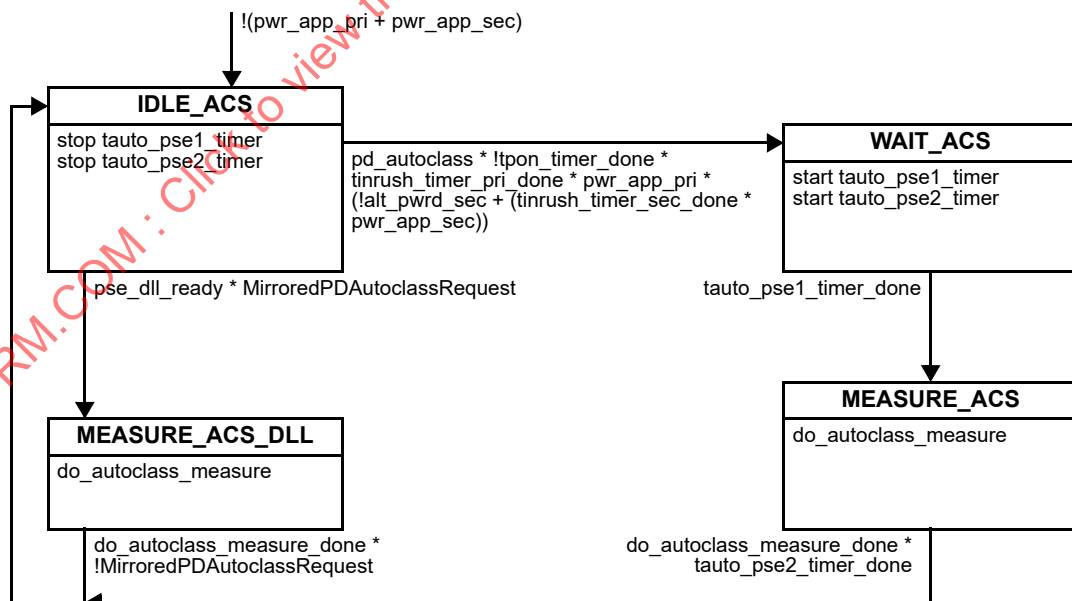


Figure 145-14—PSE Autoclass state diagram

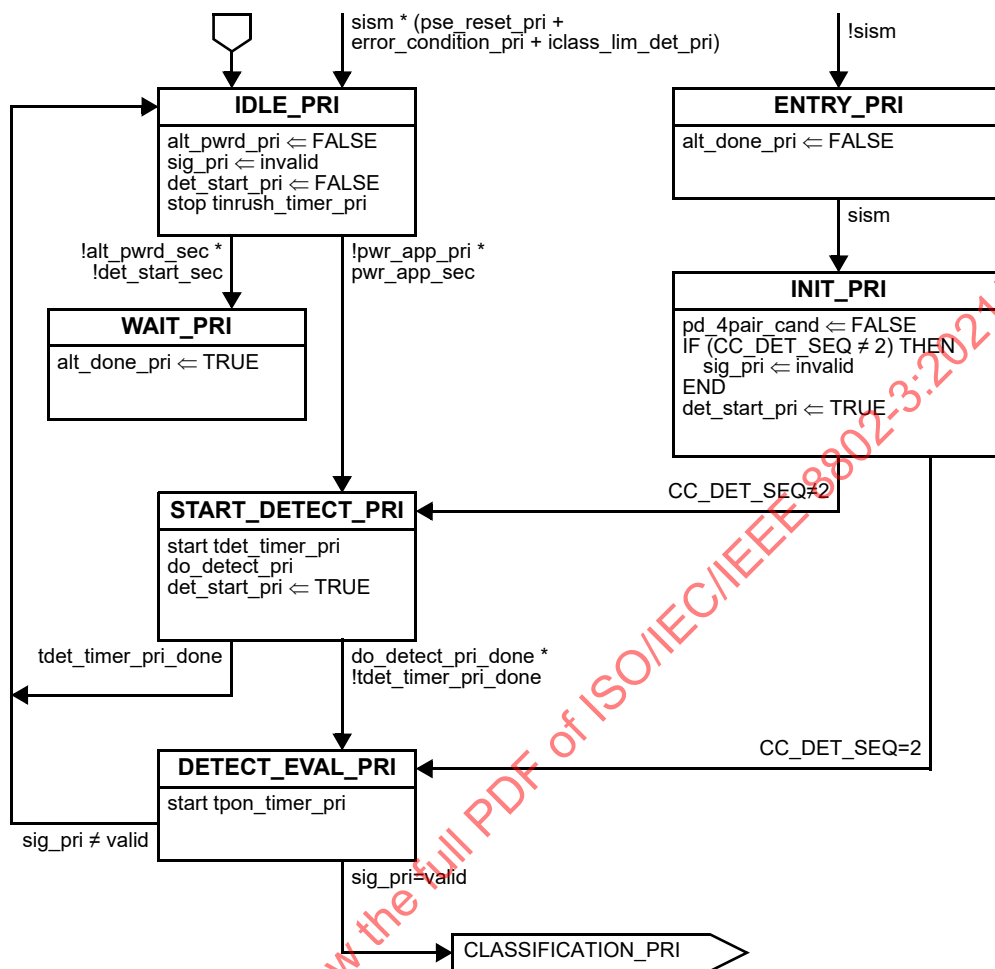


Figure 145-15—Primary Alternative dual-signature semi-independent PSE state diagram

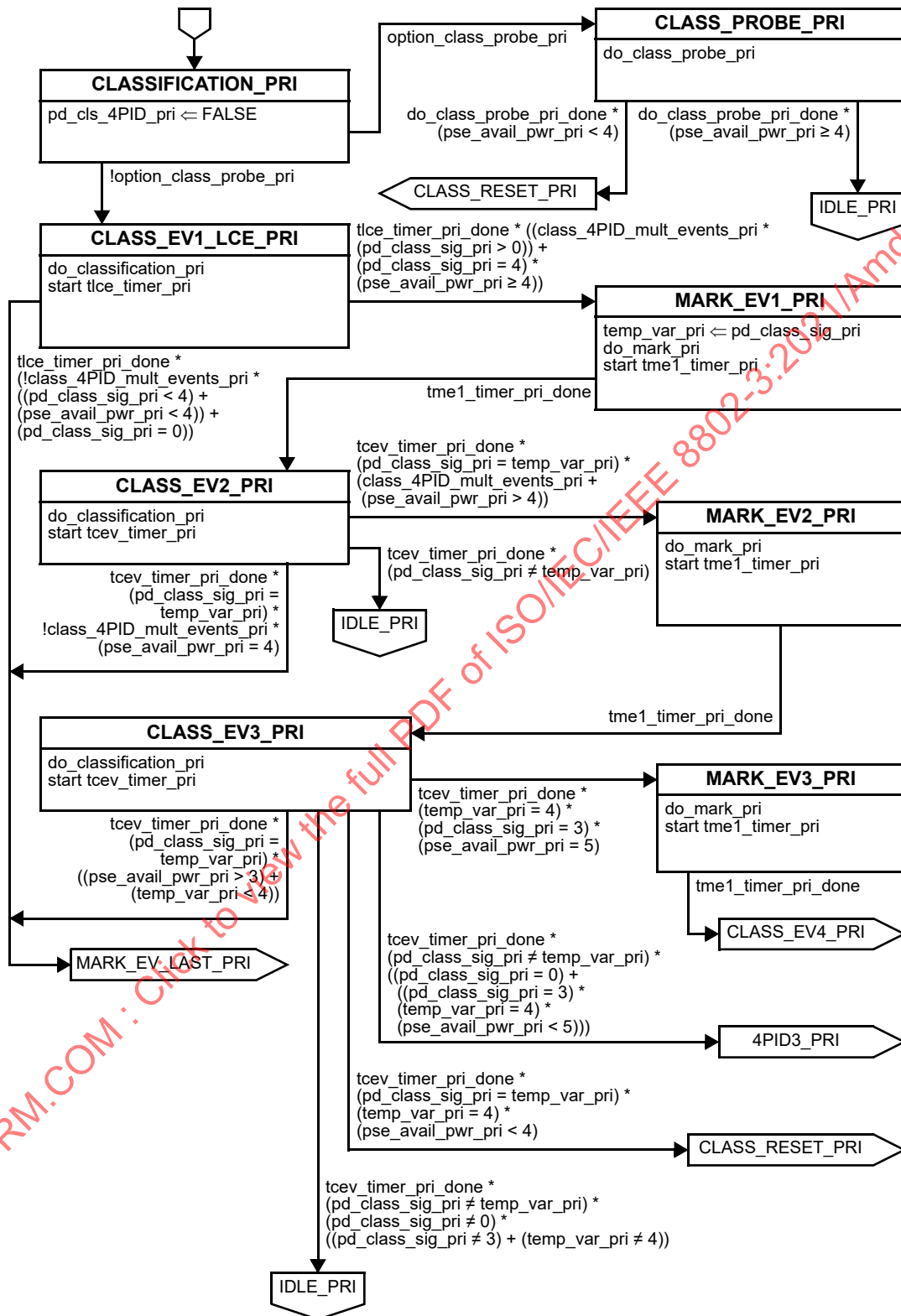


Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram (continued)

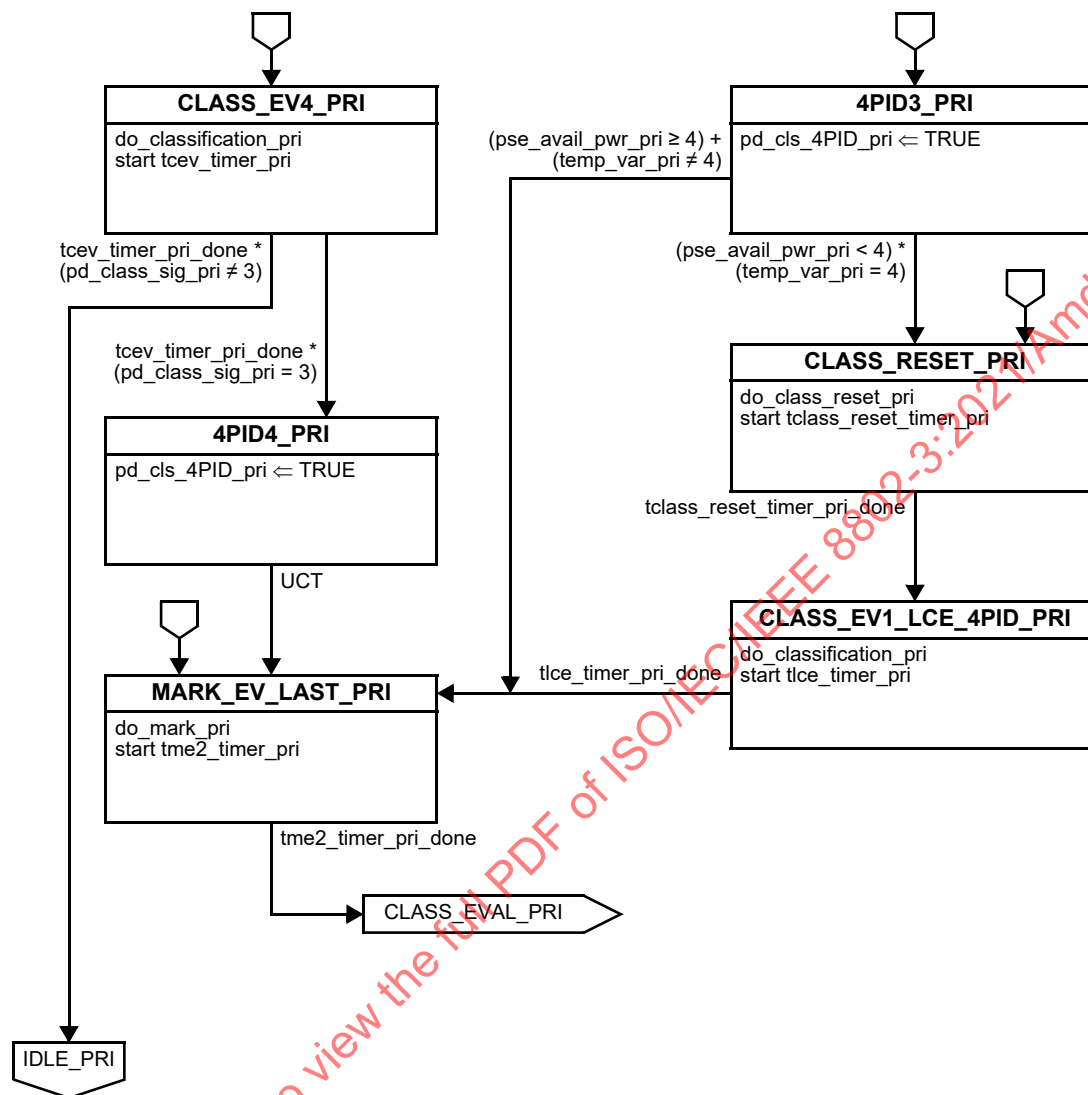


Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram (continued)

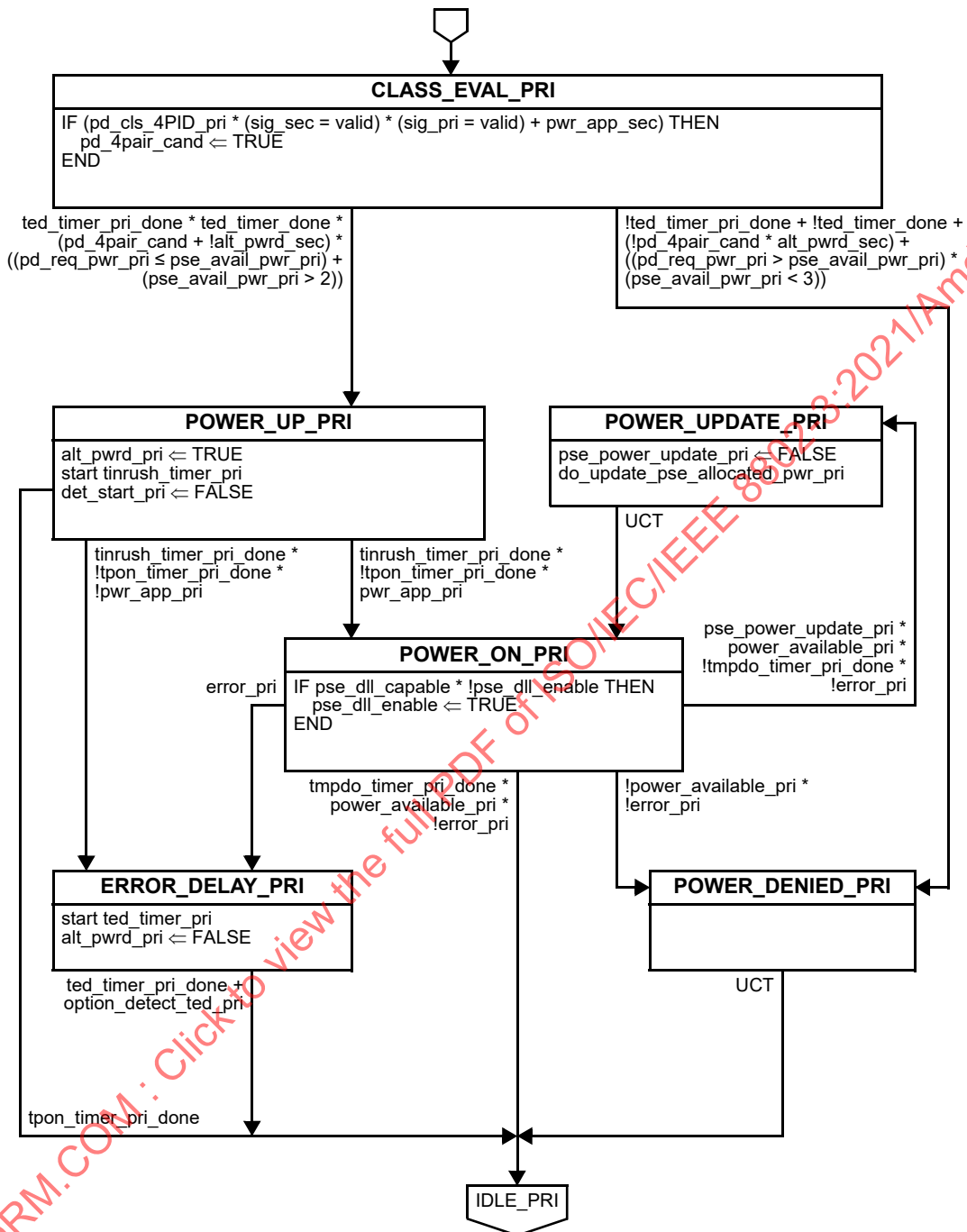


Figure 145–15—Primary Alternative dual-signature semi-independent  
PSE state diagram (continued)

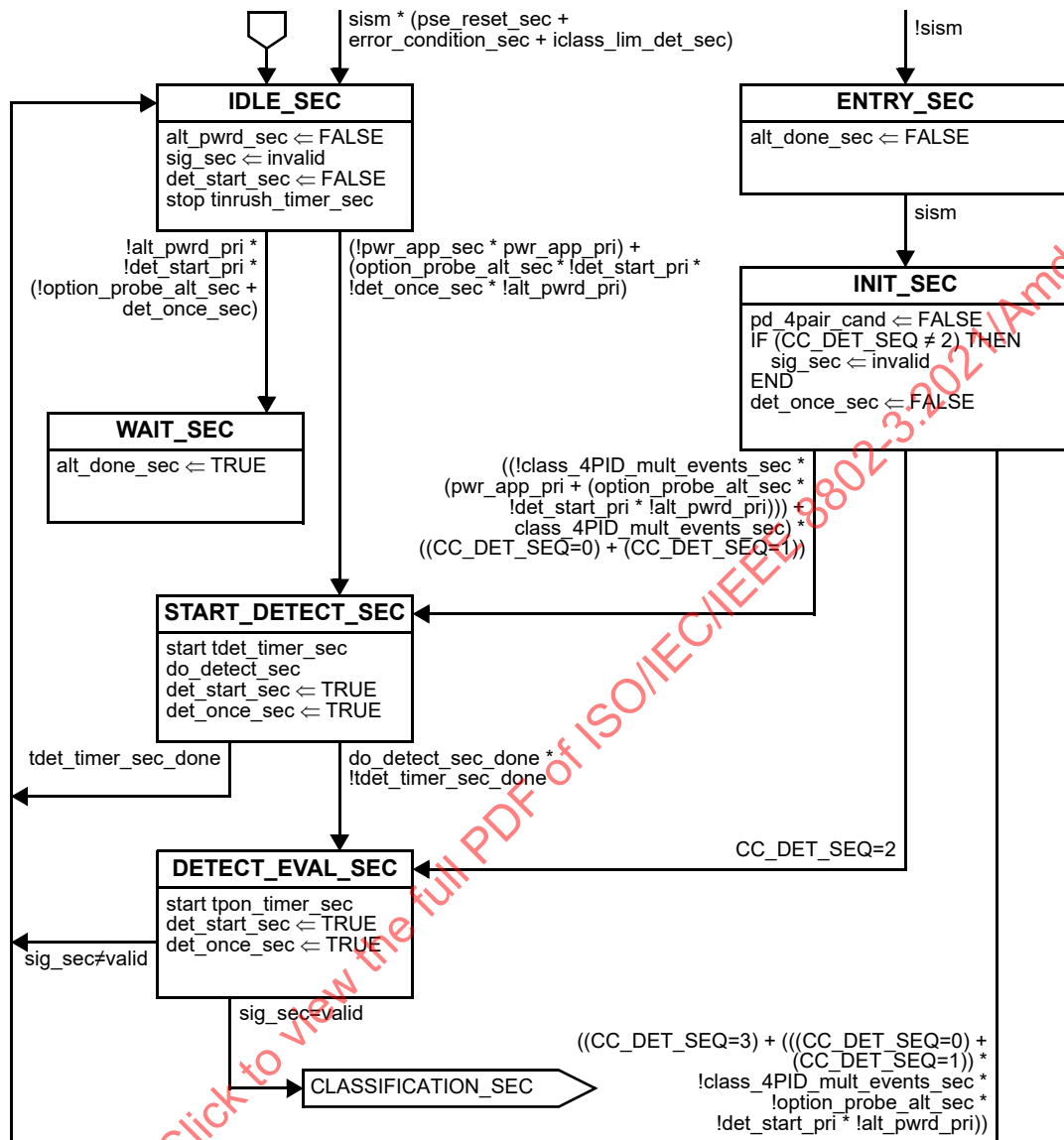


Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram

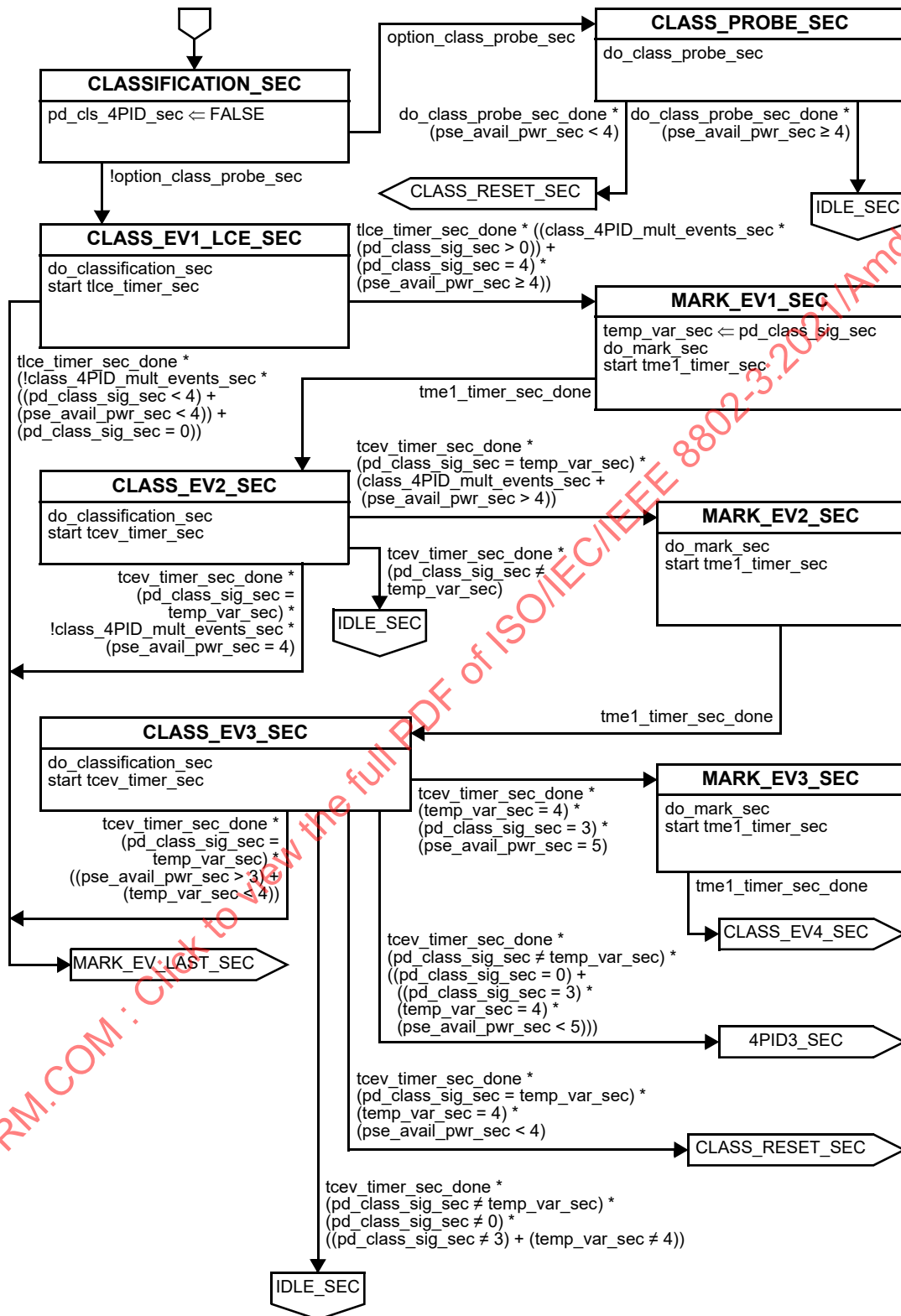


Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram (continued)

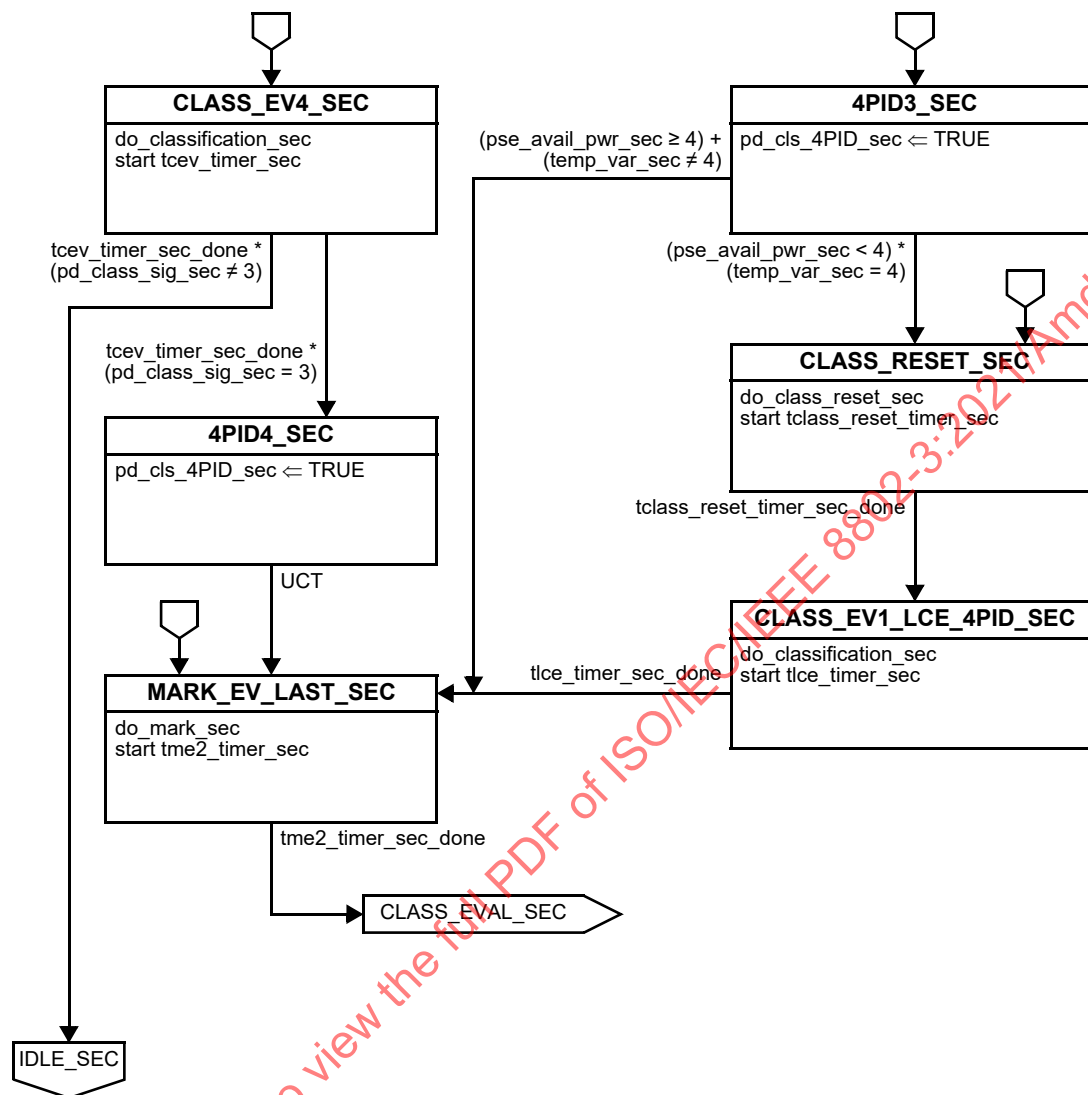


Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram (continued)

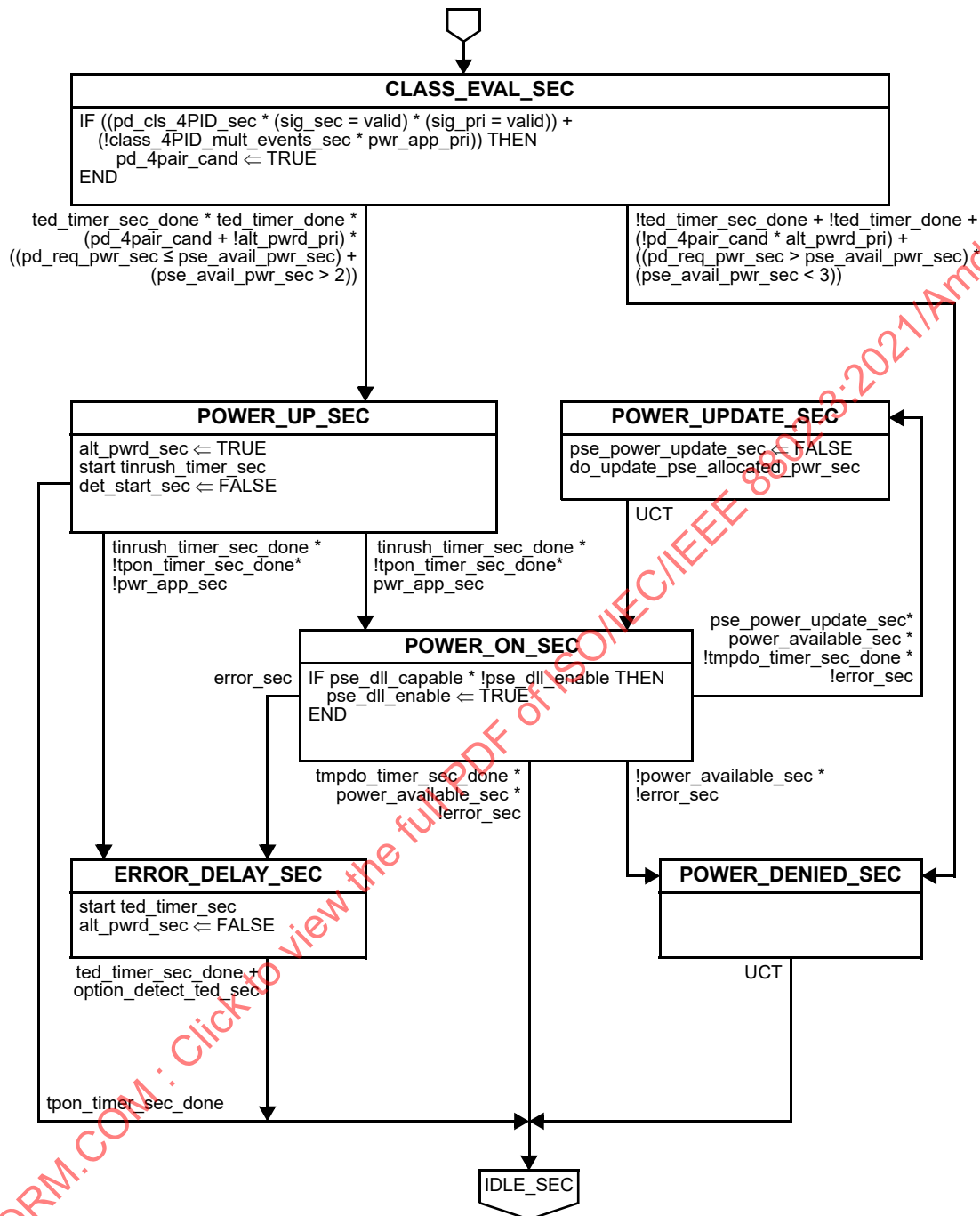


Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram (continued)

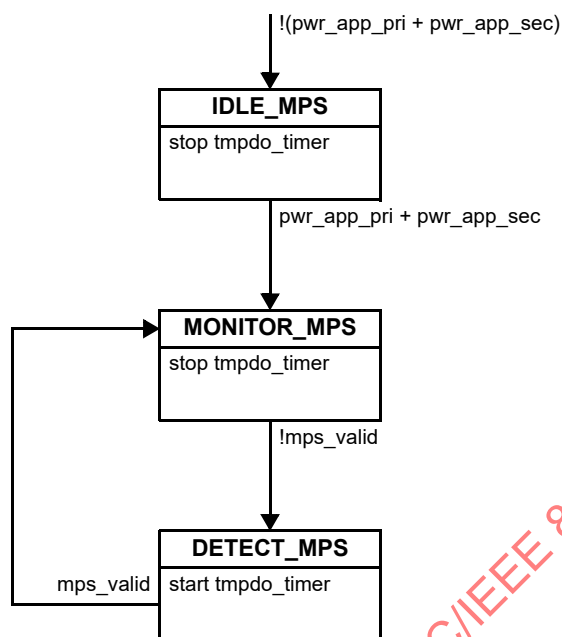


Figure 145-17—PSE MPS monitor state diagram  
for single-signature PDs or 2-pair operation

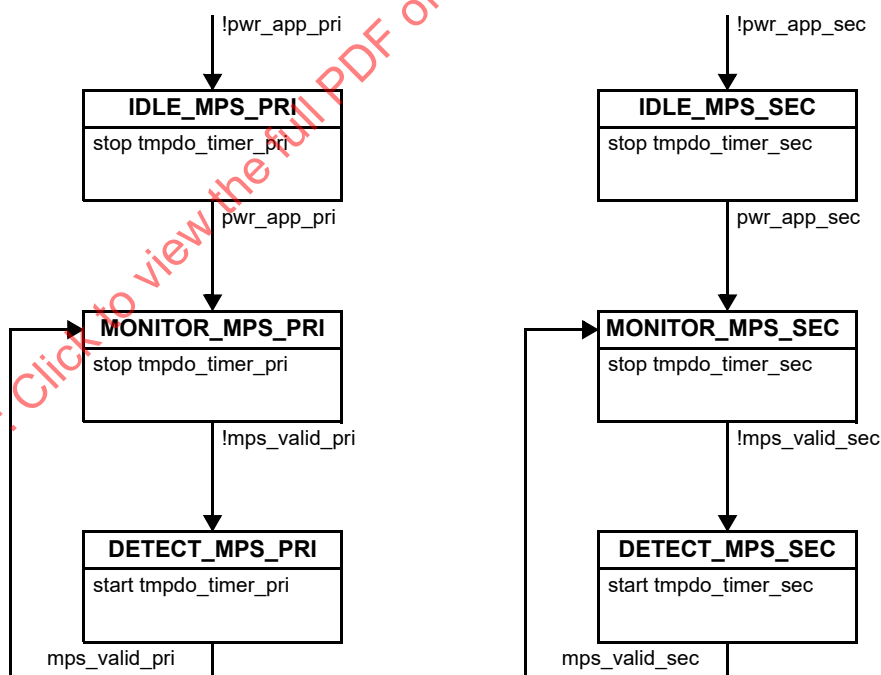


Figure 145-18—PSE MPS monitor state diagram  
for dual-signature PDs

### 145.2.6 PSE detection of PDs

The PSE shall not apply operating voltage to a pairset until the PSE has successfully detected a valid signature over that pairset. When a PSE is already in POWER\_ON, it may transition between 2-pair and 4-pair power without redoing detection as described in 145.2.10.1.

The PSE PI is connected to a PD through a link section. The PSE probes the link section in order to detect a valid PD detection signature. In the following subclauses, the link is not called out to preserve clarity.

The PSE is not required to continuously probe to detect a PD detection signature. The period of time when a PSE is not attempting to detect a PD detection signature is implementation dependent. Also, a PSE may successfully detect a PD or detect and classify a PD, but then opt not to power the detected PD.

A PSE detecting an invalid PD signature on either Alternative may perform detection on the other Alternative, and if valid may perform classification on that pairset.

#### 145.2.6.1 PSE detection validation circuit

The PSE shall detect the PD by probing via the PSE PI. The PSE shall present a non-valid PD detection signature as defined in Table 145–22 when probed in either polarity by another PSE. An illustrative embodiment of a detection circuit is shown in Figure 145–19.

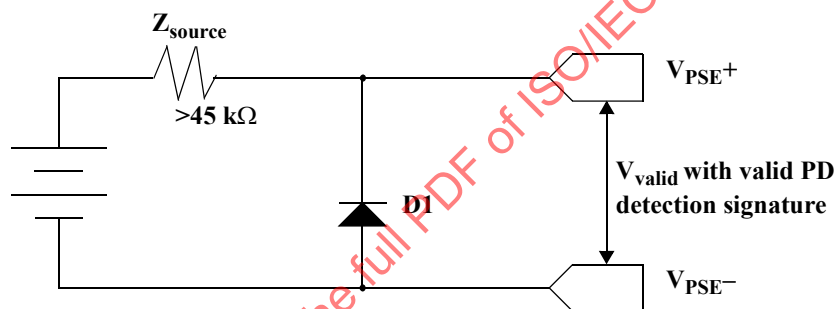


Figure 145–19—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation but restricts the PSE detection circuit to the first quadrant is shown in Figure 145–20.

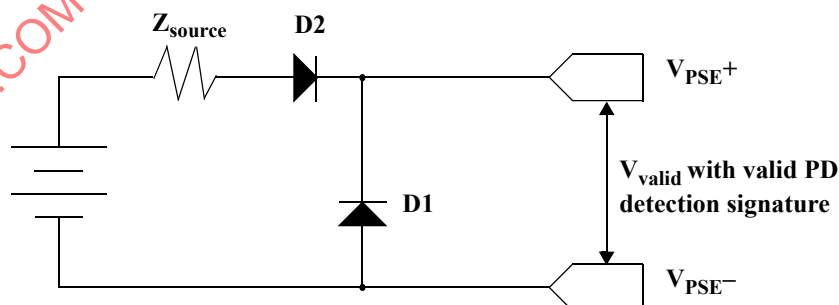


Figure 145–20—Alternative PSE detection source

In Figure 145–19 and Figure 145–20, the diode D1 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 145–7. The PSE shall not be damaged by up to 5 mA backdriven current over the range of  $V_{oc}$  as defined in Table 145–7. Output capacitance shall be as defined in Table 145–7 when  $V_{PSE}$  is in the range of 0 V to  $V_{valid}$  max.

#### 145.2.6.2 Detection probe requirements

The detection voltage at the PSE PI shall be within the  $V_{valid}$  voltage range, as defined in Table 145–7, with a valid PD detection signature connected, as defined in Table 145–21.

**Table 145–7—PSE PI per pairset detection state electrical requirements**

| Item | Parameter                              | Symbol            | Unit       | Min | Max |
|------|----------------------------------------|-------------------|------------|-----|-----|
| 1    | Open circuit voltage                   | $V_{oc}$          | V          | 0   | 30  |
| 2    | Short circuit current                  | $I_{sc}$          | mA         | —   | 5   |
| 3    | Valid test voltage                     | $V_{valid}$       | V          | 2.8 | 10  |
| 4    | Voltage difference between test points | $\Delta V_{test}$ | V          | 1   | —   |
| 5    | Slew rate                              | $V_{slew}$        | V/ $\mu$ s | —   | 0.1 |
| 6    | Pairset output capacitance             | $C_{out}$         | nF         | —   | 520 |

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with  $V_{PSE}$  values that create at least a  $\Delta V_{test}$  difference as defined in Table 145–7. An effective resistance is calculated from two or more measurements made during the detection process.

The resistance is calculated with Equation (145–1):

$$R = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \quad (145-1)$$

where

$V_1$  and  $V_2$  are the first and second voltage measurements made on the pairset, respectively  
 $I_1$  and  $I_2$  are the first and second current measurements made on the negative pair of the pairset, respectively  
 $R$  is the effective resistance

Attached PI capacitance may be determined using these measurements and the port RC time-constant charging characteristics.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after  $V_{PSE}$  has settled to within 1 % of its steady state condition with a valid PD detection signature connected (as defined in Table 145–21).

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than  $V_{slew}$  as defined in Table 145–7.

**145.2.6.3 Detection criteria**

A PSE shall accept as a valid PD detection signature a pairset with all of the characteristics specified in Table 145–8.

**Table 145–8—Valid PD detection signature electrical characteristics, as measured at the PSE PI**

| Item | Parameter                          | Symbol            | Unit             | Min | Max  | Additional information |
|------|------------------------------------|-------------------|------------------|-----|------|------------------------|
| 1    | Accept signature resistance        | $R_{\text{good}}$ | $\text{k}\Omega$ | 19  | 26.5 | —                      |
| 2    | Accept signature capacitance       | $C_{\text{good}}$ | $\mu\text{F}$    | —   | 0.15 | —                      |
| 3    | Signature offset voltage tolerance | $V_{\text{os}}$   | V                | 0   | 2    | —                      |
| 4    | Signature offset current tolerance | $I_{\text{os}}$   | $\mu\text{A}$    | 0   | 12   | —                      |

**145.2.6.4 Rejection criteria**

The PSE shall reject as an invalid detection signature, a pairset which exhibits any of the following characteristics:

- a) Resistance less than or equal to  $R_{\text{bad min}}$ , or
- b) Resistance greater than or equal to  $R_{\text{bad max}}$ , or
- c) Capacitance greater than or equal to  $C_{\text{bad min}}$ .

$R_{\text{bad min}}$ ,  $R_{\text{bad max}}$ , and  $C_{\text{bad min}}$  are defined in Table 145–9.

NOTE—Detection and rejection criteria for Clause 145 remain unchanged from Clause 33, for the purpose of maintaining interoperability with Clause 33 devices (see also 145.2.6.3).

A PSE may accept or reject a signature resistance in the band between  $R_{\text{good min}}$  and  $R_{\text{bad min}}$ , and in the band between  $R_{\text{good max}}$  and  $R_{\text{bad max}}$ . A PSE may accept or reject a parallel signature capacitance in the band between  $C_{\text{good max}}$  and  $C_{\text{bad min}}$ .

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offsets are exceeded, the detection behavior of the PSE is undefined.

**Table 145–9—Invalid PD detection signature electrical characteristics, as measured at the PSE PI**

| Item | Parameter                    | Symbol            | Unit             | Min | Max | Additional information |
|------|------------------------------|-------------------|------------------|-----|-----|------------------------|
| 1    | Reject signature resistance  | $R_{\text{bad}}$  | $\text{k}\Omega$ | 15  | 33  | —                      |
| 2    | Reject signature capacitance | $C_{\text{bad}}$  | $\mu\text{F}$    | 10  | —   | —                      |
| 3    | Open circuit resistance      | $R_{\text{open}}$ | $\text{M}\Omega$ | 0.5 | —   | —                      |

**145.2.6.5 Open circuit criteria**

If a PSE that is performing detection using Alternative B (see 145.2.4) determines that the impedance at the PI is greater than  $R_{\text{open}}$  as defined in Table 145–9, it may optionally consider the link to be open circuit and omit the  $\text{tdbo\_timer}$  interval.

**145.2.7 Connection check**

PSEs that will source power on both pairsets shall complete a connection check prior to the classification of a PD as defined in 145.2.8 to determine if the PSE is connected to a single-signature PD configuration, a dual-signature PD configuration, or neither.

NOTE—When a link segment is connected to an MDI, not all contacts are made simultaneously. A link segment connection or removal may occur at any time during connection check. PSE implementations should take these considerations into account.

During connection check the PSE shall meet the specifications for open circuit voltage,  $V_{\text{oc}}$ , and short circuit current,  $I_{\text{sc}}$ , in Table 145–7. The connection check voltage at the PSE PI shall be within the  $V_{\text{valid}}$  voltage range, as defined in Table 145–7, when a single-signature PD or a dual-signature PD is connected.

The specification of  $T_{\text{cc2det}}$ , defined in Table 145–10, applies to the time between the end of connection check and the beginning of detection on at least one pairset. If the connection check takes place after the beginning of detection, this specification does not apply.

The specification of  $T_{\text{det2det}}$ , defined in Table 145–10, applies to the time between the end of detection on the first pairset to the beginning of detection on the other pairset when the second detection occurs before power up on the first pairset.

**Table 145–10—Connection check timing requirements**

| Item | Parameter                          | Symbol               | Unit | Min | Max | Additional Information                                                         |
|------|------------------------------------|----------------------|------|-----|-----|--------------------------------------------------------------------------------|
| 1    | Connection check to detection time | $T_{\text{cc2det}}$  | s    | —   | 0.4 | Applies only when connection check is performed before the start of detection. |
| 2    | Detection to detection time        | $T_{\text{det2det}}$ | s    | —   | 0.4 | —                                                                              |

The connection check is rerun before applying power if power up fails to meet the timing requirements in both Table 145–10 and 145.2.10.14 or if power is absent on both pairsets simultaneously.

If the voltage on either pairset rises above  $V_{\text{valid}}$  max, as defined in Table 145–7, during connection check, the PSE shall reset the PD by bringing the voltage at the PI below  $V_{\text{off}}$  max, as defined in Table 145–16, for at least  $T_{\text{Reset}}$ , as defined in Table 145–14, before performing classification.

**145.2.8 PSE classification of PDs and mutual identification**

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a PSE to differentiate between Type 1, Type 2, Type 3, and Type 4 PDs. Additionally, mutual identification allows PDs to differentiate between Type 1, Type 2, Type 3, and Type 4 PSEs.

There are two forms of classification: Multiple-Event Physical Layer classification and Data Link Layer (DLL) classification.

Physical Layer classification occurs after a valid detection and before a PSE supplies power to a PD, when the PSE asserts a voltage in the range of  $V_{Class}$  as defined in Table 145–14 onto one or both pairsets. This is called a class event. The PD responds to each class event with a current representing one of a limited number of class signatures. The class signatures generated by the PD indicate the PD requested Class. See Table 145–26 and Table 145–27 for a mapping of class signature to the PD requested Class.

NOTE—Requested Class 0 is not defined for Type 3 PDs. A Type 1 PD that does not implement Physical Layer classification requests Class 0, with a power level equivalent to Class 3. Such PDs are assigned to Class 3 by Type 3 and Type 4 PSEs.

The assigned Class is the result of the PD requested Class and the number of class events produced by the PSE as shown in Table 145–11. See 145.3.6 for PD classification behavior.

When a single-signature PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3, 4, or 6, whichever is the highest that it can support. When a dual-signature PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support. The minimum output power a PSE supports depends on the assigned Class.

The minimum output power a PSE supports when powering a single-signature PD, or supplying power in 2-pair mode, is defined by Equation (145–2). PSE implementations may use  $V_{PSE} = V_{Port\_PSE-2P\ min}$  and  $R_{Chan-2P} = R_{Ch}$  when the assigned Class is 1 through 4, or  $R_{Chan} = R_{Ch}/2$  when the assigned Class is 5 through 8 to arrive at over-margined values as shown in Table 145–11.  $P_{Class}$  may subsequently be adjusted using Data Link Layer classification.

$$P_{Class} = \left\{ \begin{array}{ll} V_{PSE} \times \left( \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan-2P} \times P_{Class\_PD}}}{2 \times R_{Chan-2P}} \right) & \text{for assigned Class 1 through 4} \\ V_{PSE} \times \left( \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) & \text{for assigned Class 5 through 8} \end{array} \right\}_w \quad (145-2)$$

where

$V_{PSE}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3  
 $R_{Chan}$  is the link section DC loop resistance  
 $R_{Chan-2P}$  is the pairset DC loop resistance  
 $P_{Class\_PD}$  is the maximum power at the PD PI per the PDs assigned Class, as defined in Table 145–29

When connected to a dual-signature PD, a PSE operating over 4 pairs treats the requested power over each pairset independently. The minimum output power a PSE supports on a pairset when powering a dual-signature PD is defined by Equation (145–3). PSE implementations may use  $V_{PSE} = V_{Port\_PSE-2P\ min}$  and  $R_{Chan-2P} = R_{Ch}$  to arrive at over-margined values as shown in Table 145–11.  $P_{Class-2P}$  may subsequently be adjusted using Data Link Layer classification or Autoclass.

$$P_{Class-2P} = \left\{ V_{PSE} \times \left( \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan-2P} \times P_{Class\_PD-2P}}}{2 \times R_{Chan-2P}} \right) \right\}_W \quad (145-3)$$

where

$V_{PSE}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3  
 $R_{Chan-2P}$  is the pairset DC loop resistance  
 $P_{Class\_PD-2P}$  is the maximum power at the PD PI for a pairset per the PDs assigned Class, as defined in Table 145–29

$P_{Class}$  and  $P_{Class-2P}$  are valid over the range of  $V_{Port\_PSE-2P}$  defined in Table 145–16.

If the PD connected to the PSE performs Autoclass (see 145.2.8.2 and 145.3.6.2), the PSE may set the minimum supported output power based on  $P_{Autoclass}$ , the power drawn during the Autoclass measurement window.  $P_{Autoclass}$  shall be increased by at least  $P_{ac\_margin}$ , as defined in Table 145–15, in order to account for potential increase in link section resistance due to temperature increase, up to the value defined in Table 145–11 of the Class assigned to the PD, and with a minimum power allocation of Class 1.

When the PSE assigns Class 5 through 8 prior to a fault and then transitions to PRIMARY\_SEMI\_PWRON or SECONDARY\_SEMI\_PWRON, it shall revert the allocation of power to Class 4 and assert local\_system\_change to update PSEAllocatedPowerValue.

A PSE that measured  $P_{Autoclass}$  while providing power over 4 pairs, shall increase the power allocation by at least  $P_{ac\_extra}$ , as defined in Equation (145–4), when it provides power over 2 pairs.

$$P_{ac\_extra} = \left\{ \left( \frac{P_{Autoclass}}{V_{Port\_PSE-2P\ min}} \right)^2 \times \frac{R_{Ch}}{2} \right\}_W \quad (145-4)$$

where

$P_{Autoclass}$  is the amount of power measured by the PSE during the Autoclass measurement  
 $V_{Port\_PSE-2P\ min}$  is the minimum PSE operating voltage  
 $R_{Ch}$  is the maximum pairset DC loop resistance, as defined in Table 145–1

**Table 145–11—Physical Layer power classifications**

| PD Requested Class                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Number of PSE class events | Assigned Class | $P_{Class}$ | $P_{Class-2P}$ |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------------|-------------|----------------|
| PSEs connected to a single-signature PD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                            |                |             |                |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1                          | 1              | 4 W         | —              |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1                          | 2              | 6.7 W       | —              |
| 0, 3 to 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1                          | 3              | 14 W        | —              |
| 4 to 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2 or 3                     | 4              | 30 W        | —              |
| 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 4                          | 5              | 45 W        | —              |
| 6 to 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 4                          | 6              | 60 W        | —              |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 5                          | 7              | 75 W        | —              |
| 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 5                          | 8              | 90 W        | —              |
| PSEs connected to a dual-signature PD (classification per pairset)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                            |                |             |                |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1, 2, or 3                 | 1              | —           | 4 W            |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1, 2, or 3                 | 2              | —           | 6.7 W          |
| 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1, 2, or 3                 | 3              | —           | 14 W           |
| 4 or 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1                          | 3              | —           | 14 W           |
| 4 or 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2 or 3                     | 4              | —           | 30 W           |
| 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 4                          | 5              | —           | 45 W           |
| <p>NOTE 1—<math>P_{Class}</math> in Table 145–11 is the minimum required power at the PSE PI calculated using minimum <math>V_{Port\ PSE-2P}</math> and maximum <math>R_{Chan}</math>. Use Equation (145–2) for other values of <math>V_{Port\ PSE-2P}</math> and <math>R_{Chan}</math>. For PD requested power levels, see Table 145–26.</p> <p>NOTE 2—<math>P_{Class-2P}</math> in Table 145–11 is the minimum required power for a pairset calculated using minimum <math>V_{Port\ PSE-2P}</math> and maximum <math>R_{Chan-2P}</math>. Use Equation (145–3) for other values of <math>V_{Port\ PSE-2P}</math> and <math>R_{Chan-2P}</math>. For PD requested power levels, see Table 145–27.</p> <p>NOTE 3—The number of PSE class events refers to the number of class events since the most recent PD reset.</p> <p>NOTE 4—The values of <math>P_{Class}</math> and <math>P_{Class-2P}</math> are calculated for the lowest Type PSE that is able to support that power level.</p> |                            |                |             |                |

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 145.5) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation. Data Link Layer classification takes precedence over Physical Layer classification.

After a successful DLL classification, the assigned Class changes depending on the value of the PSEAllocatedPowerValue or PSEAllocatedPowerValue\_alt(X) variable, as defined in Table 145–12. The PSEAllocatedPowerValue or PSEAllocatedPowerValue\_alt(X) values correspond with the maximum power a PD may draw,  $P_{Class\_PD}$  or  $P_{Class\_PD-2P}$  respectively; see Table 145–29 and 145.5.3.2.2.

Subsequent to successful detection, PSEs shall perform Multiple-Event Physical Layer classification and may perform Data Link Layer classification. PSEs that will source power over 4-pair to a dual-signature PD shall perform Physical Layer classification on each pairset.

**Table 145–12—Relation of assigned Class and DLL**

| Single-signature       |                | Dual-signature                |                                 |
|------------------------|----------------|-------------------------------|---------------------------------|
| PSEAllocatedPowerValue | Assigned Class | PSEAllocatedPowerValue_alt(X) | Assigned Class on Alternative X |
| 1 to 39                | 1              | 1 to 39                       | 1                               |
| 40 to 65               | 2              | 40 to 65                      | 2                               |
| 66 to 130              | 3              | 66 to 130                     | 3                               |
| 131 to 255             | 4              | 131 to 255                    | 4                               |
| 256 to 400             | 5              | 256 to 499                    | 5                               |
| 401 to 510             | 6              |                               |                                 |
| 511 to 620             | 7              |                               |                                 |
| 621 to 999             | 8              |                               |                                 |

A PSE shall be capable of assigning the highest Class it can support by means of Multiple-Event Physical Layer classification.

A PSE shall return to IDLE if it fails to complete classification after successfully completing detection of a single-signature PD. A PSE shall return to IDLE\_PRI or IDLE\_SEC, whichever corresponds to the appropriate Alternative, if it successfully completes detection on a pairset of a dual-signature PD but fails to complete classification on that pairset.

#### 145.2.8.1 PSE Multiple-Event Physical Layer classification

Classification consists of a series of classification and mark events as defined in the state diagram in Figure 145–13, Figure 145–15, and Figure 145–16.

Voltages  $V_{Class}$ ,  $V_{Mark}$ , and  $V_{Reset}$  and currents  $I_{Class\_LIM}$  and  $I_{Mark\_LIM}$  are specified in Table 145–14. PD class signature measurements of  $I_{Class}$  are specified in Table 145–13. Classification times,  $T_{LCE}$ ,  $T_{CEV}$ ,  $T_{ME1}$ ,  $T_{ME2}$ ,  $T_{Class}$ , and  $T_{Reset}$  are specified in Table 145–14. Autoclass timing,  $T_{Class\_ACS}$  is specified in Table 145–14. See Annex 145B for more details and timing diagrams.

Type 3 PSEs:

- Shall provide a maximum of four class events and four mark events for single-signature PDs.
- Shall provide a maximum of three class events and three mark events on each pairset for dual-signature PDs.

Type 4 PSEs:

- Shall provide a maximum of five class events and five mark events for single-signature PDs.
- Shall provide a maximum of four class events and four mark events on each pairset for dual-signature PDs.

**Table 145–13—Class signatures evaluated at the PSE PI**

| Measured $I_{Class}$ | Class signature                                     |
|----------------------|-----------------------------------------------------|
| 0 mA to 5 mA         | Class signature 0                                   |
| > 5 mA and < 8 mA    | Either class signature 0 or 1                       |
| 8 mA to 13 mA        | Class signature 1                                   |
| > 13 mA and < 16 mA  | Either class signature 1 or 2                       |
| 16 mA to 21 mA       | Class signature 2                                   |
| > 21 mA and < 25 mA  | Either class signature 2 or 3                       |
| 25 mA to 31 mA       | Class signature 3                                   |
| > 31 mA and < 35 mA  | Either class signature 3 or 4                       |
| 35 mA to 45 mA       | Class signature 4                                   |
| > 45 mA and < 51 mA  | Either class signature 4 or invalid class signature |

**Table 145–14—PSE Physical Layer classification electrical requirements**

| Item | Parameter                                  | Symbol           | Units | Min         | Max  |
|------|--------------------------------------------|------------------|-------|-------------|------|
| 1    | Class event voltage                        | $V_{Class}$      | V     | 15.5        | 20.5 |
| 2    | Mark event voltage                         | $V_{Mark}$       | V     | 7           | 10   |
| 3    | Classification reset voltage               | $V_{Reset}$      | V     | 0           | 2.8  |
| 4    | Class event current limitation             | $I_{Class\_LIM}$ | A     | 0.051       | 0.1  |
| 5    | Mark event current limitation              | $I_{Mark\_LIM}$  | A     | 0.005       | 0.1  |
| 6    | Classification reset timing                | $T_{Reset}$      | ms    | 15          | —    |
| 7    | Class event $I_{Class}$ measurement timing | $T_{Class}$      | ms    | 6           | —    |
| 8    | LCE $I_{Class}$ measurement timing         | $T_{Class\_LCE}$ | ms    | $T_{Class}$ | 75   |
| 9    | Autoclass $I_{Class}$ measurement timing   | $T_{Class\_ACS}$ | ms    | 88          | —    |
| 10   | Long first class event timing              | $T_{LCE}$        | ms    | 88          | 105  |
| 11   | Second through fifth class event timing    | $T_{CEV}$        | ms    | 6           | 20   |
| 12   | Mark event timing (except last mark event) | $T_{ME1}$        | ms    | 6           | 12   |
| 13   | Last mark event timing <sup>a</sup>        | $T_{ME2}$        | ms    | 6           | —    |

<sup>a</sup> The maximum value of  $T_{ME2}$  is limited by  $T_{pon}$ , as defined in 145.2.10.14

PSEs connected to a single-signature PD shall issue no more class events than the Class they are able to support and no more than

- One class event when the PD requests Class 0 through 3
- Three class events when the PD requests Class 4
- Four class events when the PD requests Class 5 or 6
- Five class events when the PD requests Class 7 or 8

between the most recent time  $V_{PSE}$  was at  $V_{Reset}$  for at least  $T_{Reset}$  and a transition to any of the power up states.

PSEs connected to a dual-signature PD shall issue, for a given pairset, no more class events than the Class they are able to support and no more than

- Three class events when the PD requests Class 1 through 4 on the given pairset
- Four class events when the PD requests Class 5 on the given pairset

between the most recent time  $V_{PSE}$  was at  $V_{Reset}$  for at least  $T_{Reset}$  and a transition to any of the power up states.

PSEs that issue more class events than the Class they are capable of supporting, in order to determine the PD requested Class, transition to CLASS\_RESET to reset the PD's class event count.

When the PSE is in CLASS\_EV1\_LCE, CLASS\_EV1\_AUTO, CLASS\_EV1\_LCE\_PRI, CLASS\_EV1\_LCE\_SEC, CLASS\_EV1\_LCE\_4PID\_PRI, or CLASS\_EV1\_LCE\_4PID\_SEC, it shall provide to the PI or pairset  $V_{Class}$ , subject to  $T_{LCE}$  timing specification.

The PSE in CLASS\_EV1\_AUTO shall measure  $I_{Class}$  on the negative pair or pairs after  $T_{Class\_ACS}$ , referenced from the application of the first class event, to determine if the PD will perform Autoclass. If the Autoclass enabled PSE in CLASS\_EV1\_AUTO measures  $I_{Class}$  in the range of class signature 0 this indicates the PD will perform Autoclass; see 145.2.8.2 and 145.3.6.2.

When the PSE is in CLASS\_EV2, CLASS\_EV2\_PRI, CLASS\_EV2\_SEC, CLASS\_EV3, CLASS\_EV3\_PRI, CLASS\_EV3\_SEC, CLASS\_EV4, CLASS\_EV4\_PRI, CLASS\_EV4\_SEC, or CLASS\_EV5, it shall provide to the PI or pairset  $V_{Class}$ , subject to the  $T_{CEV}$  timing specification.

In all CLASS states except CLASS\_EV1\_AUTO, the PSE shall measure  $I_{Class}$  on the negative pair or pairs after  $T_{Class}$ . This measurement is referenced from the application of  $V_{Class\_min}$  to ignore initial transients.

The timing specification for PSEs in a DO\_CLASS\_PROBE state may be reduced to  $T_{CEV}$  for all class events.

When the PSE is in MARK\_EV1, MARK\_EV1\_PRI, MARK\_EV1\_SEC, MARK\_EV2, MARK\_EV2\_PRI, MARK\_EV2\_SEC, MARK\_EV3, MARK\_EV3\_PRI, MARK\_EV3\_SEC, or MARK\_EV4, it shall provide to the PI or pairset  $V_{Mark}$ . The timing specification shall be as defined by  $T_{ME1}$ .

When a PSE is in MARK\_EV\_LAST, MARK\_EV\_LAST\_PRI or MARK\_EV\_LAST\_SEC, it shall provide to the PI or pairset  $V_{Mark}$ . The timing specification shall be as defined by  $T_{ME2}$ .

The  $V_{\text{Mark}}$  requirement is to be met with load currents in the range of  $I_{\text{Mark}}$  as defined in Table 145–25.

NOTE—In a properly operating system, the port may or may not discharge to the  $V_{\text{Mark}}$  range due to the combination of the overall channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the  $V_{\text{Mark}}$  voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which  $V_{\text{Mark}}$  can be observed with minimum and maximum load current.

If any measured  $I_{\text{Class}}$  is equal to or greater than  $I_{\text{Class\_LIM}}$  min, a PSE shall return to IDLE. The PSE shall limit class event currents to  $I_{\text{Class\_LIM}}$  and shall limit mark event currents to  $I_{\text{Mark\_LIM}}$ .

All class event voltages and mark event voltages shall have the same polarity as defined for  $V_{\text{Port\_PSE-2p}}$  in 145.2.4. PSEs may issue class events on one or both pairsets, when connected to a single-signature PD and operating over 4 pairs. The PSE shall complete Multiple-Event Physical Layer classification and transition to POWER\_ON, POWER\_ON\_PRI, or POWER\_ON\_SEC without allowing the voltage at the PI or pairset to go below  $V_{\text{Mark}}$  min, unless in CLASS\_RESET, CLASS\_RESET\_PRI, or CLASS\_RESET\_SEC. If the PSE returns to IDLE, it shall maintain the PI voltage in the range of  $V_{\text{Reset}}$  for a period of at least  $T_{\text{Reset}}$  min before starting a new detection cycle. If the PSE is in any of the CLASS\_RESET states it shall maintain the PI or pairset voltage in the range of  $V_{\text{Reset}}$  for a period of at least  $T_{\text{Reset}}$  min.

A PSE that implements 4PID based on Physical Layer classification and is restricted to Class 3 power or less, when connected to a dual-signature PD, shall issue three initial class events to determine the Type of the connected PD, then transition to either CLASS\_RESET\_PRI or CLASS\_RESET\_SEC.

#### 145.2.8.2 Autoclass (optional)

PSEs may implement an extension of Physical Layer classification known as Autoclass. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. Autoclass is only defined for single-signature PDs. See Figure 145B–15 for Autoclass timing diagrams.

If the PSE implements Autoclass it shall measure  $P_{\text{Autoclass}}$  when it reaches POWER\_ON and  $\text{pd\_autoclass}$  is TRUE.  $P_{\text{Autoclass}}$  is the power provided by the PSE measured throughout the period bounded by  $T_{\text{AUTO\_PSE1}}$  and  $T_{\text{AUTO\_PSE2}}$ , defined in Table 145–15.  $P_{\text{ac\_margin}}$ , defined in Table 145–15, is the minimum amount of power the PSE adds to  $P_{\text{Autoclass}}$  in order to allocate enough power to cope with increases in the link section resistance due to temperature increase.

$P_{\text{ac\_extra}}$  is the minimum amount of additional power allocation (above  $P_{\text{Autoclass}}$  and  $P_{\text{ac\_margin}}$ ) that a PSE allocates while providing power in 2-pair mode, when it performed the measurement of  $P_{\text{Autoclass}}$  in 4-pair mode. This extra allocation covers the additional losses incurred by the increase in link section resistance in 2-pair mode.  $P_{\text{ac\_extra}}$  does not apply for PSEs that performed the  $P_{\text{Autoclass}}$  measurement in 2-pair mode.

$T_{\text{AUTO\_PSE1}}$  and  $T_{\text{AUTO\_PSE2}}$  timing is referenced from the transition of POWER\_UP to POWER\_ON. The power consumption shall be defined as the highest average power measured throughout the period bounded by  $T_{\text{AUTO\_PSE1}}$  and  $T_{\text{AUTO\_PSE2}}$ . Average power is measured using a sliding window with a width in the range of  $T_{\text{AUTO\_Window}}$  as defined in Table 145–15.

**Table 145–15—Autoclass electrical requirements**

| Item | Parameter                                     | Symbol                    | Units | Min  | Max  | Additional information                               |
|------|-----------------------------------------------|---------------------------|-------|------|------|------------------------------------------------------|
| 1    | Autoclass power measurement start             | $T_{\text{AUTO\_PSE1}}$   | ms    | 1400 | 1600 | Measured from the transition of POWER_UP to POWER_ON |
| 2    | Autoclass power measurement end               | $T_{\text{AUTO\_PSE2}}$   | ms    | 3100 | 3500 |                                                      |
| 3    | Autoclass average power sliding window width  | $T_{\text{AUTO\_Window}}$ | ms    | 150  | 300  | —                                                    |
| 4    | Autoclass power margin per the assigned Class |                           |       |      |      | —                                                    |
|      | Class 1 to 4                                  | $P_{\text{ac\_margin}}$   | W     | 0.5  | —    |                                                      |
|      | Class 5 to 6                                  |                           |       | 0.75 | —    |                                                      |
|      | Class 7 to 8                                  |                           |       | 1.5  | —    |                                                      |

**145.2.9 4PID requirements**

PSEs determine whether an attached PD is a candidate to receive power on both pairsets prior to applying operating voltage to both pairsets. This determination is referred to as 4PID. 4PID is a logical function of the detection state of both pairsets, the result of connection check as described in 145.2.7, and mutual identification. The variable  $\text{pd\_4pair\_cand}$ , defined in 145.2.5.4, contains the result of this determination.

A PSE shall not apply 4-pair power unless the PSE has detected a valid detection signature on both pairsets and one or more of the following conditions are met:

- The connected PD is a single-signature PD.
- The PSE detects a valid detection signature on the unpowered pairset when power is provided in 2-pair mode.
- The PSE has identified the PD as Type 3 or Type 4.

**145.2.10 Power supply output**

When the PSE provides power to the PI, it shall conform with Table 145–16. Table 145–16 values support worst-case operating conditions. These ranges may be narrowed when additional information is known and applied in accordance with this specification. Power may be removed from both pairsets any time power is removed from one pairset.

**Table 145–16—PSE output PI electrical requirements for all PD Classes,  
unless otherwise specified**

| Item | Parameter                                                                                         | Symbol                | Unit     | Min         | Max  | PSE Type | Additional information                                        |
|------|---------------------------------------------------------------------------------------------------|-----------------------|----------|-------------|------|----------|---------------------------------------------------------------|
| 1    | Output voltage per pairset in a power on state                                                    | $V_{Port\_PSE-2P}$    | V        | 50          | 57   | 3        | See 145.2.10.1.                                               |
|      |                                                                                                   |                       |          | 52          |      | 4        |                                                               |
| 2    | Pair-to-pair voltage difference                                                                   | $V_{Port\_PSE\_diff}$ | V        | —           | 0.01 | 3, 4     | See 145.2.10.2.                                               |
| 3    | Output voltage during transient                                                                   | $V_{Tran-2P}$         | V        | 45.3        | —    | 3        | See 145.2.10.3.                                               |
|      |                                                                                                   |                       |          | 48.4        | —    | 4        |                                                               |
| 4    | Power feeding ripple and noise:                                                                   |                       |          |             |      |          |                                                               |
|      | $f < 500$ Hz                                                                                      | $V_{Noise}$           | $V_{pp}$ | —           | 0.5  | 3, 4     | See 145.2.10.5.                                               |
|      | 500 Hz to 150 kHz                                                                                 |                       |          |             | 0.2  |          |                                                               |
|      | 150 kHz to 500 kHz                                                                                |                       |          |             | 0.15 |          |                                                               |
|      | 500 kHz to 1 MHz                                                                                  |                       |          |             | 0.1  |          |                                                               |
| 5    | Supported pair current to account for unbalance per the assigned Class (for single-signature PDs) |                       |          |             |      |          |                                                               |
|      | Class 1 to 4                                                                                      | $I_{Con-2P-unb}$      | A        | $I_{Con}^a$ | —    | 3, 4     | See 145.2.10.6 and 145.2.10.6.1.                              |
|      | Class 5                                                                                           |                       |          | 0.56        | —    | 3, 4     |                                                               |
|      | Class 6                                                                                           |                       |          | 0.692       | —    | 3, 4     |                                                               |
|      | Class 7                                                                                           |                       |          | 0.794       | —    | 4        |                                                               |
|      | Class 8                                                                                           |                       |          | 0.948       | —    | 4        |                                                               |
| 6    | Total output current of both pairs of the same polarity during POWER_UP per the assigned Class    |                       |          |             |      |          |                                                               |
|      | Single-signature PD, Class 1 to 4                                                                 | $I_{Inrush}$          | A        | 0.4         | 0.45 | 3, 4     | See 145.2.10.7 and maximum value definition in Figure 145–22. |
|      | Single-signature PD, Class 5 to 6                                                                 |                       |          | 0.4         | 0.9  | 3, 4     |                                                               |
|      | Single-signature PD, Class 7 to 8                                                                 |                       |          | 0.8         | 0.9  | 4        |                                                               |
| 7    | Current per pairset during power up per the assigned Class                                        |                       |          |             |      |          |                                                               |
|      | Single-signature PD, Class 1 to 4                                                                 | $I_{Inrush-2P}$       | A        | —           | 0.45 | 3, 4     | See 145.2.10.7 and maximum value definition in Figure 145–22. |
|      | Single-signature PD, Class 5 to 6                                                                 |                       |          | —           | 0.6  | 3, 4     |                                                               |
|      | Single-signature PD, Class 7 to 8                                                                 |                       |          | —           | 0.6  | 4        |                                                               |
|      | Dual-signature PD, Class 1 to 4                                                                   |                       |          | 0.4         | 0.45 | 3, 4     |                                                               |
|      | Dual-signature PD, Class 5                                                                        |                       |          | 0.4         | 0.45 | 4        |                                                               |
| 8    | Inrush time                                                                                       | $T_{Inrush}$          | ms       | 50          | 75   | 3, 4     | See 145.2.10.7.                                               |

**Table 145–16—PSE output PI electrical requirements for all PD Classes,  
unless otherwise specified (continued)**

| Item | Parameter                                                                                            | Symbol              | Unit | Min                 | Max      | PSE Type | Additional information                                                |
|------|------------------------------------------------------------------------------------------------------|---------------------|------|---------------------|----------|----------|-----------------------------------------------------------------------|
| 9    | Overload current per pairset detection range                                                         | I <sub>CUT-2P</sub> | A    | I <sub>Con-2P</sub> | —        | 3, 4     | Optional limit; see 145.2.10.6, 145.2.10.8, Table 145–11.             |
| 10   | Overload time limit                                                                                  | T <sub>CUT</sub>    | ms   | 50                  | 75       | 3, 4     | See 145.2.10.9.                                                       |
| 11   | Output current per pairset – at short circuit condition, per the assigned Class, single-signature PD |                     |      |                     |          |          |                                                                       |
|      | Class 1 to 3                                                                                         | I <sub>LIM-2P</sub> | A    | 0.4                 | See info | 3, 4     | See 145.2.10.9. Max value defined by Figure 145–23 and Figure 145–24. |
|      | Class 4                                                                                              |                     |      | 0.684 <sup>b</sup>  |          | 3, 4     |                                                                       |
|      | Class 5                                                                                              |                     |      | 0.58                |          | 3, 4     |                                                                       |
|      | Class 6                                                                                              |                     |      | 0.72                |          | 3, 4     |                                                                       |
|      | Class 7                                                                                              |                     |      | 0.85                |          | 4        |                                                                       |
|      | Class 8                                                                                              |                     |      | 1.005               |          | 4        |                                                                       |
|      | Output current per pairset – at short circuit condition, per the assigned Class, dual-signature PD   |                     |      |                     |          |          |                                                                       |
|      | Class 1 to 3                                                                                         | I <sub>LIM-2P</sub> | A    | 0.4                 | See info | 3, 4     | See 145.2.10.9. Max value defined by Figure 145–23 and Figure 145–24. |
|      | Class 4                                                                                              |                     |      | 0.684               |          | 3, 4     |                                                                       |
|      | Class 5                                                                                              |                     |      | 0.99                |          | 4        |                                                                       |
| 12   | Short circuit time limit                                                                             | T <sub>LIM</sub>    | ms   | 10                  | 75       | 3        | See 145.2.10.1 and 145.2.10.9.                                        |
|      |                                                                                                      |                     |      | 6                   |          | 4        |                                                                       |
| 13   | PSE Type power                                                                                       | P <sub>Type</sub>   | W    | 4                   | —        | 3        | See 145.2.10.13                                                       |
|      |                                                                                                      |                     |      | 75                  | 99.9     | 4        |                                                                       |
| 14   | Power turn on time                                                                                   | T <sub>pon</sub>    | ms   | —                   | 400      | 3, 4     | See 145.2.10.14.                                                      |
| 15   | Turn on rise time per pairset                                                                        | T <sub>Rise</sub>   | ms   | 0.015               | —        | 3, 4     | See 145.2.10.1                                                        |
| 16   | Turn off time per pairset                                                                            | T <sub>Off</sub>    | ms   | —                   | 500      | 3, 4     | See 145.2.10.10.                                                      |
| 17   | Turn off voltage per pairset                                                                         | V <sub>Off</sub>    | V    | —                   | 2.8      | 3, 4     | See 145.2.10.11.                                                      |
| 18   | Unpowered negative pair reverse current                                                              |                     |      |                     |          |          |                                                                       |
|      | Highest V <sub>PSE</sub> > 21 V                                                                      | I <sub>rev</sub>    | A    | —                   | 0.0013   | 3, 4     | See 145.2.10.4, 145.3.8.8.                                            |
|      | Highest V <sub>PSE</sub> ≤ 21 V                                                                      |                     |      |                     | 0.0005   |          |                                                                       |

**Table 145–16—PSE output PI electrical requirements for all PD Classes,  
unless otherwise specified (*continued*)**

| Item | Parameter                                                                       | Symbol               | Unit | Min   | Max   | PSE Type | Additional information                   |
|------|---------------------------------------------------------------------------------|----------------------|------|-------|-------|----------|------------------------------------------|
| 19   | DC MPS current on at least one pairset, per the assigned Class                  |                      |      |       |       |          | See 145.2.12.                            |
|      | Single-signature PD, Class 1 to 4, 2-pair                                       | $I_{\text{Hold-2P}}$ | A    | 0.004 | 0.009 | 3, 4     |                                          |
|      | Single-signature PD, Class 1 to 4, 4-pair                                       |                      |      | 0.002 | 0.005 |          |                                          |
|      | Single-signature PD, Class 5 to 8                                               |                      |      | 0.002 | 0.007 |          |                                          |
|      | DC MPS current on each pairset                                                  |                      |      |       |       |          |                                          |
|      | Dual-signature PD                                                               | $I_{\text{Hold-2P}}$ | A    | 0.002 | 0.007 | 3, 4     |                                          |
| 20   | DC MPS total current on both pairs of the same polarity, per the assigned Class |                      |      |       |       |          | See 145.2.12.                            |
|      | Single-signature PD, Class 1 to 4                                               | $I_{\text{Hold}}$    | A    | 0.004 | 0.009 | 3, 4     |                                          |
|      | Single-signature PD, Class 5 to 8                                               |                      |      | 0.004 | 0.014 | 3, 4     |                                          |
| 21   | PD MPS dropout time limit                                                       | $T_{\text{MPDO}}$    | ms   | 320   | 400   | 3,4      | See 145.2.12.                            |
| 22   | PD MPS time for validity                                                        | $T_{\text{MPS}}$     | ms   | 6     | —     | 3,4      | See 145.2.12.                            |
| 23   | Alternative B detection backoff time                                            | $T_{\text{dbo}}$     | ms   | 2000  | —     | 3, 4     | —                                        |
| 24   | Detection timing                                                                | $T_{\text{det}}$     | ms   | —     | 500   | 3, 4     | Time to complete detection on a pairset. |
| 25   | Error delay timing                                                              | $T_{\text{ed}}$      | ms   | 750   | —     | 3, 4     | See 145.2.10.15                          |

<sup>a</sup> The  $I_{\text{Con-2P-unb}}$  value is higher than the value for Class 5 as unbalance for Class 4 is not restricted.

<sup>b</sup> Unbalance at Class 4 is not restricted. The  $I_{\text{LIM-2P}}$  value is higher than the value for Class 5 for PSEs operating in 4-pair mode.

#### 145.2.10.1 Output voltage in the power on states

The specification for  $V_{\text{Port\_PSE-2P}}$  in Table 145–16 shall be met with a load step of ( $I_{\text{Hold max}} \times V_{\text{Port\_PSE-2P min}}$ ) to the maximum power per the PSE's assigned Class at a rate of change of up to 15 mA/ $\mu\text{s}$ . The voltage transients as a result of load changes up to 35 mA/ $\mu\text{s}$  shall be limited to 3.5 V/ $\mu\text{s}$ .

A PSE that has assigned Class 1 to 4 to a single-signature PD and is in a power on state may transition between 2-pair and 4-pair power at any time, including after the expiration of  $T_{\text{pon}}$ . A PSE that has assigned Class 5 to 8 to a single-signature PD shall apply power to both pairsets while in POWER\_ON.

$T_{\text{Rise}}$ , as defined in Table 145–16, is referenced from 10% to 90% of the voltage difference between the positive and the negative conductors of a pairset in a power on state from the beginning of a power up state.

#### 145.2.10.2 Output voltage pair-to-pair difference

$V_{\text{Port\_PSE\_diff}}$ , as defined in Table 145–16, is the maximum voltage difference between pairs with the same polarity, at no load condition, when operating over 4 pairs, in a power on state.

#### 145.2.10.3 Voltage transients

A PSE shall maintain an output voltage no less than  $V_{\text{Tran-2P}}$  for transient conditions lasting more than 30  $\mu\text{s}$  and less than 250  $\mu\text{s}$ , and meet the requirements of 145.2.10.9. Transients less than 30  $\mu\text{s}$  in duration may cause the voltage at the PI to fall below  $V_{\text{Tran-2P}}$ . See 145.3.8.6 for PD transient requirements. Transients lasting more than 250  $\mu\text{s}$  shall meet the  $V_{\text{Port\_PSE-2P}}$  specification.

NOTE—The occurrence of voltage transients lasting more than 250  $\mu\text{s}$  or voltage steps of significant amplitude (within the  $V_{\text{Port\_PSE-2P}}$  specification) should be limited to rare circumstances such as those involving switchover of backup power supplies or those involving significant change in current demand on the PSE power supply due to a large load step spread over multiple powered ports.

#### 145.2.10.4 Reflected voltage

When a 4-pair capable PSE provides power in 2-pair mode, whereby two pairs are connected to the positive  $V_{\text{PSE}}$ , and one pair is connected to the negative  $V_{\text{PSE}}$ , a single-signature PD may reflect a voltage of up to  $V_{\text{PSE}}$  back onto the unpowered pairset. See 145.3.8.8. This can cause a reverse current,  $I_{\text{rev}}$  as defined in Table 145–16, to flow. Reverse current is current flowing out of the PSE on a negative pair.

The PSE shall not source a current higher than  $I_{\text{rev}}$ , as defined in Table 145–16, on a negative pair. This requirement holds only when no power is being sourced into the PSE.

#### 145.2.10.5 Power feeding ripple and noise

$V_{\text{Noise}}$ , the specification for power feeding ripple and noise in Table 145–16, shall be met for common-mode and pair-to-pair noise values at all static PSE output voltages. The limits are meant to preserve data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 145.4.4, 145.4.5, and 145.4.6.

#### 145.2.10.6 Continuous current capability in the power on states

$I_{\text{Port-2P}}$  and  $I_{\text{Port-2P-other}}$  are the currents on the negative pairs and are defined in Equation (145–5) and in Equation (145–6).

$$I_{\text{Port-2P}} = \left\{ \begin{array}{l} I_{\text{Port-2P-pri}} \text{ for the Primary Alternative} \\ I_{\text{Port-2P-sec}} \text{ for the Secondary Alternative} \end{array} \right\}_A \quad (145-5)$$

$$I_{\text{Port-2P-other}} = \left\{ \begin{array}{l} I_{\text{Port-2P-sec}} \text{ for the Primary Alternative} \\ I_{\text{Port-2P-pri}} \text{ for the Secondary Alternative} \end{array} \right\}_A \quad (145-6)$$

$I_{\text{Port}}$  is the total current on both pairs with the same polarity and is defined in Equation (145-7).

$$I_{\text{Port}} = \{ I_{\text{Port-2P}} + I_{\text{Port-2P-other}} \}_A \quad (145-7)$$

where

$I_{\text{Port-2P-pri}}$  is the current supplied on the negative pair of the Primary Alternative  
 $I_{\text{Port-2P-sec}}$  is the current supplied on the negative pair of the Secondary Alternative

PSEs shall be able to supply  $I_{\text{Con-2P}}$ , the current the PSE supports on both pairs of each powered pairset, as defined in Equation (145-8).  $I_{\text{Con-2P}}$  should be measured using a sliding window with a width of 1 second.

$$I_{\text{Con-2P}} = \left\{ \begin{array}{l} P_{\text{Class}}/V_{\text{PSE}} \text{ when in 2-pair mode} \\ \min(I_{\text{Con}} - I_{\text{Port-2P-other}}, I_{\text{Con-2P-unb}}) \text{ when 4-pair powering a single-signature PD} \\ P_{\text{Class-2P}}/V_{\text{PSE}} \text{ when 4-pair powering a dual-signature PD} \end{array} \right\}_A \quad (145-8)$$

where

$P_{\text{Class}}$  is  $P_{\text{Class}}$  as defined in Equation (145-2)  
 $P_{\text{Class-2P}}$  is  $P_{\text{Class-2P}}$  as defined in Equation (145-3)  
 $V_{\text{PSE}}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3  
 $I_{\text{Con}}$  is the total current a PSE is able to source as defined in Equation (145-9)  
 $I_{\text{Con-2P-unb}}$  is the current a PSE is able to supply on each pair to account for pair-to-pair unbalance as defined in Table 145-16  
 $I_{\text{Port-2P-other}}$  is the current on the other negative pair as defined in Equation (145-6)

When powering a single-signature PD over 4 pairs, a PSE supports both:

- A total current of  $I_{\text{Con}}$ , defined in Equation (145-9), over both pairs with the same polarity;
- A minimum current of  $I_{\text{Con-2P-unb}}$  on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.

$$I_{\text{Con}} = \left\{ \frac{P_{\text{Class}}}{V_{\text{PSE}}} \right\}_A \quad (145-9)$$

where

$P_{\text{Class}}$  is  $P_{\text{Class}}$  as defined in Equation (145-2)  
 $V_{\text{PSE}}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3

The PSE shall support the AC current waveform parameter  $I_{\text{Peak-2P}}$ , defined in Equation (145–10), on both pairs of each powered pairset, while within the operating voltage range of  $V_{\text{Port\_PSE-2P}}$ , for a minimum of  $T_{\text{CUT}}$  and a duty cycle of at least 5%.

$$I_{\text{Peak-2P}} = \left\{ \begin{array}{ll} I_{\text{Peak}} & \text{when in 2-pair mode} \\ \min(I_{\text{Peak}} - I_{\text{Port-2P-other}}, I_{\text{Peak-2P-unb}}) & \text{when 4-pair powering a single-signature PD} \\ \frac{V_{\text{PSE}} - \sqrt{V_{\text{PSE}}^2 - 4 \times R_{\text{Chan-2P}} \times P_{\text{Peak\_PD-2P}}}}{2 \times R_{\text{Chan-2P}}} & \text{when 4-pair powering a dual-signature PD} \end{array} \right\}_A \quad (145-10)$$

where

- $I_{\text{Peak}}$  is the total peak current a PSE supports per Equation (145–11)
- $I_{\text{Port-2P-other}}$  is the current on the other negative pair as defined in Equation (145–6)
- $I_{\text{Peak-2P-unb}}$  is the minimum peak current supported to account for unbalance, defined in Equation (145–12)
- $V_{\text{PSE}}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3
- $R_{\text{Chan-2P}}$  is the pairset loop resistance; this parameter has a worst-case value of  $R_{\text{Ch}}$  defined in 145.1.3 and Table 145–1
- $P_{\text{Peak\_PD-2P}}$  is the peak power a dual-signature PD may draw per its assigned Class on a pairset; see Table 145–29

$I_{\text{Peak}}$ , defined in Equation (145–11), is the total current of the powered pairs with the same polarity that a PSE supports, when powering a PD over 2 pairs or powering a single-signature PD over 4 pairs.

$$I_{\text{Peak}} = \left\{ \frac{V_{\text{PSE}} - \sqrt{V_{\text{PSE}}^2 - 4 \times R_{\text{Chan}} \times P_{\text{Peak\_PD}}}}{2 \times R_{\text{Chan}}} \right\}_A \quad (145-11)$$

where

- $V_{\text{PSE}}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3
- $R_{\text{Chan}}$  is the link section loop resistance as defined in 145.1.3
- $P_{\text{Peak\_PD}}$  is the total peak power a PD may draw for its Class; see Table 145–29

$I_{\text{Peak-2P-unb}}$ , defined in Equation (145–12), is the minimum current that a PSE is able to supply on both the positive pair and the negative pair with the highest current, when powering a single-signature PD over 4 pairs.

$$I_{\text{Peak-2P-unb}} = \{I_{\text{LIM-2P}} - 0.002\}_A \quad (145-12)$$

where

- $I_{\text{LIM-2P}}$  is the  $I_{\text{LIM-2P}}$  min value per pairset for the PSE, as defined in Table 145–16

**145.2.10.6.1 PSE pair-to-pair current unbalance**

When a PSE supplies power to a PD using all 4 pairs, the current may not equally divide between the pairs that are at the same polarity. This is referred to as pair-to-pair current unbalance. The degree to which the current is unbalanced depends on the specific combination of PSE, cabling, and PD.

The maximum pair current in a system depends on the assigned Class (see 145.2.8), and is defined in Table 145–17.

**Table 145–17—Maximum pair-to-pair current unbalance**

| Parameter                 | Assigned Class | Unit | Value                          |
|---------------------------|----------------|------|--------------------------------|
| $I_{\text{Unbalance-2P}}$ | 1 to 4         | A    | $I_{\text{Con}}^{\text{a}}$    |
|                           | 5 to 8         |      | $I_{\text{Con-2P-unb}} - 0.01$ |

<sup>a</sup> Unbalance current for these assigned Classes is not restricted.

PSEs that operate over 4 pairs are subject to unbalance requirements. The contribution of PSE PI pair-to-pair effective resistance unbalance to the system end-to-end effective resistance unbalance is specified by PSE maximum ( $R_{\text{PSE\_max}}$ ) and minimum ( $R_{\text{PSE\_min}}$ ) common mode effective resistance in the powered pairs of same polarity, see Figure 145A–1. Effective resistances of  $R_{\text{PSE\_min}}$  and  $R_{\text{PSE\_max}}$  include the effects of  $V_{\text{Port\_PSE\_diff}}$  as defined in Table 145–16 and the PSE PI resistive elements. See definition and measurements in Annex 145A.

The PSE PI pair-to-pair effective resistance unbalance determined by  $R_{\text{PSE\_max}}$  and  $R_{\text{PSE\_min}}$ , along with any other parts of the system, i.e., the cabling and the PD, bounds the current such that the pair with the highest current including unbalance does not exceed  $I_{\text{Unbalance-2P}}$  as defined in Table 145–17 during normal operating conditions.  $I_{\text{Unbalance-2P}}$  is the highest pair current in case of maximum unbalance and will be higher than  $I_{\text{Con}} / 2$ .  $I_{\text{Unbalance-2P}}$  applies to link section common mode pair resistances from 0.2  $\Omega$  to  $R_{\text{Ch}}$ , as defined in 145.1.3.

$R_{\text{PSE\_max}}$  and  $R_{\text{PSE\_min}}$  are specified and measured under maximum  $P_{\text{Class\_PD}}$  load conditions, measured at the PD PI, over the  $V_{\text{Port\_PSE-2P}}$  operating range.  $R_{\text{PSE\_max}}$  and  $R_{\text{PSE\_min}}$  for the positive pairs are not necessarily the same values as for the negative pairs.

PSEs that meet  $R_{\text{PSE\_min}}$  and  $R_{\text{PSE\_max}}$ , as defined by Equation (145–13) meet the unbalance requirements under worst case conditions of link section pair to pair unbalance and PD PI pair to pair unbalance. Equation (145–13) is only applicable for  $R_{\text{PSE\_min}}$  up to a value of 1  $\Omega$  for Class 5 and Class 6, and 0.5  $\Omega$  for Class 7 and Class 8.

$$0 < R_{\text{PSE\_max}} \leq \left\{ \begin{array}{ll} 2.182 \times R_{\text{PSE\_min}} - 0.04 & \text{for Class 5} \\ 1.999 \times R_{\text{PSE\_min}} - 0.04 & \text{for Class 6} \\ 1.904 \times R_{\text{PSE\_min}} - 0.03 & \text{for Class 7} \\ 1.832 \times R_{\text{PSE\_min}} - 0.03 & \text{for Class 8} \end{array} \right\}_{\Omega} \quad (145-13)$$

where

$R_{\text{PSE\_max}}$  is, given  $R_{\text{PSE\_min}}$ , the highest supported common mode effective resistance in the powered pairs of the same polarity

$R_{\text{PSE\_min}}$  is the lower PSE common mode effective resistance in the powered pairs of the same polarity

$R_{PSE\_min}$  or  $R_{PSE\_max}$  common mode effective resistance is the resistance of the two internal conductors (including the internal components on each conductor) in a powered pair of the same polarity connected in parallel.

A PSE shall not source more than  $I_{Unbalance-2P}$  on any pair when connected to a load as shown in Figure 145–21, using values of  $R_{load\_min}$  and  $R_{load\_max}$  as defined in Equation (145–14) and Equation (145–15). This unbalance current requirement applies at the PSE PI connector (jack) when mated with a specified balanced cabling connector (plug).

$R_{load\_min}$  and  $R_{load\_max}$ , defined in Equation (145–14) and Equation (145–15), are respectively the minimum and maximum common mode effective load resistances in the powered pairs of the same polarity.

Table 145–18 specifies the resistance values used to compute  $R_{load\_min}$  and  $R_{load\_max}$  according to Equation (145–14) and Equation (145–15). The load resistances  $R_{load\_min}$  and  $R_{load\_max}$  are split into two series resistances  $R_{load1\_min}$  and  $R_{load2\_min}$ , and  $R_{load1\_max}$  and  $R_{load2\_max}$  respectively, as shown in Figure 145–21, so the power sink can be set such that the power consumption inside the  $P_{load}$  box equals  $P_{Class\_PD}$ .

$$R_{load\_min} = R_{load1\_min} + R_{load2\_min} \quad (145-14)$$

$$R_{load\_max} = R_{load1\_max} + R_{load2\_max} \quad (145-15)$$

where

$R_{load1\_max}$  is, given  $R_{load1\_min}$ , the higher resistance value representing the link section resistance

$R_{load1\_min}$  is the lower resistance representing the link section resistance

$R_{load2\_max}$  is, given  $R_{load2\_min}$ , the higher resistance value representing the PD contribution to unbalance

$R_{load2\_min}$  is the lower resistance representing the PD contribution to unbalance

**Table 145–18—PSE unbalance test fixture resistances**

| PSE Class | $R_{load1\_min}$ ( $\Omega$ ) | $R_{load1\_max}$ ( $\Omega$ ) | $R_{load2\_min}$ ( $\Omega$ ) | $R_{load2\_max}$ ( $\Omega$ ) | Additional information                   |
|-----------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|------------------------------------------|
| 5         | 0.087                         | 0.101                         | 0.638                         | 1.518                         | Low link section resistance conditions.  |
| 6         |                               |                               | 0.538                         | 1.183                         |                                          |
| 7         |                               |                               | 0.483                         | 1.017                         |                                          |
| 8         |                               |                               | 0.439                         | 0.894                         |                                          |
| 5         | 5.41                          | 6.25                          | 0.704                         | 1.026                         | High link section resistance conditions. |
| 6         |                               |                               | 0.564                         | 0.822                         |                                          |
| 7         |                               |                               | 0.491                         | 0.717                         |                                          |
| 8         |                               |                               | 0.43                          | 0.629                         |                                          |

The values for  $I_{\text{Unbalance-2P}}$  and the relation between  $R_{\text{PSE\_max}}$  and  $R_{\text{PSE\_min}}$ , as defined in Equation (145–13), are valid given that  $R_{\text{Chan-2P}}$  (see 145.1.3) ranges from  $0.2\ \Omega$  to  $12.5\ \Omega$ . See 145A.4 for guidelines on how to support low resistance link sections.

Figure 145–21 shows a verification circuit for the PSE current unbalance requirements measurement. Other methods for measuring  $R_{\text{PSE\_min}}$  and  $R_{\text{PSE\_max}}$  are described in Annex 145A.

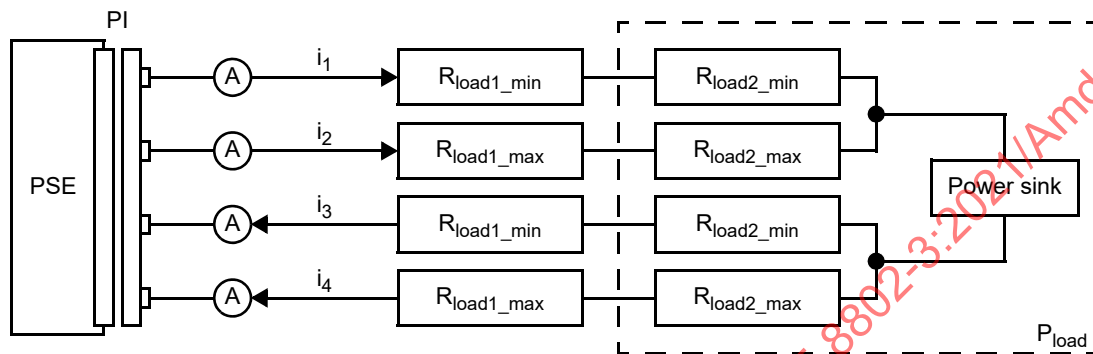


Figure 145–21—PSE current unbalance verification circuit

The evaluation method is as follows:

- Use  $R_{\text{load\_min}}$  and  $R_{\text{load\_max}}$  from Equation (145–14) and Equation (145–15) for low channel resistance conditions.
- Adjust the power sink such that  $P_{\text{load}}$  (the power consumed by the  $R_{\text{load2}}$  resistances and the power sink) equals  $P_{\text{Class\_PD}}$  for the given Class.
- Verify that currents  $i_1$ ,  $i_2$ ,  $i_3$ , and  $i_4$  are lower than  $I_{\text{Unbalance-2P}}$ , as defined in Table 145–17.
- Exchange  $R_{\text{load\_max}}$  and  $R_{\text{load\_min}}$ . Repeat steps b) and c).
- Repeat steps b) through d) for  $R_{\text{load\_min}}$  and  $R_{\text{load\_max}}$  components from Equation (145–14) and Equation (145–15) for high channel resistance conditions.

#### 145.2.10.7 Current during power up

Power up occurs on each pairset between the transition to a power up state on that pairset and the expiration of  $T_{\text{Inrush}}$ . A PSE that provides current on both pairsets during POWER\_UP shall complete power up within  $T_{\text{Inrush\_max}}$ , starting when the first pairset exceeds a voltage of 30 V. PSEs that have assigned Class 1 through 6 to a single-signature PD may perform inrush over 2 pairs or over 4 pairs. PSEs that have assigned Class 5 or Class 6 to a single-signature PD transition to 4-pair mode by  $T_{\text{Inrush}}$ . PSEs that have assigned Class 7 or Class 8 to a single-signature PD perform inrush over 4 pairs.

The PSE shall limit the current on each powered negative pair to  $I_{\text{Inrush-2P}}$  and the total current on the negative pairs to  $I_{\text{Inrush}}$  during power up per the requirements of Table 145–16, with the exception of the initial per pairset transient described in Equation (145–16).

$$I_{\text{PSEIT-2P}}(t) = \left\{ \begin{array}{ll} I_{\text{Inrush-2P max}} & \text{for } 0 \leq t < t_0 \\ 50 & \text{for } t_0 \leq t < (t_0 + 10 \times 10^{-6}) \\ I_{\text{Inrush-2P max}} + \frac{(50 - I_{\text{Inrush-2P max}}) \times (0.001 + t_0 - t)}{99 \times 10^{-5}} & \text{for } (t_0 + 10 \times 10^{-6}) \leq t < (t_0 + 0.001) \\ I_{\text{Inrush-2P max}} & \text{for } (t_0 + 0.001) \leq t < 0.075 \end{array} \right\} \quad (145-16)$$

where

- $t$  is the time in seconds
- $I_{\text{Inrush-2P max}}$  is the maximum value of  $I_{\text{Inrush-2P}}$  as defined in Table 145–16
- $t_0$  is the time when  $I_{\text{Port-2P}}$  exceeds  $I_{\text{Inrush-2P max}}$  for the first time during the power up states.  
The range for  $t_0$  is  $0 \leq t_0 \leq 49$  ms.

The PSE inrush maximum limit,  $I_{\text{PSEIT-2P}}$ , shown in Figure 145–22, is defined by Equation (145–16).

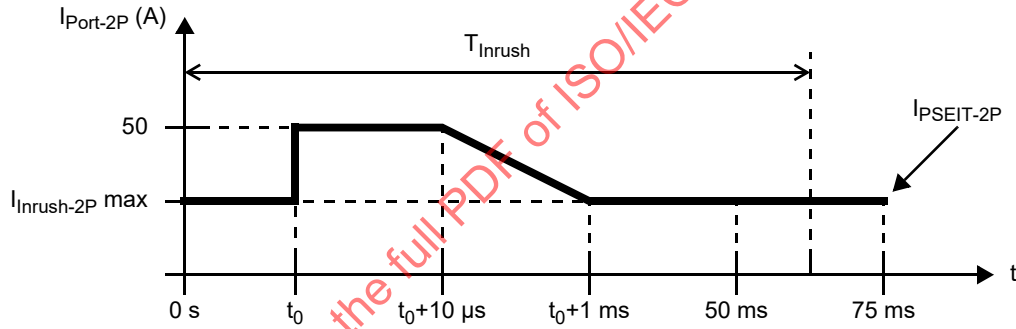


Figure 145–22—Per pairset PSE inrush maximum current

The minimum  $I_{\text{Inrush}}$  and  $I_{\text{Inrush-2P}}$  current capability as defined in Table 145–16 applies when  $V_{\text{PSE}}$  exceeds 30 V. During a power up state, the PSE shall support the following:

- When powering a single-signature PD, a minimum  $I_{\text{Inrush}}$  of 5 mA when  $V_{\text{PSE}}$  is between 0 V and 10 V, and 60 mA when  $V_{\text{PSE}}$  is between 10 V and 30 V.
- When powering a dual-signature PD, a minimum  $I_{\text{Inrush-2P}}$  of 5 mA when  $V_{\text{PSE}}$  is between 0 V and 10 V, and 60 mA when  $V_{\text{PSE}}$  is between 10 V and 30 V.

**145.2.10.8 Overload current**

If the current on either pair of a pairset exceeds  $I_{\text{CUT-2P}}$  for longer than  $T_{\text{CUT}}$ , the PSE may remove power from that pairset. The cumulative duration of  $T_{\text{CUT}}$  is measured using a sliding window of at least 1 second width.

**145.2.10.9 Short circuit current**

The PSE shall limit the pairset current to  $I_{\text{LIM-2P}}$  for a duration of at least  $T_{\text{LIM}}$  min, when  $V_{\text{PSE}}$  is in the range of  $V_{\text{Port\_PSE-2P}}$ . The cumulative duration of the current limit event may be measured with a sliding window of at most 1 second width.

The maximum value of  $I_{\text{LIM-2P}}$  is the PSE upperbound template described by Equation (145–17), Equation (145–18), Figure 145–23, and Figure 145–24. The  $I_{\text{LIM-2P}}$  minimum value in Table 145–16 for Class 5 and above includes the effective system end-to-end resistance unbalance effect.

The PSE shall remove power from a pairset before a current limit event persists on that pairset continuously for  $T_{\text{LIM}}$  max as defined in Table 145–16.

A PSE in a power on state may remove power from a pairset without regard to  $T_{\text{LIM}}$  when the voltage on that pairset no longer meets the  $V_{\text{Port\_PSE-2P}}$  specification for longer than 250  $\mu\text{s}$  or the voltage no longer meets the  $V_{\text{Tran-2P}}$  specification.

If  $I_{\text{Port-2P}}$  exceeds the PSE lowerbound template, the PSE output voltage may drop below  $V_{\text{Port\_PSE-2P}}$  min.

A PSE may remove power from the PI if the current on any pair exceeds the “PSE lowerbound template” in Figure 145–23 or Figure 145–24. Power shall be removed from a pairset of a PSE before the pairset current exceeds the “PSE upperbound template” in Figure 145–23 or Figure 145–24. When connected to a single-signature PD, the PSE should remove power from both pairsets before the current exceeds the “PSE upperbound template” on either pairset.

The right side vertical axis in Figure 145–23 and Figure 145–24 indicates the total current over both pairsets when the PSE supplies 4-pair power to a single-signature PD.

- For Type 3 PSEs, Figure 145–23, Equation (145–17) and Equation (145–19) apply.
- For Type 4 PSEs, Figure 145–24, Equation (145–18) and Equation (145–20) apply.

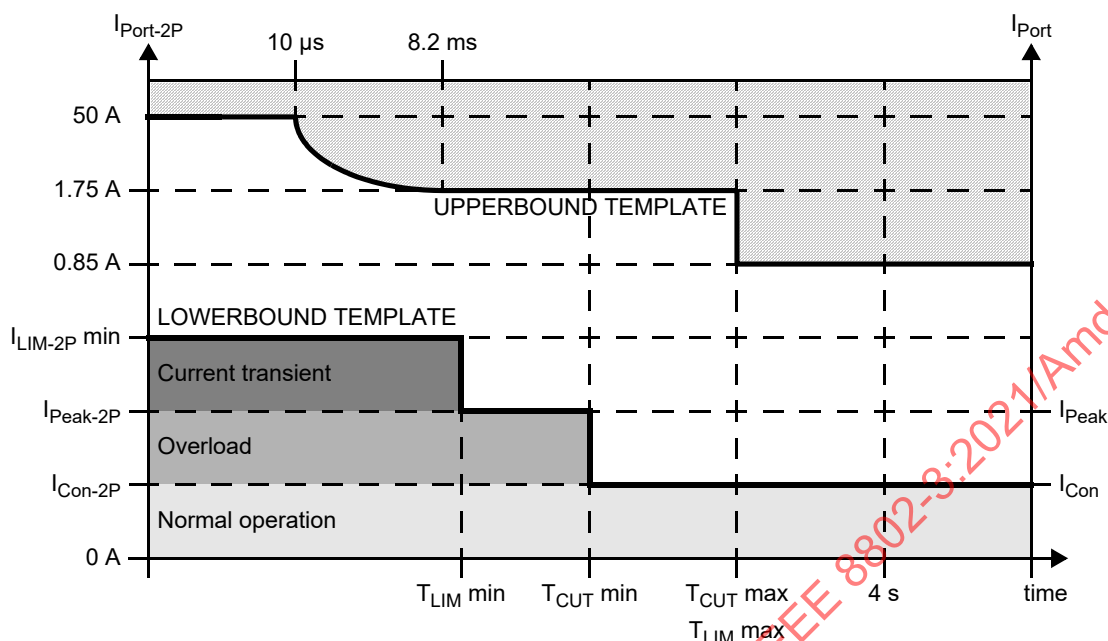


Figure 145-23—Power on states, per pairset operating current template for Type 3 PSEs

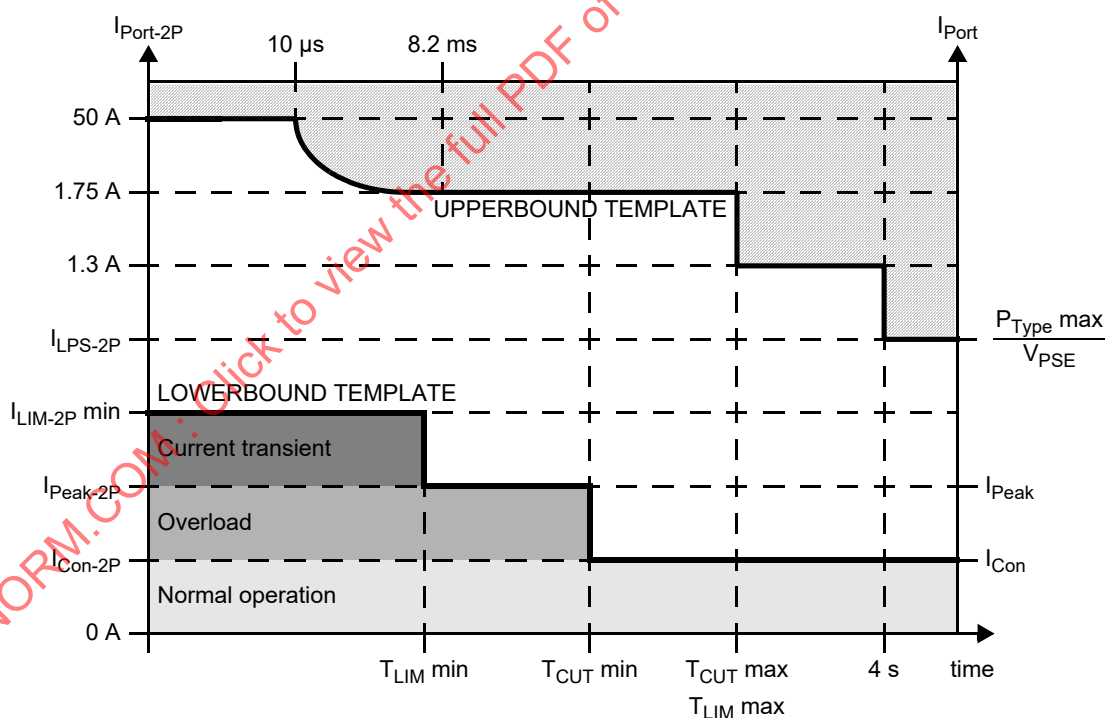


Figure 145-24—Power on states, per pairset operating current template for Type 4 PSEs

The PSE upperbound templates,  $I_{\text{PSEUT-Type3-2P}}$  and  $I_{\text{PSEUT-Type4-2P}}$ , are defined by the following segments:

$$I_{\text{PSEUT-Type3-2P}}(t) = \left\{ \begin{array}{ll} 50 & \text{for } (0 \leq t < 10 \times 10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10 \times 10^{-6} \leq t < 8.2 \times 10^{-3}) \\ 1.75 & \text{for } (8.2 \times 10^{-3} \leq t < T_{\text{CUTmax}}) \\ 0.85 & \text{for } (T_{\text{CUTmax}} \leq t) \end{array} \right\}_A \quad (145-17)$$

$$I_{\text{PSEUT-Type4-2P}}(t) = \left\{ \begin{array}{ll} 50 & \text{for } (0 \leq t < 10 \times 10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10 \times 10^{-6} \leq t < 8.2 \times 10^{-3}) \\ 1.75 & \text{for } (8.2 \times 10^{-3} \leq t < T_{\text{CUTmax}}) \\ 1.3 & \text{for } (T_{\text{CUTmax}} \leq t < 4) \\ I_{\text{LPS-2P}} & \text{for } (4 \leq t) \end{array} \right\}_A \quad (145-18)$$

where

- $t$  is the duration in seconds that the PSE sources  $I_{\text{Port-2P}}$
- $K$  is  $0.025 \text{ A}^2\text{s}$ , an energy limitation constant for the pairset current when it is not in steady state normal operation
- $T_{\text{CUTmax}}$  is  $T_{\text{CUTmax}}$  per pairset, as defined in Table 145-16
- $I_{\text{LPS-2P}}$  is the current defined in 145.2.10.13

The PSE lowerbound templates,  $I_{\text{PSELT-Type3-2P}}$  and  $I_{\text{PSELT-Type4-2P}}$ , are defined by the following segments:

$$I_{\text{PSELT-Type3-2P}}(t) = \left\{ \begin{array}{ll} I_{\text{LIM-2Pmin}} & \text{for } (0 \leq t < T_{\text{LIMmin}}) \\ I_{\text{Peak-2P}} & \text{for } (T_{\text{LIMmin}} \leq t < T_{\text{CUTmin}}) \\ I_{\text{Con-2P}} & \text{for } (T_{\text{CUTmin}} \leq t) \end{array} \right\}_A \quad (145-19)$$

$$I_{\text{PSELT-Type4-2P}}(t) = \left\{ \begin{array}{ll} I_{\text{LIM-2Pmin}} & \text{for } (0 \leq t < T_{\text{LIMmin}}) \\ I_{\text{Peak-2P}} & \text{for } (T_{\text{LIMmin}} \leq t < T_{\text{CUTmin}}) \\ I_{\text{Con-2P}} & \text{for } (T_{\text{CUTmin}} \leq t) \end{array} \right\}_A \quad (145-20)$$

where

- $t$  is the duration that the PI sources  $I_{\text{Port-2P}}$
- $I_{\text{LIM-2Pmin}}$  is the  $I_{\text{LIM-2Pmin}}$  value per pairset for the PSE as defined in Table 145-16
- $T_{\text{LIMmin}}$  is  $T_{\text{LIMmin}}$  per pairset as defined in Table 145-16
- $T_{\text{CUTmin}}$  is  $T_{\text{CUTmin}}$  per pairset, as defined in Table 145-16
- $I_{\text{Peak-2P}}$  is the minimum peak current supported on each powered pair, as defined in Equation (145-12)
- $I_{\text{Con-2P}}$  is the minimum supported continuous current on each powered pair as defined in 145.2.10.6

#### 145.2.10.10 Turn off time

The specification for  $T_{\text{Off}}$  in Table 145–16 shall apply to the discharge time from  $V_{\text{Port\_PSE-2P min}}$  to  $V_{\text{Off}}$  of a pairset with a test resistor of 320 k $\Omega$  attached to that pairset. In addition, it is recommended that the pairset be discharged when operating voltage is not applied.  $T_{\text{Off}}$  ends when  $V_{\text{PSE}} \leq V_{\text{Off}}$ .

#### 145.2.10.11 Turn off voltage

The voltage at the PI shall be equal or less than  $V_{\text{Off}}$ , as defined in Table 145–16, when the PSE is in DISABLED, IDLE, BACKOFF, or ERROR\_DELAY. The voltage at the corresponding pairset shall be equal or less than  $V_{\text{Off}}$ , as defined in Table 145–16, when the PSE is in IDLE\_PRI, WAIT\_PRI, ERROR\_DELAY\_PRI, IDLE\_SEC, WAIT\_SEC, or ERROR\_DELAY\_SEC.

#### 145.2.10.12 Intra-pair current unbalance

The PSE shall support an intra-pair current unbalance of  $I_{\text{unb}}$ , as defined in Equation (145–21). The intra-pair current unbalance is the current unbalance between the two conductors of a power pair over the current load range.

$$I_{\text{unb}} = \{ 3\% \times I_{\text{Peak-2P-unb\_max}} \}_A \quad (145-21)$$

A 100BASE-TX transmitter in a Type 3 or Type 4 Endpoint PSE shall meet the requirements of 25.4.5 in the presence of  $(I_{\text{unb}} / 2)$ .

#### 145.2.10.13 Type power

$P_{\text{Type min}}$  is the minimum power a PSE is capable of sourcing.

Type 4 PSEs shall not source more power than  $P_{\text{Type max}}$ , as defined in Table 145–16, measured using a sliding window with a width up to 4 seconds.  $I_{\text{LPS-2P}}$  is defined in Equation (145–22) and is the maximum current per pairset that results in less than  $P_{\text{Type max}}$  being sourced by the PSE.

$$I_{\text{LPS-2P}} = \left\{ \begin{array}{ll} 0.85 & \text{when in 2-pair mode} \\ \min \left( \frac{P_{\text{Type max}}}{V_{\text{PSE}}} - I_{\text{Port-2P-other}}, 1.3 \right) & \text{when in 4-pair mode} \end{array} \right\}_A \quad (145-22)$$

where

$P_{\text{Type max}}$  is the maximum power allowed for a given Type as defined in Table 145–16  
 $V_{\text{PSE}}$  is the voltage across the pairset at the PSE PI as defined in 145.1.3  
 $I_{\text{Port-2P-other}}$  is the output current on the other pairset (see 145.2.10.6)

**145.2.10.14 Power turn on time**

The specification for  $T_{\text{pon}}$  in Table 145–16 applies to the PSE power up time for a PD after completion of detection.

PSEs, when connected to a single-signature PD, shall reach POWER\_ON within  $T_{\text{pon}}$  after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach the respective power on state for a pairset within  $T_{\text{pon}}$  after completing detection on the same pairset.

**145.2.10.15 Error delay timing**

$T_{\text{ed}}$ , defined in Table 145–16, is the minimum delay time before a PSE may attempt subsequent powering of a pairset after power removal from that pairset because of an error condition.

**145.2.10.16 PSE stability**

When connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33A for PSE design guidelines for stable operation.

**145.2.11 Power supply allocation**

A PSE does not initiate power provision to one or both pairsets if the PSE has less than Class 3 power available and the connected PD requests more than the available power.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See 145.5 for a description of Data Link Layer classification.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

**145.2.12 PSE Maintain Power Signature (MPS) requirements**

A PSE removes power when a connected PD no longer draws a minimum amount of current. This is referred to as the “Maintain Power Signature.” The PSE state diagrams in Figure 145–17 and Figure 145–18 monitor for the absence of MPS.

A PSE, depending on the PD assigned Class and PD signature configuration, shall use the applicable  $I_{\text{Hold}}$ ,  $I_{\text{Hold-2P}}$ ,  $T_{\text{MPS}}$  and  $T_{\text{MPDO}}$  values as defined in Table 145–16. The specification for  $T_{\text{MPS}}$  in Table 145–16 applies only to the DC MPS component.

A PSE powering a PD over a single pairset

- Shall consider the DC MPS component to be present if  $I_{\text{Port-2P}}$  is greater than or equal to  $I_{\text{Hold-2P max}}$  continuously for a minimum of  $T_{\text{MPS}}$ .
- Shall consider the DC MPS component to be absent if  $I_{\text{Port-2P}}$  is less than or equal to  $I_{\text{Hold-2P min}}$ .
- May consider the DC MPS component to be either present or absent if  $I_{\text{Port-2P}}$  is in the range of  $I_{\text{Hold-2P}}$ .

- Shall remove power from the PI when DC MPS has been absent for a duration greater than  $T_{MPDO}$ .
- Shall not remove power from the PI when DC MPS has been present within the  $T_{MPS} + T_{MPDO}$  window. This allows a PD to minimize its power consumption.

A PSE powering a single-signature PD over both pairsets

- Shall consider the DC MPS component to be present if  $I_{Port-2P}$  of the pairset with the highest current is greater than or equal to  $I_{Hold-2P} \text{ max}$  and  $I_{Port}$  is greater than or equal to  $I_{Hold} \text{ max}$  continuously for a minimum of  $T_{MPS}$ .
- Shall consider the DC MPS component to be absent if  $I_{Port-2P}$  of the pairset with the highest current is less than or equal to  $I_{Hold-2P} \text{ min}$  and  $I_{Port}$  is less than or equal to  $I_{Hold} \text{ min}$ .
- May consider the DC MPS component to be either present or absent if  $I_{Port-2P}$  of the pairset with the highest current is within the range of  $I_{Hold-2P}$  or  $I_{Port}$  is within the range of  $I_{Hold}$ .
- Shall remove power from the PI when DC MPS has been absent for a duration greater than  $T_{MPDO}$ .
- Shall not remove power from the PI when DC MPS has been present within the  $T_{MPS} + T_{MPDO}$  window. This allows a PD to minimize its power consumption.

NOTE—The DC MPS requirements for PSEs connected to a single-signature PD are such that the PSE may measure either the total current over both pairsets ( $I_{Hold}$ ), the current on the pairset with the highest current ( $I_{Hold-2P}$ ), or both.

A PSE powering a dual-signature PD over both pairsets

- Shall consider the DC MPS component to be present or absent on each pairset independently.
- Shall consider the DC MPS component to be present on a pairset if  $I_{Port-2P}$  is greater than or equal to  $I_{Hold-2P} \text{ max}$  continuously for a minimum of  $T_{MPS}$ .
- Shall consider the DC MPS component to be absent on a pairset if  $I_{Port-2P}$  is less than or equal to  $I_{Hold-2P} \text{ min}$ .
- May consider the DC MPS component on a pairset to be either present or absent if  $I_{Port-2P}$  is within the range of  $I_{Hold-2P}$ .
- Shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than  $T_{MPDO}$ .
- Shall not remove power from a pairset when DC MPS has been present on both pairsets within the  $T_{MPS} + T_{MPDO}$  window.
- May maintain power on a pairset when DC MPS has been present on that pairset within the  $T_{MPS} + T_{MPDO}$  window. This allows a PD to minimize its power consumption.

### 145.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a PD may have the ability to draw power from an alternate power source. A PD requiring power from the PI may simultaneously draw power from an alternate power source. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

Additional electrical specifications that apply to the PD are specified in 145.4.

**145.3.1 PD Type descriptions**

PDs can be categorized as either Type 1, Type 2, Type 3, or Type 4. See 33.3 for the specification of Type 1 and Type 2 PDs. PDs can be implemented as either a single-signature configuration or a dual-signature configuration as defined in 1.4 and 145.3.5 and shown in Table 145–19. Table 145–19 shows the supported parameters of PDs.

**Table 145–19—PD supported parameters**

| PD Type                                                                                                                                                                                                                                                                                                                     | Signature configuration | PD Class | Physical Layer classification | Data Link Layer classification | Optional Capabilities |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|----------|-------------------------------|--------------------------------|-----------------------|
| Type 3                                                                                                                                                                                                                                                                                                                      | Single                  | 1 to 3   | Multiple-Event                | Optional                       | Autoclass             |
|                                                                                                                                                                                                                                                                                                                             |                         | 4 to 6   | Multiple-Event                | Mandatory                      | Autoclass             |
|                                                                                                                                                                                                                                                                                                                             | Dual                    | 1 to 3   | Multiple-Event                | Optional                       | —                     |
|                                                                                                                                                                                                                                                                                                                             |                         | 4        | Multiple-Event                | Mandatory                      | —                     |
| Type 4                                                                                                                                                                                                                                                                                                                      | Single                  | 7 to 8   | Multiple-Event                | Mandatory                      | Autoclass             |
|                                                                                                                                                                                                                                                                                                                             | Dual                    | 5        | Multiple-Event                | Mandatory                      | —                     |
| NOTE 1—See Table 145–26 and Table 145–27 for the allowed PD power for each Type and Class.<br>NOTE 2—Data Link Layer classification for dual-signature PDs is optional only if the PD requested Class on both Modes is less than or equal to 3.<br>NOTE 3—Type 4 dual-signature PDs request Class 5 on at least one pairset |                         |          |                               |                                |                       |

**145.3.2 PD PI**

The PD's PI consists of 8 conductors. The two conductors associated with a pair are at the same nominal voltage. A pairset consists of two pairs, as defined in 145.2.4. The two pairsets are named Mode A and Mode B, which correspond with Alternative A and Alternative B. Figure 145–12 in conjunction with Table 145–20 illustrate the two power modes.

PDs shall be capable of accepting power in any valid 2-pair configuration and any valid 4-pair configuration as defined in Table 145–20.

A PD shall meet the requirements of detection (145.3.4), PD signature configuration (145.3.5), and PD classification (145.3.6) in any valid 2-pair configuration, as defined in Table 145–20.

NOTE—This includes configurations with two pairs connected to the same positive potential and one pair connected to the negative potential.

A single-signature PD shall meet all specifications related to current by meeting the specified total current, where total current is the combined current of the two pairs at the same polarity, unless otherwise noted (see 145.3.8.9). A dual-signature PD shall meet all specifications related to current by meeting the specified current on the negative pair of a given Mode, unless otherwise noted (see 145.3.8.9).

The PD shall be insensitive to the polarity of the voltage applied on each Mode regardless of the polarity of the voltage applied on the other Mode. Single-signature PDs that request Class 4 or less shall be able to operate if power is supplied with any valid configuration defined in Table 145–20. All other PDs may require being supplied with a valid 4-pair configuration to operate at their nominal power level.

NOTE—PDs that support only Mode A or Mode B are specifically not allowed by this standard. PDs that are sensitive to polarity are specifically not allowed by this standard.

PDs interoperate with Type 1, Type 2, Type 3, and Type 4 PSEs, subject to power limitations. See 145.3.6.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V applied to the PD PI per any of the valid configurations defined in Table 145–20 indefinitely without permanent damage.

**Table 145–20—PD input power configurations**

| Pairsets                                                                                                                                                                                                                                                                                                                                       | Mode A                      |         | Mode B  |         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------|---------|---------|
| Pairs                                                                                                                                                                                                                                                                                                                                          | Pair 1                      | Pair 2  | Pair 3  | Pair 4  |
| Conductor                                                                                                                                                                                                                                                                                                                                      | 1 and 2                     | 3 and 6 | 4 and 5 | 7 and 8 |
|                                                                                                                                                                                                                                                                                                                                                | Valid 2-pair configurations |         |         |         |
|                                                                                                                                                                                                                                                                                                                                                | P                           | N       | —       | —       |
|                                                                                                                                                                                                                                                                                                                                                | N                           | P       | —       | —       |
|                                                                                                                                                                                                                                                                                                                                                | —                           | —       | P       | N       |
|                                                                                                                                                                                                                                                                                                                                                | —                           | —       | N       | P       |
|                                                                                                                                                                                                                                                                                                                                                | P                           | N       | P       | —       |
|                                                                                                                                                                                                                                                                                                                                                | P                           | N       | —       | P       |
|                                                                                                                                                                                                                                                                                                                                                | N                           | P       | P       | —       |
|                                                                                                                                                                                                                                                                                                                                                | N                           | P       | —       | P       |
|                                                                                                                                                                                                                                                                                                                                                | P                           | —       | P       | N       |
|                                                                                                                                                                                                                                                                                                                                                | —                           | P       | P       | N       |
|                                                                                                                                                                                                                                                                                                                                                | P                           | —       | N       | P       |
|                                                                                                                                                                                                                                                                                                                                                | —                           | P       | N       | P       |
|                                                                                                                                                                                                                                                                                                                                                | Valid 4-pair configurations |         |         |         |
|                                                                                                                                                                                                                                                                                                                                                | N                           | P       | N       | P       |
|                                                                                                                                                                                                                                                                                                                                                | N                           | P       | P       | N       |
|                                                                                                                                                                                                                                                                                                                                                | P                           | N       | N       | P       |
|                                                                                                                                                                                                                                                                                                                                                | P                           | N       | P       | N       |
| N denotes a pair connected to negative potential<br>P denotes a pair connected to positive potential<br>— denotes a pair not connected to a supply rail<br>PSEs are required to switch the negative pairs, and may switch the positive pairs as defined in 145.4.1.1.1. This may lead to both positive pairs providing current in 2-pair mode. |                             |         |         |         |

**145.3.3 PD state diagrams**

The PD state diagrams specify the externally observable behavior of a PD.

**145.3.3.1 Conventions**

The notation used in the state diagram follows the conventions of state diagrams as described in 145.2.5.2.

**145.3.3.2 Mode designation**

Dual-signature PDs are implemented on Mode A and Mode B as defined in 145.3.2. Mode information is obtained by replacing the X in the desired variable or function with the letter of the Mode of interest. Modes are referred to in general as follows:

X

Generic Mode designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.

Values:

A: Mode A

B: Mode B

**145.3.3.3 Single-signature PD state diagrams**

Single-signature PDs shall provide the behavior of the state diagram shown in Figure 145–25 and Figure 145–26.

**145.3.3.3.1 Constants**

$I_{\text{Inrush\_PD\_max}}$

The maximum PD inrush current  $I_{\text{Inrush\_PD\_max}}$  (see Table 145–29)

$V_{\text{Off\_PD\_min}}$

The minimum PD off voltage  $V_{\text{Off\_PD\_min}}$  (see Table 145–29)

$V_{\text{Reset\_PD\_max}}$

The maximum PD reset voltage  $V_{\text{Reset\_PD\_max}}$  (see Table 145–25)

**145.3.3.3.2 Variables**

$I_{\text{Port}}$

is the total PD input current as defined in 145.1.3.

$\text{mdi\_power\_required}$

A variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the PI, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. This variable may be set by the PD at any time.

Values:

FALSE: PD functionality is disabled.

TRUE: PD functionality is enabled.

$\text{nopower}$

A variable that indicates the PD has been in POWEROFF, which indicates  $V_{\text{PD}}$  was below  $V_{\text{Off\_PD}}$  while being powered, since the last time  $V_{\text{PD}}$  was below  $V_{\text{Reset}}$  for at least  $T_{\text{Reset}}$ .

Values:

FALSE: The PD has not been in POWEROFF.

TRUE: The PD has been in POWEROFF.

**pd\_acs\_full\_power**

This variable indicates whether the PD is required to draw maximum power,  $P_{\text{Autoclass\_PD}}$ . See 145.3.6.2.

Values:

- FALSE: The PD is not required to draw maximum power.
- TRUE: The PD is required to draw maximum power for Autoclass measurement.

**pd\_acs\_req**

This variable indicates if a PD draws  $P_{\text{Autoclass\_PD}}$  in the Autoclass time window after reaching POWERED. See 145.3.6.2.

Values:

- FALSE: The PD does not request Autoclass.
- TRUE: The PD requests Autoclass.

**pd\_autoclass\_enable**

A variable indicating that the PD is enabled to perform Autoclass by changing its class signature to class signature 0 during the first class event (see 145.3.6.2).

Values:

- FALSE: Autoclass is disabled.
- TRUE: Autoclass is enabled.

**pd\_dll\_capable**

This variable indicates whether the PD implements Data Link Layer classification.

Values:

- FALSE: The PD does not implement Data Link Layer classification.
- TRUE: The PD does implement Data Link Layer classification.

**pd\_dll\_enable**

A variable indicating whether the Data Link Layer classification mechanism is enabled.

Values:

- FALSE: Data Link Layer classification is not enabled.
- TRUE: Data Link Layer classification is enabled.

**pd\_inrush\_lim**

A variable indicating that the PD limits the inrush current below  $I_{\text{Inrush\_PD}}$  and  $I_{\text{Inrush\_PD-2P}}$  for the duration of the PD inrush time as defined in 145.3.8.3. This variable is set per this description.

Values:

- FALSE: The PD does not limit the inrush current.
- TRUE: The PD does limit the inrush current.

**pd\_max\_power**

A variable indicating the maximum power that the PD may draw from the PSE. See power classifications in Table 145–29.

Values:

- inrush: There is no maximum power limit on the PD
- 0: The PD may draw up to 44 mA of current
- 1: PD may draw Class 1 power
- 2: PD may draw Class 2 power
- 3: PD may draw Class 3 power
- 4: PD may draw Class 4 power
- 5: PD may draw Class 5 power
- 6: PD may draw Class 6 power
- 7: PD may draw Class 7 power
- 8: PD may draw Class 8 power

**pd\_overload**

A variable that indicates if the PD is drawing peak power in excess of  $P_{\text{Class\_PD}}$ , as defined in 145.3.8.4, or when the PD is exposed to a transient condition as defined in 145.3.8.6.

Values:

- FALSE: The PD is not drawing peak power or is exposed to a transient condition.

TRUE: The PD is drawing peak power and is not exposed to a transient condition.

pd\_power\_update  
A variable that is set when the PDMaxPowerValue in the DLL state diagram in Figure 145–44 has been updated.  
Values:  
FALSE: The value of PDMaxPowerValue has not changed.  
TRUE: The value of PDMaxPowerValue has changed.

pd\_req\_class  
A variable indicating the PD requested Class.  
Values:  
1: The PD requests Class 1.  
2: The PD requests Class 2.  
3: The PD requests Class 3.  
4: The PD requests Class 4.  
5: The PD requests Class 5.  
6: The PD requests Class 6.  
7: The PD requests Class 7.  
8: The PD requests Class 8.

pd\_reset  
An implementation-specific variable that unconditionally resets the PD state diagram to OFFLINE. This variable may be set by the PD at any time.  
Values:  
FALSE: The device has not been reset.  
TRUE: The device has been reset.

PDAutoclassRequest  
A variable output by the PD power control state diagram indicating whether the PD requests Autoclass via the Data Link Layer. See 145.5.  
Values:  
FALSE: The PD does not request an Autoclass measurement to be performed.  
TRUE: The PD requests an Autoclass measurement to be performed.

present\_class\_sig\_0  
Controls presenting the class signature ‘0’ during  $T_{ACS}$  of the first class event (see 145.3.6.2).  
Values:  
FALSE: Class signature 0 is not to be applied to the PI.  
TRUE: Class signature 0 is to be applied to the PI.

present\_class\_sig\_A  
Controls presenting the class signature that is used during first two class events (see 145.3.6) by the PD.  
Values:  
FALSE: The class signature corresponding with class\_sig\_A is not to be applied to the PI.  
TRUE: The class signature corresponding with class\_sig\_A is to be applied to the PI.

present\_class\_sig\_B  
Controls presenting the class signature that is used during the third class event and all subsequent class events (see 145.3.6) by the PD.  
Values:  
FALSE: The class signature corresponding with class\_sig\_B is not to be applied to the PI.  
TRUE: The class signature corresponding with class\_sig\_B is to be applied to the PI.

present\_det\_sig  
Controls presenting the detection signature (see 145.3.4) by the PD.  
Values:  
invalid: A non-valid PD detection signature is to be applied to both pairsets.  
valid: A valid PD detection signature is to be applied to both pairsets.  
either: Either a valid or non-valid PD detection signature may be applied to each pairset.

**present\_mark\_sig**

Controls presenting the mark event current and impedance (see 145.3.6.1.1) by the PD.

Values:

- FALSE: The PD does not present mark event behavior.  
TRUE: The PD does present mark event behavior.

**present\_mps**

Controls applying the Maintain Power Signature MPS (see 145.3.9) to the PI.

Values:

- FALSE: The MPS is not to be applied to the PI.  
TRUE: The MPS is to be applied to the PI.

**pse\_assigned\_class**

A variable that indicates the assigned Class. This variable is initially set by Physical Layer classification and may be updated through DLL classification.

Values:

- 1: Class 1  
2: Class 2  
3: Class 3  
4: Class 4  
5: Class 5  
6: Class 6  
7: Class 7  
8: Class 8

**pse\_power\_level**

A variable that indicates to the PD the level of power the PSE is supplying.

Values:

- 3: The PSE has allocated the PD requested Class or Class 3 power, whichever is less.  
4: The PSE has allocated Class 4 power.  
6: The PSE has allocated the PD requested Class or Class 6 power, whichever is less.  
8: The PSE has allocated the PD requested Class or Class 8 power, whichever is less.

**V<sub>Mark\_th</sub>**

Mark event voltage threshold (see Table 145–25)

**V<sub>Off\_PD</sub>**

PD power supply turn off voltage (see Table 145–29)

**V<sub>On\_PD</sub>**

PD power supply turn on voltage (see Table 145–29)

**V<sub>PD</sub>**

Voltage at the PD PI as defined in 145.1.3.

**V<sub>Reset\_th</sub>**

Reset voltage threshold (see Table 145–25)

**145.3.3.3.3 Timers**

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x\_timer” is asserted.

**tacspd\_timer**

A timer used to change the classification current to class signature ‘0’ when a PD uses Autoclass; see T<sub>ACS</sub> in Table 145–28.

**tauto\_pd1\_timer**

A timer indicating maximum delay until start of Autoclass power draw. Applies to Autoclass requests by Physical Layer classification; see T<sub>AUTO\_PD1</sub> in 145.3.6.2.

**tauto\_pd2\_timer**

A timer indicating minimum delay until end of Autoclass power draw. Applies to Autoclass requests by Physical Layer classification; see  $T_{\text{AUTO\_PD2}}$  in 145.3.6.2.

**tinrushpdmax\_timer**

A timer used to determine when the PD exits INRUSH; see  $T_{\text{Inrush\_PD max}}$  in Table 145–29.

**tpowerdly\_timer**

A timer used to limit the PD's current and power draw from  $T_{\text{Inrush\_PD}}$  to  $T_{\text{delay}}$ ; see  $T_{\text{delay}}$  in Table 145–29.

**145.3.3.3.4 Functions****do\_class\_timing**

This function is used to evaluate the Type of PSE connected to the PI by measuring the length of the first class event. PDs that do not measure the length of the first class event return FALSE. The class event timing requirements are defined in Table 145–25. This function returns the following variable:

**long\_class\_event:** A variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 145.3.9) the PD should use. See 145.3.7.

Values:

**FALSE:** The PSE is identified as a Type 1 or Type 2 PSE, or the PD has not measured the length of the first class event.

**TRUE:** The PSE is identified as a Type 3 or Type 4 PSE.

**do\_initialize**

This function returns the following variables (see 145.3.3.3.2):

**pd\_autoclass\_enable**

**pd\_req\_class**

**pd\_dll\_capable**

**do\_update\_pse\_assigned\_class**

A function that updates the **pse\_assigned\_class** based on the value of **PDMaxPowerValue** as defined in Table 145–23. This function returns the following variable:

**pse\_assigned\_class:** See **pse\_assigned\_class** defined in 145.3.3.3.2.

## 145.3.3.3.5 State diagrams

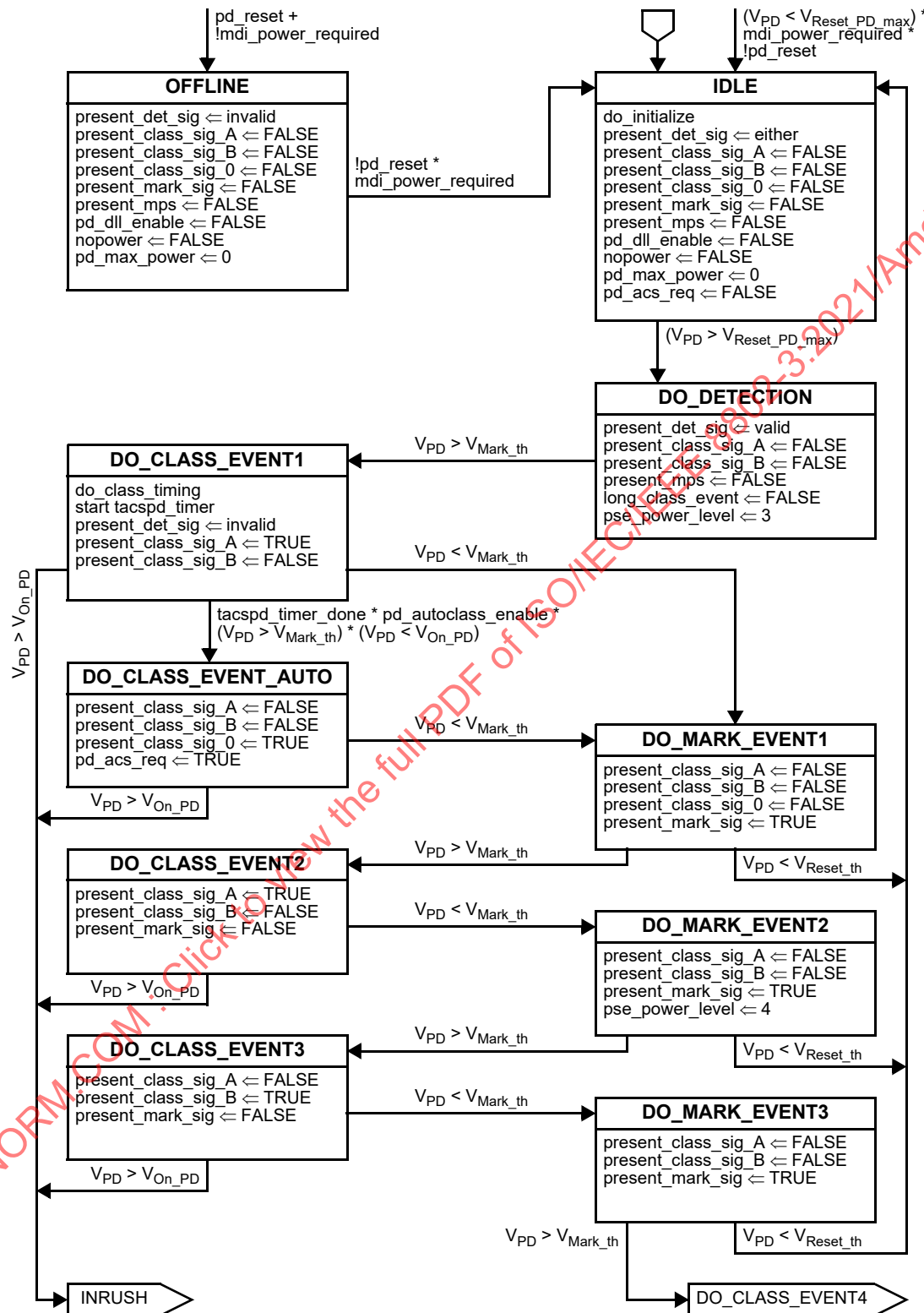


Figure 145–25—Single-signature PD state diagram

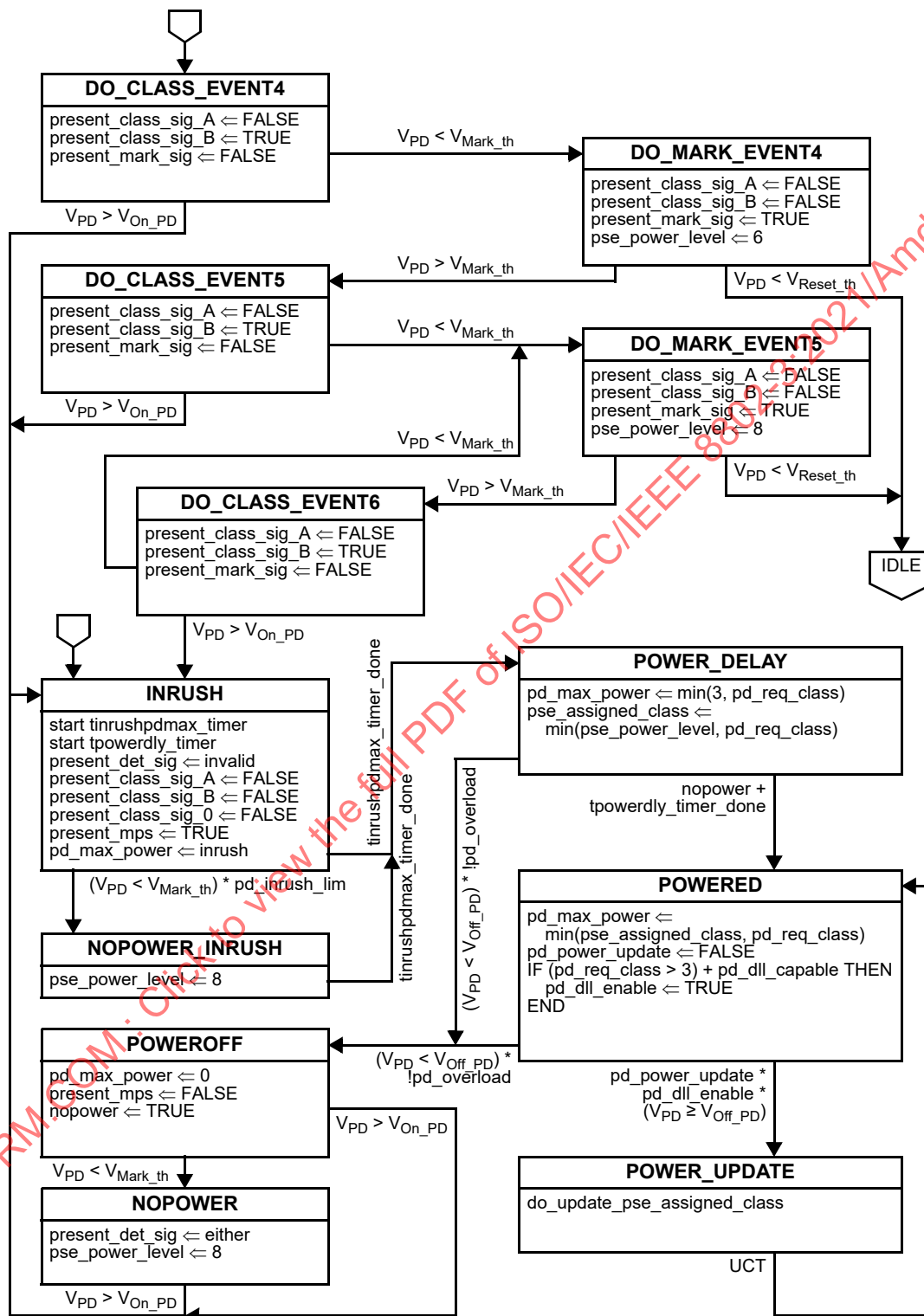


Figure 145–25—Single-signature PD state diagram (continued)

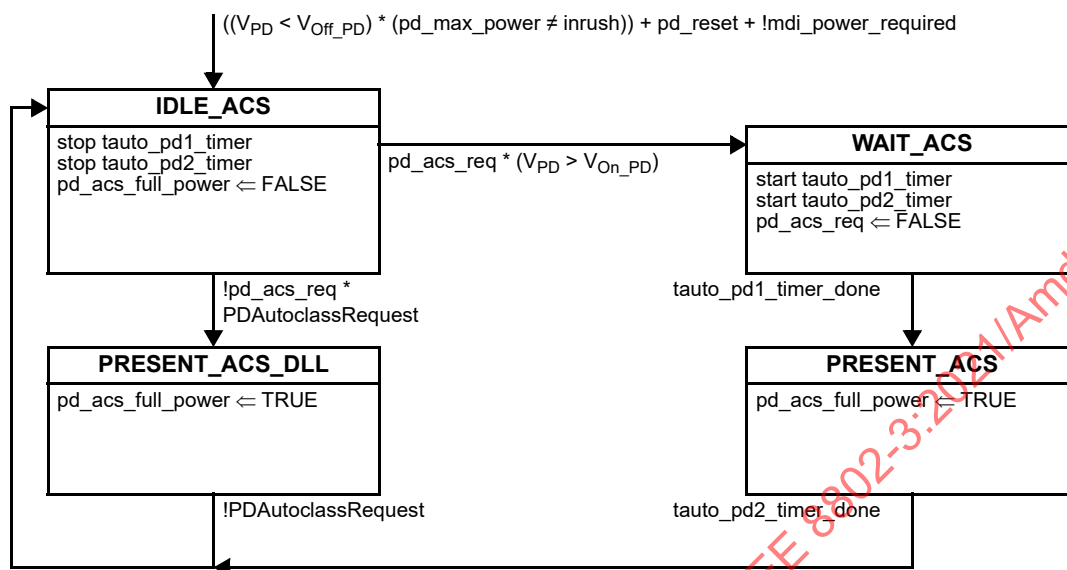


Figure 145-26—Single-signature PD Autoclass state diagram

NOTE 1—DO\_CLASS\_EVENT6 creates a defined behavior for a Type 3 or Type 4 PD that is brought into the classification range more than 5 times.

NOTE 2—In general, there is no requirement for a PD to respond with a valid class signature for any DO\_CLASS\_EVENT duration less than  $T_{Class\_PD}$  as defined in Table 145-25.

#### 145.3.3.4 Dual-signature PD state diagram

Dual-signature PDs shall provide the behavior of the state diagram shown in Figure 145-27 over each pairset independently unless otherwise specified. All the parameters that apply to Mode A and Mode B are denoted with the suffix “\_mode(X)” where “X” can be “A” or “B”. A parameter that ends with the suffix “\_mode(X)” may have different values for Mode A and Mode B in the independent state diagrams.

##### 145.3.3.4.1 Constants

$I_{Inrush\_PD\_2P\_max}$

The maximum inrush current per pairset  $I_{Inrush\_PD-2P\_max}$  (see Table 145-29)

$V_{Off\_PD\_min}$

The minimum PD off voltage  $V_{Off\_PD\_min}$  (see Table 145-29)

$V_{Reset\_PD\_max}$

The maximum PD reset voltage  $V_{Reset\_PD\_max}$  (see Table 145-25)

##### 145.3.3.4.2 Variables

$I_{Port\_2P\_mode(X)}$

Is the current on the negative pair ( $I_{Port-2P}$ ) of the Mode X pairset; see 145.1.3.

$mdi\_power\_required$

A variable indicating that the PD is enabled and should request power from the PSE by applying a PD detection signature, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. This variable may be set by the PD at any time.

Values:

- FALSE: PD functionality is disabled.  
TRUE: PD functionality is enabled.

**no\_power\_mode(X)**

A variable that indicates the PD has been in POWEROFF on Mode X, which indicates  $V_{PD}$  was below  $V_{Off\_PD}$  while being powered, since the last time  $V_{PD}$  was below  $V_{Reset}$  for at least  $T_{Reset}$ .

Values:

- FALSE: The PD has not been in POWEROFF.  
TRUE: The PD has been in POWEROFF.

**pd\_dll\_capable**

This variable indicates whether the PD implements Data Link Layer classification.

Values:

- FALSE: The PD does not implement Data Link Layer classification.  
TRUE: The PD does implement Data Link Layer classification.

**pd\_dll\_enable**

A variable indicating whether the Data Link Layer classification mechanism is enabled.

Values:

- FALSE: Data Link Layer classification is not enabled.  
TRUE: Data Link Layer classification is enabled.

**pd\_inrush\_lim\_mode(X)**

A variable indicating that the PD limits the inrush current on Mode X below  $I_{Inrush\_PD-2P}$  for the duration of the PD inrush time as defined in 145.3.8.3. This variable is set per this description.

Values:

- FALSE: The PD does not limit the inrush current on Mode X.  
TRUE: The PD does limit the inrush current on Mode X.

**pd\_max\_power\_mode(X)**

A variable indicating the maximum power that the PD may draw from the PSE on Mode X. See power classifications in Table 145–29.

Values:

- inrush: There is no maximum power limit  
0: The PD may draw up to 44 mA of current  
1: The PD may draw Class 1 power  
2: The PD may draw Class 2 power  
3: The PD may draw Class 3 power  
4: The PD may draw Class 4 power  
5: The PD may draw Class 5 power

**pd\_overload\_mode(X)**

A variable that indicates if the PD is drawing peak power in excess of  $P_{Class\_PD}$ , as defined in 145.3.8.4, or when the PD is exposed to a transient condition as defined in 145.3.8.6, on Mode X.

Values:

- FALSE: The PD is not drawing peak power or is exposed to a transient condition.  
TRUE: The PD is drawing peak power and is not exposed to a transient condition.

**pd\_power\_update\_mode(X)**

A variable that is set when the  $PDMaxPowerValue\_mode(X)$  in the DLL state diagram in Figure 145–46 or Figure 145–47 has been updated.

Values:

- FALSE: The value of  $PDMaxPowerValue\_mode(X)$  has not changed.  
TRUE: The value of  $PDMaxPowerValue\_mode(X)$  has changed.

**pd\_req\_class\_mode(X)**

A constant indicating the PD requested Class on Mode X

Values:

- 1: The PD requests Class 1.  
2: The PD requests Class 2.

- 3: The PD requests Class 3.
- 4: The PD requests Class 4.
- 5: The PD requests Class 5.

**pd\_reset\_mode(X)**

An implementation-specific variable that unconditionally resets the PD state diagram on Mode X to OFFLINE. This variable may be set by the PD at any time.

Values:

- FALSE: The device has not been reset.
- TRUE: The device has been reset.

**present\_class\_sig\_A\_mode(X)**

Controls presenting the class signature that is used during first two class events (see 145.3.6) by the PD on Mode X.

Values:

- FALSE: The class signature corresponding with class\_sig\_A is not to be applied to the pairset.
- TRUE: The class signature corresponding with class\_sig\_A is to be applied to the pairset.

**present\_class\_sig\_B\_mode(X)**

Controls presenting the class signature that is used during the third class event and all subsequent class events (see 145.3.6) by the PD on Mode X.

Values:

- FALSE: The class signature corresponding with class\_sig\_B is not to be applied to the pairset.
- TRUE: The class signature corresponding with class\_sig\_B is to be applied to the pairset.

**present\_det\_sig\_mode(X)**

Controls presenting the detection signature (see 145.3.4) by the PD on Mode X.

Values:

- invalid: A non-valid PD detection signature is to be applied to the pairset on Mode X.
- valid: A valid PD detection signature is to be applied to the pairset on Mode X.
- either: Either a valid or non-valid PD detection signature may be applied to the pairset.

**present\_mark\_sig\_mode(X)**

Controls presenting the mark event current and impedance (see 145.3.6.1.1) by the PD on Mode X.

Values:

- FALSE: The PD does not present mark event behavior.
- TRUE: The PD does present mark event behavior.

**present\_mps\_mode(X)**

Controls applying MPS (see 145.3.9) to the PD's PI on Mode X.

Values:

- FALSE: The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
- TRUE: The MPS is to be applied to the PD's PI.

**pse\_assigned\_class\_mode(X)**

A variable (generated by the PD) that indicates the PSE assigned Class on Mode X to the PD. This variable is initially set by Physical Layer classification and may be updated through DLL classification.

Values:

- 1: Class 1.
- 2: Class 2.
- 3: Class 3.
- 4: Class 4.
- 5: Class 5.

**pse\_power\_level\_mode(X)**

A variable that indicates to the PD the level of power the PSE is supplying on Mode X.

Values:

- 3: The PSE has allocated the PD requested Class or Class 3 power, whichever is less.
- 4: The PSE has allocated Class 4 power.
- 5: The PSE has allocated Class 5 power.

$V_{\text{Mark\_th}}$   
Mark event voltage threshold (see Table 145–25)

$V_{\text{Off\_PD}}$   
PD power supply turn off voltage (see Table 145–29)

$V_{\text{On\_PD}}$   
PD power supply turn on voltage (see Table 145–29)

$V_{\text{PD\_mode(X)}}$   
 $V_{\text{PD}}$  of the Mode X pairset; see 145.1.3.

$V_{\text{Reset\_th}}$   
Reset voltage threshold (see Table 145–25)

#### 145.3.3.4.3 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x\_timer” is asserted.

$\text{tinrushpdmax\_timer\_mode(X)}$   
A timer used to determine when the PD exits INRUSH on Mode X; see  $T_{\text{Inrush\_PD max}}$  in Table 145–29.

$\text{tpowerdly\_timer\_mode(X)}$   
A timer used to limit the PD’s current and power draw on Mode X from  $T_{\text{Inrush\_PD}}$  to  $T_{\text{delay}}$ ; see  $T_{\text{delay}}$  in Table 145–29.

#### 145.3.3.4.4 Functions

$\text{do\_class\_timing\_mode(X)}$   
This function is used by a PD to evaluate the Type of PSE connected to the pairset by measuring the length of the class event on Mode X. The class event timing requirements are defined in Table 145–25. This function returns the following variable:

$\text{long\_class\_event\_mode(X)}$ : A variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 145.3.9) the PD should use. See 145.3.7.

Values:

- FALSE: The PSE is identified as a Type 1 or Type 2 PSE.
- TRUE: The PSE is identified as a Type 3 or Type 4 PSE.

$\text{do\_initialize\_mode(X)}$   
This function returns the following variables (see 145.3.3.4.2):

$\text{pd\_req\_class\_mode(X)}$

$\text{pd\_dll\_capable}$

$\text{do\_update\_pse\_assigned\_class\_mode(X)}$

A function that updates the  $\text{pse\_assigned\_class\_mode(X)}$  based on the value of  $\text{PDMaxPowerValue\_mode(X)}$  as defined in Table 145–23. This function returns the following variable:

$\text{pse\_assigned\_class\_mode(X)}$ : See  $\text{pse\_assigned\_class\_mode(X)}$  defined in 145.3.3.4.2.

#### 145.3.3.4.5 State diagram

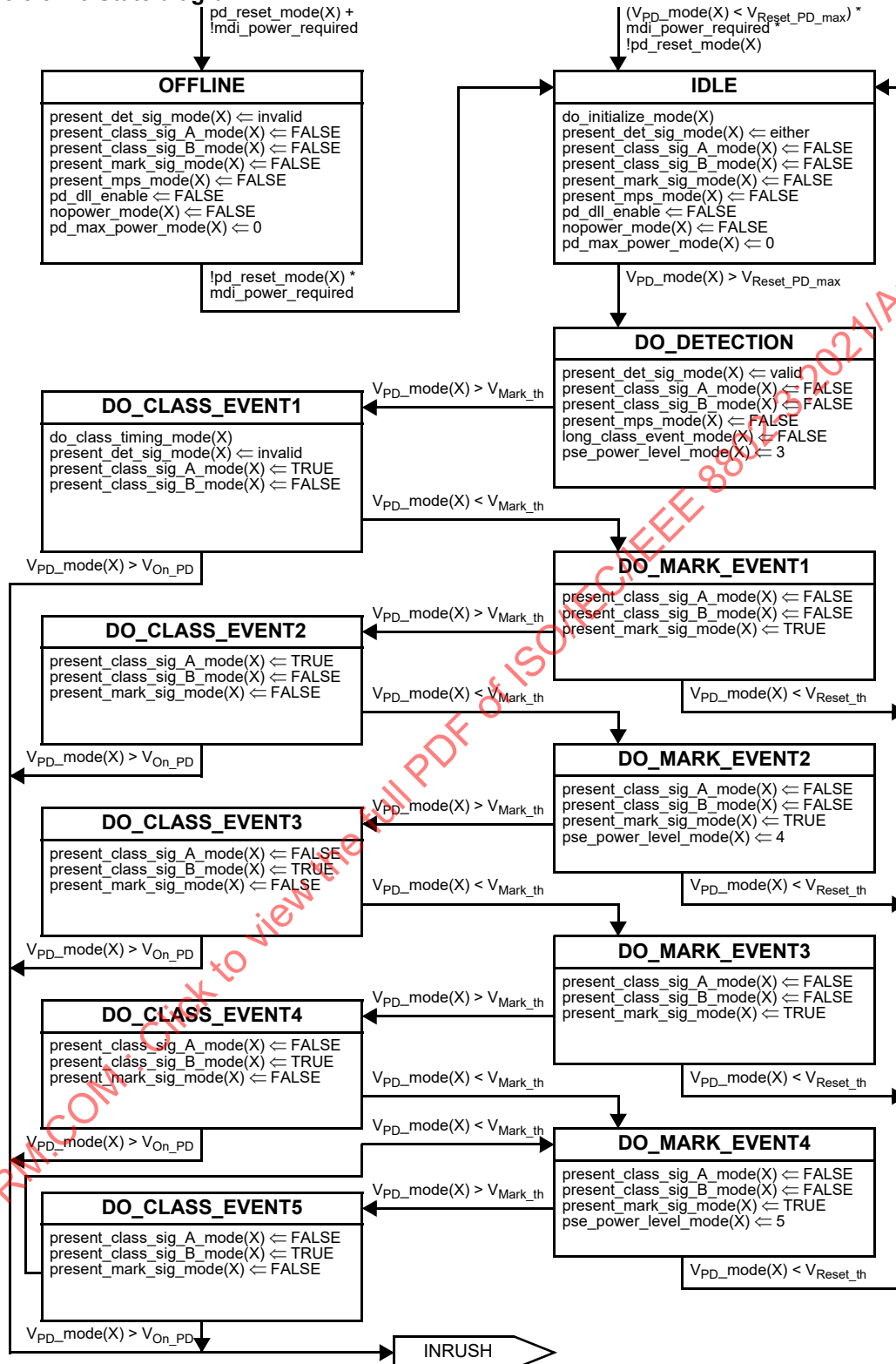


Figure 145–27—Dual-signature PD state diagram

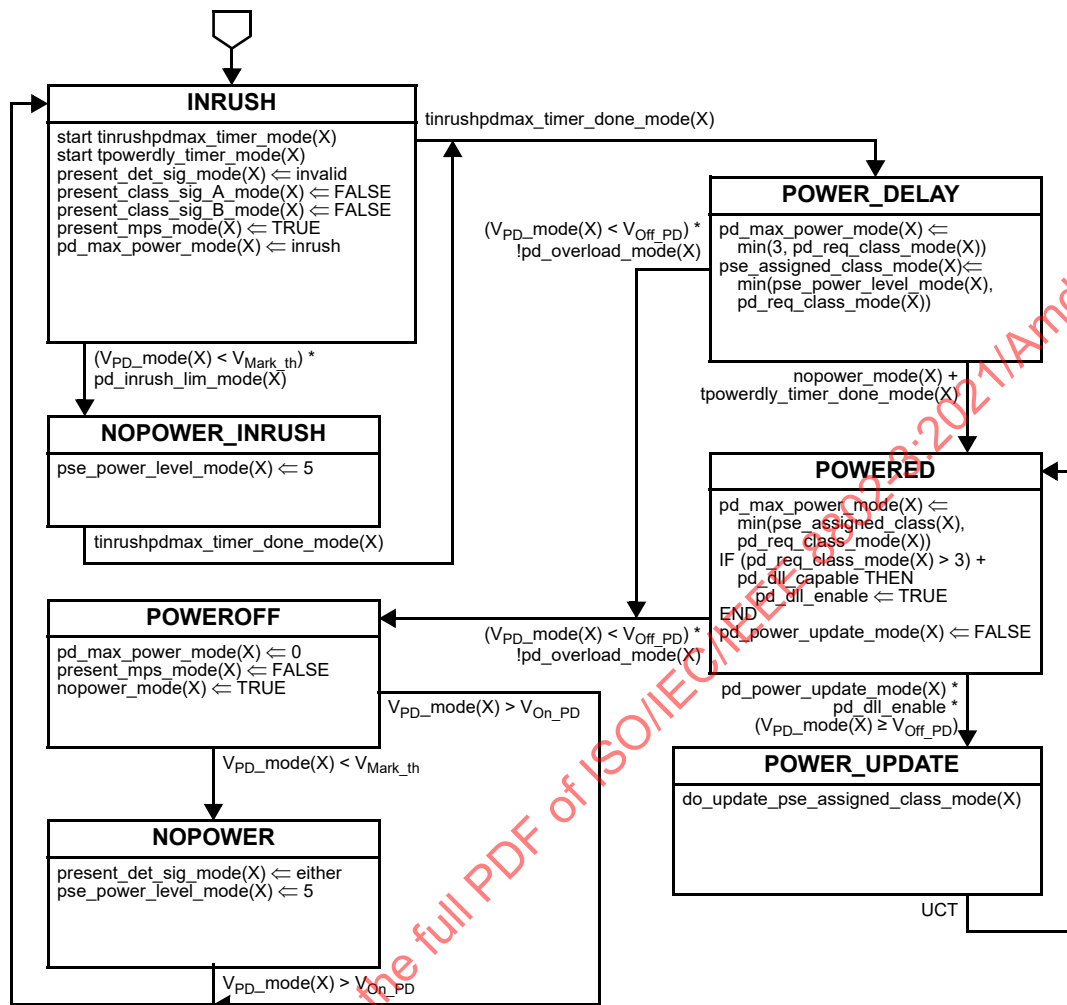


Figure 145-27—Dual-signature PD state diagram (*continued*)

#### 145.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature when it is in DO\_DETECTION per Figure 145-25 or Figure 145-27. See 145.3.5.

A PD presents a non-valid detection signature on both pairsets while it is in a state where it does not accept power via the PI per Figure 145-25 or Figure 145-27.

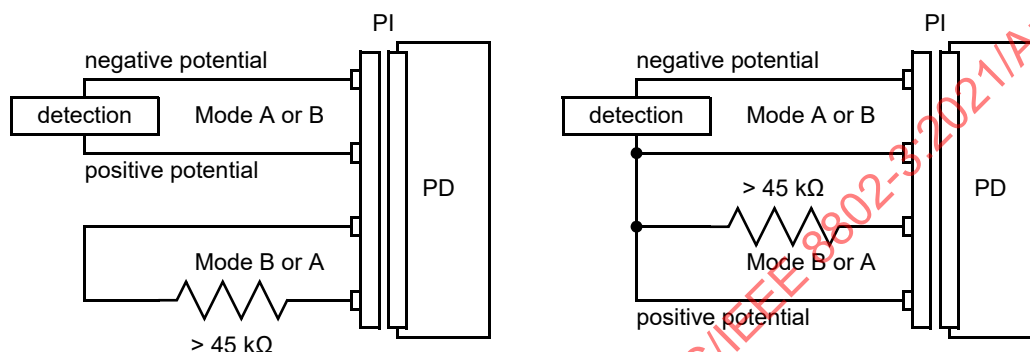
A PD presents a non-valid detection signature when in a mark event state per Figure 145-25 or Figure 145-27.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive  $V_{PD}$  and Negative  $V_{PD}$  of PD Mode A and PD Mode B as defined in 145.3.2.

While a PD presents a valid detection signature on a given Mode, that detection signature shall be valid when presented under each of the following conditions (see Figure 145–28):

- With any resistance greater than 45 kΩ across the other Mode
- With any resistance greater than 45 kΩ across the other Mode and one pair of the other Mode connected to the positive potential of the given Mode

A single-signature PD that is powered over only one pairset shall present a non-valid detection signature on the unpowered pairset. A dual-signature PD that is powered over only one pairset shall present a valid detection signature on the unpowered pairset.



**Figure 145–28—Detection signature requirements connection configurations**

A PD may or may not present a valid detection signature when in IDLE.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process as defined in Equation (145–23).

$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \quad (145-23)$$

where

$V_1$  and  $V_2$  are the first and second voltage measurements made at the PD PI, respectively  
 $I_1$  and  $I_2$  are the first and second current measurements made at the PD PI, respectively  
 $R_{\text{detect}}$  is the effective resistance

A valid PD detection signature shall have the characteristics of Table 145–21.

A non-valid detection signature shall have one or both of the characteristics in Table 145–22.

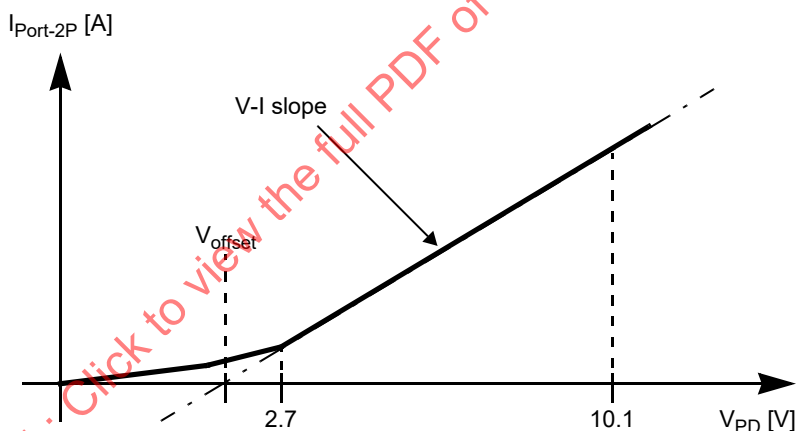
A PD that presents a detection signature outside of Table 145–21 is non-compliant, while a PD that presents the signature of Table 145–22 is assured to fail detection.

**Table 145–21—Valid PD detection signature characteristics, measured at the PD PI**

| Parameter                                                                                | Conditions                             | Min  | Max  | Unit          | Additional information |
|------------------------------------------------------------------------------------------|----------------------------------------|------|------|---------------|------------------------|
| $R_{\text{detect}}$<br>(at any 1 V or greater chord within the voltage range conditions) | 2.7 V to 10.1 V                        | 23.7 | 26.3 | k $\Omega$    | —                      |
| $V_{\text{offset}}$                                                                      | —                                      | 0    | 1.9  | V             | See Figure 145–29      |
| Voltage at the PI                                                                        | $I_{\text{Port-2P}} = 124 \mu\text{A}$ | 2.7  | —    | V             | —                      |
| Input capacitance                                                                        | 2.7 V to 10.1 V                        | 0.05 | 0.12 | $\mu\text{F}$ | —                      |
| Series input inductance                                                                  | 2.7 V to 10.1 V                        | —    | 100  | $\mu\text{H}$ | —                      |

**Table 145–22—Non-valid PD detection signature characteristics, measured at PD PI**

| Parameter           | Conditions                       | Range of values                        | Unit          |
|---------------------|----------------------------------|----------------------------------------|---------------|
| $R_{\text{detect}}$ | $V_{\text{PD}} < 10.1 \text{ V}$ | Either greater than 45 or less than 12 | k $\Omega$    |
| Input capacitance   | $V_{\text{PD}} < 10.1 \text{ V}$ | Greater than 10                        | $\mu\text{F}$ |

**Figure 145–29—Valid PD detection signature offset**

### 145.3.5 PD signature configurations

A single-signature PD shall present a valid detection signature, as defined in Table 145–21, on a given Mode when no voltage or current is applied across the other Mode, and shall not present a valid detection signature on the given Mode when any voltage in the range of 3.7 V to 57 V is applied across the other Mode or any current greater than 124  $\mu\text{A}$  is drawn from the negative pair of the other Mode. These requirements apply to both Mode A and Mode B.

NOTE—A valid detection signature meets every requirement in Table 145–21 across all specified conditions. A failure under any allowed condition is considered “not a valid signature.”

A dual-signature PD shall present a valid detection signature, as defined in Table 145–21, on a given Mode, regardless of any voltage between 0 V and 57 V applied to the other Mode. This requirement applies to both Mode A and Mode B.

These requirements allow the PD to be correctly identified by a PSE performing connection check as defined in 145.2.7.

### 145.3.6 PD classification

A PD may be classified by the PSE based on Physical Layer classification, Data Link Layer (DLL) classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used by the PSE and the PD to mutually identify the Type of the device to which they are connected.

See 145.2.8 for a general description of classification mechanisms. See 145.2.8.2 and 145.3.6.2 for a description of the optional Autoclass mechanism.

The requested Class of the PD is the Class the PD advertises during Physical Layer classification. It represents the amount of power the PD requires for operation. The PD shall draw no more power across any voltage in the range of  $V_{\text{Port PD-2P}}$  than defined for the requested Class in Table 145–26 and Table 145–27. Up to 3 class events may be required to discover the requested Class of the PD.

Depending on the number of class events produced by the PSE, the assigned Class is equal to or lower than the PD requested Class. The PD shall conform to the assigned Class, regardless of its requested Class. After a successful DLL classification, the assigned Class changes depending on the value of PDMaxPowerValue for single-signature PDs and PDMaxPowerValue\_mode(X) for dual-signature PDs, as defined in Table 145–23.

**Table 145–23—Relation of assigned Class and DLL**

| Single-signature |                | Dual-signature          |                          |
|------------------|----------------|-------------------------|--------------------------|
| PDMaxPowerValue  | Assigned Class | PDMaxPowerValue_mode(X) | Assigned Class on Mode X |
| 1 to 39          | 1              | 1 to 39                 | 1                        |
| 40 to 65         | 2              | 40 to 65                | 2                        |
| 66 to 130        | 3              | 66 to 130               | 3                        |
| 131 to 255       | 4              | 131 to 255              | 4                        |
| 256 to 400       | 5              | 256 to 499              | 5                        |
| 401 to 510       | 6              |                         |                          |
| 511 to 620       | 7              |                         |                          |
| 621 to 999       | 8              |                         |                          |

PDs shall provide Multiple-Event Physical Layer classification as defined in 145.3.6.1.

Single-signature PDs that request Class 1, 2, or 3 may provide Data Link Layer classification (see 145.5). Single-signature PDs that request Class 4 or higher and dual-signature PDs that request Class 4 or higher on at least one of its Modes shall provide DLL classification.

PD classification behavior shall conform to the state diagram in Figure 145–25 or Figure 145–27, and shall conform to the electrical specifications defined in Table 145–24 and Table 145–25.

A PD that is assigned to a Class lower than the Class it requested shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

#### 145.3.6.1 PD Multiple-Event class signature

The response of the PD to Multiple-Event Physical Layer classification consists of two class signatures, class\_sig\_A and class\_sig\_B as described by Table 145–26 or Table 145–27.

PDs shall present class\_sig\_A during DO\_CLASS\_EVENT1 and DO\_CLASS\_EVENT2 and class\_sig\_B during DO\_CLASS\_EVENT3, DO\_CLASS\_EVENT4, DO\_CLASS\_EVENT5, and DO\_CLASS\_EVENT6, as shown in Figure 145–25 and Figure 145–27, with the corresponding classification signatures specified in Table 145–24. PDs implementing Autoclass shall present class signature 0, as defined in Table 145–24, during DO\_CLASS\_EVENT\_AUTO as defined in 145.3.6.2.

After entering a DO\_CLASS\_EVENT state, the PD Physical Layer class signature shall be valid within  $T_{\text{Class\_PD}}$  as defined in Table 145–25 and remain valid for the remainder of the class event.

$V_{\text{Reset\_PD}}$ , as defined in Table 145–25, is the voltage range in which the PD remains in IDLE.

Single-signature PDs shall advertise class signatures according to the PD Type and PD requested Class, as defined in Table 145–26. For single-signature PDs, the PD requested Class on either pairset is the maximum amount of power requested by the PD.

NOTE—Requested Class 0 is not defined for Type 3 PDs. A Type 1 PD that does not implement Physical Layer classification requests Class 0, with a power level equivalent to Class 3. Such PDs are assigned to Class 3 by Type 3 and Type 4 PSEs.

Dual-signature PDs shall advertise class signatures according to the PD Type and PD requested Class on each pairset, as defined in Table 145–27. For dual-signature PDs, the PD requested Class on a pairset is the maximum amount of power requested by the PD on that pairset. Dual-signature PDs may advertise different class signatures on each pairset. A dual-signature PD that is powered over only one pairset shall present a valid class signature on the unpowered pairset.

After a successful Multiple-Event Physical Layer classification has completed, a single-signature PD sets the pse\_power\_level variable to either 3, 4, 6 or 8. Based on the value of pse\_power\_level and the PD requested Class, pd\_req\_class, the assigned Class is derived in the variable pse\_assigned\_class.

After a successful Multiple-Event Physical Layer classification has completed, a dual-signature PD sets the pse\_power\_level\_mode(X) variable to either 3, 4, or 5. Based on the value of pse\_power\_level\_mode(X) and the PD requested Class, pd\_req\_class\_mode(X), the assigned Class is derived in the variable pse\_assigned\_class\_mode(X).

**Table 145–24—Class signatures generated at the PD PI**

| Parameter                     | Conditions       | Minimum | Maximum | Unit |
|-------------------------------|------------------|---------|---------|------|
| Current for class signature 0 | 14.5 V to 20.5 V | 1       | 4       | mA   |
| Current for class signature 1 |                  | 9       | 12      |      |
| Current for class signature 2 |                  | 17      | 20      |      |
| Current for class signature 3 |                  | 26      | 30      |      |
| Current for class signature 4 |                  | 36      | 44      |      |

**Table 145–25—Multiple-Event Physical Layer classification electrical requirements**

| Item | Parameter                        | Symbol                 | Units | Min  | Max  | Additional information |
|------|----------------------------------|------------------------|-------|------|------|------------------------|
| 1    | Class event voltage              | $V_{\text{Class\_PD}}$ | V     | 14.5 | 20.5 |                        |
| 2    | Mark event voltage               | $V_{\text{Mark\_PD}}$  | V     | 6.9  | 10.1 | —                      |
| 3    | Mark event current               | $I_{\text{Mark}}$      | mA    | 0.25 | 4    | See 145.3.6.1.1        |
| 4    | Mark event threshold             | $V_{\text{Mark\_th}}$  | V     | 10.1 | 14.5 | See 145.3.6.1.1        |
| 5    | Classification reset threshold   | $V_{\text{Reset\_th}}$ | V     | 2.81 | 6.9  | See 145.3.6.1.1        |
| 6    | Classification reset voltage     | $V_{\text{Reset\_PD}}$ | V     | 0    | 2.81 | See 145.3.6.1          |
| 7    | Long first class event timing    | $T_{\text{LCE\_PD}}$   | ms    | 75.5 | 87.5 | See 145.3.7            |
| 8    | PD classification stability time | $T_{\text{Class\_PD}}$ | ms    | —    | 5    | See 145.3.6.1          |

**Table 145–26—Physical Layer classifications and Multiple Event Responses for single-signature PDs**

| PD Type | Requested Class | class_sig_A<br>class signature | class_sig_B<br>class signature | Requested power (W) |
|---------|-----------------|--------------------------------|--------------------------------|---------------------|
| 3       | 1               | 1                              | 1                              | 3.84                |
|         | 2               | 2                              | 2                              | 6.49                |
|         | 3               | 3                              | 3                              | 13                  |
|         | 4               | 4                              | 4                              | 25.5                |
|         | 5               | 4                              | 0                              | 40                  |
|         | 6               | 4                              | 1                              | 51                  |
| 4       | 7               | 4                              | 2                              | 62                  |
|         | 8               | 4                              | 3                              | 71.3                |

NOTE 1—See Table 145–24 for definition of class signatures 0 to 4.

NOTE 2—PDs may be assigned to a lower Class than the PD requested Class, which results in a lower value of  $P_{\text{Class\_PD}}$ .

**Table 145–27—Physical Layer classifications and Multiple Event Responses for dual-signature PDs**

| PD Type                                                                                                                                                                                                      | Requested Class per pairset | class_sig_A class signature | class_sig_B class signature | Requested power (W) |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----------------------------|-----------------------------|---------------------|
| 3                                                                                                                                                                                                            | 1                           | 1                           | 0                           | 3.84                |
|                                                                                                                                                                                                              | 2                           | 2                           | 0                           | 6.49                |
|                                                                                                                                                                                                              | 3                           | 3                           | 0                           | 13                  |
|                                                                                                                                                                                                              | 4                           | 4                           | 0                           | 25.5                |
| 4                                                                                                                                                                                                            | 5                           | 4                           | 3                           | 35.6                |
| NOTE 1—See Table 145–24 for definition of class signatures 0 to 4.<br>NOTE 2—PDs may be assigned to a lower Class than the PD requested Class, which results in a lower value of $P_{\text{Class\_PD-2P}}$ . |                             |                             |                             |                     |

**145.3.6.1.1 Mark Event behavior**

When the PD is presenting a mark event signature in a DO\_MARK\_EVENT state, as shown in the state diagram of Figure 145–25 and Figure 145–27, the PD shall draw  $I_{\text{Mark}}$  as defined in Table 145–25 and present a non-valid detection signature as defined in Table 145–22.

The PD shall not exceed the  $I_{\text{Mark}}$  current limits when voltage at the PI enters the  $V_{\text{Mark\_PD}}$  specification as defined in Table 145–25.

$V_{\text{Mark\_th}}$  is the PI voltage threshold at which the PD transitions into, and one of the voltage thresholds to transition out of, the DO\_CLASS\_EVENT states as shown in Figure 145–25 and Figure 145–27.

Implementations should employ appropriate methods (such as hysteresis in  $V_{\text{Mark\_th}}$ ) to avoid erroneous transitions between class and mark states when the PSE switches from a class voltage to a mark voltage or vice versa.

$V_{\text{Reset\_th}}$  is the PI voltage threshold at which the PD transitions from a DO\_MARK\_EVENT state to IDLE as shown in Figure 145–25 and Figure 145–27.

**145.3.6.2 Autoclass (optional)**

Single-signature PDs may choose to implement an extension of Physical Layer classification known as Autoclass. Autoclass is only defined for single-signature PDs. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. See 145.2.8.2.

A PD that implements Autoclass shall change its current during the first class event to class signature 0 no earlier than  $T_{\text{ACS min}}$  and no later than  $T_{\text{ACS max}}$ , as defined in Table 145–28.

After power up, a PD that implements Autoclass shall draw its highest required power,  $P_{\text{Autoclass\_PD}}$ , subject to the requirements on  $P_{\text{Class\_PD}}$  in 145.3.8.2, throughout the period bounded by  $T_{\text{AUTO\_PD1}}$  and  $T_{\text{AUTO\_PD2}}$ , measured from when  $V_{\text{PD}}$  rises above  $V_{\text{On\_PD}}$ . The PD is restricted to a maximum power draw of  $P_{\text{Autoclass\_PD}}$  until the PD successfully negotiates a higher power level through Data Link Layer classification as defined in 145.5.

**Table 145–28—Autoclass PD timing requirements**

| Item | Parameter                       | Symbol          | Units | Min  | Max  | Additional Information                               |
|------|---------------------------------|-----------------|-------|------|------|------------------------------------------------------|
| 1    | Autoclass signature timing      | $T_{ACS}$       | ms    | 75.5 | 87.5 | Measured from transition to DO_CLASS_EVENT1          |
| 2    | Autoclass power draw start time | $T_{AUTO\_PD1}$ | ms    | —    | 1350 | Measured from when $V_{PD}$ rises above $V_{On\_PD}$ |
| 3    | Autoclass power draw end time   | $T_{AUTO\_PD2}$ | ms    | 3650 | —    |                                                      |

**145.3.7 PSE Type identification**

PDs may determine the Type of the PSE they are connected to by measuring the duration of the first class event. Such a PD may set `long_class_event` to TRUE if the first class event is longer than  $T_{LCE\_PD}$  min and shall set `long_class_event` to TRUE if the first class event is longer than  $T_{LCE\_PD}$  max. If `long_class_event` is FALSE, this indicates the PSE is a Type 1 or Type 2 PSE. If `long_class_event` is TRUE this indicates the PSE is a Type 3 or Type 4 PSE. This determination allows the PD to make use of short MPS to reduce standby power.

**145.3.8 PD power**

The PD shall operate within the characteristics in Table 145–29.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

**Table 145–29—PD power supply limits**

| Item | Parameter                                           | Symbol            | Unit | Min  | Max | Additional information     |
|------|-----------------------------------------------------|-------------------|------|------|-----|----------------------------|
| 1    | Input DC voltage per pairset per the assigned Class |                   |      |      |     |                            |
|      | Class 1                                             | $V_{Port\_PD-2P}$ | V    | 42.8 | 57  | See 145.3.8.1, Table 145–1 |
|      | Class 2                                             |                   |      | 42   |     |                            |
|      | Class 3                                             |                   |      | 39.9 |     |                            |
|      | Class 4                                             |                   |      | 42.5 |     |                            |
|      | Class 5, single-signature PD                        |                   |      | 44.3 |     |                            |
|      | Class 5, dual-signature PD                          |                   |      | 41.1 |     |                            |
|      | Class 6                                             |                   |      | 42.5 |     |                            |
|      | Class 7                                             |                   |      | 42.9 |     |                            |
|      | Class 8                                             |                   |      | 41.1 |     |                            |
| 2    | Transient operating input voltage per pairset       | $V_{Tran\_PD-2P}$ | V    | 36   | —   | See 145.3.8.6              |

Table 145–29—PD power supply limits (*continued*)

| Item | Parameter                                                                            | Symbol                     | Unit | Min  | Max  | Additional information                            |
|------|--------------------------------------------------------------------------------------|----------------------------|------|------|------|---------------------------------------------------|
| 3    | Input voltage range during overload for a single-signature PD per the assigned Class |                            |      |      |      | See 145.3.8.4                                     |
|      | Class 1 to 6                                                                         | $V_{\text{Overload-2P}}$   | V    | 39.4 | —    |                                                   |
|      | Class 7 to 8                                                                         |                            |      | 40.4 | —    |                                                   |
|      | Input voltage range during overload for a dual-signature PD per the assigned Class   |                            |      |      |      |                                                   |
|      | Class 1 to 4                                                                         | $V_{\text{Overload-2P}}$   | V    | 39.4 | —    |                                                   |
|      | Class 5                                                                              |                            |      | 40.4 | —    |                                                   |
| 4    | Input inrush current for a single-signature PD per the assigned Class                |                            |      |      |      | See 145.3.8.3                                     |
|      | Class 1 to 6                                                                         | $I_{\text{Inrush\_PD}}$    | A    | —    | 0.4  |                                                   |
|      | Class 7 to 8                                                                         |                            |      | —    | 0.8  |                                                   |
| 5    | Input inrush current per pairset per the assigned Class                              |                            |      |      |      | See 145.3.8.3                                     |
|      | Single-signature PD, Class 1 to 6                                                    | $I_{\text{Inrush\_PD-2P}}$ | A    | —    | 0.4  |                                                   |
|      | Single-signature PD, Class 7 to 8                                                    |                            |      | —    | 0.6  |                                                   |
|      | Dual-signature PD, Class 1 to 5                                                      |                            |      | —    | 0.4  |                                                   |
| 6    | Inrush to PD current control delay                                                   | $T_{\text{Inrush\_PD}}$    | ms   | —    | 50   | See 145.3.8.3                                     |
| 7    | Inrush to operating state delay                                                      | $T_{\text{delay}}$         | ms   | 80   | —    | See 145.3.8.3                                     |
| 8    | Input average power for single-signature PDs per the assigned Class                  |                            |      |      |      | See 145.3.8.2, 145.3.6, Table 145–1, Table 145–26 |
|      | Class 1                                                                              | $P_{\text{Class\_PD}}$     | W    | —    | 3.84 |                                                   |
|      | Class 2                                                                              |                            |      | —    | 6.49 |                                                   |
|      | Class 3                                                                              |                            |      | —    | 13   |                                                   |
|      | Class 4                                                                              |                            |      | —    | 25.5 |                                                   |
|      | Class 5                                                                              |                            |      | —    | 40   |                                                   |
|      | Class 6                                                                              |                            |      | —    | 51   |                                                   |
|      | Class 7                                                                              |                            |      | —    | 62   |                                                   |
|      | Class 8                                                                              |                            |      | —    | 71.3 |                                                   |
| 9    | Input average power for a pairset for dual-signature PDs per the assigned Class      |                            |      |      |      | See 145.3.8.2, 145.3.6, Table 145–1, Table 145–27 |
|      | Class 1                                                                              | $P_{\text{Class\_PD-2P}}$  | W    | —    | 3.84 |                                                   |
|      | Class 2                                                                              |                            |      | —    | 6.49 |                                                   |
|      | Class 3                                                                              |                            |      | —    | 13   |                                                   |
|      | Class 4                                                                              |                            |      | —    | 25.5 |                                                   |
|      | Class 5                                                                              |                            |      | —    | 35.6 |                                                   |

Table 145–29—PD power supply limits (*continued*)

| Item | Parameter                                                                        | Symbol                   | Unit                 | Min | Max                          | Additional information      |
|------|----------------------------------------------------------------------------------|--------------------------|----------------------|-----|------------------------------|-----------------------------|
| 10   | Peak operating power for single-signature PDs per the assigned Class             |                          |                      |     |                              |                             |
|      | Class 1                                                                          | $P_{\text{Peak\_PD}}$    | W                    | —   | 5                            | See 145.3.8.4               |
|      | Class 2                                                                          |                          |                      | —   | 8.36                         |                             |
|      | Class 3                                                                          |                          |                      | —   | 14.4                         |                             |
|      | Class 4                                                                          |                          |                      | —   | 28.3                         |                             |
|      | Class 5                                                                          |                          |                      | —   | 42                           |                             |
|      | Class 6                                                                          |                          |                      | —   | 53.5                         |                             |
|      | Class 7                                                                          |                          |                      | —   | 65.1                         |                             |
|      | Class 8                                                                          |                          |                      | —   | 74.9                         |                             |
| 11   | Peak operating power for a pairset for dual-signature PDs per the assigned Class |                          |                      |     |                              |                             |
|      | Class 1                                                                          | $P_{\text{Peak\_PD-2P}}$ | W                    | —   | 5                            | See 145.3.8.4               |
|      | Class 2                                                                          |                          |                      | —   | 8.36                         |                             |
|      | Class 3                                                                          |                          |                      | —   | 14.4                         |                             |
|      | Class 4                                                                          |                          |                      | —   | 28.3                         |                             |
|      | Class 5                                                                          |                          |                      | —   | 37.4                         |                             |
| 12   | Input current slew rate                                                          | $I_{\text{Slewrte}}$     | mA/<br>$\mu\text{s}$ | —   | 4.7                          | See 145.3.8.5               |
| 13   | Single-signature PD capacitance while in INRUSH, POWER_DELAY, or POWERED         |                          |                      |     |                              |                             |
|      | Class 1 to 4                                                                     | $C_{\text{Port}}$        | $\mu\text{F}$        | 5   | —                            | See 145.3.8.3,<br>145.3.8.6 |
|      | Class 5 to 6                                                                     |                          |                      | 10  | —                            |                             |
|      | Class 7 to 8                                                                     |                          |                      | 20  | —                            |                             |
| 14   | Dual-signature PD pairset capacitance while in INRUSH, POWER_DELAY, or POWERED   |                          |                      |     |                              |                             |
|      | Class 1 to 4                                                                     | $C_{\text{Port-2P}}$     | $\mu\text{F}$        | 5   | —                            | See 145.3.8.3,<br>145.3.8.6 |
|      | Class 5                                                                          |                          |                      | 10  | —                            |                             |
| 15   | Ripple and noise                                                                 |                          |                      |     |                              |                             |
|      | < 500 Hz                                                                         | $V_{\text{Noise\_PD}}$   | $V_{\text{pp}}$      | —   | 0.5                          | See 145.3.8.7               |
|      | 500 Hz to 150 kHz                                                                |                          |                      | —   | 0.2                          |                             |
|      | 150 kHz to 500 kHz                                                               |                          |                      | —   | 0.15                         |                             |
|      | 500 kHz to 1 MHz                                                                 |                          |                      | —   | 0.1                          |                             |
| 16   | PD power supply turn on voltage                                                  | $V_{\text{On\_PD}}$      | V                    | 30  | 42                           | See 145.3.8.1               |
| 17   | PD power supply turn off voltage                                                 | $V_{\text{Off\_PD}}$     | V                    | 30  | $V_{\text{Port\_PD-2P min}}$ | See 145.3.8.1               |
| 18   | Reflected voltage                                                                | $V_{\text{refl}}$        | V                    | —   | 2.8                          | See 145.3.8.8               |

### 145.3.8.1 Input voltage

The specification for  $V_{\text{Port\_PD-2P}}$  in Table 145–29 is for the input voltage range after startup (see 145.3.8.3), and accounts for loss in the cabling plant.

The PD shall turn on at a voltage in the range of  $V_{\text{On\_PD}}$ . After the PD turns on, the PD shall stay on over the entire  $V_{\text{Port\_PD-2P}}$  range. After reaching POWER\_DELAY, the PD shall turn off at a voltage in the range of  $V_{\text{Off\_PD}}$ . For dual-signature PDs the requirements for  $V_{\text{On\_PD}}$  and  $V_{\text{Off\_PD}}$  apply to each pairset individually. A PD shall not turn off due to peak power draw, causing  $V_{\text{PD}}$  to go as low as  $V_{\text{Overload-2P}}$ , as specified in 145.3.8.4, or due to a voltage transient as defined in 145.3.8.6. This behavior is encoded in the variable `pd_overload` and `pd_overload_mode(X)`.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by  $V_{\text{Port\_PSE-2P min}}$  to  $V_{\text{Port\_PSE-2P max}}$  (as defined in Table 145–16):

- With a series resistance less than or equal to  $R_{\text{Ch}}$  for assigned Class 1 through 4 to a single-signature PD.
- With a series resistance less than or equal to  $R_{\text{Ch}} / 2$  for assigned Class 5 through 8 to a single-signature PD.
- With a series resistance less than or equal to  $R_{\text{Ch}}$  connected to a given Mode of a dual-signature PD.

$V_{\text{On\_PD min}}$  is set at 30 V to align with  $V_{\text{Off\_PD min}}$ . It is recommended that a PD implements hysteresis between  $V_{\text{On\_PD}}$  and  $V_{\text{Off\_PD}}$ .

When the PD is in POWEROFF and  $V_{\text{PD}}$  falls below  $V_{\text{Mark\_th}}$ , the PD transitions to NOPOWER and may show a valid or invalid detection signature, and may or may not draw mark current, draw any class current, and show MPS. Interoperability between PSE and PD is no longer guaranteed when nopower is TRUE or the PD has entered NOPOWER\_INRUSH since the last time  $V_{\text{PD}}$  was below  $V_{\text{Reset\_PD max}}$ .

### 145.3.8.2 Input average power

$P_{\text{Port\_PD}}$  is the average power drawn by a single-signature PD, measured using a sliding window with a width of 1 second.  $P_{\text{Port\_PD-2P}}$  is the average power drawn by a given Mode of a dual-signature PD, measured using a sliding window with a width of 1 second.

For single-signature PDs,  $P_{\text{Port\_PD}}$  shall not exceed  $P_{\text{Class\_PD}}$  for the assigned Class. For dual-signature PDs,  $P_{\text{Port\_PD-2P}}$  shall not exceed  $P_{\text{Class\_PD-2P}}$  for the assigned Class.

A PD that has enabled Autoclass during Physical Layer classification or has requested Autoclass through DLL, shall not draw more power than  $P_{\text{Autoclass\_PD}}$ , unless the PD successfully negotiates a different power level, up to the PD requested Class, through Data Link Layer classification as defined in 145.5.

$P_{\text{Class\_PD}}$  and  $P_{\text{Class\_PD-2P}}$  defined in Table 145–29 are determined per the assigned Class. The assigned PSE Class is determined by the number of class events and the PD requested Class, as shown in Table 145–11.  $P_{\text{Class\_PD}}$  is the maximum average PI power and applies to single-signature PDs.  $P_{\text{Class\_PD-2P}}$  is the maximum average power on a pairset and applies to dual-signature PDs.

PDs may dynamically adjust their maximum required operating power below  $P_{\text{Class\_PD}}$  or  $P_{\text{Class\_PD-2P}}$  as described in 145.5. PDs may also adjust their maximum required operating power below  $P_{\text{Class\_PD}}$  by using Autoclass (see 145.3.6.2).

Single-signature PDs that have successfully completed DLL classification shall not exceed a power consumption of `PDMaxPowerValue` as defined in 145.5.3.3.1. Dual-signature PDs that have successfully

completed DLL classification shall not exceed a power consumption of  $P_{\text{MaxPowerValue\_mode(X)}}$  on Mode X as defined in 145.5.3.4.2.

#### 145.3.8.2.1 Input average power exceptions

For single-signature PDs assigned to Class 8 and  $P_{\text{MaxPowerValue}}$  set to 713 or greater, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, the PD may consume greater than  $P_{\text{Class\_PD}}$  but shall not consume greater than  $P_{\text{Class}}$  at the PSE PI and shall not draw a total 4-pair current in excess of  $2 \times I_{\text{Cable}}$  as defined in Table 145–1.

For dual-signature PDs assigned to Class 5 and  $P_{\text{MaxPowerValue\_mode(X)}}$  set to 356 or greater, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, the PD may consume greater than  $P_{\text{Class\_PD-2P}}$  but shall not consume greater than  $P_{\text{Class-2P}}$  on the pairset at the PSE PI and shall not draw current in excess of  $I_{\text{Cable}}$  as defined in Table 145–1.

#### 145.3.8.2.2 System stability test conditions during startup and steady state operation

When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

Stable operation may be verified by confirming that the PD meets  $V_{\text{Noise\_PD}}$ , as defined in Table 145–29, when the PD is powered by a voltage source set in the range of  $V_{\text{Port\_PSE-2P}}$ , as defined in Table 145–16, through a series resistance of  $R_{\text{Ch}}$ , as defined in Table 145–1, and the PD is operating at or below  $P_{\text{Class\_PD}}$  or  $P_{\text{Class\_PD-2P}}$ .

#### 145.3.8.3 Input inrush current

The PD inrush time duration is defined as beginning with the application of input voltage at the PI when  $V_{\text{PD}}$  crosses the PD power supply turn on voltage,  $V_{\text{On\_PD}}$  as defined in Table 145–29, and ends after  $T_{\text{delay}}$ .

The inrush current is the initial current drawn by the PD, which is used to charge  $C_{\text{Port}}$  or  $C_{\text{Port-2P}}$ . A PD may limit the inrush current below  $I_{\text{Inrush\_PD}}$  and  $I_{\text{Inrush\_PD-2P}}$  to allow for large values of  $C_{\text{Port}}$  and  $C_{\text{Port-2P}}$ .

The PSE limits the inrush current to  $I_{\text{Inrush}}$  and  $I_{\text{Inrush-2P}}$ , for at least  $T_{\text{Inrush\_PD max}}$ , as defined in Table 145–16 and Table 145–29.

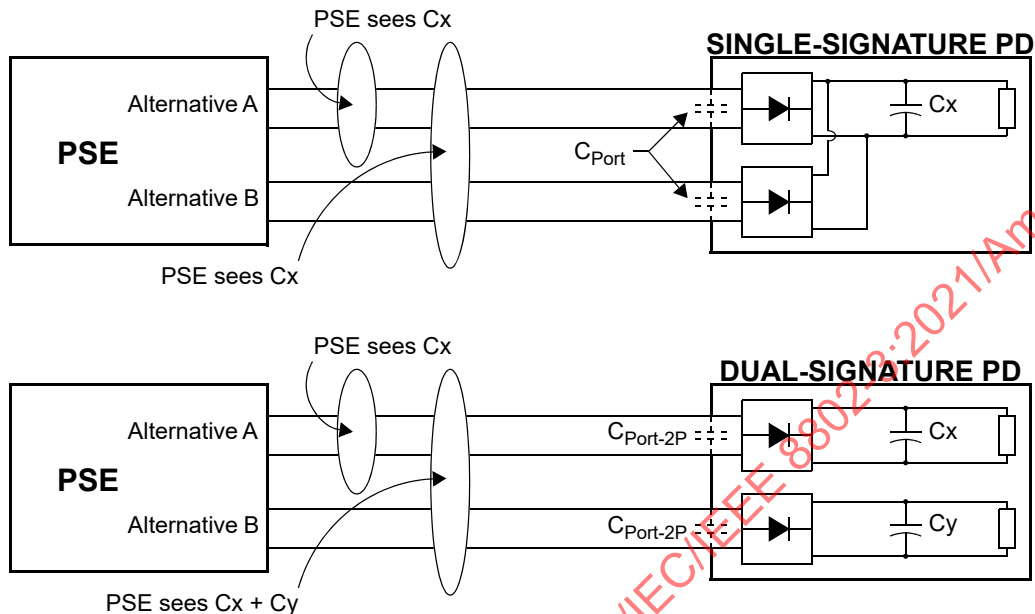
PDs shall draw less than  $I_{\text{Inrush\_PD}}$  and  $I_{\text{Inrush\_PD-2P}}$  from  $T_{\text{Inrush\_PD max}}$  until  $T_{\text{delay min}}$ , when connected to a source that meets the requirements of 145.2.10.7. This delay is required so that the PD does not enter a high power state before the PSE has had time to change the available current from the POWER\_UP to the POWER\_ON limits. A PD can meet this requirement by either having  $C_{\text{Port}}$  or  $C_{\text{Port-2P}}$  charged within  $T_{\text{Inrush\_PD max}}$  or by limiting the input inrush current.

Single-signature PDs assigned to Class 1, 2, or 3 shall conform to  $P_{\text{Class\_PD}}$  and  $P_{\text{Peak\_PD}}$  within  $T_{\text{Inrush\_PD max}}$  as defined in Table 145–29. Dual-signature PDs assigned to Class 1, 2, or 3 shall conform to  $P_{\text{Class\_PD-2P}}$  and  $P_{\text{Peak\_PD-2P}}$  within  $T_{\text{Inrush\_PD max}}$  as defined in Table 145–29 on that pairset.

NOTE—PDs may be subjected to PSE POWER\_ON current limits during inrush when the PD input voltage reaches 99% of steady state or after  $T_{\text{Inrush\_PD max}}$ . PD requirements are impacted by PSE current limits. See 145.2.10.7 for details.

$C_{\text{Port}}$  in Table 145–29 is the PD input capacitance during POWER\_UP and POWER\_ON that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD.  $C_{\text{Port-2P}}$  in Table 145–29 is the PD input capacitance during POWER\_UP\_PRI, POWER\_UP\_SEC, POWER\_ON\_PRI, and

POWER\_ON\_SEC that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure for a simplified PSE-PD  $C_{Port}$  and  $C_{Port-2P}$  interpretation model.



NOTE—The “dual-signature PD” in Figure represents a PD with two completely isolated circuits connected to Mode A and Mode B. The PSE will see a capacitance of  $C_x + C_y$ . A dual-signature PD can also be implemented with a single load, resulting in a lower than  $C_x + C_y$  capacitance value as seen by the PSE.

Figure 145-30— $C_{Port}$  interpretation model

#### 145.3.8.4 Peak operating power

$V_{Overload-2P}$  is the PD PI voltage when the PD is drawing the permissible  $P_{Peak\_PD}$  for single-signature PDs, or  $P_{Peak\_PD-2P}$  for dual-signature PDs.

At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for single-signature PDs shall not exceed  $P_{Class\_PD}$  for more than  $T_{CUT}$  min, as defined in Table 145-16 and 5% duty cycle.  $P_{Peak\_PD}$  is the maximum peak operating power and applies to single-signature PDs.

At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for a dual-signature PD shall not exceed  $P_{Class\_PD-2P}$  for more than  $T_{CUT}$  min, as defined in Table 145-16 and 5% duty cycle.  $P_{Peak\_PD-2P}$  is the maximum peak operating power on a pairset and applies to dual-signature PDs.

NOTE—The duty cycle of the peak current is measured using a sliding window with a width of 1 second.

Peak power is defined in Table 145-29 and depends on the Class assigned by the PSE. Equation (145-24) and Equation (145-25) are used to approximate the ratiometric peak powers of Class 1 through Class 8. These equations may be used to calculate  $P_{Peak\_PD}$  or  $P_{Peak\_PD-2P}$  after Data Link Layer classification and for Autoclass by substituting  $P_{MaxPowerValue}$  with the corresponding value of  $P_{Autoclass\_PD}$ .

$$P_{\text{Peak\_PD}} = \left\{ \begin{array}{l} 0.129 \times \text{PDMaxPowerValue} \text{ for assigned Class 1 and 2} \\ 0.111 \times \text{PDMaxPowerValue} \text{ for assigned Class 3 and 4} \\ 0.105 \times \text{PDMaxPowerValue} \text{ for assigned Class 5 to 8} \end{array} \right\}_w \quad (145-24)$$

$$P_{\text{Peak\_PD-2P}} = \left\{ \begin{array}{l} 0.129 \times \text{PDMaxPowerValue\_mode(X)} \text{ for assigned Class 1 and 2} \\ 0.111 \times \text{PDMaxPowerValue\_mode(X)} \text{ for assigned Class 3 and 4} \\ 0.105 \times \text{PDMaxPowerValue\_mode(X)} \text{ for assigned Class 5} \end{array} \right\}_w \quad (145-25)$$

where

PDMaxPowerValue is the actual maximum input average the PD may draw under the current power allocation; see 145.5.3.3.1  
PDMaxPowerValue\_mode(X) is the actual maximum input average the PD may draw under the current power allocation on Mode X; see 145.5.3.4.2

#### 145.3.8.4.1 Peak operating power exceptions

For single-signature PDs assigned to Class 8 and for dual-signature PDs assigned to Class 5, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, in any operating condition with any static voltage at the PI, the peak power shall not exceed maximum  $P_{\text{Port\_PD}}$  for single-signature PDs and maximum  $P_{\text{Port\_PD-2P}}$  for dual-signature PDs at the PSE PI for more than  $T_{\text{CUT}}$  min, as defined in Table 145–16 and with 5% duty cycle. Peak operating power shall not exceed  $1.05 \times P_{\text{Port\_PD}} \text{ max}$  for single-signature PDs and shall not exceed  $1.05 \times P_{\text{Port\_PD-2P}} \text{ max}$  for dual-signature PDs on each pairset.  $P_{\text{Port\_PD}} \text{ max}$  refers to the maximum power draw as permitted by 145.3.8.2.1.

#### 145.3.8.5 Input current slew rate

When the input voltage at the PI is static and in the range of  $V_{\text{Port\_PD-2P}}$  defined by Table 145–29, the input current drawn by a single-signature PD shall not change faster than  $I_{\text{Slewrte}}$  defined in Table 145–29, in either polarity. Each pairset current drawn by a dual-signature PD shall not change faster than  $I_{\text{Slewrte}}$  defined in Table 145–29, in either polarity. This limitation applies after inrush has completed (see 145.3.8.3) and before the PD has disconnected.

#### 145.3.8.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients

- Lasting longer than 30  $\mu\text{s}$  and less than 250  $\mu\text{s}$  at the PSE PI as defined in 145.2.10.3, and causing the voltage at the PD PI to fall to no less than  $V_{\text{Tran\_PD-2P}}$ , as defined in Table 145–29.
- Lasting less than 30  $\mu\text{s}$  and causing the voltage at the PD PI to fall to not less than 34 V.

During a transient the input power of the PD may exceed  $P_{\text{Peak\_PD}}$  or  $P_{\text{Peak\_PD-2P}}$ . Table 145–30 defines three PSE output voltage transients.

When transient TR1 or TR2 is applied, the PD shall meet the operating power limits within  $T_{\text{Transient}}$ , as defined in Table 145–30, referenced from when the ‘final voltage’ is reached at the source. When transient TR1 or TR2 is applied, the PD shall not cause the source to be in current limit for longer than  $T_{\text{LIM}}$  min.

When transient TR3 is applied, the PD shall meet the operating power limits within 4 ms, referenced from the beginning of the TR3 transient.

**Table 145–30—Transient conditions**

| Item | Assigned Class | 2-pair/<br>4-pair | $T_{\text{Transient}}$ | Initial voltage | Final voltage | Source dv / dt | Source resistance | Source current <sup>a</sup>                 |
|------|----------------|-------------------|------------------------|-----------------|---------------|----------------|-------------------|---------------------------------------------|
| TR1  | 1 to 4         | 2-pair            | 10 ms                  | 50 V            | 56 V          | 2.25 V/ms      | 12.5 $\Omega$     | Limit to $I_{\text{LIM-2P}} + 5 \text{ mA}$ |
|      | 1 to 6         | 4-pair            |                        |                 |               |                | 6.25 $\Omega$     |                                             |
| TR2  | 1 to 4         | 2-pair            | 6 ms                   | 52 V            |               |                | 12.5 $\Omega$     |                                             |
|      | 1 to 8         | 4-pair            |                        |                 |               |                | 6.25 $\Omega$     |                                             |
| TR3  | 1 to 8         | both              | 4 ms                   | 52 V            | 54.5 V        | 3500 V/ms      | 1.5 $\Omega$      | > 5 A capability                            |

<sup>a</sup> The source current for TR1 and TR2 is the current limit per powered pairset.

The TR1, TR2, and TR3 tests consists of a voltage source, with a current limit (for TR1 and TR2), driven from the ‘initial voltage’ to the ‘final voltage’ at the ‘source dv/dt’ rate. A source resistance, as defined in Table 145–30 is in series with this voltage source and the PD.

These requirements apply to each pairset individually for a dual-signature PD.

#### 145.3.8.7 Ripple and noise

The PD shall meet  $V_{\text{Noise\_PD}}$ , defined in Table 145–29, the common-mode or differential pair-to-pair noise at the PD PI generated by the PD circuitry.  $V_{\text{Noise\_PD}}$  applies for all operating voltages in the range of  $V_{\text{Port\_PD-2P}}$ , over the range of input power of the device, and when connected to any source resistance up to  $R_{\text{Ch}}$ .

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 145–16.

#### 145.3.8.8 Reflected voltage

For a single-signature PD, when any voltage in the range of 0 V to  $V_{\text{Port\_PD-2P max}}$  is applied per any of the valid 2-pair configurations, defined in Table 145–20, that have only a single pair connected to the positive potential (see Figure 145–31), the voltage on the Mode not connected to the voltage source, with a 100 k $\Omega$  resistor connected across that Mode, shall not exceed  $V_{\text{refl}}$  as defined in Table 145–29.

For a dual-signature PD, when any voltage in the range of 0 V to  $V_{\text{Port\_PD-2P max}}$  is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to the positive potential (see Figure 145–31), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 k $\Omega$  resistor connected across that Mode, shall not exceed  $V_{\text{refl}}$  as defined in Table 145–29.

#### 145.3.8.9 PD pair-to-pair current unbalance

When a PSE supplies power to a PD using all 4 pairs, the current may not equally divide between the pairs that are at the same polarity. This is referred to as pair-to-pair current unbalance. The degree to which the current is unbalanced depends on the specific combination of PSE, cabling, and PD.

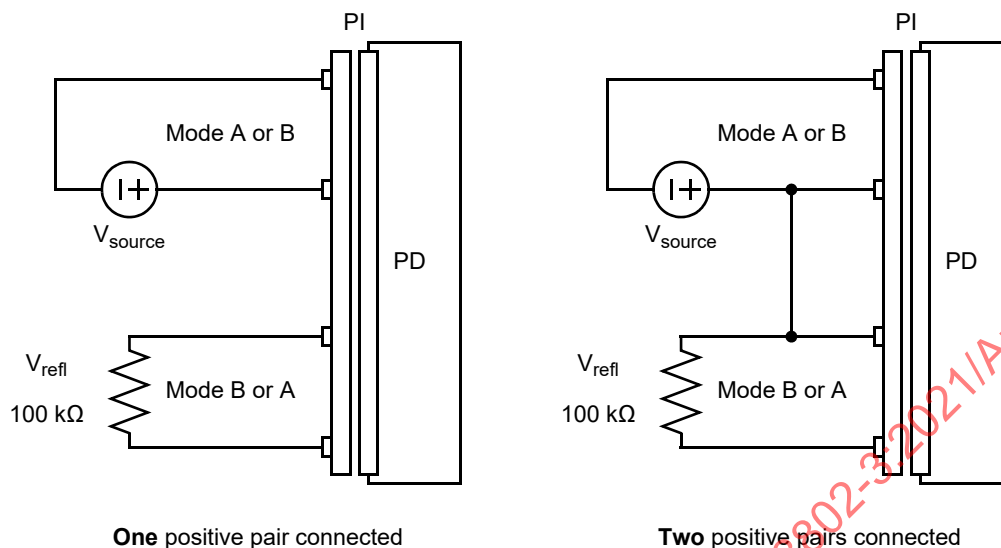


Figure 145-31—Reflected voltage requirements

The maximum pair current in a system depends on the assigned Class (see 145.3.6), and is defined in Table 145-31.

Table 145-31—Maximum pair-to-pair current unbalance

| Parameter                       | Assigned Class      | Unit | Value                                  |
|---------------------------------|---------------------|------|----------------------------------------|
| $I_{\text{Unbalance\_PD-2P}}$   | 1 to 4 <sup>a</sup> | A    | $P_{\text{Class\_PD}} / V_{\text{PD}}$ |
|                                 | 5 to 8              |      | $I_{\text{Con-2P-unb}} - 0.01$         |
| $I_{\text{Unbalance\_peak-2P}}$ | 1 to 4 <sup>a</sup> | A    | $P_{\text{Peak\_PD}} / V_{\text{PD}}$  |
|                                 | 5 to 8              |      | $I_{\text{LIM-2P}} - 0.002$            |

<sup>a</sup> There is no maximum unbalance current requirement for these assigned Classes.

This subclause describes unbalance requirements for PDs that operate over 4 pairs. The contribution of PD PI pair-to-pair effective resistance unbalance to the effective system end-to-end resistance unbalance is determined by PD maximum ( $R_{\text{PD\_max}}$ ) and minimum ( $R_{\text{PD\_min}}$ ) common mode effective resistance in the powered pairs of same polarity. See Figure 145A-3. Effective resistances of  $R_{\text{PD\_min}}$  and  $R_{\text{PD\_max}}$  include the effects of PD pair to pair voltage difference and the PD PI resistive elements. See definition and measurements in Annex 145A.5.

$R_{\text{PD\_max}}$ , defined in Equation (145-26), for a given  $R_{\text{PD\_min}}$ , is the highest supported common mode effective resistance in the powered pairs of the same polarity. PDs that meet Equation (145-26) intrinsically meet unbalance requirements. Equation (145-26) is only applicable for  $R_{\text{PD\_min}}$  up to a value of 1  $\Omega$  and power draw up to  $P_{\text{Class\_PD}}$ .

$$0 < R_{PD\_max} \leq \begin{cases} 2.182 \times R_{PD\_min} + 0.125 & \text{for assigned Class 5} \\ 1.988 \times R_{PD\_min} + 0.105 & \text{for assigned Class 6} \\ 1.784 \times R_{PD\_min} + 0.08 & \text{for assigned Class 7} \\ 1.727 \times R_{PD\_min} + 0.074 & \text{for assigned Class 8} \end{cases} \Omega \quad (145-26)$$

where

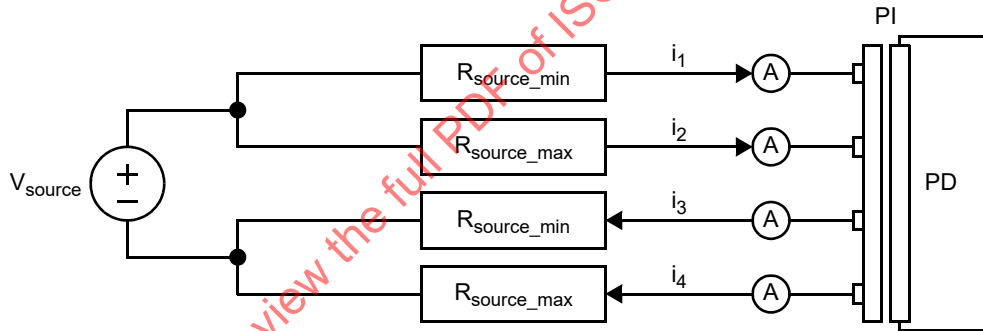
$R_{PD\_max}$  is, given  $R_{PD\_min}$ , the highest supported common mode effective resistance in the powered pairs of the same polarity

$R_{PD\_min}$  is the lower PD common mode effective resistance in the powered pairs of the same polarity

Common mode effective resistance is the resistance of the two conductors (including their components on each conductor) in a powered pair of the same polarity connected in parallel.

Figure 145A-1 illustrates the relationship between  $R_{PD\_max}$  and  $R_{PD\_min}$  effective resistances at the PD PI as defined by Equation (145-26) and the rest of the end-to-end pair to pair effective resistance components.

Single-signature PDs shall not exceed  $I_{Unbalance\_PD-2P}$  for longer than  $T_{CUT\_min}$  and 5 % duty cycle, and shall not exceed  $I_{Unbalance\_peak-2P}$ , as defined in Table 145-31 on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145-20, to any voltage in the range of  $V_{Port\_PSE-2P\_min} + 0.31\text{ V}$  to  $V_{Port\_PSE-2P\_max}$  through two common mode resistances,  $R_{source\_min}$  and  $R_{source\_max}$ , as defined in Equation (145-27) and shown in Figure 145-32.



**Figure 145-32—PD current unbalance verification circuit**

Dual-signature PDs shall not exceed  $I_{Con\_PD-2P}$ , as defined in Equation (145-28), for longer than  $T_{CUT\_min}$  and 5 % duty cycle, as defined in Table 145-16, and shall not exceed  $I_{Peak\_PD-2P}$ , as defined in Equation (145-29), on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145-20, to any voltage in the range of  $V_{Port\_PSE-2P\_min} + 0.31\text{ V}$  to  $V_{Port\_PSE-2P\_max}$  through two common mode resistances,  $R_{source\_min}$  and  $R_{source\_max}$ , as defined in Equation (145-27) and shown in Figure 145-32.

The unbalance current requirements for PDs apply at the PD PI connector (jack) when mated with a specified balanced cabling connector (plug).

NOTE 1—The duty cycle of the peak current is measured using a sliding window with a width of 1 second.

$$R_{\text{source\_max}} = \left\{ \begin{array}{l} (-0.03 \times R_{\text{source\_min}} + 1.324) \times R_{\text{source\_min}} \text{ for } (0.145\Omega \leq R_{\text{source\_min}} \leq 5.47\Omega) \end{array} \right\}_{\Omega} \quad (145-27)$$

$$I_{\text{Con\_PD-2P}} = \left\{ \frac{P_{\text{Class\_PD-2P}}}{V_{\text{PD}}} \right\}_{\text{A}} \quad (145-28)$$

$$I_{\text{Peak\_PD-2P}} = \left\{ \frac{P_{\text{Peak\_PD-2P}}}{V_{\text{PD}}} \right\}_{\text{A}} \quad (145-29)$$

where

- $R_{\text{source\_min}}$  is the lowest supported common mode effective source resistance in the powered pairs of the same polarity
- $P_{\text{Class\_PD-2P}}$  is the maximum power at the PD PI per the PDs assigned Class, as defined in Table 145-29
- $P_{\text{Peak\_PD-2P}}$  is the peak power a dual-signature PD may draw per its assigned Class on a pairset; see Table 145-29
- $V_{\text{PD}}$  is the voltage at the PD PI as defined in 145.1.3

$R_{\text{source\_min}}$  and  $R_{\text{source\_max}}$  represent the  $V_{\text{source}}$  source common mode effective resistance that consists of the PSE PI components ( $R_{\text{PSE\_min}}$  and  $R_{\text{PSE\_max}}$  as defined in 145.2.10.6.1,  $V_{\text{Port\_PSE\_diff}}$  as defined in Table 145-16, the link section resistance, and influence of  $R_{\text{PD\_min}}$  and  $R_{\text{PD\_max}}$  as function of system end-to-end unbalance). Common mode effective resistance is the resistance of two conductors of the same pair and their other components, which form  $R_{\text{source}}$ , connected in parallel including the effect of the system (PSE and PD) pair to pair voltage difference.

$R_{\text{PD\_min}}$ ,  $R_{\text{PD\_max}}$ , along with any other parts of the system, i.e., link section and the PSE, bounds the maximum current such that the maximum pair current including unbalance does not exceed  $I_{\text{Unbalance\_PD-2P}}$  as defined in Table 145-16 during normal operating conditions. See Annex 145A.

NOTE 2—The pairset current limit requirement also holds when  $R_{\text{source\_max}}$  and  $R_{\text{source\_min}}$  are exchanged.

### 145.3.9 PD Maintain Power Signature

A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI. A PD that does not maintain the MPS components may have its power removed within the limits of  $T_{\text{MPDO}}$  as defined in Table 145-16.  $I_{\text{Port\_MPS}}$ ,  $I_{\text{Port\_MPS-2P}}$ ,  $T_{\text{MPS\_PD}}$ , and  $T_{\text{MPDO\_PD}}$ , are defined in Table 145-32.  $T_{\text{LCE\_PD}}$  is defined in Table 145-25.

For single-signature PDs the MPS shall consist of current draw equal to or above  $I_{\text{Port\_MPS}}$  for a minimum duration of  $T_{\text{MPS\_PD}}$  followed by an optional MPS dropout for no longer than  $T_{\text{MPDO\_PD}}$ . A single-signature PD shall use the  $I_{\text{Port\_MPS}}$  value associated with assigned Class 1 to 4 when  $\text{pse\_assigned\_class}$  is 1, 2, 3, or 4, and  $\text{MirroredPSEAllocatedPowerValue}$  and  $\text{PDRequestedPowerValue}$  are less or equal to 255. A single-signature PD shall use the  $I_{\text{Port\_MPS}}$  value associated with assigned Class 5 to 8 when  $\text{pse\_assigned\_class}$  is 5, 6, 7, or 8, or when  $\text{PDRequestedPowerValue}$  is in the range of 256 to 999. When  $\text{PDRequestedPowerValue}$  or  $\text{PSEAllocatedPowerValue}$  is equal to 0xACAC, the PD shall use the  $I_{\text{Port\_MPS}}$  value associated with the assigned Class.

For dual-signature PDs the MPS shall consist of current draw equal to or above  $I_{\text{Port\_MPS-2P}}$  on each powered pairset independently for a minimum duration of  $T_{\text{MPS\_PD}}$  followed by an optional MPS dropout for no longer than  $T_{\text{MPDO\_PD}}$ .

**Table 145–32—PD DC Maintain Power Signature**

| Item                                                                                                                                                                                                                                                                                                                                                                                                                        | Parameter                                                            | Symbol                    | Units | Min   | Max | Conditions               |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|---------------------------|-------|-------|-----|--------------------------|
| 1                                                                                                                                                                                                                                                                                                                                                                                                                           | Total input current per the assigned Class, for single-signature PDs |                           |       |       |     |                          |
|                                                                                                                                                                                                                                                                                                                                                                                                                             | Class 1 to 4                                                         | $I_{\text{Port\_MPS}}$    | A     | 0.01  | —   | See 145.3.9              |
|                                                                                                                                                                                                                                                                                                                                                                                                                             | Class 5 to 8                                                         |                           |       | 0.016 |     |                          |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                           | Input current on each powered pairset for dual-signature PDs         |                           |       |       |     |                          |
|                                                                                                                                                                                                                                                                                                                                                                                                                             | Class 1 to 5                                                         | $I_{\text{Port\_MPS-2P}}$ | A     | 0.01  | —   | —                        |
| 3                                                                                                                                                                                                                                                                                                                                                                                                                           | PD Maintain Power Signature Time                                     | $T_{\text{MPS\_PD}}$      | ms    | 75    | —   | long_class_event = FALSE |
|                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                      |                           |       | 7     | —   | long_class_event = TRUE  |
| 4                                                                                                                                                                                                                                                                                                                                                                                                                           | PD Drop Out Period                                                   | $T_{\text{MPDO\_PD}}$     | ms    | —     | 250 | long_class_event = FALSE |
|                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                      |                           |       | —     | 310 | long_class_event = TRUE  |
| NOTE—PDs may not be able to meet the $I_{\text{Port\_MPS}}$ or $I_{\text{Port\_MPS-2P}}$ specification in Table 145–32 during the maximum allowed port voltage droop ( $V_{\text{Port\_PSE-2P max}}$ to $V_{\text{Port\_PSE-2P min}}$ with series resistance $R_{\text{Ch}}$ ). Such a PD should increase its $I_{\text{Port}}$ or $I_{\text{Port-2P}}$ or make other such provisions to meet the Maintain Power Signature. |                                                                      |                           |       |       |     |                          |

A PD connected to a Type 1 or Type 2 PSE, shall also present input impedance with resistive and capacitive components defined in Table 145–33.

**Table 145–33—PD Maintain Power Signature**

| Item | Parameter         | Symbol             | Unit          | Min  | Max  | Additional information |
|------|-------------------|--------------------|---------------|------|------|------------------------|
| 1    | Input resistance  | $R_{\text{pd\_d}}$ | k $\Omega$    | —    | 26.3 | —                      |
| 2    | Input capacitance | $C_{\text{pd\_d}}$ | $\mu\text{F}$ | 0.05 | —    | —                      |

PDs that detect a long first class event in the range of  $T_{\text{LCE\_PD}}$  may use the shorter  $T_{\text{MPS\_PD}}$  in order to draw a lower standby MPS power. In the absence of a long first class event, the minimum  $T_{\text{MPS\_PD}}$  is higher and the standby MPS power is also higher.

A PD shall meet the  $T_{\text{MPS\_PD}}$  and  $T_{\text{MPDO\_PD}}$  requirements with any series resistance less than or equal to  $R_{\text{Chan max}}$  between the PD PI and the source.

Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2, shall remove both the current draw and impedance components of the MPS. To cause Type 1 and Type 2 PSE power removal, the impedance of the PI should rise above 1980 k $\Omega$ .

Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4, shall remove the current draw component and may remove the impedance components of the MPS. See 145.2.12, 145.2.10.4, and 145.3.8.8.

## 145.4 Additional electrical specifications

This clause defines additional electrical specifications for a fully connected PoE system (that is, PSE, cabling, PD, and related PHYs) and therefore to each element of such a system. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 145.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T PHYs.

### 145.4.1 Isolation

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector. Accessible external conductors are specified in Section 6.2.1 b) of IEC 60950-1:2001 and Section 5.4.10.1 b) of IEC 62368-1:2018.

This electrical isolation shall withstand at least one of the following electrical strength tests:

- a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.2.2 of IEC 60950-1:2001 or Section 5.4.9 of IEC 62368-1:2018.
- b) 2250 V dc for 60 s, applied as specified in Section 5.2.2 of IEC 60950-1:2001 or Section 5.4.9 of IEC 62368-1:2018.
- c) An impulse test consisting of a 1500 V, 10/700  $\mu$ s waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses shall be 10/700  $\mu$ s (10  $\mu$ s virtual front time, 700  $\mu$ s virtual time of half value), as defined in Annex N of IEC 60950-1:2001 or Section 5.4.10 of IEC 62368-1:2018.

There shall be no insulation breakdown, as defined in Section 5.2.2 of IEC 60950-1:2001 or Section 5.4.9 of IEC 62368-1:2018, during the test. The resistance after the test shall be at least 2 M $\Omega$ , measured at 500 V dc.

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents. See 145.2.10.4.

Dual-signature PDs shall have less than or equal to 10  $\mu$ A of current between any negative conductor of Mode A and any negative conductor of Mode B when  $V_{PD}$ , as defined in 145.1.3, is less than  $V_{OFF\_PD}$  min, as defined in Table 145–29, on either Mode. See Table 79–6f.

#### 145.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

- **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
- **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

#### 145.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted-pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

An Environment A multiport NID does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowed to switch both conductors.

#### 145.4.1.1.2 Environment B requirements

The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

An environment B PSE that supports 4-pair power shall switch the more negative conductor. It is allowed to switch both conductors.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1:2001 and throughout IEC 62368-1, as well as any local and national codes related to safety.

#### 145.4.2 Fault tolerance

Each conductor pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, 40.8.3.4, 55.8.2.3, and 126.8.2.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE shall withstand without damage the application of short circuits of any conductors within the cable for an indefinite period of time. The magnitude of the current caused by a short circuit of any one conductor to another conductor in the cable

- Shall not exceed  $I_{PSEUT-Type3-2P}$ , as defined in Equation (145–17), for Type 3 PSEs.
- Shall not exceed  $I_{PSEUT-Type4-2P}$ , as defined in Equation (145–18), for Type 4 PSEs.

Each conductor pair shall withstand, without damage, a 1000 V common-mode impulse applied at  $E_{cm}$  of either polarity. The shape of the impulse shall be (0.3/50)  $\mu$ s (300 ns virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC 60060, where  $E_{cm}$  is an externally applied AC voltage as shown in Figure 145–33.

NOTE—PDs may receive power from a PSE over fewer conductors than specified when a link section has a fault of one or more conductor open failures.

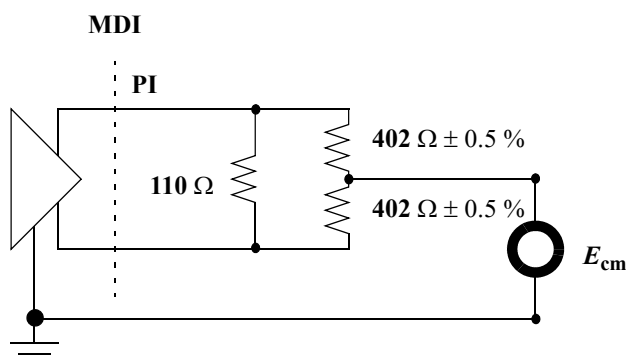


Figure 145-33—PI fault tolerance test circuit

### 145.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed the limits in Table 145-34 for all supported PHY speeds.

Table 145-34—Impedance balance limits for supported speeds

| Supported speed           | Impedance balance limit (dB)       | Frequency range          |
|---------------------------|------------------------------------|--------------------------|
| 10 Mb/s MAU               | $29 - 17 \times \log_{10}(f/10)$   | $1 \leq f \leq 20$ MHz   |
| 100 Mb/s or 1000 Mb/s PHY | $34 - 19.2 \times \log_{10}(f/50)$ | $1 \leq f \leq 100$ MHz  |
| 2.5 Gb/s PHY              | 48                                 | $1 \leq f < 10$ MHz      |
|                           | $48 - 20 \times \log_{10}(f/10)$   | $10 \leq f < 20$ MHz     |
|                           | $42 - 15 \times \log_{10}(f/20)$   | $20 \leq f \leq 125$ MHz |
| 5 Gb/s PHY                | 48                                 | $1 \leq f < 30$ MHz      |
|                           | $44 - 19.2 \times \log_{10}(f/50)$ | $30 \leq f \leq 250$ MHz |
| 10 Gb/s PHY               | 48                                 | $1 \leq f < 30$ MHz      |
|                           | $44 - 19.2 \times \log_{10}(f/50)$ | $30 \leq f \leq 500$ MHz |

The impedance balance is defined as shown in Equation (145–30):

$$\left\{ 20 \times \log_{10} \left( \frac{E_{\text{cm}}}{E_{\text{dif}}} \right) \right\}_{\text{dB}} \tag{145–30}$$

where

$E_{\text{cm}}$  is an externally applied sinusoidal voltage as shown in Figure 145–34  
 $E_{\text{dif}}$  is the voltage of the resulting waveform due only to the applied sine wave measured as shown in Figure 145–34

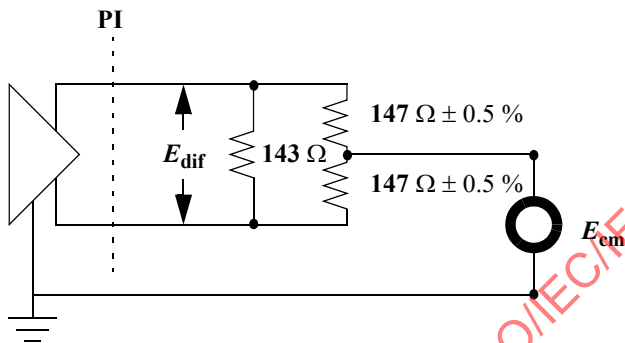
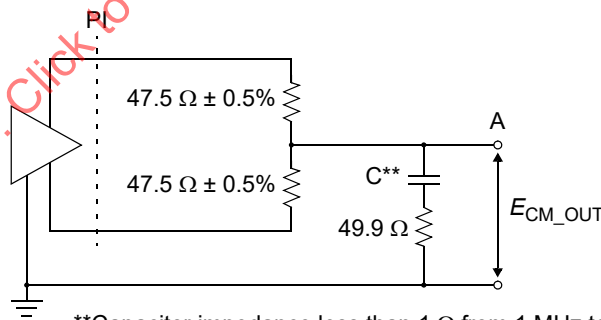


Figure 145–34—PI impedance balance test circuit

#### 145.4.4 Common-mode output voltage

The magnitude of the common-mode AC output voltage measured according to Figure 145–35 and Figure 145–36 at the transmit PI while transmitting data and with power applied,  $E_{\text{cm\_out}}$ , shall not exceed the values in Table 145–35 while operating at the specified speed, when measured over the specified bandwidth.



\*\*Capacitor impedance less than 1 Ω from 1 MHz to 500 MHz

Figure 145–35—Common-mode output voltage test

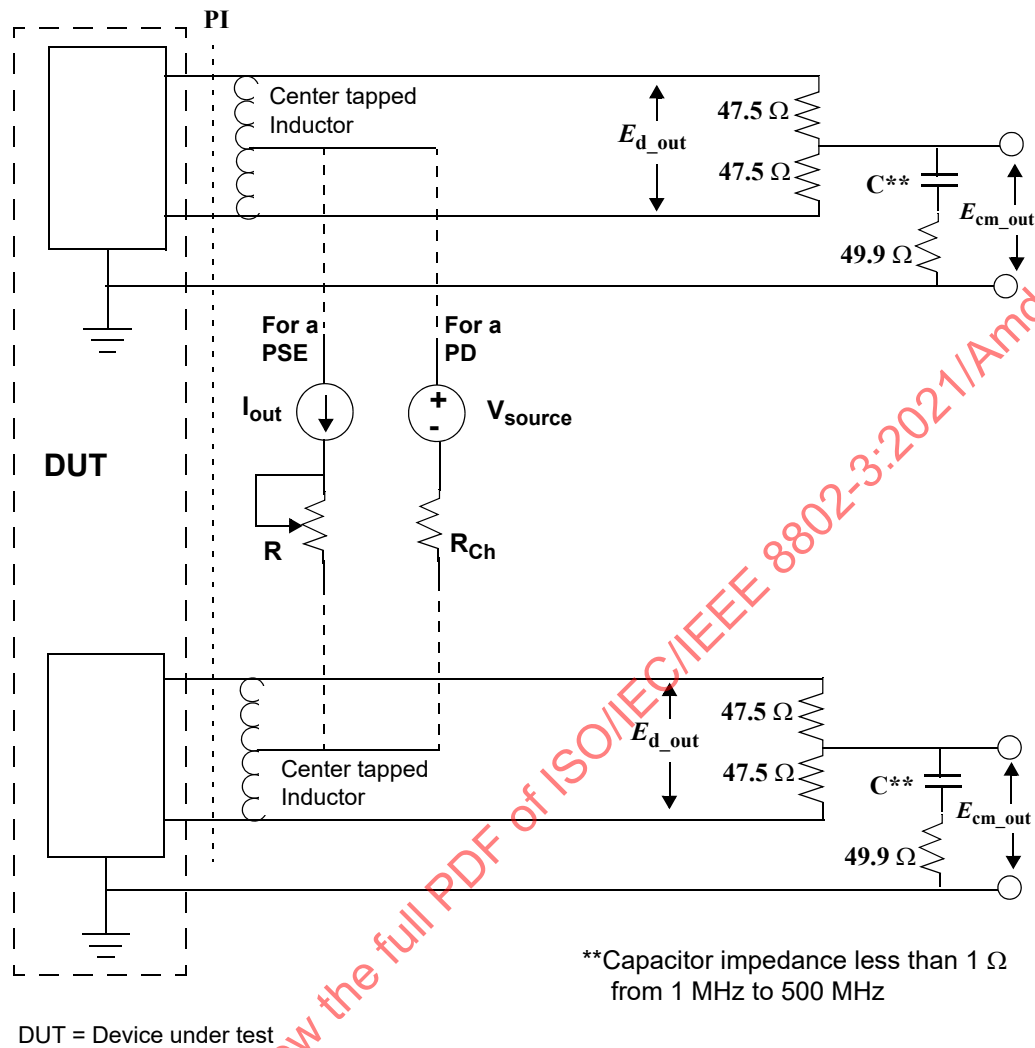


Figure 145-36—PSE and PD terminations for common-mode output voltage test

Table 145-35—Common-mode output voltage for given operating speed

| Operating speed           | Common-mode output voltage ( $E_{cm\_out}$ ) | Measurement bandwidth          |
|---------------------------|----------------------------------------------|--------------------------------|
| 10 Mb/s MAU               | 50 mV peak                                   | $1 \leq f \leq 100\text{ MHz}$ |
| 100 Mb/s or 1000 Mb/s PHY | 50 mV <sub>pp</sub>                          | $1 \leq f \leq 100\text{ MHz}$ |
| 2.5 Gb/s PHY              | 50 mV <sub>pp</sub>                          | $1 \leq f \leq 100\text{ MHz}$ |
| 5 Gb/s PHY                | 50 mV <sub>pp</sub>                          | $1 \leq f \leq 250\text{ MHz}$ |
| 10 Gb/s PHY               | 50 mV <sub>pp</sub>                          | $1 \leq f \leq 500\text{ MHz}$ |

The common-mode AC output voltage shall be measured while the PHY is transmitting data, the PSE or PD is operating with the following PSE load or PD source:

- 1) For a PSE, the PI that supplies power is terminated as illustrated in Figure 145–36. The PSE load,  $R$ , in Figure 145–36 is adjusted so that the PSE output current,  $I_{out}$ , is 16 mA and then  $I_{Cable}$  for 2-pair operation or  $2 \times I_{Cable}$  for 4-pair operation, while measuring  $E_{cm\_out}$  on the PI.
- 2) For a PD, the PI that requires power shall be terminated as illustrated in Figure 145–36.  $V_{source}$  in Figure 145–36 is adjusted to 36 Vdc and 57 Vdc, while measuring  $E_{cm\_out}$  on the PI.

NOTE—The implementer should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

#### 145.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 145–37) is limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply, Table 145–16, ‘power feeding ripple and noise’, or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

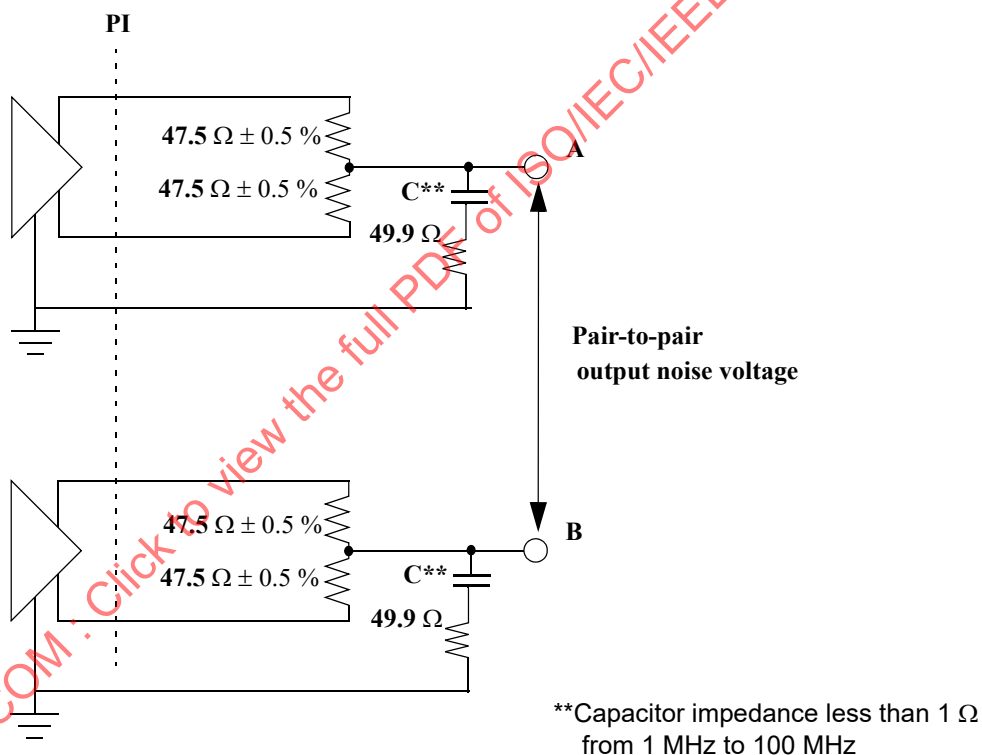


Figure 145–37—Pair-to-pair output noise voltage test

#### 145.4.6 Differential noise voltage

For 10/100/1000 Mb/s, the coupled noise,  $E_{d\_out}$  in Figure 145–36, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 145.4.4, item 1) and item 2).

For 2.5GBASE-T, 5GBASE-T, or 10GBASE-T, the coupled noise,  $E_{d\_out}$  in Figure 145–36, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1 mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T under the conditions specified in 145.4.4, item 1) and item 2).

#### 145.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified

- In 14.3.1.3.4 for a 10 Mb/s PHY.
- In ANSI INCITS 263-1995 for a 100 Mb/s PHY.
- In 40.8.3.1 for a 1000 Mb/s PHY.
- In 126.8.2.2 for a 2.5 Gb/s or 5 Gb/s PHY.
- In 55.8.2.1 for a 10 Gb/s PHY.

In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75  $\Omega$ . The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

#### 145.4.8 100BASE-TX transformer droop

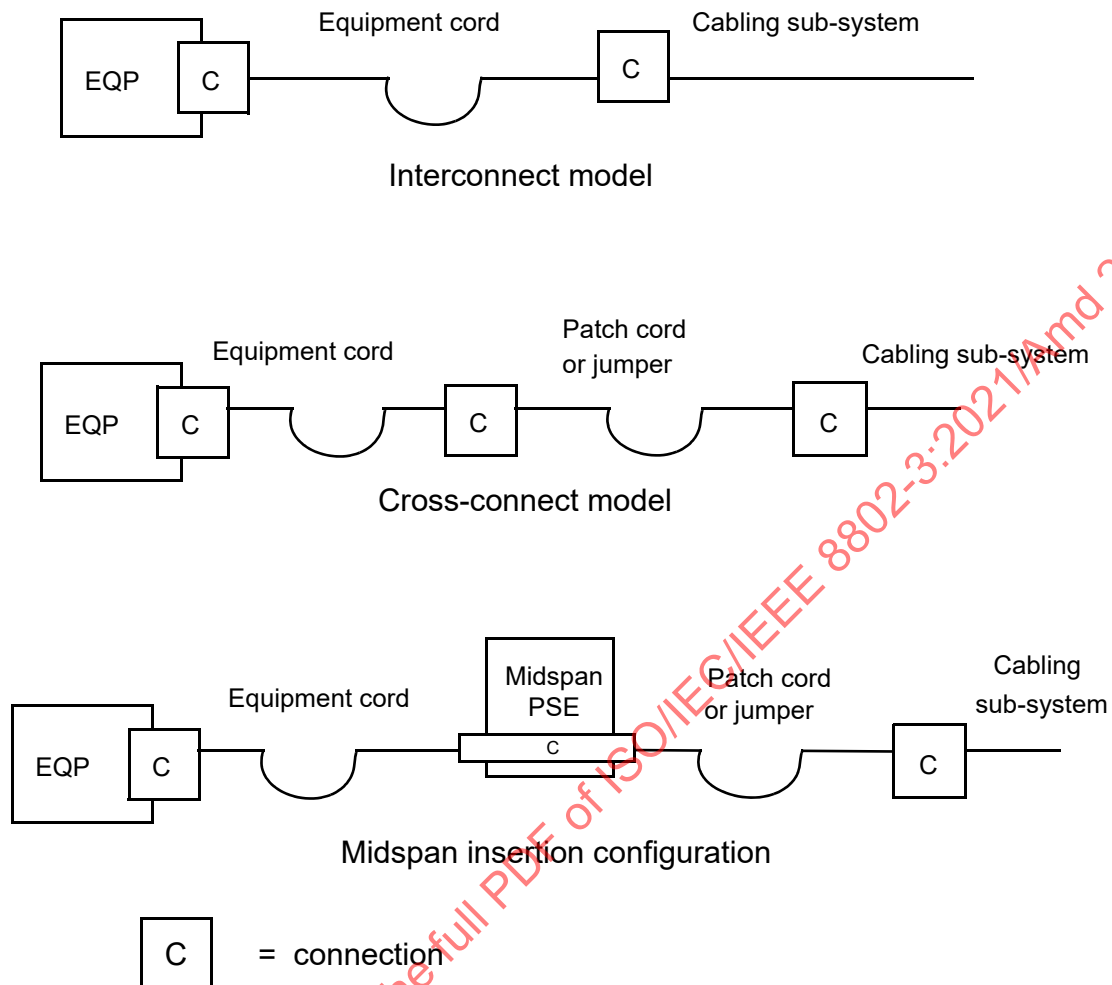
100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to a PHY transmitter with 350  $\mu$ H open circuit inductance (OCL). Alternative A Midspan PSEs that support 100BASE-TX shall enforce intra-pair current unbalance (see 145A.1) less than or equal to  $I_{unb}$  (see 145.2.10.12) or meet 145.4.9.3.

100BASE-TX Endpoint PSEs and 100BASE-TX PDs shall meet the requirements of Clause 25 in the presence of ( $I_{unb}/2$ ).

#### 145.4.9 Midspan PSE device additional requirements

The cabling specifications for 100  $\Omega$  balanced cabling are described in ISO/IEC 11801:2002. Cable conforming to ANSI/TIA-568-C.2 also meets these requirements. Some cable category specifications that only appear in earlier editions are also supported. The terms “channel” and “permanent link” are defined in ISO/IEC 11801-1 subsection 5.3.5. Midspan PSE cabling system requirements are specified in 145.1.4.

ISO/IEC 11801-1 defines in 5.1 two types of Equipment interface to the cabling system: “Interconnect model” and the “cross-connect model.” An equivalent “Interconnect model” and “cross-connect model” may be found in ANSI/TIA-568.0-D, 5.1. See Figure 145–38.



**Figure 145-38—Interconnect model, cross-connect model, and midspan insertion configuration**

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

- If the existing FD configuration is of the “Interconnect model” type, the Midspan PSE can be added, provided it does not increase the insertion loss of the resulting “channel” to more than specified for the same Class or category 100 m channel defined in ISO/IEC 11801-1 or ANSI/TIA-568.0-D.
- If the existing FD configuration is of the “Cross-connect model” type, the Midspan PSE can be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the insertion loss of the resulting “channel” to more than specified for the same Class or category 100 m channel defined in ISO/IEC 11801-1 or ANSI/TIA-568.0-D.
- For a 10GBASE-T midspan PSE, in meeting either of the above requirements, the Midspan PSE may be substituted for up to two connection pairs in the FD.

Configurations with the Midspan PSE in the cabling “channel” shall not alter the transmission requirements of the “permanent link.” A Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

The requirements for the two pair Category 5 link segment are found in 25.4.9. Specification of 4-pair cabling is beyond the scope of Clause 25.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the Midspan device.

#### 145.4.9.1 Connector Midspan PSE device transmission requirements

A connector Midspan PSE replaces one of the connectors in the link segment and shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO/IEC 11801-1 or ANSI/TIA-568-C.2 for connecting hardware.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

- 1) 10BASE-T/100BASE-TX connector Midspan PSE
- 2) 1000BASE-T connector Midspan PSE
- 3) 2.5GBASE-T connector Midspan PSE
- 4) 5GBASE-T connector Midspan PSE
- 5) 10GBASE-T connector Midspan PSE

##### 145.4.9.1.1 Near End Crosstalk (NEXT)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. For operation with 2.5GBASE-T and lower rates, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–31) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–31) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For operation with 5GBASE-T and lower rates, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXT_{conn}\}_{dB} \geq 43 - 20 \times \log_{10}\left(\frac{f}{100}\right) \quad (145-31)$$

where

$NEXT_{conn}$  is the Near End Crosstalk loss in dB  
 $f$  is the frequency expressed in MHz

For 10GBASE-T operation, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–32) when measured for the transmit and receive pairs from 1 MHz to 500 MHz. However, for frequencies that correspond to calculated values greater than 75 dB, the requirement reverts to the minimum requirement of 75 dB.

$$\{NEXT_{conn}\}_{dB} \leq \left\{ \begin{array}{ll} 54 - 20 \times \log_{10}\left(\frac{f}{100}\right) & \text{for } (1 \leq f \leq 250) \\ 46.04 - 40 \times \log_{10}\left(\frac{f}{250}\right) & \text{for } (250 < f \leq 500) \end{array} \right\}_{dB} \quad (145-32)$$

where

$NEXT_{conn}$  is the Near End Crosstalk loss in dB  
 $f$  is the frequency expressed in MHz

**145.4.9.1.2 Insertion loss**

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. For other than 5GBASE-T or 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (145–33) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (145–33) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (145–33) when measured from the transmit and receive pairs from 1 MHz to 500 MHz. For frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB.

$$\{IL_{conn}\}_{dB} \leq 0.04 \times \sqrt{f} \quad (145-33)$$

where

$IL_{conn}$  is the insertion loss in dB  
 $f$  is the frequency expressed in MHz

**145.4.9.1.3 Return loss**

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 145–36.

**Table 145–36—Connector return loss**

| Midspan PSE Variant | Frequency                                    | Return loss                |
|---------------------|----------------------------------------------|----------------------------|
| 10/100/1000BASE-T   | $1 \text{ MHz} \leq f < 20 \text{ MHz}$      | 23 dB                      |
|                     | $20 \text{ MHz} \leq f \leq 100 \text{ MHz}$ | 14 dB                      |
| 2.5GBASE-T          | $1 \text{ MHz} \leq f < 31.5 \text{ MHz}$    | 30 dB                      |
|                     | $31.5 \text{ MHz} \leq f < 100 \text{ MHz}$  | $20 - 20 \log_{10}(f/100)$ |
| 5GBASE-T            | $1 \text{ MHz} \leq f < 31.5 \text{ MHz}$    | 30 dB                      |
|                     | $31.5 \text{ MHz} \leq f < 250 \text{ MHz}$  | $20 - 20 \log_{10}(f/100)$ |
| 10GBASE-T           | $1 \text{ MHz} \leq f < 79 \text{ MHz}$      | 30 dB                      |
|                     | $79 \text{ MHz} \leq f \leq 500 \text{ MHz}$ | $28 - 20 \log_{10}(f/100)$ |

**145.4.9.2 Cord Midspan PSE**

A Midspan PSE replaces an element in a link segment and shall meet or exceed the insertion loss, NEXT, and return loss values specified Table 145–37 for all data transmitting pairs.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

- 1) 10BASE-T/100BASE-TX cord Midspan PSE
- 2) 1000BASE-T cord Midspan PSE
- 3) 2.5GBASE-T cord Midspan PSE

- 4) 5GBASE-T cord Midspan PSE
- 5) 10GBASE-T cord Midspan PSE

**Table 145–37—Cord specifications for use with Midspan PSEs**

| Highest PHY rate supported | Cord specification                                           | Frequency range                             |
|----------------------------|--------------------------------------------------------------|---------------------------------------------|
| Up to 1000BASE-T           | Category 5 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-A:1995 | $1 \text{ MHz} \leq f \leq 100 \text{ MHz}$ |
| Up to 2.5GBASE-T           | Category 5e cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2   | $1 \text{ MHz} \leq f \leq 100 \text{ MHz}$ |
| Up to 5GBASE-T             | Category 6 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2    | $1 \text{ MHz} \leq f \leq 250 \text{ MHz}$ |
| Up to 10GBASE-T            | Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2      | $1 \text{ MHz} \leq f \leq 500 \text{ MHz}$ |

#### 145.4.9.2.1 Maximum link delay

The propagation delay contribution of the Midspan PSE device shall not exceed 2.5 ns from 1 MHz to the highest referenced frequency.

#### 145.4.9.2.2 Maximum link delay skew

The propagation delay skew of the Midspan PSE device shall not exceed 1.25 ns from 1 MHz to the highest referenced frequency.

#### 145.4.9.3 Midspan signal path requirements

An Alternative A Midspan PSE transfer function gain shall be greater than that expressed by Equation (145–34) for the frequency range from 0.1 MHz to 1 MHz, at the pins of the PI used as 100BASE-TX transmit pins.

$$\left\{ -0.1 + 37.5 \times \log_{10} \left( \frac{22.4 \times f}{\sqrt{1 + 521 \times f^2}} \right) \right\}_{\text{dB}} \quad (145-34)$$

where

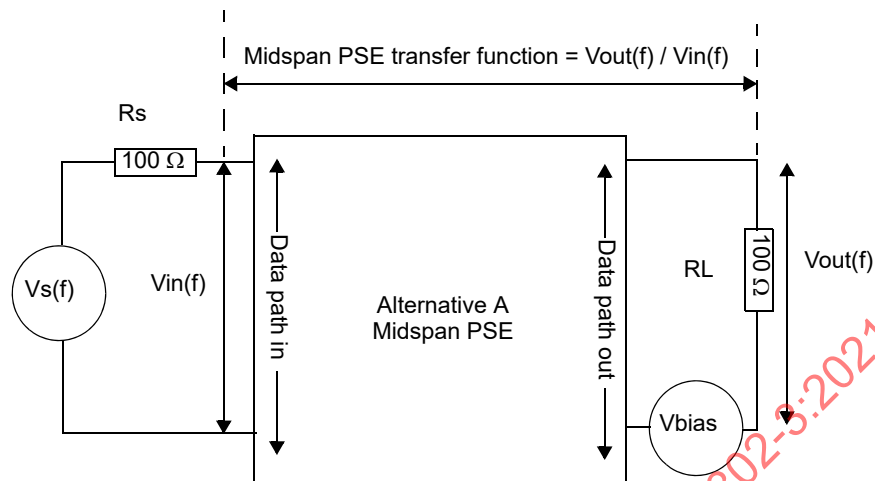
$f$  is the frequency expressed in MHz

The requirements shall be met with a DC bias current,  $I_{\text{bias}}$ , between 0 mA and  $(I_{\text{unb}}/2)$  mA ( $I_{\text{unb}}$  is defined in Table 145–16).

##### 145.4.9.3.1 Alternative A Midspan PSE signal path transfer function

The transfer function is measured by applying a test signal to the Midspan PSE signal input through a source impedance of  $100 \Omega \pm 1 \%$ . The Midspan PSE signal input and output may be connected to a 0.5 m maximum length of cable, meeting the requirements of 25.4.9, terminated with  $100 \Omega \pm 1 \%$ .

The transfer function is defined from the output termination to the Midspan PSE input. See Figure 145–39.



$V_{in}(f)$  is the sine wave signal to be used to measure the Midspan PSE transfer function.  
 $V_{bias}$  is the DC offset voltage to be applied in series with  $R_L$  in order to generate  $I_{bias}$ .  
 $V_{out}(f)$  is the Midspan PSE response to  $V_{in}(f)$ .  
Some test equipment may require isolation between measurement ports.

**Figure 145–39—Measurement setup for Alternative A Midspan PSE transfer function**

#### 145.4.9.4 Coupling parameters between link segments

Midspan PSEs intended for operation with 2.5G/5G/10GBASE-T (variants 3 through 5 in 145.4.9.1 and 145.4.9.2) are additionally required to meet the following specifications for PSANEXT and PSAFEXT for coupling signals between ports relating to different link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To bound the total alien NEXT loss and alien FEXT loss coupled between link segments, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified.

##### 145.4.9.4.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using Equation (145–35). For other than 5GBASE-T or 10GBASE-T operation, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–35) from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–35) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–35) from 1 MHz to 500 MHz. When the computed PSANEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

$$\text{PSANEXT loss} = 70.5 - 20 \times \log_{10}(f/100) \quad (145-35)$$

##### 145.4.9.4.2 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss

PSAFEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined in Equation (145–36). For other than 5GBASE-T or 10GBASE-T operation, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–36) from 1 MHz to 100 MHz. For

5GBASE-T capable midspans, PSFEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–36) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSFEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–36) from 1 MHz to 500 MHz. When the computed PSFEXT value at a certain frequency exceeds 67 dB, the PSFEXT result at that frequency is for information only.

$$\text{PSFEXT loss} = 67 - 20 \times \log_{10}(f/100) \quad (145-36)$$

## 145.5 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Single-signature PDs that request Class 4 or higher and dual-signature PDs that request Class 4 or higher on either Mode support Data Link Layer classification (see 145.3.6). Data Link Layer classification is optional for all other devices.

### 145.5.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2016; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and may support the Power via MDI Measurements TLV defined in 79.3.8.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

### 145.5.2 Data Link Layer classification timing requirements

PSEs shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable `pse_dll_enable` (145.2.5.4, 145.5.3.2.2).

PDs shall set the variable `pd_dll_ready` within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable `pd_dll_enable` (145.3.3.3.2, 145.3.3.4.2, and 145.5.3.3.1).

The PSE shall send an LLDPDU containing a Power via MDI TLV with an updated value for the ‘PSE allocated power value’ field, ‘PSE allocated power value Alternative A’ field, and ‘PSE allocated power value Alternative B’ field within 10 seconds of receiving an LLDPDU containing a Power via MDI TLV where the ‘PD requested power value’ field, ‘PD requested power value for Mode A’ field, or ‘PD requested power value for Mode B’ field is different from the previously communicated value.

The PD shall send an LLDPDU containing a Power via MDI TLV with an updated value for the ‘PD requested power value’ field, ‘PD requested power value for Mode A’ field, and ‘PD requested power value for Mode B’ field within 10 seconds of receiving an LLDPDU containing a Power via MDI TLV where the ‘PSE allocated power value’ field, ‘PSE allocated power value Alternative A’ field, or ‘PSE allocated power value Alternative B’ field is different from the previously communicated value.

### 145.5.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively.

Data Link Layer classification of PSEs shall provide the behavior in the state diagrams defined in Figure 145–40, Figure 145–41, Figure 145–42, and Figure 145–43.

Single-signature PD Data Link Layer classification shall provide the behavior of the state diagrams defined in Figure 145–44 and Figure 145–45. Dual-signature PD Data Link Layer classification shall provide the behavior of the state diagram defined in Figure 145–46 and Figure 145–47.

### 145.5.3.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 145.2.52.

### 145.5.3.2 PSE power control state diagrams

#### 145.5.3.2.1 Alternative designation

Dual-signature PSEs provide the behavior of the state diagram shown in Figure 145–46 over each pairset independently unless otherwise specified. All the parameters that apply to Alternative A and Alternative B are denoted with the suffix “\_alt(X)” where “X” can be “A” or “B”, or “\_alt(P)” where “P” can be “A” or “B”. A parameter that ends with the suffix “\_alt(X)” may have different values for Alternative A and Alternative B.

PSEs providing power to a dual-signature PD operate over two semi-independent state diagrams, one for Alternative A, another for Alternative B. Alternative information is obtained by replacing the X in the desired variable or function with the letter of the Alternative of interest. Alternatives are referred to in general as follows:

|   |                                                                                                                                                                                                                                                                                                                                      |
|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| X | Generic Alternative designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.<br>Values:<br>A: Alternative A<br>B: Alternative B                                                                                                                          |
| P | Powered Alternative designator. When P is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams. “P” refers to the Alternative that is currently powered. Its value is only defined when the PSE operates in 2-pair mode.<br>Values:<br>A: Alternative A<br>B: Alternative B |

#### 145.5.3.2.2 Variables

The PSE power control state diagrams in Figure 145–40, Figure 145–41, Figure 145–42, and Figure 145–43 use the following variables:

##### MirroredPDAutoclassRequest

The copy of the ‘PD Autoclass request’ field in the Power via MDI TLV that the PSE receives from the remote system. This variable is mapped from aLldpXdot3RemAutoclassRequest (30.12.3.1.18o) and assigned through Table 145–38.

Values:

|        |                                                                   |
|--------|-------------------------------------------------------------------|
| FALSE: | The PD does not request an Autoclass measurement to be performed. |
| TRUE:  | The PD requests an Autoclass measurement to be performed.         |

**MirroredPDRequestedPowerValue**

The copy of the 'PD Requested Power Value' field in the Power Via MDI TLV that the PSE receives from the remote system in units of 0.1 W. This variable is mapped from the aLdpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17) and set through Table 145–38.

Values: 0 through 999, and 0xACAC

**MirroredPDRequestedPowerValue\_alt(X)**

The copy of the 'PD Requested Power Value' field for Alternative(X) in the Power Via MDI TLV that the PSE receives from the remote system in units of 0.1 W. This variable is mapped from the aLdpXdot3RemPDRequestedPowerValueA and aLdpXdot3RemPDRequestedPowerValueB attribute (30.12.3.1.17a and 30.12.3.1.17b) and set through Table 145–38.

Values: 0 through 499

**MirroredPSEAllocatedPowerValueEcho**

The copy of the 'PSE Allocated Power Value' field in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLdpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18) and set through Table 145–38.

Values: 0 through 999, and 0xACAC

**MirroredPSEAllocatedPowerValueEcho\_alt(X)**

The copy of the 'PSE Allocated Power Value' field for Alternative(X) in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLdpXdot3RemPSEAllocatedPowerValueA and aLdpXdot3RemPSEAllocatedPowerValueB attribute (30.12.3.1.18a and 30.12.3.1.18b) and set through Table 145–38.

Values: 0 through 499

**PDRequestedPowerValueEcho**

This variable is updated by the PSE state diagram. This variable maps into the aLdpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values: 0 through 999, and 0xACAC

**PDRequestedPowerValueEcho\_alt(X)**

This variable is updated by the PSE state diagram. This variable maps into the aLdpXdot3LocPDRequestedPowerValueA and aLdpXdot3LocPDRequestedPowerValueB attribute (30.12.2.1.17a and 30.12.2.1.17b).

Values: 0 through 499

**PSEAllocatedPowerValue**

Integer that indicates the PSE allocated power value in the PSE in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD ever draws. This variable maps to the aLdpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18). A value higher than 713 indicates that the PSE is capable of supporting a power level beyond  $P_{Class\_PD}$  at the PD PI. This may require an output power level higher than  $P_{Type}$  min. See 145.2.8.

Values: 0 through 999, and 0xACAC

**PSEAllocatedPowerValue\_alt(X)**

Integer that indicates the PSE allocated power value in the PSE in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD ever draws. This variable maps to the aLdpXdot3LocPSEAllocatedPowerValueA and aLdpXdot3LocPSEAllocatedPowerValueB attribute (30.12.2.1.18a and 30.12.2.1.18b). A value higher than 356 indicates that the PSE is capable of supporting a power level beyond  $P_{Class\_PD}$  at the PD PI. This may require an output power level higher than  $P_{Type}$  min. See 145.2.8.

Values: 0 through 499

**PSEAutoclassCompleted**

A Boolean that indicates the PSE has completed the PD Autoclass request. This variable is mapped into the aLdpXdot3LocPSEAutoclassCompleted (30.12.2.1.18n) attribute.

Values:

- FALSE: The PSE has not completed the Autoclass measurement, or it is not performing a Autoclass measurement.
- TRUE: The PSE has completed the Autoclass measurement.

**PSEAutoclassSupport**

A Boolean variable that indicates if the PSE supports Autoclass in the PSE. This variable is mapped into the aLldpXdot3LocPSEAutoclassSupport (30.12.2.1.18m) attribute.

Values:

- FALSE: The PSE does not support Autoclass.
- TRUE: The PSE supports Autoclass.

**TempVar**

A variable used to store Power Value in units of 0.1 W.

Values: 0 through 999, and 0xACAC

**TempVar\_alt(X)**

A variable used to store a Power Value in units of 0.1 W.

Values: 0 through 499.

**alt\_pri**

A variable used to select which Alternative assumes the role of Primary Alternative in the PSE state diagram in Figure 145–13.

Values:

- a: Alternative A assumes the role of Primary Alternative. When operating over 4 pairs, Alternative B assumes the role of Secondary Alternative.
- b: Alternative B assumes the role of Primary Alternative. When operating over 4 pairs, Alternative A assumes the role of Secondary Alternative.

**fourpairmode**

Alias for the following term: (alt\_pwrd\_pri \* alt\_pwrd\_sec)

**local\_system\_change**

An implementation-specific variable that indicates that the local system wants to change the allocated power value. This indicates the PSE is going to change the power allocated to the PD. This variable may be set by the PSE at any time.

Values:

- FALSE: The PSE does not want to change the power allocation.
- TRUE: The PSE wants to change the power allocation.

**local\_system\_change\_alt(X)**

An implementation-specific variable that indicates that the local system wants to change the allocated power value. This indicates the PSE is going to change the power allocated to the PD for Alternative(X). This variable may be set by the PSE at any time.

Values:

- FALSE: The PSE does not want to change the power allocation.
- TRUE: The PSE wants to change the power allocation.

**pse\_alternative**

This variable defined in 145.2.5.4 indicates which Pinout Alternative the PSE uses to apply power to the PI (see Table 145–3).

Values:

- a: The PSE uses PSE pinout Alternative A.
- b: The PSE uses PSE pinout Alternative B.
- both: The PSE uses both Alternative A and Alternative B.

**pse\_dll\_enable**

A variable output by the PSE state diagram (Figure 145–13) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values:

- FALSE: PSE Data Link Layer classification is not enabled.
- TRUE: PSE Data Link Layer classification is enabled.

**pse\_dll\_ready**

See pse\_dll\_ready in 145.2.5.4.

**pse\_initial\_value**

The value of this variable is valid after classification and is derived from the `pse_allocated_pwr` and `pd_autoclass` variables (145.2.5.4), which is used in the PSE state diagrams in 145.2.5.7. The value is quantized to fit the available resolution. Additional information on power levels for Class 8 may be found in 145.3.8.2.1. This variable is set per this description.

Values:

| <code>pd_autoclass</code> | <code>pse_allocated_pwr</code> | <code>pse_initial_value</code> |
|---------------------------|--------------------------------|--------------------------------|
| FALSE                     | 1                              | 39                             |
| FALSE                     | 2                              | 65                             |
| FALSE                     | 3                              | 130                            |
| FALSE                     | 4                              | 255                            |
| FALSE                     | 5                              | 400                            |
| FALSE                     | 6                              | 510                            |
| FALSE                     | 7                              | 620                            |
| FALSE                     | 8                              | 713                            |
| TRUE                      | —                              | 0xACAC                         |

**pse\_initial\_value\_alt(X)**

The value of this variable is valid after classification and is derived from `pse_allocated_pwr_pri` and `pse_allocated_pwr_sec` variables (145.2.5.4), which is used in the PSE state diagrams in 145.2.5.7. The value is quantized to fit the available resolution. Additional information on power levels for Class 5 may be found in 145.3.8.2.1. This variable is set per this description.

Values:

| <code>pse_allocated_pwr_pri/sec</code> | <code>pse_initial_value_alt(X)</code> |
|----------------------------------------|---------------------------------------|
| 1                                      | 39                                    |
| 2                                      | 65                                    |
| 3                                      | 130                                   |
| 4                                      | 255                                   |
| 5                                      | 356                                   |

**pse\_power\_update**

A variable that is set when the `PSEAllocatedPowerValue` in the DLL state diagram in Figure 145–40 has been updated.

Values:

|        |                                                                   |
|--------|-------------------------------------------------------------------|
| FALSE: | The value of <code>PSEAllocatedPowerValue</code> has not changed. |
| TRUE:  | The value of <code>PSEAllocatedPowerValue</code> has changed.     |

**pse\_power\_update\_pri**

A variable that is set when the `PSEAllocatedPowerValue_alt(X)` in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated.

Values:

|        |                                                                          |
|--------|--------------------------------------------------------------------------|
| FALSE: | The value of <code>PSEAllocatedPowerValue_alt(X)</code> has not changed. |
| TRUE:  | The value of <code>PSEAllocatedPowerValue_alt(X)</code> has changed.     |

**pse\_power\_update\_sec**

A variable that is set when the `PSEAllocatedPowerValue_alt(X)` in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated.

Values:

|        |                                                                          |
|--------|--------------------------------------------------------------------------|
| FALSE: | The value of <code>PSEAllocatedPowerValue_alt(X)</code> has not changed. |
| TRUE:  | The value of <code>PSEAllocatedPowerValue_alt(X)</code> has changed.     |

sig\_type

A variable generated from the do\_cxn\_chk function of the PSE state diagram in Figure 145–13, which indicates if the PSE is connected to a single-signature PD or a dual-signature PD.

Values:

- invalid: Neither a single-signature PD nor a dual-signature PD connection check signature has been found. This includes an open circuit condition.
- single: The PSE has determined there is a single-signature PD configuration connected to the PI.
- dual: The PSE has determined there is a dual-signature PD configuration connected to the PI.

twopairmode

Alias for the following term: (alt\_pwrd\_pri ^ alt\_pwrd\_sec)

A summary cross-references between the Power over Ethernet classification local and remote object class attributes and the PSE power control state diagrams, including the direction of the mapping, is provided in Table 145–38.

### 145.5.3.2.3 Functions

do\_autoclass\_measure

A function defined in the PSE state diagram, which measures  $P_{\text{Autoclass}}$  as defined in 145.2.8.2.

do\_pse\_power\_review

This function evaluates the power allocation or budget of the PSE based on local system changes or changes of the PD requested power value.

The function returns the following variable:

pse\_new\_value:

The new maximum power value that the PSE expects the PD to draw in units of 0.1 W.

Valid values: 1 through 999, and 0xACAC

do\_pse\_power\_review\_alt(X)

This function evaluates the power allocation or budget of the PSE based on local system changes.

The function returns the following variable:

pse\_new\_value\_alt(X):

The new maximum power value that the PSE expects the PD to draw in units of 0.1 W.

#### 145.5.3.2.4 Attribute to state diagram variable mapping

Table 145–38 shows the mapping between state diagram variables and Clause 30 attributes for PSEs.

**Table 145–38—Attribute to state diagram variable cross reference for PSEs**

| Attribute                                     | Mapping | State diagram variable                    |
|-----------------------------------------------|---------|-------------------------------------------|
| <b>oLldpXdot3LocSystemsGroup Object Class</b> |         |                                           |
| aLldpXdot3LocPDRRequestedPowerValue           | ⇐       | PDRRequestedPowerValueEcho                |
| aLldpXdot3LocPSEAllocatedPowerValue           | ⇐       | PSEAllocatedPowerValue                    |
| aLldpXdot3LocReady                            | ⇐       | pse_dll_ready                             |
| aLldpXdot3LocPSEAutoclassSupport              | ⇐       | PSEAutoclassSupport                       |
| aLldpXdot3LocAutoclassCompleted               | ⇐       | PSEAutoclassCompleted                     |
| aLldpXdot3LocPDRRequestedPowerValueA          | ⇐       | PDRRequestedPowerValueEcho_alt(A)         |
| aLldpXdot3LocPDRRequestedPowerValueB          | ⇐       | PDRRequestedPowerValueEcho_alt(B)         |
| aLldpXdot3LocPSEAllocatedPowerValueA          | ⇐       | PSEAllocatedPowerValue_alt(A)             |
| aLldpXdot3LocPSEAllocatedPowerValueB          | ⇐       | PSEAllocatedPowerValue_alt(B)             |
| <b>oLldpXdot3RemSystemsGroup Object Class</b> |         |                                           |
| aLldpXdot3RemPDRRequestedPowerValue           | ⇒       | MirroredPDRRequestedPowerValue            |
| aLldpXdot3RemPSEAllocatedPowerValue           | ⇒       | MirroredPSEAllocatedPowerValueEcho        |
| aLldpXdot3RemAutoclassRequest                 | ⇒       | MirroredPDAutoclassRequest                |
| aLldpXdot3RemPDRRequestedPowerValueA          | ⇒       | MirroredPDRRequestedPowerValue_alt(A)     |
| aLldpXdot3RemPDRRequestedPowerValueB          | ⇒       | MirroredPDRRequestedPowerValue_alt(B)     |
| aLldpXdot3RemPSEAllocatedPowerValueA          | ⇒       | MirroredPSEAllocatedPowerValueEcho_alt(A) |
| aLldpXdot3RemPSEAllocatedPowerValueB          | ⇒       | MirroredPSEAllocatedPowerValueEcho_alt(B) |