INTERNATIONAL STANDARD

ISO/IEC/IEEE 8802-3

Second edition
2017-03-01

AMENDMENT 9
2018-10

Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements —

Part 3: Standard for Ethernet

AMENDMENT 9: Physical layer specifications and management parameters for 1000 Mb/s operation over plastic optical fiber

Technologies de l'information — Télécommunications et échange d'information entre systèmes — Réseaux locaux et métropolitains — Prescriptions spécifiques —

Partie 3: Norme pour Ethernet

AMENDEMENT 9

Reference number
ISO/IEC/IEEE 8802-3:2017/Amd.9:2018(E)

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Published in Switzerland

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IEEE Std 802.3bv™-2017
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
IEEE Std 802.3bq™-2016,
IEEE Std 802.3bp™-2016,
IEEE Std 802.3br™-2016,
IEEE Std 802.3bn™-2016,
IEEE Std 802.3bz™-2016, and
IEEE Std 802.3bu™-2016)

IEEE Standard for Ethernet

Amendment 9: Physical Layer Specifications and Management Parameters for 1000 Mb/s Operation Over Plastic Optical Fiber

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 14 February 2017
IEEE-SA Standards Board

Abstract: A family of three point-to-point physical layers (PHYs) for 1000 Mb/s operation over duplex plastic optical fiber (POF) and related management parameters are specified by this amendment to IEEE Std 802.3-2015.

Keywords: 1000BASE-H, 1000BASE-RHA, 1000BASE-RHB, 1000BASE-RXC, amendment, BASE-H, EEE, Energy Efficient Ethernet, IEEE 802.3™, IEEE 802.3bv™, PCS, Physical Coding Sublayer, Physical Medium Attachment sublayer, Physical Medium Dependent sublayer, plastic optical fiber, PMA, PMD, POF

The Institute of Electrical and Electronics Engineers, Inc.
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Print: ISBN 978-5044-3721-9 STD22413
PDF: ISBN 978-1-5044-3722-6 STDPD22413

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Introduction

This introduction is not part of IEEE Std 802.3bv-2017, IEEE Standard for Ethernet—Amendment 9: Physical Layer Specifications and Management Parameters for 1000 Mb/s Operation Over Plastic Optical Fiber

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bv-2017 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw™-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by™-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq™-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp™-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br™-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn™-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

IEEE Std 802.3bz™-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu™-2016

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

IEEE Std 802.3bv-2017

Amendment 9—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 115 and Annex 115A. This amendment adds point-to-point 1000 Mb/s Physical Layer (PHY) specifications and management parameters for operation on duplex plastic optical fiber (POF) targeting use in automotive, industrial, home-network, and other applications.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 9: Physical Layer Specifications and Management Parameters for 1000 Mb/s Operation Over Plastic Optical Fiber

1. Introduction

1.3 Normative references

Insert the following references in alphanumeric order:

IEC 60793-1-41:2010, Optical fibres—Part 1-41: Measurement methods and test procedures—Bandwidth.

IEC 60793-2-40:2009, Optical fibres—Part 2-40: Product specifications—Sectional specification for category A4 multimode fibres.

IEC 61300-2-4, Fibre optic interconnecting devices and passive components—Basic test and measurement procedures—Part 2-4: Tests—Fibre/cable retention.

IEC 61300-3-53, Fibre optic interconnecting devices and passive components—Basic test and measurement procedures—Part 3-53: Examinations and measurements—Encircled angular flux (EAF) measurement method based on two-dimensional far field data from step index multimode waveguide (including fibre).

ISO/IEC 14763-3:2014, Information technology—Implementation and operation of customer premises cabling—Part 3: Testing of optical fibre cabling.

1.4 Definitions

Insert the following new definition after 1.4.22 "1000BASE-CX":

1.4.22a 1000BASE-H: IEEE 802.3 PCS and PMA sublayers for 1000 Mb/s Ethernet that support PMDs using duplex plastic optical fiber. (See IEEE Std 802.3, Clause 115.)

Insert the following new definitions after 1.4.26 "1000BASE-PX":

1.4.26a 1000BASE-RHA: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using 1000BASE-H encoding and red light (approximately 650 nm) PMD tailored for home-network and other consumer application requirements. (See IEEE Std 802.3, Clause 115.)

1.4.26b 1000BASE-RHB: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using 1000BASE-H encoding and red light (approximately 650 nm) PMD tailored for industrial application requirements. (See IEEE Std 802.3, Clause 115.)

1.4.26c 1000BASE-RHC: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using 1000BASE-H encoding and red light (approximately 650 nm) PMD tailored for automotive application requirements. (See IEEE Std 802.3, Clause 115.)

1.4.26d 1000BASE-RHx: IEEE 802.3 specification for 1000 Mb/s Ethernet using duplex plastic optical fiber and red light (approximately 650 nm) with unspecified optical power budget (optical power budget is defined by the specific PMD type). (See IEEE Std 802.3, Clause 115.)

Change the definition 1.4.91 as follows:

1.4.91 64B/65B transmission code: A block oriented encoding where 64-bit blocks are prepended with a single bit to indicate whether the block contains only data or a mix of data and control information. The details of each 64B/65B encoding are specific to the PCS. (See IEEE Std 802.3, Clause 55, and Clause 115.)

Insert the following new definition after 1.4.245 "jumper cable assembly":

1.4.245a Kojiri-safe: A property of the mechanical design for receptacles and mated plugs to protect sensitive functional elements, especially fiber optic ferrules and receptacles. Also called scoop-proof.

Insert the following new definition after 1.4.277a "MultiGBASE-T" (inserted by IEEE Std 802.3bq-2016):

1.4.277b multi-level coset code (MLCC): A forward error correcting technique consisting of splitting the information bit stream among several levels, for each one a binary component code (possibly none) is employed with an error correction capability according to the reliability of each level in data transmission over noisy channels. (See IEEE Std 802.3, Clause 115.)

Insert the following new definitions after 1.4.326 "Physical Coding Sublayer":

1.4.326a physical data block (PDB): The minimum data unit of 65 bits used to encode the GMII data stream. (See IEEE Std 802.3, Clause 115.)

1.4.326b physical header data (PHD): Side information block embedded inside a Transmit Block that is used to exchange control and for negotiation of PCS and PMA parameters between two link partners. (See IEEE Std 802.3, Clause 115.)

1.4.326c physical header subframe (PHS): Block of symbols that are the result of adding error detection and error correction parities plus modulation to PHD (See IEEE Std 802.3, Clause 115.)

Change the definition of 1.4.401 as follows:

1.4.401 Tomlinson-Harashima precoder (THP): A precoding technique for intersymbol interference mitigation. (See IEEE Std 802.3, Clause 55, and Clause 115.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

BCH	Bose, Ray-Chaudhuri, Hocquenghem
LED	light emitting diode
MLCC	multi-level coset code
PDB	physical data block
PHD	physical header data
PHS	physical header subframe
POF	plastic optical fiber
SI-POF	step index plastic optical fiber

30. Management

30.3.2.1.2 aPhyType

Insert the following after 1000BASE-X in APPROPRIATE SYNTAX:

APPROPRIATE SYNTAX:

...
1000BASE-H Clause 115 1000 Mb/s PAM16-THP

30.3.2.1.3 aPhyTypeList

Insert the following after 1000BASE-X in APPROPRIATE SYNTAX:

APPROPRIATE SYNTAX:

...
1000BASE-H Clause 115 1000 Mb/s PAM16-THP

30.5.1.1.2 aMAUType

Insert the following enumerations after 1000BASE-KX in APPROPRIATE SYNTAX:

APPROPRIATE SYNTAX:

...
1000BASE-RHA Plastic optical fiber PHY as specified in Clause 115.
1000BASE-RHB Plastic optical fiber PHY as specified in Clause 115.
1000BASE-RHC Plastic optical fiber PHY as specified in Clause 115.

30.5.1.1.4 aMediaAvailable

Insert into the third paragraph in BEHAVIOUR DEFINED AS section of 30.5.1.1.4 after the second sentence (and before the sentences inserted by IEEE Std 802.3bw-2015 and IEEE Std 802.3bp-2016) the following:

BEHAVIOUR DEFINED AS:

...
For 1000BASE-RHx, a link_status (see 115.3.5.4 and 45.2.3.47d.3) of OK maps to the enumeration "available" and a link_status of FAIL maps to the enumeration "not available"

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the 1.22 through 1.29 Reserved row (as modified by IEEE Std 802.3bz-2016) and insert a new row above as follows:

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.22	BASE-H PMA/PMD extended ability	45.2.1.14d
~~1.22~~1.23 through 1.29	Reserved	

Change the 1.740 through 1.1099 Reserved row of Table 45-3 and insert new rows as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.740 through ~~1.1099~~1.899	Reserved	
1.900	BASE-H PMA/PMD control	45.2.1.117a
1.901 through 1.1099	Reserved	

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the below 1 1 0 1 0 x = reserved line in the Description of bits 1.7.5:0 of Table 45–7 to be two lines, including new footnote c (footnote b inserted by IEEE Std 802.3bp-2016) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 ~~1 1 0 1 0 x = reserved~~ 1 1 0 1 0 1 = reserved 1 1 0 1 0 0 = BASE-H PMA/PMD[c]	R/W

[a]R/W = Read/Write, RO = Read only
[b]If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.
[c]If BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected.

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Change Bit 1.11.15 of Table 45-14 (as modified by IEEE Std 802.3bz-2016), as follows (unchanged rows not shown):

Table 45–14—PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15	~~Reserved~~ BASE-H extended abilities	~~Value always zero~~1 = PMA/PMD has BASE-H extended abilities listed in register 1.22. 0 = PMA/PMD does not have BASE-H extended abilities	RO

[a]RO = Read Only

Insert new subclause 45.2.1.10.aaaa before 45.2.10.aaa (inserted by IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

45.2.1.10.aaaa BASE-H extended abilities (1.11.15)

When read as one, bit 1.11.15 indicates that the PMA/PMD has BASE-H extended abilities listed in register 1.22. When read as zero, bit 1.11.15 indicates that the PMA/PMD does not have BASE-H extended abilities.

Insert new subclause 45.2.1.14d and Table 45-17d after 45.2.1.14c (as inserted by IEEE Std 802.3bz-2016) as follows:

45.2.1.14d BASE-H PMA/PMD extended ability register (Register 1.22)

The assignment of bits in the BASE-H PMA/PMD extended ability register is shown in Table 45–17d. All of the bits in the BASE-H PMA/PMD extended ability register are read only; a write to the BASE-H PMA/PMD extended ability register shall have no effect.

Table 45–17d—BASE-H PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.22.15:3	Reserved	Value always 0	RO
1.22.2	1000BASE-RHC ability	1 = PMA/PMD is able to perform 1000BASE-RHC 0 = PMA/PMD is not able to perform 1000BASE-RHC	RO
1.22.1	1000BASE-RHB ability	1 = PMA/PMD is able to perform 1000BASE-RHB 0 = PMA/PMD is not able to perform 1000BASE-RHB	RO
1.22.0	1000BASE-RHA ability	1 = PMA/PMD is able to perform 1000BASE-RHA 0 = PMA/PMD is not able to perform 1000BASE-RHA	RO

[a]RO = Read Only

Insert new subclause 45.2.1.117a and Table 45-90a after 45.2.1.117 as follows:

45.2.1.117a BASE-H PMA/PMD control register (Register 1.900)

The assignment of bits in the BASE-H PMA/PMD control register is shown in Table 45–90a.

Table 45–90a—BASE-H PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.900.15:4	Reserved	Value always 0	RO
1.900.3:0	Type selection	3 2 1 0 1 x x x = Reserved 0 1 x x = Reserved 0 0 1 1 = Reserved 0 0 1 0 = 1000BASE-RHC 0 0 0 1 = 1000BASE-RHB 0 0 0 0 = 1000BASE-RHA	R/W

[a]RO = Read Only, R/W = Read Write

45.2.1.117a.1 Type selection (1.900.3:0)

Bits 1.900.3:0 are used to set the mode of operation. When these bits are set to 0000, the mode of operation is 1000BASE-RHA. When these bits are set to 0001, the mode of operation is 1000BASE-RHB. When these bits are set to 0010, the mode of operation is 1000BASE-RHC. Any attempt to configure a different value or a mode of operation not supported per register 1.22 shall have no effect.

45.2.3 PCS registers

Change the 3.420 through 3.1799 reserved row of Table 45-119 and insert new 1000BASE-H rows as follows (unchanged rows and footnotes not shown):

Table 45–119—PCS registers

Register address	Register name	Subclause
3.420 through ~~3.1799~~3.499	Reserved	
3.500	1000BASE-H OAM transmit control	45.2.3.47a
3.501 through 3.508	1000BASE-H OAM transmit message	45.2.3.47a
3.509	1000BASE-H OAM receive control	45.2.3.47b
3.510 through 3.517	1000BASE-H OAM receive message	45.2.3.47b
3.518	1000BASE-H PCS control	45.2.3.47c
3.519	1000BASE-H PCS status 1	45.2.3.47d
3.520	1000BASE-H PCS status 2	45.2.3.47e
3.521	1000BASE-H PCS status 3	45.2.3.47f
3.522	1000BASE-H PCS status 4	45.2.3.47g
3.523 through 3.1799	Reserved	

Insert 45.2.3.47a after 45.2.3.47 as follows:

45.2.3.47a 1000BASE-H OAM transmit registers (Registers 3.500 through 3.508)

Registers 3.500 through 3.508 are used to transmit messages over the 1000BASE-H OAM channel established between two link partners (see 115.9.1). The 1000BASE-H OAM message is part of the physical header data (PHD) defined for 1000BASE-H (see Table 115–6).

The transmit registers are used to compose a 1000BASE-H OAM message and to control its transmission to the link partner. Register 3.500 contains control, status, identification, and the beginning of a 1000BASE-H OAM message. Eight additional registers (3.501 through 3.508) hold the remainder of the 1000BASE-H OAM message.

The assignment of bits in the 1000BASE-H OAM transmit registers is shown in Table 45–160a.

45.2.3.47a.1 TXO_REQ (3.500.15)

Bit 3.500.15 set to one requests the 1000BASE-H based PHY to transmit the 1000BASE-H OAM message written to registers 3.500 through 3.508. Bit 3.500.15 is set to zero by the 1000BASE-H based PHY to indicate that the 1000BASE-H OAM message has been accepted for transmission, and that the 1000BASE-H OAM transmit message registers are free to accept a new 1000BASE-H OAM message.

Bit 3.500.15, together with bits 3.500.14 (TXO_PHYT), 3.500.13 (TXO_MERT), and 3.500.12 (TXO_MSGT), indicates the status of the 1000BASE-H OAM transmission channel (see 115.9.2).

Table 45–160a—1000BASE-H OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.500.15	TXO_REQ	1 = Transmission of a 1000BASE-H OAM message is pending; write as 1 to request transmission 0 = 1000BASE-H transmit registers are available for a new 1000BASE-H OAM message	R/W, SC
3.500.14	TXO_PHYT	The identifier of the last 1000BASE-H OAM message received by the remote PHY	RO
3.500.13	TXO_MERT	The identifier of the last 1000BASE-H OAM message read by the STA attached to the remote PHY	RO
3.500.12	TXO_MSGT	1000BASE-H OAM message identifier; its value change with each new transmitted message	RO
3.500.11:0	TXO_DATA0	Transmit 1000BASE-H OAM message first 12 bits	R/W
3.501.15:0	TXO_DATA1	Transmit 1000BASE-H OAM message 16-bit data word 1	R/W
3.502.15:0	TXO_DATA2	Transmit 1000BASE-H OAM message 16-bit data word 2	R/W
3.503.15:0	TXO_DATA3	Transmit 1000BASE-H OAM message 16-bit data word 3	R/W
3.504.15:0	TXO_DATA4	Transmit 1000BASE-H OAM message 16-bit data word 4	R/W
3.505.15:0	TXO_DATA5	Transmit 1000BASE-H OAM message 16-bit data word 5	R/W
3.506.15:0	TXO_DATA6	Transmit 1000BASE-H OAM message 16-bit data word 6	R/W
3.507.15:0	TXO_DATA7	Transmit 1000BASE-H OAM message 16-bit data word 7	R/W
3.508.15:0	TXO_DATA8	Transmit 1000BASE-H OAM message 16-bit data word 8	R/W

[a]R/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.3.47a.2 TXO_PHYT (3.500.14)

Bit 3.500.14 reflects the value of the bit TXO_MSGT in the last 1000BASE-H OAM message received by the remote 1000BASE-H based PHY.

45.2.3.47a.3 TXO_MERT (3.500.13)

Bit 3.500.13 reflects the value of the bit TXO_MSGT in the last 1000BASE-H OAM message read by the STA attached to the remote 1000BASE-H based PHY.

45.2.3.47a.4 TXO_MSGT (3.500.12)

Bit 3.500.12 is used for 1000BASE-H OAM message identification. Bit 3.500.12 is changed by the 1000BASE-H based PHY when it accepts a new 1000BASE-H OAM message for transmission (simultaneously setting bit 3.500.15 to zero), acting as a 1-bit sequence number.

45.2.3.47a.5 TXO_DATAx (Bits 3.500.11:0 and Registers 3.501 through 3.508)

Bits 3.500.11:0 (TXO_DATA0) contains the first 12 bits of a 1000BASE-H OAM message and registers 3.501 through 3.508 (TXO_DATA1 through TXO_DATA8) the remaining 128 bits of that 1000BASE-H OAM message.

TXO_DATA0 and TXO_DATA1 shall be a 28-bit 1000BASE-H OAM protocol identifier composed of a 24-bit Organizationally Unique Identifier (OUI) or Company ID (CID) followed by a 4-bit protocol number; where TXO_DATA0[10:0] = OUI[23:12], TXO_DATA1[15:3] = OUI[11:0], and TXO_DATA1[3:0] = protocol number. The content of TXO_DATA2 to TXO_DATA8 is vendor specific to the assignee of the OUI or CID.

45.2.3.47b 1000BASE-H OAM receive registers (Registers 3.509 through 3.517)

Registers 3.509 through 3.517 store messages received over the 1000BASE-H OAM channel established between two link partners (see 115.9.3). Register 3.509 contains status information, identification, and the first 12 bits of a 1000BASE-H OAM message, and registers 3.510 through 3.517 the following 128 bits of the received 1000BASE-H OAM message.

The assignment of bits in the 1000BASE-H OAM receive registers is shown in Table 45–160b.

Table 45–160b—1000BASE-H OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.509.15	RXO_VAL	1 = A new 1000BASE-H OAM message has arrived 0 = No new 1000BASE-H OAM message arrived since either last message was read or PMA reset	RO
3.509.14:13	Reserved	Value always 0	RO
3.509.12	RXO_MSGT	Identifier of the received 1000BASE-H OAM message	RO
3.509.11:0	RXO_DATA0	Receive 1000BASE-H OAM message first 12 bits	RO
3.510.15:0	RXO_DATA1	Receive 1000BASE-H OAM message 16-bit data word 1	RO
3.511.15:0	RXO_DATA2	Receive 1000BASE-H OAM message 16-bit data word 2	RO
3.512.15:0	RXO_DATA3	Receive 1000BASE-H OAM message 16-bit data word 3	RO
3.513.15:0	RXO_DATA4	Receive 1000BASE-H OAM message 16-bit data word 4	RO
3.514.15:0	RXO_DATA5	Receive 1000BASE-H OAM message 16-bit data word 5	RO
3.515.15:0	RXO_DATA6	Receive 1000BASE-H OAM message 16-bit data word 6	RO
3.516.15:0	RXO_DATA7	Receive 1000BASE-H OAM message 16-bit data word 7	RO
3.517.15:0	RXO_DATA8	Receive 1000BASE-H OAM message 16-bit data word 8	RO

[a]RO = Read only

45.2.3.47b.1 RXO_VAL (3.509.15)

The 1000BASE-H based PHY sets bit 3.509.15 to one to indicate the reception of a new 1000BASE-H OAM message. The 1000BASE-H based PHY sets bit 3.509.15 to zero when the last register (3.517) containing the 1000BASE-H OAM message is read (see Figure 115–43). The 1000BASE-H based PHY does not update the receive message registers until the message is read by STA as indicated by a read of register 3.517.

45.2.3.47b.2 RXO_MSGT (3.509.12)

Bit 3.509.12 is used for message identification. Bit 3.509.12 changes with every new received 1000BASE-H OAM message, acting as a 1-bit sequence number.

45.2.3.47b.3 RXO_DATAx (Bits 3.509.11:0 and Registers 3.510 through 3.517)

Bits 3.509.11:0 (RXO_DATA0) contains the first 12 bits of a received 1000BASE-H OAM message, and registers 3.510 through 3.517 (RXO_DATA1 through RXO_DATA8) the remaining 128 bits of that received 1000BASE-H OAM message.

45.2.3.47c 1000BASE-H PCS control register (Register 3.518)

The assignment of bits in the 1000BASE-H PCS control register is shown in Table 45–160c.

Table 45–160c—1000BASE-H PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.518.15:13	Operation mode	15 14 13 0 0 0 = Normal operation 0 0 1 = Test mode 1 0 1 0 = Test mode 2 0 1 1 = Test mode 3 1 0 0 = Test mode 4 1 0 1 = Test mode 5 1 1 0 = Test mode 6 1 1 1 = Reserved	R/W
3.518.12:10	Loopback mode	12 11 10 0 0 0 = No loopback 0 0 1 = GMII level loopback 0 1 0 = PMD interface level loopback 0 1 1 = Line loopback 1 x x = Reserved	R/W
3.518.9:2	Reserved	Value always 0	RO
3.518.1	1000BASE-H OAM enable	1 = Enable 1000BASE-H OAM functionality 0 = Disable 1000BASE-H OAM functionality	R/W
3.518.0	EEE enable	1 = Enable LPI mode 0 = Disable LPI mode	R/W

[a]R/W = Read/Write, RO = Read only

45.2.3.47c.1 Operation mode (3.518.15:13)

Bits 3.518.15:13 shall have a default value of binary 000, selecting normal 1000BASE-H operation. A value of binary 001 through binary 110 in bits 3.518.15:13 shall select the test mode as specified in Table 45–160c with behavior as defined in 115.5.

45.2.3.47c.2 Loopback mode (3.518.12:10)

Bits 3.518.12:10 shall select one of the loopback modes defined in 115.10. Bits 3.518.12:10 shall have a default value of binary 000 (no loopback operation). Loopback modes are only available when a 1000BASE-H based PHY is in the normal operation mode (no test mode is selected in 3.518.15:13).

45.2.3.47c.3 1000BASE-H OAM enable (3.518.1)

Bit 3.518.1 controls establishing the 1000BASE-H OAM channel with the link partner (115.9). If the 1000BASE-H based PHY does not have 1000BASE-H OAM ability (bit 3.519.1 = 0), setting bit 3.518.1 shall have no effect. Setting bit 3.518.1 to zero shall prevent establishment of a 1000BASE-H OAM channel with the link partner. Changes in a 1000BASE-H OAM enable value shall only take effect after a PMA reset. Bit 3.518.1 has no specified default value.

45.2.3.47c.4 EEE enable (3.518.0)

Setting bit 3.518.0 to one enables 1000BASE-H based PHY EEE capability (see 115.4). Setting bit 3.518.0 to zero shall prevent establishment of EEE operation with the link partner. If the 1000BASE-H based PHY does not have EEE ability (bit 3.519.0 = 0), setting bit 3.518.0 shall have no effect. Changes in EEE enable value shall only take effect after a PMA reset. Bit 3.518.0 has no specified default value.

45.2.3.47d 1000BASE-H PCS status 1 register (Register 3.519)

The assignment of bits in the 1000BASE-H PCS status 1 register is shown in Table 45–160d.

Table 45–160d— 1000BASE-H PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.519.15	Local receiver status	1 = The local receive operation is reliable 0 = The local receive operation is unreliable	RO
3.519.14	Remote receiver status	1 = The receive operation of the remote PHY is reliable 0 = The receive operation of the remote PHY is unreliable	RO
3.519.13	Link status	1 = A bidirectional reliable link is established 0 = A bidirectional reliable link is not established	RO, LL
3.519.12	Local PHD reception status	1 = PHD reception is reliable for the local PHY 0 = PHD reception is unreliable for the local PHY	RO
3.519.11	Remote PHD reception status	1 = PHD reception is reliable for the remote PHY 0 = PHD reception is unreliable for the remote PHY	RO
3.519.10	PHD lock status	1 = PHD transmission and reception are reliable 0 = PHD transmission or reception are unreliable	RO, LL
3.519.9	THP lock status	1 = THP is initialized; payload data is received with THP processing 0 = THP is not initialized	RO
3.519.8	Tx Assert LPI received	1 = Tx PCS has received LPI 0 = LPI not received by Tx PCS	RO, LH
3.519.7	Rx Assert LPI generated	1 = Rx PCS has generated LPI 0 = LPI not generated by Rx PCS	RO, LH
3.519.6	Tx LPI indication	1 = Tx PCS is currently transmitting LPI 0 = Tx PCS is not currently transmitting LPI	RO
3.519.5	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = Rx PCS is not currently receiving LPI	RO
3.519.4	Reserved	Value always 0	RO

Table 45–160d— 1000BASE-H PCS status 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.519.3	Remote 1000BASE-H OAM ability	1 = The remote PHY has 1000BASE-H OAM ability and it is enabled 0 = The remote PHY does not have 1000BASE-H OAM ability or it is disabled	RO
3.519.2	Remote EEE ability	1 = The remote PHY has EEE ability and it is enabled 0 = The remote PHY does not have EEE ability or it is disabled	RO
3.519.1	1000BASE-H OAM ability	1 = The PHY has 1000BASE-H OAM ability 0 = The PHY does not have 1000BASE-H OAM ability	RO
3.519.0	EEE ability	1 = The PHY has EEE ability 0 = The PHY does not have EEE ability	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.47d.1 Local receiver status (3.519.15)

Bit 3.519.15 reflects the value of the state variable loc_rcvr_status as determined by the PHY quality monitor state diagram (see 115.3.5.1).

45.2.3.47d.2 Remote receiver status (3.519.14)

Bit 3.519.14 reflects the value of the state variable rem_rcvr_status as determined by the link monitor state diagram (see 115.3.5.1).

45.2.3.47d.3 Link status (3.519.13)

Bit 3.519.13 reflects the value of the state variable link_status as determined by the link monitor state diagram (see 115.3.5.1). Bit 3.519.13 shall have latching low behavior. Bit 1.1.2, bit 3.1.2, and bit 3.519.13 are identical for 1000BASE-H; a read to any of these three bits shall release the latch for all the bits.

45.2.3.47d.4 Local PHD reception status (3.519.12)

Bit 3.519.12 reflects the value of the state variable loc_rcvr_hdr_lock as determined by the local PHD reception monitor state diagram (see 115.3.5.1).

45.2.3.47d.5 Remote PHD reception status (3.519.11)

Bit 3.519.11 reflects the value of the state variable rem_rcvr_hdr_lock as determined by the remote PHD reception monitor state diagram (see 115.3.5.1).

45.2.3.47d.6 PHD lock status (3.519.10)

Bit 3.519.10 reflects the value of the state variable rcvr_hdr_lock as determined by the PHD monitor state diagram (see 115.3.5.1). Bit 3.519.10 shall have latching low behavior.

45.2.3.47d.7 THP lock status (3.519.9)

Bit 3.519.9 reflects the value of the state variable rcvr_thp_lock as determined by the adaptive THP REQ state diagram (see 115.3.6.1).

45.2.3.47d.8 Tx Assert LPI received (3.519.8)

When read as a one, bit 3.519.8 indicates that the transmit 1000BASE-H PCS has received Assert LPI signaling from the TX GMII one or more times since the register was last read. When read as a zero, bit 3.519.8 indicates that the 1000BASE-H PCS transmitter has not received Assert LPI. Bit 3.519.8 shall have latching high behavior. Bit 3.519.8 is a copy of bit 3.1.11; a read of either bit shall release the latch for all the bits.

45.2.3.47d.9 Rx Assert LPI generated (3.519.7)

When read as a one, bit 3.519.7 indicates that the receive 1000BASE-H PCS has generated Assert LPI on the RX GMII one or more times since the register was last read. When read as a zero, bit 3.519.7 indicates that the 1000BASE-H PCS receiver has not generated Assert LPI on the RX GMII. Bit 3.519.7 shall have latching high behavior. Bit 3.519.7 is a copy of bit 3.1.10; a read of either bit shall release the latch for all the bits.

45.2.3.47d.10 Tx LPI indication (3.519.6)

Bit 3.519.6 indicates the current LPI mode status of the local 1000BASE-H based PHY transmit path. When read as one, the PHY transmitter is currently in LPI mode (transmitting refresh and quiet). When read as zero, the PHY transmitter is not in LPI mode (see 115.4.1). Bit 3.519.6 is a copy of bit 3.1.9.

45.2.3.47d.11 Rx LPI indication (3.519.5)

Bit 3.519.5 indicates the current LPI mode status of the local 1000BASE-H based PHY receive path. When read as a one, the PHY is receiving LPI mode signals (refresh and quiet). When read as a zero, the PHY is not receiving LPI mode signals (see 115.4.2). Bit 3.519.5 is a copy of bit 3.1.8.

45.2.3.47d.12 Remote 1000BASE-H OAM ability (3.519.3)

Bit 3.519.3 indicates the 1000BASE-H OAM ability of the remote PHY received in the PHD field PHD.CAP.OAM (see Table 115–6). When read as one, bit 3.519.3 indicates the remote PHY has both 1000BASE-H OAM ability and the 1000BASE-H OAM is enabled. When read as zero, bit 3.519.3 indicates that the remote PHY either does not have 1000BASE-H OAM ability or 1000BASE-H OAM is disabled.

45.2.3.47d.13 Remote EEE ability (3.519.2)

Bit 3.519.2 indicates the EEE ability of the remote PHY received in the PHD field PHD.CAP.LPI (see Table 115–6). When read as one, bit 3.519.2 indicates the remote PHY has both EEE ability and EEE is enabled. When read as zero, bit 3.519.2 indicates that the remote PHY either does not have EEE ability or EEE is disabled.

45.2.3.47d.14 1000BASE-H OAM ability (3.519.1)

Bit 3.519.1 indicates the 1000BASE-H OAM ability of the 1000BASE-H based PHY (see 115.9). When read as one, bit 3.519.1 indicates that the 1000BASE-H based PHY supports the 1000BASE-H OAM protocol. When read as zero, bit 3.519.1 indicates the 1000BASE-H based PHY does not support the 1000BASE-H OAM protocol.

A PHY indicating in bit 3.519.1 support of 1000BASE-H OAM shall provide the functions of registers 3.500 through 3.517 as specified in 115.9.

45.2.3.47d.15 EEE ability (3.519.0)

Bit 3.519.0 indicates the EEE ability of the 1000BASE-H based PHY. When read as one, bit 3.519.0 indicates that the 1000BASE-H based PHY implements EEE, and is able to enter LPI mode (see 115.4). When read as zero, bit 3.519.0 indicates the 1000BASE-H based PHY does not implement EEE operation.

45.2.3.47e 1000BASE-H PCS status 2 register (Register 3.520)

The assignment of bits in the 1000BASE-H PCS status 2 register is shown in Table 45–160e.

Table 45–160e—1000BASE-H PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.520.15:8	Reserved	Value always 0	RO
3.520.7:0	Local link margin	Reports the local link margin	RO

[a]RO = Read only

45.2.3.47e.1 Local link margin (3.520.7:0)

Bits 3.520.7:0 indicate the link margin of the receiver. Link margin is defined in 115.3.7.2 and is fixed-point formatted (8,3). See 115.3.8 for fixed-point format definition.

45.2.3.47f 1000BASE-H PCS status 3 register (Register 3.521)

The assignment of bits in the 1000BASE-H PCS status 3 register is shown in Table 45–160f.

Table 45–160f—1000BASE-H PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.521.15:8	Reserved	Value always 0	RO
3.521.7:0	Remote link margin	Link margin reported by the link partner	RO

[a]RO = Read only

45.2.3.47f.1 Remote link margin (3.521.7:0)

Bits 3.521.7:0 report the link margin of the remote PHY receiver as it is received in the PHD field PHD.RX.LINKMARGIN (see Table 115–6). Link margin is defined in 115.3.7.2 and is fixed-point formatted (8,3). See 115.3.8 for fixed-point format definition.

45.2.3.47g 1000BASE-H PCS status 4 register (Register 3.522)

The assignment of bits in the 1000BASE-H PCS status 4 register is shown in Table 45–160g.

Bits 3.522.15:0 are a 16-bit counter that counts the number of bits received with value 1 at the output of the binary descrambler, when the 1000BASE-H based PHY receiver is operating in test mode 1. These bits shall be reset to all zeros when the counter is read. The counter shall be held at all ones in the case of overflow.

Table 45–160g—1000BASE-H PCS status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.522.15:0	BER test mode counter	A 16-bit counter used when operating in test mode 1	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface[1]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.2 PMA/PMD MMD options

Insert the following row at the end of table 45.5.3.2 PMA/PMD MMD options (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bq-2016):

Item	Feature	Subclause	Value/Comment	Status	Support
*BH	Implementation of a BASE-H PMA/PMD			PMA:O	Yes [ ] No [ ]

45.5.3.3 PMA/PMD management functions

Insert PICS items MM150 through MM151 at the bottom of the table in 45.5.3.3 (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bp-2016) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MM150	Writes to the register 1.22 have no effect			PMA:O	Yes [ ] N/A [ ]
MM151	Writes of reserved values or modes of operation different of those advertised by register 1.22, to bits 1.900.3:0 have no effect			BH:M	Yes [ ] N/A [ ]

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.3.6 PCS options

Insert the following rows at the end of table 45.5.3.6 PCS options:

Item	Feature	Subclause	Value/Comment	Status	Support
*BHOAM	1000BASE-H OAM channel implementation	45.2.3.47a and 45.2.3.47b		PCS:O	Yes [ ] No [ ]

45.5.3.7 PCS management functions

Insert PICS items RM137 through RM156 at the bottom of the table in 45.5.3.7 (as modified by IEEE Std 802.3bp-2016) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
RM137	1000BASE-H OAM message format to be transmitted	45.2.3.47a.5	TXO_DATA0[10:0] = OUI[23:12], TXO_DATA1[15:3] = OUI[11:0], and TXO_DATA1[3:0] = protocol number. Content of TXO_DATA2 to TXO_DATA8 is vendor specific per OUI or Company ID	PCS *BHOAM :M	Yes [ ] N/A [ ]
RM138	Default operation mode	45.2.3.47c.1	Default value of bits 3.518.15:13 is binary 000 (normal mode)	PCS:M	Yes [ ] N/A [ ]
RM139	Test operation modes	45.2.3.47c.1	Values binary 001 through binary 110 of bits 3.518.15:13 select test modes of Table 45–160c, with behavior per 115.5	PCS:M	Yes [ ] N/A [ ]
RM140	Default loopback mode	45.2.3.47c.2	Default value of bits 3.518.12:10 is binary 000 (no loopback operation)	PCS:M	Yes [ ] N/A [ ]
RM141	Loopback modes	45.2.3.47c.2	Bits 3.518.12:10 select loopback modes with behavior per 115.10	PCS:M	Yes [ ] N/A [ ]
RM142	1000BASE-H OAM conditional enable	45.2.3.47c.3	Write a 1 to bit 3.518.1 only produces effect if bit 3.519.1 is read as 1	PCS *BHOAM :M	Yes [ ] N/A [ ]
RM143	1000BASE-H OAM disable	45.2.3.47c.3	Write a 0 to bit 3.518.1 prevents 1000BASE-H OAM channel establishment with link partner	PCS *BHOAM :M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM144	1000BASE-H OAM enable change effect	45.2.3.47c.3	Changes in the value of bit 3.518.1 only takes effect after PMA reset	PCS *OAM:M	Yes [ ] N/A [ ]
RM145	EEE conditional enable	45.2.3.47c.4	Write a 1 to bit 3.518.0 only produces effect if bit 3.519.0 is read as 1	PCS *EEE:M	Yes [ ] N/A [ ]
RM146	EEE disable	45.2.3.47c.4	Write a 0 to bit 3.518.0 prevents EEE operation with link partner	PCS *EEE:M	Yes [ ] N/A [ ]
RM147	EEE enable change effect	45.2.3.47c.4	Changes in the value of bit 3.518.0 only takes effect after PMA reset	PCS *EEE:M	Yes [ ] N/A [ ]
RM148	Link status behavior	45.2.3.47d.3	Bit 3.519.13 has latching low behavior	PCS:M	Yes [ ] N/A [ ]
RM149	Link status mirroring	45.2.3.47d.3	Bit 1.1.2, bit 3.1.2, and bit 3.519.13 reflect same state variable link_status and a read of any of them releases the latch of all the bits	PCS:M	Yes [ ] N/A [ ]
RM150	PHD lock status behavior	45.2.3.47d.6	Bit 3.519.10 has latching low behavior	PCS:M	Yes [ ] N/A [ ]
RM151	Tx Assert LPI received behavior	45.2.3.47d.8	Bit 3.519.8 has latching high behavior	PCS *EEE:M	Yes [ ] N/A [ ]
RM152	Tx Assert LPI received mirroring	45.2.3.47d.8	Bit 3.519.8 is a copy of bit 3.1.11 and a read of any of them releases the latch of all the bits	PCS *EEE:M	Yes [ ] N/A [ ]
RM153	Rx Assert LPI generated behavior	45.2.3.47d.9	Bit 3.519.7 has latching high behavior	PCS *EEE:M	Yes [ ] N/A [ ]
RM154	Rx Assert LPI generated mirroring	45.2.3.47d.9	Bit 3.519.7 is a copy of bit 3.1.10 and a read of any of them releases the latch of all the bits	PCS *EEE:M	Yes [ ] N/A [ ]
RM155	1000BASE-H OAM ability	45.2.3.47d.14	Registers 3.500 through 3.517 are implemented and 3.519.1 reads as 1	PCS *BHOAM :M	Yes [ ] N/A [ ]
RM156	BER test mode counter is reset to all zeros when read	45.2.3.47g		PCS:M	Yes [ ] N/A [ ]
RM157	BER test mode counter holds all ones in case of overflow	45.2.3.47g		PCS:M	Yes [ ] N/A [ ]

78. Energy-Efficient Ethernet (EEE)

78.1.4 PHY types optionally supporting EEE

Insert new 1000BASE-RHx rows into Table 78-1 after the entry for 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016), and before the entry for 2.5GBASE-T (inserted by IEEE Std 802.3bz-2016) as follows:

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
1000BASE-RHA	115
1000BASE-RHB	115
1000BASE-RHC	115

78.2 LPI mode timing parameters descriptions

Insert new 1000BASE-RHx rows into Table 78-2 after the entry for 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016), and before the entry for 2.5GBASE-T (inserted by IEEE Std 802.3bz-2016) as follows:

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY Type	T_s (μs)		T_q (μs)		T_r (μs)	
	Min	Max	Min	Max	Min	Max
1000BASE-RHA	0	0	23.52	23.52	1.3	1.3
1000BASE-RHB	0	0	23.52	23.52	1.3	1.3
1000BASE-RHC	0	0	23.52	23.52	1.3	1.3

78.5 Communication link access latency

Insert new 1000BASE-RHx rows into Table 78-4 after 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016) as follows:

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY Type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (min) (μs)	$T_{phy\_shrink\_rx}$ (min) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
1000BASE-RHA		25	25	25	0	0
1000BASE-RHB		25	25	25	0	0
1000BASE-RHC		25	25	25	0	0

115. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer, types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC

115.1 Overview

1000BASE-H comprises a Physical Coding Sublayer (PCS) and a Physical Medium Attachment (PMA) sublayer that supports Physical Medium Dependent (PMD) sublayers for operation at 1000 Mb/s over duplex plastic optical fiber (POF) as the transmission medium. The following three port types with different PMDs are defined: 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC (collectively referred to as 1000BASE-RHx).

1000BASE-RHA specifications are driven by the requirements of home and other consumer networks. Connection of the PMD to the step index plastic optical fiber (SI-POF) medium is typically not a mated connector. Rather, a bare duplex cable is attached with a clamp in the PMD receptacle.

1000BASE-RHB specifications are driven by the requirements for industrial applications. Connection of PMD to the SI-POF medium is typically with a PMD receptacle and mated plug. A harsh environment is expected (e.g., extended temperature range, dust), and the connector is typically terminated in the field to facilitate flexible equipment interconnection layout.

1000BASE-RHC specifications are driven by requirements for automotive applications. Connection of PMD to the SI-POF medium is with a PMD receptacle and mated plug. PMD and in-line connectors and the cable have to support specific requirements for installation in a vehicle: Kojiri-safe, dust protection, vibration robustness, tensile strength, etc.

115.1.1 Features

The following are the features of the 1000BASE-H set of PHYs:

a) Specified to operate with the GMII (Clause 35).
b) Full duplex operation.
c) Support for BER of 10^{-12} or better.
d) Communication side-channel for PHY management, operations, administration, and maintenance between link partners.
e) Operation in automotive, industrial, and home network environments.

115.1.2 Conventions

The notation used in the state diagrams in this clause follows the conventions in 21.5. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

115.1.3 Relationship of 1000BASE-RHx to other standards

The relationship between a 1000BASE-RHx PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 115–1. The physical layer connects one Annex 4A Media Access Control (MAC) to the medium. This clause specifies the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) components of the physical layer device (PHY).

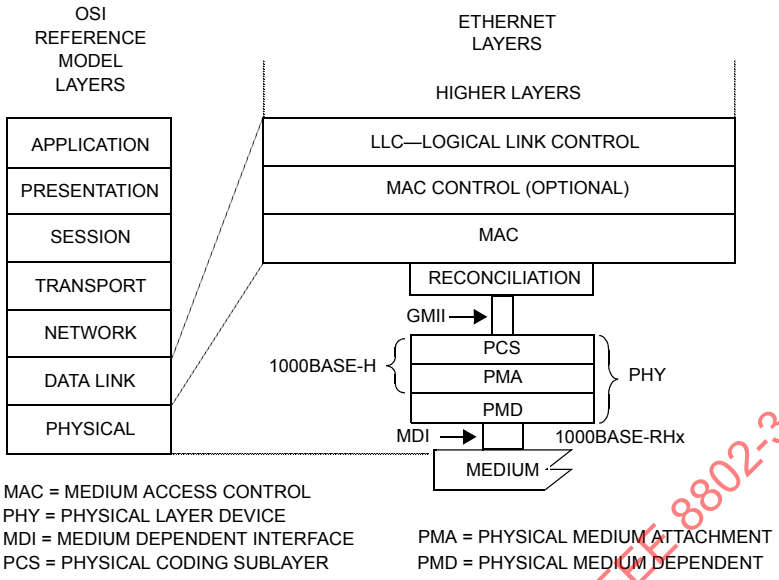

Figure 115–1—1000BASE-RHx PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 Ethernet Model

115.1.4 Relationship to other Gigabit Ethernet PHY types

1000BASE-RHx PHY types are specified with the PCS interfacing to a GMII. Physical implementation of the GMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not. The MII Management Interface used with the initial set of Gigabit Ethernet PHYs is not used for 1000BASE-RHx PHY types.

115.1.5 Operation of 1000BASE-RHx

1000BASE-RHx PHY types support full duplex operation only, using two plastic optical fibers as the medium. Each fiber is used for unidirectional transmission with the 1000BASE-RHx port on one end of the link segment transmitting on one fiber and receiving on the second fiber. A cross-over in the cabling connects the local PMD transmitter to the link partner's PMD receiver, and the link partner's PMD transmitter to the local PMD receiver. The PMD TX and PMD RX compose the PMD sublayer.

The topology of 1000BASE-RHx is illustrated in Figure 115–2.

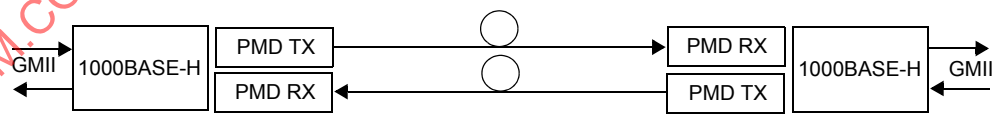

Figure 115–2—1000BASE-RHx topology

The 1000BASE-H PCS encapsulates and decapsulates the transmit and receive GMII data streams using a series of fixed length Transmit Blocks. A frame on the GMII can be contained in one or more Transmit Blocks. GMII frame boundaries have no correlation to Transmit Block boundaries.

Transmit Blocks also include pilot signals and control information. This information keeps the receiver clock aligned with the transmitter, supports channel equalization, and provides link monitoring. These signals and control information are inserted at fixed locations within the Transmit Block interrupting the transmission of the GMII data stream also included in the Transmit Block. Encapsulation of the GMII data stream within the Transmit Block also includes forward error correction encoding in fixed-length codewords inserted at fixed locations.

115.1.6 Functional block diagram

Figure 115–3 provides a functional block diagram of the 1000BASE-RHx PHY.

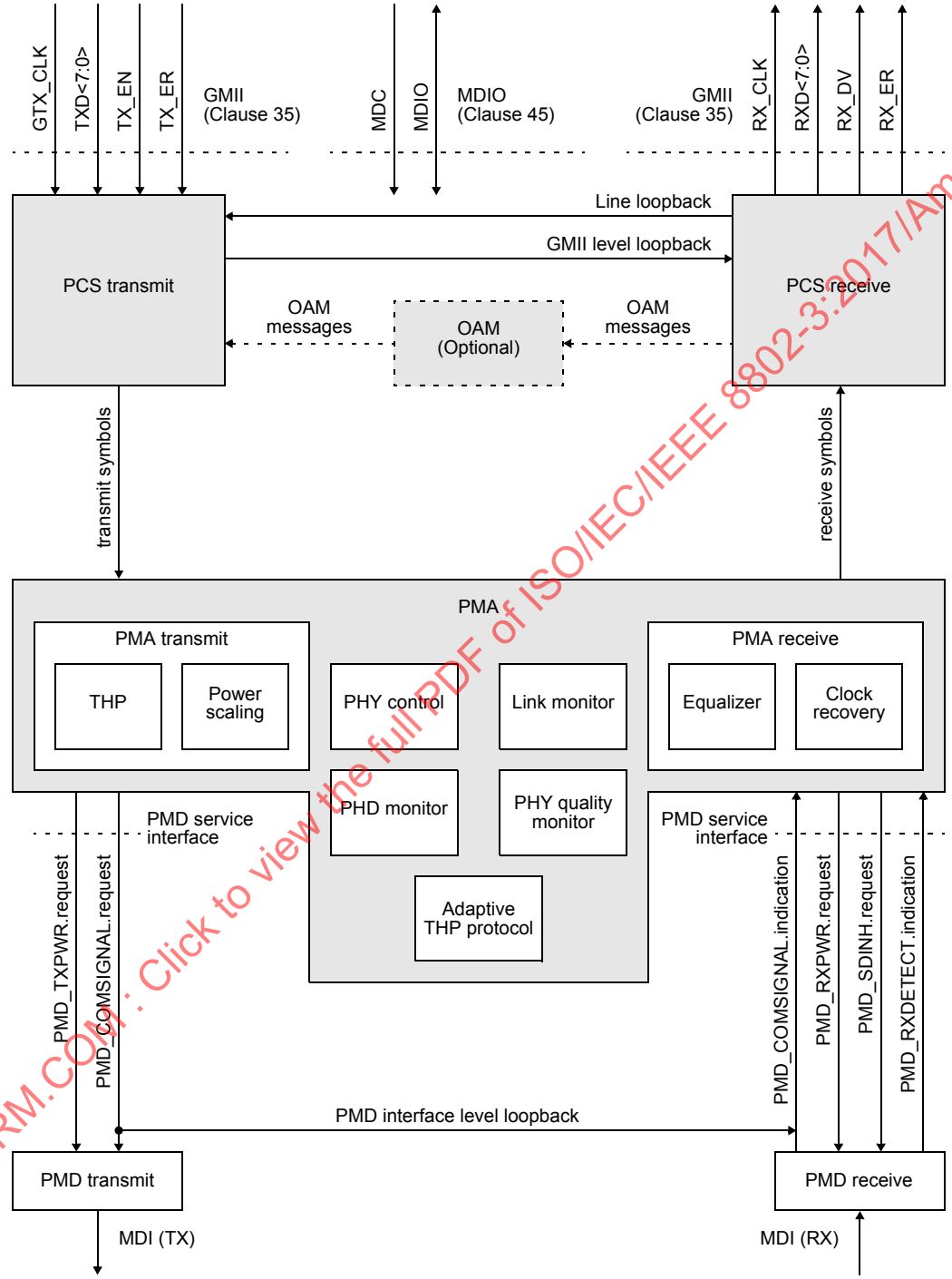

Figure 115–3—1000BASE-RHx functional block diagram

115.2 Physical Coding Sublayer (PCS)

The 1000BASE-H PCS couples a Gigabit Media Independent Interface (GMII), see Clause 35, to the Physical Medium Attachment (PMA) sublayer.

The PCS transmit function includes several steps. The GMII transmit data stream is encapsulated and encoded into 65-bit blocks called Physical Data Blocks (PDB) and then scrambled. After that, the scrambled data is encoded and mapped using a Multi-Level Coset Code (MLCC) block-oriented encoder, which generates fixed-length codewords of PAM16 symbols. The resultant MLCC codewords are symbol-by-symbol scrambled and then time division multiplexed with control information fields using various sub-blocks to create Transmit Blocks. The control information fields in Transmit Blocks are encoded differently, but the symbol time is equal for both the PAM16 symbols carrying information from the GMII and the encoded control information fields. Symbols are transmitted at a nominal rate of 325 MBd.

The PCS receive function comprises symbol descrambling and decoding of the MLCC codewords and the control information with error correction and detection.The resultant information obtained from MLCC codewords decoding is descrambled recovering the original PDB sequence that is finally processed to extract the GMII receive data stream. The decoded control information is also provided to the PMA sublayer for control of local and remote PHYs.

115.2.1 Transmit Block

The Transmit Block is the basic structure for transmission of data and control information for 1000BASE-H. On an active link, Transmit Blocks shall be transmitted continuously to allow receivers to maintain synchronization and equalizers to maintain alignment to the channel conditions.

The Transmit Block shall consist of 1 pilot S1 sub-block (S1), 13 pilot S2 sub-blocks ($S2_0$, $S2_1$, ..., $S2_{12}$), 14 physical header subframe sub-blocks (PHS_0, PHS_1, ..., PHS_{13}), and 28 payload data sub-blocks (numbered 0 through 27), which are temporally ordered as indicated in Figure 115–4. (The top part of the figure provides detail on the beginning of a Transmit Block and the bottom part of the figure the end of a Transmit Block.) The symbols composing any sub-block shall be transmitted to the PMA at the symbol rate.

The GMII data stream is encoded into the payload data sub-blocks in a stream of fixed length Transmit Blocks. Payload data sub-blocks are modified in LPI mode of operation as described in 115.4.

Each pilot S1 sub-block, pilot $S2_x$ sub-block, and PHS_x sub-block is composed of 160 symbols. For these sub-blocks the first 16 symbols (prefix) and the last 16 symbols (postfix) are zeros (see 115.3.3.1).

Each payload data sub-block is composed of 7904 symbols that span 8 MLCC codewords of 988 symbols each. The transmission of MLCC codewords are aligned with the start of the payload data sub-blocks. Since the Transmit Block includes 28 payload data sub-blocks, a total of 224 MLCC codewords (CW_0, CW_1, …, CW_{223}) are transmitted. This gives a total of 221 312 payload data symbols.

The resulting length of a Transmit Block is 225 792 symbols. Because the nominal symbol rate is 325 MBd, a Transmit Block is transmitted nominally every 694.7446 µs.

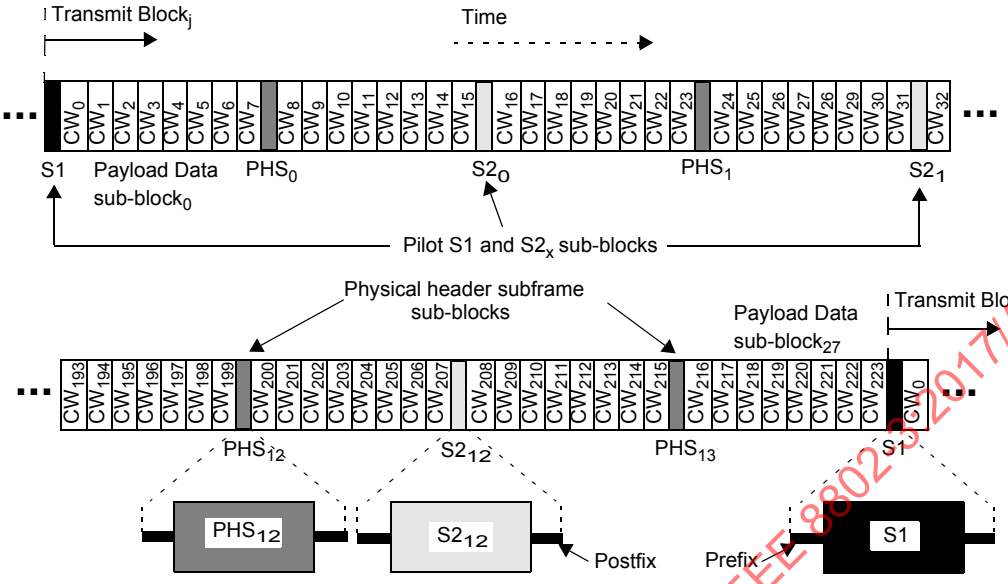

Figure 115–4—1000BASE-H Transmit Block

Transmit Blocks are generated by the multiplexer from the four data paths shown in Figure 115–5. The symbols of pilot S1, pilot S2$_x$, PHS$_x$, and payload data sub-blocks are generated in a different manner. Though the implementation method is not constrained, the input from each data path to the multiplexer may logically be viewed as a symbol FIFO, with the multiplexer selecting the appropriate data path symbols sequentially to create a sub-block. The sequence of sub-blocks results in the Transmit Block temporal order illustrated in Figure 115–4.

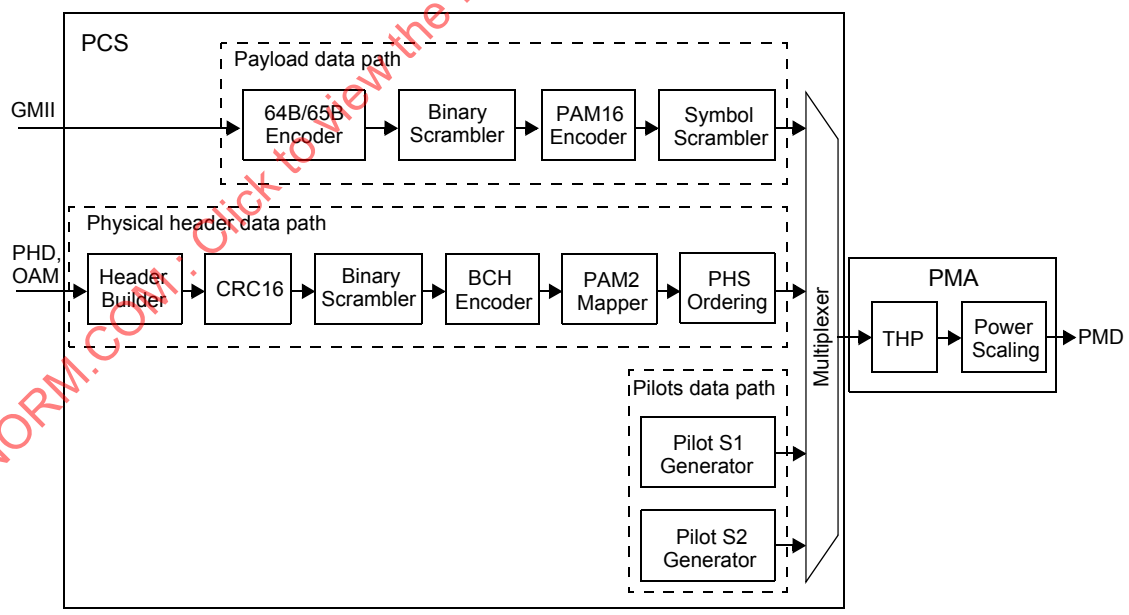

Figure 115–5—Transmit Block generation

115.2.2 Pilots data path

Pilots S1 and S2 are predefined signals transmitted in fixed allocated time slots of the Transmit Block intended to be used by the receiver for initialization and continuous tracking purposes based on data-aided signal processing. A pilot signal S1 is transmitted at the beginning of each Transmit Block as shown in Figure 115–4 and is intended for symbol synchronization and timing recovery. Pilot S2 is divided into a series of sub-blocks ($S2_x$, x = 0 through 12) that are distributed along the Transmit Block. Pilot $S2_x$ sub-blocks are intended to facilitate timing recovery, channel estimation, and equalization by the receiver.

115.2.2.1 Pilot S1 generator

A pilot S1 sub-block is transmitted at the beginning of each Transmit Block as shown in Figure 115–4. Figure 115–6 illustrates the pilot S1 generator.

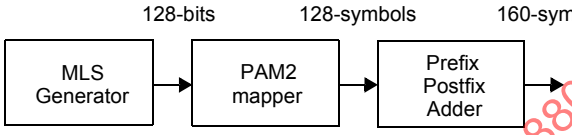

Figure 115–6—Pilot S1 generator

The S1 generator shall produce an output of one pilot S1 sub-block per Transmit Block equivalent to the following steps:

a) A maximum length sequence (MLS) generator that produces the same output as the following MATLAB®[2] (see 1.3) code[3] is used to generate a 128-bit binary sequence. This MATLAB code produces the same 128-bit binary sequence as the shift register shown in Figure 115–7 when the shift register is initialized for each pilot S1 sub-block generation with hexadecimal value of 0x172DB9D, where the leftmost digit of the initialization value corresponds to the initial value of register element r[0] and is taken to generate the first bit of the pilot S1.

```
function out = lfsr(len, seed)
  % Reset
  r = double(dec2bin(hex2dec(seed))) - double('0');
  r = [zeros(1, 25-length(r)) r];
  % Output generation
  for i = 1:len
    out(i) = r(1);
    r      = [mod(r(22)+r(25),2) r(1:24)];
  end
end
```

The variable *len* is the length of the sequence to be generated (*len* = 128 for S1), the variable *out* is the binary output sequence, and the variable seed is the initialization value of the shift register (*seed* = '172DB9D').

b) The bits generated in the previous step are mapped into PAM2 symbols so that bits with value 0 are mapped to {–1} and bits with value 1 are mapped to {+1}.

c) The resulting 128-symbol sequence is prefixed and postfixed by a sequence of 16 zero {0} symbols, thus obtaining the 160 symbol length for S1 sub-block.

[2]MATLAB is a registered trademark of The Mathworks, Inc. (http://www.mathworks.com).
[3]Copyright release for MATLAB code: Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

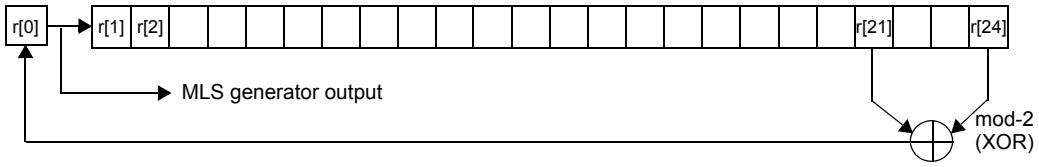

Figure 115–7—MLS generator

115.2.2.2 Pilot S2 generator

A pilot $S2_x$ sub-block is transmitted between every other payload data sub-block, alternating with PHS_x sub-blocks as shown in Figure 115–4. Figure 115–8 illustrates the pilot $S2_x$ sub-block generator.

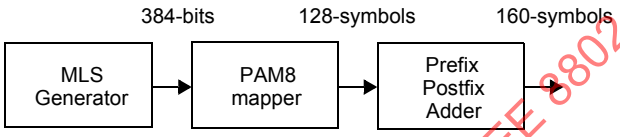

Figure 115–8—Pilot $S2_x$ sub-block generator

The S2 generator shall produce an output of 13 pilot $S2_x$ sub-blocks per Transmit Block equivalent to the following steps:

a) An MLS generator that produces the same output as the shift register shown in Figure 115–7 is used to generate 13 binary sequences of 384-bit length. The shift register is initialized for each pilot $S2_x$ sub-block generation as indicated in Table 115–1. MLS initialization and operation are as described in 115.2.2.1.

Table 115–1—Shift register initialization for $S2_x$ sub-blocks

$S2_x$ sub-block	Shift register initialization	$S2_x$ sub-block	Shift register initialization
$S2_0$	0x0945286	$S2_7$	0x050DF4E
$S2_1$	0x0F00D43	$S2_8$	0x164252F
$S2_2$	0x1AA60F3	$S2_9$	0x1E587FB
$S2_3$	0x0D89E10	$S2_{10}$	0x02CD3AD
$S2_4$	0x0DEBAC8	$S2_{11}$	0x0EE9512
$S2_5$	0x16913D1	$S2_{12}$	0x1ABFA53
$S2_6$	0x13EACDB		

b) A PAM8 mapper generates a sequence of 128 PAM8 symbols from each binary sequence generated in the previous step. The binary sequence is divided into 3-bit groups and a PAM8 symbol is

generated from each 3-bit group according to Equation (115–1). Bit $b[0]$ is the first of each 3-bit group received from the MLS generator and S the value of the PAM8 symbol.

$$S = 2b[0] + 4b[1] + 8b[2] - 7 \quad (115–1)$$

c) Each sequence of 128 PAM8 symbols is prefixed and postfixed by a sequence of 16 zero symbols, thus obtaining the 160 symbol length for each pilot $S2_x$ sub-block.

115.2.3 Physical header encoding and scrambling

The Physical Header Data (PHD) consists of 704 bits carrying physical layer control information (see 115.3.4). The PHD is scrambled, encoded, and modulated prior to transmission as illustrated in Figure 115–9. The PHD is protected by appending a 16-bit CRC code (CRC16) for extra error detection capability after decoding. The resulting sequence of 720 bits is scrambled and encoded with a (896, 720) BCH code for error correction. The 896 coded bits are mapped to generate the resulting 1792-symbol physical header subframe (PHS), which is ordered in 14 pieces regularly distributed along the Transmit Block (PHS_0 through PHS_{13}) as indicated in Figure 115–4.

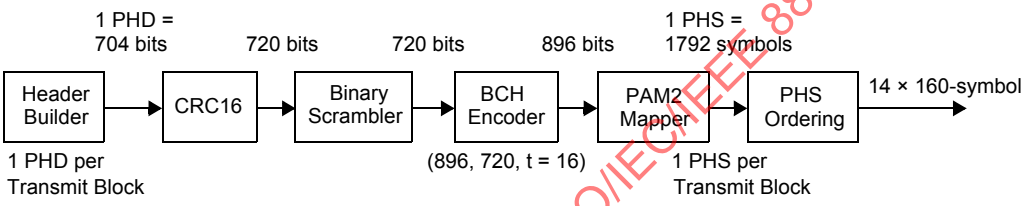

Figure 115–9—Physical header encoding and scrambling

115.2.3.1 Physical header CRC16

The 704 PHD bits from Header Builder are repeated without change and appended with 16 cyclic redundancy check bits (CRC16) for extra error detection capability after BCH decoding. The appended CRC16 shall be computed from the PHD bits and shall produce the same result as the implementation shown in Figure 115–10. The generator polynomial is $(x + 1)(x^{15} + x + 1)$. The shift register elements S_0, ..., S_{15}, shall be initialized with the value of 0x0000 for each PHD. The 704 PHD bits, in transmit bit order, are then used to compute the CRC16 with the multiplexer configured to CRCgen. After the 704 bits have been serially processed, the multiplexer is configured to CRCout and the 16 stored values are the CRC16. CRC16 is transmitted in order from S15 to S0.

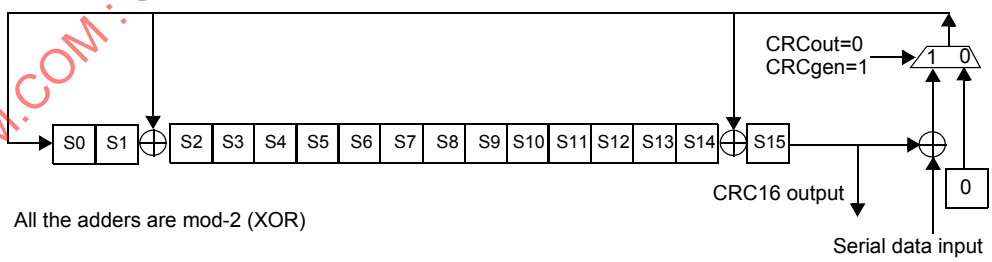

Figure 115–10—Physical header CRC16

115.2.3.2 Physical header binary scrambler

The 720 bits from the CRC16 functional block shall be scrambled prior to transmission using a binary scrambler that produces the same result as the implementation shown in Figure 115–11. The shift register shall be initialized with the value of 0x068D332 for each Transmit Block, where the leftmost digit corresponds to the initial value of register element r[0]. The initial value of r[0] is xor-ed with the first bit from the CRC16 functional block to generate the first input bit to the BCH encoder. See 115.2.2.1 for the formal definition of the shift register.

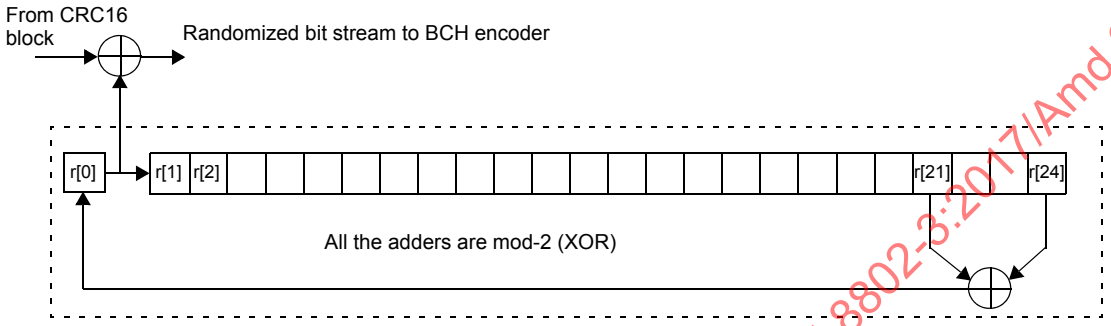

Figure 115–11—Physical header binary scrambler

115.2.3.3 Physical header BCH encoder

The scrambled 720 information bits shall be systematically encoded into 896 bits length codewords by means of a BCH (896, 720) encoder. The BCH code (896, 720) is a shortened version of the primitive BCH code (2047, 1871). It is a BCH code over Galois Field GF(2^{11}), and the error correction capability of such code is $t = 16$ bits. The number of parity bits is $p = 176$ bits. Shortening is implemented by prefixing to the 720 information bits a sequence of 1151 bits with value zero. The zero prefix sequence is not transmitted and is only used to calculate the parity from the primitive code.

The BCH code is specified by the coefficients of the generator polynomial of Equation (115–2), where $g(i)$ takes values 0 or 1.

$$G(x) = \sum_{i=0}^{p} g(i)x^i \qquad (115\text{–}2)$$

The order of $G(x)$ is $p = 176$. The 177 coefficients of $G(x)$ are given by the following hexadecimal number:

0x0001 A3E8 171D BCA4 EE1E 7CDC A7DA FB8D 8F39 8072 8516 6007

with $g(0)$ being the rightmost bit.

The parity calculation shall produce the same result as the shift register implementation shown in Figure 115–19. The delay elements $s_0, s_1, \ldots, s_{p-1}$ in Figure 115–19 shall be initialized to zero before encoding. See 115.2.4.3.2 for detailed BCH encoder operation.

115.2.3.4 Physical header modulation

The 896 bits from the BCH encoder shall be mapped into 1792 PAM2 symbols so that bits with value 0 are mapped to 2 consecutive symbols {+1, –1}, and bits with value 1 are mapped to 2 consecutive symbols {–1, +1}.

115.2.3.5 Physical header ordering

The 1792-symbol PHS sequence shall be divided for transmission into 14 pieces of 128 symbols each, regularly distributed along the Transmit Block (PHS_0 through PHS_{13}) as indicated in Figure 115–4, preserving the symbol ordering. Each piece shall be prefixed and postfixed by zero valued symbol sequences of 16 symbols length, thus obtaining the 160 symbol length of each PHS_x.

115.2.4 Payload data encoding and scrambling

The incoming data from the GMII are encapsulated and encoded into 65-bit blocks (64B/65B encoder in Figure 115–12) for transmission. The 64B/65B generates 705 600 bits per Transmit Block that are scrambled. The scrambled binary sequence is then encoded for forward error correction by a block oriented MLCC encoder that generates a 988-symbol codeword per 3150 input information bits. A total number of 224 MLCC codewords (CW_0, CW_1, …, CW_{223}) are transmitted per Transmit Block grouped in 28 payload data sub-blocks each spanning 8 MLCC codewords as specified in 115.2.1. Each payload data sub-block is composed of 8 × 988 = 7904 PAM16 symbols. The 7904 × 28 = 221 312 PAM16 symbols of a Transmit Block are symbol-by-symbol scrambled before being transmitted to the PMA sublayer.

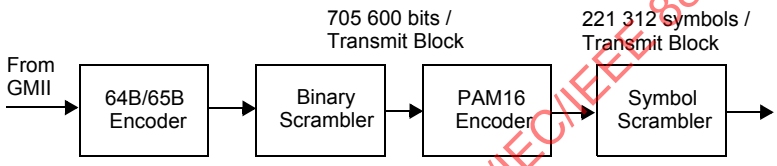

Figure 115–12—Payload data encoding and scrambling

115.2.4.1 GMII data stream encoding

The 64B/65B encoder generates a stream of 65-bit PDBs, which are serially transmitted to the binary scrambler. The nominal bit-rate of the output of the 64B/65B encoder is (65/64) × 1000 = 1015.625 Mb/s.

115.2.4.1.1 64B/65B encoding

The GMII detailed in Clause 35 supports the 1000 Mb/s operation of 1000BASE-H. It includes 8-bit transmit and receive data paths (i.e., TXD<7:0> and RXD<7:0>). Two additional signals in each direction (i.e., TX_EN, TX_ER and RX_DV, RX_ER) are used in conjunction with the data paths to delimit Ethernet packets, indicate errors, and convey other control information. The eight data and two control signals are specified relative to and sampled by a clock (GTX_CLK and RX_CLK for transmit and receive respectively).

In the transmit direction, eight consecutive GMII transfers (a GMII Chunk) are combined and then prepended by a control bit (Type) to create the PDB. TXD <7:0>, TX_EN, and TX_ER compose each GMII transfer. Two different types of PDBs, PDB.DATA and PDB.CTRL, are encoded from the set of GMII transfers defined in Table 115–2. The GMII transfers shown in Table 115–2 are the subset of permissible GMII encodings of Table 35-1 used for full duplex operation.

If the GMII Chunk only contains eight normal data transmission transfers, a PDB.DATA is generated. If the GMII Chunk contains at least one of the other three GMII control transfers shown in Table 115–2, a PDB.CTRL is generated. Both PDB.DATA and PDB.CTRL are composed of a Type bit followed by eight octets.

Table 115–2—Supported TX GMII encodings

TX_EN	TX_ER	TXD<7:0>	CTRL<1:0>	Description
1	0	00 through FF	—	Normal data transmission
0	0	00 through FF	01	Control: normal inter-frame (idle)
0	1	01	10	Control: assert low power idle (LPI)
1	1	00 through FF	00	Control: transmit error propagation

The format of a PDB.DATA is shown in Figure 115–13. It consists of 65 bits, the first bit being the Type bit (with a value of 0) followed by eight consecutive GMII data transfers (normal data transmission as shown in Table 115–2). The eight data octets are transmitted in the same order as they were received from the GMII. Bits in an octet are transmitted from least to most significant bit.

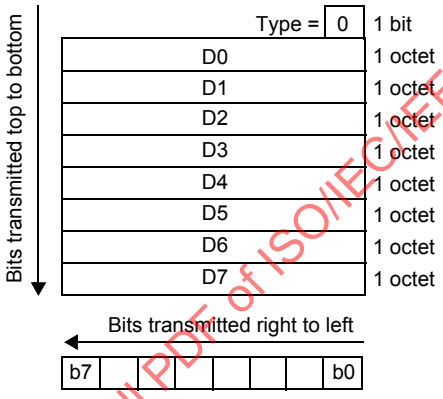

Figure 115–13—PDB.DATA format

The format of a PDB.CTRL is shown in Figure 115–14. It consists of 65 bits, encoding 8 GMII transfers [(LEN + 1) GMII control transfers and (7 – LEN) GMII data transfers, where LEN ranges from 0 through 7] preceded by the Type bit that is set to 1. The Type bit is transmitted first, followed by the 8 data and control octets generated by the encoding method described next. Bits in an octet are transmitted from least to most significant bit.

The processing of a GMII Chunk is as follows. Data octets (normal data transmission in Table 115–2) retain the value of TXD<7:0> in the GMII transfer, but every GMII control transfer is encoded in a control 8-bit byte (CB) with the following contents:

— CTRL<1:0> (CB<7:6>): This field encodes the content of the GMII control transfer as specified in Table 115–2.

— OFS<2:0> (CB<5:3>): This field indicates the offset (in GMII transfers) from the beginning of the GMII Chunk to the location of the first GMII control transfer in the GMII Chunk. This field has the same value for all CBs contained in the PDB.CTRL. The OFS value range is 0 through 7.

— LEN<2:0> (CB<2:0>): This field is the count of GMII control transfers in the GMII Chunk minus 1. This field takes the same value for all CBs contained in the PDB.CTRL. The LEN value range is 0 through 7.

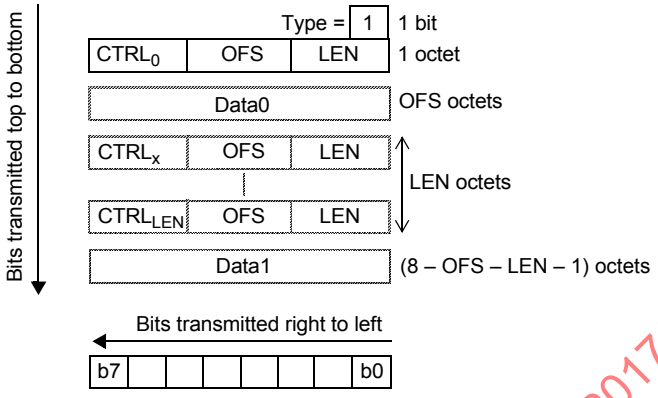

Figure 115–14—PDB.CTRL format

The octets within the PDB.CTRL are reordered as follows:

a) The CB built from the first GMII control transfer is transmitted as the first in PDB.CTRL. (This CB might encode the first GMII transfer of the GMII Chunk, or the CB might correspond to another GMII transfer of the GMII Chunk.)

b) The other seven PDB.CTRL octets are transmitted in order [not including the first CB if it was moved per step a)].

Each dotted box in Figure 115–14 represents a sequence of octets. The number of octets in a dotted box may be zero. Data0 contains OFS octets. If OFS is zero, Data0 is null. The number of CBs shown below Data0 is specified by LEN. If LEN is zero, no CB is located between Data0 and Data1. Data1 similarly may or may not be null depending on the portion of the GMII Chunk captured. Data1 completes the 8 octets included in a PDB.CTRL. It is null if 8 total octets preceded it.

NOTE—Some common example sequences of GMII transfers that illustrate the PDB.CTRL encoding include the following:

1) A GMII Chunk that only captures IPG, PDB.CTRL only includes CBs, and not Data0 or Data1.

2) A GMII Chunk that captures the end of a packet and beginning of IPG results in the first IPG GMII control transfer converted to a CB being moved ahead of the end of the packet data that is transmitted in Data0. If any more IPG GMII control transfers were captured in the GMII Chunk, they are located in the dotted boxes with control fields $CTRL_x$ through $CTRL_{LEN}$. Data1 is null.

3) A GMII Chunk that captures the end of IPG and beginning of a packet does not move any CB during encoding. The IPG is encoded in the first CB, Data0 is null and the CBs with control fields labeled $CTRL_x$ through $CTRL_{LEN}$ hold the remaining CBs encoding the IPG. The beginning of packet then appears in Data1.

4) A GMII Chunk that captures the end of a packet, shortened IPG (six or less IPG transfers), and beginning of a packet. The first IPG GMII transfer is encoded as a CB and moved ahead similar to example 2, and would have the end of packet GMII data transfer(s) in Data0, Other IPG GMII transfers are encoded as CBs in $CTRL_x$ through $CTRL_{LEN}$ and the beginning of the next packet data in Data1.

Because the minimum length of an Ethernet packet is longer than 7 octets, all the GMII control transfers in a GMII Chunk of a correct packet are contiguous. Consequently, all the CBs beyond the first are also contiguous within the PDB.CTRL.

When there are non-contiguous GMII control transfers within a GMII Chunk, the GMII data transfers between the GMII control transfers belong to an erroneous Ethernet packet. In this case, these GMII data

transfers are replaced by GMII control transfers encoding error propagation as a previous step to the PDB.CTRL encoding. The resulting GMII Chunk is then encoded following the previous description.

A minimum delay of 8 GTX_CLK cycles at the GMII is necessary for the 64B/65B encoding, because the 64B/65B encoder requires the reception of a full GMII Chunk to start generating the first bit of the corresponding PDB.

The formal definition of the 64B/65B encoding is in 115.2.4.1.2.

115.2.4.1.2 64B/65B encoding formal definition

The 64B/65B encoder shall produce the same result as the following MATLAB (see 1.3) code.[4]

```
% Variables definition
GMII.TX_ER     % GMII TX_ER signal, 1xL row vector
GMII.TX_EN     % GMII TX_EN signal, 1xL row vector
GMII.TXD       % GMII TXD bus, 1xL row vector
PCS_ENC_EN     % tx_gmii_enable (see 115.3.5.1) value for each GMII transfer,
               % 1xL vector
PDB.TYPE       % PDB type field, 1x(L/8) row vector
PDB.PAYLOAD    % PDB payload field, 8x(L/8) matrix

% 64B/65B encoding procedure
GMII.TX_EN = GMII.TX_EN & PCS_ENC_EN;
GMII.TX_ER = GMII.TX_ER & PCS_ENC_EN;

for i = 0:8:length(GMII.TXD)-1,
  TC = (GMII.TX_EN(i+1:i+8)*2 + GMII.TX_ER(i+1:i+8)) ~= 2;

  if any(TC)
    % There are at least one control byte in the 8-bytes GMII Chunk
    % The PDB is a PDB.CTRL
    PDB.TYPE(i/8 + 1) = 1;

    if any(~TC(min(find(TC)):max(find(TC))))
      % The control bytes are not contiguous in the GMII Chunk.
      % Replace data bytes that lie within control bytes with error code.
      LL=i+min(find(TC));
      UL=i+max(find(TC));
      GMII.TX_ER(LL:UL) = GMII.TX_EN(LL:UL)|GMII.TX_ER(LL:UL);

      TC(min(find(TC)):max(find(TC))) = 1;
    end

    % Valid GMII Chunk
    % OFS field computation
    OFS = min(find(TC)) - 1

    % LEN field computation
    LEN = sum(TC) - 1

    % Build the PDB.CTRL payload
    for j = 1:8,
      if TC(j)
        if ~GMII.TX_EN(i+j) & ~GMII.TX_ER(i+j)
          % Normal inter-frame
          CTRL = 1;
        elseif ~GMII.TX_EN(i+j) & GMII.TX_ER(i+j) & (GMII.TXD(i+j) == 1)
          % Assert LPI
          CTRL = 2;
        elseif GMII.TX_EN(i+j) & GMII.TX_ER(i+j)
          % Transmit error propagation
          CTRL = 0;
```

[4]Copyright release for MATLAB code: Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

```
          else
            % Otherwise, default case (normal inter-frame)
            CTRL = 1
          end

          B(j) = LEN + OFS*2^3 + CTRL*2^6;
        else
          B(j) = GMII.TXD(i+j);
        end
      end

      % Shift the first control byte
      PDB.PAYLOAD(1,      i/8 + 1) = B(OFS + 1);
      PDB.PAYLOAD(2:end, i/8 + 1) = [B(1:OFS) B(OFS+2:end)].';

    else
      % Pure normal data transmission bytes in the GMII Chunk
      % The PDB is a PDB.DATA
      PDB.TYPE(i/8 + 1)        = 0;
      PDB.PAYLOAD(:, i/8 + 1) = GMII.TXD(i+1:i+8).';
    end
  end
```

115.2.4.1.3 PDB alignment with Transmit Block

Since the number of information bits in a Transmit Block (705 600 bits) is not a multiple of the PDB length, in general PDBs are not aligned to the start of a Transmit Block. The PHY transmitter shall encode the number of bits between the first payload bit of Transmit Block j+1 and the start of the first PDB encoded in Transmit Block j+1 in the field PHD.TX.NEXT.PDB.OFFSET of the PHD of Transmit Block j. With this control information the receiver is able to align the PCS decoder for the Transmit Block j+1 once the PHD_j (part of Transmit Block j) is fully received and decoded. This is illustrated in Figure 115–15.

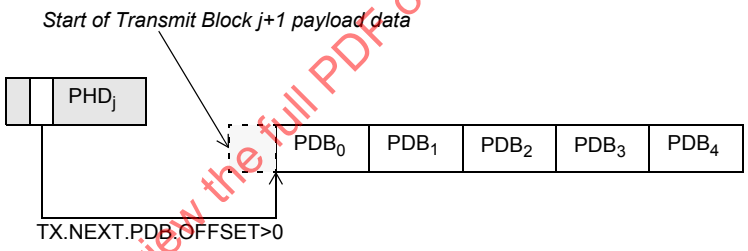

Figure 115–15—PDB alignment

The offset to the start of the first PDB in Transmit Block j+1, $\Delta(j+1)$ is calculated from the offset of the Transmit Block j, $\Delta(j)$ by using the Equation (115–3).

$$\Delta(j+1) = \mathrm{mod}(40 + \Delta(j), 65) \tag{115–3}$$

Modulo operator is defined per Equation (115–4), where floor(a) denotes the greatest integer less than or equal to the real number a.

$$\mathrm{mod}(y, x) = y - x \times \mathrm{floor}\left(\frac{y}{x}\right) \tag{115–4}$$

115.2.4.2 Payload data binary scrambler

The 705 600 bits per Transmit Block from the 64B/65B encoder shall be scrambled prior to transmission using a binary scrambler that produces the same result as the implementation shown in Figure 115–16. The

shift register shall be initialized with a hexadecimal value of 0x17C9C58 for each Transmit Block, where the leftmost digit corresponds to the initial value of register element r[0]. The initial value of r[0] is xor-ed with the first bit from the 64B/65B encoder to generate the first bit of the binary sequence that feeds the PAM16 encoder. See 115.2.2.1 for the formal definition of the shift register.

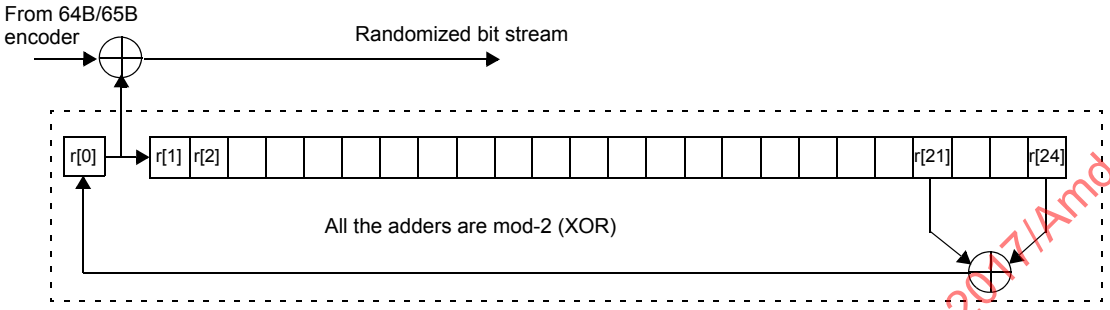

Figure 115–16—Payload data binary scrambler

115.2.4.3 PAM16 encoder

After being encapsulated and scrambled, the GMII data stream is encoded into PAM16 symbols. A two-level, block-oriented MLCC based on two-dimensional constellations is used to transmit the information with high spectral efficiency. The information is partitioned in such a way that the bits more likely to be corrupted by noise are protected by a binary BCH code, and those bits less likely to be corrupted are not additionally protected.

Figure 115–17 shows the essential parts of the MLCC encoder. A block of 3150-bit per codeword is split between the two levels that compose the encoder in an interleaved manner. The bits in the first level are encoded with a (1976, 1668) BCH code and the second level is not encoded. Bits composing the BCH codeword in the first level are mapped onto symbols of a QAM16 constellation. Bits in the second level are mapped onto symbols of a rotated QAM8 constellation. After the mapping, the two levels produce 494 2D symbols per codeword. Symbols from each level are processed by a first lattice transformation and then added to carry out the coset partitioning. The output of the adder is further processed by a second lattice transformation that produces symbols onto a rotated QAM128 constellation. Finally, in-phase and quadrature components of QAM128 symbols are multiplexed in time to generate 988 PAM16 symbols per codeword.

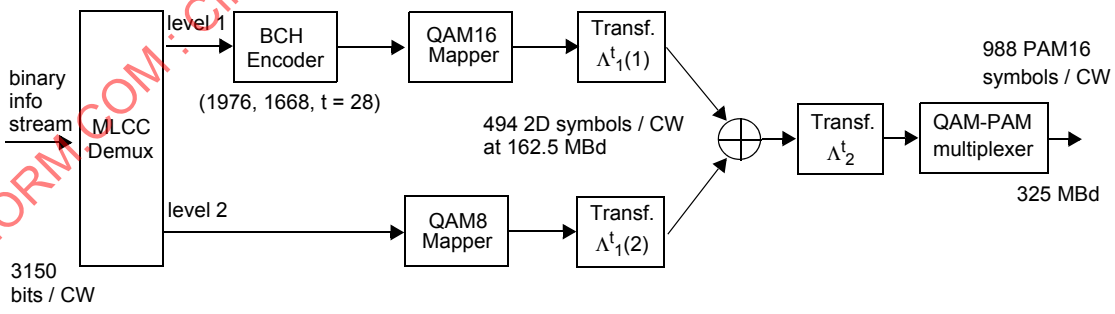

Figure 115–17—Two level coset encoder

115.2.4.3.1 MLCC demultiplexer

The 3150 information bits to be encoded in an MLCC codeword shall be demultiplexed in two flows, where the bits $7 \times k + j$, for all k from 0 through 416 and all j from 0 through 3, are transferred to the BCH encoder of the first MLCC level, and the bits $7 \times k + j$, for all k from 0 through 416 and all j from 4 through 6, and the bits from 2919 through 3149 are transferred to the second MLCC level, preserving the relative bit ordering in each flow.

Figure 115–18 illustrates the operation of the MLCC demultiplexer. In Figure 115–18, bit quadruples a_i with i from 0 through 416 and bit triples b_i with i from 0 through 493 are the portions of information transferred to the first and to the second MLCC level, respectively. The term "4b" stands for 4-bit groups, and the term "3b" stands for 3-bit groups.

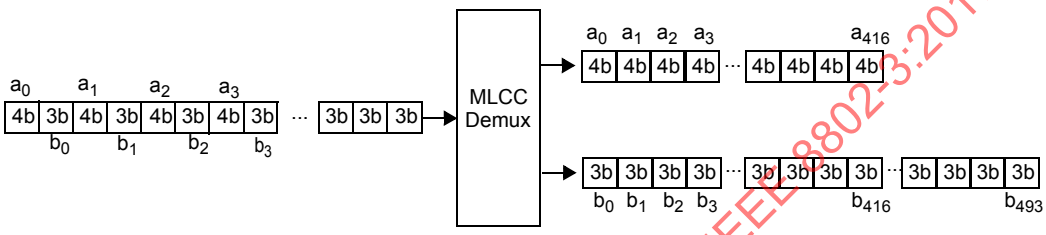

Figure 115–18—MLCC demultiplexing process

115.2.4.3.2 Payload BCH encoder

The 1668 information bits of the first level shall be systematically encoded into 1976 code bits by means of a BCH $(n, k) = (1976, 1668)$ encoder. This BCH code is a shortened version of the primitive BCH code (2047, 1739). It is a BCH code over Galois field GF(2^{11}), and the error correction capability of such code is $t = 28$. The number of parity bits is $p = 308$ bits. Shortening is implemented by prefixing to the 1668 information bits a sequence of 71 bits with value zero. The zero prefix sequence is not transmitted and is only used to calculate the parity from the primitive code.

The BCH code is specified by the coefficients of generator polynomial $G(x)$ of Equation (115–5), where $g(i)$ takes values 0 or 1. The order of $G(x)$ is $p = 308$.

$$G(x) = \sum_{i=0}^{p} g(i)x^i \qquad (115\text{–}5)$$

The 309 coefficients of $G(x)$ are given by the following hexadecimal number:

0x0014 B624 90DF 0781 4D88 99E9 B9DB 6267 00D3 7A90
49DB C0C4 484A D6C5 49AB AE7E 6F58 A406 CF86 C0BD,

with $g(0)$ being the rightmost bit of the second line.

The parity calculation shall produce the same result as the shift register implementation shown in Figure 115–19. The delay elements $s_0, s_1, \ldots, s_{p-1}$ shall be initialized to zero before encoding. All the k bits composing the information message are used to calculate the parity and enter the BCH encoder in the same order provided by the MLCC demultiplexer with the multiplexers indicated in Figure 115–19 connected with BCHgen selected. After all the k bits have been serially processed, the multiplexers are configured to

select BCHout and the p stored values $s_0, s_1, \ldots, s_{p-1}$ are the parity bits. The parity bits are then transmitted in order from s_{p-1} to s_0.

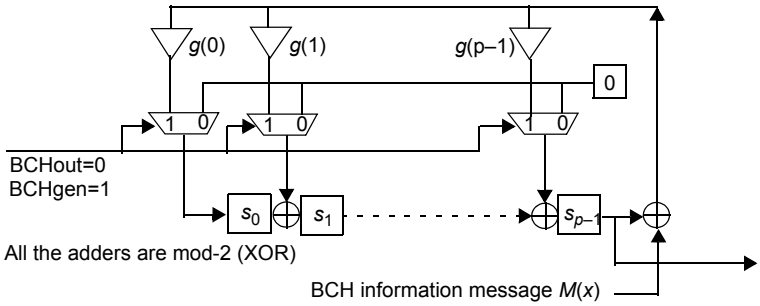

Figure 115–19—BCH encoder

The parity bits are transmitted after the information message $M(x) = m_0 + m_1x + m_2x^2 + \ldots + m_{k-1}x^{k-1}$, where m_{k-1} is the first bit of the message. To encode the message, $M(x)$ is first multiplied by x^{n-k} and the result is then divided by the generator polynomial $G(x)$. The remainder of the division of $M(x)x^{n-k}$ by $G(x)$ defines the parity $S(x) = s_0 + s_1x + s_2x^2 + \ldots + s_{p-1}x^{p-1}$, where $p = n - k$. The transmitted codeword $C(x)$ is formed by combining $M(x)$ and $S(x)$ per Equation (115–6).

$$C(x) = S(x) + M(x)x^{n-k} = s_0 + s_1x + s_2x^2 + \ldots + s_{n-k-1}x^{n-k-1} + m_0x^{n-k} + \ldots + m_{k-1}x^{n-1} \quad (115\text{–}6)$$

which shows that the codeword is produced in the required systematic form.

115.2.4.3.3 QAM16 mapper

Codewords resulting from the BCH encoding shall be mapped by means of a QAM16 mapper (see Figure 115–17) that generates 494 QAM16 symbols per 1976 bits of the MLCC codeword, doing 4-bit groups that are then mapped per Table 115–3. Bit $b[0]$ is the first received bit of each 4-bit group and S_I and S_Q are the in-phase (I) component and the quadrature (Q) component, respectively, of the QAM16 two-dimensional constellation.

Table 115–3—4B mapping to QAM16

$b[3]$	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q	$b[3]$	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q
0	0	0	0	–3	–3	1	0	0	0	–3	+3
0	0	0	1	–1	–3	1	0	0	1	–1	+3
0	0	1	0	–3	–1	1	0	1	0	–3	+1
0	0	1	1	–1	–1	1	0	1	1	–1	+1
0	1	0	0	+3	–3	1	1	0	0	+3	+3
0	1	0	1	+1	–3	1	1	0	1	+1	+3
0	1	1	0	+3	–1	1	1	1	0	+3	+1
0	1	1	1	+1	–1	1	1	1	1	+1	+1

115.2.4.3.4 QAM8 mapper

The uncoded bit stream from the MLCC demultiplexer shall be mapped by means of a QAM8 mapper (as illustrated in Figure 115–17) that generates 494 QAM8 symbols per 1482 bits of the MLCC codeword, doing 3-bit groups that are then mapped per Table 115–4. Bit $b[0]$ is the bit of each 3-bit group received first in time and S_I and S_Q are the in-phase (I) component and the quadrature (Q) component, respectively, of the QAM8 two-dimensional constellation.

Table 115–4—3B mapping to QAM8

$b[2]$	$b[1]$	$b[0]$	S_I	S_Q	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q
0	0	0	–3	–3	1	0	0	+3	–1
0	0	1	–1	–1	1	0	1	+1	–3
0	1	0	–3	+1	1	1	0	+3	+3
0	1	1	–1	+3	1	1	1	+1	+1

115.2.4.3.5 First lattice transformation

The QAM16 symbols given by the S_I and S_Q components shall be further processed by a symbol-by-symbol lattice transformation ($\Lambda_1^t(1)$ in Figure 115–17) according to Equation (115–7) and Equation (115–8). The label $t11$ indicates the result of the lattice transformation $\Lambda_1^t(1)$.

$$S_I^{t11} = \frac{1}{2}(3 + S_I) \tag{115–7}$$

$$S_Q^{t11} = \frac{1}{2}(3 + S_Q) \tag{115–8}$$

The QAM8 symbols given by the S_I and S_Q components shall be further processed by a symbol-by-symbol lattice transformation ($\Lambda_1^t(2)$ in Figure 115–17) according to Equation (115–9) and Equation (115–10). The label $t12$ indicates the result of the lattice transformation $\Lambda_1^t(2)$.

$$S_I^{t12} = S_I - S_Q \tag{115–9}$$

$$S_Q^{t12} = 6 + S_I + S_Q \tag{115–10}$$

115.2.4.3.6 Lattice addition

The symbols from the first lattice transformation of the first and second levels shall be added symbol-by-symbol according to Equation (115–11) and Equation (115–12). The resulting in-phase and quadrature components of the lattice addition are hereafter labeled as S_I^a and S_Q^a respectively. The label a indicates the result of the lattice addition.

$$S_I^a = S_I^{t11} + S_I^{t12} \tag{115–11}$$

$$S_Q^a = S_Q^{t11} + S_Q^{t12} \tag{115–12}$$

115.2.4.3.7 Second lattice transformation

The symbols from lattice addition shall be further processed by a symbol-by-symbol lattice transformation (Λ_2^t in Figure 115–17) according to Equation (115–13) and Equation (115–14). The output symbols that result of the second lattice transformation belong to a rotated QAM128 constellation. The label *t*2 indicates the result of the lattice transformation Λ_2^t.

$$S_I^{t2} = 2\text{mod}(S_I^a + S_Q^a, 16) - 15 \quad (115\text{–}13)$$

$$S_Q^{t2} = 2\text{mod}(-S_I^a + S_Q^a, 16) - 15 \quad (115\text{–}14)$$

Modulo operator is per definition of Equation (115–4).

115.2.4.3.8 QAM to PAM multiplexer

The QAM to PAM multiplexer shall generate 988 PAM16 symbols from 494 QAM128 symbols produced by the second lattice transformation per MLCC codeword, alternating the in-phase (*I*) component and the quadrature (*Q*) component, S_I^{t2} and S_Q^{t2}, respectively, of QAM128 symbols, starting the codeword with the *I* component of the first QAM symbol and ending the codeword with the *Q* component of the last QAM symbol. The PAM16 symbols generated in this way belong to the set {–15, –13, …, +13, +15}.

115.2.4.4 Payload data symbol scrambler

The 221 312 PAM16 symbols per Transmit Block from the PAM16 encoder block of Figure 115–12 shall be scrambled prior to transfer to the PMA transmit function using a scrambler implementation that produces the same output as the following steps:

a) An MLS generator that produces the same output as the shift register shown in Figure 115–7 is used to generate a 1 991 808-bit binary sequence per Transmit Block. The shift register is initialized for each Transmit Block with hexadecimal value of 0x155D559. MLS initialization and operation are as described in 115.2.2.1.

b) A mapper generates two 221 312-symbol sequences, *v* and *s*, per each binary sequence generated in the previous step, doing 9-bit groups that are then mapped so that 1 symbol of *v* and 1 symbol of *s* are generated per 9-bit group according to Equation (115–15) and Equation (115–16). Bits *b*[0] and *b*[8] are the bits of each 9-bit group received first and last in time, respectively, from the MLS generator.

$$v = -16 + 2\sum_{i=0}^{3} b[i]2^i \quad (115\text{–}15)$$

$$s = -1 + 2b[8] \quad (115\text{–}16)$$

c) The sequences *v* and *s*, generated in the previous step, are combined symbol-by-symbol basis with the payload symbols from PAM16 encoder, *x*, to generate a 221 312-symbol scrambled sequence, *y*, according to Equation (115–17) and Equation (115–18). Modulo operator is per definition of Equation (115–4).

$$u = v + s \times x \quad (115\text{–}17)$$

$$y = \text{mod}(u + 16, 32) - 16 \quad (115\text{–}18)$$

Figure 115–20 illustrates the payload data symbol scrambling process.

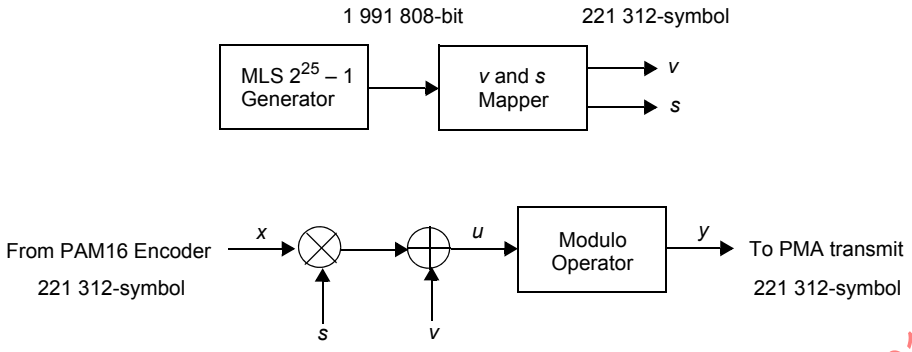

Figure 115–20—Payload data symbol scrambler

115.2.5 PCS receive function

The PCS receive function accepts equalized symbols provided by the PMA receive function. The PCS receive function knows to which part of the received Transmit Block the symbols belong, based on the symbol time alignment information provided by the clock recovery function of the PMA receive function (see 115.3.2 and 115.3.5.3). The PCS receive function shall carry out the PHD decoding, the PAM16 decoding of payload sub-blocks, and the 64B/65B decoding of payload data.

The PHD decoding comprises detection and demapping of the received PAM2 symbols, BCH decoding for error correction, binary data descrambling, and CRC16 checking for each received PHD. Only when the CRC16 computation indicates that the received PHD is correct shall the contents of the different PHD fields be available to the PMA state diagrams and to the other PCS receive functions that use this information.

The received PAM16 symbols belonging to the payload data sub-blocks are first symbol-descrambled, and the resulting symbols are MLCC decoded, with error correction and error detection. If during MLCC decoding it is detected that a codeword contains errors that could not be corrected, the resulting bits belonging to that codeword shall be marked as corrupt. The bit stream is then binary descrambled.

Using the PHD.NEXT.PDB.OFFSET field of the decoded PHD (see 115.2.4.1.3, Figure 115–15) carried in the previous Transmit Block, the PCS receiver shall determine the alignment of the first PDB of a Transmit Block to extract the PDBs from the descrambled bit stream. The PDBs are then finally processed by the 64B/65B decoder to extract the GMII receive data stream. The 64B/65B decoding also includes the information that indicates the parts of the bit stream that have been determined to be corrupted (i.e., belong to MLCC codewords that cannot be corrected). Such corrupted data is signaled on the RX GMII by setting RX_ER = 1.

The 64B/65B decoder implementation shall produce the same result as the following MATLAB (see 1.3) code,[5]

```
% Variables definition
GMII.RX_ER      % GMII RX_ER signal, 1xL row vector
GMII.RX_DV      % GMII RX_DV signal, 1xL row vector
GMII.RXD        % GMII RXD bus, 1xL row vector
PCS_DEC_EN      % rx_gmii_enable (see 115.3.5.1) value for each GMII
```

[5]Copyright release for MATLAB code: Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

```
                % transfer, 1xL vector
PDB.TYPE        % PDB type field, 1x(L/8) row vector
PDB.PAYLOAD     % PDB payload field, 8x(L/8) matrix
PDB.PAYLOAD_ERR % PDB payload error flag, 8x(L/8) matrix. It indicates
                % if any of the bits within the corresponding byte of
                % the PDB payload belongs to a codeword that could not be
                % corrected.
PDB.TYPE_ERR    % PDB type field error flag, 1x(L/8) row vector. It
                % indicates if the type bit of the PDB belongs to a
                % codeword that could not be corrected.

% 64B/65B decoding procedure
for i = 1:length(PDB.TYPE)
   if (PDB.TYPE_ERR(i) | (PDB.TYPE(i) & PDB.PAYLOAD_ERR(1,i)))
      % Complete PDB is in error. Decode forward error propagation.
      GMII.RX_DV(8*(i-1)+1:8*(i-1)+8) = ones(1, 8);
      GMII.RX_ER(8*(i-1)+1:8*(i-1)+8) = ones(1, 8);
      GMII.RXD  (1:8, i)              = zeros(8, 1);

   elseif (PDB.TYPE(i))
      % Decode PDB.CTRL payload
      OFS  = bitand(PDB.PAYLOAD(1,i),   7*2^3)/2^3;
      LEN  = bitand(PDB.PAYLOAD(1,i),   7);
      CTRL = bitand(PDB.PAYLOAD(:,i).', 3*2^6)/2^6;

      % Assign initial data.
      if (OFS > 0)
         GMII.RX_DV(8*(i-1)+1:8*(i-1)+OFS) = ...
           ones(1,OFS);

         GMII.RX_ER(8*(i-1)+1:8*(i-1)+OFS) = ...
           PDB.PAYLOAD_ERR(2:OFS+1, i).';

         GMII.RXD(8*(i-1)+1:8*(i-1)+OFS) = ...
           PDB.PAYLOAD(2:OFS+1, i).';
      end

      % Assign control information.
      GMII.RX_DV(8*(i-1)+OFS+1:8*(i-1)+OFS+1) = ...
        (CTRL(1) == 0) | PDB.PAYLOAD_ERR(1, i).';

      GMII.RX_ER(8*(i-1)+OFS+1:8*(i-1)+OFS+1) = ...
        (CTRL(1) ~= 1) | PDB.PAYLOAD_ERR(1, i).';

      GMII.RXD(8*(i-1)+OFS+1:8*(i-1)+OFS+1) = ...
        (CTRL(1) == 2);

      if (LEN > 0)
         GMII.RX_DV(8*(i-1)+OFS+2:8*(i-1)+OFS+LEN+1) = ...
           (CTRL(OFS+2:OFS+LEN+1) == 0) | ...
           PDB.PAYLOAD_ERR(OFS+2:OFS+LEN+1, i).';

         GMII.RX_ER(8*(i-1)+OFS+2:8*(i-1)+OFS+LEN+1) = ...
           (CTRL(OFS+2:OFS+LEN+1) ~= 1) | ...
           PDB.PAYLOAD_ERR(OFS+2:OFS+LEN+1, i).';

         GMII.RXD(8*(i-1)+OFS+2:8*(i-1)+OFS+LEN+1) = ...
           (CTRL(OFS+2:OFS+LEN+1) == 2);
      end

      % Assign final data.
      if ((OFS+LEN+1) < 8)
         GMII.RX_DV(8*(i-1)+OFS+LEN+2:8*(i-1)+8) = ...
           ones(1, 8-(OFS+LEN+1));

         GMII.RX_ER(8*(i-1)+OFS+LEN+2:8*(i-1)+8) = ...
           PDB.PAYLOAD_ERR(OFS+LEN+2:8, i)';

         GMII.RXD(8*(i-1)+OFS+LEN+2:8*(i-1)+8) = ...
           PDB.PAYLOAD(OFS+LEN+2:8, i)';
      end
```

```
    else
        % Decode PDB.DATA payload
        GMII.RX_DV(8*(i-1)+1:8*(i-1)+8) = ones(1,8);
        GMII.RX_ER(8*(i-1)+1:8*(i-1)+8) = PDB.PAYLOAD_ERR(1:8, i).';
        GMII.RXD  (8*(i-1)+1:8*(i-1)+8) = PDB.PAYLOAD(1:8, i).';
    end
end

% When PCS_DEC_EN = 0, idles are generated
GMII.RX_DV = GMII.RX_DV & PCS_DEC_EN;
GMII.RX_ER = GMII.RX_ER & PCS_DEC_EN;

% Data reception error is signaled when PCS_DEC_EN transitions to 0
% in the middle of a packet transfer
idx_err = find([(diff(PCS_DEC_EN) < 0) 0] & GMII.RX_DV)+1;
GMII.RX_DV(idx_err) = 1;
GMII.RX_ER(idx_err) = 1;
```

115.3 Physical Medium Attachment (PMA) sublayer

The Physical Medium Attachment sublayer includes the transmit and receive functions and the protocols for management of the 1000BASE-H link. This management includes exchange of information that is encoded within the PHD and the state diagrams that control both the local and remote PHYs. PHD information is encoded into the PHS as defined in 115.2.3. PMA operational information is gathered and organized for transmission by the Header Builder (see Figure 115–9).

115.3.1 PMA transmit function

The PMA transmit function comprises the Tomlinson-Harashima precoding for the payload data sub-blocks and the power scaling for the pilot S1, pilot $S2_x$, PHS_x, and payload data sub-blocks. The resultant payload PAM16 symbols from PCS transmit function are THP processed to compensate intersymbol interference produced in the communication channel. The THP processing is not applied to pilot S1, pilot $S2_x$, and PHS_x sub-blocks. The power scaling, with different factors, is performed producing similar dynamic range in every part of the Transmit Block before the symbols are transmitted to the PMD sublayer.

115.3.1.1 Payload data Tomlinson-Harashima precoding

The PAM16 symbols from the payload data symbol scrambler (see 115.2.4.4), x, shall be processed by the Tomlinson-Harashima precoder (THP) to produce a precoded sequence of symbols, y, according to Equation (115–19), Equation (115–20), and Equation (115–21):

$$v(m) = \sum_{i=0}^{8} c(i)y(m-i-1) \tag{115–19}$$

$$u(m) = x(m) + v(m) \tag{115–20}$$

$$y(m) = \mathrm{mod}(u(m) + 16, 32) - 16 \tag{115–21}$$

where the modulo operator is defined in Equation (115–4). The THP precoded symbols can take any value in the interval $-16 \le y(m) < +16$. The coefficients of the finite-impulse-response (FIR) feedback filter $c(i)$ are set from the PHD received from the link partner (see 115.3.6). The length of the feedback filter is 9 taps. The state of the feedback filter shall be reset before the transmission of any payload data sub-block. The Tomlinson-Harashima precoder is illustrated in Figure 115–21.

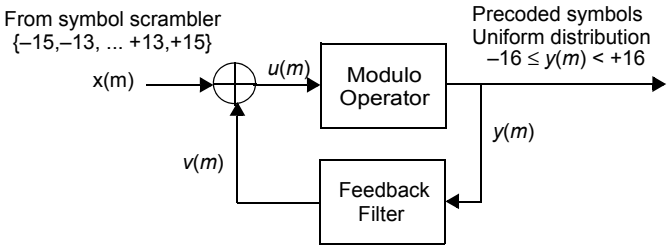

Figure 115–21—Tomlinson-Harashima precoding block diagram

115.3.1.2 Transmit power scaling

The symbols of pilot S1, pilot $S2_x$, PHS_x sub-blocks, and payload data sub-blocks shall be scaled before transmission to the PMD transmit function, by multiplying the symbols by the corresponding scaling factor specified in Table 115–5. As indicated in Table 115–5, the scaling factor used for each symbol depends on the part of the Transmit Block to which the symbol belongs.

Power scaling shall be performed directly to the symbols received from the PCS transmit for pilot S1, pilot $S2_x$, and PHS_x sub-blocks. For the payload data sub-blocks, the power scaling shall be performed to the output symbols of the Tomlinson-Harashima precoder.

Table 115–5—Transmit power scaling factors

Transmit Block part	Scaling factor
Pilot S1 sub-blocks	255/256
Pilot $S2_x$ sub-blocks	9/64
PHS_x sub-blocks	255/256
THP processed payload data sub-blocks	1/16

115.3.2 PMA receive function

The PMA receive function comprises clock recovery for correct time sampling of received symbols and adaptive channel equalization.

The PMA performs clock recovery on the received signal. The clock recovery includes coarse timing recovery for symbol synchronization and fine timing recovery to provide a stable clock to sample the received signal from the PMD with a suitable phase for reliable reception (see 115.3.7.1).

Equalization is performed using the adaptive THP protocol (115.3.6) coordinated between the receiver and link partner transmitter to condition the transmitted signal for the characteristics of the fiber optic channel. The receiver estimates the coefficients that are to be used by the remote PHY transmitter to precode the payload data sub-blocks [coefficients $c(i)$ in 115.3.1.1]. This estimation should be based on received pilot $S2_x$ sub-blocks.

In general, harmonic distortion that affects the received signal can exist due to the non-linear response of the PMD photonics. The PMA receiver should implement non-linear channel response compensation in addition to the THP protocol. For estimation of the filters that linearize the channel, the PHY should also use the received pilot $S2_x$ sub-blocks. The channel linearization technique is up to the implementer but is to be fully implemented in the PHY receiver; it does not require coordination with the link partner transmission.

115.3.3 Interface to the PMD

The interface between the PMA and the PMD are signals for which no specific implementation is specified.

115.3.3.1 Signals transmitted to the PMD

Any signal transmitted to the PMD by the PMA transmitter can be expressed in a general form independent of the specific part of the Transmit Block (see 115.2.1) as follows:

$$x(n) = SF(n) \times F_M\left(a(n) + \sum_{i=0}^{8} x(n-i-1)c(i)\right) \tag{115–22}$$

where, $a(n)$ is a PAM-M modulation symbol that can take its value from the set $\{-M+1, -M+3, \ldots +M-3, +M-1\}$ to be transmitted at time instants $n \times T_s$, where T_s is the transmit symbol period (nominally $T_s = 1000/325$ ns), $SF(n)$ is the power scaling factor specified in Table 115–5 for each part of the Transmit Block according to 115.3.1.2, $c(i)$ are the coefficients of the THP specified in 115.3.1.1, and the nonlinear operation $F_M(\alpha) = \mathrm{mod}(\alpha + M, 2M) - M$ corresponds to moving the signal $\alpha(n)$ to a reduced signal $\beta(n) = \alpha(n) + 2M \times m(n)$ with the integer $m(n)$ chosen for each sample such that the output lies in the interval $-M \le \beta(n) < M$, when THP is used.

When a pilot S1 sub-block or PHS_x sub-block is transmitted, $M = 2$. For generation of an $S2_x$ sub-block, $M = 8$. For the zero symbol sequences that prefix and postfix each pilot S1 sub-block, pilot $S2_x$ sub-block, and PHS_x sub-block, $a(n) = 0$.

When payload data sub-blocks are transmitted, $M = 16$. Only for this part of the Transmit Block can the coefficients $c(i)$ take a value different than zero, when the THP coefficients provided by the link partner are used according to the protocols defined in 115.3.6.

For any part of the Transmit Block, after scaling, the transmitter output signal $x(n)$ fits $-1 \le x(n) < +1$.

115.3.3.2 Signals received from PMD

Signals received from the PMD can be expressed as pulse-amplitude modulated signals that have been filtered by a non-linear channel and corrupted by noise as follows in Equation (115–23):

$$\begin{aligned} y(n) = {} & w_{o0} + \sum_{l_1=0}^{L} w_{o1}(l_1)x(n-l_1) + \sum_{l_1=0}^{L}\sum_{l_2=0}^{L} w_{o2}(l_1, l_2)x(n-l_1)x(n-l_2) + \ldots \\ & \ldots + \sum_{l_1=0}^{L}\sum_{l_2=0}^{L}\cdots\sum_{l_P=0}^{L} w_{oP}(l_1, l_2, \ldots l_P)x(n-l_1)x(n-l_2)\ldots x(n-l_P) + N(n) \end{aligned} \tag{115–23}$$

where the received signal $y(n)$ is sampled by the PMA receive function with the recovered clock, at the optimum phase and with a frequency equal to the transmit symbol clock with nominal value of 325 MBd.

$x(n)$ is the transmitted signal from the PMA transmit function to the PMD transmit function, $N(n)$ is the additive noise from PMD receiver due optical signal conversion, and w_{ox} are the kernels of a truncated Volterra series that represents the non-linear response of the communication channel.

The received signal $y(n)$ of Equation (115–23) includes the effect of the end-to-end communication channel composed of all the elements from the PMA transmitter to the PMA receiver, including the conversion to optical signal carried out by the PMD transmitter, the fiber optic channel, and the conversion from optical signal carried out by the PMD receive function.

115.3.4 Physical Header Data (PHD)

The PHD shall consist of the fields detailed in Table 115–6.

Table 115–6—PHD definition

Field name	Description	Number of bits	Valid values
PHD.TX.NEXT.MODE	Transmission mode of the next Transmit Block, indicated to link partner to align its reception (see 115.5.1)	3	0: normal transmission 1: zeros transmission for BER test 2 through 7: reserved
PHD.TX.NEXT.THP.SETID	Identifier of the THP coefficients set that will be used to transmit the next Transmit Block (see 115.3.6.2)	2	0: next Transmit Block is not THP processed 1, 2, 3: THP set identifier
PHD.TX.NEXT.PDB.OFFSET	Encodes the number of bits between the first payload bit of the next Transmit Block and the start of the first PDB in that block (see 115.2.4.1.3). Offset 0 indicates the first PDB starts aligned to first payload bit of Transmit Block	7	0x00 through 0x40
PHD.RX.REQ.THP.SETID	Requested THP coefficients set identifier (see 115.3.6.3)	2	0: no request to apply the THP coefficients received in PHD.RX.REQ.THP.COEF[8:0] 1, 2, 3: THP set identifier
PHD.RX.REQ.THP.COEF[0]	Requested THP coefficients when PHD.RX.REQ.THP.SETID is not equal to 0 (see 115.3.6.3). These are the 9 coefficients $c(i)$ requested to be used in transmission according to Equation (115–19) (see 115.3.1.1)	12	Fixed-point formatted (12, 2) (see 115.3.8)
PHD.RX.REQ.THP.COEF[1]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[2]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[3]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[4]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[5]		12	Fixed-point formatted (12.2)
PHD.RX.REQ.THP.COEF[6]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[7]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[8]		12	Fixed-point formatted (12, 2)

Table 115–6—PHD definition *(continued)*

Field name	Description	Number of bits	Valid values
PHD.RX.LINKSTATUS	Indicates whether the local PHY is able to receive PAM16 symbols belonging to payload data sub-blocks with reliability. The value of this field is determined by the PHY quality monitor state diagram (see 115.3.7.4). The local PHY uses this received PHD field to determine the value of the variable rem_rcvr_status (see 115.3.5.4)	1	0: NOT_OK 1: OK
PHD.RX.HDRSTATUS	Indicates whether the local PHY is able to receive the PHD from its link partner with reliability. The value of this field is determined by the local PHD reception monitor state diagram. The local PHY uses this received PHD field to determine the value of the variable rem_rcvr_hdr_lock (see 115.3.5.5)	1	0: NOT_OK 1: OK
PHD.RX.LINKMARGIN	The value of this field is determined by the PHY quality monitor state diagram (see 115.3.7.4) in response to link margin estimation as defined in 115.3.7.2. Upon PHD reception, the field is stored in bits 3.521.7:0 (see 45.2.3.47f.1)	8	This field is fixed-point formatted (8, 3) and is provided in $\log_2$ units (see 115.3.7.2). See 115.3.8 for fixed-point format.
PHD.CAP.LPI	This field indicates the PHY supports and has enabled EEE, and that it is able to transmit and receive Low Power Idle (see 115.4)	1	0: EEE is not supported or is disabled 1: EEE is supported and is enabled
PHD.CAP.OAM	This field indicates the PHY supports and has enabled 1000BASE-H OAM, and that it is able to transmit and receive management information by using the PHD.OAM.* fields (see 115.9)	1	0: 1000BASE-H OAM is not supported or is disabled 1: 1000BASE-H OAM is supported and is enabled
	Reserved	58	0
PHD.OAM.DATA0	1000BASE-H OAM message data field 0. See 115.9	12	0x000 through 0xFFF
PHD.OAM.MSGT	1000BASE-H OAM message identification bit. See 115.9	1	0 or 1
PHD.OAM.MERT	1000BASE-H OAM STA read identification bit (see 115.9)	1	0 or 1

Table 115–6—PHD definition *(continued)*

Field name	Description	Number of bits	Valid values
PHD.OAM.PHYT	1000BASE-H OAM PHY reception identification bit (see 115.9)	1	0 or 1
	Reserved	1	0
PHD.OAM.DATA1	1000BASE-H OAM message data field 1 (see 115.9)	16	0x0000 through 0xFFFF
PHD.OAM.DATA2	1000BASE-H OAM message data field 2	16	0x0000 through 0xFFFF
PHD.OAM.DATA3	1000BASE-H OAM message data field 3	16	0x0000 through 0xFFFF
PHD.OAM.DATA4	1000BASE-H OAM message data field 4	16	0x0000 through 0xFFFF
PHD.OAM.DATA5	1000BASE-H OAM message data field 5	16	0x0000 through 0xFFFF
PHD.OAM.DATA6	1000BASE-H OAM message data field 6	16	0x0000 through 0xFFFF
PHD.OAM.DATA7	1000BASE-H OAM message data field 7	16	0x0000 through 0xFFFF
PHD.OAM.DATA8	1000BASE-H OAM message data field 8	16	0x0000 through 0xFFFF
	Reserved	368	0

The fields PHD.TX.NEXT.* are used by the local PHY to provide the link partner with information about the next Transmit Block, so that the remote PHY can align its reception.

The fields PHD.RX.* are transmitted to inform the link partner of the status of the local reception. Specifically, the fields PHD.RX.REQ.THP.SETID and PHD.RX.REQ.THP.COEF[8:0] allow the PHY to request the update of link partner THP coefficients (see 115.3.6). Additionally, PHD.RX.LINKSTATUS indicates whether payload data sub-blocks are being received with reliability, and PHD.RX.HDRSTATUS signals the correct/incorrect reception of PHDs. The field PHD.RX.LINKMARGIN is used to report the link margin.

PHD.RX.REQ.THP.COEF[8:0] and PHD.RX.LINKMARGIN fields are fixed-point formatted (12, 2) and (8, 3), respectively. See 115.3.8 for fixed-point format definition.

PHD.CAP.* fields indicate if the local PHY is using optional features. PHD.CAP.LPI is used by the PHY to advertise that Energy-Efficient Ethernet (EEE) is supported and that it is enabled, and the field PHD.CAP.OAM signals that the PHY implements the capability to run the 1000BASE-H OAM message exchange protocol and that it is enabled.

PHD.OAM.* fields are used to transmit and receive 1000BASE-H OAM messages.

All the PHD fields are transmitted from the least to the most significant bit and are transmitted from top to bottom of Table 115–6.

Each PHY has to deal with transmit and receive PHDs simultaneously. The prefix LOCPHD refers to the fields of the PHD to be included in the next Transmit Block transmitted to the link partner (from the local PHY). LOCPHD fields assigned by the state diagrams shall be sampled at the start of a Transmit Block by the Header Builder to create the PHS included in that current Transmit Block.

The prefix REMPHD refers to the fields of the most recent PHD received, decoded, and validated from the link partner (from the remote PHY). The new values of REMPHD fields shall be available to the state diagrams and registers immediately after reception, decoding, and validation of the entire PHS (PHS_0 to PHS_{13}) and before the reception of the Transmit Block that includes that PHS is completed.

115.3.5 PHY control

115.3.5.1 PHY control state variables

hdr_crc16_status
: Result of the CRC16 evaluation for a received PHD from the link partner; this variable is assigned for each received PHD.
  Values: OK: The most recent received PHD is correct as determined by CRC16 verification
  NOT_OK: The most recent received PHD is not correct as determined by CRC16 verification

hdr_fail_count
: Variable used to count the reception of contiguous erroneous PHDs.

link_control
: Variable that controls PMA functional operation. All state diagrams respond to the open-ended link_control = DISABLE.
  Values: DISABLE: Prevent operation of PMA sublayer
  ENABLE: Permit operation of PMA sublayer

link_status
: Variable that is set by the link monitor state diagram and used by PHY TX and PHY RX control state diagrams to control the 64B/65B encoder and 64B/65B decoder operation.
  Values: OK: The link has been established between link partners with data reliability in both communication directions
  FAIL: Link is not established (one or both directions are not providing reliable payload data decoding)

loc_rcvr_hdr_lock
: Variable set by the local PHD reception monitor state diagram to indicate the reliability of PHD reception.
  Values: OK: Local PHD reception is reliable
  NOT_OK: Local PHD reception is unreliable

loc_rcvr_status
: Variable set by the PHY quality monitor state diagram to indicate correct or incorrect payload data decoding by the local PHY receiver.
  Values: OK: Payload data reception by the local PHY is reliable
  NOT_OK: Payload data reception by the local PHY is unreliable

new_rxblock_event
: Signal sent by the PHY receiver to indicate the start of reception of a new Transmit Block. This event persists only long enough to cause one state diagram transition.

new_rxphd_event
: Signal sent by the PHY receiver to indicate the complete reception (including data decoding and CRC16 checking) of a new PHD from the link partner. This event persists only long enough to cause one state diagram transition.

pma_reset
: Variable that causes reset of all PMA functions. PMA reset occurs with power on or the PHY

reset being set to one (bit 1.0.15). All state diagrams respond to the open-ended pma_reset = ON.
Values: ON: Reset is asserted
OFF: Reset is deasserted

rcvr_clock_lock
Variable set by the PMA receive clock recovery function to indicate that the clock has been properly recovered from the received signal.
Values: OK: Clock is stable and phase adjusted for sampling the received signal
NOT_OK: Clock has not been recovered from the received signal and/or it is not stable

rcvr_hdr_lock
Variable set by the PHD monitor state diagram to indicate the reliability of both the PHD transmission from local to remote PHY and the PHD reception from remote to local PHY.
Values: OK: PHD transmission and reception are reliable
NOT_OK: PHD transmission or reception are unreliable

rcvr_thp_lock
Variable set by the THP REQ state diagram (see 115.3.6.3) to indicate whether the Tomlinson-Harashima precoding is initialized, therefore the PHY is receiving payload data sub-blocks THP processed with the coefficients that were requested by the THP REQ state diagram.
Values: OK: THP is initialized; payload data are received THP processed
NOT_OK: THP is not initialized

rem_rcvr_hdr_lock
Variable set by the remote PHD reception monitor state diagram to indicate the reliability of PHD reception in the remote PHY (link partner).
Values: OK: Link partner PHD reception is reliable
NOT_OK: Link partner PHD reception is unreliable

rem_rcvr_status
Variable set by the link monitor state diagram. It indicates the receiver status of the remote (link partner) PHY payload data decoding.
Values: OK: Payload data reception by the remote PHY is reliable
NOT_OK: Payload data reception by the remote PHY is unreliable

rx_gmii_enable
Variable set by the PHY RX control state diagram to control the 64B/65B decoder operation (see 115.2.5).
Values: TRUE: The 64B/65B decoder receives PDBs from the link partner and decodes them into GMII receive data stream transfers
FALSE: The 64B/65B decoder does not decode received PDBs from the link partner

s1_synch
Variable set by the PMA receive clock recovery function to indicate synchronization with the start of Transmit Blocks.
Values: OK: Synchronization based on pilot S1 signal has been achieved
NOT_OK: Synchronization has not been achieved

tx_enable
Variable set by the PHY TX control state diagram to enable PCS and PMA transmission.
Values: TRUE: PCS and PMA transmission is enabled
FALSE: PCS and PMA transmission is disabled

tx_gmii_enable
Variable set by the PHY TX control state diagram to control the 64B/65B encoder operation (see 115.2.4.1.2).
Values: TRUE: The 64B/65B encoder encodes the GMII transmit data stream transfers into PDBs

FALSE: The 64B/65B encoder does not encode the GMII transmit data stream. Normal inter-frame is encoded in transmitted PDBs

tx_gmii_idle

Variable that indicates the idle status of the GMII transmit data path.

Values: TRUE: The value of TX_EN signal of the current GMII transfer in GMII transmit stream is 0
FALSE: The value of TX_EN signal of the current GMII transfer in GMII transmit stream is 1

115.3.5.2 PHY TX control state diagram

Transmit operation shall conform to the PHY TX control state diagram in Figure 115–22.

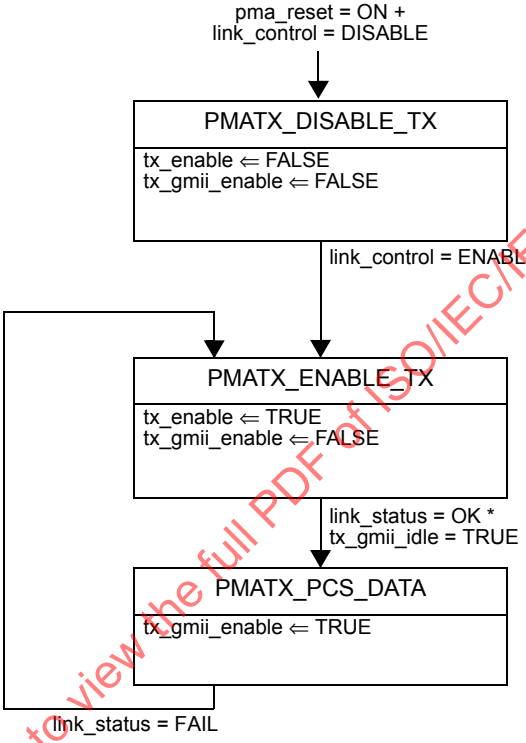

Figure 115–22—PHY TX control state diagram

Upon reset or disable of the PMA, PHY transmit operation is disabled (state PMATX_DISABLE_TX). Once the PMA is enabled (link_control = ENABLE), the local PHY starts sending Transmit Blocks as explained in 115.2.1 (state PMA_ENABLE_TX), so that the remote PHY can perform clock recovery and train its equalizers (tx_enable ⇐ TRUE).

While establishing the bi-directional link, the 64B/65B PCS encoder does not encode the GMII transmit stream (tx_gmii_enable ⇐ FALSE). Once the bidirectional link is established, the 64B/65B encoder checks, and if necessary, waits until the GMII transmit data stream transfer is not part of a packet or error propagation (link_status = OK * tx_gmii_idle = TRUE); and then begins encoding the GMII transmit stream into PDBs (tx_gmii_enable ⇐ TRUE in state PMATX_PCS_DATA). If one of the link partners fails to receive payload data sub-blocks with reliability (link_status = FAIL), the 64B/65B PCS encoder does not encode the GMII transmit stream until the bidirectional link is re-established.

115.3.5.3 PHY RX control state diagram

Receive operation shall conform to the PHY RX control state diagram in Figure 115–23.

Upon reset or disable of the PMA, PHY receive operation is disabled. Once the PMA is enabled (link_control = ENABLE), the PHY receiver begins link establishment by recovering clock from the received signal. The clock recovery comprises two stages. The first stage is coarse timing recovery in PMARX_TIMING_COARSE, where symbol synchronization shall be performed using the a priori known pilot signal contained in the S1 sub-block at the beginning of each received Transmit Block (see Figure 115–4). After symbol synchronization is achieved (s1_synch = OK), fine timing recovery shall be carried out in order to provide a stable clock that samples the received signal with a suitable phase for reliable reception (see 115.3.7.1). Fine timing recovery can be implemented with data-aided algorithms that use the received pilot S1 and pilot $S2_x$ sub-blocks.

When clock is stable (rcvr_clock_lock = OK), the PHY receiver shall train the equalizers based on the received pilot $S2_x$ sub-blocks in order to compensate the intersymbol interference caused by the communication channel. Blind tracking algorithms for timing recovery can be enabled after the equalizer training has finished.

Once the equalizers have been properly estimated, the PHY receiver processes each PHD from the link partner to determine if PHD reception is reliable in both directions. The state diagrams that monitor the reliability of PHD reception are described in 115.3.5.5.

As soon as both link partners detect reliable PHD reception (rcvr_hdr_lock = OK), the PHY receiver shall initialize the THP following the state diagram explained in 115.3.6.3. Once the local PHY is receiving payload data sub-blocks THP processed with the coefficients that were requested to the link partner (rcvr_thp_lock = OK), it has to determine according to the state diagram described in 115.3.7.3 whether this reception is reliable.

Once a bidirectional link is established (link_status = OK), the 64B/65B PCS decoder begins to decode the received PDBs onto the GMII receive data stream (rx_gmii_enable ⇐ TRUE). Furthermore, both link partners are able to properly use the PHD to carry out continuous adaptation of THP coefficients.

If one of the link partners fails to receive payload data sub-blocks with reliability (link_status = FAIL), the 64B/65B PCS decoder does not decode PDBs received from link partner into the GMII receive stream (rx_gmii_enable ⇐ FALSE) until the bidirectional link is re-established (link_status = OK).

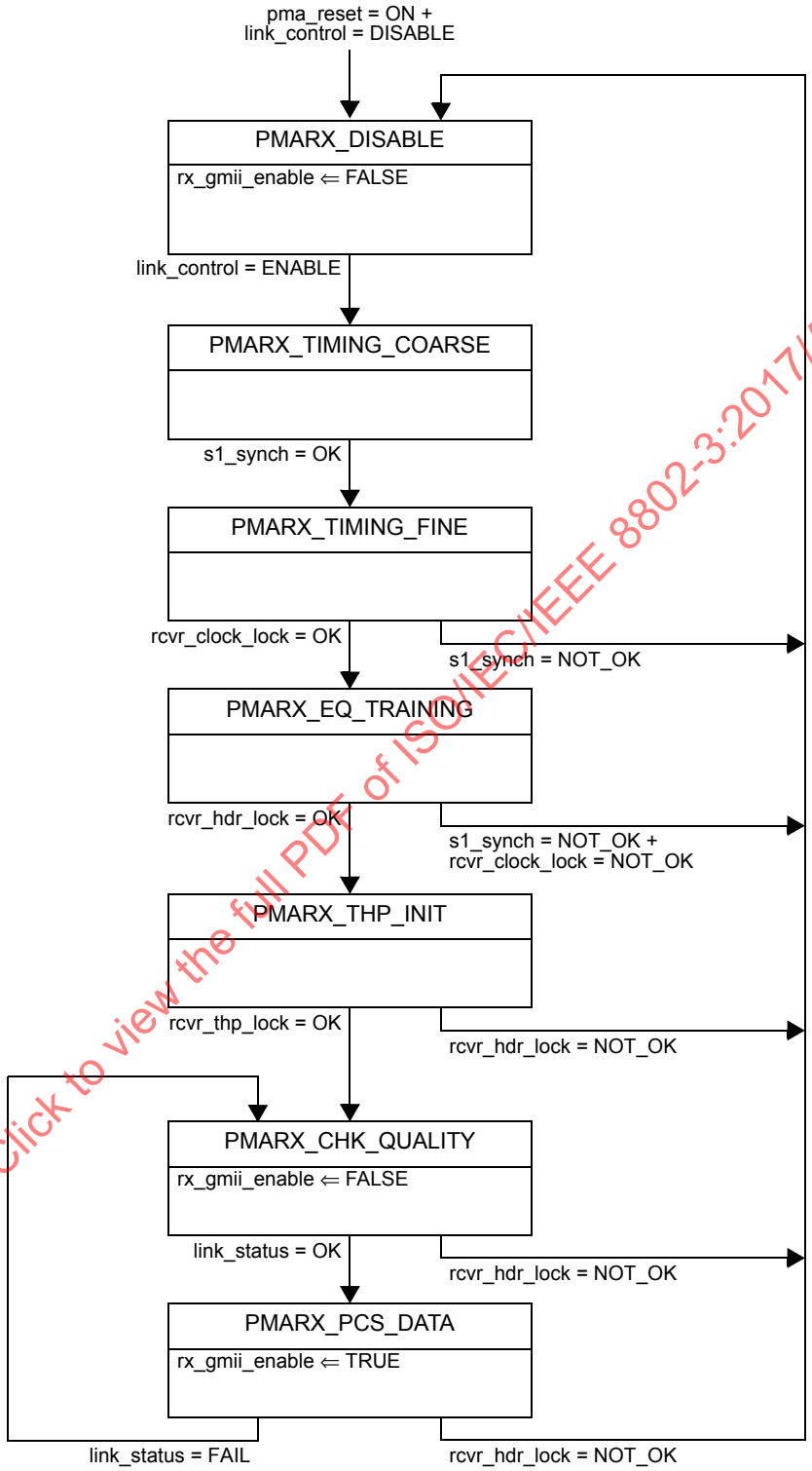

Figure 115–23—PHY RX control state diagram

115.3.5.4 Link monitor state diagram

Link status shall be determined as specified by the link monitor state diagram in Figure 115–24. The state diagram determines the value of link_status and rem_rcvr_status state variables.

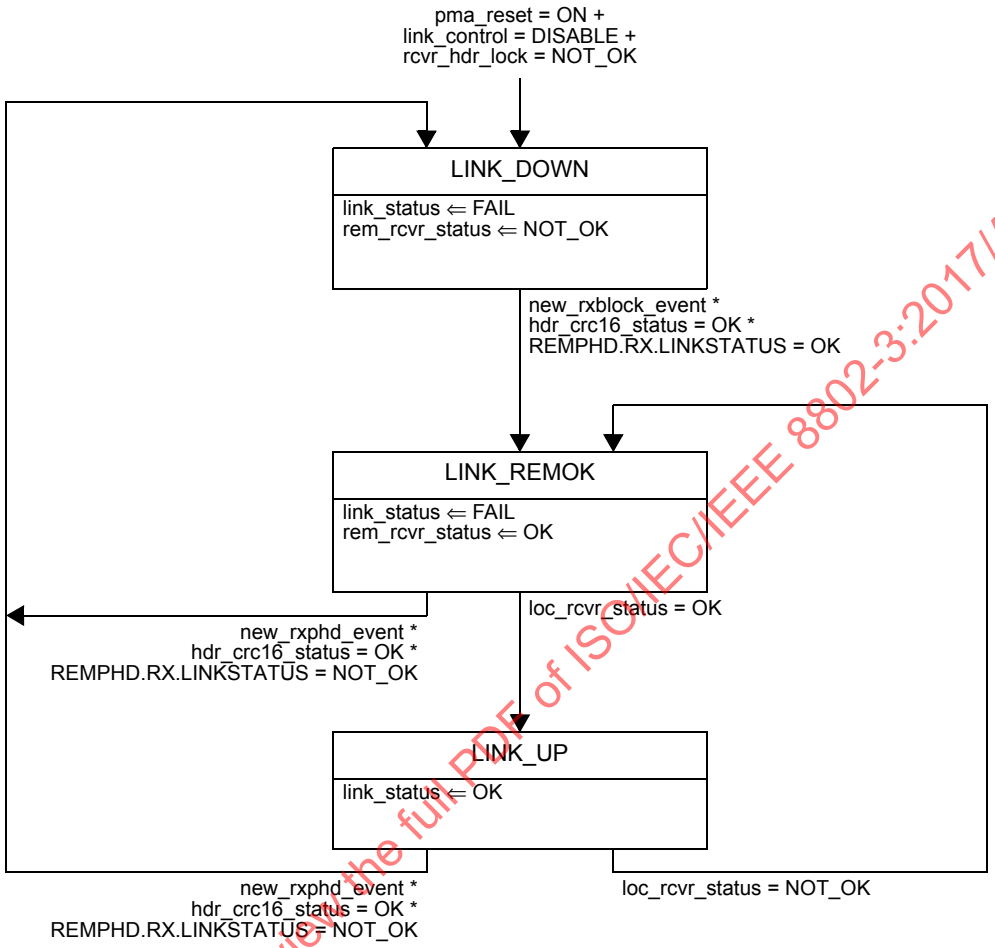

Figure 115–24—Link monitor state diagram

Upon reset, disable of the PMA or unreliable PHD communication, the link is lost (link_status ⇐ FAIL) and the remote receiver status is unknown (rem_rcvr_status ⇐ NOT_OK). When the remote PHY indicates reliable reception (REMPHD.RX.LINKSTATUS = OK), the state diagram transitions to the LINK_REMOK state synchronously on the event of receiving a new Transmit Block (new_rxblock_event). Once in this state, the bidirectional link is established (link_status ⇐ OK) when local reliable reception is signaled by the PHY quality monitor state diagram (loc_rcvr_status = OK).

If the local PHY fails to receive payload data sub-blocks with reliability (loc_rcvr_status = NOT_OK) but the remote PHY reception is indicated as reliable (REMPHD.RX.LINKSTATUS = OK), the bidirectional link is lost and the state diagram transitions to LINK_REMOK state that waits for the local receiver reliability is recovered. If the remote PHY receiver indicates that it does not operate with reliability (REMPHD.RX.LINKSTATUS = NOT_OK), the bidirectional link is lost and the state diagram transitions to LINK_DOWN state in any case.

115.3.5.5 PHD monitor state diagrams

The reliability of PHD reception and transmission shall be determined by the PHD monitor state diagrams in Figure 115–25, Figure 115–26, and Figure 115–27.

The local PHD reception monitor state diagram of Figure 115–25 monitors the PHD reception reliability for the local PHY and indicates it via the variable loc_rcvr_hdr_lock. Upon reset or disable of the PMA, or if the local PHY fails to reliably receive PHDs (loc_rcvr_hdr_lock ⇐ NOT_OK), this is indicated to the link partner by assigning NOT_OK to the field LOCPHD.RX.HDRSTATUS. In the state LOCHDR_UNLOCK, the receiver waits for reception of a valid PHD (i.e., one with correct CRC16) on entry, and the variable hdr_fail_count (the count of contiguous PHDs received with errors) is reset (hdr_fail_count ⇐ 0).

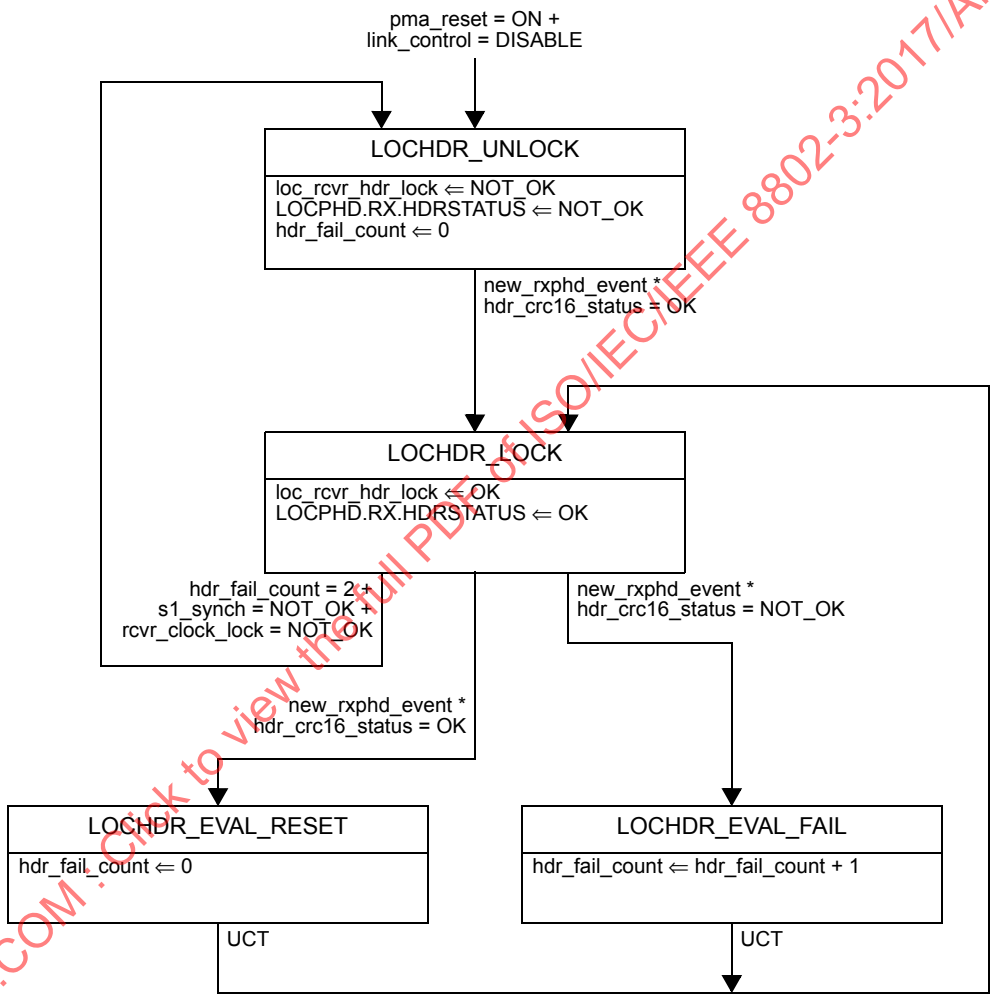

Figure 115–25—Local PHD reception monitor state diagram

In LOCHDR_UNLOCK, reception of one correct PHD triggers the transition to the state LOCHDR_LOCK. On entry to LOCHDR_LOCK the variable loc_rcvr_hdr_lock and the field LOCPHD.RX.HDRSTATUS are assigned the value OK. The PHY keeps checking the CRC16 of received PHDs, incrementing hdr_fail_count with each erroneous PHD (in state LOCHDR_EVAL_FAIL) and resetting hdr_fail_count with each valid PHD (in state LOCHDR_EVAL_RESET). If hdr_fail_count reaches the limit of 2, or the

clock recovery function detects that the PHY has lost synchronization, then the state transitions back to LOCHDR_UNLOCK.

The remote PHD reception monitor state diagram of Figure 115–26 monitors PHD reception reliability reports from the remote PHY and indicates the status via the variable rem_rcvr_hdr_lock. Upon reset, disable of the PMA or unreliable local PHD reception, the status variable rem_rcvr_hdr_lock is assigned the value NOT_OK pending the arrival of a new PHD from the link partner (REMHDR_WAIT state). From then on, the value of the variable rem_rcvr_hdr_lock is updated with the value of the field REMPHD.RX.HDRSTATUS (rem_rcvr_hdr_lock ⇐ REMPHD.RX.HDRSTATUS).

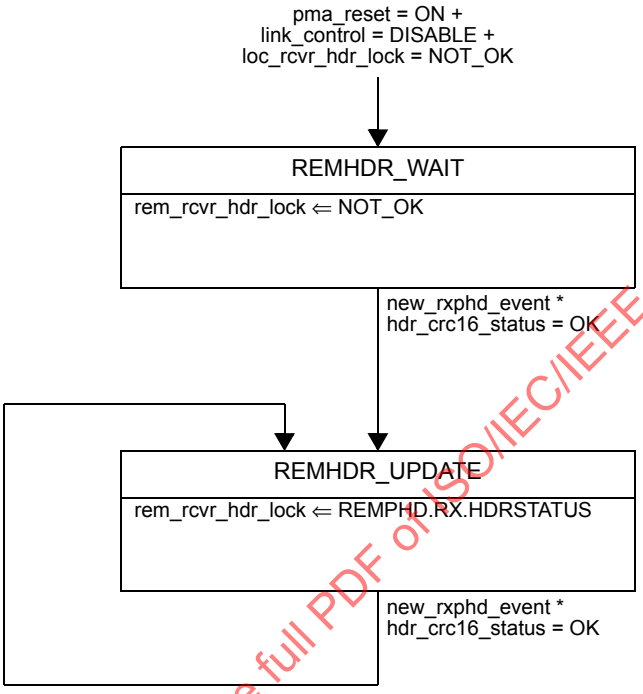

Figure 115–26—Remote PHD reception monitor state diagram

The PHD monitor state diagram of Figure 115–27 indicates via the variable rcvr_hdr_lock if both link partners are reliably receiving PHDs. Upon reset or disable of the PMA, the PHD communication is unreliable (rcvr_hdr_lock ⇐ NOT_OK). Whenever a new PHD is received from the link partner, the status of both the local (variable loc_rcvr_hdr_lock) and remote (variable rem_rcvr_hdr_lock) PHD reception are updated as indicated in Figure 115–25 and Figure 115–26, respectively.

A transition from the HDR_UNLOCK state to the HDR_LOCK state takes place when both the local and the remote PHYs are reliably receiving PHDs (loc_rcvr_hdr_lock = OK and rem_rcvr_hdr_lock = OK). The value OK is then assigned to the variable rcvr_hdr_lock to signal the reliable transmission and reception of PHDs. Subsequently, if either of the link partners fail to receive PHDs reliably (loc_rcvr_hdr_lock = NOT_OK or rem_rcvr_hdr_lock = NOT_OK), a transition to HDR_UNLOCK occurs resulting in assigning NOT_OK to the rcvr_hdr_lock variable.

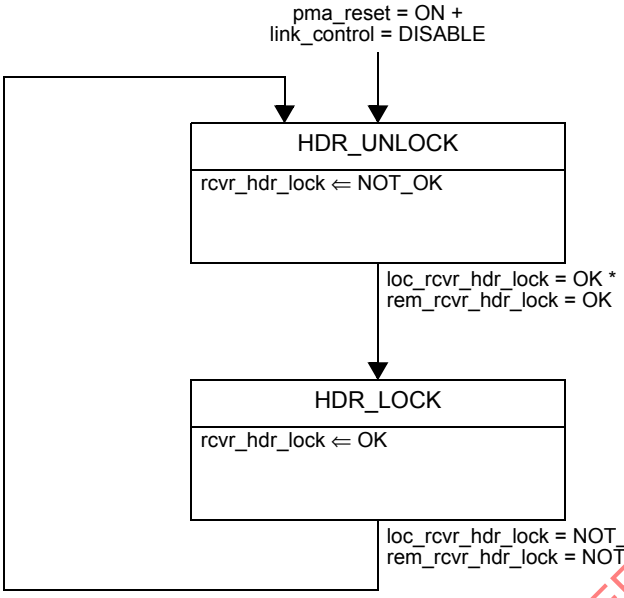

Figure 115–27—PHD monitor state diagram

115.3.6 Adaptive THP protocol

The receiver estimates the coefficients (see 115.3.2) that are used by the remote PHY transmitter for THP processing of the payload data sub-blocks [coefficients $c(i)$ in 115.3.1.1]. The state diagrams that control THP coefficients allow for dynamic adaptation of the coefficients before and after the link is established. The PHY receiver may dynamically determine variations in the channel response and request the partner to use a new set of THP coefficients. The methods to determine the channel response variation and estimate THP coefficients are implementation dependent.

The local receiver assigns a set identifier (integer number higher than 0 and lower than 4) to each new estimation to unambiguously identify it, and uses it to request the remote transmitter to apply a given set of coefficients for THP by using the field LOCPHD.RX.REQ.THP.SETID. The set of coefficients itself is sent to the link partner by using the fields LOCPHD.RX.REQ.THP.COEF[8:0].

Once the local receiver has performed the request, it waits until the remote transmitter signals via REMPHD.TX.NEXT.THP.SETID that payload data in the next Transmit Block is THP processed with the requested set of coefficients. From then on, the local receiver adapts its circuitry according to the THP coefficients used at the remote transmitter and is allowed to perform a new request to change them.

A formal definition of the THP coefficients adaptation protocol is provided in the form of state diagrams in the following subclauses.

115.3.6.1 Adaptive THP state variables

The following defines all the variables used in the adaptive THP state diagrams that have not been previously introduced:.

est_thp_coef
: Variable set by the PHY receiver that contains the coefficients estimated to compensate inter-symbol interference by means of Tomlinson-Harashima Precoding. est_thp_coef is a set of 9

real numbers.
Values: Real numbers that take values such that –2 ≤ est_thp_coef < +2

loc_thp_coef
Variable set by the adaptive THP TX state diagram. It contains the local coefficients used by the PHY for THP processing of payload data sub-blocks. loc_thp_coef is a set of 9 real numbers representing the coefficients of the feedback filter of THP [$c(i)$ in 115.3.1.1].
Values: Real numbers that take values such that –2 ≤ loc_thp_coef < +2

new_thp_coef_event
Signal sent by the PHY receiver to indicate the estimation of a new set of THP coefficients is available. This event persists only long enough to cause one state diagram transition.

new_txblock_event
Signal sent by the PHY transmitter to indicate the start of a new Transmit Block. This event persists only long enough to cause one state diagram transition.

req_thp_coef
Variable set by the adaptive THP TX state diagram when a correct PHD is received. This variable holds the coefficients requested by the link partner to be used for THP processing of the payload data sub-blocks. req_thp_coef is a set of 9 real numbers in fixed-point format (see 115.3.8) as the fields REMPHD.RX.REQ.THP.COEF[8:0].
Values: Real numbers that take values such that –2 ≤ req_thp_coef < +2

req_thp_setid
Variable set by the adaptive THP TX state diagram when a correct PHD is received. It is the set identifier assigned to the THP coefficients requested by the link partner.
Values: 0: No request to change the THP coefficients
1, 2, 3: Requested set identifier

thp_coef
Variable set by the adaptive THP REQ state diagram to store the last THP coefficients requested to the link partner. thp_coef is a set of 9 real numbers.
Values: Real numbers that take values such that –2 ≤ thp_coef < +2

thp_setid
Variable set by the adaptive THP REQ state diagram to store the last THP set identifier requested to the link partner.
Values: 0: Reset value
1, 2, 3: Set identifier

115.3.6.2 Adaptive THP TX state diagram

The update of the THP filter coefficients per link partner requests shall conform to the Adaptive THP TX state diagram in Figure 115–28.

Upon reset, disable of the PMA or unreliable PHD communication, transmitted payload data is no longer THP processed (THPTX_DISABLE state). This causes THP coefficients to be set to zero (loc_thp_coef ⇐ 0) and the field LOCPHD.TX.NEXT.THP.SETID is assigned the value 0 to indicate to the remote PHY that THP is disabled.

Once the transmission and reception of PHDs are reliable (rcvr_hdr_lock = OK), the local PHY waits for a request to adapt its THP coefficients from the link partner (THPTX_WAITFOR_REQ state).

As soon as the value of the field REMPHD.RX.REQ.THP.SETID is not equal to zero, the field REMPHD.RX.REQ.THP.COEF also contains a THP coefficients adaptation request from the link partner. The local PHY stores both the set identifier associated with the request (req_thp_setid ⇐ REMPHD.RX.REQ.THP.SETID) and the requested coefficients (req_thp_coef ⇐ REMPHD.RX.REQ.THP.COEF). This corresponds to the state THPTX_RECEIVE_REQ.

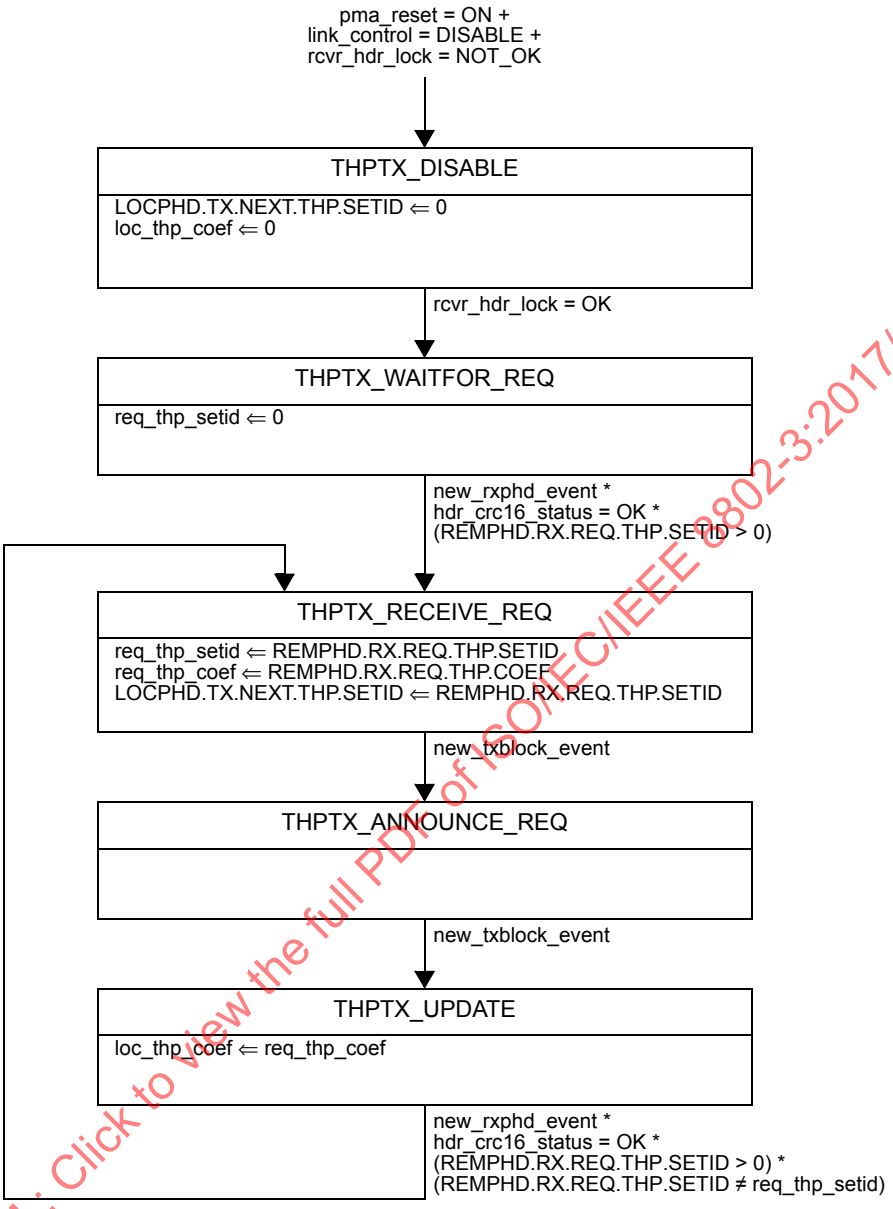

Figure 115–28—Adaptive THP TX state diagram

Triggered with the start of a new Transmit Block a transition to THPTX_ANNOUNCE_REQ occurs, where the local PHY announces that requested coefficients are to be used (LOCPHD.TX.NEXT.THP.SETID ⇐ req_thp_setid assignment of previous state).

After the announcement, the start of another new Transmit Block triggers the state transition to THPTX_UPDATE, and payload data sub-blocks of Transmit Blocks are then THP processed with the requested set of coefficients (loc_thp_coef ⇐ req_thp_coef) until a request to change THP coefficients from the link partner becomes effective. This happens when the value of the field REMPHD.RX.REQ.THP.SETID is not equal to zero and is different from the value of the variable req_thp_setid, and the new set of coefficients is stored, announced, and applied as previously explained.

115.3.6.3 Adaptive THP REQ state diagram

The requests to the link partner to update the THP filter coefficients shall conform to the Adaptive THP REQ state diagram in Figure 115–29.

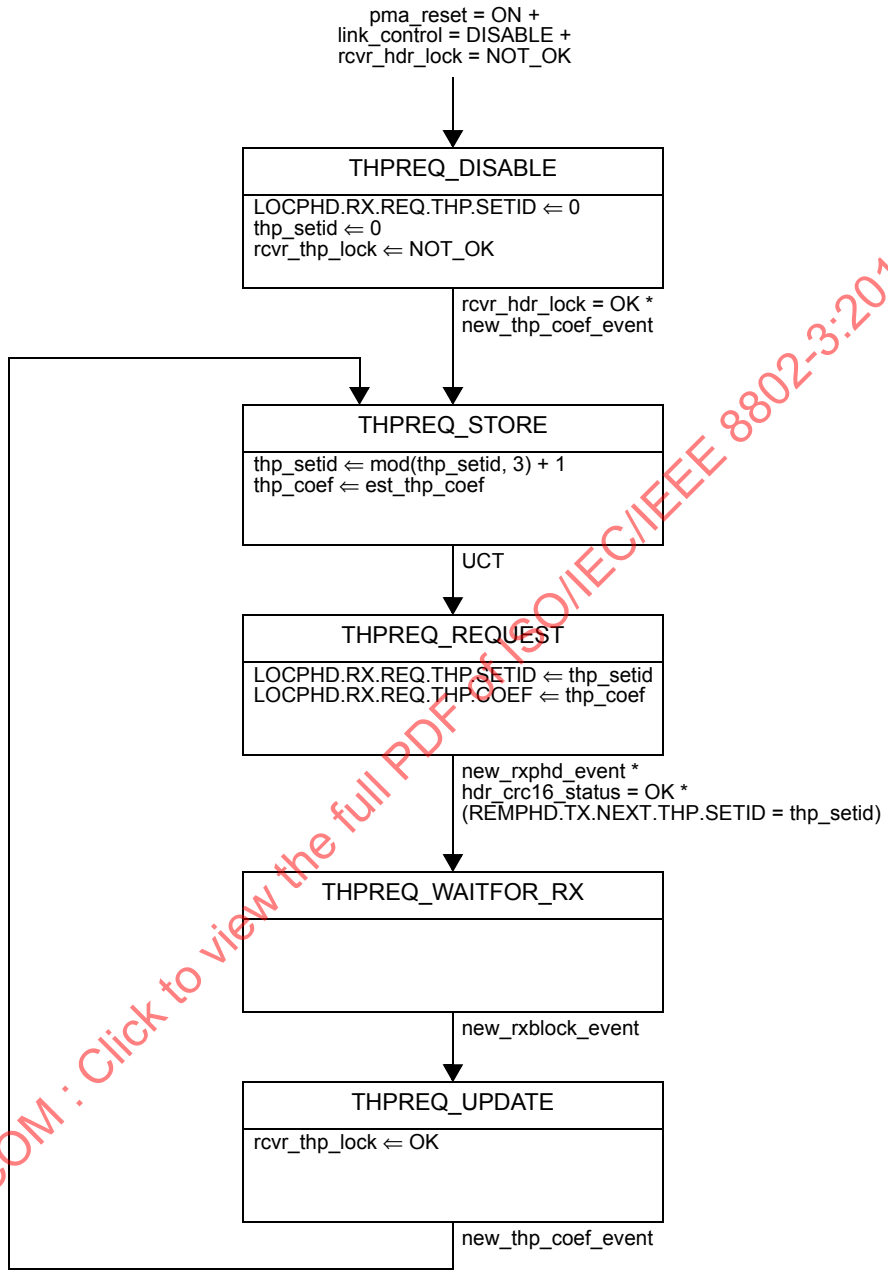

Figure 115–29—Adaptive THP REQ state diagram

Upon reset, disable of the PMA or unreliable PHD communication, the local PHY is not able to receive THP processed payload data sub-blocks (rcvr_thp_lock ⇐ NOT_OK). This is signaled to the remote PHY by assigning 0 to the field LOCPHD.RX.REQ.THP.SETID.

Once the transmission and reception of PHDs are reliable (rcvr_hdr_lock = OK) and the first set of THP coefficients are ready from the estimator (new_thp_coef_event) a transition to THPREQ_STORE occurs.

In this state, the newly estimated coefficients are stored (thp_coef ⇐ est_thp_coef) and assigned a set identifier. The set identifier is calculated based on the identifier previously requested as thp_setid ⇐ mod(thp_setid, 3) + 1, with modulo operator as defined in Equation (115–4).

The request for changing the set of THP coefficients is included in the next Transmit Block PHD (transition to THPREQ_REQUEST state). More precisely, the field LOCPHD.RX.REQ.THP.SETID indicates the associated set identifier, and the set of coefficients itself is transmitted by using the field LOCPHD.RX.REQ.THP.COEF[8:0].

In THPREQ_REQUEST, the local PHY receiver waits for the link partner to signal that the THP request has been accepted (the link partner starts using the requested coefficients for THP processing on its next Transmit Block). Once this event occurs (new_rxphd_event and hdr_crc16_status = OK and REMPHD.TX.NEXT.THP.SETID = thp_setid), a transition to THPREQ_WAITFOR_RX follows.

In THPREQ_WAITFOR_RX, the PHY receiver waits for the next Transmit Block received from the link partner. Once this event occurs, a transition to THPREQ_UPDATE is taken, where the value OK is assigned to the state variable rcvr_thp_lock, indicating that payload data sub-blocks are received with THP processing. In the THPREQ_UPDATE state the PMA receiver also adapts its circuitry to match the THP coefficients used at the remote transmitter.

Whenever a new set of THP coefficients from the estimator is available, it is stored and requested as explained previously. The local PHY receiver is not allowed to make a new THP request until the previous THP request has been acknowledged by the link partner, even if a new set of coefficients is available from the estimator.

115.3.7 PHY quality monitor

115.3.7.1 PHY quality criterion

Payload data reception is reliable when the BCH frame error ratio (BFER) is less than 8.8×10^{-11} after BCH decoding.

115.3.7.2 PHY quality assessment

The assessment of the previously defined PHY quality criterion may be based on estimation of the noise variance at the PAM16 decoder decision points $E[n_d^2]$, which expressed in base-2 logarithmic units has to be lower than a given threshold T_{LM} to enable reliable local reception of payload data. If the condition $\log_2(E[n_d^2]) < T_{LM}$ holds, the variable loc_rcvr_status is assigned the value OK. The noise variance at the PAM16 decoder can be estimated either by measuring the Modulation Error Ratio (MER) at the decision points or measuring the ratio of corrected bits per codeword carried out by the BCH decoder of MLCC level 1 (see 115.2.4.3). The value of the threshold and the information used to estimate the PAM16 decoder noise variance is implementation dependent.

As defined in 115.3.4, the local PHY reports the link margin to the link partner by using the field LOCPHD.RX.LINKMARGIN. The link margin (*LM*) is defined as the SNR margin relative to the SNR required for reception of coded PAM16 with a quality per the specification in 115.3.7.1. Link margin is formally defined per Equation (115–24).

$$LM = T_{LM} - \log_2(E[n_d^2]) \qquad (115\text{–}24)$$

In LPI mode of operation, the PHY can use the reception of pilot $S2_x$ sub-blocks contained in the refresh periods to estimate the link margin at the PAM16 decoder decision points.

115.3.7.3 PHY quality monitor state variables

The following defines all the variables used in the PHY quality monitor state diagram that have not been previously introduced:

new_link_margin_event
: Signal sent by the PHY receiver to indicate a new estimation of detector link margin is available. This event persists only long enough to cause one state diagram transition.

link_margin
: Variable set by the PHY receiver containing the value of the last link margin estimation.

  Values: Any value determined per Equation (115–24) with $E[n_d^2]$ and T_{LM} as defined in 115.3.7.2

115.3.7.4 PHY quality monitor state diagram

The variable loc_rcvr_status (see 115.3.5.1), which indicates if the local PHY is reliably receiving payload data per the specifications of 115.3.7.1 shall be determined as specified by the PHY quality monitor state diagram in Figure 115–30.

Upon reset, disable of the PMA or loss of PHD lock, the PHY quality monitor functionality is disabled (PMAMON_DISABLE state), and the state variable loc_rcvr_status is assigned the value NOT_OK. This is indicated to the link partner by assigning the value NOT_OK to the field LOCPHD.RX.LINKSTATUS. Additionally, the reported link margin is set to 0x80 (the smallest value representable in 8-bit signed format, see 115.3.8).

Once the local PHY begins to receive payload data sub-blocks that are properly THP processed (rcvr_thp_lock = OK), the state diagram waits for the first estimate of the link margin to be available (PMAMON_WAITING state). From then on, whenever a new estimate of the link margin is available (new_link_margin_event), it is evaluated. If link margin is larger than zero, the local reception of payload data sub-blocks is reliable.

Reliable local reception is indicated to the link partner by assigning OK to the field LOCPHD.RX.LINKSTATUS (state PMAMON_OK). After at least one locally transmitted Transmit Block, the local receiver status is signaled to the link monitor state diagram (loc_rcvr_status ⇐ OK) synchronously on the event of start of a new Transmit Block (state PMAMON_UPDATE).

Otherwise, when link margin is smaller than or equal to zero, unreliable receive link status is signaled (loc_rcvr_status ⇐ NOT_OK). This corresponds to the state PMAMON_FAIL. The local receiver status is always indicated to the link partner by using the field LOCPHD.RX.LINKSTATUS. The measured link margin is also reported via the field LOCPHD.RX.LINKMARGIN.

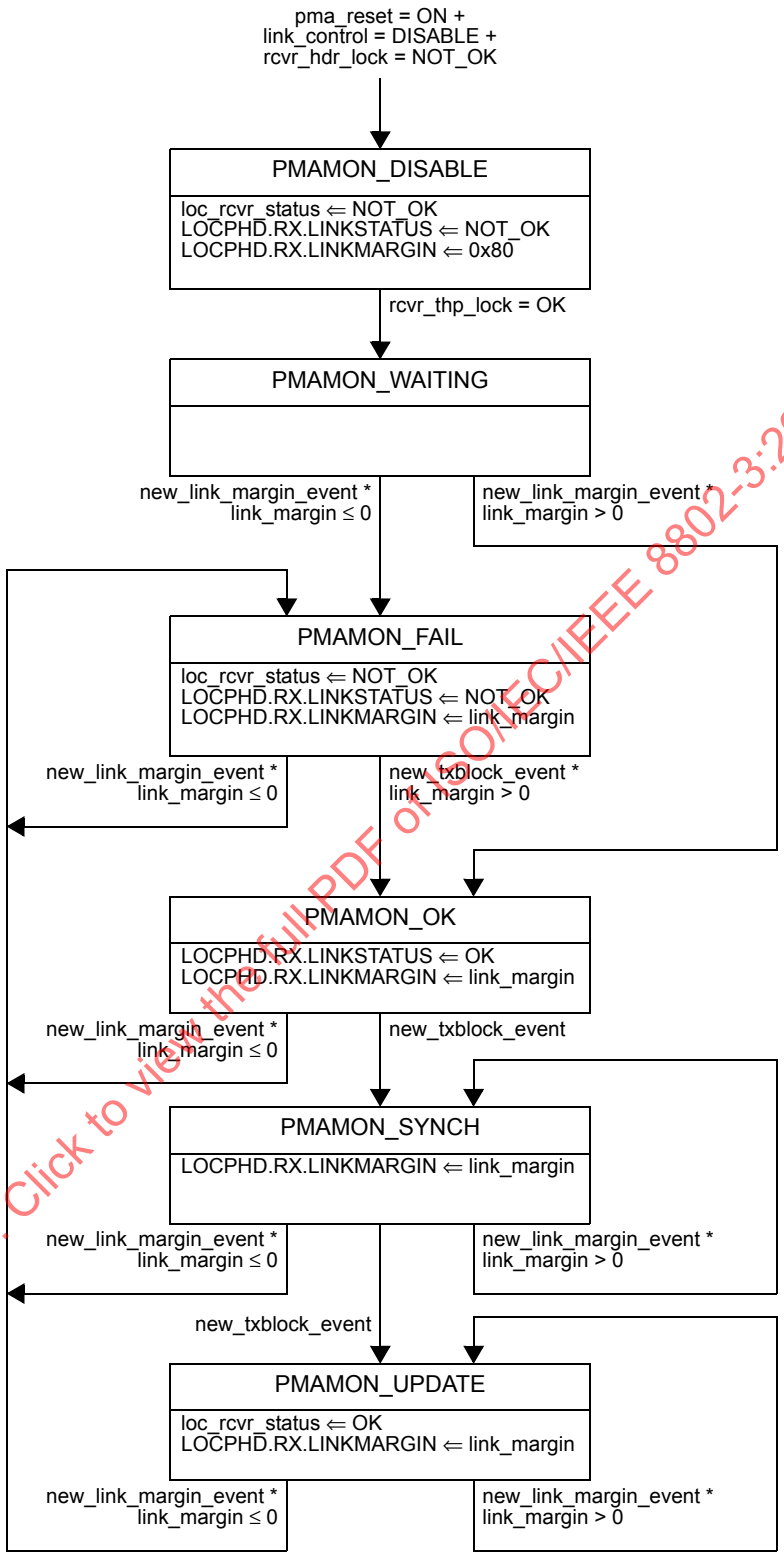

Figure 115–30—PHY quality monitor state diagram

115.3.8 Fixed-point format formal definition

The notation (m, n) is used to represent an m-bit binary word, which is to be interpreted as a signed twos complement fixed-point rational, where n is the number of bits used to represent the integer part (sign bit included) and (m – n) bits are used to represent the fractional part. Given an m-bit binary word, it is assumed that $1 \leq n \leq m$.

Any 1000BASE-H compliant PHY shall conform to the fixed-point encoding and the fixed-point decoding provided by the MATLAB (see 1.3) codes[6] in 115.3.8.1 and 115.3.8.2, respectively, for the fixed-point representation of Clause 45 registers and PHD fields (see 115.3.4).

115.3.8.1 Fixed-point encoding

```
% Parameters:
%       fdata: Row data vector in floating-point format
%       m    : Word length # of bits
%       n    : Integer part # of bits, including sign
%       rdata: Fixed-point format data vector

function rdata = float2fix(fdata, m, n)
  bdata = round(fdata*2^(m-n));
  bdata = min(bdata, 2^(m-1) - 1);
  bdata = max(bdata, -2^(m-1));
  idx_n = find(bdata < 0);
  rdata = bdata;
  rdata(idx_n) = 2^m + rdata(idx_n);
  rdata = bitand(rdata, 2^m - 1);
end
```

115.3.8.2 Fixed-point decoding

```
% Parameters:
%       rdata: Row data vector in fixed-point format
%       m    : Word length # of bits
%       n    : Integer part # of bits, including sign
%       fdata: Floating-point format data vector

function fdata = fix2float(rdata, m, n)
  % Sign extension
  bdata = bitand(rdata, 2^m - 1);
  idx_n = find(bitand(bdata, 2^(m-1)) ~= 0);
  bdata(idx_n) = bdata(idx_n) - 2^m;

  % Fix to float conversion
  fdata = bdata / (2^(m - n));
end
```

115.4 Energy-Efficient Ethernet (EEE)

Each PHY shall advertise its EEE ability to the link partner in the field PHD.CAP.LPI (see Table 115–6). PHD.CAP.LPI = 1 advertisement indicates to the link partner that the local PHY can generate Transmit Blocks as specified for the LPI mode of operation, it is able to accept Transmit Blocks from the link partner that conform to LPI operation (see 45.2.3.47d.15), and that EEE is enabled (see 45.2.3.47c.4).

EEE shall be operational only when both link partners indicate PHD.CAP.LPI = 1. If either link partner PHY does not advertise EEE ability (PHD.CAP.LPI = 0), then the link operates in normal mode in both transmit and receive directions even if “Assert LPI” encoding is detected on the GMII. When two link

[6]Copyright release for MATLAB codes: Users of this standard may freely copy or reproduce the MATLAB codes in this subclause so it can be used for its intended purpose.

partners do not agree on enabling EEE capability, the PCS encoding transparently carries the LPI signaling GMII to GMII, but the PHY does not enter LPI mode.

As shown in Figure 115–31, 1000BASE-H LPI mode consists of alternating refresh and quiet periods. Refresh is provided by transmitting all the pilot S1, pilot $S2_x$, and PHS_x sub-blocks; and quiet is provided by suspending transmission of the payload data sub-blocks. In quiet periods, the local PHY may turn off much of the PCS, PMA, and PMD transmitter. No optical power is injected into the fiber during these periods of quiet resulting in reduced power consumption. LPI mode is only entered or exited aligned to the beginning of a payload data sub-block.

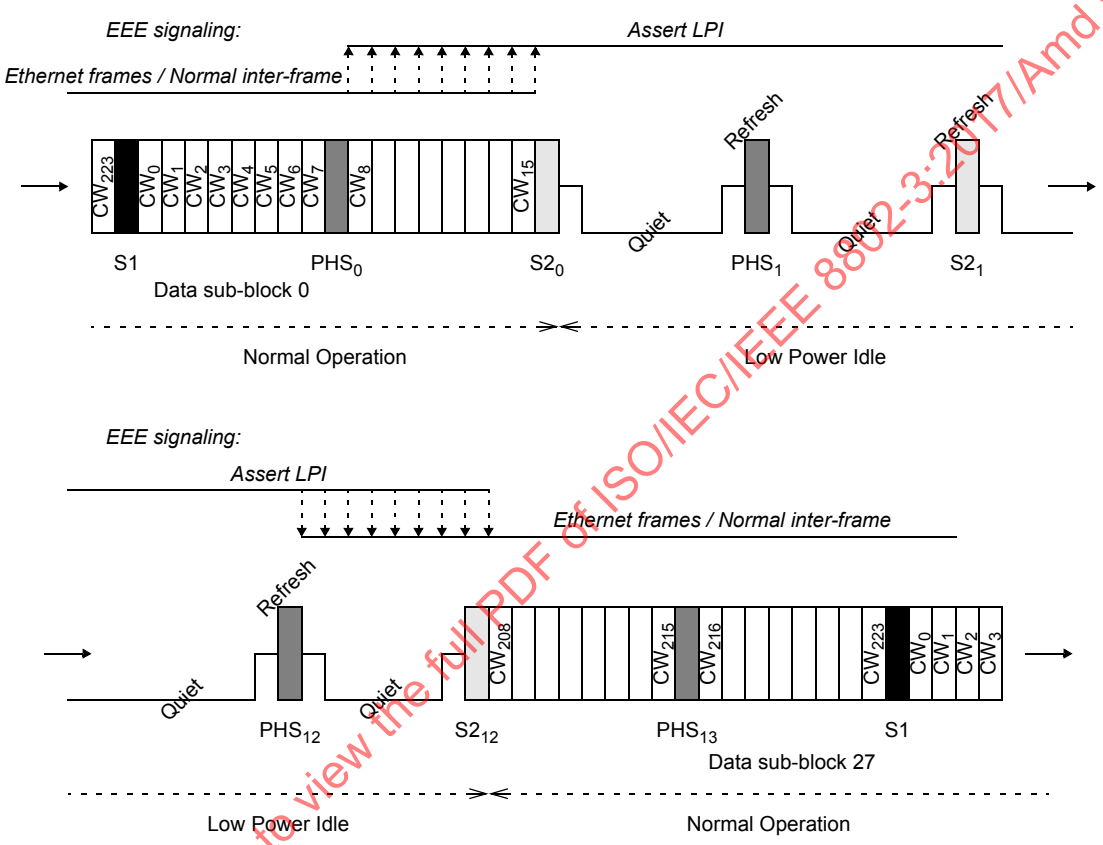

Figure 115–31— LPI operation

Pilot and PHS_x sub-blocks serve as refresh signals allowing the receiver to update adaptive filters and timing circuits in order to maintain link integrity. These sub-blocks are generated as in normal mode (see 115.2.1).

The PHY receiver detects if its link partner is operating in LPI mode based on the received signal at the beginning of each payload data sub-block. The PHY transmitter indicates to its link partner that it is entering a quiet period by the transmission of 130 contiguous zero value symbols. These follow the normal 16 zero postfix of the pilot or PHS_x sub-block. The extra zero symbols are used by the remote PHY receiver to detect that a quiet period follows, allowing the PMD receive function to save the state of circuitry and switch off the optical signal translation before the optical power is switched off at the transmitter. The transmitter then enters its quiet state until 130 symbol times before the end of the payload data sub-block, where the transmitter inserts 130 zero value symbols before the transmission of the pilot or PHS_x sub-block. This allows the link partner to prepare for reception of the sub-block that acts as a refresh signal.

115.4.1 LPI mode transmit operation

The transmit operation of a 1000BASE-H compliant PHY in LPI mode produces alternating quiet and refresh periods as shown in Figure 115–31. LPI operating mode shall only be entered once the link has been established (link_status = OK). When an "Assert LPI" transfer occurs on the GMII, the local PCS encodes the "Assert LPI" signal into a PDB as defined in Table 115–2.

The PHY transmitter shall enter LPI mode at the beginning of the next payload data sub-block, once a PDB that contains an encoded "Assert LPI" has been completely transmitted to its link partner, unless the GMII signals normal inter-frame before the end of the current payload data sub-block.

The PHY transmitter shall be enabled periodically to transmit pilot and PHS_x sub-blocks (refresh signals) at the same time as they would be transmitted in normal operating mode.

During LPI mode, the transmitter shall replace any payload data sub-block with the following:

a) Transmission of 130 zero symbols, to indicate entry to quiet (pcspma_tx = ON, see 115.4.3)
b) No output optical power during 7644 symbols (quiet, pcspma_tx = OFF)
c) Transmission of 130 zero symbols, to prepare the remote receiver for pilot and PHS_x sub-blocks used as refresh signals (pcspma_tx = ON)

The PHY transmitter shall exit LPI mode and resume normal operation at the start of the next payload data sub-block after the reception of normal inter-frame transfers on the GMII.

The 64B/65B encoder shall preserve timing during quiet mode. The time alignment of transmitted PDBs relative to FEC codewords when the PHY re-enters normal operation is the same as it would have been in the absence of LPI mode. This preserves the PCS decoder synchronization of the link partner and coherence with information encoded in the field PHD.TX.NEXT.PDB.OFFSET.

The payload data binary scrambler of 115.2.4.2, and the payload data symbol scrambler of 115.2.4.4 shall preserve timing during quiet mode. When the PHY re-enters normal operation, the scramblers values are the same as they would have been in the absence of LPI mode.

Unlike some other EEE PHYs, neither sleep nor wake specific signals are used to enter and leave the LPI mode of operation. Instead, sleep is indicated to the link partner by the transmission of 130 zero symbols that replace the beginning of a payload data sub-block. Wake is implicit in the presence of normal PAM16 Tomlinson-Harashima precoded signal at the beginning of a payload data sub-block.

115.4.2 LPI mode receive operation

The receive operation of a 1000BASE-H compliant PHY in LPI mode processes alternating quiet and refresh periods as shown in Figure 115–31.

The PHY receiver shall enter LPI mode upon detection of a sequence of zero symbols instead of PAM16-THP signal at the beginning of a payload data sub-block, consequently encoding "Assert LPI" in GMII transfers. Some receive functionality may be disabled to reduce power consumption.

NOTE—"Assert LPI" can also be encoded on the GMII receive stream due to the reception of PDBs containing LPI signaling from the link partner (this, for example, is the case of LPI assertion on the GMII transmit stream in the middle of a payload data sub-block transmission).

In LPI mode, the PHY receiver can use received pilot S1, pilot $S2_x$, and PHS_x sub-blocks, periodically sent by the link partner, to update adaptive coefficients and timing circuits and to determine the values of state variables loc_rcvr_status and link_margin.

The PHY receiver shall exit the LPI mode upon detection of PAM16-THP signal at the beginning of a payload data sub-block, returning to normal operation and sending the received payload to the GMII. The 64B/65B decoder shall resume normal operation after LPI mode, starting aligned to the boundary of the first complete PDB received from the beginning of the payload data sub-block. At this PDB, the local PHY begins to send normal inter-frame encoding on the GMII, since this is the initial information received from the remote PHY and the link returns the nominal operational mode.

115.4.3 PMD power control state variables

The following defines all the variables used in PMD power control state diagrams that have not been previously introduced:

lpi_cap
: Controls LPI functionality.
Values: TRUE: Both local and remote PHY have EEE ability and EEE functionality is enabled in both PHYs
FALSE: Either local or remote PHY do not have EEE ability or it is disabled

pcspma_tx
: State variable that indicates the symbols transmission from PMA.
Values: ON: Enable PCS and PMA transmit (during normal operation or LPI refresh periods)
OFF: Disable PCS and PMA transmit (LPI quiet periods)

pcspma_rx
: State variable that indicates the symbols reception by PMA.
Values: ON: Enable PCS and PMA receive (during normal operation or LPI refresh periods)
OFF: Disable PCS and PMA receive (LPI quiet periods)

rx_pwr
: Controls the PMD receive function.
Values: ON: The PMD receive function receives signal at MDI and transfer to the PMA receiver
OFF: The PMD receive function ignores signal at the MDI, saves the internal state of the circuitry, and may reduce power consumption

sd_inh
: Indicates to the PMD signal detect function to be, or not, inhibited.
Values: TRUE: The PMD signal detect function is inhibited
FALSE: The PMD signal detect function operates normally

tx_pwr
: Controls the PMD transmitter.
Values: ON: The PMD generates signal at the MDI
OFF: The PMD does not generate signal at the MDI, and may reduce power consumption

115.4.4 PMD power control state diagrams

Power control of PMD transmit function via tx_pwr shall conform to the PMD TX power control state diagram in Figure 115–32. Power control of PMD receive function via rx_pwr and sd_inh shall conform to the PMD RX power control state diagram in Figure 115–33.

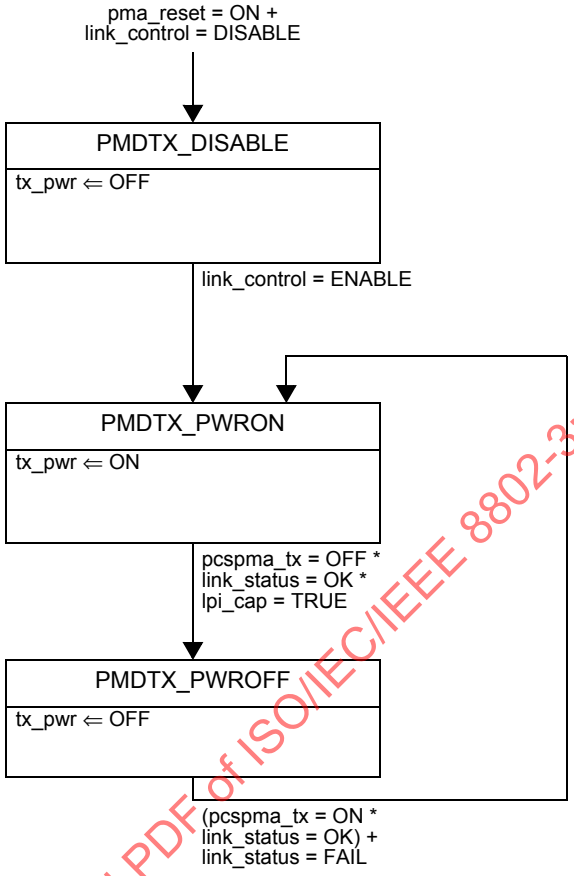

Figure 115–32—PMD TX power control state diagram

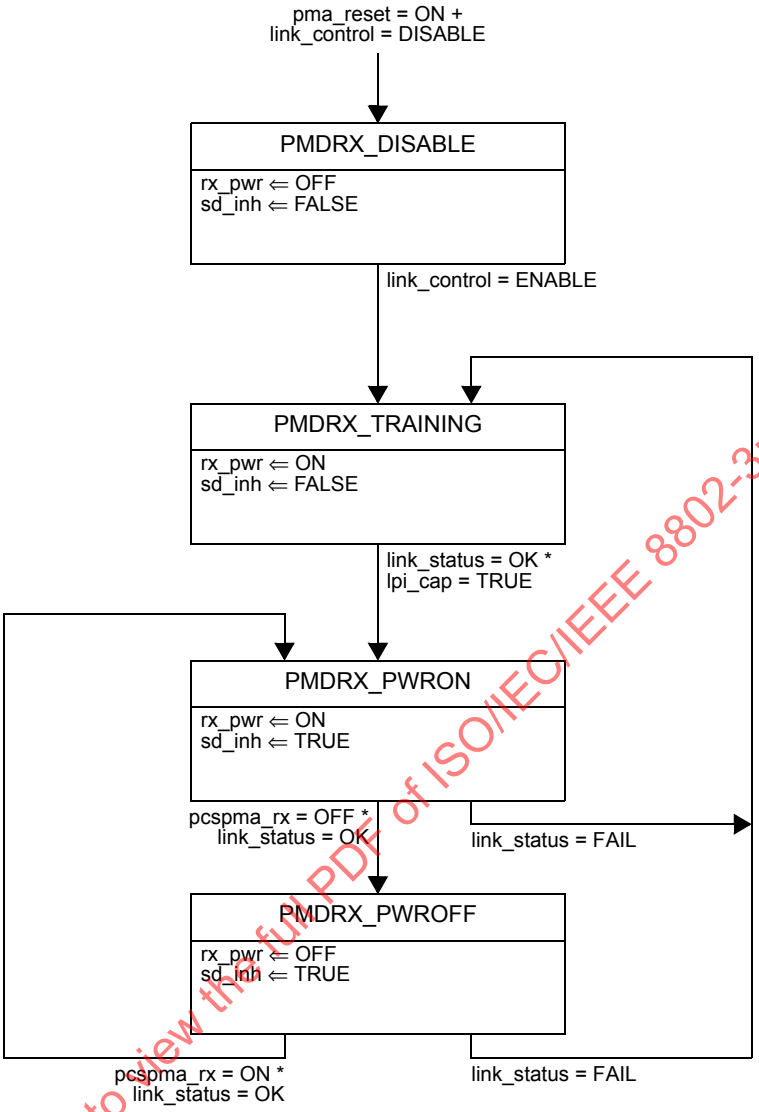

Figure 115–33—PMD RX power control state diagram

115.5 Test modes

The test mode 1 through test mode 6 shall be provided to allow PMD optical measurement requirements defined in 115.6.4 and BER testing.

These test modes shall be configured by setting the 1000BASE-H PCS control register, operation mode bits defined in 45.2.3.47c. The test modes only change the symbols provided to the transmitter circuitry and do not alter the optical and jitter characteristics at the MDI from those of normal (non-test mode) operation.

115.5.1 Test mode 1

Test mode 1 is for measurement of the bit error ratio (BER) of the link including the PCS, PMA, and PMD sublayers of two PHYs in the 1000BASE-H set and a fiber optic cable connected to them. This mode reuses the normal (non-test) mode with a zero data stream.

Operating in this test mode, the PHY shall configure the PCS transmitter to input an all zeros bit stream to the binary scrambler and ignore GMII. In the absence of errors, a zero data sequence is expected after the receiver binary descrambler. Any non-zero data bit received shall be counted as an error to be computed in the BER. The 64B/65B encoder is not used when the PCS transmitter is configured in test mode 1.

PMA and PMD functions shall operate as in normal mode (non-test) establishing the bidirectional link independent of the special configuration of the binary scrambler in PCS.

The PHY shall announce to the link partner the test mode 1 using the field PHD.TX.NEXT.MODE (see 115.3.4). The operating mode of the transmitter encoded in the field PHD.TX.NEXT.MODE is selected at PMA reset, and does not change value unless a PMA reset takes place. The receiver shall reconfigure its circuitry to support the signaled operating mode, for normal operation (the 64B/65B decoder is connected to the binary descrambler), or for BER test (a counter connected to the binary descrambler).

115.5.2 Test mode 2

When test mode 2 is enabled, the PMA shall transmit one {+1} symbol followed by one {–1} symbol continually with the transmitted symbols timed from its local symbol clock. The resulting transmitter output signal is a 162.5 MHz square wave.

115.5.3 Test mode 3

When test mode 3 is enabled, the PMA shall transmit 10 {+1} symbols followed by 10 {–1} symbols continually with the transmitted symbols timed from its local symbol clock. The transmitter output is a 16.25 MHz square wave.

115.5.4 Test mode 4

For test mode 4 definition, let $q1$ be the sub-sequence composed by 20 {+1} symbols followed by 10 {–1} symbols, and $q2$ the sub-sequence composed by 10 {+1} symbols followed by 20 {–1} symbols. When test mode 4 is enabled, the PMA shall transmit a sequence composed by 250 times the sub-sequence $q1$ followed by 250 times the sub-sequence $q2$ continually, being the transmitted symbols timed from its local symbol clock.

115.5.5 Test mode 5

When test mode 5 is enabled, the PMA shall continually transmit {0} symbols timed from its local symbol clock. The transmitter output is a dc signal.

115.5.6 Test mode 6

When test mode 6 is enabled, the PMA shall transmit the sequence of symbols s_n generated by the scrambler generator polynomials per Equation (115–25) and Equation (115–26).

$$g_0(x) = 1 + x^9 + x^{11} \quad (115–25)$$

$$g_1(x) = 1 + x^7 + x^9 + x^{10} + x^{11} \quad (115\text{–}26)$$

The two maximum-length shift registers used to generate the sequences defined by these polynomials shall be updated once per symbol interval (nominally 1000/325 ns). The reset value of both shift registers shall be 0x7FF, so the content of both registers start aligned to all ones when the PHY is configured to generate the test mode 6 pattern.

The bits stored in the shift register at a particular time n are denoted $Scr0_n[10:0]$ for the scrambler defined per Equation (115–25). At each symbol period this shift register is advanced by one bit and one new bit represented by $Scr0_n[0]$ is generated. Bits $Scr0_n[10]$ and $Scr0_n[8]$ are exclusive OR'd together to generate the next $Scr0_n[0]$ bit.

The bits stored in the shift register at a particular time n are denoted $Scr1_n[10:0]$ for the scrambler defined per Equation (115–26). At each symbol period this shift register is advanced by one bit and one new bit represented by $Scr1_n[0]$ is generated. Bits $Scr1_n[10]$, $Scr1_n[9]$, $Scr1_n[8]$, and $Scr1_n[6]$ are exclusive OR'd together to generate the next $Scr1_n[0]$ bit.

The bit sequences $x00_n$, $x01_n$, $x02_n$, and $x03_n$ generated from combinations of bits of the two scramblers shall be used to generate the PAM16 symbols, $y0_n$, according to Equation (115–27).

$$\begin{aligned} x00_n &= Scr1_n[0] \\ x01_n &= Scr1_n[1] \wedge Scr0_n[4] \\ x02_n &= Scr1_n[2] \wedge Scr0_n[9] \\ x03_n &= Scr1_n[0] \wedge Scr0_n[10] \\ y0_n &= x00_n + 2 \times x01_n + 4 \times x02_n + 8 \times x03_n \end{aligned} \quad (115\text{–}27)$$

The bit sequences $x10_n$, $x11_n$, $x12_n$, and $x13_n$ generated from combinations of bits of the two scramblers shall be used to generate the PAM16 symbols, $y1_n$, according to Equation (115–28).

$$\begin{aligned} x10_n &= Scr0_n[0] \\ x11_n &= Scr0_n[1] \wedge Scr1_n[4] \\ x12_n &= Scr0_n[2] \wedge Scr1_n[9] \\ x13_n &= Scr0_n[0] \wedge Scr1_n[10] \\ y1_n &= x10_n + 2 \times x11_n + 4 \times x12_n + 8 \times x13_n \end{aligned} \quad (115\text{–}28)$$

From $y0_n$ and $y1_n$, the PAM256 symbols s_n shall be generated according to Equation (115–29). The transmitter shall time the transmit symbols s_n from its local symbol clock.

$$s_n = \frac{1}{256}(2 \times (16 \times y0_n + y1_n) - 255) \quad (115\text{–}29)$$

115.6 Physical Medium Dependent (PMD) sublayer

115.6.1 PMD service interface

The following specifies the services provided by a PMD connected to 1000BASE-H. The PMD sublayer service interface is described in an abstract manner and does not imply any particular implementation.

The PMD service interface supports the exchange of analog signals between PMA and PMD sublayers. The PMD translates the transmit and receive PMA signals to and from optical signals suitable for the specified medium.

The following primitives are defined:

PMD_COMSIGNAL.request
PMD_COMSIGNAL.indication
PMD_TXPWR.request
PMD_RXPWR.request
PMD_RXDETECT.indication
PMD_SDINH.request

115.6.1.1 PMD_COMSIGNAL.request

This primitive defines the transfer of an analog signal amplitude from the PMA to the PMD.

115.6.1.1.1 Semantics of the primitive

PMD_COMSIGNAL.request(tx_signal)

During transmission, this primitive conveys to the PMD via the parameter tx_signal, the amplitude of the output signal to be produced by the PMD transmit function.

115.6.1.1.2 When generated

The PMA generates PMD_COMSIGNAL.request(tx_signal) synchronously with every transmit clock cycle.

115.6.1.1.3 Effect of receipt

Upon receipt of this primitive the PMD converts tx_signal into the MDI optical signal (see 115.6.2.2).

115.6.1.2 PMD_COMSIGNAL.indication

This primitive defines the transfer of an analog signal amplitude from the PMD to the PMA.

115.6.1.2.1 Semantics of the primitive

PMD_COMSIGNAL.indication(rx_signal)

This primitive conveys to the PMA via the parameter rx_signal the relative amplitude of the optical signal received by the PMD at the MDI (see 115.6.2.3).

115.6.1.2.2 When generated

The PMD_COMSIGNAL.indication(rx_signal) is continuously generated by the PMD in the form of an analog signal.

115.6.1.2.3 Effect of receipt

Upon receipt of this primitive the PMA performs clock recovery for correct time sampling of received symbols and adaptive channel equalization (see 115.3.2).

115.6.1.3 PMD_TXPWR.request

This primitive is used for optional EEE capability. The primitive is generated to request no optical output power during quiet periods of LPI mode, or to request optical signal being generated at the MDI during refresh periods of LPI mode or for normal operation of the PHY transmitter.

115.6.1.3.1 Semantics of the primitive

PMD_TXPWR.request(tx_pwr)

The tx_pwr parameter can take one of the two values: ON or OFF.

ON: The PMD transmit function generates signals at the MDI.

OFF: The PMD transmit function does not generate signal at the MDI.

115.6.1.3.2 When generated

The PMD_TXPWR.request(tx_pwr) is generated by the PMA transmitter whenever the value of tx_pwr changes as specified by the state diagram of Figure 115–32 (see 115.4.4).

115.6.1.3.3 Effect of receipt

PMD_TXPWR.request(OFF) requests the PMD transmit function to produce no optical output power, and PMD_COMSIGNAL.request(tx_signal) is ignored.

PMD_TXPWR.request(ON) requests the PMD transmit function to respond to PMD_COMSIGNAL.request(tx_signal) with generation of normal optical output.

115.6.1.4 PMD_RXPWR.request

This primitive is used for optional EEE capability. It is generated to request the PMD receive function to transition between being able to respond to received optical signals and a minimum power consumption state.

115.6.1.4.1 Semantics of the primitive

PMD_RXPWR.request(rx_pwr)

The rx_pwr parameter can take one of two values: ON or OFF.

ON: The PMD receive function responds to the received MDI optical signal.

OFF: The PMD receive function ignores the received MDI optical signal.

115.6.1.4.2 When generated

The PMD_RXPWR.request(rx_pwr) is generated by the PMA receiver whenever the value of rx_pwr changes as specified by the state diagram of Figure 115–33 (see 115.4.4).

115.6.1.4.3 Effect of receipt

PMD_RXPWR.request(OFF) requests the PMD receive function to ignore the received MDI signal and reduce power consumption.

PMD_RXPWR.request(ON) requests the PMD receive function to respond to the received MDI signal.

115.6.1.5 PMD_RXDETECT.indication

This primitive is generated by the PMD signal detect function to indicate the status of the receive optical signal from the MDI as specified in 115.6.2.4.

115.6.1.5.1 Semantics of the primitive

PMD_RXDETECT.indication(signal_detect)

The signal_detect parameter can take one of two values: OK or FAIL, indicating whether the PMD is detecting average optical power over a threshold (see 115.6.2.4) at the receiver (OK) or not (FAIL). When signal_detect = FAIL, then the rx_signal is undefined.

NOTE—signal_detect = OK does not guarantee that rx_signal provides high enough quality to allow the PHY to establish the link. It just indicates that average optical power present at the MDI exceeds a threshold. A signal_detect = OK indication with sufficient average optical power allows the PHY partners to start establishing the link and still not meet the BFER objective (see 115.3.7.1), then the PHY indicates link_status = FAIL.

115.6.1.5.2 When generated

The PMD signal detect function generates this primitive to indicate a change in the value of signal_detect.

115.6.1.5.3 Effect of receipt

PMD_RXDETECT.indication(OK) indicates that the PMD receive function is able to respond to PMD_RXPWR.request primitives (that request the PMD receive function to respond or not to the MDI signal). PMD_RXDETECT.indication(OK) also indicates to the PMA receive function that optical signal is being received from the MDI and that the link may be established with a link partner. PMD_RXDETECT.indication(OK) may be used to wake up from deep sleep in a system that includes a 1000BASE-RHx PHY.

PMD_RXDETECT.indication(FAIL) indicates the PMD receive function is not responding to the received MDI signal. PMD_RXDETECT.indication(FAIL) also indicates to the PMA receive function that optical signal is not being received so link establishment cannot be initiated. PMD_RXDETECT.indication(FAIL) may be used to transition a system that includes a 1000BASE-RHx PHY into deep sleep.

115.6.1.6 PMD_SDINH.request

This primitive supports EEE operation and is generated to request enable or inhibit of the PMD signal detect function.

115.6.1.6.1 Semantics of the primitive

PMD_SDINH.request(sd_inh)

The sd_inh parameter can take one of the two values: TRUE or FALSE.

TRUE: The PMD signal detect function is inhibited.

FALSE: The PMD signal detect function responds to the received MDI optical signal.

115.6.1.6.2 When generated

The PMD_SDINH.request(sd_inh) is generated by the PMA receiver whenever the value of sd_inh changes as specified by the state diagram of Figure 115–33 (see 115.4.4).

115.6.1.6.3 Effect of receipt

PMD_SDINH.request(FALSE) requests normal PMD signal detect operation.

PMD_SDINH.request(TRUE) requests the PMD signal detect function to inhibit processing of the received optical signal. This keeps PMD_RXDETECT.indication(signal_detect) = OK, independently of optical signal level received at MDI.

115.6.2 PMD functional specifications

115.6.2.1 PMD block diagram

For purpose of system conformance, the PMD sublayer is defined at the following points, depicted in Figure 115–34. The optical transmit signal is defined at the output end of 1 meter of plastic optical fiber consistent with the link segment type connected to the MDI. All the specified transmitter measurements are made at TP2. The optical receive signals are specified and measured at the output of the fiber optic cabling (TP3), which in a link segment is connected to the receiver.

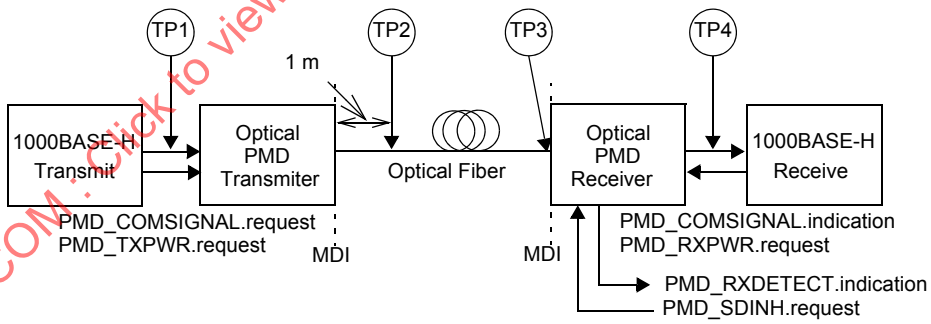

Figure 115–34—1000BASE-RHx PHY block diagram

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The specifications of the PMD service interface (TP1 and TP4) are not system compliance points of this standard (these are not readily testable in a system implementation).

115.6.2.2 PMD transmit function

The PMD transmit function translates abstract PMD service primitives into optical signals. The transmit signal characteristics at the MDI are specified in 115.6.3.1.

The PMD transmit function shall translate the amplitude parameter tx_signal (see 115.6.1.1) into optical signal p at TP2 according to the following function:

$$p = \frac{P_1 - P_0}{2} \times \text{tx\_signal} + \frac{P_1 + P_0}{2} \quad (115\text{–}30)$$

where P_0 and P_1 are respectively the minimum and maximum optical power at TP2, and the parameter tx_signal fits $-1 \leq \text{tx\_signal} < +1$ (see 115.3.3.1).

According to Equation (115–30), the maximum amplitude of tx_signal is translated into the highest optical power (P_1) at TP2 and the minimum amplitude of tx_signal is translated into the lowest optical power (P_0) at TP2.

Optionally, the PMD transmit function shall turn on and turn off the optical output as required by the PMD_TXPWR.request primitive. The transition times from receipt of this primitive until it takes effect at the MDI are specified in 115.6.3.1.

115.6.2.3 PMD receive function

The PMD receive function shall translate the optical signal received at the MDI into the analog signal amplitude provided by the abstract PMD_COMSIGNAL.indication(rx_signal) primitive. The receive signal at the MDI is specified in 115.6.3.3.

Optionally, the PMD receive function responds to or ignores the receive MDI signal during optional LPI mode, as requested by the PMD_RXPWR.request primitive.

PMD_RXPWR.request(OFF) shall cause the PMD receive function to save the internal state of the circuitry to not be affected by the received optical signal during quiet periods of LPI mode. The PMD receive function ignores the received MDI signal and may reduce its power consumption. The PMD receive function saves state to be able to quickly restart translation of received MDI signal during the LPI mode refresh periods or when normal operation is resumed.

The PMD receive function shall respond to the MDI optical signal in response to receiving a PMD_RXPWR.request(ON). This allows the PMD to process the refresh signals in LPI mode and when normal operation of the PHY is resumed. The transition times from receipt of a PMD_RXPWR.request primitive until it takes effect in the PMD receive function are specified in 115.6.3.3.

115.6.2.4 PMD signal detect function

The PMD signal detect function determines the value of the signal_detect parameter of the PMD_RXDETECT.indication primitive, which is signaled when the value of signal_detect changes.

The value of the signal_detect parameter shall be generated in response to the average optical power present at the MDI and the sd_inh parameter according to the conditions defined in Table 115–7. The PMD receive function is not required to verify whether a compliant 1000BASE-H signal is being received. This standard imposes no response time requirements on the generation of the signal_detect parameter.

Table 115–7—Signal detect value definitions

sd_inh	Receive conditions	Signal detect value
FALSE	AOP at TP3 < –35 dBm	FAIL
FALSE	AOP at TP3 > –29 dBm	OK
FALSE	–35 dBm < AOP at TP3 < –29 dBm	Unspecified (uncertainty range)
TRUE	Any value of AOP at TP3	OK

115.6.3 PMD to MDI optical specifications

Different PMD to MDI optical specifications are provided for the three port types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC.

1000BASE-RHA and 1000BASE-RHB PHYs have to be able to operate in a fiber optic channel type I. A 1000BASE-RHC PHY has to be able to operate in the fiber optic channel type II and type III. Fiber optic channel type I, type II, and type III are defined in 115.7.

115.6.3.1 Transmitter optical specifications

A 1000BASE-RHx transmitter shall meet the specifications at TP2 defined in Table 115–8 and the modal power distribution (MPD) shall be higher than the lower bound limits defined in Table 115–9 per measurement techniques defined in 115.6.4. Specification for transmit MPD is illustrated in Figure 115–35 and the measurement method is provided in 115.6.4.11.

Table 115–8—Transmit optical characteristics (RHA, RHB, and RHC)

Parameter	Symbol	Units	Value/Criteria					
			Min			Max		
			RHA	RHB	RHC	RHA	RHB	RHC
Average optical power	AOP	dBm	–6	–7	–9	1		
Average optical power of OFF transmitter	AOP_{OFF}	dBm	—			–35		
Optical return loss tolerance	ORLT	dB	—			14		
Extinction ratio	ER	dB	11			15		
Center wavelength	λ_c	nm	635			665		
Spectral width	λ_w	nm	—			20		
Rise time (10% – 90%)	t_r	ns	—			3		
Fall time (90% – 10%)	t_f	ns	—			3		
Rising-edge overshoot	OS_{rise}	%	0			20		
Falling-edge overshoot	OS_{fall}	%	0			$\frac{100}{10^{ER/10}-1}$ [a]		
Positive output droop	DO^+	dB	0			0.8		

Table 115–8—Transmit optical characteristics (RHA, RHB, and RHC) *(continued)*

Parameter	Symbol	Units	Value/Criteria					
			Min			Max		
			RHA	RHB	RHC	RHA	RHB	RHC
Negative output droop	DO^{-}	dB	–0.7			0		
Timing jitter	t_J	ps	—			10		
2nd order harmonic distortion	HD_2	dB	—			–20		
3rd order harmonic distortion	HD_3	dB	—			–23		
4th order harmonic distortion	HD_4	dB	—			–34		
Residual distortion	RD	dB	—			–40		
Relative intensity noise	RIN	dB/Hz	—			–134		
Off transition time (from tx_pwr = OFF to AOP_{OFF})	t_{off}	ns	—			100		
On transition time (from tx_pwr = ON to active operation)	t_{on}	ns				1500		

[a]Maximum permitted falling-edge overshoot depends on the actual transmit ER. The equation gives the maximum permitted falling-edge overshoot as a function of the actual ER (dB).

Table 115–9—Transmit MPD lower bound limits per EAF (RHA, RHB, and RHC)

Angle (°)	EAF	Angle (°)	EAF	Angle (°)	EAF
0.0	0.00	10.0	0.41	27.5	0.97
1.0	0.00	15.0	0.70	30.0	0.99
2.5	0.03	20.0	0.83	35.0	1.00
5.0	0.11	22.5	0.89		
7.5	0.24	25.0	0.93		

Average optical power depends on the operation mode of the PHY transmitter (normal or LPI). AOP is defined as the average optical power at TP2 when the PMD transmit function receives primitive PMD_TXPWR.request(ON) (normal operation and LPI refresh signals). AOP_{OFF} corresponds to the optical power when the PMD transmit function receives the primitive PMD_TXPWR.request(OFF) (LPI quiet periods or link_control = DISABLE). The AOP_{OFF} maximum value is compatible with the PMD signal detect function specified in 115.6.2.4.

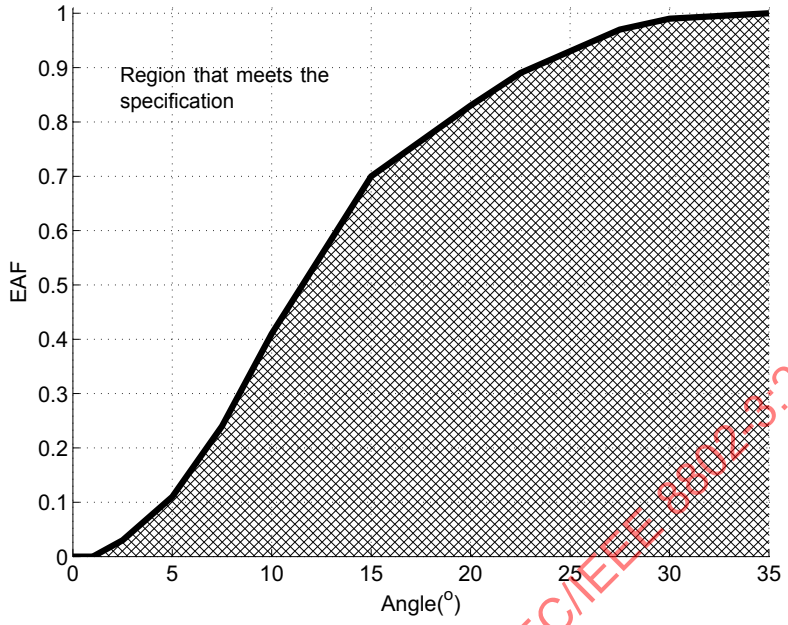

Figure 115–35—Illustration of the transmit MPD lower bound limits per EAF of Table 115–9

115.6.3.2 Transmit clock frequency

The symbol transmission rate of the PHY shall be 325.00 MBd ± 0.01%.

115.6.3.3 Receiver optical specifications

A 1000BASE-RHx receiver shall meet the specifications at TP3 defined in Table 115–10 per measurement techniques defined in 115.6.4. Each 1000BASE-RHx PHY is specified for one or two of three specified fiber optic channels (type I, type II, or type III).

A 1000BASE-RHx PHY shall be able to establish a reliable link per the specification in 115.3.7.1 throughout the average optical power (AOP) range between the minimum and maximum limit defined in Table 115–10, for signals received at the MDI that were transmitted from a remote transmitter within the specifications of 115.6.3.1, and have passed through a fiber optic channel specified in 115.7. Under these conditions, a 1000BASE-RHx PHY shall provide a BER less than 10^{-12} operating in test mode 1 (see 115.5.1), and a frame error ratio less than 1.1×10^{-10} for continuous transmission of 64-octet Ethernet frames transmitted with minimum IPG at GMII interface operating in normal (non-test) mode. These specifications apply to a complete 1000BASE-RHx link composed by two interconnected partners with their respective PCS, PMA, and PMD sublayers.

Table 115–10—Receive optical characteristics (RHA, RHB, and RHC)

Parameter	Symbol	Units	Value/Criteria							
			Min				Max			
			RHA	RHB	RHC		RHA	RHB	RHC	
			Fiber optic channel							
			Type I	Type I	Type II	Type III	Type I	Type I	Type II	Type III
Average optical power for reliable link establishment	AOP[a]	dBm	–17	–17	–17	–18.5	1			
Receiver reflectance	RR[b]	dB	—				–14			
Wavelength range	λ	nm	600				700			
Off transition time (from rx_pwr = OFF to quiet mode)	t_{off}	ns	—				200			
On transition time (from rx_pwr = ON to active operation)	t_{on}	ns	—				400			

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal that has a power level equal to the average receive optical power (max) plus at least 1 dB.
[b] See 1.4 for definition of reflectance.

115.6.3.4 Receiver boundary condition tests

The following boundary condition tests verify the receiver optical specifications defined in 115.6.3.3. A 1000BASE-RHx PHY shall be able to establish a reliable link as specified in 115.6.3.3 under boundary conditions defined in 115.6.3.4.1 and 115.6.3.4.2.

115.6.3.4.1 Receiver minimum AOP test

This test operates the 1000BASE-RHx PHY receiver in minimum AOP conditions as defined in Table 115–11. For this test, the responses of channel type I, type II, and type III are defined by the lower bound limits specified in Table 115–13, Table 115–14, and Table 115–15, respectively. Parameters of Table 115–8 and Table 115–10 that are not specified in Table 115–11 can take any value in the specification ranges.

115.6.3.4.2 Receiver maximum AOP test

This test operates a 1000BASE-RHx PHY receiver in maximum AOP conditions as defined in Table 115–12. The local receiver under test is connected to the remote transmitter by means of a plastic optical fiber of 1 meter or less consistent with the specifications of 115.7. Parameters of Table 115–8 and Table 115–10 that are not specified in Table 115–12 can take any value in the specification ranges.

Table 115–11—Parameters for receiver minimum AOP test

Parameter		Symbol	Units	Value/Criteria			
				RHA	RHB	RHC	
				Fiber optic channel			
				Type I	Type I	Type II	Type III
Transmitter	Extinction ratio	ER	dB	11			
	Fall time (90% – 10%)	t_f	ns	3			
	Rising-edge overshoot	OS_{rise}	%	0			
	Falling-edge overshoot	OS_{fall}	%	0			
Receiver	Receive average optical power	AOP	dBm	–17	–17	–17	–18.5

Table 115–12—Parameters for receiver maximum AOP test

Parameter		Symbol	Units	Value/Criteria		
				RHA	RHB	RHC
Transmitter	Extinction ratio	ER	dB	15		
Receiver	Receive average optical power	AOP	dBm	1		
	Receiver reflectance	RR[a]	dB	–14		

[a]See 1.4 for definition of reflectance.

115.6.4 Optical measurement requirements

All the optical measurements of the transmitter shall be made at TP2 (at the end of a 1m length of POF cable consistent with the link segment type). The optical measurements for the receiver shall be made at TP3.

The transmitter testing methodology assumes that a 1000BASE-RHx PMD is not tested standalone, but is always considered as part of a complete Physical Layer (i.e., PCS and PMA sublayers are also included). TP1 is not used as a stimulus point; rather, the complete PHY is instructed through management to generate signals that are measured at TP2.

115.6.4.1 Center wavelength measurement

The center wavelength shall meet the specifications according to IEC 61280-1-3, under normal (non-test) mode conditions using a valid 1000BASE-H transmit signal as specified in 115.3.3.1. For this measurement, the PHY is not connected to any link partner, therefore the bidirectional link cannot be established, MLCC codewords are not THP processed, and LPI mode is disabled.

115.6.4.2 Spectral width measurement

The spectral width (RMS) shall meet the specifications according to IEC 61280-1-3, using the same test conditions as for center wavelength measurement (see 115.6.4.1).

115.6.4.3 Average Optical Power (AOP) measurement

The AOP shall meet the specifications at TP2 and TP3 measured with a large area photo-detector able to couple all the output optical power from the optical fiber, using the same test conditions as 115.6.4.1.

115.6.4.4 Transmitter rise and fall time measurements

The transmitter rise and fall time measurements shall meet the specifications according to the following measurements procedure, using an electrical oscilloscope after optical to electrical conversion or an optical oscilloscope with a minimum bandwidth of 812.5 MHz (–3 dB cut-off frequency):

a) The PHY is configured in test mode 3 (see 115.5.3).
b) Rise time is measured as the time taken for the optical signal to transition from value $(0.1 \times P_1 + 0.9 \times P_0)$ to value $(0.1 \times P_0 + 0.9 \times P_1)$ and stay above the second value.
c) Fall time is measured as the time taken for the optical signal to transition from value $(0.1 \times P_0 + 0.9 \times P_1)$ to value $(0.1 \times P_1 + 0.9 \times P_0)$ and stay below the second value.

P_1 is the steady-state value that the optical signal reaches after a rising-edge transition and before the next falling-edge. P_1 (mW) is the average optical power measured over a 2 ns window centered 15 ns after the rising-edge crossing of the optical signal with the average optical power (AOP) level. Similarly, P_0 is the steady-state value that the optical signal reaches after a falling-edge transition and before the next rising-edge. P_0 (mW) is the average optical power measured in a 2 ns window centered 15 ns after the falling-edge AOP crossing.

115.6.4.5 Transmitter extinction ratio (*ER*) measurement

The transmitter extinction ratio (*ER*) shall meet the specifications per Equation (115–31) calculated from the optical power measurements P_1 and P_0, which are defined and measured as specified in 115.6.4.4, using the same test setup, apparatus requirements, and PHY operation mode as 115.6.4.4.

$$ER = 10 \times \log_{10}\left(\frac{P_1}{P_0}\right) \text{ (dB)} \tag{115–31}$$

115.6.4.6 Transmitter overshoot measurements

The transmitter overshoot shall meet the specifications according to Equation (115–32) and Equation (115–33) for rising edge overshoot and falling edge overshoot, respectively, using the same test setup, apparatus requirements, and PHY operation mode as 115.6.4.4.

$$OS_{\text{rise}} = \frac{P_{\max} - P_1}{P_1 - P_0} \tag{115–32}$$

$$OS_{\text{fall}} = \frac{P_0 - P_{\min}}{P_1 - P_0} \tag{115–33}$$

$P_{\max}$ (mW) is the maximum measured value of the optical signal in the time interval between a rising-edge AOP crossing and next falling-edge AOP crossing. Similarly, $P_{\min}$ (mW) is the minimum measured value in the time interval between consecutive falling and rising edges. P_0 and P_1 are defined and measured as specified in 115.6.4.4.

115.6.4.7 Transmitter output droop measurements

The transmitter output droop shall meet the specifications according to the following measurements steps, using the same test setup and apparatus requirements as 115.6.4.4:

a) A reference of extinction ratio, ER_0, is measured as specified in 115.6.4.5.
b) The PHY is configured in test mode 4 (see 115.5.4).
c) The maximum extinction ratio (ER_{max}) and the minimum extinction ratio (ER_{min}) are measured during a period of time of at least 47 µs (which assures sampling over more than a complete test mode 4 pattern). ER_{max} is calculated from the measured P_1 and P_0 values where the ratio between them is maximum. Similarly, ER_{min} is calculated from the measured P_1 and P_0 values, where the ratio between them is minimum. P_0 and P_1 are defined and measured as specified in 115.6.4.4.
d) The positive output droop DO^+ and the negative output droop DO^- are calculated as $DO^+ = ER_{max} - ER_0$ and $DO^- = ER_{min} - ER_0$, respectively.

115.6.4.8 Transmitter distortion measurement

The transmitter distortion is determined by four parameters:

a) Second order harmonic distortion (HD_2).
b) Third order harmonic distortion (HD_3).
c) Fourth order harmonic distortion (HD_4).
d) Residual distortion (RD).

These four parameters HD_2, HD_3, HD_4, and RD, shall meet the specifications according to the following procedure:

1) The PHY is configured in test mode 6 (see 115.5.6).
2) Transmitted waveform is captured at TP2 using the same test setup and apparatus requirements as 115.6.4.4 with data acquisition capabilities. To reduce frequency deviation between the transmitter and the clock used to sample the transmit waveform, the test instrument and the device under test may share the same clock reference.
3) A block of consecutive samples is processed with the MATLAB (see 1.3) code[7] given below or an equivalent. The captured block of signal is at least 13 µs long and is sampled with the minimum sampling rate of 3.25 Gsamples/s (10 times the transmit symbol rate of nominal 325 MBd). The code assumes the data acquisition clock is frequency locked to the DUT transmit clock.

```
% Post processing MATLAB code for 1000BASE-RH transmitter distortion

% Read captured data file, min 13 us long, min 3.25GSample/sec,
% high resolution capture
fid = fopen('RawData.bin', 'r');
xcap = fread(fid, inf, 'double');
fclose(fid);
xcap = reshape(xcap, 1, []);

% Set the over sampling ratio (min 10)
osr = 10;
[HD2 HD3 HD4 RD] = txdist(xcap,osr);

% Results
fprintf('HD2: %.2f dB\n', HD2);
fprintf('HD3: %.2f dB\n', HD3);
```

[7]Copyright release for MATLAB code: Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

```
fprintf('HD4: %.2f dB\n', HD4);
fprintf('RD:  %.2f dB\n', RD);


% TX distortion measurement
function [HD2 HD3 HD4 RD] = txdist(xcap, ov)
  % Compensate baseline
  xcap = xcap - mean(xcap);

  % Low-pass filter at 162.5 MHz
  [hb, ha] = butter(2, 1/ov, 'low');
  xcap = filter(hb, ha, xcap);

  % Reference test mode 6 signal
  tm6 = tm6gen();

  % Synchronization
  tm6_ov  = reshape(repmat(tm6, ov, 1), 1, []);
  xc      = filter(tm6_ov(end:-1:1), 1, [xcap zeros(1, length(tm6_ov))]);
  [mv mi] = max(abs(xc));
  dly     = mi - length(tm6_ov);
  xcap    = xcap(1+dly:end);
  xcap    = xcap(1:length(tm6_ov));

  % Decimation and clock phase recovery
  alpha = 0.7;

  min_ted = Inf;
  for i = 0:ov-1,
    xcap_dec = xcap(1+i:ov:end);
    len0     = min([length(xcap_dec) length(tm6)]);
    ted      = mean((1 - alpha)*xcap_dec(2:len0).*tm6(1:len0-1) - ...
                    alpha*xcap_dec(1:len0-1).*tm6(2:len0));

    if abs(ted) < min_ted
      min_ted = abs(ted);
      dly     = i;
    end
  end
  xcap_dec = xcap(1+dly:ov:end);

  % Normalize
  xcap_dec = xcap_dec/max(abs(xcap_dec));

  % Volterra estimation & analysis
  [HD2 HD3 HD4 RD] = volest(tm6, xcap_dec, 12, 3);
end


% Generate the reference test signal pattern for test mode 6
function tm6 = tm6gen()
  Ns = 2^11 - 1;

  scr1 = lfsrgen([1 9 11],      Ns, '7FF').';
  scr2 = lfsrgen([1 7 9 10 11], Ns, '7FF').';

  x1 = [circshift(scr2, 0), ...
        mod((circshift(scr2, 1) + circshift(scr1, 4)),  2), ...
        mod((circshift(scr2, 2) + circshift(scr1, 9)),  2), ...
        mod((circshift(scr2, 0) + circshift(scr1, 10)), 2)];

  y1 = x1(:,1) + 2*x1(:,2) + 4*x1(:,3) + 8*x1(:,4);

  x2 = [circshift(scr1, 0), ...
        mod((circshift(scr1, 1) + circshift(scr2, 4)),  2), ...
        mod((circshift(scr1, 2) + circshift(scr2, 9)),  2), ...
        mod((circshift(scr1, 0) + circshift(scr2, 10)), 2)];

  y2 = x2(:,1) + 2*x2(:,2) + 4*x2(:,3) + 8*x2(:,4);

  tm6 = ((2*(16*y1 + y2) - 255)/256).';
end
```

```
% Volterra's estimation and analysis
function [HD2 HD3 HD4 RD] = volest(x, d, n, dly)
  % Init
  R  = 0;
  rD = 0;

  % Addition autocorrelation and cross-correlation
  for k = n:length(x),
    % Volterra products
    xi = [...
      1 ...
      x(k:-1:k-n+1) ...
      x(k:-1:k-n+1)   .*x(k:-1:k-n+1)    ...
      x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1)   .*x(k:-1:k-n+1)     .*x(k:-1:k-n+1)    ...
      x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1)   .*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k:-1:k-n+1+2)   .*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1)   .*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k-1:-1:k-n+1+1).*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k-2:-1:k-n+1)   .*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1)   .*x(k:-1:k-n+1)   .*x(k:-1:k-n+1)   .*x(k:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1).*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1).*x(k-1:-1:k-n+1).*x(k-1:-1:k-n+1)];

    % Autocorrelation matrix
    R = R + xi.'*xi;

    % Cross-correlation vector
    rD = rD + d(k-dly)*xi.';
  end

  % Wiener's MMSE solution
  hw = (R\rD).';

  % Separate the Volterra kernels per channel
  lw = [1 ...
        n ...
        n (n-1) (n-2) ...
        n (n-1) (n-2) (n-1) (n-2) (n-2) ...
        n (n-1) (n-1) (n-1)];

  ofst = 0;
  for i = 1:15,
    h{i} = hw(ofst+1:ofst+lw(i));
    ofst = ofst + lw(i);
  end

  % Calculate harmonic distortion
  HD2 = -10*log10(1/3*axc(h{2})/ ...
                  (1/5*axc(h{3}) + 1/9*axc(h{4}) + 1/9*axc(h{5})));

  HD3 = -10*log10(1/3*axc(h{2})/ ...
                  (1/7*axc(h{6}) + 1/15*axc(h{7})  + 1/15*axc(h{8}) + ...
                  1/15*axc(h{9}) + 1/27*axc(h{10}) + 1/15*axc(h{11})));

  HD4 = -10*log10(1/3*axc(h{2})/ ...
                  (1/9*axc(h{12}) + 1/21*axc(h{13})  + 1/25*axc(h{14}) + ...
                  1/21*axc(h{15})));

  % Calculate residual distortion
  z = h{1} + ...
      filter(h{2},  1, x(3:end)) + ...
      filter(h{3},  1, x(3:end).*x(3:end))   + ...
      filter(h{4},  1, x(3:end).*x(2:end-1)) + ...
      filter(h{5},  1, x(3:end).*x(1:end-2)) + ...
      filter(h{6},  1, x(3:end).*x(3:end)  .*x(3:end))   + ...
      filter(h{7},  1, x(3:end).*x(3:end)  .*x(2:end-1)) + ...
      filter(h{8},  1, x(3:end).*x(3:end)  .*x(1:end-2)) + ...
```

```
        filter(h{9},  1, x(3:end).*x(2:end-1).*x(2:end-1)) + ...
        filter(h{10}, 1, x(3:end).*x(2:end-1).*x(1:end-2)) + ...
        filter(h{11}, 1, x(3:end).*x(1:end-2).*x(1:end-2)) + ...
        filter(h{12}, 1, x(3:end).*x(3:end)  .*x(3:end)  .*x(3:end))   + ...
        filter(h{13}, 1, x(3:end).*x(3:end)  .*x(3:end)  .*x(2:end-1)) + ...
        filter(h{14}, 1, x(3:end).*x(3:end)  .*x(2:end-1).*x(2:end-1)) + ...
        filter(h{15}, 1, x(3:end).*x(2:end-1).*x(2:end-1).*x(2:end-1));

  z = z(1+dly-2+n:end);
  d = d(1+n:end);
  l = min([length(z) length(d)]);
  e = z(1:l) - d(1:l);

  RD = -10*log10(1/3*axc(h{2})/var(e));
end


% Auto-correlation, main term
function xc = axc(x)
  xc = sum(x.^2);
end


% LFSR
function out = lfsrgen(poly, len, seed)
  r = double(dec2bin(hex2dec(seed))) - 48;
  r = [zeros(1,poly(end)-length(r)) r];

  for i = 1:len,
    out(i) = r(1);
    fb = 0;
    for j = 2:length(poly),
      fb = mod(fb + r(poly(j)), 2);
    end
    r = [fb r(1:poly(end))];
  end
end
```

115.6.4.9 Transmitter timing jitter measurement

The transmitter timing jitter shall meet the specifications per the following measurement procedure:

a) The PHY is configured in test mode 2 (115.5.2).

b) RMS (Root Mean Square) jitter of the crossing events of transmit signal with the average optical power is measured relative to the corresponding edges of an unjittered clock reference with a frequency of 162.5 MHz (one half the symbol rate), over an interval of 2 ms ± 10%.

The measurement device connected to TP2 shall meet the following specifications:

1) Capture capability.

2) High-frequency low-pass corner of at least 32.5 MHz with slope of –20 dB/decade.

3) Low-frequency high-pass corner of maximum 1 kHz with slope of +20 dB/decade.

4) The unjittered reference is a constant frequency clock extracted from each record of captured output at TP2, and is based on linear regression of frequency and phase that produces a minimum Time Interval Error.

115.6.4.10 Transmitter relative intensity noise (RIN) measurement

This test might not be an appropriate system level test in all implementations, but all implementations shall meet the specified performance. The PHY is configured in test mode 5 (115.5.5). RIN is measured according to 58.7.7 with the following exceptions:

a) The low-pass filter bandwidth is 162.5 MHz (one half the symbol rate).

b) Step d) of the test procedure in 58.7.7.3 is replaced by measuring the value of the photocurrent of the optical to electrical converter I_{oe}.

c) Step e) of the test procedure in 58.7.7.3 is replaced by using the following equation to evaluate RIN:

$$RIN = 10 \times \log_{10}\left(\frac{P_N}{BW \times I_{oe}^{\ 2} \times R}\right) - G \text{ (dB/Hz)} \qquad (115\text{–}34)$$

where

RIN	is the relative intensity noise
P_N	is the electrical noise power in Watts with modulation off
BW	is the low-pass bandwidth of the apparatus – high-pass bandwidth of the apparatus due to dc blocking capacitor
I_{oe}	is the photocurrent of the optical to electrical converter
R	is the effective load impedance of the optical to electrical converter (for example, a 50 Ω detector load in parallel with a 50 Ω power meter would give R equal to 25)
G	is the gain in dB of any amplifier in the noise measurement path

115.6.4.11 Transmitter modal power distribution measurement

The modal power distribution (MPD) at TP2 shall meet the specifications of 115.6.3.1 using an encircled angular flux (EAF) measurement method based on two-dimensional far field pattern data captured at TP2, which conforms to IEC 61300-3-53, defined for step-index multimode fibers.

When making this measurement the PHY is configured in normal (non-test) operation. A measured MPD meets the specification when it is higher than the lower bound limits defined for every angle. For the angle points not specified in Table 115–9, the EAF lower bound limit is calculated by linear interpolation.

115.7 Characteristics of the fiber optic cabling (channel)

The fiber optic cabling model is shown in Figure 115–36.

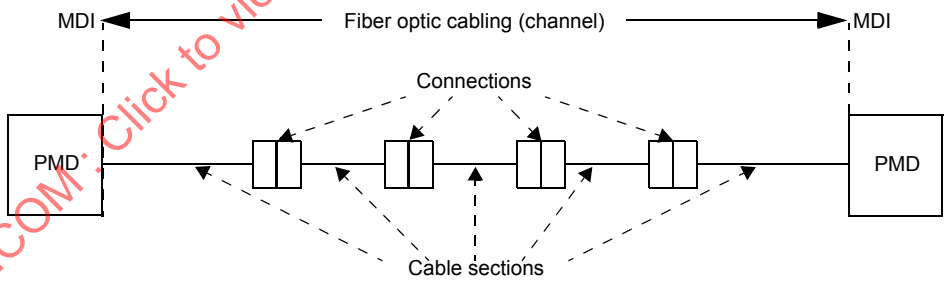

Figure 115–36—Fiber optic cabling model (channel)

1000BASE-RHx operation requires fiber optic cable meeting the requirements of IEC 60793-2-40 sub-category A4a.2 multimode plastic optical fibers with appropriate augmentation as specified in this subclause. The link segment uses two optical fibers, one for each direction (see 115.1.5), and is comprised of one or more cable sections and their in-line connections. The fiber optic cabling model (channel) defined

here is a simplex fiber optic link segment, which is sufficient for testing purposes. The term channel is used here for consistency with generic cabling standards.

The following three different fiber optic channel types are specified:

a) Fiber optic channel type I supports reliable link per the specifications of 115.6.3.3 with reach up to at least 50 m. The fiber optic channel type I shall meet a maximum insertion loss of 9.5 dB without in-line connections and the transfer function specification of 115.7.1, per measurement techniques defined in 115.7.4 and 115.7.5, and under spectral distribution and launching modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1.

b) Fiber optic channel type II supports reliable link per the specifications of 115.6.3.3 with reach up to at least 40 m. The fiber optic channel type II shall meet a maximum insertion loss of 8 dB without in-line connections and the transfer function specification of 115.7.2, per measurement techniques defined in 115.7.4 and 115.7.5, and under spectral distribution and launching modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1. The parameters of this channel type include additional considerations for the environmental conditions of the intended application.

c) Fiber optic channel type III supports reliable link per the specifications of 115.6.3.3 with reach up to at least 15 m. The fiber optic channel type III shall meet a maximum insertion loss of 3 dB without in-line connections and the transfer function specification of 115.7.3, per measurement techniques defined in 115.7.4 and 115.7.5, and under spectral distribution and launching modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1. The parameters of this channel type include additional considerations for the environmental conditions of the intended application.

NOTE—It may be possible to construct compliant fiber optic cables longer than indicated. Length of a fiber optic cable does not imply compliance to specifications.

The fiber optic channel transfer function captures the frequency-dependent propagation of the light through the fiber that is caused by the modal and chromatic dispersion. The transfer function is specified in magnitude normalized at dc and is given as a lower bound limit. Any fiber optic channel including in-line connections shall meet the transfer function specification of each type.

The number of supported in-line connections is not normative but instead depends on the specific in-line connection technology and the unallocated link margin (see 115.7.6).

115.7.1 Transfer function of fiber optic channel type I

The transfer function of a fiber optic channel is compliant with type I when it is higher than the lower bound limits of Table 115–13 for any frequency less than or equal to 162.5 MHz. For the frequency points not specified, the transfer function is calculated by linear interpolation. The transfer function lower bound limits of a fiber optic channel type I are illustrated in Figure 115–37.

Table 115–13—Transfer function lower bound limits for fiber optic channel type I

Frequency (MHz)	Transfer function magnitude (dB)	Frequency (MHz)	Transfer function magnitude (dB)
0	0.0	70	–4.0
10	–0.1	85	–5.4
20	–0.3	105	–6.9
30	–0.7	125	–7.8
40	–1.3	145	–8.7
50	–2.1	162.5	–9.5
60	–3.0		

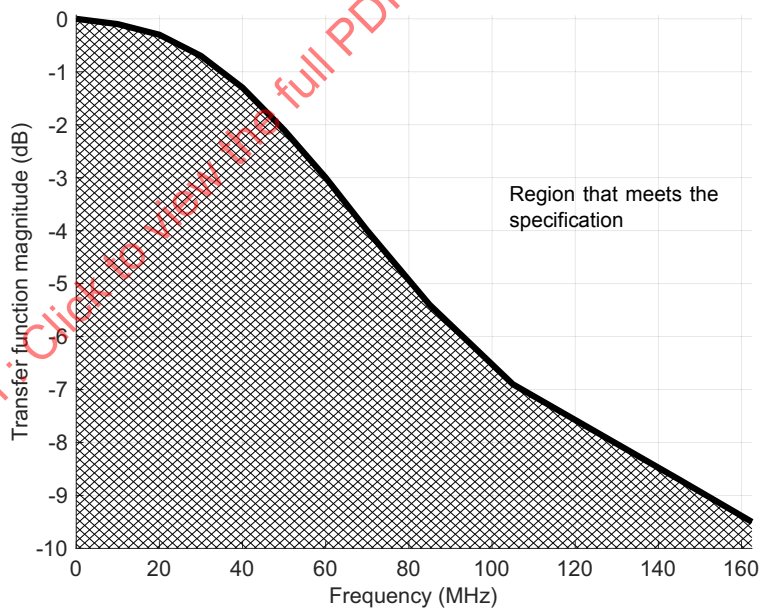

Figure 115–37—Transfer function illustration for fiber optic channel type I

115.7.2 Transfer function of fiber optic channel type II

The transfer function of a fiber optic channel is compliant with type II when it is higher than the lower bound limits of Table 115–14 for any frequency less than or equal to 162.5 MHz. For the frequency points not specified, the transfer function is calculated by linear interpolation. The transfer function lower bound limits of a fiber optic channel type II are illustrated in Figure 115–38.

Table 115–14—Transfer function lower bound limits for fiber optic channel type II

Frequency (MHz)	Transfer function magnitude (dB)	Frequency (MHz)	Transfer function magnitude (dB)
0	0	70	–2.2
10	–0.1	85	–3.2
20	–0.2	105	–4.8
30	–0.4	125	–6.2
40	–0.7	145	–7.4
50	–1.1	162.5	–8.1
60	–1.6		

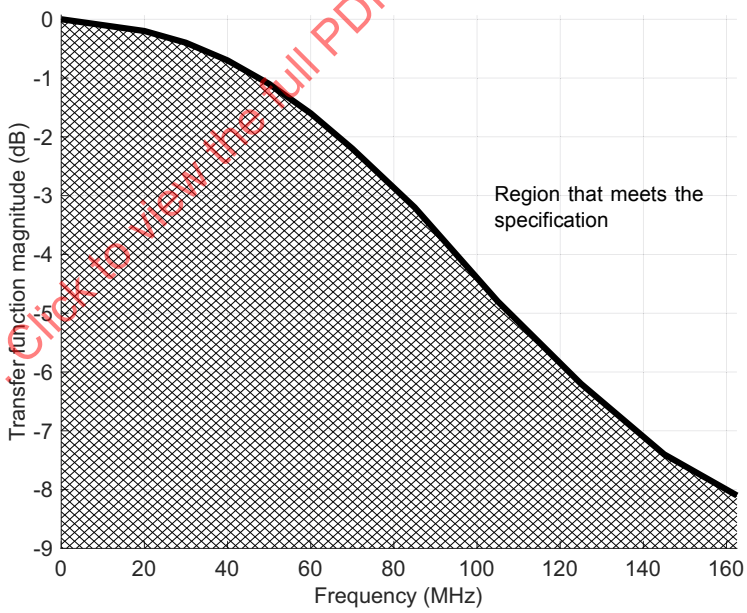

Figure 115–38—Transfer function illustration for fiber optic channel type II

115.7.3 Transfer function of fiber optic channel type III

The transfer function of a fiber optic channel is compliant with type III when it is higher than the lower bound limits of Table 115–15 for any frequency less than or equal to 162.5 MHz. For the frequency points not specified, the transfer function is calculated by linear interpolation. The transfer function lower bound limits of a fiber optic channel type III are illustrated in Figure 115–39.

Table 115–15—Transfer function lower bound limits for fiber optic channel type III

Frequency (MHz)	Transfer function magnitude (dB)
0	0
50	–0.1
85	–0.5
125	–1.4
162.5	–2.5

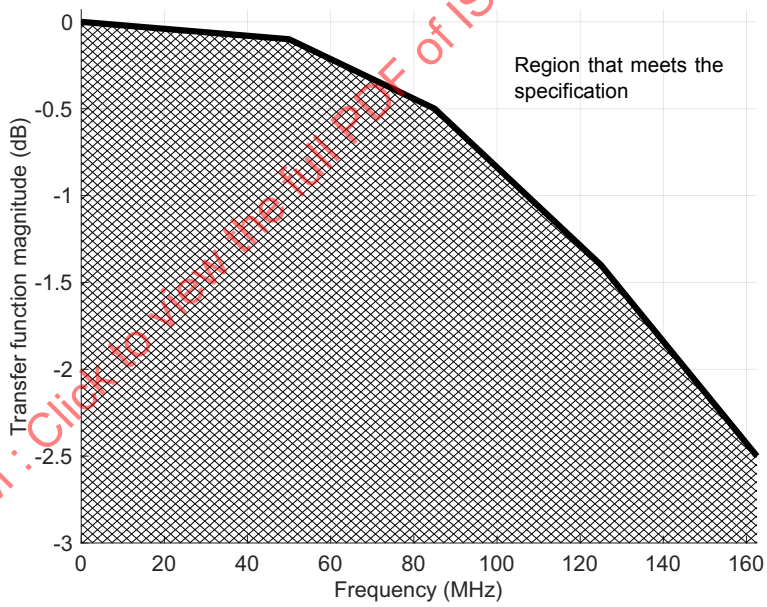

Figure 115–39—Transfer function illustration for fiber optic channel type III

115.7.4 Fiber optic channel insertion loss measurement

The fiber optic channel shall meet the insertion loss specification per measurement according to ISO/IEC 14763-3, under spectral distribution and launch modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1.

115.7.5 Fiber optic channel transfer function measurement

The fiber optic channel shall meet the transfer function specification per measurement according to IEC 60793-1-41, under spectral distribution and launch modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1.

115.7.6 Worst-case 1000BASE-RHx link power budget

Table 115–16 shows the worst-case link power budget and the unallocated link margin for a 1000BASE-RHx PHY, which are derived from the transmitter and the receiver optical specifications as well as fiber optic channel specifications provided in 115.6.3.1, 115.6.3.3, and 115.7, respectively.

Table 115–16—Worst case link power budget

Parameter	Units	RHA	RHB	RHC	
		Fiber optic channel			
		Type I	Type I	Type II	Type III
Link power budget (min)	dB	11	10	8	9.5
Channel insertion loss without in-line connections (max)	dB	9.5	9.5	8	3
Unallocated link margin (min)[a]	dB	1.5	0.5	0	6.5

[a] Unallocated link margin may be used for in-line connections (connectors). Maximum 1.5 dB insertion loss per in-line connection is assumed.

115.8 Medium Dependent Interface (MDI)

The 1000BASE-RHx PMD is coupled to the fiber optic cabling through a connection at the Medium Dependent Interface (MDI). The MDI mechanical interface for 1000BASE-RHA is defined in 115.8.1. An MDI mechanical interface is not specified for 1000BASE-RHB and 1000BASE-RHC.

The transmit signal characteristics are defined at the output end of a 1 meter length (TP2) of plastic optical fiber. The optical receive signal is defined at the output of the fiber optic cabling (TP3). Therefore, both the transmitter and the receiver optical characteristics are specified including the MDI mechanical implementation.

115.8.1 MDI mechanical interface for 1000BASE-RHA

The 1000BASE-RHA PMD and the associated MDI receptacle are coupled to the prepared fiber optic cabling without a plug.

The 1000BASE-RHA MDI receptacle shall be a duplex housing consisting of two separated slots (transmit and receive). Viewed from the link segment side of the connection, the 1000BASE-RHA MDI receptacle

shall properly indicate with labeling the slot of the transmitter and the slot of the receiver. Figure 115–40 illustrates example MDI receptacle with labeling.

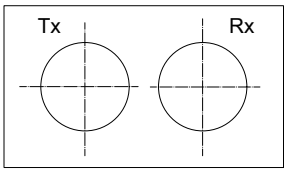

Figure 115–40—Example MDI receptacle (link segment side view)

The 1000BASE-RHA MDI receptacle shall accept link segment duplex cable compliant with specifications of buffered A4 fibers per IEC 60794-2-41.

The 1000BASE-RHA MDI receptacle shall have defined open and close states. The close state shall provide a stable and resilient connection by utilizing a retention mechanism with a minimum steady-state retention force of 4 N aligned with the center line of the receptacle hole in the direction of cable extraction for polyethylene (PE) jacket buffered fibers. Retention force per test procedure of IEC 61300-2-4 shall result in a loss of less than 0.4 dB of the AOP coupled by the PMD transmitter into the fiber while the load is applied and after the load is removed.

The duplex POF cable needs to be properly prepared and split into two single jacketed fibers for connection to the 1000BASE-RHA MDI receptacle.

The POF cable is normally prepared without polishing by using a POF cutting tool. The cutting tool may clamp the POF cable, without damaging the jacket, to prevent movement when cutting it (e.g., with a razor blade). The cutting tool shall provide the following results:

— The resultant fiber end facets are perpendicular to the cable axis with end angle error less than 2.5º.
— The flatness of the fiber end facet produces an insertion loss of less than 1.5 dB, per butt coupling of the two resultant fiber segments.

The duplex cable is split to enable the following:

— Full insertion and guidance inside the MDI receptacle slot
— Bend radius over 25 mm

The 1000BASE-RHA MDI receptacle vendor shall clearly indicate the minimum split length needed for a suitable connection. The left side of Figure 115–41 illustrates the duplex POF cable splitting and the right side illustrates the fiber cable connection to 1000BASE-RHA MDI receptacle.

One of the jackets of the duplex POF cable shall have marking. A possible marking is illustrated in Figure 115–41. Such marking can facilitate installation when the optical transmitters of the link partners are off. There may be specific application marking requirements.

Two different installation scenarios can be considered for correct link segment crossover—the scenario where visible transmit light is used and the scenario where the fiber cable marking is used.

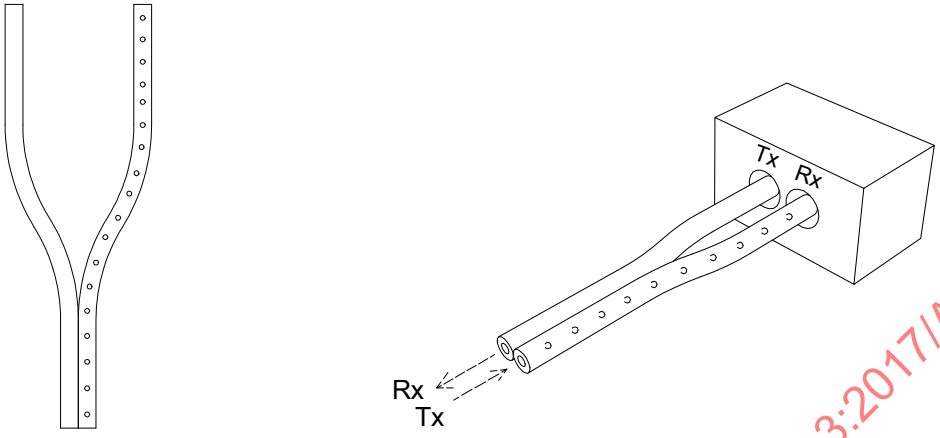

Figure 115–41—Duplex POF cable splitting and connection to the 1000BASE-RHA MDI receptacle

When the remote link partner is transmitting, the fiber used by the link partner to transmit can be easily distinguished because of the 1000BASE-RHA visible light. This fiber is connected to the local receiver, and the other fiber of duplex cable is connected from the local transmitter to the remote receiver. When the remote link partner is not transmitting, the cable specific marking can be used to implement a single crossover between the link partners identifying the correct insertion of the fiber ends into the MDI receptacle.

115.9 1000BASE-H Operations, Administration, and Maintenance (1000BASE-H OAM) channel

The optional 1000BASE-H OAM channel provides a mechanism to reliably exchange messages between station management entity (STA) peers attached to link partners. The 1000BASE-H OAM message exchange occurs in the PCS, as part of the PHD, and does not impact the normal GMII to GMII data transmission. Moreover, the 1000BASE-H OAM message exchange is not affected by EEE operation.

The 1000BASE-H OAM channel utilizes 1000BASE-H OAM transmit and receive registers accessible via the MDIO as well as capabilities specified in the following channel descriptions. All MDIO accessible registers for 1000BASE-H OAM operation are specified in 45.2.3.47a and 45.2.3.47b.

The 1000BASE-H OAM channel uses several control bits (MSGT, MERT, PHYT) for message identification, message delivery notification, and flow control.

115.9.1 1000BASE-H OAM message transmission protocol

When the STA connected to the local PHY needs to transmit a new message it shall follow these steps:

a) Wait until bit TXO_REQ of register 3.500 is zero, which indicates that the 1000BASE-H OAM transmit registers are free and that a new 1000BASE-H OAM message can be written.
b) Write the 128 user data bits of the 1000BASE-H OAM message into registers 3.501 through 3.508.