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Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) —

Part 3: Physical and data link protocols for control communication

Télécommunications et échange d'information entre systèmes — Réseau de zone de drones (Unmanned aircraft area network - UAAN) —

Partie 3: Protocoles de liaison de données et physiques pour la communication de contrôle

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Foreword

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This document was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 6, *Telecommunications and information exchange between systems*.

A list of all parts in the ISO/IEC 4005 series can be found on the ISO and IEC websites.

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Introduction

Unmanned aircrafts (UAs) operating at low altitudes will provide a variety of commercial services in the near future. UAs that provide these services are distributed in the airspace. In low uncontrolled airspace, many people operate their own UAs without the assignment of communication channels from a central control centre.

This document describes control communication, which is a wireless distributed communication. Control communication allows control pairs of UA and controller distributed over the airspace to communicate with each other without serious interference. The channel used for control communication has a multi-channel structure, which enables UAs and controllers to independently use the communication link occupied by each other. A wireless distributed communication described by this document is intended to be used in licensed frequency bands.

The ISO/IEC 4005 series consists of the following four parts:

ISO/IEC 4005-1: To support various services for UAs, it describes a wireless distributed communication model and the requirements that this model shall satisfy.

ISO/IEC 4005-2: It describes communication in which all units involved in UA operation can broadcast or exchange information by sharing communication resources with each other.

ISO/IEC 4005-3 (this document): It describes the control communication for the controller to control the UA.

ISO/IEC 4005-4: It describes video communication for UAs to send video to a controller.

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Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) —

Part 3:
Physical and data link protocols for control communication

1 Scope

This document specifies communication protocols for the physical and data link layer for control communication, which is wireless distributed communication network for units related with unmanned aircrafts (UAs) in level II.

This document describes control communication, which is one-to-one communication between a UA and a controller.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 4005-1, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 1: Communication model and requirements*

ISO/IEC 4005-2:2023, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 2: Physical and data link protocols for shared communication*

ISO/IEC 4005-4, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 4: Physical and data link protocols for video communication*

ISO 21384-4, *Unmanned aircraft systems — Part 4: Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions defined in ISO/IEC 4005-1, ISO/IEC 4005-2, ISO 21384-4 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

3.1
subchannel map
2-bit string indicating whether subchannels are available

Note 1 to entry: In wireless distributed communication, the subchannel map of each unit is generally different.

4 Abbreviated terms

CC Control Communication

CRC	Cyclic Redundancy Check
CSCH	Control Subchannel
DLL	Data Link Layer
DS	Dedicated Slot
FN	Frame Number
IWR	Initial Work Resource
LFSR	Linear Feedback Shift Register
PB	Parsing Block
PKH	Packet Header
PN	Pseudo Noise
SA	Source Address
SC	Shared Communication
TSB	Tone Slot Block
TX	Transmission
UTC	Coordinated Universal Time
VC	Video Communication
VSCH	Video Subchannel

5 Physical layer

5.1 Channel and frame structure for data channel

5.1.1 Number of data channels and bandwidth

The number of data channels is *N* as shown in Figure 1. *N* is greater than or equal to one. The bandwidth of one data channel is 1,25 MHz. The *N* is determined in the upper layer.

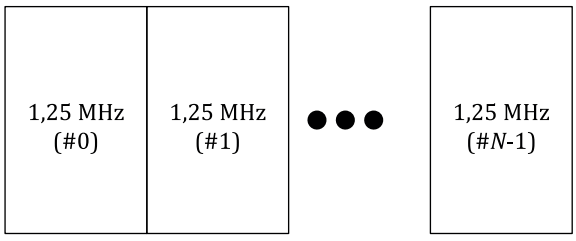
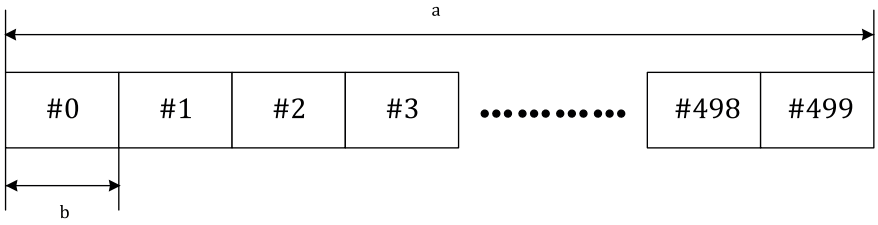


Figure 1 — Data channels in frequency region

5.1.2 Frame structure

The frame length of the data channel is 1 sec and consists of 500 slots and one slot time T_s is 2 ms as shown in Figure 2. *FN* is a frame number that varies from 0 to 59 and has the same value as the second of the current time.



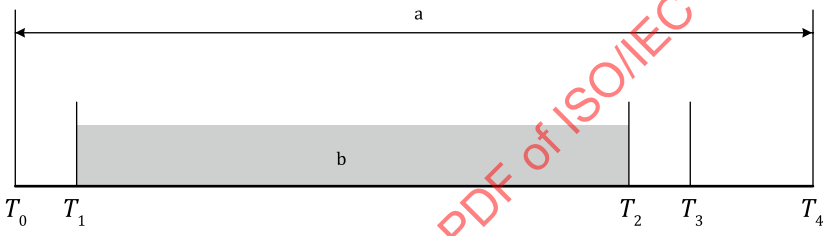
a 1 frame, T_f = 1 sec = 500 T_s.

b 1 slot, T_s = 2 ms.

Figure 2 — Frame structure of the control channel

5.1.3 Slot transmit time mask

The transmission time mask of a slot is shown in Figure 3.



a 2 ms.

b Modulated signal.

Figure 3 — The transmission time mask of a slot

T_1, T_2, T_3, T_4 are symbol offsets from T_0 and symbol time is 1/672000 sec. Each value is as follows: T_1 is 2, T_2 is 1297, T_3 is 1299, T_4 is 1344.

T_0 is 0 µs as the start time of the slot and the power amplifier is gated on and unmodulated fine signals begin to be transmitted. T_1 is an offset at which modulation signal transmission starts. T_2 is an offset at which the transmission of the modulated signal ends. T_3 is an offset at which the power amplifier is gated off, and transmission of unmodulated fine signals is stopped. The transmit power of T_0 to T_1, T_2 to T_3 shall be at least 50 dB less than the modulation signal transmit power.

5.1.4 Subchannels

5.1.4.1 General

One data channel consists of 20 subchannels as shown in Figure 4. Subchannel y of control channel x is composed of the following slot set.

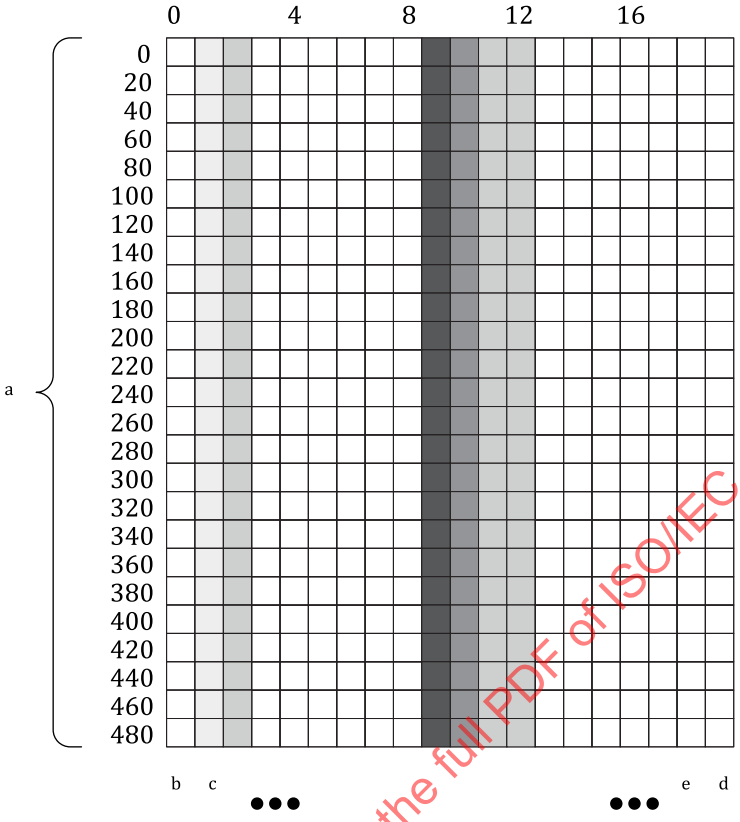
$$CCH_{x,y} = S_{x,z}, S_{x,z+20}, S_{x,z+40}, \ldots, S_{x,z+480}$$

$$z = \begin{cases} y, & evenframe \\ y+2-\lfloor (y \bmod 4)/2 \rfloor \times 4, & oddframe \end{cases} \quad (1)$$

where

y is subchannel number, y=0, 1, ..., 19;

$S_{x,z}$ is slot z of control channel x.



a CCH_x
b $CCH_{x,0}$
c $CCH_{x,1}$
d $CCH_{x,18}$
e $CCH_{x,19}$

Figure 4 — Subchannel structure of control communication in even frame

A subchannel consists of 25 slots, the i-th slot resource of the subchannel y of the channel x is indicated by $SR_{x,y,i}$ and the subchannel y of frequency channel x is indicated by $CCH_{x,y}$. Therefore, $CCH_{x,y}$ *is* as follows.

$$CCH_{x,y} = SR_{x,y,0}, SR_{x,y,1}, \ldots, SR_{x,y,24} \quad (2)$$

where $SR_{x,y,i}$ is i-th slot resource of subchannel y of channel x, i=0, ..., 24.

5.1.4.2 Up and down link decision of slot resources

For $SR_{x,y,i}$, 5 slots satisfying (i *mod* 5) =(FN *mod* 5) are downlink and remain 20 slots are uplink, where *mod* means modulo operation.

5.1.5 Initial work resources (IWR) and channel

The upper layer can set the initial work resource (IWR) as follows, and the use of the IWR is determined by the upper layer.

Four subchannels of frequency channel N_IWR, $CCH_{N\_IWR,16}$, $CCH_{N\_IWR,17}$, $CCH_{N\_IWR,18}$, $CCH_{N\_IWR,19}$ are designated as initial work channels. They are newly named $IWRCH_0$, $IWRCH_1$, $IWRCH_2$, $IWRCH_3$ respectively. These four initial work channels are not used for control, but are initially used to allocate control subchannels (CSCHs) between the UA and the controller, where N_IWR is received from the upper layer with UPtoDL.InfoIWRSlot.

The 25 slots of $IWRCH_y$ are divided into five IWRs in order.

$$IR_{y,i} = ISR_{x,5i}, ISR_{x,5i+1}, ISR_{x,5i+2}, ISR_{x,5i+3}, ISR_{x,5i+4} \quad (3)$$

where

y is an *IWRCH* number and has the value from 0 to 3;

$ISR_{x,y,i}$ is i-th slot resource of $IWRCH_y$.

5.1.6 Dedicated slots and dedicated subchannels

The upper layer can pre-determine one or more subchannels as dedicated subchannels. In this case, the tone subslot sets mapped with the dedicated subchannel is not used as a competition tone and can be used for other purposes. Slots in the dedicated subchannel are used as dedicated slots (DSs). One or several dedicated slots can be assigned to UAs and controllers in advance. UAs and controllers use the dedicated slots without competition.

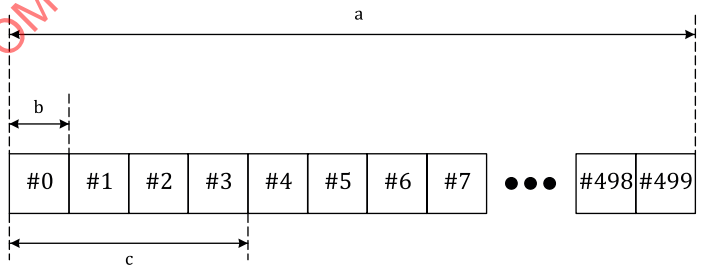
It is recommended to set the dedicated subchannel in frequency channel N_IWR.

Dedicated subchannel information and dedicated slot information are received from an upper layer through UPtoDL.InfoDedicatedChannel and UPtoDL.InfoDedicatedSlot.

5.2 Channel and frame structure for tone channel

5.2.1 Frame structure and bandwidth

The tone channel of the control communication indicates a competitive tone channel. The frame length of tone channel is 1 sec and the number of slots per frame is 500. Four tone slots constitute one tone slock block (TSB). Thus, there are 125 TSBs in one second frame as shown in Figure 5.



a 1 frame, T_f = 1 second = 500 T_s.

b 1 slot, T_s = 2 ms.

c 1 slot block, T_{sb} = 8 ms.

Figure 5 — Frame structure of tone channel in control communication

The bandwidth of the tone channel is 250 kHz. *FN* is a frame number that varies from 0 to 59 and has the same value as the second of the current time.

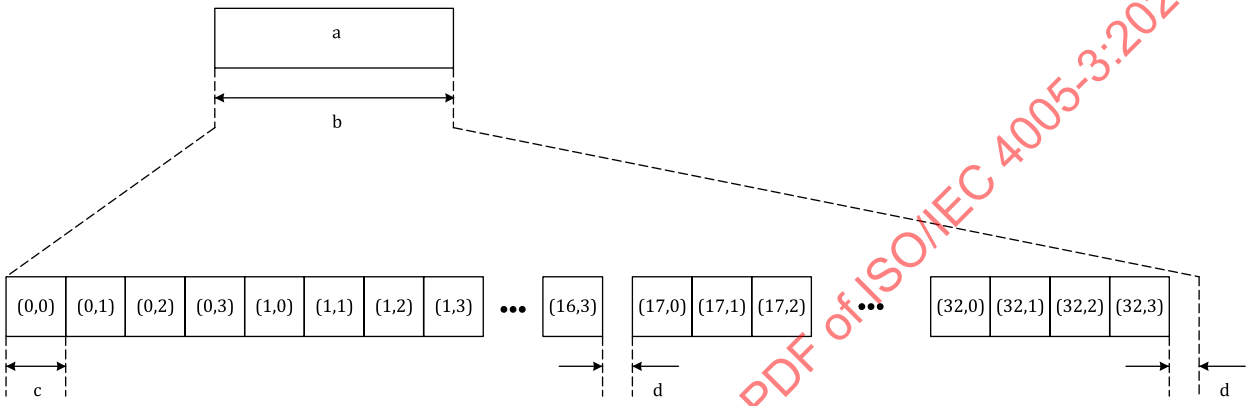
5.2.2 Slot transmit power

The maximum slot transmission power of the tone channel, PmaxTCH, is received as UPtoDL. InfoPowerParamCCH from the upper layer. The transmission power of the tone subslot signal is determined by adding the PTX_CCHTCH_differ value to the transmission power of the mapped CSCH.

5.2.3 Slot block structure

There are three types of slot blots. TSBtype0, TSBtype1, TSBtype2 are these. The type of each slot blot of the TCH is received from the upper layer as UPtoDL.InfoTSBTypeMap.

There are 132 subslots in one slot block of TSBtype0. The length T_{ss} of the subslot is 60 µs. The 132 subslots are divided into four parts, as shown in Figure 6, according to each slot numbers.



a Type 0.

b 1 slot block, T_{sb} = 8 ms.

c T_{ss} = 60 µs.

d 40 µs.

Figure 6 — Type 0 TSB structure

In case of TSBtype0, n-th slot block is composed as follows.

— (0, 4n), (0, (4n + 1)), (0, (4n + 2)), (0, (4n + 3)), (1, 4n), (1, (4n + 1)), (1, (4n + 2)), (1, (4n + 3)),… , (32, 4n), (32, (4n + 1)), (32, (4n + 2)), (32, (4n + 3))

where (x, y) is the x-th subslot of the y-th subslot set. The 132 subslots are divided into four subslot sets.

— $\{S_{4n}\}$ = {(0, 4n), (1, 4n), …, (32, 4n)}

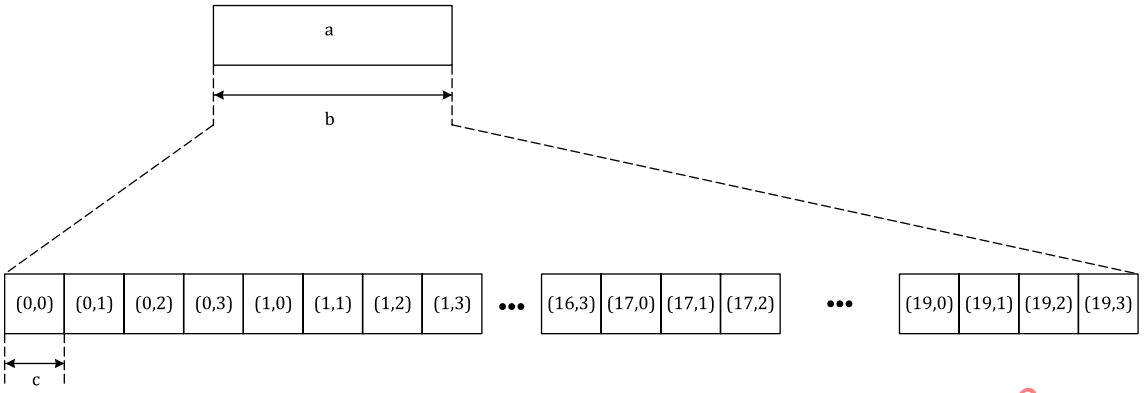
— $\{S_{4n+1}\}$ = {(0, (4n + 1)), (1, (4n + 1)), …, (32, (4n + 1))}

— $\{S_{4n+2}\}$ = {(0, (4n + 2)), (1, (4n + 2)), …, (32, (4n + 2))}

— $\{S_{4n+3}\}$ = {(0, (4n + 3)), (1, (4n + 3)), …, (32, (4n + 3))}

where $\{S_x\}$ is the x-th subslot set.

There are a total of 80 subslots in TSBtype1. The length T_{ss} of the subslot is 100 µs. The 80 subslots are divided into four parts, as shown in Figure 7, according to each slot number.



a Type1.

b 1 slot block, T_{sb} = 8 ms.

c T_{ss} = 100 µs.

Figure 7 — Type 1 TSB structure

The *n*-th slot block that belongs to TSBtype1 is composed of the following subslot combinations.

— (0, 4*n*), (0, (4*n* + 1)), (0, (4*n* + 2)), (0, (4*n* + 3)), (1, 4*n*), (1, (4*n* + 1)), (1, (4*n* + 2)), (1, (4*n* + 3)),... , (19, 4*n*), (19, (4*n* + 1)), (19, (4*n* + 2)), (19, (4*n* + 3))

The 80 subslots make up four subslot sets.

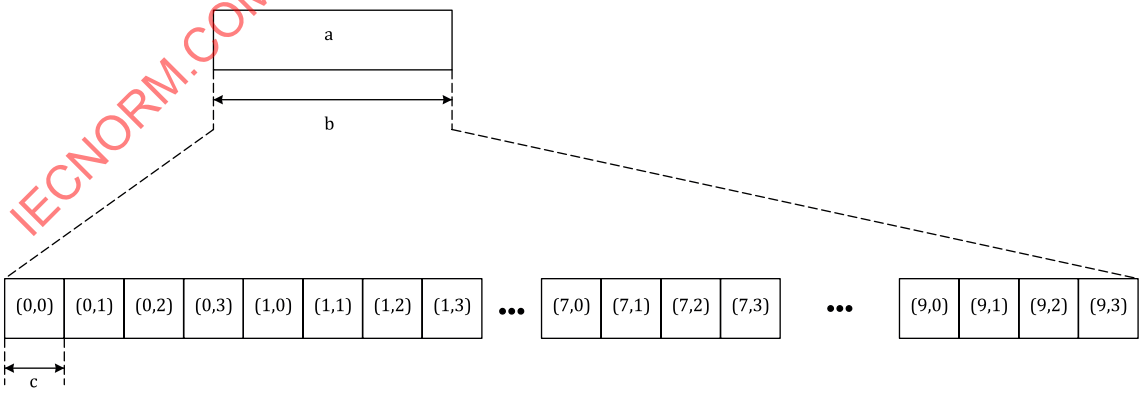
— $\{S_{4n}\}$ = {(0, 4*n*), (1, 4*n*), ..., (19, 4*n*)}

— $\{S_{4n+1}\}$ = {(0, (4*n* + 1)), (1, (4*n* + 1)), ..., (19, (4*n* + 1))}

— $\{S_{4n+2}\}$ = {(0, (4*n* + 2)), (1, (4*n* + 2)), ..., (19, (4*n* + 2))}

— $\{S_{4n+3}\}$ = {(0, (4*n* + 3)), (1, (4*n* + 3)), ..., (19, (4*n* + 3))}

There are a total of 40 subslots in TSBtype2. The length T_{ss} of the subslot is 200 µs. The 40 subslots are divided into four parts, as shown in Figure 8, according to each slot numbers.



a Type2.

b 1 slot block, T_{sb} = 8 ms.

c T_{ss} = 200 µs.

Figure 8 — Type 2 TSB structure

The *n*-th slot block that belongs to TSBtype2 is composed of the following subslot combinations.

— (0, 4*n*), (0, (4*n* + 1)), (0, (4*n* + 2)), (0, (4*n* + 3)), (1, 4*n*), (1, (4*n* + 1)), (1, (4*n* + 2)), (1, (4*n* + 3)),... , (9, 4*n*), (9, (4*n* + 1)), (9, (4*n* + 2)), (9, (4*n* + 3))

The 40 subslots make up four subslot sets.

— $\{S_{4n}\}$ = {(0, 4*n*), (1, 4*n*), ..., (9, 4*n*)}

— $\{S_{4n+1}\}$ = {(0, (4*n* + 1)), (1, (4*n* + 1)), ..., (9, (4*n* + 1))}

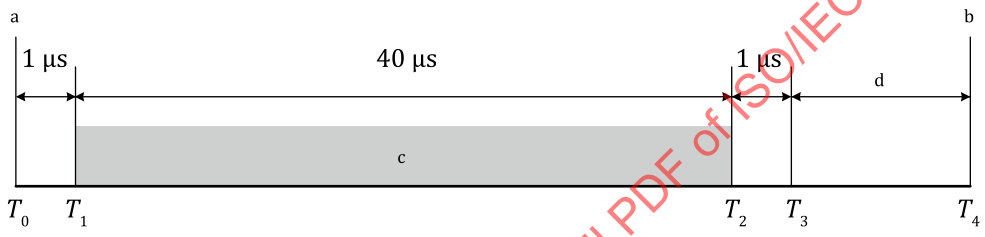
— $\{S_{4n+2}\}$ = {(0, (4*n* + 2)), (1, (4*n* + 2)), ..., (9, (4*n* + 2))}

— $\{S_{4n+3}\}$ = {(0, (4*n* + 3)), (1, (4*n* + 3)), ..., (9, (4*n* + 3))}

Regardless of the type of TSB, there are a total of 500 subslot sets in one frame.

5.2.4 Subslot transmission time mask

Subslot transmission time mask is shown in Figure 9.



Key

T_0	0 µs
T_1, T_2, T_3, T_4	time offsets from T_0
a	Subslot start.
b	Subslot end.
c	Tone signal.
d	Guard time.

Figure 9 — Subslot transmission time mask

T_1, T_2, T_3, and T_4 are time offsets from T_0. T_1 is 1 µs, T_2 is 41 µs, and T_3 is 42 µs.

In TSBtype0, T_4 is 60 µs, guard time is 18 µs.

In TSBtype1, T_4 is 100 µs, guard time is 58 µs.

In TSBtype2, T_4 is 200 µs, guard time is 158 µs.

T_0 is the time when the power amplifier is gated on, and unmodulated fine signals begin to be transmitted. T_1 is the time at which transmission of the modulated signal begins. T_2 is the time at which transmission of the modulated signal is terminated. T_3 is the time when the power amplifier is gated off and the transmission of unmodulated fine signals is stopped. The transmission power of the time region from T_0 to T_1 and the transmission power of the time region from T_2 to T_3 shall be 50dB or more less than the modulated signal transmission power.

5.2.5 Subslot signal waveform

The subslot signal waveform is the same as that of shared communication. See ISO/IEC 4005-2:2023, 5.1.2.3.

The modulation scheme of subslot signal is on-off keying. The subslot signal is started at T_1 and transmitted during the 40 µs interval. The waveform of the subslot transmission signal uses a raised cosine function. The subslot signal is generated by the following formula.

$$g(t;\alpha)=\frac{\cos(\pi\alpha(t-2T))}{1-(2\alpha(t-2T)/T)^2}\sin c\left(\frac{(t-2T)}{T}\right), \quad 0\le t\le 4T \tag{4}$$

where

α is 0,75 as a roll-off factor;

T is 10 µs as a raised cosine period.

5.3 Encoding procedure

The encoding procedure is identical with that of shared communication. See ISO/IEC 4005-2:2023, 5.2.

The final encoded signal is located between T_1 and T_2 in Figure 3, i.e. in the modulated signal part.

5.4 Physical layer procedure

5.4.1 Synchronization

All messages shall be transmitted based on UTC absolute time. All times are measured on UTC.

The synchronization mode of the unit includes 'A sync', 'B sync' and 'C sync'.

— A sync is synchronization obtained from UTC.

— B sync is secondary synchronization acquired from the synchronization signal of the A sync unit.

— C sync is sync status within 20 sec after sudden loss of sync in A or B sync mode.

A sync unit shall know the date, hour, minute, second, slot number.

The time error of A sync shall be within ±0,4 µs. The time error of B sync shall be within ±4 µs. The time error of C sync shall be within ±5 µs.

The frequency error of A sync shall be within ±0,1 ppm. The frequency error of the B sync shall be within ±0,2 ppm. The frequency error of the C sync shall be within ±0,3 ppm.

5.4.2 Subchannel power

The maximum power of the CSCH, PmaxCCH, is received as UPtoDL.InfoPowerParamCCH from the upper layer. The maximum transmission power and minimum transmission power of each CSCH are received from the upper layer as UPtoDL.InfoPowerParamCCHsub. The power control of each CSCH is described in the resource allocation procedure.

5.4.3 Measurements

The physical layer shall have the ability to measure the following parameters. The received signal power of a tone subslot, the received signal power of a data slot, and propagation delay time of the received data signal shall be measured. The receiving power determination point shall be the receiving antenna connector.

5.4.4 Coexistence operation

If the hardware of shared communication described in ISO/IEC 4005-2 and the hardware of control communication described in this document and the hardware of video communication described in

ISO/IEC 4005-4 are completely physically isolated and do not affect each other at all, it shall be allowed that they do not perform coexistence operations, which is implementation dependent. In general, the three communications affect each other, and in this case, the following coexistence operations shall be performed.

The TX operation of a shared slot includes the TX of the corresponding shared slot and the TX operation in the mapped tone subslot set. The TX operation of a control communication includes TX of the mapped tone subslot set and CSCH TX. The TX operation of video communication includes TX of a mapped tone subslot set and VSCH TX.

When a UA periodically broadcasts its information to a shared slot of a shared channel, a shared slot and a tone subslot set mapped to the shared slot generally require 1 slot and 4 slots, respectively, for TX operation. If the TX operation of the shared slot used for mandatory periodic broadcasting and the TX operation of the control channel overlap, the TX operation of the shared slot shall be performed.

A CSCH and a VSCH shall be allocated so that they do not overlap in time.

The TX time of the tone subslot set mapped with mandatory periodically broadcasted shared slot, the TX time of the tone subslot set mapped with the CSCH, and the TX time of the tone subslot set mapped with the VSCH shall not overlap each other. If the control TSB type is TSBtype0, the control tone subslot set and the shared tone subslot set can be located in the same TSB. In this case, the two tone subslot set numbers shall be different. If the control TSB type is not TSBtype0, the control tone subslot set and the shared tone subslot set cannot be located in the same TSB.

The TX operation time of the tone subslot set mapped with a CSCH can overlap the TX time of a VSCH, and in this case, the corresponding video slot cannot be transmitted. The TX operation time of the tone subslot set mapped with a VSCH can overlap with the slot TX time of a CSCH, and in this case, the corresponding control slot cannot be transmitted.

The coexistence operation of the tone subslot set mapped with an IWR is the same with coexistence operation of the tone subslot set mapped with the CSCH.

6 Data link layer

6.1 General

The data link layer allocates subchannels consisting of 25 slots to controllers and UAs. The controller can use this subchannel to control the UA. The typical application service of control communication is that the controller controls the UA, but it is possible to provide other services through the occupied control link. This is determined at the upper layer.

The procedure of using the subchannel is shown in Figure 10 and as follows:

— negotiation of subchannel number to be allocated;

— competition for allocation and generated link confirmation;

— occupation and management of subchannels;

— subchannel return or reallocation.

Firstly, the UA and the controller each create a map of the available subchannels. The controller selects one of the subchannels available together and the controller transfers the selected subchannel number to the other unit. This process can be performed by the CC DLL as well as SC DLL.

After that, the UA and the controller attempt to allocate subchannel at the same time. Subchannel can be allocated only when the UA and the controller succeed in allocation at the same time. Therefore, it is necessary to confirm whether a link is formed.

If the subchannel allocation is successful, the UA and the controller simultaneously perform slot clearing to occupy the subchannel. While occupying a subchannel, the UA and the controller constantly check for collisions of subchannel resources. They also calculate the amount of interference from neighboring channels.

If collision of subchannel resources or interference with neighbouring channels exceeding the threshold is detected, the UA and the controller reallocate the subchannel. To do this, the UA and the controller decide which subchannels to reallocate and perform allocation competition on that subchannel.

The UA and the controller return the subchannel when they can no longer maintain or need to maintain them.

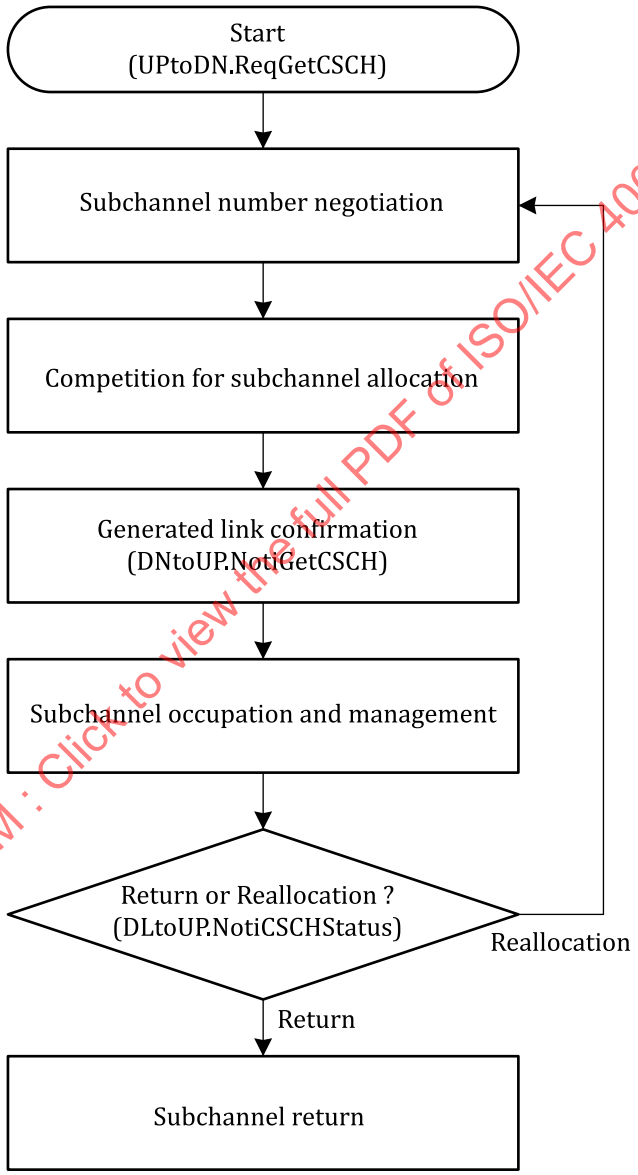


Figure 10 — Subchannel use procedure

NOTE Detecting resource collision satisfies the data link design requirement described in ISO 21384-2[1] that the design of the data link mitigates co-channel interference with other users of the spectrum.

6.2 Channel mapping and measurements

6.2.1 General

Allocating subchannel resources is performed by a tone channel. One subslot set in a tone channel and one subchannel have a mapping relationship. When one tone subslot set is allocated, the subchannel mapped thereto is allocated.

In order for a UA and a controller to allocate a subchannel, the UA and the controller shall find subchannels that can be allocated at the same time. To this end, the UA and the controller determine allocable subchannels by calculating the interference power for each subchannel.

6.2.2 Mapping of communication resources and subslot sets

The competition for allocating a subchannel or an IWR is performed in the subslot set mapped thereto. Subslot sets are mapped to subchannels or IWRs.

If the upper layer does not specify IWRs, the tone subslot set 0 to the tone subslot set 19 are left empty. When the IWRs are specified, the tone subslot sets are mapped as follows.

The tone subslot sets $\{S_0\}$, $\{S_1\}$, $\{S_2\}$, and $\{S_3\}$ are mapped to $IR_{0,0}$, $IR_{1,0}$, $IR_{2,0}$, and $IR_{3,0}$ respectively.

The tone subslot sets $\{S_4\}$, $\{S_5\}$, $\{S_6\}$, and $\{S_7\}$ are mapped to $IR_{0,1}$, $IR_{1,1}$, $IR_{2,1}$, and $IR_{3,1}$ respectively.

The tone subslot sets $\{S_8\}$, $\{S_9\}$, $\{S_{10}\}$, and $\{S_{11}\}$ are mapped to $IR_{0,2}$, $IR_{1,2}$, $IR_{2,2}$, and $IR_{3,2}$ respectively.

The tone subslot sets $\{S_{12}\}$, $\{S_{13}\}$, $\{S_{14}\}$, and $\{S_{15}\}$ are mapped to $IR_{0,3}$, $IR_{1,3}$, $IR_{2,3}$, and $IR_{3,3}$ respectively.

The tone subslot sets $\{S_{16}\}$, $\{S_{17}\}$, $\{S_{18}\}$, and $\{S_{19}\}$ are mapped to $IR_{0,4}$, $IR_{1,4}$, $IR_{2,4}$, and $IR_{3,4}$ respectively.

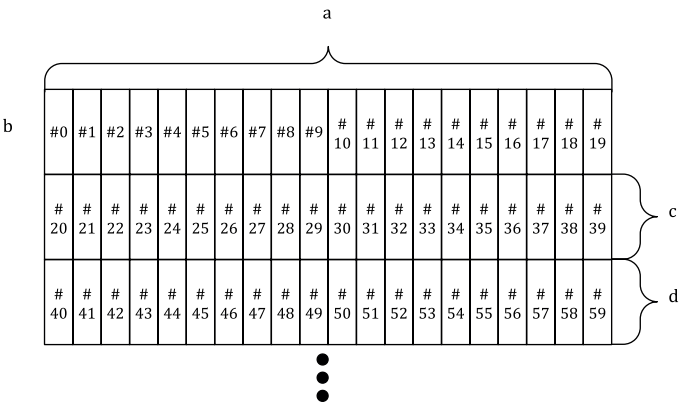
The tone subslot set $\{S_{m+20+n}\}$ is mapped to the subchannel $CCH_{x,y}$, where m is $20x+((y+8) \ mod \ 20)$ and n is as follows.

$$n = \begin{cases} 0, & even frame \\ 20-(x \bmod 2)\times 40, & odd \ frame \end{cases} \tag{5}$$

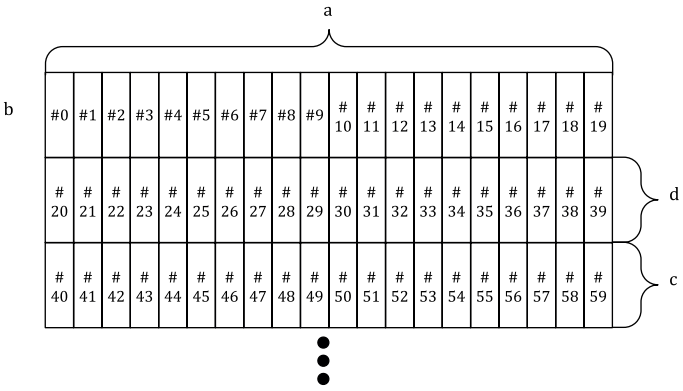
Thereafter, $\{S_{m+20+n}\}$ mapped to $CCH_{x,y}$ is expressed as $\{S_{x,y}\}$.

As mentioned above, the four subchannels of frequency channel N_IWR, $CCH_{\text{N\_IWR},16}$, $CCH_{\text{N\_IWR},17}$, $CCH_{\text{N\_IWR},18}$, $CCH_{\text{N\_IWR},19}$ are newly renamed as $IWRCH_0$, $IWRCH_1$, $IWRCH_2$, $IWRCH_3$. Therefore, the tone subslot sets mapped with these four subchannels are not used. The upper layer can designate these tone subslot sets as information tone subslot sets. The slot block type of the tone subslot sets from $\{S_0\}$ to $\{S_{19}\}$ is TSBtype2.

This mapping is shown in Figure 11.



a) Even frame



b) Odd frame

a $IR_{0,0}$, $IR_{1,0}$, $IR_{2,0}$, $IR_{3,0}$, $IR_{0,1}$, $IR_{1,1}$, …, $IR_{2,4}$, $IR_{3,4}$

b Tone subslot set.

c $CCH_{0,12}$, $CCH_{0,13}$, … $CCH_{0,11}$

d $CCH_{1,12}$, $CCH_{1,13}$, … $CCH_{1,11}$

Figure 11 — Mapping of control subchannel (CSCH) and tone subslot sets

6.2.3 Interference power calculation

In order to allocate the CSCH, the unit shall calculate the interference power in the allocable subchannels. The interference constants for calculating the interference power are N, IC_1, IC_2, …, IC_{N-1} and received as UPtoDL.InfoICConstant from the upper layer. Where N is the number of CCH channels. The unit of interference constants is dB. The estimated interference power of the subchannel is expressed as $PImCCH_{xy}$.

The interference of the subchannel CCH_{xy} experienced by the controller is calculated as follows.

$$P\,\mathrm{Im}c\,CCH_{x,y} = \sum_{i=0,i\neq x}^{N-1} (PmdCCH_{i,y} - IC_{|x-i|}) \tag{6}$$

where $PImdCCH_{i,y}$ is the reception power of the tone transmitted by the UA in the tone subslot set mapped with $CCH_{i,y}$, and the unit of this is dBm. The unit of ($PImdCCH_{i,y}$-$IC_{|x-i|}$) is also dBm.

The interference of the subchannel CCH_{xy} experienced by the UA is calculated as follows.

$$P\,\mathrm{Im}dCCH_{x,y} = \sum_{i=0,i\neq x}^{N-1} (PmcCCH_{i,y} - IC_{|x-i|}) \tag{7}$$

where $PImcCCH_{i,y}$ is the reception power of the tone transmitted by the controller in the tone subslot set mapped with $CCH_{i,y}$.

IWRs exist in four subchannels of frequency channel N_IWR, $CCH_{\mathrm{N\_IWR},16}$, $CCH_{\mathrm{N\_IWR},17}$, $CCH_{\mathrm{N\_IWR},18}$ and $CCH_{\mathrm{N\_IWR},19}$. Therefore, the interference power of the IWR is equal to the interference power of $CCH_{\mathrm{N\_IWR},16}$, $CCH_{\mathrm{N\_IWR},17}$, $CCH_{\mathrm{N\_IWR},18}$ and $CCH_{\mathrm{N\_IWR},19}$. $PImcIR_{i,y}$ is the interference power of the IWR in controller and $PImdIR_{i,y}$ is the interference power of the IWR in UA.

$$\begin{aligned} PImcIR_{i,y} &= PImcCCH_{N\_IWR,16+y} \\ PImdIR_{i,y} &= PImdCCH_{N\_IWR,16+y} \end{aligned} \tag{8}$$

6.2.4 Subchannel map

Each unit shall make a subchannel map indicating the availability of subchannels. The subchannel map is expressed in 2 bits per subchannel. If the subchannel interference $PImCCH_{x,y}$ is equal to or less than PTH_SMI0, 2 bits are '11'. If it is greater than PTH_SMI0 and less than PTH_SMI1, 2 bits are '10'. If it is greater than PTH_SMI1 and less than PTH_SMI2, 2 bits are '01'. And if it is greater than PTH_SMI12, 2 bits are '00', where PTH_SMI0, PTH_SMI1, and PTH_SMI2 are threshold values for writing a subchannel map and are received as UPtoDL.InfoPowerParamCCH from an upper layer. In addition, the upper layer can designate available subchannels as UPtoDL.InfoApprovedSubchMap and subchannels that cannot be used are written as '00'.

A UA that has allocated a control channel shall broadcast its own location, controller location, and transmission power through the SC using a 0x86 parsing header, where '0x' means hex notation and each unit shall receive an SC signal transmitted by other units.

Each unit can know the currently occupied subchannels from the SC signal, and if the distance to the UA or the controller occupying the subchannels is greater than d_map1, subchannels whose transmission power is less than PTXmap0 are expressed as '10', and subchannels above PTXmap0 and below PTXmap1 are expressed as '01', and subchannels above PTXmap1 are expressed as '00'. If the distance to the UA or the controller occupying the subchannels is greater than d_map0 and less than or equal to d_map1, subchannels with transmission power less than PTXmap2 are expressed as '10', and subchannels greater than PTXmap2 and smaller than PTXmap3 are expressed as '01' and subchannels greater than or equal to PTXmap3 are expressed as '00', where PTXmap0, PTXmap1, PTXmap2, PTXmap3, d_map0 and d_map1 are threshold values for subchannel map creation, and are received as UPtoDL.InfoPowerParamCCH from an upper layer.

As a result of receiving the tone signal of a tone subslot set, if the received power is greater than PTH_TONE, i.e. if the subchannel is occupied, the subchannel is expressed as '00'. In addition, if there is no information on the subchannel, it is expressed as '00'. In addition, the subchannels, $CCH_{N\_IWR,16}$, $CCH_{N\_IWR,17}$, $CCH_{N\_IWR,18}$ and $CCH_{N\_IWR,19}$ are always expressed as '00'. The number of bits of the subchannel map is $40N$. N is the number of CCH channels. The upper layer can transmit a subchannel map in one packet or divided into several packets and it is also possible to transmit through a SC broadcast slot.

When creating a subchannel map, a UA can create a subchannel map with '00' for subchannels in which transmission overlaps with a shared slot currently occupied by itself and the tone subslot set mapped thereto. Among the 20 subchannels existing in one control channel, 6 subchannels correspond to this. The upper layer can request this by using SCmake00 of the UPtoDL.InfoMapOption interface.

6.3 Subchannel negotiation for allocation

6.3.1 General

The upper layer can determine in advance a CSCH to be allocated and transfer it to the data link. In this case, UPtoDL.ReqAllocatingDedicatedCSCH or UPtoDL.ReqUsingDedicatedCSCH is used. When a subchannel to be allocated is not determined, a UA and a controller shall first negotiate which subchannel to allocate before allocating a subchannel as shown in Figure 12. In this case, UPtoDL.ReqGetCSCH is used.

a) For subchannel negotiation, the controller first requests the UA to transmit a subchannel map with PB 0x02.

b) When the UA receives this request, it transmits its own subchannel map to the controller using PB 0x03.

c) After receiving the UA's subchannel map, the controller selects one of the allocable subchannels. Then, it requests the UA to allocate the selected subchannel using PB 0x04.

d) If the subchannel requested for allocation is allocable, the UA transmits an ACK using PB 0x05 and goes to the subchannel allocation stage. If it is not allocable, it transmits its own subchannel map again with NACK.

e) When the controller receives an ACK, the controller goes to the subchannel allocation stage or receiving the NACK, the controller performs c) again. If all ACK/NACK is not received, the controller performs a) again or report a failure to the upper layer.

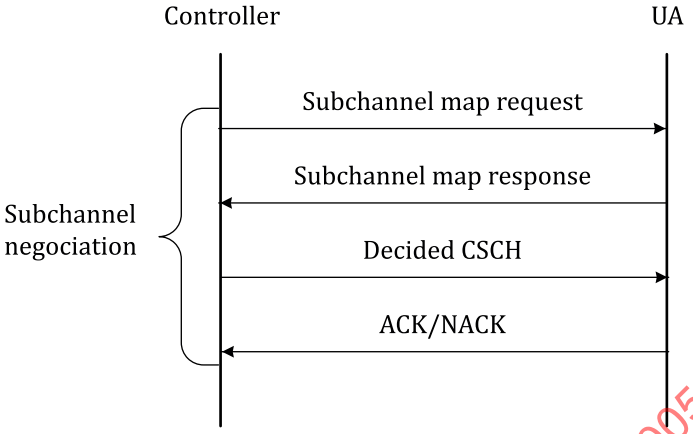


Figure 12 — General subchannel map negotiation procedure

When the UA is transmitting its own subchannel map using PB 0x87 in the shared channel, and the controller can receive this, it is possible that the controller does not request the UA to transmit the subchannel map as shown in Figure 13. The procedure in this case is as follows.

a) The controller selects one subchannel from among allocable subchannels using the received subchannel map of the UA. Then, it requests the UA to allocate the selected subchannel using PB 0x04.

b) If the subchannel requested for allocation is allocable, the UA transmits an ACK using PB 0x05 and goes to the subchannel allocation stage. If it is not allocable, it transmits its own subchannel map again with NACK.

c) When the controller receives an ACK, the controller goes to the subchannel allocation stage. If NACK is received or not all ACK/NACK is received, a) is performed again or a failure is reported to the upper layer.

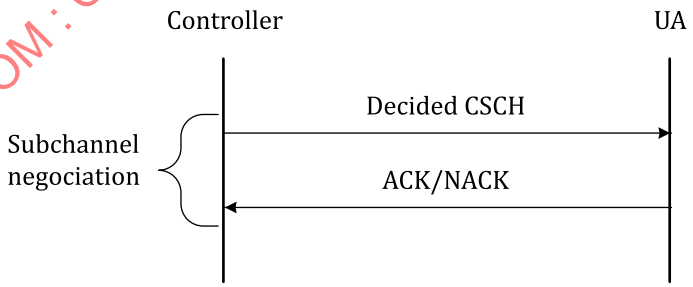


Figure 13 — Subchannel map negotiation procedure when subchannel map is broadcast

When the UA and the controller negotiate a subchannel number, they perform subchannel negotiation using shared communication or a dedicated slot or IWR. Transmission power control related to subchannel negotiation is performed using PB 0x06 and PB 0x07. PB 0x06 represents its own transmission power and reception power of the counterpart's signal, and PB 0x07 represents its own transmission power and designates the power to be transmitted by the counterpart.

6.3.1.1 Generation of effective subchannel map

The controller receives the subchannel map from the UA and generate an effective subchannel map. The effective subchannel map is generated by selecting a lower value from the controller subchannel map and the UA subchannel map.

6.3.1.2 Parsing block of shared channel related to subchannel allocation

The UA can broadcast its subchannel map using PB 0x87 in the slot of the shared channel. The parsing field of PB 0x87 is shown in Table 1.

Table 1 — Parsing field of 0x87

Bits	Description
[0:4]	Starting channel number
[5:9]	Map length that indicates [5:9]*40.
[10:[5:9]*40+9]	Variable subchannel map
[*x*:*y*] means from the *x*-th bit to the *y*-th bit of the related field.	

6.3.1.3 Parsing block of control channel related to subchannel allocation

The parsing blocks used in the control channel are 0x02, 0x03, 0x04, 0x05, 0x06, 0x07. PB 0x02 has no parsing field. The parsing field of PB 0x03 is shown in Table 2.

Table 2 — Parsing field of 0x03

Bits	Description
[0:4]	Starting channel number
[5:9]	Map length is [5:9]*40.
[10:[5:9]*40+9]	Variable subchannel map

The parsing field of PB 0x04 is shown in Table 3.

Table 3 — Parsing field of 0x04

Bits	Description
[0:4]	Channel number
[5:9]	Subchannel number

The parsing field of PB 0x05 is shown in Table 4 and Table 5.

Table 4 — Parsing field of 0x05 with ACK

Bits	Description
[0]	This bit is '1' and means ACK.

Table 5 — Parsing field of 0x05 with NACK

Bits	Description
[0]	This bit is '0' and means NACK.
[1:5]	Starting channel number
[6:10]	Map length is [6:10]*40.
[11:[6:10]*40+10]	Variable subchannel map

The parsing field of PB 0x06 is shown in Table 6.

Table 6 — Parsing field of 0x06

Bits	Description
[0:6]	Own transmit power with the range of -40 dBm(0) ~ 40 dBm(80)
[7:13]	Received power of counterpart signal with the range of -115 dBm(1) ~ -10dBm(106), 0xFF means 'unknown' and 0x00 means smaller than -115dBm.

The parsing field of PB 0x03 is shown in Table 7.

Table 7 — Parsing field of 0x07

Bits	Description
[0:6]	Own transmit power with the range of -40 dBm(0) ~ 40dBm(80)
[7:13]	Required transmit power of counterpart, the range is same with [0:6].

6.3.1.4 Subchannel selection for allocation

The data link of the controller generates an effective subchannel map using the subchannel map transmitted by the UA and its own subchannel map. When the UA transmits only a part of the subchannel map, all values that are not transmitted are regarded as a value of '00'. The effective subchannel map is achieved by selecting a lower value from the two subchannel maps, i.e. if one of the two values is '00', regardless of the other value, the bit of the corresponding subchannel is '00'. The data link of the controller determines one subchannel for allocation from the effective subchannel map. If there is no valid subchannel, it is reported to the upper layer.

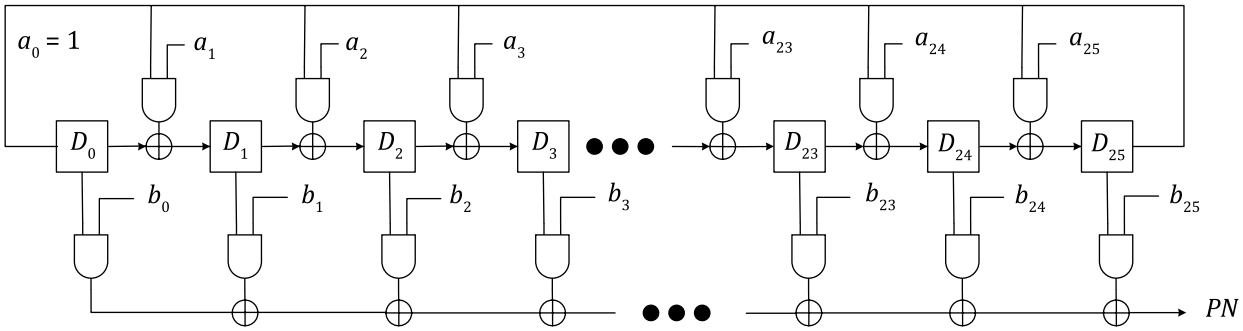
If there are subchannels having a value of '11', the controller shall select one of the subchannels.

If there are no subchannels having a value of '11' the controller can select one subchannel from among the subchannels having a value of '10' only when the value of SubChannelAbility10 of the UPtoDL. InfoMapOption interface is set to 1.

If there are no subchannels having a value of '11' or '10', the controller can select subchannel from among subchannels having a value of '01' only when the value of SubChannelAbility01 is set to 1.

If the number of selectable subchannels is $NUM_{selectable\_subch}$, the controller calculates the *Nordinal*-th usable subchannel from the effective subchannel map using a PN code generator. The order from the zeroth subchannel to the ($NUM_{selectable\_subch}$ -1)-th subchannel is determined by the following rules.

The smaller the x value in the subchannel $CCH_{x,y}$, the faster the order. And when the x values are the same, the smaller the y value, the faster the order.



Key

a_k a k-th bit for AND operation with D_{25}
b_k a k-th bit for AND operation with D_k
D_k a k-th register
PN PN code generator output

Figure 14 — PN code generator

The *Nordinal* is calculated with PN code generator shown in Figure 14 as follows, where $[x_{i-1}, x_{i-2}, ..., x_0]$ is the i-bit binary representation of x.

$$
\begin{aligned}
&[D_{25}(0), D_{24}(0), \ldots, D_0(0)] = [SA_{25}, SA_{24}, \ldots, SA_0] \\
&[b_{25}, b_{24}, \ldots, b_{17}] = [SA_8, SA_7, \ldots, SA_0] \\
&[b_{16}, b_{15}, \ldots, b_{11}] = [f_5, f_4, \ldots, f_0] \\
&[b_{10}, b_9, \ldots, b_0] = [M_5, M_4, M_3, M_2, M_1, M_0, H_4, H_3, H_2, H_1, H_0] \\
&[a_{25}, a_{24}, \ldots, a_0] = [SA_0, SA_1, \ldots, SA_{24}, 1] \\
&PN(clk) = (D_0(clk) \,\&\, b_0)(D_1(clk) \,\&\, b_1) \wedge \ldots \wedge (D_{25}(clk) \,\&\, b_{25}) \\
&N_{PN} = [PN(15), PN(14), \ldots, PN(1), PN(0)] \\
&Nordinal = floor((N_{PN} \times NUM_{selectable\_subch}) / 2^{16})
\end{aligned}
\tag{9}
$$

where

$D_x(clk)$ is a x-th bit of shift register D at clock clk;

SA_x is a x-th bit of source address, the number of SA bits is greater than or equal 26;

f_x is a x-th bit of frame number, the number of f bits is 6;

M_x is a x-th bit of minute, the number of M bits is 6;

H_x is a x-th bit of hour for 24-hour clock, the number of H bits is 5 and H has the value from 0 to 23;

$PN(clk)$ is a pseudo random bit of PN code generator at clock clk;

& is AND bit operation that means a logical multiplication;

^ is exclusive OR bit operation that means exclusive logical sum operation;

$floor(x)$ means the largest integer among integers smaller than or equal to x.

6.3.2 Subchannel negotiation using shared channel

6.3.2.1 General

UAs and controllers can perform subchannel negotiation using shared channels. To do this, the controller shall allocate a talk slot of a shared channel to communicate with the UA. Allocating a talk slot in a shared channel shall follow the scheme described in ISO/IEC 4005-2. When transmitting and receiving data related to the control channel in the shared channel, PKH 0x04 and PKH 0x05 are used. When two PKHs are used, the PBs from 0x00 to 0x7F mean the PBs of the control channel. CC DLL receives UPtoDL.ReqGetCSCH from the upper layer. At this time, if the NegoMethod parameter is '0', CCtoSC. ReqNegoCSCH, which is a subchannel negotiation request, is transmitted to SC DLL. Upon receiving this, the SC DLL shall perform subchannel negotiation. When the subchannel negotiation is over, the SC DLL delivers SCtoCC.NotiNegoCSCH to the CC DLL. If the subchannel negotiation is successful, the CC DLL enters the subchannel negotiation stage, and if the subchannel negotiation fails, the CC DLL notifies the upper layer of the failure with DLtoUP.NotiGetCSCH.

The controller's SC DLL performs subchannel negotiation as follows. However, when the UA broadcasts the subchannel map using PB 0x87, steps b) and c) can be omitted.

a) SC DLL receives the CCtoSC.ReqNegoCSCH requesting subchannel allocation from CC DLL. At this time, *m* and *n* are set. *m* and *n* can have negative values.

b) SC DLL requests the UA to transmit the UA subchannel map. For this, the controller shall transmit a request packet by allocating the talk slot of the SC. The PKH of the SC used here is 0x05, and the subchannel map transmission request PB is 0x02, where the controller SC DLL can use PB 0x81 to utilize the SC broadcast slot of UA for subchannel negotiation. If talk slot allocation and transmission fails, *m* is increased.

c) The SC DLL repeats b), increasing *m* until it receives PB 0x03. If PB 0x03 is not received and *m* is greater than 3, the SC DLL reports it to the CC DLL using SCtoCC.NotiNegoCSCH and performs d) when the subchannel map is received, where the controller can receive the subchannel map through the response slot related to the allocated talk slot or the currently occupied broadcast slot of the UA.

d) After receiving the UA's subchannel map, the SC DLL generates an effective subchannel map and selects one subchannel from the effective subchannel map.

e) After allocating the talk slot, the SC DLL transmits the allocation request for the selected subchannel to the UA using PB 0x04. If talk slot allocation and transmission fails, *n* is increased.

f) When SC DLL receives ACK from PB 0x05, it notifies CC DLL to SCtoCC.NotiNegoCSCH. Upon receiving the NACK, d) is performed again. If PB 0x05 is not received, *n* is increased, and if *n* is greater than 3, it is reported to the CC DLL as SCtoCC.NotiNegoCSCH, and if it is less than or equal to 3, d) is performed again, where,the controller receives ACK/NACK through a response slot related to the allocated talk slot or a currently occupied broadcast slot of the UA.

Figure 15 shows controller's subchannel negotiation procedure using SC.

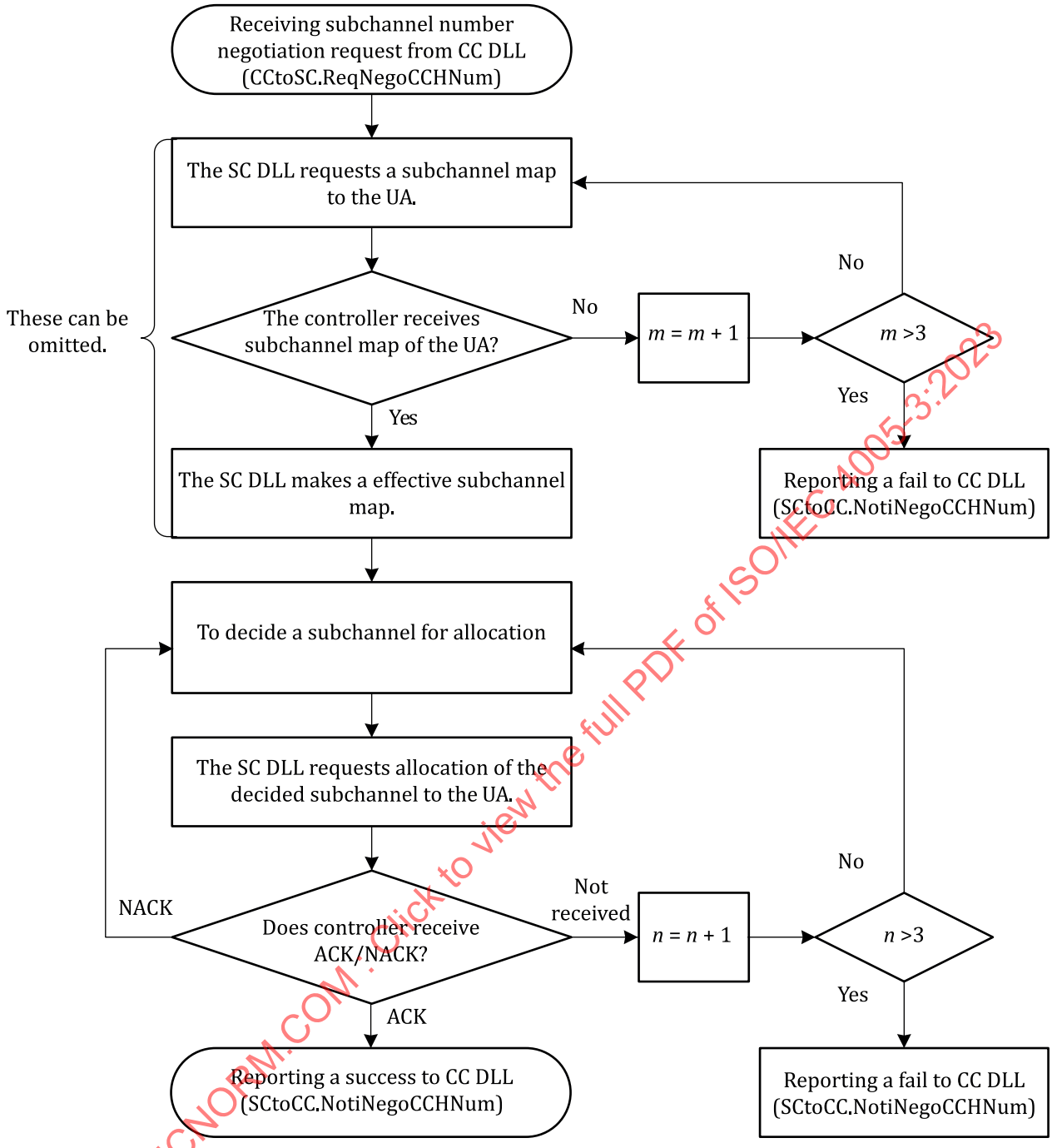


Figure 15 — Controller's subchannel negotiation procedure using SC

The UA's SC DLL shall respond to the controller's request for subchannel negotiation. First, when a subchannel map request is received by PB 0x02, the UA's SC DLL shall transmit its subchannel map to the controller using PB 0x03. When a UA transmits a subchannel map, it shall transmit a subchannel map of a length that can be transmitted.

The UA's SC DLL receives a subchannel allocation request by PB 0x04, and if the subchannel is available for allocation, transmits an ACK to the controller using PB 0x05, and informs the CC DLL of the ACK transmission through SCtoCC.NotiNegoCSCH. If the subchannel cannot be allocated, it transmits NACK and its own subchannel map to the controller. After UA's CC DLL receives SCtoCC.NotiNegoCSCH, if the parameter IsSuccess is 1, it enters the subchannel allocation stage.

If PB 0x81 is included in the packet sent by the controller and the parsing field RequestMethod has a value of '0', the UA responds with the SC broadcast slot it has already occupied. If the parsing field RequestMethod has a value of '1', the UA responds with the SC broadcast slot it has already occupied, and simultaneously performs response clearing and allocation competition, and responds with a talk slot allocated by the controller. If PB 0x81 is not included in the controller's packet, response clearing and allocation competition are performed to respond with a talk slot allocated by the controller.

When responding to the SC broadcast slot, the control channel parsing block is transmitted using PB 0x8B. The parsing field of the parsing block 0x8B carries the control parsing block. When responding with an SC talk slot, PKH 0x05 is used.

6.3.2.2 Transmission power in subchannel negotiation

When the controller and UA perform subchannel negotiation with the SC, they use the transmit power specified in the SC.

6.3.3 Subchannel negotiation using dedicated slot

6.3.3.1 General

The upper layer can determine one or more CSCHs as dedicated subchannels, and slots constituting the dedicated subchannel can be dedicated as control dedicated slots. The data link receives corresponding information from the upper layer through UPtoDL.InfoDedicatedSlot.

In order for the controller and the UA to negotiate a subchannel using a dedicated slot, the following conditions shall be satisfied.

a) The controller and the UA shall know each other about the pre-allocated dedicated slot information.

b) The controller and UA shall always receive when the dedicated slot is not transmitted.

The UA and the controller can perform CSCH negotiation using a predetermined dedicated slot. The procedure for the controller to perform subchannel negotiation is as follows.

a) The CC DLL of the controller receives the subchannel allocation command UPtoDL.ReqGetCSCH from the upper layer. At this time, NegoMethod is '1', and *m* and *n* are set.

b) The controller requests the UA to transmit the UA subchannel map using PB 0x02. For this, the controller uses a dedicated slot.

c) The controller repeats b) while increasing *m* until it receives the UA subchannel map through PB 0x03. If the subchannel map is not received and *m* is greater than 3, the data link reports a failure to the upper layer with DLtoUP.NotiGetCSCH, and performs d) when the subchannel map is received. Where, the controller receives the subchannel map in a dedicated slot next to the dedicated slot used in b).

d) After receiving the UA's subchannel map, the controller generates an effective subchannel map and selects one subchannel from the effective subchannel map.

e) The controller transmits the allocation request for the selected subchannel to the UA using PB 0x04.

f) When the controller receives an ACK from the UA, it goes to the subchannel allocation stage. Upon receiving the NACK, d) is performed again. If all ACK/NACK are not received, *n* is increased, and if *n* is greater than 3, the failure is reported to the upper layer with DLtoUP.NotiGetCSCH, and if less than or equal to 3, d) is performed again. Here, the controller receives ACK/NACK in a dedicated slot next to the dedicated slot used in e).

The UA continuously receives its dedicated slots according to the settings of the upper layer. When a UA receives a packet requiring a response from the controller, it shall transmit a response in a dedicated slot next to the dedicated slot in which the request was received.

When receiving a subchannel map request PB 0x02 in a dedicated slot, the UA's CC DLL shall transmit its subchannel map to the controller in a dedicated slot next to the dedicated slot in which the request was received.

The UA responds with PB 0x05 after receiving the subchannel allocation request PB 0x04. At this time, if the subchannel is available for allocation, an ACK is transmitted to the controller and the UA enters the subchannel allocation stage. If the subchannel cannot be allocated, it transmits NACK and its own subchannel map to the controller.

6.3.3.2 Transmission power in subchannel negotiation

The maximum power of DS is PmaxDS and the minimum power is PminDS. When using the dedicated slot, the initial transmit power of the controller is as follows.

a) When SC signal is received from UA:

$$PTX\_CO\_DS\_ini = MIN((PtargetDS + PL\_SCd + SNRrequiredDS + PmarginDS), PmaxDS) \quad (10)$$

where

PtargetDS is the target receiving power of the dedicated slot;

PL_SCd is the path loss measured from the SC signal received by the controller;

SNRrequiredDS is the SNR required to receive the dedicated slot;

PmarginDS is the power margin for the dedicated slot;

MIN means a minimum value among elements.

PtargetDS, SNRrequiredDS, PmarginDS, PmaxDS values are received from the upper layer as UPtoDN. InfoPowerParamDS.

b) In case SC signal is not received from UA:

$$PTX\_CO\_DS\_ini = PmaxDS \quad (11)$$

When using a dedicated slot, the controller shall transmit its own transmit power and the UA's transmit power to the UA using PB 0x07.

The initial transmit power *PTX_DR_DS_ini* of the UA designated by the controller is determined by adding the PoffCtoD value received from the upper UPtoDL.InfoPowerParamCCH to the controller transmission power.

$$PTX\_DR\_DS\_ini = MIN((PTX\_CO\_DS\_ini + PoffCtoD), PmaxDS) \quad (12)$$

When the UA receives PB 0x07, it responds with the designated transmit power. At this time, it is necessary to use PB 0x06 to deliver its own transmit power and receive power of controller signals.

The power control of the UA and controller after initial transmission is as follows.

Upon receiving the PB 0x06, the controller transmits PB 0x06 to the UA and adjusts its own transmit power as follows.

$$PTX\_CO\_DS = MIN((PtargetDS + PL\_DS\_CtoD + SNRrequiredDS + PmarginDS), PmaxDS) \quad (13)$$

where *PL_DS_CtoD* is the path loss of the dedicated slot signal transmitted by the controller to the UA.

The controller that has not received PB 0x06 adjusts the transmit power in the next dedicated slot as follows.

$$PTX\_CO\_DS = MIN((PTX\_CO\_DS\_prev + 3), PmaxDS) \quad (14)$$

where *PTX_CO_DS_prev* is the controller transmit power in the previously dedicated slot. The controller that does not receive PB 0x06 transmits PB 0x07 to the UA. At this time, the UA's transmit power *PTX_DR_DS* designated by the controller is as follows, where *PTX_DR_DS_prev* is the UA transmission power in the previous dedicated slot.

$$PTX\_DR\_DS = MIN((PTX\_DR\_DS\_prev + 3), PmaxDS) \quad (15)$$

When the UA receives PB 0x07, it responds with the designated transmit power. At this time, it is necessary to use PB 0x06 to deliver its own transmit power and receive power of controller signals.

Upon receiving PB 0x06, the UA adjusts its own transmit power as follows, where *PL_DS_DtoC* is the path loss of the dedicated slot signal transmitted by the UA to the controller.

$$PTX\_DR\_DS = MIN((PtargetDS + PL\_DS\_CtoD + SNRrequiredDS + PmarginDS), PmaxDS) \quad (16)$$

Also, when dedicated slots are used for purposes other than subchannel negotiation, the transmission power control of the controller and UA is as described above.

6.3.4 Subchannel negotiation using IWR

6.3.4.1 General

When a shared channel or dedicated slot is available, it is not recommended to use IWR.

In order to use $IR_{i,y}$ for subchannel negotiation, the controller allocates one $IR_{i,y}$.

The controller uses the allocated IWR slot to perform subchannel negotiation. First, the controller transmits PB 0x02 through the allocated IWR slot. When the UA receives this, the UA checks whether there is a collision of IWR resources from its point of view. If no collision has occurred, the UA performs subchannel negotiation. In the case of a collision, the UA does not perform subchannel negotiation, and informs the controller by transmitting PB 0x08 in the next IWR slot. When the controller receives PB 0x08 from the UA, it does not perform subchannel negotiation and shall allocate IWR resources again.

The procedure for the controller to perform subchannel negotiation is as follows.

a) When the upper layer receives the subchannel allocation request UPtoDL.ReqGetCSCH whose NegoMethod is '2', the DLL first allocates IWR. At this time, *l* is automatically set to 5, *m* to 2, and *n* to 1. If IWR allocation fails more than *l* times, the failure is reported to the upper layer as DLtoUP. NotiGetCSCH.

b) The controller requests the UA to transmit the UA subchannel map. This request is made using the allocated IWR slot.

c) The controller repeats b) while increasing *m* until it receives the UA subchannel map. If the subchannel map is not received and *m* is greater than 3, the data link reports a failure to the upper layer with DLtoUP.NotiGetCSCH, and d) is performed when the subchannel map is received. If PB

0x08 is received from the UA, a) is performed again, where the controller receives the subchannel map in the next IWR allocation slot of the IWR allocation slot used in b).

d) After receiving the UA's subchannel map, the controller generates an effective subchannel map and selects one subchannel from the effective subchannel map.

e) The controller transmits an allocation request for the selected subchannel to the UA.

f) When the controller receives an ACK, it goes to the subchannel allocation stage. If NACK is received or if both ACK and NACK are not received, the DLL increments *n*. At this time, if *n* is greater than 3, the DLL reports the failure to the upper layer with DLtoUP.NotiGetCSCH, and if it is less than or equal to 3, d) is executed again, where the controller receives ACK/NACK in the next IWR allocation slot of the IWR allocation slot used in e).

The procedure for the UA to perform subchannel negotiation is as follows.

First, if the RxOn parameter of the upper layer UPtoDL.InfoIWRSlot interface is 1, the UA continuously receives corresponding IWR slots. In addition, the UA shall respond to the controller's request when negotiating a subchannel.

When a subchannel map request is received in a slot of an IWR, the UA shall transmit its subchannel map to the controller in the next IWR slot of the IWR slot that received the request.

After the UA receives the subchannel allocation request, if the subchannel is available for allocation, it transmits an ACK to the controller and enters the subchannel allocation stage. If the subchannel cannot be allocated, it transmits NACK and its own subchannel map to the controller. The UA shall transmit ACK/NACK to the controller in the next IWR slot of the IWR slot that received the request.

6.3.4.2 IWR selection and IWR allocation and occupation

In order to allocate IWRs, the controller selects three IWRs to attempt to allocate, and tries to allocate from the selected IWRs. The tone subslot set to which the allocation is made are shown in 6.2.1.

The three IWRs are calculated with PN code generator shown in Figure 14 as follows.

$$
\begin{aligned}
&[D_{25}(0), D_{24}(0), \ldots, D_0(0)] = [SA_{25}, SA_{24}, \ldots, SA_0] \\
&[b_{25}, b_{24}, \ldots, b_{17}] = [SA_8, SA_7, \ldots, SA_0] \\
&[b_{16}, b_{15}, \ldots, b_{11}] = [f_5, f_4, \ldots, f_0] \\
&[b_{10}, b_9, \ldots, b_0] = [M_5, M_4, M_3, M_2, M_1, M_0, H_4, H_3, H_2, H_1, H_0] \\
&[a_{25}, a_{24}, \ldots, a_0] = [SA_0, SA_1, \ldots, SA_{24}, 1] \\
&PN(clk) = (D_0(clk) \,\&\, b_0)(D_1(clk) \,\&\, b_1)\hat{}\ldots\hat{}(D_{25}(clk) \,\&\, b_{25}) \\
&Niwr0 = [PN(15), PN(14), \ldots, PN(0)] \\
&Niwr1 = [PN(31), PN(30), \ldots, PN(16)] \\
&Niwr\_try0 = floor((Niwr0 \times 4)/2^{16}) \\
&Niwr\_try1 = floor((Niwr1 \times 5)/2^{16})
\end{aligned}
\tag{17}
$$

where

$D_x(clk)$ is a *x*-th bit of shift register *D* at clock *clk*;

SA_x is a *x*-th bit of source address, the number of *SA* bits is greater than or equal 26;

f_x is a *x*-th bit of frame number, the number of *f* bits is 6;

M_x	is a *x*-th bit of minute, the number of *M* bits is 6;
H_x	is a *x*-th bit of hour for 24-hour clock, the number of *H* bits is 5 and *H* has the value from 0 to 23;
PN(*clk*)	is a pseudo random bit of PN code generator at clock clk;
&	is AND bit operation that means a logical multiplication;
^	is exclusive OR bit operation that means exclusive logical sum operation;
floor(*x*)	means the largest integer among integers smaller than or equal to *x*.

The three selected $IR_{i,y}$ are $IR_{Niwr\_try0,\ Niwr\_try1}$, $IR_{(Niwr\_try0+1)\ mod\ 4,\ (Niwr\_try1+1)\ mod\ 5}$, $IR_{(Niwr\_try0+2)\ mod4,\ (Niwr\_try1+2)\ mod\ 5}$. When allocating IWR, the controller tries to allocate sequentially from $IR_{Niwr\_try0,\ Niwr\_try1}$, and can make up to 3 attempts until the allocation is successful. If the allocation is successful, the controller stops the allocation.

The type of the slot block used for IWR allocation is TSBtype2, and competition for TSBtype2 is described in 6.4.1. IWR allocation competition is performed by the controller alone, the address used for the competition is UA's address, and SS_{start} is 1.

After allocating IWR, the controller can perform one slot clearing in the next frame. When the controller receives the PB 0x08 from the UA, slot clearing is not performed after that.

The UA shall receive tone subslot sets mapped with IWRs to determine which IWR is currently occupied. When the UA receives a signal from the related controller in an IWR, if the IWR is not occupied, the UA performs slot clearing once in the next frame. If the corresponding IWR is occupied, slot clearing is not performed in the next frame.

If the subchannel negotiation is finished in the first frame, neither the UA nor the controller performs slot clearing in the next frame.

6.3.4.3 Power control in subchannel negotiation

The maximum power of IWR is PmaxIWR and the minimum power is PminIWR. When using IWR, the initial transmit power of the controller is as follows.

a) When SC signal is received from the relative UA:

$$PTX\_CO\_IWR\_ini = MIN((PtargetIWR + PL\_SCd + SNRrequiredIWR + PmarginIWR), PmaxIWR) \quad (18)$$

where

PtargetIWR	is the target receiving power of IWR;
PL_SCd	is the path loss measured from the SC signal received by the controller;
SNRrequiredIWR	is the SNR required to receive the IWR slot;
PmarginIWR	is the power margin for the IWR slot.

PtargetIWR, SNRrequiredIWR, PmarginIWR, PmaxIWR are received from the upper layer as UPtoDN. InfoPowerParamIWR.

b) When SC signal is not received from the relative UA:

$$PTX\_CO\_IWR\_ini = PmaxIWR \quad (19)$$

where the controller shall transmit its own transmission power and the UA's initial transmission power to the UA using PB 0x07. The initial transmit power *PTX_DR_IWR_ini* of the UA designated by the controller is determined by adding the PoffCtoD value received from upper layer as UPtoDL. InfoPowerParamCCH to the controller transmission power.

$$PTX\_DR\_IWR\_ini = MIN(\ (PTX\_CO\_IWR\_ini + PoffCtoD), PmaxIWR) \tag{20}$$

When the UA receives PB 0x07, it responds with the designated transmit power. At this time, it is necessary to use PB 0x06 to deliver its own transmit power and receive power of controller signals.

The power control of the UA and controller after initial transmission is as follows.

Upon receiving PB 0x06, the controller transmits PB 0x06 to the UA and adjusts the transmit power as follows. Where, *PL_IWR_CtoD* is the path loss of the IWR slot signal sent by the controller to the UA.

$$PTX\_CO\_IWR = MIN((PtargetIWR + PL\_IWR\_CtoD + SNRrequiredIWR + PmarginIWR), PmaxIWR) \tag{21}$$

The controller that has not received PB 0x06 adjusts the transmit power in the next IWR slot as follows.

$$PTX\_CO\_IWR = MIN((PTX\_CO\_IWR\_prev + 3), PmaxIWR) \tag{22}$$

where *PTX_CO_IWR_prev* is the controller transmit power in the previous IWR slot. The controller that does not receive PB 0x06 transmits PB 0x07 to the UA. At this time, the transmit power *PTX_DR_IWR* of the UA designated by the controller is as follows, where *PTX_DR_IWR_prev* is the UA transmission power in the previous IWR slot.

$$PTX\_DR\_IWR = MIN((PTX\_DR\_IWR\_prev + 3), PmaxIWR) \tag{23}$$

When the UA receives PB 0x07, it responds with the designated transmit power. At this time, it is necessary to use PB 0x06 to deliver its own transmit power and receive power of the controller signal. In the case of receiving PB 0x06, it responds with PB 0x06 as well.

Upon receiving the 0x06 parsing block, the UA adjusts its own transmit power as follows.

$$PTX\_DR\_IWR = MIN((PtargetIWR + PL\_IWR\_CtoD + SNRrequiredIWR + PmarginIWR), PmaxIWR) \tag{24}$$

6.4 Resource allocation competition and generated link confirmation

6.4.1 General

When the subchannel negotiation is completed, each unit shall first perform allocation competition in the tone subslot set mapped with the corresponding subchannel. At this time, the UA and the controller compete at the same time in the same tone subslot set.

If the UA and the controller fail to allocate a resource, they report the failure to DLtoUP.NotiGetCSCH to the upper layer.

If the UA and the controller successfully allocate a resource, they perform a generated link confirmation for 2 sec. After transmitting and receiving packets for the first 1 sec and calculating the received packet error rate, if the received packet error rate is less than the LinkConfirmError of UPtoDL. InfoControlChannel, the packet is transmitted and received for the next 1 sec. Otherwise, it transmits PB 0x0C for the next 1 sec and then reports failure with DLtoUP.NotiGetCSCH to the upper layer.

In case that the packet is transmitted/received for the second 1 sec, if the received packet error rate is 100 % or PB 0x0C is detected in the received packet, the failure is reported as DLtoUP.NotiGetCSCH to

the upper layer. Otherwise, allocation success is reported as DLtoUP.NotiGetCSCH to the upper layer and the unit enters the occupation stage.

Figure 16 shows the procedure of resource allocation competition and generated link confirmation.

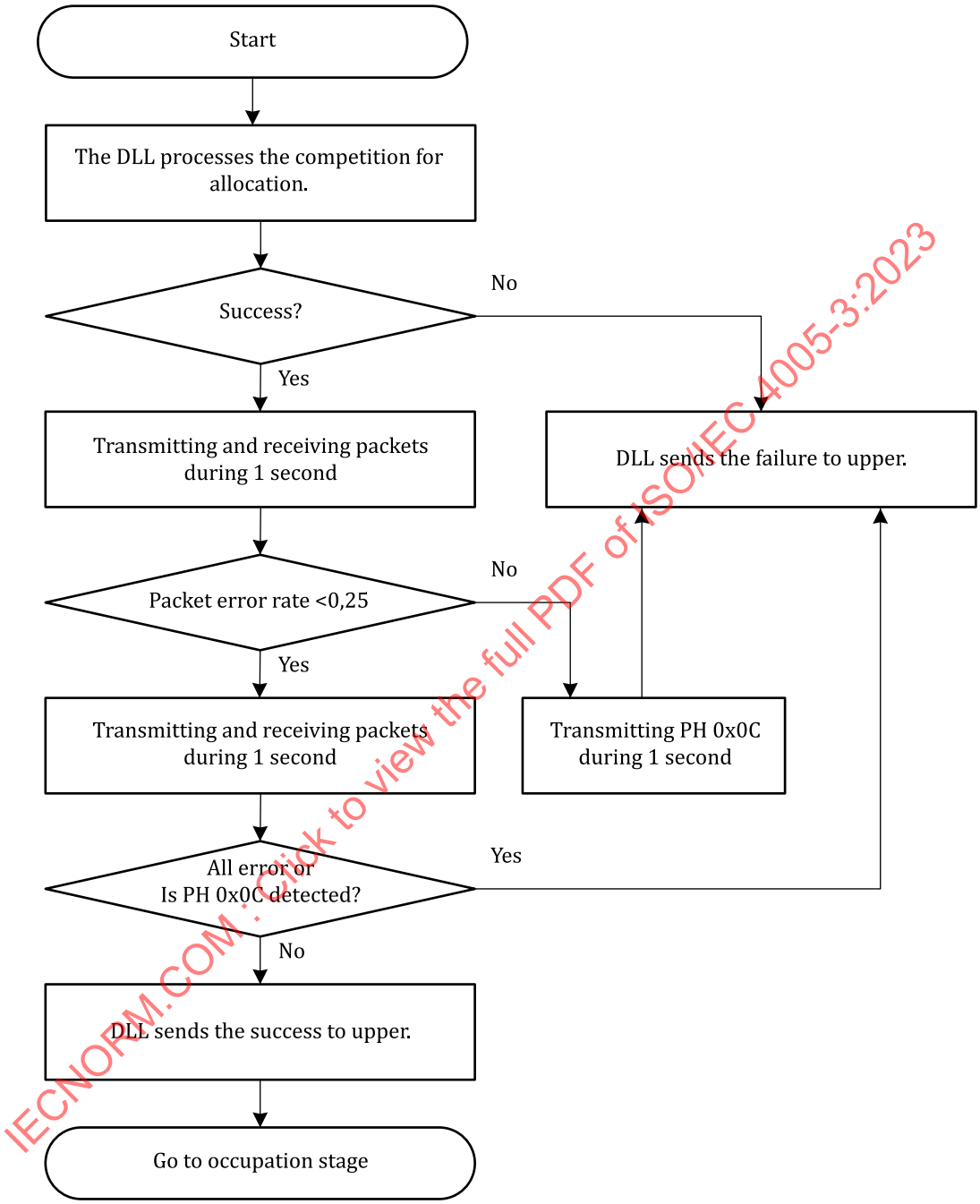


Figure 16 — Resource allocation competition and generated link confirmation

6.4.2 Subchannel resource allocation competition

6.4.2.1 General

In the case of subchannel resource allocation, the UA and the controller simultaneously compete for the subchannel promised to be allocated. At this time, the UA and the controller compete using the UA's source address. That is, the UA and the controller select the same first and second subslots.

The competition for allocating control channel is performed twice in the same subslot set $\{S_{x,y}\}$. These are the first competition and the second competition, where SS_z means the z-th tone subslot constituting $\{S_{x,y}\}$.

The first competition is performed as follows.

a) The first subslot, SS_{first} is selected among the subslots from SS_{start} to SS_{end}.

b) Carrier sensing is performed until before SS_{first}.

c) If the carrier sensing result is 'signal detection', it is determined that the competition is lost, where the reception power threshold value for determining tone detection is PRXtoneCompeteThre.

d) If the carrier sensing result is 'no signal detection', the tone signal transmission starts from the first subslot.

The second competition is performed only by the unit winning the first competition. If the first subslot number is SS_{end}, the second competition is not performed.

The second competition is performed as follows.

a) The second subslot, SS_{second} is selected among the subslots from the next subslot of SS_{first} to SS_{end}.

b) The unit performs carrier sensing instead transmitting a competition tone signal in the second subslot.

c) If the sensing result is 'signal detection', it is determined that the competition is lost and unit stops to transmit a competition tone signal.

d) If the sensing result is 'no signal detection', a competition tone signal is transmitted from the next subslot of SS_{second} to SS_{end}.

In case of TSBtype0, TSBtype1, TSBtype2, SS_{end} is 32, 19, 9, respectively. SS_{start} is 1.

The first subslot number and second subslot number are calculated with PN code generator shown in Figure 14 as follows.

$$[D_{25}(0), D_{24}(0), \ldots, D_0(0)] = [SA_{25}, SA_{24}, \ldots, SA_0]$$

$$[b_{25}, b_{24}, \ldots, b_{17}] = [SA_8, SA_7, \ldots, SA_0]$$

$$[b_{16}, b_{15}, \ldots, b_{11}] = [f_5, f_4, \ldots, f_0]$$

$$[b_{10}, b_9, \ldots, b_0] = [M_5, M_4, M_3, M_2, M_1, M_0, H_4, H_3, H_2, H_1, H_0]$$

$$[a_{25}, a_{24}, \ldots, a_0] = [SA_0, SA_1, \ldots, SA_{24}, 1]$$

$$PN(clk) = (D_0(clk) \,\&\, b_0)(D_1(clk) \,\&\, b_1)\text{^}\ldots\text{^}(D_{25}(clk) \,\&\, b_{25}) \quad (25)$$

$$N_{PN1} = [PN(12), PN(11), \ldots, PN(1), PN(0)]$$

$$N_{PN2} = [PN(25), PN(24), \ldots, PN(14), PN(13)]$$

$$SS_{first} = SS_{start} + floor((N_{PN1} \times (SS_{end} + 1 - SS_{start}))/2^{13})$$

$$SS_{second} = SS_{first} + 1 + floor((N_{PN2} \times (SS_{end} - SS_{first}))/2^{13})$$

where

$D_x(clk)$ is a x-th bit of shift register D at clock clk;

SA_x is a x-th bit of source address, the number of SA bits is greater than or equal 26;

s_x	is a x-th bit of subslot set number, the number of s bits is 9;
f_x	is a x-th bit of frame number, the number of f bits is 6;
M_x	is a x-th bit of minute, the number of M bits is 6;
H_x	is a x-th bit of hour for 24-hour clock, the number of H bits is 5 and H has the value from 0 to 23;
$PN(clk)$	is a pseudo random bit of PN code generator at clock clk;
&	is AND bit operation that means a logical multiplication;
^	is exclusive OR bit operation that means exclusive logical sum operation;
$floor(x)$	means the largest integer among integers smaller than or equal to x.

6.4.2.2 Tone subslot transmission power in subchannel allocation

When the controller and UA perform subchannel allocation, the transmit power of the tone subslot signal is calculated as follows.

First, when subchannel negotiation is performed with an SC signal, it is as follows.

$$PTX\_nego\_Tone = MIN((PtargetCCH + PL\_SC + SNRrequiredCCH + PmarginTCH), PmaxTCH) \quad (26)$$

where

PtargetCCH	is the target reception power of the CCH;
PL_SC	is the path loss measured from the received SC signal;
SNRrequiredCCH	is the SNR required for the control channel to be received;
PmarginTCH	is the power margin for the tone channel linked to the control channel.

These parameters are received from the upper layer as UPtoDN.InfoPowerParamCCH.

Second, when negotiation is performed with a dedicated slot or IWR, a value obtained by adding PTX_CCHTCH_differ to the transmission power of a data slot used in subchannel negotiation is used.

6.4.3 Generated link confirmation

6.4.3.1 General

The generated link confirmation stage is 2 sec after success in the subchannel allocation competition.

UAs in the generated link confirmation stage shall broadcast related subchannel information in their SC occupied slot.

In the generated link confirmation stage, the UA transmits a packet in the downlink slot of the allocated subchannel and receives the packet in the uplink slot of the allocated subchannel. When the UA transmits a downlink packet, it shall contain a PB 0x0A consisting of ACKs for the uplink packet received from the controller.

In the generated link confirmation stage, the controller transmits a packet in the uplink slot of the allocated subchannel and receives the packet in the downlink slot of the allocated subchannel. When the controller transmits an uplink packet, it shall include a PB 0x0B consisting of ACKs for the received downlink packet.

When one second passes in the generated link confirmation stage, if the error rate of the packet it receives exceeds LinkConfirmError, the UA and the controller stop occupying the subchannel after transmitting PB 0x0C notifying the link confirmation failure for the next 1 sec.

When 2 sec elapse in the generated link confirmation stage, the UA and the controller stop occupying the subchannel when receiving PB 0x0C or when the packet error rate for the last 1 sec is 100 %. Otherwise, it is determined that the link has been generated.

6.4.3.2 Packet error rate measurement

The UA measures the uplink error rate, and the controller measures the downlink error rate.

The uplink error rate is the number of CRC fail divided by the total number of received uplink packets. The downlink error rate is the number of CRC fail divided by the total number of received downlink packets. The error rate is measured every frame.

6.4.3.3 Initial transmit power at generated link confirmation

The initial transmission power of the UA and controller used in the subchannel initialization process is as follows.

a) In case of performing subchannel negotiation with SC signal:

$$PTX\_CO\_CCH\_ini = MIN((PtargetCCH + PL\_SCd + SNRrequiredCCH + PmarginCCH),\ PmaxCCH) \quad (27)$$

$$PTX\_DR\_CCH\_ini = MIN((PtargetCCH + PL\_SCc + SNRrequiredCCH + PmarginCCH),\ PmaxCCH) \quad (28)$$

where

PtargetCCH is the target reception power of the CCH;

PL_SCd is the path loss measured from the SC signal received by the controller;

PL_SCc is the path loss measured from the SC signal received by the UA;

SNRrequiredCCH is the SNR required to receive the control channel;

PmarginCCH is the power margin for the control channel.

These parameters are received from the upper layer as UPtoDN.InfoPowerParamCCH.

b) When negotiation is performed with dedicated slot or IWR, the last transmission power used during negotiation is used:

$$PTX\_CO\_CCH\_ini = PTX\_CO\_DS\_prevorPTX\_CO\_IWR\_prev \quad (29)$$

$$PTX\_DR\_CCH\_ini = PTX\_DR\_DS\_prevorPTX\_DR\_IWR\_prev \quad (30)$$

The UA and controller determine the subchannel transmission power plus PTX_CCHTCH_differ as the transmission power of the tone subslot.

6.4.3.4 Transmission power control at generated link confirmation

The controller shall inform its own transmit power using PB 0x06 and inform the downlink received power PRX_CCH_dn. The UA shall inform its own transmit power and uplink received power PRX_CCH_up by using PB 0x06. The controller and the UA can calculate the path loss using the information

received from PB 0x06 received from the counterpart. It is implementation dependent for the controller and the UA to perform transmit power control using the calculated path loss. However, the following rules shall be observed in the transmit power control.

a) The transmit power within one frame is the same. The power change is applied when the frame changes.

b) The power of one frame can be up to 4 dB greater than the power of the previous frame.

c) If the transmission power of the UA and that of the controller are different, the difference shall be less than 4dB.

The UA and the controller determine the subchannel transmission power plus PTX_CCHTCH_differ as the transmission power of the tone subslot.

6.4.3.5 ACK parsing block

The parsing field of PB 0x0A transmitted by the UA is shown in Table 8.

Table 8 — Parsing field of PB 0x0A

Bits	Description
[0:5]	6 ACK bits, 1 means ACK, 0 means NACK, ACKs for uplink slots between two downlink slots, i.e. bit 0 is an ACK on earliest downlink slot.

The parsing field of PB 0x0A transmitted by the controller is shown in Table 9.

Table 9 — Parsing field of PB 0x0B

Bits	Description
[0:1]	2 ACK bits, 1 means ACK, 0 means NACK, ACKs for the downlink slot received before the corresponding uplink slot, bit 0 is an ACK on earliest uplink slot.

PB 0x0C transmitted by a UA or controller does not have a parsing field.

6.4.4 Broadcasting control channel information being allocated or occupied

The UA shall broadcast the CSCH information it is allocating or occupying to the occupying SC slot. The related PBs are PB 0x86 and PB 0x8A, and the related parsing fields are shown in Table 10.

Table 10 — Parsing field of 0x86 in SC

Bits	Description
[0:4]	Control channel number
[5:9]	CSCH number
[10:33]	Own latitude, see ISO/IEC 4005-2:2023, B.1
[34:57]	Own longitude, see ISO/IEC 4005-2:2023, B.2
[58:69]	Own altitude, see ISO/IEC 4005-2:2023, B.3
[70:85]	Latitude difference between the controller and the UA, see ISO/IEC 4005-2:2023, B.7
[86:105]	Longitude difference between the controller and the UA, see ISO/IEC 4005-2:2023, B.8
[106:113]	Altitude difference between the controller and the UA, see ISO/IEC 4005-2:2023, B.9
[114:120]	CSCH TX power of an unit that has bigger power among the UA and the controller, the range of -40dBm(0) ~ 40dBm(80)

The parsing field of PB 0x8A shall follow the description in ISO/IEC 4005-4.

In this document, PB 0x86 is described, but an upper layer can additionally designate another parsing block for CSCH information transmission.

The shared slot transmission power of the SC uses the general SC slot transmission power as it is.

6.5 Subchannel occupation and collision management

6.5.1 General

At this stage, the UA and the controller occupy the subchannel. Occupation is performed by slot clearing. The UA and the controller perform slot clearing tone transmission and collision tone transmission in the tone subslot set mapped with the occupied subchannel. Resource collision monitoring is performed by detecting collision tones of other units. Measurement of the amount of interference for neighboring channels is also performed.

In the occupation stage, the UA shall transmit information such as the allocated subchannel number, the location of the UA and the controller, and the bigger transmission power with a SC slot using PB 0x86. Using the transmitted and received SC information, subchannel collision and new subchannel allocation are determined.

6.5.2 Subchannel occupation and return

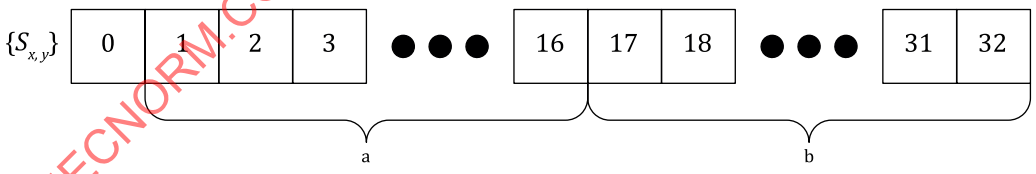
Subchannel occupation is achieved by the UA and the controller transmitting a tone signal at subslot 0 of the tone subslot set mapped to the subchannel together, i.e. the UA and the controller perform slot clearing at the same subslot. The return of the occupied subchannel is done by stopping slot clearing. The upper layer, if necessary, can request the return of the occupied CSCH by UPtoDN.ReqReturnCSCH.

6.5.3 Collision tone transmission and collision management

When the UA and the controller perform slot clearing for subchannel occupation, the collision tone shall be transmitted in the same subslot set. In addition, the UA and the controller shall detect the collision tone of another terminal in the subslot where the collision tone is not transmitted.

The UA and the controller transmit two collision tones of their own in the relative subslot set.

In the case of TSBtype0, the transmission region of the collision tone is divided into two parts as shown in Figure 17. The first transmission region is from subslot 1 to subslot 15 and the second transmission region is from subslot 16 to subslot 32.



Key

$\{S_{x,y}\}$ tone subslot set mapped to data slot S_y of control channel x

a First transmission region.

b Second transmission region.

Figure 17 — Transmission region of collision tone in TSBtype0

In the case of TSBtype1, the first transmission region is from subslot 1 to subslot 9, and the second transmission region is from subslot 10 to subslot 19.

In the case of TSBtype2, the first transmission region is from subslot 1 to subslot 4, and the second transmission region is from subslot 5 to subslot 9.

The first transmission region is used by the UA, and the second transmission region is used by the controller.

In the case of TSBtype0, the UA calculates the subslot numbers transmitting its own tone in each transmission region using the PN code generator in Figure 14 as follows.

$$
\begin{aligned}
&[D_{25}(0), D_{24}(0), \ldots, D_0(0)] = [SA_{25}, SA_{24}, \ldots, SA_0] \\
&[b_{25}, b_{24}, \ldots, b_{17}] = [s_8, s_7, \ldots, s_0] \\
&[b_{16}, b_{15}, \ldots, b_{11}] = [f_5, f_4, \ldots, f_0] \\
&[b_{10}, b_9, \ldots, b_0] = [M_5, M_4, M_3, M_2, M_1, M_0, H_4, H_3, H_2, H_1, H_0] \\
&[a_{25}, a_{24}, \ldots, a_0] = [SA_0, SA_1, \ldots, SA_{24}, 1] \\
&PN(clk) = (D_0(clk) \,\&\, b_0)(D_1(clk) \,\&\, b_1)\hat{}\ldots\hat{}(D_{25}(clk) \,\&\, b_{25}) \\
&N_{PN1}(n) = [PN(12n+11), PN(12n+10), \ldots, PN(12n+1), PN(12n)] \\
&N_{CT}(0) = floor((15 \times N_{PN1}(0))/2^{12}) \\
&N_{CT}(1) = floor((14 \times N_{PN1}(1))/2^{12})
\end{aligned}
\tag{31}
$$

where

$D_x(clk)$ is a x-th bit of shift register D at clock clk;

SA_x is a x-th bit of source address, the number of SA bits is greater than or equal 26;

s_x is a x-th bit of slot number, the number of s bits is 9;

f_x is a x-th bit of frame number, the number of f bits is 6;

M_x is a x-th bit of minute, the number of M bits is 6;

H_x is a x-th bit of hour for 24-hour clock, the number of H bits is 5 and H has the value from 0 to 23;

$PN(clk)$ is a pseudo random bit of PN code generator at clock clk;

& is AND bit operation that means a logical multiplication;

^ is exclusive OR bit operation that means exclusive logical sum operation;

$floor(x)$ means the largest integer among integers smaller than or equal to x.

The positions N_{C0} and N_{C1} of the two collision tones are as follows.

$$
\begin{aligned}
N_{C0} &= N_{CT}(0) + N_{CToffset} \\
N_{C1} &= N_{CT}(1) + N_{CToffset}, \quad if N_{CT}(1) < N_{CT}(0) \\
&= N_{CT}(1) + 1 + N_{CToffset}, \; if N_{CT}(0) \le N_{CT}(1)
\end{aligned}
\tag{32}
$$

where $N_{CToffset}$ is 1 for the UA and 16 for the controller in TSBtype0, 1 for the UA and 10 for the controller in TSBtype1, 1 for the UA and 5 for the controller in TSBtype2.

In the case of TSBtype0, the controller changes the N_{CT} part in Formula (32) as follows.

$$N_{CT}(0) = floor((16 \times N_{PN1}(0))/2^{12})$$
$$N_{CT}(1) = floor((15 \times N_{PN1}(1))/2^{12}) \quad (33)$$

In the case of TSBtype1, the controller changes the N_{CT} part in Formula (32) as follows.

$$N_{CT}(0) = floor((10 \times N_{PN1}(0))/2^{12})$$
$$N_{CT}(1) = floor((9 \times N_{PN1}(1))/2^{12}) \quad (34)$$

In the case of TSBtype1, the UA changes the N_{CT} part in Formula (32) as follows.

$$N_{CT}(0) = floor((9 \times N_{PN1}(0))/2^{12})$$
$$N_{CT}(1) = floor((8 \times N_{PN1}(1))/2^{12}) \quad (35)$$

In the case of TSBtype2, the controller changes the N_{CT} part in Formula (32) as follows.

$$N_{CT}(0) = floor((5 \times N_{PN1}(0))/2^{12})$$
$$N_{CT}(1) = floor((4 \times N_{PN1}(1))/2^{12}) \quad (36)$$

In the case of TSBtype2, the UA changes the N_{CT} part in Formula (32) as follows.

$$N_{CT}(0) = floor((4 \times N_{PN1}(0))/2^{12})$$
$$N_{CT}(1) = floor((3 \times N_{PN1}(1))/2^{12}) \quad (37)$$

The UA and the controller pair shall always receive subslots except for subslot 0 and four collision tone transmission subslots in the subslot set mapped with the occupied subchannel.

If two or more collision tones are detected in a subslot set whose received power is greater than PRXcollsiontoneThre0 and smaller than PRXcollsiontoneThre1, the unit decides to return subchannel resources. PRXcollsiontoneThre0 and PRXcollsiontoneThre1 are received from the upper layer as UPtoDL.InfoPowerParamCCH.

When a collision tone whose reception power is greater than PRXcollsiontoneThre0 and smaller than PRXcollsiontoneThre1 is detected for two consecutive frames, the unit decides to return the subchannel resource.

When a collision tone whose reception power is greater than PRXcollsiontoneThre1 is detected from the collision unit, the unit decides to return the subchannel resource.

When *FrmAvgDT* is equal to or greater than PRXcollsiontoneThre3, the slot return is determined. Here, *FrmAvgDT* is an average power of one frame average power during PRXnumAvgFrm. One frame average power is calculated in a subslot set by averaging received power values of detected tones those received powers are equal to or greater than PRXcollsiontoneThre2. If the number of detected tones is greater than 2 in the subslot set, the one frame average power is calculated with the two values of the largest received power.

When it is determined to return the subchannel resource, the unit shall inform the counterpart unit of it using PB 0x0D.

6.5.4 Power control in occupation stage

The controller shall inform its own transmit power and downlink receive power PRX_CCH_dn using PB 0x06. The UA shall inform its own transmit power and uplink receive power PRX_CCH_up by using PB 0x06. The controller and UA can calculate the path loss using the information received from the PB 0x06 received from the counterpart. Using the calculated path loss, it is implementation dependent for

the unit to perform transmit power control. However, the following rules shall be observed in transmit power control.

a) The transmit power within one frame is the same. The power change is applied when the frame changes.

b) If the transmission power is more than Pmax_dmap1 and less than Pmax_dmap2, the maximum power increase per frame is 4 dB, and when the transmission power is Pmax_dmap2 or more, the maximum power increase per frame is 2 dB. Where, Pmax_dmap1 and Pmax_dmap2 are received as UPtoDL.InfoPowerParamCCH from the upper layer.

c) If the transmission power of the UA and the controller is different, the difference shall be less than 5dB.

d) The maximum power in the occupation stage, *Pmax_occupy*, is generally equal to PmaxCCH. However, a case in which a unit using the same channel resource is found in the SC is as follows. If the distance to the unit is greater than d_map1, *Pmax_occupy* is Pmax_dmap2, and if the distance to the unit is less than d_map1 and greater than d_map0, *Pmax_occupy* is Pmax_dmap1. If the distance to the unit is less than or equal to d_map0, the unit maintains the current power for the associated subchannel.

e) A controller with a transmission power of Pmax_dmap0 or more shall broadcast the UA's location, its location, allocated subchannel, and current transmission power through the SC for 4 sec when increasing the transmission power by 8 dB or more for 5 sec. If the SC slot for this is not allocated, power increase is prohibited for 4 sec.

The unit determines the subchannel transmission power plus PTX_CCHTCH_differ as the transmission power of the tone subslot. The transmit power of the tone subslot cannot exceed PmaxTCH.

6.6 Reallocation

6.6.1 General

When a same resource collision occurs or when neighbouring channel interference is greater than the threshold value, the unit that detects this shall reallocate the subchannel. The unit can detect the same resource collision through a collision tone, or the SC reception. The neighbouring channel interference can be detected by receiving the mapping subslot sets of the tone channel or by the SC reception.

When reallocation is determined, the existing control channel can be used for reallocation. Reallocation using existing control channels depends on implementation.

6.6.2 Reallocation decision

6.6.2.1 Reallocation decision due to same resource collision

Reallocation decisions due to collision tone detection are described in 6.5.2.

Units allocated the same subchannel can be detected by SC reception. In this case, subchannel reallocation is determined under the following conditions.

a) When another control pair allocated the same subchannel is detected, and the distance between these two units of the control pair is 500m or more.

b) When another control pair allocated the same subchannel is detected, and the transmission power of one or both units of the corresponding control pair is greater than or equal to Pmax_dmap2.

c) When a unit allocated with the same subchannel is detected at a distance less than d_map0.

d) When a unit allocated with the same subchannel is detected and the unit has a transmission power of Pmax_dmap1 or more, and the distance between itself and the unit is more than d_map0 and less than d_map1.

6.6.2.2 Reallocation decision due to neighbour channel interference

Neighbouring channel interference exists between UAs and controllers. Because the uplink and downlink are separated in time region, there is no channel interference between UAs or between controllers.

Measurement of the amount of interference due to neighbouring channels using a competition tone channel is described in 6.2.2 and subchannel reallocation is determined under the following conditions.

a) When the calculated interference power is greater than (PImin-PImargin-6dB) and less than (PImin-PImargin-3dB), which lasts for 4 sec.

b) When the calculated interference power is greater than (PImin-PImargin-3dB) and less than (PImin-PImargin), which lasts for 2 sec.

c) When the calculated interference power is greater than or equal to (PImin – PImargin).

PImin and PImargin are received as UPtoDL.InfoPowerParamCCH from the upper layer.

Subchannel reallocation is determined when the interference of the same neighbouring channel is the following condition according to the SC reception information.

a) If the interference power calculated from the current position and the transmission power of the controller using the interference channel is greater than PIrealloc0, the UA determines reallocation, where the interference power is calculated as follows.

$$PI_{CitoDj} = PTXscCO_i - L_{fs}(d) - IC_{|i-j|} \tag{38}$$

where

i is the channel number used by the interference controller;

$PTXscCO_i$ is the CSCH transmit power of the interference channel i;

j is the channel number of the UA;

d is the distance between the UA and the interference controller in km, and shall be calculated based on location information.

The free space path loss $L_{fs}(d)$ is calculated as follows.

$$L_{fs}(d) = 32{,}45dB + 20log_{10}(d_{km} \cdot f_{MHz}) \tag{39}$$

where f_{MHz} is the center frequency of the channel used by the interference controller and is calculated from the upper interface UPtoDL.InfoControlChannel.

b) If the interference power calculated from the transmission power and current location of the UA using the interference channel are greater than PIrealloc0, the controller determines the reallocation.

where the interference power is calculated as follows.

$$PI_{DjtoCi} = PTXscDR_j - L_{fs}(d) - IC_{|i-j|} \tag{40}$$

where

i is the channel number used by the controller;

j is the channel number used by the interference UA;

$PTXscDR_j$ is the CHCS transmission power of the interference channel j;

d is the distance between the controller and the interference UA in km.

The free space path loss $L_{fs}(d)$ is calculated as follows.

$$L_{fs}(d) = 32{,}45dB + 20log_{10}(d_{km} \cdot f_{MHz}) \quad (41)$$

where f_{MHz} is the centre frequency of the interference channel used by the UA where PIrealloc0 is received as UPtoDL.InfoPowerParamCCH from the upper layer.

Subchannel reallocation is recommended when the neighboring channel interference calculated from the SC reception information is the following conditions.

a) If the future interference power calculated from the transmission power and location of the controller using the neighboring channel and the future UA's own way point are expected to be greater than PIrealloc1, the UA can determine reallocation, where the interference power is calculated as follows.

$$PIf_{CitoDj} = PTXscCO_i - L_{fs}(d_f) - IC_{|i-j|} \quad (42)$$

where

i is the channel number used by the interference controller;

$PTXscCO_i$ is the CSCH transmit power of the interference channel i;

j is the channel number of the UA;

d_f is the minimum distance between the interference controller and the UA in the next 10 sec.

It shall be calculated from the way points, which is implementation dependent. The free space path loss $L_{fs}(d_f)$ is calculated as follows.

$$L_{fs}(d_f) = 32{,}45dB + 20log_{10}(d_{f\ km} \cdot f_{MHz}) \quad (43)$$

where f_{MHz} is the center frequency of the interference channel used by the controller.

b) If the future interference power calculated from the transmission power and location and the future UA's way point of the UA using the neighboring channel are expected to be greater than PIrealloc1, the controller can determine reallocation, where the interference power is calculated as follows.

$$PIf_{DjtoCi} = PTXscDR_j - L_{fs}(d_f) - IC_{|i-j|} \quad (44)$$

where

i is the channel number of the controller;

j is the channel number used by the interference UA;

$PTXscDR_j$ is the CSCH transmission power of the interference channel j;

d_f is the minimum distance between the controller and the interfering UA that will be obtained within the next 10 sec.

It shall be calculated from the current position and way points of the interfering channel UA, which is implementation dependent. The free space path loss $L_{fs}(d_f)$ is calculated as follows.

$$L_{fs}\left(d_f\right) = 32{,}45dB + 20log_{10}\left(d_{f\ km} \cdot f_{MHz}\right) \quad (45)$$

where f_{MHz} is the center frequency of the interference channel used by the UA where PIrealloc1 is received as UPtoDL.InfoPowerParamCCH from the upper layer.

6.6.2.3 Reallocation decision by increasing packet error rate

Subchannel reallocation by increasing packet error rate is implementation dependent.

6.6.3 Subchannel reallocation procedure

6.6.3.1 General

When the UA or controller decides to reallocate, it shall notify the counterpart using PB 0x0D. The unit that receives the PB 0x0D indicating the decision to return the subchannel resource shall transmit the PB 0x0D whose parsing field value is 4. This PB 0x0D exchange shall take place within TimeOf0DTry seconds. If the PB 0x0D exchange fails, the unit immediately returns the subchannel.

If the UA decides to reallocate, it can transmit its own subchannel map using PB 0x03 together with PB 0x0D. When the controller decides to reallocate, it can request the UA's subchannel map transmission by using PB 0x02 with PB 0x0D.

When subchannel reallocation is performed, the existing allocated subchannel is occupied for maximum TcchReturns. If reallocation is completed within TcchReturn, the existing subchannel is immediately returned. TcchReturn is received as UPtoDN.InfoTimeParam from the upper layer.

The subchannel reallocation procedure is the same as the subchannel allocation procedure except for the subchannel negotiation.

Subchannel negotiation is first performed in the manner indicated by the ReallocMethod parameter of UPtoDL.InfoControlChannel. If ReallocMethod is '0' and the controller cannot receive the UA's SC slot, subchannel negotiation is performed with IWR.

The method that the UA and the controller perform subchannel negotiation is the same as in 6.3, but in the case of subchannel reallocation, additionally currently allocated subchannels can be used simultaneously. The unit can request and respond to a subchannel map with the currently allocated subchannel and can transmit and respond to the determined subchannel number.

The operation of using the currently allocated subchannel together during such subchannel negotiation is implementation dependent.

If subchannel reallocation is successful, this shall be notified to the upper layer with DLtoUP. NotiCSCHStatus instead of DLtoUP.NotiGetCSCH.

A UA or controller performing the subchannel reallocation procedure can continue to perform power control for the currently allocated subchannel.

6.6.3.2 Parsing block for reallocation

The parsing field of PB 0x0D indicating the reallocation decision is shown in Table 11.

Table 11 — Parsing field of 0x0D

Bits	Description
[0:2]	0 – Collision tone detection 1 – Collision detection of the same resource through SC reception 2 – Threshold excess of neighboring channel interference 3 – Prediction of threshold excess of neighboring channel interference 4 - Response to counterpart unit's decision to reallocate

6.7 Data exchange

6.7.1 General

Parsing blocks that are equal to or higher than 0x80 share the same parsing blocks with SC. PBs that can be used in the control channel are PBs from 0x00 to 0x7F, which is shared with the video channel.

The upper layer can request packet transmission using UPtoDL.ReqTxCCH. The DLL shall deliver the received packet to the upper layer using DLtoUP.RsvCCHData. At this time, if all PBs included in the received packet are in the header list of Table 13, it is possible that they are not delivered to the upper layer.

6.7.2 Data packet format

6.7.2.1 General

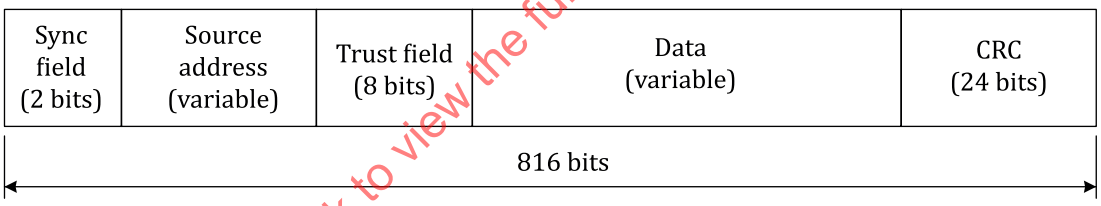


Figure 18 — Control channel packet format except IWR

Figure 18 shows the packet format of the data link layer. The source address is generally 26 bits, but higher layers can allocate a larger address with UPtoDN.InfoPacketParam. The total length of the packet is 816 bits, and the maximum length of data varies according to the length of the source address. The upper layer can deliver data of length less than or equal to the maximum length of data to DLL. CRC is added at the physical layer.

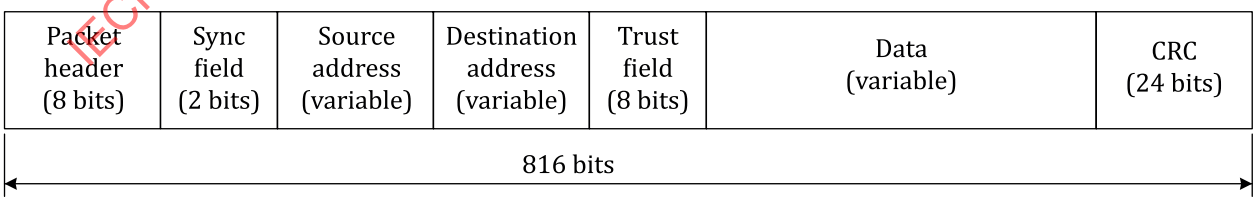


Figure 19 — IWR packet format

The packet format of IWR is shown in Figure 19. The source address and destination address are generally 26 bits. Where, the length of the source address and the length of the destination address are the same. The total length of the packet is 816 bits, and the maximum length of data varies according to the length of the source address and destination address. PKH 0x00 is used for control channel allocation in this document. Remain PKHs is determined at the upper layer.

6.7.2.2 Sync field

The sync field is 2 bits. The meaning of the sync field is shown in Table 12.

Table 12 — Sync field meaning

Value	Description
0x0	A sync
0x1	B sync
0x2	C sync
0x3	reserved

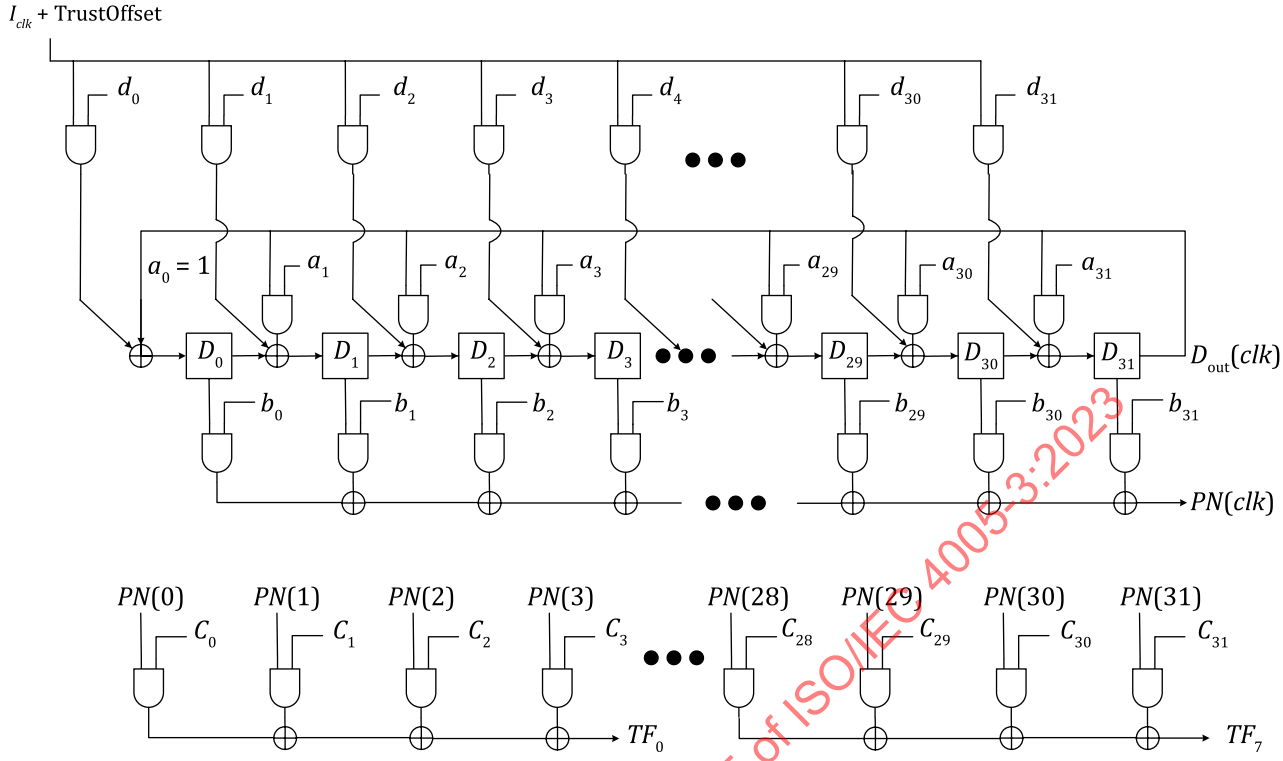
6.7.2.3 Source address and destination address

It is recommended to set the source address and destination address to 26 bits. However, the upper layer can set the unit address bit number larger. In this case, the upper layer shall shorten the maximum data field length by the increased number of bits.

6.7.2.4 Trust field

The trust field shall be received by all units, but the trust check shall be performed only by an authorized receiver.

The method of generating a trust field uses LFSR structure shown in Figure 20.



Key

$I_{clk+\text{TrustOffset}}$	a (*clk*+TrustOffset)-th bit of input data from upper layer or encrypted data
a_k	a *k*-th bit for AND operation with D_{out}
b_k	a *k*-th bit for AND operation with D_k
c_k	a *k*-th bit for AND operation with *PN*(*k*)
d_k	a *k*-th bit for AND operation with *input*(*clk*+TrustOffset)
D_k	a *k*-th register
$D_{\text{out}}(clk)$	output of shift register D_{31} at clock *clk*
$PN(clk)$	PN coded generator output for trust field generation at clock *clk*
TF_x	a *x*-th bit of trust field

Figure 20 — LFSR structure for trust field generation

The value of *PN* and the *i*-th trust bit TF_i are as follows.

$$[D_{31}(0), D_{30}(0), \ldots, D_{26}(0)] = [K_{101}, K_{100}, \ldots, K_{96}]$$
$$[D_{25}(0), D_{24}(0), \ldots, D_{0}(0)] = [SA_{25}, SA_{24}, \ldots, SA_{0}]$$
$$[d_{31}, d_{30}, \ldots, d_{23}] = [s_8, s_7, \ldots, s_0]$$
$$[d_{22}, d_{21}, \ldots, d_{17}] = [f_5, f_4, \ldots, f_0]$$
$$[d_{16}, d_{15}, \ldots, d_{11}] = [M_5, M_4, M_3, M_2, M_1, M_0]$$
$$[d_{10}, d_9, \ldots, d_6] = [H_4, H_3, H_2, H_1, H_0]$$
$$[d_5, d_4, \ldots, d_0] = [J_4, J_3, \ldots, J_0, K_0]$$
$$[b_{31}, b_{30}, \ldots, b_0] = [K_{95}, K_{94}, \ldots, K_{64}]$$
$$[c_{31}, c_{30}, \ldots, c_0] = [K_{63}, K_{62}, \ldots, K_{32}]$$
$$[a_{31}, a_{30}, \ldots, a_0] = [K_{31}, K_{30}, \ldots, K_1, 1]$$
$$PN(clk) = (D_0(clk) \,\&\, b_0)(D_1(clk) \,\&\, b_1)\wedge \ldots \wedge (D_{31}(clk) \,\&\, b_{31})$$
$$TFn = (PN(4n) \,\&\, c_{4n})(PN(4n+1) \,\&\, c_{4n+1})(PN(4n+2) \,\&\, c_{4n+2})(PN(4n+3) \,\&\, c_{4n+3}), n = 0,1,\ldots,7,$$
$$[c_{4n}, c_{4n+1}, c_{4n+2}, c_{4n+3}] \neq [0, 0, 0, 0] \quad (46)$$

where

$D_x(clk)$ is a *x*-th bit of shift register *D* at *clk*;

SA_x is a *x*-th bit of source address, the number of *SA* bits is greater than or equal 26;

f_x is a *x*-th bit of frame number, the number of *f* bits is 6;

s_x is a *x*-th bit of slot number, the number of *s* bits is 9;

M_x is a *x*-th bit of minute, the number of *M* bits is 6;

H_x is a *x*-th bit of hour for 24-hour clock, the number of *H* bits is 5 and *H* has the value from 0 to 23;

J_x is a *x*-th bit of date, the number of *J* bits is 5 and *J* has the value from 1 to 31;

K_x is a *x*-th bit of secret key between the trust check system and the unit and has a length of 102 bits;

$PN(clk)$ is a pseudo random bit of PN code generator at *clk*, and $PN(0)$ is the *PN* value when the initial value is loaded into the PN code generation register.

The LFSR is updated as follows.

$$D_0(clk+1) = (D_{31}(clk) \,\&\, a_0)(I_{TrustOffset+clk} \,\&\, d_0)$$
$$D_i(clk+1) = D_{i-1}(clk)(D_{31}(clk) \,\&\, a_i)(I_{TrustOffset+clk} \,\&\, d_i), i = 1, \ldots, 31 \quad (47)$$

where

I_x is a *x*-th bit of input data from upper layer or encrypted bit if data security is applied;

TrustOffset is an offset of data field.

6.7.2.5 Data field

6.7.2.5.1 General

The data field consists of parsing blocks. The parsing block consists of a parsing header and a parsing field. The parsing header is 8 bits, and the length of the parsing field depends on the parsing header. Each parsing block can be inserted anywhere in the data field. However, a parsing block and another parsing block shall be attached without empty space, and the first parsing block shall be located immediately after the trust field.

The upper layer shall transmit data of a length less than or equal to the length of the data field to the data link layer. If the length of information provided from the upper layer is smaller than the length of the data field, the remaining bits are processed as follows.

If the length of unused extra data bits is less than 8, the extra data bits are filled with '0'. If the length of unused extra data bits is greater than or equal to 8, the extra data bits are filled with a parsing header '0x80' and a padding bit string of length 97 indicating padding. The padding bits are constructed by using a string of bits of length 97 repeatedly. A 97-bit sequence consists of the next 96-bit sequence followed by a bit of '1'.

— ‘0x71E5477D_A5B32BF7_E5469C8E’

where '_' is used to distinguish 32 bits without meaning.

6.7.2.5.2 Parsing header and parsing field

The parsing header consists of 8 bits. If the most significant bit of the parsing header is '1', it has the same meaning in common in SC, CC, and VC. If the most significant bit of the parsing header is '0' in CSCH, it has a meaning related to CC and VC. The parsing header is specified in Table 13. Upper layers can define different parsing headers.

Table 13 — Parsing header list

Value	Description
0x02	Request to transmit a subchannel map, it does not have a parsing field.
0x03	Subchannel map
0x04	Subchannel allocation request
0x05	ACK on subchannel allocation request
0x06	Own transmission power and reception power of the counterpart's signal
0x07	Own transmission power and designation of the counterpart’s transmission power
0x08	IWR resource collision notification, this has no parsing field.
0x0A	ACKs for uplink packets
0x0B	ACKs for downlink packets
0x0C	Link confirmation failure, this has no parsing field.
0x0D	Notification of reallocation decision

6.8 Synchronization

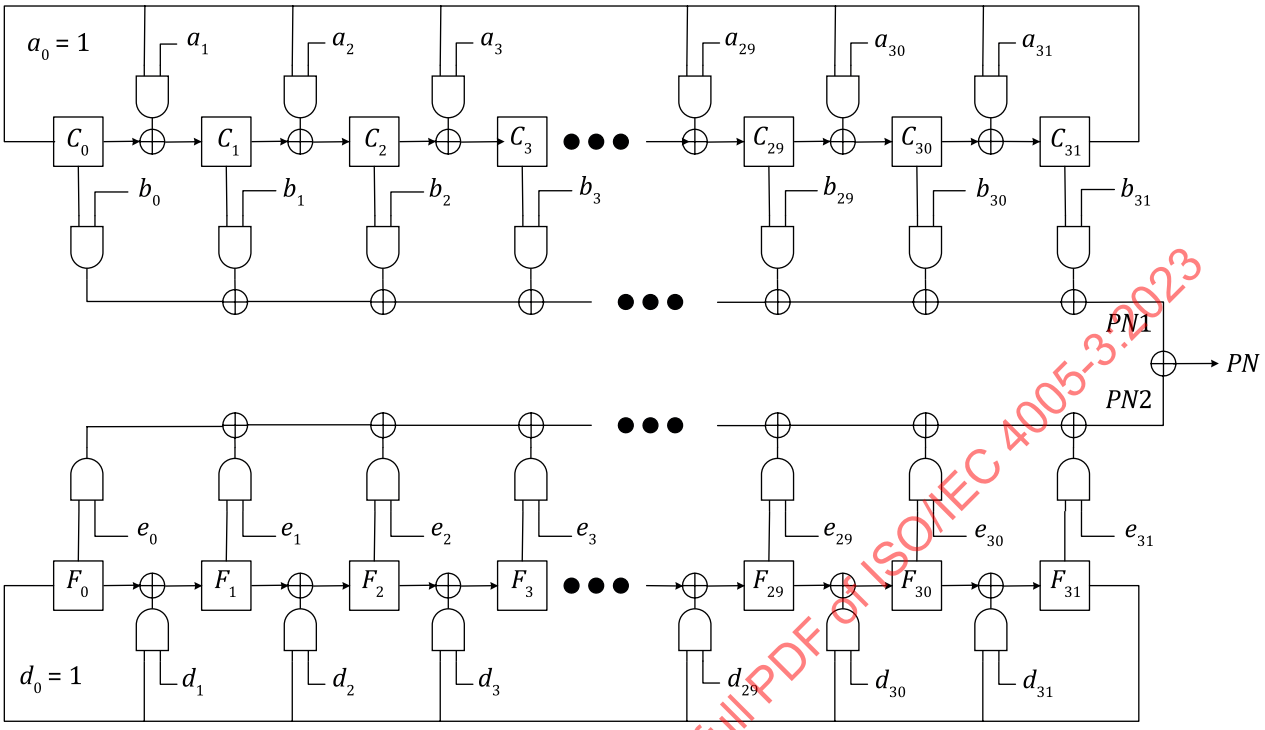
A sync, B sync and C sync units shall know the date, hour, minute, second, slot number in order to transmit a packet.

6.9 Data link layer security

In control communication, units perform one-to-one communication. Security can be applied depending on the service of one-on-one communication.

If an upper layer requests the use of data link security, then the following security shall be used.

The data link layer receives the security key U from the upper layer. The data field is scrambled by the PN code generated by the PN generator as shown in Figure 21.



Key

a_k	a k-th bit for AND operation with C_{31}
b_k	a k-th bit for AND operation with C_k
C_k	a k-th register of upper LFSR
F_k	a k-th register of lower LFSR
d_k	a k-th bit for AND operation with F_{31}
e_k	a k-th bit for AND operation with F_k
$PN1$	output of upper LFSR
$PN2$	output of lower LFSR
PN	output of PN code generator

Figure 21 — PN code generator used for data scrambling

$$[a_{31}, a_{30}, \ldots, a_0] = [U_{26}, U_{25}, s_8, U_{24}, \ldots, U_{16}, s_6, U_{15}, \ldots, U_8, s_3, U_7, \ldots, U_0, s_0, 1]$$

$$[b_{31}, b_{30}, \ldots, b_0] = [U_{55}, \ldots, U_{47}, f_5, U_{46}, \ldots, U_{37}, f_3, U_{36}, \ldots, U_{28}, f_0, U_{27}]$$

$$[C_{31}(0), C_{30}(0), \ldots, C_0(0)] = [U_{77}, \ldots, U_{73}, M_5, M_4, M_2, H_4, H_3, H_2, U_{72}, \ldots, U_{61}, Y_3, Y_1, W_3, W_1, U_{60}, \ldots, U_{56}]$$

$$[d_{31}, d_{30}, \ldots, d_0] = [U_{103}, s_7, s_5, U_{102}, \ldots, U_{93}, s_4, U_{92}, \ldots, U_{85}, s_2, U_{84}, \ldots, U_{78}, s_1, 1]$$

$$[e_{31}, e_{30}, \ldots, e_0] = [U_{132}, \ldots, U_{126}, f_4, U_{125}, \ldots, U_{114}, f_2, U_{113}, \ldots, U_{105}, f_1, U_{104}]$$

$$[F_{31}(0), F_{30}(0), \ldots, F_0(0)] = [U_{154}, \ldots, U_{150}, M_3, M_1, M_0, H_1, H_0, U_{149}, \ldots, U_{138}, Y_4, Y_2, Y_0, W_2, W_0, U_{137}, \ldots, U_{133}]$$

$$PN1(clk) = (C_0(clk) \,\&\, b_0) \hat{} (C_1(clk) \,\&\, b_1) \hat{} \ldots \hat{} (C_{31}(clk) \,\&\, b_{31})$$

$$PN2(clk) = (F_0(clk) \,\&\, e_0) \hat{} (F_1(clk) \,\&\, e_1) \hat{} \ldots \hat{} (F_{31}(clk) \,\&\, e_{31})$$

$$PN(clk) = PN1(clk) \hat{} PN2(clk) \quad (48)$$

where

$C_x(clk)$	is a *x*-th bit of upper shift register *C* at *clk*;
$F_x(clk)$	is a *x*-th bit of lower shift register *F* at *clk*;
U_x	is a *x*-th bit of a security key provided by the upper layer;
f_x	is a *x*-th bit of frame number, the number of *f* bits is 6;
s_x	is a *x*-th bit of slot number, the number of *s* bits is 9;
M_x	is a *x*-th bit of minute, the number of *M* bits is 6;
H_x	is a *x*-th bit of hour for 24-hour clock, the number of *H* bits is 5 and *H* has the value from 0 to 23;
Y_x	is a *x*-th bit of date, with a value from 1 to 31, the number of *Y* bits is 5;
W_x	is a *x*-th bit of month, with a value from 1 to 12, the number of *W* bits is 4;
$PN(clk)$	is a pseudo random bit of PN code generator at *clk*, and $PN(0)$ is the *PN* value when the initial value is loaded into the two PN code generation registers.

The first bit of the data field is scrambled with $PN(O_{offset})$. Subsequent data bits are also scrambled sequentially. Where O_{offset} is $[U_{159}, U_{158}, ..., U_{155}]$.

The padding block in data field is not scrambled.

6.10 Interface with upper layers

6.10.1 General

The interface with the upper layer consists of the interface header and the following parameters as shown in Figure 22. The number of bits of the header is 8 bits, and the number of parameters and the number of bits of each parameter are different for each interface header.

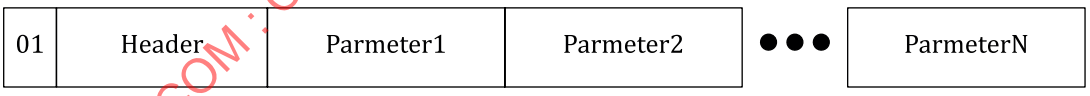


Figure 22 — Interface packet structure with upper layer

The upper layer can send an interface packet to the DLL and likewise the DLL can send an interface packet to the upper layer. In this case, sending ACK/NACK in response to each interface is optional and implementation dependent.

6.10.2 Initialization interface

6.10.2.1 General

The initialization interface is used when the unit is initialized. The upper layer can use this interface after initialization if necessary. Table 14 shows an initialization interface list.

Table 14 — Initialization interface list

Interface name	Header value	Direction
UPtoDL.InfoPowerParamCCH	0x01	to DL

Table 14 *(continued)*

Interface name	Header value	Direction
UPtoDL.InfoPowerParamCCHsub	0x02	to DL
UPtoDN.InfoPowerParamDS	0x03	to DL
UPtoDN.InfoPowerParamIWR	0x04	to DL
UPtoDL.InfoTSBTypeMap	0x05	to DL
UPtoDL.InfoMapOption	0x06	to DL
UPtoDL.InfoApprovedSubchMap	0x07	to DL
UPtoDL.InfoICConstant	0x08	to DL
UPtoDN.InfoTimeParam	0x09	to DL
UPtoDN.InfoPacketParam	0x0A	to DL
UPtoDL.InfoDedicatedSlot	0x0B	to DL
UPtoDL.InfoIWRSlot	0x0C	to DL
UPtoDL.InfoControlChannel	0x0D	to DL
UPtoDL.InfoSecurity	0x0E	to DL

6.10.2.2 UPtoDL.InfoPowerParamCCH

UPtoDL.InfoPowerParamCCH has many parameters. The meaning of each parameter is shown in Table 15.

Table 15 — Parameters of UPtoDL.InfoPowerParamCCH

Parameter name	bits	Description
PmaxCCH	7	Max CCH transmission power, -40dBm(0) ~ 40dBm(80)
PminCCH	7	Min CCH transmission power, -40dBm(0) ~ 40dBm(80)
PtargetCCH	5	PtargetCCH is the target reception power of the CCH. -110dBm(0) ~ 79dBm(31)
PmarginCCH	4	Control channel power margin, 0 dB(0)~15 dB(15)
PmaxTCH	7	Max TCH transmission power, -43dBm(0) ~ 37dBm(80)
PmarginTCH	4	Power margin of tone channel mapped with the control channel, 0 dB(0)~15 dB(15)
PTX_CCHTCH_differ	4	Difference between subchannel transmission power and tone channel transmission power, -15 dB(0)~0 dB(15)
PoffCtoD	4	Power offset used when the controller specifies the UA's initial transmit power, 0 dB(0)~15 dB(15)
SNRrequiredCCH	4	Required SNR of control channel, 0 dB(0)~15 dB(15)
PRXtoneCompeteThre	5	The detection threshold of the tone subslot performing competition, -115dBm(0) ~ -84dBm(31)