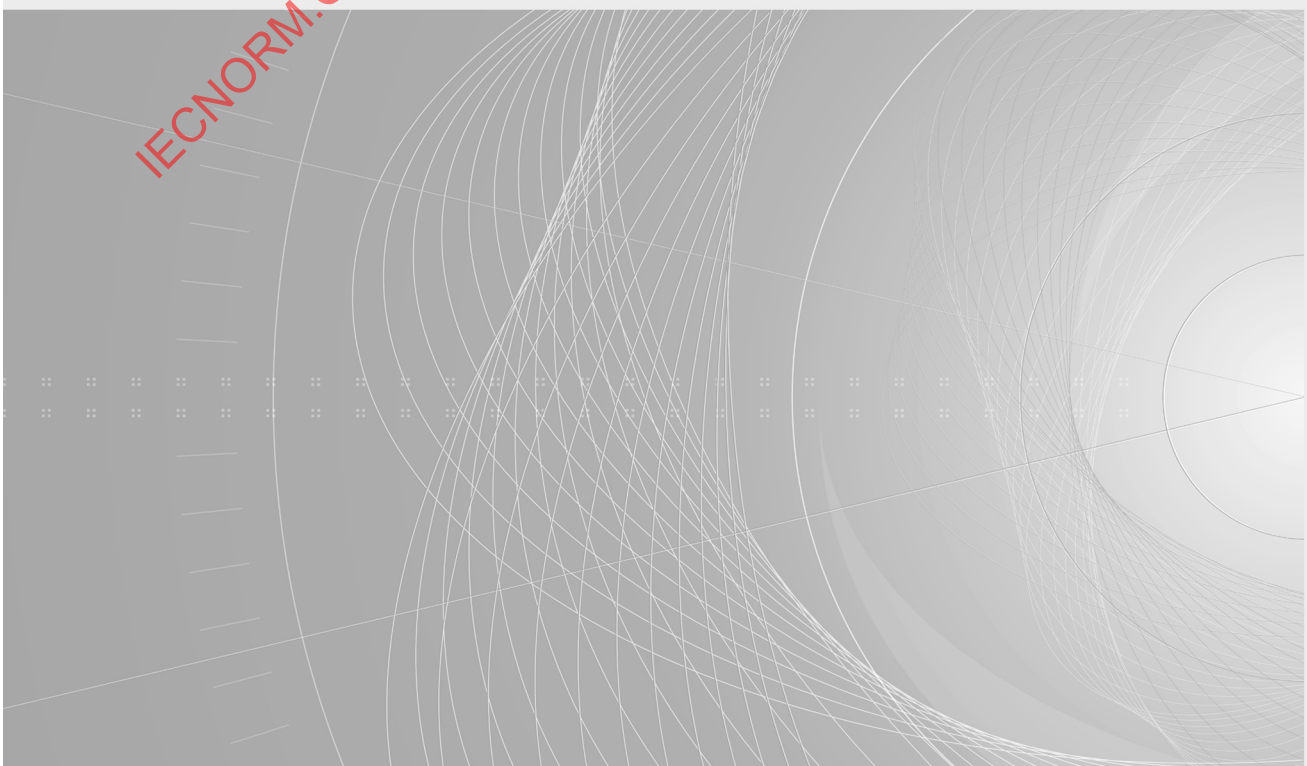
ISO/IEC 24739-1

Edition 1.0 2009-09

INTERNATIONAL STANDARD

Information technology – AT attachment with packet interface-7 –
Part 1: Register delivered command set, logical register set (ATA/ATAPI-7 V1)



ISO/IEC 24739-1:2009(E)

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INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 1: Register delivered command set, logical register set (ATA/ATAPI-7 V1)

FOREWORD

1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards. Their preparation is entrusted to technical committees; any ISO and IEC member body interested in the subject dealt with may participate in this preparatory work. International governmental and non-governmental organizations liaising with ISO and IEC also participate in this preparation.

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International Standard ISO/IEC 24739-1 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

The list of all currently available parts of the ISO/IEC 24739 series, under the general title *Information technology – AT attachment with packet interface-7,* can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies, and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

ISO/IEC 24739-1 is to be used in conjunction with ISO/IEC 24739-2 and ISO/IEC 24739-3.

The contents of the corrigendum of September 2013 have been included in this copy.

INTRODUCTION

ISO/IEC 24739 defines the AT attachment with packet interface (ATAPI). The standard includes the command set and two transport protocols to support parallel and serial physical interconnects. ISO/IEC 24739 is partitioned into three parts:

Part 1: Register delivered command set, logical register set (ATA/ATAPI-7 V1)

Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7 V2)

Part 3: Serial transport protocols and physical interconnect (ATA/ATAPI-7 V3)

ISO/IEC 24739 is partitioned in this way to separate the command set (Part 1) for ease of reference and maintenance. The command set is the same for both the parallel transport (Part 2) and the serial transport (Part 3).

Parts 1 and Part 2 were substantially derived from the prior version of this standard (ATA/ATAPI-6, ANSI INCITS 361-2002). Part 3 is new material defining the serial transport of the ATA/ATAPI interface.

All three parts have a clause that includes introductory material, a common glossary and an index to the major clauses of the other two parts. After Clause 3 in each of the parts, the material is part specific. Within each part, references are made to other parts, given with the full reference of the publication and major clause number, e.g. ISO/IEC 24739-3, Clause 4.

In order to implement the standard for a parallel transport, it is necessary to comply with both ISO/IEC 24739-1 and ISO/IEC 24739-2. In order to implement the serial transport, it is necessary to comply with both ISO/IEC 24739-1 and ISO/IEC 24739-3. It should be recognized, however, that the serial transport as described in ISO/IEC 24739-3 relies heavily on logical interconnect and protocol concepts and requirements described in ISO/IEC 24739-2. These concepts are called "parallel emulation" in ISO/IEC 24739-3. In some cases, references are made to the parallel implementation of ATA, which refers to the parallel transport (ISO/IEC 24739-2). The reader is strongly advised to consult all three parts when implementing the serial transport.

This International Standard (ISO/IEC 24739-1) contains the command feature sets for ATA. It defines structures used by the parallel implementation of ATA and the serial implementation of ATA. The command descriptions are in alphabetical order, with a cross-reference by command codes in Annex A.

The ISO/IEC 24739 series of standards consists of the following parts and clauses:

Part 1

Clause 1 describes the scope.

Clause 2 provides normative references for the entire standard.

Clause 3 provides definitions, abbreviations and conventions used within the entire standard.

Clause 4 describes the general operating requirements of the command layer.

Clause 5 describes the I/O registers.

Clause 6 contains descriptions of the commands.

Clauses 7 through 12 point to the material in ISO/IEC 24739-2.

Clauses 13 through 19 point to material in ISO/IEC 24739-3.

Part 2

Clause 1 describes the scope.

Clause 2 provides normative references for the entire standard.

Clause 3 provides definitions, abbreviations and conventions used within the entire standard.

Clauses 4, 5 and 6 point to the material in ISO/IEC 24739-1.

Clause 7 contains the electrical and mechanical characteristics.

Clause 8 contains the signal descriptions.

Clause 9 describes the general operating requirements of the physical, data link and transport layers.

Clause 10 contains describes register addressing.

Clause 11 contains the transport protocols.

Clause 12 contains the interface timing diagrams.

Clauses 13 through 19 point to material in ISO/IEC 24739-3.

Part 3

Clause 1 describes the scope.

Clause 2 provides normative references for the entire standard.

Clause 3 provides definitions, abbreviations and conventions used within the entire standard.

Clauses 4, 5 and 6 point to the material in ISO/IEC 24739-1.

Clauses 7 through 12 point to the material in ISO/IEC 24739-2.

Clause 13 contains a general overview of the serial interface.

Clause 14 describes the serial physical layer.

Clause 15 describes the serial link layer.

Clause 16 describes the serial transport layer.

Clause 17 describes the device command layer protocol for the serial interface.

Clause 18 describes the host command layer protocol for the serial interface.

Clause 19 describes the serial interface host adapter register interface.

Clause 20 describes the serial interface error handling.

INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 1: Register delivered command set, logical register set (ATA/ATAPI-7 V1)

1 Scope

This part of ISO/IEC 24739 specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers and suppliers of intelligent storage devices.

ISO/IEC 24739-1 defines the register delivered commands used by devices implementing the standard. ISO/IEC 24739-2 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals and the protocols for the transporting of commands, data and status over the interface for the parallel interface. ISO/IEC 24739-3 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals and the protocols for the transporting of commands, data and status over the interface for the serial interface. Figure 1 shows the relationship of these documents. For devices implementing the PACKET command feature set, additional command layer standards are listed in Table 1 and described in Clause 2.

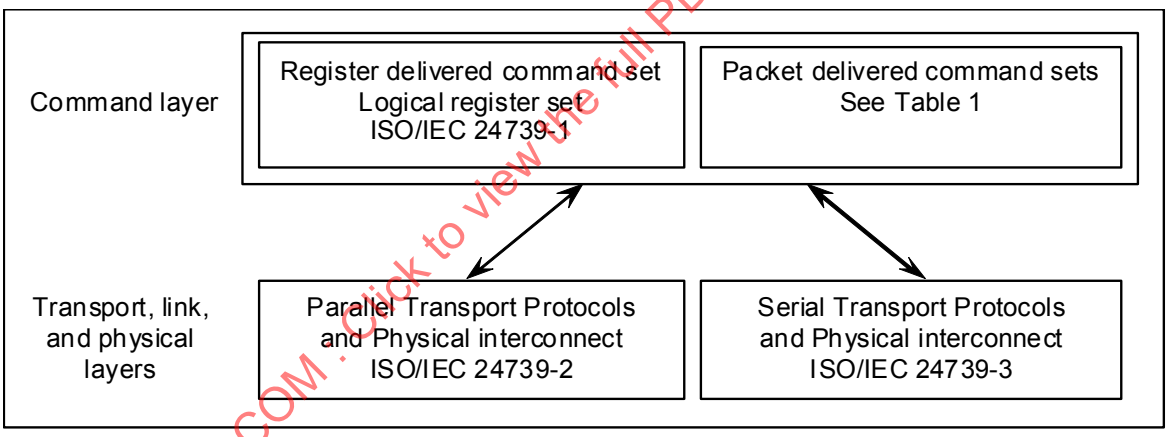


Figure 1 – ATA document relationships

Table 1 – PACKET delivered command sets

Standard
SCSI Primary Commands (SPC)
ISO/IEC 14776-452, SCSI Primary Commands 2 (SPC-2)
ISO/IEC 14776-453, SCSI Primary Commands-3 (SPC-3)
ISO/IEC 14776-322, SCSI Block Commands (SBC-2)
ISO/IEC 14776-331, SCSI Stream Commands (SSC)
Multimedia Commands (MMC)
ISO/IEC 14776-362, Multimedia Commands-2 (MMC-2)
ISO/IEC 14776-363, Multimedia Commands-3 (MMC-3)
ISO/IEC 14776-364: Multimedia Commands-4 (MMC-4)
ATAPI for Removable Media (SFF8070I)
ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D

This standard maintains compatibility with the AT Attachment with packet interface-6 standard (ATA/ATAPI-6), ANSI INCITS 361-2002, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references only the edition cited applies. For undated references the latest edition (including any amendments) applies.

ISO/IEC 14776-321, *Information technology – Small computer system interface (SCSI-3) – Part 321: Block commands (SBC)* [ANSI INCITS 306-1998 (R2003)]

ISO/IEC 14776-322, *Information technology – Small computer system interface (SCSI) – Part 322: Block commands-2 (SBC-2)* [T10/1417-D]

ISO/IEC 14776-331, *Information technology – Small computer system interface (SCSI) – Part 331: Stream commands (SSC)* [ANSI INCITS 335-2000]

ISO/IEC 14776-362, *Information technology – Small computer system interface (SCSI) – Part 362: Multimedia commands-2 (MMC-2)* [ANSI INCITS 333-2000]

ISO/IEC 14776-363, *Information technology – Small computer system interface (SCSI) – Part 363: Multimedia commands-3 (MMC-3)* [ANSI INCITS 360-2002]
(under consideration)

ISO/IEC 14776-364, *Information technology – Small computer system interface (SCSI) – Part 364: Multimedia commands-4 (MMC-4)* [T10/1545D]
(under consideration)

ISO/IEC 14776-452, *Information technology – Small computer system interface (SCSI) – Part 452: Primary commands-2 (SPC-2)* *[ANSI INCITS 351-2001]*

ISO/IEC 14776-453, *Information technology – Small computer system interface (SCSI) – Part 453: Primary commands-3 (SPC-3)* [T10/1416-D]
(under consideration)

ISO/IEC 13213:1994, *Information technology – Microprocessor systems – Control and Status Register (CSR) Architecture for microprocessor buses*

ISO 7779:1999, *Acoustics – Measurement of airborne noise emitted by information technology and telecommunications equipment*

AT Attachment with Packet Interface Extension (ATA/ATAPI-4)[ANSI INCITS 317-1998] (R2003)

SCSI-3 Primary Commands (SPC) [ANSI INCITS 301-1997 (R2002)]

Multimedia Commands (MMC) [ANSI INCITS 304-1997 (R2002)]

Protected Area Run Time Interface Extensions (PARTIES) [ANSI INCITS 346-2001]

ATAPI for Rewritable Media (under development) [SFF-8070i]

3 Definitions, abbreviations and conventions

3.1 Definitions and abbreviations

For the purposes of this standard, the following definitions apply.

3.1.1
ASCII Character
designates 8-bit value that is encoded using the ASCII character set

3.1.2
acoustics
measurement of airborne noise emitted by information technology and telecommunications equipment [see ISO 7779:1999(E)]

3.1.3
ATA (AT Attachment)
ATA defines the physical, electrical, transport and command protocols for the internal attachment of storage devices to host systems

3.1.4
ATA-1 device
device that complied with ANSI X3.221-1994, the AT Attachment interface for disk drives

NOTE ANSI X3.221-1994 has been withdrawn.

3.1.5
ATA-2 device
device that complied with ANSI X3.279-1996, the AT Attachment interface with extensions

NOTE ANSI X3.279-1996 has been withdrawn.

3.1.6
ATA-3 device
device that complies with ANSI INCITS 298-1997, the AT Attachment-3 Interface

NOTE ANSI INCITS 298-1997 has been withdrawn.

3.1.7
ATA/ATAPI-4 device
device that complies with ANSI INCITS 317-1998

NOTE For reference, see bibliography.

3.1.8
ATA/ATAPI-5 device
device that complies with ANSI INCITS 340-2000

NOTE For reference, see bibliography.

3.1.9
ATA/ATAPI-6 device
device that complies with ANSI INCITS 361-2002

NOTE For reference, see bibliography.

3.1.10
ATA/ATAPI-7 device
device that complies with this standard

3.1.11
ATAPI (AT Attachment Packet Interface) device
device implementing the Packet Command feature set

3.1.12
AU (Allocation Unit)
minimum number of logically contiguous sectors on the media as used in the Streaming feature set

NOTE An Allocation Unit may be accessed with one or more requests.

3.1.13
AV (Audio-Video)
Audio-Video applications use data that is related to video images and/or audio; the distinguishing characteristic of this type of data is that accuracy is of lower priority than timely transfer of the data

3.1.14
backchannel
when transmitting a FIS, the backchannel is the receive channel

3.1.15
BER (bit error rate)
the statistical probability of a transmitted encoded bit being erroneously received in a communication system

3.1.16
bus release
for devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed; this allows the host to select the other device or deliver another queued command

3.1.17
byte count
value placed in the Byte Count register by the device to indicate the number of bytes to be transferred during this DRQ assertion when executing a PACKET PIO data transfer command

3.1.18
byte count limit
value placed in the Byte Count register by the host as input to a PACKET PIO data transfer command to specify the maximum byte count that may be transferred during a single DRQ assertion

3.1.19
CFA (CompactFlash™ Association)
the CompactFlash™ Association which created the specification for compact flash memory that uses the ATA interface

(CompactFlash™ is a registered trade mark of the CompactFlash™ Association)

3.1.20
check condition
for devices implementing the PACKET Command feature set, this indicates an error or exception condition has occurred

3.1.21
CHS (cylinder-head-sector)
obsolete method of addressing the data on the device by cylinder number, head number and sector number

3.1.22
code violation
in a serial interface implementation, a code violation is an error that occurs in the decoding of an encoded character (see ISO/IEC 24739-3, Clause 15)

3.1.23
command aborted
command completion with ABRT set to one in the Error register and ERR set to one in the Status register

3.1.24
command acceptance
a command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the Status register and the host writes to the Command register

NOTE An exception exists for the DEVICE RESET command (see Clause 6). In a serial implementation, command acceptance is a positive acknowledgment of a host to device register FIS.

3.1.25
Command Block registers
interface registers used for delivering commands to the device or posting status from the device; in a serial implementation, the command block registers are FIS payload fields

3.1.26
command completion
completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the Error register, the placing of the appropriate status bits in the Status register, the clearing of both BSY and DRQ to zero, and Interrupt Pending

3.1.27
command packet
data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters

3.1.28
command released
when a device supports overlap or queuing, a command is considered released when a bus release occurs before command completion

3.1.29
Control Block registers
in a parallel implementation, interface registers used for device control and to post alternate status
in a serial interface implementation, the logical field of a FIS corresponding to the Device Register bits of a parallel implementation

3.1.30
control character
in a serial interface implementation, an encoded character that represents a non-data byte (see ISO/IEC 24739-3, Clause 15)

3.1.31
CRC (Cyclical Redundancy Check)
a means used to check the validity of certain data transfers

3.1.32
Cylinder High register
name used for the LBA High register in previous ATA/ATAPI standards

3.1.33
Cylinder Low register
name used for the LBA Mid register in previous ATA/ATAPI standards

3.1.34
data character
in a serial interface implementation, an encoded character that represents a data byte. (See ISO/IEC 24739-3, Clause 15)

3.1.35
data-in
protocol that moves data from the device to the host; such transfers are initiated by READ commands

3.1.36
data-out
protocol that moves data from the host to the device; such transfers are initiated by WRITE commands

3.1.37
Delayed LBA
any sector for which the performance specified by the Streaming Performance Parameters log is not valid

3.1.38
device
a storage peripheral

NOTE Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.

3.1.39
device selection
in a parallel implementation, a device is selected when the DEV bit of the Device register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal

in a serial implementation the device ignores the DEV bit, the host adapter may use this bit to emulate device selection

3.1.40
disparity
difference between the number of ones and the number of zeroes in an encoded character (see ISO/IEC 24739-3, Clause 15)

3.1.41
DMA (direct memory access) data transfer
a means of data transfer between device and host memory without host processor intervention

3.1.42
don't care
indicates that a value is irrelevant for the particular function described

3.1.43
driver
active circuit inside a device or host that sources or sinks current to assert or negate a signal on the bus

3.1.44
DRQ data block
a unit of data words transferred during a single assertion of DRQ when using PIO data transfer

3.1.45
elasticity buffer
in a serial interface implementation, a portion of the receiver where character slipping and/or character alignment is performed

3.1.46
encoded character
in a serial interface implementation, the output of the 8b/10b encoder (see ISO/IEC 24739-3, Clause 15)

3.1.47
First party DMA access
method by which a device accesses host memory

NOTE First party DMA differs from DMA in that the device sends a DMA Setup FIS to select host memory regions; whereas for DMA the host configures the DMA controller.

3.1.48
FIS (Frame Information Structure)
data structure that is the payload of a frame and does not include the SOF primitive, CRC and EOF primitive

3.1.49
frame
unit of information exchanged between the host adapter and a device

NOTE A frame consists of an SOF primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS and an EOF primitive.

3.1.50
FUA (Forced Unit Access)
requires that user data be transferred to or from the device media before command completion even if caching is enabled

3.1.51
Gen1 DWORD Time
the time it takes to transmit a 40 bit encoded value at 1,5 Gbit/s

3.1.52
host
the computer system executing the software BIOS and/or operating system device driver controlling the device and the adapter hardware for the ATA interface to the device

3.1.53
host adapter
the implementation of the host transport, link and physical layers

3.1.54
Interrupt Pending
in a parallel implementation, an internal state of a device; in this state, the device asserts INTRQ if nIEN is cleared to zero and the device is selected (see Clause 8)

in a serial implementation, the Interrupt Pending state is an internal state of the host adapter; this state is entered by reception of a FIS with the I field set to one (see ISO/IEC 24739-3, Clause 16)

3.1.55
LBA (logical block address)
the addressing of data on the device by the linear mapping of sectors

3.1.56
LFSR (Linear Feedback Shift Register)
(See ISO/IEC 24739-3, Clause 15)

3.1.57
link
the link layer manages the phy layer to achieve the delivery and reception of frames (see ISO/IEC 24739-3, Clause 15)

3.1.58
logical sector
a uniquely addressable set of 256 words (512 bytes)

3.1.59
native max address
the highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command

3.1.60
overlap
a protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device (if present) on the bus

3.1.61
packet delivered command
a command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters

NOTE See also register delivered command.

3.1.62
phy
physical layer electronics (see ISO/IEC 24739-3, Clause 14)

3.1.63
physical sector
a group of contiguous logical sectors that are read from or written to the device media in a single operation

3.1.64
PIO (programmed input/output) data transfer
PIO data transfers are performed by the host processor utilizing accesses to the Data register

3.1.65
primitive
in a serial interface implementation, a single DWORD of information that consists of a control character in byte 0 followed by three additional data characters in byte 1 through 3

3.1.66
queued
command queuing allows the host to issue concurrent commands to the same device

NOTE Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred but command completion has not occurred.

3.1.67
read command
a command that causes the device to transfer data from the device to the host (e.g., READ SECTOR(S), READ DMA, etc.)

3.1.68
regiser
a register may be a physical hardware register or a logical field

3.1.69
register delivered command
command that is delivered to the device by placing the command and all of the parameters for the command in the device Command Block registers

NOTE See also packet delivered command.

3.1.70
register transfers
host reading and writing any device register except the Data register; register transfers are 8 bits wide

3.1.71
released
in a parallel interface implementation, indicates that a signal is not being driven

NOTE For drivers capable of assuming a high-impedance state, this means that the driver is in the high-impedance state. For open-collector drivers, the driver is not asserted.

3.1.72
sector
uniquely addressable set of 256 words (512 bytes)

3.1.73
Sector Number register
LBA Low register in previous ATA/ATAPI standards

3.1.74
Shadow Command Block
in a serial interface implementation, a set of virtual fields in the host adapter that map the Command Block registers defined at the command layer to the fields within the FIS content

3.1.75
Shadow Control Block
in a serial interface implementation, a set of virtual fields in the host adapter that map the Control Block registers defined at the command layer to the fields within the FIS content

3.1.76
signature
unique set of values placed in the Command Block registers by the device to allow the host to distinguish devices implementing the PACKET Command feature set from those devices not implementing the PACKET Command feature set

3.1.77
SMART (Self-Monitoring, Analysis and Reporting Technology)
for prediction of device degradation and/or faults

3.1.78
transport
the transport layer manages the lower layers (link and phy) as well as constructing and parsing FISs (see ISO/IEC 24739-3, Clause 13)

3.1.79
Ultra DMA burst
the period from an assertion of DMACK− to the subsequent negation of DMACK− when an Ultra DMA transfer mode has been enabled by the host

3.1.80
unaligned write
write command that does not start at the first logical sector of a physical sector or does not end at the last logical sector of a physical sector

3.1.81
unit attention condition
state that a device implementing the PACKET Command feature set maintains while the device has asynchronous status information to report to the host

3.1.82
unrecoverable error
when the device sets either the ERR bit or the DF bit to one in the Status register at command completion

3.1.83
VS (Vendor Specific)
bits, bytes, fields and code values that are reserved for vendor specific purposes

NOTE 1 These bits, bytes, fields, and code values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE 2 Industry practice could result in conversion of a Vendor Specific bit, byte, field or code value into a defined standard value in a future standard.

3.1.84
write command
command that causes the device to transfer data from the host to the device (e.g., WRITE SECTOR(S), WRITE DMA, etc.)

3.1.85
WWN (world wide name)
a 64-bit worldwide unique name based upon a company's IEEE identifier (see IDENTIFY DEVICE Words 108 to 111 in ISO/IEC 24739-1, Clause 6)

3.2 Abbreviations

ABRT	Abort
a/r	As Required
BSY	Busy
CCTL	Command Completion Time Limit
C/D	Command/Data
CFA	Compact Flash Association
DASP	Drive Active / Slave Present
DD	Device Data
DEV	Device
DF	Device fault
DF/SE	Device Fault / Stream Error
DIOW	Device Input Output Write
DMA	Direct Memory Access
DMACK	DMA aknowledge
DMARQ	DMA request
DRDY	Device ready
DRQ	Date Request
ECC	Error Correcting Code
ENB	Enable
ERR	Errror
ERR/CHK	Error check
FIFO	First in / First Out
HOB	High Order Bit
ID	Identification
IEEE OUI	Institute of Electrical and Electronics Engineers Organization Unique Identifier
INTRQ	Interupt Request
I/O	Input / Output
LBA	Logical Block Address
na	Not Applicable
NAA	Network Address Authority
nIEN	Negative Interupt Enable
NM	No media
NOP	No Operation
obs	Obsolete
OVL	Overlap
PDIAG	Passed Diagnostics
PIO	programmed input/output
REL	Release
R/W	Read / Write
SERV	Service

SRST Soft Reset

3.3 Conventions

3.3.1 General

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in Clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.3.7 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., LBA Mid register).

The expression “word n” or “bit n” shall be interpreted as indicating the content of word n or bit n.

3.3.2 Precedence

If there is a conflict between text, figures and tables, the precedence shall be tables, figures and then text.

3.3.3 Lists

Ordered lists, those lists describing a sequence, are of the form:

a)
b)
c)

Unordered list are of the form:

1)
2)
3)

3.3.4 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

3.2.4.1
expected
A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

3.2.4.2
mandatory
A keyword indicating items to be implemented as defined by this standard.

3.2.4.3
may
A keyword that indicates flexibility of choice with no implied preference.

3.2.4.4
obsolete
A keyword indicating that the designated bits, bytes, words, fields and code values that may have been defined in previous standards are not defined in this standard and shall not be reclaimed for other uses in future standards. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility.

Obsolete commands should not be used by the host. Commands defined as obsolete may be command aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

3.2.4.5
optional
A keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

3.2.4.6
prohibited
A keyword indicating that an item shall not be implemented by an implementation.

3.2.4.7
reserved
A keyword indicating reserved bits, bytes, words, fields and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

3.2.4.8
retired
A keyword indicating that the designated bits, bytes, words, fields and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, words, fields or code values are used before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

3.2.4.9
shall
A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

3.2.4.10
should
A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

3.3.5 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

3.3.6 Signal conventions

Signal names are shown in all uppercase letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates the signal is a low active signal. A low active signal is true when the signal is below V_{iL}, and is false when the signal is above V_{iH}. No dash at the end of a signal name indicates the signal is a high active signal. A high active signal is true when the signal is above V_{iH}, and is false when the signal is below V_{iL}.

“Asserted” means that the signal is driven by an active circuit to the true state. Negated means that the signal is driven by an active circuit to the false state. “Released” means that

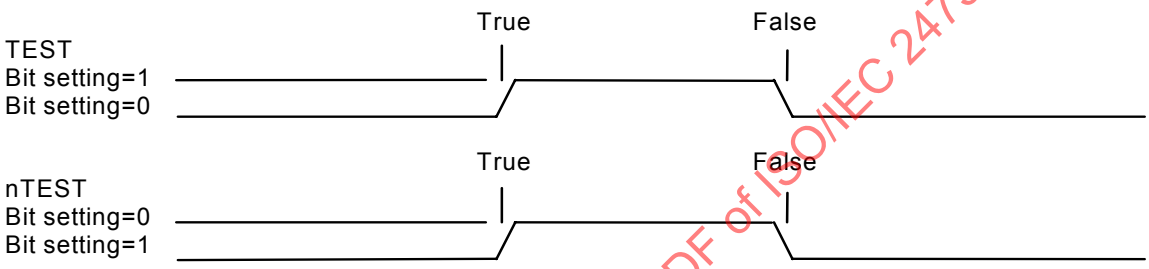
the signal is not actively driven to any state (see clause 6). Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal.

Control signals that may be used for more than one mutually exclusive functions are identified with their function names separated by a colon (e.g., DIOW-:STOP).

SIGNAL(n:m) denotes a set of signals, for example, DD(15:0).

3.3.7 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true, and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero the meaning of the bit is true and when nBIT is set to one the meaning of the bit is false.



Bit (n:m) denotes a set of bits, for example, bits (7:0).

3.3.8 State diagram conventions

State diagrams shall be as shown in Figure 2.

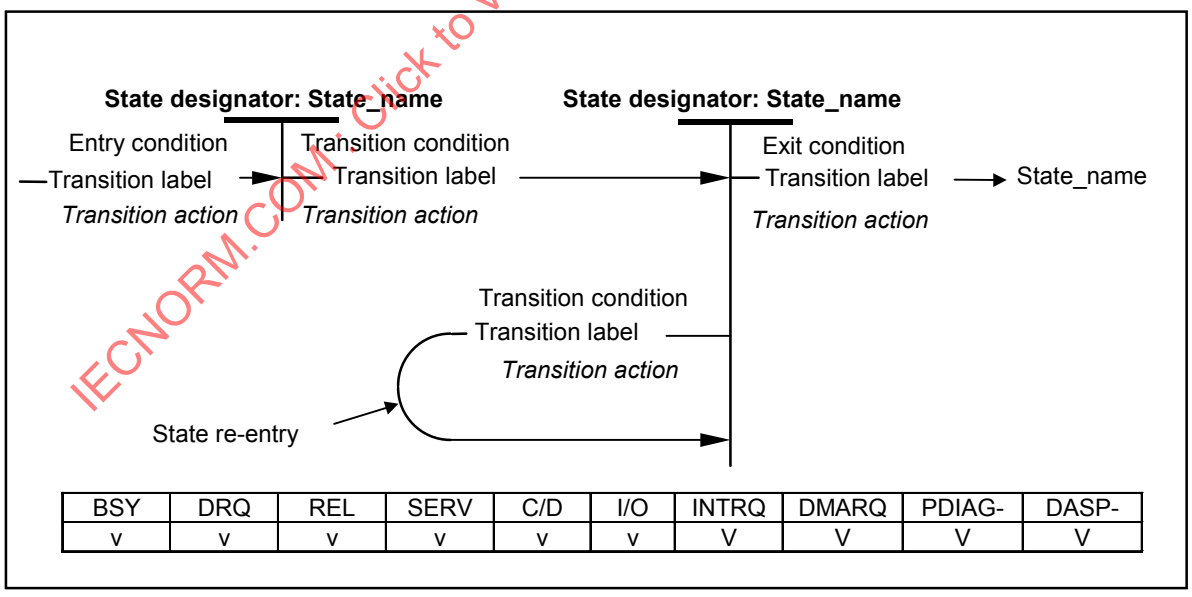


Figure 2 – State diagram convention

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized in the title of the figure containing the state diagram followed by a unique number. The state name is a brief description of the primary action taken during the state, and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique

letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

In device command protocol state diagrams, the state of bits and signals that change state during the execution of this state diagram are shown under the state designator:state_name, and a table is included that shows the state of all bits and signals throughout the state diagram as follows:

v = bit value changes

1 = bit set to one

0 = bit cleared to zero

x = bit is don't care

V = signal changes

A = signal is asserted

N = signal is negated

R = signal is released

X = signal is don't care.

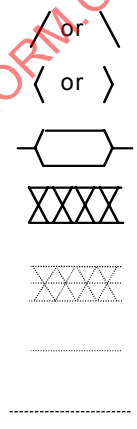
Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made followed by the state designator of the state to which the transition is being made. In some cases, the transition to enter or exit a state diagram may come from or go to a number of state diagrams, depending on the command being executed. In this case, the state designator is labeled xx. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action, indicated in italics, that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

Transitions from state to state shall be instantaneous.

3.3.9 Timing conventions

Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.

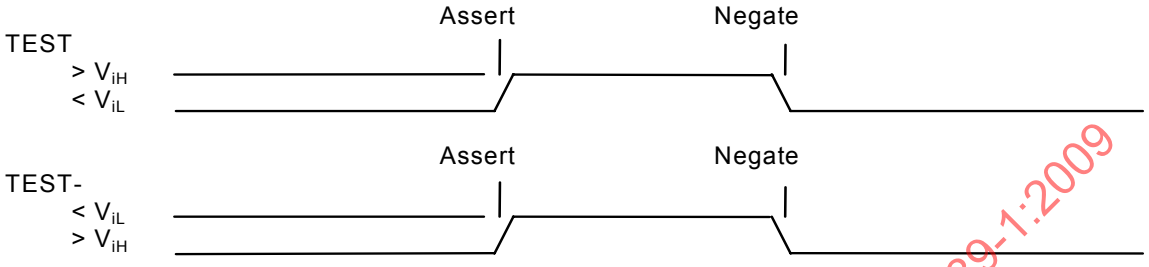


- signal transition (asserted or negated)
- data transition (asserted or negated)
- data valid
- undefined but not necessarily released
- asserted, negated or released
- released
- the "other" condition if a signal is shown with no change

All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent on electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



3.3.10 Byte ordering for data transfers

Data is transferred in blocks using either PIO or DMA protocols. PIO data transfers occur when the BSY bit is cleared to zero and the DRQ bit is set to one. These transfers are usually 16-bit but CFA devices may implement 8-bit PIO transfers. Data is transferred in blocks of one or more bytes known as a DRQ block. DMA data transfers occur when the host asserts DMACK− in response to the device asserting DMARQ. DMA transfers are always 16-bit. Each assertion of DMACK− by the host defines a DMA data burst. A DMA data burst is two or more bytes.

Assuming a DRQ block or a DMA burst of data contains "n" bytes of information, the bytes are labeled Byte(0) through Byte(*n*-1), where Byte(0) is first byte of the block, and Byte(*n*-1) is the last byte of the block. Table 2 shows the order the bytes shall be presented in when such a block of data is transferred on the interface using 16-bit PIO and DMA transfers. Table 3 shows the order the bytes shall be presented in when such a block or burst of data is transferred on the interface using 8-bit PIO.

Table 2 – Byte order

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (*n*-1)								Byte (*n*-2)							

Table 3 – Byte order

	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (0)							
Second transfer	Byte (1)							
.....								
Last transfer	Byte (*n*-1)							

NOTE The above description is for data on the interface. Host systems and/or host adapters may cause the order of data as seen in the memory of the host to be different.

Some parameters are defined as a string of ASCII characters. ASCII data fields shall contain only code values 20h through 7Eh. For the string “Copyright”, the character “C” is the first byte, the character “o” is the second byte, etc. When such fields are transferred, the order of transmission is:

the 1st character (“C”) is on DD(15:8) of the first word,

the 2nd character (“o”) is on DD(7:0) of the first word,

the 3rd character (“p”) is on DD(15:8) of the second word,

the 4th character (“y”) is on DD(7:0) of the second word,

the 5th character (“r”) is on DD(15:8) of the third word,

the 6th character (“i”) is on DD(7:0) of the third word,

the 7th character (“g”) is on DD(15:8) of the fourth word,

the 8th character (“h”) is on DD(7:0) of the fourth word,

the 9th character (“t”) is on DD(15:8) of the fifth word,

the 10th character (“space”) is on DD(7:0) of the fifth word,

etc.

Word (n:m) denotes a set of words, for example, words 100 to 103.

3.3.11 Byte, word and DWORD relationships

Figure 3 illustrates the relationship between bytes, words and DWORDs for serial interface implementations.

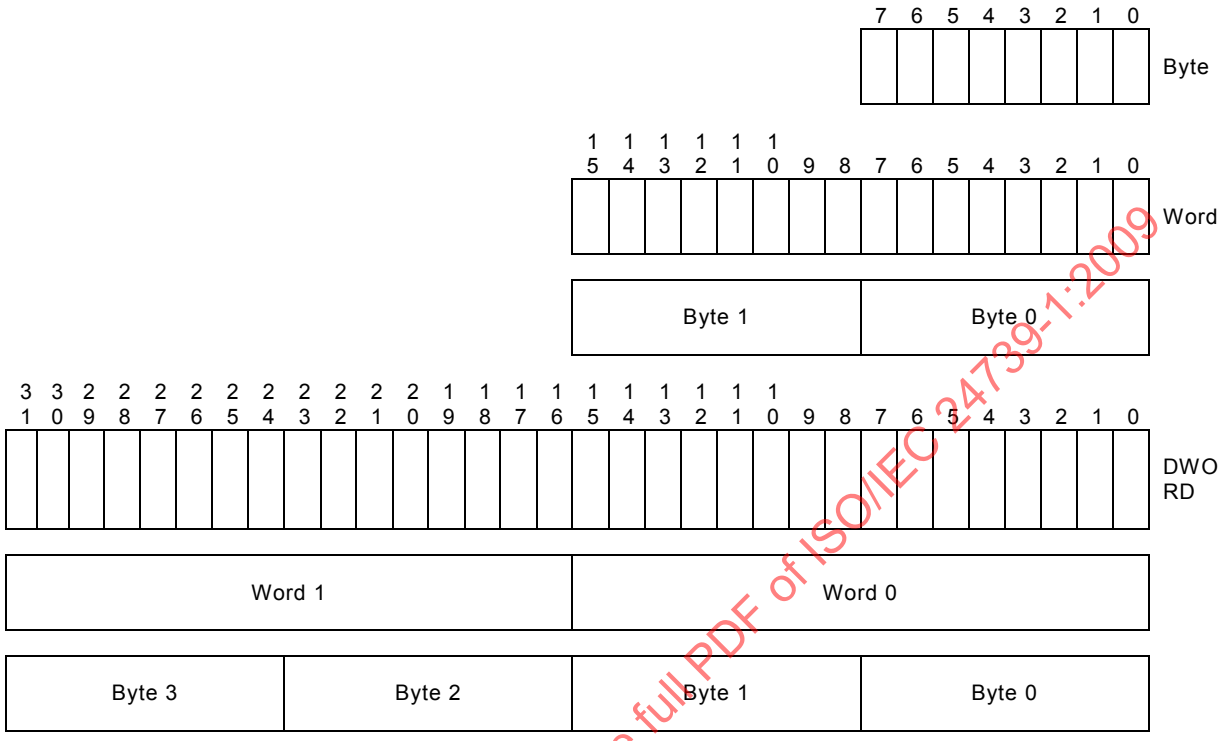


Figure 3 – Byte, word and DWORD relationships

4 General operational requirements

4.1 Command delivery

Commands may be delivered in two forms. For devices that do not implement the PACKET Command feature set, all commands and command parameters are delivered by writing the device Command Block registers. Such commands are defined as register delivered commands.

Devices that implement the PACKET Command feature set use packet delivered commands as well as some register delivered commands.

All register delivered commands and the PACKET command are described in Clause 5.

NOTE The content of command packets delivered during execution of the PACKET command are not described in this standard. See Clause 2 for standards and specifications that define command packet content.

4.2 Register delivered data transfer command sector addressing

4.2.1 General

For register delivered data transfer commands all addressing of data sectors recorded on the device's media is by a logical sector address. There is no implied relationship between logical sector addresses and the actual physical location of the data sector on the media. All devices shall support LBA translation.

In standards ATA/ATAPI-5 and earlier, a CHS translation was defined. This translation is obsolete but if implemented it shall be implemented as defined in ATA/ATAPI-5.

4.2.2 Definitions and value ranges of IDENTIFY DEVICE data words

(Also see 6.17)

1) Words 60 to 61 shall contain the value one greater than the total number of user-addressable sectors in 28-bit addressing and shall not exceed 0FFFFFFFh. The content of words 60 to 61 shall be greater than or equal to one and less than or equal to 268,435,455.
2) Words 100 to 103 shall contain the value one greater than the total number of user-addressable sectors in 48-bit addressing and shall not exceed 0000FFFFFFFFFFFFh.
3) The contents of words 60 to 61 and 100 to 103 may be affected by the host issuing a SET MAX ADDRESS or SET MAX ADDRESS EXT command.
4) The contents of words 60 to 61 and 100 to 103 shall not be used to determine if 48-bit addressing is supported. IDENTIFY DEVICE bit 10 word 83 indicates support for 48-bit addressing.

4.2.3 Addressing constraints and error reporting

Devices shall set IDNF to one or ABRT to one in the Error register and ERR to one in the Status register in response to any command where the requested LBA number is greater than or equal to the content of words 60 to 61 for a 28-bit addressing command or greater or equal to the contents of words 100 to 103 for a 48-bit addressing command.

4.3 General feature set

4.3.1 General

The General feature set defines the common commands implemented by devices.

4.3.2 General feature set for devices not implementing the PACKET command feature set

The following General feature set commands are mandatory for all devices that are capable of both reading and writing their media and do not implement the PACKET command feature set:

- EXECUTE DEVICE DIAGNOSTIC
- FLUSH CACHE
- IDENTIFY DEVICE
- READ DMA
- READ MULTIPLE
- READ SECTOR(S)
- READ VERIFY SECTOR(S)
- SET FEATURES
- SET MULTIPLE MODE
- WRITE DMA
- WRITE MULTIPLE
- WRITE SECTOR(S)

The following General feature set commands are mandatory for all devices that are capable of only reading their media and do not implement the PACKET command feature set:

- EXECUTE DEVICE DIAGNOSTIC
- IDENTIFY DEVICE
- READ DMA
- READ MULTIPLE
- READ SECTOR(S)
- READ VERIFY SECTOR(S)

- SET FEATURES
- SET MULTIPLE MODE

The following General feature set commands are optional for devices not implementing the PACKET command feature set:

- DOWNLOAD MICROCODE
- NOP
- READ BUFFER
- WRITE BUFFER

The following General feature set command is prohibited for use by devices not implementing the PACKET command feature set:

- DEVICE RESET

The following resets are mandatory for devices not implementing the PACKET command feature set:

- Power-on reset: Executed at power-on, the device may execute a series of diagnostics and shall set default values (see Clauses 11 and 17)
- Hardware reset: Executed in response to the assertion of the RESET- signal the device may execute a series of diagnostics and shall set default values (see Clauses 11 and 17).
- Software reset: Executed in response to the setting of the SRST bit in the Device Control register the device resets the interface circuitry (see Clauses 11 and 17).

4.3.3 General feature set for devices implementing the PACKET command feature set

The following General feature set commands are mandatory for all devices implementing the PACKET command feature set:

- EXECUTE DEVICE DIAGNOSTIC
- IDENTIFY DEVICE
- NOP
- READ SECTOR(S)
- SET FEATURES

The following General feature set commands are optional for all devices implementing the PACKET command feature set:

- FLUSH CACHE

The following General command set commands are prohibited for use by devices implementing the PACKET command feature set. These functions are supported by Packet commands.

- DOWNLOAD MICROCODE
- READ BUFFER
- READ DMA
- READ MULTIPLE
- READ VERIFY
- SET MULTIPLE MODE
- WRITE BUFFER
- WRITE DMA
- WRITE MULTIPLE
- WRITE SECTOR(S)

The following resets are mandatory for devices implementing the PACKET command feature set:

- Power-on reset: Executed at power-on, the device may execute a series of diagnostics and shall set default values (see clause 11).
- Hardware reset: Executed in response to the assertion of the RESET- signal the device may execute a series of and shall set default values (see clause 11).
- Software reset: Executed in response to the setting of the SRST bit in the Device Control register the device resets the interface circuitry (see clause 11).
- DEVICE RESET: Executed in response to the DEVICE RESET command the device resets the interface circuitry (see 6.11).

4.4 PACKET Command feature set

4.4.1 General

The optional PACKET Command feature set provides for devices that require command parameters that are too extensive to be expressed in the Command Block registers. Devices implementing the PACKET Command feature set exhibit responses different from those exhibited by devices not implementing this feature set.

The commands unique to the PACKET Command feature set are:

- PACKET
- DEVICE RESET
- IDENTIFY PACKET DEVICE

4.4.2 Identification of PACKET Command feature set devices

When executing a power-on, hardware, DEVICE RESET or software reset, a device implementing the PACKET Command feature set shall perform the same reset protocol as other devices, but leaves the registers with a signature unique to PACKET Command feature set devices (see 5.15).

In addition, the IDENTIFY DEVICE command shall not be executed but shall be command aborted and shall return a signature unique to devices implementing the PACKET Command feature set. The IDENTIFY PACKET DEVICE command is used by the host to get identifying parameter information for a device implementing the PACKET Command feature set (see 6.17.5.2 and 6.18).

4.4.3 PACKET Command feature set resets

Devices implementing the PACKET Command feature set respond to power-on, hardware, and software resets as any other device except for the resulting contents in the device registers as described above. However, software reset should not be issued while a PACKET command is in progress. PACKET commands used by some devices do not terminate if a software reset is issued.

The DEVICE RESET command is provided to allow the device to be reset without affecting the other device on the bus.

4.4.4 The PACKET command

The PACKET command allows a host to send a command to the device via a command packet. The command packet contains the command and command parameters that the device is to execute.

Upon receipt of the PACKET command the device sets BSY to one and prepares to receive the command packet. When ready, the device sets DRQ to one and clears BSY to zero. The command packet is then transferred to the device by PIO transfer. When the last word of the command packet is transferred, the device sets BSY to one, and clears DRQ to zero (see 6.25 and clause 10 in ISO/IEC 24739-2).

4.5 Power Management feature set

4.5.1 General

A device shall implement power management. A device implementing the PACKET Command feature set may implement the power management as defined by the PACKET command set implemented by the device. Otherwise, the device shall implement the Power Management feature set as described in this standard.

The Power Management feature set permits a host to modify the behavior of a device in a manner that reduces the power required to operate. The Power Management feature set provides a set of commands and a timer that enable a device to implement low power consumption modes. A register delivered command device that implements the Power Management feature set shall implement the following minimum set of functions: See also 4.6 and 4.12.

- A Standby timer
- CHECK POWER MODE command
- IDLE command
- IDLE IMMEDIATE command
- SLEEP command
- STANDBY command
- STANDBY IMMEDIATE command

A device that implements the PACKET Command feature set and implements the Power Management feature set shall implement the following minimum set of functions:

- CHECK POWER MODE command
- IDLE IMMEDIATE command
- SLEEP command
- STANDBY IMMEDIATE command

4.5.2 Power management commands

The CHECK POWER MODE command allows a host to determine if a device is currently in, going to or leaving Standby or Idle mode. The CHECK POWER MODE command shall not change the power mode or affect the operation of the Standby timer.

The IDLE and IDLE IMMEDIATE commands move a device to Idle mode immediately from the Active or Standby modes. The IDLE command also sets the Standby timer count and enables or disables the Standby timer.

The STANDBY and STANDBY IMMEDIATE commands move a device to Standby mode immediately from the Active or Idle modes. The STANDBY command also sets the Standby timer count and enables or disables the Standby timer.

The SLEEP command moves a device to Sleep mode. The device's interface becomes inactive at command completion of the SLEEP command. A hardware or software reset or DEVICE RESET command is required to move a device out of Sleep mode.

4.5.3 Standby timer

The Standby timer provides a method for the device to automatically enter Standby mode from either Active or Idle mode following a host programmed period of inactivity. If the Standby timer is enabled and if the device is in the Active or Idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the Standby mode.

If the Standby timer is disabled, the device may automatically enter Standby mode.

4.5.4 Power modes

Figure 4 shows the set of mode transitions that shall be implemented.

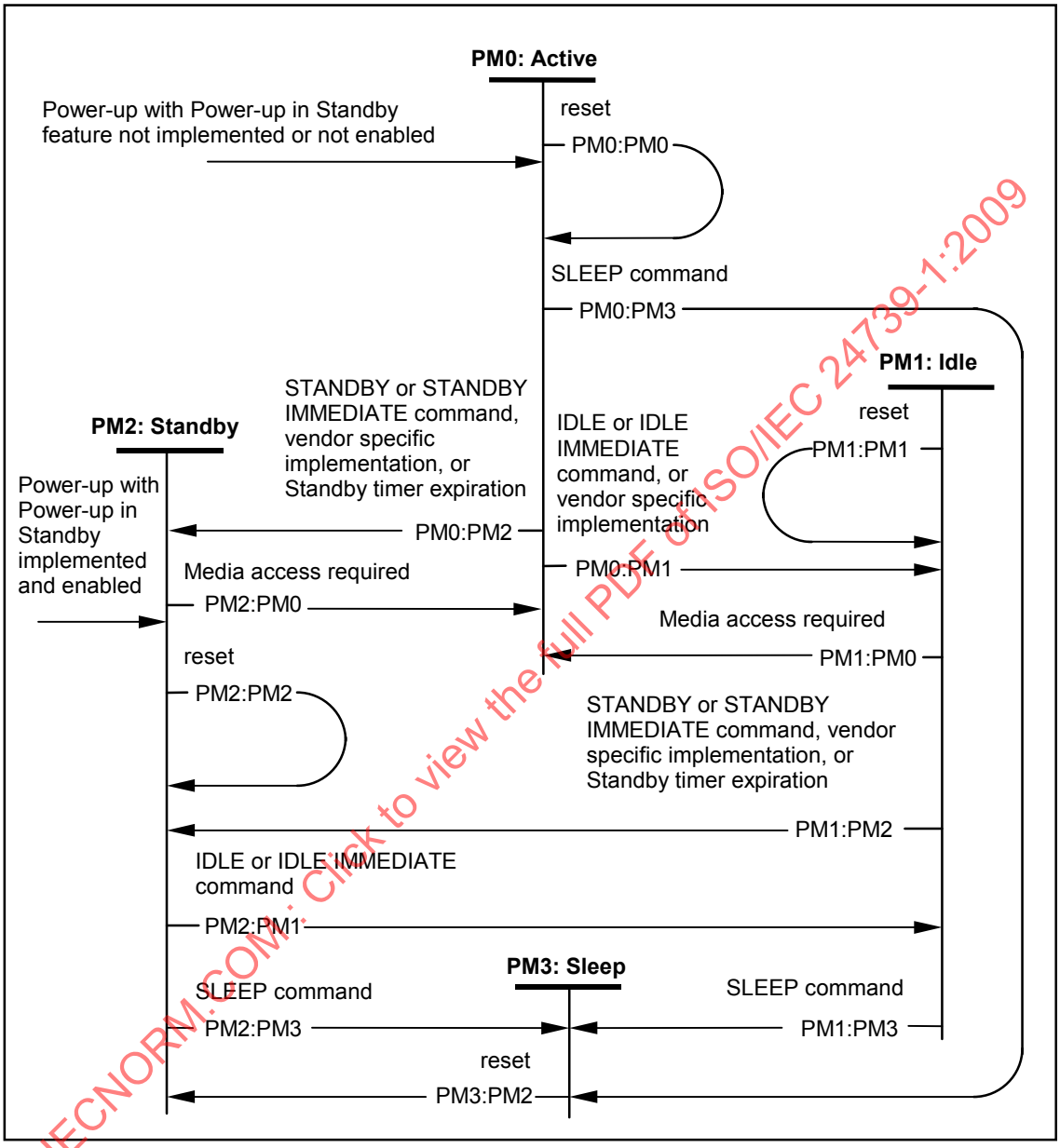


Figure 4 – Power management state diagram

PM0: Active: This mode shall be entered when the device receives a media access command while in Idle or Standby mode. This mode shall also be entered when the device is powered-up with the Power-Up In Standby feature not implemented or not enabled (see 4.12).

In Active mode the device is capable of responding to commands. During the execution of a media access command a device shall be in Active mode. Power consumption is greatest in this mode.

Transition PM0:PM0: When hardware reset, software reset or DEVICE RESET command is received, the device shall make a transition to the PM0: Active mode when the reset protocol is completed.

Transition PM0:PM1: When an IDLE or IDLE IMMEDIATE command is received or when a vendor specific implementation determines a transition is required, then the device shall make a transition to the PM1:Idle mode.

Transition PM0:PM2: When a STANDBY or STANDBY IMMEDIATE command is received, the Standby timer expires, or a vendor specific implementation determines a transition is required, then the device shall make a transition to the PM2:Standby mode.

Transition PM0:PM3: When a SLEEP command is received, the device shall make a transition to the PM3:Sleep mode.

PM1: Idle: This mode shall be entered when the device receives an IDLE or IDLE IMMEDIATE command. Some devices may perform vendor specific internal power management and make a transition to the Idle mode without host intervention.

In Idle mode the device is capable of responding to commands but the device may take longer to complete commands than when in the Active mode. Power consumption may be reduced from that of Active mode.

Transition PM1:PM0: When a media access is required, the device shall make a transition to the PM0:Active mode.

Transition PM1:PM1: When hardware reset, software reset, or DEVICE RESET command is received, the device shall make a transition to the PM1:Idle mode when the reset protocol is completed.

Transition PM1:PM2: When a STANDBY or STANDBY IMMEDIATE command is received, the Standby timer expires, or a vendor specific implementation determines a transition is required, then the device shall make a transition to the PM2:Standby mode.

Transition PM1:PM3: When a SLEEP command is received, the device shall make a transition to the PM3:Sleep mode.

PM2: Standby: This mode shall be entered when the device receives a STANDBY command, a STANDBY IMMEDIATE command or the Standby timer expires. Some devices may perform vendor specific internal power management and make a transition to the Standby mode without host intervention. This mode shall also be entered when the device is powered-up with the Power-Up In Standby feature implemented and enabled.

In Standby mode the device is capable of responding to commands but the device may take longer to complete commands than in the Idle mode. The time to respond could be as long as 30 s. Power consumption may be reduced from that of Idle mode.

Transition PM2:PM0: When a media access is required, the device shall make a transition to the PM0:Active mode.

Transition PM2:PM1: When an IDLE or IDLE IMMEDIATE command is received, or a vendor specific implementation determines a transition is required, then the device shall make a transition to the PM1:Idle mode.

Transition PM2:PM2: When hardware reset, software reset, or DEVICE RESET command is received, the device shall make a transition to the PM2:Standby mode when the reset protocol is completed.

Transition PM2:PM3: When a SLEEP command is received, the device shall make a transition to the PM3:Sleep mode.

PM3: Sleep: This mode shall be entered when the device receives a SLEEP command.

In Sleep mode the device requires a hardware or software reset or a DEVICE RESET command to be activated. The time to respond could be as long as 30 s. Sleep mode provides the lowest power consumption of any mode.

In Sleep mode, the device's interface is not active. The content of the Status register is invalid in this mode.

Transition PM3:PM2: When hardware reset, software reset or DEVICE RESET command is received the device shall make a transition to the PM2:Standby mode.

4.6 Advanced Power Management feature set

The Advanced Power Management feature set is an optional feature set that allows the host to select a power management level. The power management level is specified using a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. A device may implement one power management method for two or more contiguous power management levels. For example, a device may implement one power management method from level 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

The Advanced Power Management feature set uses the following functions:

– A SET FEATURES subcommand to enable Advanced Power Management
– A SET FEATURES subcommand to disable Advanced Power Management

Advanced Power Management is independent of the Standby timer setting. If both Advanced Power Management and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that the Standby state should be entered.

The device shall indicate:

a) feature set support in IDENTIFY DEVICE data and IDENTIFY PACKET DEVICE data word 83 bit 3;
b) feature set enabled in IDENTIFY DEVICE data and IDENTIFY PACKET DEVICE data word 86 bit 3; and
c) APM Level in IDENTIFY DEVICE data and IDENTIFY PACKET DEVICE data word 91.

4.7 Security Mode feature set

4.7.1 General

The optional Security Mode feature set is a password system that restricts access to user data stored on a device. The system has two passwords, User and Master, and two security levels, High and Maximum. The security system is enabled by sending a user password to the device with the SECURITY SET PASSWORD command. When the security system is enabled, access to user data on the device is denied after a power cycle until the User password is sent to the device with the SECURITY UNLOCK command.

A Master password may be set in addition to the User password. The purpose of the Master password is to allow an administrator to establish a password that is kept secret from the user, and which may be used to unlock the device if the User password is lost. Setting the Master password does not enable the password system.

The security level is set to High or Maximum with the SECURITY SET PASSWORD command. The security level determines device behavior when the Master password is used to unlock

the device. When the security level is set to High the device requires the SECURITY UNLOCK command and the Master password to unlock. When the security level is set to Maximum the device requires a SECURITY ERASE PREPARE command and a SECURITY ERASE UNIT command with the Master password to unlock. Execution of the SECURITY ERASE UNIT command erases all user data on the device.

The SECURITY FREEZE LOCK command prevents changes to passwords until a following power cycle. The purpose of the SECURITY FREEZE LOCK command is to prevent password setting attacks on the security system.

A device that implements the Security Mode feature set shall implement the following minimum set of commands:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

Support of the Security Mode feature set is indicated in IDENTIFY DEVICE data word 82 and data word 128.

4.7.2 Security mode initial setting

When the device is shipped by the manufacturer, the state of the Security Mode feature shall be disabled. The initial Master password value is not defined by this standard.

If the Master Password Revision Code feature is supported, the Master Password Revision Code shall be set to FFFEh by the manufacturer.

4.7.3 User password lost

If the User password sent to the device with the SECURITY UNLOCK command does not match the user password previously set with the SECURITY SET PASSWORD command, the device shall not allow the user to access data.

If the Security Level was set to High during the last SECURITY SET PASSWORD command, the device shall unlock if the Master password is received.

If the Security Level was set to Maximum during the last SECURITY SET PASSWORD command, the device shall not unlock if the Master password is received. The SECURITY ERASE UNIT command shall erase all user data and unlock the device if the Master password matches the last Master password previously set with the SECURITY SET PASSWORD command.

4.7.4 Attempt limit for SECURITY UNLOCK command

The device shall have an attempt limit counter. The purpose of this counter is to defeat repeated trial attacks. After each failed User or Master password SECURITY UNLOCK command, the counter is decremented. When the counter value reaches zero the EXPIRE bit (bit 4) of IDENTIFY DEVICE data word 128 is set to one, and the SECURITY UNLOCK and SECURITY UNIT ERASE commands are command aborted until the device is powered off or hardware reset. The EXPIRE bit shall be cleared to zero after power-on or hardware reset. The counter shall be set to five after a power-on or hardware reset.

4.7.5 Security mode states

Figure 5 decribes security mode states and state transitions.

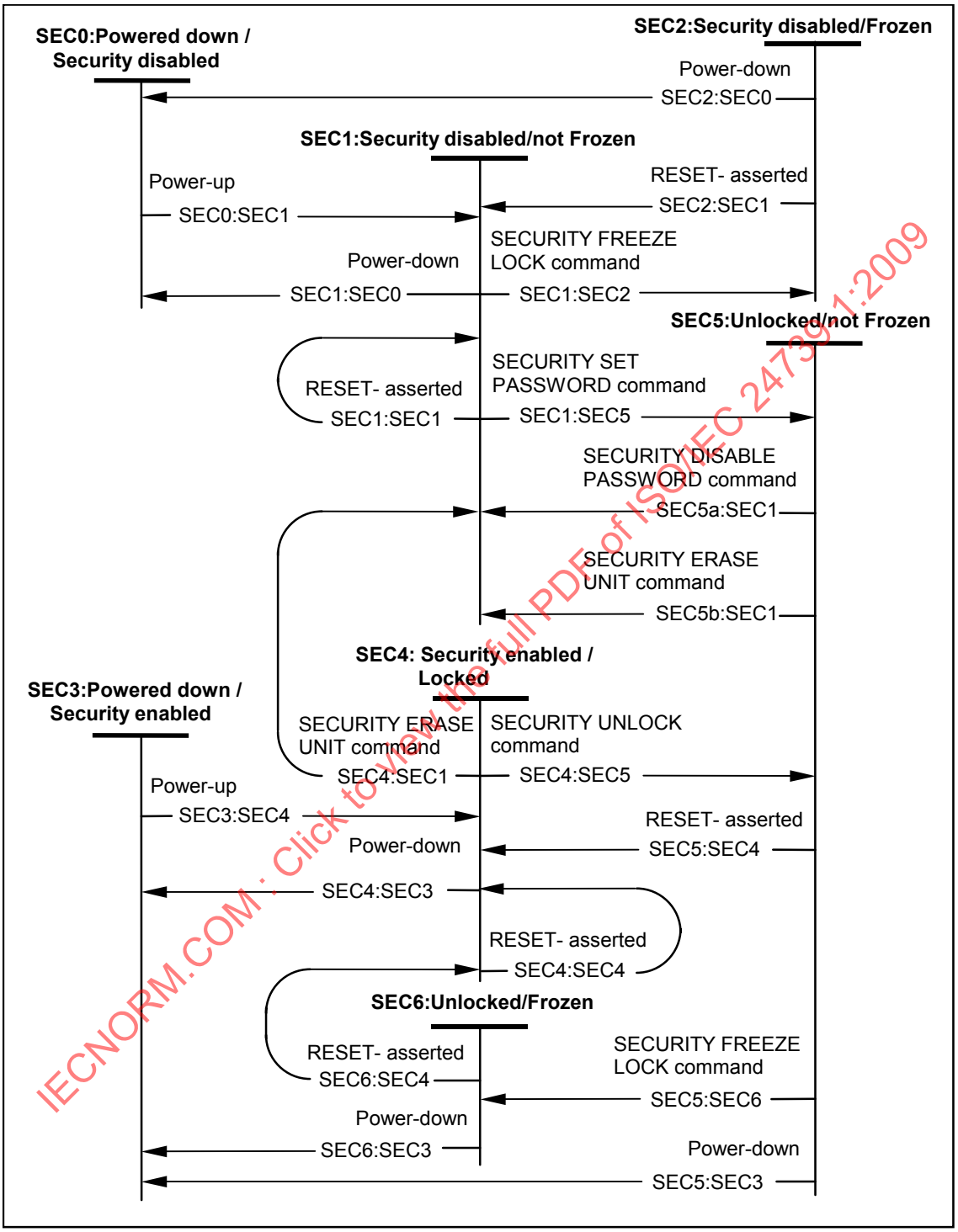


Figure 5 – Security mode state diagram

SEC0: Powered down/Security disabled: This mode shall be entered when the device is powered-down with the Security Mode feature set disabled.

Transition SEC0:SEC1: When the device is powered-up, the device shall make a transition to the SEC1: Security disabled/not Frozen state.

SEC1: Security disabled/not Frozen: This mode shall be entered when the device is powered-up or a hardware reset is received with the Security Mode feature set disabled or when the Security Mode feature set is disabled by a SECURITY DISABLE PASSWORD or SECURITY ERASE UNIT command.

In this state, the device is capable of responding to all commands (see Table 4 Unlocked column).

Transition SEC1:SEC0: When the device is powered-down, the device shall make a transition to the SEC0: Powered down/Security disabled state.

Transition SEC1:SEC1: When the device receives a hardware reset, the device shall make a transition to the SEC1: Security disabled/not Frozen state.

Transition SEC1:SEC2: When a SECURITY FREEZE LOCK command is received, the device shall make a transition to the SEC2: Security disabled/Frozen state.

Transition SEC1:SEC5: When a SECURITY SET PASSWORD command is received, the device shall make a transition to the SEC5: Unlocked/not frozen state.

SEC2: Security disabled/Frozen: This mode shall be entered when the device receives a SECURITY FREEZE LOCK command while in Security disabled/not Frozen state.

In this state, the device is capable of responding to all commands except those indicated in Table 4, Frozen column.

Transition SEC2:SEC0: When the device is powered-down, the device shall make a transition to the SEC0: Powered down/Security disabled state.

Transition SEC2:SEC1: When the device receives a hardware reset, the device shall make a transition to the SEC1: Security disabled/not Frozen state.

SEC3: Powered down/Security enabled: This mode shall be entered when the device is powered-down with the Security Mode feature set enabled.

Transition SEC3:SEC4: When the device is powered-up, the device shall make a transition to the SEC4: Security enabled/locked state.

SEC4: Security enabled/Locked: This mode shall be entered when the device is powered-up or a hardware reset is received with the Security Mode feature set enabled.

In this state, the device shall only respond to commands that do not access data in the user data area of the media (see Table 4 Locked column).

Transition SEC4:SEC3: When the device is powered-down, the device shall make a transition to the SEC3: Powered down/Security enabled state.

Transition SEC4:SEC4: When the device receives a hardware reset, the device shall make a transition to the SEC4: Security enabled/locked state.

Transition SEC4:SEC5: When a valid SECURITY UNLOCK command is received, the device shall make a transition to the SEC5: Unlocked/not Frozen state.

Transition SEC4:SEC1: When a SECURITY ERASE PREPARE command is received and is followed by a SECURITY ERASE UNIT command, the device shall make a transition to the SEC1: Security disabled/not Frozen state.

SEC5: Unlocked/not Frozen: This mode shall be entered when the device receives a SECURITY SET PASSWORD command to enable the lock or a SECURITY UNLOCK command.

In this state, the device shall respond to all commands (see Table 4, Unlocked column).

Transition SEC5a:SEC1: When a valid SECURITY DISABLE PASSWORD command is received, the device shall make a transition to the SEC1: Security disabled/not Frozen state.

Transition SEC5b:SEC1: When a SECURITY ERASE PREPARE command is received and is followed by a SECURITY ERASE UNIT command, the device shall make a transition to the SEC1: Security disabled/not Frozen state.

Transition SEC5:SEC6: When a SECURITY FREEZE LOCK command is received, the device shall make a transition to the SEC6: Unlocked/Frozen state.

Transition SEC5:SEC3: When the device is powered-down, the device shall make a transition to the SEC3: Powered down/Security enabled state.

Transition SEC5:SEC4: When the device receives a hardware reset, the device shall make a transition to the SEC4: Security enabled/Locked state.

SEC6: Unlocked/ Frozen: This mode shall be entered when the device receives a SECURITY FREEZE LOCK command while in Unlocked/Locked state.

In this state, the device is capable of responding to all commands except those indicated in Table 4, Frozen column.

Transition SEC6:SEC3: When the device is powered-down, the device shall make a transition to the SEC3: Powered down/Security enabled state.

Transition SEC6:SEC4: When the device receives a hardware reset, the device shall make a transition to the SEC4: Security enabled/Locked state.

Table 4 – Security mode command actions

Command	Locked	Unlocked	Frozen
CFA ERASE SECTORS	Command aborted	Executable	Executable
CFA REQUEST EXTENDED ERROR CODE	Executable	Executable	Executable
CFA TRANSLATE SECTOR	Executable	Executable	Executable
CFA WRITE MULTIPLE WITHOUT ERASE	Command aborted	Executable	Executable
CFA WRITE SECTORS WITHOUT ERASE	Command aborted	Executable	Executable
CHECK MEDIA CARD TYPE	Command aborted	Executable	Executable
CHECK POWER MODE	Executable	Executable	Executable
CONFIGURE STREAM	Command aborted	Executable	Executable
DEVICE CONFIGURATION	Command aborted	Executable	Executable
DEVICE RESET	Executable	Executable	Executable
DOWNLOAD MICROCODE	Vendor Specific	Vendor Specific	Vendor Specific
EXECUTE DEVICE DIAGNOSTIC	Executable	Executable	Executable
FLUSH CACHE	Command aborted	Executable	Executable
FLUSH CACHE EXT	Command aborted	Executable	Executable
GET MEDIA STATUS	Command aborted	Executable	Executable
IDENTIFY DEVICE	Executable	Executable	Executable
IDENTIFY PACKET DEVICE	Executable	Executable	Executable
IDLE	Executable	Executable	Executable
IDLE IMMEDIATE	Executable	Executable	Executable
MEDIA EJECT	Command aborted	Executable	Executable
MEDIA LOCK	Command aborted	Executable	Executable
MEDIA UNLOCK	Command aborted	Executable	Executable
NOP	Executable	Executable	Executable
PACKET	Command aborted	Executable	Executable
READ BUFFER	Executable	Executable	Executable
READ DMA	Command aborted	Executable	Executable
READ DMA EXT	Command aborted	Executable	Executable
READ DMA QUEUED	Command aborted	Executable	Executable
READ DMA QUEUED EXT	Command aborted	Executable	Executable
READ LOG EXT	Command aborted	Executable	Executable
READ MULTIPLE	Command aborted	Executable	Executable
READ MULTIPLE EXT	Command aborted	Executable	Executable
READ NATIVE MAX ADDRESS	Executable	Executable	Executable
READ NATIVE MAX ADDRESS EXT	Executable	Executable	Executable
READ SECTOR(S)	Command aborted	Executable	Executable
READ SECTOR(S) EXT	Command aborted	Executable	Executable
READ STREAM DMA EXT	Command aborted	Executable	Executable
READ STREAM EXT	Command aborted	Executable	Executable
READ VERIFY SECTOR(S)	Command aborted	Executable	Executable
READ VERIFY SECTOR(S) EXT	Command aborted	Executable	Executable
SECURITY DISABLE PASSWORD	Command aborted	Executable	Command aborted
SECURITY ERASE PREPARE	Executable	Executable	Command aborted

Command	Locked	Unlocked	Frozen
SECURITY ERASE UNIT	Executable	Executable	Command aborted
SECURITY FREEZE LOCK	Command aborted	Executable	Executable
SECURITY SET PASSWORD	Command aborted	Executable	Command aborted
SECURITY UNLOCK	Executable	Executable	Command aborted
SERVICE	Command aborted	Executable	Executable
SET FEATURES	Executable	Executable	Executable
SET MAX ADDRESS	Command aborted	Executable	Executable
SET MAX ADDRESS EXT	Command aborted	Executable	Executable
SET MAX SET PASSWORD	Command aborted	Executable	Executable
SET MAX LOCK	Command aborted	Executable	Executable
SET MAX FREEZE LOCK	Command aborted	Executable	Executable
SET MAX UNLOCK	Command aborted	Executable	Executable
SET MULTIPLE MODE	Executable	Executable	Executable
SLEEP	Executable	Executable	Executable
SMART DISABLE OPERATIONS	Executable	Executable	Executable
SMART ENABLE/DISABLE AUTOSAVE	Executable	Executable	Executable
SMART ENABLE OPERATIONS	Executable	Executable	Executable
SMART EXECUTE OFF-LINE IMMEDIATE	Executable	Executable	Executable
SMART READ DATA	Executable	Executable	Executable
SMART READ LOG	Executable	Executable	Executable
SMART RETURN STATUS	Executable	Executable	Executable
SMART WRITE LOG	Executable	Executable	Executable
STANDBY	Executable	Executable	Executable
STANDBY IMMEDIATE	Executable	Executable	Executable
WRITE BUFFER	Executable	Executable	Executable
WRITE DMA	Command aborted	Executable	Executable
WRITE DMA EXT	Command aborted	Executable	Executable
WRITE DMA FUA EXT	Command aborted	Executable	Executable
WRITE DMA QUEUED	Command aborted	Executable	Executable
WRITE DMA QUEUED EXT	Command aborted	Executable	Executable
WRITE DMA QUEUED FUA EXT	Command aborted	Executable	Executable
WRITE LOG EXT	Command aborted	Executable	Executable
WRITE MULTIPLE	Command aborted	Executable	Executable
WRITE MULTIPLE EXT	Command aborted	Executable	Executable
WRITE MULTIPLE FUA EXT	Command aborted	Executable	Executable
WRITE SECTOR(S)	Command aborted	Executable	Executable
WRITE SECTOR(S) EXT	Command aborted	Executable	Executable
WRITE STREAM DMA EXT	Command aborted	Executable	Executable
WRITE STREAM EXT	Command aborted	Executable	Executable

4.8 SMART (self-monitoring, analysis and reporting technology) feature set

4.8.1 General

The intent of self-monitoring, analysis and reporting technology (the SMART feature set) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in the IDENTIFY DEVICE data.

Devices that implement the PACKET Command feature set shall not implement the SMART feature set as described in this standard. Devices that implement the PACKET Command feature set and SMART shall implement SMART as defined by the command packet set implemented by the device. This feature set is optional if the PACKET Command feature set is not supported.

4.8.2 Device SMART data structure

SMART feature set capability and status information for the device are stored in the device SMART data structure. The off-line data collection capability and status data stored herein may be useful to the host if the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented (see 6.54.5).

4.8.3 On-line data collection

Collection of SMART data in an “on-line” mode shall have no impact on device performance. The SMART data that is collected or the methods by which data is collected in this mode may be different from those in the off-line data collection mode for any particular device and may vary from one device to another.

4.8.4 Off-line data collection

The device shall use off-line mode for data collection and self-test routines that have an impact on performance if the device is required to respond to commands from the host while performing that data collection. This impact on performance may vary from device to device. The data that is collected or the methods by which the data is collected in this mode may be different from those in the on-line data collection mode for any particular device and may vary from one device to another.

4.8.5 Threshold exceeded condition

This condition occurs when the device’s SMART reliability status indicates an impending degrading or fault condition.

4.8.6 SMART feature set commands

These commands use a single command code and are differentiated from one another by the value placed in the Features register (see 6.54).

If the SMART feature set is implemented, the following commands shall be implemented.

- SMART DISABLE OPERATIONS
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATIONS
- SMART RETURN STATUS

If the SMART feature set is implemented, the following commands may be implemented.

- SMART EXECUTE OFF-LINE IMMEDIATE
- SMART READ DATA
- SMART READ LOG
- SMART WRITE LOG
- READ LOG EXT
- WRITE LOG EXT

4.8.7 SMART operation with power management modes

When used with a host that has implemented the Power Management feature set, a SMART enabled device should automatically save the device accumulated SMART data upon receipt of an IDLE IMMEDIATE, STANDBY IMMEDIATE, or SLEEP command or upon return to an Active or Idle mode from a Standby mode (see 6.54.6).

If a SMART feature set enabled device has been set to use the Standby timer, the device should automatically save the device accumulated SMART data prior to going from an Idle mode to the Standby mode or upon return to an Active or Idle mode from a Standby mode.

A device shall not execute any routine to automatically save the device accumulated SMART data while the device is in a Standby or Sleep mode.

4.8.8 SMART device error log reporting

Logging of reported errors is an optional SMART feature. If error logging is supported by a device, it is indicated in byte 370 of the SMART READ DATA command response and bit 0 of word 84 of the IDENTIFY DEVICE response. If error logging is supported, the device shall provide information on the last five errors that the device reported as described in the SMART READ LOG command (see 6.54.7). The device may also provide additional vendor specific information on these reported errors.

If error logging is supported, it shall not be disabled when SMART is disabled. Error log information shall be gathered when the device is powered-on except that logging of errors when in a reduced power mode is optional. If errors are logged when in a reduced power mode, the reduced power mode shall not change. Disabling SMART shall disable the delivering of error log information via the SMART READ LOG command.

If a device receives a firmware modification, all error log data shall be discarded and the device error count for the life of the device shall be reset to zero.

4.9 Host Protected Area feature set

4.9.1 General

A reserved area for data storage outside the normal operating system file system is required for several specialized applications. Systems may wish to store configuration data or save memory to the device in a location that the operating systems cannot change. The optional Host Protected Area feature set allows a portion of the device to be reserved for such an area when the device is initially configured. A device that implements the Host Protected Area feature set shall implement the following minimum set of commands:

- READ NATIVE MAX ADDRESS
- SET MAX ADDRESS

A device that implements the Host Protected Area feature set and supports the 48-bit Address feature set shall implement the following additional set of commands:

- READ NATIVE MAX ADDRESS EXT
- SET MAX ADDRESS EXT

Devices supporting this feature set shall set bit 10 of word 82 to one in the data returned by the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command.

In addition, a device supporting the Host Protected Area feature set may optionally include the security extensions. The Host Protected Area security commands use a single command code and are differentiated from one another by the value placed in the Features register.

- SET MAX SET PASSWORD
- SET MAX LOCK
- SET MAX FREEZE LOCK
- SET MAX UNLOCK

Devices supporting these extensions shall set bit 10 of word 82 and bit 8 of word 83 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to one.

The READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command allows the host to determine the maximum native address space of the device even when a protected area has been allocated.

The SET MAX ADDRESS or SET MAX ADDRESS EXT command allows the host to redefine the maximum address of the user accessible address space. That is, when the SET MAX ADDRESS or SET MAX ADDRESS EXT command is issued with a maximum address less than the native maximum address, the device reduces the user accessible address space to the maximum specified by the command, providing a protected area above that maximum address. The SET MAX ADDRESS or SET MAX ADDRESS EXT command shall be immediately preceded by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command. After the SET MAX ADDRESS or SET MAX ADDRESS EXT command has been issued, the device shall report only the reduced user address space in response to an IDENTIFY DEVICE command in words 60, 61, 100, 101, 102 and 103. Any read or write command to an address above the maximum address specified by the SET MAX ADDRESS or SET MAX ADDRESS EXT command shall cause command completion with the IDNF bit set to one and ERR set to one, or command aborted. A volatility bit in the Sector Count register allows the host to specify if the maximum address set is preserved across power-on or hardware reset cycles. On power-on or hardware reset the device maximum address returns to the last non-volatile address setting regardless of subsequent volatile SET MAX ADDRESS or SET MAX ADDRESS EXT commands. If the SET MAX ADDRESS or SET MAX ADDRESS EXT command is issued with a value that exceeds the native maximum address command aborted shall be returned.

Typical use of these commands would be

- on reset
  a) BIOS receives control after a system reset;
  b) BIOS issues a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command to find the max capacity of the device;
  c) BIOS issues a SET MAX ADDRESS or SET MAX ADDRESS EXT command to the values returned by READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT;
  d) BIOS reads configuration data from the highest area on the disk;
  e) BIOS issues a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command followed by a SET MAX ADDRESS or SET MAX ADDRESS EXT command to reset the device to the size of the file system.
- on save to disk
  a) BIOS receives control prior to shut down;
  b) BIOS issues a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command to find the max capacity of the device;

c) BIOS issues a volatile SET MAX ADDRESS or SET MAX ADDRESS EXT command to the values returned by READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT;

d) Memory is copied to the reserved area;

e) Shut down completes;

f) On power-on or hardware reset the device max address returns to the last non-volatile setting.

These commands are intended for use only by system BIOS or other low-level boot time process. Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device. Devices should return command aborted if a subsequent non-volatile SET MAX ADDRESS or SET MAX ADDRESS EXT command is received after a power-on or hardware reset.

The SET MAX SET PASSWORD command allows the host to define the password to be used during the current power-on cycle. The password does not persist over a power cycle but does persist over a hardware or software reset. This password is not related to the password used for the Security Mode Feature set. When the password is set the device is in the Set_Max_Unlocked mode.

The SET MAX LOCK command allows the host to disable the SET MAX commands (except SET MAX UNLOCK) until the next power cycle or the issuance and acceptance of the SET MAX UNLOCK command. When this command is accepted the device is in the Set_Max_Locked mode.

The SET MAX UNLOCK command changes the device from the Set_Max_Locked mode to the Set_Max_Unlocked mode.

The SET MAX FREEZE LOCK command allows the host to disable the SET MAX commands (including SET MAX UNLOCK) until the next power cycle. When this command is accepted the device is in the Set_Max_Frozen mode.

4.9.2 BIOS determination of SET MAX security exension status

When the device is locked bit 8 of word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be set to one.

4.9.3 BIOS locking SET MAX

To allow for multiple BIOSs to gain access to the protected area the host BIOS should only lock the protected area immediately prior to booting the operating system.

Figure 6 is the SET MAX state diagram.

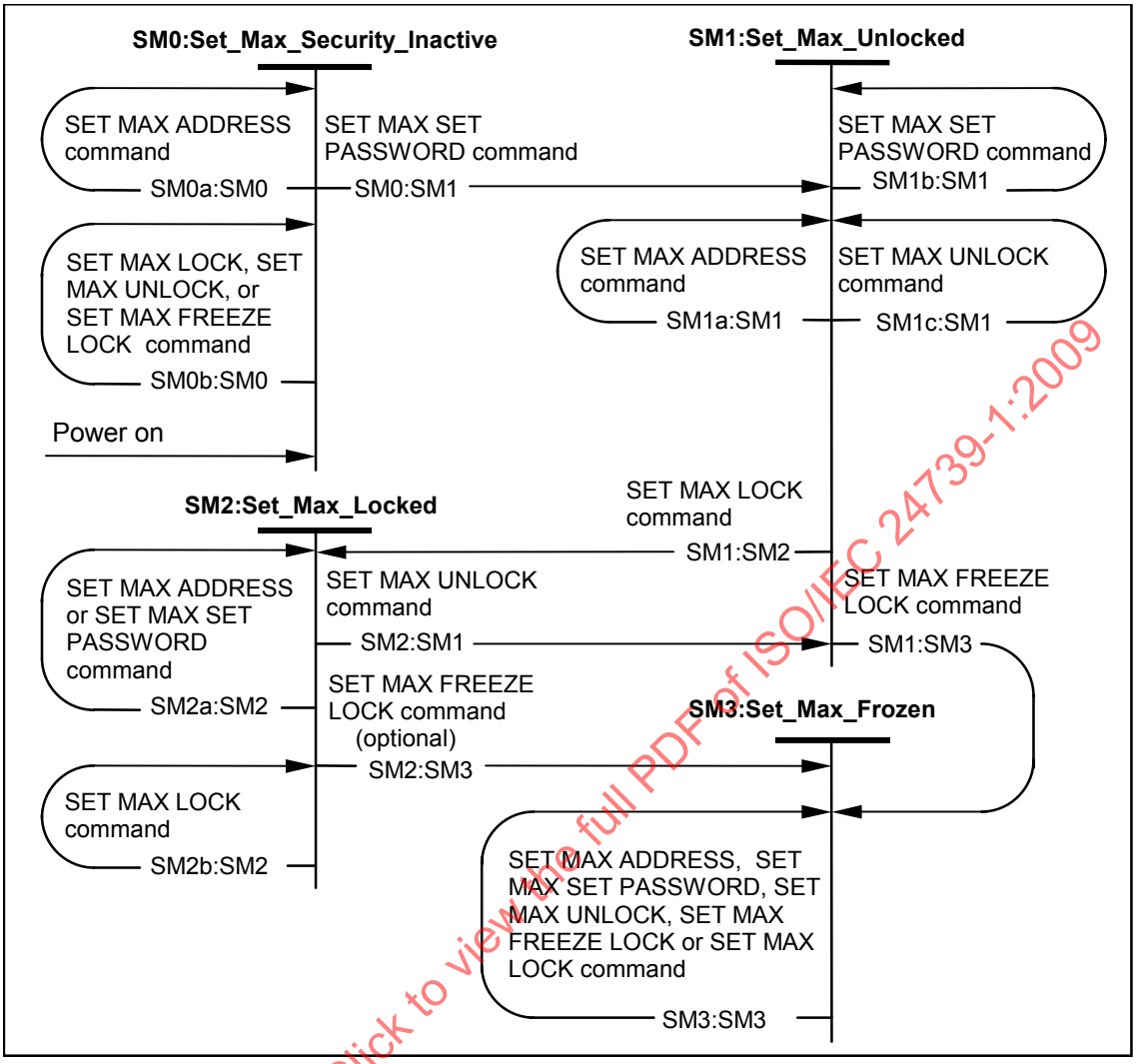


Figure 6 – SET MAX security state diagram

SM0: Set_Max_Security_Inactive: This state shall be entered when the device is powered-on.

When in this state, SET MAX security is disabled.

Transition SM0a:SM0: When a SET MAX ADDRESS command is received, the command shall be executed and the device shall make a transition to the SM0: Set_MAX_Security_Inactive state.

Transition SM0b:SM0: When a SET MAX LOCK, SET MAX UNLOCK, or SET MAX FREEZE LOCK command is received, the device shall abort the command and make a transition to the SM0: Set_MAX_Security_Inactive state.

Transition SM0:SM1: When a SET MAX SET PASSWORD command is received, the device shall make a transition to the SM1: Set_Max_Unlocked state.

SM1: Set_Max_Unlocked: This state is entered when a SET MAX SET PASSWORD or a SET MAX UNLOCK command is received.

When in this state, a SET MAX security password has been established and the SET MAX security is unlocked. Bit 8 of word 86 of the IDENTIFY DEVICE data shall be set to one.

Transition SM1a:SM1: When a SET MAX ADDRESS command is received, the command shall be executed and the device shall make a transition to the SM1: Set_MAX_Unlocked state.

Transition SM1b:SM1: When a SET MAX SET PASSWORD is received, the password stored by the device shall be changed to the new value and the device shall make a transition to the SM1: Set_MAX_Unlocked state.

Transition SM1c:SM1: When a SET MAX UNLOCK command is received, the command shall not be executed and the device shall make a transition to the SM1: Set_MAX_Unlocked state.

Transition SM1:SM2: When a SET MAX LOCK command is received, the device shall make a transition to the SM2: Set_Max_Locked state.

Transition SM1:SM3: When a SET MAX FREEZE LOCK command is received, the device shall make a transition to the SM3: Set_Max_Frozen state.

SM2: Set_Max_Locked: This state is entered when a SET MAX LOCK command is received.

When in this state, a SET MAX security password has been established and the SET MAX security is locked. Bit 8 of word 86 of the IDENTIFY DEVICE data shall be set to one.

Transition SM2a:SM2: When a SET MAX ADDRESS or SET MAX SET PASSWORD command is received, the command shall be aborted and the device shall make a transition to the SM2: Set_Max_Locked state.

Transition SM2b:SM2: When a SET MAX LOCK command is received, the command shall be executed and the device shall make a transition to the SM2: Set_Max_Locked state.

Transition SM2:SM1: When a SET MAX UNLOCK command is received, the device shall make a transition to the SM1: Set Max Unlocked state.

Transition SM2:SM3: When a SET MAX FREEZE LOCK command is received, the device may make a transition to the SM3: Set_Max_Frozen state. Hosts should not issue the SET MAX FREEZE LOCK command when in this state.

SM3: Set_Max_Frozen: This state is entered when a SET MAX FREEZE LOCK command is received.

In this state, the device may not transition to any other state except by a power cycling. When in this mode bit 8 of word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be set to one.

Transition SM3:SM3: When a SET MAX ADDRESS, SET MAX SET PASSWORD, SET MAX UNLOCK, SET MAX FREEZE LOCK or SET MAX LOCK command is received, the command shall be aborted and the device shall make a transition to the SM3: Set_Max_Frozen state.

4.10 CompactFlash™ Association (CFA) feature set

The optional CompactFlash™ Association (CFA) feature set provides support for solid state memory devices. A device that implements the CFA feature set shall implement the following minimum set of commands:

- CFA REQUEST EXTENDED ERROR CODE
- CFA WRITE SECTORS WITHOUT ERASE
- CFA ERASE SECTORS
- CFA WRITE MULTIPLE WITHOUT ERASE

– CFA TRANSLATE SECTOR
– SET FEATURES Enable/Disable 8-bit transfer

Devices reporting the value 848Ah in IDENTIFY DEVICE data word 0 or devices having bit 2 of IDENTIFY DEVICE data word 83 set to one shall support the CFA feature Set. If the CFA feature set is implemented, all five commands shall be implemented.

Support of DMA commands is optional for devices that support the CFA feature set.

The CFA ERASE SECTORS command preconditions the sector for a subsequent CFA WRITE SECTORS WITHOUT ERASE or CFA WRITE MULTIPLE WITHOUT ERASE command to achieve higher performance during the write operation. The CFA TRANSLATE SECTOR command provides information about a sector such as the number of write cycles performed on that sector and an indication of the sector's erased precondition. The CFA REQUEST EXTENDED ERROR CODE command provides more detailed error information.

Command codes B8h through BFh are reserved for assignment by the CompactFlash™ Association.

4.11 Removable Media Status Notification and Removable Media feature sets

4.11.1 General

This subclause describes two feature sets that secure the media in removable media storage devices using the ATA/ATAPI interface protocols. The Removable Media Status Notification feature set is intended for use in both devices implementing the PACKET Command feature set and those not implementing the PACKET Command feature set. The Removable Media feature set is intended for use only in devices not implementing the PACKET Command feature set. Only one of these feature sets shall be enabled at any time. If the Removable Media Status Notification feature set is in use then the Removable Media feature set is disabled and vice versa.

The reasons for implementing the Removable Media Status Notification feature set or the Removable Media feature set are

– to prevent data loss caused by writing to new media while still referencing the previous media's information,
– to prevent data loss by locking the media until completion of a cached write,
– to prevent removal of the media by unauthorized persons.

4.11.2 Removable Media Status Notification feature set

The Removable Media Status Notification feature set is the preferred feature set for securing the media in removable media storage devices. This feature set uses the SET FEATURES command to enable Removable Media Status Notification. Removable Media Status Notification gives the host system maximum control of the media. The host system determines media status by issuing the GET MEDIA STATUS command and controls the device eject mechanism via the MEDIA EJECT command (for devices not implementing the PACKET Command feature set). While Removable Media Status Notification is enabled devices not implementing the PACKET Command feature set execute MEDIA LOCK and MEDIA UNLOCK commands without changing the media lock state (no-operation). While Removable Media Status Notification is enabled the eject button does not eject the media.

Removable Media Status Notification is persistent through medium removal and insertion and is only disabled via the SET FEATURES command, hardware reset, software reset, the DEVICE RESET command, the EXECUTE DEVICE DIAGNOSTIC command, or power-on reset. Removable Media Status Notification shall be re-enabled after any of the previous reset conditions occur. All media status is reset when Removable Media Status Notification is disabled because a reset condition occurred. Any pending media change or media change request is cleared when the Removable Media Status Notification reset condition occurs.

The following commands are defined to implement the Removable Media Status Notification feature set.

- GET MEDIA STATUS
- MEDIA EJECT
- SET FEATURES (Enable media status notification)
- SET FEATURES (Disable media status notification)

NOTE Devices implementing the PACKET Command feature set control the media eject mechanism via the START/STOP UNIT command packet.

The preferred sequence of events to use the Removable Media Status Notification feature set is as follows:

a) Host system checks whether or not the device implements the PACKET Command feature set via the device signature in the Command Block registers.

b) Host system issues the IDENTIFY DEVICE command or the IDENTIFY PACKET DEVICE command and checks that the device is a removable media device and that the Removable Media Status Notification feature set is supported.

c) Host system uses the SET FEATURES command to enable Media Status Notification that gives control of the media to the host. At this time the host system checks the LBA High register to determine if
   - the device is capable of locking the media,
   - the device is capable of power ejecting the media,
   - Media Status Notification was enabled prior to this command.

d) Host system periodically checks media status using the GET MEDIA STATUS command to determine if any of the following events occurred
   - no media is present in the device (NM),
   - media was changed since the last command (MC),
   - a media change request has occurred (MCR).
   - media is write protected (WP).

4.11.3 Removable Media feature set

The Removable Media feature set is intended only for devices not implementing the PACKET Command feature set. This feature set operates with Media Status Notification disabled. The MEDIA LOCK and MEDIA UNLOCK commands are used to secure the media and the MEDIA EJECT command is used to remove the media. While the media is locked, the eject button does not eject the media. Media status is determined by checking the media status bits returned by the MEDIA LOCK and MEDIA UNLOCK commands.

Power-on reset, hardware reset, and the EXECUTE DEVICE DIAGNOSTIC command clear the Media Lock (LOCK) state and the Media Change Request (MCR) state. Software reset clears the Media Lock (LOCK) state, clears the Media Change Request (MCR) state, and preserves the Media Change (MC) state.

The following commands are defined to implement the Removable Media feature set.

- MEDIA EJECT
- MEDIA LOCK
- MEDIA UNLOCK

The preferred sequence of events to use the Removable Media feature set is as follows:

a) Host system checks whether or not the device implements the PACKET Command feature set via the device signature in the Command Block registers.

b) Host system issues the IDENTIFY DEVICE command and checks that the device is a removable media device and that the Removable Media feature set is supported.

c) Host system periodically issues MEDIA LOCK commands to determine if
   – no media is present in the device (NM) - media is locked if present,
   – a media change request has occurred (MCR).

4.12 Power-Up in Standby feature set

The optional Power-Up In Standby feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices. This optional feature set may be enabled or disabled via the SET FEATURES command or may be enabled by use of a jumper or similar means, or both. When enabled by a jumper, the feature set shall not be disabled via the SET FEATURES command. The IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data indicates whether this feature set is implemented and/or enabled.

The enabling of this feature set shall be persistent after power-down and power-up. When this feature set is enabled, the device shall power-up into Standby.

A device may implement a SET FEATURES subcommand that notifies the device to spin-up to the Active state when the device has powered-up into Standby. If the device implements this SET FEATURES subcommand and power-up into Standby is enabled, the device shall remain in Standby until the SET FEATURES subcommand is received. If the device implements this SET FEATURES subcommand, the fact that the feature is implemented is reported in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

If the device

– implements the enable/disable power-up in Standby subcommand,
– power-up into Standby is enabled, and
– an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is received while the device is in Standby as a result of powering up into Standby,

the device shall respond to the command and remain in Standby without spinning-up.

If the device has IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data that requires access to the media, the device shall set word 0 bit 2 to one to indicate that the response is incomplete. At a minimum, word 0 and word 2 shall be correctly reported. The fields that cannot be provided shall be filled with zeros. Once the full IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data has been accessed, a full response shall be returned until the next power-down/power-up sequence has taken place.

If the device does not implement the SET FEATURES subcommand to spin-up the device after power-up and power-up into Standby is enabled, the device shall spin-up upon receipt of the first command that requires the device to access the media.

4.13 Automatic Acoustic Management (AAM) feature set

The Automatic Acoustic Management feature set is an optional feature set that allows the host to select an acoustic management level. The acoustic management level ranges from the setting of 00h to FFh, although many levels are currently reserved (see Table 43). Device performance and acoustic emanation may increase with increasing acoustic management levels. The acoustic management levels may contain discrete bands. For example, a device may implement one acoustic management method from level 80h to A0h, and a higher performance, higher acoustic emanation method from level A1h to FEh.

The Automatic Acoustic Management feature set uses the following functions:

– a SET FEATURES subcommand to enable the Automatic Acoustic Management feature set;
– A SET FEATURES subcommand to disable the Automatic Acoustic Management feature set.

The IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data indicates if the Automatic Acoustic Management feature set is supported, if the Automatic Acoustic Management feature set is enabled, and the current automatic acoustic management level if the Automatic Acoustic Management feature set is enabled.

4.14 48-bit Address feature set

The optional 48-bit Address feature set allows devices with capacities up to 281 474 976 710 655 sectors. This allows device capacity up to 144 115 188 075 855 360 bytes. In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector count to 16 bits.

The commands in the 48-bit Address feature set are prohibited from use for devices implementing the PACKET Command feature set.

Commands unique to the 48-bit Address feature set are

- FLUSH CACHE EXT
- READ DMA EXT
- READ DMA QUEUED EXT
- READ MULTIPLE EXT
- READ NATIVE MAX ADDRESS EXT
- READ SECTOR(S) EXT
- READ VERIFY SECTOR(S) EXT
- SET MAX ADDRESS EXT
- WRITE DMA EXT
- WRITE DMA FUA EXT
- WRITE DMA QUEUED EXT
- WRITE DMA QUEUED FUA EXT
- WRITE MULTIPLE EXT
- WRITE MULTIPLE FUA EXT
- WRITE SECTOR(S) EXT

The 48-bit Address feature set operates in LBA only. Devices implementing the 48-bit Address feature set shall also implement commands that use 28-bit addressing. 28-bit and 48-bit commands may be intermixed. Support of the 48-bit Address feature set is indicated in the IDENTIFY DEVICE response.

In a device implementing the 48-bit Address feature set, the Features register, the Sector Count register, the LBA Low register, the LBA Mid register, and the LBA High register are each a two byte deep FIFO. Each time one of these registers is written, the new content written is placed into the most recently written location and the previous content of the register is moved to previous content location. For example, when a 48-bit Address feature set READ SECTOR(S) EXT command is written to the device Command register, the address used by the command is as described in Table 5.

Table 5 – 48-bit addresses

Register	Most recently written	Previous content
Features	Reserved	Reserved
Sector count	Sector count (7:0)	Sector count (15:8)
LBA Low	LBA (7:0)	LBA (31:24)
LBA Mid	LBA (15:8)	LBA (39:32)
LBA High	LBA (23:16)	LBA (47:40)
Device register	Bits 7 and 5 are obsolete, the LBA bit shall be set to one, the DEV bit shall indicate the selected device, bits (3:0) are reserved	Reserved

When a READ SECTOR(S) command utilizing 28-bit addressing is written to the device Command register, the address used by the command is as described in Table 6. Thus commands utilizing 28-bit addressing still function as described in the command descriptions.

Table 6 – 28-bit addresses

Register	Most recently written	Previous content
Features	na	na
Sector Count	Sector count (7:0)	na
LBA Low	LBA (7:0)	na
LBA Mid	LBA (15:8)	na
LBA High	LBA (23:16)	na
Device register	LBA (27:24)	na

The host may read the previous content of the Features, Sector Count, LBA Low, LBA Mid, and LBA High registers by first setting the High Order Bit (HOB, bit 7) of the Device Control register to one and then reading the desired register. If HOB (bit 7) in the Device Control register is cleared to zero the host reads the most recently written content when the register is read. A write to any Command Block register shall cause the device to clear the HOB bit to zero in the Device Control register. The most recently written content always gets written by a register write regardless of the state of HOB (bit 7) in the Device Control register.

Registers are written and read as described in Clause 5.

The device shall indicate support of the 48-bit Address feature set in the IDENTIFY DEVICE response. In addition, IDENTIFY DEVICE data words 100 to 103 contain the maximum user LBA + 1 that is accessible by 48-bit addressable commands.

If the value contained in IDENTIFY DEVICE data words 100 to 103 is equal to or less than 268 435 455, then the content of words 60 to 61 shall be as described in 4.2.2. If the value in contained IDENTIFY DEVICE data words 100 to 103 is greater than 268 435 455, then the maximum value in words 60 to 61 shall be 268,435,455. That is, if the device contains greater than the capacity addressable with 28-bit commands, words 60 to 61 shall describe the maximum capacity that can be addressed by 28-bit commands.

When the 48-bit Address feature set is implemented, the native maximum address is the highest address accepted by the device in the factory default condition using a 48-bit Address feature set command. The native maximum address is the value returned by a READ NATIVE MAX ADDRESS EXT command. If the native maximum address of a device is equal to or less than 268 435 455 a READ NATIVE MAX ADDRESS shall return the native maximum address. If the native maximum address is greater than 268 435 455, a READ NATIVE MAX ADDRESS command shall cause the device to return a maximum value of 268 435 454.

When the 48-bit Address feature set is implemented, the SET MAX ADDRESS command shall execute as described in 6.50.2. However, in addition to modifying the content of words 60 to 61, the new content of words 60 to 61 shall also be placed in words 100 to 103. When a SET MAX ADDRESS EXT command is issued and the address requested is greater than 268 435 455 words 100 to 103 shall be modified to reflect the requested value but words 60 and 61 shall not be modified. When a SET MAX ADDRESS EXT command is issued and the address requested is equal to or less than 268 435 455 words 100 to 103 shall be modified to reflect the requested value and words 60 and 61 shall be modified as described in 6.50.2.8.

If a Host Protected Area has been created using the SET MAX ADDRESS command, all SET MAX ADDRESS EXT commands shall result in command aborted until the Host Protected Area is eliminated by use of the SET MAX ADDRESS command with the address value returned by the READ NATIVE MAX ADDRESS command. If a Host Protected Area has been created using the SET MAX ADDRESS EXT command, all SET MAX ADDRESS commands shall result in command aborted until the Host Protected Area is eliminated by use of the SET MAX ADDRESS EXT command with the address value returned by the READ NATIVE MAX ADDRESS EXT command.

The WRITE DMA FUA EXT, WRITE DMA QUEUED FUA EXT, and WRITE MULTIPLE FUA EXT commands are unique in that regardless whether or not caching is enabled in the device, the user data shall be written to the media before ending status for the command is reported.

4.15 Device Configuration Overlay feature set

The optional Device Configuration Overlay feature set allows a utility program to modify some of the optional commands, modes, and feature sets that a device reports as supported in the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data as well as the capacity reported.

Commands unique to the Device Configuration Overlay feature set use a single command code and are differentiated from one another by the value placed in the Features register. These commands are:

- DEVICE CONFIGURATION FREEZE LOCK
- DEVICE CONFIGURATION IDENTIFY
- DEVICE CONFIGURATION RESTORE
- DEVICE CONFIGURATION SET.

The Device Configuration Overlay feature set may affect words 60 to 61, 63, 82 to 88 and 100 to 103 of the IDENTIFY DEVICE and IDENTIFY PACKET DEVICE command responses. Certain bits in these words that indicate that a command, mode, capacity or feature set is supported and enabled may be cleared by a DEVICE CONFIGURATION SET command. For a particular command, mode, capacity or feature set, when a bit is cleared indicating that the device does not support the feature, the device shall not provide the feature. Also, the maximum capacity of the device may be reduced. Since a Host Protected Area may be lost if the capacity of the device is reduced, when a Host Protected Area is set the DEVICE CONFIGURATION SET command shall cause the device to return command aborted. The address value returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command is modified by the DEVICE CONFIGURATION SET command modifying the maximum capacity of the device. If a DEVICE CONFIGURATION FREEZE LOCK command has been issued since the device powered-up, the DEVICE CONFIGURATION SET command shall cause the device to return command aborted. The settings made by a DEVICE CONFIGURATION SET command are maintained over power-down and power-up.

A DEVICE CONFIGURATION IDENTIFY command specifies the selectable commands, modes, capacity and feature sets that the device is capable of supporting. After the execution of a DEVICE CONFIGURATION SET command this information is no longer available from an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command.

A DEVICE CONFIGURATION RESTORE command disables an overlay that has been set by a DEVICE CONFIGURATION SET command and returns the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data to that indicated by the DEVICE CONFIGURATION IDENTIFY command. Since a Host Protected Area may be lost if the capacity of the device is reduced, when a Host Protected Area is set the DEVICE CONFIGURATION RESTORE command shall cause the device to return command aborted. If a DEVICE CONFIGURATION FREEZE LOCK command has been issued since the device powered-up, the DEVICE CONFIGURATION RESTORE command shall cause the device to return command aborted.

A DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the state of the Device Configuration Overlay feature set. A device always powers-up with configuration freeze lock not set. After a successful DEVICE CONFIGURATION FREEZE LOCK command is executed, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION IDENTIFY and DEVICE CONFIGURATION RESTORE commands are aborted by the device until the device is powered-down and powered-up again. The freeze locked state is not affected by hardware or software reset.

Figure 7 and the text following the figure describe the operation of the Device Configuration Overlay feature set.

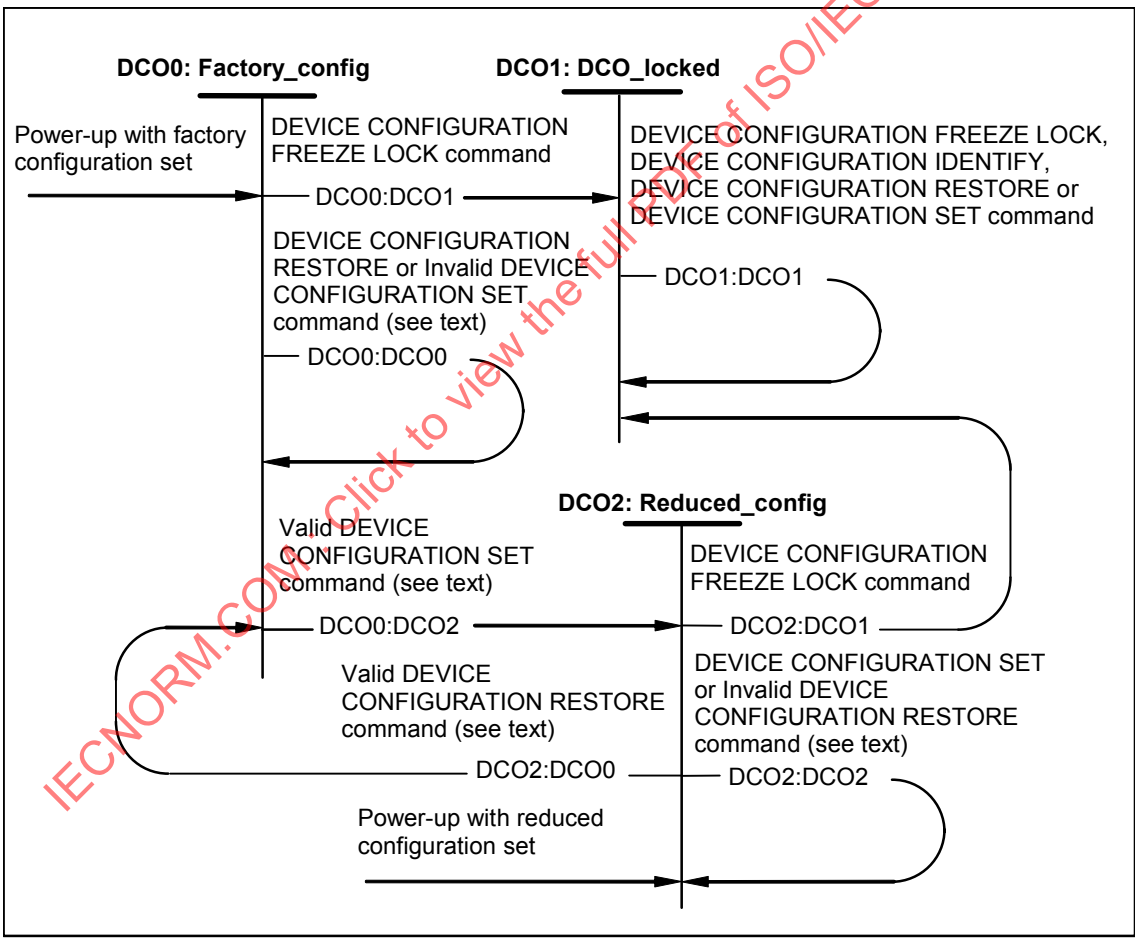


Figure 7 – Device configuration overlay state diagram

DCO0: Factory_config State: This state is entered when the device powers-up with the factory configuration set or a valid DEVICE CONFIGURATION RESTORE command is received.

When in this state, the device shall support all commands, modes, features sets, and the capacity indicated by the response to a DEVICE CONFIGURATION IDENTIFY command.

Transition DCO0:DCO1: When a DEVICE CONFIGURATION FREEZE LOCK command is received, the device shall return successful command completion and make a transition to the DCO1: DCO_locked state.

Transition DCO0:DCO2: When a valid DEVICE CONFIGURATION SET command is received, the device shall return successful command completion and make a transition to the DCO2: Reduced_config state. See transition DCO0:DCO0 for the definition of conditions that make a DEVICE CONFIGURATION SET command invalid. This transition is made even if the configuration described by the DEVICE SET CONFIGURATION SET command is the same as the factory configuration.

Transition DCO0:DCO0: When a DEVICE CONFIGURATION RESTORE command is received, the device shall return command aborted and make a transition to the DCO0: Factory_config state. When an invalid DEVICE CONFIGURATION SET command is received, the device shall return command aborted and make a transition to the DCO0: Factory_config state. A DEVICE CONFIGURATION SET command is invalid if the DEVICE CONFIGURATION SET command requests:

- a Host Protected Area has been established using the SET MAX ADDRESS command,
- the elimination of support of a Multiword or Ultra DMA mode if that mode is currently selected or a higher numbered mode is currently selected,
- the elimination of support of the Host Protected Area feature set if a Host Protected Area has been established using a SET MAX ADDRESS command,
- the elimination of support of the Power-up in Standby feature set if the feature set has been enabled by a jumper,
- the elimination of support of the Security feature set if the feature set has been enabled,
- the elimination of support of the SMART feature set if bits (2:1) of word 7 are not cleared to zero or if the SMART feature set has been enabled by use of the SMART ENABLE OPERATIONS command.

DCO1: DCO_locked State: This state is entered when a DEVICE CONFIGURATION RESTORE command is received.

When in this state, all DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, DEVICE CONFIGURATION SET or DEVICE CONFIGURATION RESTORE commands shall return command abort and shall remain in the locked state.

Transition DCO1:DCO1: When a DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, DEVICE CONFIGURATION SET or DEVICE CONFIGURATION RESTORE command is received, the device shall return command aborted and make a transition to the DCO1: DCO_locked state.

DCO2: Reduced_config State: This state is entered when the device powers-up with a reduced configuration set or a valid DEVICE CONFIGURATION SET command is received.

When in this state, the device shall support all commands, modes, features sets and the capacity specified by the DEVICE CONFIGURATION SET command that caused this state to be entered.

Transition DCO2:DCO1: When a DEVICE CONFIGURATION FREEZE LOCK command is received, the device shall return successful command completion and make a transition to the DCO1: DCO_locked state.

Transition DCO2:DCO0: When a valid DEVICE CONFIGURATION RESTORE command is received, the device shall return successful command completion and make a transition to the

DCO0: Factory_config state. See transition DCO2:DCO2 for the definition of conditions that make a DEVICE CONFIGURATION RESTORE command invalid.

Transition DCO2:DCO2: When a DEVICE CONFIGURATION SET command is received, the device shall return command aborted and make a transition to the DCO2: Reduced_config state. When an invalid DEVICE CONFIGURATION RESTORE command is received, the device shall return command aborted and make a transition to the DCO2: Reduced_config state. A DEVICE CONFIGURATION RESTORE command is invalid if a Host Protected Area has been established using the SET MAX ADDRESS command.

4.16 Media Card Pass Through Command feature set

The Media Card Pass Through commands are implemented by a Media Pass Through device. A device implementing the Media Card Pass Through Command feature set is a bridge to one or more types of media card storage devices. The bridge device responds to the same command set as described in 4.3.2 and to the commands included in this feature set.

Use of the Media Card Pass Through Command feature set is prohibited for PACKET devices.

The Media Card Pass Through Command feature set uses the command codes D1h, D2h, D3h, and D4h and bits in word 84 and word 87 of the IDENTIFY DEVICE response. The command codes D2h through D4h are reserved for the Media Card Pass Through Command feature set if this feature set is enabled by the CHECK MEDIA CARD TYPE command (D1h). This feature set embeds small-format flash memory card commands inside the ATA commands. The adapter's firmware passes the embedded memory card's command to the memory card as is from the ATA command. The Media Card Pass Through Command feature set reduces the number of commands required for this feature set regardless of the number or type of memory card commands. It also reduces the adapter's firmware overhead in processing them. As new memory cards types are defined in the market, they can all be supported within this one feature.

The commands unique to the Media Card Pass Through Command feature set are:

– CHECK MEDIA CARD TYPE
– Command codes D2h through D4h

The CHECK MEDIA CARD TYPE command returns the supporting status of the device to this feature set. It also enables and disables the device from running the Media Card Pass Through Command feature set. When the Media Card Pass Through Command feature set is disabled, the command codes D2h through D4h shall not be interpreted as Media Card Pass Through Command feature set commands and the device shall return command aborted. Power-on, hardware or software reset shall disable the Media Card Pass Through Command feature set.

The definitions of the commands D2h-D4h are media card type dependent. Table 7 lists the Media card types and their associated reference document:

Table 7 – Media Card type references

Media card type	Reference document
SD card	SD Card ATA Command Extension (SDA 3C)
Smart media	Smart Media ATA Command Extension (SSFDC Forum)

4.17 Streaming feature set

4.17.1 General

The Streaming feature set is an optional feature set that allows a host to request delivery of data from a contiguous logical block address range within an allotted time. This places a priority on time to access the data rather than the integrity of the data. Streaming feature set commands only support 48-bit addressing.

A device that implements the Streaming feature set shall implement the following minimum set of commands:

- CONFIGURE STREAM
- READ STREAM EXT
- WRITE STREAM EXT
- READ STREAM DMA EXT
- WRITE STREAM DMA EXT
- READ LOG EXT
- WRITE LOG EXT

Support of the Streaming feature set is indicated in IDENTIFY DEVICE data word 84 bit 4.

NOTE PIO versions of these commands limit the transfer rate (16.6 MB/s), provide no CRC protection and limit status reporting as compared to a DMA implementation.

4.17.2 Streaming commands

4.17.2.1 General

The streaming commands are defined to be time critical data transfers rather than the standard data integrity critical commands. Each command shall be completed within the time specified in the CONFIGURE STREAM command or in the streaming command itself in order to ensure the stream requirements of the AV type application. The device may execute background tasks as long as the READ STREAM and WRITE STREAM command execution time limits are still met.

Using the CONFIGURE STREAM command, the host may define the various stream properties including the default Command Completion Time Limit (CCTL) to assist the device in setting up its caching for best performance. If the host does not use a CONFIGURE STREAM command, the device shall use the CCTL specified in each streaming command, and the time limit is effective for one time only. If the CCTL is not set by a CONFIGURE STREAM command, the operation of a streaming command with a zero CCTL is device vendor specific. If Stream ID is not set by a CONFIGURE STREAM command, the device shall operate according to the Stream ID set by the streaming command. The operation is device vendor specific.

The streaming commands may access any user LBA on a device. These commands may be interspersed with non-streaming commands, but there may be an impact on performance due to the unknown time required to complete the non-streaming commands.

The streaming commands should be issued using a specified minimum number of sectors transferred per command, as specified in word 95 of the IDENTIFY DEVICE response. The transfer length of a request should be a multiple of the minimum number of sectors per transfer.

The host provided numeric stream identifier, Stream ID, may be used by the device to configure its resources to support the streaming requirements of the AV content. One Stream ID may be configured for each read and write operation with different command completion time limits by each CONFIGURE STREAM command.

4.17.2.2 Urgent bit

The Urgent bit in the READ STREAM and WRITE STREAM commands specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit.

4.17.2.3 Flush to Disk bit

The Flush to Disk bit in the WRITE STREAM command specifies that all data for the specified stream shall be flushed to the media before posting command completion. If a host requests flushes at times other than the end of each Allocation Unit, streaming performance may be degraded. The SET FEATURES command to enable/disable caching shall not affect caching for streaming commands.

4.17.2.4 Not Sequential bit

The Not Sequential bit specifies that the next read stream command with the same Stream ID may not be sequential in LBA space. This information helps the device with pre-fetching decisions.

4.17.2.5 Read Continuous bit

If the Read Continuous bit is set to one for the command, the device shall transfer the requested amount of data to the host within the Command Completion Time Limit even if an error occurs. The data sent to the host by the device in an error condition is vendor specific.

4.17.2.6 Write Continuous bit

If the Write Continuous bit is set to one for the command and an error is encountered, the device shall complete the request without posting an error. If an error cannot be resolved within the Command Completion Time Limit, the erroneous section on the media may be unchanged or may contain undefined data. A future read of this area may not report an error, even though the data is erroneous.

4.17.2.7 Handle Streaming Error bit

The Handle Streaming Error bit specifies to the device that this command starts at the LBA of a recently reported error section, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier. This mechanism allows the host to schedule error recovery and defect management for content critical data.

4.17.3 Streaming logs

The Streaming Data Transfer feature set requires two error logs and one performance log. These logs are accessed via the READ LOG EXT command. The information included in the error logs is volatile and is not maintained across power cycles, hard resets, or sleep. These error logs are 512 bytes in length and retain the last 31 errors that occurred during any Streaming Data transfer.

The Streaming Performance log provides specific drive performance characteristics to the host that allows for calculating of streaming performance values. The contents of the Streaming Performance Parameters Log may be affected by the host issuing a SET FEATURES subcommand 42h, C2h, or 43h (Automatic Acoustic Management and Typical Host Interface Sector Time). The host should base its calculations on the larger of its Typical Host Interface Sector Time and the device reported Sector Time values, and on the sum of the device reported Access Time values and any additional latency that only the host is aware of (host command overhead, etc).

4.18 General Purpose Logging feature set

The General Purpose Logging feature set provides a mechanism for accessing logs in a device. These logs are associated with specific feature sets such as SMART. Support of the individual logs is determined by support of the associated feature set. If the device supports a particular feature set, support for any associated log(s) is mandatory.

Support for the General Purpose Logging feature set shall not be disabled. If the feature set associated with a requested log is disabled, the device shall return command abort.

If the General Purpose Logging feature set is implemented, the following commands shall be supported:

- READ LOG EXT
- WRITE LOG EXT.

4.19 Overlapped feature set

Serial implementations of ATA have different requirements (see Clause 5).

The optional Overlap feature set allows devices that require extended command time to perform a bus release so that the other device on the bus may be used. To perform a bus release the device shall clear both DRQ and BSY to zero. When selecting the other device during overlapped operations, the host shall disable assertion of INTRQ via the nIEN bit on the currently selected device before writing the Device register to select the other device and then may re-enable interrupts.

The only commands that may be overlapped are:

- NOP (with a subcommand code other than 00h)
- PACKET
- READ DMA QUEUED
- READ DMA QUEUED EXT
- SERVICE
- WRITE DMA QUEUED
- WRITE DMA QUEUED EXT
- WRITE DMA QUEUED FUA EXT.

For the PACKET command, overlap is specified by the OVL bit in the Features register when the PACKET command is issued.

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been enabled via the SET FEATURES command, then the device shall perform a bus release when the command packet has been received. This allows the host to select the other device to execute commands. When the device is ready to continue the command, the device sets SERV to one, and asserts INTRQ if selected and nIEN is cleared to zero. The host then issues the SERVICE command to continue the execution of the command.

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, then the device may or may not perform a bus release. If the device is ready to complete execution of the command, the device may complete the command immediately as described in the non-overlap case. If the device is not ready to complete execution of the command, the device may perform a bus release and complete the command as described in the previous paragraph.

For the READ DMA QUEUED and WRITE DMA QUEUED commands, the device may or may not perform a bus release. If the device is ready to complete execution of the command, the

device may complete the command immediately. If the device is not ready to complete execution of the command, the device may perform a bus release and complete the command via a service request.

If a device has an outstanding command that has been released, the device can only indicate that service is required when the device is selected. This implies that the host has to poll each device to determine if a device is requesting service. The polling can be performed at the host either by hardware or by a software routine. The latter implies a considerable host processor overhead. Hardware polling is initiated by the NOP Auto Poll command.

The NOP Poll command is a host adapter function and is ignored by the device. The host software can test for the support of this feature by issuing the NOP Auto Poll subcommand and examining the Status register. If the host adapter does not support this feature, the response received by the host will be from the device with the ERR bit set to one. If the host adapter does support the command, the response will be from the host adapter with the ERR bit cleared to zero. The only action taken by a device supporting the Overlapped feature set will be to return the error indication in the Status register and to not abort any outstanding commands.

When this command is received, the user data shall be written to the device media before the command ending status is reported regardless of the state of any write cache or queue. A queue shall not be aborted.

4.20 Queued feature set

The Queued feature set allows the host to issue concurrent commands to the same device. The Queued feature set is optional if the Overlap feature set is supported. Only commands included in the Overlapped feature set may be queued. The queue contains all commands for which command acceptance has occurred but command completion has not occurred. If a queue exists when a non-queued command is received, the non-queued command shall be command aborted and the commands in the queue shall be discarded. The ending status shall be command aborted and the results are indeterminate.

The maximum queue depth supported by a device shall be indicated in word 75 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

A queued command shall have a Tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this Tag shall be restored so that the host may identify the command for which status is being presented. A Tag value may be any value between 0 and 31, regardless of the queue depth supported. If a queued command is issued with a Tag value that is identical to the Tag value for a command already in the queue, the entire queue shall be aborted including the new command. The ending status shall be command aborted and the results are indeterminate. If any error occurs, the command queue shall be aborted.

When the device is ready to continue the processing of a bus released command and BSY and DRQ are both cleared to zero, the device requests service by setting SERV to one, setting a pending interrupt and setting Interrupt Pending if selected and if nIEN is cleared to zero. SERV shall remain set until all commands ready for service have been serviced. A read of the Status register or a write of the Command register shall clear the Interrupt Pending.

When the device is ready to continue the processing of a bus released command and BSY or DRQ is set to one (i.e., the device is processing another command on the bus), the device requests service by setting SERV to one. SERV shall remain set until all commands ready for service have been serviced. At command completion of the current command processing (i.e., when both BSY and DRQ are cleared to zero), the device shall process Interrupt Pending and INTRQ per the protocol for the command being completed. No additional INTRQ assertion shall occur due to other commands ready for service until after the device's SERV bit has been cleared to zero.

When the device receives a new command while queued commands are ready for service, the device shall execute the new command and process Interrupt Pending and INTRQ per the protocol for the new command. If the queued commands ready for service still exist at command completion of this command, SERV remains set to one but no additional INTRQ assertion shall occur due to commands ready for service.

When queuing commands, the host shall disable INTRQ assertion via the nIEN bit before writing a new command to the Command register and may re-enable INTRQ assertion after writing the command. When reading status at command completion of a command, the host shall check the SERV bit since the SERV bit may be set because the device is ready for service associated with another command. The host receives no additional INTRQ assertion to indicate that a queued command is ready for service.

4.21 Long physical sector feature set for non-packet devices

The purpose of the long physical sector feature set is to allow increased media format efficiency. During write operations devices calculate and error correction code, ECC and write the ECC on the media following the data. ECC encoding is more efficient when used over a larger amount of data.

The long physical sector feature set allows a device to be formatted so that there are multiple logical sectors per physical sector on the media. Each physical sector has an ECC field. This allows, for example, a device to have 2 048 word physical sectors each containing 8 logical sectors or one ECC field per 8 256 word logical sectors, see Figure 8, example 3.

A performance penalty may be incurred when writing to devices that implement long physical sector feature set. A physical sector is read or written in a single operation. If a host system does not write all of the logical sectors in a physical sector during a single command the device may need to read the logical sectors that are not to be changed into memory and then write the entire physical sector, see Annex B.

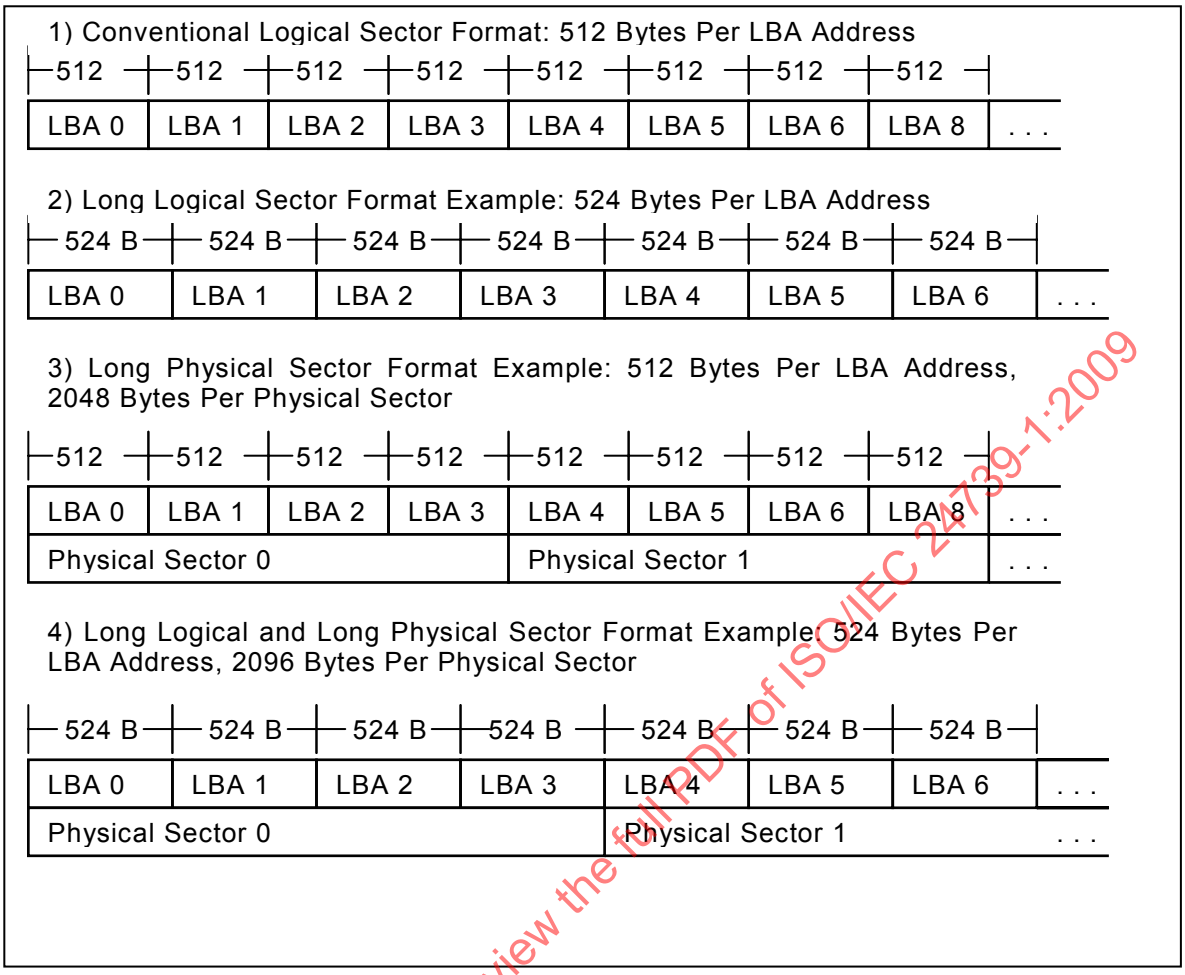


Figure 8 – Long Logical and long Physical Sector Example

4.22 Long logical Sector feature set for non-packet devices

The purpose of the long logical sector feature set is to allow additional data words per sector for server applications. Sectors with 520 or 528 bytes are typical. Devices with long logical sectors set IDENTIFY DEVICE data word 106 bit 13 to 1. The Long Logical Sector length is described by IDENTIFY DEVICE data words 117 to 118.

Devices that implement the Long Logical Sector feature set are not backward compatible with applications that use 256 word logical sectors, e.g. desktop and laptop system.

Table 8 – Long logical sector function

Command	Words per sector transferred
CFA ERASE SECTORS	-
CFA REQUEST EXTENDED ERROR CODE	-
CFA TRANSLATE SECTOR	IDENTIFY DEVICE data words 117 to 118
CFA WRITE MULTIPLE WITHOUT ERASE	IDENTIFY DEVICE data words 117 to 118
CFA WRITE SECTORS WITHOUT ERASE	-
CHECK MEDIA CARD TYPE	-
CHECK POWER MODE	-
CONFIGURE STREAM	-
DEVICE CONFIGURATION	-
DEVICE RESET	-
DOWNLOAD MICROCODE	256
EXECUTE DEVICE DIAGNOSTIC	-
FLUSH CACHE	-
FLUSH CACHE EXT	-
GET MEDIA STATUS	-
IDENTIFY DEVICE	256
IDENTIFY PACKET DEVICE	-
IDLE	-
IDLE IMMEDIATE	-
MEDIA EJECT	-
MEDIA LOCK	-
MEDIA UNLOCK	-
NOP	-
PACKET	-
READ BUFFER	256
READ DMA	IDENTIFY DEVICE data words 117 to 118
READ DMA EXT	IDENTIFY DEVICE data words 117 to 118
READ DMA QUEUED	IDENTIFY DEVICE data words 117 to 118
READ DMA QUEUED EXT	IDENTIFY DEVICE data words 117 to 118
READ LOG EXT	256
READ MULTIPLE	IDENTIFY DEVICE data words 117 to 118
READ MULTIPLE EXT	IDENTIFY DEVICE data words 117 to 118
READ NATIVE MAX ADDRESS	-
READ NATIVE MAX ADDRESS EXT	-
READ SECTOR(S)	IDENTIFY DEVICE data words 117 to 118
READ SECTOR(S) EXT	IDENTIFY DEVICE data words 117 to 118
READ STREAM DMA EXT	IDENTIFY DEVICE data words 117 to 118
READ STREAM EXT	IDENTIFY DEVICE data words 117 to 118
READ VERIFY SECTOR(S)	IDENTIFY DEVICE data words 117 to 118
READ VERIFY SECTOR(S) EXT	-
SECURITY DISABLE PASSWORD	256
SECURITY ERASE PREPARE	-

Command	Words per sector transferred
SECURITY ERASE UNIT	256
SECURITY FREEZE LOCK	-
SECURITY SET PASSWORD	256
SECURITY UNLOCK	256
SEEK	-
SERVICE	-
SET FEATURES	-
SET MAX SET PASSWORD	256
SET MAX LOCK	-
SET MAX FREEZE LOCK	-
SET MAX UNLOCK	256
SET MAX ADDRESS	-
SET MAX ADDRESS EXT	-
SET MULTIPLE MODE	-
SLEEP	-
SMART DISABLE OPERATIONS	-
SMART ENABLE/DISABLE AUTOSAVE	-
SMART ENABLE OPERATIONS	-
SMART EXECUTE OFF-LINE IMMEDIATE	-
SMART READ DATA	256
SMART READ LOG	256
SMART RETURN STATUS	-
SMART WRITE LOG	256
STANDBY	-
STANDBY IMMEDIATE	-
WRITE BUFFER	256
WRITE DMA	IDENTIFY DEVICE data words 117 to 118
WRITE DMA EXT	IDENTIFY DEVICE data word 117
WRITE DMA QUEUED	IDENTIFY DEVICE data word 117
WRITE DMA QUEUED EXT	IDENTIFY DEVICE data word 117
WRITE LOG EXT	256
WRITE MULTIPLE	IDENTIFY DEVICE data word 117
WRITE MULTIPLE EXT	IDENTIFY DEVICE data word 117
	(continued)
WRITE SECTOR(S)	IDENTIFY DEVICE data word 117
WRITE SECTOR(S) EXT	IDENTIFY DEVICE data word 117
WRITE STREAM DMA EXT	IDENTIFY DEVICE data word 117
WRITE STREAM EXT	IDENTIFY DEVICE data word 117

Table 8 describes the command behavior of drives that have been manufactured with long logical sectors. Data transfer commands transfer either the long logical sector length or 256 words depending on the command. For example, Read and Write Extended commands transfer data in long logical sectors while READ LOG EXT and WRITE LOG EXT commands transfer 256 words per sector, regardless of the logical sector length. Figure 8 example 2 shows a diagram of a device formatted with long logical sectors.

4.23 Devices implementing the Long Physical Sector Feature Set and the Long Logical Feature Sector Set

The long physical sector feature set and the long logical sector feature set are not exclusive. Figure 8, example 4 illustrates a device implementing both the Long Physical Sector and Long Logical Sector feature sets.

5 I/O register descriptions

5.1 Overview

The Command Block registers are used for sending commands to the device or posting status from the device. The Control Block registers are used for device control and to post alternate status. Table 9 identifies these registers for both devices that implement and do not implement the PACKET command feature set.

References to parallel implementation bus signals (e.g. DMACK, DMARQ, etc) apply only to parallel implementations. See ISO/IEC 24739-3 for additional information on serial protocol. Some register bits (e.g. nIEN, SRST, etc.) have different requirements in the serial implementation (see ISO/IEC 24739-3).

Table 9 – I/O registers

Registers used by devices not implementing the PACKET command feature set		Registers used by devices implementing the PACKET command feature set	
Command Block registers		Command Block registers	
When read	When written	When read	When written
Data	Data	Data	Data
Error	Features	Error	Features
Sector count	Sector count	Interrupt reason	Sector count
LBA Low	LBA Low	LBA Low	LBA Low
LBA Mid	LBA Mid	Byte Count Low	Byte Count Low
LBA High	LBA High	Byte Count High	Byte Count High
Device	Device	Device select	Device select
Status	Command	Status	Command
Alternate Status	Device Control	Alternate Status	Device Control

Each register description in the following subclauses contain the following format:

- Direction specifies if the register is read/write, read only, or write only from the host.
- Access restrictions specifies when the register may be accessed.
- Effect specifies the effect of accessing the register.
- Functional description describes the function of the register.
- Field/bit description describes the content of the register.

5.2 Alternate Status register

5.2.1 Direction

This register is read only. If this address is written to by the host, the Device Control register is written.

5.2.2 Access restrictions

When the BSY bit is set to one, the other bits in this register shall not be used. The contents of this register are not valid while the device is in Sleep mode.

5.2.3 Effect

Reading this register shall not clear a pending interrupt.

5.2.4 Functional description

This register contains the same information as the Status register in the Command Block.

See 5.14 for definitions of the bits in this register.

5.3 Command register

5.3.1 Direction

This register is write only. If this address is read by the host, the Status register is read.

5.3.2 Access restrictions

For all commands except DEVICE RESET, this register shall only be written when BSY and DRQ are both cleared to zero and DMACK− is not asserted. If written when BSY or DRQ is set to one, the results of writing the Command register are indeterminate except for the DEVICE RESET command. For a device in the Sleep mode, writing of the Command register shall be ignored except for writing of the DEVICE RESET command to a device that implements the PACKET Command feature set.

5.3.3 Effect

Command processing begins when this register is written. The content of the Command Block registers become parameters of the command when this register is written. Writing this register clears any pending interrupt condition.

5.3.4 Functional description

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The executable commands and the command codes for each command are summarized in Tables A.1 to A.3.

5.3.5 Field/bit description

7	6	5	4	3	2	1	0
Command code							

5.4 Data port

5.4.1 Direction

This port is read/write.

5.4.2 Access restrictions

This port shall be accessed for host DMA data transfers only when DMACK− and DMARQ are asserted.

5.4.3 Effect

DMA data-out transfers are processed by a series of writes to this port, each write transferring the data that follows the previous write. DMA data-in transfers are processed by a series of reads to this port, each read transferring the data that follows the previous read. The results of a read during a DMA out or a write during a DMA in are indeterminate.

5.4.4 Functional description

The data port is 16-bits in width.

5.4.5 Field/bit description

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

5.5 Data register

5.5.1 Direction

This register is read/write.

5.5.2 Access restrictions

This register shall be accessed for host PIO data transfer only when DRQ is set to one and DMACK− is not asserted. The contents of this register are not valid while a device is in the Sleep mode.

5.5.3 Effect

PIO data-out transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. PIO data-in transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. The results of a read during a PIO out or a write during a PIO in are indeterminate.

5.5.4 Functional description

The data register is 16 bits wide. When a CFA device is in 8-bit PIO data transfer mode this register is 8 bits wide using only DD7 to DD0.

5.5.5 Field/bit description

15	14	13	12	11	10	9	8
Data (15:8)							

7	6	5	4	3	2	1	0
Data (7:0)							

5.6 Device register

5.6.1 Direction

This register is read/write.

5.6.2 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK− is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. For devices not implementing the PACKET Command feature set, the contents of this register are not valid while a device is in the Sleep mode. For devices implementing the PACKET Command feature set, the contents of this register are valid while the device is in Sleep mode.

5.6.3 Effect

The DEV bit becomes effective when this register is written by the host or the signature is set by the device. All other bits in this register become a command parameter when the Command register is written.

5.6.4 Functional description

Bit 4, DEV, in this register selects the device. Other bits in this register are command dependent (see Clause 6).

5.6.5 Field/bit description

7	6	5	4	3	2	1	0
Obsolete	#	Obsolete	DEV	#	#	#	#

– Obsolete - These bits are obsolete.

NOTE Some hosts set these bits to one. Devices shall ignore these bits.

– # - The content of these bits is command dependent (see Clause 6).

– DEV - Device select. Cleared to zero selects Device 0. Set to one selects Device 1.

5.7 Device control register

5.7.1 Direction

This register is write only. If this address is read by the host, the Alternate Status register is read.

5.7.2 Access restrictions

This register shall only be written when DMACK− is not asserted.

5.7.3 Effectiveness

The content of this register shall take effect when written.

5.7.4 Functional description

This register allows a host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When the Device Control register is written, both devices respond to the write regardless of which device is selected. When the SRST bit is set to one, both devices shall perform the software reset protocol. The device shall respond to the SRST bit when in the SLEEP mode.

5.7.5 Field/bit description

7	6	5	4	3	2	1	0
HOB	r	r	r	r	SRST	nIEN	0

- HOB (high order byte) is defined by the 48-bit Address feature set (see 4.14). A write to any Command Block register shall clear the HOB bit to zero.
- Bits (6:3) are reserved.
- SRST is the host software reset bit (see Clause 11).
- nIEN is the enable bit for the device assertion of INTRQ to the host. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer and shall be asserted or negated by the device as appropriate. When the nIEN bit is set to one or the device is not selected, the device shall release the INTRQ signal.
- Bit 0 shall be cleared to zero.

5.8 Error register

5.8.1 Direction

This register is read only. If this address is written to by the host, the Features register is written.

5.8.2 Access restrictions

The contents of this register shall be valid when BSY and DRQ are cleared to zero and either ERR or SE is set to one. The contents of this register shall be valid upon completion of power-on, or after a hardware or software reset or after command completion of an EXECUTE DEVICE DIAGNOSTICS or DEVICE RESET command. The contents of this register are not valid while a device is in the Sleep mode.

5.8.3 Effect

None.

5.8.4 Functional description

At command completion of any command except EXECUTE DEVICE DIAGNOSTIC or DEVICE RESET, the contents of this register are valid when the ERR bit is set to one in the Status register.

Following a power-on, a hardware or software reset (see Clause 11), or command completion of an EXECUTE DEVICE DIAGNOSTIC or DEVICE RESET command (see Clause 6) this register contains a diagnostic code.

5.8.5 Field/bit description

7	6	5	4	3	2	1	0
#	#	#	#	#	ABRT	#	#

- Bit 2 ABRT (command aborted) is set to one to indicate the requested command has been command aborted because the command code or a command parameter is invalid, the command is not supported, a prerequisite for the command has not been met, or some other error has occurred.
- # The content of this bit is command dependent (see Clause 6).

5.9 Features register

5.9.1 Direction

This register is write only. If this address is read by the host, the Error register is read.

5.9.2 Access restrictions

This register shall be written only when BSY and DRQ equal zero and DMACK− is not asserted. If this register is written when BSY or DRQ is set to one, the result is indeterminate.

5.9.3 Effect

The content of this register becomes a command parameter when the Command register is written.

5.9.4 Functional description

The content of this register is command dependent (see Clause 6).

5.10 LBA High/Byte Count High register

5.10.1 Direction

This register is read/write.

5.10.2 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK− is not asserted. The contents of this register are valid only when BSY and DRQ are cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

5.10.3 Effect

The content of this register becomes a command parameter when the Command register is written.

5.10.4 Functional description

The content of this register is command dependent (see Clause 6). For devices not implementing the PACKET command feature set, this register is called the LBA High register. For devices implementing the PACKET command feature set, this register is called the Byte Count High register.

5.11 LBA Low register

5.11.1 Direction

This register is read/write.

5.11.2 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK− is not asserted. The contents of this register are valid only when both BSY and DRQ are cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

5.11.3 Effect

The content of this register becomes a command parameter when the Command register is written.

5.11.4 Functional description

The content of this register is command dependent (see Clause 6).

5.12 LBA Mid/Byte Count Low register

5.12.1 Direction

This register is read/write.

5.12.2 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK− is not asserted. The contents of this register are valid only when BSY and DRQ are cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

5.12.3 Effect

The content of this register becomes a command parameter when the Command register is written.

5.12.4 Functional description

The content of this register is command dependent (see Clause 6). For devices not implementing the PACKET command feature set, this register is called the LBA Mid register. For devices implementing the PACKET command feature set, this register is called the Byte Count Low register.

5.13 Sector Count/Interrupt Reason register

5.13.1 Direction

This register is read/write.

5.13.2 Access restrictions

This register shall be written only when both BSY and DRQ are cleared to zero and DMACK− is not asserted. The contents of this register are valid only when both BSY and DRQ are cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminate. The contents of this register are not valid while a device is in the Sleep mode.

5.13.3 Effect

The content of this register becomes a command parameter when the Command register is written.

5.13.4 Functional description

The content of this register is command dependent (see Clause 6). For devices not implementing the PACKET command feature set, this register is called the Sector Count register. For devices implementing the PACKET command feature set, this register is called the Interrupt Reason register.

5.14 Status register

5.14.1 Direction

This register is read only. If this address is written to by the host, the Command register is written.

5.14.2 Access restrictions

The contents of this register, except for BSY, shall be ignored when BSY is set to one. The contents of this register are not valid while a device is in the Sleep mode.

5.14.3 Effect

Reading this register when an interrupt is pending causes the Interrupt Pending to be cleared (see Clause 8). The host should not read the Status register when an interrupt is expected as this may clear the Interrupt Pending before the INTRQ can be recognized by the host.

5.14.4 Functional description

This register contains the device status. The contents of this register are updated to reflect the current state of the device.

5.14.5 Field/bit description

5.14.5.1 General

7	6	5	4	3	2	1	0
BSY	DRDY	DF/SE	#	DRQ	Obsolete	Obsolete	ERR / CHK

5.14.5.2 BSY (Busy)

BSY is set to one to indicate that the device is busy. After the host has written the Command register the device shall have either the BSY bit set to one, or the DRQ bit set to one, until command completion or the device has performed a bus release for an overlapped command.

The BSY bit shall be set to one by the device only when one of the following events occurs:

- after either the negation of RESET- or the setting of the SRST bit to one in the Device Control register;
- after writing the Command register if the DRQ bit is not set to one;
- between blocks of a data transfer during PIO data-in commands before the DRQ bit is cleared to zero;
- after the transfer of a data block during PIO data-out commands before the DRQ bit is cleared to zero;
- during the data transfer of DMA commands either the BSY bit, the DRQ bit, or both shall be set to one;
- after the command packet is received during the execution of a PACKET command.

NOTE The BSY bit may be set to one and then cleared to zero so quickly, that host detection of the BSY bit being set to one is not certain.

When BSY is set to one, the device has control of the Command Block Registers and:

1) a write to a Command Block register by the host shall cause indeterminate behavior except for writing DEVICE RESET command;
2) a read from a Command Block register by the host may yield invalid contents except for the BSY bit itself.

The BSY bit shall be cleared to zero by the device:

1) after setting DRQ to one to indicate the device is ready to transfer data;
2) at command completion;
3) upon releasing the bus for an overlapped command;
4) when the device is ready to accept commands that do not require DRDY during a power-on, hardware or software reset.

When BSY is cleared to zero, the host has control of the Command Block registers, the device shall:

1) not set DRQ to one;
2) not change ERR bit;
3) not change the content of any other Command Block register;

4) set the SERV bit to one when ready to continue an overlapped command that has been bus released.

5) clear the DSC bit to zero when an action that uses this bit is completed.

5.14.5.3 DRDY (Device ready)

The DRDY bit shall be cleared to zero by the device

1) when power-on, hardware or software reset or DEVICE RESET or EXECUTE DEVICE DIAGNOSTIC commands for devices implementing the PACKET command feature set.

When the DRDY bit is cleared to zero, the device shall accept and attempt to execute commands as described in ISO/IEC 24739-2, Clause 11.

The DRDY bit shall be set to one by the device

1) when the device is capable of accepting all commands for devices not implementing the PACKET command feature set,

2) prior to command completion except the DEVICE RESET or EXECUTE DEVICE DIAGNOSTIC command for devices implementing the PACKET command feature set.

When the DRDY bit is set to one

1) the device shall accept and attempt to execute all implemented commands,

2) devices that implement the Power Management feature set shall maintain the DRDY bit set to one when they are in the Idle or Standby modes.

5.14.5.4 DF/SE (Device Fault/Stream Error)

Device Fault is implemented by many but not all commands (see Clause 6). A Device Fault is any event that prevents the device from completing a command that is not the result of an error described in the Error register. Recovery from Device Fault is device specific. See Streaming Command feature Set, (see Clause 4.17) for description of SE bit.

5.14.5.5 Command dependent

The use of bits marked with # are command dependent (see Clause 6). Bit 4 was formerly the DSC (Device Seek Complete) bit.

5.14.5.6 DRQ (Data request)

DRQ indicates that the device is ready to transfer data between the host and the device. After the host has written the Command register the device shall either set the BSY bit to one or the DRQ bit to one, until command completion or the device has performed a bus release for an overlapped command.

The DRQ bit shall be set to one by the device

1) when BSY is set to one and data is ready for PIO transfer,

2) during the data transfer of DMA commands either the BSY bit, the DRQ bit or both shall be set to one.

When the DRQ bit is set to one, the host may

1) transfer data via PIO mode,

2) transfer data via DMA mode if DMARQ and DMACK− are asserted.

The DRQ bit shall be cleared to zero by the device

1) when the last word of the data transfer occurs;

2) when the last word of the command packet transfer occurs for a PACKET command.

When the DRQ bit is cleared to zero, the host may

1) transfer data via DMA mode if DMARQ and DMACK- are asserted and BSY is set to one.

5.14.5.7 Obsolete bits

Some bits in this register were defined in previous ATA standards but have been declared obsolete in this standard.

5.14.5.8 ERR/CHK (Error/Check)

ERR indicates that an error occurred during execution of the previous command. For the PACKET and SERVICE commands, this bit is defined as CHK and indicates that an exception condition exists (see clause 2).

The ERR bit shall be set to one by the device

1) when BSY or DRQ is set to one and an error occurs in the executing command.

When the ERR bit is set to one

2) the bits in the Error register shall be valid,
3) the device shall not change the contents of the following registers until a new command has been accepted, the SRST bit is set to one or RESET- is asserted:
   - Error register;
   - LBA High/Mid/Low registers;
   - Sector Count register;
   - Device register.

The ERR bit shall be cleared to zero by the device

4) when a new command is written to the Command register,
5) when the SRST bit is set to one,
6) when the RESET− signal is asserted.

When the ERR bit is cleared to zero at the end of a command the content of the Error register shall be ignored by the host.

References to parallel implementation bus signals (e.g. DMACK, DMARQ, etc) apply only to parallel implementations. Some register bits (e.g. nIEN, SRST, etc.) are handled differently in the serial implementation (see ISO/IEC 24739-3).

5.15 Signature and persistence

5.15.1 Signature for devices not implementing the PACKET command feature set

A device not implementing the PACKET command feature set shall place the signature in the Command Block registers listed below for power-on reset, hardware reset, software reset, and the EXECUTE DEVICE DIAGNOSTIC command.

If the device does not implement the PACKET command feature set, the signature shall be:

Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h

A device implementing the PACKET command feature set shall place the signature in the Command Block registers listed below for power-on reset, hardware reset, software reset, the EXECUTE DEVICE DIAGNOSTIC command, and the DEVICE RESET command. The DEVICE RESET command shall not change the value of the DEV bit when writing the signature into the Device register for a device implementing the PACKET command feature set. If the device

implements the PACKET command feature set, the signature is also written in the registers for the IDENTIFY DEVICE and READ SECTOR(S) commands.

5.15.2 Signature for devices implementing the PACKET command feature set

If the device implements the PACKET command feature set, the signature shall be:

Interrupt Reason	01h
LBA Low	01h
Byte Count Low	14h
Byte Count High	EBh

If the PACKET command feature set is implemented by a device, then the signature values written by the device in the Command Block registers following power-on reset, hardware reset, software reset, or the DEVICE RESET command shall not be changed by the device until the device receives a command that sets DRDY to one. Writes by the host to the Command Block registers that contain the signature values shall overwrite the signature values and invalidate the signature.

5.15.3 Reserved signatures for Serial ATA working groups

The following signatures are Reserved. The uses of these signatures is not defined by this standard.

Signature 3Ch:

Sector Count	01h
LBA Low	01h
LBA Mid	3Ch
LBA High	C3h

Signature 69h:

Interrupt Reason	01h
LBA Low	01h
Byte Count Low	69h
Byte Count High	96h

5.16 Single device configurations

5.16.1 Device 0 only configurations

In a single device configuration where Device 0 is the only device and the host selects Device 1, Device 0 shall respond as follows:

1) a write to the Device Control register shall complete as if Device 0 was the selected device;
2) a write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected;
3) a write to the Command register shall be ignored, except for EXECUTE DEVICE DIAGNOSTIC;
4) if the device does not implement the PACKET Command feature set, a read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected. A read of the Status or Alternate status register shall return the value 00h.;
5) if the device implements the PACKET Command feature set, a read of the Control Block or Command Block registers shall return the value 00h.

NOTE Even though Device 1 is not present, the register content may appear valid for Device 1. Further means may be necessary to determine the existence of Device 1 (e.g., issuing a command).

5.16.2 Device 1 only configurations

Host support of Device 1 only configurations is host specific.

In a single device configuration where Device 1 is the only device and the host selects Device 0, Device 1 shall respond to accesses of the Command Block and Control Block registers in the same way it would if Device 0 was present. This is because Device 1 cannot determine if Device 0 is, or is not, present.

Host implementation of read and write operations to the Command and Control Block registers of non-existent Device 0 are host specific.

The remainder of this subclause is a recommendation for hosts. The host implementer should be aware of the following when supporting Device 1 only configurations.

1) Following a hardware reset or software reset, the following steps may be used to reselect Device 1:
   a) Write to the Device register with DEV bit set to one;
   b) Using one or more of the Command Block registers that may be both written and read, such as the Sector Count or LBA Low, write a data pattern other than 00h or FFh to the register(s);
   c) Read the register(s) written in step (b). If the data read is the same as the data written, proceed to step (e);
   d) Repeat steps (a) to (c) until the data matches in step (c) or until 31 s has past. After 31 s the host may assume that Device 1 is not functioning properly;
   e) Read the Status register and Error registers. Check the Status and Error register contents for any error conditions that Device 1 may have posted.

   Following the execution of an EXECUTE DEVICE DIAGNOSTIC command, no Interrupt Pending should be set to signal command completion. After writing the EXECUTE DEVICE DIAGNOSTIC command to the Command register, execute steps a) to e) as described in 1) above;

   At all other times, do not write zero into the DEV bit of the Device register. All other commands execute normally.

6 Command descriptions

6.1 Overview

Commands are issued to the device by loading the required registers in the command block with the needed parameters and then writing the command code to the Command register. Required registers are those indicated by a specific content in the Inputs table for the command, i.e., not noted as na or obs.

References to parallel implementation bus signals (e.g. DMACK, DMARQ, etc) apply only to parallel implementations. See ISO/IEC 24739-3 for additional information on serial protocol. Some register bits (e.g. nIEN, SRST, etc.) have different requirements in the serial implementation (see ISO/IEC 24739-3).

- Each command description in the following clauses contains the following subclauses:
- Command code specifies the command code for this command.
- Feature set specifies feature set and if the command is mandatory or optional.
- Protocol specifies which protocol is used by the command (see Clause 11).
- Inputs describes the Command Block register data that the host shall supply.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
LBA Low								
LBA Mid								
LBA High								
Device								
Command	Command code							

NOTE
– na specifies the content of a bit or field is not applicable to the particular command.
– obs specifies that the use of this bit is obsolete.

Normal outputs describes the Command Block register data returned by the device at the end of a command.

Register	7	6	5	4	3	2	1	0
Error								
Sector Count								
LBA Low								
LBA Mid								
LBA High								
Device								
Status								

NOTE
– na specifies the content of a bit or field is not applicable to the particular command.
– obs specifies that the use of this bit is obsolete.

Error outputs describes the Command Block register data that shall be returned by the device at command completion with an unrecoverable error.

Register	7	6	5	4	3	2	1	0
Error								
Sector Count								
LBA Low								
LBA Mid								
LBA High								
Device								
Status								

NOTE
– na specifies the content of a bit or field is not applicable to the particular command.
– obs specifies that the use of this bit is obsolete..

Prerequisites, any prerequisite commands or conditions that shall be met before the command is issued.

Description, the description of the command function(s).

6.2 CFA ERASE SECTORS

6.2.1 Command code

C0h

6.2.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

This command code is Vendor Specific for devices not implementing the CFA feature set.

6.2.3 Protocol

Non-data (see Clause 11).

6.2.4 Inputs

The LBA High, LBA Mid, LBA Low, and Device registers specify the starting sector address to be erased. The Sector Count register specifies the number of sectors to be erased.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	C0h							

Sector Count
: number of sectors to be erased. A value of 00h specifies that 256 sectors are to be erased.

LBA Low
: starting LBA bits (7:0).

LBA Mid
: starting LBA bits (15:8).

LBA High
: starting LBA bits (23:16).

Device
: the LBA bit shall be set to one to specify the address is an LBA, starting LBA bits (27:24).

6.2.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be cleared to zero.

6.2.6 Error outputs

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	MED
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	na	na	na	ERR

Error Register
IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.
ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.
MED shall be set to one if a media error is detected.
LBA Low, LBA Mid, LBA High, Device
shall be written with the address of first unrecoverable error.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
ERR shall be set to one if an Error register bit is set to one.

6.2.7 Prerequisites

DRDY set to one.

6.2.8 Description

This command pre-erases and conditions from 1 to 256 sectors as specified in the Sector Count register. This command should be issued in advance of a CFA WRITE SECTORS WITHOUT ERASE or a CFA WRITE MULTIPLE WITHOUT ERASE command to increase the execution speed of the write operation.

6.3 CFA REQUEST EXTENDED ERROR CODE

6.3.1 Command code

03h

6.3.2 Feature set

CFA feature set.

- If the CFA feature set is implemented this command shall be implemented.

6.3.3 Protocol

Non-data (see Clause 11).

6.3.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	03h							

6.3.5 Normal outputs

The extended error code written into the Error register is an 8-bit code. Table 10 defines these values.

Register	7	6	5	4	3	2	1	0
Error	Extended error code							
Sector Count	Vendor specific							
LBA Low	Vendor specific							
LBA Mid	Vendor specific							
LBA High	Vendor specific							
Device	obs	na	obs	DEV	Vendor specific			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
Extended error code.
LBA Low, LBA Mid, LBA High, Device
May contain additional information.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be cleared to zero.

Table 10 – Extended error codes

Extended error code	Description
00h	No error detected / no additional information
01h	Self-test passed
03h	Write / Erase failed
05h	Self-test or diagnostic failed
09h	Miscellaneous error
0Bh	Vendor specific
0Ch	Corrupted media format
0D-0Fh	Vendor specific
10h	ID Not Found / ID Error
11h	Uncorrectable ECC error
14h	ID Not Found
18h	Corrected ECC error
1Dh, 1Eh	Vendor specific
1Fh	Data transfer error / command aborted
20h	Invalid command
21h	Invalid address
22-23h	Vendor specific
27h	Write protect violation
2Fh	Address overflow (address too large)
30-34h	Self-test or diagnostic failed
35h, 36h	Supply or generated voltage out of tolerance
37h, 3Eh	Self-test or diagnostic failed
38h	Corrupted media format
39h	Vendor specific
3Ah	Spare sectors exhausted
3Bh 3Ch, 3Fh	Corrupted media format
3Dh	Vendor specific
All other values	Reserved

6.3.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	na	na	na	ERR

Error Register

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
ERR shall be set to one if an Error register bit is set to one.

6.3.7 Prerequisites

DRDY set to one.

6.3.8 Description

This command provides an extended error code which identifies the cause of an error condition in more detail than is available with Status and Error register values. The CFA REQUEST EXTENDED ERROR CODE command shall return an extended error code if the previous command completed with an error or a no error detected extended error code if the previous command completed without error.

6.4 CFA TRANSLATE SECTOR

6.4.1 Command code

87h

6.4.2 Feature set

CFA feature set

– If the CFA feature set is implemented this command shall be implemented.

This command code is vendor specific for devices not implementing the CFA feature set.

6.4.3 Protocol

PIO data-in (see Clause 11).

6.4.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	87h							

LBA Low
LBA bits (7:0).
LBA Mid
LBA bits (15:8).
LBA High
LBA bits (23:16).
Device
the LBA bit shall be set to one to specify the address is an LBA, LBA bits (27:24).

6.4.5 Normal outputs

A 512 byte information table is transferred to the host. Table 11 defines these values.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be cleared to zero.

Table 11 – CFA TRANSLATE SECTOR Information

Byte	Description
00h	Obsolete
01h	Obsolete
02h	Obsolete
03h	Obsolete
04h	LBA bits (23:16)
05h	LBA bits (15:8)
06h	LBA bits (7:0)
07-12h	Reserved
13h	Sector erased flag (FFh = erased; 00h = not erased)
14-17h	Reserved
18h	Sector write cycles count bits (23:16)
19h	Sector write cycles count bits (15:8)
1Ah	Sector write cycles count bits (7:0)
1B-FFh	Reserved

6.4.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	na	na	na	ERR

Error Register

ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
ERR shall be set to one if an Error register bit is set to one.

6.4.7 Prerequisites

DRDY set to one.

6.4.8 Description

This command provides information related to a specific sector. The data indicates the erased or not erased status of the sector and the number of erase and write cycles performed on that sector. Devices may return zero in fields that do not apply or that are not supported by the device.

6.5 CFA WRITE MULTIPLE WITHOUT ERASE

6.5.1 Command code

CDh

6.5.2 Feature set

CFA feature set.

– If the CFA feature set is implemented this command shall be implemented.

6.5.3 Protocol

PIO data-out (see Clause 11).

6.5.4 Inputs

The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	CDh							

Sector Count

number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low

starting LBA bits (7:0).

LBA Mid

starting LBA bits (15:8).

LBA High

starting LBA bits (23:16).

Device/Head

the LBA bit shall be set to one to specify the address is an LBA, starting LBA bits (27:24).

6.5.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be cleared to zero.

6.5.6 Error outputs

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	MED
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error Register

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.
ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.
MED shall be set to one if a media error is detected

LBA Low, LBA Mid, LBA High, Device

shall be written with the address of first unrecoverable error.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.5.7 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE data word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall precede a CFA WRITE MULTIPLE WITHOUT ERASE command.

6.5.8 Description

This command is similar to the WRITE MULTIPLE command. Interrupts are not generated on every sector, but on the transfer of a block that contains the number of sectors defined by the SET MULTIPLE MODE.

Command execution is identical to the WRITE MULTIPLE operation except that the sectors are written without an implied erase operation. The sectors should be pre-erased by a preceding CFA ERASE SECTORS command.

6.6 CFA WRITE SECTORS WITHOUT ERASE

6.6.1 Command code

38h

6.6.2 Feature set

CFA feature set.

– If the CFA feature set is implemented this command shall be implemented.

6.6.3 Protocol

PIO data-out (see Clause 11).

6.6.4 Inputs

The LBA Mid, LBA High, Device and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	38h							

Sector Count
: number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low
: starting LBA bits (7:0).

LBA Mid
: starting LBA bits (15:8).

LBA High
: starting LBA bits (23:16).

Device
: the LBA bit shall be set to one to specify the address is an LBA, starting LBA bits (27:24).

6.6.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be cleared to zero.

6.6.6 Error outputs

The device shall return command aborted if the command is not supported. An unrecoverable error encountered during execution of this command results in the termination of the command. The command block registers contain the address of the sector where the first unrecovered error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	MED
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error Register
IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.
ABRT shall be set to one if the command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.
MED shall be set to one if a media error is detected.
LBA Low, LBA Mid, LBA High, Device
shall be written with the address of first unrecoverable error.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.6.7 Prerequisites

DRDY set to one.

6.6.8 Description

This command is similar to the WRITE SECTORS command. Command execution is identical to the WRITE SECTORS operation except that the sectors are written without an implied

erase operation. The sectors should be pre-erased by a preceding CFA ERASE SECTORS command.

6.7 CHECK MEDIA CARD TYPE

6.7.1 Command code

D1h

6.7.2 Feature set

Mandatory when the Media Card Pass Through Command feature set is implemented.

6.7.3 Protocol

Non-data (see Clause 11)

6.7.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							ENB
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	D1h							

Feature register

ENB shall be set to one to enable the Media Card Pass Through Command feature set. ENB cleared to zero shall disable the Media Card Pass Through Command feature set.

NOTE Power-on, hardware, or software reset disables the Media Card Pass Through Command feature set.

Device register

DEV shall specify the selected device.

6.7.5 Normal outputs

The device shall return 55H in Sector Count register and AAH in LBA Low register.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	55h							
LBA Low	AAh							
LBA Mid	Card specific data							
LBA High	Card specific data							
Device	obs	na	obs	DEV	WP	Media Type		
Status	BSY	DRDY	DF	na	DRQ	0	0	ERR

Sector Count register shall contain 55H
LBA Low register shall contain AAH
LBA Mid register shall contain card-specific data
LBA High register shall contain card-specific data
Device register

DEV shall indicate the selected device

WP shall be set to one if the device is write protected, WP shall be cleared to zero if the device is not write protected.
Media Type shall be set as follows:

001b	SD Memory Card
010b	MMC
011b	SD IO Card
100b	Smart Media card
000b, 101b-111b	Reserved

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.7.6 Error Outputs

If this command is not supported or there is an error in processing this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one If the command is not supported or if an error occurred during the execution of the command.
Device/Head register
DEV shall indicate the selected device.
Status register
ERR (B0) shall be set to 1 to indicate error occurred.
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.7.7 Description

The CHECK MEDIA CARD TYPE command allows the host to determine if the device supports the Media Card Pass Through Command feature set. If the ENB bit in the Features register is set to one, IDENTIFY DEVICE data bit 3 word 87 shall be set to one upon successful command completion.

If the adapter supports the Media Card Pass Through Command feature set and the ENB bit of the Features register is set to one, the adapter shall process any further Media Card Pass Through Command feature set commands. If the ENB bit is cleared to zero, the adapter shall not interpret the command codes D2 through D4 as the Media Card Pass Through Command feature set commands. If the adapter does not support the Media Card Pass Through Command feature set or the host has disabled the Media Card Pass Through Command feature set mode by clearing the ENB bit to zero, the host shall not send any further Media Card Pass Through Command feature set commands to the adapter.

6.8 CHECK POWER MODE

6.8.1 Command code

E5h

6.8.2 Feature set

Power Management feature set.

- This command is mandatory for devices not implementing the PACKET Command feature set.
- Power Management feature set is mandatory when power management is not implemented by the PACKET command set implemented by the device.
- This command is mandatory when the Power Management feature set is implemented.

6.8.3 Protocol

Non-data command (see Clause 11).

6.8.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	E5h							

Device register

DEV shall specify the selected device.

6.8.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Result value							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

Device register

DEV shall indicate the selected device.

Sector Count result value
00h - device is in Standby mode.
80h - device is in Idle mode.
FFh - device is in Active mode or Idle mode.

6.8.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.8.7 Prerequisites

DRDY set to one.

6.8.8 Description

The CHECK POWER MODE command allows the host to determine the current power mode of the device. The CHECK POWER MODE command shall not cause the device to change power or affect the operation of the Standby timer.

6.9 CONFIGURE STREAM

6.9.1 Command code

51h

6.9.2 Feature set

Mandatory if the Streaming feature set is implemented.

6.9.3 Protocol

Non-data (see Clause 11)

6.9.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	A/R	R/W	Reserved			Stream ID		
	Previous	Default CCTL (7:0)							
Sector Count	Current	AU Size In Sectors (7:0)							
	Previous	AU Size In Sectors (15:8)							
LBA Low	Current	Reserved (7:0)							
	Previous	Reserved (31:24)							
LBA Mid	Current	Reserved (15:8)							
	Previous	Reserved (39:32)							
LBA High	Current	Reserved (23:16)							
	Previous	Reserved (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		51h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Features register current

A/R specifies a request to add a new stream if set to one. If cleared to zero, a request to remove a previous configured stream is specified.

R/W specifies a read stream if cleared to zero and a write stream if set to one.

The Stream ID shall be a value between 0 and 7.

Features register previous

The default Command Completion Time Limit (CCTL). The value is calculated as follows:

(Default CCTL) = ((content of the Features register) × (IDENTIFY DEVICE data words 98 to 99)) µs

This time shall be used by the device when a streaming command with the same stream ID and a CCTL of zero is issued. The time is measured from the write of the command register to the final INTRQ for command completion.

Sector Count Current

The size of an Allocation Unit in sectors (bits 7 to 0).

Sector Count Previous

The size of an Allocation Unit in sectors (bits 15:8).

Device

the LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

6.9.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	SE	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SE shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.9.6 Error Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	ABRT	na	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	SE	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

ABRT shall be set to one if

the drive cannot support the requested stream configuration.

A/R = 0 and the Features Register contains an unconfigured Stream ID.

The Default CCTL cannot be supported by the device.

The device does not support the Streaming Feature Set.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
SE shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be set to one.

6.9.7 Prerequisites

DRDY set to one and BSY cleared to zero.

6.9.8 Description

The CONFIGURE STREAM command specifies the operating parameters of an individual stream. A CONFIGURE STREAM command may be issued for each stream that is to be added or removed from the current operating configuration. If A/R = 1 and the specified Stream ID is already valid at the device, the new parameters shall replace the old parameters, unless Command Abort is returned (see ABRT conditions for Error register). In this case the old parameters for the specified Stream ID shall remain in effect.

6.10 DEVICE CONFIGURATION

6.10.1 General

Individual Device Configuration Overlay feature set commands are identified by the value placed in the Features register. Table 12 shows these Features register values.

Table 12 – Device Configuration Overlay Features register values

Value	Command
C0h	DEVICE CONFIGURATION RESTORE
C1h	DEVICE CONFIGURATION FREEZE LOCK
C2h	DEVICE CONFIGURATION IDENTIFY
C3h	DEVICE CONFIGURATION SET
00h-BFh, C4h-FFh	Reserved

6.10.2 DEVICE CONFIGURATION RESTORE

6.10.2.1 Command code

B1h with a Features register value of C0h.

6.10.2.2 Feature set

Device Configuration Overlay feature set.

– Mandatory when the Device Configuration Overlay feature set is implemented.

6.10.2.3 Protocol

Non-data (see Clause 11)

6.10.2.4 Inputs

The Features register shall be set to C0h.

Register	7	6	5	4	3	2	1	0
Features	C0h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na			DEV	na			
Command	B1h							

Device
DEV shall specify the selected device.

6.10.2.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.10.2.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if the device does not support this command, if a Host Protected Area has been set by a SET MAX ADDRESS or SET MAX ADDRESS EXT command, or if DEVICE CONFIGURATION FREEZE LOCK is set.

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.10.2.7 Prerequisites

DRDY set to one.

6.10.2.8 Description

The DEVICE CONFIGURATION RESTORE command disables any setting previously made by a DEVICE CONFIGURATION SET command and returns the content of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data to the original settings as indicated by the data returned from the execution of a DEVICE CONFIGURATION IDENTIFY command.

6.10.3 DEVICE CONFIGURATION FREEZE LOCK

6.10.3.1 Command code

B1h with a Features register value of C1h.

6.10.3.2 Feature set

Device Configuration Overlay feature set.
– Mandatory when the Device Configuration Overlay feature set is implemented.

6.10.3.3 Protocol

Non-data (see Clause 11).

6.10.3.4 Inputs

The Features register shall be set to C1h.

Register	7	6	5	4	3	2	1	0
Features	C1h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na			DEV	na			
Command	B1h							

Device
DEV shall specify the selected device.

6.10.3.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.10.3.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if the device does not support this command or the device has executed a previous DEVICE CONFIGURATION FREEZE LOCK command since power-up.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.10.3.7 Prerequisites

DRDY set to one.

6.10.3.8 Description

The DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a DEVICE CONFIGURATION FREEZE LOCK command, all DEVICE CONFIGURATION SET, DEVICE

CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands shall be aborted by the device. The DEVICE CONFIGURATION FREEZE LOCK condition shall be cleared by a power-down. The DEVICE CONFIGURATION FREEZE LOCK condition shall not be cleared by hardware or software reset.

6.10.4 DEVICE CONFIGURATION IDENTIFY

6.10.4.1 Command code

B1h with a Features register value of C2h.

6.10.4.2 Feature set

Device Configuration Overlay feature set.

– Mandatory when the Device Configuration Overlay feature set is implemented.

6.10.4.3 Protocol

PIO data-in (see Clause 11).

6.10.4.4 Inputs

The Features register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	C2h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na			DEV	na			
Command	B1h							

Device

DEV shall specify the selected device.

6.10.4.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.10.4.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if the device does not support this command or the device has executed a previous DEVICE CONFIGURATION FREEZE LOCK command since power-up.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.10.4.7 Prerequisites

DRDY set to one.

6.10.4.8 Description

6.10.4.8.1 General

The DEVICE CONFIGURATION IDENTIFY command returns a 512 byte data structure via PIO data-in transfer. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a DEVICE CONFIGURATION SET command has been issued reducing the capabilities, the response to an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command will reflect the reduced set of capabilities, while the DEVICE CONFIGURATION IDENTIFY command will reflect the entire set of selectable capabilities.

The term “is allowed” indicates that the device may report that a feature is supported and/or enabled.

If the device is not “allowed” to report support, then the device shall not support and shall report that the selected feature is both “not supported” and if appropriate “not enabled.”

The format of the Device Configuration Overlay data structure is shown in Table 13.

Table 13 – Device Configuration Identify data structure

Word	Content
0	Data structure revision
1	Multiword DMA modes supported 15-3 Reserved 2 1 = Reporting support for Multiword DMA mode 2 and below is allowed 1 1 = Reporting support for Multiword DMA mode 1 and below is allowed 0 1 = Reporting support for Multiword DMA mode 0 is allowed
2	Ultra DMA modes supported 15-7 Reserved 6 1 = Reporting support for Ultra DMA mode 6 and below is allowed 5 1 = Reporting support for Ultra DMA mode 5 and below is allowed 4 1 = Reporting support for Ultra DMA mode 4 and below is allowed 3 1 = Reporting support for Ultra DMA mode 3 and below is allowed 2 1 = Reporting support for Ultra DMA mode 2 and below is allowed 1 1 = Reporting support for Ultra DMA mode 1 and below is allowed 0 1 = Reporting support for Ultra DMA mode 0 is allowed
3-6	Maximum LBA
7	Command set/feature set supported 15-14 Reserved 13 1 = Reporting support for SMART Conveyance self-test is allowed 12 1 = Reporting support for SMART Selective self-test is allowed 11 1 = Reporting support for Forced Unit Access is allowed 10 Reserved 9 1 = Reporting support for Streaming feature set is allowed 8 1 = Reporting support for 48-bit Addressing feature set is allowed 7 1 = Reporting support for Host Protected Area feature set is allowed 6 1 = Reporting support for Automatic acoustic management is allowed 5 1 = Reporting support for READ/WRITE DMA QUEUED commands is allowed 4 1 = Reporting support for Power-up in Standby feature set is allowed 3 1 = Reporting support for Security feature set is allowed 2 1 = Reporting support for SMART error log is allowed 1 1 = Reporting support for SMART self-test is allowed 0 1 = Reporting support for SMART feature set is allowed
8-9	Reserved for serial ATA
10-254	Reserved
255	Integrity word 15-8 Checksum 7-0 Signature

6.10.4.8.2 Word 0: Data structure revision

Word 0 shall contain the value 0002h.

6.10.4.8.3 Word 1: Multiword DMA modes supported

Word 1 bits (2:0) contain the same information as contained in word 63 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data (see 6.17.31). Bits (15:3) of word 1 are reserved.

6.10.4.8.4 Word 2: Ultra DMA modes supported

Word 2 bits (6:0) contain the same information as contained in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data (see 6.17.44). Bits (15:7) of word 2 are reserved.

6.10.4.8.5 Words 3 to 6: Maximum LBA

Words 3 to 6 define the maximum LBA. This is the highest address accepted by the device in the factory default condition. If no DEVICE CONFIGURATION SET command has been executed modifying the factory default condition, this is the same value as that returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command.

6.10.4.8.6 Word 7: Command/features set supported

Word 7 bit 0 if set to one indicates that the device is allowed to report support for the SMART feature set.
Word 7 bit 1 if set to one indicates that the device allowed to report support for SMART self-test including the self-test log.
Word 7 bit 2 if set to one indicates that the device is allowed to report support for SMART error logging.
Word 7 bit 3 if set to one indicates that the device is allowed to report support for the Security feature set.
Word 7 bit 4 is cleared to zero to disable support for the Power-up in Standby feature set and has the effect of clearing bits (6:5) to zero in word 83 and word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If Power-up in Standby has been enabled by a jumper, these bits shall not be cleared.
Word 7 bit 5 if set to one indicates that the device is allowed to report support for the READ DMA QUEUED and WRITE DMA QUEUED commands.
Word 7 bit 6 if set to one indicates that the device is allowed to report support for the Automatic Acoustic Management feature set.
Word 7 bit 7 if set to one indicates that the device is allowed to report support for the Host Protected Area feature set.
Word 7 bit 8 if set to one indicates that the device is allowed to report support for the 48-bit Addressing feature set.
Word 7 bit 9 if set to one indicates that the device is allowed to report support for Streaming feature set.
Word 7 bit 10 Reserved
Word 7 bit 11 if set to one indicates that the device is allowed to report support for Force Unit Access commands.
Word 7 bit 12 if set to one indicates that the device is allowed to report support for SMART Selective self-test.
Word 7 bit 13 if set to one indicates that the device is allowed to report support for SMART Conveyance self-test.

6.10.4.8.7 Words 8 to 9: Reserved for serial ATA

These words are reserved for future serial ATA use.

6.10.4.8.8 Words 10 to 254: Reserved

6.10.4.8.9 Word 255: Integrity word

Bits (7:0) of this word shall contain the value A5h. Bits (15:8) of this word shall contain the data structure checksum. The data structure checksum shall be the two's complement of the sum of all byte in words 0 to 154 and the byte consisting of bits (7:0) of word 255. Each byte

shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all bytes is zero when the checksum is correct.

6.10.5 DEVICE CONFIGURATION SET

6.10.5.1 Command code

B1h with a Features register value of C3h.

6.10.5.2 Feature set

Device Configuration Overlay feature set.

– Mandatory when the Device Configuration Overlay feature set is implemented.

6.10.5.3 Protocol

PIO data out (see Clause 11).

6.10.5.4 Inputs

The Features register shall be set to C3h.

Register	7	6	5	4	3	2	1	0
Features	C3h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	na			DEV	na			
Command	B1h							

Device

DEV shall specify the selected device.

6.10.5.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.10.5.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	Vendor specific							
LBA Low	Bit location low							
LBA Mid	Bit location high							
LBA High	Word location							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if the device does not support this command, if a DEVICE CONFIGURATION SET command has already modified the original settings as reported by a DEVICE CONFIGURATION IDENTIFY command, if DEVICE CONFIGURATION FREEZE LOCK is set, if any of the bit modification restrictions described in 6.10.5.8 are violated, or if a Host Protected Area has been established by the execution of a SET MAX ADDRESS or SET MAX ADDRESS EXT command, or if an attempt was made to modify a mode or feature that cannot be modified with the device in its current state.

Sector Count

This register may contain a vendor specific value.

LBA Low

If the command was aborted because an attempt was made to modify a mode or feature that cannot be modified with the device in its current state, this register shall contain bits (7:0) set in the bit positions that correspond to the bits in the device configuration overlay data structure words 1, 2 or 7 for each mode or feature that cannot be changed. If not, the value shall be 00h.

LBA Mid

If the command was aborted because an attempt was made to modify a mode or feature that cannot be modified with the device in its current state, this register shall contain bits (15:8) set in the bit positions that correspond to the bits in the device configuration overlay data structure words 1, 2 or 7 for each mode or feature that cannot be changed. If not, the value shall be 00h.

LBA High

If the command was aborted because an attempt was made to modify a bit that cannot be modified with the device in its current state, this register shall contain the offset of the first word encountered that cannot be changed. If an illegal maximum LBA is encountered, the offset of word 3 shall be entered. If a checksum error occurred, the value FFh shall be entered. A value of 00h indicates that the Data Structure Revision was invalid.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.10.5.7 Prerequisites

DRDY set to one.

6.10.5.8 Description

6.10.5.8.1 General

The DEVICE CONFIGURATION SET command allows a device manufacturer or a personal computer system manufacturer to reduce the set of optional commands, modes or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command.

The DEVICE CONFIGURATION SET command transfers an overlay that modifies some of the bits set in words 63, 82, 83, 84 and 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command data. When the bits in these words are cleared, the device shall no longer support the indicated command, mode or feature set. If a bit is set in the overlay transmitted by the device that is not set in the overlay received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit. Modifying the maximum LBA of the device also modifies the address value returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command.

The format of the overlay transmitted by the device is described in Table 14. The restrictions on changing these bits is described in the text following Table 14. If any of the bit modification restrictions described are violated, the device shall return command aborted.

The term “is allowed” indicates that the device may report that a feature is supported and/or enabled.

If the device is not “allowed’ to report support, then the device shall not support and shall report that the selected feature is both “not supported” and if appropriate “not enabled.”

Table 14 – Device Configuration Overlay data structure

Word	Content
0	Data structure revision
1	Multiword DMA modes supported 15-3 Reserved 2 1 = Reporting support for Multiword DMA mode 2 and below is allowed 1 1 = Reporting support for Multiword DMA mode 1 and below is allowed 0 1 = Reporting support for Multiword DMA mode 0 is allowed
2	Ultra DMA modes supported 15-7 Reserved 6 1 = Reporting support for Ultra DMA mode 6 and below is allowed 5 1 = Reporting support for Ultra DMA mode 5 and below is allowed 4 1 = Reporting support for Ultra DMA mode 4 and below is allowed 3 1 = Reporting support for Ultra DMA mode 3 and below is allowed 2 1 = Reporting support for Ultra DMA mode 2 and below is allowed 1 1 = Reporting support for Ultra DMA mode 1 and below is allowed 0 1 = Reporting support for Ultra DMA mode 0 is allowed
3-6	Maximum LBA
7	Command set/feature set supported 15-14 Reserved 13 1 = Reporting support for SMART Conveyance self-test is allowed 12 1 = Reporting support for SMART Selective self-test is allowed 11 1 = Reporting support for Forced Unit Access is allowed 10 -Reserved for technical report 9 1 = Reporting support for Streaming feature set is allowed 8 1 = Reporting support for 48-bit Addressing feature set is allowed 7 1 = Reporting support for Host Protected Area feature set is allowed 6 1 = Reporting support for Automatic acoustic management is allowed 5 1 = Reporting support for READ/WRITE DMA QUEUED commands is allowed 4 1 = Reporting support for Power-up in Standby feature set is allowed 3 1 = Reporting support for Security feature set is allowed 2 1 = Reporting support for SMART error log is allowed 1 1 = Reporting support for SMART self-test is allowed 0 1 = Reporting support for SMART feature set is allowed
8-9	Reserved for serial ATA
10-254	Reserved
255	Integrity word 15-8 Checksum 7-0 Signature

6.10.5.8.2 Word 0: Data structure revision

Word 0 shall contain the value 0002h.

6.10.5.8.3 Word 1: Multiword DMA modes supported

Word 1 bits (15:3) are reserved.
Word 1 bit 2 is cleared to disable support for Multiword DMA mode 2 and has the effect of clearing bit 2 in word 63 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Multiword DMA mode 2 is currently selected.
Word 1 bit 1 is cleared to disable support for Multiword DMA mode 1 and has the effect of clearing bit 1 to zero in word 63 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Multiword DMA mode 2 is supported or Multiword DMA mode 1 or 2 is selected.
Word 1 bit 0 shall not be cleared to zero.

6.10.5.8.4 Word 2: Ultra DMA modes supported

Word 2 bits (15:7) are reserved.

Word 2 bit 6 is cleared to zero to disable support for Ultra DMA mode 6 and has the effect of clearing bit 6 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 6 is currently selected.

Word 2 bit 5 is cleared to zero to disable support for Ultra DMA mode 5 and has the effect of clearing bit 5 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 5 is currently selected.

Word 2 bit 4 is cleared to zero to disable support for Ultra DMA mode 4 and has the effect of clearing bit 4 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 5 is supported or if Ultra DMA mode 5 or 4 is selected.

Word 2 bit 3 is cleared to zero to disable support for Ultra DMA mode 3 and has the effect of clearing bit 3 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 5 or 4 is supported or if Ultra DMA mode 5, 4 or 3 is selected.

Word 2 bit 2 is cleared to zero to disable support for Ultra DMA mode 2 and has the effect of clearing bit 2 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 5, 4 or 3 is supported or if Ultra DMA mode 5, 4, 3 or 2 is selected.

Word 2 bit 1 is cleared to zero to disable support for Ultra DMA mode 1 and has the effect of clearing bit 1 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 5, 4, 3 or 2 is supported or if Ultra DMA mode 5, 4, 3, 2 or 1 is selected.

Word 2 bit 0 is cleared to zero to disable support for Ultra DMA mode 0 and has the effect of clearing bit 0 to zero in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared to zero if Ultra DMA mode 5, 4, 3, 2 or 1 is supported or if Ultra DMA mode 5, 4, 3, 2, 1 or 0 is selected.

6.10.5.8.5 Words 3 to 6: Maximum LBA

Words 3 to 6 define the maximum LBA. This shall be the highest address accepted by the device after execution of the command. When this value is changed, the content of IDENTIFY DEVICE data words 60 to 61 and 100 to 103 shall be changed as described in the SET MAX ADDRESS and SET MAX ADDRESS EXT command descriptions to reflect the maximum address set with this command. This value shall not be changed and command aborted shall be returned if a Host Protected Area has been established by the execution of a SET MAX ADDRESS or SET MAX ADDRESS EXT command with an address value less than that returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command. Any data contained in the Host Protected Area is not affected.

6.10.5.8.6 Word 7: Command/features set supported

Word 7 bits (15:14) are reserved.

Word 7 bit 13 is cleared to zero to disable support for the SMART Conveyance self-test. Subsequent attempts to start this test via the SMART EXECUTE OFF-LINE IMMEDIATE command shall cause that command to abort. In addition, the SMART READ DATA command shall clear bit 5 to zero in the Off-line data collection capabilities field. If this bit is supported by DEVICE CONFIGURATION SET, then this feature shall not be disabled by bit 1 of word 7.

Word 7 bit 12 is cleared to zero to disable support for the SMART Selective self-test. Subsequent attempts to start this test test via the SMART EXECUTE OFF-LINE IMMEDIATE command shall cause that command to abort. In addition, the SMART READ DATA command shall clear bit 6 to zero in the Off-line data collection capabilities field. If this bit is supported by DEVICE CONFIGURATION SET, then this feature shall not be disabled by bit 1 of word 7.

Word 7 bit 11 is cleared to zero to disable support for the Force Unit Access commands and has the effect of clearing bits 6 and 7 to zero in word 84 and word 87 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 10 is Reserved.

Word 7 bit 9 is cleared to zero to disable support for the Streaming feature set and has the effect of clearing bits 4, 9 and 10 to zero in word 84 and word 87 and clearing the value in words 95 to 99 and word 104 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 8 is cleared to zero to disable support for the 48-bit Addressing feature set and has the effect of clearing bit 10 to zero in word 83 and word 86 and clearing the value in words 100 to 103 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 7 is cleared to zero to disable support for the Host Protected Area feature set and has the effect of clearing bit 10 to zero in word 82 and word 85 and clearing bit 8 to zero in word 83 and word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If a Host Protected Area has been established by use of the SET MAX ADDRESS or SET MAX ADDRESS EXT command, these bits shall not be cleared to zero and the device shall return command aborted.

Word 7 bit 6 is cleared to zero to disable for the Automatic Acoustic Management feature set and has the effect of clearing bit 9 to zero in word 83 and word 94 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 5 is cleared to zero to disable support for the READ DMA QUEUED and WRITE DMA QUEUED commands and has the effect of clearing bit 1 to zero in word 83 and word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 4 is cleared to zero to disable support for the Power-up in Standby feature set and has the effect of clearing bits (6:5) to zero in word 83 and word 86 and clearing the value in word 94 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If Power-up in Standby has been enabled by a jumper, these bits shall not be cleared.

Word 7 bit 3 is cleared to zero to disable support for the Security feature set and has the effect of clearing bit 1 to zero in word 82 and word 85 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. These bits shall not be cleared if the Security feature set has been enabled.

Word 7 bit 2 is cleared to zero to disable support for the SMART error logging and has the effect of clearing bit 0 to zero in word 84 and word 87 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 1 is cleared to zero to disable support for the SMART self-test and has the effect of clearing bit 1 to zero in word 84 and word 87 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. Word 7 bit 1 disables support for the offline, short , extended self-tests (off-line and captive modes). If bit 12 or bit 13 of word 7 are not supported, Word 7 bit 1 may also disable support for conveyance self-test and selective self-test.

Word 7 bit 0 is cleared to zero to disable support for the SMART feature set and has the effect of clearing bit 0 to zero in word 82 and word 85 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If bits (2:1) of word 7 are not cleared to zero or if the SMART feature set has been enabled by use of the SMART ENABLE OPERATIONS command, these bits shall not be cleared and the device shall return command aborted.

6.10.5.8.7 Words 8 to 9: Reserved for serial ATA

These words are reserved for future serial ATA use.

6.10.5.8.8 Words 10 to 254: Reserved

6.10.5.8.9 Word 255: Integrity word

Bits (7:0) of this word shall contain the value A5h. Bits (15:8) of this word shall contain the data structure checksum. The data structure checksum shall be the two's complement of the sum of all byte in words 0 to 254 and the byte consisting of bits (7:0) of word 255. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all bytes is zero when the checksum is correct.

6.11 DEVICE RESET

6.11.1 Command code

08h

6.11.2 Feature set

General feature set

- Use prohibited when the PACKET Command feature set is not implemented.
- Mandatory when the PACKET Command feature set is implemented.

6.11.3 Protocol

Device reset (see Clause 11).

6.11.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	08h							

Device register
DEV shall specify the selected device.

6.11.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	Diagnostic results							
Sector Count	signature							
LBA Low	signature							
LBA Mid	signature							
LBA High	signature							
Device	0	0	0	DEV	0	0	0	0
Status	See Clause 11							

Error register
The diagnostic code as described in 6.13 is placed in this register.
Sector Count, LBA Low, LBA Mid, LBA High
Signature (see 5.15).
Device register
DEV shall indicate the selected device.
Status register
See Clause 11.

6.11.6 Error outputs

If supported, this command shall not end in an error condition. If this command is not supported and the device has the BSY bit or the DRQ bit set to one when the command is written, the results of this command are indeterminate. If this command is not supported and the device has the BSY bit and the DRQ bit cleared to zero when the command is written, the device shall respond with command aborted.

6.11.7 Prerequisites

This command shall be accepted when BSY or DRQ is set to one, DRDY is cleared to zero or DMARQ is asserted. This command shall be accepted when in Sleep mode.

6.11.8 Description

The DEVICE RESET command enables the host to reset an individual device without affecting the other device.

6.12 DOWNLOAD MICROCODE

6.12.1 Command code

92h

6.12.2 Feature set

General feature set
- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

6.12.3 Protocol

PIO data-out (see Clause 11).

6.12.4 Inputs

Bits (3:0) of the Device register shall always be cleared to zero. The LBA High and LBA Mid registers shall be cleared to zero. The LBA Low and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Sector count (low order)							
LBA Low	Sector count (high order)							
LBA Mid	00h							
LBA High	00h							
Device	obs	na	obs	DEV	0	0	0	0
Command	92h							

Device register

DEV shall specify the selected device.

6.12.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.12.6 Error outputs

The device shall return command aborted if the device does not support this command or did not accept the microcode data. The device shall return command aborted if subcommand code is not a supported value.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if the device does not support this command or did not accept the microcode data. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.12.7 Prerequisites

DRDY set to one.

6.12.8 Description

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the LBA Low register and the Sector Count register. The LBA Low register shall be used to extend the Sector Count register to create a 16-bit sector count value. The LBA Low register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the LBA Low register and the Sector Count register shall specify no data is to be transferred. This allows transfer sizes from 0 bytes to 33 553 920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Features register are:

- 01h - download is for immediate, temporary use.
- 07h - save downloaded code for immediate and future use.

Either or both values may be supported. All other values are reserved.

6.13 EXECUTE DEVICE DIAGNOSTIC

6.13.1 Command code

90h

6.13.2 Feature set

General feature set
– Mandatory for all devices.

6.13.3 Protocol

Device diagnostic (see Clause 11).

6.13.4 Inputs

Only the command code (90h). All other registers shall be ignored.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	na	na	na	na	na
Command	90h							

Device register
DEV shall be ignored.

6.13.5 Normal outputs

The diagnostic code written into the Error register is an 8-bit code. Table 15 defines these values. The values of the bits in the Error register are not as defined in Clause 5. Both Device 0 and Device 1 shall provide these register contents.

Register	7	6	5	4	3	2	1	0
Error	Diagnostic code							
Sector Count	Signature							
LBA Low	Signature							
LBA Mid	Signature							
LBA High	Signature							
Device	Signature							
Status	See Clause 11							

Error register
Diagnostic code.
Sector Count, LBA Low, LBA Mid, LBA High, Device registers
device signature (see 5.15).
Device register
DEV shall be cleared to zero.
Status register
See Clause 11.

Table 15 - Diagnostic codes

Code (see note 1)	Description
When this code is in the Device 0 Error register	
01h	Device 0 passed, Device 1 passed or not present
00h, 02h-7Fh	Device 0 failed, Device 1 passed or not present
81h	Device 0 passed, Device 1 failed
80h, 82h-FFh	Device 0 failed, Device 1 failed
When this code is in the Device 1 Error register	
01h	Device 1 passed (see note 2)
00h, 02h-7Fh	Device 1 failed (see note 2)
NOTE 1 Codes other than 01h and 81h may indicate additional information about the failure(s).	
NOTE 2 If Device 1 is not present, the host may see the information from Device 0 even though Device 1 is selected.	

6.13.6 Error outputs

Table 15 shows the error information that is returned as a diagnostic code in the Error register.

6.13.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

6.13.8 Description

This command shall cause the devices to perform the internal diagnostic tests. Both devices, if present, shall execute this command regardless of which device is selected.

If the host issues an EXECUTE DEVICE DIAGNOSTIC command while a device is in or going to a power management mode except Sleep, then the device shall execute the EXECUTE DEVICE DIAGNOSTIC sequence.

6.14 FLUSH CACHE

6.14.1 Command code

E7h

6.14.2 Feature set

General feature set

– Mandatory for all devices not implementing the PACKET Command feature set.
– Optional for devices implementing the PACKET Command feature set.

6.14.3 Protocol

Non-data (see Clause 11).

6.14.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	E7h							

Device register
DEV shall specify the selected device.

6.14.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.14.6 Error outputs

An unrecoverable error encountered during execution of writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE commands continue the process of flushing the cache starting with the first sector after the sector in error.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT may be set to one if the device is not able to complete the action requested by the command.
LBA Low, LBA Mid, LBA High, Device
shall be written with the address of the first unrecoverable error. If the device supports the 48-bit Address feature set and the error occurred in an address greater than FFFFFFFh, the value set in the LBA Low, LBA Mid, and LBA High registers shall be FFh and the value set in bits (3:0) of the Device register shall be Fh.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
--
ERR shall be set to one if an Error register bit is set to one.

6.14.7 Prerequisites

DRDY set to one.

6.14.8 Description

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

NOTE This command may take longer than 30 s to complete.

6.15 FLUSH CACHE EXT

6.15.1 Command code

EAh

6.15.2 Feature set

48-bit Address feature set
– Mandatory for all devices implementing the 48-bit Address feature.
– Prohibited for devices implementing the PACKET Command feature set.

6.15.3 Protocol

Non-data (see Clause 11).

6.15.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Reserved							
	Previous	Reserved							
LBA Low	Current	Reserved							
	Previous	Reserved							
LBA Mid	Current	Reserved							
	Previous	Reserved							
LBA High	Current	Reserved							
	Previous	Reserved							
Device		obs	na	obs	DEV	na			
Command		EAh							
NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Device register

DEV shall specify the selected device.

6.15.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.15.6 Error outputs

An unrecoverable error encountered while writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. Subsequent FLUSH CACHE EXT commands continue the process of flushing the cache starting with the first sector after the sector in error.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	ABRT	na	na
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

ABRT shall be set to one if the device is not able to complete the action requested by the command.

LBA Low

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB set to one.

LBA Mid

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB set to one.

LBA High

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB is set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

6.15.7 Prerequisites

DRDY set to one.

6.15.8 Description

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the madia.The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

NOTE This command may take longer than 30 s to complete.

6.16 GET MEDIA STATUS

6.16.1 Command code

DAh

6.16.2 Feature set

Removable Media Status Notification feature set

– Mandatory for devices implementing the Removable Media Status Notification feature set.

Removable Media feature set

– Optional for devices implementing the Removable Media feature set.

6.16.3 Protocol

Non-data (see Clause 11).

6.16.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	DAh							

Device register

DEV shall specify the selected device.

6.16.5 Normal outputs

Normal outputs are returned if Media Status Notification is disabled or if no bits are set to one in the Error register.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.16.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	WP	MC	na	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.

NM (No Media) shall be set to one if no media is present in the device. This bit shall be set to one for each execution of GET MEDIA STATUS until media is inserted into the device.

MCR (Media Change Request) shall be set to one if the eject button is pressed by the user and detected by the device. The device shall reset this bit after each execution of the GET MEDIA STATUS command and only set the bit again for subsequent eject button presses.

MC (Media Change) shall be set to one when the device detects media has been inserted. The device shall reset this bit after each execution of the GET MEDIA STATUS command and only set the bit again for subsequent media insertions.

WP (Write Protect) shall be set to one for each execution of GET MEDIA STATUS while the media is write protected.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.16.7 Prerequisites

DRDY set to one.

6.16.8 Description

This command returns media status bits WP, MC, MCR, and NM, as defined above. When Media Status Notification is disabled this command returns zeros in the WP, MC, MCR, and NM bits.

6.17 IDENTIFY DEVICE

6.17.1 Command code

ECh

6.17.2 Feature set

General feature set

- Mandatory for all devices.
- Devices implementing the PACKET Command feature set (See 6.17.5.2).

6.17.3 Protocol

PIO data-in (see Clause 11).

6.17.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	ECh							

Device register

DEV shall specify the selected device.

6.17.5 Outputs

6.17.5.1 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.17.5.2 Outputs for PACKET Command feature set devices

In response to this command, devices that implement the PACKET Command feature set shall post command aborted and place the PACKET Command feature set signature in the Command Block registers (see 5.15).

6.17.6 Error outputs

Devices not implementing the PACKET Command feature set shall not report an error.

6.17.7 Prerequisites

DRDY set to one.

6.17.8 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 16 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0 (see 3.3.10). For serial implementation see 3.3.11.

Some parameters are defined as 32-bit values (e.g., words 60 to 61). Such fields are transferred using two successive word transfers. The device shall first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits (31:16) of the value, shall be transferred on DD(15:0) respectively (See 3.3.10).

Some parameters are defined as a string of ACSII characters. Such fields are transferred as defined in 3.3.10.

Table 16 – IDENTIFY DEVICE data

Word	O/M	F/V	Description
0	M		General configuration bit-significant information:
		F	15 0 = ATA device
		X	14-8 Retired
		F	7 1 = removable media device
		X	6 Obsolete
		X	5-3 Retired
		V	2 Response incomplete
		X	1 Retired
		F	0 Reserved
1		X	Obsolete
2	O	V	Specific configuration
3		X	Obsolete
4-5		X	Retired
6		X	Obsolete
7-8	O	V	Reserved for assignment by the CompactFlash™ Association
9		X	Retired
10-19	M	F	Serial number (20 ASCII characters)
20-21		X	Retired
22		X	Obsolete
23-26	M	F	Firmware revision (8 ASCII characters)
27-46	M	F	Model number (40 ASCII characters)
47	M	F	15-8 80h
		F	7-0 00h = Reserved
		F	01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands
48		F	Reserved
49	M		Capabilities
		F	15-14 Reserved for the IDENTIFY PACKET DEVICE command.
		F	13 1 = Standby timer values as specified in this standard are supported
			0 = Standby timer values shall be managed by the device
		F	12 Reserved for the IDENTIFY PACKET DEVICE command.
		F	11 1 = IORDY supported
			0 = IORDY may be supported
		F	10 1 = IORDY may be disabled
		F	9 1 = LBA supported
		F	8 1 = DMA supported.
		X	7-0 Retired
50	M		Capabilities
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
		F	13-2 Reserved.
		X	1 Obsolete

Word	O/M	F/V	Description
		F	0 Shall be set to one to indicate a device specific Standby timer value minimum.
51-52		X	Obsolete
53	M	F	15-3 Reserved
		F	2 1 = the fields reported in word 88 are valid
			0 = the fields reported in word 88 are not valid
		F	1 1 = the fields reported in words 64 to 70 are valid
			0 = the fields reported in words 64 to 70 are not valid
		X	0 Obsolete
54-58		X	Obsolete
59	M	F	15-9 Reserved
		V	8 1 = Multiple sector setting is valid
		V	7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	M	F	Total number of user addressable sectors
62		X	Obsolete
63	M	F	15-11 Reserved
		V	10 1 = Multiword DMA mode 2 is selected
			0 = Multiword DMA mode 2 is not selected
		V	9 1 = Multiword DMA mode 1 is selected
			0 = Multiword DMA mode 1 is not selected
		V	8 1 = Multiword DMA mode 0 is selected
			0 = Multiword DMA mode 0 is not selected
		F	7-3 Reserved
		F	2 1 = Multiword DMA mode 2 and below are supported
		F	1 1 = Multiword DMA mode 1 and below are supported
		F	0 1 = Multiword DMA mode 0 is supported
64	M	F	15-8 Reserved
		F	7-0 PIO modes supported
65	M		Minimum Multiword DMA transfer cycle time per word
		F	15-0 Cycle time in nanoseconds
66	M		Manufacturer's recommended Multiword DMA transfer cycle time
		F	15-0 Cycle time in nanoseconds
67	M		Minimum PIO transfer cycle time without flow control
		F	15-0 Cycle time in nanoseconds
68	M		Minimum PIO transfer cycle time with IORDY flow control
		F	15-0 Cycle time in nanoseconds
69-70		F	Reserved (for future command overlap and queuing)
71-74		F	Reserved for the IDENTIFY PACKET DEVICE command.
75	O		Queue depth
		F	15-5 Reserved
		F	4-0 Maximum queue depth - 1
76-79		F	Reserved for Serial ATA

Word	O/M	F/V		Description
80	M			Major version number
				0000h or FFFFh = device does not report version
		F	15	Reserved
		F	14	Reserved for ATA/ATAPI-14
		F	13	Reserved for ATA/ATAPI-13
		F	12	Reserved for ATA/ATAPI-12
		F	11	Reserved for ATA/ATAPI-11
		F	10	Reserved for ATA/ATAPI-10
		F	9	Reserved for ATA/ATAPI-9
		F	8	Reserved for ATA/ATAPI-8
		F	7	1 = supports ATA/ATAPI-7
		F	6	1 = supports ATA/ATAPI-6
		F	5	1 = supports ATA/ATAPI-5
		F	4	1 = supports ATA/ATAPI-4
		F	3	Obsolete
		X	2	Obsolete
		X	1	Obsolete
		F	0	Reserved
81	M	F		Minor version number
				0000h or FFFFh = device does not report version
				0001h-FFFEh = See 6.17.41
82	M			Command set supported.
		X	15	Obsolete
		F	14	1 = NOP command supported
		F	13	1 = READ BUFFER command supported
		F	12	1 = WRITE BUFFER command supported
		X	11	Obsolete
		F	10	1 = Host Protected Area feature set supported
		F	9	1 = DEVICE RESET command supported
		F	8	1 = SERVICE interrupt supported
		F	7	1 = release interrupt supported
		F	6	1 = look-ahead supported
		F	5	1 = write cache supported
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3	1 = mandatory Power Management feature set supported
		F	2	1 = Removable Media feature set supported
		F	1	1 = Security Mode feature set supported
		F	0	1 = SMART feature set supported
83	M			Command sets supported.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13	1 = FLUSH CACHE EXT command supported
		F	12	1 = mandatory FLUSH CACHE command supported
		F	11	1 = Device Configuration Overlay feature set supported
		F	10	1 = 48-bit Address feature set supported

Word	O/M	F/V		Description
		F	9	1 = Automatic Acoustic Management feature set supported
		F	8	1 = SET MAX security extension supported
		F	7	See Address Offset Reserved Area Boot, INCITS TR27:2001
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		F	5	1 = Power-Up In Standby feature set supported
		F	4	1 = Removable Media Status Notification feature set supported
		F	3	1 = Advanced Power Management feature set supported
		F	2	1 = CFA feature set supported
		F	1	1 = READ/WRITE DMA QUEUED supported
		F	0	1 = DOWNLOAD MICROCODE command supported
84	M			Command set/feature supported extension.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
		F	12	Reserved for technical report
		F	11	Reserved for technical report
		F	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT
		F	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT
		F	8	1 = 64-bit World wide name supported
		F	7	1 = WRITE DMA QUEUED FUA EXT command supported
		F	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
		F	5	1 = General Purpose Logging feature set supported
		F	4	1 = Streaming feature set supported
		F	3	1 = Media Card Pass Through Command feature set supported
		F	2	1 = Media serial number supported
		F	1	1 = SMART self-test supported
		F	0	1 = SMART error logging supported
85	M			Command set/feature enabled.
		X	15	Obsolete
		F	14	1 = NOP command enabled
		F	13	1 = READ BUFFER command enabled
		F	12	1 = WRITE BUFFER command enabled
		X	11	Obsolete
		V	10	1 = Host Protected Area feature set enabled
		F	9	1 = DEVICE RESET command enabled
		V	8	1 = SERVICE interrupt enabled
		V	7	1 = release interrupt enabled
		V	6	1 = look-ahead enabled
		V	5	1 = write cache enabled
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3	1 = Power Management feature set enabled
		F	2	1 = Removable Media feature set enabled
		V	1	1 = Security Mode feature set enabled

Word	O/M	F/V		Description
		V	0	1 = SMART feature set enabled
86	M			Command set/feature enabled.
		F	15-14	Reserved
		F	13	1 = FLUSH CACHE EXT command supported
		F	12	1 = FLUSH CACHE command supported
		F	11	1 = Device Configuration Overlay supported
		F	10	1 = 48-bit Address features set supported
		V	9	1 = Automatic Acoustic Management feature set enabled
		F	8	1 = SET MAX security extension enabled by SET MAX SET PASSWORD
		F	7	See Address Offset Reserved Area Boot, INCITS TR27:2001
		F	6	1 = SET FEATURES subcommand required to spin-up after power-up
		V	5	1 = Power-Up In Standby feature set enabled
		V	4	1 = Removable Media Status Notification feature set enabled
		V	3	1 = Advanced Power Management feature set enabled
		F	2	1 = CFA feature set enabled
		F	1	1 = READ/WRITE DMA QUEUED command supported
		F	0	1 = DOWNLOAD MICROCODE command supported
87	M			Command set/feature default.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
		V	12	Reserved for technical report-
		V	11	Reserved for technical report-
		F	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT
		F	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT
		F	8	1 = 64 bit World wide name supported
		F	7	1 = WRITE DMA QUEUED FUA EXT command supported
		F	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
		F	5	1 = General Purpose Logging feature set supported
		V	4	1 = Valid CONFIGURE STREAM command has been executed
		V	3	1 = Media Card Pass Through Command feature set enabled
		V	2	1 = Media serial number is valid
		F	1	1 = SMART self-test supported
		F	0	1 = SMART error logging supported
88	O	F	15	Reserved
		V	14	1 = Ultra DMA mode 6 is selected
				0 = Ultra DMA mode 6 is not selected
		V	13	1 = Ultra DMA mode 5 is selected
				0 = Ultra DMA mode 5 is not selected
		V	12	1 = Ultra DMA mode 4 is selected
				0 = Ultra DMA mode 4 is not selected
		V	11	1 = Ultra DMA mode 3 is selected
				0 = Ultra DMA mode 3 is not selected
		V	10	1 = Ultra DMA mode 2 is selected

Word	O/M	F/V	Description
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
		F	7 Reserved
		F	6 1 = Ultra DMA mode 6 and below are supported
		F	5 1 = Ultra DMA mode 5 and below are supported
		F	4 1 = Ultra DMA mode 4 and below are supported
		F	3 1 = Ultra DMA mode 3 and below are supported
		F	2 1 = Ultra DMA mode 2 and below are supported
		F	1 1 = Ultra DMA mode 1 and below are supported
		F	0 1 = Ultra DMA mode 0 is supported
89	O	F	Time required for security erase unit completion
90	O	F	Time required for Enhanced security erase completion
91	O	V	Current advanced power management value
92	O	V	Master Password Revision Code
93	*		Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset.
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
		V	13 1 = device detected CBLID- above ViH
			0 = device detected CBLID- below ViL
			12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:
		F	12 Reserved.
		V	11 0 = Device 1 did not assert PDIAG-.
			1 = Device 1 asserted PDIAG-.
		V	10-9 These bits indicate how Device 1 determined the device number:
			00 = Reserved.
			01 = a jumper was used.
			10 = the CSEL signal was used.
			11 = some other method was used or the method is unknown.
			8 Shall be set to one.
			7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:
		F	7 Reserved.
		F	6 0 = Device 0 does not respond when Device 1 is selected.
			1 = Device 0 responds when Device 1 is selected.
		V	5 0 = Device 0 did not detect the assertion of DASP-.
			1 = Device 0 detected the assertion of DASP-.
		V	4 0 = Device 0 did not detect the assertion of PDIAG-.
			1 = Device 0 detected the assertion of PDIAG-.
		V	3 0 = Device 0 failed diagnostics.
			1 = Device 0 passed diagnostics.
		V	2-1 These bits indicate how Device 0 determined the device

Word	O/M	F/V	Description
			number:
			00 = Reserved.
			01 = a jumper was used.
			10 = the CSEL signal was used.
			11 = some other method was used or the method is unknown.
		F	0 Shall be set to one.
94	O	V	15-8 Vendor's recommended acoustic management value.
		V	7-0 Current automatic acoustic management value.
95		F	Stream Minimum Request Size
96		V	Streaming Transfer Time - DMA
97		V	Streaming Access Latency - DMA and PIO
98-99		F	Streaming Performance Granularity
100-103	O	V	Maximum user LBA for 48-bit Address feature set.
104	O	V	Streaming Transfer Time - PIO
105		F	Reserved
106	O		Physical sector size / Logical Sector Size
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = Device has multiple logical sectors per physical sector.
			12 1= Device Logical Sector Longer than 256 Words
		F	11-4 Reserved
		F	3-0 2X logical sectors per physical sector
107	O	F	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108	O	F	15-12 NAA (3:0) 11-0 IEEE OUI (23:12)
109	O	F	15-4 IEEE OUI (11:0) 3-0 Unique ID (35:32)
110	O	F	15-0 Unique ID (31:16)
111	O	F	15-0 Unique ID (15:0)
112-115	O	F	Reserved for world wide name extension to 128 bits
116	O	V	Reserved for technical report-
117-118	O	F	Words per Logical Sector
119-126		F	Reserved
127	O		Removable Media Status Notification feature set support
		F	15-2 Reserved
		F	1-0 00 = Removable Media Status Notification feature set not supported
			01 = Removable Media Status Notification feature supported
			10 = Reserved
			11 = Reserved
128	O		Security status
		F	15-9 Reserved
		V	8 Security level 0 = High, 1 = Maximum
		F	7-6 Reserved
		F	5 1 = Enhanced security erase supported
		V	4 1 = Security count expired

Word	O/M	F/V	Description
		V	3 1 = Security frozen
		V	2 1 = Security locked
		V	1 1 = Security enabled
		F	0 1 = Security supported
129-159		X	Vendor specific
160	O		CFA power mode 1
		F	15 Word 160 supported
		F	14 Reserved
		F	13 CFA power mode 1 is required for one or more commands implemented by the device
		V	12 CFA power mode 1 disabled
		F	11-0 Maximum current in ma
161-175		X	Reserved for assignment by the CompactFlash™ Association
176-205	O	V	Current media serial number
206-254		F	Reserved
255	M	X	Integrity word
			15-8 Checksum
			7-0 Signature

Key

O/M = Mandatory/optional requirement.

M = Support of the word is mandatory.

O = Support of the word is optional.

* = See 6.17.49.

F/V = Fixed/variable content

F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.

V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.

X = the content of the word may be fixed or variable.

(concluded)

6.17.9 Word 0: General configuration

Devices that conform to this standard shall clear bit 15 to zero.
If bit 7 is set to one, the device is a removable media device.
Bit 6 is obsolete.
If bit 2 is set to one it indicates that the content of the IDENTIFY DEVICE data is incomplete. This will occur if the device supports the Power-up in Standby feature set and required data is contained on the device media. In this case the content of at least word 0 and word 2 shall be valid.
Devices supporting the CFA feature set shall place the value 848Ah in word 0. In this case, the above definitions for the bits in word 0 are not valid.

6.17.10 Word 1: Obsolete

6.17.11 Word 2: Specific configuration.

Word 2 shall be set as follows:

Value	Description
37C8h	Device requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE data is incomplete (See 4.12).
738Ch	Device requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE data is complete (See 4.12).
8C73h	Device does not require SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE data is incomplete (See 4.12).
C837h	Device does not require SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE data is complete (See 4.12).
All other values	Reserved.

6.17.12 Word 3: Obsolete

6.17.13 Word 4 to 5: Retired.

6.17.14 Word 6: Obsolete

6.17.15 Words 7 to 8: Reserved for assignment by the CompactFlash™ Association

6.17.16 Word 9: Retired.

6.17.17 Words 10 to 19: Serial number

This field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (words 10 to 19) and Model number (words 27 to 46) shall be unique for a given manufacturer (see 3.3.10).

6.17.18 Word 20 to 21: Retired.

6.17.19 Word 22: Obsolete.

6.17.20 Word 23 to 26: Firmware revision

This field contains the firmware revision number of the device. The contents of this field is an ASCII character string of eight bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length (See 3.3.10).

6.17.21 Words 27 to 46: Model number

This field contains the model number of the device. The contents of this field is an ASCII character string of forty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (words 10 to 19) and Model number (words 27 to 46) shall be unique for a given manufacturer (see 3.3.10).

6.17.22 Word 47: READ/WRITE MULTIPLE support

Bits (7:0) of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands. If the serial interface is implemented, this field shall be set to 16 or less.

6.17.23 Word 48: Reserved

6.17.24 Word 50 to 49: Capabilities

Bits (15:14) of word 49 are reserved for use in the IDENTIFY PACKET DEVICE command data.
Bit 13 of word 49 is used to determine whether a device uses the Standby timer values as defined in this standard. Table 19 specifies the Standby timer values used by the device if bit 13 is set to one. If bit 13 is cleared to zero, the timer values shall be vendor specific.
Bit 12 of word 49 is reserved for use in the IDENTIFY PACKET DEVICE command data.
Bit 11 of word 49 indicates whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. All devices except CFA and PCMCIA devices shall support PIO mode 3 or higher, shall support IORDY, and shall set this bit to one. If the serial interface is implemented, this bit shall be set to one.
Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command. If the serial interface is implemented, this bit shall be set to one.
Bit 9 of word 49 shall be set to one to indicate that an LBA transition is supported.
Bits 8 of word 49 shall be set to one to indicate that DMA is supported. For devices not implementing the CompactFlash feature set this bit shall be set to one.
Bits (7:0) of word 49 are retired.
Bit 15 of word 50 shall be cleared to zero to indicate that the contents of word 50 are valid.
Bit 14 of word 50 shall be set to one to indicate that the contents of word 50 are valid.
Bits (13:2) of word 50 are reserved.
Bit 1 of word 50 is obsolete.
Bit 0 of word 50 set to one indicates that the device has a minimum Standby timer value that is device specific.

6.17.25 Words 51 to 52: Obsolete

6.17.26 Word 53: Field validity

Bit 0 of word 53 is obsolete.
If bit 1 of word 53 is set to one, the values reported in words 64 to 70 are valid. If this bit is cleared to zero, the values reported in words 64 to 70 are not valid. All devices except CFA and PCMCIA devices shall support PIO mode 3 or above and shall set bit 1 of word 53 to one and support the fields contained in words 64 to 70. If the serial interface is implemented, this bit shall be set to one.
If the device supports Ultra DMA and the values reported in word 88 are valid, then bit 2 of word 53 shall be set to one. If the device does not support Ultra DMA and the values reported in word 88 are not valid then this bit is cleared to zero. If the serial interface is implemented, this bit shall be set to one.

6.17.27 Word 58 to 54: Obsolete

6.17.28 Word 59: Multiple sector setting

If bit 8 is set to one, bits (7:0) reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. This field may default to the preferred value for the device (see 6.52).

6.17.29 Word 60 to 61: Total number of user addressable sectors

This field contains a value that is one greater than the maximum user accessable logical block address (See 4.2). The maximum value that shall be placed in this field is 0FFFFFFFh.

6.17.30 Word 62: Obsolete

6.17.31 Word 63: Multiword DMA transfer

6.17.31.1 General

Word 63 identifies the Multiword DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is enabled, then no Multiword DMA mode shall be enabled. If a Multiword DMA mode is enabled then no Ultra DMA mode shall be enabled.

6.17.31.2 Reserved

Bits (15:11) of word 63 are reserved.

6.17.31.3 Multiword DMA mode 2 selected

If bit 10 of word 63 is set to one, then Multiword DMA mode 2 is selected. If this bit is cleared to zero, then Multiword DMA mode 2 is not selected. If bit 9 is set to one or if bit 8 is set to one, then this bit shall be cleared to zero.

6.17.31.4 Multiword DMA mode 1 selected

If bit 9 of word 63 is set to one, then Multiword DMA mode 1 is selected. If this bit is cleared to zero then Multiword DMA mode 1 is not selected. If bit 10 is set to one or if bit 8 is set to one, then this bit shall be cleared to zero.

6.17.31.5 Multiword DMA mode 0 selected

If bit 8 of word 63 is set to one, then Multiword DMA mode 0 is selected. If this bit is cleared to zero then Multiword DMA mode 0 is not selected. If bit 10 is set to one or if bit 9 is set to one, then this bit shall be cleared to zero.

6.17.31.6 Reserved

Bits (7:3) of word 63 are reserved.

6.17.31.7 Multiword DMA mode 2 supported

If bit 2 of word 63 is set to one, then Multiword DMA modes 2 and below are supported. If this bit is cleared to zero, then Multiword DMA mode 2 is not supported. If Multiword DMA mode 2 is supported, then Multiword DMA modes 1 and 0 shall also be supported. If this bit is set to one, bits (1:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.31.8 Multiword DMA mode 1 supported

If bit 1 of word 63 is set to one, then Multiword DMA modes 1 and below are supported. If this bit is cleared to zero, then Multiword DMA mode 1 is not supported. If Multiword DMA mode 1 is supported, then Multiword DMA mode 0 shall also be supported. If this bit is set to one, bit 0 shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.31.9 Multiword DMA mode 0 supported

If bit 0 of word 63 is set to one, then Multiword DMA mode 0 is supported. If the serial interface is implemented, this bit shall be set to one.

6.17.32 Word 64: PIO transfer modes supported

Bits (7:0) of word 64 of the IDENTIFY DEVICE data is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting.
Of these bits, bits (7:2) are Reserved for future PIO modes. Bit 0, if set to one, indicates that the device supports PIO mode 3. All devices except CFA and PCMCIA devices shall support PIO mode 3 and shall set bit 0 to one. Bit 1, if set to one, indicates that the device supports PIO mode 4. If the serial interface is implemented, bits (1:0) shall be set to one.

6.17.33 Word 65: Minimum Multiword DMA transfer cycle time per word

Word 65 of the parameter information of the IDENTIFY DEVICE command data is defined as the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the device supports when performing Multiword DMA transfers on a per word basis. If the serial interface is implemented, this value shall be set to indicate 120 ns.
If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.
If bit 1 of word 53 is set to one because a device supports a field in words 64 to 70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

6.17.34 Word 66: Device recommended Multiword DMA cycle time

Word 66 of the parameter information of the IDENTIFY DEVICE command data is defined as the device recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. If the serial interface is implemented, this value shall be set to indicate 120 ns.
If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.
If bit 1 of word 53 is set to one because a device supports a field in words 64 to 70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

6.17.35 Word 67: Minimum PIO transfer cycle time without IORDY flow control

Word 67 of the parameter information of the IDENTIFY DEVICE command data is defined as the minimum PIO transfer without IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If the serial interface is implemented, this value shall be set to indicate 120 ns.
If this field is supported, bit 1 of word 53 shall be set to one.
Any device that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.
If bit 1 of word 53 is set to one because a device supports a field in words 64 to 70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

6.17.36 Word 68: Minimum PIO transfer cycle time with IORDY flow control

Word 68 of the parameter information of the IDENTIFY DEVICE command data is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data

transfers while utilizing IORDY flow control. If the serial interface is implemented, this value shall be set to indicate 120 ns.
If this field is supported, bit 1 of word 53 shall be set to one.
All devices except CFA and PCMCIA devices shall support PIO mode 3 and shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device. The maximum value reported in this field shall be 180 to indicate support for PIO mode 3 or above.
If bit 1 of word 53 is set to one because a device supports a field in words 64 to 70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

6.17.37 Words 69 to 74: Reserved

6.17.38 Word 75: Queue depth

Bits (4:0) of word 75 indicate the maximum queue depth supported by the device. The queue depth includes all commands for which command acceptance has occurred and command completion has not occurred. The value in this field equals (maximum queue depth −1), e.g., a value of zero indicates a queue depth of one, a value of 31 indicates a queue depth of 32. If bit 1 of word 83 is cleared to zero indicating that the device does not support READ/WRITE DMA QUEUED commands, the value in this field shall be zero. A device may support READ/WRITE DMA QUEUED commands to provide overlap only (i.e., queuing not supported), in this case, bit 1 of word 83 shall be set to one and the queue depth shall be set to zero. Support of this word is mandatory if the Queuing feature set is supported.

6.17.39 Words 76 to 79: Reserved for Serial ATA

6.17.40 Word 80: Major version number

If not 0000h or FFFFh, the device claims compliance with the major version(s) as indicated by bits (6:3) being set to one. Values other than 0000h and FFFFh are bit significant. Since ATA standards maintain downward compatibility, a device may set more than one bit.

6.17.41 Word 81: Minor version number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 shall be 0000h or FFFFh.
Table 17 defines the value that may optionally be reported in word 81 to indicate the revision of the standard that guided the implementation.

Table 17 - Minor version number

Value	Minor revision
0001h	Obsolete
0002h	Obsolete
0003h	Obsolete
0004h	Obsolete
0005h	Obsolete
0006h	Obsolete
0007h	Obsolete
0008h	Obsolete
0009h	Obsolete
000Ah	Obsolete
000Bh	Obsolete
000Ch	Obsolete
000Dh	ATA/ATAPI-4 X3T13 1153D revision 6
000Eh	ATA/ATAPI-4 T13 1153D revision 13
000Fh	ATA/ATAPI-4 X3T13 1153D revision 7
0010h	ATA/ATAPI-4 T13 1153D revision 18
0011h	ATA/ATAPI-4 T13 1153D revision 15
0012h	ATA/ATAPI-4 published, ANSI INCITS 317-1998
0013h	ATA/ATAPI-5 T13 1321D revision 3
0014h	ATA/ATAPI-4 T13 1153D revision 14
0015h	ATA/ATAPI-5 T13 1321D revision 1
0016h	ATA/ATAPI-5 published, ANSI INCITS 340-2000
0017h	ATA/ATAPI-4 T13 1153D revision 17
0018h	ATA/ATAPI-6 T13 1410D revision 0
0019h	ATA/ATAPI-6 T13 1410D revision 3a
001Ah	ATA/ATAPI-7 T13 1532D revision 1
001Bh	ATA/ATAPI-6 T13 1410D revision 2
001Ch	ATA/ATAPI-6 T13 1410D revision 1
001Dh	Reserved
001Eh	ATA/ATAPI-7 T13 1532D revision 0
001Fh	Reserved
0020h	Reserved
0021h	ATA/ATAPI-7 T13 1532D revision 4a
0022h	ATA/ATAPI-6 published, ANSI INCITS 361-2002
0023h-FFFFh	Reserved

6.17.42 Words 82 to 84: Features/command sets supported

Words 82 to 84 shall indicate features/command sets supported. If a defined bit is cleared to zero, the indicated features/command set is not supported. If bit 14 of word 83 is set to one and bit 15 of word 83 is cleared to zero, the contents of words 82 to 84 contain valid support information. If not, support information is not valid in these words. If bit 14 of word 84 is set to one and bit 15 of word 84 is cleared to zero, the contents of word 84 contains valid support information. If not, support information is not valid in this word.
If bit 0 of word 82 is set to one, the SMART feature set is supported.
If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
If bit 2 of word 82 is set to one, the Removable Media feature set is supported.

Bit 3 of word 82 shall be set to one indicating the mandatory Power Management feature set is supported.
Bit 4 of word 82 shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
If bit 5 of word 82 is set to one, write cache is supported.
If bit 6 of word 82 is set to one, look-ahead is supported.
If bit 7 of word 82 is set to one, release interrupt is supported.
If bit 8 of word 82 is set to one, SERVICE interrupt is supported.
If bit 9 of word 82 is set to one, the DEVICE RESET command is supported.
If bit 10 of word 82 is set to one, the Host Protected Area feature set is supported.
Bit 11 of word 82 is obsolete.
If bit 12 of word 82 is set to one, the device supports the WRITE BUFFER command.
If bit 13 of word 82 is set to one, the device supports the READ BUFFER command.
If bit 14 of word 82 is set to one, the device supports the NOP command.
Bit 15 of word 82 is obsolete.
If bit 0 of word 83 is set to one, the device supports the DOWNLOAD MICROCODE command.
If bit 1 of word 83 is set to one, the device supports the READ DMA QUEUED and WRITE DMA QUEUED commands.
If bit 2 of word 83 is set to one, the device supports the CFA feature set.
If bit 3 of word 83 is set to one, the device supports the Advanced Power Management feature set.
If bit 4 of word 83 is set to one, the device supports the Removable Media Status feature set.
If bit 5 of word 83 is set to one, the device supports the Power-Up In Standby feature set.
If bit 6 of word 83 is set to one, the device requires the SET FEATURES subcommand to spin-up after power-up if the Power-Up In Standby feature set is enabled (see 6.49.15).
Bit 7 is defined in Address Offset Reserved Area Boot, INCITS TR27:2001.
If bit 8 of word 83 is set to one, the device supports the SET MAX security extension.
If bit 9 of word 83 is set to one, the device supports the Automatic Acoustic Management feature set.
If bit 10 of word 83 is set to one, the 48-bit Address feature set is supported.
If bit 11 of word 83 is set to one, the device supports the Device Configuration Overlay feature set.
Bit 12 of word 83 shall be set to one indicating the device supports the mandatory FLUSH CACHE command.
If bit 13 of word 83 is set to one, the device supports the FLUSH CACHE EXT command.
If bit 0 of word 84 is set to one, the device supports SMART error logging.
If bit 1 of word 84 is set to one, the device supports SMART self-test.
If bit 2 of word 84 is set to one, the device supports the media serial number field words 176 to 205.
If bit 3 of word 84 is set to one, the device supports the Media Card Pass Through Command feature set.
If bit 4 of word 84 is set to one, the device supports the Streaming feature set.
If bit 5 of word 84 is set to one, the device supports the General Purpose Logging feature set.
If bit 6 of word 84 is set to one, the device supports the WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands.
If bit 7 of word 84 is set to one, the device supports the WRITE DMA QUEUED FUA EXT command.
If bit 8 of word 84 is set to one, the device supports a world wide name.
If bit 9 of word 84 is set to one, the device supports the URG bit for READ STREAM DMA EXT and READ STREAM EXT commands.

If bit 10 of word 84 is set to one, the device supports the URG bit for WRITE STREAM DMA EXT and WRITE STREAM EXTcommands.
Bit 11 of word 84 is reserved for technical report.
Bit 12 of word 84 is reserved for technical report.
If bit 13 of word 84 is set to one, the device supports IDLE IMMEDIATE with UNLOAD FEATURE.

6.17.43 Words 85 to 87: Features/command sets enabled

Words 85 to 87 shall indicate features/command sets enabled. If a defined bit is cleared to zero, the indicated features/command set is not enabled. If a supported features/command set is supported and cannot be disabled, it is defined as supported and the bit shall be set to one. If bit 14 of word 87 is set to one and bit 15 of word 87 is cleared to zero, the contents of words 85 to 87 contain valid information. If not, information is not valid in these words.
If bit 0 of word 85 is set to one, the SMART feature set has been enabled via the SMART ENABLE OPERATIONS command. If bit 0 of word 85 is cleared to zero, the SMART feature set has been disabled via the SMART DISABLE OPERATIONS command.
If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the SECURITY SET PASSWORD command. If bit 1 of word 85 is cleared to zero, the Security Mode feature set has been disabled via the SECURITY DISABLE PASSWORD command.
If bit 2 of word 85 is set to one, the Removable Media feature set is supported.

Bit 3 of word 85 shall be set to one indicating the mandatory Power Management feature set is supported.
Bit 4 of word 85 shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
If bit 5 of word 85 is set to one, write cache has been enabled via the SET FEATURES command (see 6.49.10). If bit 5 of word 85 is cleared to zero, write cache has been disabled via the SET FEATURES command.
If bit 6 of word 85 is set to one, look-ahead has been enabled via the SET FEATURES command (see 6.49.19). If bit 6 of word 85 is cleared to zero, look-ahead has been disabled via the SET FEATURES command.
If bit 7 of word 85 is set to one, release interrupt has been enabled via the SET FEATURES command (see 6.49.20). If bit 7 of word 85 is cleared to zero, release interrupt has been disabled via the SET FEATURES command.
If bit 8 of word 85 is set to one, SERVICE interrupt has been enabled via the SET FEATURES command (see 6.49.21). If bit 8 of word 85 is cleared to zero, SERVICE interrupt has been disabled via the SET FEATURES command.
If bit 9 of word 85 is set to one, the DEVICE RESET command is supported.
If bit 10 of word 85 is set to one, the Host Protected Area feature set is supported.
Bit 11 of word 85 is obsolete.
If bit 12 of word 85 is set to one, the device supports the WRITE BUFFER command.
If bit 13 of word 85 is set to one, the device supports the READ BUFFER command.
If bit 14 of word 85 is set to one, the device supports the NOP command.
Bit 15 of word 85 is obsolete.
If bit 0 of word 86 is set to one, the device supports the DOWNLOAD MICROCODE command.
If bit 1 of word 86 is set to one, the device supports the READ DMA QUEUED and WRITE DMA QUEUED commands.
If bit 2 of word 86 is set to one, the device supports the CFA feature set.
If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the SET FEATURES command. If bit 3 of word 86 is cleared to zero, the Advanced Power Management feature set has been disabled via the SET FEATURES command.
If bit 4 of word 86 is set to one, the Removable Media Status feature set has been enabled via the SET FEATURES command. If bit 4 of word 86 is cleared to zero, the Removable Media Status feature set has been disabled via the SET FEATURES command.
If bit 5 of word 86 is set to one, the Power-Up In Standby feature set has been enabled via the SET FEATURES command (see 6.49.13). If bit 5 of word 86 is cleared to zero, the Power-Up In Standby feature set has been disabled via the SET FEATURES command.
If bit 6 of word 86 is set to one, the device requires the SET FEATURES subcommand to spin-up after power-up (see 6.49.15).
Bit 7 of word 86 is defined in Address Offset Reserved Area Boot, INCITS TR-27:2001.

If bit 8 of word 86 is set to one, the device has had the SET MAX security extension enabled via a SET MAX SET PASSWORD command.
If bit 9 of word 86 is set to one, the device has had the Automatic Acoustic Management feature set enabled via a SET FEATURES command and the value in word 94 is valid.
If bit 10 of word 86 is set to one, the 48-bit Address feature set is supported.
If bit 11 of word 86 is set to one, the device supports the Device Configuration Overlay feature set.
Bit 12 of word 86 shall be set to oneindicating the device supports the mandatory FLUSH CACHE command.
If bit 13 of word 86 is set to one, the device supports the FLUSH CACHE EXT command.
If bit 0 of word 87 is set to one, the device supports SMART error logging.
If bit 1 of word 87 is set to one, the device supports SMART self-test.
If bit 2 of word 87 is set to one, the media serial number field in words 176 to 205 is valid. This bit shall be cleared to zero if the media does not contain a valid serial number or if no media is present.
If bit 3 of word 87 is set to one, the Media Card Pass Through feature set has been enabled.
If bit 4 of word 87 is set to one, a valid CONFIGURE STREAM command has been executed.
If bit 5 of word 87 is set to one, the device supports the General Purpose Logging feature set.
If bit 6 of word 87 is set to one, the device supports the WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands.
If bit 7 of word 87 is set to one, the device supports the WRITE DMA QUEUED FUA EXT command.
If bit 8 of word 87 is set to one, the device supports a world wide name.
If bit 9 of word 87 is set to one, the device supports the URG bit for READ STREAM DMA EXT and READ STREAM EXT commands.
If bit 10 of word 87 is set to one, the device supports the URG bit for WRITE STREAM DMA EXT and WRITE STREAM EXT commands.
Bit 11 of word 87 is reserved for technical report.
Bit 12 of word 87 is reserved for technical report.
If bit 13 of word 87 is set to one, the device supports IDLE IMMEDIATE with UNLOAD FEATURE.

6.17.44 Word 88: Ultra DMA modes

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.

6.17.44.1 Reserved

Bit (15) of word 88 is reserved.

6.17.44.2 Ultra DMA mode 6 selected

If bit 14 of word 88 is set to one, then Ultra DMA mode 6 is selected. If this bit is cleared to zero, then Ultra DMA mode 6 is not selected. If bit 13 or bit 12 or bit 11 or bit 10 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

6.17.44.3 Ultra DMA mode 5 selected

If bit 13 of word 88 is set to one, then Ultra DMA mode 5 is selected. If this bit is cleared to zero, then Ultra DMA mode 5 is not selected. If bit 12 or bit 11 or bit 10 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

6.17.44.4 Ultra DMA mode 4 selected

If bit 12 of word 88 is set to one, then Ultra DMA mode 4 is selected. If this bit is cleared to zero, then Ultra DMA mode 4 is not selected. If bit 13 or 11 or bit 10 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

6.17.44.5 Ultra DMA mode 3 selected

If bit 11 of word 88 is set to one, then Ultra DMA mode 3 is selected. If this bit is cleared to zero, then Ultra DMA mode 3 is not selected. If bit 13 or 12 or bit 10 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

6.17.44.6 Ultra DMA mode 2 selected

If bit 10 of word 88 is set to one, then Ultra DMA mode 2 is selected. If this bit is cleared to zero, then Ultra DMA mode 2 is not selected. If bit 13 or 12 or bit 11 or bit 9 or bit 8 is set to one, then this bit shall be cleared to zero.

6.17.44.7 Ultra DMA mode 1 selected

If bit 9 of word 88 is set to one, then Ultra DMA mode 1 is selected. If this bit is cleared to zero then Ultra DMA mode 1 is not selected. If bit 13 or 12 or bit 11 or bit 10 or bit 8 is set to one, then this bit shall be cleared to zero.

6.17.44.8 Ultra DMA mode 0 selected

If bit 8 of word 88 is set to one, then Ultra DMA mode 0 is selected. If this bit is cleared to zero then Ultra DMA mode 0 is not selected. If bit 13 or 12 or bit 11 or bit 10 or bit 9 is set to one, then this bit shall be cleared to zero.

6.17.44.9 Reserved

Bit (7) of word 88 are reserved.

6.17.44.10 Ultra DMA mode 6 supported

If bit 6 of word 88 is set to one, then Ultra DMA modes 6 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 6 is not supported. If Ultra DMA mode 6 is supported, then Ultra DMA modes 5, 4, 3, 2, 1 and 0 shall also be supported. If this bit is set to one, then bits (5:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.44.11 Ultra DMA mode 5 supported

If bit 5 of word 88 is set to one, then Ultra DMA modes 5 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 5 is not supported. If Ultra DMA mode 5 is supported, then Ultra DMA modes 4, 3, 2, 1 and 0 shall also be supported. If this bit is set to one, then bits (4:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.44.12 Ultra DMA mode 4 supported

If bit 4 of word 88 is set to one, then Ultra DMA modes 4 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 4 is not supported. If Ultra DMA mode 4 is supported, then Ultra DMA modes 3, 2, 1 and 0 shall also be supported. If this bit is set to one, then bits (3:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.44.13 Ultra DMA mode 3 supported

If bit 3 of word 88 is set to one, then Ultra DMA modes 3 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 3 is not supported. If Ultra DMA mode 3 is supported, then Ultra DMA modes 2, 1 and 0 shall also be supported. If this bit is set to one, then bits (2:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.44.14 Ultra DMA mode 2 supported

If bit 2 of word 88 is set to one, then Ultra DMA modes 2 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 2 is not supported. If Ultra DMA mode 2 is supported,

then Ultra DMA modes 1 and 0 shall also be supported. If this bit is set to one, bits (1:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.44.15 Ultra DMA mode 1 supported

If bit 1 of word 88 is set to one, then Ultra DMA modes 1 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 1 is not supported. If Ultra DMA mode 1 is supported, then Ultra DMA mode 0 shall also be supported. If this bit is set to one, bit 0 shall be set to one. If the serial interface is implemented, this bit shall be set to one.

6.17.44.16 Ultra DMA mode 0 supported

If bit 0 of word 88 is set to one, then Ultra DMA mode 0 is supported. If this bit is cleared to zero, then Ultra DMA is not supported. If the serial interface is implemented, this bit shall be set to one.

6.17.45 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete. Support of this word is mandatory if the Security feature set is supported.

Value	Time
0	Value not specified
1 to 254	(Value×2) min
255	>508 min

6.17.46 Word 90: Time required for enhanced security erase unit completion

Word 90 specifies the time required for the ENHANCED SECURITY ERASE UNIT command to complete. Support of this word is mandatory if support of the Enhanced Security feature set is supported.

Value	Time
0	Value not specified
1 to 254	(Value×2) min
255	>508 min

6.17.47 Word 91: Advanced power management level value

Bits (7:0) of word 91 contain the current Advanced Power Management level setting. Support of this word is mandatory if advanced power management is supported.

6.17.48 Word 92: Master Password Revision Code

Word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision is not supported. Support of this word is mandatory if the Security feature set is supported.

6.17.49 Word 93: Hardware configuration test results

If bit 14 of word 93 is set to one and bit 15 of word 93 is cleared to zero, the content of word 93 contains valid information. During hardware reset execution, Device 0 shall clear bits (12:8) of this word to zero and shall set bits (7:0) of the word as indicated to show the result of the hardware reset execution. During hardware reset execution, Device 1 shall clear bits (7:0) of this word to zero and shall set bits (12:8) as indicated to show the result of the hardware reset execution. Support of bits (15:13) are mandatory. Support of bits (12:0) is optional.
Bit 13 shall be set or cleared by the selected device to indicate whether the device detected CBLID− above V_{IH} or below V_{IL} at any time during execution of each IDENTIFY DEVICE routine after receiving the command from the host but before returning data to the host. This test may be repeated as desired by the device during command execution (see ISO/IEC 24739-2, Annex A).
If the serial interface is implemented, word 93 shall be set to the value 0000h.

6.17.50 Word 94: Current automatic acoustic management value

Bits (15:8) contain the device vendor's recommended acoustic management level (see Table 44 for an enumeration of all of the possible acoustic management levels). If the host desires the drive to perform with highest performance, it should set the automatic acoustic management level to Feh. If the OEM host desires the vendor's recommended acoustic management level as defined by the device's vendor, the host should set the automatic acoustic management level to the value returned to the host in these 8 bits of the IDENTIFY DEVICE data. The use of this setting may not provide the lowest acoustics, or the best tradeoff of acoustics and performance, in all configurations. Support of this word is mandatory if the Acoustic Management feature set is supported.
Bits (7:0) contain the current automatic acoustic management level. If the Automatic Acoustic Management feature set is supported by the device, but the level has not been set by the host, this byte shall contain the drive's default setting. If the Automatic Acoustic Management feature set is not supported by the device, the value of this byte shall be zero.

6.17.51 Word 95: Stream Minimum Request Size

Number of sectors that provides optimum performance in a streaming environment. This number shall be a power of two, with a minimum of eight sectors (4096 bytes). The starting LBA value for each streaming command should be evenly divisible by this request size.

6.17.52 Word 96: Streaming Transfer Time – DMA

Word 96 defines the Streaming Transfer Time for DMA mode. The worst-case sustainable transfer time per sector for the device is calculated as follows:

Streaming Transfer Time = (word 96) × (words 98 to 99) / 65 536)

The content of IDENTIFY DEVICE data word 96 may be affected by the host issuing a SET FEATURES subcommand 43h (Typical Host Interface Sector Time for DMA mode). Because of this effect, an IDENTIFY DEVICE command shall be issued after a SET FEATURES command that may affect these words. If the Streaming Feature Set is not supported by the device, the content of word 96 shall be zero.

6.17.53 Word 97: Streaming Access Latency – DMA and PIO

Word 97 defines the Streaming Access Latency for DMA and PIO mode. The worst-case access latency of the device for a streaming command is calculated as follows:

Access Latency = (word 97) × (words 98 to 99) / 256

The content of IDENTIFY DEVICE data word 97 may be affected by the host issuing a SET FEATURES subcommand 42h or C2h (Automatic Acoustic Management). Because of this effect, an IDENTIFY DEVICE command shall be issued after a SET FEATURES command that may affect these words. If the Streaming Feature Set is not supported by the device, the content of word 97 shall be zero.

6.17.54 Words 98 to 99: Streaming Performance Granularity

These words define the fixed unit of time that is used in IDENTIFY DEVICE data words 96 to 97 and 104, and SET FEATURES subcommand 43h, and in the Streaming Performance Parameters log, which is accessed by use of the READ LOG EXT command, and in the Command Completion Time Limit that is passed in streaming commands. The unit of time for this parameter shall be in microseconds, e.g., a value of 10 000 indicates 10 ms. If yy was returned by the drive for this parameter, then:

1) the Command Completion Time Limit in the Features register for a streaming command shall be yy µs.
2) the Streaming Transfer Time shall be ((word 96) × (yy/65 536)) µs, ((word 104) × (yy/65536)) µs, or ((a Sector Time array entriy in the Streaming Performance Parameters log) × (yy/65 536)) µs.
3) the Streaming Access Latency shall be ((word 97) × (yy/256)) µs, or ((an Access Time array entries in the Streaming Performance Parameters log) × (yy/256)) µs.
4) taking these units into account, the host may calculate the estimated time for a streaming command of size S sectors as ((word 96 × S / 65536) + (word 97 / 256)) × yy µs for DMA mode.
5) taking these units into account, the host may calculate the estimated time for a streaming command of size S sectors as ((word 104 × S / 65 536) + (word 97 / 256)) × yy µs for PIO mode.

The value of the Streaming Performance Granularity is vendor specific and fixed for a device.

6.17.55 Words 100 to 103: Maximum user LBA for 48-bit Address feature set

Words 100 to 103 contain a value that is one greater than the maximum LBA in user accessable space when the 48-bit Addressing feature set is supported. The maximum value that shall be placed in this field is 0000FFFFFFFFFFFFh. Support of these words is mandatory if the 48-bit Address feature set is supported.

6.17.56 Word 104: Streaming Transfer Time – PIO

The content of IDENTIFY DEVICE data word 104 may be affected by the host issuing a SET Word 104 defines the Streaming Transfer Time for PIO mode. The worst-case sustainable transfer time per sector for the device is calculated as follows:

Streaming Transfer Time = (word 104) × (words 98 to 99) / 65 536)

FEATURES subcommand 43h (Typical Host Interface Sector Time for PIO mode). Because of this effect, an IDENTIFY DEVICE command shall be issued after a SET FEATURES command that may affect these words. If the Streaming Feature Set is not supported by the device, the content of word 104 shall be zero.

6.17.57 Word 106: Physical sector size / Logical Sector Size

If bit 14 of word 106 is set to one and bit 15 of word 106 is cleared to zero, the contents of word 106 contain valid information. If not, information is not valid in this word.
Bit 13 of word 106 shall be set to one to indicate that the device has more than one logical sector per physical sector.
Bit 12 of word 106 shall be set to 1 to indicate that the device has been formatted with a logical sector size larger than 256 words. Bit 12 of word 106 shall be cleared to 0 to indicate that words 117 to 118 are invalid and that the logical sector size is 256 words.
Bits (11:4) of word 106 are reserved.
Bits (3:0) of word 106 indicate the size of the device physical sectors in power of two logical sectors.
Examples:

Bits (3:0): 0 = 2^0 = 1 logical sector per physical sector
Bits (3:0): 1 = 2^1 = 2 logical sector per physical sector
Bits (3:0): 2 = 2^2 = 4 logical sector per physical sector
Bits (3:0): 3 = 2^3 = 8 logical sector per physical sector

6.17.58 Word 107: Inter-seek delay for ISO 7779 standard acoustic testing

Word 107 is defined as the manufacturer's recommended time delay between seeks during ISO 7779 standard acoustic testing in microseconds (ISO 7779 value t_D). (See ISO 7779:1999 (E) Clause C.9, Equipment Category: Disk units and storage subsystems.)

6.17.59 Words 108 to 111: World wide name

Words 108 to 111 shall contain the optional value of the world wide name (WWN) for the device.
Word 108 bits 15-12 shall contain 5h, indicating that the naming authority is IEEE. All other values are reserved.
Words 108 bits 11-0 and word 109 bits 15-4 shall contain the Organization Unique Identifier (OUI) for the device manufacturer. The OUI shall be assigned by the IEEE/RAC as specified by ISO/IEC 13213:1994 (see 3.1.80).
The identifier may be obtained from:

Institute of Electrical and Electronic Engineers, Inc.
Registration Authority Committee
445 Hoes Lane
Piscataway, NJ 08855-1331

Word 109 bits 3-0, word 110, and word 111 shall contain a value assigned by the vendor that is unique for the OUI domain.

6.17.60 Words 112 to 115: Reserved for a 128-bit world wide name

6.17.61 Word 116: Reserved for technical report

6.17.62 Words 117 to 118: Logical Sector Size

Words 117 to 118 indicate the size of device logical sectors in words. The value of words 117 to 118 shall be equal to or greater than 256. The value in words 117 to 118 shall be valid when word 106 bit 12 is set to 1. All logical sectors on a device shall have a length equal to the value in words 117 to 118.

6.17.63 Words 119 to 126: Reserved

6.17.64 Word 127: Removable Media Status Notification feature set support

If bit 0 of word 127 is set to one and bit 1 of word 127 is cleared to zero, the device supports the Removable Media Status Notification feature set. Bits (15:2) shall be cleared to zero. Support of this word is mandatory if the Removable Media Status Notification feature set is supported.

6.17.65 Word 128: Security status

Support of this word is mandatory if the Security feature set is supported.
Bit 8 of word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.
Bit 5 of word 128 indicates the Enhanced security erase unit feature is supported. If bit 5 is set to one, the Enhanced security erase unit feature set is supported.
Bit 4 of word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hardware reset.
Bit 3 of word 128 indicates security frozen. If bit 3 is set to one, the security is frozen.
Bit 2 of word 128 indicates security locked. If bit 2 is set to one, the security is locked.
Bit 1 of word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.
Bit 0 of word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

6.17.66 Words 129 to 159: Vendor specific

6.17.67 Word 160: CFA power mode

Word 160 indicates the presence and status of a CFA feature set device that supports CFA Power Mode 1. Support of this word is mandatory if CFA Power Mode 1 is supported.
If bit 13 of word 160 is set to one then the device shall be in CFA Power Mode 1 to perform one or more commands implemented by the device.
If bit 12 of word 160 is set to one the device is in CFA Power Mode 0 (see 6.49.14).
Bits (11:0) indicate the maximum average RMS current in Milliamperes required during 3.3V or 5V device operation in CFA Power Mode 1.

6.17.68 Words 161 to 175: Reserved for assignment by the CompactFlash™ Association

6.17.69 Words 176 to 205: Current media serial number

Words 176 to 205 contain the current media serial number. Serial numbers shall consist of 60 bytes. The first 40 bytes shall indicate the media serial number and the remaining 20 bytes shall indicate the media manufacturer.
For removable ATA devices (e.g., flash media with native ATA interfaces) that do not support removable media, the first 20 words of this field shall be the same as words 27 to 46 of the IDENTIFY DEVICE data and the next ten words shall be the same as words 10 to 19 of the IDENTIFY DEVICE response.

6.17.70 Words 206 to 254: Reserved

6.17.71 Word 255: Integrity word

The use of this word is optional. If bits (7:0) of this word contain the signature A5h, bits (15:8) contain the data structure checksum. The data structure checksum is the two's complement of the sum of all bytes in words 0 to 254 and the byte consisting of bits (7:0) in word 255. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct.

6.18 IDENTIFY PACKET DEVICE

6.18.1 Command code

A1h

6.18.2 Feature set

PACKET Command feature set

- Use prohibited for devices not implementing the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.

6.18.3 Protocol

PIO data-in (see Clause 11).

6.18.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	A1h							

Device register
DEV shall specify the selected device.

6.18.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.18.6 Error outputs

The device shall return command aborted if the device does not implement this command, otherwise, the device shall not report an error.

6.18.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

6.18.8 Description

The IDENTIFY PACKET DEVICE command enables the host to receive parameter information from a device that implements the PACKET Command feature set.
Some devices may have to read the media in order to complete this command.
When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 18 defines the arrangement and meanings of the parameter words in the buffer. All reserved bits or words shall be zero.
References to parallel implementation bus signals (e.g. DMACK, DMARQ, etc) apply only to parallel implementations. See ISO/IEC 24739-3 for additional information on serial protocol. Some register bits (e.g. nIEN, SRST, etc.) have different requirements in the serial implementation (see ISO/IEC 24739-3).
Some parameters are defined as a group of bits. A word that is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).
Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0 (see 3.3.10).
Some parameters are defined as 32-bit values (e.g., words 60 to 61). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits (15:0) of the value, on bits DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits (31:16) of the value, shall be transferred on DD(15:0) respectively (see 3.3.10).
Some parameters are defined as a string of ASCII characters (see 3.3.10).

Table 18 – IDENTIFY PACKET DEVICE data

Word	O/M	F/V	Description
0	M		General configuration bit-significant information:
		F	15-14 10 = ATAPI device
		F	11 = Reserved
		F	13 Reserved
		F	12-8 Field indicates command packet set used by device
		F	7 1 = removable media device
		F	6-5 00 = Device shall set DRQ to one within 3 ms of receiving PACKET command. 01 = Obsolete. 10 = Device shall set DRQ to one within 50 µs of receiving PACKET command. 11 = Reserved
		F	4-3 Reserved
		V	2 Incomplete response
		F	1-0 00 = 12 byte command packet 01 = 16 byte command packet 1x = Reserved
1		F	Reserved
2		V	Unique configuration
3-9		F	Reserved
10-19	M	F	Serial number (20 ASCII characters)
20-22		F	Reserved
23-26	M	F	Firmware revision (8 ASCII characters)
27-46	M	F	Model number (40 ASCII characters)
47-48		F	Reserved
49	M		Capabilities
		F	15 1 = interleaved DMA supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	14 1 = command queuing supported
		F	13 1 = overlap operation supported
		F	12 1 = ATA software reset required (Obsolete)
		F	11 1 = IORDY supported
		F	10 1 = IORDY may be disabled
		F	9 Shall be set to one.
		F	8 1 = DMA supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0
		X	7-0 Vendor specific
50	O		Capabilities
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
		F	13-2 Reserved
		X	1 Obsolete
		F	0 Shall be set to one to indicate a device specific Standby timer value minimum.
51-52		X	Obsolete

Word	O/M	F/V	Description	
53	M	F	15-3	Reserved
		F	2	1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid
		F	1	1 = the fields reported in words 64 to 70 are valid 0 = the fields reported in words 64 to 70 are not valid
		X	0	Obsolete
54-61		F	Reserved	
62	M	F	15	1 = DMADIR bit in the Packet command is required for DMA transfers 0 = DMADIR bit in Packet command is not required for DMA transfers.
		F	14-11	Reserved
		F	10	1 = DMA is supported
		F	9	1 = Multiword DMA mode 2 is supported
		F	8	1 = Multiword DMA mode 1 is supported
		F	7	1 = Multiword DMA mode 0 is supported
		F	6	1 = Ultra DMA mode 6 and below are supported
		F	5	1 = Ultra DMA mode 5 and below are supported
		F	4	1 = Ultra DMA mode 4 and below are supported
		F	3	1 = Ultra DMA mode 3 and below are supported
		F	2	1 = Ultra DMA mode 2 and below are supported
		F	1	1 = Ultra DMA mode 1 and below are supported
		F	0	1 = Ultra DMA mode 0 is supported
63	M	F	15-11	Reserved
		V	10	1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected
		V	9	1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected
		V	8	1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected
		F	7-3	Reserved
		F	2	1 = Multiword DMA mode 2 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	1	1 = Multiword DMA mode 1 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	0	1 = Multiword DMA mode 0 is supported Multiword DMA mode selected Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
64	M	F	15-8	Reserved
		F	7-0	PIO transfer modes supported
65	M		Minimum Multiword DMA transfer cycle time per word	
		F	15-0	Cycle time in nanoseconds
66	M		Manufacturer's recommended Multiword DMA transfer cycle time	
		F	15-0	Cycle time in nanoseconds
67	M		Minimum PIO transfer cycle time without flow control	
		F	15-0	Cycle time in nanoseconds
68	M		Minimum PIO transfer cycle time with IORDY flow control	
		F	15-0	Cycle time in nanoseconds

Word	O/M	F/V	Description
69-70		F	Reserved (for future command overlap and queuing)
71	O	F	Typical time in ns from receipt of PACKET command to bus release.
72	O	F	Typical time in ns from receipt of SERVICE command to BSY cleared to zero
73-74		F	Reserved
75	O		Queue depth
		F	15-5 Reserved
		F	4-0 Maximum queue depth supported - 1
76-79		R	Reserved for Serial ATA
80	M		Major version number 0000h or FFFFh = device does not report version
		F	15 Reserved
		F	14 Reserved for ATA/ATAPI-14
		F	13 Reserved for ATA/ATAPI-13
		F	12 Reserved for ATA/ATAPI-12
		F	11 Reserved for ATA/ATAPI-11
		F	10 Reserved for ATA/ATAPI-10
		F	9 Reserved for ATA/ATAPI-9
		F	8 Reserved for ATA/ATAPI-8
		F	7 1 = Supports ATA/ATAPI-7
		F	6 1 = supports ATA/ATAPI-6
		F	5 1 = supports ATA/ATAPI-5
		F	4 1 = supports ATA/ATAPI-4
		F	3 Obsolete
		X	2 Obsolete
		X	1 Obsolete
		F	0 Reserved
81	M		Minor version number 0000h or FFFFh=device does not report version 0001h-FFFEh=See 6.17.41

Word	O/M	F/V		Description
82	M			Command set supported. If words 82 to 83 = 0000h or FFFFh command set notification not supported.
		X	15	Obsolete
		F	14	1 = NOP command supported
		F	13	1 = READ BUFFER command supported
		F	12	1 = WRITE BUFFER command supported
		X	11	Obsolete
		F	10	1 = Host Protected Area feature set supported
		F	9	1 = DEVICE RESET command supported
		F	8	1 = SERVICE interrupt supported
		F	7	1 = release interrupt supported
		F	6	1 = look-ahead supported
		F	5	1 = write cache supported
		F	4	Shall be set to one indicating the PACKET Command feature set is supported.
		F	3	1 = Power Management feature set supported
		F	2	1 = Removable Media feature set supported
		F	1	1 = Security Mode feature set supported
		F	0	1 = SMART feature set supported
83	M			Command sets supported. If words 82 to 83 = 0000h or FFFFh command set notification not supported.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13	Reserved
		F	12	1 = FLUSH CACHE command supported
		F	11	1 = Device Configuration Overlay feature set supported
		F	10	Reserved
		F	9	1 = AUTOMATIC Acoustic Management feature set supported
		F	8	1 = SET MAX security extension supported
		F	7	See Address Offset Reserved Area Boot, INCITS TR27:2001
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		F	5	1 = Power-Up In Standby feature set supported
		F	4	1 = Removable Media Status Notification feature set supported
		F	3-1	Reserved
		F	0	1 = DOWNLOAD MICROCODE command supported
84	M			Command set/feature supported extension. If words 82, 83, and 84 = 0000h or FFFFh command set notification extension is not supported.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13-0	Reserved

Word	O/M	F/V		Description
85	M			Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported.
		X	15	Obsolete
		F	14	1 = NOP command enabled
		F	13	1 = READ BUFFER command enabled
		F	12	1 = WRITE BUFFER command enabled
		X	11	Obsolete
		V	10	1 = Host Protected Area feature set enabled
		F	9	1 = DEVICE RESET command enabled
		V	8	1 = SERVICE interrupt enabled
		V	7	1 = release interrupt enabled
		V	6	1 = look-ahead enabled
		V	5	1 = write cache enabled
		F	4	Shall be set to one indicating the PACKET Command feature set is supported.
		F	3	1 = Power Management feature set enabled
		V	2	1 = Removable Media feature set enabled
		V	1	1 = Security Mode feature set enabled
		V	0	1 = SMART feature set enabled
86	M			Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported.
		F	15-13	Reserved
		V	12	1 = FLUSH CACHE command supported
		F	11	1 = Device Configuration Overlay feature set supported
		F	10	Reserved
		V	9	1 = Automatic Acoustic Management feature set enabled
		V	8	1 = SET MAX security extension enabled by a SET MAX SET PASSWORD
		V	7	See Address Offset Reserved Area Boot, INCITS TR27:2001
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		V	5	1 = Power-Up In Standby feature set enabled
		V	4	1 = Removable Media Status Notification feature set enabled via the SET FEATURES command.
		F	3-1	Reserved
		F	0	1 = DOWNLOAD MICROCODE command enabled
87	M			Command set/feature default. If words 85, 86, and 87 = 0000h or FFFFh command set default notification is not supported.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13-0	Reserved

Word	O/M	F/V	Description
88	M	F	15 Reserved
			14 1 = Ultra DMA mode 6 is selected
			0 = Ultra DMA mode 6 is not selected
		V	13 1 = Ultra DMA mode 5 is selected
			0 = Ultra DMA mode 5 is not selected
		V	12 1 = Ultra DMA mode 4 is selected
			0 = Ultra DMA mode 4 is not selected
		V	11 1 = Ultra DMA mode 3 is selected
			0 = Ultra DMA mode 3 is not selected
		V	10 1 = Ultra DMA mode 2 is selected
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
		F	7 Reserved
		F	6 1 = Ultra DMA mode 6 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	5 1 = Ultra DMA mode 5 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	4 1 = Ultra DMA mode 4 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	3 1 = Ultra DMA mode 3 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	2 1 = Ultra DMA mode 2 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	1 1 = Ultra DMA mode 1 and below are supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
		F	0 1 = Ultra DMA mode 0 is supported Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
89-92		F	Reserved

Word	O/M	F/V	Description
93	*		Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset.
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
		V	13 1 = device detected CBLID- above V_{iH}
			0 = device detected CBLID- below V_{iL}
			12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:
		F	12 Reserved.
		V	11 0 = Device 1 did not assert PDIAG−.
			1 = Device 1 asserted PDIAG−.
		V	10-9 These bits indicate how Device 1 determined the device number:
			00 = Reserved.
			01 = a jumper was used.
			10 = the CSEL signal was used.
			11 = some other method was used or the method is unknown.
		F	8 Shall be set to one.
			7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:
		F	7 Reserved.
		F	6 0 = Device 0 does not respond when Device 1 is selected.
			1 = Device 0 responds when Device 1 is selected.
		V	5 0 = Device 0 did not detect the assertion of DASP−.
			1 = Device 0 detected the assertion of DASP−.
		V	4 0 = Device 0 did not detect the assertion of PDIAG−.
			1 = Device 0 detected the assertion of PDIAG−.
		V	3 0 = Device 0 failed diagnostics.
			1 = Device 0 passed diagnostics.
			2-1 These bits indicate how Device 0 determined the device number:
		F	00 = Reserved.
		V	01 = a jumper was used.
		V	10 = the CSEL signal was used.
		V	11 = some other method was used or the method is unknown.
		F	0 Shall be set to one.
94	O	V	15-8 Vendor's recommended acoustic management value.
		V	7-0 Current automatic acoustic mamagement value.
95-124		F	Reserved
125	M	F	ATAPI byte count = 0 behavior
126		X	Obsolete
127	O		Removable Media Status Notification feature set support
		F	15-2 Reserved
		F	1-0 00 = Removable Media Status Notification feature set not supported
			01 = Removable Media Status Notification feature set supported
			10 = Reserved
			11 = Reserved

Word	O/M	F/V	Description
128	O		Security status
		F 15-9	Reserved
		V 8	Security level 0 = High, 1 = Maximum
		F 7-6	Reserved
		F 5	1 = Enhanced security erase supported
		V 4	1 = Security count expired
		V 3	1 = Security frozen
		V 2	1 = Security locked
		V 1	1 = Security enabled
		F 0	1 = Security supported
129-159		X	Vendor specific
160-175		F	Reserved for assignment by the CompactFlash™ Association
176-254		F	Reserved
255	O	X	Integrity word
			15-8 Checksum
			7-0 Signature

Key

O/M = Mandatory/optional requirement.

M = Support of the word is mandatory.

O = Support of the word is optional.

* = See 6.17.49.

F/V = Fixed/variable content.

F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.

V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.

X = the content of the word may be fixed or variable.

6.18.9 Word 0: General configuration

Bits (15:14) of word 0 indicate the type of device. Bit 15 shall be set to one and bit 14 shall be cleared to zero to indicate the device implements the PACKET Command feature set.

Bits (12:8) of word 0 indicate the command packet set implemented by the device. This value follows the peripheral device type value as defined in SCSI Primary Commands, ANSI INCITS 301:1997.

Value	Description
00h	Direct-access device
01h	Sequential-access device
02h	Printer device
03h	Processor device
04h	Write-once device
05h	CD-ROM device
06h	Scanner device
07h	Optical memory device
08h	Medium changer device
09h	Communications device
0A-0Bh	Reserved for ACS IT8 (Graphic arts pre-press devices)
0Ch	Array controller device
0Dh	Enclosure services device
0Eh	Reduced block command devices
0Fh	Optical card reader/writer device
10-1Eh	Reserved
1Fh	Unknown or no device type

Bit 7 if set to one indicates that the device has removable media.
Bits (6:5) of word 0 indicate the DRQ response time when a PACKET command is received. A value of 00b indicates a maximum time of 3 ms from receipt of PACKET to the setting of DRQ to one. A value of 10b indicates a maximum time of 50 μs from the receipt of PACKET to the setting of DRQ to one. The value 11b is reserved.
If bit 2 is set to one it indicates that the content of the IDENTIFY PACKET DEVICE data is incomplete. This will occur if the device supports the Power-up in Standby feature set and required data is contained on the device media. In this case the content of at least word 0 and word 2 shall be valid.
Bits (1:0) of word 0 indicate the packet size the device supports. A value of 00b indicates that a 12-byte packet is supported; a value of 01b indicates a 16 byte packet. The values 10b and 11b are reserved.

6.18.10 Word 1: Reserved

6.18.11 Word 2: Specific configuration

Word 2 shall have the same content described for word 2 of the IDENTIFY DEVICE command.

6.18.12 Words 3 to 9: Reserved

6.18.13 Words 10 to 19: Serial number

The use of these words is optional. If not implemented, the content shall be zeros. If implemented, the content shall be as described in words 10 to 19 of the IDENTIFY DEVICE command (see 6.17).

6.18.14 Words 20 to 22: Reserved

6.18.15 Words 23 to 26: Firmware revision

Words 23 to 26 shall have the content described for words 23 to 26 of the IDENTIFY DEVICE command.

6.18.16 Words 27 to 46: Model number

Words 27 to 46 shall have the content described for words 27 to 46 of the IDENTIFY DEVICE command.

6.18.17 Words 47 to 48: Reserved

6.18.18 Word 49: Capabilities

Bit 15 of word 49 is used to indicate that the device supports interleaved DMA data transfer for overlapped DMA commands. Devices which require the DMADIR bit in the Packet command shall clear this bit to 0.
Bit 14 of word 49 is used to indicate that the device supports command queuing for overlapped commands. If bit 14 is set to one, bit 13 shall be set to one.
Bit 13 of word 49 is used to indicate that the device supports command overlap operation.
Bit 12 of word 49 is obsolete.
Bit 11 of word 49 is used to determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This ensures backward compatibility. If a device supports PIO mode 3 or higher, then this bit shall be set to one. If the serial interface is implemented, this bit shall be set to one.
Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command. If the serial interface is implemented, this bit shall be set to one.
Bit 9 of word 49 shall be set to one.
Bit 8 of word 49 indicates that DMA is supported. Devices which require the DMADIR bit in the Packet command shall clear this bit to 0

6.18.19 Word 50: Capabilities

Word 50 shall have the content described for word 50 of the IDENTIFY DEVICE command. Support of this word is mandatory if the STANDBY command is supported.

6.18.20 Word 51: Obsolete

6.18.21 Word 52: Reserved

6.18.22 Word 53: Field validity

Word 53 shall have the content described for word 53 of the IDENTIFY DEVICE command.

6.18.23 Words 54 to 61: Reserved

6.18.24 Word 62: DMADIR

ATAPI devices that use a serial ATA bridge chip for connection to a serial ATA host may require use of the DMADIR bit to indicate transfer direction for Packet DMA commands. Word 62 is used to indicate if such support is required.
If bit 15 of word 62 is set to one, then DMADIR bit in the Packet Command is required by the device for Packet DMA and Bits 2:0 of word 63, bits 15 and 8 in word 49, and bits 6:0 of word 88 shall be cleared to 0.
If bit 15 of word 62 is cleared to 0, DMADIR bit in the PACKET command is not required. If bit 15 of word 62 is cleared to zero, then all bits of word 62 shall be cleared to zero.
Bits (14:11) are reserved.
Bits (10:1) indicate DMA mode support. Since the DMADIR bit is only used for a Serial ATAPI device, all of these bits are set to 1.

6.18.25 Word 63: Multiword DMA transfer

Word 63 identifies the Multiword DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is enabled, then no Multiword DMA mode shall be enabled. If a Multiword DMA mode is enabled then no Ultra DMA mode shall be enabled.

Bits (15:11) are reserved.
Bits 10:8 shall have the content described for word 63 of the IDENTIFY DEVICE command.
Bits (7:3) are reserved.
.
If bit 2 of Word 63 is set to one, then Multiword DMA modes 2 and below are supported. If this bit is cleared to zero, then Multiword DMA mode 2 is not supported. If Multiword DMA mode 2 is supported, then Multiword DMA modes 1 and 0 shall also be supported.
If bit 2 of Word 63 is set to one, bits (1:0) shall be set to one. If the serial interface is implemented, this bit shall be set to one except this bit shall be cleared 0 for Serial ATAPI devices requiring the DMADIR bit in the PACKET command.
If bit 1 of Word 63 is set to one, then Multiword DMA modes 1 and below are supported. If this bit is cleared to zero, then Multiword DMA mode 1 is not supported. If Multiword DMA mode 1 is supported, then Multiword DMA mode 0 shall also be supported.
If bit 1 of Word 63 is set to one, bit 0 shall be set to one. If the serial interface is implemented, this bit shall be set to one except this bit shall be cleared to 0 for Serial ATAPI devices which require the DMADIR bit in the PACKET command.
If bit 0 of word 63 is set to one, then Multiword DMA mode 0 is supported. If the serial interface is implemented, this bit shall be set to one except this bit shall be cleared to 0 for Serial ATAPI devices which require the DMADIR bit in the PACKET command.

6.18.26 Word 64: PIO transfer mode supported

Word 64 shall have the content described for word 64 of the IDENTIFY DEVICE command.

6.18.27 Word 65: Minimum multiword DMA transfer cycle time per word

Word 65 shall have the content described for word 65 of the IDENTIFY DEVICE command.

6.18.28 Word 66: Device recommended multiword DMA cycle time

Word 66 shall have the content described for word 66 of the IDENTIFY DEVICE command.

6.18.29 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 shall have the content described for word 67 of the IDENTIFY DEVICE command.

6.18.30 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 shall have the content described for word 68 of the IDENTIFY DEVICE command.

6.18.31 Word 69 to 70: Reserved

6.18.32 Word 71: PACKET to bus release time

Word 71 shall contain the time (for 99.7 % of the occurances) in microseconds from the receipt of a PACKET command until the device performs a bus release. Support of this word is mandatory if the Overlap or Queuing feature set is supported.

6.18.33 Word 72: SERVICE to bus release time

Word 72 shall contain the time (for 99.7 % of the occurances) in microseconds from the receipt of a SERVICE command until the device performs a bus release. Support of this word is mandatory if the Overlap or Queuing feature set is supported.

6.18.34 Word 73 to 74: Reserved

6.18.35 Word 75: Queue depth

Bits (4:0) of word 75 shall have the content described for word 75 of the IDENTIFY DEVICE command. Support of this word is mandatory if the Queuing feature set is supported.

6.18.36 Words 76 to 79: Reserved for Serial ATA

6.18.37 Word 80: Major revision number

Word 80 shall have the content described for word 80 of the IDENTIFY DEVICE command.

6.18.38 Word 81: Minor revision number

Word 81 shall have the content described for word 81 of the IDENTIFY DEVICE command.

6.18.39 Words 82 to 84: Features/command sets supported

Words 82 to 84 shall have the content described for words 82 to 84 of the IDENTIFY DEVICE command except that bit 4 of word 82 shall be set to one to indicate that the PACKET Command feature set is supported.

6.18.40 Words 85 to 87: Features/command sets enabled

Words 85 to 87 shall have the content described for words 85 to 87 of the IDENTIFY DEVICE command except that bit 4 of word 85 shall be set to one to indicate that the PACKET Command feature set is supported.

6.18.41 Word 88:Ultra DMA modes

Word 88 shall have the content described for word 88 of the IDENTIFY DEVICE command, except bits (6:0) shall be cleared to 0 for Serial ATAPI devices which require the DMADIR bit in the Packet command.

6.18.42 Word 89: Time required for Security erase unit completion

Word 89 shall have the content described for word 89 of the IDENTIFY DEVICE command.

6.18.43 Word 90: Time required for Enhanced security erase unit completion

Word 90 shall have the content described for word 90 of the IDENTIFY DEVICE command.

6.18.44 Word 91 to 92: Reserved

6.18.45 Word 93: Hardware reset results

Word 93 shall have the content described for word 93 of the IDENTIFY DEVICE command. Support of bits (13:15) is mandatory. Support of bits (12:0) is optional.

6.18.46 Word 94: Current automatic acoustic management value

Word 94 shall have the content described for word 94 of the IDENTIFY DEVICE command.

6.18.47 Word 95 to 124: Reserved

6.18.48 Word 125 ATAPI byte count=0 behavior

If the contents of word 125 are 0000h and the value of the byte count limit is zero, the device shall return command aborted.
If the contents of word 125 are non-zero and the value of the byte count limit is zero, the device shall use the contents of word 125 as the actual byte count limit for the current command and shall not abort.
The device may be reconfigured to report a new value. However, after the device is reconfigured, the content of word 125 reported shall not change until after the next hardware reset or power-on reset event.

6.18.49 Word 126: Obsolete

6.18.50 Word 127: Removable Media Status Notification feature set support

Word 127 shall have the content described for word 127 of the IDENTIFY DEVICE command. Support of this word is mandatory if the Removable Media Status Notification feature set is supported.

6.18.51 Word 128: Security status

Word 128 shall have the content described for word 128 of the IDENTIFY DEVICE command. Support of this word is mandatory if the Security feature set is supported.

6.18.52 Words 129 to 160: Reserved

6.18.53 Words 161 to 175: Reserved for assignment by the CompactFlash™ Association

6.18.54 Words 176 to 254: Reserved

6.18.55 Word 255: Integrity Word

Word 255 shall have the content described for word 255 of the IDENTIFY DEVICE command. Word 255 should be implemented.

6.19 IDLE

6.19.1 Command code

E3h

6.19.2 Feature set

Power Management feature set.

- This command is mandatory for devices not implementing the PACKET Command feature set.
- Power Management feature set is mandatory when power management is not implemented by the PACKET command set implemented by the device.
- This command is mandatory when the Power Management feature set is implemented.

6.19.3 Protocol

Non-data (see Clause 11).

6.19.4 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer. Table 19 defines these values.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	E3h							

Device register

DEV shall indicate the selected device.

Table 19 – Automatic Standby timer periods

Sector Count register contents		Corresponding timeout period
0	(00h)	Timeout disabled
1-240	(01h-F0h)	(value × 5) s
241-251	(F1h-FBh)	((value − 240) ×30) min
252	(FCh)	21 min
253	(FDh)	Period between 8 h and 12 h
254	(Feh)	Reserved
255	(FFh)	21 min 15 s
NOTE Times are approximate.		

6.19.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.19.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.19.7 Prerequisites

DRDY set to one.

6.19.8 Description

The IDLE command allows the host to place the device in the Idle mode and also set the Standby timer. INTRQ may be asserted even though the device may not have fully transitioned to Idle mode.
If the Sector Count register is non-zero then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer (see 4.5). If the Sector Count register is zero then the Standby timer is disabled.

6.20 IDLE IMMEDIATE

6.20.1 Command code

E1h

6.20.2 Feature set

Power Management feature set.

- This command is mandatory for devices not implementing the PACKET Command feature set.
- Power Management feature set is mandatory when power management is not implemented by the PACKET command set implemented by the device.
- This command is mandatory when the Power Management feature set is implemented.
- The Unload Feature of the command is optional.

6.20.3 Protocol

Non-data (see Clause 11).

6.20.4 Inputs (default function)

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	E1h							

Device register
DEV shall specify the selected device.

6.20.5 Inputs (Unload Feature)

Register	7	6	5	4	3	2	1	0
Features	44h							
Sector Count	00h							
LBA Low	4Ch							
LBA Mid	4Eh							
LBA High	55h							
Device	obs	na	obs	DEV	na	na	na	na
Command	E1h							

Device register
DEV shall specify the selected device.

6.20.6 Normal outputs (default function)

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.20.7 Normal outputs (Unload Feature)

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	C4h							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

LBA Low
C4h to indicate that unloading successfully completed.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.20.8 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if Power Management feature set is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.20.9 Prerequisites

DRDY set to one.

6.20.10 Description

Default Function:
The IDLE IMMEDIATE command allows the host to immediately place the device in the Idle mode. INTRQ may be asserted even though the device may not have fully transitioned to Idle mode (see 4.5).
Unload Feature:
The UNLOAD FEATURE of the IDLE IMMEDIATE command allows the host to immediately unload/park the heads. The device shall stop read look-ahead if it is in process. If the device is performing a write operation, the device shall suspend writing cached data onto the media as soon as possible, and keep unwritten sectors stored in the buffer until receiving a new command.
A device that supports load/unload technology shall retract the head(s) onto the ramp position as soon as receiving this command. INTRQ shall be asserted and BSY shall be cleared after the head(s) is(are) completely retracted onto the ramp position and latched if available. The time to complete the unload operation is vendor specific, this typically would be within 500 ms of receiving the command. The unload controlling method by the Unload Feature of the Idle Immediate command shall be the same as that by Power mode transition, and shall not effect the specification of normal load/unload times per device life.
A device that supports contact start/stop technology shall seek to the landing zone. INTRQ shall be asserted and BSY shall be cleared after seek completion. The time to complete the seek operation is vendor specific, this typically would be within 300 ms of receiving this command.
The device shall stay at Low Power Idle mode, shall not go into Standby mode and shall not load the head(s) onto the media until receiving a new command. Power consumption of the device is not an issue for this case. If a device receives this command while the head(s) is(are) currently on ramp/parked no physical action is needed.

The device shall retain data in the write cache and resume writing the cached data onto the media after receiving a Software Reset, a Hardware Reset, or any new command except IDLE IMMEDIATE with UNLOAD FEATURE.

6.21 MEDIA EJECT

6.21.1 Command code

EDh

6.21.2 Feature set

Removable Media Status Notification feature set

- Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media Status Notification feature set.
- Prohibited for devices implementing the PACKET command feature set.

Removable Media feature set

- Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media feature set.
- Prohibited for devices implementing the PACKET command feature set.

6.21.3 Protocol

Non-data (see Clause 11).

6.21.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	Edh							

Device register

DEV shall specify the selected device.

6.21.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.21.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	NM	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.

NM (No Media) shall be set to one if no media is present in the device.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.21.7 Prerequisites

DRDY set to one.

6.21.8 Description

This command causes any pending operations to complete, spins down the device if needed, unlocks the media if locked, and ejects the media. The device keeps track of only one level of media lock.

6.22 MEDIA LOCK

6.22.1 Command code

DEh

6.22.2 Feature set

Removable Media Status Notification feature set

– Optional for devices not implementing the PACKET command feature set and implementing the Removable Media Status Notification feature set.
– Prohibited for device implementing the PACKET command feature set.

Removable Media feature set

– Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media feature set.
– Prohibited for devices implementing the PACKET command feature set.

6.22.3 Protocol

Non-data (see Clause 11).

6.22.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	Deh							

Device register
DEV shall specify the selected device.

6.22.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.22.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.

NM (No Media) shall be set to one if no media is present in the device.

MCR (Media Change Request) shall be set to one if the device is locked and a media change request has been detected by the device.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.22.7 Prerequisites

DRDY set to one.

6.22.8 Description

This command shall be used to lock the media, if Media Status Notification is disabled. If Media Status Notification is enabled, this command shall return good status (no ERR bit in the Status register) and perform no action.

If the media is unlocked and media is present, the media shall be set to the LOCKED state and no Error register bit shall be set to one. The device keeps track of only one level of media lock. Subsequent MEDIA LOCK commands, while the media is in the LOCKED state, do not set additional levels of media locks.

If the media is locked, the status returned shall indicate whether a media change request has been detected by the device. If a media change request has been detected, the MCR bit in the Error register and the ERR bit in the Status register shall be set to one.

When media is in the LOCKED state, the device shall respond to the media change request button, by setting the MCR bit in the Error register and the ERR bit in the Status register to one, until the media LOCKED condition is cleared.

6.23 MEDIA UNLOCK

6.23.1 Command code

DFh

6.23.2 Feature set

Removable Media Status Notification feature set

– Optional for devices not implementing the PACKET command feature set and implementing the Removable Media Status Notification feature set.

– Prohibited for devices implementing the PACKET command feature set.

Removable Media feature set

– Mandatory for devices not implementing the PACKET command feature set and implementing the Removable Media feature set.

– Prohibited for devices implementing the PACKET command feature set.

6.23.3 Protocol

Non-data (see Clause 11).

6.23.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	DFh							

Device register
DEV shall specify the selected device.

6.23.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.23.6 Error outputs

If the device does not support this command, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	NM	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if device does not support this command. ABRT may be set to one if the device is not able to complete the action requested by the command.
NM (No Media) shall be set to one if no media is present in the device.
Device register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.23.7 Prerequisites

DRDY set to one.

6.23.8 Description

This command can be used to unlock the device, if Media Status Notification is disabled. If Media Status Notification is enabled, this command will return good status (no ERR bit in the Status register) and perform no action.
If the media is present, the media shall be set to the UNLOCKED state and no Error register bit shall be set to one. The device keeps track of only one level of media lock. A single MEDIA UNLOCK command unlocks the media.
If a media change request has been detected by the device prior to the issuance of this command, the media shall be ejected at MEDIA UNLOCK command completion.

6.24 NOP

6.24.1 Command code

00h

6.24.2 Feature set

General feature set
– Optional for devices not implementing the PACKET Command feature set.
– Mandatory for devices implementing the PACKET Command feature set.
– Mandatory for devices implementing the Overlapped feature set.

6.24.3 Protocol

Non-data (see Clause 11).

6.24.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	00h							

Features register

Subcommand code	Description	Action
00h	NOP	Return command aborted and abort any outstanding queued commands.
01h	NOP Auto Poll	Return command aborted and do not abort any outstanding queued commands.
02h-FFh	Reserved	Return command aborted and do not abort any outstanding queued commands.

Device register
DEV shall specify the selected device.

6.24.5 Normal outputs

This command always fails with an error.

6.24.6 Error outputs

The Command Block registers, other than the Error and Status registers, are not changed by this command. This command always fails with the device returning command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	Initial value							
LBA Low	Initial value							
LBA Mid	Initial value							
LBA High	Initial value							
Device	Initial value							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one.
Sector Count, LBA Low, LBA Mid, LBA High, Device
value set by host is not changed.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one.

6.24.7 Prerequisites

DRDY set to one.

6.24.8 Description

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

6.25 PACKET

6.25.1 Command code

A0h

6.25.2 Feature set

PACKET Command feature set
– Use prohibited for devices not implementing the PACKET Command feature set.
– Mandatory for devices implementing the PACKET Command feature set.

6.25.3 Protocol

Packet (see Clause 11).

6.25.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na	na	na	na	na	DMADIR	OVL	DMA
Sector Count	Tag					na		
LBA Low	na							
Byte Count Low	Byte Count limit (7:0)							
Byte Count High	Byte Count limit (15:8)							
Device	obs	na	obs	DEV	na	na	na	na
Command	A0h							

Features register

DMADIR This bit indicates Packet DMA direction and is used only for devices that implement the Packet Command feature set with a Serial ATA bridge that require direction indication from the host. Support for this bit is determined by reading bit 15 of word 62 in the IDENTIFY PACKET DEVICE data. If bit 15 of word 62 is set to 1, the device requires the use of the DMADIR bit for Packet DMA commands.

If the device requires the DMADIR bit to be set for Packet DMA operations and the current operations is DMA (i.e. bit 0, the DMA bit, is set), this bit indicates the direction of data transfer (0 = transfer to the device; 1 = transfer to the host).

If the device requires the DMADIR bit to be set for Packet DMA operations but the current operations is PIO (i.e. bit 0, the DMA bit, is cleared), this bit is ignored.

Since the data transfer direction will be set by the host as the command is constructed, the DMADIR bit should not conflict with the data transfer direction of the command. If a conflict between the command transfer direction and the DMADIR bit occurs, the device should return with an ABORTED command, and the sense key set to ILLEGAL REQUEST.

If the device does not require the DMADIR bit for Packet DMA operations, this bit should be cleared to 0.

A device that does not support the DMADIR feature may abort a command if the DMADIR bit is set to 1.

OVL This bit is set to one to inform the device that the PACKET command is to be overlapped.

DMA This bit is set to one to inform the device that the data transfer (not the command packet transfer) associated with this command is via Multiword DMA or Ultra DMA mode.

Sector Count register

Tag If the device supports command queuing, this field contains the command Tag for the command being delivered. A Tag may have any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this field is not applicable.

Byte Count low and Byte Count high registers

These registers are written by the host with the maximum byte count that is to be transferred in any single DRQ assertion for PIO transfers. The byte count does not apply to the command packet transfer. If the PACKET command does not transfer data, the byte count is ignored.

If the PACKET command results in a data transfer:

1) the host should not set the byte count limit to zero. If the host sets the byte count limit to zero, the contents of IDENTIFY PACKET DEVICE data word 125 determines the expected behavior;
2) the value set into the byte count limit shall be even if the total requested data transfer length is greater than the byte count limit;
3) the value set into the byte count limit may be odd if the total requested data transfer length is equal to or less than the byte count limit;
4) the value FFFFh is interpreted by the device as though the value were FFFEh.

Device register
DEV shall specify the selected device.

6.25.5 Normal outputs

6.25.5.1 Awaiting command

When the device is ready to accept the command packet from the host the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason	Tag					REL	I/O	C/D
LBA Low	na							
Byte Count Low	Byte Count (7:0)							
Byte Count High	Byte Count (15:8)							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	na	DMRD	SERV	DRQ	na	na	CHK

Byte Count High/Low shall reflect the value set by the host when the command was issued.
Interrupt reason register
Tag If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.
REL shall be cleared to zero.
I/O shall be cleared to zero indicating transfer to the device.
C/D shall be set to one indicating the transfer of a command packet.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero.
DMRD (DMA ready) shall be cleared to zero.
SERV (Service) shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.
DRQ shall be set to one.
CHK shall be cleared to zero.

6.25.5.2 Data transmission

If overlap is not supported or not specified by the command, data transfer shall occur after the receipt of the command packet. If overlap is supported and the command specifies that the command may be overlapped, data transfer may occur after receipt of the command packet or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason	Tag					REL	I/O	C/D
LBA Low	na							
Byte Count Low	Byte Count (7:0)							
Byte Count High	Byte Count (15:8)							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	na	DMRD	SERV	DRQ	na	na	CHK

Byte Count High/Low If the transfer is to be in PIO mode, the byte count of the data to be transferred for this DRQ assertion shall be presented.

Valid byte count values are as follows:

1) the byte count shall be less than or equal to the byte count limit value from the host;
2) the byte count shall not be zero;
3) the byte count shall be less than or equal to FFFEh;
4) the byte count shall be even except for the last transfer of a command;
5) if the byte count is odd, the last valid byte transferred is on DD(7:0) and the data on DD(15:8) is a pad byte of undefined value;
6) if the last transfer of a command has a pad byte, the byte count shall be odd.

Interrupt reason register

Tag If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL shall be cleared to zero.

I/O shall be cleared to zero if the transfer is to the device and shall be set to one if the transfer is to the host.

C/D shall be cleared to zero indicating the transfer of data.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero.

DMRD (DMA ready) shall be set to one if the transfer is to be a DMA or Ultra DMA transfer and the device supports overlap DMA.

SERV (Service) shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DRQ shall be set to one.

CHK shall be cleared to zero.

6.25.5.3 Bus release (overlap feature set only)

After receiving the command packet, the device sets BSY to one and clears DRQ to zero. If the command packet requires a data transfer, the OVL bit is set to one, the Release interrupt is disabled, and the device is not prepared to immediately transfer data, the device may perform a bus release by placing the following register content in the Command Block registers. If the command packet requires a data transfer, the OVL bit is set to one, and the Release interrupt is enabled, the device shall perform a bus release by setting the register content as follows.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason	Tag					REL	I/O	C/D
LBA Low	na							
Byte Count Low	na							
Byte Count High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Byte Count High/Low na.

Interrupt reason register

Tag If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL shall be set to one.

I/O shall be cleared to zero.

C/D shall be cleared to zero.

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating bus release.
DRDY na.
DMRD (DMA ready) shall be cleared to zero.
SERV (Service) shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.
DRQ shall be cleared to zero.
CHK shall be cleared to zero.

6.25.5.4 Service request (overlap feature set only)

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see 10). When the SERVICE command is received, the device shall set outputs as described in data transfer, successful command completion or error outputs depending on the service the device requires.

6.25.5.5 Successful command completion

When the device has command completion without error, the device sets the following register content.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason	Tag					REL	I/O	C/D
LBA Low	na							
Byte Count Low	na							
Byte Count High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Byte Count High/Low na.
Interrupt reason register
Tag If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.
REL shall be cleared to zero.
I/O shall be set to one.
C/D shall be set to one.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DMRD (DMA ready) na.
SERV (Service) shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.
DRQ shall be cleared to zero.
CHK shall be cleared to zero.

6.25.6 Error outputs

The device shall not terminate the PACKET command with an error before the last byte of the command packet has been written (see Clause 11).

Register	7	6	5	4	3	2	1	0
Error	Sense key				na	ABRT	EOM	ILI
Interrupt reason	Tag					REL	I/O	C/D
LBA Low	na							
Byte Count Low	na							
Byte Count High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	SERV	DRQ	na	na	CHK

Error register

Sense Key is a command packet set specific error indication.

ABRT shall be set to one if the requested command has been command aborted because the command code or a command parameter is invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

EOM the meaning of this bit is command set specific. See the appropriate command set standard for the definition of this bit.

ILI the meaning of this bit is command set specific. See the appropriate command set standard for the definition of this bit.

Interrupt reason register

Tag If the device supports command queuing and overlap is enabled, this field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this field is not applicable.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SERV (Service) shall be set to one if another command is ready to be serviced. If overlap is not supported, this bit is command specific.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

CHK shall be set to one if an Error register sense key or code bit is set.

6.25.7 Prerequisites

This command shall be accepted regardless of the state of DRDY.

6.25.8 Description

The PACKET command is used to transfer a device command via a command packet. If the native form of the encapsulated command is shorter than the packet size reported in bits (1:0) of word 0 of the IDENTIFY PACKET DEVICE response, the encapsulated command shall begin at byte 0 of the packet. Packet bytes beyond the end of the encapsulated command are reserved.

If the device supports overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, the device may or may not perform a bus release. If the device is ready for the data transfer, the device may begin the transfer immediately as described in the non-overlapped protocol (see Clause 11). If the data is not ready, the device may perform a bus release and complete the transfer after the execution of a SERVICE command.

6.26 READ BUFFER

6.26.1 Command code

E4h

6.26.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

6.26.3 Protocol

PIO data-in (see Clause 11).

6.26.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	E4h							

Device register

DEV shall specify the selected device.

6.26.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.26.6 Error outputs

The device shall return command aborted if the command is not supported.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.26.7 Prerequisites

DRDY set to one. The command prior to a READ BUFFER command shall be a WRITE BUFFER command.

6.26.8 Description

The READ BUFFER command enables the host to read the current contents of the device's sector buffer.
The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

6.27 READ DMA

6.27.1 Command code

C8h

6.27.2 Feature set

General feature set

– Mandatory for devices not implementing the PACKET Command feature set.
– Use prohibited for devices implementing the PACKET Command feature set.

6.27.3 Protocol

DMA (see Clause 11).

6.27.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	C8h							

Sector Count
number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.
LBA Low
starting LBA bits (7:0).
LBA Mid
starting LBA bits (15:8).
LBA High
starting LBA bits (23:16).
Device
the LBA bit shall be set to one to specify the address is an LBA,
DEV shall specify the selected device.
Bits (3:0) shall be starting LBA bits (27:24).

6.27.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.27.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

LBA Low, LBA Mid, LBA High, Device

shall be written with the address of first unrecoverable error.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

6.27.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

6.27.8 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

6.28 READ DMA EXT

6.28.1 Command code

25h

6.28.2 Feature set

48-bit Address feature set

- Mandatory for devices implementing the 48-bit Address feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

6.28.3 Protocol

DMA (see Clause 11).

6.28.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		25h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Sector Count Current
number of sectors to be transferred low order, bits (7:0).

Sector Count Previous
number of sectors to be transferred high order, bits (15:8). 0000h in the Sector Count register specifies that 65 536 sectors are to be transferred.

LBA Low Current
LBA (7:0).

LBA Low Previous
LBA (31:24).

LBA Mid Current
LBA (15:8).

LBA Mid Previous
LBA (39:32).

LBA High Current
LBA (23:16).

LBA High Previous
LBA (47:40).

Device
DEV shall specify the selected device.
LBA bit shall be set to 1

6.28.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE – HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.28.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

LBA Low

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA Mid

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA High

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one; however, if SE is set to one, ERR shall be cleared to zero.

6.28.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

6.28.8 Description

The READ DMA EXT command allows the host to read data using the DMA data transfer protocol.

6.29 READ DMA QUEUED

6.29.1 Command code

C7h

6.29.2 Feature set

Overlapped feature set

- Mandatory for devices implementing the Overlapped feature set and not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET command feature set.

6.29.3 Protocol

DMA QUEUED (see Clause 11).

6.29.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	C7h							

Features
: number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

Sector count
: if the device supports command queuing, bits (7:3) contain the Tag for the command being delivered. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this register shall be set to the value 00h.

LBA Low
: starting LBA bits (7:0).

LBA Mid
: starting LBA bits (15:8).

LBA High
: starting LBA bits (23:16).

Device
: the LBA bit shall be set to one to specify the address is an LBA.
DEV shall specify the selected device.
Bits (3:0) starting LBA bits (27:24).

6.29.5 Normal outputs

6.29.6 Data transmission

Data transfer may occur after receipt of the command or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	SERV	DRQ	na	na	CHK

Sector Count register
Tag This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this register shall be set to the value 00h.
REL shall be cleared to zero.
I/O shall be set to one indicating the transfer is to the host.
C/D shall be cleared to zero indicating the transfer of data.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
SERV (Service) shall be set to one if another command is ready to be serviced.
DRQ shall be set to one.
CHK shall be cleared to zero.

6.29.7 Bus release

If the device performs a bus release before transferring data for this command, the register content upon performing a bus release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Sector Count register
Tag If the device supports command queuing, this field shall contain the Tag of the command being bus released. If the device does not support command queuing, this field shall be set to the value 00h.
REL shall be set to one.
I/O shall be zero.
C/D shall be zero.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating bus release.
DRDY shall be set to one.
SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service. SERV shall be set to one when the device has prepared this command for service.
DF (Device Fault) shall be cleared to zero.
DRQ bit shall be cleared to zero.
ERR bit shall be cleared to zero.

6.29.8 Service request

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see Clause 10). When the SERVICE command is received, the device shall set outputs as described in data transfer, command completion or error outputs depending on the service the device requires.

6.29.9 Command completion

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	I/O	C/D
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Sector Count register

Tag If the device supports command queuing, this field shall contain the Tag of the completed command. If the device does not support command queuing, this field shall be set to the value 00h.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service.

DF (Device Fault) shall be cleared to zero.

DRQ bit shall be cleared to zero.

ERR bit shall be cleared to zero.

6.29.10 Error outputs

The Sector Count register contains the Tag for this command if the device supports command queuing. The device shall return command aborted if the command is not supported or if the device has not had overlapped interrupt enabled. The device shall return command aborted if the device supports command queuing and the Tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	Tag					REL	I/O	C/D
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Error register

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if ABRT is not set to one.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count register

Tag If the device supports command queuing, this field shall contain the Tag of the completed command. If the device does not support command queuing, this field shall be set to the value 00h.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

LBA Low, LBA Mid, LBA High, Device

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.29.11 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

6.29.12 Description

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or may execute the data transfer without performing a bus release if the data is ready to transfer.

6.30 READ DMA QUEUED EXT

6.30.1 Command code

26h

6.30.2 Feature set

48-bit Address feature set

- Mandatory for devices implementing the Overlapped feature set and the 48-bit Address feature set and not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET command feature set.

6.30.3 Protocol

DMA QUEUED (see Clause 11).

6.30.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
Sector Count	Current	Tag					Reserved		
	Previous	Reserved							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		26h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Features Current
number of sectors to be transferred low order, bits (7:0).

Features Previous
number of sectors to be transferred high order, bits (15:8). 0000h in the Features register specifies that 65 536 sectors are to be transferred.

Sector Count Current
if the device supports command queuing, bits (7:3) contain the Tag for the command being delivered. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If queuing is not supported, this register shall be set to the value 00h.

Sector Count Previous
Reserved

LBA Low Current
LBA (7:0).

LBA Low Previous
LBA (31:24).

LBA Mid Current -
LBA (15:8).

LBA Mid Previous
LBA (39:32).

LBA High Current
LBA (23:16).

LBA High Previous
LBA (47:40).

Device
DEV shall specify the selected device.
LBA shall be set to one

6.30.5 Normal outputs

6.30.5.1 Data transmission

Data transfer may occur after receipt of the command or may occur after the receipt of a SERVICE command. When the device is ready to transfer data requested by a data transfer command, the device sets the following register content to initiate the data transfer.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Tag					REL	I/O	C/D
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Sector Count (when the HOB bit of the Device Control register is cleared to zero)

Tag This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this register shall be set to the value 00h.

REL shall be cleared to zero.

I/O shall be set to one indicating the transfer is to the host.

C/D shall be cleared to zero indicating the transfer of data.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.30.5.2 Bus release

If the device performs a bus release before transferring data for this command, the register content upon performing a bus release shall be as shown below.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Tag					REL	I/O	C/D
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Sector Count (when the HOB bit of the Device Control register is cleared to zero)

Tag This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this register shall be set to the value 00h.

REL shall be set to one.

I/O shall be set to one indicating the transfer is to the host.

C/D shall be cleared to zero indicating the transfer of data.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service. SERV shall be set to one when the device has prepared this command for service.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.30.5.3 Service request

When the device is ready to transfer data or complete a command after the command has performed a bus release, the device shall set the SERV bit and not change the state of any other register bit (see Clause 10). When the SERVICE command is received, the device shall set outputs as described in data transfer, command completion or error outputs depending on the service the device requires.

6.30.5.4 Command completion

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Tag					REL	I/O	C/D
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Sector Count (when the HOB bit of the Device Control register is cleared to zero)

Tag This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this register shall be set to the value 00h.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

SERV (Service) shall be cleared to zero when no other queued command is ready for service. SERV shall be set to one when another queued command is ready for service.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.30.6 Error outputs

The Sector Count register contains the Tag for this command if the device supports command queuing. The device shall return command aborted if the command is not supported or if the device has not had overlapped interrupt enabled. The device shall return command aborted if the device supports command queuing and the Tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort.

Register		7	6	5	4	3	2	1	0
Error		ICRC	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Tag					REL	I/O	C/D
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	SERV	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

Sector Count (when the HOB bit of the Device Control register is cleared to zero)

Tag This field contains the command Tag for the command. A Tag value may be any value between 0 and 31 regardless of the queue depth supported. If the device does not support command queuing or overlap is disabled, this register shall be set to the value 00h.

REL shall be cleared to zero.

I/O shall be set to one.

C/D shall be set to one.

LBA Low

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA Mid

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA High

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.30.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

6.30.8 Description

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or may execute the data transfer without performing a bus release if the data is ready to transfer.

6.31 READ LOG EXT

6.31.1 Command code

2Fh

6.31.2 Feature set

General Purpose Logging feature set

– Mandatory for devices implementing the General Purpose Logging feature set.

6.31.3 Protocol

PIO data-in (see Clause 11)

6.31.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	Log address							
	Previous	Reserved							
LBA Mid	Current	Sector offset (7:0)							
	Previous	Sector offset (15:8)							
LBA High	Current	Reserved							
	Previous	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Command		2Fh							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Sector Count Specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.

LBA Low Specifies the log to be returned as described in Table 20. A device may support a subset of the available logs. Support for individual logs is determined by support for the associated feature set. Support of the associated log(s) is mandatory for devices implementing the associated feature set. The host vendor specific logs may be used by the host to store any data desired. If a host vendor specific log has never been written by the host, when read the content of the log shall be zeros. Device vendor specific logs may be used by the device vendor to store any data and need only be implemented if used.

LBA Mid Specifies the first sector of the log to be read.

Device/Head register

DEV shall indicate the selected device.

Table 20 – Log address definition

Log address	Content	Feature set	R/W
00h	Log directory	na	RO
01h	Reserved	na	Reserved
02h	Comprehensive SMART error log	SMART error logging	See note
03h	Extended Comprehensive SMART error log	SMART error logging	RO
04h-05h	Reserved	na	Reserved
06h	SMART self-test log	SMART self-test	See note
07h	Extended SMART self-test log	SMART self-test	RO
08h-0Fh	Reserved	na	Reserved
10h-17h	Reserved for Serial ATA		
18h-1Fh	Reserved	na	Reserved
20h	Streamingperformance log	Streaming	RO
21h	Write stream error log	Streaming	RO
22h	Read stream error log	Streaming	RO
23h	Delayed sector log	General Purpose Logging	RO
24h-7Fh	Reserved	na	Reserved
80h-9Fh	Host vendor specific	SMART	R/W
A0h-BFh	Device vendor specific	SMART	VS
C0h-FFh	Reserved	na	Reserved

Key

RO = Log is read only by the host.

R/W = Log is read or written by the host.

VS = Log is vendor specific thus read/write ability is vendor specific.

NOTE If log address 02h or log address 06h are accessed using the READ LOG EXT or WRITE LOG EXT commands, command abort shall be returned.

The Comprehensive SMART error log and the SMART self-test log are defined in 6.54.7 and 6.54.9. If log address 02h or log address 06h are accessed using the READ LOG EXT or WRITE LOG EXT commands, command abort shall be returned.

All 28-bit entries contained in the Comprehensive SMART log shall also be included in the Extended Comprehensive SMART error log with the 48-bit entries.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log sector shall also be included in the Comprehensive SMART self-test log sector with the 48-bit entries.

6.31.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device/Head register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.31.6 Error outputs

If the device does not support this command, if the feature set associated with the log specified in the LBA Low register is not supported or enabled, or if the values in the Features, Sector Count, LBA Mid or LBA High registers are invalid, the device shall return command aborted.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	na	IDNF	na	ABRT	na	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device/Head		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

UNC shall be set to one if the log contains one or more sectors that are uncorrectable. IDNF shall be set to one if the log sector's ID field was not found or data structure checksum error occurred.

ABRT shall be set to one if this command is not supported, if the feature associated with the log specified in the LBA Low register is not supported, or if other register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if the Sector Count register contains a count larger than the log size reported in the Log Directory. ABRT shall be set to one if the host issues a READ LOG EXT or WRITE LOG EXT command with a value of zero in the Sector Count register.

Device/Head register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be set to one indicating that a device fault has occurred.

DRQ shall be cleared to zero indicating that there is no data to be transferred.

ERR shall be set to one if any Error register bit is set to one.

6.31.7 Prerequisites

DRDY set to one.

6.31.8 Description

6.31.8.1 General

This command returns the specified log to the host. The device shall interrupt for each DRQ block transferred. See 6.54.7.

6.31.8.2 General Purpose Log Directory

Table 21 defines the 512 bytes that make up the General Purpose Log Directory.

Table 21 – General Purpose Log Directory

Byte	Descriptions
0-1	General Purpose Logging Version
2	Number of sectors in the log at log address 01h (7:0)
3	Number of sectors in the log at log address 01h (15:8)
4	Number of sectors in the log at log address 02h (7:0)
5	Number of sectors in the log at log address 02h (15:8)
...	
256	10h sectors in the log at log address 80h
257	00h sectors in the log at log address 80h
...	
510-511	Number of sectors in the log at log address FFh

The value of the General Purpose Logging Version word shall be 0001h. A value of 0000h indicates that no General Purpose log Directory exists.

The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

6.31.8.3 Extended Comprehensive SMART Error log

6.31.8.3.1 General

Table 22 defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. The maximum size of the Extended Comprehensive SMART error log is 65 536 sectors. Devices may support fewer than 65 535 sectors. All multi-byte fields shown in this structure follow the byte ordering described in Clause 3. Error log data structures shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Error log data structures shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or invalid addresses.
All 28-bit entries contained in the Comprehensive SMART log, defined in 6.54.7.8.3.7, shall also be included in the Extended Comprehensive SMART error log with the 48-bit entries.

Table 22 – Extended Comprehensive SMART error log

Byte	First sector	Subsequent sectors
0	SMART error log version	Reserved
1	Reserved	Reserved
2	Error log index (7:0)	Reserved
3	Error log index (15:8)	Reserved
4-127	First error log data structure	Data structure 4*n*+1
128-251	Second error log data structure	Data structure 4*n*+2
252-375	Third error log data structure	Data structure 4*n*+3
376-499	Fourth error log data structure	Data structure 4*n*+4
500-501	Device error count	Reserved
502-510	Reserved	Reserved
511	Data structure checksum	Data structure checksum
n is the sector number within the log. The first sector is sector zero		

6.31.8.3.2 Error log version

The value of the SMART error log version byte shall be 01h.

6.31.8.3.3 Error log index

The error log index indicates the error log data structure representing the most recent error. If there have been no error log entries, the error log index is cleared to zero. Valid values for the error log index are zero to 65 536.

6.31.8.3.4 Extended Error log data structure

6.31.8.3.4.1 General

The error log is viewed as a circular buffer. When the last supported error log sector has been filled, the next error shall create an error log data structure that replaces the first error log data structure in sector zero. The next error after that shall create an error log data structure that replaces the second error log data structure in sector zero. The fifth error after the log has filled shall replace the first error log data structure in sector one, and so on.
The error log index indicates the most recent error log data structure. Unused error log data structures shall be filled with zeroes.
The content of the error log data structure entries is defined in Table 23.

Table 23 – Extended Error log data structure

Byte	Descriptions
n thru *n*+17	First command data structure
n+18 thru *n*+35	Second command data structure
n+36 thru *n*+53	Third command data structure
n+54 thru *n*+71	Fourth command data structure
n+72 thru *n*+89	Fifth command data structure
n+90 thru *n*+123	Error data structure

6.31.8.3.4.2 Command data structure

The fifth command data structure shall contain the command or reset for which the error is being reported. The fourth command data structure should contain the command or reset that preceded the command or reset for which the error is being reported, the third command data structure should contain the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures shall be zero filled, for example, if only three commands and resets preceded the command or reset for which the error is being reported, the first command data structure shall be zero filled. In some devices, the hardware implementation may preclude the device from reporting the commands that preceded the command for which the error is being reported or that preceded a reset. In this case, the command data structures are zero filled.

If the command data structure represents a command or software reset, the content of the command data structure shall be as shown in Table 24. If the command data structure represents a hardware reset, the content of byte *n* shall be FFh, the content of bytes *n*+1 through *n*+13 are vendor specific, and the content of bytes *n*+14 through *n*+17 shall contain the timestamp.

Table 24 – Command data structure

Byte	Descriptions
n	Content of the Device Control register when the Command register was written.
n+1	Content of the Features register (7:0) when the Command register was written (see note).
n+2	Content of the Features register (15:8) when the Command register was written.
n+3	Content of the Sector Count register (7:0) when the Command register was written.
n+4	Content of the Sector Count register (15:8) when the Command register was written.
n+5	Content of the LBA Low register (7:0) when the Command register was written.
n+6	Content of the LBA Lowregister (15:8) when the Command register was written.
n+7	Content of the LBA Mid register (7:0) when the Command register was written.
n+8	Content of the LBA Mid register (15:8) when the Command register was written.
n+9	Content of the LBA High register (7:0) when the Command register was written.
n+10	Content of the LBA High register (15:8) when the Command register was written.
n+11	Content of the Device/Head register when the Command register was written.
n+12	Content written to the Command register.
n+13	Reserved
n+14	Timestamp (least significant byte)
n+15	Timestamp (next least significant byte)
n+16	Timestamp (next most significant byte)
n+17	Timestamp (most significant byte)
NOTE Bits (7:0) refer to the most recently written contents of the register. Bits (15:8) refer to the contents of the register prior to the most recent write to the register.	

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

6.31.8.3.4.3 Error data structure

The error data structure shall contain the error description of the command for which an error was reported as described in Table 25. If the error was logged for a hardware reset, the content of bytes *n*+1 through *n*+11 shall be vendor specific and the remaining bytes shall be as defined in Table 25.

Table 25 – Error data structure

Byte	Descriptions
n	Reserved
n+1	Content of the Error register after command completion occurred.
n+2	Content of the Sector Count register (7:0) after command completion occurred (see note).
n+3	Content of the Sector Count register (15:8) after command completion occurred (see note).
n+4	Content of the LBA Low register (7:0) after command completion occurred.
n+5	Content of the LBA Low register (15:8) after command completion occurred.
n+6	Content of the LBA Mid register (7:0) after command completion occurred.
n+7	Content of the LBA Mid register (15:8) after command completion occurred.
n+8	Content of the LBA High register (7:0) after command completion occurred.
n+9	Content of the LBA High register (15:8) after command completion occurred.
n+10	Content of the Device/Head register after command completion occurred.
n+11	Content written to the Status register after command completion occurred.
n+12 through *n*+30	Extended error information
n+31	State
n+32	Life timestamp (least significant byte)
n+33	Life timestamp (most significant byte)
NOTE Bits (7:0) refer to the contents if the register were read with bit 7 of the Device Control register cleared to zero. Bits (15:8) refer to the contents if the register were read with bit 7 of the Device Control register set to one.	

Extended error information shall be vendor specific.

State shall contain a value indicating the state of the device when the command was written to the Command register or the reset occurred as described in Table 26.

Table 26 – State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique
The value of x is vendor specific and may be different for each state.	

Sleep indicates the reset for which the error is being reported was received when the device was in the Sleep mode.
Standby indicates the command or reset for which the error is being reported was received when the device was in the Standby mode.
Active/Idle with BSY cleared to zero indicates the command or reset for which the error is being reported was received when the device was in the Active or Idle mode and BSY was cleared to zero.
Executing SMART off-line or self-test indicates the command or reset for which the error is being reported was received when the device was in the process of executing a SMART off-line or self-test.

Life timestamp shall contain the power-on lifetime of the device in hours when command completion occurred.

6.31.8.3.5 Device error count

The device error count field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. These errors shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. This count shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached, the count shall remain at the maximum value when additional errors are encountered and logged.

6.31.8.3.6 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

6.31.8.4 Extended Self-test log sector

6.31.8.4.1 General

Table 27 defines the format of each of the sectors that comprise the Extended SMART self-test log. The maximum size of the self-test log is 65 535 sectors. Devices may support fewer than 65 536 sectors. All multi-byte fields shown in this structure follow the byte ordering described in Clause 3.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log, defined in 6.54.7.8.4 shall also be included in the Extended SMART self-test log with all 48-bit entries.

Table 27 – Extended Self-test log data structure

Byte	First sector	Subsequent sectors
0	Self-test log data structure revision number	Reserved
1	Reserved	Reserved
2	Self-test descriptor index (7:0)	Reserved
3	Self-test descriptor index (15:8)	Reserved
4-29	Descriptor entry 1	Descriptor entry 19*n*+1
30-55	Descriptor entry 2	Descriptor entry 19*n*+2
....	....	....
472-497	Descriptor entry 19	Descriptor entry 19*n*+19
498-499	Vendor specific	Vendor specific
500-510	Reserved	Reserved
511	Data structure checksum	Data structure checksum
n is the sector number within the log. The first sector is sector zero		

This log is viewed as a circular buffer. When the last supported self-test log sector has been filled, the next self-test shall create a descriptor that replaces descriptor entry 1 in sector 0. The next self-test after that shall create a descriptor that replaces descriptor entry 2 in sector 0, and so on. All unused self-test descriptors shall be filled with zeroes.

6.31.8.4.2 Self-test descriptor index

The Self-test descriptor index indicates the most recent self-test descriptor. If there have been no self-tests, the Self-test descriptor index is set to zero. Valid values for the Self-test descriptor index are zero to 65 535.

6.31.8.4.3 Self-test log data structure revision number

The value of the self-test log data structure revision number shall be 01h.

6.31.8.4.4 Extended Self-test log descriptor entry

The content of the self-test descriptor entry is shown in Table 28.

Table 28 – Extended Self-test log descriptor entry

Byte	Descriptions
n	Content of the LBA Low register.
n+1	Content of the self-test execution status byte.
n+2	Life timestamp (least significant byte).
n+3	Life timestamp (most significant byte).
n+4	Content of the self-test failure checkpoint byte.
n+5	Failing LBA (7:0).
n+6	Failing LBA (15:8).
n+7	Failing LBA (23:16).
n+8	Failing LBA (31:24).
n+9	Failing LBA (39:32).
n+10	Failing LBA (47:40).
n+11 - *n*+25	Vendor specific.

Content of the LBA Low register shall be the content of the LBA Low register when the *n*th self-test subcommand was issued (see 6.54.5.8).
Content of the self-test execution status byte shall be the content of the self-test execution status byte when the *n*th self-test was completed (see 6.54.6.10).
Life timestamp shall contain the power-on lifetime of the device in hours when the *n*th self-test subcommand was completed.
Content of the self-test failure checkpoint byte may contain additional information about the self-test that failed.
The failing LBA shall be the LBA of the sector that caused the test to fail. If the device encountered more than one failed sector during the test, this field shall indicate the LBA of the first failed sector encountered. If the test passed or the test failed for some reason other than a failed sector, the value of this field is undefined.

6.31.8.4.5 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

6.31.8.5 Read Stream Error log

Table 29 defines the format of the Read Stream Error log. Entries are placed into the Read Stream Error log only when the SE bit is set to one in the Status register. The 512 bytes returned shall contain a maximum of 31 error entries. The Read Stream Error Count shall contain the total number of Read Stream Errors detected since the last successful completion of the READ LOG EXT command with LBA Low register set to 22h. This error count may be greater than 31, but only the most recent 31 errors are represented by entries in the log. If the Read Stream Error Count reaches the maximum value that can be represented, after the next error is detected the Read Stream Error Count shall remain at the maximum value. After successful completion of a READ LOG EXT command with the LBA Low Register set to 22h, the Read Stream Error log shall be reset to a power-on or hardware reset condition, with the

Error Log Index and Read Stream Error Count cleared to zero. The Read Stream Error log is not preserved across power cycles and hardware reset.

Table 29 – Read Stream Error log

Byte	Content
0	Structure Version
1	Error Log Index
2-3	Read Stream Error Log Count
4-15	Reserved
16-31	Read Stream Error Log Entry #1
32-47	Read Stream Error Log Entry #2
48-63	Read Stream Error Log Entry #3
64-511	Read Stream Error Log Entries #4 through #31

The Data Structure Version field shall contain a value of 02h indicating the second revision of the structure format.
The Read Stream Error Log Count field shall contain the number of uncorrected sector entries currently reportable to the host. This value may exceed 31.
The Error Log Index indicates the error log data structure representing the most recent error. Only values (31:1) are valid.
Table 30 defines the format of each entry in the Read Stream Error log.

Table 30 – Error Log Entry

Byte	7	6	5	4	3	2	1	0
0	Feature Register Contents Value (current)							
1	Feature Register Contents Value (previous)							
2	Status Register Contents Value							
3	Error Register Contents Value							
4	LBA (7:0)							
5	LBA (15:8)							
6	LBA (23:16)							
7	LBA (31:24)							
8	LBA (39:32)							
9	LBA (47:40)							
10-11	Reserved							
12	Sector Count (LSB)							
13	Sector Count (MSB)							
14	Reserved							
15	Reserved							

Byte (1:0) (Feature Register Contents Value) contains the contents of the Feature Register when the error occurred. This value shall be set to 0FFFFh for a deferred write error.
Byte 2 (Status Register Contents Value) contains the contents of the Status Register when the error occurred.
Byte 3 (Error Register Contents Value) contains the contents of the Error Register when the error occurred.
Bytes (9:4) (LBA) indicate the starting LBA of the error.
Bytes (13:12) (Sector Count) indicate the length of the error. Therefore, each entry may describe a range of sectors starting at the given address and spanning the specified number of sectors.

6.31.8.6 Write Stream Error log

Table 31 defines the format of the Write Stream Error log. Entries are placed into the Write Stream Error log only when the SE bit is set to one in the Status register. The 512 bytes returned shall contain a maximum of 31 error entries. The Write Stream Error Count shall contain the total number of Write Stream Errors detected since the last successful completion of the READ LOG EXT command with LBA Low register set to 21h. This error count may be greater than 31, but only the most recent 31 errors are represented by entries in the log. If the Write Stream Error Count reaches the maximum value that can be represented, after the next error is detected the Write Stream Error Count shall remain at the maximum value. After successful completion of a READ LOG EXT command with the LBA Low Register set to 21h, the Write Stream Error log shall be reset to a power-on or hardware reset condition, with the Error Log Index and Write Stream Error Count cleared to zero. The Write Stream Error log is not preserved across power cycles and hardware reset.

Table 31 – Write Stream Error log

Byte	Content
0	Structure Version
1	Error Log Index
2-3	Write Stream Error Log Count
4-15	Reserved
5-7	Reserved
16-31	Write Stream Error Log Entry #1
32-47	Write Stream Error Log Entry #2
48-63	Write Stream Error Log Entry #3
64-511	Write Stream Error Log Entries #4 through #31

The Data Structure Version field shall contain a value of 02h indicating the second revision of the structure format.
The Write Stream Error Log Count field shall contain the number of WRITE STREAM command entries since the last power on, since this log was last read or since a hardware reset was executed.
The Error Log Index indicates the error log data structure representing the most recent error. Only values (31:0) are valid.
Table 30 defines the format of each entry in the Error Log.

6.31.8.7 Streaming Performance log

Table 32, Table 33, Table 34 and Table 35 define the format of the log returned by the READ LOG EXT command, when the LBA Low register is 20h. This data set is referred to as the Streaming Performance Parameters log, the length of which (in sectors) is statically indicated in READ LOG EXT log address 00h (Log Directory).
The contents of Streaming Performance Parameters log may be affected by the host issuing a SET FEATURES subcommand 42h, C2h, or 43h and may also affect the Delayed LBA log.

NOTE The host should check the content of the Streaming Performance Parameters log and the Delayed LBA log after issuing SET FEATURES subcommands 42h, 43h or C2h.

The host should base its calculations on the larger of its Typical Host Interface Sector Time and the device reported Sector Time values and on the sum of the device reported Access Time values and any additional latency that only the host is aware of (e.g., host command overhead, etc).

Table 32 – Streaming Performance Parameters log

Bytes	Description
2	Stream Performance Parameters log version
2	K, Number of Regions in Sector Time Array
2	L, Number of Positions in Position Array
2	M, Number of Position-differences in Access Time Array
K×8	Sector Time Array (see Table 33)
L×8	Position Array (see Table 34)
M×4	Access Time Array (see Table 35)
Last sector remainder	Reserved

Table 33 – Sector Time Array Entry (Linearly Interpolated)

Byte	Descriptions
n-(*n*+5)	Logical Block Address of reference location (LBA(7:0)...LBA(47:40))
(*n*+6)-(*n*+7)	(IDENTIFY DEVICE data words 98 to 99)/65536 time units per sector at the reference location

Table 34 – Position Array Entry (Linearly Interpolated)

Byte	Descriptions
n-(*n*+5)	Logical Block Address of start of region (LBA(7:0)...LBA(47:40))
(*n*+6)-(*n*+7)	Position number in the range 0...32767

Table 35 – Access Time Array Entry (Linearly Interpolated)

Byte	Descriptions
n-(*n*+1)	Difference in position from last stream access to new stream access
(*n*+2)-(*n*+3)	Time that may be required to begin access at new stream access position, in (IDENTIFY DEVICE data words 88 to 89)/256 time units.

6.31.8.8 Delayed LBA log

6.31.8.8.1 General

Table 36 defines the format of each of the sectors that comprise the Delayed LBA log. The maximum size of the Delayed LBA log is vendor specific. The alternate physical location, access method or access time for a Delayed LBA are vendor specific.

If the maximum size of the Delayed LBA log is reached and an additional Delayed LBA is detected by the device, the most recent Delayed LBA shall not be added to the log.

The device may add entries to the log at any time. The device shall not remove entries from this log. The log is returned to the host ordered by timestamp, the most recently added entry is last.

The Delayed LBA log is non-volatile, it is preserved across power cycles and hardware reset.

Table 36 – Delayed LBA log

Byte	First sector	Subsequent sectors
0	Delayed LBA Log Version	Reserved
1	Reserved	Reserved
2-3	Number of Delayed LBA entries	Reserved
4-9	LBA (7:0) of 1st Delayed LBA	LBA of (63*n*+1) Delayed LBA
	LBA (15:8)	
	LBA (23:16)	
	LBA (31:24)	
	LBA (39:32)	
	LBA (47:40)	
10	Life Timestamp (7:0) of 1st Delayed LBA	Life Timestamp (7:0) of (63*n*+1) Delayed LBA
11	Life Timestamp (15:8) of 1st Delayed LBA	Life Timestamp (15:8) of (63*n*+1) Delayed LBA
12-17	LBA of 2nd Delayed LBA	LBA of (63*n*+2) Delayed LBA
18-19	Life Timestamp of 2nd Delayed LBA	Reserved
…	…	…
500-505	LBA of 63rd Delayed LBA	LBA of (63*n*+63) Delayed LBA
506-507	Life Timestamp of 63rd Delayed LBA	Life Timestamp of (63*n*+63) Delayed LBA
508-510	Reserved	Reserved
511	Data Structure Checksum	Data Structure Checksum
n is the sector number within the log. The first sector is sector 0.		

6.31.8.8.2 Delayed LBA Log Version

The value of the Delayed LBA Log Version shall be set to 01h.

6.31.8.8.3 Number of Delayed LBA entries

The Number of Delayed LBA entries shall contain the total count of Delayed LBA entries, and shall be consistent with the number of LBA entries in the Delayed LBA Log. If the maximum value for this field is reached (corresponding to the vendor-specific maximum number of sectors in the log), the count shall remain at the maximum value when additional Delayed LBA entries are added.

6.31.8.8.4 Life Timestamp

The Life Timestamp shall contain the power-on lifetime of the device, in hours, when the sector was entered into the log.

6.32 READ MULTIPLE

6.32.1 Command code

C4h

6.32.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

6.32.3 Protocol

PIO data-in (see Clause 11).

6.32.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:0)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	C4h							

Sector Count
number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.
LBA Low
starting LBA bits (7:0).
LBA Mid
starting LBA bits (15:8).
LBA High
starting LBA bits (23:16).
Device
DEV shall specify the selected device.
bits (3:0) starting LBA bits (27:24).

6.32.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.32.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

LBA Low, LBA Mid, LBA High, Device

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.32.7 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE data word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall precede a READ MULTIPLE command.

6.32.8 Description

This command reads the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 in the IDENTIFY DEVICE data. The device shall interrupt for each DRQ block transferred.

When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for *n* sectors, where *n* = remainder (sector count/ block count).

If the READ MULTIPLE command is received when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with command aborted.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set to one and the data transfer shall take place, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

6.33 READ MULTIPLE EXT

6.33.1 Command code

29h

6.33.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set.
- Use prohibited when the PACKET command feature set is implemented

6.33.3 Protocol

PIO data-in (see Clause 11).

6.33.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		29h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Sector Count Current
: number of sectors to be transferred low order, bits (7:0).

Sector Count Previous
: number of sectors to be transferred high order, bits (15:8). 0000h in the Sector Count register specifies that 65,536 sectors are to be transferred.

LBA Low Current
: LBA (7:0).

LBA Low Previous
: LBA (31:24).

LBA Mid Current
: LBA (15:8).

LBA Mid Previous
: LBA (39:32).

LBA High Current
: LBA (23:16).

LBA High Previous
: LBA (47:40).

Device
: DEV shall specify the selected device.
LBA shall be set to one

6.33.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.33.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

UNC shall be set to one if data is uncorrectable

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

LBA Low

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA Mid

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA High

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.33.7 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE data word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall precede a READ MULTIPLE EXT command.

6.33.8 Description

This command reads the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits (7:0) in word 47 in the IDENTIFY DEVICE data. The device shall interrupt for each DRQ block transferred.

When the READ MULTIPLE EXT command is issued, the Sector Count register contains the number of sectors (not the number of blocks) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for *n* sectors, where *n* = remainder (sector count/ block count).

If the READ MULTIPLE EXT command is received when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with command aborted.

Device errors encountered during READ MULTIPLE EXT commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set to one and the data transfer shall take place, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block that had a sector in error are

undefined. The host should retry the transfer as individual requests to obtain valid error information.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

6.34 READ NATIVE MAX ADDRESS

6.34.1 Command code

F8h

6.34.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set is implemented.
- Use prohibited when Removable feature set is implemented.

6.34.3 Protocol

Non-data (see Clause 11).

6.34.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	LBA	obs	DEV	na			
Command	F8h							

Device
the LBA bit shall be set to one to specify the address is an LBA.
DEV shall specify the selected device.

6.34.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	Native max address LBA (7:0)							
LBA Mid	Native max address LBA (15:8)							
LBA High	Native max address LBA (23:16)							
Device	obs	na	obs	DEV	Native max address LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

LBA Low
maximum native LBA bits (7:0) for native max address on the device.
LBA Mid
maximum native LBA bits (15:8) for native max address on the device.
LBA High
maximum native LBA bits (23:16) for native max address on device.
Device
maximum native LBA bits (27:24) for native max address on the device.
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.34.6 Error outputs

If this command is not supported the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be set to one if an Error register bit is set to one.

6.34.7 Prerequisites

DRDY set to one.

6.34.8 Description

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS command. If the 48-bit Address feature set is supported and the 48-bit native max address is greater than 268 435 455, the READ NATIVE MAX ADDRESS command shall return a maximum value of 268 435 454.

6.35 READ NATIVE MAX ADDRESS EXT

6.35.1 Command code

27h

6.35.2 Feature set

Host Protected Area feature set and 48-bit Address feature set.

- Mandatory when the Host Protected Area feature set and the 48-bit Address feature set are implemented.
- Use prohibited when Removable feature set is implemented.
- Use prohibited when PACKET Command feature set is implemented.

6.35.3 Protocol

Non-data (see Clause 11).

6.35.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Reserved							
	Previous	Reserved							
LBA Low	Current	Reserved							
	Previous	Reserved							
LBA Mid	Current	Reserved							
	Previous	Reserved							
LBA High	Current	Reserved							
	Previous	Reserved							
Device		obs	LBA	obs	DEV	na			
Command		27h							
NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.									

Device register

the LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

6.35.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Native max address LBA (7:0)							
	HOB = 1	Native max address LBA (31:24)							
LBA Mid	HOB = 0	Native max address LBA (15:8)							
	HOB = 1	Native max address LBA (39:32)							
LBA High	HOB = 0	Native max address LBA (23:16)							
	HOB = 1	Native max address LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

LBA Low

LBA (7:0) of the address of the Native max address when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the Native max address when read with Device Control register HOB bit set to one.

LBA Mid

LBA (15:8) of the address of the Native max address when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the Native max address when read with Device Control register HOB bit set to one.

LBA High

LBA (23:16) of the address of the Native max address when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the Native max address when read with Device Control register HOB bit set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.35.6 Error outputs

If this command is not supported the device shall return command aborted.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	ABRT	na	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Error register

ABRT shall be set to one if this command is not supported.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.35.7 Prerequisites

DRDY set to one.

6.35.8 Description

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS EXT command.

6.36 READ SECTOR(S)

6.36.1 Command code

20h

6.36.2 Feature set

General feature set

- Mandatory for all devices.
- PACKET Command feature set devices (see 6.36.5.2).

6.36.3 Protocol

PIO data-in (see Clause 11).

6.36.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	20h							

Sector Count
number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low
starting LBA bits (7:0).

LBA Mid
starting LBA bits (15:8).

LBA High
starting LBA bits (23:16).

Device
DEV shall specify the selected device.
bits (3:0) starting LBA bits (27:24).

6.36.5 Outputs

6.36.5.1 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.36.5.2 Outputs for PACKET Command feature set devices

In response to this command, devices that implement the PACKET Command feature set shall post command aborted and place the PACKET Command feature set signature in the LBA High and the LBA Mid register (see 5.15).

6.36.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

LBA Low, LBA Mid, LBA High, Device

shall be written with the address of first unrecoverable error.

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.36.7 Prerequisites

DRDY set to one.

6.36.8 Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High and Device registers. The device shall interrupt for each DRQ block transferred.

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition.

6.37 READ SECTOR(S) EXT

6.37.1 Command code

24h

6.37.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set.
- Use prohibited when the PACKET command feature set is implemented.

6.37.3 Protocol

PIO data-in (see Clause 11).

6.37.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		24h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Sector Count Current
number of sectors to be transferred low order, bits (7:0).
Sector Count Previous
number of sectors to be transferred high order, bits (15:8).
LBA Low Current
LBA (7:0).
LBA Low Previous
LBA (31:24).
LBA Mid Current
LBA (15:8).
LBA Mid Previous
LBA (39:32).
LBA High Current
LBA (23:16).
LBA High Previous
LBA (47:40).
Device
the LBA bit shall be set to one to specify the address is an LBA.
DEV shall specify the selected device.

6.37.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.37.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register
UNC shall be set to one if data is uncorrectable
MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.
IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.
MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.
ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.
NM shall be set to one if no media is present in a removable media device.
LBA Low
LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.
LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.
LBA Mid
LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.
LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.
LBA High
LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.
LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.37.7 Prerequisites

DRDY set to one.

6.37.8 Description

This command reads from 1 to 65 536 sectors as specified in the Sector Count register. A sector count of 0000h requests 65 536 sectors. The transfer shall begin at the sector specified in the LBA Low, LBA Mid, and LBA High registers. The device shall interrupt for each DRQ block transferred.
The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition.

6.38 READ STREAM DMA EXT

6.38.1 Command code

2Ah

6.38.2 Feature set

– Mandatory if the Streaming feature set is implemented.
– Use prohibited if PACKET Command feature set is implemented.

6.38.3 Protocol

DMA (see Clause 11 of ISO/IEC 14739-2)

6.38.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	URG	RC	NS	HSE	r	Stream ID		
	Previous	Command Completion Time Limit (7:0)							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		2Ah							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Features register current

URG specifies an urgent transfer request. The Urgent bit specifies that the command should be completed in the minimum possible time by the device and shall be completed within the specified Command Completion Time Limit. This bit is optional (see 6.17.42).

RC specifies Read Continuous mode enabled. If the Read Continuous bit is set to one, the device shall not stop execution of the command due to errors.

If thr RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC, UNC, IDNF or ABRT, reported in the error log.

If the RC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one.

In all cases, the device shall attempt to transfer the amount of data requested within the Comand Completion Time Limit even if some data transferred is in error.

NS (Not Sequential) may be set to one if the next read stream command with the same Stream ID may not be sequential in LBA space. Any read of the device media or internal device buffer management as a result of the state of the NS bit is device vendor specific.

HSE (Handle Streaming Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.

r specifies reserved.

Stream ID specifies the stream to be read. The device shall operate according to the Stream ID set by the READ STREAM command. Any read of the device media or internal device buffer management as a result of the Stream ID is device vendor specific.

Features register previous

The time allowed for the current command's completion is calculated as follows:

Command Completion Time Limit = (content of the Features register

Previous) × (IDENTIFY DEVICE data words 98 to 99) µs

If the value is zero, the device shall use the Default Command Completion Time Limit supplied with a previous CONFIGURE STREAM command for this Stream ID. If the Default Command Completion Time Limit is zero, or no previous Configure Stream command was defined for this Stream ID, the result is vendor specific. The time is measured from the write of the command register to the final INTRQ for command completion.

Sector Count Current
number of sectors to be transferred low order, bits (7:0).

Sector Count Previous
number of sectors to be transferred high order, bits (15:8).

LBA Low Current
LBA (7:0).

LBA Low Previous
LBA (31:24).

LBA Mid Current
LBA (15:8).

LBA Mid Previous
LBA (39:32).

LBA High Current
LBA (23:16).

LBA High Previous
LBA (47:40).

Device
LBA shall be set to one.
DEV shall specify the selected device.

6.38.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	SE	na	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Device/Head register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
SE (Stream Error) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.38.6 Error outputs

If the RC bit is cleared to zero, the content of the registers shal be as shown below. If the RC bit is set to one, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the content of the Error register shown below shall be placed in the error log.

Register		7	6	5	4	3	2	1	0
Error		ICRC	UNC	MC	IDNF	MCR	ABRT	NM	CCTO
Sector Count	HOB = 0	Length of Stream Error (7:0)							
	HOB = 1	Length of Stream Error (15:8)							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	SE	DWE	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Error register

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

CCTO (Command Completion Time Limit Out) bit shall be set to one if a Command Completion Time Limit Out error has occurred.

Sector Count Current

bits (7:0) number of contiguous sectors containing potentially bad data, beginning with the LBA of the first sector with an uncorrectable error.

Sector Count Previous

bits (15:8) of the number of contiguous sectors containing potentially bad data, starting at the address of the first uncorrectable error

LBA Low Current

bits (7:0) of the address of the first uncorrectable error when read with Device Control register HOB cleared to zero.

LBA Low Previous

bits (31:24) of the address of the first uncorrectable error when read with Device Control register HOB set to one.

LBA Mid Current

bits (15:8) of the address of the first uncorrectable error when read with Device Control register HOB cleared to zero.

LBA Mid Previous
bits (39:32) of the address of the first uncorrectable error when read with Device Control register HOB set to one.

LBA High Current
bits (23:16) of the address of the first uncorrectable error when read with Device Control register HOB cleared to zero.

LBA High Current
bits (47:40) of the address of the first uncorrectable error when read with Device Control register HOB set to one.

Device register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
SE (Stream Error) shall be set to one if an error has occurred during the execution of the command and the RC bit is set to one. In this case the LBA returned in the Sector Number registers shall be the address of the first sector in error, and the Sector Count registers shall contain the number of consecutive sectors that may contain errors. If the RC bit is set to one when the command is issued and an ICRC, UNC, IDNF, ABRT, or CCTO error occurs, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the bits that would normally be set in the Error register shall be set in the error log.
DWE (Deferred Write Error) shall be set to one if an error was detected in a deferred write to the media for a previous WRITE STREAM DMA EXT or WRITE STREAM EXT command. This error is from a previously issued command. If DWE is set to one, the location of the deferred error is only reported in the Write Stream error log.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one and the RC bit is cleared to zero. If the RC bit is set to one when the command is issued and an ICRC UNC, IDNF, ABRT or CCTO error occurs, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the bits that would normally be set in the Error register shall be set in the error log.

6.38.7 Prerequisites

DRDY set to one and BSY cleared to zero.

6.38.8 Description

The command reads from 1 to 65 536 sectors as specified in the Sector Count register. A value of 0000h in the Sector Count register requests 65 536 sectors.
The RC bit indicates that the drive operate in a continuous read mode for the READ STREAM command. When RC is cleared to zero the drive shall operate in normal Streaming read mode. When the Read Continuous mode is enabled, the device shall transfer data of the requested length without setting the ERR bit to one. The SE bit shall be set to one if the data transferred includes errors. The data may be erroneous in this case. If an error is encountered, it may be necessary for the device to pad the data being transferred in order to fulfill the host's requested transfer size. The implementation of the padding is vendor specific.
If the Read Continuous bit is set to one, the device shall not stop execution of the command due to errors. If thr RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, ICRC, UNC, IDNF or ABRT, reported in the error log. If the RC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one. In all cases, the device shall attempt to transfer the amount of data requested within the Comand Completion Time Limit even if some data transferred is in error.

6.39 READ STREAM EXT

6.39.1 Command code

2Bh

6.39.2 Feature set

– Mandatory if the Streaming feature set is implemented.
– Use prohibited if PACKET Command feature set is implemented.

6.39.3 Protocol

PIO data-in (see Clause 11)

6.39.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	URG	RC	NS	HSE	r	Stream ID		
	Previous	Command Completion Time Limit (7:0)							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		2Bh							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Features register current

URG specifies an urgent transfer request. The Urgent bit specifies that the command should be completed in the minimum possible time by the device and within the specified Command Completion Time Limit. This bit is optional (see 6.17.42).

RC specifies Read Continuous mode enabled. If the Read Continuous bit is set to one,the device shall not stop execution of the command due to errors.

If the RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, UNC, IDNF, or ABRT, reported in the error log.

If the RC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one.

In all cases, the device shall attempt to transfer the amount of data requested within the Comand Completion Time Limit even if some data transferred is in error.

NS (Not Sequential) may be set to one if the next read stream command with the same Stream ID may not be sequential in LBA space. Any read of the device media or internal device buffer management as a result of the state of the NS bit is device vendor specific.

HSE (Handle Streaming Error) specifies that this command starts at the LBA of the last reported error for this stream, so the device may attempt to continue its corresponding error recovery sequence where it left off earlier.

r indicates reserved.

Stream ID specifies the stream being read. The device shall operate according to the Stream ID set by the READ STREAM command. Any read of the device media or internal device buffer management as a result of the Stream ID is device vendor specific.

Features register previous

The additional time allowed for the current command's completion is calculated as follows:

Command Completion Time Limit = (content of the Features register Previous) × (IDENTIFY DEVICE data words 98 to 99) µs

If the value is zero, the device shall use the Default Command Completion Time Limit supplied with a previous CONFIGURE STREAM command for this Stream ID. If the Default Command Completion Time Limit is zero, or no previous Configure Stream command was defined for this Stream ID, the result is vendor specific. The time is measured from the write of the command register to command completion.

Sector Count Current

number of sectors to be transferred low order, bits (7:0).

Sector Count Previous -

number of sectors to be transferred high order, bits (15:8).

LBA Low Current

LBA (7:0).

LBA Low Previous

LBA (31:24).

LBA Mid Current

LBA (15:8).

LBA Mid Previous

LBA (39:32).

LBA High Current

LBA (23:16).

LBA High Previous

LBA (47:40).

Device

the LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

6.39.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	SE	na	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Device/Head register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
SE (Stream Error) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.39.6 Error outputs

If the RC bit is cleared to zero, the content of the registers shal be as shown below. If the RC bit is set to one, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the content of the Error register shown below shall be placed in the error log.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	CCTO
Sector Count	HOB = 0	Length of Stream Error (7:0)							
	HOB = 1	Length of Stream Error (15:8)							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	SE	DWE	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register
UNC shall be set to one if data is uncorrectable.
MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.
IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.
MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.
ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.
NM shall be set to one if no media is present in a removable media device.
CCTO (Command Completion Time Limit Out) bit shall be set to one if a Command Completion Time Limit Out error has occurred.
Sector Count Current
bits (7:0) number of contiguous sectors containing potentially bad data, beginning with the LBA of the first sector with an uncorrectable error.
Sector Count Previous
bits (15:8) of the number of contiguous sectors containing potentially bad data, starting at the address of the first uncorrectable error
LBA Low Current

bits (7:0) of the address of the first uncorrectable error when read with Device Control register HOB cleared to zero.

LBA Low Previous
bits (31:24) of the address of the first uncorrectable error when read with Device Control register HOB set to one.

LBA Mid Current
bits (15:8) of the address of the first uncorrectable error when read with Device Control register HOB cleared to zero.

LBA Mid Previous
bits (39:32) of the address of the first uncorrectable error when read with Device Control register HOB set to one.

LBA High Current
bits (23:16) of the address of the first uncorrectable error when read with Device Control register HOB cleared to zero.

LBA High Current
bits (47:40) of the address of the first uncorrectable error when read with Device Control register HOB set to one.

Device register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
SE (Stream Error) shall be set to one if an error has occurred during the execution of the command and the RC bit is set to one. In this case the LBA returned in the Sector Number registers shall be the address of the first sector in error, and the Sector Count registers shall contain the number of consecutive sectors that may contain errors. If the RC bit is set to one when the command is issued and a UNC, IDNF, ABRT or CCTO error occurs, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the bits that would normally be set in the Error register shall be set in the error log.
DWE (Deferred Write Error) shall be set to one if an error was detected in a deferred write to the media for a previous WRITE STREAM DMA EXT or WRITE STREAM EXT command. This error is from a previously issued command. If DWE is set to one, the location of the deferred error is only reported in the Write Stream error log.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one and RC is cleared to zero. If the RC bit is set to one when the command is issued and a UNC, IDNF, ABRT or CCTO error occurs, the SE bit shall be set to one, the ERR bit shall be cleared to zero, and the bits that would normally be set in the Error register shall be set in the error log.

6.39.7 Prerequisites

DRDY set to one and BSY cleared to zero.

6.39.8 Description

The command reads from 1 to 65 536 sectors as specified in the Sector Count register. A sector count of value 0000h requests 65 536 sectors. The transfer shall begin at the sector specified in the Sector Number register.

The RC bit specifies that the drive operate in a continuous read mode for the READ STREAM command. When RC is cleared to zero the drive shall operate in normal Streaming read mode. When the Read Continuous mode is enabled, the device shall transfer data of the requested length without setting the error bit. The SE bit shall be set to one if the data transferred includes errors. The data may be erroneous in this case. If an error is encountered, it may be necessary for the device to pad the data being transferred in order to fulfill the host's requested transfer size. The implementation of the padding is vendor specific.

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition.

If the Read Continuous bit is set to one,the device shall not stop execution of the command due to errors. If thr RC bit is set to one and errors occur in reading or transfer of the data, the device shall continue to transfer the amount of data requested and then provide ending status

with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and the type of error, UNC, IDNF, or ABRT, reported in the error log. If the RC bit is set to one and the Command Completion Time Limit expires, the device shall stop execution of the command and provide ending status with the BSY bit cleared to zero, the SE bit set to one, the ERR bit cleared to zero, and report the fact that the Command Completion Time Limit expired by setting the CCTO bit in the error log to one. In all cases, the device shall attempt to transfer the amount of data requested within the Comand Completion Time Limit even if some data transferred is in error.

6.40 READ VERIFY SECTOR(S)

6.40.1 Command code

40h

6.40.2 Feature set

General feature set

- Mandatory for all devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

6.40.3 Protocol

Non-data (see Clause 11).

6.40.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	LBA	obs	DEV	LBA (27:24)			
Command	40h							

Sector Count
: number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low
: starting LBA bits (7:0).

LBA Mid
: starting LBA bits (15:8).

LBA High
: starting LBA bits (23:16).

Device
: the LBA bit shall be set to one to specify the address is an LBA.
DEV shall specify the selected device.
bits (3:0) starting LBA bits (27:24).

6.40.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.40.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
UNC shall be set to one if data is uncorrectable.
MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.
IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.
MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.
ABRT shall be set to one if this command is not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.
NM shall be set to one if no media is present in a removable media device.
LBA Low, LBA Mid, LBA High, Device
shall be written with the address of first unrecoverable error.
DEV shall indicate the selected device.
Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.40.7 Prerequisites

DRDY set to one.

6.40.8 Description

This command is identical to the READ SECTOR(S) command, except that the device shall have read the data from the media, the DRQ bit is never set to one, and no data is transferred to the host.

6.41 READ VERIFY SECTOR(S) EXT

6.41.1 Command code

42h

6.41.2 Feature set

48-bit Address feature set

- Mandatory for all devices implementing the 48-bit Address feature set.
- Use prohibited when the PACKET command feature set is implemented.

6.41.3 Protocol

Non-data (see Clause 11).

6.41.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Sector count (7:0)							
	Previous	Sector count (15:8)							
LBA Low	Current	LBA (7:0)							
	Previous	LBA (31:24)							
LBA Mid	Current	LBA (15:8)							
	Previous	LBA (39:32)							
LBA High	Current	LBA (23:16)							
	Previous	LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		42h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Sector Count Current
number of sectors to be transferred low order, bits (7:0).
Sector Count Previous
number of sectors to be transferred high order, bits (15:8).
LBA Low Current
LBA (7:0).
LBA Low Previous
LBA (31:24).

LBA Mid Current
LBA (15:8).
LBA Mid Previous
LBA (39:32).
LBA High Current
LBA (23:16).
LBA High Previous
LBA (47:40).
Device
the LBA bit shall be set to one to specify the address is an LBA.
DEV shall specify the selected device.

6.41.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.41.6 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Register		7	6	5	4	3	2	1	0
Error		na	UNC	MC	IDNF	MCR	ABRT	NM	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	LBA (7:0)							
	HOB = 1	LBA (31:24)							
LBA Mid	HOB = 0	LBA (15:8)							
	HOB = 1	LBA (39:32)							
LBA High	HOB = 0	LBA (23:16)							
	HOB = 1	LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR

NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.

Error register

UNC shall be set to one if data is uncorrectable.

MC shall be set to one if the media in a removable media device changed since the issuance of the last command. The device shall clear the device internal media change detected state.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

MCR shall be set to one if a media change request has been detected by a removable media device. This bit is only cleared by a GET MEDIA STATUS or a media access command.

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one of an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

NM shall be set to one if no media is present in a removable media device.

LBA Low

LBA (7:0) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA Mid

LBA (15:8) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

LBA High

LBA (23:16) of the address of the first unrecoverable error when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the first unrecoverable error when read with Device Control register HOB bit set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.41.7 Prerequisites

DRDY set to one.

6.41.8 Description

This command is identical to the READ SECTOR(S) EXT command, except that the device shall have read the data from the media, the DRQ bit is never set to one, and no data is transferred to the host.

6.42 SECURITY DISABLE PASSWORD

6.42.1 Command code

F6h

6.42.2 Feature set

Security Mode feature set.

– Mandatory when the Security Mode feature set is implemented.

6.42.3 Protocol

PIO data-out (see Clause 11).

6.42.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F6h							

Device register

DEV shall specify the selected device.

6.42.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.42.6 Error outputs

The device shall return command aborted if the command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.42.7 Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

6.42.8 Description

The SECURITY DISABLE PASSWORD command transfers 512 bytes of data from the host. Table 37 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password is set (see 4.7).

Table 37 – Security password content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare User password 1=compare Master password
	Bit (15:1)	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

6.43 SECURITY ERASE PREPARE

6.43.1 Command code

F3h

6.43.2 Feature set

Security Mode feature set.

– Mandatory when the Security Mode feature set is implemented.

6.43.3 Protocol

Non-data (see Clause 11).

6.43.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F3h							

Device register

DEV shall specify the selected device.

6.43.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.43.6 Error outputs

The device shall return command aborted if the command is not supported or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBAHigh	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported or device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

NOTE In a previous revision of this standard, there were conflicting descriptions of the handling of this command when in the Frozen mode.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.43.7 Prerequisites

DRDY set to one.

6.43.8 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

6.44 SECURITY ERASE UNIT

6.44.1 Command code

F4h

6.44.2 Feature set

Security Mode feature set.

– Mandatory when the Security Mode feature set is implemented.

6.44.3 Protocol

PIO data-out (see Clause 11).

6.44.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	F4h							

Device register
DEV shall specify the selected device.

6.44.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.44.6 Error outputs

The device shall return command aborted if the command is not supported, the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBAHigh	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported, device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.44.7 Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

6.44.8 Description

This command transfers 512 bytes of data from the host. Table 38 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase mode is specified, the device shall write predetermined data patterns to all user data areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later when a new User password is set.

Table 38 – SECURITY ERASE UNIT password

Word	Content		
0	Control word		
	Bit 0	Identifier	0=Compare User password
			1=Compare Master password
	Bit 1	Erase mode	0=Normal Erase
			1=Enhanced Erase
	Bit (15:2)	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

6.45 SECURITY FREEZE LOCK

6.45.1 Command code

F5h

6.45.2 Feature set

Security Mode feature set.

– Mandatory when the Security Mode feature set is implemented.

6.45.3 Protocol

Non-data (see Clause 11).

6.45.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F5h							

Device register

DEV shall specify the selected device.

6.45.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.45.6 Error outputs

The device shall return command aborted if the command is not supported, or the device is in Locked mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported or device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.45.7 Prerequisites

DRDY set to one.

6.45.8 Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device is in Frozen mode, the command executes and the device shall remain in Frozen mode.

Commands disabled by SECURITY FREEZE LOCK are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

6.46 SECURITY SET PASSWORD

6.46.1 Command code

F1h

6.46.2 Feature set

Security Mode feature set.

- Mandatory when the Security Mode feature set is implemented.

6.46.3 Protocol

PIO data-out (see Clause 11).

6.46.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F1h							

Device register
DEV shall specify the selected device.

6.46.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.46.6 Error outputs

The device shall return command aborted if the command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported, if device is in Frozen mode, or if device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.46.7 Prerequisites

DRDY set to one.

6.46.8 Description

This command transfers 512 bytes of data from the host. Table 39 defines the content of this information. The data transferred controls the function of this command. Table 40 defines the interaction of the identifier and security level bits.
The revision code field shall be returned in the IDENTIFY DEVICE data word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Table 39 – SECURITY SET PASSWORD data content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set User password 1=set Master password
	Bits (7:1)	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits (15:9)	Reserved	
1-16	Password (32 bytes)		
17	Master Password Revision Code (valid if word 0 bit 0 = 1)		
18-255	Reserved		

Table 40 – Identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be used to unlock the device.
Master	High or maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

6.47 SECURITY UNLOCK

6.47.1 Command code

F2h

6.47.2 Feature set

Security Mode feature set.

– Mandatory when the Security Mode feature set is implemented.

6.47.3 Protocol

PIO data-out (see Clause 11).

6.47.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F2h							

Device register

DEV shall specify the selected device.

6.47.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.47.6 Error outputs

The device shall return command aborted if the command is not supported or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported or if device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.47.7 Prerequisites

DRDY set to one.

6.47.8 Description

This command transfers 512 bytes of data from the host. Table 37 defines the content of this information.

If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password.

If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall be decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

6.48 SERVICE

6.48.1 Command code

A2h

6.48.2 Feature set

Overlap and Queued feature sets
Mandatory when the Overlapped feature set is implemented.

6.48.3 Protocol

PACKET or READ/WRITE DMA QUEUED (see Clause 11).

6.48.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Command	A2h							

Device register
DEV shall specify the selected device.

6.48.5 Outputs

Outputs as a result of a SERVICE command are described in the command description for the command for which SERVICE is being requested.

6.48.6 Prerequisites

The device shall have performed a bus release for a previous overlap PACKET, READ DMA QUEUED, READ DMA QUEUED EXT, WRITE DMA QUEUED, or WRITE DMA QUEUED EXT command and shall have set the SERV bit to one to request the SERVICE command be issued to continue data transfer and/or provide command status (See 6.49.21).

6.48.7 Description

The SERVICE command is used to provide data transfer and/or status of a command that was previously bus released.

6.49 SET FEATURES

6.49.1 Command code

EFh

6.49.2 Feature set

General feature set

- Mandatory for all devices.
- Set transfer mode subcommand is mandatory.
- Enable/disable write cache subcommands are mandatory when a write cache is implemented.
- Enable/disable Media Status Notification sub commands are mandatory if the Removable Media feature set is implemented.
- All other subcommands are optional.

6.49.3 Protocol

Non-data (see Clause 11 of ISO/IEC 24739-2).

6.49.4 Inputs

Table 41 defines the value of the subcommand in the Feature register. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Subcommand specific							
LBA Low	Subcommand specific							
LBA Mid	Subcommand specific							
LBA High	Subcommand specific							
Device	obs	na	obs	DEV	na	na	na	na
Command	EFh							

Device register
DEV shall specify the selected device.

6.49.5 Normal outputs

See the subcommand descriptions.

6.49.6 Error outputs

If any subcommand input value is not supported or is invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if this subcommand is not supported or if the value is invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.49.7 Prerequisites

DRDY shall be set to one.

6.49.8 Description

This command is used by the host to establish parameters that affect the execution of certain device features. Table 41 defines these features.
At power-on, or after a hardware reset, the default settings of the functions specified by the subcommands are vendor specific.

Table 41 – SET FEATURES register definitions

Value (See note)	
01h	Enable 8-bit PIO transfer mode (CFA feature set only)
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register. Table 42 defines values.
04h	Obsolete
05h	Enable advanced power management
06h	Enable Power-Up In Standby feature set.
07h	Power-Up In Standby feature set device spin-up.
09h	Reserved for Address offset reserved area boot method technical report.
0Ah	Enable CFA power mode 1
10h	Reserved for Serial ATA
20h	Reserved for technical report
21h	Reserved for technical report
31h	Disable Media Status Notification
33h	Obsolete
42h	Enable Automatic Acoustic Management feature set
43h	Set Maximum Host Interface Sector Times
44h	Obsolete
54h	Obsolete
55h	Disable read look-ahead feature
5Dh	Enable release interrupt
5Eh	Enable SERVICE interrupt
66h	Disable reverting to power-on defaults
77h	Obsolete
81h	Disable 8-bit PIO transfer mode (CFA feature set only)
82h	Disable write cache
84h	Obsolete
85h	Disable advanced power management
86h	Disable Power-Up In Standby feature set.
88h	Obsolete
89h	Reserved for Address offset reserved area boot method technical report
8Ah	Disable CFA power mode 1
90h	Reserved for Serial ATA
95h	Enable Media Status Notification
99h	Obsolete
9Ah	Obsolete
Aah	Enable read look-ahead feature
Abh	Obsolete

BBh	Obsolete
C2h	Disable Automatic Acoustic Management feature set
CCh	Enable reverting to power-on defaults
DDh	Disable release interrupt
Deh	Disable SERVICE interrupt
E0h	Obsolete
F0h-FFh	Reserved for assignment by the CompactFlash™ Association
NOTE All values not shown are reserved for future definition.	

6.49.9 Enable/disable 8-bit PIO data transfer

Devices implementing the CFA feature set shall support 8-bit PIO data transfers. Devices not implementing the CFA feature set shall not support 8-bit PIO data transfers. When 8-bit PIO data transfer is enabled the Data register is 8-bits wide using only DD7 to DD0.

6.49.10 Enable/disable write cache

Subcommand codes 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before command completion (See 6.14). This subcommand does not apply to commands that have a Flush to Disk bit.

6.49.11 Set transfer mode

A host selects the transfer mechanism by Set Transfer Mode, subcommand code 03h and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. The host may change the selected modes by the SET FEATURES command.

Table 42 – Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode
Retired	00010b	na
Multiword DMA mode	00100b	mode
Ultra DMA mode	01000b	mode
Reserved	10000b	na
mode = transfer mode number		

If a device supports this standard, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000000b”, the device shall set the default PIO mode. If the value is “00000001b” and the device supports disabling of IORDY, then the device shall set the default PIO mode and disable IORDY. A device shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.
Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.
A device shall support all Multiword DMA modes below the highest mode supported, e.g., if Multiword DMA mode 1 is supported Multiword DMA mode 0 shall be supported.
A device shall support all Ultra DMA modes below the highest mode supported, e.g., if Ultra DMA mode 1 is supported Ultra DMA mode 0 shall be supported.

If an Ultra DMA mode is enabled any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device.
For systems using a cable assembly, the host shall detect that an 80-conductor cable assembly is connecting the host with the device(s) before enabling any Ultra DMA mode greater than 2 in the device(s) (see ISO/IEC 24739-2, Annex A).

6.49.12 Enable/disable advanced power management

Subcommand code 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a SET FEATURES command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table 43 shows these values.

Table 43 – Advanced power management levels

Level	Sector Count value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.
Subcommand code 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement SET FEATURES subcommand 05h.

6.49.13 Enable/disable Power-Up In Standby feature set

Subcommand code 06h enables the Power-Up In Standby feature set. When this feature set is enabled, the device shall power-up into Standby mode, i.e., the device shall be ready to receive commands but shall not spinup (see 4.12). Having been enabled, this feature shall remain enabled through power-down, hardware reset and software rest.
Subcommand code 86h disables the Power-Up In Standby feature set. When this feature set is disabled, the device shall power-up into Active mode. The factory default for this feature set shall be disabled.

6.49.14 Enable/disable CFA power mode 1

Subcommand code 0Ah enables CFA Power Mode 1. CFA devices may consume up to 500 mA maximum average RMS current for either 3.3 V or 5 V operation in Power Mode 1. CFA devices revert to Power Mode 1 on hardware or power-on reset. CFA devices revert to Power Mode 1 on software reset except when Set Features disable reverting to power-on defaults is set (see 6.17.67). Enabling CFA Power Mode 1 does not spin up rotating media devices.
Subcommand 8Ah disables CFA Power Mode 1, placing the device to CFA Power Mode 0. CFA devices may consume up to 75 mA maximum average RMS current for 3.3 V or 100 mA maximum average RMS current for 5 V operation in Power Mode 0.
A device in Power Mode 0 shall accept the following commands:

- IDENTIFY DEVICE
- SET FEATURES (function codes 0Ah and 8Ah)
- STANDBY
- STANDBY IMMEDIATE

- SLEEP
- CHECK POWER MODE
- EXECUTE DEVICE DIAGNOSTICS
- CFA REQUEST EXTENDED ERROR

A device in Power Mode 0 may accept any command that the device is capable of executing within the Power Mode 0 current restrictions. Commands that require more current than specified for Power Mode 0 shall be rejected with an abort error.

6.49.15 Power-Up In Standby feature set device spin-up

Subcommand code 07h shall cause a device that has powered-up into Standby to go to the Active state (See 4.12 and Figure 4).

6.49.16 Enable/disable Media Status Notification

Subcommand code 31h disables Media Status Notification and leaves the media in an unlocked state. If Media Status Notification is disabled when this subcommand is received, the subcommand has no effect.
Subcommand code 95h enables Media Status Notification and clears any previous media lock state. This subcommand returns the device capabilities for media eject, media lock, previous state of Media Status Notification and the current version of Media Status Notification supported in the LBA Mid and LBA High registers as described below.

Register	7	6	5	4	3	2	1	0
LBA Mid	VER							
LBA High	Reserved					PEJ	LOCK	PENA

LBA Mid register

VER shall contain the Media Status Notification version supported by the device (currently 0x00h).

LBA High register

PENA shall be set to one if Media Status Notification was enabled prior to the receipt of this command.

LOCK shall be set to one if the device is capable of locking the media preventing manual ejection.

PEJ shall be set to one if the device has a power eject mechanism that is capable of physically ejecting the media when a MEDIA EJECT command is sent to the device. This bit shall be set to zero if the device only unlocks the media when the device receives a MEDIA EJECT command.

6.49.17 Enable/disable Automatic Acoustic Management

Subcommand code 42h allows the host to enable the Automatic Acoustic Management feature set. To enable the Automatic Acoustic Management feature set, the host writes the Sector Count register with the requested automatic acoustic management level and executes a SET FEATURES command with subcommand code 42h. The acoustic management level is selected on a scale from 01h to FEh. Table 44 shows the acoustic management level values.
Enabling or disabling of the Automatic Acoustic Management feature set, and the current automatic acoustic management level setting shall be preserved by the device across all forms of reset, i.e., power-on, hardware and software resets.

Table 44 – Automatic acoustic management levels

Level	Sector Count value
Reserved	FFh
Maximum performance	FEh
Intermediate acoustic management levels	81h-FDh
Minimum acoustic emanation level	80h
Retired	01h-7Fh
Vendor specific	00h

Device performance may increase with increasing acoustic management levels. Device power consumption may decrease with decreasing acoustic management levels. The acoustic management levels may contain discrete bands. For example, a device may implement one acoustic management method from 80h to BFh and a higher performance, higher acoustic management method from level C0h to FEh.
Upon successful completion of this SET FEATURES subcommand, IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data word 94, bits (7:0) shall be updated by the device. If the command is aborted by the device, the previous automatic acoustic management state shall be retained.
Subcommand code C2h disables the Automatic Acoustic Management feature set. Devices that implement SET FEATURES subcommand 42h are not required to implement subcommand C2h. If device successfully completes execution of this subcommand, then the acoustic behavior of the device shall be vendor-specific, and the device shall return zeros in bits (7:0) of word 94 and bit 9 of word 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data words.
Upon completion of SET FEATURES subcommands 42h and C2h, the device may update words 96 to 97 and word 104 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data words, and the contents of the Stream Performance Parameters Log in the READ LOG EXT command.

6.49.18 Set maximum Host Interface Sector Times

Subcommand code 43h allows the host to inform the device of a host interface rate limitation. This information shall be used by the device to meet the Command Completion Time Limits of the commands of the streaming feature set. To inform the device of a host interface rate limitation, the host writes the LSB and MSB value of its Typical PIO Host Interface Sector Time to the Sector Count and LBA Low registers and writes the LSB and MSB value of its Typical DMA Host Interface Sector Time to the LBA Mid and LBA High registers. The Typical Host Interface Sector Times have the same units as IDENTITY DEVICE data word 96 for DMA and word 104 for PIO. A value of zero indicates that the host interface shall be capable of transferring data at the maximum rate allowed by the selected transfer mode. The Typical PIO Mode Host Interface Sector Time includes the host's interrupt service time.
Upon completion of SET FEATURES subcommand 43h, the device may adjust IDENTIFY DEVICE data words 96 to 97 and the contents of the Stream Performance Parameters log in the READ LOG EXT command to allow for the specified host interface sector time.

Register	7	6	5	4	3	2	1	0
Sector Count	Typical PIO Mode Host Interface Sector Time (7:0)							
LBA Low	Typical PIO Mode Host Interface Sector Time (15:8)							
LBA Mid	Typical DMA Mode Host Interface Sector Time (7:0)							
LBA High	Typical DMA Mode Host Interface Sector Time (15:8)							

6.49.19 Enable/disable read look-ahead

Subcommand codes AAh and 55h allow the host to request the device to enable or disable read look-ahead. Error recovery performed by the device is vendor specific.

6.49.20 Enable/disable release interrupt

Subcommand codes 5Dh and DDh allow a host to enable or disable the asserting of Interrupt Pending when a device releases the bus for an overlapped PACKET command.

6.49.21 Enable/disable SERVICE interrupt

Subcommand codes 5Eh and DEh allow a host to enable or disable the asserting of an Interrupt Pending when DRQ is set to one in response to a SERVICE command.

6.49.22 Enable/disable reverting to defaults

Subcommand codes CCh and 66h allow the host to enable or disable the device from reverting to power-on default values. A setting of 66h allows settings that may have been modified since power-on to remain at the same setting after a software reset.

6.50 SET MAX

6.50.1 General

Individual SET MAX commands are identified by the value placed in the Features register. Table 45 shows these Features register values.

Table 45 – SET MAX Features register values

Value	Command
00h	Obsolete
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
05h-FFh	Reserved

6.50.2 SET MAX ADDRESS

6.50.2.1 Command code

F9h (see 6.50.2.7).

6.50.2.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set is implemented.
- Use prohibited when the Removable feature set is implemented.

6.50.2.3 Protocol

Non-data (see Clause 11).

6.50.2.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							V V
LBA Low	SET MAX LBA (7:0)							
LBA Mid	SET MAX LBA (15:8)							
LBA High	SET MAX LBA (23:16)							
Device	obs	LBA	obs	DEV	SET MAX LBA (27:24)			
Command	F9h							

Sector Count

V V (Value volatile). If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

LBA Low

contains LBA bits (7:0) value to be set.

LBA Mid
contains LBA bits (15:8) value to be set.

LBA High
contains the LBA bits (23:16) value to be set.

Device
the LBA bit shall be set to one to specify the address is an LBA.
DEV shall specify the selected device.
Bits (3:0) contain the LBA bits (27:24) value to be set.

6.50.2.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	LBA (7:0)							
LBA Mid	LBA (15:8)							
LBA High	LBA (23:16)							
Device	obs	na	obs	DEV	LBA (27:24)			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

LBA Low
LBA bits (7:0) set on the device.

LBA Mid
LBA bits (15:8) set on the device.

LBA High
LBA bits (23:16) set on device.

Device
DEV shall indicate the selected device.
LBA bits (27:24) set on the device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.50.2.6 Error outputs

If this command is not supported, the maximum value to be set exceeds the capacity of the device, a host protected area has been established by a SET MAX ADDRESS EXT command, or the device is in the Set_Max_Locked or Set_Max_Frozen state, then the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported, maximum value requested exceeds the device capacity, a host protected area has been established by a SET MAX ADDRESS EXT command, the device is in the Set_Max_Locked or

Set_Max_Frozen state or the command is not immediately preceded by a READ NATIVE MAX ADDRESS command. ABRT may be set to one if the device is not able to complete the action requested by the command.

IDNF shall be set to one if the command was the second non-volatile SET MAX ADDRESS command after power-on or hardware reset.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

ERR shall be set to one if an Error register bit is set to one.

6.50.2.7 Prerequisites

DRDY set to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.

6.50.2.8 Description

After successful command completion, all read and write access attempts to addresses greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error. IDENTIFY DEVICE data words 60 to 61 shall reflect the maximum address set with this command.

If the 48-bit Address feature set is supported, the value placed in IDENTIFY DEVICE data words 100 to 103 shall be the same as the value placed in words 60 to 61.

Hosts shall not issue more than one non-volatile SET MAX ADDRESS or SET MAX ADDRESS EXT command after a power-on or hardware reset. Devices should report an IDNF error upon receiving a second non-volatile SET MAX ADDRESS command after a power-on or hardware reset.

The contents of IDENTIFY DEVICE data words and the max address shall not be changed if a SET MAX ADDRESS command fails.

After a successful SET MAX ADDRESS command using a new maximum LBA the content of all IDENTIFY DEVICE data words shall comply with 4.2.2 and the content of words 61 to 60 shall be equal to the new Maximum LBA +1.

6.50.3 SET MAX SET PASSWORD

6.50.3.1 Command code

F9h with the content of the Features register equal to 01h.

6.50.3.2 Feature set

Host Protected Area feature set.

– Mandatory when the Host Protected Area feature set security extensions are implemented.
– Use prohibited when the Removable feature set is implemented.

6.50.3.3 Protocol

PIO data-out (see Clause 11).

6.50.3.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	01h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F9h							

Device
DEV shall specify the selected device.

6.50.3.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.50.3.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported or the device is in the Set_Max_Locked or Set_Max_Frozen state. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be set to one if an Error register bit is set to one.

6.50.3.7 Prerequisites

DRDY set to one. This command shall not be immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.

6.50.3.8 Description

This command requests a transfer of a single sector of data from the host. Table 46 defines the content of this sector of information. The password is retained by the device until the next power cycle. When the device accepts this command the device is in Set_Max_Unlocked state.

Table 46 – SET MAX SET PASSWORD data content

Word	Content
0	Reserved
1-16	Password (32 bytes)
17-255	Reserved

6.50.4 SET MAX LOCK

6.50.4.1 Command code

F9h with the content of the Features register equal to 02h.

6.50.4.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set security extensions are implemented.
- Use prohibited when the Removable feature set is implemented.

6.50.4.3 Protocol

Non-data (see Clause 11).

6.50.4.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	02h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F9h							

Device

DEV shall specify the selected device.

6.50.4.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.50.4.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported or the device is not in the Set_Max_Locked state. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be set to one if an Error register bit is set to one.

6.50.4.7 Prerequisites

DRDY set to one. This command shall not be immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.

6.50.4.8 Description

The SET MAX LOCK command sets the device into Set_Max_Locked state. After this command is completed any other SET MAX commands except SET MAX UNLOCK and SET MAX FREEZE LOCK shall be command aborted. The device shall remain in this state until a power cycle or command completion without error of a SET MAX UNLOCK or SET MAX FREEZE LOCK command.

6.50.5 SET MAX UNLOCK

6.50.5.1 Command code

F9h with the content of the Features register equal to 03h.

6.50.5.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set security extensions are implemented.
- Use prohibited when the Removable feature set is implemented.

6.50.5.3 Protocol

PIO data-out (see Clause 11).

6.50.5.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	03h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F9h							

Device
DEV shall specify the selected device.

6.50.5.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.50.5.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported or the device is not in the Set_Max_Locked state. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.

ERR shall be set to one if an Error register bit is set to one.

6.50.5.7 Prerequisites

DRDY set to one. This command shall not be immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.

6.50.5.8 Description

This command requests a transfer of a single sector of data from the host. Table 46 defines the content of this sector of information.
The password supplied in the sector of data transferred shall be compared with the stored SET MAX password.
If the password compare fails, then the device shall return command aborted and decrement the unlock counter. On the acceptance of the SET MAX LOCK command, this counter is set to a value of five and shall be decremented for each password mismatch when SET MAX UNLOCK is issued and the device is locked. When this counter reaches zero, then the SET MAX UNLOCK command shall return command aborted until a power cycle.
If the password compare matches, then the device shall make a transition to the Set_Max_Unlocked state and all SET MAX commands shall be accepted.

6.50.6 SET MAX FREEZE LOCK

6.50.6.1 Command code

F9h with the content of the Features register equal to 04h.

6.50.6.2 Feature set

Host Protected Area feature set.

- Mandatory when the Host Protected Area feature set security extensions are implemented.
- Use prohibited when the Removable feature set is implemented.

6.50.6.3 Protocol

Non-data (see Clause 11).

6.50.6.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	04h							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	F9h							

Device

DEV shall specify the selected device.

6.50.6.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.50.6.6 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported or the device is in the Set_Max_Unlocked state. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
ERR shall be set to one if an Error register bit is set to one.

6.50.6.7 Prerequisites

DRDY set to one. A SET MAX SET PASSWORD command shall previously have been successfully completed. This command shall not be immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.

6.50.6.8 Description

The SET MAX FREEZE LOCK command sets the device to Set_Max_Frozen state. After command completion any subsequent SET MAX commands shall be command aborted.

Commands disabled by SET MAX FREEZE LOCK are:

- SET MAX ADDRESS
- SET MAX SET PASSWORD
- SET MAX LOCK
- SET MAX UNLOCK

6.51 SET MAX ADDRESS EXT

6.51.1 Command code

37h

6.51.2 Feature set

Host Protected Area feature set and 48-bit Address feature set.

- Mandatory when the Host Protected Area feature set and the 48-bit Address feature set are implemented.
- Use prohibited when the Removable Media feature set is implemented.
- Use prohibited when PACKET Command feature set is implemented.

6.51.3 Protocol

Non-data (see Clause 11).

6.51.4 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	Reserved							
	Previous	Reserved							
Sector Count	Current	Reserved							V V
	Previous	Reserved							
LBA Low	Current	SET MAX LBA (7:0)							
	Previous	SET MAX LBA (31:24)							
LBA Mid	Current	SET MAX LBA (15:8)							
	Previous	SET MAX LBA (39:32)							
LBA High	Current	SET MAX LBA (23:16)							
	Previous	SET MAX LBA (47:40)							
Device		obs	LBA	obs	DEV	Reserved			
Command		37h							

NOTE The value indicated as Current is the value most recently written to the register. The value indicated as Previous is the value that was in the register before the most recent write to the register.

Sector Count Current

V V (Value volatile). If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

LBA Low Current

SET MAX LBA (7:0).

LBA Low Previous

SET MAX LBA (31:24).

LBA Mid Current

SET MAX LBA (15:8).

LBA Mid Previous

SET MAX LBA (39:32).

LBA High Current

SET MAX LBA (23:16).

LBA High Previous

SET MAX LBA (47:40).

Device

the LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

6.51.5 Normal outputs

Register		7	6	5	4	3	2	1	0
Error		na							
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	SET MAX LBA (7:0)							
	HOB = 1	SET MAX LBA (31:24)							
LBA Mid	HOB = 0	SET MAX LBA (15:8)							
	HOB = 1	SET MAX LBA (39:32)							
LBA High	HOB = 0	SET MAX LBA (23:16)							
	HOB = 1	SET MAX LBA (47:40)							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	DF	na	DRQ	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

LBA Low

LBA (7:0) of the address of the SET MAX ADDRESS EXT when read with Device Control register HOB bit cleared to zero.

LBA (31:24) of the address of the SET MAX ADDRESS EXT when read with Device Control register HOB bit set to one.

LBA Mid

LBA (15:8) of the address of the SET MAX ADDRESS EXT when read with Device Control register HOB bit cleared to zero.

LBA (39:32) of the address of the SET MAX ADDRESS EXT when read with Device Control register HOB bit set to one.

LBA High

LBA (23:16) of the address of the SET MAX ADDRESS EXT when read with Device Control register HOB bit cleared to zero.

LBA (47:40) of the address of the SET MAX ADDRESS EXT when read with Device Control register HOB bit set to one.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.51.6 Error outputs

If this command is not supported, the maximum value to be set exceeds the capacity of the device, a host protected area has been established by a SET MAX ADDRESS command, the command is not immediately preceded by a READ NATIVE MAX ADDRESS EXT command, or the device is in the Set_Max_Locked or Set_Max_Frozen state, then the device shall return command aborted.

Register		7	6	5	4	3	2	1	0
Error		na	na	na	IDNF	na	ABRT	na	obs
Sector Count	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Low	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA Mid	HOB = 0	Reserved							
	HOB = 1	Reserved							
LBA High	HOB = 0	Reserved							
	HOB = 1	Reserved							
Device		obs	na	obs	DEV	Reserved			
Status		BSY	DRDY	na	na	na	na	na	ERR
NOTE HOB = 0 indicates the value read by the host when the HOB bit of the Device Control register is cleared to zero. HOB = 1 Indicates the value read by the host when the HOB bit of the Device Control register is set to one.									

Error register

ABRT shall be set to one if this command is not supported, maximum value requested exceeds the device capacity, a host protected area has been established by a SET MAX ADDRESS command, or the command is not immediately preceded by a READ NATIVE MAX ADDRESS EXT command. ABRT may be set to one if the device is not able to complete the action requested by the command.

IDNF shall be set to one if the command was the second non-volatile SET MAX ADDRESS or SET MAX ADDRESS EXT command after power-on or hardware reset.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

6.51.7 Prerequisites

DRDY set to one. A successful READ NATIVE MAX ADDRESS EXT command shall immediately precede a SET MAX ADDRESS EXT command.

6.51.8 Description

After successful command completion, all read and write access attempts to addresses greater than specified by the successful SET MAX ADDRESS EXT command shall be rejected with an IDNF error.

Hosts shall not issue more than one non-volatile SET MAX ADDRESS or SET MAX ADDRESS EXT command after a power-on or hardware reset. Devices shall report an IDNF error upon receiving a second non-volatile SET MAX ADDRESS EXT command after a power-on or hardware reset.

The contents of IDENTIFY DEVICE data words and the max address shall not be changed if a SET MAX ADDRESS EXT command fails.

After a successful SET MAX ADDRESS EXT command using a new maximum LBA the content of all IDENTIFY DEVICE data words shall comply with 6.2.1.

6.52 SET MULTIPLE MODE

6.52.1 Command code

C6h

6.52.2 Feature set

General feature set
- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

6.52.3 Protocol

Non-data (see Clause 11).

6.52.4 Inputs

If the content of the Sector Count register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value in bits (7:0) in word 47 in the IDENTIFY DEVICE data. The host should set the content of the Sector Count register to 1, 2, 4, 8, 16, 32, 64 or 128.
If the content of the Sector Count register is zero and the SET MULTIPLE command completes without error, then the device shall respond to any subsequent READ MULTIPLE or WRITE MULTIPLE command with command aborted until a subsequent successful SET MULTIPLE command completion where the Sector Count register is not set to zero.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sectors per block							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	C6h							

Device register
DEV shall specify the selected device.

6.52.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.52.6 Error outputs

If a block count is not supported, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if the block count is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.52.7 Prerequisites

DRDY set to one.

6.52.8 Description

This command establishes the block count for READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE and WRITE MULTIPLE EXT commands.
Devices shall support the block size specified in the IDENTIFY DEVICE parameter word 47, bits (7:0), and may also support smaller values.

Upon receipt of the command, the device checks the Sector Count register. If the content of the Sector Count register is not zero, the Sector Count register contains a valid value and the block count is supported, then the value in the Sector Count register is used for all subsequent READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE and WRITE MULTIPLE EXT commands and their execution is enabled. If the content of the Sector Count register is zero, the device may:

1) disable multiple mode and respond with command aborted to all subsequent READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE and WRITE MULTIPLE EXT commands;
2) respond with command aborted to the SET MULTIPLE MODE command;
3) retain the previous multiple mode settings.

After a successful SET MULTIPLE command the device shall report the valid value set by that command in bits (7:0) in word 59 in the IDENTIFY DEVICE data.
After a power-on or hardware reset, if bit 8 is set to one and bits (7:0) are cleared to zero in word 59 of the IDENTIFY DEVICE data, a SET MULTIPLE command is required before issuing a READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE or WRITE MULTIPLE EXT command. If bit 8 is set to one and bits (7:0) are not cleared to zero, a SET MULTIPLE command may be issue to change the multiple value required before issuing a READ MULTIPLE, READ MULTIPLE EXT, WRITE MULTIPLE or WRITE MULTIPLE EXT command.

6.53 SLEEP

6.53.1 Command code

E6h

6.53.2 Feature set

Power Management feature set.

- This command is mandatory for devices not implementing the PACKET Command feature set.
- Power Management feature set is mandatory when power management is not implemented by the PACKET command set implemented by the device.
- This command is mandatory when the Power Management feature set is implemented.

6.53.3 Protocol

Non-data (see Clause 11).

6.53.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Command	E6h							

Device register

DEV shall specify the selected device.

6.53.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.53.6 Error outputs

The device shall return command aborted if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if the device does not support the Power Management feature set. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.53.7 Prerequisites

DRDY set to one.

6.53.8 Description

This command is the only way to cause the device to enter Sleep mode.
This command shall cause the device to set the BSY bit to one, prepare to enter Sleep mode, clear the BSY bit to zero and assert INTRQ. The host shall read the Status register in order to clear the Interrupt Pending and allow the device to enter Sleep mode. In Sleep mode, the device shall only respond to the assertion of the RESET− signal and the writing of the SRST bit in the Device Control register and shall release the device driven signal lines (see Figure 4). The host shall not attempt to access the Command Block registers while the device is in Sleep mode.
Because some host systems may not read the Status register and clear the Interrupt Pending, a device may release INTRQ and enter Sleep mode after a vendor-specific time period of not less than 2 s.
The only way to recover from Sleep mode is with a software reset, a hardware reset or a DEVICE RESET command.
A device shall not power-on in Sleep mode nor remain in Sleep mode following a reset sequence.

6.54 SMART

6.54.1 General

Individual SMART commands are identified by the value placed in the Feature register. Table 47 shows these Feature register values.

Table 47 – SMART Feature register values

Value	Command
00h-CFh	Reserved
D0h	SMART READ DATA
D1h	Obsolete
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D3h	Obsolete
D4h	SMART EXECUTE OFF-LINE IMMEDIATE
D5h	SMART READ LOG
D6h	SMART WRITE LOG
D7h	Obsolete
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS
DAh	SMART RETURN STATUS
DBh	Obsolete
DCh-DFh	Reserved
E0h-FFh	Vendor specific

6.54.2 SMART DISABLE OPERATIONS

6.54.2.1 Command code

B0h with a Feature register value of D9h.

6.54.2.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

6.54.2.3 Protocol

Non-data (see Clause 11).

6.54.2.4 Inputs

The Features register shall be set to D9h. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	na							
LBA Low	na							
LBA Mid	4Fh							
LBA High	C2h							
Device	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device register

DEV shall specify the selected device.

6.54.2.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.54.2.6 Error outputs

If the device does not support this command, if SMART is not enabled, or if the values in the Features, LBA Mid or LBA High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported, if SMART is not enabled or if input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.54.2.7 Prerequisites

DRDY set to one. SMART enabled.

6.54.2.8 Description

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations. SMART data shall no longer be monitored or

saved by the device. The state of SMART, either enabled or disabled, shall be preserved by the device across power cycles.
After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATIONS commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

6.54.3 SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

6.54.3.1 Command code

B0h with a Feature register value of D2h.

6.54.3.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

6.54.3.3 Protocol

Non-data (see Clause 11 of ISO/IEC 24739-2).

6.54.3.4 Inputs

The Features register shall be set to D2h. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h. The Sector Count register shall be set to 00h to disable attribute autosave and a value of F1h shall be set to enable attribute autosave.

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
LBA Low	na							
LBA Mid	4Fh							
LBA High	C2h							
Device	obs	na	obs	DEV	na	na	na	na
Command	B0h							

Device register
DEV shall specify the selected device.

6.54.3.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.54.3.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, LBA Mid or LBA High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
ABRT shall be set to one if this command is not supported, if SMART is disabled or if the input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.54.3.7 Prerequisites

DRDY set to one. SMART enabled.

6.54.3.8 Description

This command enables and disables the optional attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attribute values to non-volatile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) shall be preserved by the device across power cycles.
A value of zero written by the host into the device's Sector Count register before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.
A value of F1h written by the host into the device's Sector Count register before issuing this command shall cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command may differ from device to device. The meaning of any non-zero value written to this register at this time shall be preserved by the device across power cycles.
If this command is not supported by the device, the device shall return command aborted upon receipt from the host.
During execution of the autosave routine the device shall not set BSY to one nor clear DRDY to zero. If the device receives a command from the host while executing the autosave routine the device shall begin processing the command within two seconds.

6.54.4 SMART ENABLE OPERATIONS

6.54.4.1 Command code

B0h with a Feature register value of D8h.

6.54.4.2 Feature set

SMART feature set.

- Mandatory when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

6.54.4.3 Protocol

Non-data (see Clause 11 of ISO/IEC 24739-2).

6.54.4.4 Inputs

The Features register shall be set to D8h. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	na							
LBA Low	na							
LBA Mid	4Fh							
LBA High	C2h							
Device	obs	na	obs	DEV	na			
Command	B0h							

Device register

DEV shall specify the selected device.

6.54.4.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.54.4.6 Error outputs

If the device does not support this command or if the values in the Features, LBA Mid or LBA High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT shall be set to one if this command is not supported or if the input register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

6.54.4.7 Prerequisites

DRDY set to one.

6.54.4.8 Description

This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

6.54.5 SMART EXECUTE OFF-LINE IMMEDIATE

6.54.5.1 Command code

B0h with the content of the Features register equal to D4h

6.54.5.2 Feature set

SMART feature set.

– Optional when the SMART feature set is implemented.
– Use prohibited when the PACKET Command feature set is implemented.

6.54.5.3 Protocol

Non-data (see Clause 11 of ISO/IEC 24739-2).

6.54.5.4 Inputs

The Features register shall be set to D4h. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h. Table 48 defines the subcommand that shall be executed based on the value in the LBA Low register.

Register	7	6	5	4	3	2	1	0
Features	D4h							
Sector Count	na							
LBA Low	Subcommand specific							
LBA Mid	4Fh							
LBA High	C2h							
Device	obs	na	obs	DEV	na			
Command	B0h							

Device register
DEV shall specify the selected device.

6.54.5.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na or 4Fh							
LBA High	na or C2h							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

LBA Mid
na when the subcommand specified an off-line routine including an off-line self-test routine.
4Fh when the subcommand specified a captive self-test routine (see 6.54.5.10) that has executed without failure.

LBA High
na when the subcommand specified an off-line routine including an off-line self-test routine.
C2h when the subcommand specified a captive self-test routine that has executed without failure.

Device register
DEV shall indicate the selected device.

Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one indicating that the device is capable of receiving any command.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.54.5.6 Error outputs

If the device does not support this command, if SMART is disabled, or if the values in the Features, LBA Mid or LBA High registers are invalid, the device shall return command aborted. When a failure occurs while executing a test in captive mode, the device shall return command aborted with the LBA Mid register value of F4h and the LBA High value of 2Ch.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na or 4Fh or F4h							
LBA High	na or C2h or 2Ch							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

IDNF shall be set to one if SMART data sector's ID field could not be found.

ABRT shall be set to one if this command is not supported, if SMART is not enabled, if register values are invalid or if a self-test fails while executing a sequence in captive mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Mid register

na when the subcommand specified an off-line routine (including an off-line self-test routine).

4Fh when the subcommand specified a captive self-test routine and some error other than a self-test routine failure occurred (i.e., if the subcommand is not supported or register values are invalid)

F4h when the subcommand specified a captive self-test routine which has failed during execution.

LBA High register

na when the subcommand specified an off-line routine (including an off-line self-test routine).

2Ch when the subcommand specified a captive self-test routine which has failed during execution.

C2h when the subcommand specified a captive self-test routine and some error other than a self-test routine failure occurred (i.e., if the subcommand is not supported or register values are invalid)

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be set to one indicating that a device fault has occurred.

DRQ shall be cleared to zero indicating that there is no data to be transferred.

ERR shall be set to one if any Error register bit is set to one.

6.54.5.7 Prerequisites

DRDY set to one. SMART enabled.

6.54.5.8 Description

This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory or execute a self-diagnostic test routine in either captive or off-line mode.

Table 48 – SMART EXECUTE OFF-LINE IMMEDIATE LBA Low register values

Value	Description of subcommand to be executed
0	Execute SMART off-line routine immediately in off-line mode
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART Extended self-test routine immediately in off-line mode
3	Execute SMART Conveyance self-test routine immediately in off-line mode
4	Execute SMART Selective self-test routine immediately in off-line mode
5-63	Reserved
64-126	Vendor specific
127	Abort off-line mode self-test routine
128	Reserved
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART Extended self-test routine immediately in captive mode
131	Execute SMART Conveyance self-test routine immediately in captive mode
132	Execute SMART Selective self-test routine immediately in captive mode
133-191	Reserved
192-255	Vendor specific

6.54.5.9 Off-line mode

The following describes the protocol for executing a SMART EXECUTE OFF-LINE IMMEDIATE subcommand routine (including a self-test routine) in the off-line mode.

a) The device shall execute command completion before executing the subcommand routine.
b) After clearing BSY to zero and setting DRDY to one after receiving the command, the device shall not set BSY nor clear DRDY during execution of the subcommand routine.
c) If the device is in the process of performing the subcommand routine and is interrupted by any new command from the host except a SLEEP, SMART DISABLE OPERATIONS, SMART EXECUTE OFF-LINE IMMEDIATE or STANDBY IMMEDIATE command, the device shall suspend or abort the subcommand routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command from the host the device may immediately re-initiate or resume the subcommand routine without any additional commands from the host (see 6.54.6.12).
d) If the device is in the process of performing a subcommand routine and is interrupted by a SLEEP command from the host, the device may abort the subcommand routine and execute the SLEEP command. If the device is in the process of performing any self-test routine and is interrupted by a SLEEP command from the host, the device shall abort the subcommand routine and execute the SLEEP command.
e) If the device is in the process of performing the subcommand routine and is interrupted by a SMART DISABLE OPERATIONS command from the host, the device shall suspend or abort the subcommand routine and service the host within two seconds after receipt of the command. Upon receipt of the next SMART ENABLE OPERATIONS command the device may, either re-initiate the subcommand routine or resume the subcommand routine from where it had been previously suspended.
f) If the device is in the process of performing the subcommand routine and is interrupted by a SMART EXECUTE OFF-LINE IMMEDIATE command from the host, the device shall abort the subcommand routine and service the host within two seconds after receipt of the command. The device shall then service the new SMART EXECUTE OFF-LINE IMMEDIATE subcommand.
g) If the device is in the process of performing the subcommand routine and is interrupted by a STANDBY IMMEDIATE or IDLE IMMEDIATE command from the host, the device shall suspend or abort the subcommand routine and service the host within two seconds after receipt of the command. After receiving a new command that causes the device to exit a power saving mode, the device shall initiate or resume the subcommand routine without

any additional commands from the host unless these activities were aborted by the host (see 6.54.6.8).

h) While the device is performing the subcommand routine it shall not automatically change power states (e.g., as a result of its Standby timer expiring).

i) If a test failure occurs while a device is performing a self-test routine the device may discontinue the testing and place the test results in the Self-test execution status byte (see Table 49).

6.54.5.10 Captive mode

When executing a self-test in captive mode, the device sets BSY to one and executes the self-test routine after receipt of the command. At the end of the routine the device places the results of this routine in the Self-test execution status byte (see Table 49) and executes command completion. If an error occurs while a device is performing the routine, the device may discontinue its testing, place the results of this routine in the Self-test execution status byte and complete the command.

6.54.5.11 SMART off-line routine

This routine shall only be performed in the off-line mode. The results of this routine are placed in the Off-line data collection status byte (see Table 50).

6.54.5.12 SMART Short self-test routine

Depending on the value in the LBA Low register, this self-test routine may be performed in either the captive or the off-line mode. This self-test routine should take on the order of ones of minutes to complete (see 6.54.6.8).

6.54.5.13 SMART Extended self-test routine

Depending on the value in the LBA Low register, this self-test routine may be performed in either the captive or the off-line mode. This self-test routine should take on the order of tens of minutes to complete (see 6.54.6.8).

6.54.5.14 SMART Conveyance self-test routine

Depending on the value in the LBA Low register, this self-test routine may be performed in either the captive or the off-line mode. This self-test routine is intended to identify damage incurred during transporting of the device. This self-test routine should take on the order of minutes to complete (see 6.54.6.8).

6.54.5.15 SMART Selective self-test routine

The SMART Selective self-test routine is an optional self-test routine. If the routine is implemented, all features of the routine shall be implemented. Support for the routine is indicated in off-line data collection capabilities (see 6.54.6.12).

When the value in the LBA Low register is 4 or 132, the Selective self-test routine shall be performed. This self-test routine shall include the initial tests performed by the Extended self-test routine plus a selectable read scan. The host shall not write the Selective self-test log while the execution of a Selective self-test command is in progress.

The user may choose to do read scan only on specific areas of the media. To do this, the user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. When all specified test spans have been completed, the test is terminated and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. Figure 9 shows an example of a Selective self-test definition with three test spans defined. In this example, the test terminates when all three test spans have been scanned.

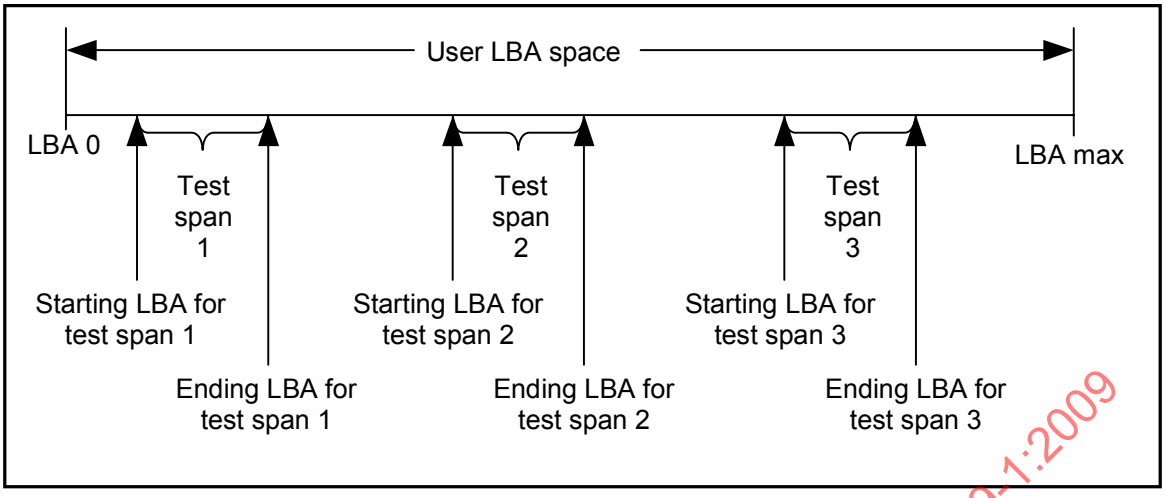


Figure 9 – Selective self-test test span example

After the scan of the selected spans described above, a user may wish to have the rest of the media read scanned as an off-line scan. In this case, the user shall set the flag to enable off-line scan in addition to the other settings. If an error occurs during the scanning of the test spans, the error is reported in the self-test execution status in the SMART READ DATA response and the off-line scan is not executed. When the test spans defined have been scanned, the device shall then set the off-line scan pending and active flags in the Selective self-test log to one, the span under test to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan shall complete as rapidly as possible, no pauses between block reads, and any errors encountered shall not be reported to the host. Instead error locations may be logged for future reallocation. If the device is powered-down before the off-line scan is completed, the off-line scan shall resume when the device is again powered-up. From power-up, the resumption of the scan shall be delayed the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time the pending flag shall be set to one and the active flag shall be set to zero in the Selective self-test log. Once the time expires, the active flag shall be set to one, and the off-line scan shall resume. When the entire media has been scanned, the off-line scan shall terminate, both the pending and active flags shall be cleared to zero, and the off-line data collection status in the SMART READ DATA response shall be set to 02h indicating completion.

During execution of the Selective self-test, the self-test executions time byte in the Device SMART Data Structure may be updated but the accuracy may not be exact because of the nature of the test span segments. For this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test spans is indicated in the selective self-test log.

A hardware or software reset shall abort the Selective self-test except when the pending bit is set to one in the Selective self-test log (see 6.54.7.8.5). The receipt of a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine, in the LBA Low register shall abort Selective self-test regardless of where the device is in the execution of the command. If a second self-test is issued while a selective self-test is in progress, the selective self-test is aborted and the newly requested self-test is executed.

6.54.6 SMART READ DATA

6.54.6.1 Command code

B0h with the content of the Features register equal to D0h.

6.54.6.2 Feature set

SMART feature set.

- Optional when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

6.54.6.3 Protocol

PIO data-in (see Clause 11).

6.54.6.4 Inputs

The Features register shall be set to D0h. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	na							
LBA Low	na							
LBA Mid	4Fh							
LBA High	C2h							
Device	obs	na	obs	DEV	na			
Command	B0h							

Device register

DEV shall specify the selected device.

6.54.6.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.54.6.6 Error outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, LBA Mid or LBA High registers are invalid, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

UNC shall be set to one if SMART data is uncorrectable.

IDNF shall be set to one if SMART data sector's ID field could not be found or data structure checksum occurred.

ABRT shall be set to one if this command is not supported, if SMART is not enabled or if register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be set to one indicating that a device fault has occurred.

DRQ shall be cleared to zero indicating that there is no data to be transferred.

ERR shall be set to one if any Error register bit is set to one.

6.54.6.7 Prerequisites

DRDY set to one. SMART enabled.

6.54.6.8 Description

This command returns the Device SMART data structure to the host.

Table 49 defines the 512 bytes that make up the Device SMART data structure. All multi-byte fields shown in this structure follow the byte ordering described in Clause 3.

Table 49 – Device SMART data structure

Byte	F/V	Descriptions
0-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-510	X	Vendor specific
511	V	Data structure checksum

Key

F = the content of the byte is fixed and does not change.

V = the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X = the content of the byte is vendor specific and may be fixed or variable.

R = the content of the byte is reserved and shall be zero.

6.54.6.9 Off-line collection status byte

The value of the off-line data collection status byte defines the current status of the off-line activities of the device. Table 50 lists the values and their respective definitions.

Table 50 – Off-line data collection status byte values

Value	Definition
00h or 80h	Off-line data collection activity was never started.
01h	Reserved
02h or 82h	Off-line data collection activity was completed without error.
03h	Off-line activity in progress.
04h or 84h	Off-line data collection activity was suspended by an interrupting command from host.
05h or 85h	Off-line data collection activity was aborted by an interrupting command from host.
06h or 86h	Off-line data collection activity was aborted by the device with a fatal error.
07h-3Fh	Reserved
40h-7Fh	Vendor specific
81h	Reserved
83h	Reserved
87h-BFh	Reserved
C0h-FFh	Vendor specific

6.54.6.10 Self-test execution status byte

The self-test execution status byte reports the execution status of the self-test routine.

- Bits (3:0) (Percent Self-Test Remaining) The value in these bits indicates an approximation of the percent of the self-test routine remaining until completion in ten percent increments. Valid values are 9 through 0. A value of 0 indicates the self-test routine is complete. A value of 9 indicates 90 % of total test time remaining.
- Bits (7:4) (Self-test Execution Status) The value in these bits indicates the current Self-test Execution Status (see Table 51).

Table 51 – Self-test execution status values

Value	Description
0	The previous self-test routine completed without error or no self-test has ever been run.
1	The self-test routine was aborted by the host.
2	The self-test routine was interrupted by the host with a hardware or software reset.
3	A fatal error or unknown test error occurred while the device was executing its self-test routine and the device was unable to complete the self-test routine.
4	The previous self-test completed having a test element that failed and the test element that failed is not known.
5	The previous self-test completed having the electrical element of the test failed.
6	The previous self-test completed having the servo (and/or seek) test element of the test failed.
7	The previous self-test completed having the read element of the test failed.
8	The previous self-test completed having a test element that failed and the device is suspected of having handling damage.
9-14	Reserved.
15	Self-test routine in progress.

6.54.6.11 Total time to complete off-line data collection

The total time in seconds to complete off-line data collection activity word specifies how many seconds the device requires to complete the sequence of off-line data collection activity. Valid values for this word are from 0001h to FFFFh.

6.54.6.12 Off-line data collection capabilities

The following describes the definition for the off-line data collection capability bits. If the value of all of these bits is cleared to zero, then no off-line data collection is implemented by this device.

- Bit 0 (EXECUTE OFF-LINE IMMEDIATE implemented bit) If this bit is set to one, then the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented by this device. If this bit is cleared to zero, then the SMART EXECUTE OFF-LINE IMMEDIATE command is not implemented by this device.
- Bit 1 (vendor specific).
- Bit 2 (abort/restart off-line by host bit) If this bit is set to one, then the device shall abort all off-line data collection activity initiated by an SMART EXECUTE OFF-LINE IMMEDIATE command upon receipt of a new command within 2 s of receiving the new command. If this bit is cleared to zero, the device shall suspend off-line data collection activity after an interrupting command and resume off-line data collection activity after some vendor-specified event.
- Bit 3 (off-line read scanning implemented bit) If this bit is cleared to zero, the device does not support off-line read scanning. If this bit is set to one, the device supports off-line read scanning.
- Bit 4 (self-test implemented bit) If this bit is cleared to zero, the device does not implement the Short and Extended self-test routines. If this bit is set to one, the device implements the Short and Extended self-test routines.
- Bit 5 (conveyance self-test implemented bit) If this bit is cleared to zero, the device does not implement the Conveyance self-test routines. If this bit is set to one, the device implements the Conveyance self-test routines.
- Bit 6 (Selective self-test implemented bit) If this bit is cleared to zero, the device does not implement the Selective self-test routine. If this bit is set to one, the device implements the Selective self-test routine.
- Bit 7 (Reserved).

6.54.6.13 SMART capablilities

The following describes the definition for the SMART capabilities bits.

- Bit 0 If this bit is set to one, the device saves SMART data prior to going into a power saving mode (Idle, Standby or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If this bit is cleared to zero, the device does not save SMART data prior to going into a power saving mode (Idle, Standby or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.
- Bit 1 This bit shall be set to one to indicate that the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.
- Bits (15:2) (Reserved).

6.54.6.14 Self-test routine recommended polling time

The self-test routine recommended polling time shall be equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

6.54.6.15 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

6.54.7 SMART READ LOG

6.54.7.1 Command code

B0h with the content of the Features register equal to D5h.

6.54.7.2 Feature set

SMART feature set.

- Optional when the SMART feature set is implemented.
- Use prohibited when the PACKET Command feature set is implemented.

6.54.7.3 Protocol

PIO data-in (see Clause 11).

6.54.7.4 Inputs

The Features register shall be set to D5h. The Sector Count register shall specify the number of sectors to be read from the log number specified by the LBA Low register. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D5h							
Sector Count	Number of sectors to be read							
LBA Low	Log address							
LBA Mid	4Fh							
LBA High	C2h							
Device	obs	na	obs	DEV	na			
Command	B0h							

Sector count specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the first sector in the specified log, regardless of the sector count requested.

LBA Low specifies the log to be returned as described in Table 52. If this command is implemented, all address values for which the contents are defined shall be implemented and all address values defined as host vendor specific shall be implemented. The host vendor specific logs may be used by the host to store any data desired. If a host vendor-specific log has never been written by the host, then the read content of the log shall be zeroes. Device vendor-specific logs may be used by the device vendor to store any data and need only be implemented if used.

Table 52 – Log address definition

Log address	Content	R/W
00h	Log directory	RO
01h	Summary SMART error log	RO
02h	Comprehensive SMART error log	RO
03h	Extended Comprehensive SMART error log	See note
04h-05h	Reserved	Reserved
06h	SMART self-test log	RO
07h	Extended self-test log	See note
08h	Reserved	Reserved
09h	Selective self-test log	R/W
0Ah-1Fh	Reserved	Reserved
20h	Streaming performance log	See note
21h	Write stream error log	See note
22h	Read stream error log	See note
23h	Delayed sector log	See note
24h-7Fh	Reserved	Reserved
80h-9Fh	Host vendor specific	R/W
A0h-BFh	Device vendor specific	VS
C0h-FFh	Reserved	Reserved

Key

RO = Log is read only by the host.

R/W = Log is read or written by the host.

VS = Log is vendor specific thus read/write abiltiy is vendor specific.

NOTE Log addresses 03h, 07h, 20h, 21h , 22h and 23h are used by the READ LOG EXT and WRITE LOG EXT commands. If these log addresses are used with the SMART READ LOG command, the device shall return command aborted.

Device register

DEV shall specify the selected device.

6.54.7.5 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one indicating that the device is capable of receiving any command.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.54.7.6 Error outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, LBA Low, Sector Count, LBA Mid or LBA High registers are invalid, the device shall return command aborted. If the host issues a SMART READ LOG or SMART WRITE LOG command with a Sector Count value of zero, the device shall return command aborted.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	obs
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	Na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register
UNC shall be set to one if SMART log sector is uncorrectable.
IDNF shall be set to one if SMART log sector's ID field was not found or data structure checksum error occurred.
ABRT shall be set to one if this command is not supported, if SMART is not enabled, if the log sector address is not implemented, if the Sector Count value is zero or if other register values are invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.
Device register
DEV shall indicate the selected device.
Status register
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one indicating that the device is capable of receiving any command.
DF (Device Fault) shall be set to one indicating that a device fault has occurred.
DRQ shall be cleared to zero indicating that there is no data to be transferred.
ERR shall be set to one if any Error register bit is set to one.

6.54.7.7 Prerequisites

DRDY set to one, SMART enabled.

6.54.7.8 Description

6.54.7.8.1 General

This command returns the specified log to the host.

6.54.7.8.2 SMART Log Directory

Table 53 defines the 512 bytes that make up the SMART Log Directory, which is optional. If implemented, the SMART Log Directory is SMART Log address zero and is defined as one sector long.

Table 53 – SMART Log Directory

Byte	Descriptions
0-1	SMART Logging Version
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
…	…
510	Number of sectors in the log at log address 255
511	Reserved

The value of the SMART Logging Version word shall be 01h if the drive supports multi-sector SMART logs. In addition, if the drive supports multi-sector logs, then the logs at log addresses 80-9Fh shall each be defined as 16 sectors long.
If the drive does not support multi-sector SMART logs, then log number zero is defined as reserved, and the drive shall return a command aborted response to the host's request to read log number zero.

6.54.7.8.3 Summary error log sector

6.54.7.8.3.1 General

Table 54 defines the 512 bytes that make up the SMART summary error log sector. All multi-byte fields shown in this structure follow the byte ordering described in Clause 3. Summary error log data structures shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Summary error log data structures shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or invalid addresses. If the device supports comprehensive error log (address 02h), then the summary error log sector duplicates the last five error entries in the comprehensive error log. The summary error log supports 28-bit addressing only.

Table 54 – SMART summary error log sector

Byte	Descriptions
0	SMART error log version
1	Error log index
2-91	First error log data structure
92-181	Second error log data structure
182-271	Third error log data structure
272-361	Fourth error log data structure
362-451	Fifth error log data structure
452-453	Device error count
454-510	Reserved
511	Data structure checksum

6.54.7.8.3.2 Error log version

The value of the SMART summary error log version byte shall be 01h.

6.54.7.8.3.3 Error log index

The error log index indicates the error log data structure representing the most recent error. Only values 5 through 0 are valid. If there are no error log entries, the value of the error log index shall be zero.

6.54.7.8.3.4 Error log data structure

6.54.7.8.3.4.1 General

An error log data structure shall be presented for each of the last five errors reported by the device. These error log data structure entries are viewed as a circular buffer. That is, the first error shall create the first error log data structure; the second error, the second error log structure; etc. The sixth error shall create an error log data structure that replaces the first error log data structure; the seventh error replaces the second error log structure, etc. The error log pointer indicates the most recent error log structure. If fewer than five errors have occurred, the unused error log structure entries shall be zero filled. Table 55 describes the content of a valid error log data structure.

Table 55 – Error log data structure

Byte	Descriptions
n thru *n*+11	First command data structure
n+12 thru *n*+23	Second command data structure
n+24 thru *n*+35	Third command data structure
n+36 thru *n*+47	Fourth command data structure
n+48 thru *n*+59	Fifth command data structure
n+60 thru *n*+89	Error data structure

6.54.7.8.3.4.2 Command data structure

The fifth command data structure shall contain the command or reset for which the error is being reported. The fourth command data structure should contain the command or reset that preceded the command or reset for which the error is being reported, the third command data structure should contain the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures shall be zero filled, for example, if only three commands and resets preceded the command or reset for which the error is being reported, the first command data structure shall be zero filled. In some devices, the hardware implementation may preclude the device from reporting the commands that preceded the command for which the error is being reported or that preceded a reset. In this case, the command data structures are zero filled.

If the command data structure represents a command or software reset, the content of the command data structure shall be as shown in Table 56. If the command data structure represents a hardware reset, the content of byte *n* shall be FFh, the content of bytes *n*+1 through *n*+7 are vendor specific, and the content of bytes *n*+8 through *n*+11 shall contain the timestamp.

Table 56 – Command data structure

Byte	Descriptions
n	Content of the Device Control register when the Command register was written.
n+1	Content of the Features register when the Command register was written.
n+2	Content of the Sector Count register when the Command register was written.
n+3	Content of the LBA Low register when the Command register was written.
n+4	Content of the LBA Mid register when the Command register was written.
n+5	Content of the LBA High register when the Command register was written.
n+6	Content of the Device register when the Command register was written.
n+7	Content written to the Command register.
n+8	Timestamp (least significant byte)
n+9	Timestamp (next least significant byte)
n+10	Timestamp (next most significant byte)
n+11	Timestamp (most significant byte)

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

6.54.7.8.3.4.3 Error data structure

The error data structure shall contain the error description of the command for which an error was reported as described in Table 57. If the error was logged for a hardware reset, the content of bytes *n*+1 through *n*+7 shall be vendor specific and the remaining bytes shall be as defined in Table 57.

Table 57 – Error data structure

Byte	Descriptions
n	Reserved
n+1	Content of the Error register after command completion occurred.
n+2	Content of the Sector Count register after command completion occurred.
n+3	Content of the LBA Low register after command completion occurred.
n+4	Content of the LBA Mid register after command completion occurred.
n+5	Content of the LBA High register after command completion occurred.
n+6	Content of the Device register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 thru *n*+26	Extended error information
n+27	State
n+28	Life timestamp (least significant byte)
n+29	Life timestamp (most significant byte)

Extended error information shall be vendor specific.

State shall contain a value indicating the state of the device when command was written to the Command register or the reset occurred as described in Table 58.

Table 58 – State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique
The value of x is vendor specific and may be different for each state.	

Sleep indicates the reset for which the error is being reported was received when the device was in the Sleep mode.
Standby indicates the command or reset for which the error is being reported was received when the device was in the Standby mode.
Active/Idle with BSY cleared to zero indicates the command or reset for which the error is being reported was received when the device was in the Active or Idle mode and BSY was cleared to zero.
Executing SMART off-line or self-test indicates the command or reset for which the error is being reported was received when the device was in the process of executing a SMART off-line or self-test.
Life timestamp shall contain the power-on lifetime of the device in hours when command completion occurred.

6.54.7.8.3.5 Device error count

The device error count field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. These errors shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached, the count shall remain at the maximum value when additional errors are encountered and logged.

6.54.7.8.3.6 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

6.54.7.8.3.7 Comprehensive error log

Table 59 defines the format of each of the sectors that comprise the SMART comprehensive error log. The SMART Comprehensive error log provides logging for 28-bit addressing only. For 48-bit addressing see 6.31.8.3. The maximum size of the SMART comprehensive error log shall be 51 sectors. Devices may support fewer than 51 sectors. All multi-byte fields shown in this structure follow the byte ordering described in Clause 3. The comprehensive error log data structures shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Comprehensive error log data structures shall not include errors attributed to the receipt of faulty commands such as command codes not supported by the device or requests with invalid parameters or invalid addresses.

Table 59 – Comprehensive error log

Byte	First sector	Subsequent sectors
0	SMART error log version	Reserved
1	Error log index	Reserved
2-91	First error log data structure	Data structure 5*n*+1
92-181	Second error log data structure	Data structure 5*n*+2
182-271	Third error log data structure	Data structure 5*n*+3
272-361	Fourth error log data structure	Data structure 5*n*+4
362-451	Fifth error log data structure	Data structure 5*n*+5
452-453	Device error count	Reserved
454-510	Reserved	Reserved
511	Data structure checksum	Data structure checksum
n is the sector number within the log. The first sector is sector zero		

6.54.7.8.3.8 Error log version

The value of the error log version byte shall be set to 01h.

6.54.7.8.3.9 Error log index

The error log index indicates the error log data structure representing the most recent error. If there have been no error log entries, the error log index is set to zero. Valid values for the error log index are zero to 255.

6.54.7.8.3.10 Error log data structure

The error log is viewed as a circular buffer. The device may support from two to 51 error log sectors. When the last supported error log sector has been filled, the next error shall create an error log data structure that replaces the first error log data structure in sector zero. The next error after that shall create an error log data structure that replaces the second error log data structure in sector zero. The sixth error after the log has filled shall replace the first error log data structure in sector one, and so on.
The error log index indicates the most recent error log data structure. Unused error log data structures shall be filled with zeroes.
The content of the error log data structure entries is defined in 6.54.7.8.3.4.

6.54.7.8.3.11 Device error count

The device error count field is defined in 6.54.7.8.3.5.

6.54.7.8.3.12 Data structure checksum

The data structure checksum is defined in 6.54.7.8.3.6.

6.54.7.8.4 Self-test log sector

6.54.7.8.4.1 General

Table 60 defines the 512 bytes that make up the SMART self-test log sector. All multi-byte fields shown in this structure follow the byte ordering described in Clause 3. The self-test log sector supports 28-bit addressing only.

Table 60 – Self-test log data structure

Byte	Descriptions
0-1	Self-test log data structure revision number
2-25	First descriptor entry
26-49	Second descriptor entry
.....	.....
482-505	Twenty-first descriptor entry
506-507	Vendor specific
508	Self-test index
509-510	Reserved
511	Data structure checksum

This log is viewed as a circular buffer. The first entry shall begin at byte 2, the second entry shall begin at byte 26, and so on until the twenty-second entry, that shall replace the first entry. Then, the twenty-third entry shall replace the second entry, and so on. If fewer than 21 self-tests have been performed by the device, the unused descriptor entries shall be filled with zeroes.

6.54.7.8.4.2 Self-test log data structure revision number

The value of the self-test log data structure revision number shall be 0001h.

6.54.7.8.4.3 Self-test log descriptor entry

The content of the self-test descriptor entry is shown in Table 61.

Table 61 – Self-test log descriptor entry

Byte	Descriptions
n	Content of the LBA Low register.
n+1	Content of the self-test execution status byte.
n+2	Life timestamp (least significant byte).
n+3	Life timestamp (most significant byte).
n+4	Content of the self-test failure checkpoint byte.
n+5	Failing LBA (least significant byte).
n+6	Failing LBA (next least significant byte).
n+7	Failing LBA (next most significant byte).
n+8	Failing LBA (most significant byte).
n+9 to *n*+23	Vendor specific.

Content of the LBA Low register shall be the content of the LBA Low register when the *n*th self-test subcommand was issued (see 6.54.5.8).
Content of the self-test execution status byte shall be the content of the self-test execution status byte when the nth self-test was completed (see 6.54.6.10).
Life timestamp shall contain the power-on lifetime of the device in hours when the *n*th self-test subcommand was completed.
Content of the self-test failure checkpoint byte may contain additional information about the self-test that failed.
The failing LBA shall be the LBA of the uncorrectable sector that caused the test to fail. If the device encountered more than one uncorrectable sector during the test, this field shall

indicate the LBA of the first uncorrectable sector encountered. If the test passed or the test failed for some reason other than an uncorrectable sector, the value of this field is undefined.

6.54.7.8.4.4 Self-test index

The self-test index shall point to the most recent entry. Initially, when the log is empty, the index shall be set to zero. It shall be set to one when the first entry is made, two for the second entry, etc., until the 22nd entry, when the index shall be reset to one.

6.54.7.8.4.5 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

6.54.7.8.5 Selective self-test log

6.54.7.8.5.1 General

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. Table 62 defines the content of the Selective self-test log.

Table 62 – Selective self-test log

Byte	Description	Read/write
0-1	Data structure revision number	R/W
2-9	Starting LBA for test span 1	R/W
10-17	Ending LBA for test span 1	R/W
18-25	Starting LBA for test span 2	R/W
26-33	Ending LBA for test span 2	R/W
34-41	Starting LBA for test span 3	R/W
42-49	Ending LBA for test span 3	R/W
50-57	Starting LBA for test span 4	R/W
58-65	Ending LBA for test span 4	R/W
66-73	Starting LBA for test span 5	R/W
74-81	Ending LBA for test span 5	R/W
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags	R/W
504-507	Vendor specific	Vendor specific
508-509	Selective self-test pending time	R/W
510	Reserved	Reserved
511	Data structure checksum	R/W

6.54.7.8.5.2 Data structure revision number

The value of the data structure revision number filed shall be 01h. This value shall be written by the host and returned unmodified by the device.