ISO/IEC 14776-153

Edition 1.0 2015-02

INTERNATIONAL STANDARD

colour inside

Information technology – Small computer system interface (SCSI) – Part 153: Serial attached SCSI - 2.1 (SAS-2.1)

ISO/IEC 14776-153:2015-02(en)

ISO/IEC 14776-153

Edition 1.0 2015-02

INTERNATIONAL STANDARD

Information technology – Small computer system interface (SCSI) – Part 153: Serial attached SCSI - 2.1 (SAS-2.1)

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 35.200

ISBN 978-2-8322-2204-1

CONTENTS

INFORMATION TECHNOLOGY –
SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 153: SERIAL ATTACHED SCSI - 2.1 (SAS-2.1)

FOREWORD

1) ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.
2) The formal decisions or agreements of IEC and ISO on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees and ISO member bodies.
3) IEC, ISO and ISO/IEC publications have the form of recommendations for international use and are accepted by IEC National Committees and ISO member bodies in that sense. While all reasonable efforts are made to ensure that the technical content of IEC, ISO and ISO/IEC publications is accurate, IEC or ISO cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees and ISO member bodies undertake to apply IEC, ISO and ISO/IEC publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any ISO, IEC or ISO/IEC publication and the corresponding national or regional publication should be clearly indicated in the latter.
5) ISO and IEC do not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. ISO or IEC are not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or ISO or its directors, employees, servants or agents including individual experts and members of their technical committees and IEC National Committees or ISO member bodies for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication of, use of, or reliance upon, this ISO/IEC publication or any other IEC, ISO or ISO/IEC publications.
8) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this ISO/IEC publication may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

International Standard ISO/IEC 14776-153 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

The list of all currently available parts of the ISO/IEC 14776 series, under the general title *Information technology – Small computer system interface (SCSI)*, can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2, as far as is practicable.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

General

The SCSI family of standards provides for many different transport protocols that define the rules for exchanging information between different SCSI devices. This standard specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer (SPL) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 2.1 (SAS-2.1) and beyond, defining the rules for exchanging information between SCSI devices using a serial interconnect. Other SCSI transport protocol standards define the rules for exchanging information between SCSI devices using other interconnects.

SCSI standards family

Figure 1 shows the relationship of this standard to the other standards and related projects in the SCSI family of standards.

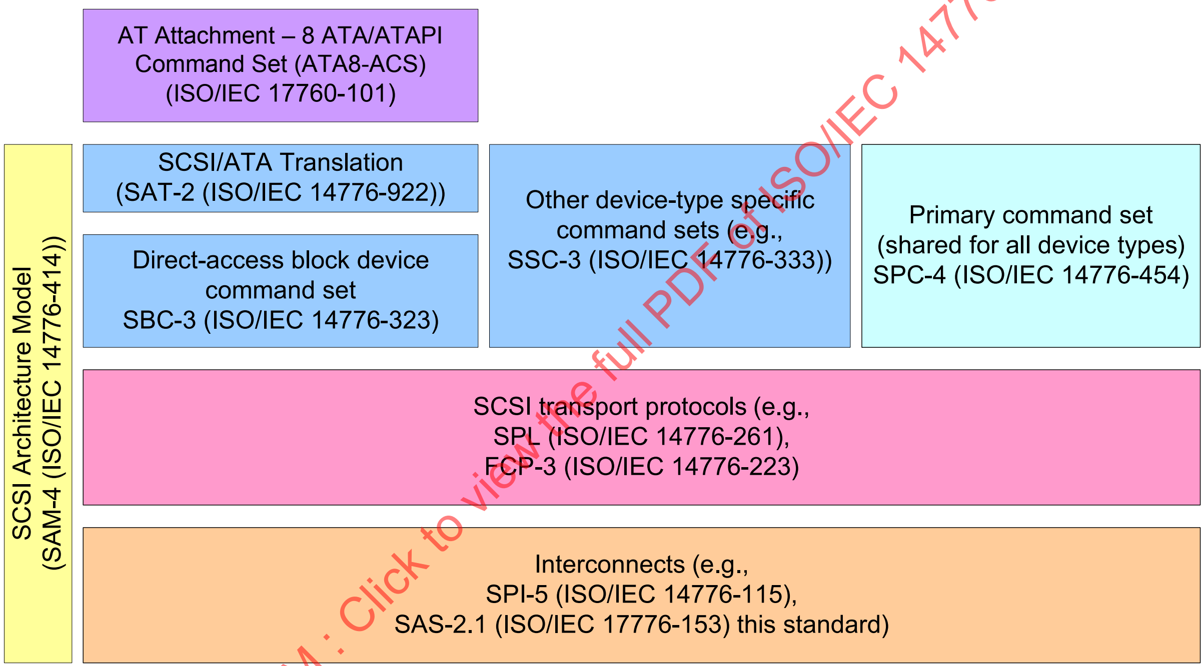


Figure 1 — SCSI document relationships

Figure 2 shows the relationship of this standard to other standards and related projects in the ATA family of standards.

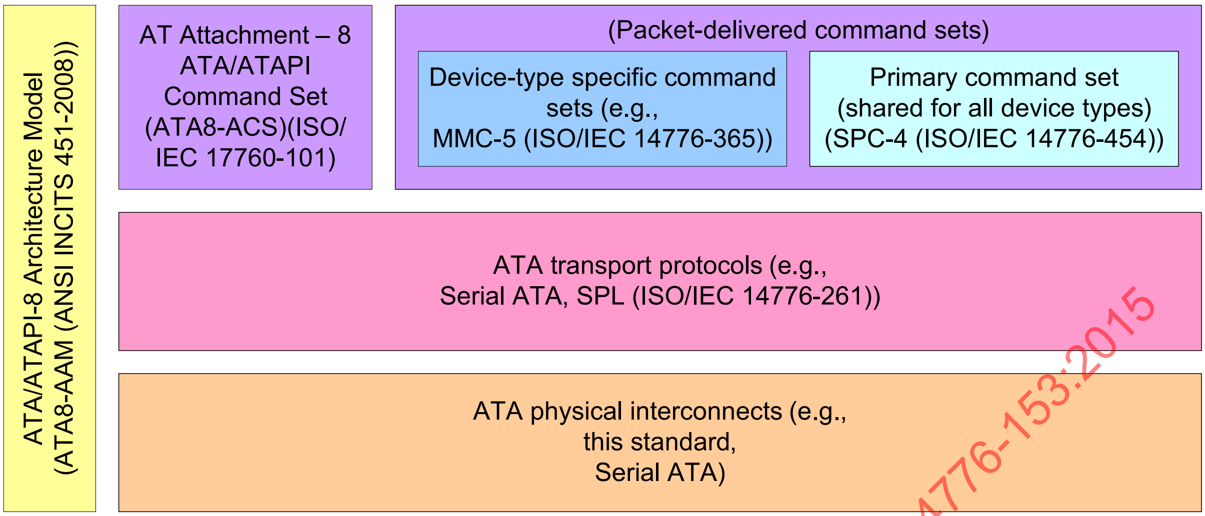


Figure 2 — ATA document relationships

Figure 1 and figure 2 show the general relationship of the documents to one another, and do not imply a relationship such as a hierarchy, protocol stack or system architecture.

These standards specify the interfaces, functions and operations necessary to ensure interoperability between conforming implementations. This standard is a functional description. Conforming implementations may employ any design technique that does not violate interoperability.

INFORMATION TECHNOLOGY –

SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 153: SERIAL ATTACHED SCSI - 2.1 (SAS-2.1)

1 Scope

This part of ISO/IEC 14776 defines the physical layer of the Serial Attached SCSI (SAS) interconnect.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 14165-117, *Information technology – Fibre channel – Part 117: Methodologies for jitter and signal quality (MJSQ)*[1 2]

ISO/IEC 14776-261, *Information technology – Small Computer System Interface (SCSI) – Part 261: SAS Protocol Layer (SPL)*[3]

ISO/IEC 14776-414, *Information technology – Small Computer System Interface (SCSI) – Part 414: SCSI Architecture Model - 4 (SAM-4)*

ANSI INCITS 451-2008, *Information technology – AT Attachment-8 ATA/ATAPI Architecture Model (ATA8-AAM)*

For information on the current status of the listed documents, or regarding availability, contact the indicated organization.

Serial ATA Revision 3.0 (SATA). 2 June 2009

NOTE 1 For more information on Serial ATA international Organization, see www.sata-io.org.

SFF-8086, *Compact Multilane Series: Common Elements*

SFF-8087, *Compact Multilane Series: Unshielded*

SFF-8088, *Compact Multilane Series: Shielded*

SFF-8147, *54mm x 71mm Form Factor w/micro SAS Connector*

SFF-8223, *2.5" Drive Form Factor with Serial Connector*

SFF-8323, *3.5" Drive Form Factor with Serial Connector*

SFF-8410, *HSS Copper Testing and Performance Requirements*

SFF-8416, *Measurement and Performance Requirements for HPEI Bulk Cable*

SFF-8436, *QSFP+ Copper and Optical Modules*

SFF-8449, *Mini Multilane Series Management Interface*

SFF-8460, *HSS Backplane Design Guidelines*

SFF-8482, *Unshielded Dual Port Serial Attachment Connector*

1.ANSI INCITS TR-35-2004
2.When MJSQ is referenced from this standard, the FC Port terminology used within MJSQ should be substituted with SAS phy terminology.
3.T10/2124-D

SFF-8484, *Multi-Lane Unshielded Serial Attachment Connectors*

SFF-8485, *Serial GPIO (SGPIO) Bus*

SFF-8486, *Serial Attachment Micro Connector*

SFF-8523, *5.25" Drive Form Factor with Serial Connector*

SFF-8643, *Mini Multilane Series: Unshielded HD Integrated Connector*

SFF-8644, *Mini Multilane Series: Shielded HD Integrated Connector*

NOTE 2 For more information on the current status of SFF documents, contact the SFF Committee at 408-867-6630 (phone), or 408-867-2115 (fax). To obtain copies of these documents, contact the SFF Committee at 14426 Black Walnut Court, Saratoga, CA 95070 at 408-867-6630 (phone) or 408-741-1600 (fax) or see http://www.sffcommittee.org.

ASTM Standard B 258-02, 2002, *Standard specification for standard nominal diameters and cross-sectional areas of AWG sizes of solid round wires used as electrical conductors*, ASTM International, West Conshohocken, PA, USA.

NOTE 3 For more information on ASTM International standards, see www.astm.org.

PANTONE® Color Formula Guide

NOTE 4 Pantone® and PANTONE MATCHING SYSTEM® are registered trademarks of Pantone, Inc. For more information on Pantone colors, contact Pantone, Inc. (see http://www.pantone.com). This information is given for the convenience of users of this standard and does not constitute an endorsement by [ISO or IEC] of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Touchstone® File Format Specification. Revision 1.1. IBIS Open Forum.

NOTE 5 Touchstone® is a registered trademark of Agilent Corporation. For more information on the Touchstone specification, contact the IBIS Open Forum (see http://www.eigroup.org). This information is given for the convenience of users of this standard and does not constitute an endorsement by [ISO or IEC] of the product named. Equivalent products may be used if they can be shown to lead to the same results.

MATLAB® 7 Programming Fundamentals. Release 2008b.

NOTE 6 MATLAB® is a registered trademark of The MathWorks, Inc. For more information on MATLAB, contact The Mathworks, Inc. (see http://www.mathworks.com). This information is given for the convenience of users of this standard and does not constitute an endorsement by [ISO or IEC] of the product named. Equivalent products may be used if they can be shown to lead to the same results.

3 Terms, definitions, symbols, abbreviations, keywords, and conventions

3.1 Terms and definitions

For the purposes of this document the following terms and definitions apply.

3.1.1
active cable assembly
cable assembly (see 3.1.9) that requires power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.2
AT Attachment
ATA
standard for the internal attachment of storage devices to hosts

Note 1 to entry: See ATA8-AAM.

3.1.3
baud rate
nominal signaling speed, expressed as the maximum number of times per second that the signal (see 3.1.87) may change the state of the physical link (see 3.1.66)

Note 1 to entry: Each state change produces a transition (i.e., signal edge).

Note 2 to entry: The baud rate is the reciprocal of the *UI* (i.e., $f_{baud} = 1 / UI$) (see 3.1.103).

3.1.4
bit error ratio
BER
number of logical bits output from a receiver circuit that differ from the correct transmitted logical bits, divided by the number of transmitted logical bits

Note 1 to entry: The BER is computed on the raw bit stream before 10b8b decoding.

Note 2 to entry: The BER is usually expressed as a coefficient and a power of 10 (e.g., 2 erroneous bits out of 100 000 bits transmitted is expressed as 2 out of 10^5 or 2×10^{-5}).

Note 3 to entry: See MJSQ.

3.1.5
bit time
nominal duration of a signal transmission bit (e.g., 666,6 ps at 1,5 Gbit/s, 333,3 ps at 3 Gbit/s, and 166,6 ps at 6 Gbit/s)

3.1.6
bounded uncorrelated jitter
BUJ
part of DJ (see 3.1.23) not aligned in time with the signal being measured; specifically, BUJ excludes ISI (see 3.1.47) and duty cycle distortion

Note 1 to entry: See MJSQ.

3.1.7
burst time
part of an OOB signal (see 3.1.60) where the OOB burst (see 3.1.56) is transmitted (see 5.9)

3.1.8
byte
sequence of eight contiguous bits considered as a unit

3.1.9
cable assembly
bulk cable with a separable connector at each end plus any retention, backshell, shielding features, or circuitry used for cable management or signal transmission

Note 1 to entry: See 5.4.3.

3.1.10
clock data recovery
CDR
function provided by the receiver circuit responsible for producing a regular clock signal (i.e., the recovered clock) from the received signal and for aligning the recovered clock to the symbols (i.e., bits) being transmitted with the signal

Note 1 to entry: The CDR uses the recovered clock to recover the bits.

Note 2 to entry: See MJSQ.

3.1.11
common SSC transmit clock
implementation that employs a single transmit clock for multiple transmitter devices and enables or disables SSC (see 5.7.6) on the transmit clock signal to all transmitter devices in common rather than allowing each transmitter device to independently control SSC

3.1.12
compliance point
interoperability point where interoperability specifications are met

Note 1 to entry: See 5.3.

3.1.13
compliant jitter tolerance pattern
CJTPAT
test pattern for jitter testing

Note 1 to entry: See 5.7.3.5 and Annex A.

3.1.14
connector
electro-mechanical components consisting of a receptacle and a plug that provide a separable interface between two transmission segments

Note 1 to entry: See 5.4.3.

3.1.15
cumulative distribution function
CDF
probability that jitter (see 3.1.48) is less than a given value

Note 1 to entry: See MJSQ.

3.1.16
D.C. idle
differential signal level that is nominally 0 V(P-P), used during the idle time (see 3.1.45) and negation time (see 3.1.55) of an OOB signal (see 3.1.60) when D.C. mode (see 3.1.17) is enabled

Note 1 to entry: See 5.7.4.

3.1.17
D.C. mode
mode in which D.C. idle (see 3.1.16) is used during the idle time (see 3.1.45) and negation time (see 3.1.55) of an OOB signal (see 3.1.60)

3.1.18
data dependent jitter
DDJ
jitter (see 3.1.48) that is added when the transmission pattern is changed from a clock-like to a non-clock-like pattern

Note 1 to entry: See MJSQ.

3.1.19
decibel
dB
ten times the common logarithm (i.e., $\log_{10}$) of the ratio of relative powers

Note 1 to entry: The ratio of powers P_1 and P_2 in dB is $10 \times \log_{10} (P_1 / P_2)$. If $P_1 = V_1^2 / R_1$, $P_2 = V_2^2 / R_2$, and $R_1 = R_2$, then this ratio is equivalent to 20 times the common logarithm of the relative voltage ratio (i.e., dB = $20 \times \log_{10} (V_1 / V_2)$). A ratio of 1 results in a dB value of 0 (e.g., $20 \times \log_{10} (1) = 0$ dB), a ratio greater than 1 results in a positive dB value (e.g., $20 \times \log_{10} (2) = 6$ dB) and a ratio less than 1 results in a negative dB value (e.g., $20 \times \log_{10} (0.5) = -6$ dB).

3.1.20
dB millivolts
dBmV
decibel ratio of an RMS voltage value relative to 1 mV

Note 1 to entry: 20 mV(r.m.s.) is equal to $20 \times \log_{10}(20 \text{ mV} / 1 \text{ mV}) = 26$ dBmV; this does not depend on the impedance level.

3.1.21
dB milliwatts
dBm
decibel ratio of a power value relative to 1 mW

Note 1 to entry: 20 mW is equal to $10 \times \log_{10}(20 \text{ mW} / 1 \text{ mW}) = 13$ dBm. If power is measured with a 50 Ω impedance level, then 20 mW is equivalent to $(0.02 \text{ W} \times 50\ \Omega)^{(1/2)} = 1$ V or 60 dBmV. If power is measured with a 25 Ω impedance level (i.e., the reference impedance for common mode measurements), then 20 mW is equivalent to $(0.02 \text{ W} \times 25\ \Omega)^{(1/2)} = 0.707$ V or 57 dBmV.

3.1.22
decision feedback equalizer
DFE
nonlinear equalizer that uses a feedback loop based on previously decoded symbols

3.1.23
deterministic jitter
DJ
jitter (see 3.1.48) with non-Gaussian distribution that is bounded in amplitude and has specific causes

Note 1 to entry: See MJSQ.

3.1.24
direct current
D.C.
non-A.C. component of a signal

Note 1 to entry: In this standard, all frequency components below 100 kHz.

3.1.25
disparity
difference between the number of ones and zeros in a character

Note 1 to entry: See SPL.

3.1.26
dispersion
signal pulse broadening and distortion from all causes

3.1.27
duty cycle distortion
DCD
one-half of the difference of the average width of a one and the average width of a zero in a signal waveform eye pattern measurement

Note 1 to entry: See MJSQ.

3.1.28
dword
sequence of four contiguous bytes or four contiguous characters considered as a unit

Note 1 to entry: See SPL.

3.1.29
electromagnetic interference
EMI
any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics/electrical equipment

3.1.30
enclosure
box, rack, or set of boxes providing the powering, cooling, mechanical protection, EMI protection, and external electronic interfaces for one or more end device(s) (see 3.1.34) and/or expander device(s) (see SPL)

Note 1 to entry: The enclosure provides the outermost electromagnetic boundary and acts as an EMI barrier.

3.1.31
enclosure in port
set of expander phys with subtractive routing attributes using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL.

3.1.32
enclosure out port
set of expander phys with table routing attributes in an expander device that does not support table-to-table attachment using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL.

3.1.33
enclosure universal port
set of expander phys with table routing attributes in an expander device that supports table-to-table attachment using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL.

3.1.34
end device
SAS device or SATA device that is not contained within an expander device (see 3.1.36)

Note 1 to entry: See SPL.

3.1.35
etch
printed circuit board copper conductor path

3.1.36
expander device
device that is part of a service delivery subsystem (see SAM-4), facilitates communication between SAS devices (see 3.1.80) and SATA devices (see 3.1.83)

Note 1 to entry: See SPL.

3.1.37
expander phy
phy in an expander device that interfaces to a service delivery subsystem (see SAM-4)

3.1.38
expander port
expander device object that interfaces to a service delivery subsystem (see SAM-4) and to SAS ports in other devices

Note 1 to entry: See SPL.

3.1.39
external connector
bulkhead connector (see 3.1.14) that carries signals into and out of an enclosure (see 3.1.30) and exits the enclosure with only minor compromise to the shield effectiveness of the enclosure (e.g., a Mini SAS 4x receptacle or Mini SAS HD receptacle)

Note 1 to entry: See 5.4.3.4.

3.1.40
eye contour
locus of points in a signal level versus time eye diagram where the CDF of 10^{-12} in the actual signal population exists

Note 1 to entry: Comparison of the measured eye contour to the jitter eye mask determines whether a jitter eye mask violation has occurred.

Note 2 to entry: See 5.7.3 and MJSQ.

3.1.41
fall time
time interval for the falling signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this standard, the measurement points are the 80 % and 20 % voltage levels.

Note 2 to entry: See also rise time (see 3.1.79).

3.1.42
fanout cable assembly
cable assembly with one connector on one end and multiple connectors on the other end

Note 1 to entry: See 5.4.4.1.3.

3.1.43
field
group of one or more contiguous bits

3.1.44
golden phase lock loop
golden PLL
function that conforms to the jitter timing reference frequency response requirements in MJSQ that extracts the jitter timing reference from the data stream under test to be used as the timing reference for the instrument used for measuring the jitter in the signal under test

Note 1 to entry: See MJSQ.

3.1.45
idle time
part of an OOB signal (see 3.1.60) where OOB idle (see 3.1.16) is being transmitted

Note 1 to entry: See 5.9.

3.1.46
insertion loss
ratio of incident power to delivered power

Note 1 to entry: The dB magnitude of S_{12} or S_{21} is the negative of insertion loss in dB.

Note 2 to entry: The insertion loss ratio is usually expressed in dB.

Note 3 to entry: See clause D.10.

3.1.47
intersymbol interference
ISI
reduction in the distinction of a pulse caused by overlapping energy from neighboring pulses

Note 1 to entry: Neighboring pulses are pulses that are close enough to have significant energy overlapping the affected pulse and does not imply or exclude adjacent pulses (i.e., many bit times (see 3.1.5) may separate the pulses, especially in the case of reflections).

Note 2 to entry: ISI may result in DDJ and vertical eye closure.

Note 3 to entry: Several mechanisms produce ISI (e.g., dispersion, reflections, and circuits that lead to baseline wander).

Note 4 to entry: See MJSQ.

3.1.48
jitter
collection of instantaneous deviations of signal edge times at a defined signal level of the signal from the reference times for those events

Note 1 to entry: Reference times such as times defined by the jitter timing reference.

Note 2 to entry: See MJSQ.

3.1.49
jitter timing reference
signal used as the basis for calculating the jitter in the signal under test

Note 1 to entry: See MJSQ.

3.1.50
jitter tolerance
ability of the receiver device to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal applied to the receiver device compliance point

Note 1 to entry: See MJSQ.

3.1.51
jitter tolerance pattern
JTPAT
test pattern for jitter testing

Note 1 to entry: See 5.7.3.5 and Annex A.

3.1.52
least mean square
LMS
algorithm for adaptively adjusting the tap coefficients of a DFE (see 3.1.22) based on the difference between the desired and actual signal

3.1.53
managed connector category
category of connectors that support a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.54
near-end crosstalk
NEXT
crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the disturbing channel

Note 1 to entry: The terminals of the disturbed channel, at which the near-end crosstalk is present, and the energized terminals of the disturbing channel are usually near each other.

3.1.55
negation time
part of an OOB signal during which OOB idle is transmitted after the last OOB burst

Note 1 to entry: See 5.9.

3.1.56
OOB burst
transmission of signal transitions or ALIGN3 primitives for a burst time (see 3.1.7)

Note 1 to entry: See 5.9.1.

3.1.57
OOB idle
transmission of D.C. idle (see 3.1.16) when D.C. mode (see 3.1.17) is enabled, or a defined sequence of dwords when optical mode (see 3.1.61) is enabled

3.1.58
OOB interval
time basis for burst times (see 3.1.7), idle times (see 3.1.45), negation times (see 3.1.55), and signal times (see 3.1.90) used to create OOB signals (see 3.1.60)

Note 1 to entry: See 5.9.1.

3.1.59
OOB sequence
sequence where two phys exchange OOB signals (see 3.1.60)

Note 1 to entry: See SPL.

3.1.60
OOB signal
pattern of idle time (see 3.1.45), burst time (see 3.1.7), and negation time (see 3.1.55) used during the link reset sequence

Note 1 to entry: See 5.9.

3.1.61
optical mode
mode in which a defined sequence of dwords is used during the idle time (see 3.1.45) and negation time (see 3.1.55) of an OOB signal (see 3.1.60)

Note 1 to entry: See 5.9.

3.1.62
part per million
ppm
dimensionless unit used to express signal clock frequency deviation relative to the nominal reference frequency

Note 1 to entry: The value for ppm is obtained by multiplying the fractional variation of the measured signal clock frequency from the nominal signal clock frequency value by 1 million.

3.1.63
passive cable assembly
cable assembly (see 3.1.9) that does not require external power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.64
passive TxRx connection
complete simplex signal path between the transmitter circuit (see 3.1.98) and receiver circuit (see 3.1.72) that does not include powered circuitry used in the transmission of the signal through the TxRx connection (see 3.1.101)

Note 1 to entry: See 5.5.1.

3.1.65
phy
object in a device that is used to interface to other devices

Note 1 to entry: Other devices are, for example, an expander phy (see 3.1.37) or a SAS phy (see 3.1.81).

Note 2 to entry: See 4.1.

3.1.66
physical link
two differential signal pairs, one pair in each direction, that connect two physical phys (see 3.1.68)

Note 1 to entry: See 4.1.

3.1.67
physical link rate
link rate between two physical phys established as a result of speed negotiation between those phys

3.1.68
power on
power being applied

3.1.69
probe point
physical position in a test load where signal characteristics for compliance points are measured

Note 1 to entry: See 5.6.

3.1.70
random jitter
RJ
jitter (see 3.1.48) characterized by a Gaussian distribution and that is unbounded

Note 1 to entry: See MJSQ.

3.1.71
rate
data transfer rate of a physical or logical link

Note 1 to entry: Typical data transfer rates are 1.5 Gbit/s, 3 Gbit/s, or 6 Gbit/s.

3.1.72
receiver circuit
electronic circuit that converts an analog serial input signal to a logic signal

3.1.73
receiver device
Rx
device downstream from a receiver device compliance point (see 3.1.12) containing a portion of the physical link and a receiver circuit (see 3.1.72)

3.1.74
reference receiver device
set of parameters defining electrical performance characteristics that provide a set of minimum electrical performance requirements for a receiver device and that are also used in mathematical modeling to determine compliance of a TxRx connection or transmitter device

Note 1 to entry: See 5.7.5.7.3.

3.1.75
reference transmitter device
set of parameters defining electrical performance characteristics of a transmitter device that are used in mathematical modeling to determine compliance of a TxRx connection

Note 1 to entry: See 5.7.4.6.5.

3.1.76
reference transmitter test load
set of S-parameters defining the electrical characteristics of a TxRx connection used as the basis for transmitter device and receiver device performance evaluation through mathematical modeling

Note 1 to entry: See 5.6.5.

3.1.77
reflection coefficient
ρ
ratio of reflected voltage to incident voltage

3.1.78
return loss
ratio of incident power to reflected power

Note 1 to entry: The dB magnitude of S_{11} or S_{22} is the negative of return loss in dB.

Note 2 to entry: Return loss is usually expressed in decibel (dB).

Note 3 to entry: See clause D.10.

3.1.79
rise time
time interval for the rising signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this standard, the measurement points are the 20 % and 80 % voltage levels.

Note 2 to entry: See fall time (see 3.1.41).

3.1.80
SAS device
SAS initiator device and/or a SAS target device

Note 1 to entry: See SPL.

3.1.81
SAS phy
phy in a SAS device (see 3.1.80) that interfaces to a service delivery subsystem

Note 1 to entry: See SAM-4.

3.1.82
SAS target device
device containing SSP, STP, and/or SMP target ports in a SAS domain

Note 1 to entry: See SPL.

3.1.83
SATA device
ATA device (see ATA8-AAM) that contains a SATA device port in an ATA domain

Note 1 to entry: See SPL.

3.1.84
SATA phy
phy in a SATA device or SATA port selector that interfaces to a service delivery subsystem

Note 1 to entry: For ATA device (see SPL), for SATA port selector (see SPL), and for a service delivery subsystem (see SAM-4).

Note 2 to entry: Analogous to a SAS phy (see 3.1.81).

3.1.85
Serial ATA
protocol defined by SATA

Note 1 to entry: See SATA.

3.1.86
Serial Attached SCSI
set of protocols defined in SPL and the interconnect defined by this standard

Note 1 to entry: See SAS.

3.1.87
signal
detectable transmitted energy that is used to carry information

3.1.88
signal amplitude
property of the overall signal (see 3.1.87) that describes the peak or peak-to-peak values of the signal level (see 3.1.89)

3.1.89
signal level
instantaneous intensity of a signal (see 3.1.87) measured in volts

3.1.90
signal time
time of an OOB signal (see 3.1.60), consisting of six burst times (see 3.1.7), six idle times (see 3.1.45), and one negation time (see 3.1.55)

Note 1 to entry: See 5.9.

3.1.91
signal tolerance
ability of the receiver device to recover transmitted bits in an incoming data stream with maximum jitter and minimum amplitude

Note 1 to entry: See MJSQ.

3.1.92
sinusoidal jitter
SJ
single frequency jitter (see 3.1.48) applied during signal tolerance testing

3.1.93
spread spectrum clocking
SSC
technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions

Note 1 to entry: The operating frequency of a transmitted signal is the physical ink rate.

Note 2 to entry: See SPL.

3.1.94
symbol
smallest unit of data transmission on a physical link

Note 1 to entry: The smallest unit of data is a bit.

Note 2 to entry: A symbol represents a single transition if the maximum transition rate (i.e., a 0101b pattern) is occurring.

3.1.95
total jitter
TJ
jitter (see 3.1.48) from all sources

Note 1 to entry: See MJSQ.

3.1.96
trained
physical link rate negotiated with Train-SNW

Note 1 to entry: See SPL.

3.1.97
transceiver
physical entity that contains both a transmitter device (see 3.1.100) and a receiver device (see 3.1.73)

3.1.98
transmitter circuit
electronic circuit that converts a logic signal to an analog serial output signal

3.1.99
transmitter compliance transfer function
TCTF
mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask

Note 1 to entry: See 5.7.4.1.

3.1.100
transmitter device
Tx
device upstream from a transmitter device compliance point (see 3.1.12) containing a portion of the physical link and a transmitter circuit (see 3.1.98)

3.1.101
TxRx connection
complete simplex signal path between the transmitter circuit (see 3.1.98) and receiver circuit (see 3.1.72)

Note 1 to entry: See 5.5.1.

3.1.102
TxRx connection segment
that portion of a TxRx connection (see 3.1.101) delimited by separable connectors or changes in the conductive material

Note 1 to entry: See 5.5.1.

3.1.103
unit interval
UI
normalized, dimensionless, nominal duration of a symbol (see 3.1.94)

Note 1 to entry: Typical *UI*s are $666.\overline{6}$ ps at 1.5 Gbit/s, $333.\overline{3}$ ps at 3 Gbit/s, and $166.\overline{6}$ ps at 6 Gbit/s, for example.

Note 2 to entry: The *UI* is the reciprocal of the baud rate (i.e., $UI = 1 / f_{baud}$) (see 3.1.3).

3.1.104
unmanaged active connector category
category of connectors that support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2), but do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.105
unmanaged passive connector category
category of connectors that do not support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2) and do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.106
untrained
physical link rate not negotiated with Train-SNW

Note 1 to entry: See SPL.

3.1.107
usage variable
SASWDP parameter set to a value that determines if the stressor file is to be added to the simulation

Note 1 to entry: See Annex B.

3.1.108
voltage modulation amplitude
VMA
difference in electrical voltage of a signal (see 3.1.87) between the stable one level and the stable zero level

3.1.109
waveform dispersion penalty
WDP
simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device

Note 1 to entry: See 5.7.4.6.1 and Annex B.

3.2 Symbols and abbreviations

3.2.1 Abbreviations

See clause 2 for abbreviations of standards bodies (e.g., ISO). Abbreviations used in this standard:

Abbreviation	Meaning
A.C.	alternating current (a.c. within a sentence)
ATA	AT attachment (see 3.1.1)
ATAPI	AT attachment packet interface
ATA8-AAM	AT Attachment - 8 ATA/ATAPI Architecture Model standard (see clause 2)
AWG	American wire gauge (see ASTM Standard B 258-02) (see clause 2)
BER	bit error ratio (see 3.1.4)
BUJ	bounded uncorrelated jitter (see 3.1.6)
CDF	cumulative distribution function (see 3.1.15)
CDR	clock data recovery (see 3.1.10)
CIC	compliance interconnect channel (see SATA)
CJTPAT	compliant jitter tolerance pattern (see 3.1.13)
CR	inter-enclosure (i.e., cabinet) receiver device compliance point (see 5.3)
CT	inter-enclosure (i.e., cabinet) transmitter device compliance point (see 5.3)
D.C.	direct current (see 3.1.24)
DCD	duty cycle distortion (see 3.1.27)
DDJ	data dependent jitter (see 3.1.18)
DFE	decision feedback equalizer (see 3.1.22)
DJ	deterministic jitter (see 3.1.23)
EMI	electromagnetic interference (see 3.1.29)
ESD	electrostatic discharge
G1	generation 1 physical link rate (i.e., 1.5 Gbit/s)
G2	generation 2 physical link rate (i.e., 3 Gbit/s)
G3	generation 3 physical link rate (i.e., 6 Gbit/s)
Gen1i	SATA generation 1 physical link rate (i.e., 1.5 Gbit/s) (see SATA)
Gen2i	SATA generation 2 physical link rate (i.e., 3 Gbit/s) (see SATA)
Gen3i	SATA generation 3 physical link rate (i.e., 6 Gbit/s) (see SATA)

Abbreviation	Meaning
GPIO	general purpose input/output
HD	high-density
IR	intra-enclosure (i.e., internal) receiver device compliance point (see 5.3)
ISI	intersymbol interference (see 3.1.47)
IT	intra-enclosure (i.e., internal) transmitter device compliance point (see 5.3)
JMD	jitter measurement device
JTF	jitter transfer function (see 5.7.3.2)
JTPAT	jitter tolerance pattern (see 3.1.51)
LED	light-emitting diode
LMS	least mean square (see 3.1.52)
N/A	not applicable
NEXT	near-end crosstalk (see 3.1.54)
OOB	out-of-band
OOBI	out-of-band interval (see 3.1.58)
PCB	printed circuit board
PJ	periodic jitter
PLL	phase lock loop
P-P	peak-to-peak
RD	running disparity (see SPL)
RJ	random jitter (see 3.1.70)
RMS	root mean square
RTTL	reference transmitter test load (see 3.1.76)
Rx	receiver device (see 3.1.73)
SAM-4	SCSI Architecture Model - 4 standard (see clause 2)
SAS	Serial Attached SCSI (see 3.1.86)
SATA	Serial ATA (see 3.1.85) or the Serial ATA 3.0 specification (see clause 2)
SCSI	Small Computer System Interface
SGPIO	serial GPIO
SJ	sinusoidal jitter (see 3.1.92)
SMA	subminiature version A connector
SPC-4	SCSI Primary Commands - 4 standard
SPL	SAS Protocol Layer (see clause 2)
SSC	spread spectrum clocking
STP	Serial ATA Tunneled Protocol
TCTF	transmitter compliance transfer function (see 3.1.99)
TDNA	time domain network analyzer (i.e., TDR/TDT plus analysis software that performs a VNA-style output)
TDR	time domain reflectometer
TDT	time domain transmission
TJ	total jitter (see 3.1.95)
Tx	transmitter device (see 3.1.100)
VMA	voltage modulation amplitude (see 3.1.108)
VNA	vector network analyzer

Abbreviation	Meaning
WDP	waveform dispersion penalty (see 3.1.109)

3.2.2 Units

Units used in this standard:

Units	Meaning
dB	decibel (see 3.1.19)
dBm	decibel milliwatts (see 3.1.21)
dBmV	decibel millivolts (see 3.1.20)
Gbit/s	gigabits per second (i.e., 10^9 bits per second)
GHz	gigahertz (i.e., 10^9 cycles per second)(i.e., s^{-9})
Hz	hertz (i.e., cycles per second)(i.e., s^{-1})
kHz	kilohertz (i.e., 10^3 cycles per second)(i.e., s^{-3})
µA	microampere (i.e., 10^{-6} amperes)
µs	microsecond (i.e., 10^{-6} seconds)
m	meter
mA	milliampere (i.e., 10^{-3} amperes)
MB/s	megabytes per second (i.e., 10^6 bytes per second)
MHz	megahertz (i.e., 10^6 cycles per second)(i.e., s^{-6})
ms	millisecond (i.e., 10^{-3} seconds)
mV	millivolt (i.e., 10^{-3} volts)
mW	milliwatt (i.e., 10^{-3} watts)
nF	nanofarad (i.e., 10^{-9} farads)
ns	nanosecond (i.e., 10^{-9} seconds)
ppm	parts per million (i.e., 10^{-6})
ps	picosecond (i.e., 10^{-12} seconds)
r.m.s.	root mean square (i.e., quadratic mean)
s	second (unit of time)
sgn	signum function (i.e., sign function)
UI	unit interval (see 3.1.103)
V	volt
W	watt

3.2.3 Symbols

Symbols used in this standard:

Symbols	Meaning
Dxx.y	data character (see 3.1.18)
S_{ij}	S-parameter for port j to port i (see D.10)
S_{CCij}	S-parameter for common-mode to common-mode port j to port i (see D.10)
S_{CDij}	S-parameter for differential to common-mode port j to port i (see D.10)
S_{DCij}	S-parameter for common-mode to differential port j to port i (see D.10)
S_{DDij}	S-parameter for differential to differential port j to port i (see D.10)
Δ (Delta)	difference operator
ϕ (phi)	phase

Symbols	Meaning
π (pi)	3.141 59... , the ratio of the circumference of a circle to its diameter
ρ (rho)	reflection coefficient (see 3.1.77)
τ (tau)	time constant
®	registered trademark

3.2.4 Mathematical operators

Mathematical operators used in this standard:

Mathematical Operators	Meaning
e	2.718 28..., the base of the natural (i.e., hyperbolic) system of logarithms
sgn	signum function (i.e., sign function)
^	exclusive logical OR
<	less than
≤	less than or equal to
>	greater than
≥	greater than or equal to
±	plus or minus
×	multiplication
/	division
|v|	the absolute value (i.e., magnitude) of v
~	approximately equal to

3.3 Keywords

3.3.1
invalid
a keyword used to describe an illegal or unsupported bit, byte, word, field or code value; receipt of an invalid bit, byte, word, field or code value shall be reported as an error

3.3.2
mandatory
a keyword indicating an item that is required to be implemented as defined in this standard

3.3.3
may
a keyword that indicates flexibility of choice with no implied preference (equivalent to “may or may not”)

3.3.4
may not
keywords that indicate flexibility of choice with no implied preference (equivalent to “may or may not”)

3.3.5
obsolete
a keyword indicating that an item was defined in prior standards but has been removed from this standard

3.3.6
optional
a keyword that describes features that are not required to be implemented by this standard; however, if any optional feature defined in this standard is implemented, then it shall be implemented as defined in this standard

3.3.7
reserved
a keyword referring to bits, bytes, words, fields and code values that are set aside for future standardization; a reserved bit, byte, word or field shall be set to zero, or in accordance with a future extension to this standard; recipients are not required to check reserved bits, bytes, words or fields for zero values. Receipt of reserved code values in defined fields shall be reported as an error

3.3.8
restricted
a keyword referring to bits, bytes, words, and fields that are set aside for other identified standardization purposes; a restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears

3.3.9
shall
a keyword indicating a mandatory requirement; designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard

3.3.10
should
a keyword indicating flexibility of choice with a strongly preferred alternative (equivalent to “is strongly recommended”)

3.3.11
vendor specific
something (e.g., a bit, field, or code value) that is not defined by this standard and may be used differently in various implementations

3.4 Editorial conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

Names of signals are in all uppercase (e.g., GROUND).

Normal case is used for words having the normal English meaning.

A binary number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Underscores or spaces may be included between characters in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b or 0_0101_1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Underscores or spaces may be included between characters in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h or B_FD8C_FA23h).

A decimal number is represented in this standard by any sequence of digits consisting of only the Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

This standard uses the following conventions for representing decimal numbers:

a) the decimal separator (i.e., separating the integer and fractional portions of the number) is a period;
b) the thousands separator (i.e., separating groups of three digits in a portion of the number) is a space; and
c) the thousands separator is used in both the integer portion and the fraction portion of a number.

Table 1 shows some examples of decimal numbers using various numbering conventions.

Table 1 — Numbering conventions

French	English	This standard
0,6	0.6	0.6
3,141 592 65	3.14159265	3.141 592 65
1 000	1,000	1 000
1 323 462,95	1,323,462.95	1 323 462.95

A decimal number represented in this standard with an overline over one or more digits following the decimal point is a number where the overlined digits are infinitely repeating (e.g., $666.\overline{6}$ means 666.666 666... or 666 2/3, and $12.\overline{142\ 857}$ means 12.142 857 142 857... or 12 1/7).

Lists sequenced by letters (e.g., a) red, b) blue, c) green) show no ordering relationship between the listed items. Lists sequenced by numbers (e.g., 1) red, 2) blue, 3) green) show an ordering relationship between the listed items.

In the event of conflicting information the precedence for requirements defined in this standard is:

1) text;
2) tables; and
3) figures.

Notes do not constitute any requirements for implementers.

4 General

4.1 Physical links and phys

A physical link is a set of four wires used as two differential signal pairs. One differential signal transmits in one direction while the other differential signal transmits in the opposite direction. Data may be transmitted in both directions simultaneously.

A physical phy contains a transceiver which electrically interfaces to a physical link, which attaches to another physical phy.

Phys are contained in ports (see SPL). Phys interface to a service delivery subsystem (see SAM-4).

Figure 3 shows two phys attached with a physical link.

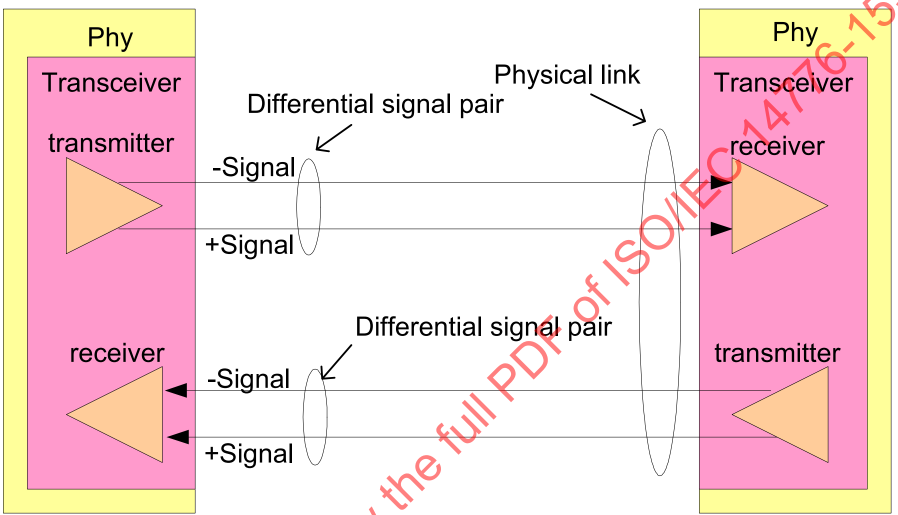


Figure 3 — Physical links and phys

An attached phy is the phy to which a phy is attached over a physical link.

The transceiver follows the electrical specifications defined in 5.7. Phys transmit and receive bits at physical link rates defined in 5.7. The bits are parts of 10-bit characters (see SPL), which are parts of dwords (see SPL). The physical link rates supported by a phy are specified or indicated by the following fields in the SMP DISCOVER response (see SPL), the SMP PHY CONTROL request (see SPL), and the Phy Control and Discover mode page (see SPL):

a) the NEGOTIATED PHYSICAL LINK RATE field;
b) the HARDWARE MINIMUM PHYSICAL LINK RATE field;
c) the HARDWARE MAXIMUM PHYSICAL LINK RATE field;
d) the PROGRAMMED MINIMUM PHYSICAL LINK RATE field; and
e) the PROGRAMMED MAXIMUM PHYSICAL LINK RATE field.

4.2 Phy test functions

Phy test functions (e.g., transmission of test patterns) are used for phy and interconnect characterization and diagnosis. The phy may be attached to test equipment while performing a phy test function. See SPL for the optional mechanisms for invoking phy test function.

Each phy test function is optional.

If the phy test function requires a specific phy test pattern and/or phy test function physical link rate, then the mechanism for invoking the phy test function (see SPL) also specifies the phy test pattern and phy test function physical link rate.

5 Physical layer

5.1 Physical layer overview

The physical layer defines:

a) passive interconnect (e.g., connectors and cable assemblies); and
b) transmitter and receiver device electrical characteristics.

Within this standard, references to connector gender use the terms plug and receptacle as equivalent to the terms free and fixed, respectively, that may be used in the references that define the connectors. Fixed and free terminology has no relationship to the application of the connector.

5.2 Conventions for defining maximum limits for S-parameters

The following values are specified by this standard to define the maximum limits for certain S-parameters (e.g., for cable assemblies and backplanes (see 5.5.3), transmitter devices (see 5.7.4.6.3), and receiver devices (see 5.7.5.7.2)):

a) *L* is the maximum value in dB at the low frequency asymptote;
b) *N* is the maximum value in dB at the Nyquist frequency (i.e., f_{max} / 2)(e.g., 3 GHz for 6 Gbit/s);
c) *H* is the maximum value in dB at the high frequency asymptote;
d) *S* is the slope in dB/decade;
e) f_{min} is the minimum frequency of interest; and
f) f_{max} is the maximum frequency of interest.

The frequencies at which *L* and *H* intersect the slope *S* may or may not be within the region of f_{min} to f_{max}.

Figure 4 shows the values in a graph.

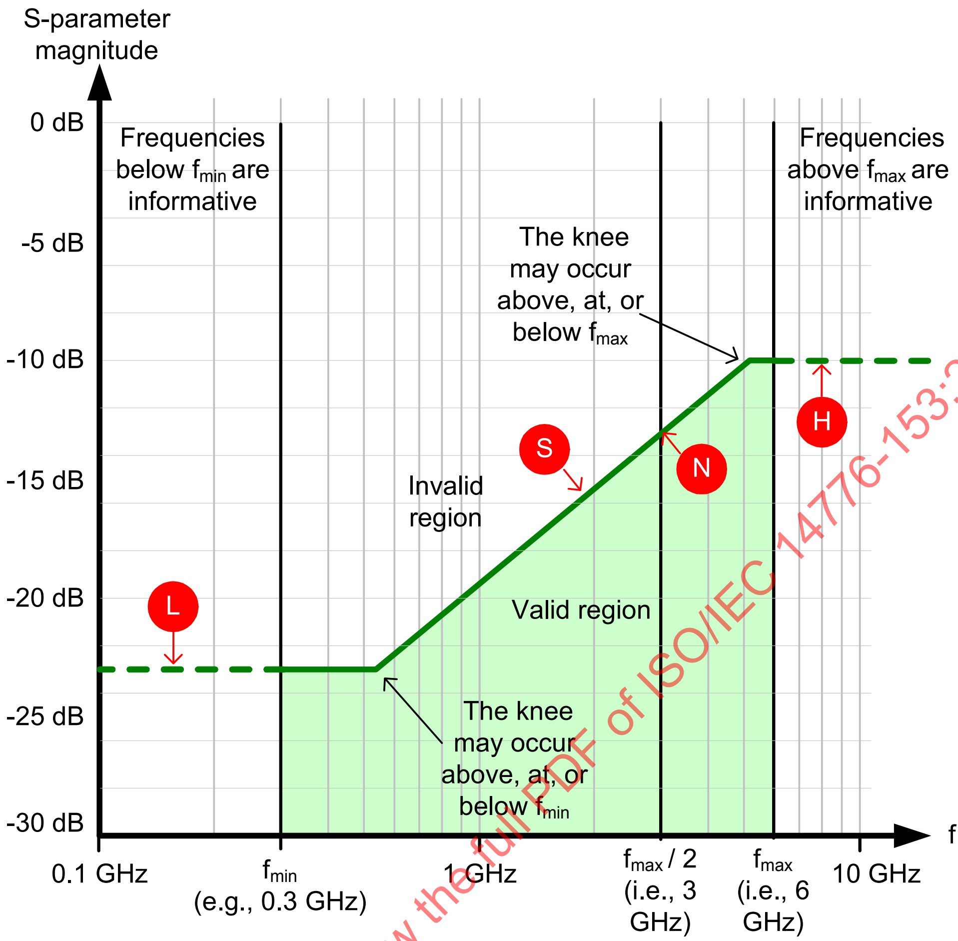


Figure 4 — Maximum limits for S-parameters definitions

5.3 Compliance points

A TxRx connection is the complete simplex signal path between the transmitter circuit and receiver circuit.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in conductive material.

This standard defines the electrical requirements of the signal at the compliance points IT, IR, CT, and CR in a TxRx connection (see table 2). Each compliant phy shall be compatible with these electrical requirements to allow interoperability within a SAS environment.

Signal behavior at separable connectors requires compliance with signal characteristics defined by this standard only if the connectors are identified as compliance points by the supplier of the parts that contain the candidate compliance point.

Signal characteristics for compliance points are measured at physical positions called probe points in a test load (see 5.6). Measurements at the probe points in a test load approximate measurements at the compliance point in the actual TxRx connection. Some components in the test load may be de-embedded as described in clause D.5.

Table 2 — Compliance points

Compliance point	Type	Description
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device, as measured at probe points in a test load attached with an internal connector.
IT_S [a]	intra-enclosure (i.e., internal)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector.
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device, as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector.
CT_S [a]	inter-enclosure (i.e., cabinet)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector.
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.

[a] Because the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device S-parameter specifications do not include the mated connector, transmitter device S-parameter measurement points are at the IT_S compliance point and CT_S compliance point. 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s receiver device S-parameter measurement points are at the IR compliance point and CR compliance point.

The TxRx connection includes the characteristics of the mated connectors at both the transmitter device and receiver device ends. One end of a TxRx connection is a IT_S compliance point or CT_S compliance point, and the other end of the TxRx connection is the corresponding IR compliance point or CR compliance point.

Figure 5 shows the locations of the CT compliance points and CR compliance points using an external cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

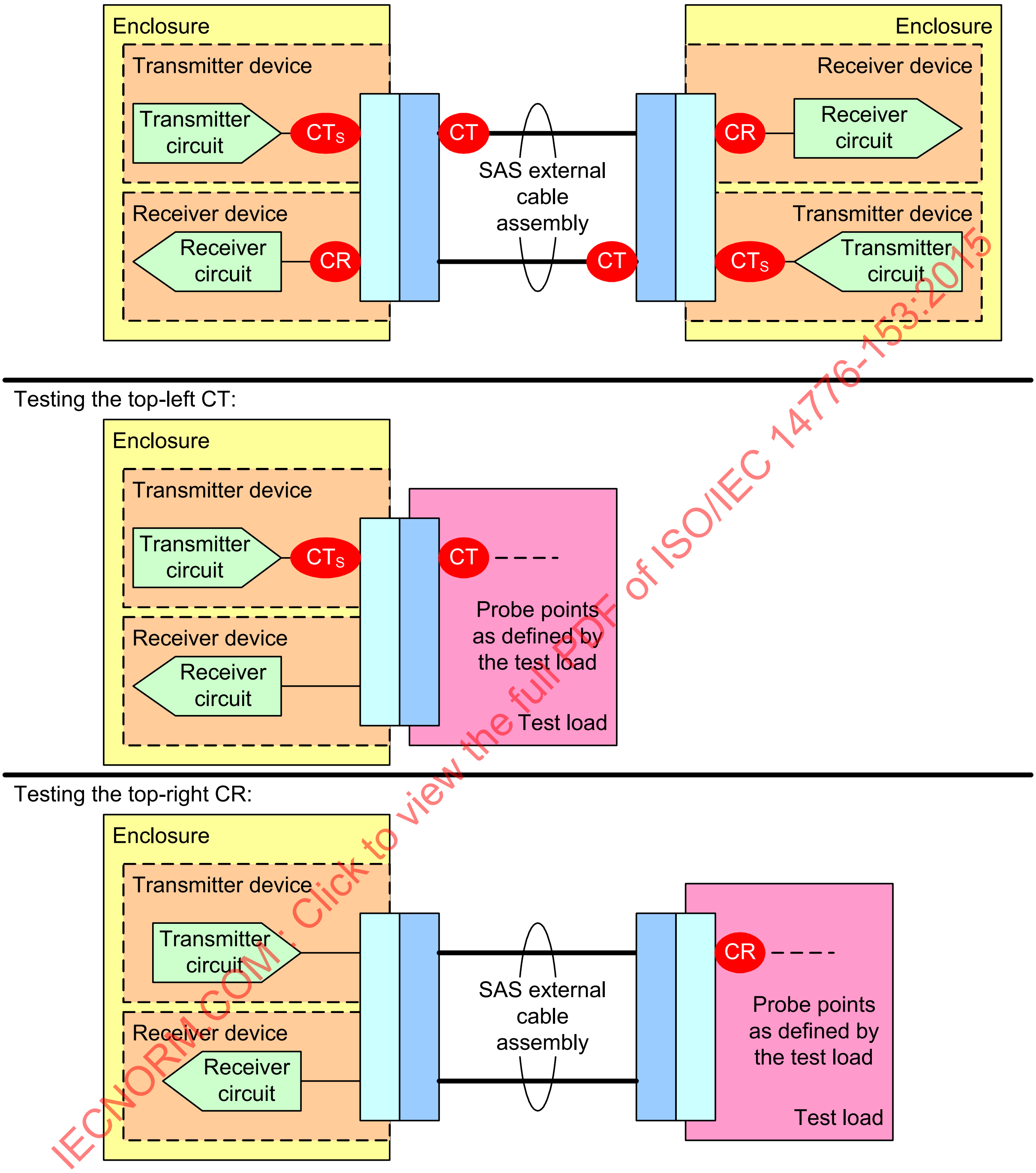


Figure 5 — External cable assembly CT compliance points and CR compliance points

Figure 6 shows the locations of the IT compliance points and IR compliance points using a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3) that is not using SATA, and shows how the compliance points are tested using test loads (see 5.6).

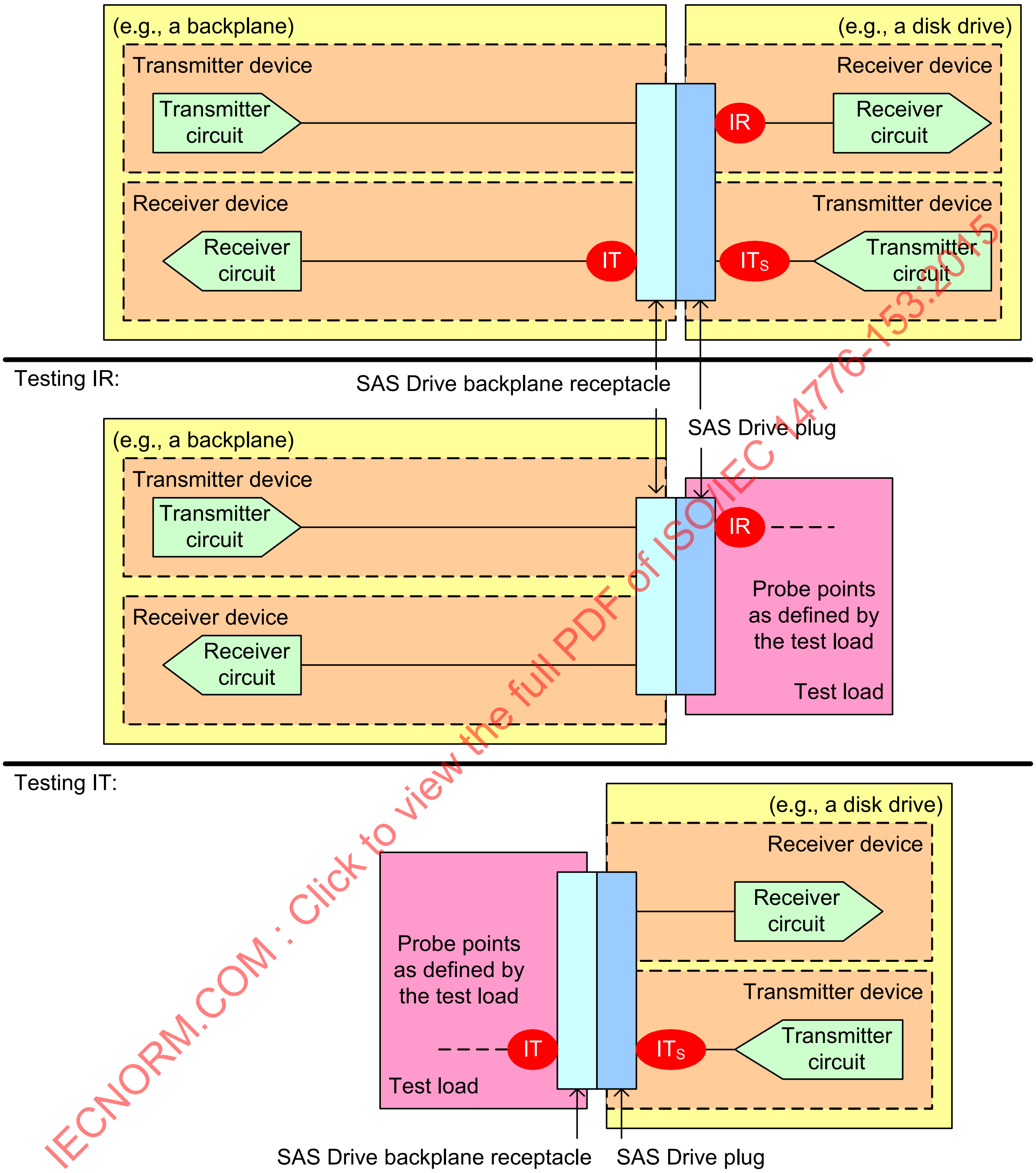


Figure 6 — Backplane with SAS Drive connector IT compliance points and IR compliance points

If the backplane supports SATA, then there are no IT compliance points or IR compliance points. SATA defines the signal characteristics that the SATA phy delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 7.

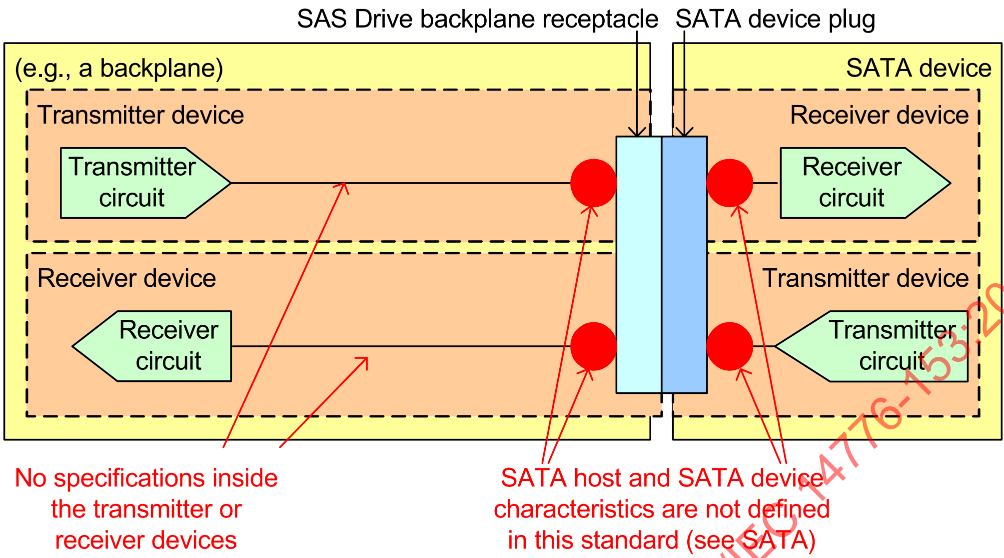


Figure 7 — Backplane with SAS Drive connector compliance points with SATA phy attached

Figure 8 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

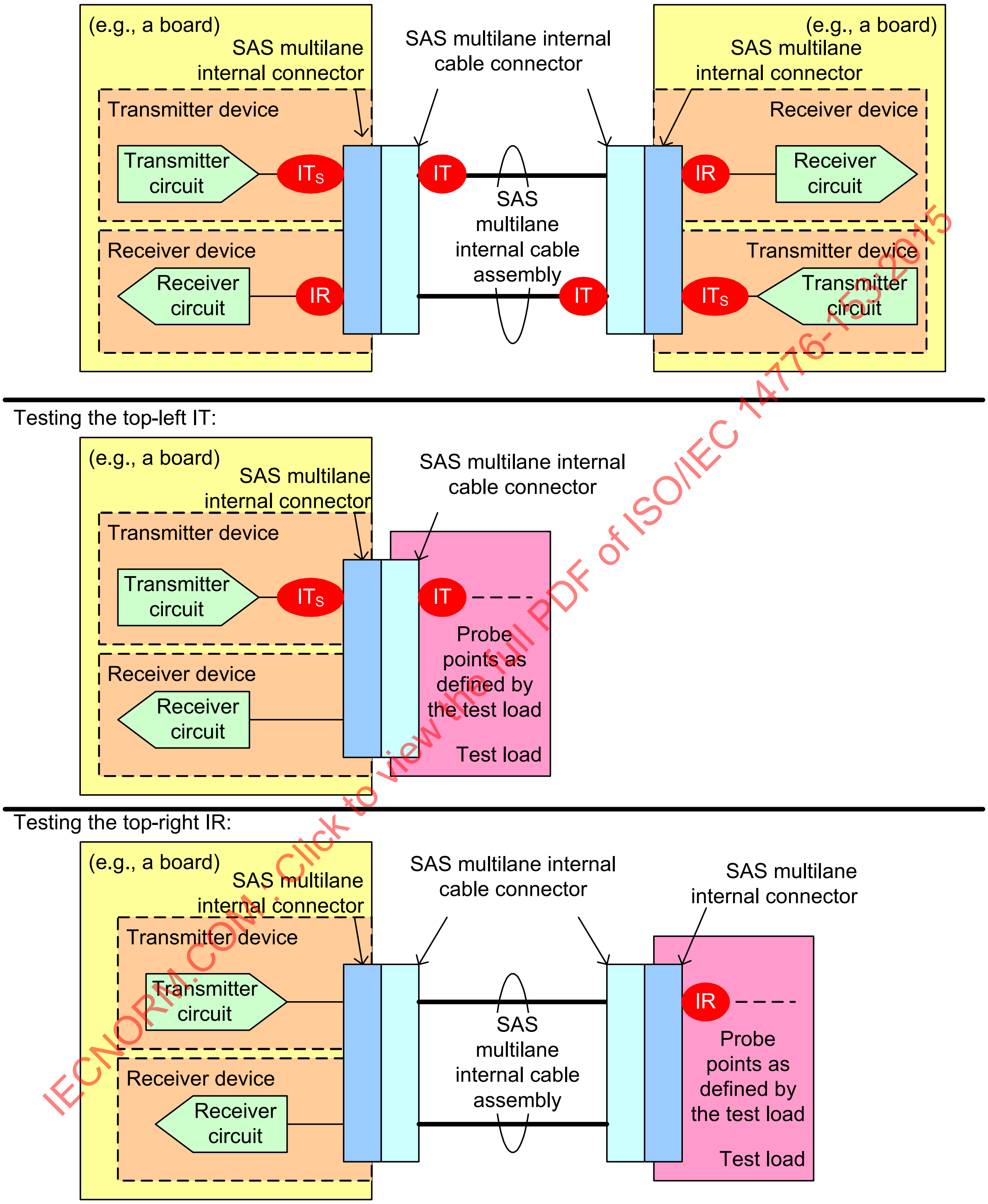


Figure 8 — SAS multilane internal cable assembly IT compliance points and IR compliance points

Figure 9 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3), where the backplane is not attached to a SATA device, and shows how two of the compliance points are tested using test loads (see 5.6).

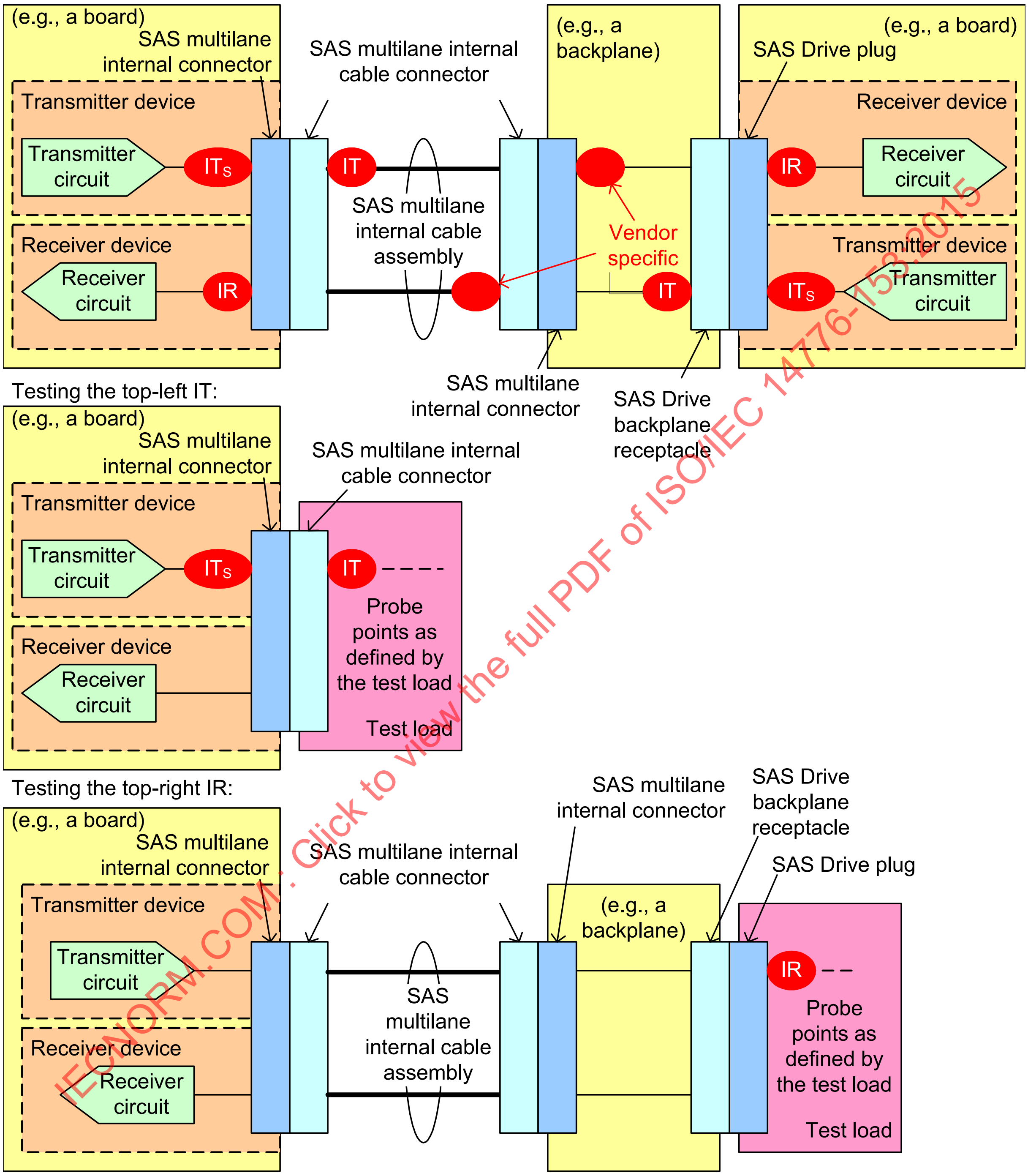


Figure 9 — SAS multilane internal cable assembly and backplane IT compliance points and IR compliance points

Figure 10 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3) that supports being attached to a SATA device. There are no IT compliance points and IR compliance points at the SAS Drive backplane receptacle connector when a SATA device is attached. In that case, SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device. There are compliance points at the SAS multilane internal connector, however.

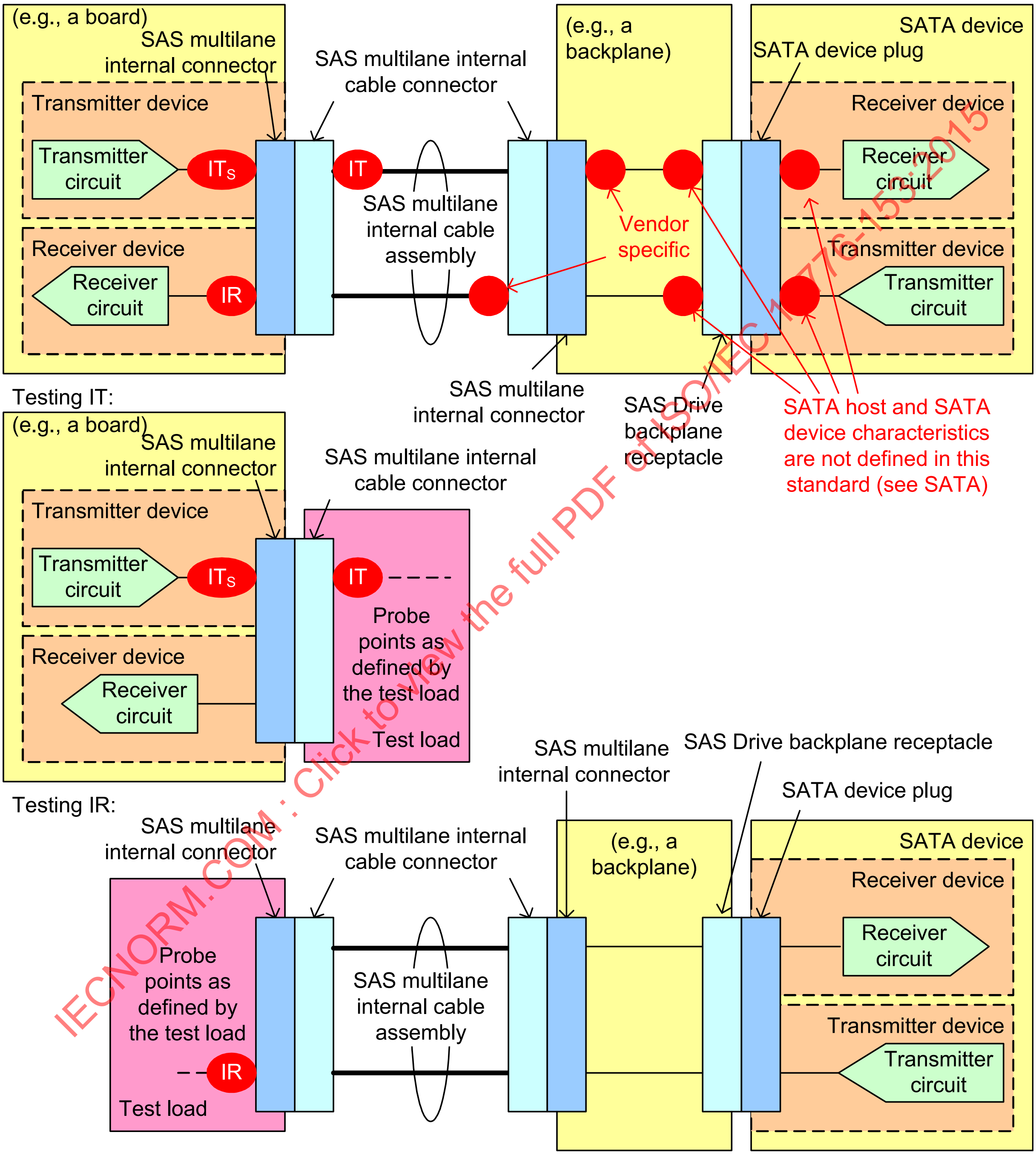


Figure 10 — SAS multilane internal cable assembly and backplane IT compliance points and IR compliance points with SATA device attached

Figure 11 shows the locations of the IT compliance points and IR compliance points using a SAS Drive cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

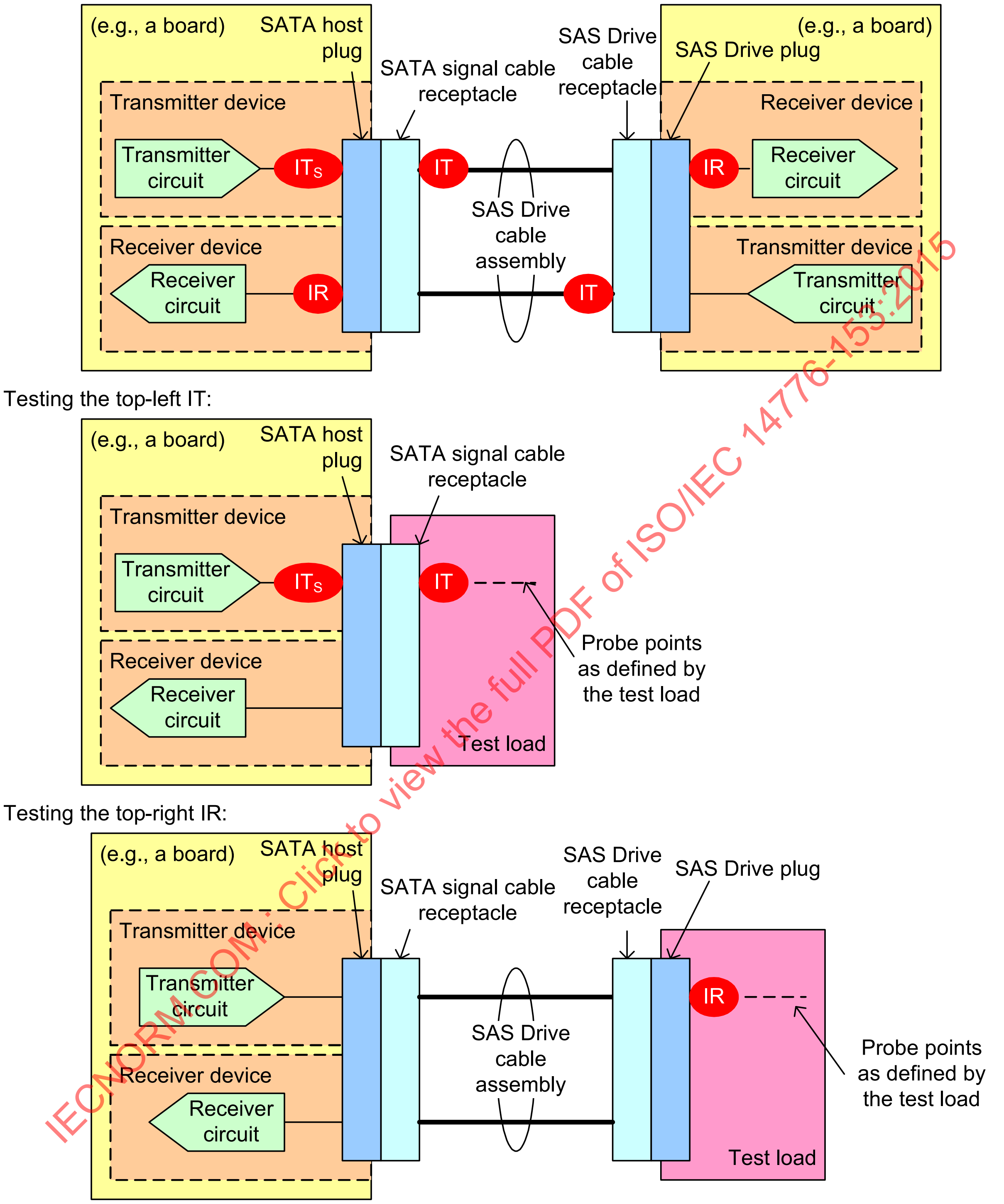


Figure 11 — SAS Drive cable assembly IT compliance points and IR compliance points

5.4 Interconnects

5.4.1 SATA connectors and cable assemblies

Figure 12 shows a representation of the connectors and cables defined by SATA. A SATA host is analogous to a SAS initiator device (see SPL) and a SATA device is analogous to a SAS target device (see SPL).

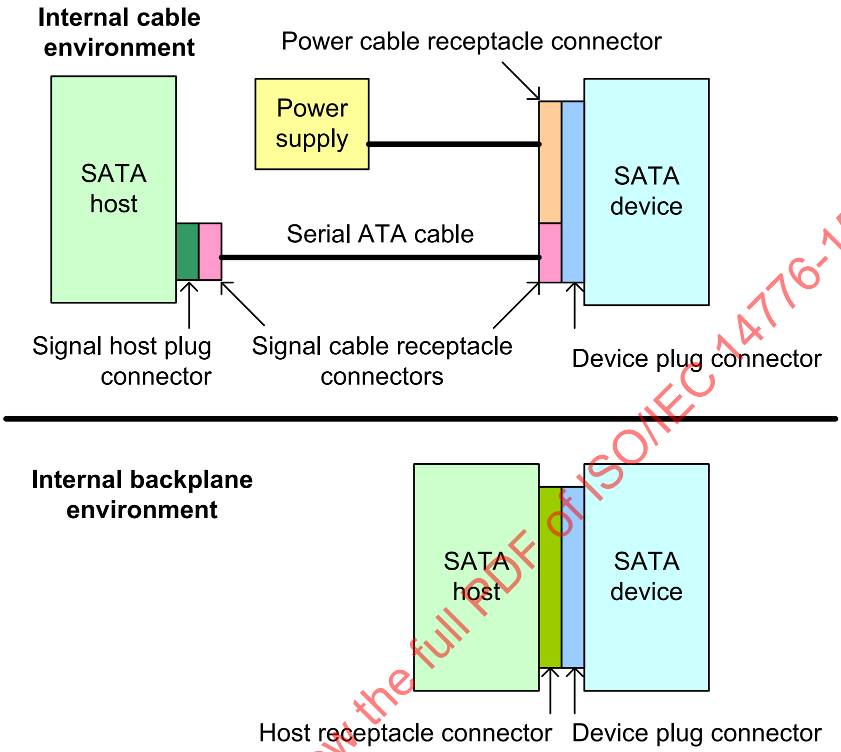


Figure 12 — SATA connectors and cables

5.4.2 SAS connectors and cables

This standard defines SAS Drive cable, SAS Drive backplane, SAS internal cable, and SAS external cable environments.

Figure 13 shows a representation of the SAS Drive cable environments.

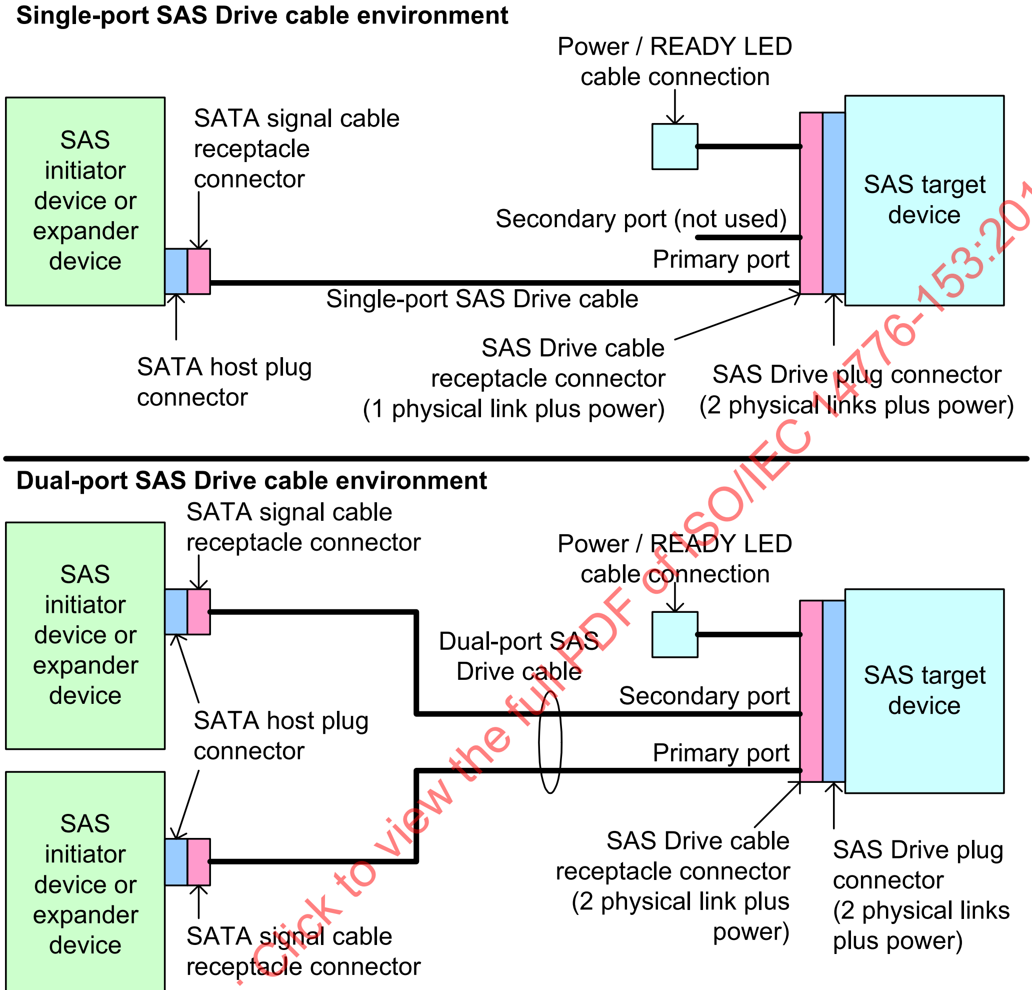


Figure 13 — SAS Drive cable environments

Figure 14 shows a representation of the SAS Drive backplane environment.

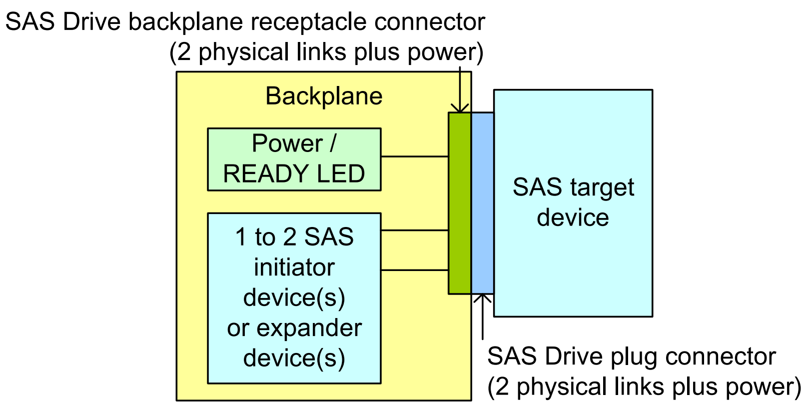


Figure 14 — SAS Drive backplane environment

Figure 15 shows a representation of the SAS external cable environment.

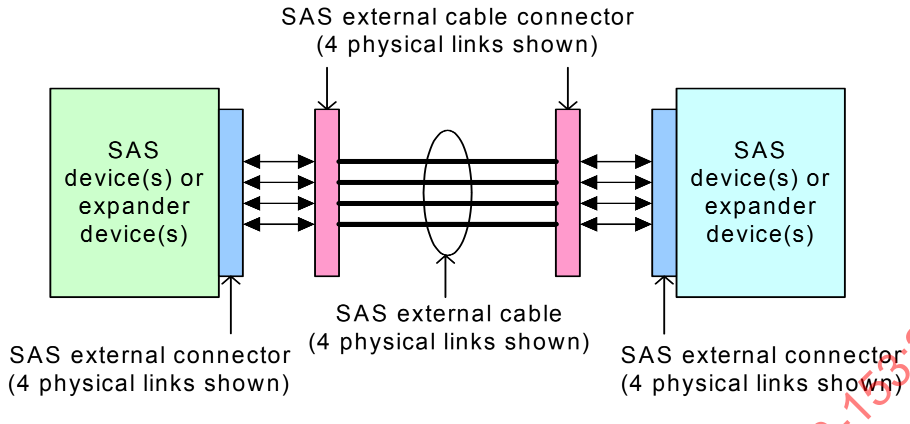


Figure 15 — SAS external cable environment

Figure 16 shows a representation of the SAS internal cable environment attaching a controller to a backplane using a SAS internal symmetric cable (see 5.4.4.1.2).

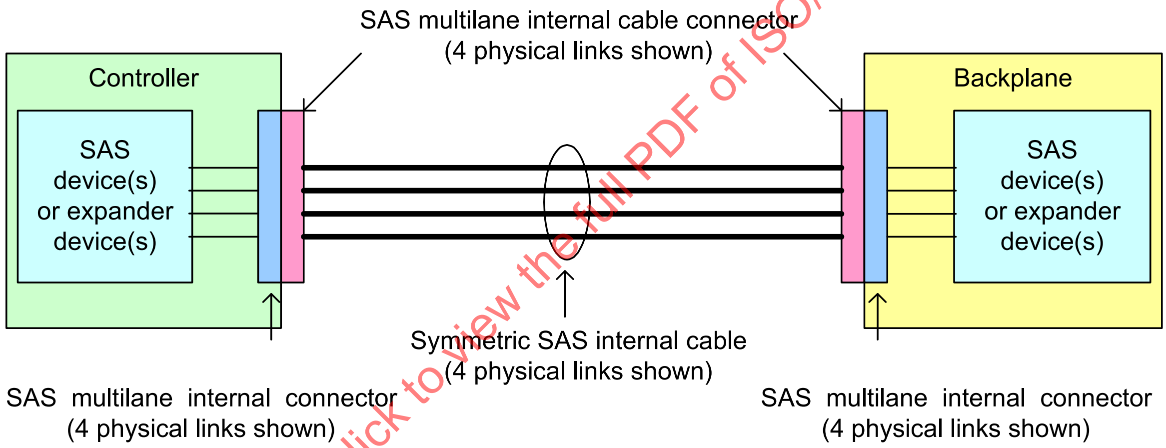


Figure 16 — SAS internal symmetric cable environment - controller to backplane

A SAS internal symmetric cable provides one to eight physical links, and may be used as any combination of wide links and narrow links (see SPL) using those physical links.

Figure 17 shows a representation of the SAS internal cable environment attaching a controller to a controller using a SAS internal symmetric cable (see 5.4.4.1.2). Two controllers may also be attached together with a SAS internal symmetric cable.

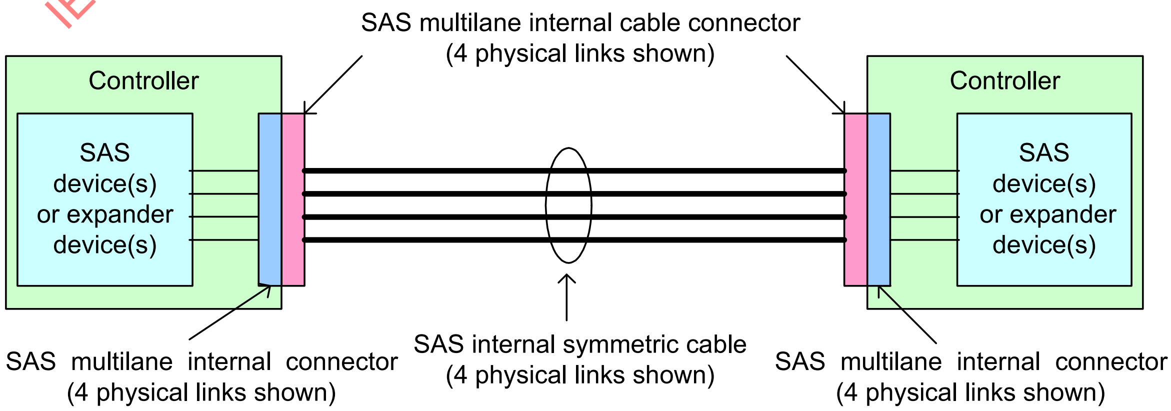


Figure 17 — SAS internal symmetric cable environment - controller to controller

Figure 18 shows a representation of the SAS internal cable environment using a SAS controller-based fanout cable (see 5.4.4.1.3).

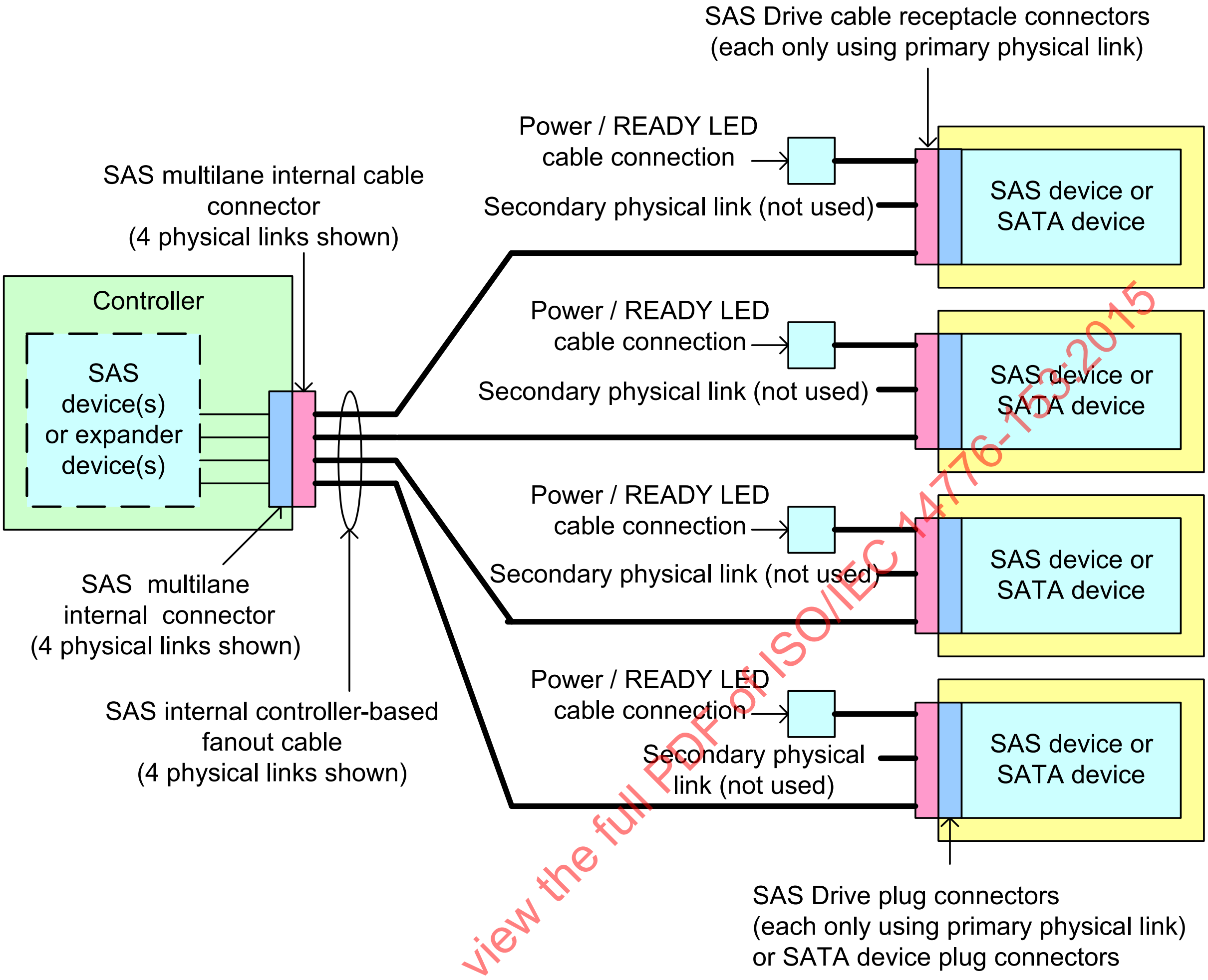


Figure 18 — SAS internal controller-based fanout cable environment

Figure 19 shows a representation of the SAS internal cable environment using a SAS backplane-based fanout cable (see 5.4.4.1.3).

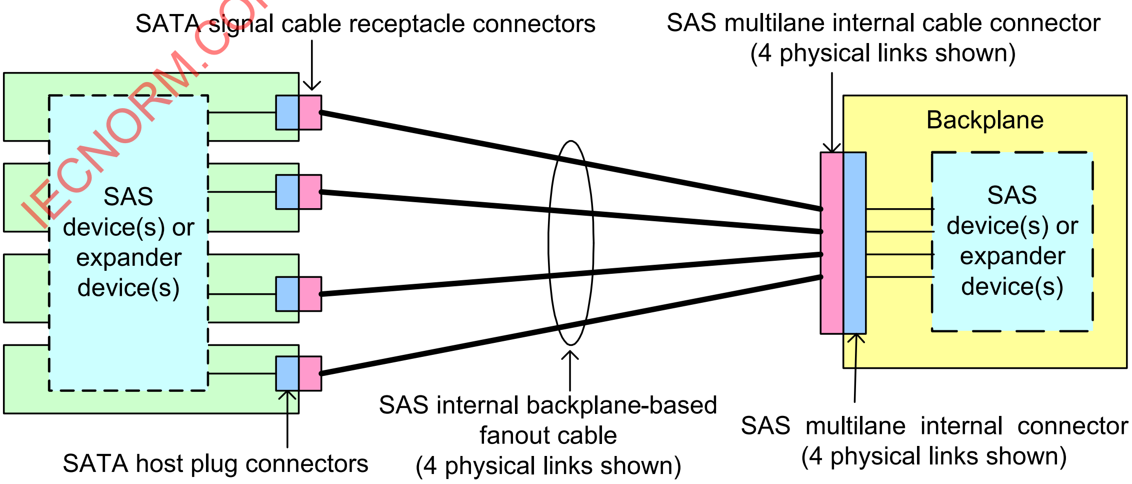


Figure 19 — SAS internal backplane-based fanout cable environment

5.4.3 Connectors

5.4.3.1 Connectors overview

Table 3 summarizes the connectors defined in this standard.

Table 3 — Connectors (part 1 of 2)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	**Physical links**	**Reference**
SATA internal connectors used by SAS					
SATA signal cable receptacle	1	SATA	SATA host plug	1	SATA
SATA host plug	1	SATA	SATA signal cable receptacle	1	SATA
SATA device plug	1	SATA	SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2
			SAS Drive backplane receptacle	2	5.4.3.3.1.3
Micro SATA backplane connector	1	SATA	Micro SATA device plug	1	SATA
Micro SATA power receptacle connector	0	SATA	Micro SATA device plug	1	SATA
Micro SATA device plug	1	SATA	Micro SATA backplane connector	1	SATA
			Micro SAS receptacle	2	5.4.3.3.1.6
SAS internal connectors - SAS Drive connectors					
SAS Drive plug	2	5.4.3.3.1.1	SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2
			SAS Drive backplane receptacle	2	5.4.3.3.1.3
SAS Drive cable receptacle	1 or 2	5.4.3.3.1.2	SAS Drive plug	2	5.4.3.3.1.1
			SATA device plug	1	SATA
SAS Drive backplane receptacle	2	5.4.3.3.1.3	SAS Drive plug	2	5.4.3.3.1.1
			SATA device plug	1	SATA
Micro SAS plug	2	5.4.3.3.1.5	Micro SAS receptacle	2	5.4.3.3.1.6
Micro SAS receptacle	2	5.4.3.3.1.6	Micro SAS plug	2	5.4.3.3.1.5
			Micro SATA device plug	1	SATA
SAS internal connectors - other					
SAS 4i cable receptacle	4	5.4.3.3.2.1	SAS 4i plug	4	5.4.3.3.2.2
SAS 4i plug	4	5.4.3.3.2.2	SAS 4i cable receptacle	4	5.4.3.3.2.1
Mini SAS 4i cable plug	4	5.4.3.3.3.1	Mini SAS 4i receptacle	4	5.4.3.3.3.2
Mini SAS 4i receptacle	4	5.4.3.3.3.2	Mini SAS 4i cable plug	4	5.4.3.3.3.1

Table 3 — Connectors (part 2 of 2)

Type of connector	Physical links	Reference	Attaches to		
			Type of connector	Physical links	Reference
Mini SAS HD 4i cable plug	4	5.4.3.3.4.1	Mini SAS HD 4i receptacle	4	5.4.3.3.4.3
			Mini SAS HD 8i receptacle	8	5.4.3.3.4.4
Mini SAS HD 8i cable plug	8	5.4.3.3.4.2	Mini SAS HD 8i cable receptacle	8	5.4.3.3.4.4
Mini SAS HD 4i receptacle	4	5.4.3.3.4.3	Mini SAS HD 4i cable plug	4	5.4.3.3.4.1
Mini SAS HD 8i receptacle	8	5.4.3.3.4.4	Mini SAS HD 4i cable plug	4	5.4.3.3.4.1
			Mini SAS HD 8i cable plug	8	5.4.3.3.4.2
SAS external connectors					
Mini SAS 4x cable plug	4	5.4.3.4.1.1	Mini SAS 4x receptacle Mini SAS 4x active receptacle	4	5.4.3.4.1.2
Mini SAS 4x receptacle	4	5.4.3.4.1.2	Mini SAS 4x cable plug	4	5.4.3.4.1.1
Mini SAS 4x active cable assembly plug	4	5.4.3.4.1.1	Mini SAS 4x active receptacle	4	5.4.3.4.1.2
Mini SAS 4x active receptacle	4	5.4.3.4.1.2	Mini SAS 4x cable plug Mini SAS 4x active cable assembly plug	4	5.4.3.4.1.1
Mini SAS HD 4x cable plug	4	5.4.3.4.2.1	Mini SAS HD 4x receptacle	4	5.4.3.4.2.3
			Mini SAS HD 8x receptacle	8	5.4.3.4.2.4
			Mini SAS HD 16x receptacle	16	5.4.3.4.2.5
Mini SAS HD 8x cable plug	8	5.4.3.4.2.2	Mini SAS HD 8x receptacle	8	5.4.3.4.2.4
			Mini SAS HD 16x receptacle	16	5.4.3.4.2.5
Mini SAS HD 4x receptacle	4	5.4.3.4.2.3	Mini SAS HD 4x cable plug	4	5.4.3.4.2.1
Mini SAS HD 8x receptacle	8	5.4.3.4.2.4	Mini SAS HD 4x cable plug	4	5.4.3.4.2.1
			Mini SAS HD 8x cable plug	8	5.4.3.4.2.2
Mini SAS HD 16x receptacle	16	5.4.3.4.2.5	Mini SAS HD 4x cable plug	4	5.4.3.4.2.1
			Mini SAS HD 8x cable plug	8	5.4.3.4.2.2
QSFP+ cable plug	4	5.4.3.4.3.1	QSFP+ receptacle	4	5.4.3.4.3.2
QSFP+ receptacle	4	5.4.3.4.3.2	QSFP+ cable plug	4	5.4.3.4.3.1

A SAS icon (see Annex G) should be placed on or near each SAS connector.

5.4.3.2 Connector categories

The relationship between connector categories and connectors is shown in table 4.

Table 4 — Connector categories

Connector category	Connectors in category
Unmanaged passive	All connectors listed in table 3 (see 5.4.3.1) that are not listed elsewhere in this table
Unmanaged active	Mini SAS 4x active connectors (see 5.4.3.4.1)
Managed	Mini SAS HD external connectors (see 5.4.3.4.2) QSFP+ connectors (see 5.4.3.4.3)

5.4.3.3 SAS internal connectors

5.4.3.3.1 SAS Drive connectors

5.4.3.3.1.1 SAS Drive plug connector

The SAS Drive plug connector is the Device Free (Plug) connector defined in SFF-8482.

See SFF-8223, SFF-8323, and SFF-8523 for the SAS Drive plug connector locations on common form factors.

Figure 20 shows the SAS Drive plug connector.

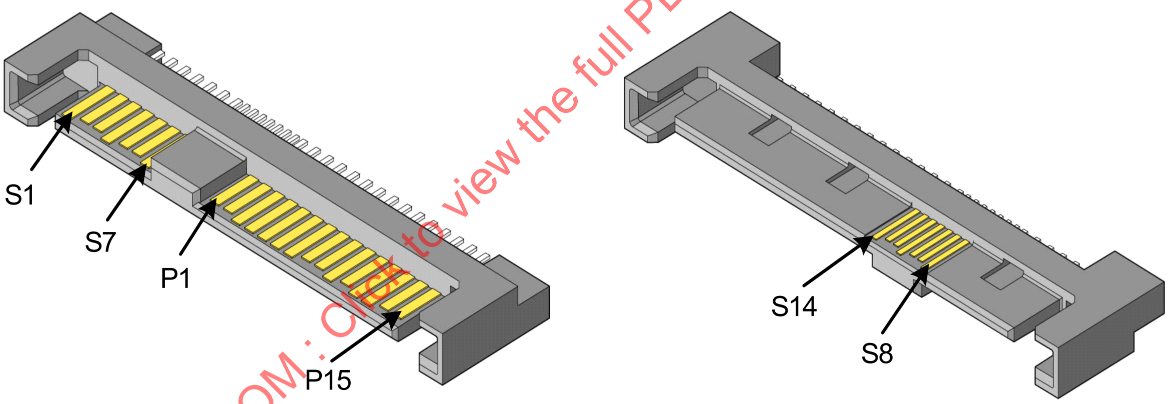


Figure 20 — SAS Drive plug connector

Table 5 (see 5.4.3.3.1.4) defines the pin assignments for the SAS Drive plug connector.

5.4.3.3.1.2 SAS Drive cable receptacle connector

The SAS Drive cable receptacle connector is the Internal Cable Fixed (Receptacle) connector defined in SFF-8482.

The single-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link; or
b) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 21 shows the single-port version of the SAS Drive cable receptacle connector.

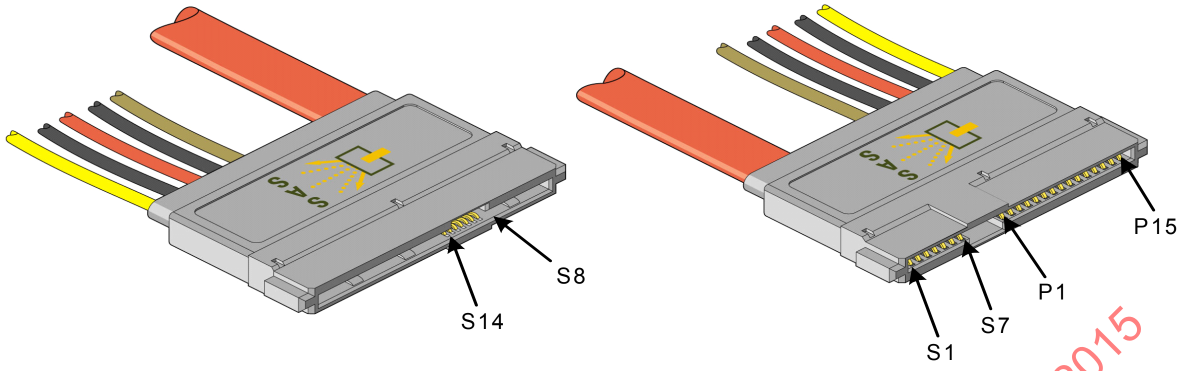


Figure 21 — Single-port SAS Drive cable receptacle connector

The dual-port version attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both the primary and secondary physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 22 shows the dual-port version of the SAS Drive cable receptacle connector.

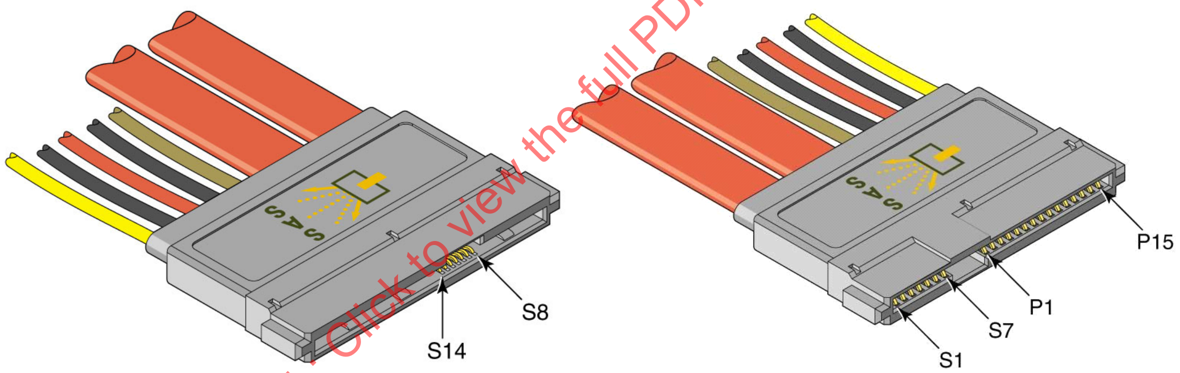


Figure 22 — Dual-port SAS Drive cable receptacle connector

Table 5 (see 5.4.3.3.1.4) defines the pin assignments for the SAS Drive cable receptacle connector. The secondary physical link (i.e., pins S8 through S14) is not supported by the single-port internal cable receptacle.

5.4.3.3.1.3 SAS Drive backplane receptacle connector

The SAS Drive backplane receptacle connector is the Backplane Fixed (Receptacle) connector defined in SFF-8482.

The SAS Drive backplane receptacle connector attaches to:

a) a SAS Drive plug connector, providing contact for the power pins and only the primary physical link;
b) a SAS Drive plug connector, providing contact for the power pins and both primary and secondary physical links; or
c) a SATA device plug connector, providing contact for the power pins and the primary physical link.

Figure 23 shows the SAS Drive backplane receptacle connector.

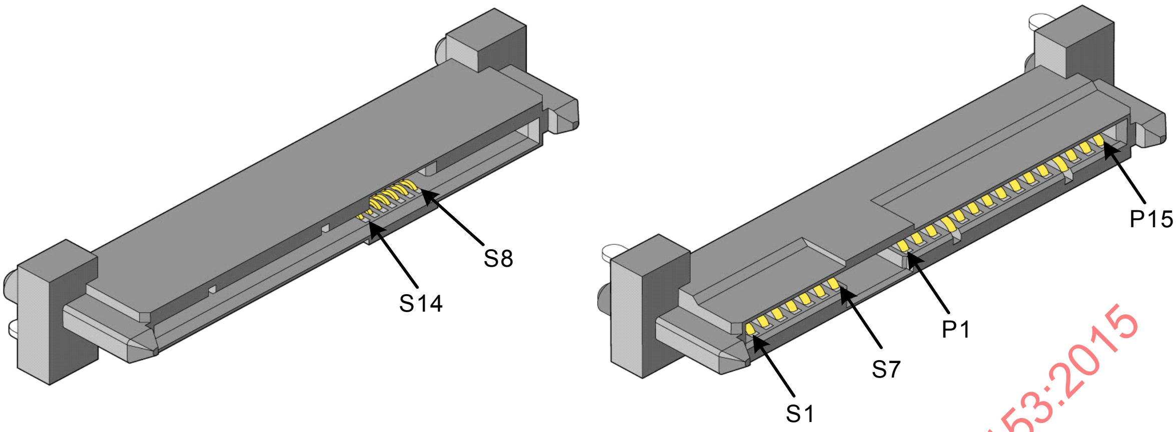


Figure 23 — SAS Drive backplane receptacle connector

Table 5 (see 5.4.3.3.1.4) defines the pin assignments for the SAS Drive backplane receptacle connector.

5.4.3.3.1.4 SAS Drive connector pin assignments

Table 5 defines the SAS target device pin assignments for the SAS Drive plug connector (see 5.4.3.3.1.1), the SAS Drive cable receptacle connector (see 5.4.3.3.1.2), and the SAS Drive backplane receptacle connector (see 5.4.3.3.1.3). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

SAS Drive plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a SATA device plug connector (see SATA).

Table 5 — SAS Drive connector pin assignments

Segment	Pin	Backplane receptacle	SAS Drive plug and SAS Drive cable receptacle
Primary signal segment	S1	SIGNAL GROUND	
	S2	TP+	RP+
	S3	TP-	RP-
	S4	SIGNAL GROUND	
	S5	RP-	TP-
	S6	RP+	TP+
	S7	SIGNAL GROUND	
Secondary signal segment [a]	S8	SIGNAL GROUND	
	S9	TS+	RS+
	S10	TS-	RS-
	S11	SIGNAL GROUND	
	S12	RS-	TS-
	S13	RS+	TS+
	S14	SIGNAL GROUND	
Power segment [b]	P1	V_{33} [c]	
	P2	V_{33} [c]	
	P3	V_{33}, precharge [c]	
	P4	GROUND	
	P5	GROUND	
	P6	GROUND	
	P7	V_5, precharge [c]	
	P8	V_5 [c]	
	P9	V_5 [c]	
	P10	GROUND	
	P11	READY LED [d]	
	P12	GROUND	
	P13	V_{12}, precharge [c]	
	P14	V_{12} [c]	
	P15	V_{12} [c]	

[a] S8 through S14 are not connected on single-port implementations.

[b] Backplane receptacle connectors and SAS Drive cable receptacle connectors provide V_{33}, V_5, and V_{12}. SAS Device plug connectors receive V_{33}, V_5, and V_{12}.

[c] Behind a SAS Drive plug connector, the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_5, precharge pin P7 is connected to the two V_5 pins P8 and P9).

[d] Electrical characteristics for READY LED are defined in 5.8 and signal behavior is defined in SPL. SATA devices use P11 for activity indication and staggered spin-up disable and have different electrical characteristics (see SATA).

5.4.3.3.1.5 Micro SAS plug connector

The Micro SAS plug connector is defined in SFF-8486. The Micro SAS plug mates with the Micro SAS Receptacle (see 5.4.3.3.1.6), but not the Micro SATA receptacle (see SATA).

See SFF-8147 for the Micro SAS plug connector locations on common form factors. Figure 24 shows the Micro SAS plug connector.

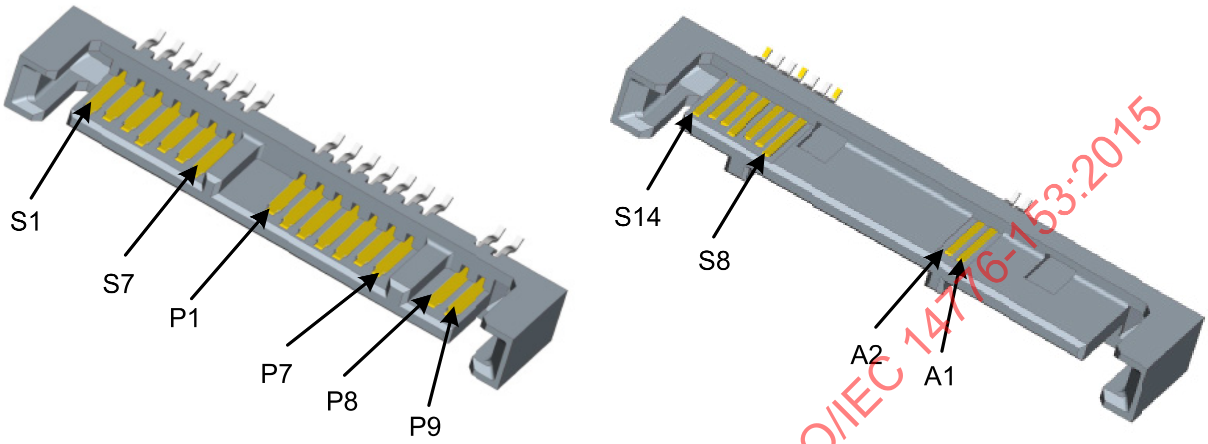


Figure 24 — Micro SAS plug connector

5.4.3.3.1.6 Micro SAS receptacle connector

The Micro SAS receptacle connector is defined in SFF-8486. The Micro SAS receptacle mates with the Micro SAS plug connector (see 5.4.3.3.1.5) or the Micro SATA device plug (see SATA).

Figure 25 shows the Micro SAS receptacle connector.

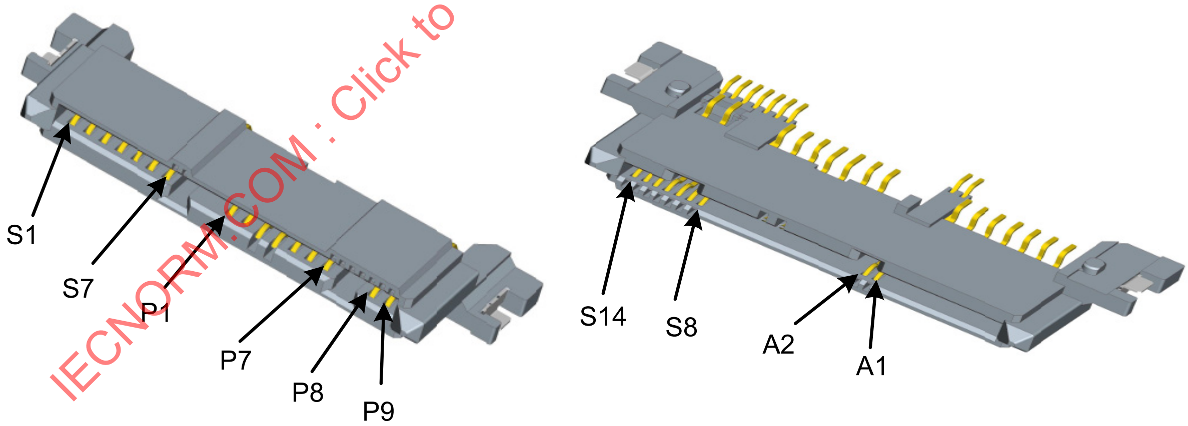


Figure 25 — Micro SAS receptacle connector

5.4.3.3.1.7 Micro SAS connector pin assignments

Table 6 defines the SAS target device pin assignments for the Micro SAS plug connector (see 5.4.3.3.1.5) and the Micro SAS receptacle connector (see 5.4.3.3.1.6). TP+, TP-, RP+, and RP- are used by the primary physical link. TS+, TS-, RS+, and RS- are used by the secondary physical link, if any.

Micro SAS plug connector pin assignments, except for the addition of the secondary physical link when present, are in the same locations as they are in a Micro SATA device plug connector (see SATA).

Table 6 — Micro SAS connector pin assignments

Segment	Pin	Micro SAS receptacle	Micro SAS plug	Mating level [e]
Primary signal segment	S1	SIGNAL GROUND		Second
	S2	TP+	RP+	Third
	S3	TP-	RP-	Third
	S4	SIGNAL GROUND		Second
	S5	RP-	TP-	Third
	S6	RP+	TP+	Third
	S7	SIGNAL GROUND		Second
Secondary signal segment [a]	S8	SIGNAL GROUND		Second
	S9	TS+	RS+	Third
	S10	TS-	RS-	Third
	S11	SIGNAL GROUND		Second
	S12	RS-	TS-	Third
	S13	RS+	TS+	Third
	S14	SIGNAL GROUND		Second
Power segment [b]	P1	V_{33} [c]		Third
	P2	V_{33}, precharge [c]		Second
	P3	GROUND		First
	P4	GROUND		First
	P5	V_5, precharge [c]		Second
	P6	V_5 [c]		Third
	P7	Reserved		Third
	P8	N/C [d]	Manufacturing diagnostic	Third
	P9	N/C [d]	Manufacturing diagnostic	Third
Auxiliary contacts	A1	Vender specific		Third
	A2	Vender specific		Third

[a] S8 through S14 are not connected on single-port implementations.
[b] The Micro SAS receptacle connector (see 5.4.3.3.1.6) provides V_{33} and V_5. The Micro SATA power receptacle connector (see SATA) provides V_{33} and optionally V_5. The Micro SAS plug connector (see 5.4.3.3.1.5) receives V_{33} and V_5.
[c] Behind a Micro SAS plug connector (see 5.4.3.3.1.5), the precharge pin and each corresponding voltage pin shall be connected together on the SAS target device (e.g., the V_{33}, precharge pin P2 is connected to the V_{33} pin P1).
[d] N/C = not connected
[e] The mating level assumes zero angular offset between connectors and indicates the physical dimension of the contact (see SFF-8486 and SATA).

5.4.3.3.2 SAS 4i connectors

5.4.3.3.2.1 SAS 4i cable receptacle connector

The SAS 4i cable receptacle connector is the 4 Lane Cable Receptacle (fixed) with Backshell connector defined in SFF-8484.

Figure 26 shows the SAS 4i cable receptacle connector.

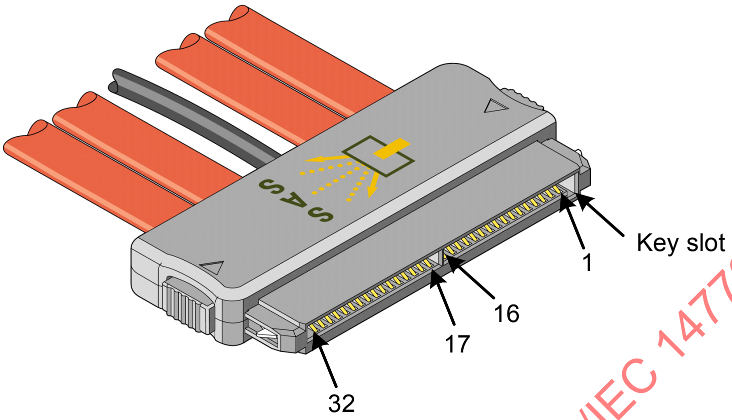


Figure 26 — SAS 4i cable receptacle connector

Table 7 and table 8 (see 5.4.3.3.2.3) define the pin assignments for the SAS 4i cable receptacle connector.

5.4.3.3.2.2 SAS 4i plug connector

The SAS 4i plug connector is the 4 Lane Vertical Plug (free) or 4 Lane R/A Plug (free) connector defined in SFF-8484.

Figure 27 shows the SAS 4i plug connector.

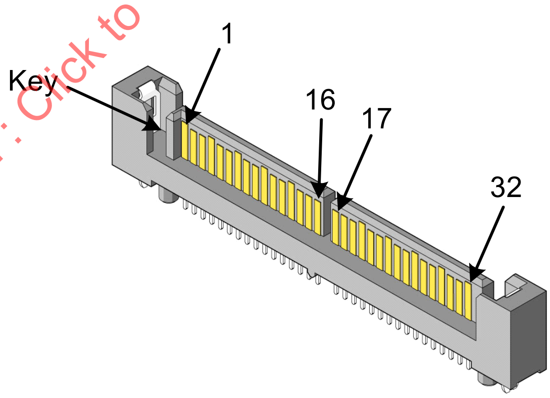


Figure 27 — SAS 4i plug connector

Table 7 and table 8 (see 5.4.3.3.2.3) define the pin assignments for the SAS 4i plug connector.

5.4.3.3.2.3 SAS 4i connector pin assignments

Table 7 defines the pin assignments for SAS 4i cable receptacle connectors (see 5.4.3.3.2.1) and SAS 4i plug connectors (see 5.4.3.3.2.2) for controller applications using one, two, three, or four of the physical links.

Table 7 — Controller SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]			
	One	Two	Three	Four
Rx 0+	2	2	2	2
Rx 0-	3	3	3	3
Tx 0-	5	5	5	5
Tx 0+	6	6	6	6
Rx 1+	N/C	8	8	8
Rx 1-	N/C	9	9	9
Tx 1-	N/C	11	11	11
Tx 1+	N/C	12	12	12
Sideband 0	14	14	14	14
Sideband 1	15	15	15	15
Sideband 2	16	16	16	16
Sideband 3	17	17	17	17
Sideband 4	18	18	18	18
Sideband 5	19	19	19	19
Rx 2+	N/C	N/C	21	21
Rx 2-	N/C	N/C	22	22
Tx 2-	N/C	N/C	24	24
Tx 2+	N/C	N/C	25	25
Rx 3+	N/C	N/C	N/C	27
Rx 3-	N/C	N/C	N/C	28
Tx 3-	N/C	N/C	N/C	30
Tx 3+	N/C	N/C	N/C	31
SIGNAL GROUND	1, 4, 7, 10, 13, 20, 23, 26, 29, 32			
[a] N/C = not connected				

The use of the sideband signals by a controller is vendor specific. One implementation of the sideband signals by a controller is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 8 defines the pin assignments for SAS 4i plug connectors (see 5.4.3.3.2.1) and SAS 4i cable receptacle connectors (see 5.4.3.3.2.1) for backplane applications using one, two, three, or four of the physical links.

Table 8 — Backplane SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]			
	One	Two	Three	Four
Rx 3+	N/C	N/C	N/C	2
Rx 3-	N/C	N/C	N/C	3
Tx 3-	N/C	N/C	N/C	5
Tx 3+	N/C	N/C	N/C	6
Rx 2+	N/C	N/C	8	8
Rx 2-	N/C	N/C	9	9
Tx 2-	N/C	N/C	11	11
Tx 2+	N/C	N/C	12	12
Sideband 5	14	14	14	14
Sideband 4	15	15	15	15
Sideband 3	16	16	16	16
Sideband 2	17	17	17	17
Sideband 1	18	18	18	18
Sideband 0	19	19	19	19
Rx 1+	N/C	21	21	21
Rx 1-	N/C	22	22	22
Tx 1-	N/C	24	24	24
Tx 1+	N/C	25	25	25
Rx 0+	27	27	27	27
Rx 0-	28	28	28	28
Tx 0-	30	30	30	30
Tx 0+	31	31	31	31
SIGNAL GROUND	1, 4, 7, 10, 13, 20, 23, 26, 29, 32			

[a] N/C = not connected

The use of the sideband signals by a backplane is vendor specific. One implementation of the sideband signals by a backplane is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.3.3 Mini SAS 4i connectors

5.4.3.3.3.1 Mini SAS 4i cable plug connector

The Mini SAS 4i cable plug connector is the free (plug) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 28 shows the Mini SAS 4i cable plug connector.

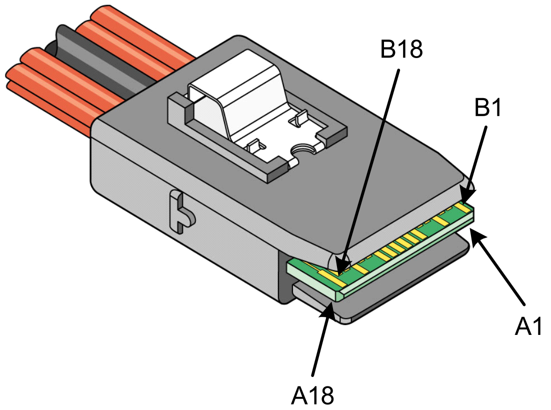


Figure 28 — Mini SAS 4i cable plug connector

Table 9 and table 10 (see 5.4.3.3.3.3) define the pin assignments for the Mini SAS 4i cable plug connector.

5.4.3.3.3.2 Mini SAS 4i receptacle connector

The Mini SAS 4i receptacle connector is the fixed (receptacle) 36-circuit unshielded compact multilane connector defined in SFF-8087 and SFF-8086.

Figure 29 shows the Mini SAS 4i receptacle connector.

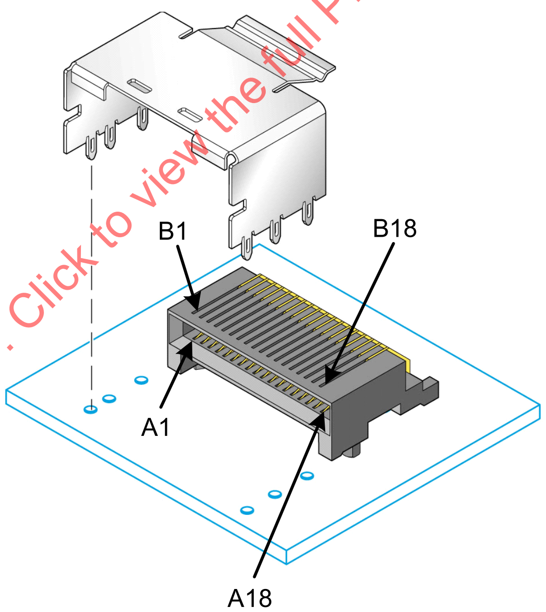


Figure 29 — Mini SAS 4i receptacle connector

Table 9 and table 10 (see 5.4.3.3.4.5) define the pin assignments for the Mini SAS 4i receptacle connector.

5.4.3.3.3.3 Mini SAS 4i connector pin assignments

Table 9 defines the pin assignments for Mini SAS 4i plug connectors (see 5.4.3.3.3.1) and Mini SAS 4i cable receptacle connectors (see 5.4.3.3.3.2) for controller applications using one, two, three, or four of the physical links.

Table 9 — Controller Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Sideband 7	A8	A8	A8	A8	First
Sideband 3	A9	A9	A9	A9	
Sideband 4	A10	A10	A10	A10	
Sideband 5	A11	A11	A11	A11	
Rx 2+	N/C	N/C	A13	A13	Third
Rx 2-	N/C	N/C	A14	A14	
Rx 3+	N/C	N/C	N/C	A16	
Rx 3-	N/C	N/C	N/C	A17	
Tx 0+	B2	B2	B2	B2	Third
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Sideband 0	B8	B8	B8	B8	First
Sideband 1	B9	B9	B9	B9	
Sideband 2	B10	B10	B10	B10	
Sideband 6	B11	B11	B11	B11	
Tx 2+	N/C	N/C	B13	B13	Third
Tx 2-	N/C	N/C	B14	B14	
Tx 3+	N/C	N/C	N/C	B16	
Tx 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 10 defines the pin assignments for Mini SAS 4i plug connectors (see 5.4.3.3.3.1) and Mini SAS 4i cable receptacle connectors (see 5.4.3.3.3.2) for backplane applications using one, two, three, or four of the physical links.

Table 10 — Backplane Mini SAS 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Sideband 0	A8	A8	A8	A8	First
Sideband 1	A9	A9	A9	A9	
Sideband 2	A10	A10	A10	A10	
Sideband 6	A11	A11	A11	A11	
Rx 2+	N/C	N/C	A13	A13	Third
Rx 2-	N/C	N/C	A14	A14	
Rx 3+	N/C	N/C	N/C	A16	
Rx 3-	N/C	N/C	N/C	A17	
Tx 0+	B2	B2	B2	B2	Third
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Sideband 7	B8	B8	B8	B8	First
Sideband 3	B9	B9	B9	B9	
Sideband 4	B10	B10	B10	B10	
Sideband 5	B11	B11	B11	B11	
Tx 2+	N/C	N/C	B13	B13	Third
Tx 2-	N/C	N/C	B14	B14	
Tx 3+	N/C	N/C	N/C	B16	
Tx 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

[a] N/C = not connected

[b] The mating level indicates the physical dimension of the contact (see SFF-8086).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.3.4 Mini SAS HD internal connectors

5.4.3.3.4.1 Mini SAS HD 4i cable plug connector

The Mini SAS HD 4i cable plug connector is the 4 lane cable (free) connector defined in SFF-8643. Figure 30 shows the Mini SAS HD 4i cable plug connector.

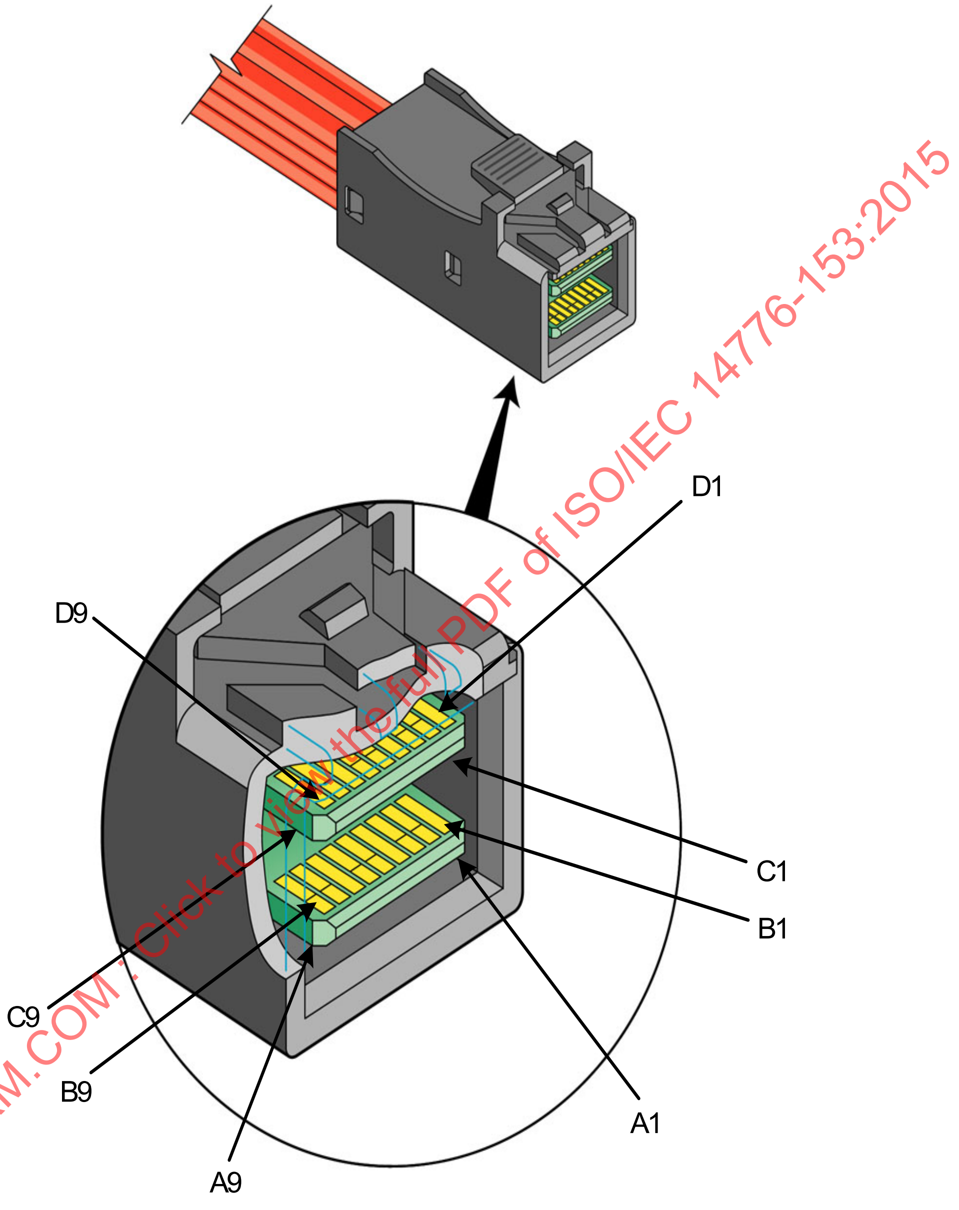


Figure 30 — Mini SAS HD 4i cable plug connector

Table 9 and table 10 (see 5.4.3.3.4.5) define the pin assignments for the Mini SAS HD 4i cable plug connector.

5.4.3.3.4.2 Mini SAS HD 8i cable plug connector

The Mini SAS HD 8i cable plug connector is the dual 4 lane cable plug (free) connector defined in SFF-8643.

Figure 31 shows the Mini SAS HD 8i cable plug connector. This connector is a modular version of repeating Mini SAS HD 4i cable plug connectors (see 5.4.3.3.4.1). Module labeling is shown in figure 31. See figure 30 (see 5.4.3.3.4.1) for pin designations.

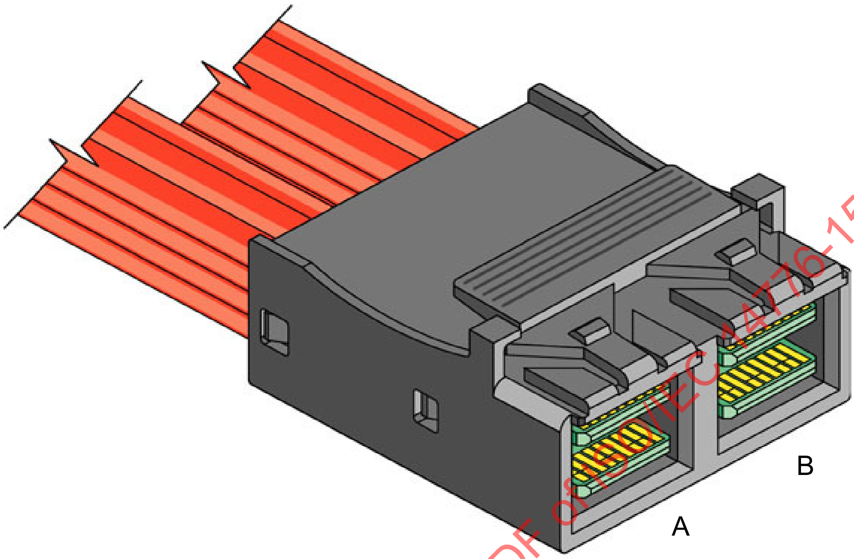


Figure 31 — Mini SAS HD 8i cable plug connector

Table 9 and table 10 (see 5.4.3.3.4.5) define the pin assignments for the Mini SAS HD 4i cable plug connector (see 5.4.3.3.4.1). The pin assignments are repeated for each module of the Mini SAS 8i cable plug connector.

5.4.3.3.4.3 Mini SAS HD 4i receptacle connector

The Mini SAS HD 4i receptacle connector is the 4 lane receptacle (fixed) connector defined in SFF-8643. Figure 32 shows the Mini SAS HD 4i receptacle connector.

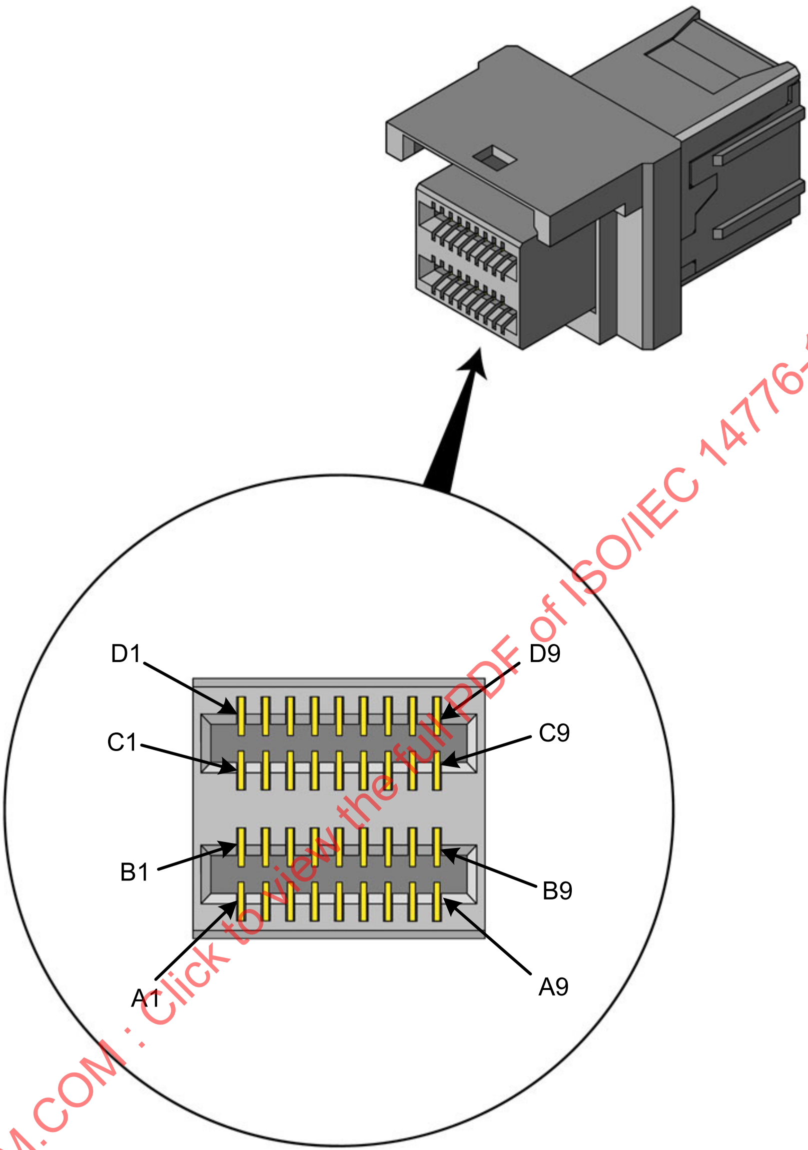


Figure 32 — Mini SAS HD 4i receptacle connector

Table 9 and table 10 (see 5.4.3.3.4.5) define the pin assignments for the Mini SAS HD 4i receptacle connector.

5.4.3.3.4.4 Mini SAS HD 8i receptacle connector

The Mini SAS HD 8i receptacle connector is a dual 4 lane receptacle (fixed) connector defined in SFF-8643. Figure 33 shows the Mini SAS HD 8i receptacle connector. This connector is a modular version of the Mini SAS HD 4i receptacle connector (see 5.4.3.3.4.3). Module labeling is shown in figure 33. See figure 32 (see 5.4.3.3.4.3) for pin designations.

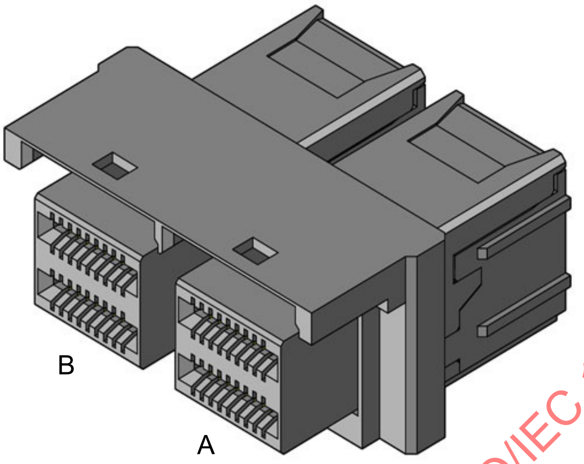


Figure 33 — Mini SAS HD 8i receptacle connector

Table 11 and table 12 (see 5.4.3.3.4.5) define the pin assignments for the Mini SAS HD 8i receptacle connector. The connector is a modular design of repeating Mini SAS HD 4i receptacles (see 5.4.3.3.4.3). This connector accepts one Mini SAS HD 8i plug connector (see 5.4.3.3.4.2) or two Mini SAS HD 4i plug connectors (see 5.4.3.3.4.1).

5.4.3.3.4.5 Mini SAS HD 4i connector pin assignments

Table 11 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.4.3.3.4.1) and Mini SAS HD 4i receptacle connectors (see 5.4.3.3.4.3) for controller applications using one, two, three, or four of the physical links.

Table 11 — Controller Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	B4	B4	B4	B4	Third
Rx 0-	B5	B5	B5	B5	
Rx 1+	N/C	A4	A4	A4	
Rx 1-	N/C	A5	A5	A5	
Sideband 7	A1	A1	A1	A1	Second
Sideband 3	B1	B1	B1	B1	
Sideband 4	C1	C1	C1	C1	
Sideband 5	D1	D1	D1	D1	

Table 11 — Controller Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 2+	N/C	N/C	B7	B7	Third
Rx 2-	N/C	N/C	B8	B8	
Rx 3+	N/C	N/C	N/C	A7	
Rx 3-	N/C	N/C	N/C	A8	
Tx 0+	D4	D4	D4	D4	Third
Tx 0-	D5	D5	D5	D5	
Tx 1+	N/C	C4	C4	C4	
Tx 1-	N/C	C5	C5	C5	
Sideband 0	A2	A2	A2	A2	Second
Sideband 1	B2	B2	B2	B2	
Sideband 2	C2	C2	C2	C2	
Sideband 6	D2	D2	D2	D2	
Tx 2+	N/C	N/C	D7	D7	Third
Tx 2-	N/C	N/C	D8	D8	
Tx 3+	N/C	N/C	N/C	C7	
Tx 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by controller applications is vendor specific. One implementation of the sideband signals by a controller application is an SGPIO initiator interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

Table 12 defines the pin assignments for Mini SAS HD 4i cable plug connectors (see 5.4.3.3.4.1) and Mini SAS HD 4i receptacle connectors (see 5.4.3.3.4.3) for backplane applications using one, two, three, or four of the physical links.

Table 12 — Backplane Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	B4	B4	B4	B4	Third
Rx 0-	B5	B5	B5	B5	
Rx 1+	N/C	A4	A4	A4	
Rx 1-	N/C	A5	A5	A5	

Table 12 — Backplane Mini SAS HD 4i connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Sideband 0	A1	A1	A1	A1	Second
Sideband 1	B1	B1	B1	B1	
Sideband 2	C1	C1	C1	C1	
Sideband 6	D1	D1	D1	D1	
Rx 2+	N/C	N/C	B7	B7	Third
Rx 2-	N/C	N/C	B8	B8	
Rx 3+	N/C	N/C	N/C	A7	
Rx 3-	N/C	N/C	N/C	A8	
Tx 0+	D4	D4	D4	D4	Third
Tx 0-	D5	D5	D5	D5	
Tx 1+	N/C	C4	C4	C4	
Tx 1-	N/C	C5	C5	C5	
Sideband 7	A2	A2	A2	A2	Second
Sideband 3	B2	B2	B2	B2	
Sideband 4	C2	C2	C2	C2	
Sideband 5	D2	D2	D2	D2	
Tx 2+	N/C	N/C	D7	D7	Third
Tx 2-	N/C	N/C	D8	D8	
Tx 3+	N/C	N/C	N/C	C7	
Tx 3-	N/C	N/C	N/C	C8	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8643).

The use of the sideband signals by backplane applications is vendor specific. One implementation of the sideband signals by a backplane application is an SGPIO target interface (see SFF-8485). Other implementations shall be compatible with the signal levels defined in SFF-8485.

5.4.3.4 SAS external connectors

5.4.3.4.1 Mini SAS 4x connectors

5.4.3.4.1.1 Mini SAS 4x cable plug connector

The Mini SAS 4x cable plug connector and the MiniSAS 4x active plug connector are the free (plug) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086.

Figure 34 shows the Mini SAS 4x cable plug connector.

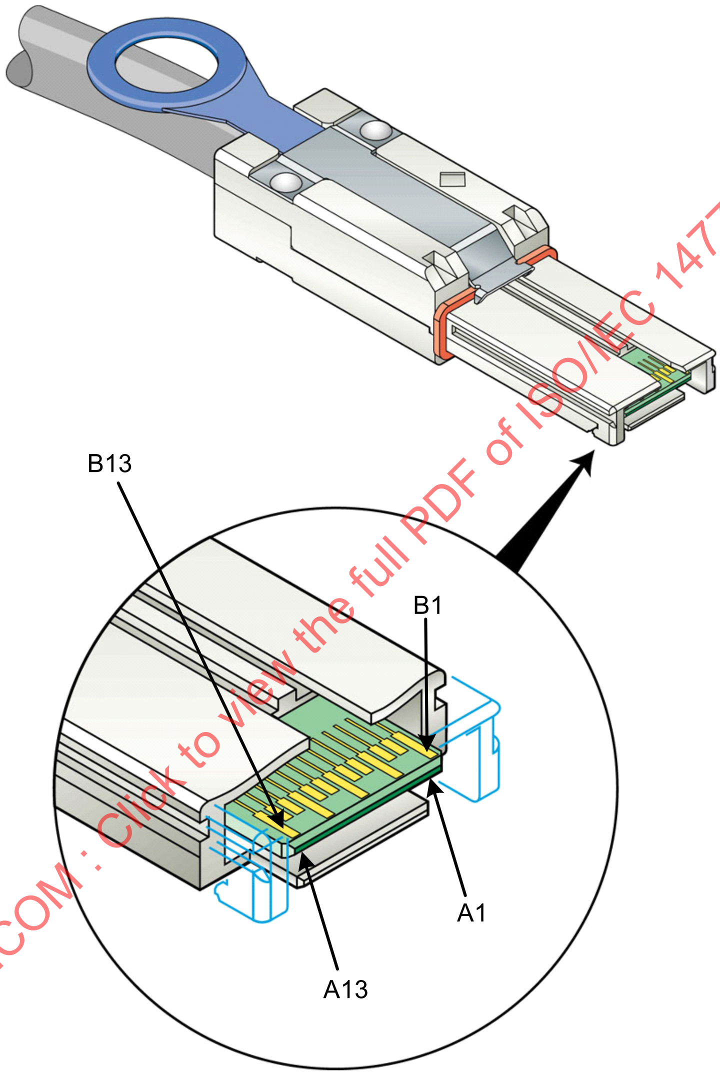


Figure 34 — Mini SAS 4x cable plug connector

If constructed with a pull tab as shown in figure 34, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 15 (see 5.4.3.4.1.3) and table 16 (see 5.4.3.4.1.3) define the pin assignments for the Mini SAS 4x cable plug connector.

Mini SAS 4x cable plug connectors shall include key slots to allow attachment to Mini SAS 4x receptacle connectors (see 5.4.3.4.1.2) with matching keys and key slots.

To ensure active cable assemblies are not intermateable with Mini SAS 4x receptacles that do not support active cable assemblies, differentiating keying shall be provided by having a blocking key on the plug connector in addition to the key slots. Table 13 defines the icons that shall be placed on or near

Mini SAS 4x cable plug connectors and the key slot and key positions (see SFF-8088) that shall be used by Mini SAS 4x cable plug connectors.

Table 13 — Mini SAS 4x cable plug connector and Mini SAS 4x active cable plug connector icons, key slot positions, and key positions

End of a SAS external cable		Icon	Key slot positions	Key positions	Reference
Electrical compliance	Attaches to				
Untrained 1.5 Gbit/s and 3 Gbit/s [a]	Out or in [b]	Diamond and circle	2, 4, 6	none	Figure 35
	Out [c]	Diamond	2, 4	none	Figure 36
	In [d]	Circle	4, 6	none	Figure 37
Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [e]	Out or in [b]	Two diamonds and two circles	2, 4, 6	3	Figure 38
	Out [c]	Two diamonds	2, 4	3	Figure 39
	In [d]	Two circles	4, 6	3	Figure 40
	Out or in [b]	Two triangles, diamond, and circle	2, 4, 6	5	Figure 41 [f]
	Out [c]	Two triangles and diamond	2, 4	5	Figure 42 [f]
	In [d]	Two triangles and circle	4, 6	5	Figure 43 [f]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[b] Attaches to an end device, an enclosure out port, an enclosure in port, or an enclosure universal port.
[c] Attaches to an end device, an enclosure out port, or an enclosure universal port.
[d] Attaches to an end device, an enclosure in port, or an enclosure universal port.
[e] Complies with the TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[f] Mini SAS 4x active cable plug connector.

Figure 35 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 45, figure 48, and figure 51 in 5.4.3.4.1.2), an enclosure out port (see figure 46, figure 49, and figure 52 in 5.4.3.4.1.2), or an enclosure in port (see figure 47, figure 50, and figure 53 in 5.4.3.4.1.2).

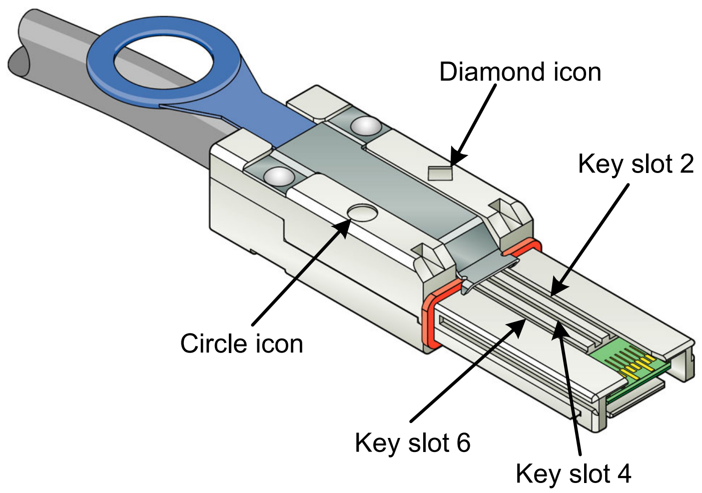


Figure 35 — Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 36 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 45, figure 48, and figure 51 in 5.4.3.4.1.2) or an enclosure out port (see figure 46, figure 49, and figure 52 in 5.4.3.4.1.2).

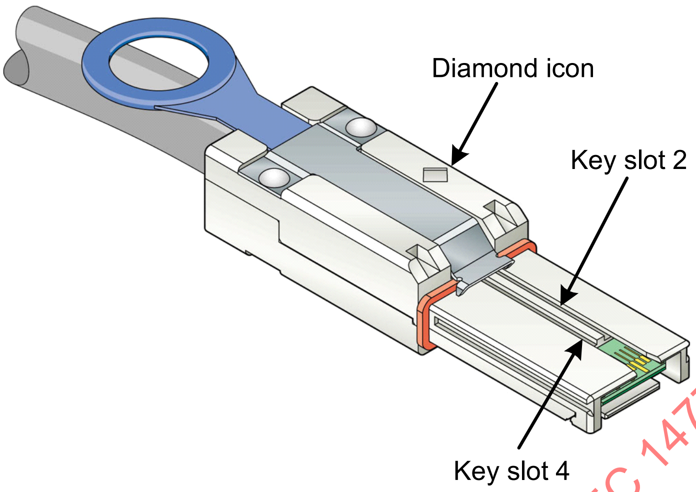


Figure 36 — Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port

Figure 37 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 45, figure 48, and figure 51 in 5.4.3.4.1.2) or an enclosure in port (see figure 47, figure 50, and figure 53 in 5.4.3.4.1.2).

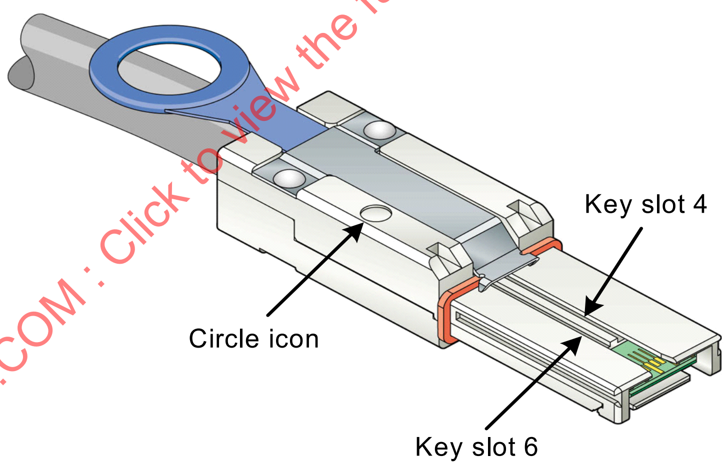


Figure 37 — Mini SAS 4x cable plug connector for untrained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure in port

Figure 38 shows the key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 48 and figure 51 in 5.4.3.4.1.2), an enclosure out port (see figure 49 and figure 52 in 5.4.3.4.1.2), or an enclosure in port (figure 50 and figure 53 in 5.4.3.4.1.2).

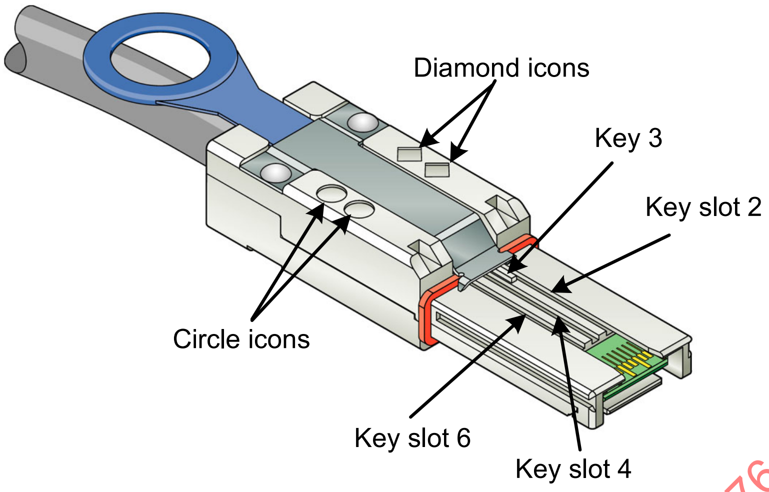


Figure 38 — Mini SAS 4x cable plug connector for trained 1.5 Gbit/s and 3 Gbit/s that attaches to an enclosure out port or an enclosure in port

Figure 39 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port (see figure 48 and figure 51 in 5.4.3.4.1.2) or an enclosure out port (see figure 49 and figure 52 in 5.4.3.4.1.2).

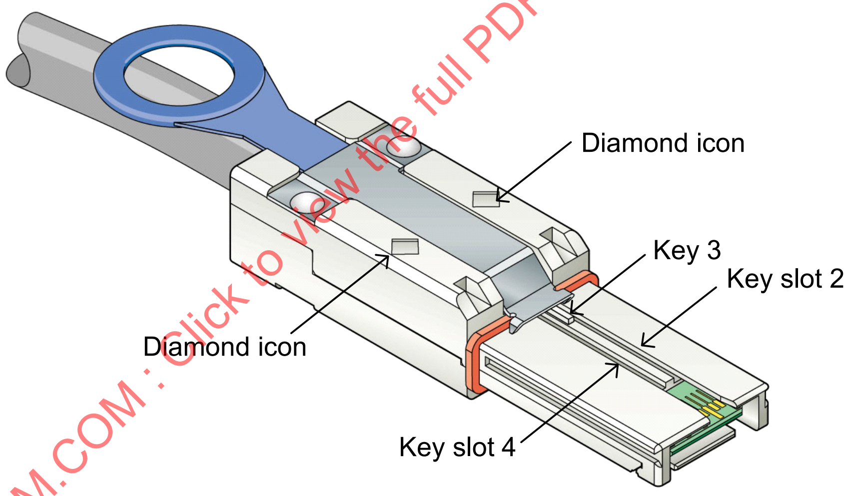


Figure 39 — Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure out port

Figure 40 shows the key and key slots on the Mini SAS 4x cable plug connector for a cable assembly supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an end device or an enclosure universal port ((see figure 48 and figure 51 in 5.4.3.4.1.2) or an enclosure in port (see figure 50 and figure 53 in 5.4.3.4.1.2).

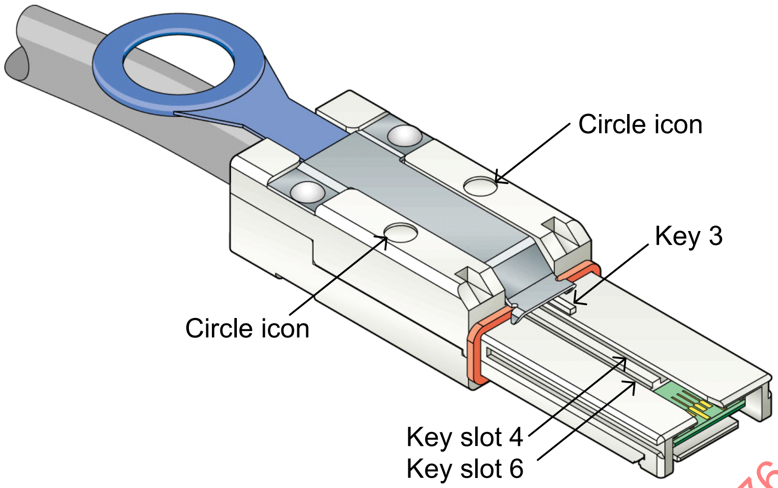


Figure 40 — Mini SAS 4x cable plug connector for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s that attaches to an enclosure in port

Figure 41 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 51 in 5.4.3.4.1.2), an enclosure out port (see figure 52 in 5.4.3.4.1.2), or an enclosure in port (see figure 53 in 5.4.3.4.1.2).

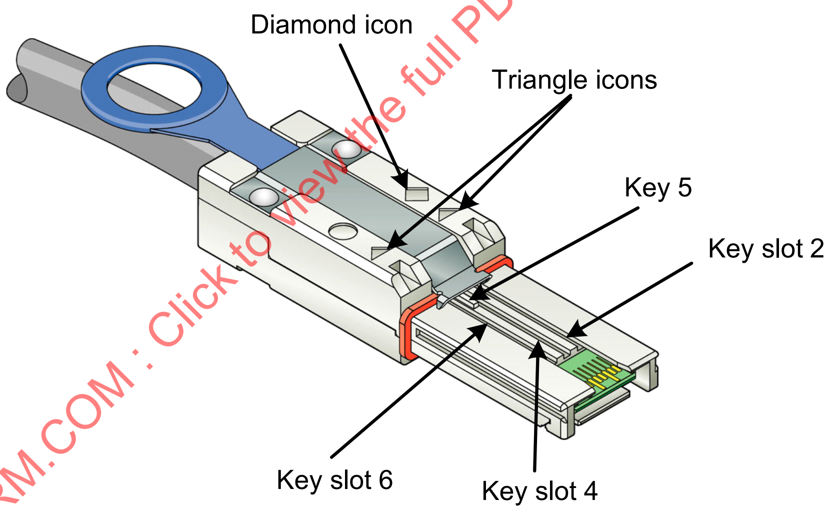


Figure 41 — Mini SAS 4x active cable plug connector that attaches to an enclosure out port or an enclosure in port

Figure 42 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 51 in 5.4.3.4.1.2) or enclosure out port (see figure 52 in 5.4.3.4.1.2).

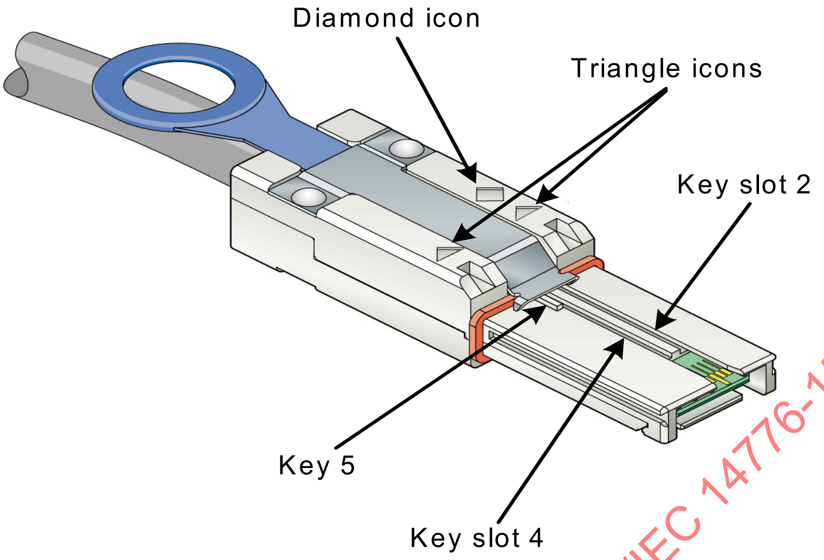


Figure 42 — Mini SAS 4x active cable plug connector that attaches to an enclosure out port

Figure 43 shows the key slots on the Mini SAS 4x active cable plug connector for an active cable assembly supporting trained 1.5 Gbit/s and 3 Gbit/s that attaches to an end device or an enclosure universal port (see figure 51 in 5.4.3.4.1.2) or an enclosure in port (see figure 53 in 5.4.3.4.1.2).

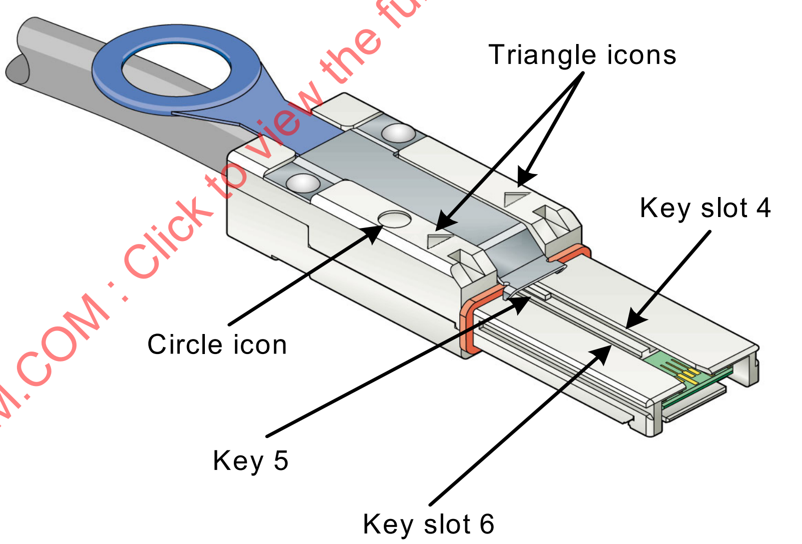


Figure 43 — Mini SAS 4x active cable plug connector that attaches to an enclosure in port

5.4.3.4.1.2 Mini SAS 4x receptacle connector

The Mini SAS 4x receptacle connector is the fixed (receptacle) 26-circuit shielded compact multilane connector defined in SFF-8088 and SFF-8086.

A Mini SAS 4x receptacle connector may be used by one or more SAS devices (e.g., one SAS device using physical links 0 and 3, another using physical link 1, and a third using physical link 2).

A Mini SAS 4x receptacle connector shall be used by no more than one expander device at a time, and all physical links shall be used by the same expander port (i.e., all the expander phys shall have the same routing attribute (e.g., subtractive or table) (see SPL)).

Figure 44 shows the Mini SAS 4x receptacle connector.

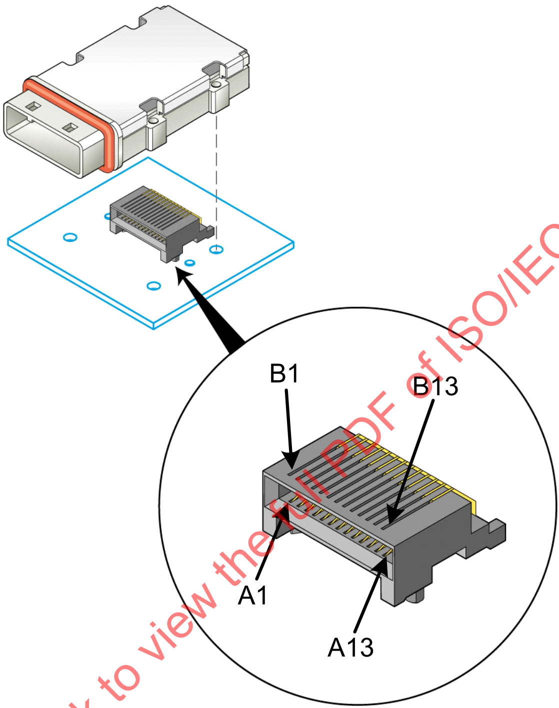


Figure 44 — Mini SAS 4x receptacle connector

Table 15 (see 5.4.3.4.1.3) and table 16 (see 5.4.3.4.1.3) define the pin assignments for the Mini SAS 4x receptacle connector.

Mini SAS 4x receptacle connectors and Mini SAS 4x active receptacle connectors shall include keys and key slots to prevent attachment to Mini SAS 4x cable plug connectors (see 5.4.3.4.1.1) without matching keys and key slots.

Table 14 defines the icons that shall be placed on or near Mini SAS 4x receptacle connectors and the key and key slot positions (see SFF-8088) that shall be used by Mini SAS 4x receptacle connectors.

Table 14 — Mini SAS 4x receptacle connector icons, key positions, and key slot positions

Electrical compliance	Use	Icons	Key position	Key slot position	Reference
Untrained 1.5 Gbit/s and 3 Gbit/s [a]	End device or enclosure universal port	Diamond and circle	4	none	Figure 45
	Enclosure out port	Diamond	2	none	Figure 46
	Enclosure in port	Circle	6	none	Figure 47
Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [b]	End device or enclosure universal port	Two diamonds and two circles	4	3	Figure 48
	Enclosure out port	Two diamonds	2	3	Figure 49
	Enclosure in port	Two circles	6	3	Figure 50
	End device or enclosure universal port	Two triangles, diamond, and circle	4	3, 5	Figure 51 [c]
	Enclosure out port	Two triangles and diamond	2	3, 5	Figure 52 [c]
	Enclosure in port	Two triangles and circle	6	3, 5	Figure 53 [c]

[a] Complies with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[b] Complies with the TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5) and does not comply with the TxRx connection characteristics for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4).
[c] Mini SAS 4x active receptacle.

Figure 45 shows the key on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 35, figure 36, and figure 37 (see 5.4.3.4.1.1) may be attached to this connector.

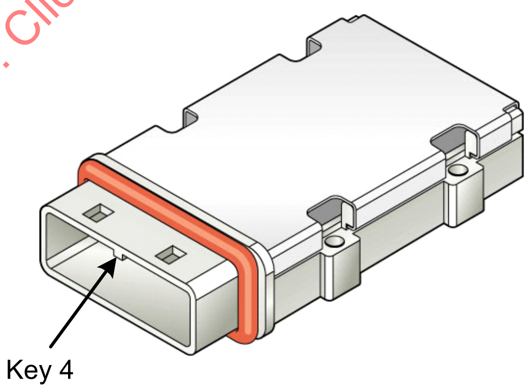


Figure 45 — Mini SAS 4x receptacle connector - end device or enclosure universal port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 46 shows the key on a Mini SAS 4x receptacle connector used by an enclosure out port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 35 and figure 36 (see 5.4.3.4.1.1) may be attached to this connector.

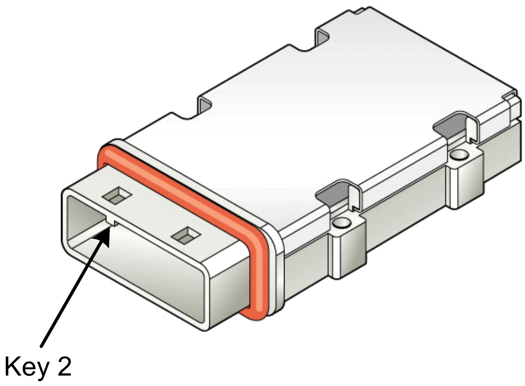


Figure 46 — Mini SAS 4x receptacle connector - enclosure out port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 47 shows the key on a Mini SAS 4x receptacle connector used by an enclosure in port that supports untrained 1.5 Gbit/s and 3 Gbit/s. The Mini SAS 4x cable plug connectors shown in figure 35 and figure 37 (see 5.4.3.4.1.1) may be attached to this connector.

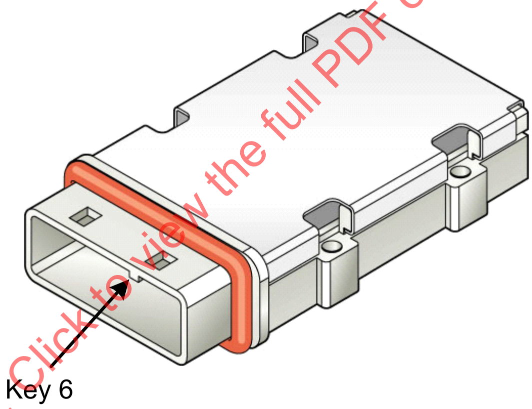


Figure 47 — Mini SAS 4x receptacle connector - enclosure in port for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 48 shows the key and key slot on a Mini SAS 4x receptacle connector used by an end device or enclosure universal port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 35, figure 36, figure 37, figure 38, figure 39, and figure 40 (see 5.4.3.4.1.1) may be attached to this connector.

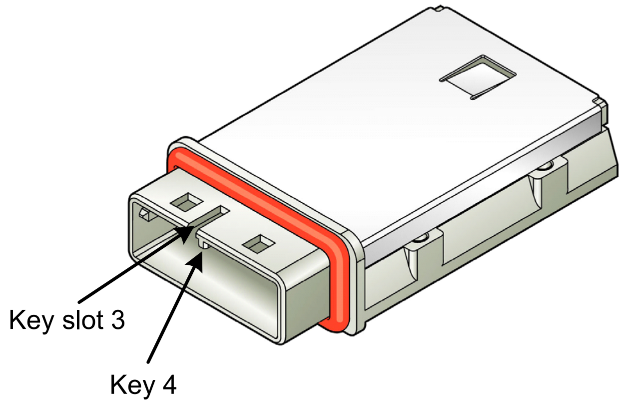


Figure 48 — Mini SAS 4x receptacle connector - end device or enclosure universal port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 49 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 35, figure 36, figure 38, and figure 39, (see 5.4.3.4.1.1) may be attached to this connector.

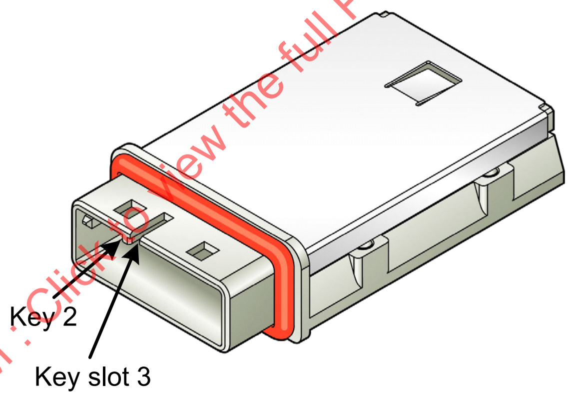


Figure 49 — Mini SAS 4x receptacle connector - enclosure out port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 50 shows the key and key slot on a Mini SAS 4x receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 35, figure 37, figure 38, and figure 40 (see 5.4.3.4.1.1) may be attached to this connector.

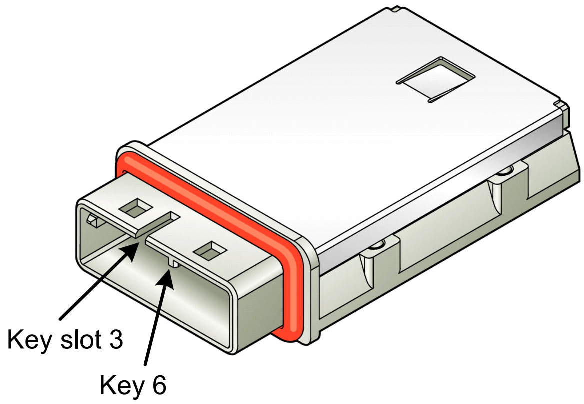


Figure 50 — Mini SAS 4x receptacle connector - enclosure in port for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s and for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 51 shows an Mini SAS 4x active receptacle connector used by end devices or an enclosure universal port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 35, figure 36, figure 37, figure 38, figure 39, figure 40, figure 41, figure 42, and figure 43 (see 5.4.3.4.1.1) may be attached to this connector.

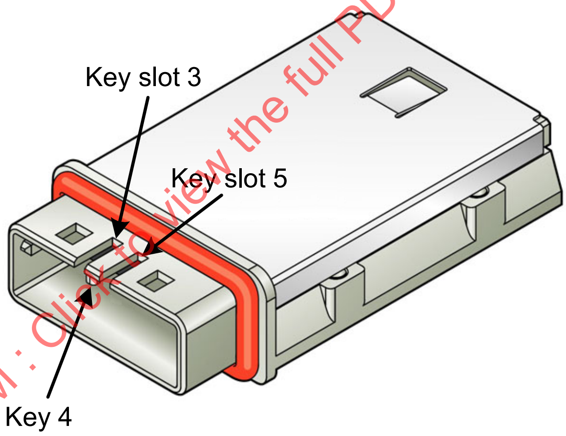


Figure 51 — Mini SAS 4x active receptacle connector - end device or enclosure universal port

Figure 52 shows an Mini SAS 4x active receptacle connector used by an enclosure out port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 35, figure 36, figure 38, figure 39, figure 41, and figure 42 (see 5.4.3.4.1.1) may be attached to this connector.

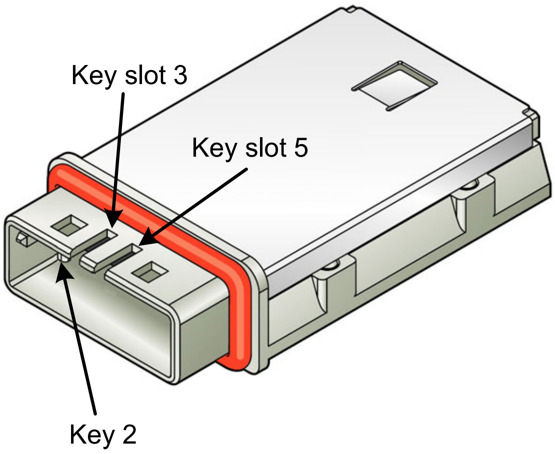


Figure 52 — Mini SAS 4x active receptacle connector - enclosure out port

Figure 53 shows an Mini SAS 4x active receptacle connector used by an enclosure in port that supports:

a) trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s; and
b) untrained 1.5 Gbit/s and 3 Gbit/s.

The Mini SAS 4x cable plug connectors shown in figure 35, figure 37, figure 38, figure 40, figure 41, and figure 43 (see 5.4.3.4.1.1) may be attached to this connector.

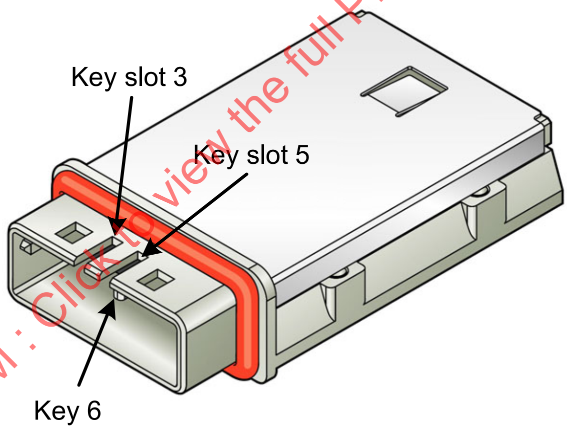


Figure 53 — Mini SAS 4x active receptacle connector - enclosure in port

5.4.3.4.1.3 Mini SAS 4x connector pin assignments

Table 15 defines the pin assignments for Mini SAS 4x cable plug connectors (see 5.4.3.4.1.1) and Mini SAS 4x receptacle connectors (see 5.4.3.4.1.2) for applications using one, two, three, or four of the physical links.

Table 15 — Mini SAS 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Rx 2+	N/C	N/C	A8	A8	
Rx 2-	N/C	N/C	A9	A9	
Rx 3+	N/C	N/C	N/C	A11	
Rx 3-	N/C	N/C	N/C	A12	
Tx 0+	B2	B2	B2	B2	
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Tx 2+	N/C	N/C	B8	B8	
Tx 2-	N/C	N/C	B9	B9	
Tx 3+	N/C	N/C	N/C	B11	
Tx 3-	N/C	N/C	N/C	B12	
SIGNAL GROUND	A1, A4, A7, A10, A13 B1, B4, B7, B10, B13				First
CHASSIS GROUND	Housing				N/A

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.4.3.4.1.4 Mini SAS 4x active connector pin assignments

Table 16 defines the pin assignments for Mini SAS 4x active cable plug connectors (see 5.4.3.4.1.1) and Mini SAS 4x active receptacle connectors (see 5.4.3.4.1.2) for implementations using one, two, three, or four of the physical links.

Table 16 — Mini SAS 4x active connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	
Rx 2+	N/C	N/C	A8	A8	
Rx 2-	N/C	N/C	A9	A9	
Rx 3+	N/C	N/C	N/C	A11	
Rx 3-	N/C	N/C	N/C	A12	
Tx 0+	B2	B2	B2	B2	
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	
Tx 2+	N/C	N/C	B8	B8	
Tx 2-	N/C	N/C	B9	B9	
Tx 3+	N/C	N/C	N/C	B11	
Tx 3-	N/C	N/C	N/C	B12	
SENSE [c]	B1				
V_{CC} [d]	B13				
SIGNAL GROUND	A1, A4, A7, A10, A13, B4, B7, B10				First
CHASSIS GROUND	Housing				

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8086).
[c] Electrical characteristics are defined in 5.4.3.4.1.5.
[d] Electrical characteristics are defined in 5.4.3.4.1.5.

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the connector when used in a cable assembly.

5.4.3.4.1.5 Mini SAS 4x active cable power requirements

Mini SAS 4x active cable assemblies may contain integrated circuitry (e.g., drivers, repeaters, or equalizers). To enable the operation of circuitry inside the Mini SAS 4x active cable assemblies, Mini SAS 4x active receptacle connectors provide power when connected to a Mini SAS 4x active cable assembly (see 5.4.4.2.2). Mini SAS 4x active receptacle connectors shall be intermateable with Mini SAS 4x passive cable assemblies. To be intermateable, Mini SAS 4x active receptacle connectors define a pin (i.e., SENSE (see table 16) (see 5.4.3.4.1.4)) to allow control of power. Power shall only be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x active cable assembly is present. Power shall not be applied to the Mini SAS 4x active cable receptacle when a Mini SAS 4x passive cable assembly or no cable assembly is present. An example of a power supply logic circuitry design is shown in Annex F.

The voltage and current requirements for the power supplied to the Mini SAS 4x active cable receptacle enable support for Mini SAS 4x active cable assemblies with power consumption of up to 1 W per each end of the cable assembly. These requirements are defined in table 17.

Table 17 — Mini SAS 4x active cable supplied power requirements

Characteristic	Units	Minimum	Nominal	Maximum
Supply voltage	V	3.135 [a]	3.3	3.465 [b]
Supply current	mA			319.4 [c]
Current consumption	mA			288.6 [d]
Power consumption	mW			1 000 [d e]

a At the maximum supply current.
b The power supply shall not exceed this value at any current.
c The power supply shall deliver this amount of current at the minimum voltage of 3.135 V.
d Maximum consumption for each end of the active cable assembly at the maximum voltage of 3.465 V.
e This is a derived quantity obtained from: (maximum supply voltage) x (maximum current consumption).

The Mini SAS 4x active cable assembly shall provide a connection of the SENSE pin to ground through a 5 kΩ (±5 %) resistor.

The active cable power circuitry shall enable power to the Mini SAS 4x receptacle connector only when the presence of the sense resistor is detected and power shall be disabled if the SENSE pin is open (i.e., no Mini SAS 4x cable assembly plugged in) or shorted to ground (i.e., Mini SAS 4x passive cable plugged in).

The active cable power circuitry shall have protection against the connection of the V_{CC} pin to ground or excessive current loading.

To support hot plugging, the active cable power circuitry shall be able to detect the sense resistor and provide full current within 50 ms of active cable assembly connection.

The active cable assembly and Mini SAS active cable receptacle power pins (i.e., the V_{CC} pin and SENSE pin) shall be coupled to ground via bypass capacitors so that they possess low impedance to ground from 100 MHz to 1.5 times the fundamental frequency of the maximum baud rate supported by the attached transmitter device and the attached receiver device.

The power planes of the printed circuit board on the receptacle side shall be coupled to ground.

In implementations where the circuitry in the Mini SAS 4x active cable assembly requires voltages other than the provided 3.3 V, voltage regulators may be located within the Mini SAS 4x active cable assembly.

5.4.3.4.2 Mini SAS HD external connectors

5.4.3.4.2.1 Mini SAS HD 4x cable plug connector

The Mini SAS HD 4x cable plug connector is the free (plug) 36-circuit connector defined in SFF-8644.

Figure 54 shows the Mini SAS HD 4x cable plug connector.

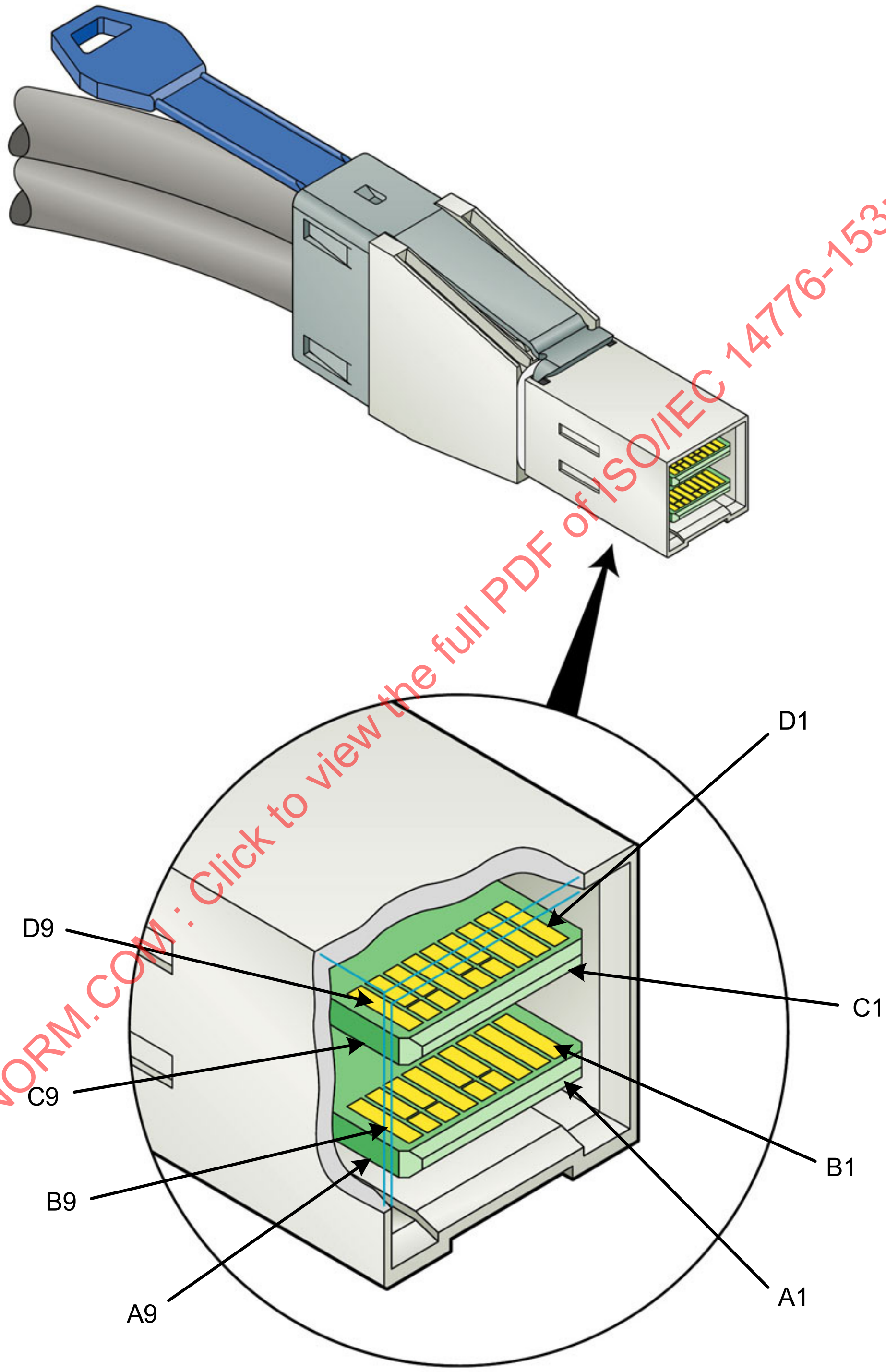


Figure 54 — Mini SAS HD 4x cable plug connector

If constructed with a pull tab as shown in figure 54, then the pull tab should use PANTONE 279 C (i.e., light blue).

Table 18 (see 5.4.3.4.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector.

The Mini SAS HD 4x cable plug connectors shall not include keying.

5.4.3.4.2.2 Mini SAS HD 8x cable plug connector

The Mini SAS HD 8i cable plug connector is the dual 4 lane cable plug (free) connector defined in SFF-8644. Figure 55 shows the Mini SAS HD 8x cable plug connector. This connector is a modular version of repeating Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1). Module labeling is shown in figure 55. See figure 54 (see 5.4.3.4.2.1) for pin designations. Mini SAS HD 8x cable plug connectors shall not include keying.

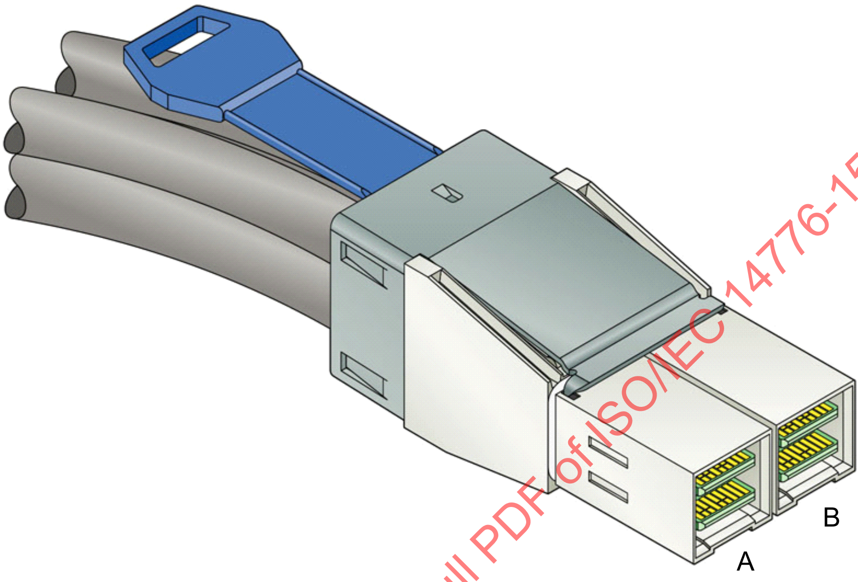


Figure 55 — Mini SAS HD 8x cable plug connector

Table 18 (see 5.4.3.4.2.6) define the pin assignments for the Mini SAS HD 4x cable plug connector (see 5.4.3.4.2.1). The pin assignments are repeated for each module of the Mini SAS 8x cable plug connector.

5.4.3.4.2.3 Mini SAS HD 4x receptacle connector

The Mini SAS HD 4x receptacle connector is the 4 lane receptacle (fixed) connector defined in SFF-8644. Figure 56 shows the Mini SAS HD 4x receptacle connector.

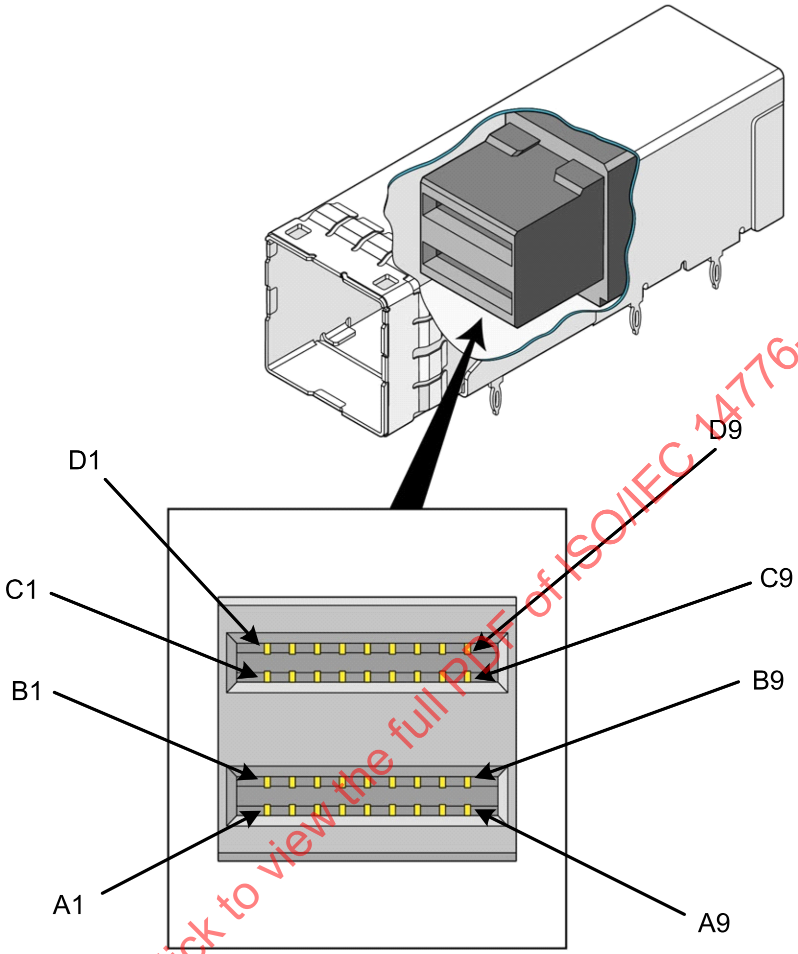


Figure 56 — Mini SAS HD 4x receptacle connector

Table 18 (see 5.4.3.4.2.6) defines the pin assignments for the Mini SAS HD 4x receptacle connector.

5.4.3.4.2.4 Mini SAS HD 8x receptacle connector

The Mini SAS HD 8x receptacle connector is a dual 4 lane receptacle (fixed) connector defined in SFF-8644. Figure 57 shows the Mini SAS HD 8x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.4.3.4.2.3). Module labeling is shown in figure 57. See figure 56 (see 5.4.3.4.2.3) for pin designations.

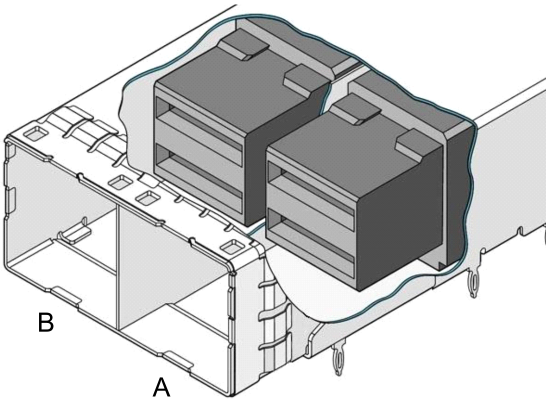


Figure 57 — Mini SAS HD 8x receptacle connector

Table 18 (see 5.4.3.4.2.6) defines the pin assignments for the Mini SAS HD 8x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.4.3.4.2.3). The Mini SAS HD 8x receptacle connector accepts one Mini SAS HD 8x plug connector (see 5.4.3.4.2.2) or one or two Mini SAS HD 4x plug connectors (see 5.4.3.4.2.1).

5.4.3.4.2.5 Mini SAS HD 16x receptacle connector

The Mini SAS HD 16x receptacle connector is a quad 4 lane receptacle (fixed) connector defined in SFF-8644. Figure 58 shows the Mini SAS HD 16x receptacle connector. This connector is a modular version of the Mini SAS HD 4x receptacle connector (see 5.4.3.4.2.3). Module labeling is shown in figure 58. See figure 56 (see 5.4.3.4.2.3) for pin designations.

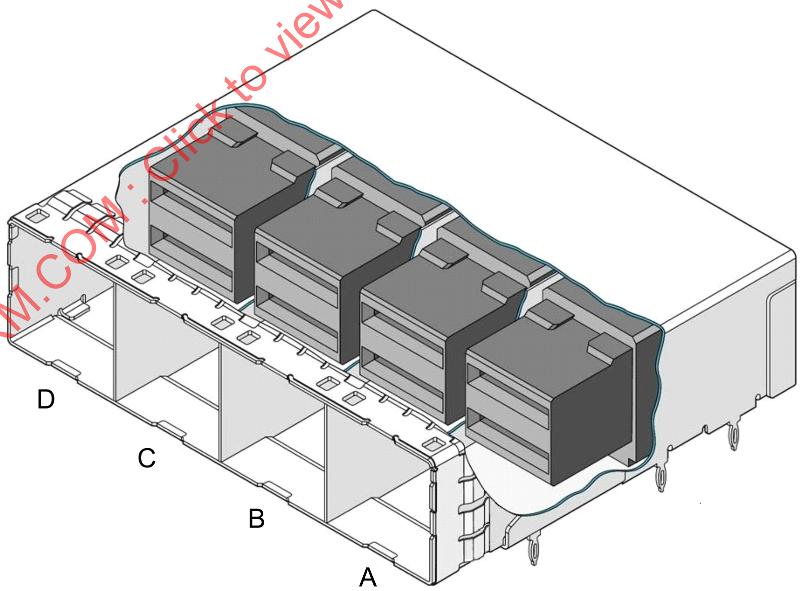


Figure 58 — Mini SAS HD 16x receptacle connector

Table 18 (see 5.4.3.4.2.6) defines the pin assignments for the Mini SAS HD 16x receptacle connector. The connector is a modular design of repeating Mini SAS HD 4x receptacles (see 5.4.3.4.2.3). The Mini SAS HD 16x receptacle connector accepts:

a) one or two Mini SAS HD 8x cable plug connectors (see 5.4.3.4.2.2);
b) one, two, three, to four Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1); or

c) a combination of one Mini SAS HD 8x cable plug connector (see 5.4.3.4.2.2) and one or two Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1).

A Mini SAS HD 4x cable plug connector (see 5.4.3.4.2.1) may be plugged into module A, module B, module C, or module D. A Mini SAS HD 8x cable plug connectors (see 5.4.3.4.2.2) may be plugged into module A and module B, module B and module C, or module C and module D.

5.4.3.4.2.6 Mini SAS HD 4x connector pin assignments

Table 18 defines the pin assignments for Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1) and Mini SAS HD 4x receptacle connectors (see 5.4.3.4.2.3) for controller applications using one, two, three, or four of the physical links.

Table 18 — Mini SAS HD 4x connector pin assignments and physical link usage

Signal	Pin usage based on number of physical links supported by the cable assembly [a]				Mating level [b]
	One	Two	Three	Four	
Rx 0-	B5	B5	B5	B5	Third
Rx 0+	B4	B4	B4	B4	
Rx 1-	N/C	A5	A5	A5	
Rx 1+	N/C	A4	A4	A4	
IntL [c]	A2	A2	A2	A2	Second
Reserved [c]	A1	A1	A1	A1	
ModPrsL [c]	B2	B2	B2	B2	
Vact [c]	B1	B1	B1	B1	
Rx 2-	N/C	N/C	B8	B8	Third
Rx 2+	N/C	N/C	B7	B7	
Rx 3-	N/C	N/C	N/C	A8	
Rx 3+	N/C	N/C	N/C	A7	
Tx 0-	D5	D5	D5	D5	Third
Tx 0+	D4	D4	D4	D4	
Tx 1-	N/C	C5	C5	C5	
Tx 1+	N/C	C4	C4	C4	
SDA [c]	C2	C2	C2	C2	Second
SCL [c]	C1	C1	C1	C1	
Vman [c]	D2	D2	D2	D2	
Vact [c]	D1	D1	D1	D1	
Tx 2-	N/C	N/C	D8	D8	Third
Tx 2+	N/C	N/C	D7	D7	
Tx 3-	N/C	N/C	N/C	C8	
Tx 3+	N/C	N/C	N/C	C7	
SIGNAL GROUND	A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6, D9				First

[a] N/C = not connected
[b] The mating level indicates the physical dimension of the contact (see SFF-8644).
[c] Table 19 (see 5.4.3.4.2.7) defines the connection requirements of this signal.

5.4.3.4.2.7 Mini SAS HD external connector management interface

Each 4x module shall include a 2-wire serial management interface to:

a) monitor circuitry residing in the cable assembly;
b) control circuitry residing in the cable assembly; and
c) obtain physical characteristics of the cable encoded in a non-volatile storage device located in the cable assembly.

Table 19 defines the connection requirements of the management interface signals. Mini SAS HD 4x receptacle connectors (see 5.4.3.4.2.3), Mini SAS HD 8x receptacle connectors (see 5.4.3.4.2.4), Mini SAS HD 16x receptacle connectors (see 5.4.3.4.2.5), Mini SAS HD 4x cable plug connectors (see 5.4.3.4.2.1), and Mini SAS HD 8x cable plug connectors (see 5.4.3.4.2.2) shall support the signals in table 19 in each 4x module. See SFF-8449 for a complete signal definition, management interface memory map, and timing diagrams for the two-wire interface.

Table 19 — Management interface connection requirements

Signal	Connection requirements [a]
IntL	Active Low Module Interrupt: The cable assembly shall assert this pin to indicate an interrupt bit has been set to one in the management interface memory map. This pin shall be connected to Vman on the receptacle side of the management interface. The source of the interrupt may be identified using the 2-wire serial management interface. If a cable assembly does not support interrupts, then all interrupt bits in the cable management interface memory map shall be set to zero and the cable assembly shall negate this pin (e.g., all interrupt bits of a passive cable assembly may be programmed to a clear state and the IntL pin not connected on the cable plug side of the management interface).
ModPrsL	Active Low Module Present: On the cable plug side of the management interface, ModPrsL shall be connected directly to the signal ground pins specified in table 18 (see 5.4.3.4.2.6). ModPrsL shall be connected to Vman on the receptacle side of the management interface to negate this signal when the plug is not fully mated to the receptacle.
Reserved	This pin shall be not connected on the receptacle side and cable plug side of the management interface.
SCL	Two-wire interface clock: The receptacle side of the management interface shall connect this signal to Vman.
SDA	Two-wire interface data: The receptacle side of the management interface shall connect this signal to Vman.
Vact	Active cable power: If the receptacle side of the management interface supports active cable assemblies, then it shall provide all non-management interface power to the cable assembly on the Vact pins. To support equal loading, both Vact pins shall be connected together on the receptacle side of the management interface. If the receptacle side of the management interface does not support active cable assemblies, then the Vact pins should be not connected.
Vman	Management interface power: The receptacle side of the management interface shall provide power on the Vman pin to enable the management interface circuitry of the cable. Power may be removed to reset the management circuitry in the cable assembly.

[a] Electrical characteristics are defined in SFF-8449.

5.4.3.4.2.8 Mini SAS HD external connector memory map

SFF-8449 defines the Mini SAS HD external connector management interface memory map. The Mini SAS HD external cable assembly shall support the following management interface memory map registers:

a) supported SAS baud rate;
b) vendor name;

c) vendor part number;
d) vendor revision;
e) copper cable attenuation;
f) power class;
g) minimum operating voltage;
h) transmitter technology;
i) cable width; and
j) propagation delay.

5.4.3.4.3 QSFP+ connectors

5.4.3.4.3.1 QSFP+ cable plug

The QSFP+ cable plug connector is the free (plug) 38-circuit connector defined in SFF-8436. Figure 59 shows the QSFP+ cable plug connector.

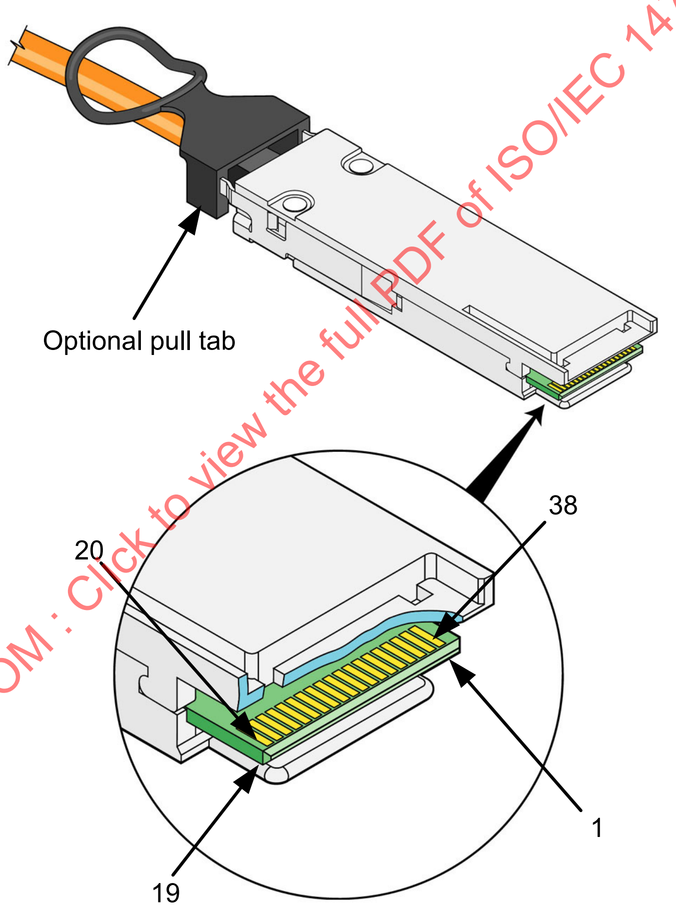


Figure 59 — QSFP+ cable plug connector

Table 20 (see 5.4.3.4.3.3) define the pin assignments for the QSFP+ cable plug connector.

The QSFP+ cable plug connectors shall not include keying.

5.4.3.4.3.2 QSFP+ receptacle

The QSFP+ receptacle connector is the fixed (receptacle) 38-circuit connector defined in SFF-8436. Figure 60 shows the QSFP+ receptacle connector.

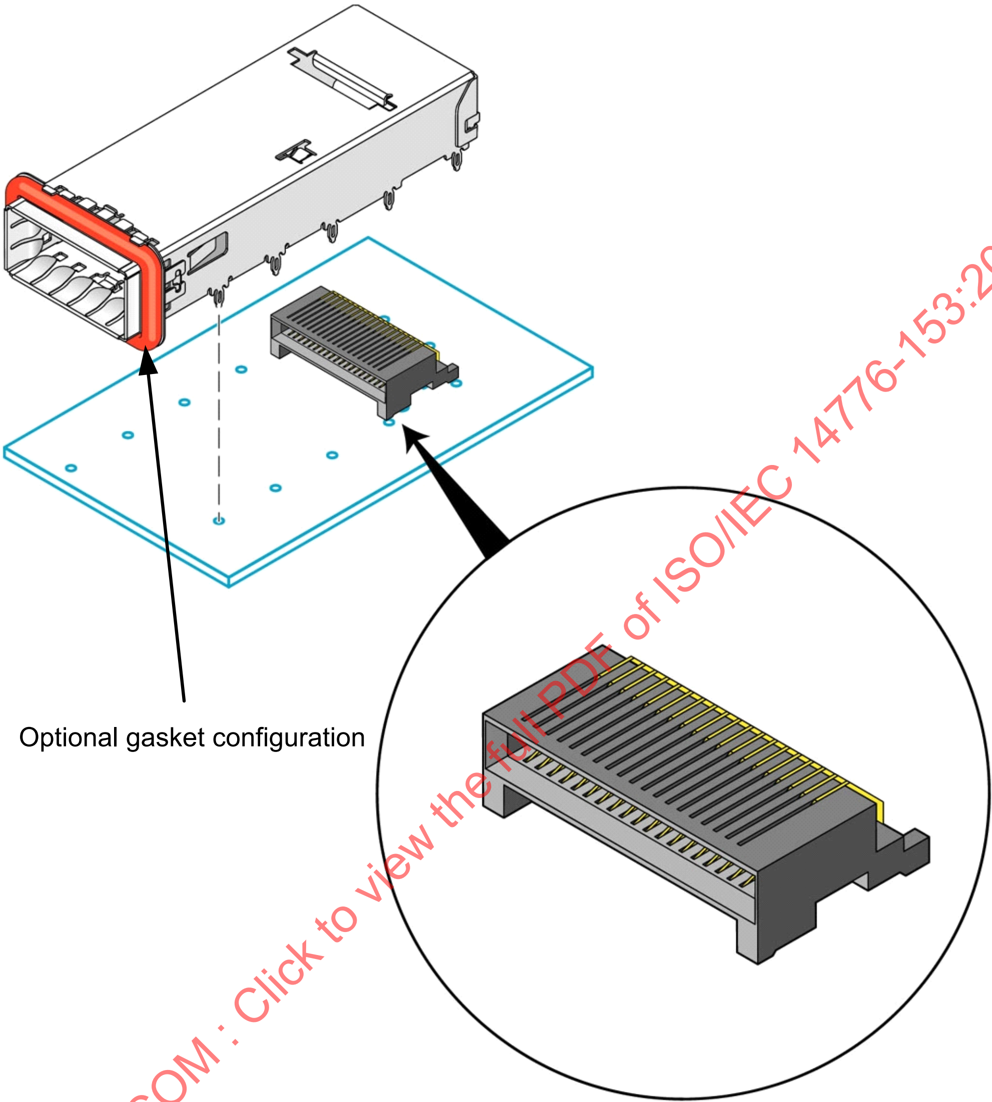


Figure 60 — QSFP+ receptacle **connector**

Table 20 (see 5.4.3.4.3.3) define the pin assignments for the QSFP+ receptacle connector.

The QSFP+ receptacle connectors shall not include keying.

5.4.3.4.3.3 QSFP+ connector pin assignments

Table 20 defines the pin assignments for QSFP+ connectors (see 5.4.3.4.3.1 and 5.4.3.4.3.2). Specific pins are used to provide managed cable communication and power to the cable assembly.

Table 20 — QSFP+ connector pin assignments (part 1 of 2)

Pin	Signal	Description	Mating level [a]
1	GND [b]	Ground	First
2	Tx2n	Transmitter inverted data input	Third
3	Tx2p	Transmitter non-inverted data input	Third
4	GND [b]	Ground	First
5	Tx4n	Transmitter inverted data input	Third
6	Tx4p	Transmitter non-inverted data input	Third
7	GND [b]	Ground	First
8	ModSelL	Module select	Third
9	ResetL	Module reset	Third
10	Vcc Rx [c]	+3.3V power supply receiver	Second
11	SCL	2-wire serial interface clock	Third
12	SDA	2-wire serial interface data	Third
13	GND [b]	Ground	First
14	Rx3p	Receiver non-inverted data output	Third
15	Rx3n	Receiver inverted data output	Third
16	GND [b]	Ground	First
17	Rx1p	Receiver non-inverted data output	Third
18	Rx1n	Receiver inverted data output	Third
19	GND [b]	Ground	First
20	GND [b]	Ground	First
21	Rx2n	Receiver inverted data output	Third
22	Rx2p	Receiver non-inverted data output	Third
23	GND [b]	Ground	First
24	Rx4n	Receiver inverted data output	Third
25	Rx4p	Receiver non-inverted data output	Third
26	GND [b]	Ground	First
27	ModPrsL	Module present	Third
28	IntL	Interrupt	Third
29	Vcc Tx [c]	+3.3V power supply transmitter	Second

Table 20 — QSFP+ connector pin assignments (part 2 of 2)

Pin	Signal	Description	Mating level [a]
30	Vcc1 [c]	+3.3V power supply	Second
31	LPMode	Low power mode	Third
32	GND [b]	Ground	First
33	Tx3p	Transmitter non-inverted data input	Third
34	Tx3n	Transmitter inverted data input	Third
35	GND [b]	Ground	First
36	Tx1p	Transmitter non-inverted data input	Third
37	Tx1n	Transmitter inverted data input	Third
38	GND [b]	Ground	First

[a] The mating level indicates the physical dimension of the contact. See SFF-8436.
[b] GND is the symbol for signal ground and power ground for QSFP+. Signal ground and power ground are common within the QSFP+ cable connector and all voltages are referenced to this ground unless otherwise specified. Signal ground and power ground shall be connected directly to the host board signal ground.
[c] Power shall be applied concurrently to Vcc Rx, Vcc1, and Vcc Tx. Within the QSFP+ cable connector, Vcc Rx, Vcc1, and Vcc Tx may be connected in any combination.

5.4.3.4.3.4 QSFP+ memory map

The memory map for QSFP+ is used for identification information, cable characteristics, control functions, and digital monitoring. The 2-wire serial interface is required for all QSFP+ devices. SFF-8436 defines the supported SAS baud rate codes. See SFF-8436 for register map details and the operation of the 2-wire serial interface.

5.4.4 Cable assemblies

5.4.4.1 SAS internal cable assemblies

5.4.4.1.1 SAS Drive cable assemblies

A SAS Drive cable assembly is either:

a) a single-port SAS Drive cable assembly; or
b) a dual-port SAS Drive cable assembly.

A SAS Drive cable assembly has:

a) a SAS Drive cable receptacle connector (see 5.4.3.3.1.2) on the SAS target device end; and
b) a SATA signal cable receptacle connector (see SATA) on the SAS initiator device or expander device end (see SPL).

The power and READY LED signal connection is vendor specific.

A SAS initiator device shall use a SATA host plug connector (see SATA) for connection to a SAS Drive cable assembly. The signal assignment for the SAS initiator device or expander device (see SPL) with this connector shall be the same as that defined for a SATA host (see SATA).

Figure 61 shows the Single-port SAS Drive cable assembly.

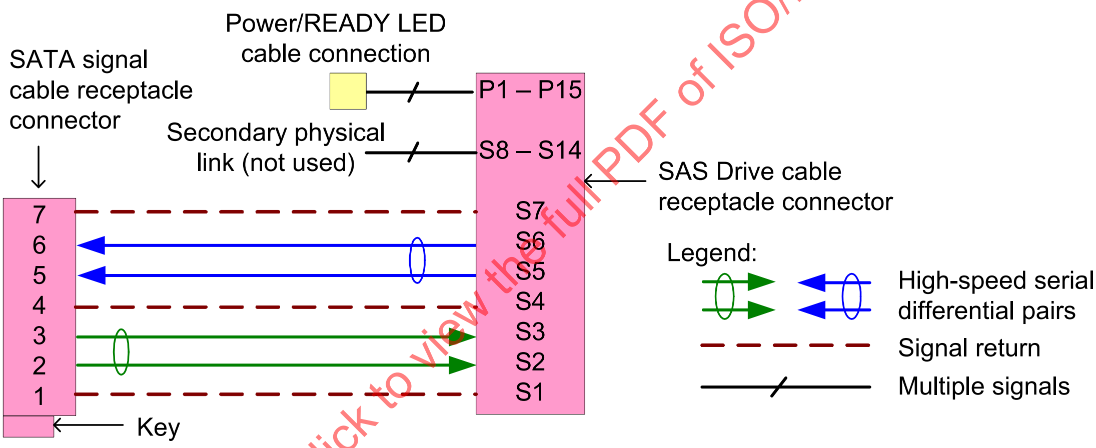


Figure 61 — Single-port SAS Drive cable assembly

Figure 62 shows the Dual-port SAS Drive cable assembly.

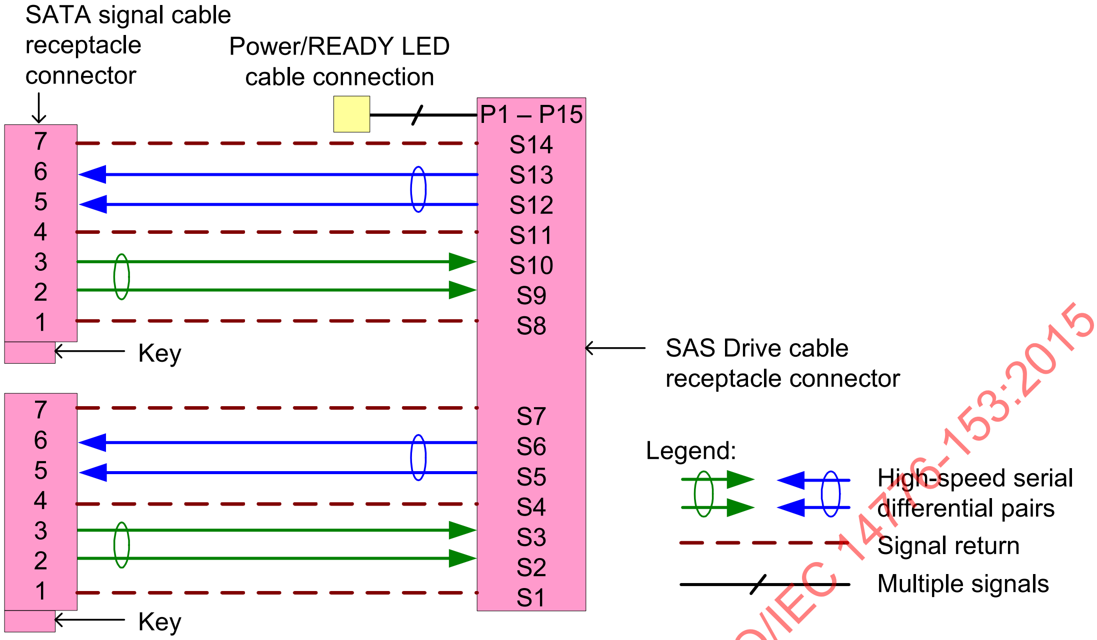


Figure 62 — Dual-port SAS Drive cable assembly

5.4.4.1.2 SAS internal symmetric cable assemblies

5.4.4.1.2.1 SAS internal symmetric cable assemblies overview

A SAS internal symmetric cable assembly has:

a) a SAS 4i cable receptacle connector (see 5.4.3.3.2.1) on each end (see 5.4.4.1.2.2);
b) a Mini SAS 4i cable plug connector (see 5.4.3.3.3.1) on each end (see 5.4.4.1.2.3);
c) a Mini SAS HD 4i cable plug connector on each end;
d) a Mini SAS HD 8i cable plug connector on each end;
e) a SAS 4i cable receptacle connector on one end and a Mini SAS 4i cable plug connector on the other end, with vendor specific sidebands (see 5.4.4.1.2.5);
f) a SAS 4i cable receptacle connector on the controller end and a Mini SAS 4i cable plug connector on the backplane end, with sidebands supporting SGPIO (see 5.4.4.1.2.7);
g) a Mini SAS 4i cable plug connector on the controller end and a SAS 4i cable receptacle connector on the backplane end, with sidebands supporting SGPIO (see 5.4.4.1.2.8); or
h) a Mini SAS 4i cable plug connector on one end and a Mini SAS HD 4i cable plug connector on the other end (see 5.4.4.1.2.9).

In a SAS internal symmetric cable assembly, the Tx signals on one end shall be connected to Rx signals on the other end (e.g., a Tx + of one connector shall connect to an Rx + of the other connector. SAS internal symmetric cable assemblies should be labeled to indicate how many physical links are included (e.g., 1X, 2X, 3X, and 4X on each connector's housing).

5.4.4.1.2.2 SAS internal symmetric cable assembly - SAS 4i

Figure 63 shows the SAS internal symmetric cable assembly with SAS 4i cable receptacle connectors at each end.

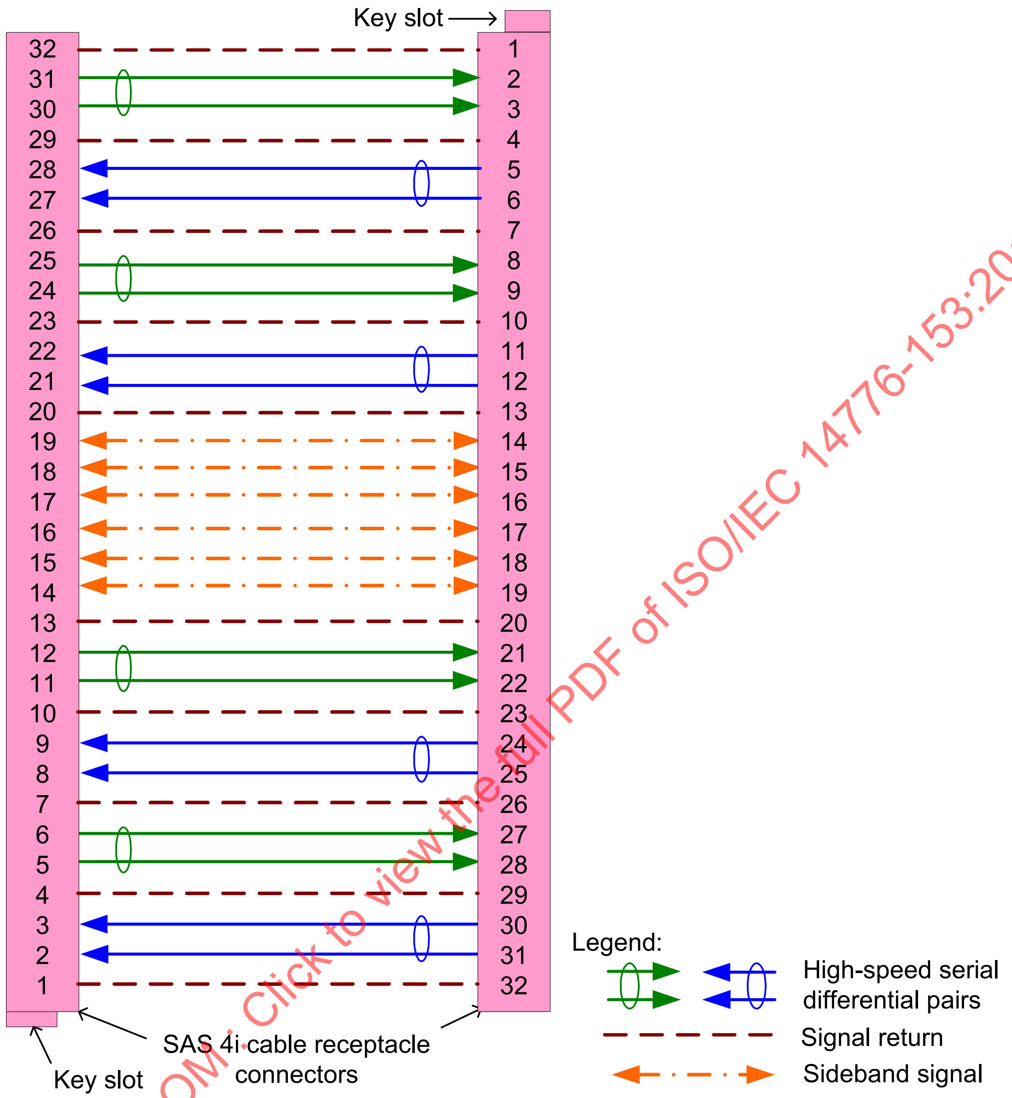


Figure 63 — SAS internal symmetric cable assembly - SAS 4i

In addition to the signal return connections shown in figure 63, one or more of the signal returns may be connected together in this cable assembly.

For controller-to-backplane applications, this cable assembly may support one to four physical links. SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, this cable assembly shall support all four physical links and the controllers should use all four physical links, because one controller's physical links 0 and 1 are attached the other controller's physical links 3 and 2, respectively. If both controllers use one or two physical links starting with physical links 0, communication is not possible. If both controllers use physical links 0, 1, and 2, then only communication over physical links 1 and 2 is possible. SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND5 of the other controller).

5.4.4.1.2.3 SAS internal symmetric cable assembly - Mini SAS 4i

Figure 64 shows the SAS internal cable assembly with Mini SAS 4i cable plug connectors at each end.

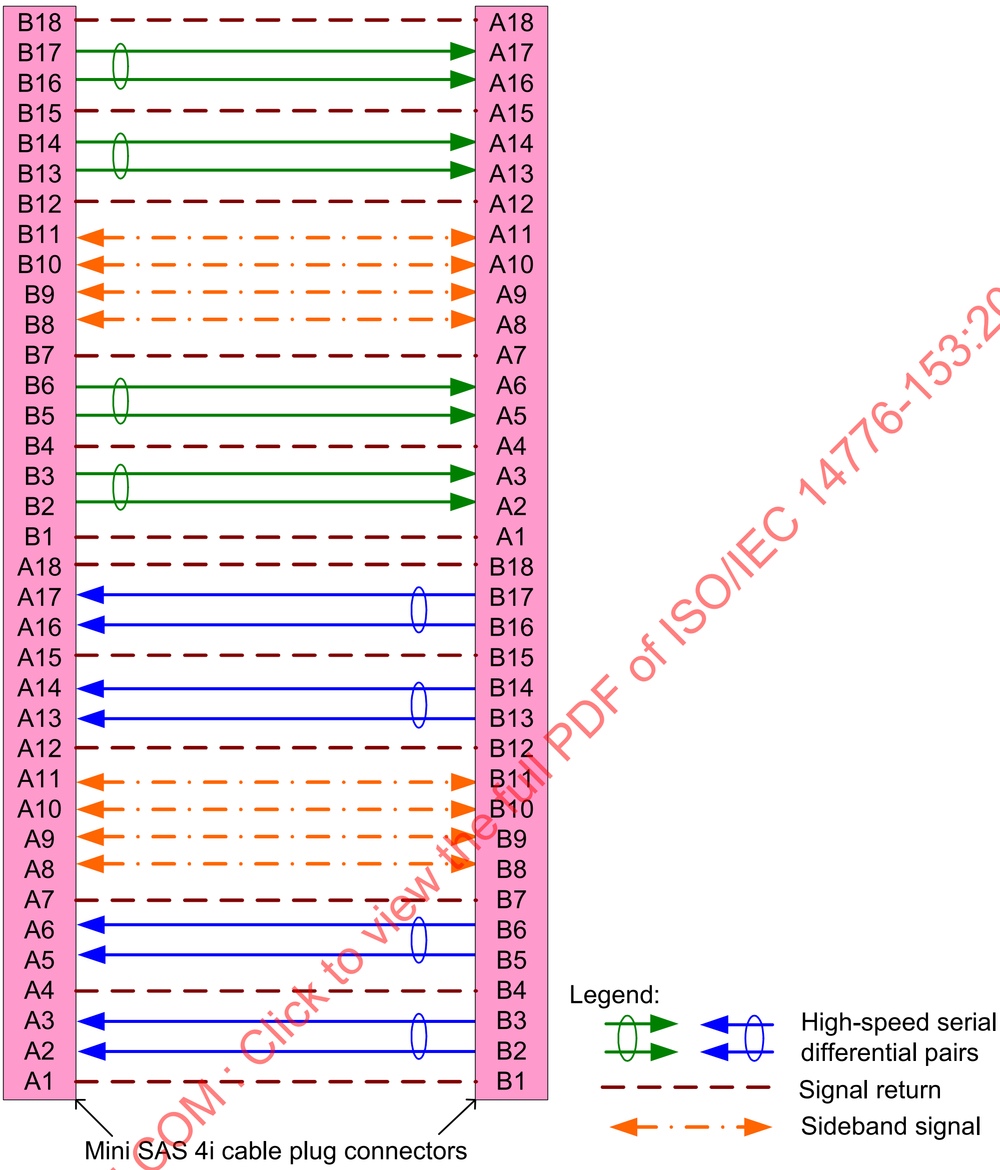


Figure 64 — SAS internal symmetric cable assembly - Mini SAS 4i

In addition to the signal return connections shown in figure 64, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.2.4 SAS internal symmetric cable assembly - Mini SAS HD 4i

Figure 65 shows the SAS internal cable assembly with Mini SAS HD 4i cable plug connectors at each end.

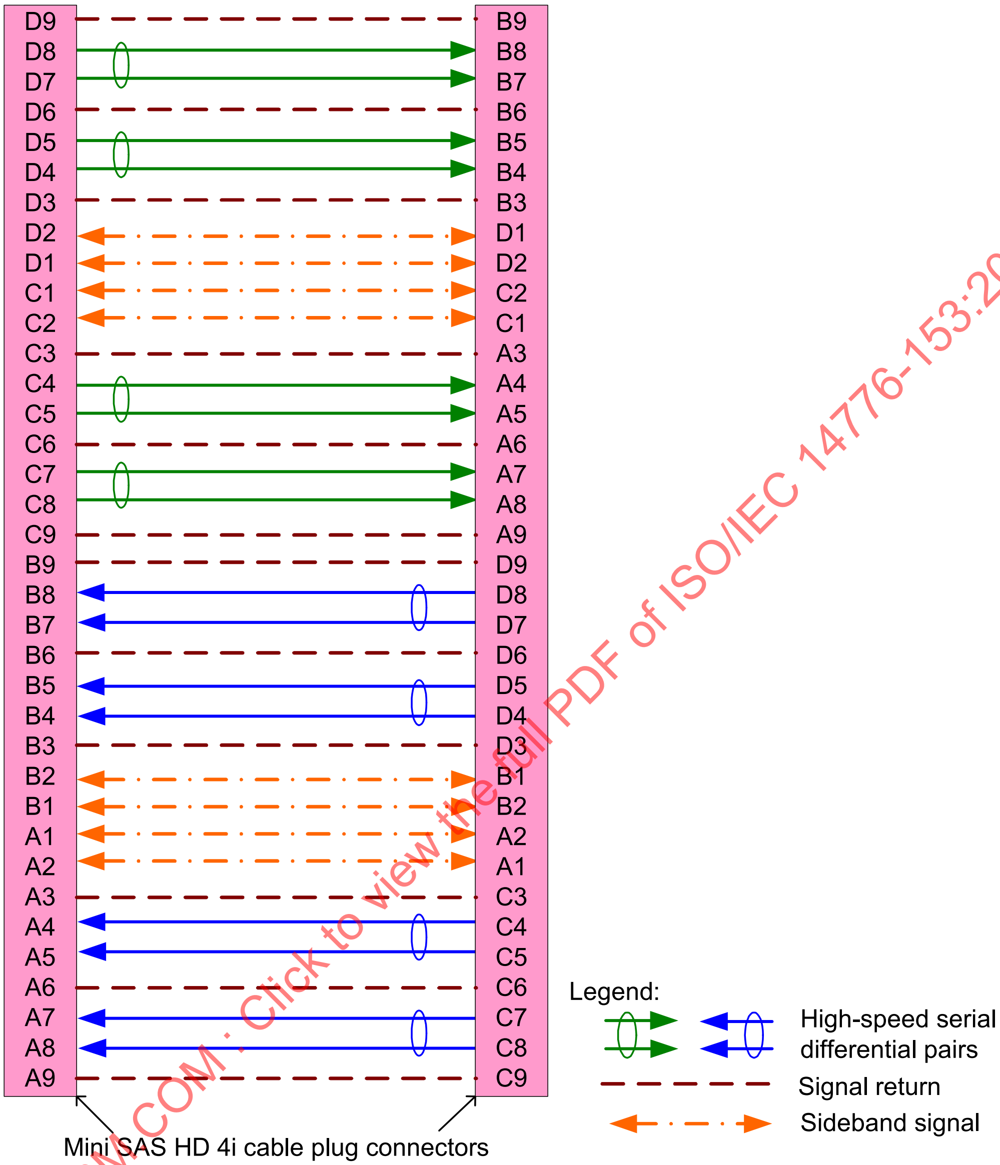


Figure 65 — SAS internal symmetric cable assembly - Mini SAS HD 4i

In addition to the signal return connections shown in figure 65, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.2.5 SAS internal symmetric cable assembly - Mini SAS HD 8i

Figure 66 shows the SAS internal cable assembly with Mini SAS HD 8i cable plug connectors at each end.

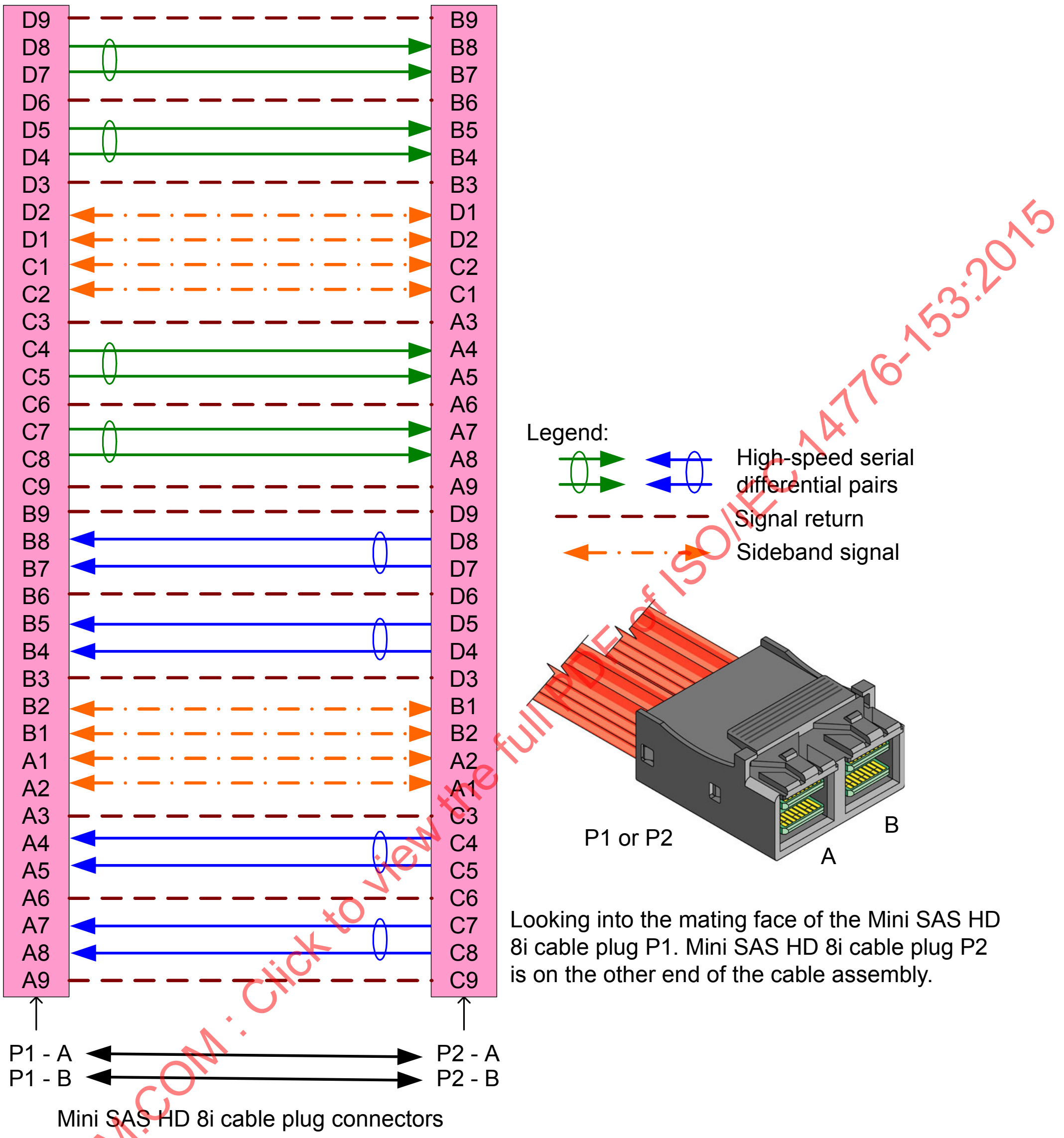


Figure 66 — SAS internal symmetric cable assembly - Mini SAS HD 8i

In addition to the signal return connections shown in figure 66, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.4.3.3.4.5 for connector module pin assingments.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.2.6 SAS internal symmetric cable assembly - SAS 4i to Mini SAS 4i with vendor specific sidebands

Figure 67 shows the SAS internal symmetric cable assembly with a SAS 4i cable receptacle connector at one end and a Mini SAS 4i cable plug connector at the other end, with vendor specific sidebands.

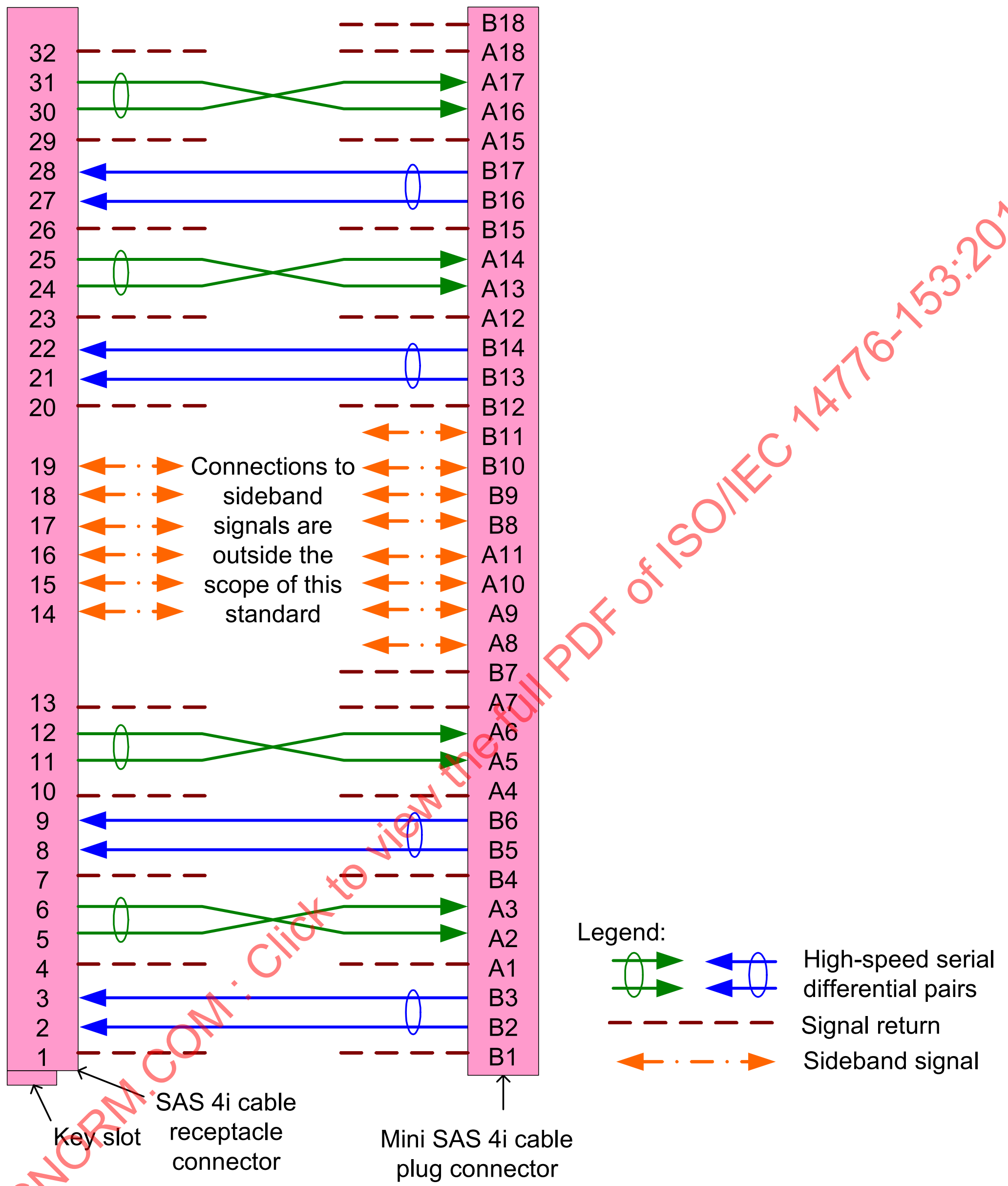


Figure 67 — SAS internal symmetric cable assembly - SAS 4i to Mini SAS 4i with vendor specific sidebands

NOTE 7 This cable assembly may require different SIDEBAND signal routing based on whether the controller or backplane is using the SAS 4i connector.

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

For controller-to-backplane applications with the SAS 4i cable receptacle connector on the controller end, this cable assembly may support one to four physical links.

For controller-to-controller applications, this cable assembly may support one to four physical links.

For controller-to-backplane applications with the Mini SAS 4i cable receptacle connector on the controller end, this cable assembly shall support all four physical links and the controller should use all four physical links, because the controller's physical links 0, 1, 2, and 3 are attached to the backplane's physical links 3, 2, 1, and 0, respectively. If both the controller and the backplane use one or two physical links starting with physical links 0, communication is not possible. If both the controller and the backplane use physical links 0, 1, and 2, then only communication over physical links 1 and 2 is possible.

5.4.4.1.2.7 SAS internal symmetric cable assembly - SAS 4i controller to Mini SAS 4i backplane with SGPIO

Figure 68 shows the SAS internal symmetric cable assembly with a SAS 4i cable receptacle connector at the controller end and a Mini SAS 4i cable plug connector at the backplane end, with sidebands connected to support SGPIO (see SFF-8485).

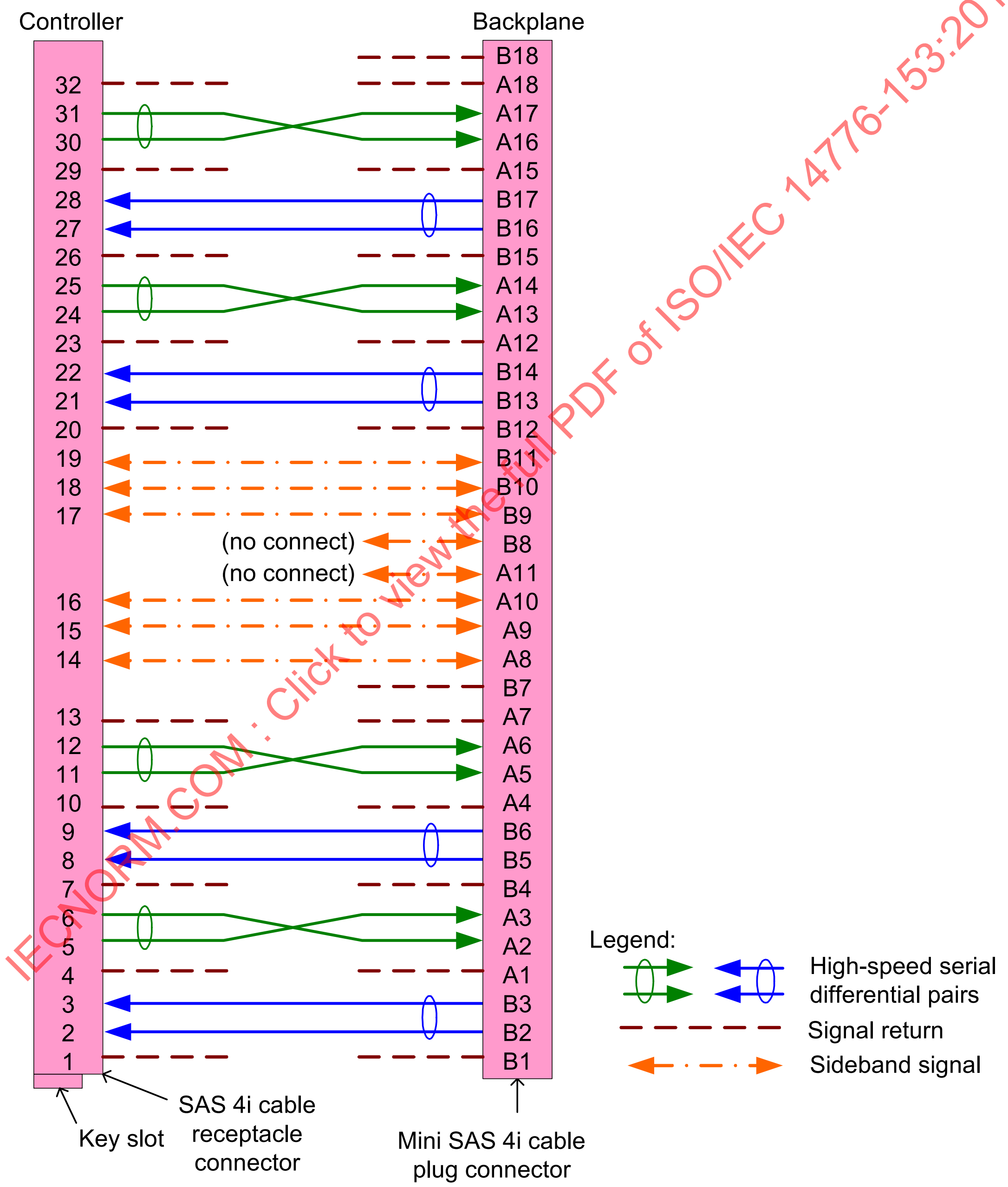


Figure 68 — SAS internal symmetric cable assembly - SAS 4i controller to Mini SAS 4i backplane with SGPIO

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

5.4.4.1.2.8 SAS internal symmetric cable assembly - Mini SAS 4i controller to SAS 4i backplane with SGPIO

Figure 69 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable receptacle connector at the controller end and a SAS 4i cable plug connector at the backplane end, with sidebands connected to support SGPIO (see SFF-8485).

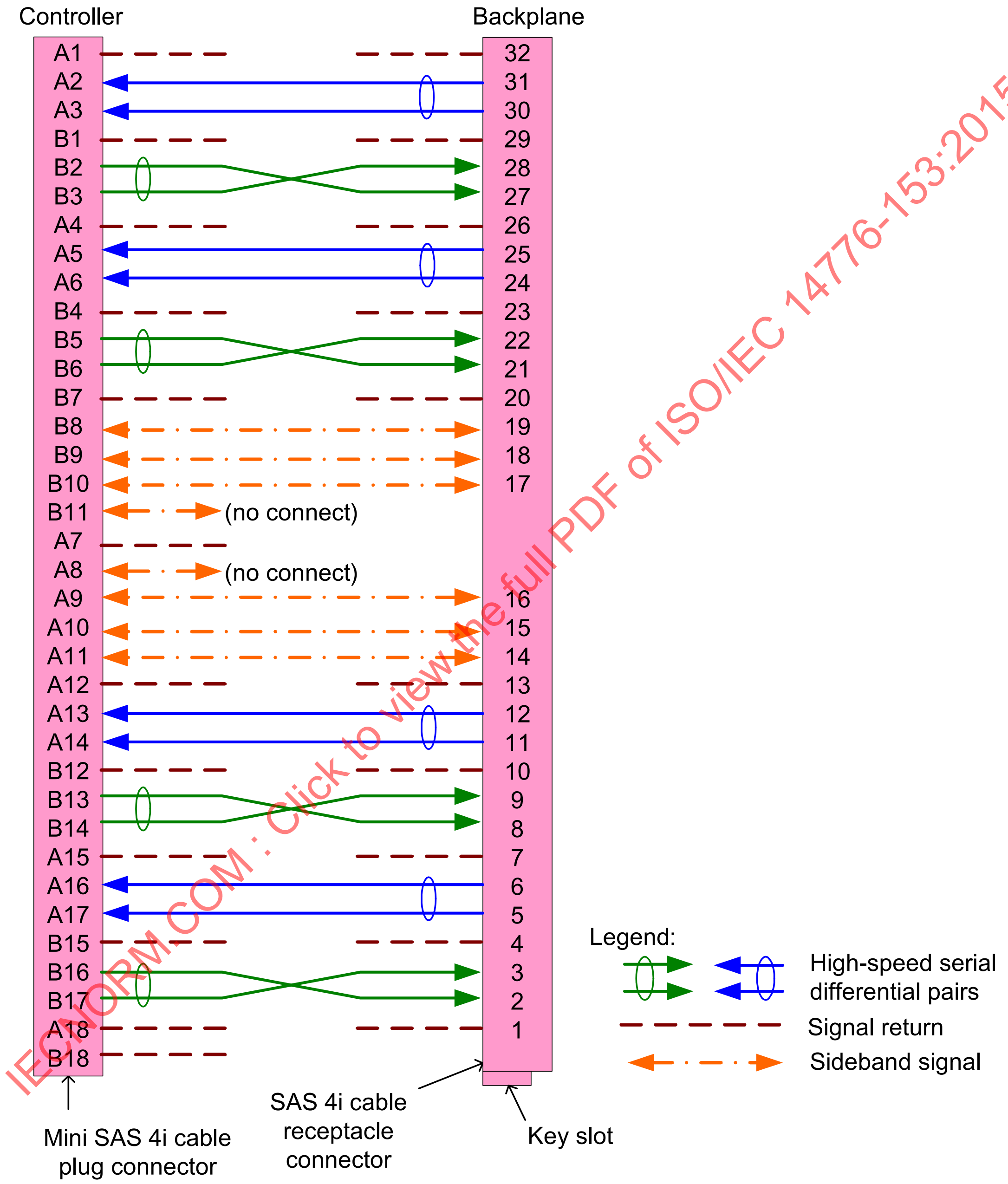


Figure 69 — SAS internal symmetric cable assembly - Mini SAS 4i controller to SAS 4i backplane with SGPIO

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

5.4.4.1.2.9 SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

Figure 70 shows the SAS internal symmetric cable assembly with a Mini SAS 4i cable plug connector at one end and a Mini SAS HD 4i cable plug connector at the other end.

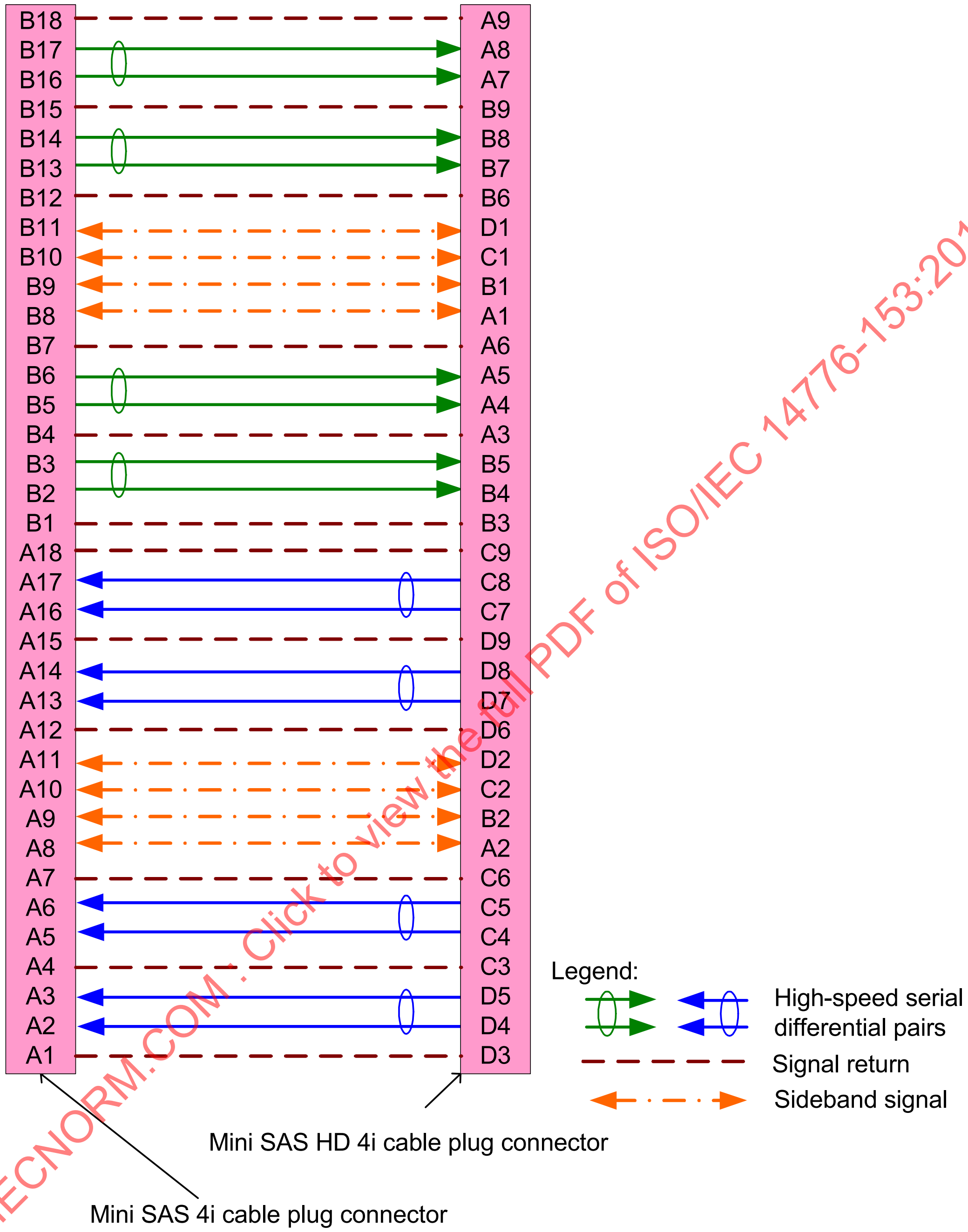


Figure 70 — SAS internal symmetric cable assembly - Mini SAS 4i to Mini SAS HD 4i

In addition to the signal return connections shown in figure 70, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to four physical links.

For controller-to-backplane applications, SIDEBAND signals on the controller are attached to the corresponding SIDEBAND signals on the backplane (e.g., SIDEBAND0 of the controller is attached to SIDEBAND0 of the backplane).

For controller-to-controller applications, SIDEBAND signals on one controller are not attached to their corresponding SIDEBAND signals on the other controller (e.g., SIDEBAND0 of one controller is attached to SIDEBAND7 of the other controller).

5.4.4.1.3 SAS internal fanout cable assemblies

5.4.4.1.3.1 SAS internal fanout cable assemblies overview

A SAS internal fanout cable assembly is either:

a) a SAS internal controller-based fanout cable assembly (see 5.4.4.1.3.2) with:
   A) a SAS 4i cable receptacle connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end;
   B) a Mini SAS 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end; or
   C) a Mini SAS HD 4i cable plug connector on one end (i.e., the controller end) and four SAS Drive cable receptacle connectors on the other end;

   or

b) a SAS internal backplane-based fanout cable assembly (see 5.4.4.1.3.3) with:
   A) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a SAS 4i cable receptacle connector on the other end (i.e., the backplane end);
   B) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS 4i cable plug connector on the other end (i.e., the backplane end); or
   C) four SATA signal cable receptacle connectors on one end (i.e., the controller end) and a Mini SAS HD 4i cable plug connector on the other end (i.e., the backplane end).

In a SAS internal fanout symmetric cable assembly, the Tx signals on one end shall be connected to Rx signals on the other end (e.g., a Tx + of one connector shall connect to an Rx + of the other connector).

5.4.4.1.3.2 SAS internal controller-based fanout cable assemblies

Figure 71 shows the SAS internal controller-based fanout cable assembly with a SAS 4i cable receptacle connector at the controller end.

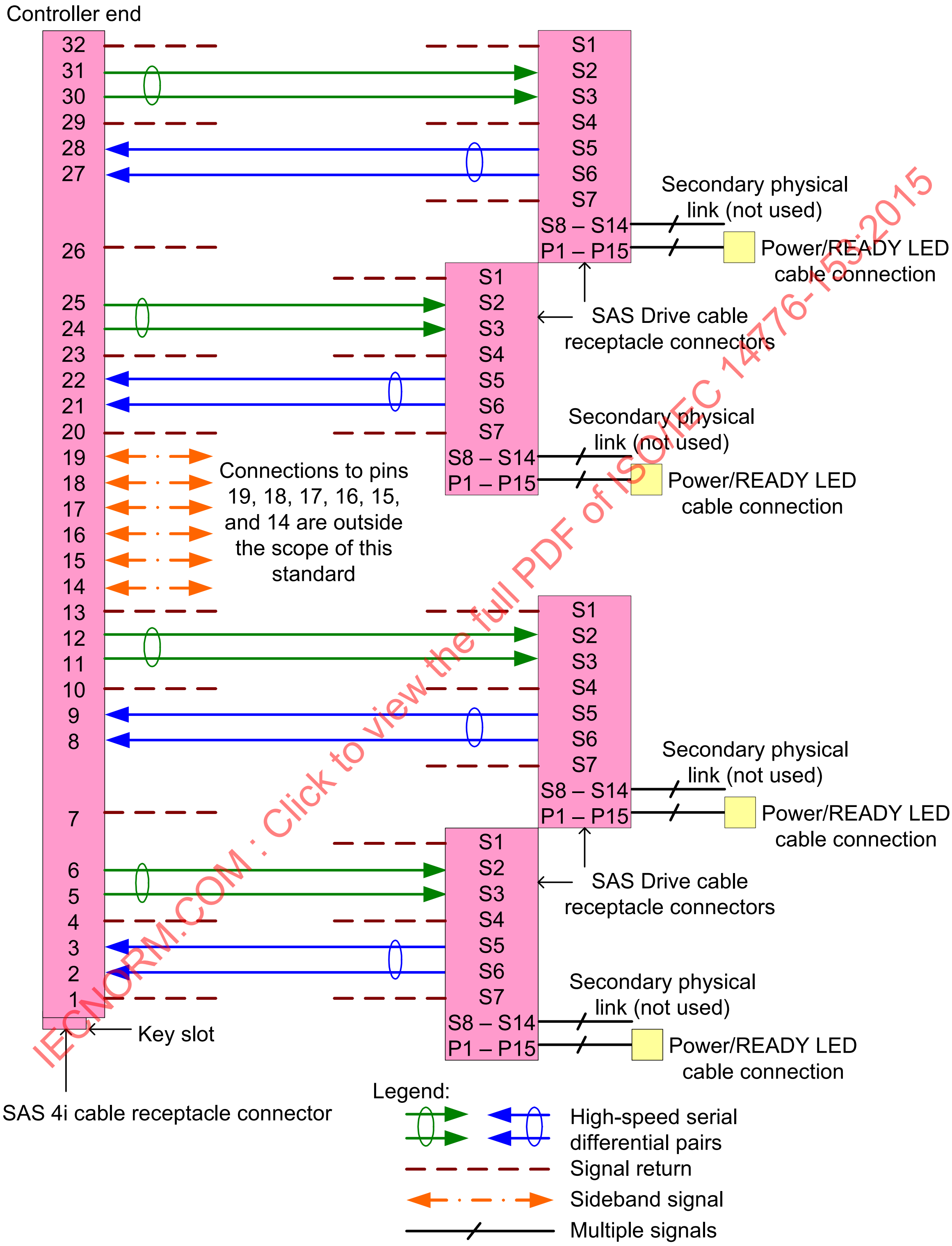


Figure 71 — SAS internal controller-based fanout cable assembly - SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 72 shows the SAS internal controller-based fanout cable assembly with a Mini SAS 4i cable plug connector at the controller end.

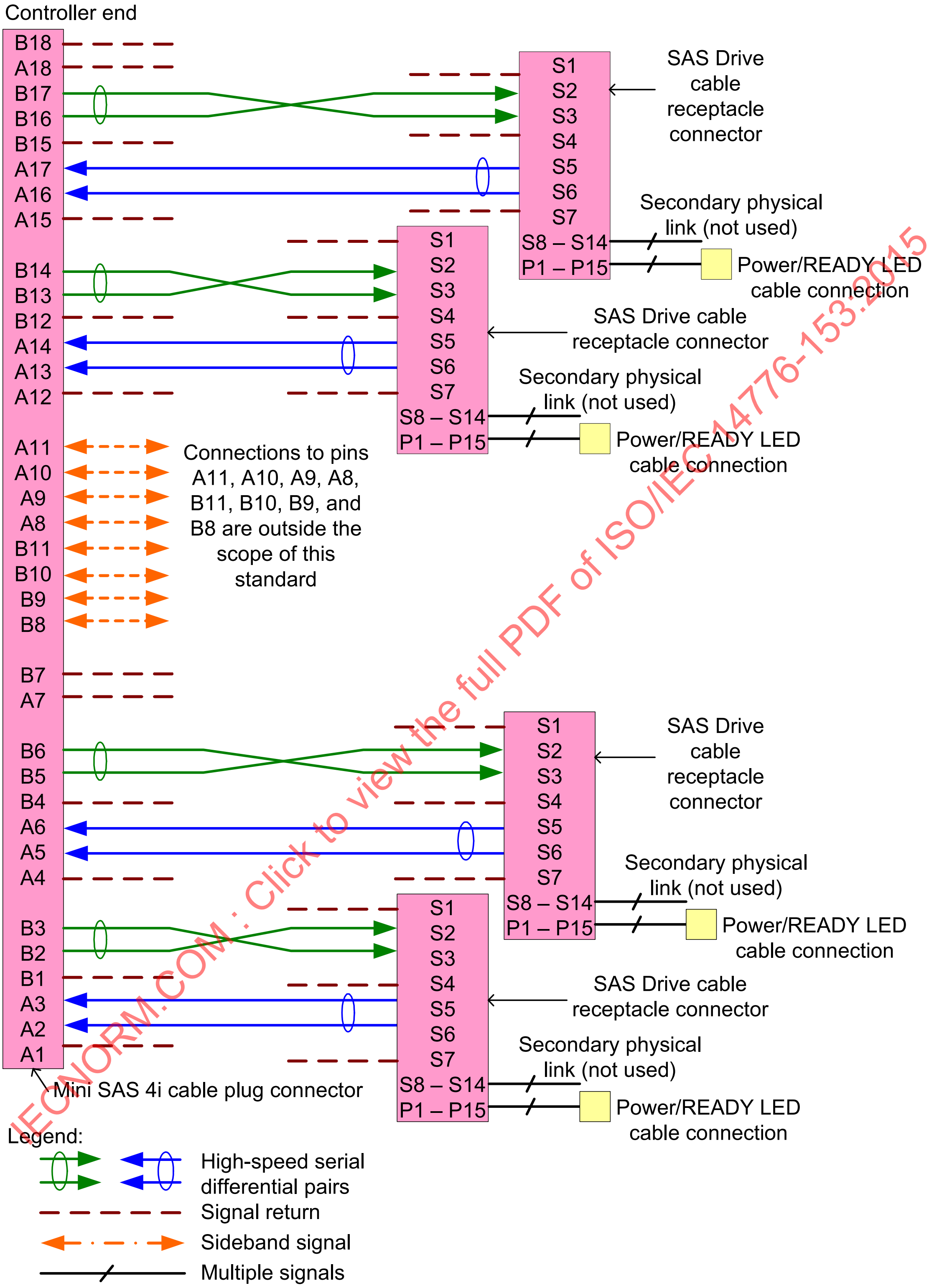


Figure 72 — SAS internal controller-based fanout cable assembly - Mini SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 73 shows the SAS internal controller-based fanout cable assembly with a Mini SAS HD 4i cable plug connector at the controller end.

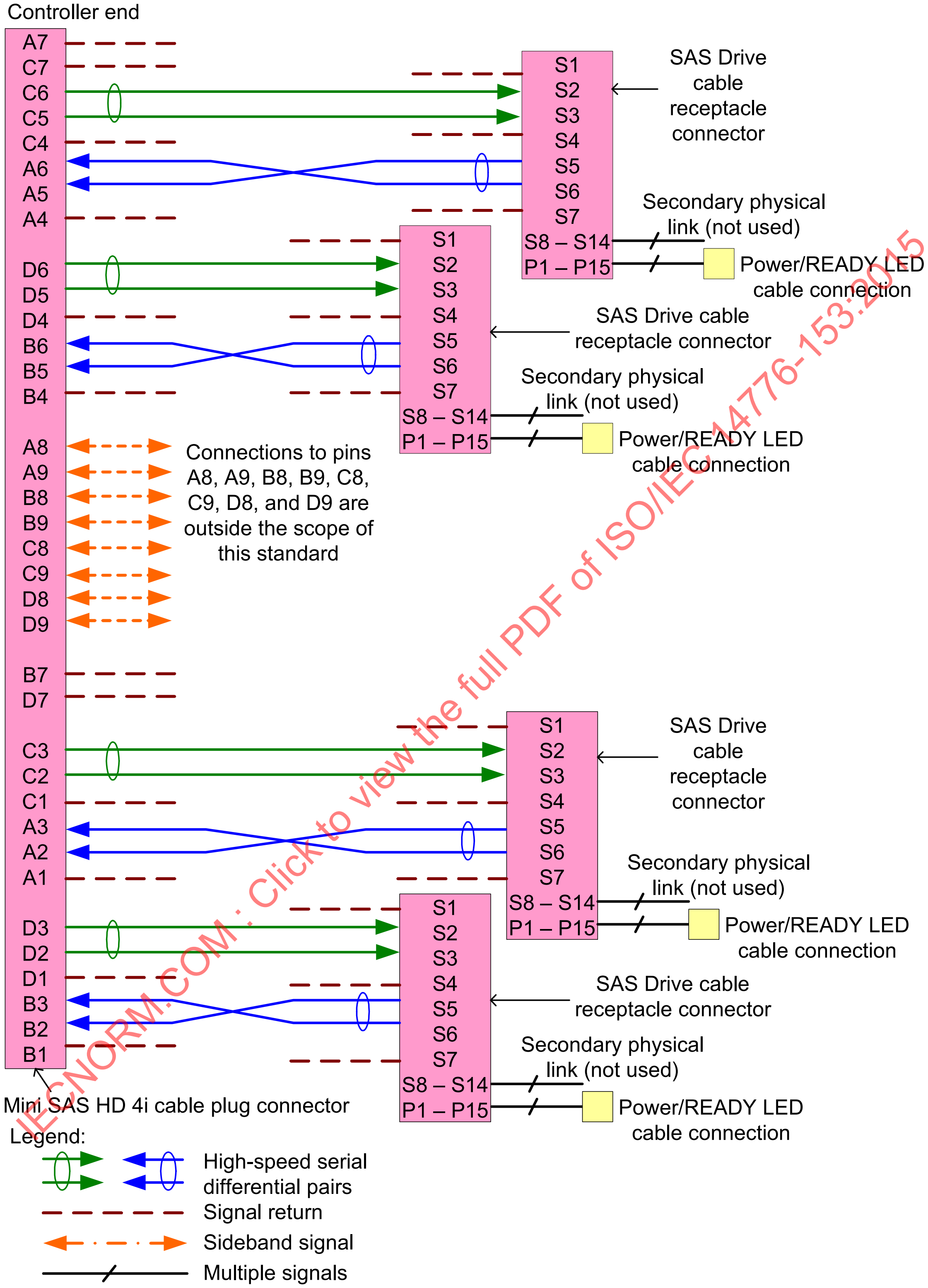


Figure 73 — SAS internal controller-based fanout cable assembly - Mini SAS HD 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.1.3.3 SAS internal backplane-based fanout cable assemblies

Figure 74 shows the SAS internal backplane-based fanout cable assembly with the SAS 4i cable receptacle connector.

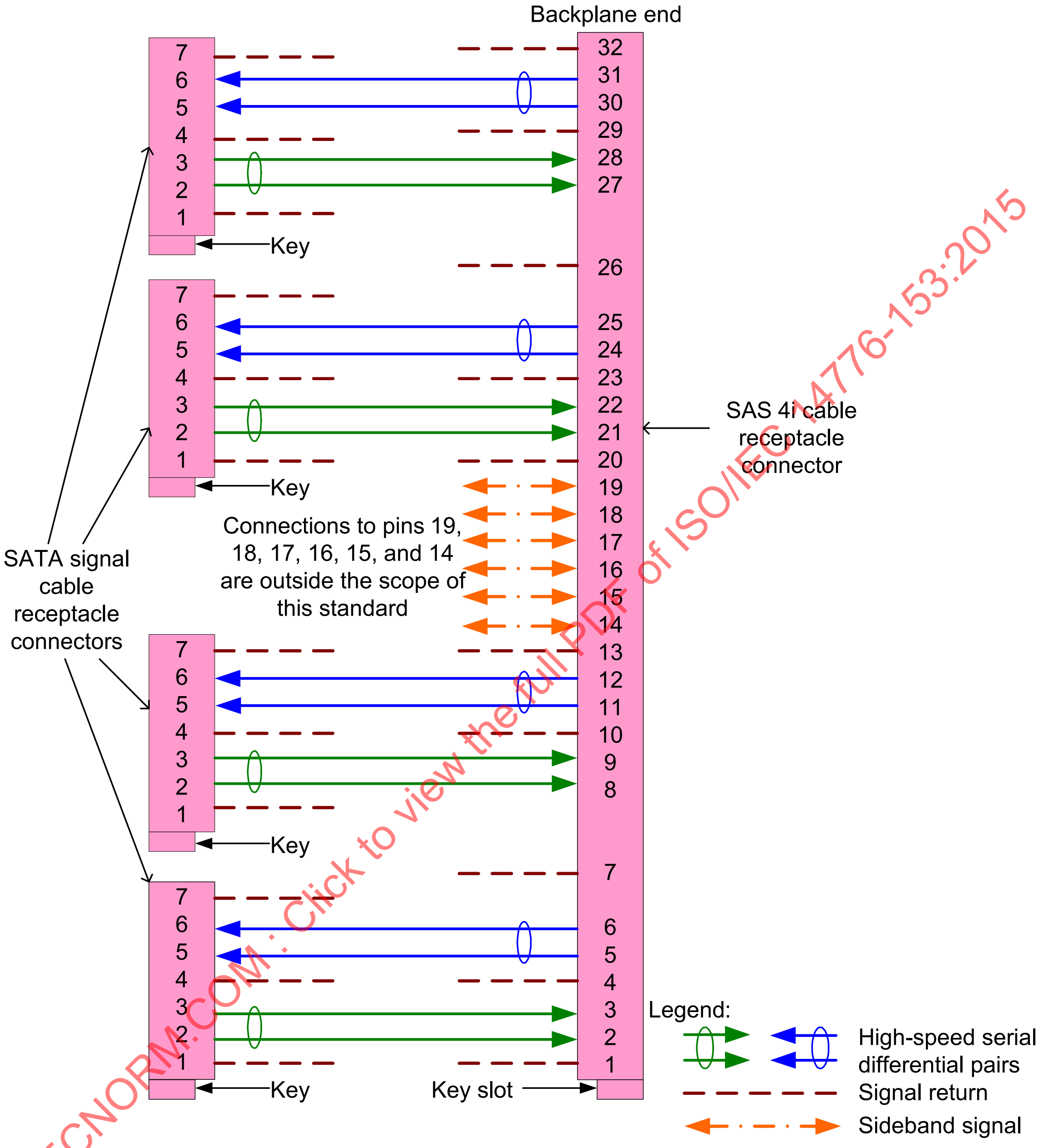


Figure 74 — SAS internal backplane-based fanout cable assembly - SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 75 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS 4i cable receptacle connector.

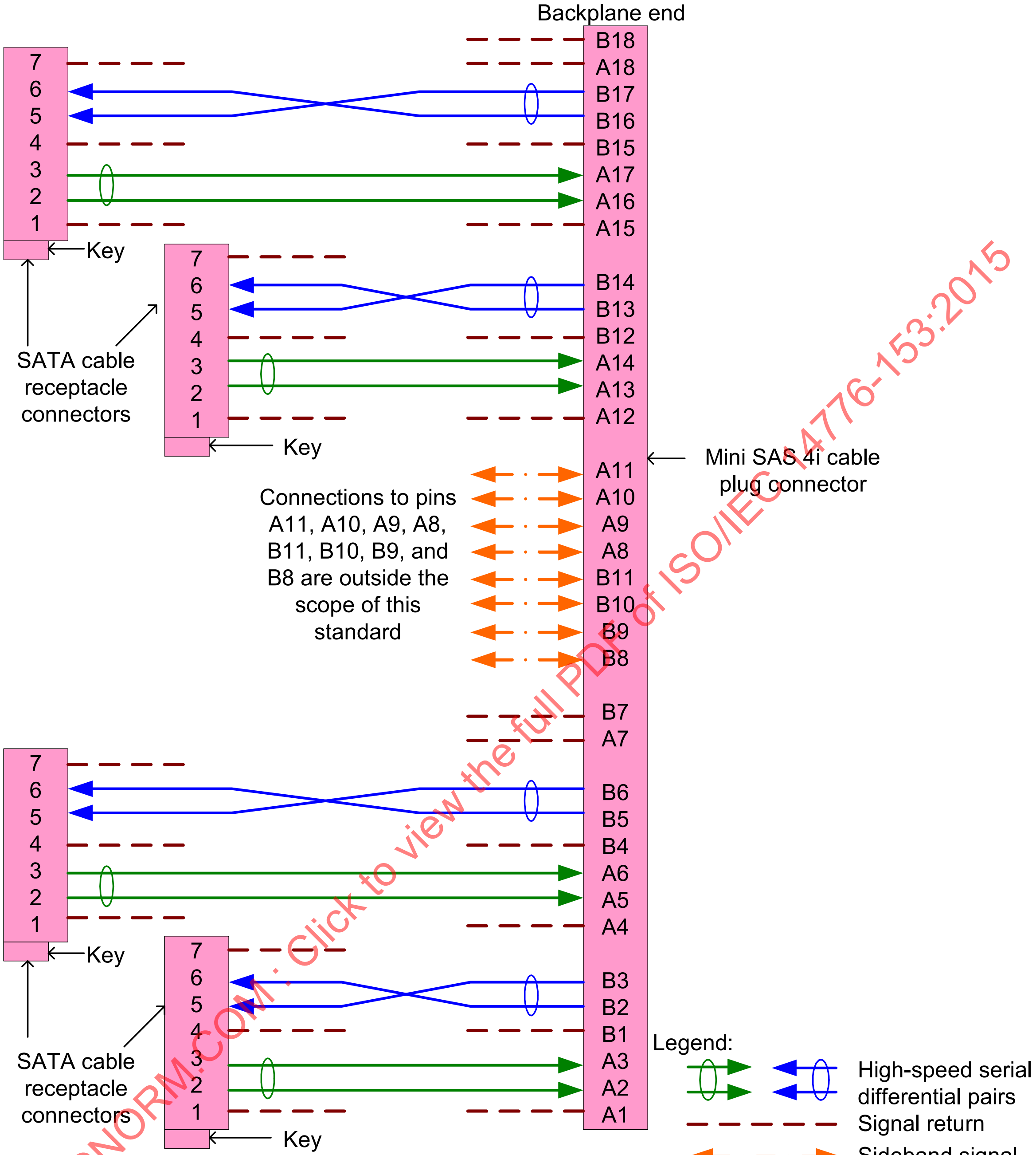


Figure 75 — SAS internal backplane-based fanout cable assembly - Mini SAS 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

Figure 76 shows the SAS internal backplane-based fanout cable assembly with the Mini SAS HD 4i cable receptacle connector.

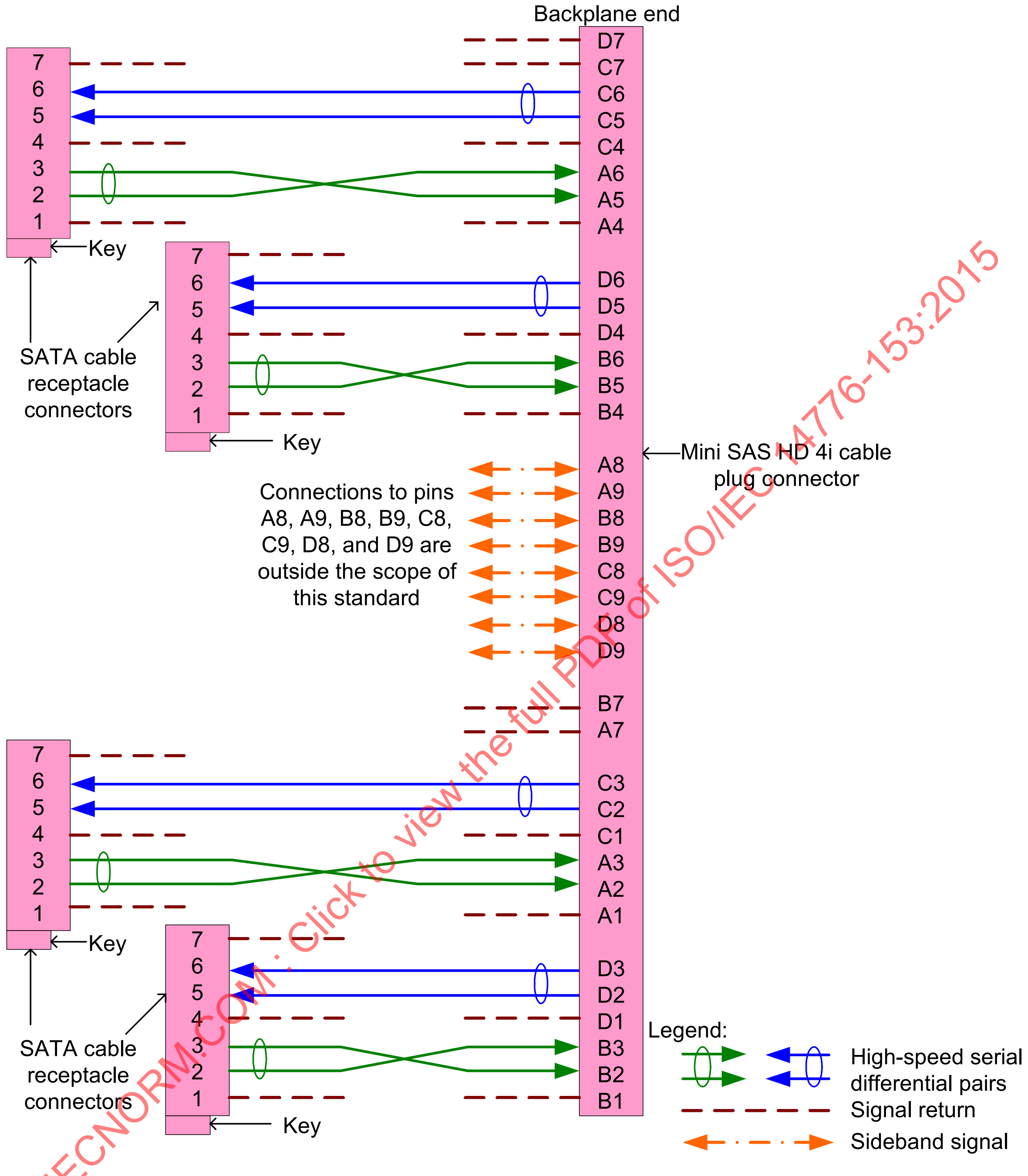


Figure 76 — SAS internal backplane-based fanout cable assembly - Mini SAS HD 4i

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.2 SAS external cable assemblies

5.4.4.2.1 SAS external cable assemblies overview

A SAS external cable assembly has:

a) a Mini SAS 4x cable plug connector (see 5.4.3.4.1.1) at each end (see 5.4.4.2.2);
b) a Mini SAS HD 4x cable plug connector (see 5.4.3.4.2.1) at each end (see 5.4.4.2.3);
c) a Mini SAS HD 8x cable plug connector (see 5.4.3.4.2.2) at each end (see 5.4.4.2.4);

d) a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end (see 5.4.4.2.5); or
e) a QSFP+ cable plug connector (see 5.4.3.4.3.1) at each end (see 5.4.4.2.6).

SAS external cable assemblies do not include power or the READY LED signal.

Although the connector always supports four or eight physical links, a SAS external cable assembly may support one to eight physical links. SAS external cable assemblies should be labeled to indicate how many physical links are included (i.e., 1X, 2X, 3X, 4X, 5X, 6X, 7X, or 8X on each connector's housing).

The Tx signals on one end shall be connected to the corresponding Rx signals of the other end (e.g., Tx 0+ of one connector shall be connected to Rx 0+ of the other connector).

Signal returns shall not be connected to CHASSIS GROUND in the cable assembly.

In addition to the SAS icon (see Annex G), additional icons are defined for external connectors to guide users into making compatible attachments (i.e., not attaching expander device table routing phys to expander device table routing phys in externally configurable expander devices (see SPL), which is not allowed (see SPL)). Connectors that have one or more matching icons are intended to be attached together. Connectors that do not have a matching icon should not be attached together.

One end of the SAS external cable assembly shall support being attached to an end device, an enclosure out port, or an enclosure universal port. The other end of the SAS external cable assembly shall support being attached to an end device, an enclosure in port, or an enclosure universal port. If a Mini SAS 4x cable plug connector is used, then it shall include icons and key slots as defined in 5.4.3.4.1.1.

5.4.4.2.2 SAS external cable assembly - Mini SAS 4x

Figure 77 shows the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end.

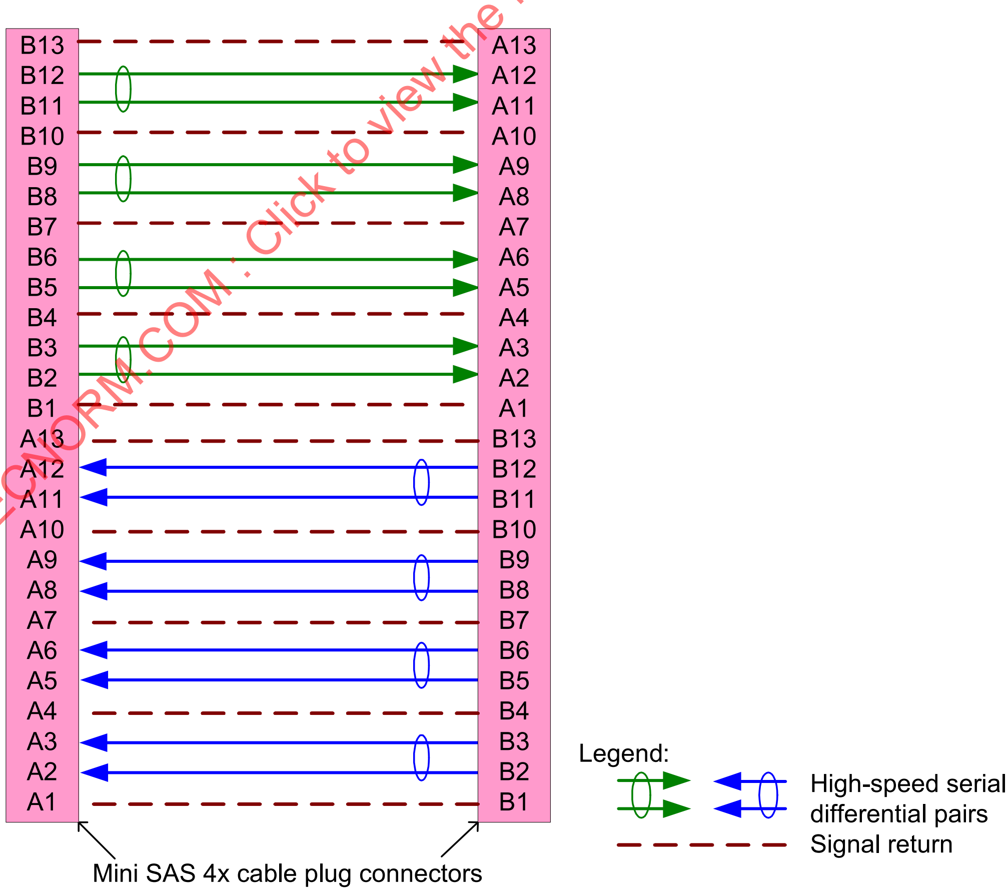


Figure 77 — Mini SAS 4x external cable assembly

In addition to the signal return connections shown in figure 77, one or more of the signal returns may be connected together in this cable assembly.

Figure 78 shows the SAS external cable assembly with Mini SAS 4x active cable assembly plug connectors at each end.

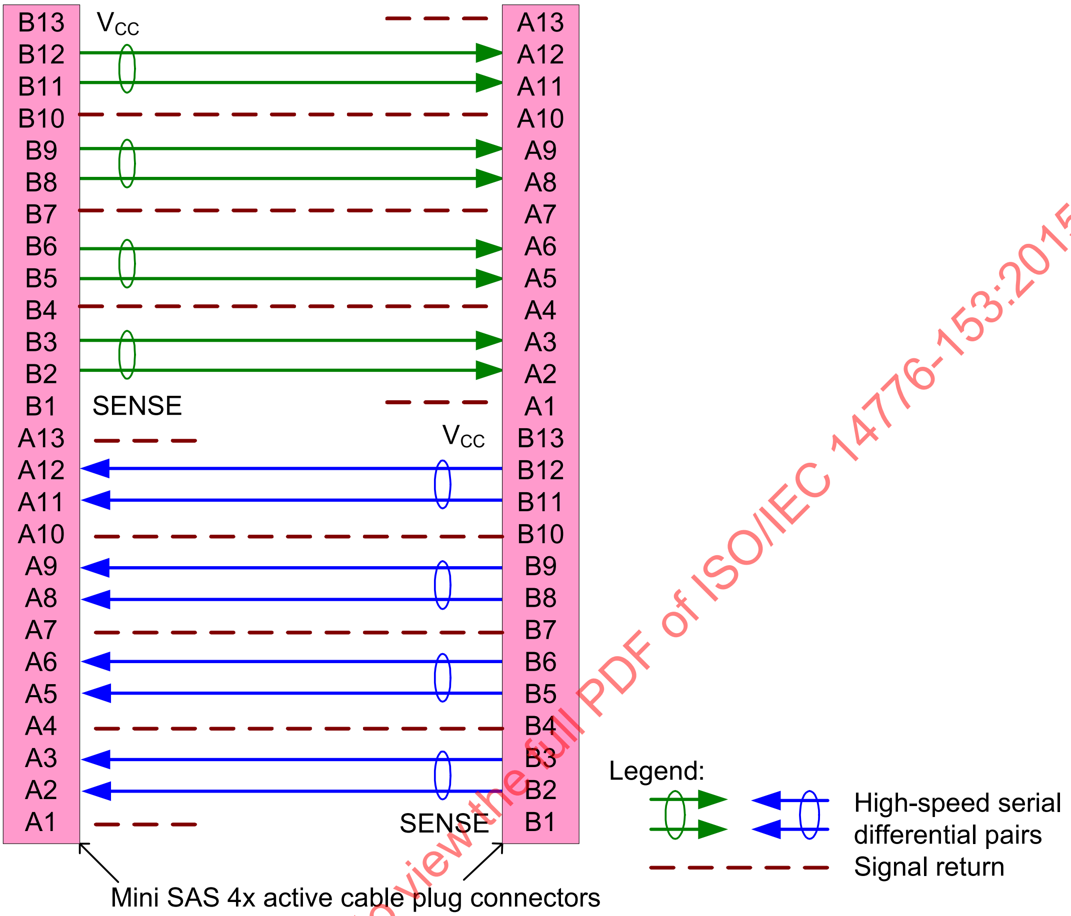


Figure 78 — Mini SAS 4x active external cable assembly

In addition to the signal return connections shown in figure 78, one or more of the signal returns may be connected together in this cable assembly.

Figure 79 shows an example cable with icons and key slots in the SAS external cable assembly with Mini SAS 4x cable plug connectors at each end. Depending on the cable configuration, the Mini SAS 4x cable connectors may also include different icon, key slot, and key combinations than shown in figure 79 (see 5.4.3.4.1.1).

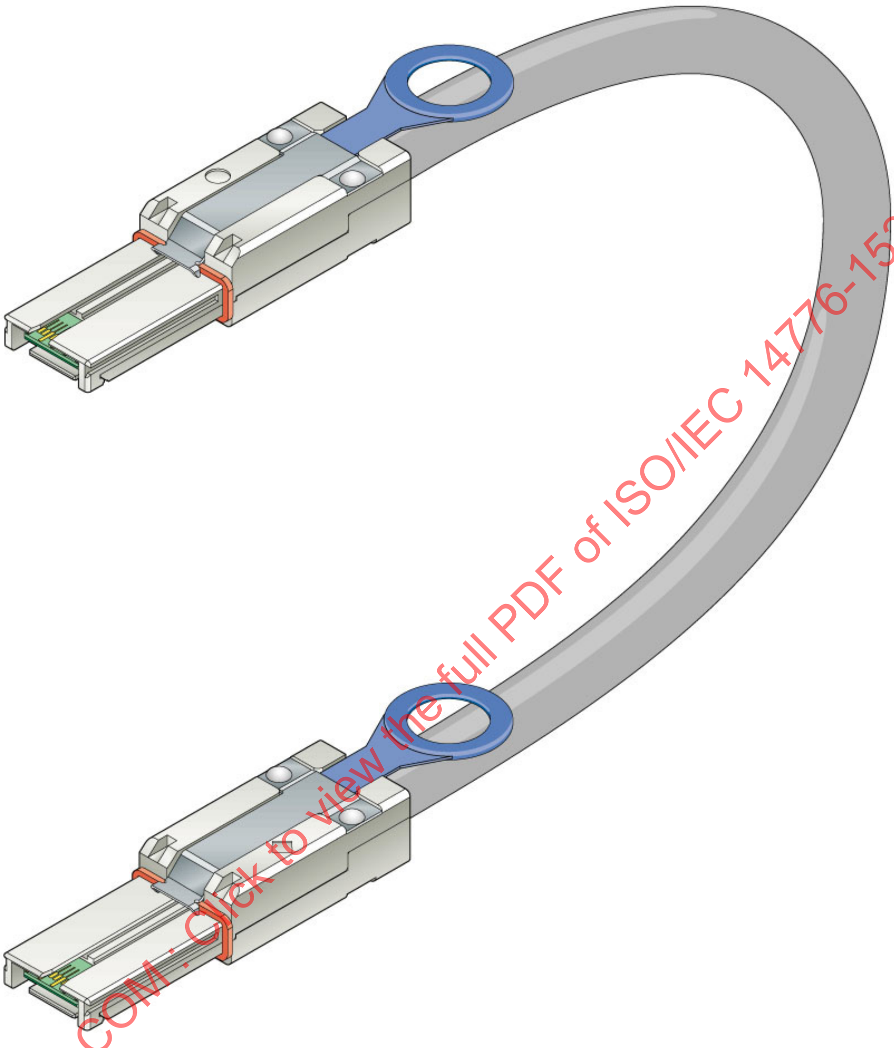


Figure 79 — SAS external cable assembly with Mini SAS 4x cable plug connectors

Although the topology is supported by this standard and SPL, a SAS external cable assembly with Mini SAS 4x connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL.

5.4.4.2.3 SAS external cable assembly - Mini SAS HD 4x

Figure 80 shows the SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

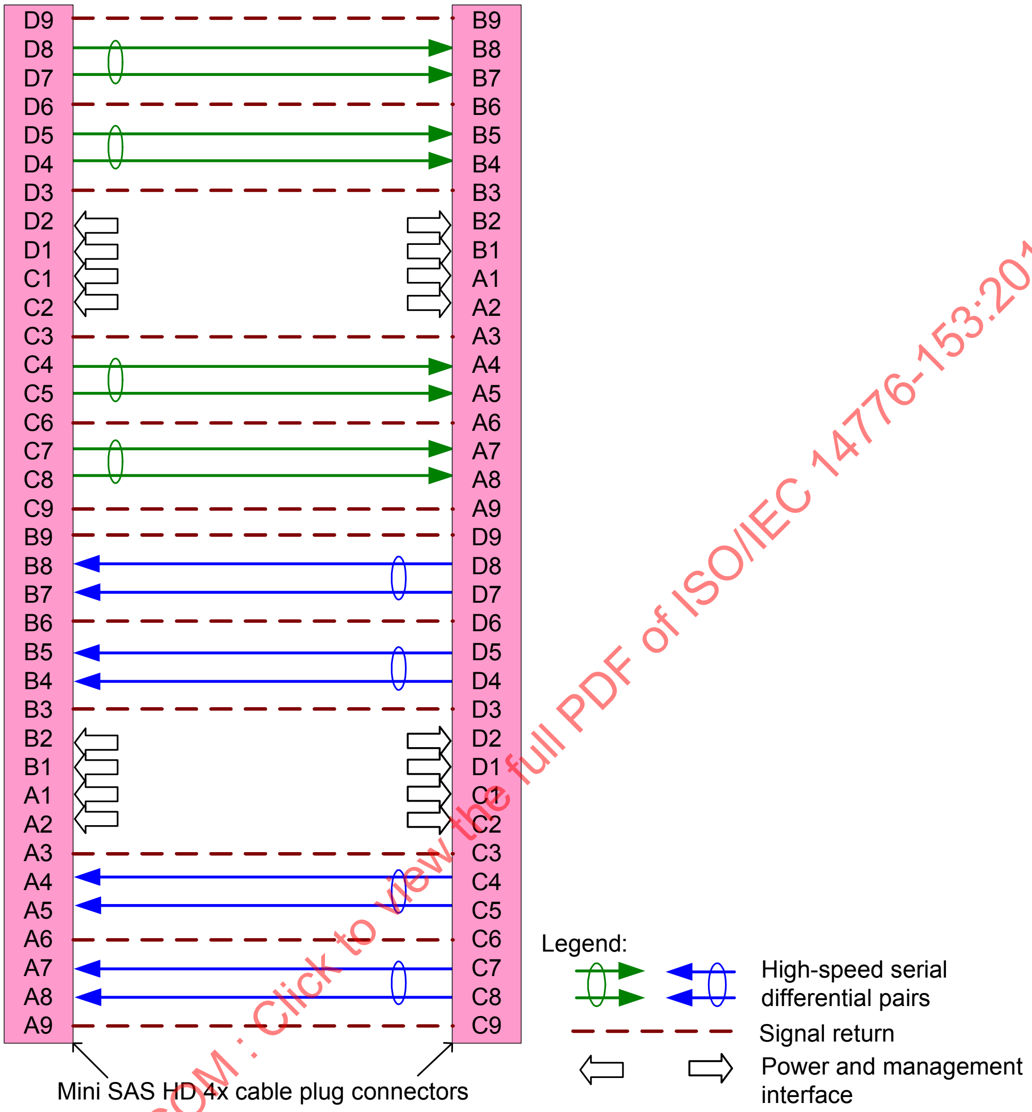


Figure 80 — SAS external cable assembly - Mini SAS HD 4x

In addition to the signal return connections shown in figure 80, one or more of the signal returns may be connected together in this cable assembly.

Figure 81 shows the SAS external cable assembly with Mini SAS HD 4x cable plug connectors at each end.

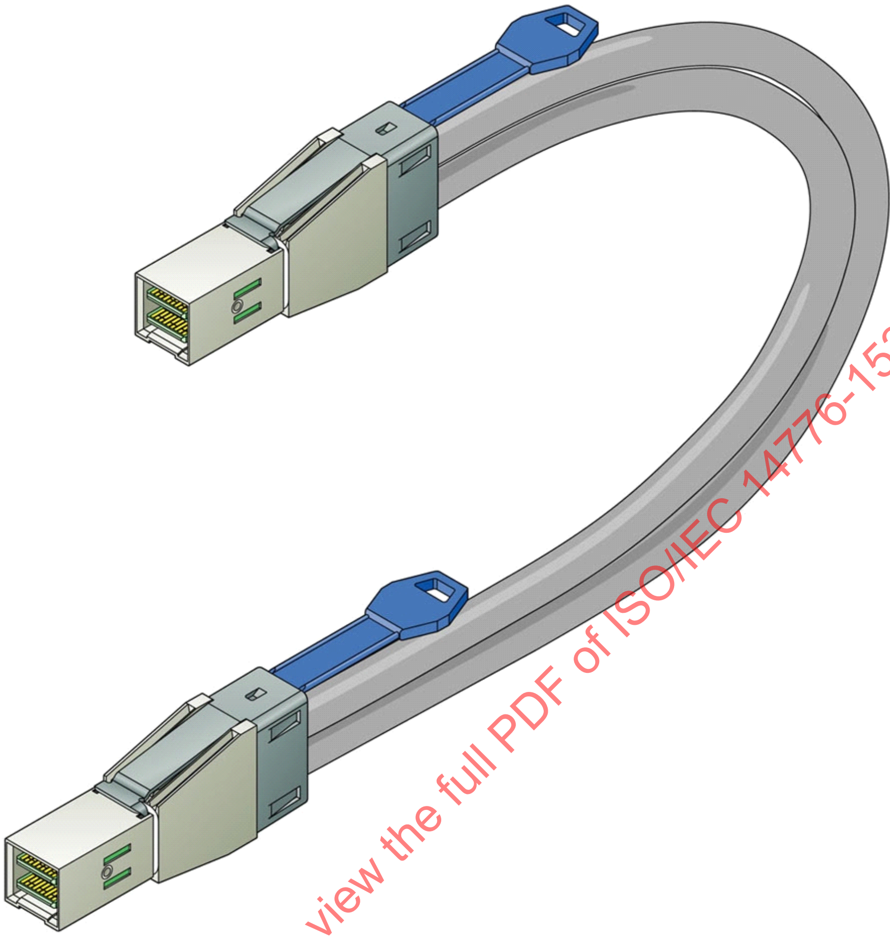


Figure 81 — SAS external cable assembly with Mini SAS HD 4x cable plug connectors

Although the topology is supported by this standard and SPL, a SAS external cable assembly with Mini SAS HD 4x connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL.

5.4.4.2.4 SAS external cable assembly - Mini SAS HD 8x

Figure 82 shows the SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

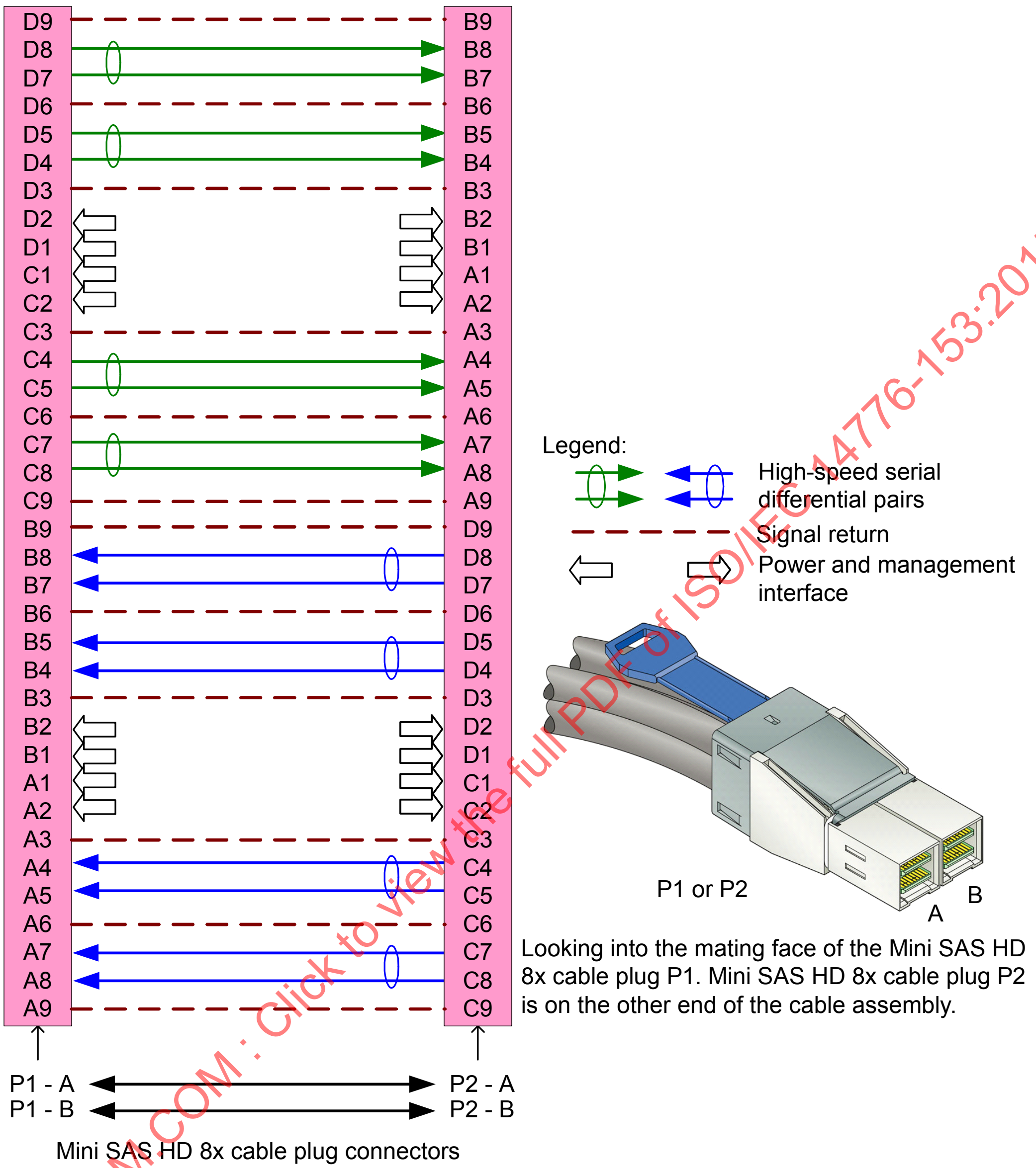


Figure 82 — SAS external cable assembly - Mini SAS HD 8x

In addition to the signal return connections shown in figure 82, one or more of the signal returns may be connected together in this cable assembly.

This cable assembly may support one to eight physical links. If less than eight physical links are supported, then module A shall be populated first, followed by module B (e.g., if six physical links are supported, then module A has four physical links connected and module B has two physical inks connected). See 5.4.3.4.2.6 for connector module pin assingments.

Figure 83 shows the SAS external cable assembly with Mini SAS HD 8x cable plug connectors at each end.

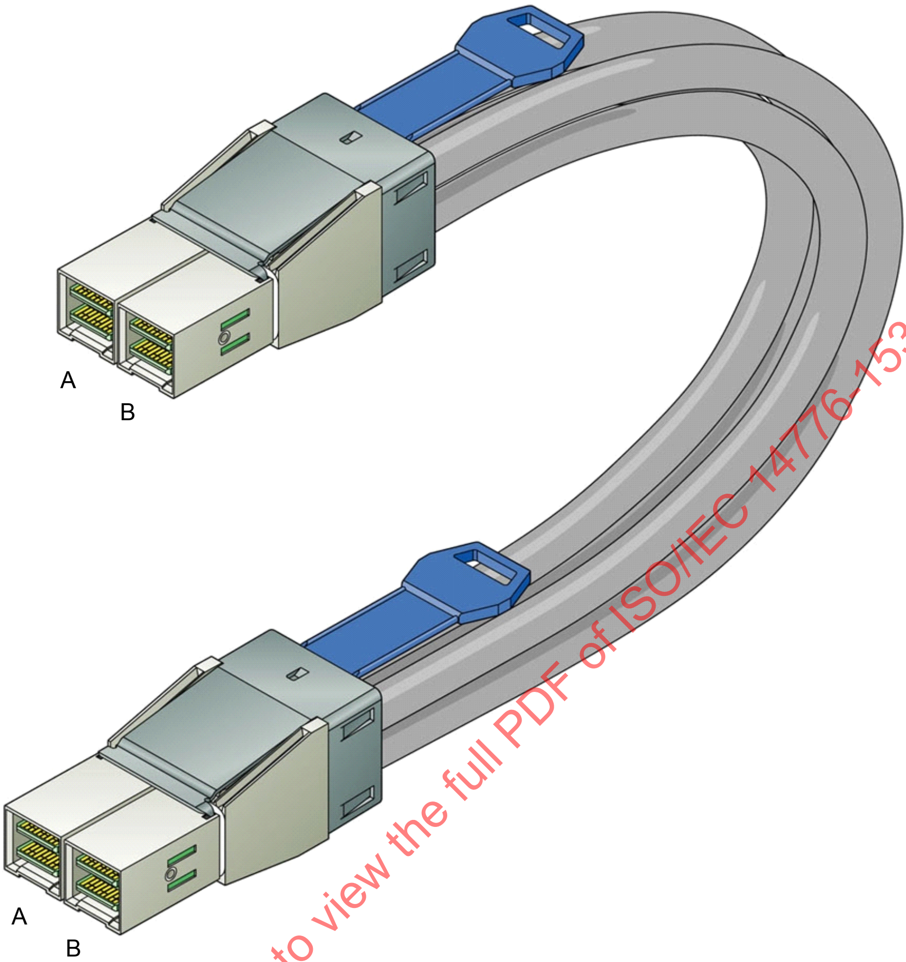


Figure 83 — SAS external cable assembly with Mini SAS HD 8x cable plug connectors

Although the topology is supported by this standard and SPL, a SAS external cable assembly with Mini SAS HD 8x connectors on each end that attaches an enclosure in port to another enclosure in port is not defined by this standard and SPL.

5.4.4.2.5 SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Figure 84 shows the SAS external cable assembly with a Mini SAS HD 4x cable plug connector at one end and a Mini SAS 4x cable plug connector at the other end.

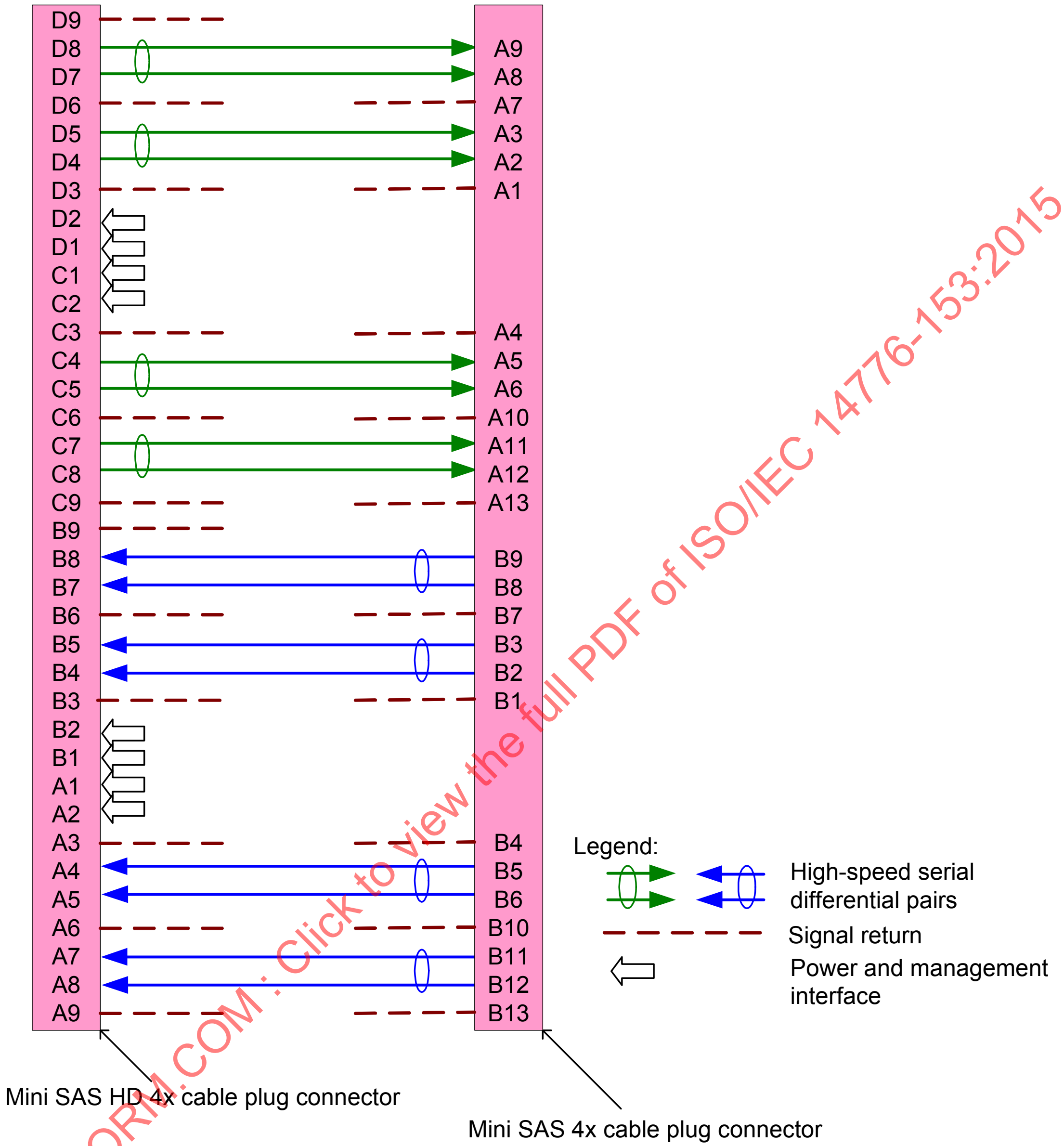


Figure 84 — SAS external cable assembly - Mini SAS HD 4x to Mini SAS 4x

Each signal return on one end of this cable assembly shall be connected to at least one signal return on the other end of the cable assembly. One or more of the signal returns may be connected together in this cable assembly.

5.4.4.2.6 SAS external cable assembly - QSFP+

QSFP+ cable assemblies are defined in SFF-8436. QSFP+ cable assemblies for SAS shall comply with the TxRx connection characteristics specified in this standard (see 5.5).

5.4.5 Backplanes

SAS backplane designs should follow the recommendations in SFF-8460.

5.5 TxRx connection characteristics

5.5.1 TxRx connection characteristics overview

Each TxRx connection shall support a bit error ratio (BER) that is less than 10^{-12} (i.e., fewer than one bit error per 10^{12} bits). The parameters specified in this standard support meeting this requirement under all conditions including the minimum input and output amplitude levels.

A TxRx connection may be constructed from multiple TxRx connection segments (e.g., backplanes and cable assemblies). It is the responsibility of the implementer to ensure that the TxRx connection is constructed from individual TxRx connection segments such that the overall TxRx connection requirements are met. Loss characteristics for individual TxRx connection segments are beyond the scope of this standard.

Each TxRx connection segment shall comply with the impedance requirements detailed in 5.5.2 for the conductive material from which they are formed. A passive equalizer network, if present, shall be considered part of the TxRx connection.

TxRx connections shall be applied only to homogeneous ground applications (e.g., between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane).

5.5.2 TxRx connection general characteristics

Table 21 defines the TxRx connection general characteristics.

Table 21 — TxRx connection general characteristics

Characteristic [a] [b]	Units	Value
Differential impedance (nominal)	Ω	100
Bulk cable or backplane:		
Differential characteristic impedance [d] [e]	Ω	100
Mated connectors:		
Differential characteristic impedance [f]	Ω	100
Passive cable assembly and backplane:		
Maximum propagation delay [c]	ns	53
Minimum $\|S_{DD21}\|$ for internal cable assemblies [g] [h]	dB	-6
Minimum $\|S_{DD21}\|$ for external cable assemblies and backplanes	See 5.5	
Mini SAS 4x active cable assembly:		
Maximum propagation delay [i]	ns	133
Differential characteristic impedance [f]	Ω	100
Managed cable assembly:		
Maximum propagation delay [j]	ns	510
Differential characteristic impedance [f]	Ω	100

[a] All measurements are made through mated connector pairs.

[b] The equivalent maximum TDR rise time from 20 % to 80 % shall be 70 ps. Filtering may be used to obtain the equivalent rise time. The filter consists of the two-way launch/return path of the test fixture, the two-way launch/return path of the test cable, and the software or hardware filtering of the TDR scope. The equivalent rise time is the rise time of the TDR scope output after application of all filter components. When configuring software or hardware filters of the TDR scope to obtain the equivalent rise time, filtering effects of test cables and test fixtures shall be included.

[c] This is based on propagation delay for a 10 m Mini SAS 4x passive cable assembly. See SPL for STP flow control details.

[d] The impedance measurement identifies the impedance mismatches present in the bulk cable or backplane when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the bulk cable or backplane, when present, but includes any intermediate connectors or splices.

[e] Where the bulk cable or backplane has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[f] The characteristic impedance is a measurement reference impedance for the test environment.

[g] An internal cable assembly may be a TxRx connection segment or a full TxRx connection. The full TxRx connection is required to comply with the requirements for intra-enclosure compliance points defined in 5.7.

[h] The range for this frequency domain measurement is 10 MHz to 4 500 MHz.

[i] This is based on propagation delay for a 25 m Mini SAS 4x active cable assembly. TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL for STP flow control details.

[j] This is based on propagation delay for a 100 m optical cable. Managed cables shall report the propagation delay through the cable management interface (see 5.4.3.4.2.7). TxRx connections with propagation delay > 53 ns may not support STP unless the necessary STP flow control buffer size is implemented. See SPL for STP flow control details.

5.5.3 Passive TxRx connection S-parameter limits

S-parameters limits are calculated per the following formula:

Measured value < max [L, min [H, $N + 13.3 \times \log_{10}(f / 3\ \text{GHz})$]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 22 defines the maximum limits for S-parameter of the passive TxRx connection.

Table 22 — Maximum limits for S-parameters of the passive TxRx connection

Characteristic [a] [b] [c] [d]	***L*** [e] **(dB)**	***N*** [e] **(dB)**	***H*** [e] **(dB)**	***S*** [e] **(dB / decade)**	f_{min} [e] **(MHz)**	f_{max} [e] **(GHz)**
[$20 \times \log_{10}(\lvert S_{CD21}\rvert)$] - [$20 \times \log_{10}(\lvert S_{DD21}\rvert)$]		-10		0	100	6.0
Maximum near-end crosstalk (NEXT) for each receive signal pair [f] [g]		-26		0	100	6.0
$20 \times \log_{10}(\lvert S_{DD22}\rvert)$	-10	-7.9	0	13.3	100	6.0
$20 \times \log_{10}(\lvert S_{CD22}\rvert)$	-26	-12.7	-10	13.3	100	6.0
$20 \times \log_{10}(\lvert S_{CD21}\rvert)$		-18		0	100	6.0

[a] All measurements are made through mated connector pairs.
[b] The range for this frequency domain measurement is 100 MHz to 6 000 MHz.
[c] Specifications apply to any combination of cable assemblies and backplanes that are used to form a passive TxRx connection.
[d] $\lvert S_{CC22}\rvert$ and $\lvert S_{DC22}\rvert$ are not specified.
[e] See figure 4 in 5.2 for definitions of *L*, *N*, *H*, *S*, f_{min}, and f_{max}.
[f] NEXT is not an S-parameter.
[g] Determine all valid aggressor/victim near-end crosstalk transfer modes. Over the complete frequency range of this measurement, determine the sum of the crosstalk transfer ratios, measured in the frequency domain, of all crosstalk transfer modes. To remove unwanted bias due to test fixture noise, crosstalk sources with magnitudes less than -50 dB (e.g., -60 dB) at all frequencies may be ignored. The following equation details the summation process of the valid near-end crosstalk sources:

$$\text{TotalNEXT}(f) = 10 \times \log \sum_{1}^{n} 10^{\langle \text{NEXT}(f)/10 \rangle}$$

where:

f frequency; and
n number of the near-end crosstalk source.

All NEXT values expressed in dB format in a passive transfer network shall have negative dB magnitude.

Figure 85 shows the passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits defined in table 22.

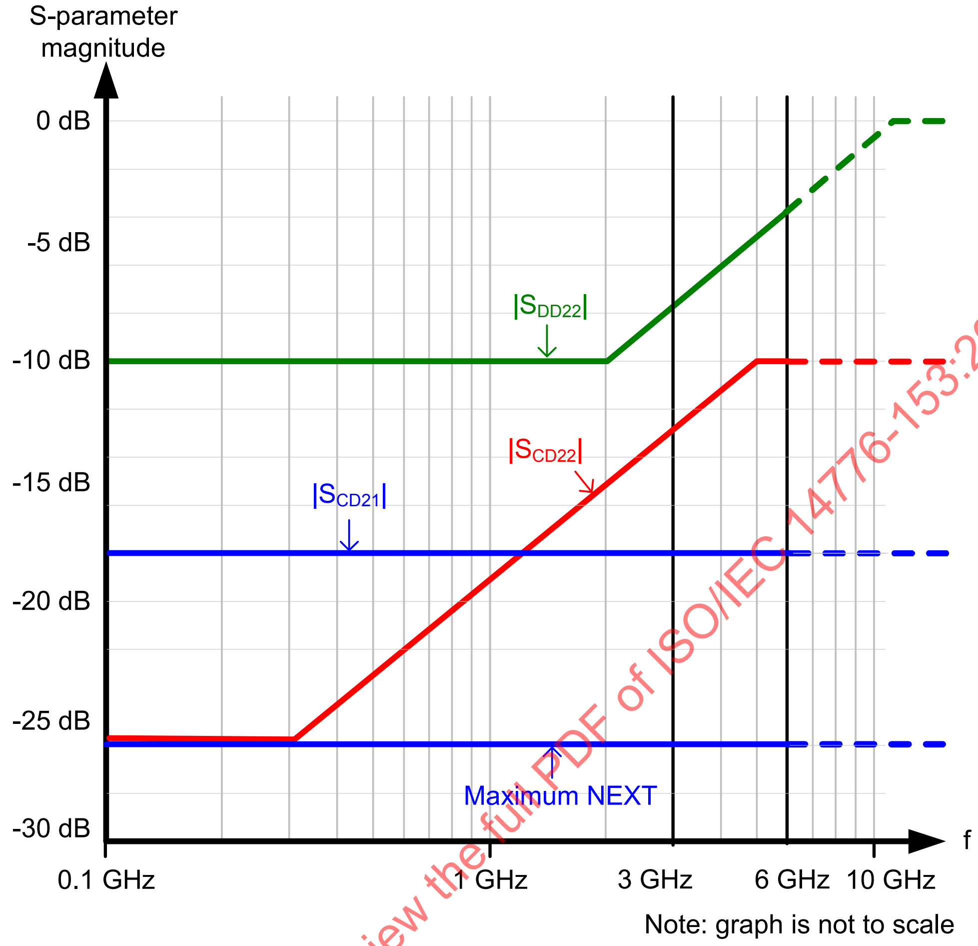


Figure 85 — Passive TxRx connection $|S_{DD22}|$, $|S_{CD22}|$, $|S_{CD21}|$, and NEXT limits

5.5.4 Passive TxRx connection characteristics for untrained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

For untrained 1.5 Gbit/s and 3 Gbit/s, each external passive TxRx connection shall be designed such that its loss characteristics are less than the loss of the TCTF test load plus ISI at CT at 3 Gbit/s (see figure 93 in 5.6.3) over the frequency range of 50 MHz to 3 000 MHz.

For untrained 1.5 Gbit/s and 3 Gbit/s, each internal passive TxRx connection shall be designed such that its loss characteristics are less than:

a) the loss of the TCTF test load plus ISI at IT at 3 Gbit/s (see figure 92 in 5.6.3) over the frequency range of 50 MHz to 3 000 MHz; or
b) if the system supports SATA devices using Gen2i levels (see SATA) but the receiver device does not support SATA Gen2i levels through the TCTF test load (see table 40 in 5.7.5.4), the loss of the low-loss TCTF test load plus ISI (see figure 97 in 5.6.4) over the frequency range of 50 MHz to 3 000 MHz.

For untrained 1.5 Gbit/s and 3 Gbit/s, each passive TxRx connection shall meet the delivered signal specifications in table 40 (see 5.7.5.4).

For untrained 6 Gbit/s (i.e., SATA devices using Gen3i levels (see SATA)), then the internal passive TxRx connection should be less than the CIC (see SATA). See SATA for delivered signal specifications.

For external cable assemblies, these electrical requirements are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 6 m long, provided that no other TxRx connection segments are included in the TxRx connection.

5.5.5 Passive TxRx connection characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the passive TxRx connection shall support a bit error ratio (BER) that is less than 10^{-15} (i.e., fewer than one bit error per 10^{15} bits) based on simulation results using:

a) S-parameter measurements of the passive TxRx connection;
b) the reference transmitter device (see 5.7.4.6.5); and
c) the reference receiver device (see 5.7.5.7.3).

The simulation shall not include sources of crosstalk. Since simulations do not include all aspects of noise that may degrade the received signal quality, a BER that is less than 10^{-15} is expected to yield an actual BER that is less than 10^{-12}.

The S-parameter measurements shall:

a) have a maximum step size of 10 MHz;
b) have a maximum frequency of at least 20 GHz;
c) be passive (i.e., the output power is less than or equal to the input power); and
d) be causal (i.e., the output depends only on past inputs).

Figure 86 shows an example circuit for simulation. The specific simulation program used is not specified by this standard. Annex C includes the StatEye program from http://www.stateye.org, which is one such simulation program.

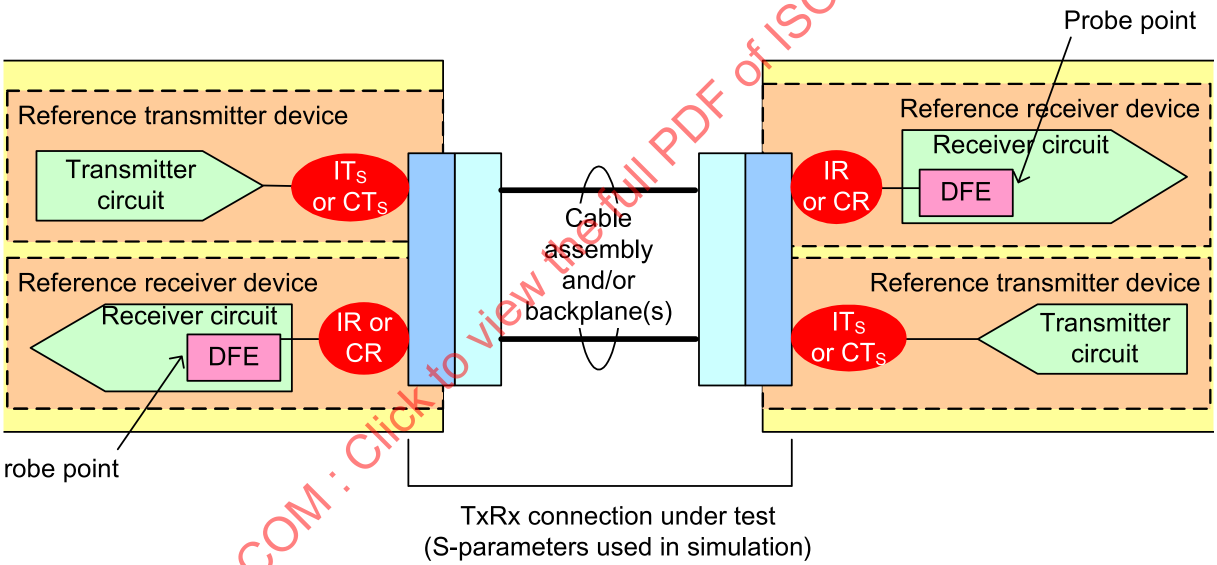


Figure 86 — Example passive TxRx connection compliance testing for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Table 23 defines the required passive TxRx connection characteristics.

Table 23 — Passive TxRx connection characteristics for trained 6 Gbit/s

Characteristic	Units	6 Gbit/s
Minimum voltage [a]	mV(P-P)	84
Maximum TJ [a]	UI	0.64
[a] As reported by simulation of the passive TxRx connection S-parameters with the reference transmitter device and the reference receiver device. Values are reported at a BER of 10^{-15} inside the reference receiver device after equalization at 6 Gbit/s. This standard does not define values for trained 3 Gbit/s and 1.5 Gbit/s. Passive TxRx connections that comply with the 6 Gbit/s characteristics are expected to operate correctly at slower physical link rates.		

For external cable assemblies, these electrical requirements are consistent with using good quality passive Mini SAS 4x cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 10 m long, provided that no other TxRx connection segments are included in the TxRx connection.

A passive TxRx connection supporting trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s may not support untrained 1.5 Gbit/s and 3 Gbit/s and may not support SATA. Trained transceiver devices incorporate features to allow them to operate over the following passive TxRx connections:

a) passive TxRx connections with higher loss than TxRx connections compliant with versions of SAS standards previous to SAS-2;
b) passive TxRx connections defined in this standard for untrained 1.5 Gbit/s and 3 Gbit/s (see 5.5.4); and
c) passive TxRx connections supporting SATA.

5.5.6 TxRx connection characteristics for active cable assemblies

5.5.6.1 Active cable assembly electrical characteristics overview

Active cable assemblies shall support a bit error ratio (BER) that is less than 10^{-12} when used with trained transmitter devices and trained receiver devices defined in 5.7.

In addition to complying with electrical characteristics necessary for the required BER performance, active cable assemblies shall comply with the OOB signaling defined in 5.9. The circuitry incorporated in these cable assemblies preserves D.C. idle with response times that support the OOB signal receiver device idle time detection requirements in table 60 (see 5.9.3).

5.5.6.2 Active cable assembly output electrical characteristics for trained 6 Gbit/s

Table 24 defines active cable assembly output electrical characteristics for trained 6 Gbit/s.

Table 24 — Active cable assembly output electrical characteristics for trained 6 Gbit/s

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage	mV (P-P)	400		1 200
RJ [a b d]	UI			0.22
TJ [a c d]	UI			0.56

[a] Based on TX input per table 32 (see 5.7.4.6.1) and recommended TX interoperability settings per table 35 (see 5.7.4.6.4).

[b] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}.

[c] The TJ measurement shall be performed with at least 58 dwords (i.e., 2 320 bits on the physical link) of the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) with SSC enabled.

[d] The measurement shall include the effects of the JTF (see 5.7.3.2).

For active cable assemblies, these characteristics are consistent with good quality half-active (i.e., with circuitry only on the receive end of the assembly) cable assemblies constructed with shielded twinaxial cable with 24 AWG solid wire up to 25 m long, provided that no other TxRx connection segments are included in the TxRx connection.

Active cable assembly output electrical characteristics are not defined for untrained 1.5 Gbit/s and 3 Gbit/s. Active cables that comply with trained 6 Gbit/s characteristics should operate within the specified error rate at slower physical link rates.

5.5.6.3 Active cable assembly S-parameter limits

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, $N + 13.3 \times \log_{10}(f / 3\ \text{GHz})$]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 25 defines the maximum limits for S-parameters of the active cable assembly.

Table 25 — Maximum limits for S-parameters for active cable assemblies

Characteristic [b] [d]	L [c] (dB)	N [c] (dB)	H [c] (dB)	S [c] (dB / decade)	f_{min} [c] (MHz)	f_{max} [c] (GHz)
$\|S_{CC22}\|$ [a]	-6.0	-5.0	0	13.3	100	6.0
$\|S_{DD11}\|$, $\|S_{DD22}\|$ [a]	-10	-7.9	0	13.3	100	6.0
$\|S_{CD11}\|$, $\|S_{CD22}\|$ [a]	-20	-12.7	-10	13.3	100	6.0

[a] For $|S_{CC22}|$, $|S_{DD22}|$ and $|S_{CD22}|$ measurements, the transmitter device attached to the active cable assembly under test shall transmit a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See D.10.4.4 and D.10.4.5

[b] $|S_{CC11}|$, $|S_{DC11}|$ and $|S_{DC22}|$ are not specified.

[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

[d] Power shall be applied to the active cable assembly during these measurements.

Figure 87 shows the active cable assembly $|S_{CC22}|$, $|S_{DD11}|$, $|S_{DD22}|$, $|S_{CD11}|$ and $|S_{CD22}|$ limits defined in table 25.

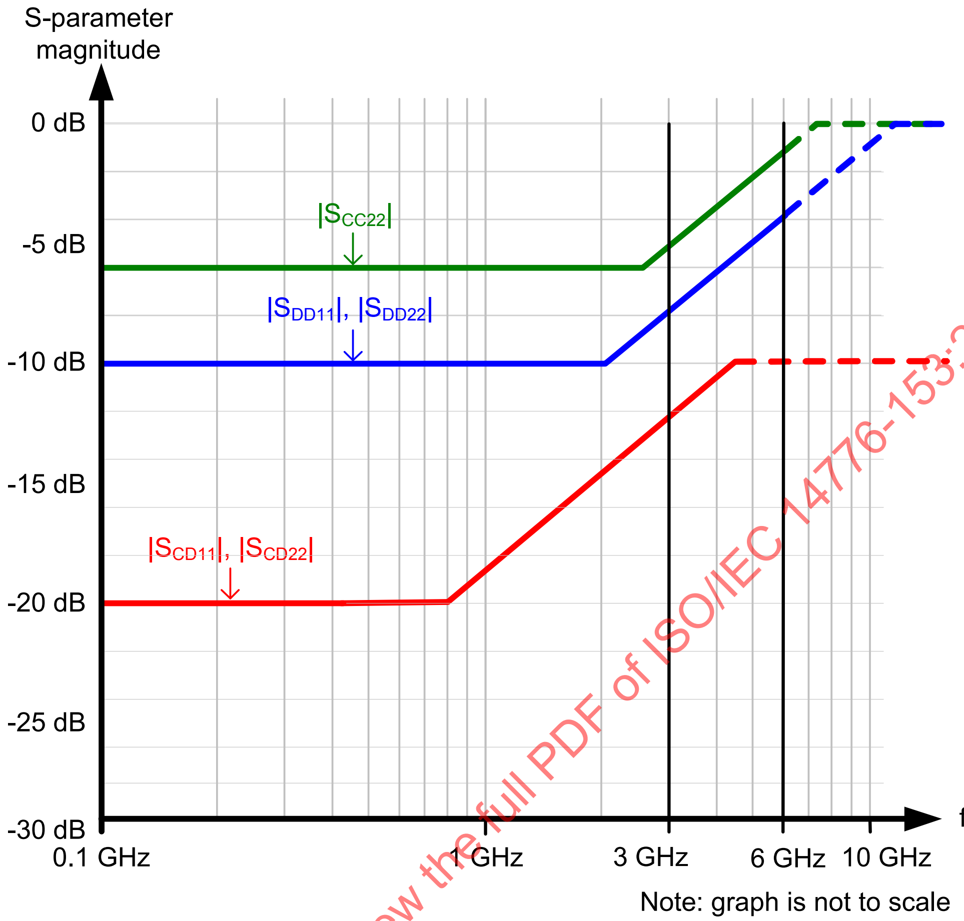


Figure 87 — Active cable S-parameter limits

5.6 Test loads

5.6.1 Test loads overview

This standard uses a test load methodology to specify transmitter device signal output characteristics (see 5.7.4.4 and 5.7.4.5) and delivered signal characteristics (see 5.7.5.4). This methodology specifies the signal as measured at specified probe points in specified test loads.

For untrained 1.5 Gbit/s and 3 Gbit/s (e.g., the physical link rate is negotiated in Final-SNW (see SPL) or the physical link is SATA), the test loads used by the methodology are:

a) zero-length test load (see 5.6.2): used for testing transmitter device compliance points and receiver device compliance points;
b) transmitter compliance transfer function (TCTF) test load (see 5.6.3): used for testing transmitter device compliance points;
c) low-loss TCTF test load (see 5.6.4): used for testing transmitter device compliance points if SATA devices using Gen2i levels (see SATA) are supported and the SAS receiver device does not support the signal levels received through a full TCTF test load (see 5.6.3); and
d) CIC (see SATA): used for testing transmitter device compliance points if SATA devices using Gen3i levels (see SATA) are supported.

For trained (e.g., the physical link rate is negotiated in Train-SNW (see SPL)) 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the test loads used by the methodology are:

a) zero-length test load (see 5.6.2): used for:

A) testing transmitter device compliance points;
B) testing receiver device compliance points; and
C) used with a reference receiver device (see 5.7.5.7.3) in simulation to determine the delivered signal;

and

b) reference transmitter test load (see 5.6.5): used with a reference receiver device (see 5.7.5.7.3) in simulation to determine the delivered signal.

Physical positions denoted as probe points identify the position in the test load where the signal properties are measured, but do not imply that physical probing is used for the measurement. Physical probing may be disruptive to the signal and should not be used unless verified to be non-disruptive.

5.6.2 Zero-length test load

Figure 88 shows the zero-length test load as used for testing a transmitter device compliance point.

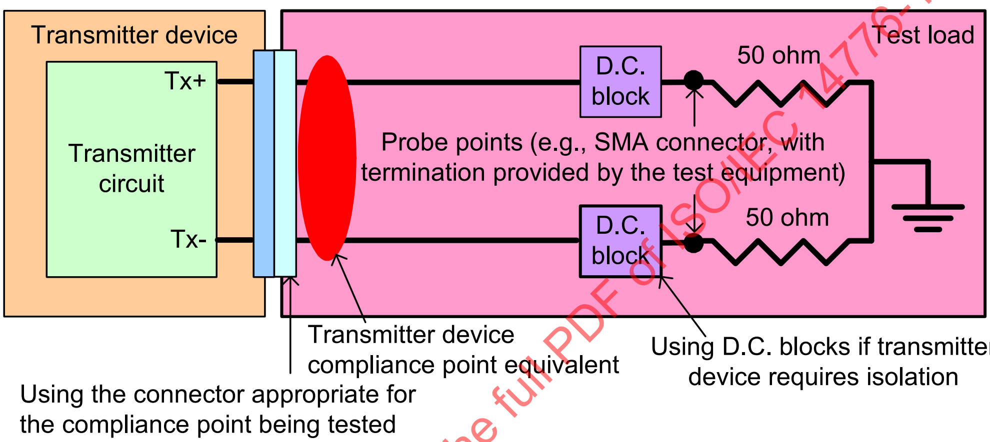


Figure 88 — Zero-length test load for transmitter device compliance point

Figure 89 shows the zero-length test load as used for testing a receiver device compliance point.

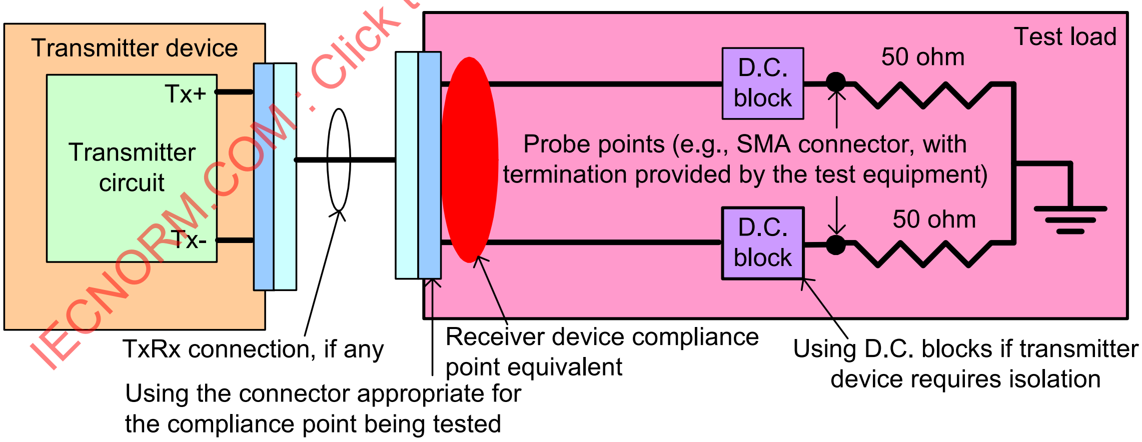


Figure 89 — Zero-length test load for receiver device compliance point

Figure 88 and figure 89 show ideal designs. Implementations may include:

a) insertion loss between the compliance and probe points; and
b) return loss due one or more impedance mismatches between the compliance point and 50 Ω termination points.

Not shown are non-ideal effects of the test equipment raw measurements (e.g., additional insertion loss and return loss). For de-embedding methods to remove non-ideal effects see Annex D.

Usage of fixturing and test equipment shall comply with the requirements defined in this subclause. The requirements in this subclause include the combined effects of the fixturing and test equipment.

The zero-length test load is defined by a set of S-parameters (see D.10). Only the magnitude of S_{DD21}(f) and the magnitude of S_{DD11}(f) are specified by this standard.

The zero-length test load, including all fixturing and instrumentation required for the measurement, shall comply with the following equations:

For 50 MHz < $f \leq$ 6.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.0 \times 10^{-6} \times f^{0.5}) + (2.8 \times 10^{-11} \times f) + (5.3 \times 10^{-21} \times f^2)) - 0.2 \text{ dB}$$

$$|S_{DD11}(f)| \leq -15 \text{ dB}$$

where:

$\lvert S_{DD21}(f)\rvert$	magnitude of $S_{DD21}(f)$;
$\lvert S_{DD11}(f)\rvert$	magnitude of $S_{DD11}(f)$; and
f	signal frequency in Hz.

Figure 90 shows the allowable $|S_{DD21}(f)|$ of a zero-length test load and the $|S_{DD21}(f)|$ of a sample zero-length test load.

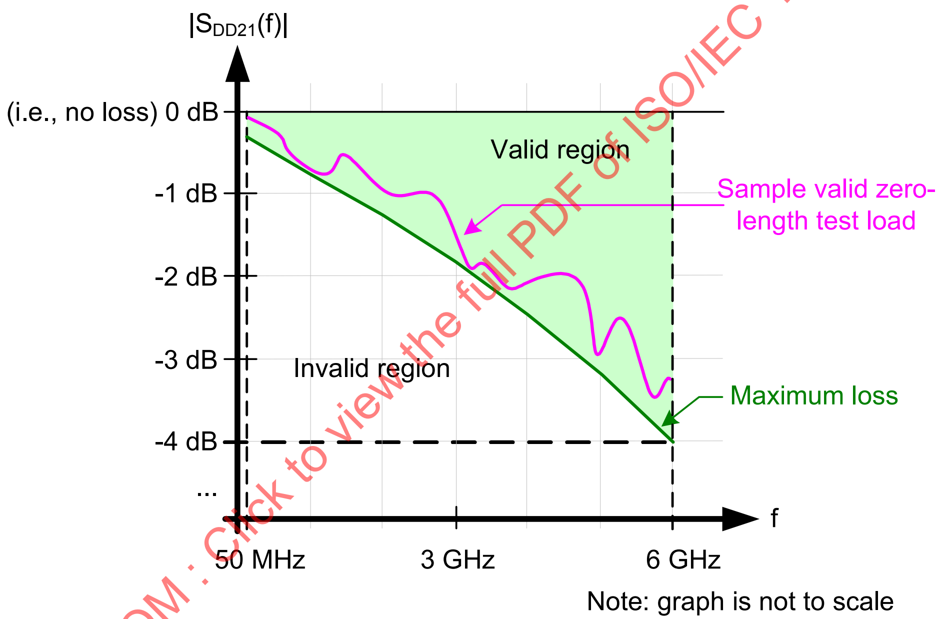


Figure 90 — Zero-length test load $|S_{DD21}(f)|$ requirements

5.6.3 TCTF test load

Figure 91 shows the TCTF test load. This test load is used for untrained 1.5 Gbit/s and 3 Gbit/s characterization.

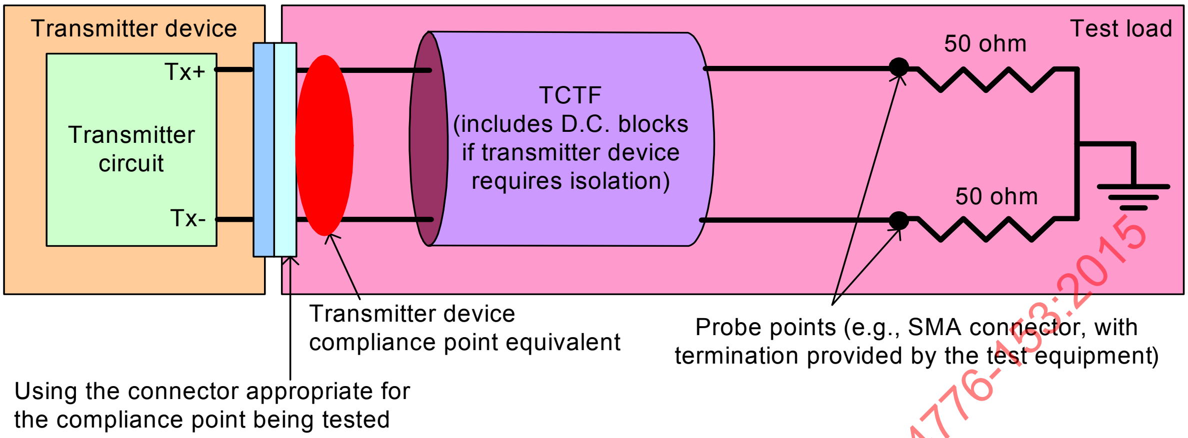


Figure 91 — TCTF test load

The TCTF test load shall meet the requirements in 5.5.2. The nominal impedance shall be the target impedance.

The TCTF test load is defined by a set of S-parameters (see D.10). Only the magnitude of $S_{DD21}(f)$ is specified by this standard.

For testing an untrained 3 Gbit/s transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \le -20 \times \log_{10}(e) \times ((6.5 \times 10^{-6} \times f^{0.5}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^2))\ \text{dB}$$

and for 3.0 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \le -10.9\ \text{dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 300\ \text{MHz})| - |S_{DD21}(f = 1\ 500\ \text{MHz})| > 3.9\ \text{dB}$$

where:

$\lvert S_{DD21}(f)\rvert$	magnitude of $S_{DD21}(f)$; and
f	signal frequency in Hz.

Figure 92 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 3 Gbit/s.

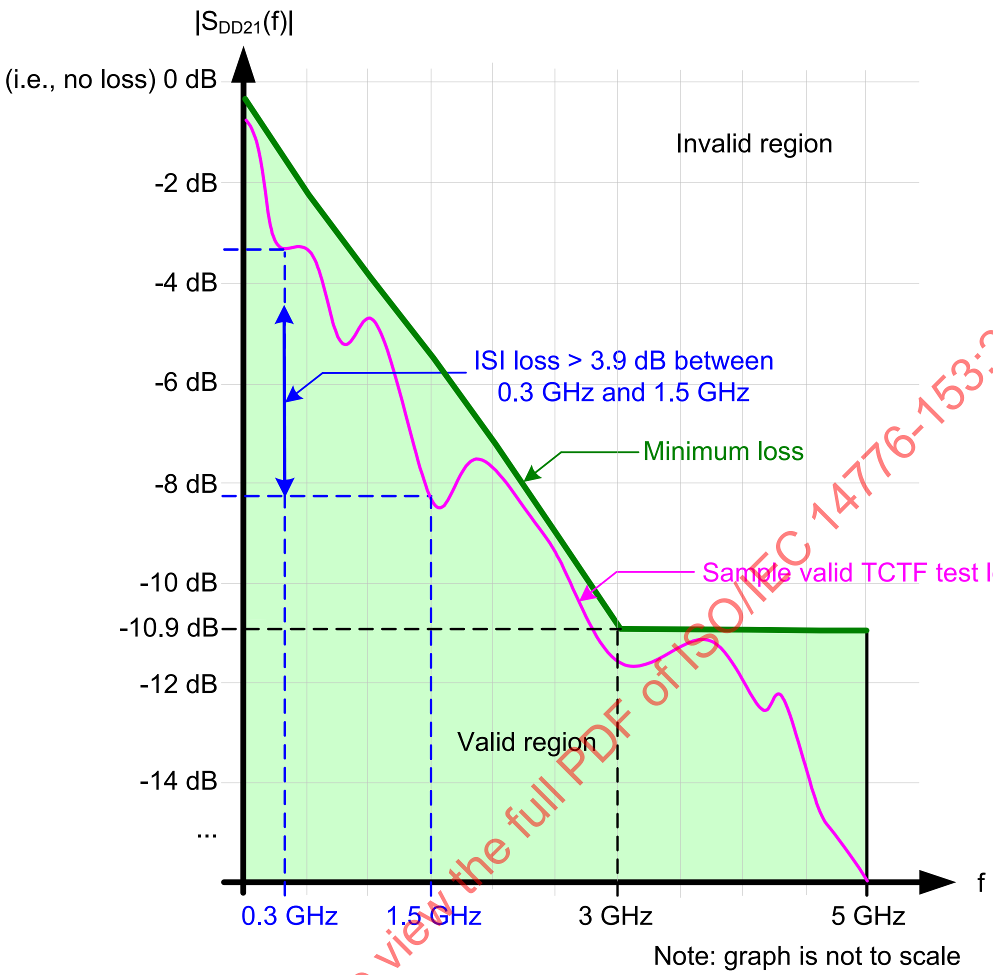


Figure 92 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 3 Gbit/s

For testing an untrained 3 Gbit/s transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < $f \le 3.0$ GHz:

$$|S_{DD21}(f)| \le -20 \times \log_{10}(e) \times ((1.7 \times 10^{-5} \times f^{0.5}) + (1.0 \times 10^{-10} \times f))\ \text{dB}$$

and for 3.0 GHz < $f \le 5.0$ GHz:

$$|S_{DD21}(f)| \le -10.7\ \text{dB}$$

and, specifying a minimum ISI loss:

$$|S_{DD21}(f = 300\ \text{MHz})| - |S_{DD21}(f = 1\ 500\ \text{MHz})| > 3.9\ \text{dB}$$

where:

$|S_{DD21}(f)|$	magnitude of $S_{DD21}(f)$; and
f	signal frequency in Hz.

Figure 93 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 3 Gbit/s.

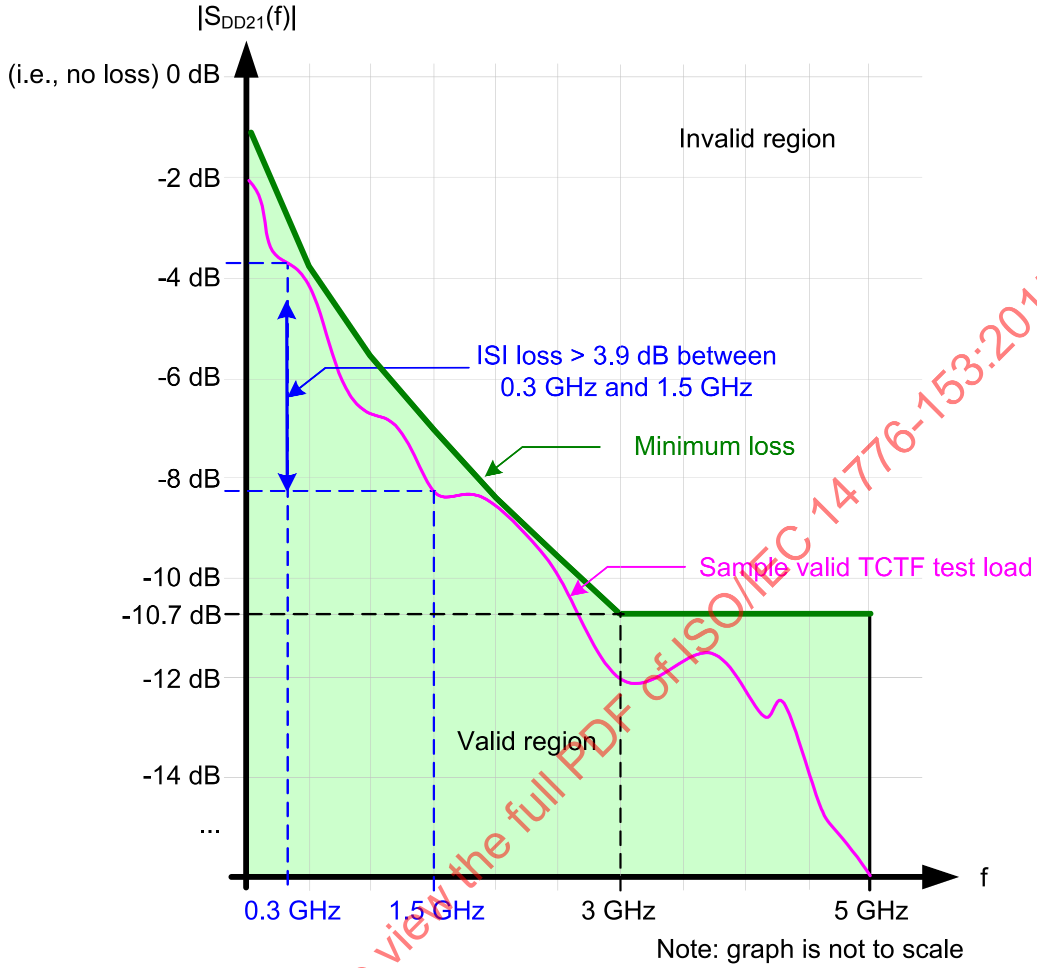


Figure 93 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 3 Gbit/s

For testing an untrained 1.5 Gbit/s transmitter device at IT, the TCTF test load shall comply with the following equations:

For 50 MHz < $f \leq$ 1.5 GHz:

$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((6.5 \times 10^{-6} \times f^{0.5}) + (2.0 \times 10^{-10} \times f) + (3.3 \times 10^{-20} \times f^{2}))$ dB

and for 1.5 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq -5.4$ dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 150\text{ MHz})| - |S_{DD21}(f = 750\text{ MHz})| > 2.0$ dB

where:

$\|S_{DD21}(f)\|$	magnitude of $S_{DD21}(f)$; and
f	signal frequency in Hz.

Figure 94 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at IT for untrained 1.5 Gbit/s.

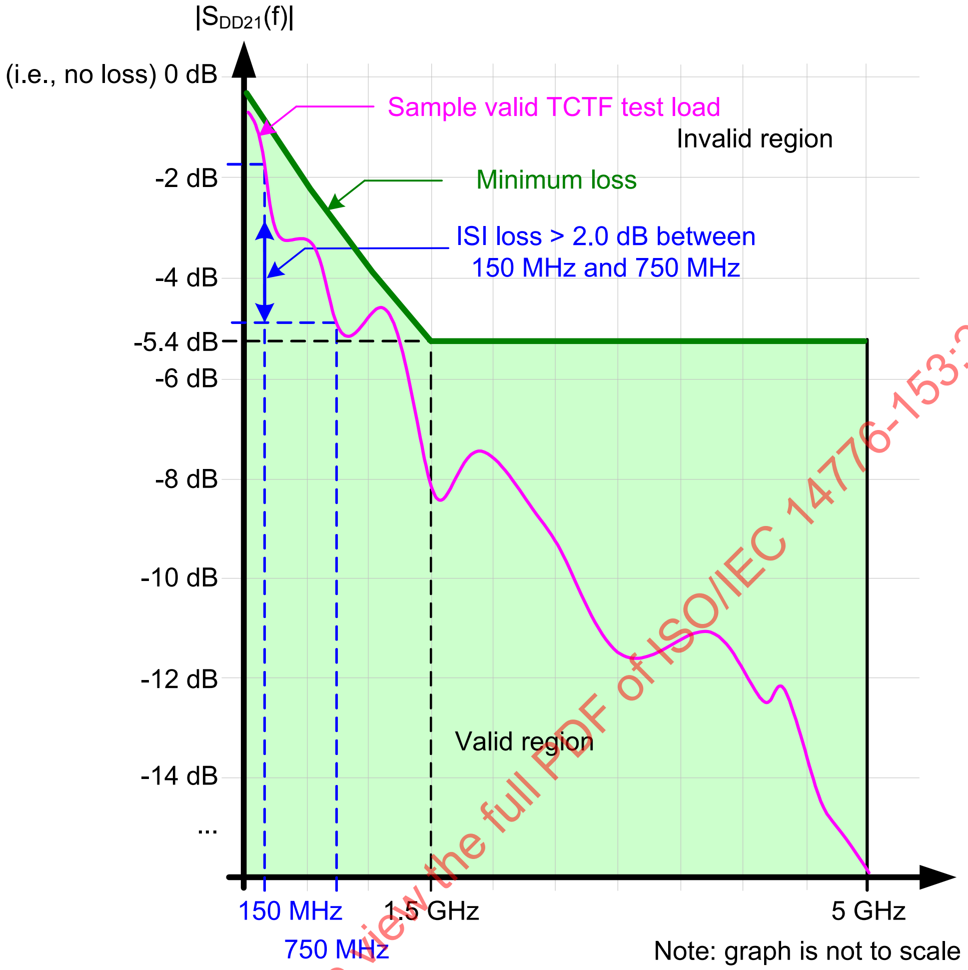


Figure 94 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at IT for untrained 1.5 Gbit/s

For testing an untrained 1.5 Gbit/s transmitter device at CT, the TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 1.5 GHz:

$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((1.7 \times 10^{-5} \times f^{0.5}) + (1.0 \times 10^{-10} \times f))$ dB

and for 1.5 GHz < f ≤ 5.0 GHz:

$|S_{DD21}(f)| \leq -7.0$ dB

and, specifying a minimum ISI loss:

$|S_{DD21}(f = 150\text{ MHz})| - |S_{DD21}(f = 750\text{ MHz})| > 2.0$ dB

where:

$|S_{DD21}(f)|$ magnitude of $S_{DD21}(f)$; and

f signal frequency in Hz.

Figure 95 shows the allowable $|S_{DD21}(f)|$ and minimum ISI loss of a TCTF test load and the $|S_{DD21}(f)|$ of a sample TCTF test load at CT for untrained 1.5 Gbit/s.

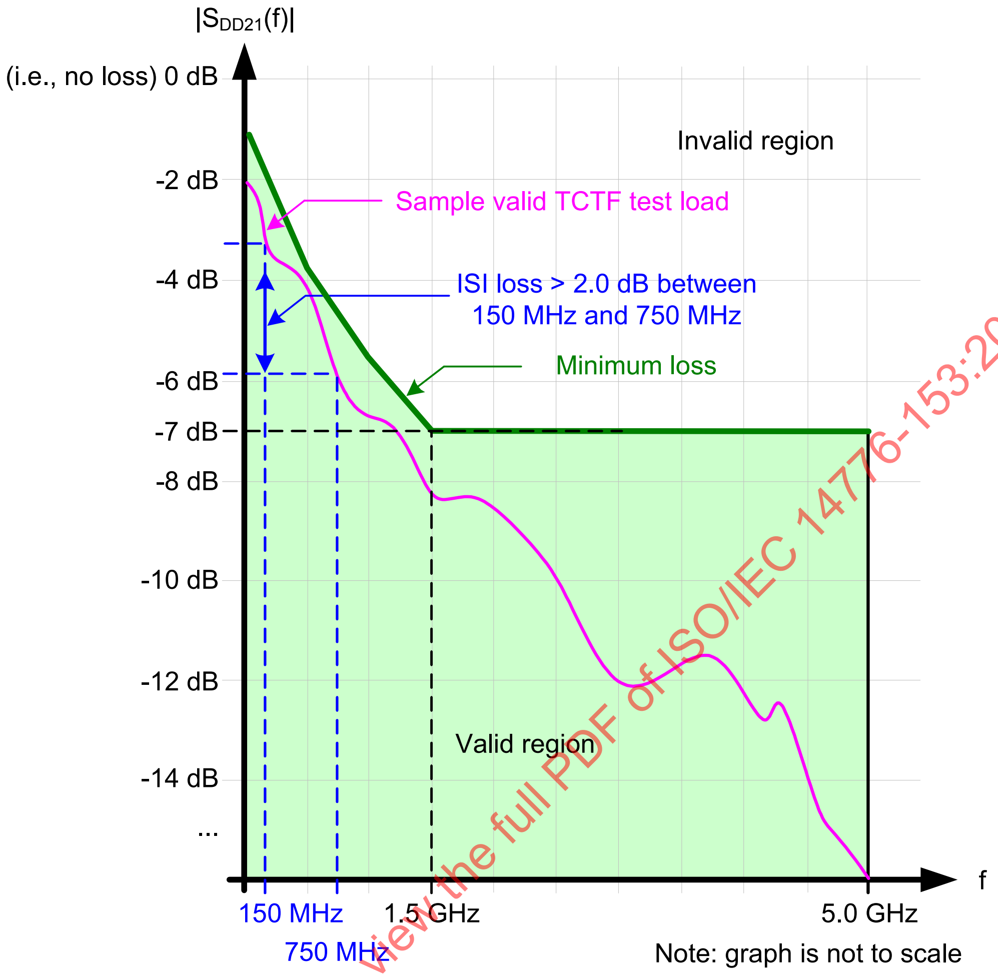


Figure 95 — TCTF test load $|S_{DD21}(f)|$ and ISI loss requirements at CT for untrained 1.5 Gbit/s

5.6.4 Low-loss TCTF test load

Figure 96 shows the low-loss TCTF test load. This test load is used for untrained 1.5 Gbit/s and 3 Gbit/s characterization.

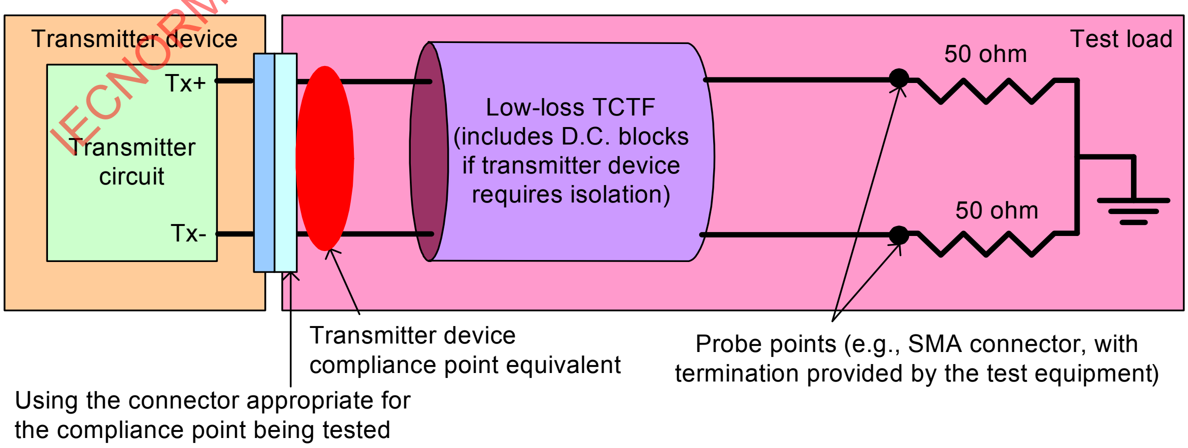


Figure 96 — Low-loss TCTF test load

The low-loss TCTF test load shall meet the requirements defined in 5.5.2. The nominal impedance shall be the target impedance.

The low-loss TCTF test load is defined by a set of S-parameters (see D.10). Only the magnitude of $S_{DD21}(f)$ is specified by this standard.

The low-loss TCTF test load shall comply with the following equations:

For 50 MHz < f ≤ 3.0 GHz:

$$|S_{DD21}(f)| \leq -20 \times \log_{10}(e) \times ((2.2 \times 10^{-6} \times f^{0.5}) + (6.9 \times 10^{-11} \times f) + (1.1 \times 10^{-20} \times f^{2}))\ \text{dB}$$

for 3.0 GHz < f ≤ 5.0 GHz:

$$|S_{DD21}(f)| \leq -3.7\ \text{dB}$$

and, specifying a minimum I*S*I loss:

$$|S_{DD21}(f = 300\ \text{MHz})| - |S_{DD21}(f = 1\ 500\ \text{MHz})| > 1.3\ \text{dB}$$

where:

$\|S_{DD21}(f)\|$	magnitude of $S_{DD21}(f)$; and
f	signal frequency in Hz.

Figure 97 shows the allowable $|S_{DD21}(f)|$ and minimum I*S*I loss of a low-loss TCTF test load and the $|S_{DD21}(f)|$ of a sample low-loss TCTF test load.

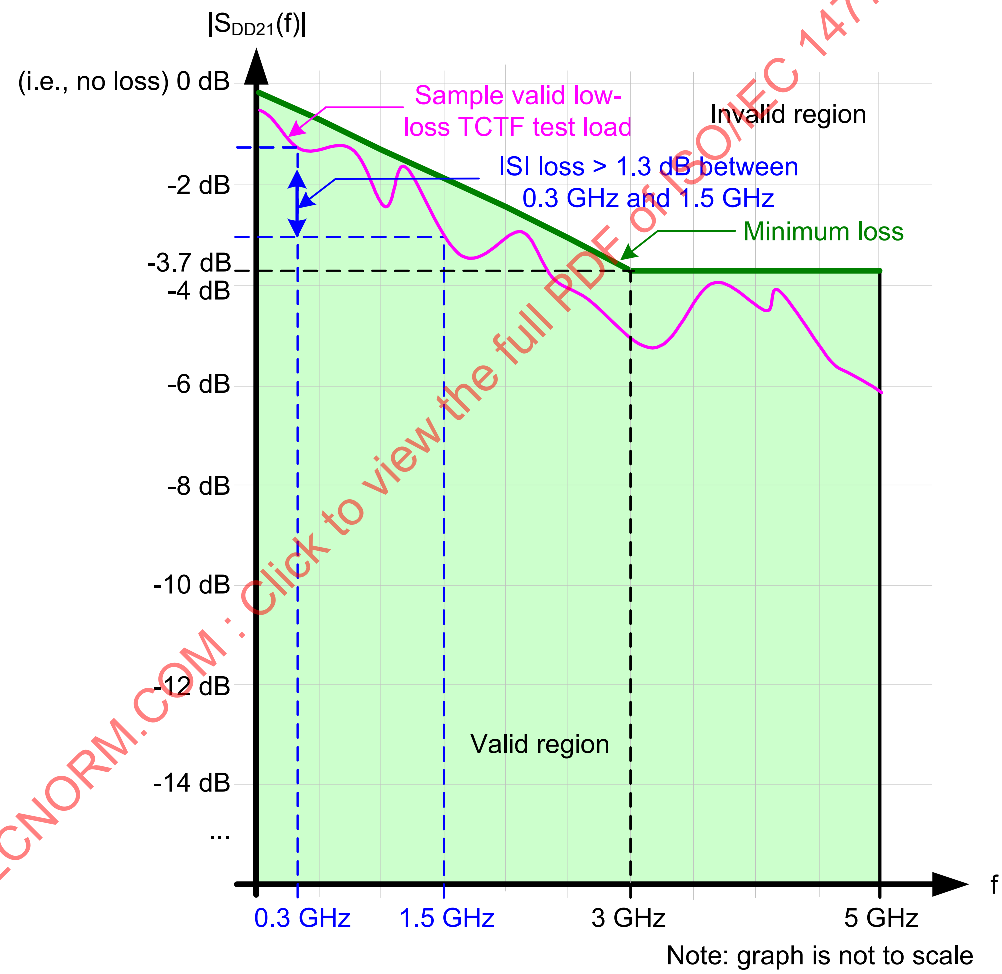


Figure 97 — Low-loss TCTF test load $|S_{DD21}(f)|$ and IS*I* loss requirements

5.6.5 Reference transmitter test load

The reference transmitter test load is a set of parameters defining the electrical performance characteristics of a 10 m Mini SAS 4x cable assembly, used:

a) in simulation to determine compliance of a transmitter device (see 5.7.4.6); and
b) as a representative component of an ISI generator used to determine compliance of a receiver device (see 5.7.5.7.4).

The following Touchstone model of the reference transmitter test load is included with this standard:

a) SAS2_transmittertestload.s4p.

See Annex E for a description of how the Touchstone model was created.

Figure 98 shows the reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz.

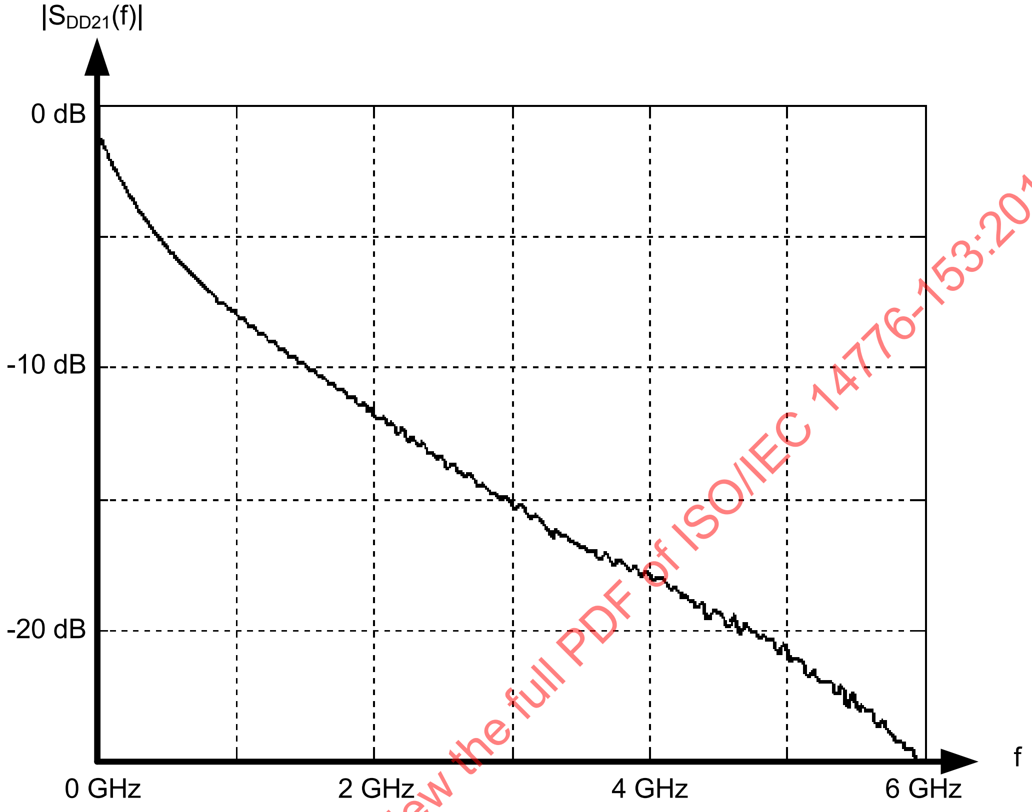


Figure 98 — Reference transmitter test load $|S_{DD21}(f)|$ up to 6 GHz

Figure 99 shows the reference transmitter test load pulse response.

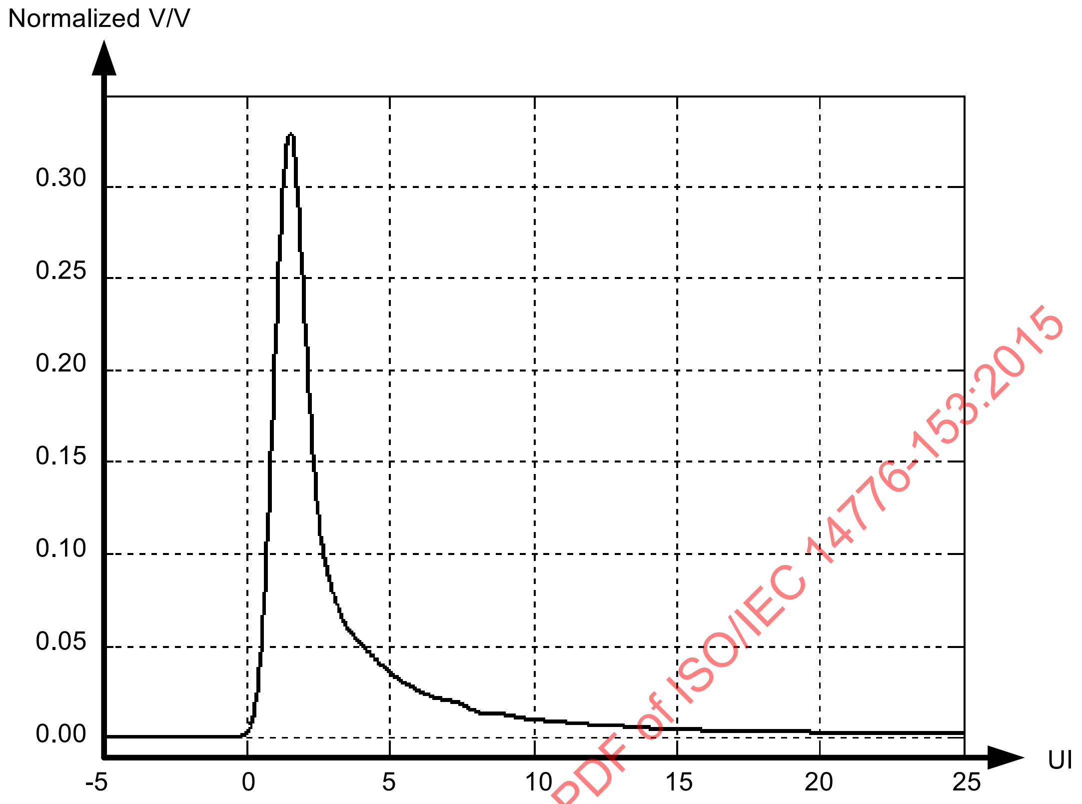


Figure 99 — Reference transmitter test load pulse response

The following impulse response model of the reference transmitter test load is included with this standard:

a) sas2_stressor_6g0_16x.txt.

Figure 100 shows the reference transmitter test load impulse response found in the sas2_stressor_6g0_16x.txt.

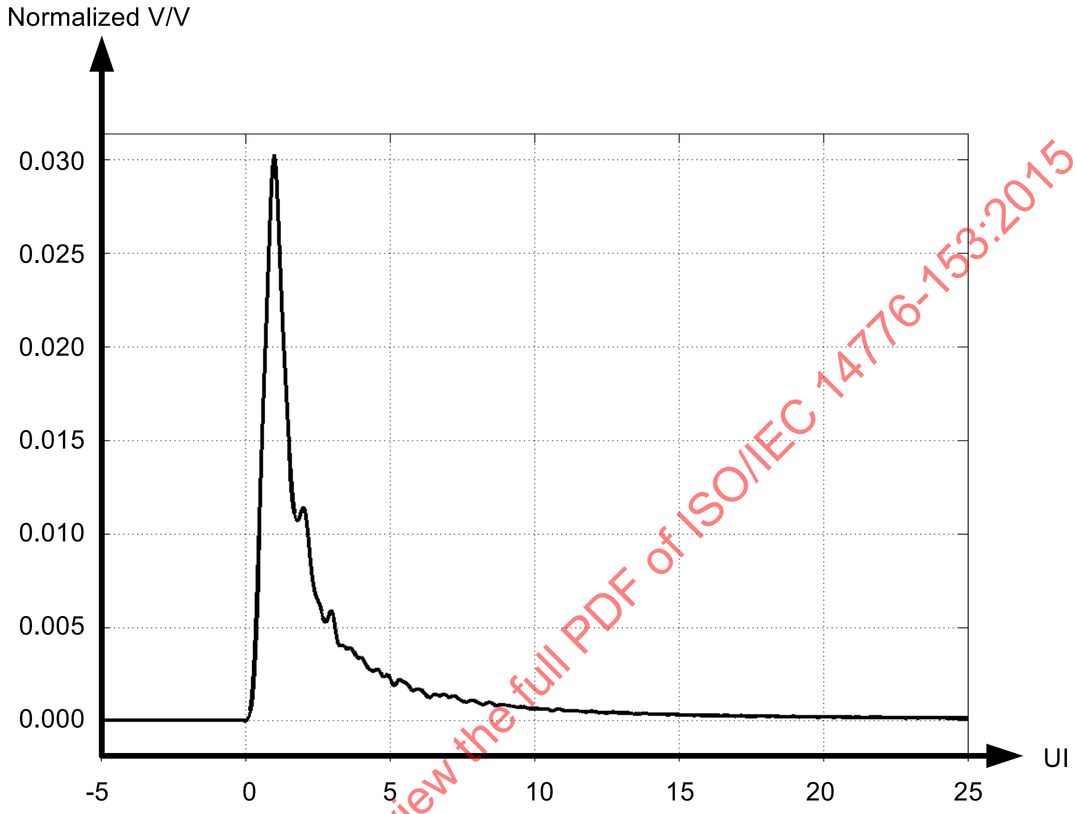


Figure 100 — Reference transmitter test load impulse response

Figure 101 shows the reference transmitter test load repeating 0011b or 1100b pattern (e.g., D24.3) response.

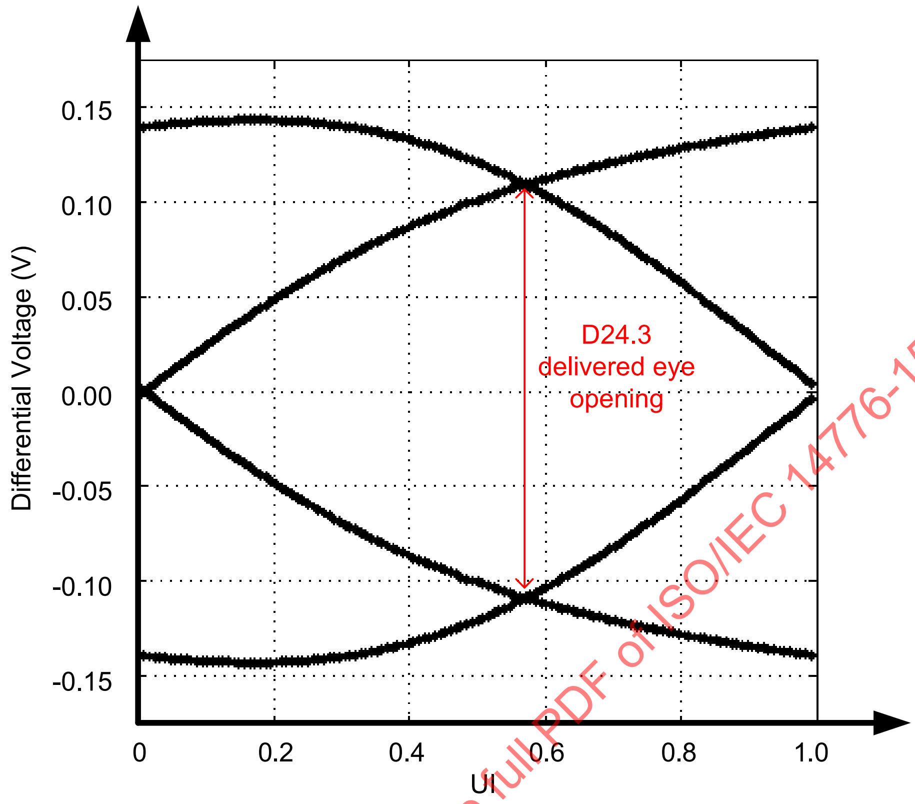


Figure 101 — Reference transmitter test load D24.3 response

5.7 Transmitter device and receiver device electrical characteristics

5.7.1 General electrical characteristics

Table 26 defines the general electrical characteristics, which apply to both transmitter devices and receiver devices.

Table 26 — General electrical characteristics

Characteristic	Units	1.5 Gbit/s (i.e., G1)	3 Gbit/s (i.e., G2)	6 Gbit/s (i.e., G3)
Physical link rate (nominal)	Mbyte/s	150	300	600
Unit interval (UI) (nominal) [a]	ps	$666.\overline{6}$	$333.\overline{3}$	$166.\overline{6}$
Baud rate (f_{baud}) (nominal)	Gigasymbols/s	1.5	3	6
Maximum A.C. coupling capacitor [b]	nF	12		
Maximum noise during OOB idle time [c] [d]	mV(P-P)	120		

[a] $666.\overline{6}$ equals 2 000 / 3. $333.\overline{3}$ equals 1 000 / 3. $166.\overline{6}$ equals 500 / 3.
[b] The coupling capacitor value for A.C. coupled transmit and receive pairs. See 5.7.4.2 for A.C. coupling requirements for transmitter devices. See 5.7.5.2 for A.C. coupling requirements for receiver devices. The equivalent series resistance at 3 GHz should be less than 1 Ω.
[c] With a measurement bandwidth of 1.5 × f_{baud} (e.g., 9 GHz for 6 Gbit/s), no signal level during the idle time shall exceed the specified maximum differential amplitude.
[d] This is not applicable when optical mode is enabled.

5.7.2 Transmitter device and receiver device transients

Transients may occur at transmitter devices or receiver devices as a result of changes in supply power conditions or mode transitions.

A mode transition is an event that may result in a measurable transient due to the response of the transmitter device or receiver device. The following conditions constitute a mode transition:

a) enabling or disabling driver circuitry;
b) enabling or disabling receiver common-mode circuitry;
c) hot plug event;
d) adjusting driver amplitude;
e) enabling or disabling de-emphasis; and
f) adjusting terminator impedance.

Transmitter device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 102 during all power state and mode transitions. Receiver device transients are measured at nodes V_P and V_N with respect to GROUND on the test circuit shown in figure 103 during all power state and mode transitions. Test conditions shall include power supply power on and power off conditions, voltage sequencing, and mode transitions.

Figure 102 shows the test circuit attached to IT or CT to test transmitter device transients.

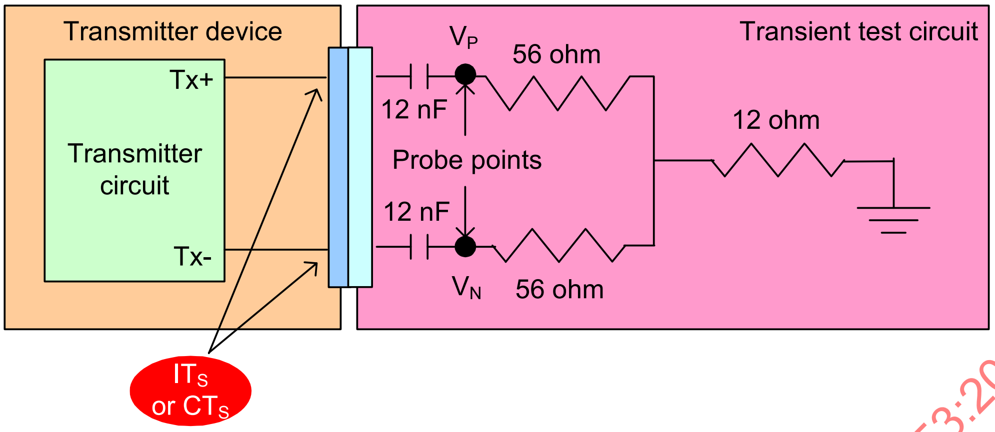


Figure 102 — Transmitter device transient test circuit

Figure 103 shows the test circuit attached to IR or CR to test receiver device transients.

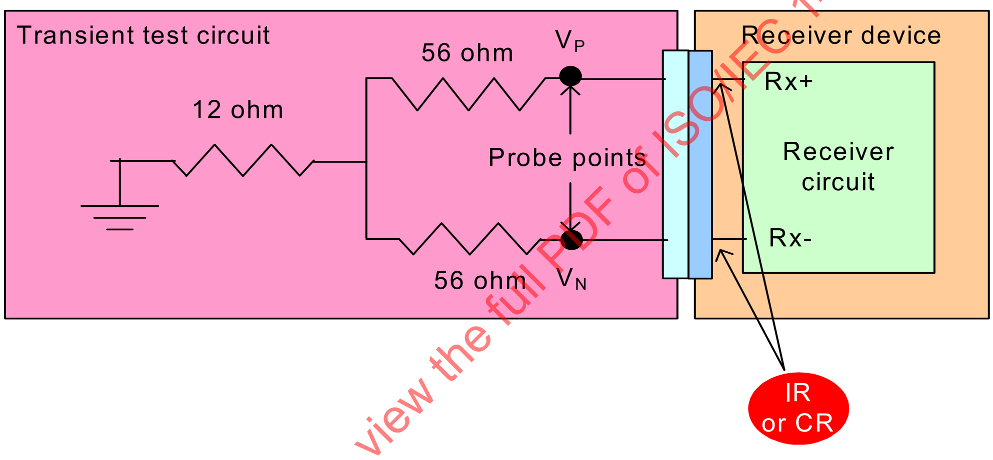


Figure 103 — Receiver device transient test circuit

5.7.3 Eye masks and the jitter transfer function (JTF)

5.7.3.1 Eye masks overview

The eye masks shown in this subclause shall be interpreted as graphical representations of the voltage and time limits of the signal. The eye mask boundaries define the eye contour of:

a) the 10^{-12} jitter population for untrained 1.5 Gbit/s and 3 Gbit/s measured eyes; and
b) the 10^{-15} jitter population for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s simulated eyes.

For untrained 1.5 Gbit/s and 3 Gbit/s, equivalent time sampling oscilloscope technology is not practical for measuring compliance to the eye masks. See MJSQ for methods that are suitable for verifying compliance to these eye masks.

CJTPAT (see Annex A) shall be used for all jitter testing unless otherwise specified. Annex A defines the required pattern on the physical link and provides information regarding special considerations for running disparity (see SPL) and scrambling (see SPL).

5.7.3.2 Jitter transfer function (JTF)

With the possible presence of SSC, the application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667) as specified in versions of SAS standards previous to SAS-2 does not separate the SSC component from the actual jitter and thus may overstate the transmitter device jitter. To differentiate between allowable timing variation due to SSC and jitter, the frequency-weighting JTF shall be applied to the signal at the compliance point when determining the eye mask.

The jitter measurement device shall comply with the JTF. The reference clock characteristics are controlled by the resulting JTF characteristics obtained by taking the time difference between the PLL output (i.e., the reference clock) and the data stream sourced to the PLL. The PLL's closed loop transfer function's -3 dB corner frequency and other adjustable parameters (e.g., peaking) are determined by the value required to meet the requirements of the JTF.

The JTF shall have the characteristics specified in table 27 for a repeating 0011b or 1100b pattern (e.g., D24.3) See the phy test patterns in the Protocol-Specific diagnostic page in SPL.

The JTF -3 dB corner frequency and the magnitude peaking requirements shall be measured with SJ applied, with a peak-to-peak amplitude of 0.3 *UI* ± 10 %. The relative attenuation at 30 kHz shall be measured with sinusoidal phase (i.e., time) modulation applied, with a peak-to-peak amplitude of 20.8 ns ± 10 %. See
Annex D for the detailed calibration procedure.

A proportional decrease of the JTF -3 dB corner frequency should be observed for a decrease in pattern transition density compared to a 0.5 transition density. If a JMD shifts the JTF -3 dB corner frequency in a manner that does not match this characteristic, or does not shift at all, then measurements of jitter with patterns with transition densities different than 0.5 may lead to discrepancies in reported jitter levels. In the case of reported jitter discrepancies between JMDs, the JMD with the shift of the -3 dB corner frequency that is closest to the proportional characteristic of the reference transmitter test load (see 5.6.5) shall be considered correct. This characteristic may be measured with the conditions defined above for measuring the -3 dB corner frequency but substituting other patterns with different transition densities.

Table 27 — JTF parameters

Characteristic	Untrained		Trained without SSC support			Trained with SSC support		
	1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s	6 Gbit/s	1.5 Gbit/s	3 Gbit/s	6 Gbit/s
JTF -3 dB point (kHz) [a] [b]	900 ± 500	1 800 ± 500	900 ± 500	1 800 ± 500	3 600 ± 500	1 300 ± 500	1 838 ± 500	2 600 ± 500
JTF slope (dB/decade)	20	20	20	20	20	40	40	40
Attenuation at 30 kHz ± 1 % (dB) [c]	N/A	N/A	N/A	N/A	N/A	61.5 ± 1.5	67.5 ± 1.5	73.5 ± 1.5
Maximum Peaking (dB)	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5

[a] For untrained or trained without SSC support this value equals f_{baud}/1 667 ± 500 kHz. [d]
[b] For trained with SSC support this value equals $(f_{baud})^{0.5}$ x 33.566 x $Hz^{0.5}$ ± 500 kHz. [d]
[c] For trained with SSC support this value equals 73.5 dB + [20 x log(f_{baud} / 6 x 10^9 Hz)] dB ± 1.5 dB. [d]
[d] For the above equations, f_{baud} is expressed in Hz (i.e., 1.5 GHz for 1.5 Gbit/s, 3.0 GHz for 3 Gbit/s, 6.0 GHz for 6 Gbit/s).

5.7.3.3 Transmitter device eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 104 describes the eye mask used for testing the signal output of the transmitter device at IT and CT for untrained 1.5 Gbit/s and 3 Gbit/s (see table 31 in 5.7.4.5) and OOB signals (see table 37 in 5.7.4.7). This eye mask applies to jitter after the application of the JTF (see 5.7.3.2).

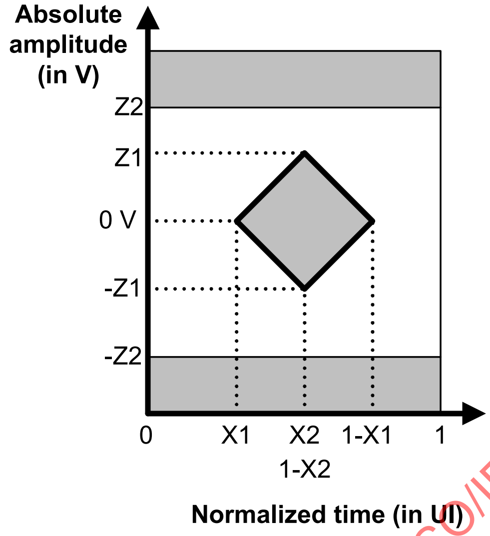


Figure 104 — Transmitter device eye mask

Verifying compliance with the limits represented by the transmitter device eye mask should be done with reverse channel traffic present on the channel under test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.7.3.4 Receiver device eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 105 describes the eye mask used for testing the signal delivered to the receiver device at IR and CR for untrained 1.5 Gbit/s and 3 Gbit/s (see table 40 in 5.7.5.4). This eye mask applies to jitter after the application of the JTF (see 5.7.3.2). This requirement accounts for the low frequency tracking properties and response time of the CDR circuitry in receiver devices.

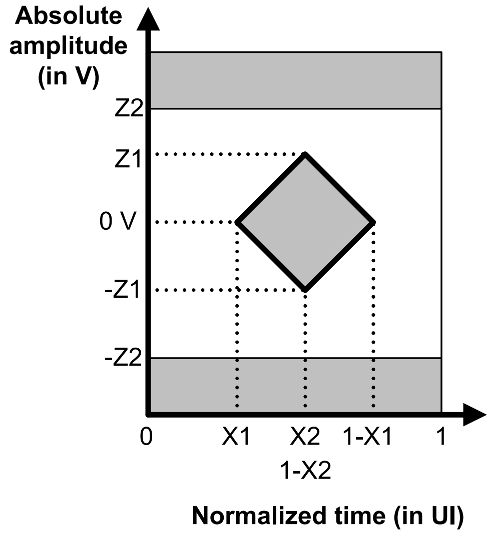


Figure 105 — Receiver device eye mask

Verifying compliance with the limits represented by the receiver device eye mask should be done with reverse channel traffic present on the channel-under-test and with forward and reverse traffic present on all other channels, in order that the effects of crosstalk are taken into account.

5.7.3.5 Receiver device jitter tolerance eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

Figure 106 describes the eye mask used to test the jitter tolerance of the receiver device at IR and CR for untrained 1.5 Gbit/s and 3 Gbit/s (see table 40 in 5.7.5.4). For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, jitter tolerance is included in the delivered signal specifications for stressed receiver device jitter tolerance testing (see 5.7.5.7.4).

The eye mask shall be constructed as follows:

a) X2 and Z2 shall be the values for the delivered signal listed in table 40 (see 5.7.5.4);
b) $X1_{OP}$ shall be half the value of TJ for maximum delivered jitter listed in table 41 (see 5.7.5.5); and
c) $X1_{TOL}$ shall be half the value of TJ for receiver device jitter tolerance listed in table 42 (see 5.7.5.6), for applied SJ frequencies above (f_{baud} / 1 667).

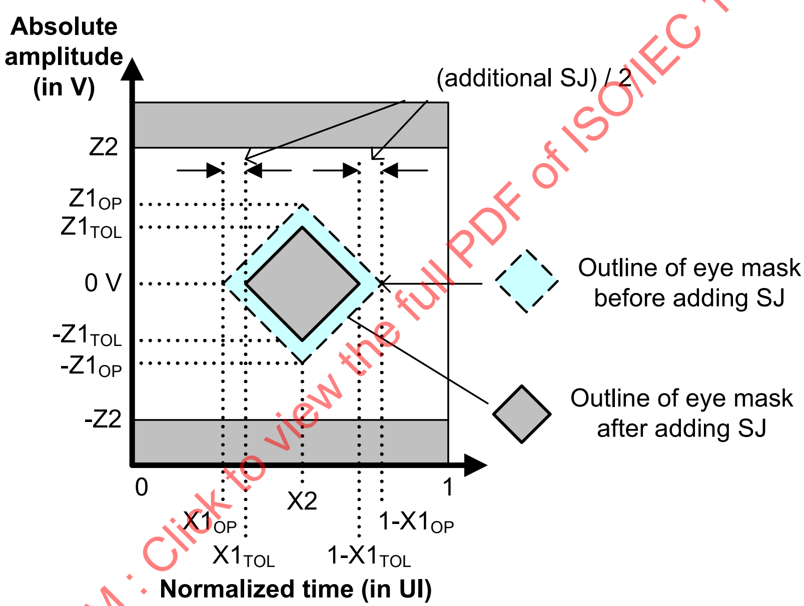


Figure 106 — Deriving a receiver device jitter tolerance eye mask for untrained 1.5 Gbit/s and 3 Gbit/s

The leading and trailing edge slopes of the receiver device eye mask in figure 105 (see 5.7.3.4) shall be preserved. As a result, the amplitude value of Z1 is less than that given for the delivered signal in table 40 (see 5.7.5.4), and $Z1_{TOL}$ and $Z1_{OP}$ shall be defined from those slopes by the following equation:

$$Z1_{TOL} = Z1_{OP} \times \frac{X2 - \left(\frac{ASJ}{2}\right) - X1_{OP}}{X2 - X1_{OP}}$$

where:

$Z1_{TOL}$	is the value for Z1 to be used for the receiver device jitter tolerance eye mask;
$Z1_{OP}$	is the Z1 value for the delivered signal in table 40;
$X1_{OP}$	is the X1 value for the delivered signal in table 40;
X2	is the X2 value for the delivered signal in table 40; and
ASJ	is the additional SJ for applied SJ frequencies above (f_{baud} / 1 667) (see figure 112 in 5.7.5.6).

The X1 points in the receiver device jitter tolerance eye mask (see figure 106) are greater than the X1 points in the receiver device eye mask (see figure 105) due to the addition of SJ.

5.7.4 Transmitter device characteristics

5.7.4.1 Transmitter device characteristics overview

Transmitter devices may or may not incorporate de-emphasis (i.e., pre-emphasis) and other forms of compensation. The transmitter device shall use the same settings (e.g., de-emphasis and voltage swing) with both the zero-length test load and the appropriate TCTF test load or reference transmitter test load (see 5.6).

See D.6 for a methodology for measuring transmitter device signal output.

5.7.4.2 Transmitter device A.C. coupling requirements

AC coupling requirements for transmitter devices are as follows:

a) transmitter devices using inter-enclosure TxRx connections (i.e., attached to CT compliance points) shall be A.C. coupled to the interconnect through a transmission network;
b) transmitter devices using intra-enclosure TxRx connections (i.e., attached to IT compliance points) that support SATA shall be A.C. coupled to the interconnect through a transmission network; and
c) transmitter devices using intra-enclosure TxRx connections (i.e., attached to IT compliance points) that do not support SATA may be A.C. or D.C. coupled.

See table 26 (see 5.7.1) for the coupling capacitor value.

5.7.4.3 Transmitter device general electrical characteristics

Table 28 defines the transmitter device general electrical characteristics.

Table 28 — Transmitter device general electrical characteristics

Characteristic	Units	1.5 Gbit/s	3 Gbit/s	6 Gbit/s
Physical link rate long-term stability at IT and CT	ppm	± 100		
Physical link rate SSC modulation at IT and CT	ppm	See table 52 and table 53 in 5.7.6.2		
Maximum transmitter device transients [a]	V	± 1.2		
[a] See 5.7.2 for transient test circuits and conditions.				

Table 29 defines the transmitter device termination characteristics.

Table 29 — Transmitter device termination characteristics

Characteristic	Units	Untrained		Trained 1.5 Gbit/s, 3 Gbit/s, 6 Gbit/s
		1.5 Gbit/s	3 Gbit/s	
Differential impedance [a]	Ω	60 minimum 115 maximum		See 5.7.4.6.1
Maximum differential impedance imbalance [a] [b]	Ω	5		See 5.7.4.6.3 [c]
Common-mode impedance [b]	Ω	15 minimum 40 maximum		See 5.7.4.6.1

[a] All transmitter device termination measurements are made through mated connector pairs.
[b] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.
[c] Measurement replaced by S_{CD22} specifications (i.e., differential to common mode conversion).

5.7.4.4 Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load

Table 30 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load (see 5.6.2) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.7.4.6 for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device signal output characteristics. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 30 — Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero-length test load at IT and CT

Signal characteristic [a]	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Maximum intra-pair skew [b]	ps	20	15
Maximum transmitter device off voltage [c] [d]	mV(P-P)	50	
Maximum (i.e., slowest) rise/fall time [e]	ps	273	137
Minimum (i.e., fastest) rise/fall time [e]	ps	41.6	
Maximum transmitter output imbalance [f]	%	10	

[a] All tests in this table shall be performed with zero-length test load (see 5.6.2).
[b] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Tx+ and Tx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Tx+ signal and the Tx- signal.
[c] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).
[d] This is not applicable when optical mode is enabled.
[e] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) on the physical link.
[f] The maximum difference between the V+ and V- A.C. r.m.s. transmitter device amplitudes measured with CJTPAT (see Annex A) into the zero-length test load shown in figure 88 (see 5.6.2), as a percentage of the average of the V+ and V- A.C. r.m.s. amplitudes.

5.7.4.5 Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load

Table 31 specifies the signal output characteristics for the transmitter device for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load (i.e., the zero-length test load (see 5.6.2) and either the TCTF test load (see 5.6.3) or the low-loss TCTF test load (see 5.6.4)) attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements. See 5.7.4.6 for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device signal output characteristics. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) transmitter device signal output characteristics.

Table 31 — Transmitter device signal output characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with each test load at IT and CT

Signal characteristic	Units	IT, untrained		CT, untrained	
		1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 104) if SATA is not supported	mV(P-P)	1 600			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 104) if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 104), if SATA is not supported	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 104), if SATA is supported	mV(P-P)	see SATA [a]		N/A	
Maximum DJ [b c d]	UI	0.35			
Maximum half of TJ (i.e., X1 in figure 104) [b c d e f g h]	UI	0.275			
Center of bit time (i.e., X2 in figure 104)	UI	0.50			
Maximum intra-pair skew [i]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] All DJ and TJ values are level 1 (see MJSQ).

[c] The values for jitter in this table are measured at the average signal amplitude point.

[d] The DJ and TJ values in this table apply to jitter measured as described in 5.7.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.

[e] TJ is specified at a CDF level of 10^{-12}.

[f] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.

Jitter peak-to-peak measured < (maximum TJ - |Asymmetry|).

[g] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability, direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[h] The value for X1 is also half the value of TJ for maximum delivered jitter listed in table 41 (see 5.7.5.5). The test or analysis shall include the effects of the JTF (see 5.7.3.2).

[i] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Tx+ and Tx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Tx+ signal and the Tx- signal at the probe points.

5.7.4.6 Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

5.7.4.6.1 Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s overview

Table 32 specifies the signal output characteristics for the transmitter device for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s as measured with the zero-length test load (see 5.6.2), unless otherwise specified, attached at a transmitter device compliance point (i.e., IT or CT). All specifications are based on differential measurements.

Table 32 — Transmitter device signal output characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s at IT and CT

Signal characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850		1 200
Transmitter device off voltage [b] [c]	mV(P-P)			50
Withstanding voltage (non-operational)	mV(P-P)	2 000		
Rise/fall time [d]	ps	41.6		
Reference differential impedance [e]	Ω		100	
Reference common mode impedance [e]	Ω		25	
Common mode voltage limit (r.m.s.) [f]	mV			30
RJ [g] [h]	UI			0.15 [i]
TJ [j] [h]	UI			0.25 [k]
WDP at 6 Gbit/s [l]	dB			13
WDP at 3 Gbit/s [l]	dB			7
WDP at 1.5 Gbit/s [l]	dB			4.5

[a] See 5.7.4.6.6 for the V_{P-P} measurement method.

[b] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[c] This is not applicable when optical mode is enabled.

[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) on the physical link.

[e] See 5.7.4.6.3 for transmitter device S-parameters characteristics.

[f] This is a broadband limit. For additional limits on spectral content, see figure 107 and table 33.

[g] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of 10^{-12}. For simulations based on a BER of 10^{-15}, the RJ specified is 16 times the RJ 1 sigma value.

[h] The measurement shall include the effects of the JTF (see 5.7.3.2).

[i] 0.15 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.

[j] The TJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.

[k] 0.25 UI is 41.6 ps at 6 Gbit/s, 83.3 ps at 3 Gbit/s, and 166.6 ps at 1.5 Gbit/s.

[l] See 5.7.4.6.2 for the transmitter device test procedure.

Table 33 defines the transmitter device common mode voltage limit characteristics.

Table 33 — Transmitter device common mode voltage limit characteristics

Characteristic	Reference	*L* [a] (dBmV) [b]	*N* [a] (dBmV) [b] [c]	*S* [a] (dBmV/decade) [b]	f_{min} [a] (MHz)	f_{max} [a] (GHz)
Spectral limit of common mode voltage [d]	Figure 107	12.7	26.0	13.3	100	6.0

[a] See figure 4 in 5.2 for definitions of *L*, *N*, *S*, f_{min}, and f_{max}. For this parameter, units of dBmV is used in place of dB.
[b] For dBmV, the reference level of 0 dBmV is 1 mV (r.m.s.). Hence, 0 dBm is 1 mW which is 158 mV (r.m.s.) across 25 Ωs (i.e., the reference impedance for common mode voltage) which is 20 × $\log_{10}(158)$ = +44 dBmV. +26 dBmV is therefore -18 dBm.
[c] Maximum value at the Nyquist frequency (i.e., 3 GHz) (see figure 107).
[d] The transmitter device common mode voltage shall be measured with a 1 MHz resolution bandwidth through the range of 100 MHz to 6 GHz with the transmitter device output of CJTPAT (see Annex A). The end points of the range shall be at the center of the measurement bandwidth.

Figure 107 shows the transmitter device common mode voltage limit defined in table 33.

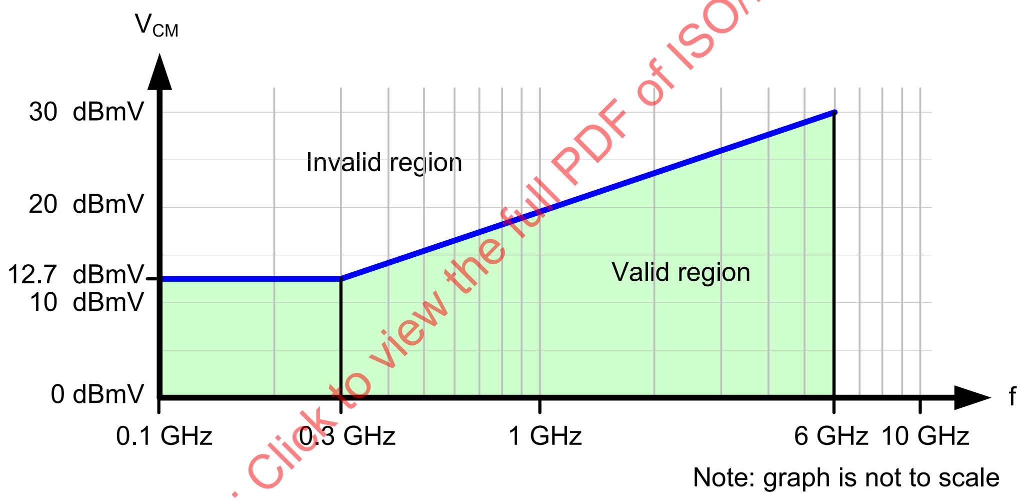


Figure 107 — Transmitter device common mode voltage limit

5.7.4.6.2 Transmitter device test procedure

The transmitter device test procedure is as follows:

1) attach the transmitter device to a zero-length test load, where its signal output is captured by an oscilloscope;
2) configure the transmitter device to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL);
3) configure the transmitter device to minimize DCD and BUJ;

NOTE 8 WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

4) capture at least 58 dwords (i.e., 2 320 bits on the physical link). Use averaging to minimize RJ; and
5) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to ‘SAS2_TWDP’.

The WDP value is a characterization of the signal output within the reference receiver device (see 5.7.5.7.3) after equalization.

5.7.4.6.3 Transmitter device S-parameter limits

S-parameter limits are calculated per the following formula:

Measured value < max [L, min [H, N + 13.3 × $\log_{10}(f / 3\text{ GHz})$]]

where:

L	is the minimum value (i.e., the low frequency asymptote);
H	is the maximum value (i.e., the high frequency asymptote);
N	is the value at the Nyquist frequency (i.e., 3 GHz);
f	is the frequency of the signal in Hz;
max [A, B]	is the maximum of A and B; and
min [A, B]	is the minimum of A and B.

Table 34 defines the maximum limits for S-parameters of the transmitter device.

Table 34 — Maximum limits for S-parameters at IT_s or CT_s

Characteristic [a] [b]	***L*** [c] **(dB)**	***N*** [c] **(dB)**	***H*** [c] **(dB)**	***S*** [c] **(dB / decade)**	f_{min} [c] **(MHz)**	f_{max} [c] **(GHz)**
$\lvert S_{CC22}\rvert$	-6.0	-5.0	0	13.3	100	6.0
$\lvert S_{DD22}\rvert$	-10	-7.9	0	13.3	100	6.0
$\lvert S_{CD22}\rvert$	-26	-12.7	-10	13.3	100	6.0

[a] For S-parameter measurements, the transmitter device under test shall transmit a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL). The amplitude applied by the test equipment shall be less than -4.4 dBm (190 mV zero to peak) per port. See D.10.4.2.

[b] $\lvert S_{DC22}\rvert$ is not specified.

[c] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 108 shows the transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in table 34.

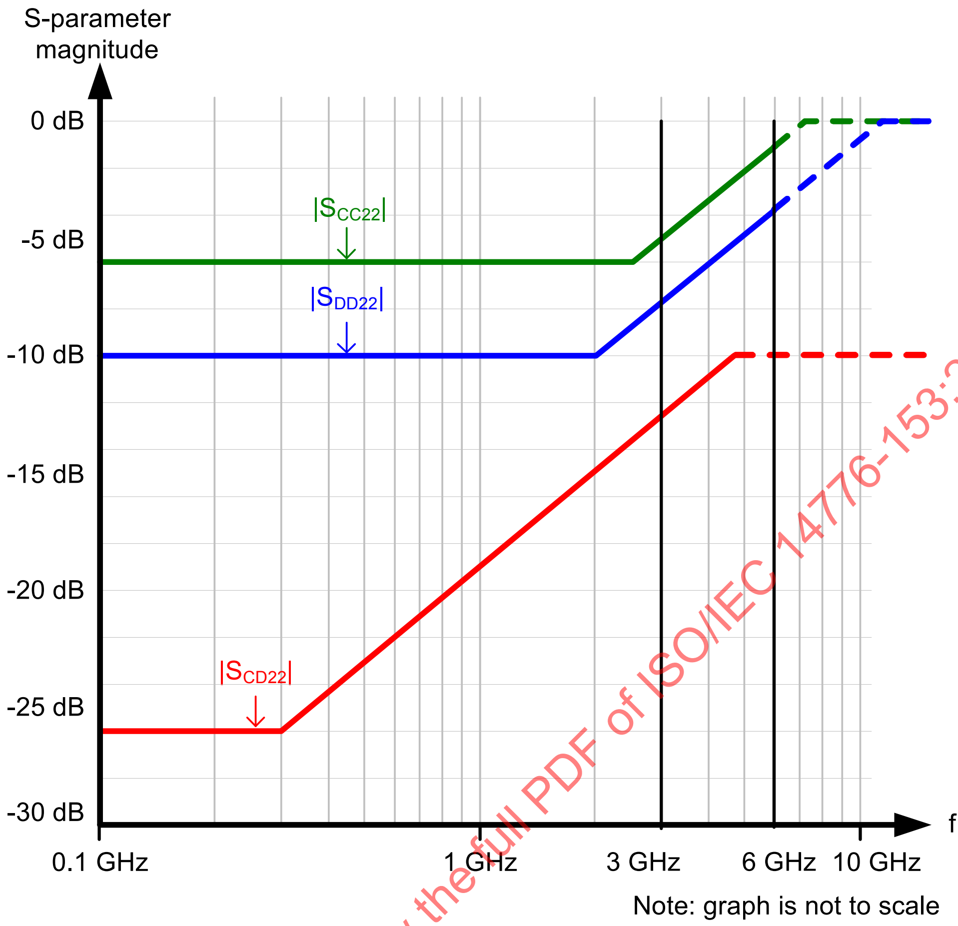


Figure 108 — Transmitter device $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits

5.7.4.6.4 Recommended transmitter device settings for interoperability

Table 35 defines recommended values for transmitter devices to provide interoperability with a broad range of implementations utilizing compliant TxRx connections and compliant receiver devices. The values are based on the evaluation of simulations with a variety of characterized physical hardware. Use of the recommended values does not guarantee that an implementation is capable of achieving a specific BER.

Specific implementations may obtain increased margin by deviating from the recommended values. However, such implementations are beyond the scope of this standard.

Table 35 — Recommended transmitter device settings at IT and CT

Characteristic	Units	Minimum	Nominal	Maximum
Differential voltage swing (mode) (VMA) [a]	mV	600	707	
Transmitter equalization [a]	dB	2	3	4
[a] See 5.7.4.6.6 for measurement method.				

5.7.4.6.5 Reference transmitter device characteristics

The reference transmitter device is a set of parameters defining the electrical performance characteristics of a transmitter device used in simulation to determine compliance of a TxRx connection (see 5.5.5).

Figure 109 shows a reference transmitter device.

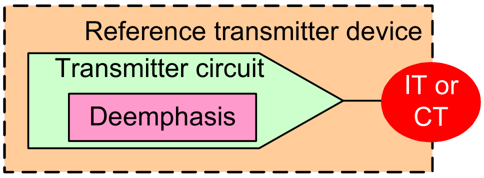


Figure 109 — Reference transmitter device

Table 36 defines the reference transmitter device characteristics.

Table 36 — Reference transmitter device characteristics at IT and CT

Characteristic	Units	Value
Peak to peak voltage (V_{P-P}) [a]	mV(P-P)	850
Transmitter equalization [a]	dB	2
Maximum (i.e., slowest) rise/fall time [b]	UI	0.41 [c]
RJ	UI	0.15 [d]
BUJ	UI	0.10 [e]

[a] See 5.7.4.6.6 for measurement method.
[b] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL).
[c] 0.41 UI is 68.3 ps at 6 Gbit/s, 136.6 ps at 3 Gbit/s, and 273.3 ps at 1.5 Gbit/s.
[d] 0.15 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[e] 0.10 UI is 16.6 ps at 6 Gbit/s, 33.3 ps at 3 Gbit/s, and 66.6 ps at 1.5 Gbit/s.

The following Touchstone model of the reference transmitter device termination is included with this standard:

a) SAS2_TxRefTerm.s4p.

Figure 110 shows the S-parameters of the reference transmitter device termination model.

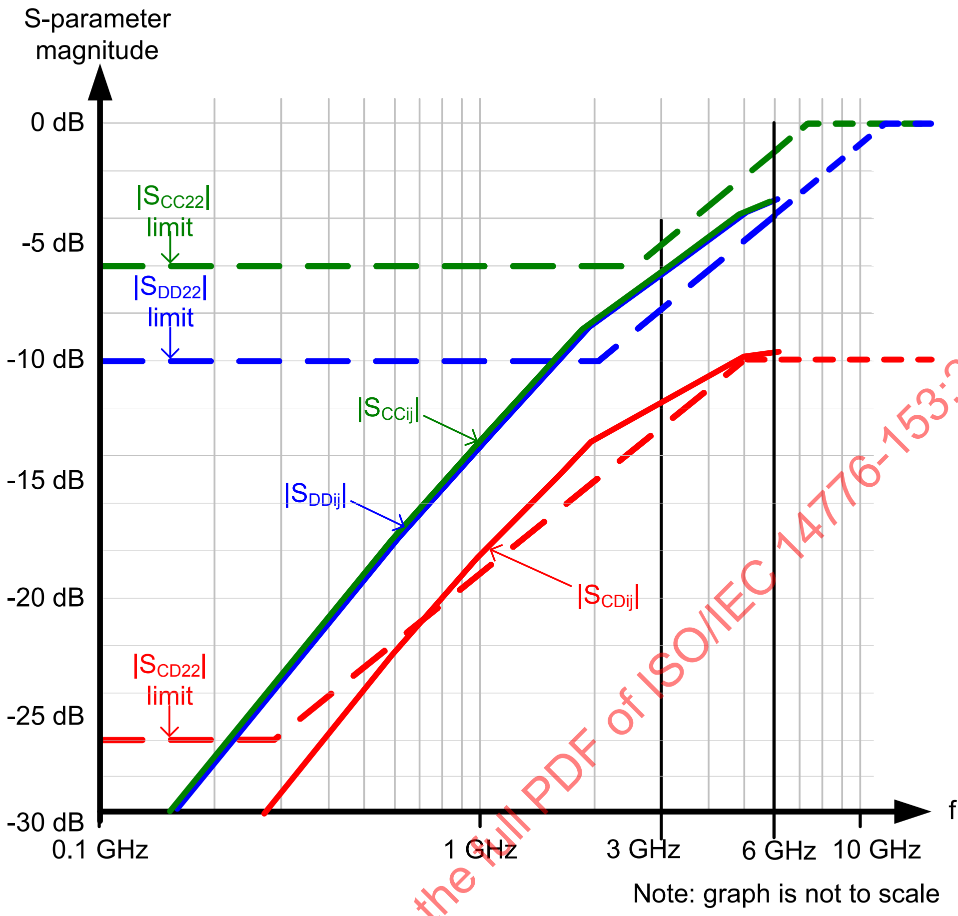


Figure 110 — Reference transmitter device termination S-parameters

The Touchstone model does not exactly match the $|S_{CC22}|$, $|S_{DD22}|$, and $|S_{CD22}|$ limits defined in 5.7.4.6.3 at all frequencies; it is a reasonable approximation for use in simulations. See Annex E for a description of how the Touchstone model was created.

5.7.4.6.6 Transmitter equalization, VMA, and V_{P-P} measurement

The transmitter equalization measurement shall be based on the following values:

a) VMA: a mode (i.e., the most frequent value of a set of data) measurement; and
b) V_{P-P}: a peak-to-peak measurement with a repeating 7Eh (i.e., D30.3) pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL).

The VMA and V_{P-P} measurements shall be made with the transmitter device terminated through the interoperability point into a zero length test load (see 5.6.2).

The VMA and V_{P-P} measurements shall be made using an equivalent time sampling scope with a histogram function with the following or an equivalent procedure:

1) calibrate the sampling scope for measurement of a 3 GHz signal; and
2) determine VMA and V_{P-P} as shown in figure 111. A sample size of 1 000 minimum to 2 000 maximum histogram hits for VMA shall be used to determine the values. The histogram is a combination of two histograms: an upper histogram for Tx+ and a lower histogram for Tx-. The histograms on the left represent the test pattern signal displayed on the right. VMA and V_{P-P} are determined by adding the values measured for Tx+ and Tx-.

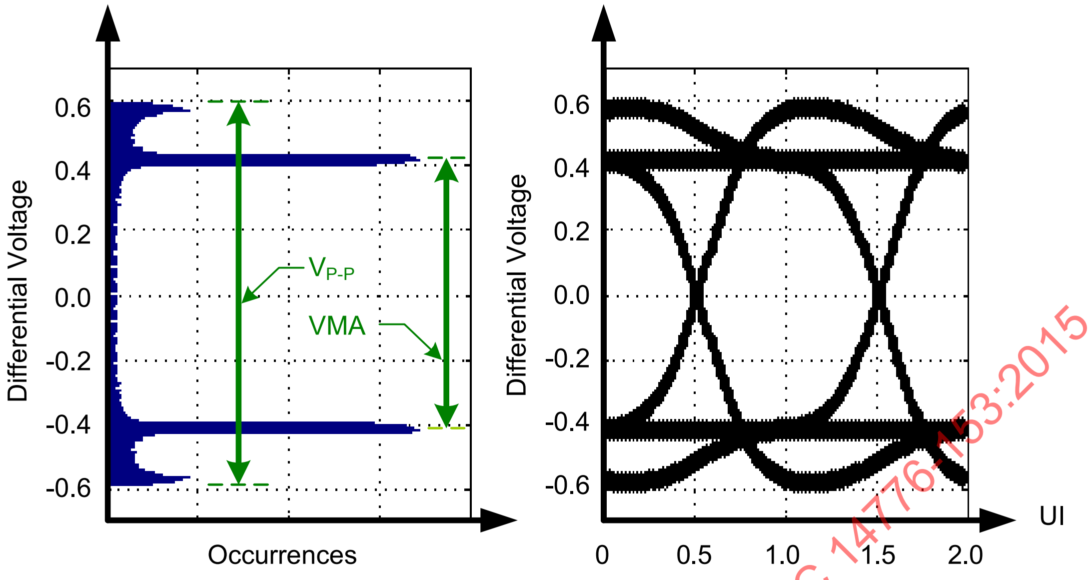


Figure 111 — Transmitter equalization measurement

The following formula shall be used to calculate the transmitter equalization value:

Transmitter equalization = $20 \times \log_{10} (V_{P\text{-}P} / VMA)$ dB

where:

$V_{P\text{-}P}$ is the peak-to-peak value; and

VMA is the mode value.

5.7.4.7 Transmitter device signal output characteristics for OOB signals

Transmitter devices supporting SATA shall use SATA Gen1i, Gen2i, or Gen3i signal output levels (see SATA) during the first OOB sequence (see SPL) after a power on or hard reset. If the phy does not receive COMINIT within a hot-plug timeout (see SPL), then the transmitter device shall increase its transmit levels to the OOB signal output levels specified in table 37 and perform the OOB sequence again. If no COMINIT is received within a hot-plug timeout of the second OOB sequence, then the transmitter device shall initiate another OOB sequence using SATA Gen1i, Gen2i, or Gen3i signal output levels. The transmitter device shall continue alternating between transmitting COMINIT using SATA Gen1i, Gen2i, or Gen3i signal output levels and transmitting COMINIT with SAS signal output levels until the phy receives COMINIT.

If the phy both transmits and receives COMSAS (i.e., a SAS phy or expander phy is attached), then the transmitter device shall set its transmit levels to the SAS signal output levels (see 5.7.4.4, 5.7.4.5, and 5.7.4.6) prior to beginning the SAS speed negotiation sequence (see SPL). If transmitter device had been using SATA Gen1i, Gen2i, or Gen3i signal output levels, this mode transition (i.e., output voltage change) may result in a transient (see 5.7.2) during the idle time between COMSAS and the SAS speed negotiation sequence.

If the transmitter device is using SAS signal output levels and the phy does not receive COMSAS (i.e., a SATA phy is attached), then the transmitter device shall set its transmit levels to the SATA Gen1i, Gen2i, or Gen3i signal output levels and restart the OOB sequence.

Transmitter devices that do not support SATA or that have optical mode enabled shall transmit OOB signals using SAS signal output levels. In low phy power conditions (see SPL) the output common mode specification OOB common mode delta (see table 37) is relaxed to enable transmitter device power savings. During low phy power conditions, the transmitter device should reduce its output swing level to save power. Before exiting a low phy power condition the transmitter device shall wait for its common mode to settle.

Table 37 defines the transmitter device signal output characteristics for OOB signals.

Table 37 — Transmitter device signal output characteristics for OOB signals

Characteristic	Units	IT	CT
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 104) [a]	mV(P-P)	1 600	
OOB offset delta [b] [c]	mV	± 25	
OOB common mode delta [c] [d]	mV	± 50	
Minimum OOB burst amplitude [e], if SATA is not supported	mV(P-P)	240 [f]	
Minimum OOB burst amplitude [e], if SATA is supported	mV(P-P)	240 [f] [g]	N/A

[a] The recommended maximum peak to peak voltage is 1 200 mV(P-P).
[b] The maximum difference in the average differential voltage (D.C. offset) component between the burst times and the idle times of an OOB signal.
[c] This is not applicable when optical mode is enabled or in low phy power conditions.
[d] The maximum difference in the average of the common-mode voltage between the burst times and the idle times of an OOB signal.
[e] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst as measured with each test load at IT and CT.
[f] The OOB burst contains either 1.5 Gbit/s repeating 0011b or 1100b pattern (e.g., D24.3), 1.5 Gbit/s ALIGN (0) primitives, or 3 Gbit/s ALIGN (0) primitives (see SPL and SATA).
[g] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.7.5 Receiver device characteristics

5.7.5.1 Receiver device characteristics overview

The receiver device shall operate within the required BER (see 5.5.1) when a signal with valid voltage and timing characteristics is delivered to the receiver device compliance point from a nominal 100 Ω source. The received signal shall be considered valid if it meets the voltage and timing limits specified in table 40 (see 5.7.5.4) for untrained 1.5 Gbit/s and 3 Gbit/s and table 44 (see 5.7.5.7.1) for trained 1.5 Gbit/s, 3 Gbit/s, and
6 Gbit/s. See SATA for untrained 6 Gbit/s (i.e., SATA Gen3i) receiver device requirements.

Additionally, for untrained 1.5 Gbit/s and 3 Gbit/s the receiver device shall operate within the required BER when the signal has additional SJ present as specified in table 42 (see 5.7.5.6) with the common-mode signal V_{CM} as specified in table 38 (see 5.7.1). Jitter tolerance for receiver device compliance points is shown in figure 106 (see 5.7.3.5). Figure 106 assumes that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver device, the additional 0.1 UI of SJ may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiver device. The additional jitter reduces the eye opening in both voltage and time. For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, the additional jitter and common mode voltage is included in the stressed receiver device jitter tolerance test (see 5.7.5.7.4).

See clause D.9 for a methodology for measuring receiver device signal tolerance.

Receiver device implementation is vendor specific. A receiver device shall provide equivalent performance to the reference receiver device (see 5.7.5.7.3) and shall operate within the required BER when attached to:

a) any transmitter device compliant with this standard (see 5.7.4); and
b) any TxRx connection compliant with this standard (see 5.5).

5.7.5.2 Receiver device A.C. coupling requirements

AC coupling requirements for receiver devices are as follows:

a) all receiver devices (i.e., attached to IR or CR compliance points) shall be A.C. coupled to the interconnect through a receive network.

See table 26 (see 5.7.1) for the coupling capacitor value.

5.7.5.3 Receiver device general electrical characteristics

Table 38 defines the receiver device general electrical characteristics.

Table 38 — Receiver device general electrical characteristics

Characteristic	Units	1.5 Gbit/s	3 Gbit/s	6 Gbit/s
Physical link rate long-term tolerance at IR if SATA is not supported	ppm	± 100		
Physical link rate long-term tolerance at IR if SATA is supported	ppm	± 350		
Physical link rate SSC modulation tolerance at IR	ppm	See table 54 in 5.7.6.3		
Maximum receiver device transients [a]	V	± 1.2		
Minimum receiver A.C. common-mode voltage tolerance V_{CM} [b]	mV(P-P)	150		
Receiver A.C. common-mode frequency tolerance range F_{CM} [b c]	MHz	2 to 200		2 to 3 000

[a] See 5.7.2 for transient test circuits and conditions.
[b] Receiver devices shall tolerate sinusoidal common-mode noise components within the peak-to-peak amplitude (V_{CM}) and the frequency range (F_{CM}).
[c] The measurement shall be made with a channel equivalent to the channel used in the zero-length test load (see figure 90) (see 5.6.2).

Table 39 defines the receiver device termination characteristics.

Table 39 — Receiver device termination characteristics

Characteristic	Units	Untrained		Trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s
		1.5 Gbit/s	3 Gbit/s	
Differential impedance [a b c]	Ω	100 ± 15		See 5.7.5.7.1
Maximum differential impedance imbalance [a b c d]	Ω	5		See 5.7.5.7.2 [e]
Maximum receiver termination time constant [a b c]	ps	150	100	N/A
Common-mode impedance [a b]	Ω	20 minimum 40 maximum		See 5.7.5.7.1

[a] All receiver device termination measurements are made through mated connector pairs.

[b] The receiver device termination impedance specification applies to all receiver devices in a TxRx connection and covers all time points between the connector nearest the receiver device, the receiver device, and the transmission line terminator. This measurement shall be made from that connector.

[c] At the time point corresponding to the connection of the receiver device to the transmission line, the input capacitance of the receiver device and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. With impedance measured using amplitude in units of ρ (i.e., the reflection coefficient, a dimensionless unit) and duration in units of time, the area of the impedance dip caused by this capacitance is the receiver termination time constant. The receiver termination time constant shall not be greater than the values shown in this table.

An approximate value for the receiver termination time constant is given by the following equation:

$$\text{RTTC} = \text{amp} \times \text{width}$$

where:

RTTC receiver termination time constant in seconds;
amp amplitude of the dip in units of ρ (i.e., the difference between the reflection coefficient at the nominal impedance and the reflection coefficient at the minimum impedance point); and
width width of the dip in units of time, as measured at the half amplitude point.

The value of the receiver device excess input capacitance is given by the following equation:

$$C = \frac{\text{RTCC}}{(R_0 \parallel R_R)}$$

where:

C receiver device excess input capacitance in farads;
R*TCC* receiver termination time constant in seconds;
R_0 transmission line characteristic impedance in Ωs;
R_R termination resistance at the receiver device in Ωs; and
$(R_0 \parallel R_R)$ parallel combination of R_0 and R_R.

[d] The difference in measured impedance to SIGNAL GROUND on the plus and minus terminals on the interconnect, transmitter device, or receiver device, with a differential test signal applied to those terminals.

[e] Measurement replaced by S_{CD11} specifications (i.e., differential to common mode conversion).

5.7.5.4 Delivered signal characteristics for untrained 1.5 Gbit/s and 3 Gbit/s

Table 40 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.6.2) at the receiver device compliance point (i.e., IR or CR) for untrained 1.5 Gbit/s and 3 Gbit/s. These also serve as the required signal tolerance characteristics of the receiver device. For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, see 5.7.5.7.

Table 40 — Delivered signal characteristics for untrained 1.5 Gbit/s and 3 Gbit/s as measured with the zero length test load at IR and CR

Signal characteristic	Units	IR, untrained		CR, untrained	
		1.5 Gbit/s	3 Gbit/s	1.5 Gbit/s	3 Gbit/s
Maximum voltage (non-operational)	mV(P-P)	2 000			
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 105) if a SATA phy is not attached	mV(P-P)	1 600		1 600	
Maximum peak to peak voltage (i.e., 2 × Z2 in figure 105) if a SATA phy is attached	mV(P-P)	see SATA [a]		N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 105), if a SATA phy is not attached	mV(P-P)	325	275	275	
Minimum eye opening (i.e., 2 × Z1 in figure 105), if a SATA phy using Gen1i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.6.3)	mV(P-P)	225 [a]	N/A	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 105), if a SATA phy using Gen2i levels is attached and the TxRx connection is characterized with the TCTF test load (see 5.6.3)	mV(P-P)	N/A	175 [a]	N/A	
Minimum eye opening (i.e., 2 × Z1 in figure 105), if a SATA phy is attached and the TxRx connection is characterized with the low-loss TCTF test load (see 5.6.4)	mV(P-P)	275 [a]		N/A	
Jitter tolerance (see figure 106 in 5.7.3.5) [b] [c]	N/A	See table 42 in 5.7.5.6			
Maximum half of TJ (i.e., X1 in figure 105) [d]	UI	0.275			
Center of bit time (i.e., X2 in figure 105)	UI	0.50			
Maximum intra-pair skew [e]	ps	80	75	80	75

[a] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

[b] The value for X1 applies at a TJ probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter requirements.

[c] SSC shall be enabled if the receiver device supports being attached to SATA. Jitter setup shall be performed prior to application of SSC.

[d] The value for X1 shall be half the value given for TJ in table 41. When SSC is disabled, the test or analysis shall include the effects of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of (f_{baud} / 1 667).

[e] The intra-pair skew measurement shall be made at the midpoint of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL) on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Rx+ and Rx- signals. Intra-pair skew is defined as the time difference between the means of the midpoint crossing times of the Rx+ signal and the Rx- signal at the probe points.

5.7.5.5 Maximum delivered jitter for untrained 1.5 Gbit/s and 3 Gbit/s

Table 41 defines the maximum jitter the system shall deliver to the receiver device at the receiver device compliance point (i.e., IR or CR) for untrained 1.5 Gbit/s and 3 Gbit/s. For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, see 5.7.5.7.4.

Table 41 — Maximum delivered jitter for untrained 1.5 Gbit/s and 3 Gbit/s at IR and CR

Signal characteristic [a] [b]	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Deterministic jitter (DJ) [c]	UI	0.35	
Total jitter (TJ) [c] [d] [e]	UI	0.55	

[a] All DJ and TJ values are level 1 (see MJSQ).
[b] The values for jitter in this table are measured at the average signal amplitude point.
[c] The DJ and TJ values in this table apply to jitter measured as described in 5.7.3.3. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.
[d] TJ is specified at a CDF level of 10^{-12}.
[e] If TJ received at any point is less than the maximum allowed, then the jitter distribution of the signal is allowed to be asymmetric. The TJ plus the magnitude of the asymmetry shall not exceed the allowed maximum TJ. The numerical difference between the average of the peaks with a BER that is less than 10^{-12} and the average of the individual events is the measure of the asymmetry.
Jitter peak-to-peak measured < (maximum TJ - |Asymmetry|)

5.7.5.6 Receiver device jitter tolerance for untrained 1.5 Gbit/s and 3 Gbit/s

Table 42 defines the amount of jitter the receiver device shall tolerate at the receiver device compliance point (i.e., IR or CR) for untrained 1.5 Gbit/s and 3 Gbit/s. Receiver device jitter testing shall be performed with the maximum (i.e., slowest) rise/fall times, minimum signal amplitude, and maximum TJ, and should be performed with normal activity in the receiver device (e.g., with other transmitter circuits and receiver circuits on the same board as the receiver device performing normal activity) with SSC enabled if SSC is supported by the receiver device. Jitter setup shall be performed prior to application of SSC. For trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s, see 5.7.5.7.4.

Table 42 — Receiver device jitter tolerance for untrained 1.5 Gbit/s and 3 Gbit/s at IR and CR

Signal characteristic	Units	Untrained	
		1.5 Gbit/s	3 Gbit/s
Applied sinusoidal jitter (SJ) from f_c to f_{max} [a]	UI	0.10 [e]	0.10 [f]
Deterministic jitter (DJ) [b c]	UI	0.35 [g]	0.35 [h]
Total jitter (TJ) [b c d]	UI	0.65	

[a] The jitter values given are normative for a combination of applied SJ, DJ, and TJ that receiver devices shall be able to tolerate without exceeding the required BER (see 5.5.1). Receiver devices shall tolerate applied SJ of progressively greater amplitude at lower frequencies than f_c, according to figure 112, with the same DJ and RJ levels as were used from f_c to f_{max}.

[b] All DJ and TJ values are level 1 (see MJSQ).

[c] The DJ and TJ values in this table apply to jitter measured as described in 5.7.3.4. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the calculation of level 1 jitter compliance levels method in MJSQ.

[d] No value is given for RJ. For compliance with this standard, the actual RJ amplitude shall be the value that brings TJ to the stated value at a probability of 10^{-12}. The additional 0.1 UI of applied SJ is added to ensure the receiver device has sufficient operating margin in the presence of external interference.

[e] Applied sinusoidal swept frequency for 1.5 Gbit/s: 900 kHz to 5 MHz.

[f] Applied sinusoidal swept frequency for 3 Gbit/s: 1 800 kHz to 7.5 MHz.

[g] The measurement bandwidth for 1.5 Gbit/s shall be 900 kHz to 750 MHz.

[h] The measurement bandwidth for 3 Gbit/s shall be 1 800 kHz to 1 500 MHz.

Figure 112 defines the applied SJ for table 42.

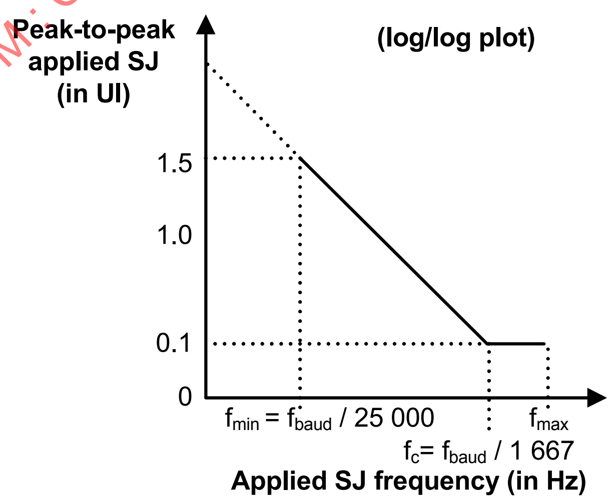


Figure 112 — Applied SJ for untrained 1.5 Gbit/s and 3 Gbit/s

Table 43 defines f_{min}, f_c, and f_{max} for figure 112. f_{baud} is defined in table 26 (see 5.7.1).

Table 43 — f_{min}, f_c, and f_{max} for untrained 1.5 Gbit/s and 3 Gbit/s

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbit/s	60 kHz	900 kHz	5 MHz
3 Gbit/s	120 kHz	1 800 kHz	7.5 MHz

5.7.5.7 Receiver device and delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

5.7.5.7.1 Delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s

Table 44 specifies the requirements of the signal delivered by the system with the zero-length test load (see 5.6.2), unless otherwise specified, attached at the receiver device compliance point (i.e., IR or CR) for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s. These also serve as the required signal tolerance characteristics of the receiver device. All specifications are based on differential measurements.

Table 44 — Delivered signal characteristics for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s at IR and CR

Characteristic	Units	Minimum	Nominal	Maximum
Peak to peak voltage for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s [a] [b]	mV(P-P)			1 200
Non-operational input voltage	mV(P-P)			2 000
Reference differential impedance [c]	Ω		100	
Reference common mode impedance [c]	Ω		25	

[a] See 5.7.4.6.6 for measurement method.
[b] During OOB, SNW-1, SNW-2, and SNW-3 (see SPL), the untrained 1.5 Gbit/s and 3 Gbit/s specifications in 5.7.5.4 apply.
[c] For receiver device S-parameter characteristics, see 5.7.5.7.2.

5.7.5.7.2 Receiver device S-parameter limits

S-parameter limits are calculated per the following formula:

$$\text{Measured value} < \max [\, L, \min [\, H, N + 13.3 \times \log_{10}(f / 3\ \text{GHz}) \,] \,]$$

where:

- L is the minimum value (i.e., the low frequency asymptote);
- H is the maximum value (i.e., the high frequency asymptote);
- N is the value at the Nyquist frequency (i.e., 3 GHz);
- f is the frequency of the signal in Hz;
- max [A, B] is the maximum of A and B; and
- min [A, B] is the minimum of A and B.

Table 45 defines the maximum limits for S-parameters of the receiver device.

Table 45 — Maximum limits for S-parameters at IR or CR

Characteristic [a]	L [b] (dB)	N [b] (dB)	H [b] (dB)	S [b] (dB / decade)	f_{min} [b] (MHz)	f_{max} [b] (GHz)
$\|S_{CC11}\|$	-6.0	-5.0	0	13.3	100	6.0
$\|S_{DD11}\|$	-10	-7.9	0	13.3	100	6.0
$\|S_{CD11}\|$	-26	-12.7	-10	13.3	100	6.0

[a] $|S_{DC11}|$ is not specified.
[b] See figure 4 in 5.2 for definitions of L, N, H, S, f_{min}, and f_{max}.

Figure 113 shows the receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in table 45.

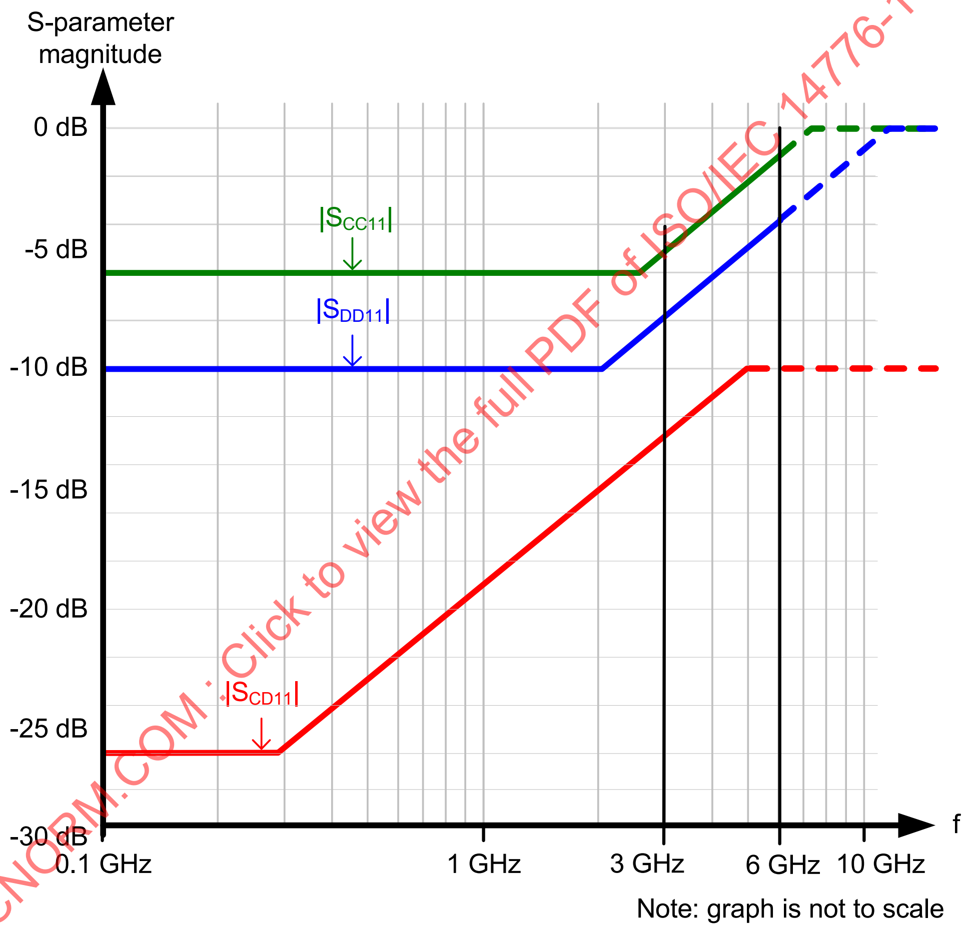


Figure 113 — Receiver device $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits

5.7.5.7.3 Reference receiver device characteristics

The reference receiver device is a set of parameters defining the electrical performance characteristics of a receiver device used in simulation to:

a) determine compliance of a transmitter device (see 5.7.4.6); and
b) determine compliance of a TxRx connection (see 5.5.5).

Figure 114 shows a reference receiver device.

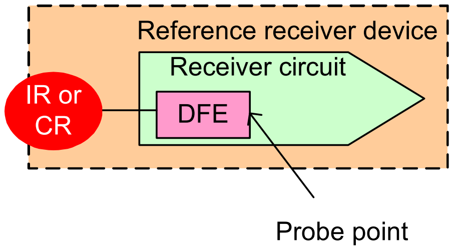


Figure 114 — Reference receiver device

The reference receiver device includes a 3 tap DFE with infinite precision taps and unit interval tap spacing. The reference coefficient adaptation algorithm is the LMS algorithm. The DFE may be modeled at the center of the eye as:

$$y_k = x_k - \sum_{i=1}^{3} d_i \times \text{sgn}(y_{k-i})$$

where:

y	equalizer differential output voltage;
x	equalizer differential input voltage;
d	equalizer feedback coefficient; and
k	sample index in *UI*.

The reference receiver device equalizer feedback coefficients (i.e., d_i) have absolute magnitudes that are less than 0.5 times the peak of the equivalent pulse response of the reference receiver device.

NOTE 9 For more information on DFE and LMS, see John R. Barry, Edward A. Lee, and David G. Messerschmitt. *Digital Communication - Third Edition*. Kluwer Academic Publishing, 2003. See http://users.ece.gatech.edu/~barry/digital.

The following Touchstone model of the reference receiver device termination is included with this standard:

a) SAS2_RxRefTerm.s4p.

Figure 115 shows the S-parameters of the reference receiver device termination model.

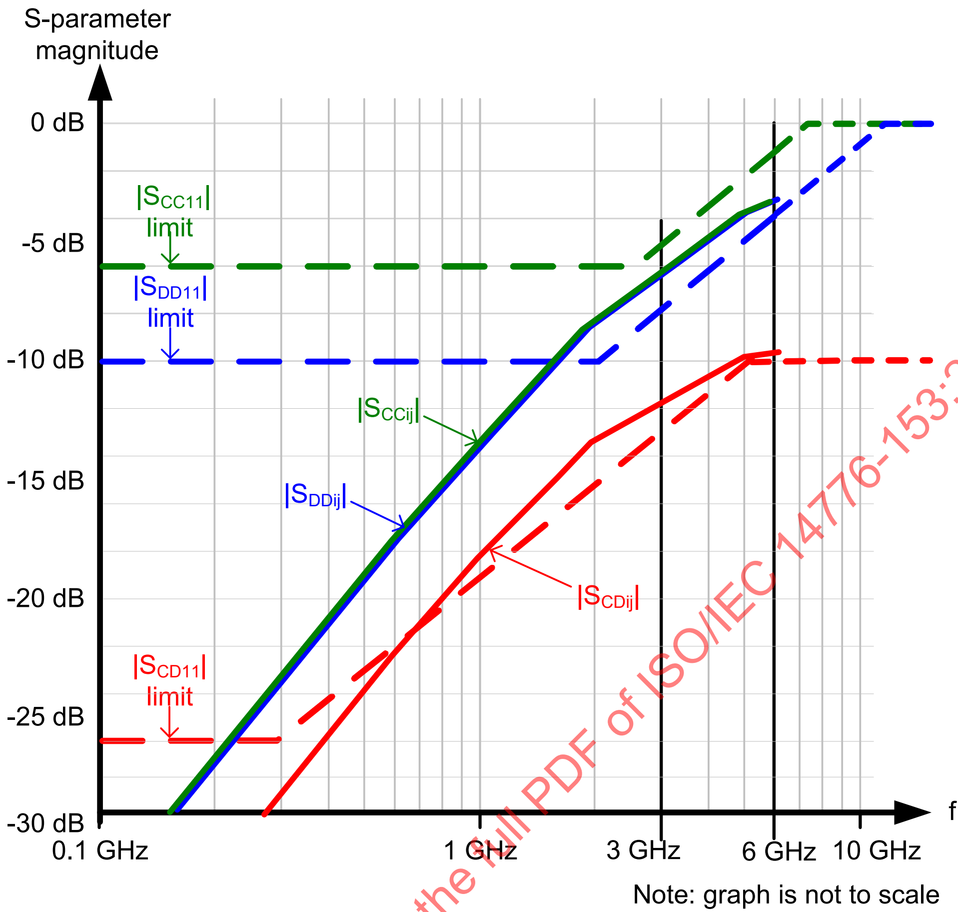


Figure 115 — Reference receiver device termination S-parameters

The Touchstone model does not exactly match the $|S_{CC11}|$, $|S_{DD11}|$, and $|S_{CD11}|$ limits defined in 5.7.5.7.2 at all frequencies; it is a reasonable approximation for use in simulations. See Annex E for a description of how the Touchstone model was created.

5.7.5.7.4 Stressed receiver device jitter tolerance test

5.7.5.7.4.1 Stressed receiver device jitter tolerance test overview

A receiver device shall pass the stressed receiver device jitter tolerance test described in this subclause.

The stressed receiver device jitter tolerance test shall be applied at the receiver device compliance point (i.e., IR or CR) as a means to perform physical validation of predicted performance of the receiver device. Any implementation of the stressed signal generation hardware is permitted for the stressed receiver signal as long as it provides the ISI-stressed signal with jitter and noise as defined in this subclause.

Figure 116 shows the block diagram of the stressed receiver device jitter tolerance test.

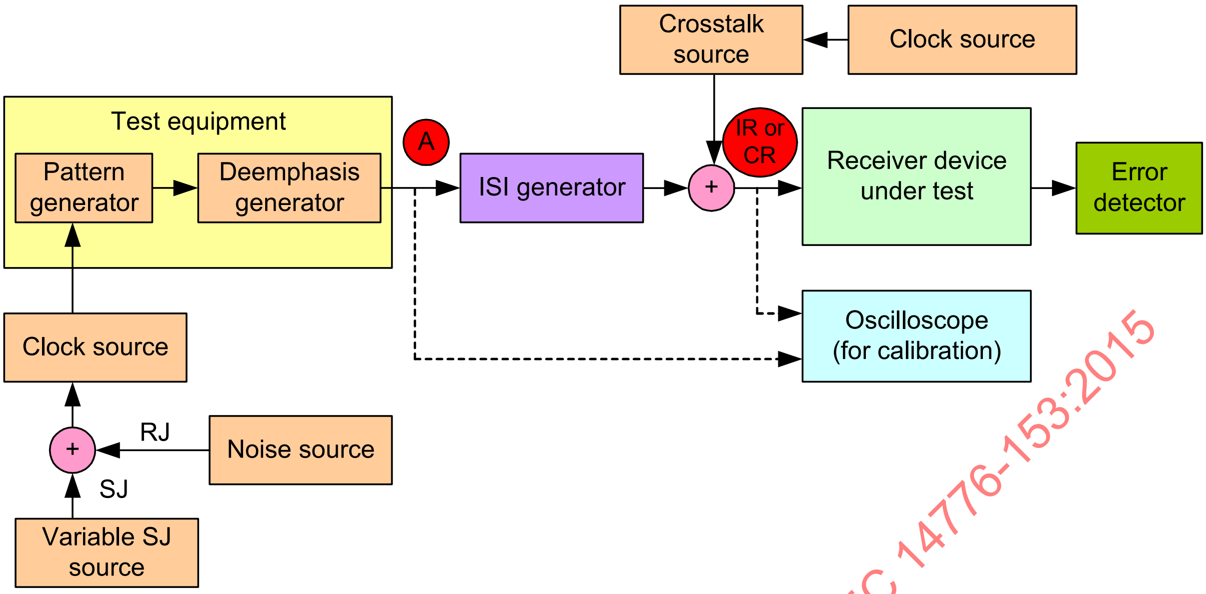


Figure 116 — Stressed receiver device jitter tolerance test block diagram

The ISI generator shall be representative of, and at least as stressful as, the reference transmitter test load (see 5.6.5). The reference transmitter test load (see 5.6.5), with a nominal $|S_{DD21}|$ of -15 dB at (f_{baud} / 2), may be used as a component of the ISI generator.

The receiver device under test demonstrates its ability to compensate for channel intersymbol interference (ISI) representative of the reference transmitter test load (see 5.6.5) while subjected to the budgeted jitter and crosstalk sources.

Table 46 defines the stressed receiver device jitter tolerance test characteristics. Unless otherwise noted, characteristics are measured at IR or CR in figure 116.

Table 46 — Stressed receiver device jitter tolerance test characteristics

Characteristic	Units	Minimum	Nominal	Maximum	Reference
Tx peak to peak voltage [a]	mV(P-P)		850		5.7.4.6.1
Transmitter equalization [a]	dB		2		5.7.4.6.6
Tx RJ [b c d]	UI	0.135 [e]	0.150 [f]	0.165 [g]	5.7.4.6.1
Tx SJ [c]	UI	See figure 118 and figure 119			5.7.5.7.4.5
WDP at 6 Gbit/s [b h]	dB	13		14.5	
WDP at 3 Gbit/s [b h]	dB	7		8.5	
WDP at 1.5 Gbit/s [b h]	dB	4.5		6	
D24.3 eye opening [b i]	mV(P-P)	200	215	230	5.7.3.4
NEXT offset frequency [i j k]	ppm	2 500			
Total crosstalk amplitude [i k]	mV_{rms}	4			
Receiver device configuration [l]					

[a] For a characteristic with only a nominal value, the test setup shall be configured to be as close to that value as possible while still complying with other characteristics in this table.
[b] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.
[c] Measured at point A in figure 116.
[d] Measured after application of the JTF (see 5.7.3.2).
[e] 0.135 UI is 22.5 ps at 6 Gbit/s, 45 ps at 3 Gbit/s, and 90 ps at 1.5 Gbit/s.
[f] 0.150 UI is 25 ps at 6 Gbit/s, 50 ps at 3 Gbit/s, and 100 ps at 1.5 Gbit/s.
[g] 0.165 UI is 27.5 ps at 6 Gbit/s, 55 ps at 3 Gbit/s, and 110 ps at 1.5 Gbit/s.
[h] This value is obtained by simulation with SASWDP (see Annex B). BUJ and RJ shall be minimized for WDP simulations. The WDP value is a characterization of the signal output within the reference receiver device (see 5.7.5.7.3) after equalization.
[i] The repeating 0011b or 1100b pattern (e.g., D24.3) eye opening pertains to the delivered signal at IR or CR. Figure 117 defines this value in an eye diagram.
[j] The NEXT source may use SSC modulation rather than have a fixed offset frequency.
[k] Observed with a histogram of at least 1 000 samples. Additional pseudo-random crosstalk shall be added, if needed, to meet the total crosstalk amplitude specification.
[l] All transmitter devices and receiver devices adjacent to the receiver device under test shall be active with representative traffic with their maximum amplitude and maximum frequency of operation.

Figure 117 shows the stressed receiver device jitter tolerance test repeating 0011b or 1100b pattern (e.g., D24.3) eye opening.

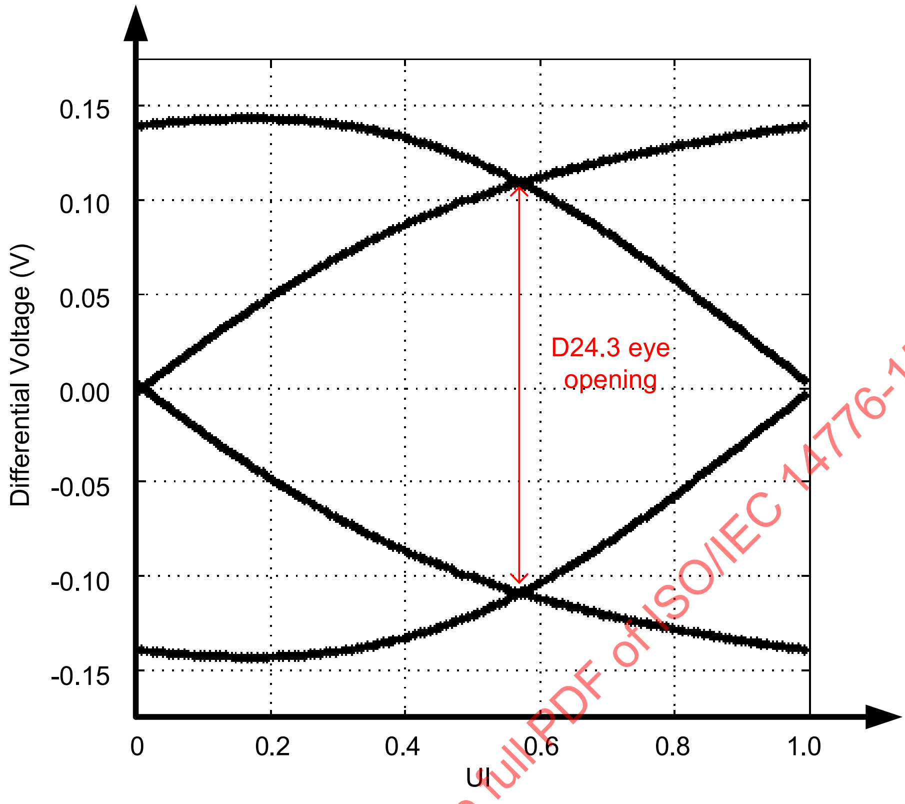


Figure 117 — Stressed receiver device jitter tolerance test D24.3 eye opening

5.7.5.7.4.2 Stressed receiver device jitter tolerance test procedure

The stressed receiver device jitter tolerance test procedure is as follows:

1) calibrate the test equipment and ISI generator as specified in 5.7.5.7.4.3;
2) calibrate the crosstalk source as specified in 5.7.5.7.4.4;
3) attach the test equipment and ISI generator and the crosstalk source to the receiver device under test;
4) configure the applied SJ as specified in 5.7.5.7.4.5;
5) configure the pattern generator to transmit CJTPAT (see Annex A); and
6) ensure that the receiver device under test has a BER that is less than 10^{-12} with a confidence level of 95 %.

Table 47 defines the number of bits that shall be received with a certain number of errors to have a confidence level of 95 % that the BER is less than 10^{-12}.

Table 47 — Number of bits received per number of errors for desired BER

Number of errors	Number of bits
0	3.00×10^{12}
1	4.74×10^{12}
2	6.30×10^{12}
3	7.75×10^{12}
4	9.15×10^{12}
5	1.05×10^{13}

5.7.5.7.4.3 Test equipment and ISI generator calibration

The test equipment and ISI generator calibration procedure is as follows:

1) ensure that the ISI generator has an $|S_{DD21}|$ comparable to that of the reference transmitter test load (see 5.6.5). $|S_{DD21}|$ delivered by the ISI generator shall be measured by observing the D24.3 eye opening at IR or CR as defined in table 46;
2) attach the test equipment and ISI generator to a zero-length test load, where its signal output is captured by an oscilloscope;
3) disable the crosstalk source;
4) disable the variable SJ source and the random noise source;

NOTE 10 WDP values computed by SASWDP are influenced by all sources of eye closure including DCD, BUJ, and ISI, and increased variability in results may occur due to increases in those sources other than ISI.

5) configure the pattern generator to transmit the SCRAMBLED_0 pattern (see the phy test patterns in the Protocol-Specific diagnostic page in SPL);
6) capture at least 58 dwords (i.e., 2 320 bits on the physical link). Waveform averaging shall be used to minimize the impact of measurement noise and jitter on the WDP calculations;
7) input the captured pattern into SASWDP simulation (see Annex B) with the usage variable set to 'SAS2_LDP'; and
8) adjust the ISI generator until the WDP is within the range defined in table 46 (see 5.7.5.7.4.1).

5.7.5.7.4.4 Crosstalk source calibration

The crosstalk source calibration procedure is as follows:

1) attach the test equipment and ISI generator and the crosstalk source to a zero-length test load, where its signal output is captured by an oscilloscope;
2) disable the pattern generator;
3) enable the crosstalk source;
4) set the center frequency of the crosstalk source to be frequency offset from the pattern generator to sweep all potential relative phase alignments between the crosstalk source and the signal from the ISI generator;
5) generate a histograph of the signal delivered to the test equipment; and
6) adjust the crosstalk source until the crosstalk amplitude complies with table 46 (see 5.7.5.7.4.1).

5.7.5.7.4.5 Applied SJ

Figure 118 defines the applied SJ for trained receiver devices that do not support SSC.

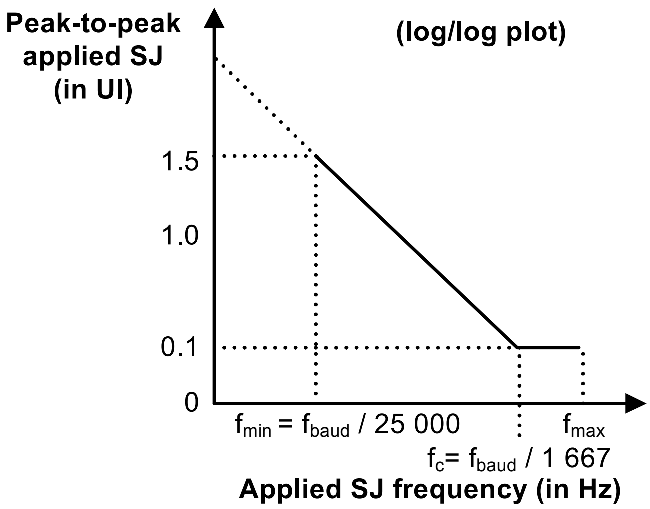


Figure 118 — Applied SJ for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s without SSC support

Table 48 defines f_{min}, f_c, and f_{max} for figure 118. f_{baud} is defined in table 26 (see 5.7.1).

Table 48 — f_{min}, f_c, and f_{max} for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s without SSC support

Physical link rate	f_{min}	f_c	f_{max}
1.5 Gbit/s	60 kHz	900 kHz	5 MHz
3 Gbit/s	120 kHz	1 800 kHz	7.5 MHz
6 Gbit/s	240 kHz	3 600 kHz	15 MHz

Figure 119 defines the applied SJ for trained receiver devices that support SSC.

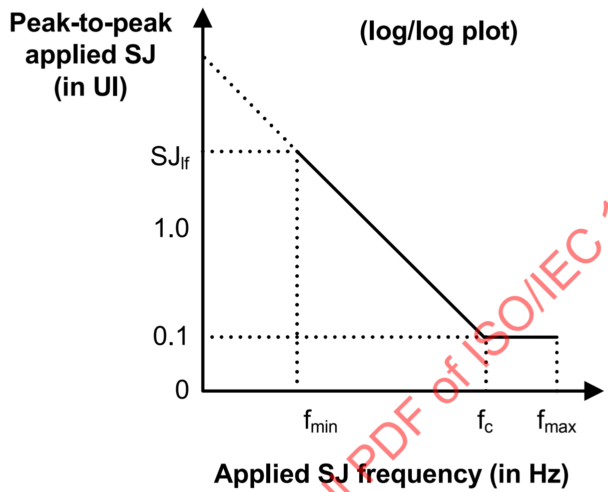


Figure 119 — Applied SJ for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s with SSC support

Table 49 defines f_{min}, f_c, f_{max}, and SJ_{lf} for figure 119.

Table 49 — f_{min}, f_c, f_{max}, and SJ_{lf} for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s with SSC support

Physical link rate	f_{min}	f_c	f_{max}	SJ_{lf}
1.5 Gbit/s	97 kHz	1.03 MHz	5 MHz	11.3 UI
3 Gbit/s	97 kHz	1.46 MHz	7.5 MHz	22.6 UI
6 Gbit/s	97 kHz	2.06 MHz	15 MHz	45.3 UI

5.7.5.8 Delivered signal characteristics for OOB signals

Table 50 defines the amplitude requirements of the OOB signal delivered by the system with the zero-length test load (see 5.6.2) at the receiver device compliance point (i.e., IR or CR). These also serve as the required signal tolerance characteristics of the receiver device.

Table 50 — Delivered signal characteristics for OOB signals

Characteristic	Units	IR	CR
Minimum OOB burst amplitude [a], if SATA is not supported	mV(P-P)	240 [b]	
Minimum OOB burst amplitude [a], if SATA is supported	mV(P-P)	225 [c d]	N/A

[a] With a measurement bandwidth of 4.5 GHz, each signal level during the OOB burst shall exceed the specified minimum differential amplitude before transitioning to the opposite bit value or before termination of the OOB burst.

[b] The OOB burst contains either 1.5 Gbit/s repeating 0011b or 1100b pattern (e.g., D24.3), 1.5 Gbit/s ALIGN (0) primitives, or 3 Gbit/s ALIGN (0) primitives (see SPL).

[c] The OOB burst contains either 1.5 Gbit/s repeating 0011b or 1100b pattern (e.g., D24.3) or 1.5 Gbit/s ALIGN (0) primitives (see SPL and SATA).

[d] Amplitude measurement methodologies of SATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies used in this standard may indicate less signal amplitude than the technique specified by SATA. Implementers of designs supporting SATA are required to ensure interoperability and should perform additional system characterization with an eye diagram methodology using SATA devices.

5.7.6 Spread spectrum clocking (SSC)

5.7.6.1 SSC overview

Spread spectrum clocking (SSC) is the technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions.

Phys transmit with SSC as defined in 5.7.6.2 and receive with SSC as defined in 5.7.6.3.

Table 51 defines the SSC modulation types.

Table 51 — SSC modulation types

SSC modulation type	Maximum SSC frequency deviation (SSC_{tol}) [a]
Center-spreading	+2 300 / -2 300 ppm
No-spreading	+0 / -0 ppm
Down-spreading	+0 / -2 300 ppm
SATA down-spreading [b]	+0 / -5 000 ppm

[a] This is in addition to the physical link rate long-term stability and tolerance defined in table 28 and table 38 (see 5.7.1).

[b] This is only used as a receiver parameter.

A phy may be transmitting with a different SSC modulation type than it is receiving (e.g., a phy is transmitting with center-spreading while it is receiving with down-spreading).

If the SSC modulation type is not no-spreading, then the phy shall transmit within the specified maximum SSC frequency deviation with an SSC modulation frequency that is a minimum of 30 kHz and a maximum of 33 kHz.

The SSC modulation profile (e.g., triangular) is vendor specific, but should provide the maximum amount of electromagnetic interference (EMI) reduction. For center-spreading, the average amount of up-spreading (i.e., > 0 ppm) in the SSC modulation profile shall be the same as the average amount of down-spreading (i.e., < 0 ppm). The amount of asymmetry in the SSC modulation profile shall be less than 288 ppm.

NOTE 11 288 ppm is the rate of deletable primitives (see SPL) that are left over after accounting for the physical link rate long-term stability. It is calculated as the deletable primitive rate defined in the SAS standard of 1/2 048 (i.e., 488 ppm) minus the width between the extremes of the physical link rate long-term stability of +100/-100 ppm (i.e., 200 ppm).

SSC-induced jitter is included in TJ at the transmitter output.

The slope of the frequency deviation should not exceed 850 ppm/µs when computed over any 0.27 ± 0.01 µs interval of the SSC modulation profile, after filtering of the transmitter device jitter output by a single-pole low-pass filter with a cutoff frequency of 3.7 ± 0.2 MHz. Alternatively, the transmitter device jitter may be filtered by the closed-loop transfer function of a measurement equipment's PLL that is compliant with the JTF.

The slope is computed from the difference equation:

slope = (f(t) - f(t - 0.27 µs)) / 0.27 µs

where:

f(*t*) is the SSC frequency deviation expressed in ppm.

A ± 2 300 ppm triangular SSC modulation profile has a slope of approximately 310 ppm/µs and meets the informative slope specification. Other SSC modulation profiles (e.g., exponential) may not meet the slope requirement. A modulation profile that has a slope of ± 850 ppm/µs over 0.27 µs creates a residual jitter of approximately 16.7 ps (i.e., 0.10 UI at 6 Gbit/s) after filtering by the JTF. This consumes the total BUJ budget of the transmitter device, which does not allow the transmitter device to contribute any other type of BUJ.

Activation or deactivation of SSC on a physical link that is not OOB idle or negotiation idle (see SPL) shall be done without violating TJ at the transmitter device output after application of the JTF.

5.7.6.2 Transmitter SSC modulation

A SAS phy transmits with the SSC modulation types defined in table 52.

Table 52 — SAS phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Required	Optional
While attached to a phy that does not support SSC	No-spreading	
While attached to a phy that supports SSC	No-spreading	Down-spreading

[a] SAS phys compliant with versions of SAS standards previous to SAS-2 only transmitted with an SSC modulation type of no-spreading.

An expander phy transmits with the SSC modulation types defined in table 53.

Table 53 — Expander phy transmitter SSC modulation types

Condition	SSC modulation type(s) [a]	
	Required	Optional
While attached to a SAS phy or expander phy that does not support SSC	No-spreading	
While attached to a SAS phy or expander phy that supports SSC	No-spreading	Center-spreading
While attached to a SATA phy	No-spreading	Down-spreading

[a] Expander phys compliant with versions of SAS standards previous to SAS-2 only transmitted with an SSC modulation type of no-spreading.

A SAS device (see SPL) or expander device (see SPL) should provide independent control of SSC on each transmitter device. However, it may implement a common SSC transmit clock in which multiple transmitter devices do not have independent controls to enable and disable SSC. In such implementations, SSC may be disabled on a transmitter device that is already transmitting with SSC enabled if another transmitter device sharing the same common SSC transmit clock is required to perform SNW-1, SNW-2, SNW-3, or Final-SNW (see SPL) or SAS speed negotiation (see SPL).

If any transmitter device sharing a common SSC transmit clock enters a non-SSC transmission state (e.g., SNW-1, SNW-2, Final-SNW, or Train-SNW with SSC disabled (see SPL)), then any transmitter device sharing that common SSC transmit clock may disable SSC. These transmitter devices are compliant with the SSC requirements even if the transmitter device has negotiated SSC enabled but its transmit clock has SSC disabled, provided that the transmitted signal does not exceed the maximum SSC frequency deviation limits specified in table 51.

The disabling and enabling of SSC may occur at any time (see 5.7.6.1) except during SNW-1, SNW-2, and Final-SNW (see SPL).

5.7.6.3 Receiver SSC modulation tolerance

SAS phys and expander phys support (i.e., tolerate) receiving with SSC modulation types defined in table 54.

Table 54 — Receiver SSC modulation types tolerance

Type of phys	SSC modulation type(s) [a] [b]	
	Required	Optional [c]
Phys that support being attached to SATA phys	No-spreading and SATA down-spreading	Center-spreading and down-spreading
Phys that do not support being attached to SATA phys	No-spreading	Center-spreading and down-spreading

[a] This is in addition to the physical link rate long-term tolerance defined in table 38 (see 5.7.1).
[b] Phys compliant with versions of SAS standards previous to SAS-2 that do not support being attached to SATA devices were only required to tolerate an SSC modulation type of no-spreading. Phys compliant with versions of SAS standards previous to SAS-2 that support being attached to SATA devices were only required to tolerate SSC modulation types of no-spreading and SATA down-spreading.
[c] If either the SSC modulation type of center-spreading or down-spreading is supported, then both shall be supported.

5.7.6.4 Expander device center-spreading tolerance buffer

Expander devices supporting the SSC modulation type of center-spreading shall support a center-spreading tolerance buffer for each connection with the buffer size defined in table 55. The expander device uses this buffer to hold any dwords that it receives during the up-spreading portion(s) of the SSC modulation period that it is unable to forward because the ECR (see SPL) and/or the transmitting expander phy is slower than the receiving expander phy and because the dword stream does not include enough deletable primitives (see SPL). The expander device unloads the center-spreading tolerance buffer during the down-spreading portion(s) of the SSC modulation period when the receiving expander phy is slower than the ECR and the transmitting expander phy.

Table 55 — Expander device center-spreading tolerance buffer

Physical link rate	Minimum buffer size
6 Gbit/s	14 dwords
3 Gbit/s	8 dwords
1.5 Gbit/s	4 dwords

NOTE 12 The minimum buffer size is based on the number of dwords that may be transmitted during half of the longest allowed SSC modulation period (i.e., half of the period indicated by 30 kHz) at the maximum physical link rate (i.e., +2 400 ppm) minus the number that may be transmitted at the minimum physical link rate (i.e., -2 400 ppm). This accounts for forwarding dwords in a connection (see SPL) that originated from a phy compliant with versions of SAS standards previous to SAS-2 (i.e., a phy with an SSC modulation type of no-spreading and inserting deletable primitives at a rate supporting only the long-term frequency stability).

Figure 120 shows an example of center-spreading tolerance buffer usage.

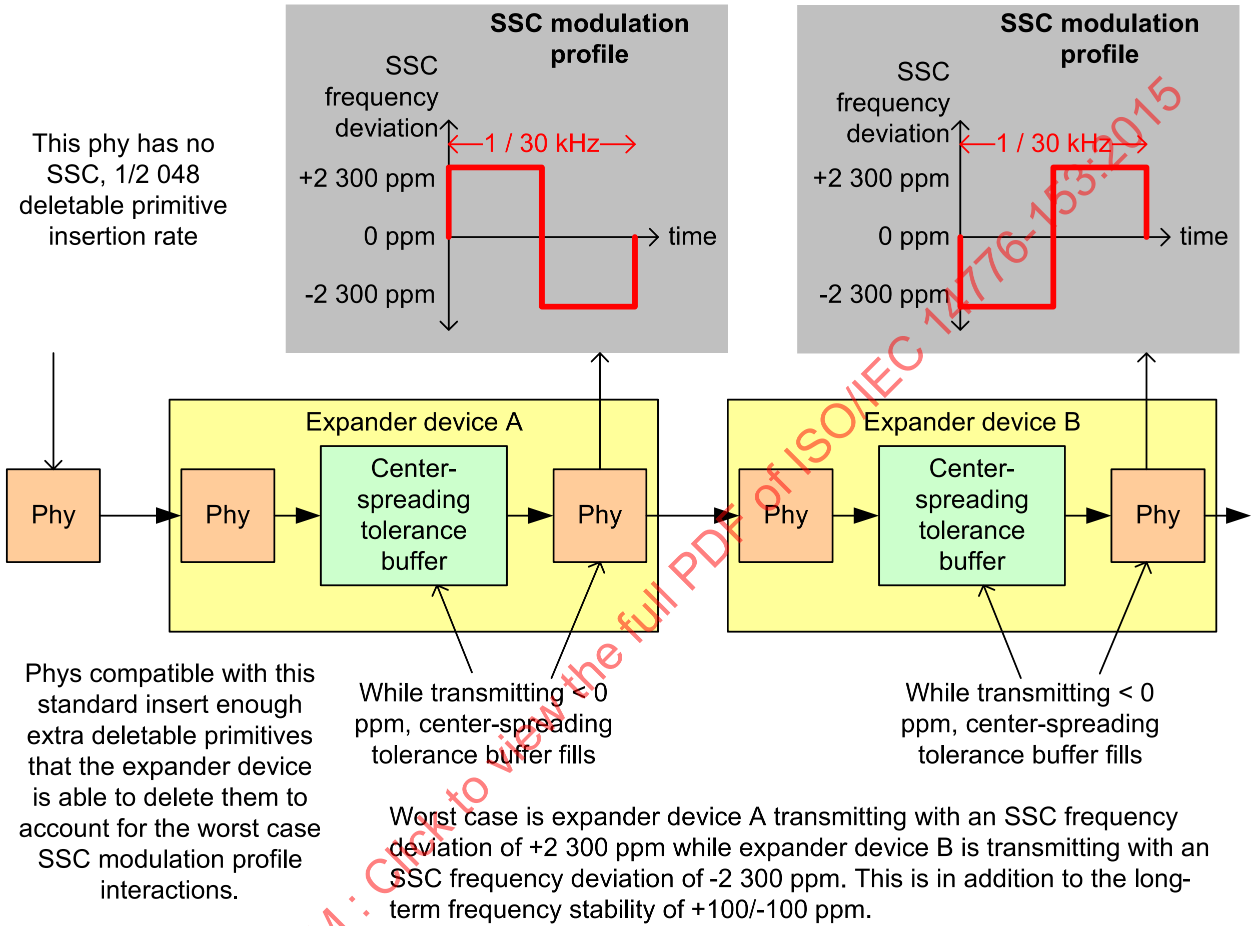


Figure 120 — Center-spreading tolerance buffer

5.7.7 Non-tracking clock architecture

Transceivers shall be designed with a non-tracking clock architecture (i.e., the receive clock derived from the bit stream received by the receiver device shall not be used as the transmit clock by the transmitter device).

Receiver devices that support SATA shall tolerate clock tracking by the SATA device. Receiver devices that do not support SATA are not required to tolerate clock tracking by the SATA device.

5.8 READY LED signal electrical characteristics

A SAS target device uses the READY LED signal to activate an externally visible LED that indicates the state of readiness and activity of the SAS target device.

All SAS target devices (see SPL) using the SAS Drive plug connector (see 5.4.3.3.1.1) shall support the READY LED signal.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain transmitter circuit. The LED and the current limiting circuitry shall be external to the SAS target device.

Table 56 describes the output characteristics of the READY LED signal.

Table 56 — Output characteristics of the READY LED signal

State	Test condition	Requirement
Negated (LED off)	$0\ V \le V_{OH} \le 3.6\ V$	$-100\ \mu A < I_{OH} < 100\ \mu A$
Asserted (LED on)	$I_{OL} = 15\ mA$	$0 \le V_{OL} \le 0.225\ V$

The READY LED signal behavior is defined in SPL.

NOTE 13 SATA devices use the pin used by the READY LED signal (i.e., P11) for activity indication and staggered spin-up disable (see SATA). The output characteristics differ from those in table 56.

5.9 Out of band (OOB) signals

5.9.1 OOB signals overview

When D.C. mode is enabled, OOB signals are low-speed signal patterns that do not appear in normal data streams. When optical mode is enabled, OOB signals consist of a defined series of dwords. OOB signals consist of defined amounts of idle time followed by defined amounts of burst time. During the idle time, the physical link carries OOB idle. During the burst time, the physical link carries dwords. The signals are differentiated by the length of idle time between the burst times. OOB signals are not decoded unless dword synchronization has been lost (see SPL). Once high-speed data transfers are underway, the data pattern amplitude might fall to levels that are falsely detected as OOB signals. A phy shall either have D.C. mode enabled or optical mode enabled. The method to enable D.C. mode or optical mode is outside the scope of this standard.

SATA defines two OOB signals: COMINIT/COMRESET and COMWAKE. COMINIT and COMRESET are used in this standard interchangeably. Phys compliant with this standard identify themselves with an additional SAS-specific OOB signal called COMSAS.

Table 57 defines the timing specifications for OOB signals.

Table 57 — OOB signal timing specifications

Parameter	Minimum	Nominal	Maximum	Comments
OOB Interval (OOBI) [a]	$665.0\overline{6}$ ps [b]	$666.\overline{6}$ ps [c]	$668.2\overline{6}$ ps [d]	The time basis for burst times and idle times used to create OOB signals.
COMSAS detect timeout	13.686 µs [e]			The minimum time a receiver device shall allow to detect COMSAS after transmitting COMSAS.

[a] OOBI is different than UI(OOB) defined in SATA (e.g., SAS has tighter physical link rate long-term stability and different SSC frequency deviation). OOBI is based on:
A) 1.5 Gbit/s UI (see table 26 in 5.7.1);
B) physical link rate long-term stability (see table 28 in 5.7.2); and
C) center-spreading SSC (see table 51 in 5.7.6.1).

[b] $665.0\overline{6}$ ps equals $666.\overline{6} \times (1 - 0.0024)$.

[c] $666.\overline{6}$ equals 2 000 / 3.

[d] $668.2\overline{6}$ ps equals $666.\overline{6} \times 1.002\,4$.

[e] 13.686 µs is 512 × 40 × Maximum OOBI.

To interoperate with interconnects compliant with versions of SAS standards previous to SAS-2, phys should create OOB burst times and idle times based on the UI for 1.5 Gbit/s without SSC modulation.

NOTE 14 Versions of SAS standards previous to SAS-2 defined OOBI based on the nominal UI for 1.5 Gbit/s with physical link rate long-term stability tolerance (see table 26 in 5.7.1) but not with SSC modulation (see table 51 in 5.7.6.1). Interconnects compliant with versions of SAS standards previous to SAS-2 may have assumed phys had that characteristic.

5.9.2 Transmitting OOB signals

Table 58 describes the OOB signal transmitter requirements for the burst time, idle time, negation times, and signal times that are used to form each OOB signal.

Table 58 — OOB signal transmitter device requirements

Signal	Burst time	Idle time	Negation time	Signal time [a]
COMWAKE	160 OOBI [b]	160 OOBI [b]	280 OOBI [c]	2 200 OOBI [g]
COMINIT/COMRESET	160 OOBI [b]	480 OOBI [d]	800 OOBI [e]	4 640 OOBI [i]
COMSAS	160 OOBI [b]	1 440 OOBI [f]	2 400 OOBI [h]	12 000 OOBI [j]

[a] A signal time is six burst times plus six idle times plus one negation time.
[b] 160 OOBI is nominally $106.\overline{6}$ ns (see table 57 in 5.9.1).
[c] 280 OOBI is nominally $186.\overline{6}$ ns.
[d] 480 OOBI is nominally 320 ns.
[e] 800 OOBI is nominally $533.\overline{3}$ ns.
[f] 1 440 OOBI is nominally 960 ns.
[g] 2 200 OOBI (e.g., COMWAKE) is nominally $1\ 466.\overline{6}$ ns.
[h] 2 400 OOBI is nominally 1 600 ns.
[i] 4 640 OOBI (e.g., COMINIT/COMRESET) is nominally $3\ 093.\overline{3}$ ns.
[j] 12 000 OOBI (e.g., COMSAS) is nominally 8 000 ns.

When D.C. mode is enabled, an OOB idle consists of the transmission of D.C. idle.

When optical mode is enabled, an OOB idle consists of repetitions of the following steps:

1) transmission of six OOB_IDLE primitives with either starting disparity at 3 Gbit/s; and
2) transmission of up to 512 data dwords (e.g., two data dwords for COMWAKE idle time, 18 data dwords for COMINIT/COMRESET idle time, and 66 data dwords for COMSAS idle time) set to 0000_0000h that are 8b10b encoded, scrambled, and transmitted at 3 Gbit/s.

An OOB burst consists of:

a) when D.C. mode is enabled, transmission of repeating 0011b or 1100b patterns (e.g., D24.3) or ALIGN (0) primitives with either starting disparity. The OOB burst should consist of repeating 0011b or 1100b patterns (e.g., D24.3) at 1.5 Gbit/s; or
b) when optical mode is enabled, transmission of ALIGN (3) primitives with either starting disparity at 3 Gbit/s.

To transmit an OOB signal, the transmitter device shall repeat these steps six times:

1) transmit OOB idle for an idle time; and
2) transmit an OOB burst for a burst time.

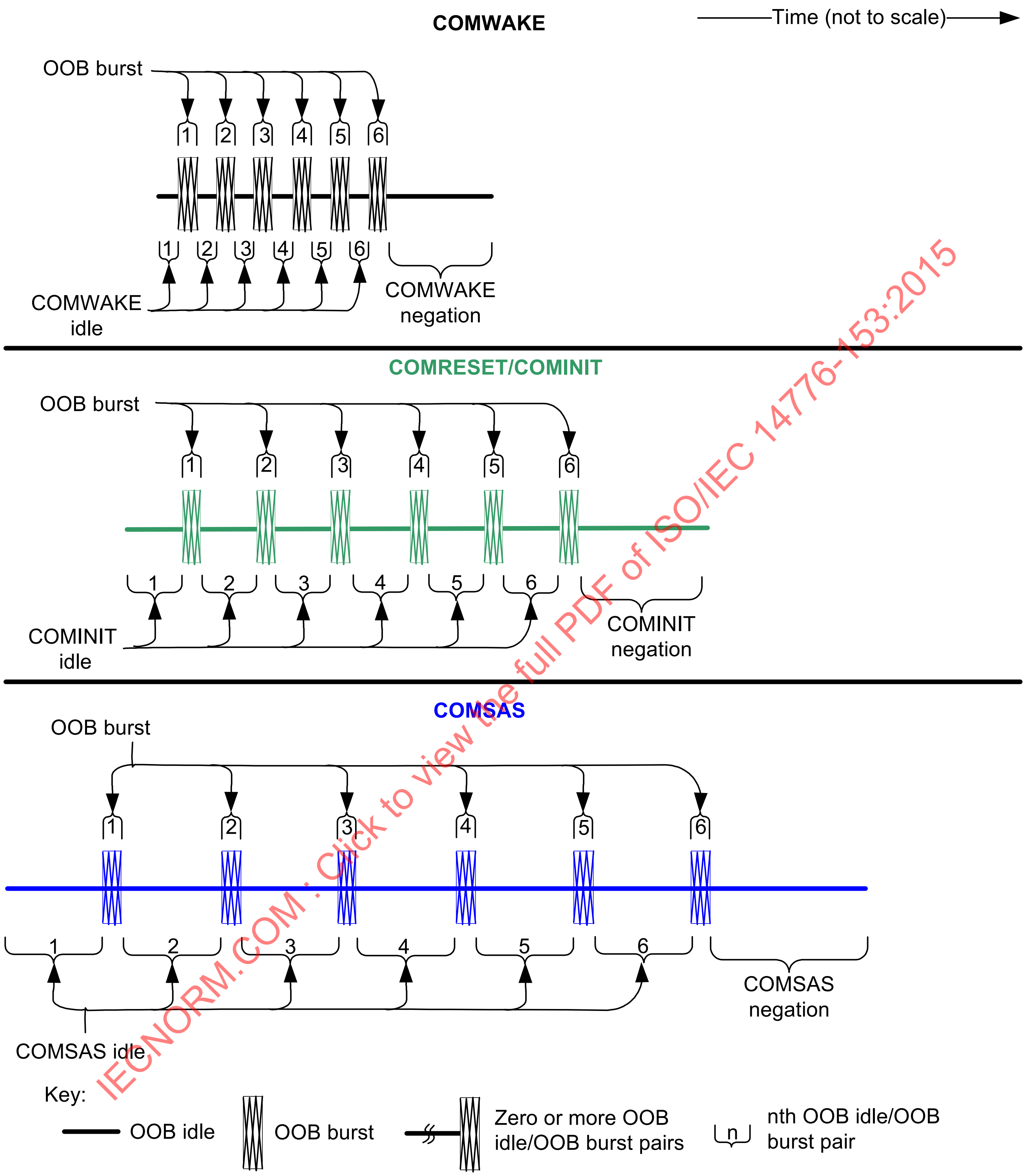
The transmitter device shall then transmit OOB idle for an OOB signal negation time.

The transmitter device shall use signal output levels during burst time and idle time as described in 5.7.4.7.

When D.C. mode is enabled, the repeating 0011b or 1100b patterns (e.g., D24.3) or ALIGN (0) primitives (see SPL) used in OOB signals shall be transmitted and the OOB burst is only required to generate an envelope for the detection circuitry, as required for any signaling that may be A.C. coupled. A burst of repeating 0011b or 1100b patterns (e.g., D24.3) at 1.5 Gbit/s is equivalent to a square wave pattern that has a one for two OOBI and a zero for two OOBI. A transmitter may use this square wave pattern for the OOB burst. The start of the pattern may be one or zero. The signal rise and fall times:

a) shall be greater than (i.e., slower) or equal to the minimum (i.e., fastest) rise and fall times allowed by the fastest supported physical link rate of the transmitter device (see table 30 in 5.7.4.4); and
b) shall be less than (i.e., faster) or equal to the maximum (i.e., slowest) rise and fall times allowed at 1.5 Gbit/s.

Figure 121 describes OOB signal transmission.



Note: OOB idle is shown here as a neutral signal for visual clarity only.

Figure 121 — OOB signal transmission

5.9.3 Receiving OOB signals

Table 59 describes the OOB signal receiver device requirements for detecting burst times, assuming T_{burst} is the length of the detected burst time. The burst time is not used to distinguish between signals.

Table 59 — OOB signal receiver device burst time detection requirements

Signal [a]	may detect	shall detect
COMWAKE	$T_{burst} \leq$ 100 ns or $T_{burst} >$ 112 ns	100 nS < $T_{burst} \leq$ 112 ns
COMINIT/COMRESET	$T_{burst} \leq$ 100 ns or $T_{burst} >$ 112 ns	100 nS < $T_{burst} \leq$ 112 ns
COMSAS	$T_{burst} \leq$ 100 ns or $T_{burst} >$ 112 ns	100 nS < $T_{burst} \leq$ 112 ns

[a] Each burst time is transmitted as 160 OOBI, which is nominally $106.\overline{6}$ ns (see table 58 in 5.9.2).

Table 60 describes the OOB signal receiver device requirements for detecting idle times, assuming T_{idle} is the length of the detected idle time.

Table 60 — OOB signal receiver device idle time detection requirements

Signal	may detect	shall detect	shall not detect
COMWAKE [a]	35 ns $\leq T_{idle} <$ 175 ns	101.3 ns $\leq T_{idle} \leq$ 112 ns	$T_{idle} <$ 35 ns or $T_{idle} \geq$ 175 ns
COMINIT/ COMRESET [b]	175 ns $\leq T_{idle} <$ 525 ns	304 ns $\leq T_{idle} \leq$ 336 ns	$T_{idle} <$ 175 ns or $T_{idle} \geq$ 525 ns
COMSAS [c]	525 ns $\leq T_{idle} <$ 1 575 ns	911.7 ns $\leq T_{idle} \leq$ 1 008 ns	$T_{idle} <$ 525 ns or $T_{idle} \geq$ 1 575 ns

[a] COMWAKE idle time is transmitted as 160 OOBI, which is nominally $106.\overline{6}$ ns (see table 58 in 5.9.2).
[b] COMINIT/COMRESET idle time is transmitted as 480 OOBI, which is nominally 320 ns.
[c] COMSAS idle time is transmitted as 1 440 OOBI, which is nominally 960 ns.

Table 61 describes the OOB signal receiver device requirements for detecting negation times, assuming T_{idle} is the length of the detected idle time.

Table 61 — OOB signal receiver device negation time detection requirements

Signal	shall detect
COMWAKE [a]	$T_{idle} >$ 175 ns
COMINIT/COMRESET [b]	$T_{idle} >$ 525 ns
COMSAS [c]	$T_{idle} >$ 1 575 ns

[a] COMWAKE negation time is transmitted as 280 OOBI, which is nominally $186.\overline{6}$ ns (see table 58 in 5.9.2).
[b] COMINIT/COMRESET negation time is transmitted as 800 OOBI, which is nominally $533.\overline{3}$ ns.
[c] COMSAS negation time, which is transmitted as 2 400 OOBI, which is nominally 1 600 ns.

When D.C. mode is enabled, a SAS receiver device shall detect OOB bursts formed from any of the following:

a) D24.3 characters (see SPL) at 1.5 Gbit/s;
b) ALIGN (0) primitives (see SPL) at 1.5 Gbit/s; or
c) ALIGN (0) primitives at 3 Gbit/s.

NOTE 15 Detection of ALIGN (0) primitives at 3 Gbit/s provides interoperability with transmitter devices compliant with versions of SAS standards previous to SAS-2.

When D.C. mode is enabled, a SAS receiver device shall not qualify the OOB burst based on the characters received.

When optical mode is enabled, a SAS receiver device shall detect OOB bursts formed from ALIGN (3) primitives at 3 Gbit/s.

5.9.4 Transmitting the SATA port selection signal

The SATA port selection signal shown in figure 122 causes the attached SATA port selector (see SPL) to select the attached phy (i.e., one of the SATA port selector's host phys) as the active phy (see SATA).

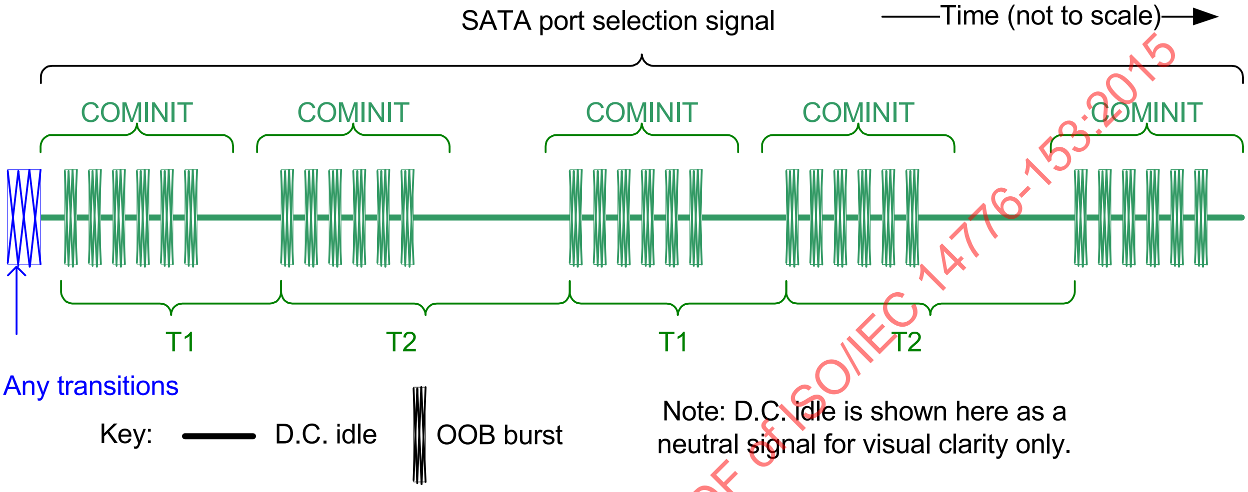


Figure 122 — SATA port selection signal

The SATA port selection signal shall be composed of five COMINIT signals, each starting a specified time interval, T1 or T2, as shown in figure 122, after the start of the OOB burst portion of the previous COMINIT signal. The values of T1 and T2 shall be as shown in table 62.

Table 62 — SATA port selection signal transmitter device requirements

Parameter	Time
T1	3×10^6 OOBI [a]
T2	12×10^6 OOBI [b]

[a] 3×10^6 OOBI is nominally 2 ms (see table 57 in 5.9.1).
[b] 12×10^6 OOBI is nominally 8 ms.

See SPL for information on usage of the SATA port selection signal.

Annex A
(normative)

Jitter tolerance pattern (JTPAT)

The jitter tolerance pattern (JTPAT) consists of:

1) a long run of low transition density pattern;
2) a long run of high transition density pattern; and
3) another short run of low transition density pattern.

The transitions between the pattern segments stress the receiver. The JTPAT is designed to contain the phase shift in both polarities, from zero to one and from one to zero. The critical pattern sections with the phase shifts are underlined in table A.1 and table A.2.

Table A.1 shows the JTPAT when there is positive running disparity (RD+) (see SPL) at the beginning of the pattern. The 8b and 10b values of each character (see SPL) are shown.

Table A.1 — JTPAT for RD+

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD+
		1000011100b	0111100011b	1000011100b	0111100011b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD+	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D20.3 (74h)	RD-
		1000011100b	0111100011b	1000011100b	0010111100b	
	The above dword containing phase shift 11100001011b is sent one time					
42	RD-	D30.3 (7Eh)	D11.5 (ABh)	D21.5 (B5h)	D21.5 (B5h)	RD+
		0111100011b	1101001010b	1010101010b	1010101010b	
	The above dword containing phase shift 00011110100b is sent one time					
43 to 54	RD+	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	D21.5 (B5h)	RD+
		1010101010b	1010101010b	1010101010b	1010101010b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD+	D21.5 (B5h)	D30.2 (5Eh)	D10.2 (4Ah)	D30.3 (7Eh)	RD+
		1010101010b	1000010101b	0101010101b	0111100011b	
	The above dword containing phase shift 01010000b and 10101111b is sent one time					

If the same 8b characters specified in table A.1 are used when there is negative running disparity (RD-) at the beginning of the pattern, then the resulting 10b pattern is different than the positive running disparity for the same 8b character and does not provide the critical phase shifts. To achieve the same phase shift effects with RD-, a different 8b pattern is required. Table A.2 shows the JTPAT when there is negative running disparity (RD-) at the beginning of the pattern. The 8b and 10b values of each character are shown.

The compliant jitter tolerance pattern (CJTPAT) is the JTPAT for RD+ (see table A.1) and RD- (see table A.2) included as the payload in an SSP DATA frame or an SMP frame. A phy or test equipment transmitting CJTPAT outside connections may transmit it with fixed content. See SPL.

Table A.2 — JTPAT for RD-

Dword(s)	Beginning RD	First character	Second character	Third character	Fourth character	Ending RD
0 to 40	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	RD-
		0111100011b	1000011100b	0111100011b	1000011100b	
	The above dword of low transition density pattern is sent a total of forty-one times					
41	RD-	D30.3 (7Eh)	D30.3 (7Eh)	D30.3 (7Eh)	D11.3 (6Bh)	RD+
		0111100011b	1000011100b	0111100011b	1101000011b	
	The above dword containing phase shift 00011110100b is sent one time					
42	RD+	D30.3 (7Eh)	D20.2 (54h)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		1000011100b	0010110101b	0101010101b	0101010101b	
	The above dword containing phase shift 11100001011b is sent one time					
43 to 54	RD-	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	D10.2 (4Ah)	RD-
		0101010101b	0101010101b	0101010101b	0101010101b	
	The above dword of high transition density pattern is sent a total of twelve times					
55	RD-	D10.2 (4Ah)	D30.5 (BEh)	D21.5 (B5h)	D30.3 (7Eh)	RD-
		0101010101b	0111101010b	1010101010b	1000011100b	
	The above dword containing phase shift 10101111b and 01010000b is sent one time					

Annex B
(normative)

SASWDP

B.1 SASWDP introduction

SASWDP is a MATLAB program used for transmitter device compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.7.4.6.1) and for receiver device compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.7.5.7.4). Equivalent simulation programs may be used if they lead to the same results.

B.2 SASWDP.m

```
% MATLAB (R) script to compute TWDP, WDP, and NC-DDJ %%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Version: 1.9
% Date: September 11, 2009
%
% © 2004, 2005, 2006, 2007, 2008, 2009 ClariPhy Communications, Inc. and
% LSI Corporation. All rights reserved.
% Permission is hereby granted to the ANSI INCITS standards body to copy and
% distribute this code in source and binary form, as necessary to publish the
% standard, namely the ANSI INCITS SAS-2.1 standard, to which this source or
% binary code applies provided that the following conditions are met:
% Redistribution of source code must retain the above copyright notice, this
% list of conditions and the following disclaimer.
% Redistributions in binary form must retain the above copyright notice, this
% list of conditions and the following disclaimer in the documentation and/or
% other materials provided with the distribution.
% The names of ClariPhy Communications, Inc., LSI Corporation and the names of
% individual authors or contributors may NOT be used to endorse or promote
% products derived from this software without specific prior written permission.
% THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS"
% AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE
% IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE
% ARE DISCLAIMED. NO WARRANTY OF NON-INFRINGEMENT OF ANY PATENT IS PROVIDED.
% IN NO EVENT SHALL THE COPYRIGHT OWNER(S) OR CONTRIBUTORS BE LIABLE FOR ANY
% DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES
% (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES;
% LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND
% ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
% (INCLUDING INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS, NEGLIGENCE OR
% OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF
% ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. THE LICENSE GRANTED HEREIN IS TO
% THE COPYRIGHT ON THE SOURCE AND BINARY FORMS OF THIS CODE ONLY AND DOES NOT
% INCLUDE A LICENSE TO ANY PATENT RIGHTS, OWNED BY THE COPYRIGHT HOLDERS,
% CONTRIBUTORS OR OTHERS, WHICH MAY BE IMPLICATED BY THE MAKING, USING,
% SELLING, OFFERING FOR SALE OR IMPORTING OF THE SOFTWARE OR PRODUCTS MAKING
% USE OF THE SOFTWARE.
%
% Based on original TWDP methodology described in IEEE Std 802.3aq(TM)-2006
%
% Reference: N. L. Swenson, P. Voois, T. Lindsay, and S. Zeng, "Standards
% compliance testing of optical transmitters using a software-based equalizing
% reference receiver", paper NWC3, Optical Fiber Communication Conference and
% Exposition and The National Fiber Optic Engineers Conference on CD-ROM
% (Optical Society of America, Washington, DC), Feb. 2007
%
% Syntax:
```

```
% [xWDP, ncDDJ, MeasuredxMA, yout] = SASWDP( WaveformFile, TxDataFile, ...
%     SymbolRate, OverSampleRate, Usage, ShowEye )
%
% Inputs:
% -------
% WaveformFile: The waveform consists of exactly N samples per unit interval
%  T, where N is the oversampling rate. The waveform must be circularly
%  shifted to align with the transmit data sequence. The file format is ASCII
%  with a single column of chronological numerical samples, in signal level,
%  with no headers or footers. Enter as a string.
%  This may also be entered as a row or column vector of values.
% TxDataFile: The transmit data sequence should be one of standard test
%  patterns The file format is ASCII with a single column of chronological
%  ones and zeros with no headers or footers. Enter as a string.
%  This may also be entered as a row or column vector of values.
% SymbolRate: The reciprocal of the unit interval in GBd. Enter as a double.
% OverSampleRate: Number of samples, N, per unit interval. Enter as a double.
% Usage: Defines the parameter set specific to the requirement to be verified.
%  In this version, the only permissible values are 'SAS2_TWDP' and
%  'SAS2_LDP'. Enter as a string.
% ShowEye: Controls the graphical display of the slicer input eye. Any value
% greater than zero enables the display (and is the figure number for the
% first figure generated). Enter as a double.
%
% Outputs:
% --------
% xWDP: Waveform Dispersion Penalty (dBe)
% ncDDJ: non-compensable DDJ. This is computed from twice the worst-case eye
%        closure and should be improved.
% MeasuredxMA: Approximative magnitude of the waveform (from 40-60% amplitude
%              of a 5-zeros/5-ones pattern)
% yout is the result of the convolution with the channel response
%      (for debugging purposes).
%
% This script requires the file 'sas2_stressor_6g0_16x.txt' in
% the same directory

%% Function: SASWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [xWDP,ncDDJ,MeasuredxMA,yout]=...
    SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usage,ShowEye)
%% Program constants
SymbolPeriod=1/SymbolRate;
Q0=7.94; % BER = 10^(-15)
%% Load input waveform and data sequence, generate filter and other matrices
% Accept vectors
if ischar(WaveformFile)
  yout0=load(WaveformFile);
else
  yout0=WaveformFile(:);
end
if ischar(TxDataFile)
  XmitData=load(TxDataFile);
else
  % Convert to double otherwise toeplitz may think it is logical...
  XmitData=double(TxDataFile(:));
end
%yout0=load(WaveformFile);
%XmitData=load(TxDataFile);

PtrnLength=length(XmitData);
TotLen=PtrnLength*OverSampleRate;
Fgrid=(-TotLen/2:TotLen/2-1).'/(PtrnLength*SymbolPeriod);

% MG as a first thing, convolve with channel. MeasuredxMA is unused in GetParams
[EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
```

```
    GetParams(Usage,Fgrid,SymbolPeriod,1);

yout0=real(ifft(fft(yout0).*fftshift(H_chan)));

%% Enforce column vectors
yout0 = yout0(:);
XmitData = XmitData(:);
%% Normalize the received OMA or VMA to 1. Estimate the xMA of the captured
%% waveform by using a linear fit to estimate a pulse response, synthesize a
%% square wave, and calculate the xMA of the synthesized square wave per IEEE
%% 802.3, clause 52.9.5.
ant=4; mem=40; % Anticipation and memory parameters for linear fit
X=zeros(ant+mem+1,PtrnLength); % Size data matrix for linear fit
Y=zeros(OverSampleRate,PtrnLength); % Size observation matrix for linear fit
for ind=1:ant+mem+1 % Wrap appropriately for linear fit
    X(ind,:)=XmitData(mod((0:PtrnLength-1)-ind+ant+1,PtrnLength)+1).';
end
X=[X;ones(1,PtrnLength)]; % The all-ones row is included to compute the bias
for ind=1:OverSampleRate
    Y(ind,:)=yout0((0:PtrnLength-1)*OverSampleRate+ind)'; % 1 bit per column
end
Qmat=Y*X'*(X*X')^(-1); % Coefficient matrix resulting from linear fit. Each
%% column (except the last) is one bit period of the pulse response. The last
%% column is the bias.
SqWvPer=10; % Even number; sets the period of the sq wave used to compute xMA
SqWv=[zeros(SqWvPer/2,1);ones(SqWvPer/2,1)]; % One period of sq wave (column)
X=zeros(ant+mem+1,SqWvPer); % Size data matrix for synthesis
for ind=1:ant+mem+1 % Wrap appropriately for synthesis
    X(ind,:)=SqWv(mod((0:SqWvPer-1)-ind+ant+1,SqWvPer)+1).';
end
X=[X;ones(1,SqWvPer)]; % Include the bias
Y=Qmat*X;Y=Y(:); % Synthesize the modulated square wave, put into one column
Y=AlignY(Y,SqWvPer,OverSampleRate);
avgpos=(0.4*SqWvPer/2*OverSampleRate:0.6*SqWvPer/2*OverSampleRate);
ZeroLevel=mean(Y(round(avgpos),:)); % Average over middle 20% of "zero" run
%% Average over middle 20% of "one" run, compute xMA
MeasuredxMA=mean(Y(round(SqWvPer/2*OverSampleRate+avgpos),:))-ZeroLevel;
%% Subtract zero level and normalize xMA
youtn=(yout0-ZeroLevel)/MeasuredxMA;
%% Get usage parameters for the application

%[MG] Removing the second call to GetParams
%[EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
%     GetParams(Usage,Fgrid,SymbolPeriod,MeasuredxMA);

ONE=ones(PtrnLength,1);
%% Set search range for equalizer delay, specified in symbol periods. Lower end
%% of range is minimum channel delay less 5 for a guardband. Upper end of range
%% accounts for the FFE. Round up and add 5 to guardband for the channel and
%% antialiasing filter.
EqDelMin=-5;
EqDelMax=ceil(EqNf/2)+5;
%% Compute the minimum slicer MSE and corresponding xWDP and ncDDJ
X=toeplitz(XmitData,[XmitData(1);XmitData(end:-1:end+1-EqNb)]);
Xtil=toeplitz(XmitData(mod((0:PtrnLength-1)-EqDelMin,PtrnLength )+1),...
    XmitData(mod(-EqDelMin:-1:-(EqDelMax+EqNb),PtrnLength)+1));
Rxx=X'*X; % Used in MSE calculation
for ii=1:size(H_chan,2) % index for stressor
    %% Compute the noise autocorrelation sequence at the output of the front-end
    %% antialiasing filter and rate-2/T sampler.
    N0=SymbolPeriod/2/(Q0*10^(PAlloc(ii)/dBscale))^2;
    Snn=N0/2*fftshift(abs(H_r).^2)*1/SymbolPeriod*OverSampleRate;
    Rnn=real(ifft(Snn));
    Corr=Rnn(1:OverSampleRate/2:end);
    C=toeplitz(Corr(1:EqNf));
```

```
    % [MG] Removing convolution at this point
    yout=youtn;
%     yout=real(ifft(fft(youtn).*fftshift(H_chan(:,ii))));
    if AAfilter > 0
        %% Process signal through front-end antialiasing filter
        yout=real(ifft(fft(yout).*fftshift(H_r)));
    end
    %% Compute the sampling function and sample the processed waveform
    [yk,tk,index1]=CDRSample(yout,OverSampleRate,PtrnLength,UseLAMP);
    %% Compute MMSE-DFE %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %% The MMSE-DFE filter coefficients computed below minimize mean-squared
    %% error at the slicer input. The derivation follows from the fact that the
    %% slicer input over the period of the data sequence can be expressed as
    %% Z = (R+N)*W - X*[0 B]', where R and N are Toeplitz matrices constructed
    %% from the signal and noise components, respectively, at the sampled
    %% output of the antialiasing filter, W is the feedforward filter, X is a
    %% Toeplitz matrix constructed from the input data sequence, and B is the
    %% feedback filter. The computed W and B minimize the mean square error
    %% between the input to the slicer and the transmitted sequence due to
    %% residual ISI and Gaussian noise. Minimize MSE over FFE delay and
    %% determine BER.
    Rout=toeplitz(yk,[yk(1);yk(end:-1:end-EqNf+2)]);
    R=Rout(index1:2:end,:);
    RINV=inv([R'*R+PtrnLength*C,R'*ONE;ONE'*R,PtrnLength]);
    R=[R,ONE]; % Add all-ones column to compute optimal offset
    Rxr=Xtil'*R; Px_r=Rxr*RINV*Rxr';
    %% Minimize MSE over equalizer delay
    MseOpt=Inf;
    for kk=1:EqDelMax-EqDelMin+1
        SubRange=(kk:kk+EqNb);
        SubRange=mod(SubRange-1,PtrnLength)+1;
        P=Rxx-Px_r(SubRange,SubRange);
        P00=P(1,1); P01=P(1,2:end); P11=P(2:end,2:end);
        Mse=P00-P01*inv(P11)*P01';
        if (Mse < MseOpt)
            MseOpt=Mse;
            B=-inv(P11)*P01'; % Feedback filter
            XSel=Xtil(:,SubRange);
            W=RINV*R'*XSel*[1;B]; % Feedforward filter
            Z=R*W-XSel*[0;B]; % Input to slicer
            %% Compute BER using semi-analytic method
            MseGaussian=W(1:end-1)'*C*W(1:end-1);
            Ber=mean(0.5*erfc((abs(Z-0.5)/sqrt(MseGaussian))/sqrt(2)));
        end
    end
    %% Compute equivalent SNR %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %% This function computes the inverse of the Gaussian error probability
    %% function. The built-in function erfcinv() is not sensitive enough for
    %% low probability of error cases.
    if Ber>10^(-12),Q=sqrt(2)*erfinv(1-2*Ber);
    elseif Ber>10^(-323),Q=2.1143*(-1.0658-log10(Ber)).^0.5024;
    else Q=min(abs(Z-0.5))/sqrt(MseGaussian);
    end
    %% Compute penalty and ncDDJ %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    RefSNR=dBscale*log10(Q0)+PAlloc(ii);
    xWDP(ii)=RefSNR-dBscale*log10(Q);
    xWDP(ii)=xWDP(ii)-xMAGain(ii); % Offset xWDP by the eligible xMA gain
    ncDDJ(ii)=AnalyzeEye(yout,tk,index1,W,B,XSel,MseGaussian,...
        ShowEye,Usage,ii,MeasuredxMA,Q,Q0,xWDP(ii),dBscale);
end
%% End of SASWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: GetParams %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [EqNf,EqNb,H_chan,AAfilter,H_r,PAlloc,dBscale,xMAGain,UseLAMP]=...
    GetParams(Usage,Fgrid,SymbolPeriod,MeasuredxMA)
```

```
switch upper(Usage)
    case 'SAS2_TWDP'
        EqNf=1;
        EqNb=3;
        %% Import stressor response from file %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        %% stressorFile : Contains the stressor impulse response(s) sampled
        %% at an interval of "stressorStep". The file format is ASCII with a
        %% column of chronological numerical samples for each stressor with
        %% no headers or footers.
        stressorFile='sas2_stressor_6g0_16x.txt';
        stressorStep=1/(16*6.0);
        %% Resample the stressor at an interval of "SymbolPeriod/OverSampleRate"
        OverSampleRate=round(length(Fgrid)*mean(diff(Fgrid))*SymbolPeriod);
        stressor0=load(stressorFile);
        stressor0Time=(0:length(stressor0)-1)*stressorStep;
        stressorTime=(0:length(Fgrid)-1)*SymbolPeriod/OverSampleRate;
        stressor=interp1(stressor0Time,stressor0.',stressorTime,'linear',0);
        stressor=stressor*SymbolPeriod/(OverSampleRate*stressorStep);
        H_chan=fftshift(fft(stressor.'),1);
        %% AAFilter disables anti-aliasing filter processing of the signal
        %% under test (noise is still shaped). This parameter is used by
        %% Fibre Channel but recommended to be set to 1 for other
        %% applications.
        AAfilter=1;
        %% Denominator coefficients for 7.5 GHz 4-port Butterworth filter
        a=[1,123.140658357,7581.81087032,273453.656327,4931335.23359];
      AABW=0.75/SymbolPeriod;  % Scale coefficients for different bandwidth
        sc=(AABW/7.5).^[0:4]; a=a.*sc;
        H_r=a(end)./polyval(a,j*2*pi*Fgrid);
        PAlloc=15.4;
        dBscale=20;
        xMAGain=0;
        UseLAMP=0;
        % UseLAMP=1;
    case 'SAS2_LDP'
        EqNf=1;
        EqNb=3;
        H_chan=1;
        %% AAFilter disables anti-aliasing filter processing of the signal
        %% under test (noise is still shaped). This parameter is used by
        %% Fibre Channel but recommended to be set to 1 for other
        %% applications.
        AAfilter=1;
        %% Denominator coefficients for 7.5 GHz 4-port Butterworth filter
        a=[1,123.140658357,7581.81087032,273453.656327,4931335.23359];
      AABW=0.75/SymbolPeriod;  % Scale coefficients for different bandwidth
        sc=(AABW/7.5).^[0:4]; a=a.*sc;
        H_r=a(end)./polyval(a,j*2*pi*Fgrid);
        PAlloc=15.4;
        dBscale=20;
        xMAGain=0;
        UseLAMP=0;
        % UseLAMP=1;
    otherwise
        error('Usage not recognized.');
end
%% End of GetParams %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: AlignY %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function Y = AlignY(Y0,SqWvPer,OverSampleRate)
%% Aligns the mid crossing of the xMA square waveform to its ideal position.
Y=Y0-mean(Y0); % AC-couple so crossings are at 0.
%% Look only for the crossing in the middle by ignoring any within ~2 UI from
%% its beginning. Due to possible misalignment of the captured waveform, this
%% is the only crossing that is certain.
```

```
%% x=find(sign(Y(2*OverSampleRate:end-1))~=...
%%      sign(Y(2*OverSampleRate+1:end)),1)+2*OverSampleRate-1;
x=min(find(sign(Y(2*OverSampleRate:end-1))~=...
    sign(Y(2*OverSampleRate+1:end))))+2*OverSampleRate-1;
%% Find a more exact crossing point.
xinterp=interp1([Y(x),Y(x+1)],[x,x+1],0);
%% Shift to create the aligned square waveform.
SqWvLen=SqWvPer*OverSampleRate;
Y=Y0(mod((0:SqWvLen-1)-SqWvLen/2+x,SqWvLen)+1); % Coarse shift.
X=(1:length(Y))';Y=interp1(X,Y,(1:length(Y))'+xinterp-x,'spline'); % Fine shift.
%% End of AlignY %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: CDRSample %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [yk,tk,index1] = ...
    CDRSample(yout,OverSampleRate,PtrnLength,UseLAMP)
%% Derive normalized frequency grid from the input arguments
TotLen=OverSampleRate*PtrnLength;
Fgridn=(-TotLen/2:TotLen/2-1).'/PtrnLength;
%% Compute the frequency response for spectral line bandpass filter
w1=2*pi*(1-1/3000); % Define the pass band (normalized to signaling speed)
w2=2*pi*(1+1/3000);
w0=sqrt(w1*w2);
Bw=w2-w1;
% Denominator and numerator coefficients for a prototype low pass filter
ap=[1,2,1];
bp=[0,2,1];
% Apply frequency transformation to realize the desired bandpass filter
s=j*2*pi*Fgridn(find(Fgridn ~= 0));
sprime=(s.^2+w0^2)./(Bw*s);
Hp=zeros(1,TotLen);
Hp(find(Fgridn ~= 0))=polyval(bp,sprime)./polyval(ap,sprime);
%% Compute the sampling function and sample the waveform
km1=mod((0:TotLen-1)-1,TotLen)+1;
kp1=mod((0:TotLen-1)+1,TotLen)+1;
if UseLAMP > 0
    ylim=tanh(10*(yout-mean(yout)));
    yclk=real(ifft(fft(abs(ylim(kp1)-ylim(km1))).*fftshift(Hp(:))));
else
    yclk=real(ifft(fft(abs(yout(kp1)-yout(km1))).*fftshift(Hp(:))));
end
yclk=yclk(kp1)-yclk(km1);
time=(0:TotLen).'/OverSampleRate; % Wrap waveforms to ensure all edges are
yout=[yout;yout(1)];             % are detected
yclk=[yclk;yclk(1)];
yclk=yclk/(max(yclk)-min(yclk))+0.5; % Normalize clock waveform
kr=find(diff(yclk > 0.5) > 0); % Eye center index
kf=find(diff(yclk > 0.5) < 0); % Eye crossing index
k=sort([kr;kf]);
index1=double(kr(1) > kf(1))+1; % Index of the first eye center
tk=time(k)-(1/OverSampleRate)*(yclk(k)-0.5)./(yclk(k+1)-yclk(k));
yk=interp1(time,yout,tk);
%% End of CDRSample %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Subfunction: AnalyzeEye %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function ncDDJ=AnalyzeEye(yout,tk,index1,W,B,XSel,MseGaussian, ...
    showEye,usage,ii,MeasuredxMA,Q,Q0,xWDP,dBscale)
%% Extract required equalizer parameters from the input arguments.
EqNf=length(W)-1; % Number of T/2-spaced feed-forward taps
EqNb=length(B); % Number of T-spaced feedback taps
xr=XSel(:, 1); % Error-free decisions
%% Define the axes of the bit error ratio map
dphi=1/100; % Phase step (unit interval)
dvee=1/200; % Eye diagram amplitude step (unit amplitude)
phiList=linspace(-0.5,0.5,round(1/dphi)+1);
veeList=linspace(-0.5,0.5,round(1/dvee)+1);
```

```
if ~(showEye > 0),veeList = 0;end
%% Compute the bit error ratio at each point in the time-amplitude grid.
PtrnLength=length(xr);
OverSampleRate=round(length(yout)/PtrnLength);
time=(0:OverSampleRate*PtrnLength).'/OverSampleRate;
yout=[yout;yout(1)];
for jj=1:length(phiList)
    phi=phiList(jj);
    yk=interp1(time,yout,mod(tk+phi,time(end)));
    Y=toeplitz(yk,[yk(1);yk(end:-1:end-EqNf+2)]);
    Y=Y(index1:2:end,:);
    Y=[Y,ones(PtrnLength,1)];
    zk=Y*W-XSel*[0; B];
    %% Compute the minimum distance from the noiseless, equalized samples
    %% to the decision threshold.
    eyeLid0(jj)=max(zk(find(xr == 0)));
    eyeLid1(jj)=min(zk(find(xr == 1)));
    %% Compute the bit error ratio as a function of offset from the nominal
    %% sampling time and decision threshold.
    dk=ones(length(veeList),1)*zk.'-veeList(:)*ones(1,PtrnLength);
    dk(:,find(xr == 0))=0.5-dk(:,find(xr == 0));
    dk(:,find(xr == 1))=dk(:,find(xr == 1))-0.5;
    berMap(:, jj)=mean(erfc(dk/sqrt(2*MseGaussian))/2,2);
end
eyeList=2*min([0.5-eyeLid0;eyeLid1-0.5]);
%% Compute the non-compensable jitter.
kDDJ=find(abs(diff(eyeList > 0)) > 0);
phiDDJ=phiList(kDDJ)-dphi*eyeList(kDDJ)./(eyeList(kDDJ+1)-eyeList(kDDJ));
if length(phiDDJ) == 0
    phiDDJ=[0,0];
end
if length(phiDDJ) == 1
    phiDDJ=sort([phiDDJ,-sign(phiDDJ)/2]);
end
ncDDJ=1-2*max(min([-phiDDJ(1),phiDDJ(2)]),0);
%% Display the bit error ratio map, if requested.
if showEye > 0
    figure(showEye-1+ii);
    clf;
    imagesc(phiList,veeList+0.5,log10(berMap));
    hold on
    plot(phiList,eyeLid0,'--','Color','white');
    plot(phiList,eyeLid1,'--','Color','white');
    hold off
    jetColors=jet;
    colormap(jet);
    caxis([round(log10(erfc(Q0/sqrt(2))/2)),0]);
    colorbar;
    set(gca,'YDir','normal');
    set(gca,'Color',jetColors(end,:));
    if dBscale == 10,units={'W','dBo'};
    else units={'V','dBe'};end
    tapStr=sprintf('\nxMA = %.3e %s',MeasuredxMA,units{1});
    tapStr=[tapStr,sprintf('\nW = [%.3f', W(1))];
    for jj=2:EqNf
        tapStr=[tapStr,sprintf(', %.3f',W(jj))];
    end
    tapStr=[tapStr, ']'];
    if EqNb > 0
        tapStr=[tapStr,sprintf('\nB = [%.3f',B(1))];
        for jj=2:EqNb
            tapStr=[tapStr,sprintf(', %.3f',B(jj))];
        end
        tapStr=[tapStr,']'];
    else
```

```
        tapStr=[tapStr,sprintf('\nB = []')];
    end
    eyeStr=sprintf('SNR = %.1f %s\n',dBscale*log10(Q),units{2});
    eyeStr=[eyeStr,sprintf('xWDP = %.1f %s\n',xWDP,units{2})];
    eyeStr=[eyeStr,sprintf('NC-DDJ = %.3f UI\n',ncDDJ)];
    titleStr=sprintf('[SASWDP] %s',usage);
    titleStr=[titleStr,sprintf('(%d): Bit error ratio map',ii)];
    text(-0.45,0.90,tapStr,'Color','white');
    text(-0.45,0.10,eyeStr,'Color','white');
    title(titleStr, 'Interpreter','none');
    ylabel('Normalized amplitude');
    xlabel('Time (UI)');
end
%% End of AnalyzeEye %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

B.3 SASWDP_testcase.m

The following MATLAB program runs SASWDP with a variety of input files.

```
% SASWDP_testcase.m
clear all,close all
format compact
x1='SCRAMBLED_0RDP10m_symbols.txt';
x2='SCRAMBLED_0RDN10m_symbols.txt';
x3='SCRAMBLED_0RDP_symbols.txt';
x4='SCRAMBLED_0RDN_symbols.txt';
y1='SCRAMBLED_0RDP10m_samples.txt';
y2='SCRAMBLED_0RDN10m_samples.txt';
y3='SCRAMBLED_0RDP_samples.txt';
y4='SCRAMBLED_0RDN_samples.txt';
if 1==0 % to check oversample rate
z=load('WaveformFile_0m-prbs10.txt')
plot(mod([1:length(z)],12),z,'.')
clf,plot(mod([1:length(z)],16),z,'.')
end
for i=1:2
eval(['WaveformFile = y',num2str(i),';'])
eval(['TxDataFile = x',num2str(i),';'])
SymbolRate = 6;
OverSampleRate = 16;
Usage = 'SAS2_LDP';
ShowEye = 1;
[WDP,ncDDJ,MeasuredxMA]=SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usa
     ge,ShowEye)
end
for i=3:4
eval(['WaveformFile = y',num2str(i),';'])
eval(['TxDataFile = x',num2str(i),';'])
SymbolRate = 6;
OverSampleRate = 16;
Usage = 'SAS2_TWDP';
ShowEye = 1;
[WDP,ncDDJ,MeasuredxMA]=SASWDP(WaveformFile,TxDataFile,SymbolRate,OverSampleRate,Usa
     ge,ShowEye)
end
```

Annex C
(informative)

StatEye

C.1 StatEye introduction

StatEye is a Python program that may be used for simulating TxRx connection compliance for trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s (see 5.5.5). Equivalent simulation programs may be used if they lead to the same results.

NOTE 16 See http://www.stateye.org for more information on StatEye.

C.2 analysis.py

The following Python file loads pattern measurement files, and is not used for TxRx connection compliance simulations.

```
from string import rstrip
from re import split, search

version = “071210.a”

def loadcsv(filename,startline,endline,timecol,sigcol) :
time = []
signal = []
_line = 0
flag = 0

for line in file(‘%s.csv’%filename) :
    if flag == 0:
        if search(‘^[0-9,]’,line) :
            flag = 1

    if flag == 1:
        _line += 1
        if (_line > endline) and (endline>0) :
            break
        if _line > startline :
            line = rstrip(line)
            a = split(‘,’,line)
            _time = eval(a[timecol])
            _signal = eval(a[sigcol])
            time += [_time]
            signal += [_signal]

return([time,signal])

def loadtxt(filename,startline,endline,timecol,sigcol) :
time = []
signal = []
_line = 0
flag = 0

for line in file(‘%s.txt’%filename) :
    if flag == 0:
```

```
            if search('^[0-9,]',line) :
                  flag = 1

      if flag == 1:
            _line += 1
            if (_line > endline) and (endline>0) :
                  break
            if _line > startline :
                  line = rstrip(line)
                  a = split(' ',line)
                  _time = eval(a[timecol])
                  _signal = eval(a[sigcol])
                  time += [_time]
                  signal += [_signal]

return([time,signal])


def polar2rect(r, w, deg=0):# radian if deg=0; degree if deg=1
    from math import cos, sin, pi
    if deg:
w = pi * w / 180.0
    return [r * cos(w), r * sin(w)]

def rect2polar(x, y, deg=0):# radian if deg=0; degree if deg=1
    from math import hypot, atan2, pi
    if deg:
return hypot(x, y), 180.0 * atan2(y, x) / pi
    else:
return [hypot(x, y), atan2(y, x)]
```

C.3 cdr.py

The following Python file extracts the clock from a pattern measurement, and is not used for TxRx connection compliance simulations.

```
from numpy import *
from pylab import *

# version 071210.a

def cdr (edges,k,m,name) :

period0 = min(diff(edges[10:2000]))

period = [period0]

phase = [edges[0]]
phaseError = []
nperiod = []
phaseInOld = edges[0]-period[-1]

for phaseIn in edges :
      nperiod += [ floor( (phaseIn+0.5*period[-1] - phaseInOld) /
period[-1]) ]
      phaseInOld = phaseIn
```

```
        _phaseError = phaseIn - phase[-1] + period[-1]/2
        phaseError += [ mod( _phaseError , period[-1]) - period[-1]/2 ]
        period += [period[-1] + phaseError[-1] * k]
        phase += [phase[-1] + phaseError[-1] * m + nperiod[-1]*period[-1]]

figure()
subplot(3,1,1)
hold(0)
plot(phase/mean(period))
hold(1)
plot(edges/mean(period))
grid(1)
xlabel('time [UI]')
ylabel('Absolute Phase[UI]')
title(name)

subplot(3,1,2)
plot(diff(edges))
hold(1)
plot(array(period))
grid(1)
xlabel('time [UI]')
ylabel('Period\nDeviation [%mean]')

subplot(3,1,3)
plot(array(phaseError) / mean(period) )
grid(1)
xlabel('time [UI]')
ylabel('Phase Error[UI]')

savefig('cdrExtraction.png')

return([phaseError, period])
```

C.4 extractJitter.py

The following Python file extracts jitter from a pattern measurement, and is not used for TxRx connection compliance simulations.

```
from numpy import *
from pylab import *

# version 071210.a

def extractJitter(inputT, outputsignalF, signalF, offset, RJ, timestep,
mylength) :

# the offset parameter will eventually be automatically calculated

from scipy.special import erfinv
from penrose import
extractApproxEdge,extractAccurateEdge,extractAccurateEdge
from cdr import cdr
import pdb

_inputT = extractApproxEdge(inputT)
```

```
_outputsignalF = extractAccurateEdge(outputsignalF)
_signalF = extractAccurateEdge(signalF)

j = array(_inputT)[offset:len(_outputsignalF)+offset] - (
array(_outputsignalF) -
array(_signalF)[offset:len(_outputsignalF)+offset] )

# extract the noise inbetween two edges
# this could be improved!!
noise = []
for i in range(len(_outputsignalF)-1) :
      noise += [ signalF[ int(
(_signalF[offset+i]+_signalF[offset+i+1])/2.0 ) ] - outputsignalF[ int(
(_outputsignalF[i]+_outputsignalF[i+1])/2.0 ) ] ]


figure()
hold(0)
plot(noise)
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
title('Transmitter Noise')
savefig('noise.png')

outtime  = arange(len(noise)) * timestep
outfile = open('noise.csv','w')
for index in range(len(outtime)) :
      outfile.writelines('%e,%e\n'%(outtime[index],noise[index]))
outfile.close()

if 0:
      figure()
      hold(0)
      plot(_inputT,'x')
      hold(1)
      plot(_outputsignalF,'x')
      plot(_signalF,'x')
      plot(j,'o')
      grid(1)

[pe,per]=cdr(j,0.005,0.005,'CDR Jitter Extraction')

_per = mean(per[1000:])
[pdf,t]=histogram(array(pe[1000:])/_per,100)

# pdb.set_trace()

pdf[find(pdf<5)] = 0
pdf = pdf*1.0 / sum(pdf)
mid = min(find(t>0))
left = max(find(pdf[:mid] == 0)) + 1
rght = min(find(pdf[mid:] == 0)) - 1 + mid

leftcdf = cumsum(pdf[left:mid])
leftcdf[find(leftcdf==1)] = 1-1e-15
rghtcdf = flipud(cumsum(flipud(pdf[mid:rght])))
rghtcdf[find(rghtcdf==1)] = 1-1e-15
```

```
leftt = t[left:mid]
rghtt = t[mid:rght]

Qleft = -sqrt(2) * erfinv( 2.0 * (1 - leftcdf) -1 )
Qrght = -sqrt(2) * erfinv( 2.0 * (1 - rghtcdf) -1 )

npoints = 4
# Pleft = polyfit(leftt[0:npoints],Qleft[0:npoints],1)
# Prght = polyfit(rghtt[-npoints:],Qrght[-npoints:],1)

_Qleft = concatenate(( [-7] , Qleft ))
_Qrght = concatenate(( Qrght , [-7] ))

# _RJ = ( 1.0 / abs(Pleft[0]) + 1.0 / abs(Prght[0]) ) / 2.0
DJ = -Qrght[-1] * RJ - Qleft[0] * RJ

_leftt = concatenate(( [ leftt[0] - (Qleft[0]+7)*RJ ] , leftt ))
_rghtt = concatenate(( rghtt , [ rghtt[-1] + (Qrght[-1]+7)*RJ ] ))

print 'Extracted RJ = %0.4f, DJ = %0.4f'%(RJ, DJ)

figure()
hold(0)
plot(_leftt,_Qleft)
hold(1)
plot(_rghtt,_Qrght)
grid(1)
xlabel('Time [UI]')
ylabel('Q')
title('Extracted Transmit Jitter, RJ = %0.4f, DJ = %0.4f'%(RJ, DJ) )
savefig('ExtractedJitter.png')

return([RJ,DJ])
```

C.5 penrose.py

The following Python file extracts the step response from a pattern measurement, and is not used for TxRx connection compliance simulations.

```
from analysis import *
from numpy import *
import numpy
from pylab import *
import time
from string import rsplit, rstrip
from scipy import linalg, interp
from re import *
import pdb

# version 080110.a

def extractApproxEdge(x) :
y = find( abs(diff( (array(x)>0)*1.0 )) == 1.0 )
return(y)
```

```
def extractAccurateEdge(x) :
from scipy import interp
y = []
for i in range(len(x)-1) :
      if ( ((x[i] < 0.0) and (x[i+1] > 0.0)) or ((x[i] > 0.0) and
(x[i+1] < 0.0)) ) :
            _y = interp([0],[x[i],x[i+1]],[i,i+1])[0]
            y += [_y]
return(y)

def filter(x,k) :
y = [x[0]]
for _x in x:
      y += [ (_x-y[-1])*k + y[-1] ]
return(y)

def buildM(x,l) :
M = []
for i in range(len(x)-l) :
      M += [ x[i:i+l] ]
return(M)


def penrose(filename, mylength,start,finish,timecol,sigcol) :
#mylength = 800
#start      = 37000
#finish     = 41000
signalFilter= 0.90
stimFilter= 0.90
outputFilter= 0.90


[time,signal]=loadcsv(filename,start,finish,timecol,sigcol)
start = (array(signal)<0).nonzero()[0][0]
end = (array(signal)>0).nonzero()[0][-1]

print 'Signal analysis from %d to %d'%(start,end)

signalF = filter(signal,signalFilter)
signalF = signalF[start:end+1]
inputT      = (array(signalF)>0)*2.0-1.0
inputF      = filter(inputT,stimFilter)
M_inputF = buildM(inputF,mylength)
IM_inputF = linalg.pinv(transpose(M_inputF))
taps        =
matrixmultiply(transpose(IM_inputF),(signalF[mylength/2:mylength/2 +
len(IM_inputF)]))
outputsignal= matrixmultiply(M_inputF,taps)
outputsignalF = filter(outputsignal,outputFilter)

testT             = ones(mylength*10)*-1.0
testT[mylength*5:]= 1.0
testF             = filter(testT,stimFilter)
M_testF           = buildM(testF,mylength)
outputtest  = matrixmultiply(M_testF,taps)
outputtestF = filter(outputtest,outputFilter)

#figure()
#hold(0)
```

```
#plot(taps)
#grid(1)
#xlabel('time [sample #]')
#ylabel('amplitude [V]')
#savefig('taps.png')

figure()
llength = 10000
hold(0)
plot(signalF[mylength/2-1:llength])
hold(1)
plot(inputF[mylength/2-1:llength])
plot(outputsignalF[:llength])
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
legend(['Measured Signal', 'Fundamental Transmitter', 'Reconstructed'])
title('Signal Reconstruction')
axis([axis()[1]/2,axis()[1]/2+1000,axis()[2],axis()[3]])
savefig('inAndOutSignal.png')

figure()
hold(0)
plot(outputtestF)
grid(1)
xlabel('time [sample #]')
ylabel('amplitude [V]')
#axis([4900,5100,axis()[2],axis()[3]])
title('Extracted Step Response')
savefig('step.png')

outtime  = arange(len(outputtestF)) * (time[1]-time[0])
outfile = open('extractedStep.csv','w')
for index in range(len(outtime)) :
      outfile.writelines('%e,%e\n'%(outtime[index],outputtestF[index]))
outfile.close()

return([inputT, outputsignalF, signalF, time[1]-time[0]])
```


C.6 portalocker.py

The following Python file locks files for exclusive access.

NOTE 17 See the ActiveState Code web site at http://aspn.activestate.com/ASPN/Cookbook/Python/Recipe/65203 for information about the portalocker code recipe.

```
# portalocker.py - Cross-platform (posix/nt) API for flock-style file
locking.
#                  Requires python 1.5.2 or better.
# The MIT License
#
# Copyright (c) 2008 Jonathan Feinberg
#
# Permission is hereby granted, free of charge, to any person obtaining
a copy
```

```
# of this software and associated documentation files (the "Software"),
to deal
# in the Software without restriction, including without limitation the
rights
# to use, copy, modify, merge, publish, distribute, sublicense, and/or
sell
# copies of the Software, and to permit persons to whom the Software is
# furnished to do so, subject to the following conditions:
#
# The above copyright notice and this permission notice shall be
included in
# all copies or substantial portions of the Software.
#
# THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND,
EXPRESS OR
# IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF
MERCHANTABILITY,
# FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT
SHALL THE
# AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER
# LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE,
ARISING FROM,
# OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS
IN
# THE SOFTWARE.

"""Cross-platform (posix/nt) API for flock-style file locking.

Synopsis:

   import portalocker
   file = open("somefile", "r+")
   portalocker.lock(file, portalocker.LOCK_EX)
   file.seek(12)
   file.write("foo")
   file.close()

If you know what you're doing, you may choose to

   portalocker.unlock(file)

before closing the file, but why?

Methods:

   lock( file, flags )
   unlock( file )

Constants:

   LOCK_EX
   LOCK_SH
   LOCK_NB

Exceptions:

    LockException

Notes:
```

```
For the ‘nt’ platform, this module requires the Python Extensions for
Windows.
Be aware that this may not work as expected on Windows 95/98/ME.

History:

I learned the win32 technique for locking files from sample code
provided by John Nielsen <nielsenjf@my-deja.com> in the documentation
that accompanies the win32 modules.

Author: Jonathan Feinberg <jdf@pobox.com>,
        Lowell Alleman <lalleman@mfps.com>
Version: $Id: portalocker.py 5474 2008-05-16 20:53:50Z lowell $

“““


__all__ = [
    “lock”,
    “unlock”,
    “LOCK_EX”,
    “LOCK_SH”,
    “LOCK_NB”,
    “LockException”,
]

import os

class LockException(Exception):
    # Error codes:
    LOCK_FAILED = 1

if os.name == ‘nt’:
    import win32con
    import win32file
    import pywintypes
    LOCK_EX = win32con.LOCKFILE_EXCLUSIVE_LOCK
    LOCK_SH = 0 # the default
    LOCK_NB = win32con.LOCKFILE_FAIL_IMMEDIATELY
    # is there any reason not to reuse the following structure?
    __overlapped = pywintypes.OVERLAPPED()
elif os.name == ‘posix’:
    import fcntl
    LOCK_EX = fcntl.LOCK_EX
    LOCK_SH = fcntl.LOCK_SH
    LOCK_NB = fcntl.LOCK_NB
else:
    raise RuntimeError, “PortaLocker only defined for nt and posix
platforms”

if os.name == ‘nt’:
    def lock(file, flags):
        hfile = win32file._get_osfhandle(file.fileno())
        try:
           win32file.LockFileEx(hfile, flags, 0, -0x10000, __overlapped)
        except pywintypes.error, exc_value:
            # error: (33, ‘LockFileEx’, ‘The process cannot access the
file because another process has locked a portion of the file.’)
```

```
            if exc_value[0] == 33:
                raise LockException(LockException.LOCK_FAILED,
exc_value[2])
            else:
                # Q:  Are there exceptions/codes we should be dealing
with here?
                raise

    def unlock(file):
        hfile = win32file._get_osfhandle(file.fileno())
        try:
            win32file.UnlockFileEx(hfile, 0, -0x10000, __overlapped)
        except pywintypes.error, exc_value:
            if exc_value[0] == 158:
                # error: (158, 'UnlockFileEx', 'The segment is already
unlocked.')
                # To match the 'posix' implementation, silently ignore
this error
                pass
            else:
                # Q:  Are there exceptions/codes we should be dealing
with here?
                raise

elif os.name == 'posix':
    def lock(file, flags):
        try:
            fcntl.flock(file.fileno(), flags)
        except IOError, exc_value:
            #  IOError: [Errno 11] Resource temporarily unavailable
            if exc_value[0] == 11:
                raise LockException(LockException.LOCK_FAILED,
exc_value[1])
            else:
                raise

    def unlock(file):
        fcntl.flock(file.fileno(), fcntl.LOCK_UN)



if __name__ == '__main__':
    from time import time, strftime, localtime
    import sys
    import portalocker

    log = open('log.txt', "a+")
    portalocker.lock(log, portalocker.LOCK_EX)

    timestamp = strftime("%m/%d/%Y %H:%M:%S\n", localtime(time()))
    log.write( timestamp )

    print "Wrote lines. Hit enter to release lock."
    dummy = sys.stdin.readline()

    log.close()
```

C.7 stateye.py

The following Python file computes the statistical eye.

```
from numpy import *
import pdb
import time
from matplotlib import *

##############################################################
# stateye class

class stateye :

##############################################################
# constructor

def __init__(self) :

      self.version='080110.a'

      # debug file
      self.debug = open('stateye.debug','w')

      # transitionState[currentState] = [<possible next state>]
      self.transitionState= []

      # edge[currentState] = [<edge index corresponding to
transitionState>]
      self.edge    = []

      # step[<edge index>] = [<time vs. amplitude>]
      # where @t=0;a=0, @t=inf;a=final
      self.step    = []

      # length of each step must be the same and equal to rxLength
      self.UImax   = 0

      # number of states.
      self.nStates= 0

      # bins construction
      # bins is a Markov pdf; bin[<state>][<amplitude index>]
      self.bins    = []
      # see binIndex and binValue for explanation of bin coefficients
      self.noBins = 4001
      self.midBin = 2001
      self.kBin    = 2000
      self.binMax = 2.0
      self.binaxis= (arange(self.noBins) - self.midBin) * self.binMax /
self.kBin

      # parameters for cursor to step time conversion
      # are loaded when generating step responses
      # see cursor2index for details
      self.nomUI   = 1          # number of time indexes in step response
for UI
      self.nomOffset= 0         # simple offset for peak centring
      # amplitude of pulse width shrinkage
```

```
            self.pws     = 0          # in UI

      def __del__(self) :
            self.debug.flush()
            self.debug.close()

      ############################################################
      # simple routine to index into pdf bins given a value
      def binIndex(self, x)  :
            return( round(x / self.binMax * self.kBin) + self.midBin )

      ############################################################
      # simple route to find value for pdf bin given a index
      def binValue(self, i):
            return( 1.0 * (i-self.midBin) / self.kBin * self.binMax )

      ############################################################
      # simple routine to convert cursor index and sweep offset into time
      index of step response
      def cursor2index(self, cursor, sweep) :
            return( int( round( (cursor+sweep) * self.nomUI + self.nomOffset )
      ) )

      ############################################################
      # simple routine to convert index to cursor
      def index2cursor(self, index) :
            return( (index - self.nomOffset) * 1.0 / self.nomUI )

      ############################################################
      # shift a pdf bin description as convolution
      def binShift(self, bin, x)  :
            i = self.midBin - self.binIndex(x)
            if i < 0 :
                  return( concatenate(( bin[-i:], zeros(-i) )) )
            if i > 0 :
                  return( concatenate(( zeros(i), bin[0:-i] )) )
            if i==0 :
                  return(bin)

      # perform stateye algorithm for single sample phase
      # clearly includes pws but not mid band jitter
      def
      calcpdf(self,sweepdelta,startCursor,lastCursor,dj,rj,noise_x,noise_y) :
                      from pylab import find
            import pdb
            self.cdf=[]
            self.sweep = arange(-0.75,0.75,sweepdelta)
            #self.sweep = [0.0]
            self.pdf=zeros(( len(self.sweep), len(self.binaxis) ))

            # generate a pre-indexed step response for acceleration of the pdf
      calculation
            # should consider this for other variable as well, e.g. dfecoef
            self.stepK = []
            for _step in self.step :
                  _stepK = []
                  for __step in _step :
                        _stepK += [self.midBin - self.binIndex(__step)]
                  self.stepK += [ _stepK ]
```

```
      print 'folding %d steps'%len(self.sweep)
      binstore = [ 1.0*zeros((self.nStates,self.noBins)),
1.0*zeros((self.nStates,self.noBins)) ]
      for i_sweep in range(len(self.sweep)) :
            #self.debug.writelines('at sweep %d from
%d\n'%(i_sweep,len(self.sweep)))
            #delta = time.time() - tag
            print '%d'%(i_sweep+1),
            #tag = time.time()
            # scan from last cursor to first cursor
            # i.e. back cursor tracing
            # for debug
            bintag = 0
            _bins = binstore[bintag]
            bins = binstore[1-bintag]
            bins = self.start_bins
            _bins[:] = 0.0
            # the value of the step for the given cursor and sweep
            _sweep       = self.sweep[i_sweep]
            for cursor in flipud(range(startCursor,lastCursor)) :
                  # self.debug.writelines('at cursor %d\n'%cursor)
                  #print 'at cursor %d'%cursor

                  # where am I on the time axis
                  currentIndex = self.cursor2index(cursor,_sweep)

                  # next Markov pdf contents
                  # perform Markov convolution
                  # scan through each state
                  for state in range(self.nStates) :

                        # enable for tracking speed of exection
                        # print 'at state %d'%state

                        # scan each possible transition from this state
                        for transition in
range(len(self.transitionState[state])) :
                              # sweep the pws assuming a simple dirac
distribution

                              # for debug
                              # for pws in [-self.pws,self.pws] :
                              for pws in [0] :
                                    # calculate the next state for the
given state
                                    _nextState =
self.transitionState[state][transition]

                                    # the edge needed to get to this
state
                                    _edge       =
self.edge[state][transition]

                                    # when pws is enabled then
currentIndex clearly needs to be correctly modulated
                                    _delta      = -self.stepK[ _edge ][
currentIndex + pws]

                                    # perform a convoltion using a
```

```
simple shift and addition for the state given
                                    if _delta==0 :
                                          _bins[_nextState]+=
bins[state]
                                    else :
                                          if (_delta<0) :
                                                _t =
bins[state][-_delta:]

_bins[_nextState][:len(_t)] +=  _t
                                          else :
                                                _t =
bins[state][:-_delta]

_bins[_nextState][-len(_t):] += _t


                  # enable for dumping the pdfs as they are built up
                  #for _state in range(self.nStates) :
                  #     if len(pylab.find(bins[_state]>0) > 0) :
                  #           print '%s =
%s'%(self.states[_state],array2string(self.binValue(pylab.find(bins[_st
ate]>0))))

                  bintag = 1-bintag
                  _bins = binstore[bintag]
                  bins = binstore[1-bintag]
                  _bins[:] = 0.0

                  # dfe condition
                  # this is also taking a second
                  if cursor==2 :
                        for dfeCoef in self.dfeCoef :
                              for state in range(self.nStates) :

                                    # going to make a big assumption
here!!! That the threshold for greater than and less than is the same
                                    # also going to make a bug
assumption that the gt and lt results index are also inverse
                                    if 1:
                                          _threshold =
self.binIndex(self.gt_h0[state])

                                          _shift      = self.binShift(
\

concatenate(( \

zeros(_threshold), bins[state][_threshold:] )), \

-self.gt_true[state] * dfeCoef )
                                          _bins[state] =
add(_bins[state], _shift)

                                          _shift      = self.binShift(
\

concatenate(( \
```

```
bins[state][:_threshold],  zeros(self.noBins - _threshold) )), \

-self.gt_false[state] * dfeCoef )
                                            _bins[state] =
add(_bins[state], _shift)
                                      else :
                                            for binIndex in
range(self.noBins) :
                                                  if
self.binValue(binIndex) > self.gt_h0[state] :
                                                        _binValue =
self.binValue(binIndex) + self.gt_true[state] * dfeCoef
                                                  else :
                                                        _binValue =
self.binValue(binIndex) + self.gt_false[state] * dfeCoef

_bins[state][self.binIndex(_binValue)] += bins[state][binIndex]

                              bintag = 1-bintag
                              _bins = binstore[bintag]
                              bins = binstore[1-bintag]
                              _bins[:] = 0.0

                         # enable for dumping the pdfs as they are built
up
                         #for _state in range(self.nStates) :
                         #     if len(pylab.find(bins[_state]>0) > 0) :
                         #           print '%s =
%s'%(self.states[_state],array2string(self.binValue(pylab.find(bins[_st
ate]>0))))

            _pdf = zeros(self.noBins)

            # typical good place to break for debugging
            # pdb.set_trace()
            # firstly what if sum = 0; secondly the sum for difference
states may be different???
            # this scaling of the pdf is still not quite workig
correctly
            bins = bins / bins.sum()
            for state in range(self.nStates) :
                  _pdf = add(_pdf, bins[state])
                  # this additional of the fliped array is mainly for
8b10b support. As we only run one set of the codes
                  # we need to add in the other half. I believe this is
correct, but am checking it again
                  _pdf = add(_pdf, flipud(bins[state]))
            _pdf = _pdf / _pdf.sum()
            self.pdf[i_sweep] = _pdf
            self.debug.writelines('final =
%s\n'%(array2string(self.binValue(find(_pdf>0)))))

      print '\nfolding noise'
      # convolve the noise into
      if 0:
            self.pdf_n = zeros(( len(self.sweep), len(self.binaxis) ))
            for i_sweep in range(len(self.sweep)) :
                  for _noise in range(len(noise_x)) :
                        if noise_y[_noise] >0 :
```

```
                              _shift = self.binShift(self.pdf[i_sweep],
noise_x[_noise] ) * noise_y[_noise]
                              self.pdf_n[i_sweep]  =
add(self.pdf_n[i_sweep], _shift)
                  self.pdf_n[i_sweep] = self.pdf_n[i_sweep] /
(self.pdf_n[i_sweep]).sum()
      else :
            self.pdf_n = self.pdf

      print 'folding jitter'
      # final pdf containing the jittered version
      if 1:
        self.p = []
        sigma = rj;
        mean  = dj/2;
        for _sweep in self.sweep :
            p = 1/(sigma*sqrt(2*pi)) *
exp(-((_sweep-mean)**2)/(2*sigma**2)) + \
                  1/(sigma*sqrt(2*pi)) *
exp(-((_sweep+mean)**2)/(2*sigma**2)) + \
                  1/(sigma*sqrt(2*pi)) *
exp(-((_sweep)**2)/(2*sigma**2));
            if p>1.0e-12 :
                  self.p += [p]
            else :
                  self.p += [0.0]

        self.p = self.p / sum(self.p);

        self.pdf_pj=zeros(( len(self.sweep), len(self.binaxis) ))
        _jmid = len(self.sweep)/2
        for _i in range(len(self.sweep)) :
                  #print 'at sweep %d'%_i
                            for _j in range(len(self.sweep)) :
                                _k = _i + _j - _jmid
                                if (_k > 0) and (_k<len(self.sweep)) :
                  self.pdf_pj[_i] += self.p[_j] * self.pdf_n[_k]
                  self.pdf_pj[_i] = self.pdf_pj[_i] /
self.pdf_pj[_i].sum()

def loadStep(self, inputStep, _ui, _pws) :
      from pylab import find
      # define pulse response
      self.inputStep = inputStep
      self.converge= max(inputStep)
      self.pulse = add(-inputStep[:-_ui], +inputStep[_ui:])
      self.nomOffset = find(self.pulse==max(self.pulse))[0]

      # load the step response parameters for
      self.nomUI= _ui
      self.pws= _pws

      # start and last cursor must allow for some margin
      self.startCursor =
(range(self.nomOffset,0,-_ui)[-2]-self.nomOffset)/_ui
      self.lastCursor=
(range(self.nomOffset,len(inputStep),_ui)[-2]-self.nomOffset)/_ui
      self.xindex =
arange(self.cursor2index(self.startCursor,0),self.cursor2index(self.las
```

```
tCursor,0))

        #print 'start cursor %d, finish cursor
%d'%(self.startCursor,self.lastCursor)

def create2TapFIR(self, c, noDFEtaps) :
        from pylab import find
        # input step is the fundamental step response of the system to a
1V step, and is assumed to be 0@t=0
        # c is a 1x2 array containing the FIR coefficients
        # this function defines the transitionStates, edge transitions and
generates the necessary steps

        self.nStates = 4

        # for each state x
        #                              0        1        2        3
        x                  = [   [0,0],      [0,1],      [1,0],      [1,1]
]
        x = array(x)*2.0 - 1.0
        self.states = [   '00',       '01',       '10',       '11'   ]
        # load the possible state transition
        self.transitionState = [ [0,1], [2,3], [0,1],   [2,3] ]
        # define the edge used to move from state to state
        self.edge   = [   [0,1],      [2,3],      [4,5],      [6,7] ]
        # load empty steps
        self.step   = [     [],[],        [],[],[],[],[],[] ]

        # preload the Markov pdf with the converged values for the two
stable states,
        # leave the other state empty
        self.start_bins              = zeros((self.nStates,self.noBins))
        self.start_bins[0][self.binIndex( sum(x[0]*c)*self.converge )] =
1
        self.start_bins[3][self.binIndex( sum(x[3]*c)*self.converge )] =
1

        # this could be more efficient in storage of the indexes, but for
a simple example it doesn't matter
        # for each state and transitions an edge is defined
        # copy the inputStep into each step array, given the correct
factor needed to move states
        for _state in range(self.nStates) :
                for _transition in range(len(self.edge[_state])) :
                        k =
(sum(x[self.transitionState[_state][_transition]]*flipud(c)) -
sum(x[_state]*flipud(c)))
                        self.debug.writelines('in state %d, transitioning to
state %d, using %0.3f\n'\

%(_state,self.transitionState[_state][_transition],k))
                        self.step[self.edge[_state][_transition]] =
self.inputStep * k

        # this is the post equalised step response
        self.pulse = add( add ( \
                        self.step[ self.edge[0][1] ][self.nomUI*2:] , \
                        self.step[ self.edge[1][0] ][self.nomUI:-self.nomUI]
) , \
```

```
                  self.step[ self.edge[2][0] ][:-self.nomUI*2] )
      self.pulse = self.pulse/2.0
      self.nomOffset = find(self.pulse==max(self.pulse))[0]

      self.dfeCoef = []
      h0 = self.pulse[self.cursor2index(0 , 0)]
      print 'found h0=%0.3f'%h0
      #                  00    01    10    11
      self.gt_h0 = [-h0, +h0, -h0,  +h0]
      self.gt_true = [-1.0, -1.0,-1.0,-1.0]
      self.gt_false = [+1.0, +1.0,+1.0,+1.0]
      self.lt_h0 = [-h0,+h0,  -h0,  +h0]
      self.lt_true = [+1.0,+1.0,+1.0, +1.0]
      self.lt_false = [-1.0,-1.0,-1.0, -1.0]

      # clearly we need to include here the proper algorithm for finding
the optimum sampling point!!
      for cursor in range(noDFEtaps) :
            self.dfeCoef += [ abs(
self.pulse[self.cursor2index(cursor+1, 0)] ) ]
            print 'Extracting cursor %d, found %0.3f'%(cursor+1,
self.dfeCoef[-1])


def create8b10b_2TapFIR(self,c,noDFEtaps) :
      from pylab import find
      import pdb

      word10b_p = def8b10b()
      words = sort(word10b_p)
      states = ['x','x']

      # scan through all possible 8b10b codes, truncating to a given
length l
      # collect all possible codes
      for l in range(1,11) :
            for _words in words :
                  short = _words[:l]
                  if not(any(array(states)==short)) :
                        states += [short]

      # initialise the transition state matrix
      transitionState = []
      for i in range(len(states)) :
            transitionState += [[]]

      # fill transition state matrx
      for i in range(len(states)) :
            # as we search for where this code could have come from, we
only start searching when the
            # code would be a minimum of 2 characters long. e.g. if the
code word is 1001, we search for
            # 100 as the source of this code word
            if len(states[i])>1 :
                  # find the index into the state matrix, for the source
of the current word
                  source = find(states[i][:-1]==array(states))[0]
                  # add this code word index to the transition matrix
entry for the source of this code wor
```

```
                  # clearly we will only find one single source per code
word
                  transitionState[source] += [i]
            # if we are at the final word, then also add the transitions
to this entry in the transition
            # matrix for getting back to 0 & 1. However, as we are
implementing a 2 tap FIR, we must maintain
            # also the second entry, hence the starting states are
00,01,10 & 11
            if len(states[i])==10 :
                  if states[i][-1]=='0' :
                        transitionState[i] += [0]
                        transitionState[i] += [1]
                  if states[i][-1]=='1' :
                        transitionState[i] += [2]
                        transitionState[i] += [3]

      # as stated above we must over write the first four states to be
correct
      states[0:4] = ['00','01','10','11']
      transitionState[0] = transitionState[2]
      transitionState[1] = transitionState[3]

      # generate all possible transitions
      k = []
      transitionLookUp = []
      step  = []
      for _i in range(2**3) :
            if _i > 0 :
                  transitionLookUp += [binary_repr(_i)]
            else :
                  transitionLookUp += ['']
            while(len(transitionLookUp[-1])<3) :
                  transitionLookUp[-1] = '0' + transitionLookUp[-1]
            _k = 0
            for _j in range(2) :
                  # the polarity here needs to be checked
                  _k -= (eval(transitionLookUp[-1][_j])*2.0-1.0) *
flipud(c)[_j] - (eval(transitionLookUp[-1][_j+1])*2.0-1.0) *
flipud(c)[_j]
            k += [_k]
            step += [self.inputStep * _k]
            self.debug.writelines('edge %s/%d is
%0.3f\n'%(transitionLookUp[-1],_i,_k))

      # scan through actual transitions and enter edge index into array
      edgeText = []
      edge = []
      for _state in range(len(states)) :
            _edgeText=[]
            _edge=[]
            for _transition in range(len(transitionState[_state])) :
                  _nextstate = transitionState[_state][_transition]
                  __edgeText = states[_state][-2:] +
states[_nextstate][-1]
                  _edgeText += [__edgeText]
                  __edge = find( __edgeText == array(transitionLookUp) )
                  _edge += [__edge]
                  self.debug.writelines('from %s to %s using
```

```
%s/%d\n'%(states[_state],states[_nextstate],__edgeText,__edge))
            edge += [_edge]
            edgeText += [_edgeText]

      self.states = states
      self.transitionState = transitionState
      self.edge    = edge
      self.step    = step

      self.nStates       = len(self.states)
      self.start_bins                = zeros((self.nStates,self.noBins))
      # this is the current initialisation matrix which need extending
      # see the commented conditional statements below
      if 0 :
            self.start_bins[0][self.binIndex( self.converge *
sum(array([-1,-1])*c) )] = 1
            self.start_bins[3][self.binIndex( self.converge *
sum(array([+1,+1])*c) )] = 1
      else :
            for _states in range(len(states)) :
                  if (states[_states][-2:]=='00') :
                        self.start_bins[_states][self.binIndex(
self.converge * sum(array([-1,-1])*c) )] = 1
                  #if (states[_states][-2:]=='01') :
                  #     self.start_bins[_states][self.binIndex(
self.converge * sum(array([-1,+1])*c) )] = 1
                  #if (states[_states][-2:]=='10') :
                  #     self.start_bins[_states][self.binIndex(
self.converge * sum(array([+1,-1])*c) )] = 1
                  if (states[_states][-2:]=='11') :
                        self.start_bins[_states][self.binIndex(
self.converge * sum(array([+1,+1])*c) )] = 1

      # this is the post equalised step response
      self.pulse = add( add ( \
                  self.step[ 1 ][self.nomUI*2:] , \
                  self.step[ 2 ][self.nomUI:-self.nomUI] ) , \
                  self.step[ 4 ][:-self.nomUI*2] )
      self.pulse = self.pulse/2.0
      self.nomOffset = find(self.pulse==max(self.pulse))[0]
      self.dfeCoef = []
      h0 = self.pulse[self.cursor2index(0 , 0)]

      # clearly we need to include here the proper algorithm for finding
the optimum sampling point!!
      for cursor in range(noDFEtaps) :
            self.dfeCoef += [ abs(
self.pulse[self.cursor2index(cursor+1, 0)] ) ]
            print 'Extracting cursor %d, found %0.3f'%(cursor+1,
self.dfeCoef[-1])

      # setup the DFE correction matrix
      self.gt_h0 = []
      self.gt_true = []
      self.gt_false= []
      self.lt_h0 = []
      self.lt_true = []
      self.lt_false= []
      #pdb.set_trace()
```

```
		for _states in states :
			if (_states[-2:]==’00’) or (_states[-2:]==’10’) :
				self.gt_h0 += [-h0]
				self.gt_true+= [-1.0]
				self.gt_false+= [+1.0]
				self.lt_h0 += [-h0]
				self.lt_true+= [+1.0]
				self.lt_false+= [-1.0]
			if (_states[-2:]==’01’) or (_states[-2:]==’11’) :
				self.gt_h0 += [+h0]
				self.gt_true+= [-1.0]
				self.gt_false+= [+1.0]
				self.lt_h0 += [+h0]
				self.lt_true+= [+1.0]
				self.lt_false+= [-1.0]



	# simple example based on step.py in steptheory
	# probably doesn’t work anymore since extending the code to support more
features
	def bist(self) :
		# states are
		# 0 = 0 0
		# 1 = 0 1
		# 2 = 1 0
		# 3 = 1 1
		self.transitionState = [[0,1],[2,3],[0,1],[2,3]]
		self.edge		= [[0,1],[2,3],[4,5],[6,7]]
		self.step	= [[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0, 0.0], \
				[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 1.04,
1.3600000000000001, 1.5200000000000002, 1.6000000000000001,
1.6000000000000001, 1.6000000000000001], \
				[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
-1.1700000000000002, -1.53, -1.7100000000000002, -1.8, -1.8, -1.8],
[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, -0.12999999999999998,
-0.16999999999999996, -0.18999999999999997, -0.19999999999999996,
-0.19999999999999996, -0.19999999999999996], \
				[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.12999999999999998, 0.16999999999999996, 0.18999999999999997,
0.19999999999999996, 0.19999999999999996, 0.19999999999999996], \
				[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
1.1700000000000002, 1.53, 1.7100000000000002, 1.8, 1.8, 1.8], [0.0, 0.0,
0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, -1.04, -1.3600000000000001,
-1.5200000000000002, -1.6000000000000001, -1.6000000000000001,
-1.6000000000000001], \
				[0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0, 0.0,
0.0, 0.0, 0.0, 0.0, 0.0]]
		self.stepLength= 15
		self.nStates= 4
		self.start_bins= 1.0*zeros((self.nStates,self.noBins))
		self.start_bins[0][self.binIndex(-0.7)] = 1.0
		self.start_bins[3][self.binIndex(+0.7)] = 1.0
		self.calcpdf()


	###############################################################
	# simple functions to load all the possible 8b10b words
```