INTERNATIONAL STANDARD

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2005-04

Information technology –
Fibre Channel –

Part 114:
100 MB/s balanced copper physical interface (FC-100-DF-EL-S)

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CONTENTS

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FOREWORD

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International Standard ISO/IEC 14165-114 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

ISO/IEC 14165-114 has to be read in conjunction with the forthcoming International Standard ISO/IEC 14165-115.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

INTRODUCTION

This standard builds on ISO/IEC 14165-115 and ISO/IEC 14165-251 (see bibliography). It specifies a Media Dependent Interface for duplex Ethernet transmission of 100 MB/s: a physical layer interface for a signalling rate of 1 062,5 Mbit/s over two pairs. It is specified for operation over Class F balanced cabling channels, for up to 100 m of Category 7 balanced (twisted pair) cabling. The interface is referred to as 100-DF-EL-S based on the nomenclature defined in 5.9 of ISO/IEC 14165-115.

This standard eliminates the need for implementation of the complex functions specified in ISO/IEC 8802-3 that cancel the effects of crosstalk and return loss. This provides a solution that can operate at a much lower power level, and that can be implemented at a lower cost than products that use Clause 40 of ISO/IEC 8802-3. Therefore, it also has the potential for multiple ports per chip.

Model

A 1000BASE-TX2/4 PHY model is shown in Figure 1. Although sublayers within the 1000BASE-TX2/4 PHY may be present, e.g. for management, reconciliation or auto-negotiation as defined in ISO/IEC 8802-3, they are not presented in Figure 1.

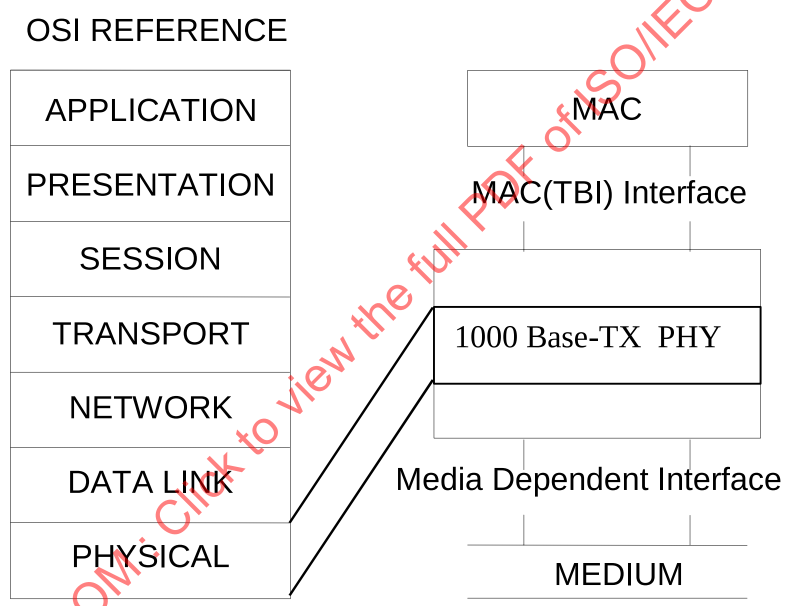


Figure 1 – Model

Relation to other standards

This standard specifies a dedicated full-duplex Ethernet PHY layer, as defined in ISO/IEC 7498-1: Open Systems Interconnection (OSI) reference model, but does not support Carrier Sense or Collision Detect. The MAC interface specified in this standard inter-operates with the GMII interface specified in ISO/IEC 8802-3 at full duplex. Implementers may choose to be compliant with this international standard along with clauses in other standards.

INFORMATION TECHNOLOGY – FIBRE CHANNEL – Part 114: 100 MB/s Balanced copper physical interface (FC-100-DF-EL-S)

1 Scope

This International Standard describes a physical interface for Fibre Channel that is based on and adds to ISO/IEC 14165-115. It specifies a Medium Dependent Interface for 1000BASE-TX2/4 PHY layers as defined in ISO/IEC 7498-1 together with the consequences for the physical layer and the MAC (TBI) Interface. Scrambling, coding and modulation necessary to provide a bit error rate of 10^{-12} or less are specified. This standard also specifies the requirements for the medium (transmission channel). These requirements are within the minimum performance of a dedicated balanced Class F channel (in general made of up to 100 m Class F balanced (twisted pair) cabling, as specified in ISO/IEC 11801:2002). This International Standard supports full duplex transmission with a signalling rate of 1 062,5 Mbit/s.

This International Standard provides a low-complexity Media Independent Interface and the functional description of an Ethernet physical layer for 100 MB/s transmission that can easily be implemented by many vendors. This standard takes advantage of the improved transmission characteristics provided by balanced cabling channels of Class F, as specified in ISO/IEC 11801:2002.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060 (all parts), *High-voltage test techniques*

IEC 60950 (all parts), *Information technology equipment - Safety*

IEC 61076-3-104, *Connectors for electronic equipment - Part 3-104: Rectangular connectors - Detail specification for 8-way, shielded free and fixed connectors for data transmissions with frequencies up to 600 MHz minimum*

IEC 62151, *Safety of equipment electrically connected to a telecommunication network*

ISO/IEC 7498-1:1994, *Information technology – Open Systems Interconnection - Basic Reference Model: The Basic Model*

ISO/IEC 8802-3:2000, *Information technology – Local and metropolitan area networks – Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications*

ISO/IEC 11801, *Information technology – Generic cabling for customer premises*

3 Definitions, symbols, and abbreviations

3.1 Definitions

For the purposes of this International Standard, the following definitions apply.

3.1.1
Gigabit Media Independent Interface (GMII)
interface between the reconciliation sublayer and the physical coding sublayer (PCS) for 1 000 Mbit/s operation

[1.4.136 of ISO/IEC 8802-3]

NOTE – See also Clause 35 of ISO/IEC 8802-3.

3.1.2
Media Access Control (MAC)
data link sublayer that is responsible for transferring data to and from the Physical Layer

[1.4.167 of of ISO/IEC 8802-3]

3.1.3

Media-Dependent Interface (MDI)
mechanical and electrical interface between the transmission medium and the Medium Attachment Unit (MAU)

3.1.4
Media-Independent Interface (MII)
A transparent signal interface at the bottom of the Reconciliation sublayer
[1.4.168 of ISO/IEC 8802-3]

NOTE – See also Clause 22 of ISO/IEC 8802-3.

3.1.5
Physical Coding Sublayer (PCS)
a sublayer used to couple the Media Independent Interface (MII) or Gigabit Media Independent Interface (GMII) and the Physical Medium Attachment (PMA)
The PCS contains the functions to encode data bits into code-groups that can be transmitted over the physical medium.

NOTE – See also Clauses 23, 24, 32, 36 and 40 of ISO/IEC 8802-3.

3.1.6
Physical Layer entity (PHY)
the portion of the Physical Layer between the Medium Dependent Interfaces (MII) and the Media Independent Interface (MDI)
The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium.

3.1.7
Physical Medium Attachment (PMA) sublayer
the portion of the Physical Layer that contains the functions for transmission, reception, and (depending on the PHY) collision detection, clock recovery and skew alignment

3.1.8
Physical Medium Dependent sublayer (PMD)
the portion of the Physical Layer responsible for interfacing to the transmission medium
The PMD is located just above the Medium Dependent Interface (MDI) and the Media Conversion sublayer.

3.1.9
Ten Bit Interface (TBI)
physical instantiation of the PMA service interface, as a partition between the PMA sublayer and the PCS and MAC sublayers, intended for use as a chip-to-chip interface with no mechanical connector specified

NOTE – See also Clause 36 of ISO/IEC 8802-3.

3.2 Symbols

f frequency in MHz
^ XOR logical operator

3.3 Abbreviations

BER	Bit Error Rate
EF	End of Frame
GMII	Gigabit Media Independent Interface
MAC	Media Access Control
MDI	Medium Dependent Interface
MII	Medium Independent Interface
PCS	Physical Coding Sublayer
PHY	Physical Layer entity
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
SF	Start of Frame
TBI	Ten Bit Interface
WC	Wiring Closet

4 MAC interface

4.1 General

This clause specifies the logical and electrical service interface between the MAC and the physical layer. The purpose of this clause is to specify the minimum requirements to comply with this standard. This interface shall meet the requirements of ISO/IEC 8802-3 that are explicitly referenced in this clause.

4.2 Overview

Figure 2 illustrates the required interface. Each direction of data is serviced by an eight bit wide data bus, data valid, error, and clock signals. The interface may be used as a chip-to-chip interface. The interface provides a media independent interface to a MAC and is specified as a minimum set of requirements.

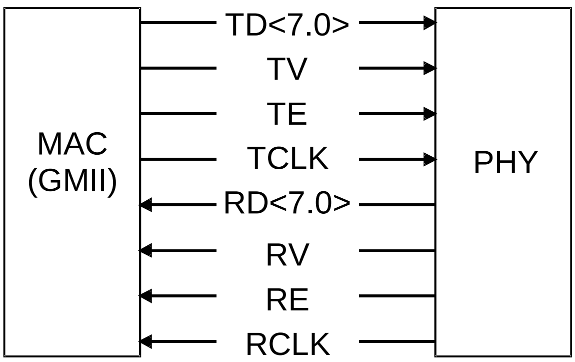


Figure 2 – MAC interface

The interface between physical layer and medium interface is specified so as to support a signalling rate of 1 062,5 Mbit/s. Figure 3 illustrates the full duplex operation to provide a signalling rate of 1 062,5 Mbit/s over 2 pairs.

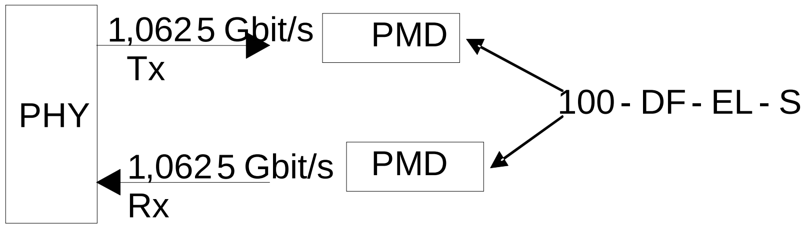


Figure 3 – Interface overview via 100 Ω Class F cabling

4.3 Detailed specification

The receive (RD<7:0>, RV, RE, RCLK) and the transmit (TD<7:0>, TV, TE, TCLK) signals shall meet the following requirements. Other uses for the signals that support additional functions, such as that defined in ISO/IEC 8802-3, Clause 35, are not specifically excluded.

This standard does not require support of carrier extend or carrier extend error.

4.3.1 RD<7:0> received data

The eight bits of the RD<7:0> are the received data from the physical layer. The received data is valid when RV is true and on the rising edge of the RCLK. All data transfers are aligned on eight bit boundaries. RD<0> is the least significant bit. The eight data signals shall meet the d.c. characteristics specified in 4.3.9 and the a.c. characteristics specified in 4.3.10.

4.3.2 RV receive valid

The RV shall indicate that on the next rising edge of the RCLK that the data is valid. RV shall become true before the rising edge of RCLK and remain true during all data transfers from the PHY until the last valid data byte. The RV signal shall meet the d.c. characteristics specified in 4.3.9 and the a.c. characteristics specified in 4.3.10.

4.3.3 RE receive error

When RE is true at least for one full clock cycle while RV is true, this indicates that the PHY has determined that there is an unrecoverable error in the data stream. The RV signal shall meet the d.c. characteristics specified in 4.3.9 and the a.c. characteristics specified in 4.3.10.

4.3.4 RCLK receive clock

The RCLK is the received data clock from the PHY. The RCLK is a continuous clock that provides the timing reference for RD<7:0>, RV, and RE. During non data transfer times the RCLK can extend a half cycle period by no more than two clock cycles. The RCLK signal shall meet the d.c. characteristics defined in 4.3.9 and the a.c. characteristics in 4.3.10.

4.3.5 TD<7:0> transmit data

The eight bits of the TD<7:0> are the transmit data for the PHY. The transmit data is valid when TV is true and on the rising edge of the TCLK. All data transfers are aligned on eight bit boundaries. TD<0> is the least significant bit. The eight data signals shall meet the d.c. characteristics specified in 4.3.9 and the a.c. characteristics specified in 4.3.10.

4.3.6 TV transmit valid

The TV shall indicate to the PHY on the next rising edge of the TCLK that the data is valid. TV shall become true before the rising edge of TCLK and remain true during all data transfers to the PHY until the last valid data byte. The TV signal shall meet the d.c. characteristics defined in 4.3.9 and the a.c. characteristics in 4.3.10.

4.3.7 TE transmit error

When TE is true for at least one full clock cycle while TV is true, this indicates to the PHY that it shall insert a transmit error into the output data stream. The TV signal shall meet the d.c. characteristics defined in 4.3.9 and the a.c. characteristics in 4.3.10.

4.3.8 TCLK transmit clock

The TCLK is the transmit data clock to the PHY. The TCLK is a continuous clock that provides the timing reference for TD<7:0>, TV and TE. During non data transfer times the TCLK can extend a half cycle period by no more than two clock cycles. The TCLK signal shall meet the d.c. characteristics defined in 4.3.9 and the a.c. characteristics in 4.3.10.

4.3.9 DC characteristics

All MAC interface signals shall meet the d.c. specifications in Table 1.

Table 1 – DC characteristics

Symbol	Parameter	Conditions		Min.	Max.
VOH	Output high voltage	IOH= -1,0 mA	VCC= Min	2,10 V	3,60 V
VOL	Output low voltage	IOL= 1,0 mA	VCC= Min	GND	0,50 V
VIH	Input high voltage			1,70 V	
VIL	Input low voltage				0,9 V
IIH	Input high current	VCC= Max	VIN= 2,1 V		40 µA
IIL	Input low current	VCC= Max	VIN= 0,5 V	-600 µA	

4.3.10 MAC characteristics

All MAC interface signals shall meet the a.c. specifications in Table 2.

Table 2 – AC characteristics

Symbol	Parameter	Min.	Max.
VIL	Input low		0,70 V
VIH	Input high	1,90 V	
Freq.	R/TCLK	125 MHz ± 100 ppm	
t period	R/TCLK	7,5 ns	8,5 ns
t rtf	CLK rise/fall time		1 ns
t setup	R/TV,E,D<7:0>	2,5 ns	
t hold	R/TV,E,D<7:0>	0,5 ns	

4.3.11 MAC, GMII and MII interfaces

The MAC interface signals defined in 4.3.1 to 4.3.8 are equivalent to GMII signals illustrated in Table 3. If a MII interface as defined in Clause 22 of ISO/IEC 8802-3 is implemented, it shall conform to the signal mapping specified in Table 3 and in Clause 22 of ISO/IEC 8802-3.

Table 3 – Signal mapping

MAC Interface	GMII	MII
TE	TX_ER	TX_ER
TV	TX_EN	TX_EN
TD <7>	TXD <7>	
TD <6>	TXD <6>	
TD <5>	TXD <5>	
TD <4>	TXD <4>	
TD <3>	TXD <3>	TX <3>
TD <2>	TXD <2>	TX <2>
TD <1>	TXD <1>	TX <1>
TD <0>	TXD <0>	TX <0>
TCLK	GTX_CLK	TX_CLK
RE	RX_ER	RX_ER
RV	RX_EN	RX_EN
RD <7>	RXD <7>	
RD <6>	RXD <6>	
RD <5>	RXD <5>	
RD <4>	RXD <4>	
RD <3>	RXD <3>	RX <3>
RD <2>	RXD <2>	RX <2>
RD <1>	RXD <1>	RX <1>
RD <0>	RXD <0>	RX <0>
RCLK	RX_CLK	RX_CLK

4.4 Testing

All MAC interface signals that are equivalent to a GMII interface shall be tested in accordance with specifications defined for GMII devices in 35.4.2.1 and 35.4.2.2 of ISO/IEC 8802-3.

4.5 Data stream

Data streams transmitted to and from the MAC interface shall be transferred with the field shown in Figure 4.

← TV/RV valid →

<preamble><sfd><data>

Figure 4 – MAC interface data stream

The preamble and sfd are defined in 35.2.3.2 of ISO/IEC 8802-3, for both transmit and receive. The data consists of a continuous stream of octets. An end of transmission is indicated by de-assertion of TV. The preamble may be omitted when transmitting to the MAC.

4.6 Service control functions

There are no service control functions required for PHY control across the MAC interface. An implementation of a management control is defined in 22.2.4, 28.2.4 and 37.2.6 of ISO/IEC 8802-3.

4.7 Timers

There are no required timers for PHY control at the MAC interface.

4.8 Delay requirements

The PHY shall conform to the MAC/Media interface delay requirements specified in Table 4.

Table 4 – Delay requirements

Event	MAX. bit time	Timing reference
TV= 1 to MDI Output	135	TD <7,0> to TP1/TP2
MDI Input to RV= 1	192	TP1/TP2 to RD <7,0>

4.9 Reset

A PHY reset shall be executed at power up or when requested by a management function.

5 Operation

5.1 Detail of the physical interfaces

The PHY employs a full duplex base band transmission. It is possible to transmit with a signalling rate of 1 062,5 Mbit/s over 2 pairs full duplex. There is one pair for receive and one for transmit with a MLT-3 coding scheme (without scrambling), see Figure 5, Figure 6 and Figure 7. Optionally, the scrambler described in 8.3 may be used.

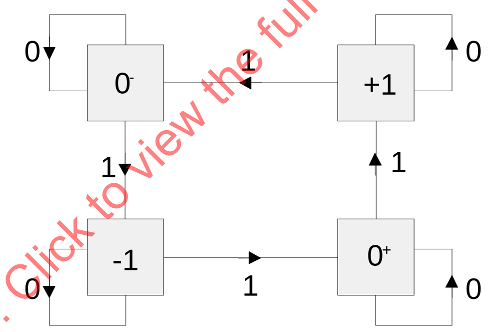


Figure 5 – State diagram of MLT-3

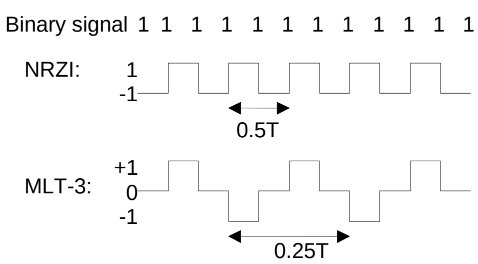


Figure 6 – Coding scheme of MLT-3

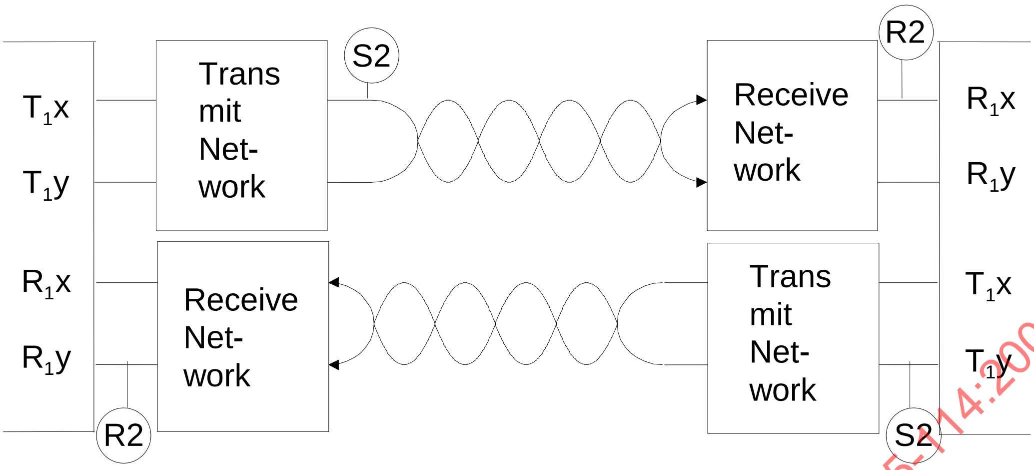


Figure 7 – Transmission with MLT-3

An optional equalizer network, when present in a link, shall not be part of the cable plant. It should be seen as a part of the transmitting and (or) receiving circuit. The dividing line between cable plant and data terminating equipment is at the end of the channel (as described in the cabling standard ISO/IEC 11801:2002).

5.2 Signalling

Special code sets are used to transmit IDLE and control: start of frame (SF), end of frame (EF) and a transmit error are defined in ISO/IEC 8802-3.

NOTE Mapping between GMII and Fibre Channel start-of-frame, end-of-frame and other primitive signals is for further study.

5.3 Frame format

Frames passed to the coding sublayer shall have the structure as illustrated in Figure 8**.**

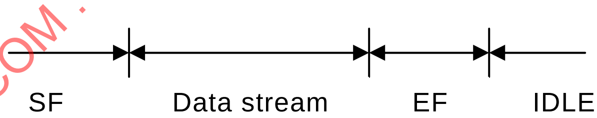


Figure 8 – Frame format

At the beginning of a frame of transmission indicated by the TV at the MAC interface two code sets representing a start of frame, SF, are transmitted followed by the data stream from the MAC, defined in 4.5. The SF replaces the first two bytes of the MAC data stream (preamble). The completion of a frame, determined by TV, is followed by two code sets of end of frame, EF; then the idle code sets, IDLE. A transmit error code set is transmitted when indicated by the TE signal at the MAC interface.

At the detection of SF by the receiving PHY the MAC interface shall indicate a start of data with the RV signal. The SF is not passed on to the MAC interface. When the PHY receives the EF frame signal it will indicate the end of data by the RV signal. Only decoded data octets are transmitted to the MAC interface. If the PHY receives a transmit error code set or an invalid coding it will indicate this to the MAC interface with the RE signal.

5.4 Functions at the MAC interface

Table 5 lists a cross reference of parameters used for the control of the MAC interface to those defined in Clause 40 of ISO/IEC 8802-3.

Table 5 – Control functions

1000 BASE-TX	Clause 40[1)]
TD <7,0>	TXD [7,0]
RD <7,0>	RXD [7,0]
time *t* and *t* +1 code set *n*	*n*
transmitting	tx_enable , tx_mode
undefined	SEND_Z
transmit IDLE	SEND_I
receive status OL	rcvr_status = OK
undefined	Csreset
undefined	Cext_CSExtend
transmit error	tx_error, TX_ER, xmt_err
SF	SSD
EF	ESD
1) See Clause 40 of ISO/IEC 8802-3.	

6 Coding

6.1 Timers

There are no required timers for transmit or receive operation.

6.2 Receive status OK

When PHY is successfully receiving valid symbols then the receive status OK shall be set true; otherwise it shall be set false.

6.3 Errors

The PHY shall use the transmit error code set to transmit an error when indicated by the TE signal from the MAC interface. Decoding errors or a received error code shall be indicated to the MAC with the interface RE signal.

6.4 PHY control

Normal operation begins after power up, if the receive status OK is true and after a successful auto-negotiation (if implemented).

6.5 Bit error rate

The PHY shall maintain a bit error rate (BER) of better than 10^{-12} (BER on the medium).

7 Test

7.1 General

A test mode shall be provided to allow for testing of the transmit waveform. To enable the test mode, it is recommended to use test mode 1 as specified in 40.6.1.1.2 of ISO/IEC 8802-3.

7.2 Tests

The transmitter eye shall be measured with an eye diagram, see Figure 10, while transmitting a pseudo random pattern. The display of the transmitter signal shall contain at least 2 000 traces for an accurate measurement.

7.3 Fixtures

To perform the tests the PHY shall terminate the transmission pair in 100 Ω while measuring the output waveform with an oscilloscope or data acquisition device with a high impedance differential probe.

7.4 Interoperability compliance points

Interoperability compliance points are defined in ISO/IEC 8802-3.

8 Transmitter signal

8.1 General

This Clause details the requirements for the transmitter output signal. The electrical requirements for any MDI port are defined in Clause 10.

8.2 Differential output voltage and accuracy

The peak voltage of output waveform at point S2 during the transmission of a single +1 and -1 symbol shall fall within the range of ± (0,67 V to 0,82 V)X2, and during the transmission of a 0 symbol the voltage shall be 0 (MLT3).

8.3 Scrambling

The scrambling scheme is shown in Figure 9. It shall use the polynomial $1 + x^{14} + x^{15}$.

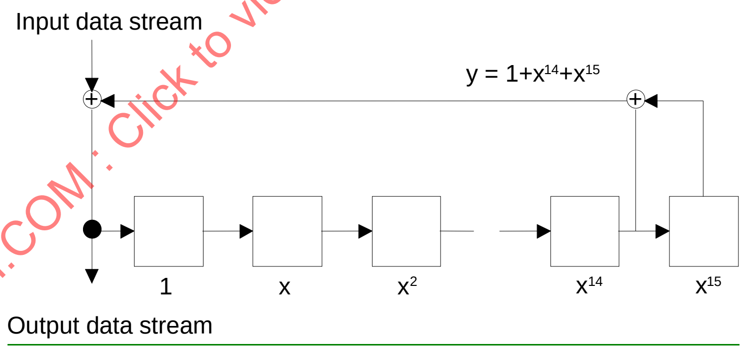
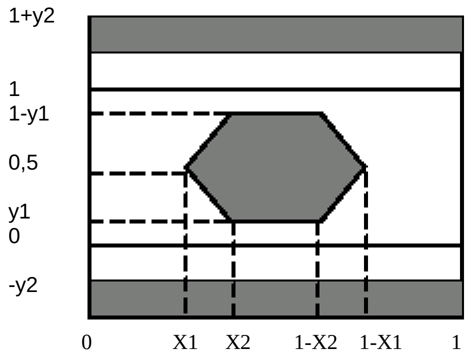


Figure 9 – Scrambler polynomial and correspondent circuit diagram

8.4 Transmit eye diagram

The required transmitter pulse shape characteristics are specified in the form of an eye diagram or mask. Within each level of the MLT3 signal the open eye shall conform to the eye diagram in Figure 10. The eye diagrams of the two levels shall be combined and may be scaled or shifted in time for best concurrent fit.



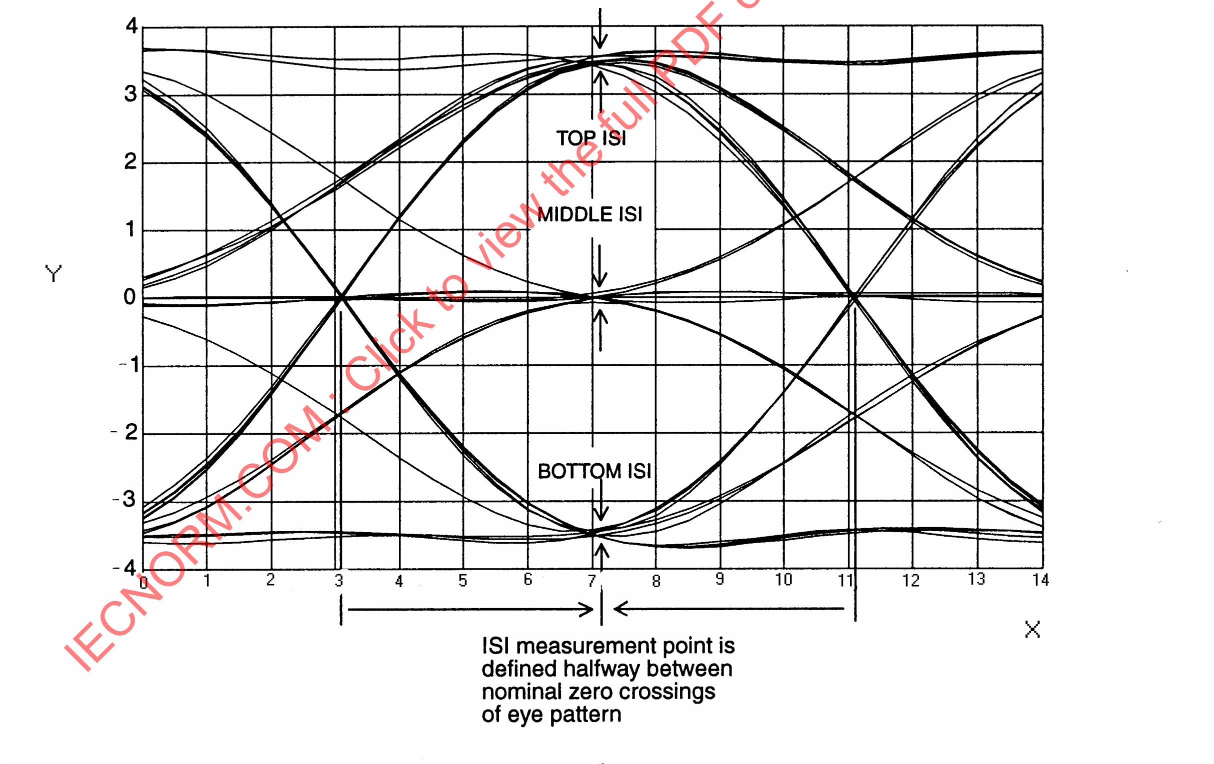
X1=0,09

X2=0,29

Y1=0,2

Y2=0,1

Figure 10 – Transmission eye diagram



The voltage on Y-axis Vy = (value) x 0,41/V

The time on X-axis Ty = (Value) x 0,25/ns

Figure 11 – Transmission eye diagram detail

8.5 Jitter

The maximum jitter is defined in ISO/IEC 8802-3.

9 Receiver signal

9.1 General

This clause details the requirements for the receiver input signal. The electrical requirements for any MDI port are defined in Clause 10.

9.2 Differential input voltage and accuracy

The peak voltage of receiving waveform at point R2 during the transmission of a single +1 and –1 symbol shall fall within the range of ± (0,027 V to 1,64 V), and during the transmission of a 0 symbol the voltage shall be 1 mV (MLT3). These values are based on Class F channel performance as specified in ISO/IEC 11801:2002, the minimum performance of a channel at a maximum length and a minimum transmitter voltage, and 0 m for the minimum length and maximum transmitter voltage. The minimum voltage during 0 symbols results out of the NEXT-values of the cabling channel.

9.3 Descrambling

The same scrambling algorithm as described in 8.3 for descrambling shall be used.

9.4 Receive eye diagram

The required receiver pulse shape characteristics at point R2 are specified in the form of an eye diagram or mask. Within each level of the MLT3 signal the open eye shall conform to the eye diagram in Figure 12. The eye diagrams of the two levels shall be combined and may be scaled or shifted in time for best concurrent fit.

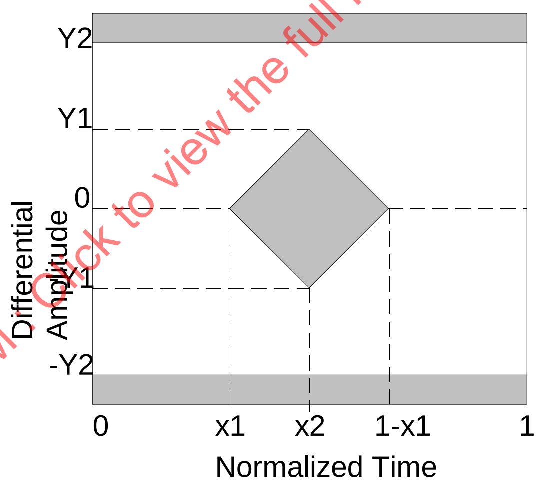


Figure 12 – Receiver eye diagram

Table 6 – Eye diagram mask at points R1 and R2

Coding	X1	Y1	Y2
MLT3	0,3	0,014	0,82