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Third edition
2019-10

Cards and security devices for personal identification — Test methods —

Part 7: Contactless vicinity objects

Cartes et dispositifs de sécurité pour l'identification personnelle — Méthodes d'essai —

Partie 7: Objets sans contact de voisinage

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents).

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For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see www.iso.org/iso/foreword.html.

This document was prepared by Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Cards and security devices for personal identification*.

This third edition cancels and replaces the second edition (ISO/IEC 10373-7:2008), which has been technically revised.

The main changes compared to the previous edition are as follows:

— Annex G and Annex H have been added.

A list of all parts in the ISO/IEC 10373 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at https://www.iso.org/members.html.

Cards and security devices for personal identification — Test methods —

Part 7: Contactless vicinity objects

1 Scope

The ISO/IEC 10373 series defines test methods for characteristics of identification cards according to the definition given in ISO/IEC 7810. Each test method is cross-referenced to one or more base standards, which can be ISO/IEC 7810 or one or more of the supplementary standards that define the information storage technologies employed in identification card applications.

NOTE 1 Criteria for acceptability do not form part of the ISO/IEC 10373 series, but can be found in the International Standards mentioned above.

NOTE 2 Test methods defined in the ISO/IEC 10373 series are intended to be performed separately. A given card is not required to pass through all the tests sequentially.

This document deals with test methods, which are specific to contactless integrated circuit card (vicinity card) technology. ISO/IEC 10373-1 deals with test methods which are common to one or more ICC technologies and other parts in the ISO/IEC 10373 series deal with other technology-specific tests.

Unless otherwise specified, the tests in this document apply exclusively to vicinity cards defined in ISO/IEC 15693-1, ISO/IEC 15693-2 and ISO/IEC 15693-3.

2 Normative reference(s)

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7810, *Identification cards — Physical characteristics*

ISO/IEC 15693-1:2018, *Cards and security devices for personal identification — Contactless vicinity objects — Part 1: Physical characteristics*

ISO/IEC 15693-2:2019, *Cards and security devices for personal identification — Contactless vicinity objects — Part 2: Air interface and initialization*

ISO/IEC 15693-3:2019, *Cards and security devices for personal identification — Contactless vicinity objects — Part 3: Anticollision and transmission protocol*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1.1
base standard
standard which the *test method* (3.1.2) is used to verify conformance to

3.1.2
test method
method for testing characteristics of identification cards for the purpose of confirming their compliance with International Standards

3.2 Symbols and abbreviated terms

DUT	device under test
ESD	electrostatic discharge
f_c	frequency of the operating field
f_{s1}, f_{s2}	frequencies of the subcarriers
H_{max}	maximum field strength of the VCD antenna field
H_{min}	minimum field strength of the VCD antenna field
VCD	vicinity coupling device
VICC	vicinity card

4 Default items applicable to the test methods

4.1 Test environment

Unless otherwise specified, testing shall take place in an environment of temperature 23 °C ± 3 °C (73 °F ± 5 °F) and of relative humidity 40 % to 60 %.

4.2 Pre-conditioning

Where pre-conditioning is required by the test method, the identification cards to be tested shall be conditioned to the test environment for a period of 24 h before testing.

4.3 Default tolerance

Unless otherwise specified, a default tolerance of ±5 % shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

4.4 Spurious inductance

Resistors and capacitors should have negligible inductance.

4.5 Total measurement uncertainty

The total measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

Basic information is given in ISO/IEC Guide 98-3.

5 Static electricity test

ISO/IEC 10373-1 defines test methods which are common to one or more integrated circuit card technologies and other parts in the ISO/IEC 10373 series deal with other technology specific tests.

6 Test apparatus and test circuits

6.1 General

This clause defines the test apparatus and test circuits for verifying the operation of a VICC or a VCD according to ISO/IEC 15693-2 and ISO/IEC 15693-3. The test apparatus includes:

— calibration coil (see 6.2),

— test VCD assembly (see 6.3),

— reference VICC (see 6.4),

— digital sampling oscilloscope (see 6.5).

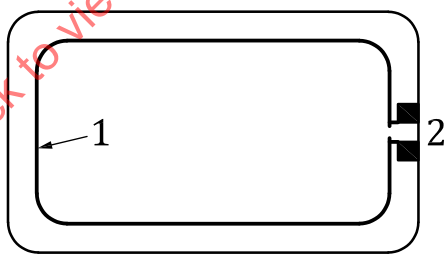
6.2 Calibration coil card

6.2.1 General

This subclause defines the size, thickness and characteristics of the calibration coil.

6.2.2 Size of the calibration coil card

The calibration coil card consists of an area, which shall have the height and width defined in ISO/IEC 7810 for ID-1 type containing a single turn coil concentric with the card outline (see Figure 1).



Key

1 coil 72 × 42 mm (1 turn)

2 connections

Figure 1 — Calibration coil for ISO/IEC 7810 ID-1 outline

6.2.3 Thickness and material of the calibration coil card

The thickness of the calibration coil card shall be 0,76 mm with a tolerance of ±10 %. It shall be constructed of a suitable insulating material.

6.2.4 Coil characteristics

The coil on the calibration coil card shall have one turn. The relative dimensional tolerance shall be ±2 %. The outer size of the coil shall be 72 mm × 42 mm with corner radius 5 mm.

NOTE 1 The area over which the field is integrated is approximately 3 000 mm^2.

The coil is made as a printed coil on PCB plated with 35 µm copper. Track width shall be 500 µm with a relative tolerance of ±20 %. The size of the connection pads shall be 1,5 mm × 1,5 mm.

NOTE 2 At 13,56 MHz the approximate inductance is 200 nH and the approximate resistance is 0,25 Ω.

A high impedance oscilloscope probe (e.g. >1 MΩ, <14 pF) shall be used to measure the (open circuit) voltage in the coil. The resonance frequency of the whole set (calibration coil, connecting leads and probe) shall be above 60 MHz.

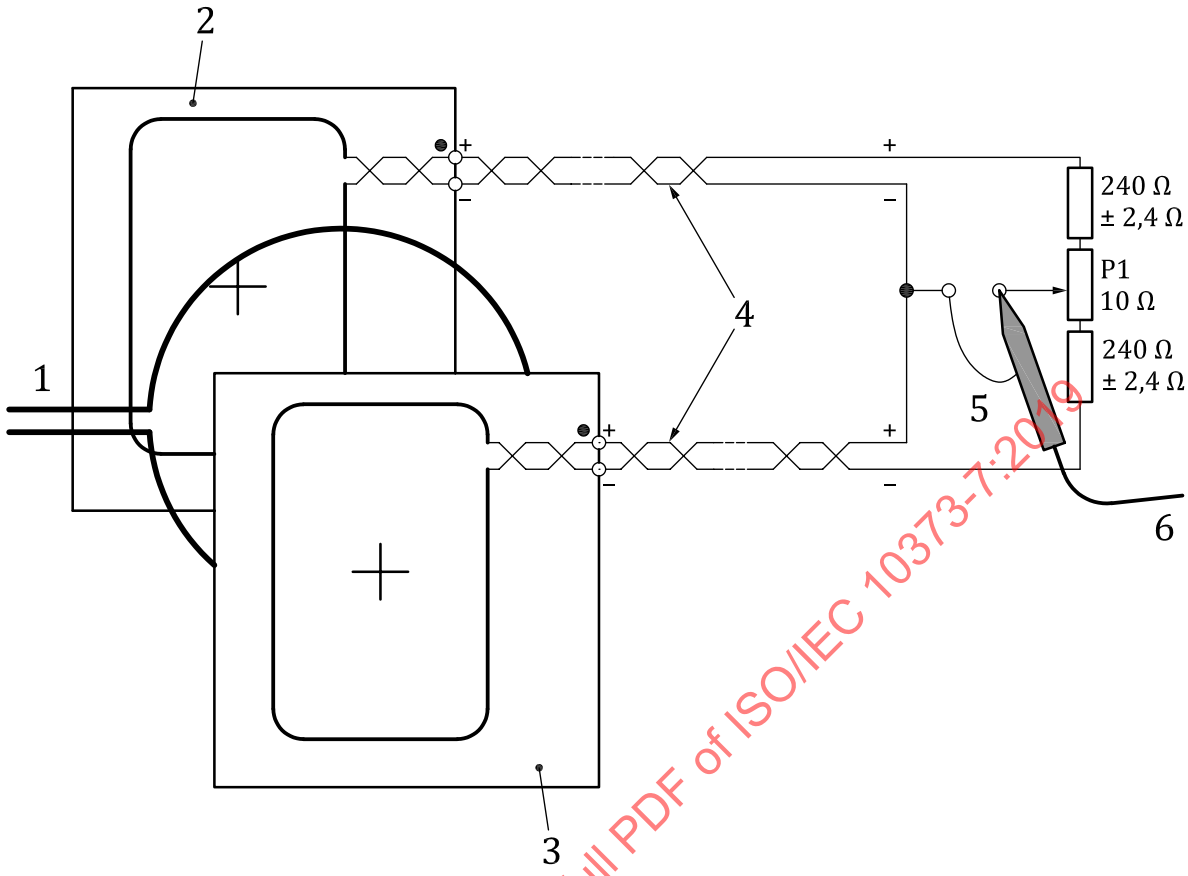
NOTE 3 A parasitic capacitance of the probe assembly of less than 35 pF normally ensures a resonant frequency for the whole set of greater than 60 MHz.

The open circuit calibration factor for this coil is 0,32 V (rms) per A/m (rms) [equivalent to 900 mV (peak-to-peak) per A/m (rms)].

6.3 Test VCD assembly

6.3.1 General

The test VCD assembly for load modulation consists of a 150 mm diameter VCD antenna and two parallel sense coils: sense coil a; and sense coil b. The test set-up is shown in Figure 2. The sense coils are connected such that the signal from one coil is in an opposite phase to the other. The 10 Ω potentiometer P1 serves to fine adjust the balance point when the sense coils are not loaded by a VICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.



Key

1 VCD antenna
2 sense coil b
3 sense coil a
4 identical length of twisted pairs with less than 150 mm.
5 probe
6 to oscilloscope
P1 potentiometer

Figure 2 — Load modulation test circuit

The maximum length of 150 mm of the twisted pairs takes the wider spacing of the sense coils in comparison to the set-up in ISO/IEC 10373-6 into account.

In order to avoid any unintended misalignment in case of an unsymmetrical set-up the tuning range of the potentiometer P1 is only 10 Ω. If the set-up cannot be compensated by the 10 Ω potentiometer P1 the overall symmetry of the set-up should be checked.

The capacitance of the connections and oscilloscope probe should be kept to a minimum for reproducibility.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

6.3.2 Test VCD antenna

The test VCD antenna shall have a diameter of 150 mm and its construction shall conform to the drawings in Annex A. The tuning of the antenna may be accomplished with the procedure given in Annex B.

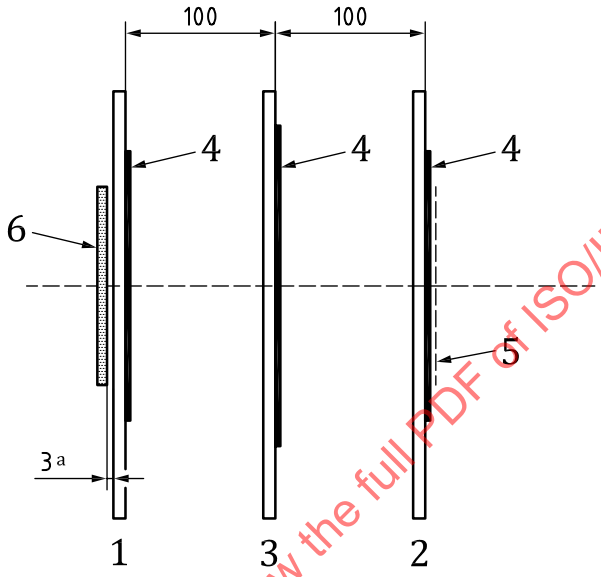
6.3.3 Sense coils

The size of the sense coils is 100 mm × 70 mm. The sense coil construction shall conform to the drawings in Annex C.

6.3.4 Assembly of test VCD

The sense coils and test VCD antenna are assembled in parallel, with the sense and antenna coils coaxial and such that the distance between the active conductors is 100 mm as in Figure 3. The distance between the coil in the DUT and the calibration coil shall be equal with respect to the coil of the test VCD antenna.

Dimensions in millimetres



Key

1 sense coil a
2 sense coil b
3 VCD antenna
4 active conductors
5 calibration coil
6 DUT
a 3 mm air spacing.

NOTE 1 The distance of 100 mm reflects a larger read distance and the 3mm air spacing avoids parasitic effects such as detuning by closer spacing or ambiguous results due to noise and other environmental effects.

NOTE 2 Drawings are not to scale.

Figure 3 — Test VCD assembly

6.4 Reference VICCs

6.4.1 General

Reference VICCs are defined

— to test H_{min} and H_{max} produced by a VCD (under conditions of loading by a VICC);

— to test the ability of a VCD to power a VICC;

— to detect the minimum load modulation signal from the VICC.

6.4.2 Reference VICC for VCD power

Annex D shows the schematic the power test shall use. Power dissipation can be set by the resistor R1 or R2 respectively in order to measure H_{max} and H_{min} as defined in 8.1.2. The resonant frequency can be adjusted with C2.

6.4.3 Reference VICC for load modulation test

A suggested schematic for the load modulation test is shown in Annex E. The load modulation can be chosen to be resistive or reactive.

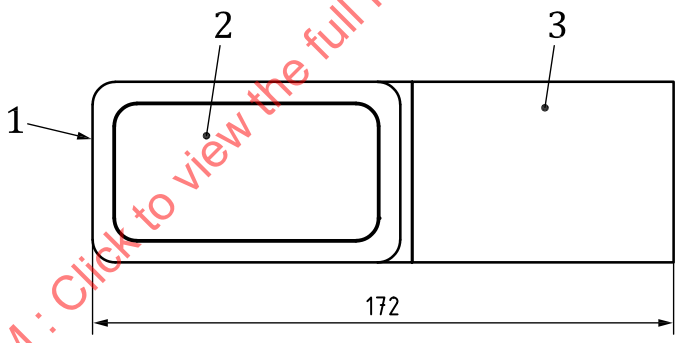
This reference VICC is calibrated by using the test VCD assembly as follows:

The reference VICC is placed in the position of the DUT. The load modulation signal amplitude is measured as described in 7.2. This amplitude should correspond to the minimum amplitude at all values of field strength required by the base standard.

6.4.4 Dimensions of the reference VICCs

The reference VICCs consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required VICC functions, is appended in a way as to allow insertion into the test set-ups described below and so as to cause no interference to the tests. The dimensions shall be as in Figure 4.

Dimensions in millimetres



Key

1 outline ISO/IEC 7810 ID-1 type

2 coil

3 circuitry

NOTE Drawings are not to scale.

Figure 4 — Reference VICC dimensions

6.4.5 Thickness of the reference VICC board

The thickness of the reference VICC active area shall be 0,76 mm, with a tolerance of ±10 %.

6.4.6 Coil characteristics

The coil in the active area of the reference VICC shall have 4 turns and shall be concentric with the area outline.

The outer size of the coils shall be 72 mm × 42 mm with relative tolerance of ±2 %.

The coil is printed on PCB plated with 35 µm copper.

Track width and spacing shall be 500 µm with a relative tolerance of ±20 %.

6.5 Digital sampling oscilloscope

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 100 million samples per second with a resolution of at least 8 bits at optimum scaling. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using external software programmes (Annex F).

7 Functional test — VICC

7.1 Purpose

The purpose of this test is to determine the amplitude of the VICC load modulation signal within the operating field range [H_{min}, H_{max}] as specified in ISO/IEC 15693-2:2019, 6.3 and the functionality of the VICC with the modulation under emitted fields as defined in ISO/IEC 15693-2:2019, Figure 1 and Figure 2.

7.2 Test procedure

Step 1: The load modulation test circuit of Figure 2 and the test VCD assembly of Figure 3 are used.

The RF power delivered by the signal generator to the test VCD antenna shall be adjusted to the required field strength and modulation waveforms as measured by the calibration coil without any VICC. The output of the load modulation test circuit of Figure 2 is connected to a digital sampling oscilloscope. The 10 Ω potentiometer P1 shall be trimmed to minimise the residual carrier. This signal shall be at least 40 dB lower than the signal obtained by shorting one sense coil.

Step 2: The VICC under test shall be placed in the DUT position, concentric and aligned with sense coil a. The RF drive into the test VCD antenna shall be re-adjusted to the required field strength.

Care should be taken to apply a proper synchronization method for low amplitude load modulation.

Exactly two subcarrier cycles of the sampled modulation waveform shall be Fourier transformed. A discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude shall be used. To minimize transient effects, a subcarrier cycle immediately following a non-modulating period shall be avoided. In case of two subcarrier frequencies this procedure shall be repeated for the second subcarrier frequency.

The resulting amplitudes of the two upper sidebands at f_c+f_{s1} and f_c+f_{s2} and the two lower sidebands at f_c-f_{s1} and f_c-f_{s2}, respectively, shall be above the value defined in 8.2 of the base standard.

An appropriate command sequence as defined in ISO/IEC 15693-3 shall be sent by the reference VCD to obtain a signal or load modulation response from the VICC.

7.3 Test report

The test report shall give the measured amplitudes of the upper sidebands at f_c+f_{s1} and f_c+f_{s2} and the lower sidebands at f_c-f_{s1} and f_c-f_{s2} and the applied fields and modulations.

8 Functional test — VCD

8.1 VCD field strength and power transfer

8.1.1 Purpose

This test measures the field strength produced by a VCD with its specified antenna in its operating volume as defined in accordance with the base standard. The test procedure of 8.1.2 is also used to determine that the VCD with its specified antenna shall generate a field not higher than the value specified in ISO/IEC 15693-1:2018, 4.3.

This test uses a reference VICC as defined in Annex D to determine that a specific VCD to be tested is able to supply a certain power to a VICC placed anywhere within the defined operating volume.

8.1.2 Test procedure

Procedure for H_{max} test:

1) Set Jumper J1 to position 'a' to activate R1.

2) Tune the reference VICC to 13,56 MHz.

   NOTE The resonance frequency of the reference VICC is measured by using an impedance analyser or a LCR-meter connected to a calibration coil. The coil of the reference VICC is placed on the calibration coil with (3 ± 0.3) mm spacing, with the axes of the two coils being congruent. The resonance frequency is that frequency at which the reactive part of the measured complex impedance is at maximum.

3) Set Jumper J1 to position “b” to activate R2.

4) Calibrate the reference VICC in the test VCD assembly set to produce H_{max} operating condition for an output voltage of V_{DC} = 3 V by adjusting R2.

5) Position the reference VICC within the defined operating volume of VCD under test.

6) The DC voltage (V_{DC}) across resistor R3 (Annex D) is measured with a high impedance voltmeter and shall not exceed 3 V.

Procedure for H_{min} test:

1) Set Jumper J1 to position “a” to activate R1.

2) Tune the reference VICC to 13,56 MHz.

3) Calibrate the reference VICC in the test VCD assembly set to produce H_{min} operating condition for an output voltage of V_{DC} = 3 V by adjusting R1.

4) Position the reference VICC within the defined operating volume of the VCD under test.

5) The DC voltage (V_{DC}) across resistor R3 is measured with a high impedance voltmeter and shall exceed 3 V.

8.1.3 Test report

The test report shall give the measured values for V_{DC} at H_{min} and H_{max} under the defined conditions.

8.2 Modulation index and waveform

8.2.1 Purpose

This test is used to determine the index of modulation of the VCD field as well as the rise and fall times and the overshoot values as defined in ISO/IEC 15693-2:2019, Figure 1 and Figure 2 within the defined operating volume.

8.2.2 Test procedure

The calibration coil is positioned anywhere within the defined operating volume, and the modulation index and waveform characteristics are determined from the induced voltage on the coil displayed on a suitable oscilloscope.

8.2.3 Test report

The test report shall give the measured modulation index of the VCD field, the rise and fall times and the overshoot values as defined in ISO/IEC 15693-2:2019, Figure 1 and Figure 2 within the defined volume.

8.3 Load modulation reception

This test may be used to verify that a VCD correctly detects the load modulation of a VICC which conforms to the base standard. It is supposed that the VCD has means to indicate correct reception of the subcarrier(s) produced by a test VICC.

Annex E shows a circuit which can be used in conjunction with the test apparatus to determine the sensitivity of a VCD to load modulation within the defined operating volume.

9 Additional test methods

9.1 Additional VICC test methods

The test methods shall be carried out as specified in Annex G.

9.2 Additional VCD test methods

The test methods shall be carried out as specified in Annex H.

Annex A
(normative)

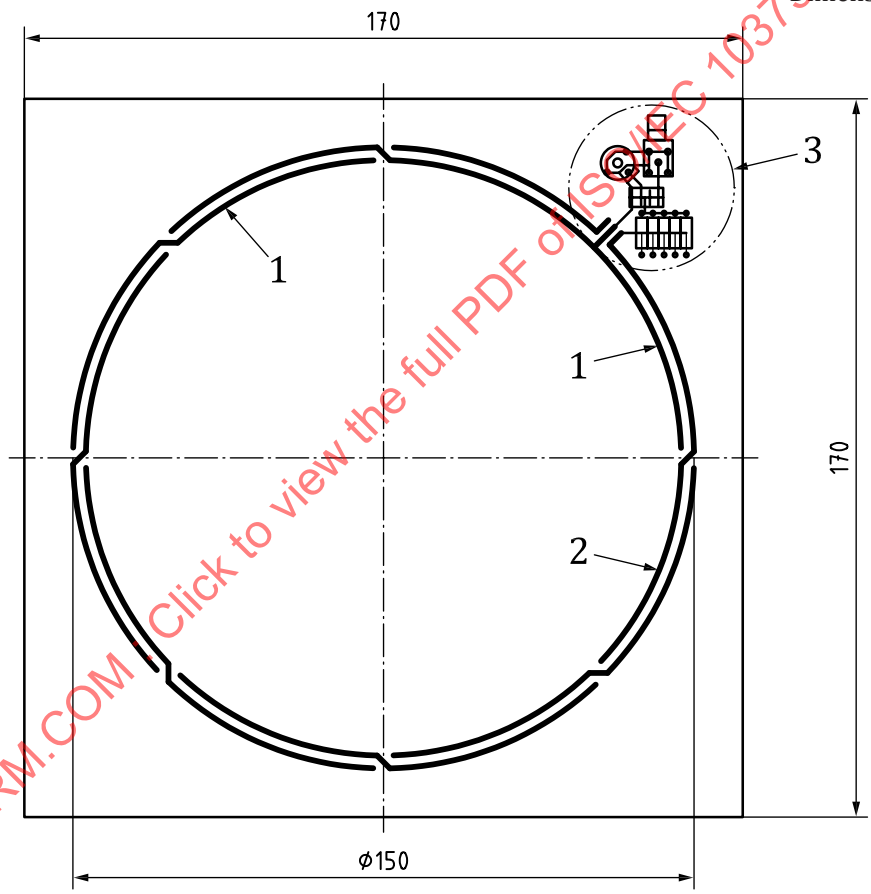
Test VCD antenna

A.1 Test VCD antenna layout including impedance matching network

Figure A.1 and Figure A.2 show the VCD antenna layout.

NOTE The layout of the impedance matching network is informative.

Dimensions in millimetres



Key

1 ground compensation coil
2 antenna coil
3 impedance matching network

NOTE 1 The antenna coil track width is 1,8 mm (except for through-plated holes).

NOTE 2 Starting from the impedance matching network there are crossovers every 45°.

NOTE 3 PCB: FR4 material thickness 1,6 mm, double sided with 35 µm copper.

NOTE 4 The drawing is not to scale.

Figure A.1 — Test VCD antenna layout including impedance matching network (view from front)

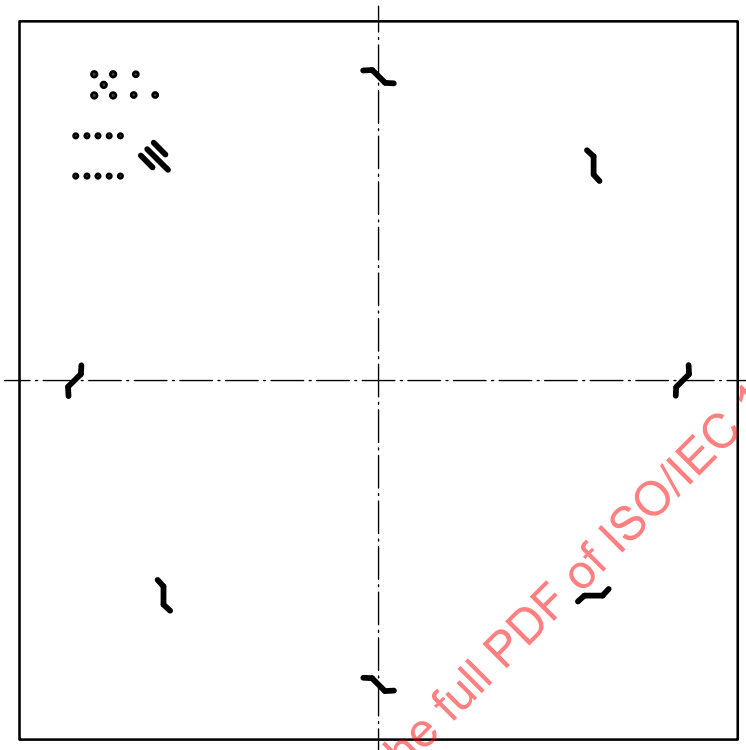


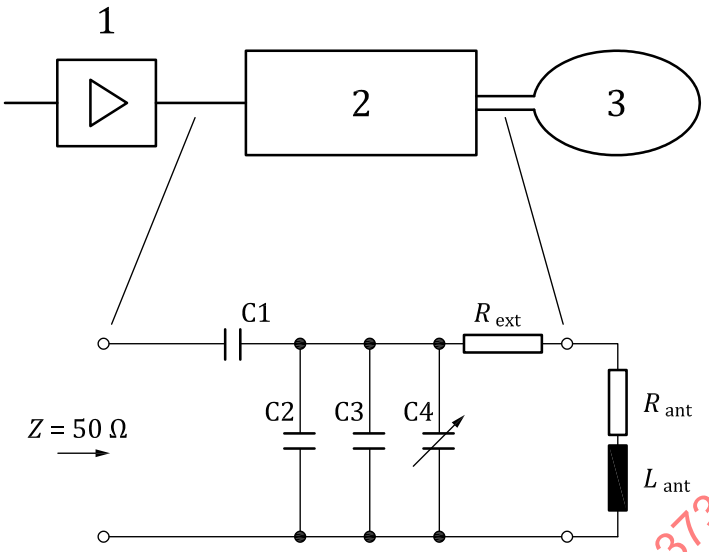
Figure A.2 — VCD antenna layout (view from back)

A.2 Impedance matching network

The antenna impedance (R_{ant}, L_{ant}) is adapted to the function generator output impedance (Z = 50 Ω) by a matching circuit (see Figure A.3). The capacitors C1, C2 and C3 have fixed values. The input impedance phase can be adjusted with the variable capacitor C4 (see Table A.1).

Care shall be taken to keep maximum voltages and maximum power dissipation within the specified limits of the individual components.

The linear low distortion variable output 50 Ω power driver should be capable of emitting appropriate signal sequences. The modulation index should be adjustable in the ranges of 10 % to 30 % and 95 % to 100 %. The output power should be adjustable to deliver H fields in the range of 150 mA/m to 12 A/m. Care should be taken with the duration of fields above the upper operating range of 5 A/m.



Key

1	50 Ω power driver
2	impedance matching network
3	antenna coil
Z	input impedance
R_{ext}	external resistance
R_{ant}	antenna resistance
L_{ant}	antenna inductance
C1, C2, C3, C4	capacitors

Figure A.3 — Impedance matching network

Table A.1 — Component list

Component	Value[a]	Unit
C1	47	pF
C2	180	pF
C3	33	pF
C4	2 to27	pF
R_{ext}	5 × 4.7 (parallel)	Ω

[a] The component table gives typical values which may have to be modified slightly to give more precise adjustment.

C4 shall be adjusted for an input impedance of (50 ± 5) Ω with a phase angle of (0 ± 5) °.

Annex B
(informative)

Test VCD antenna tuning

B.1 General

Figure B.1 and Figure B.2 show the two steps of a simple phase tuning procedure to match the impedance of the antenna to that of the driving generator. After the two steps of the tuning procedure the signal generator shall be directly connected to the antenna output for the tests.

B.2 Step 1

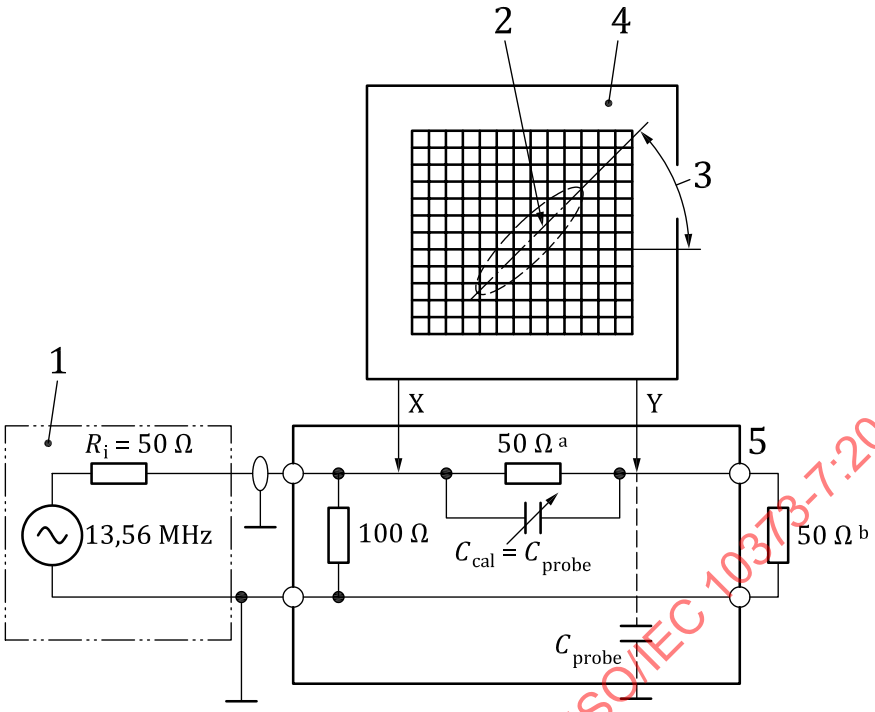
A high precision resistor of 50 Ω, with a tolerance of ±1 % (e.g. 50 Ω BNC resistor) is inserted in the signal line between the signal generator output and an antenna connector. The two probes of the oscilloscope are connected to both sides of the serial reference resistor. The oscilloscope displays a Lissajous figure when it is set in Y to X presentation. The signal generator is set to:

— Wave form: Sinusoidal

— Frequency: 13,56 MHz

— Amplitude: 2 V (rms) – 5 V (rms)

The output is terminated with a second high precision resistor of 50 Ω, with a tolerance of ±1 % (e.g. 50 Ω BNC terminating resistor). The probe, which is in parallel to the output connector, has a small parasitic capacitance C_{probe}. A calibration capacitance C_{cal} in parallel to the reference resistor compensates this probe capacitor if $C_{cal} = C_{probe}$. The probe capacitor is compensated when the Lissajous figure is completely closed.



Key

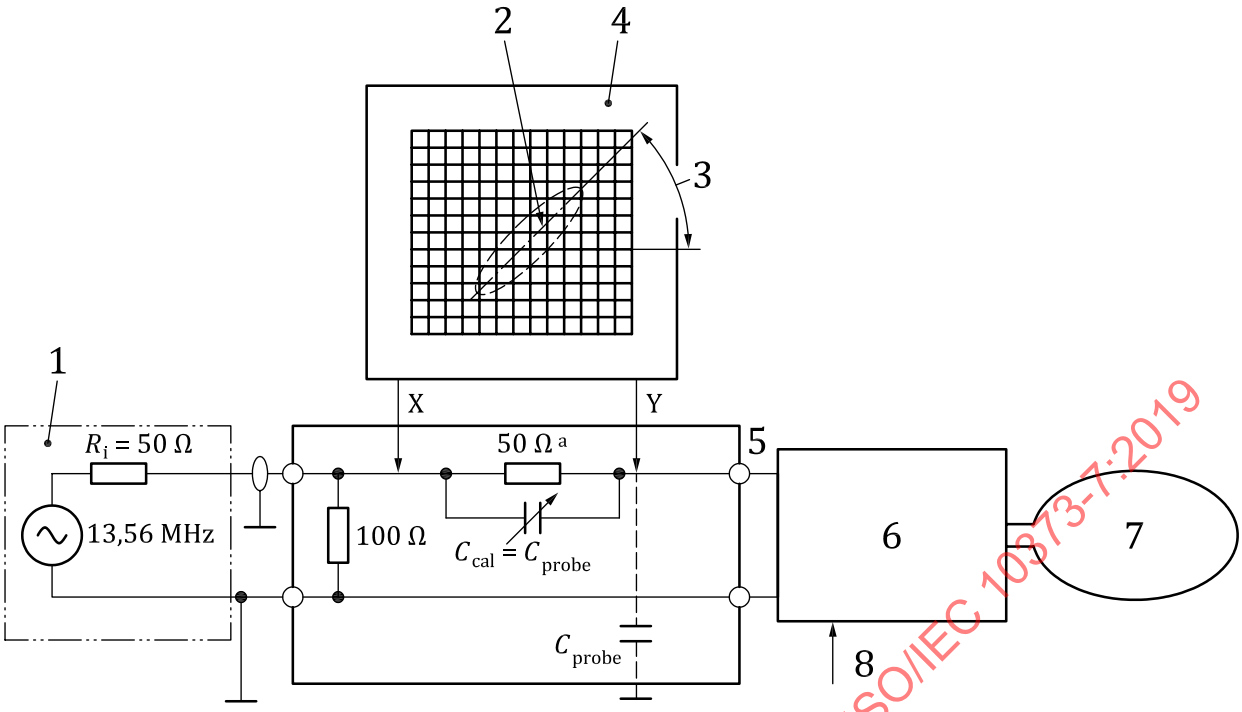
1	signal generator
2	closed figure: Phi = 0
3	angle corresponding to 50 Ω
4	oscilloscope
5	output
R_i	output impedance of signal generator
C_{probe}	parasitic capacitance of probe
C_{cal}	calibration capacitance
a	Reference resistor.
b	Calibration resistor.

Figure B.1 — Calibration set-up (Step 1)

The ground cable shall be run close to the probe to avoid induced voltages caused by the magnetic field.

B.3 Step 2

Using the same values as set for step 1, in the second step the matching circuitry is connected to the antenna output. The capacitor C4 on the antenna board is used to tune the phase to zero.



Key

1	signal generator
2	closed figure: Phi = 0
3	angle corresponding to 50 Ω
4	oscilloscope
5	output
6	impedance matching network
7	antenna coil
8	phase calibration by C4 in the impedance matching network
R_i	output impedance of signal generator
C_{probe}	parasitic capacitance of probe
C_{cal}	calibration capacitance
a	Reference resistor.

Figure B.2 — Calibration set-up (Step 2)

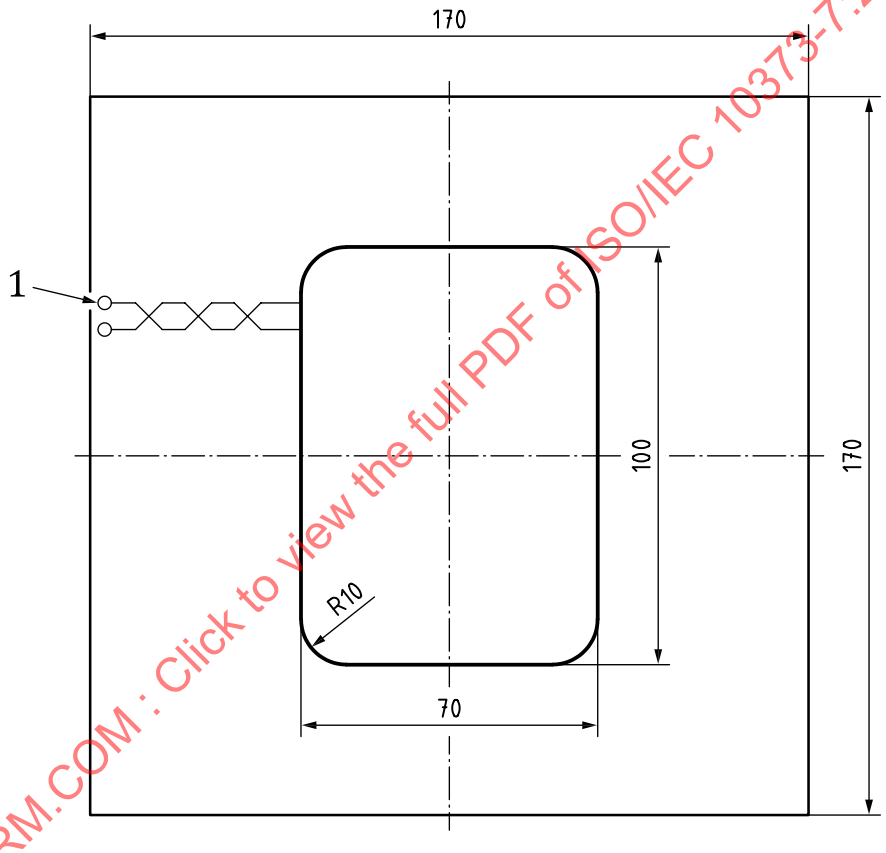
Annex C
(normative)

Sense coil

C.1 Sense coil layout

Figure C.1 illustrates sense coils 1 layout.

Dimensions in millimetres



Key

1 connections

NOTE 1 The sense coils track width is 0,5 mm with a relative tolerance of ±20 % (except for through-plated holes).

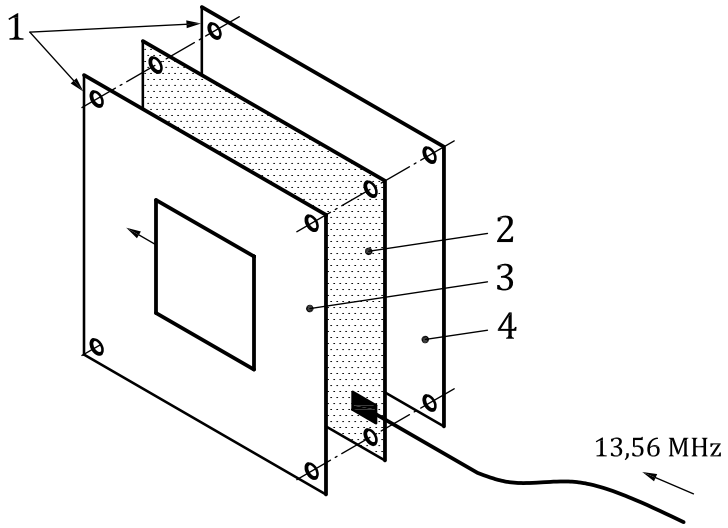
NOTE 2 Sizes of the coils refer to the outer dimensions.

NOTE 3 PCB: FR4 material thickness 1,6 mm, double sided with 35 µm copper.

Figure C.1 — Layout for sense coils a and b

C.2 Sense coil assembly

Figure C.2 illustrates the sense coil assembly.



Key

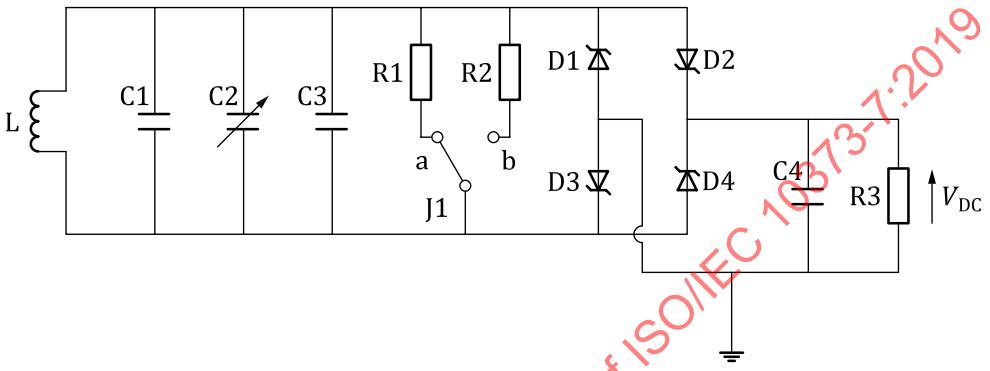
1 connections
2 test VCD antenna
3 sense coil a
4 sense coil b

Figure C.2 — Sense coil assembly

Annex D
(normative)

Reference VICC for VCD power test

The Reference VICC shall have a circuit diagram as defined in Figure D.1 and component values as defined in Table D.1 and Table D.2.



Key

L	antenna coil
C1, C2, C3, C4	capacitors
D1, D2, D3, D4	diodes
R1, R2, R3	resistors
J1	jumper settings
V_{DC}	output voltage

Figure D.1 — Circuit diagram for Reference VICC

Table D.1 — Component list

Component	Value
L	See 6.4.6
C1	Stray capacitance < 5pF
C2	2 ... 10 pF
C3	27 pF
C4	10 nF
D1, D2, D3, D4	See characteristics in Table D.2 (BAR 43 or equivalent)
R1[a]	11 kΩ
R2[a]	91 Ω
R3	100 kΩ
J1	Jumper settings: a: minimum field strength b: maximum field strength

[a] The component table gives typical values for R1 and R2 which may have to be modified slightly to give more precise adjustment (see 8.1.2).

Table D.2 — Specification of basic characteristics of D1, D2, D3, D4

Symbol	Test Condition at T_j = 25 °C	Typ.	Max.	Unit
V_F	I_F=2mA		0,33	V
C	V_R=1V, F=1 MHz	7		pF
t_{rr}	I_F=10mA, I_R=10mA, I_{rr}=1mA		5	ns

Key

V_F: Forward voltage drop

V_R: Reverse voltage

I_F: Forward current

I_R: Reverse current

t_{rr}: Reverse recovery time

I_{rr}: Reverse recovery current

T_j: Junction temperature

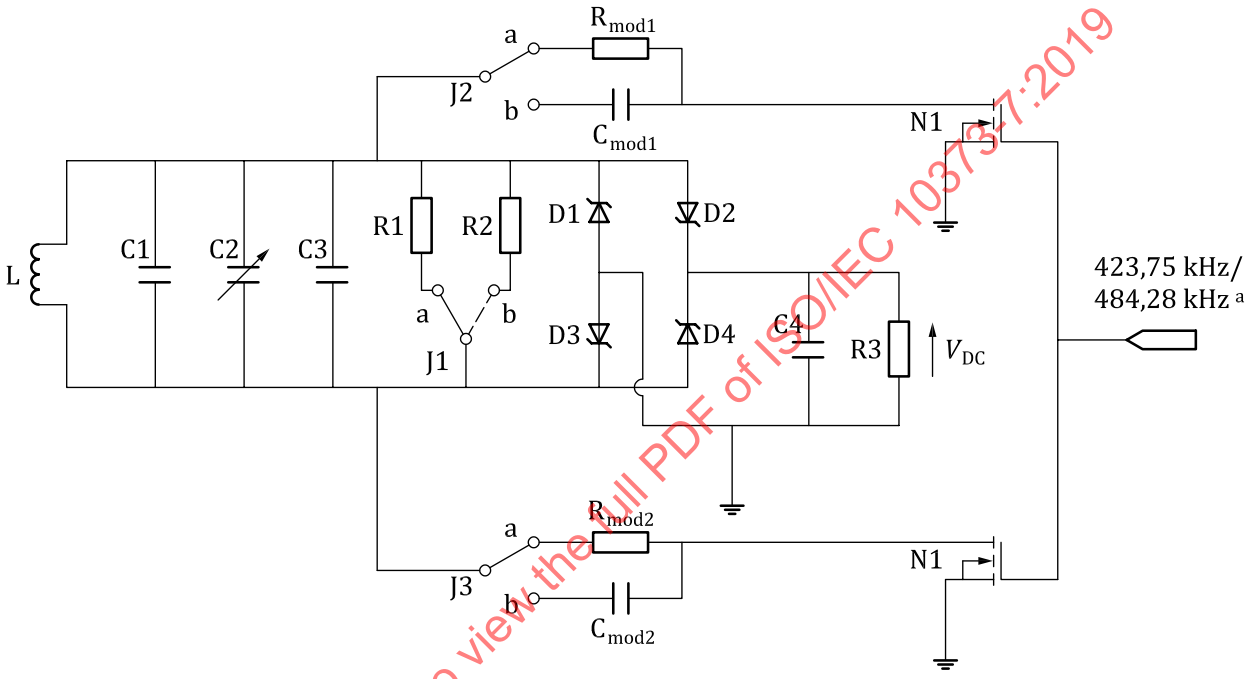
F: Frequency

C: Junction capacitance

Annex E
(informative)

Reference VICC for load modulation test

The Reference VICC for load modulation test shall have a circuit diagram as defined in Figure E.1 and component values as defined in Table E.1 and Table E.2.



Key

L	antenna coil
C1, C2, C3, C4, C_{mod1}, C_{mod2}	capacitors
D1, D2, D3, D4	diodes
R1, R2, R3, R_{mod1}, R_{mod2}	resistors
J1, J2, J3	jumper setting
N1, N2	N-MOS transistor
V_{DC}	output voltage
a	Load switching signal

Figure E.1 — Circuit diagram for Reference VICC for load modulation test

Table E.1 — Adjust following components for required emulation

Component	Function	Value
C2	adjust resonance	between 2 pF and 10 pF
C_{mod1}, C_{mod2}	capacitive modulation	between 3,0 pF and 120 pF
R_{mod1}, R_{mod2}	resistive modulation	between 100 Ω and 2,7 kΩ

Table E.2 — Component list

Component	Value
R1	11 kΩ
R2	91 Ω
R3	100 kΩ
D1, D2, D3, D4	As defined in Table D.1
L	see 6.4.6
C1	Stray capacitance < 5 pF
C3	27 pF
C4	10 nF
J1	Jumper settings: a: minimum field strength b: maximum field strength
J2, J3	Jumper settings: a: resistance load b: capacitive load
N1, N2	N-MOS transistor with low parasitic capacitance

Annex F
(informative)

Program for evaluation of the spectrum

The following program written in C language gives an example for the calculation of the magnitude of the spectrum from the VICC.

```
/*****************************************************************/
/***  This program calculates the fourier coefficients         ***/
/***  of load modulated voltage of a VICC according            ***/
/***  the ISO/IEC 10373-7 Test methods.                        ***/
/***  The coefficient are calculated for the frequency         ***/
/***    Carrier:            13.5600 MHz                        ***/
/***    Subcarrier:         423.75 kHz  / 484.286 kHz          ***/
/***    see #define N_FSUB:   32             28                ***/
/***    Upper sideband:     13.9838 MHz / 14.0443 MHz          ***/
/***    Lower sideband:     13.1363 MHz / 13.0757 MHz          ***/
/*****************************************************************/
/*** Input:                                                    ***/
/***  File in CSV Format containing a table of two             ***/
/***  columns (time and test VCD output voltage vd, clause 7)***/
/***                                                           ***/
/***  data format of input-file:                               ***/
/***  --------------------------                               ***/
/***  - one data-point per line:                               ***/
/***     {time[seconds], sense-coil-voltage[volts])            ***/
/***  - contents in ASCII, no headers                          ***/
/***  - data-points shall be equidistant time                  ***/
/***  - minimum sampling rate: 100 MSamples/second             ***/
/***  - modulation waveform centred                            ***/
/***      (max. tolerance: half of subcarrier cycle)           ***/
/***                                                           ***/
/***    "screen-shot of centred modulation-waveform            ***/
/***     with 8 subcarrier cycles":                            ***/
/***                                                           ***/
/***    XXXXXXXXXX  xx  xx  xx  xx  xx  xx  xx  xxXXXXXXXXXX   ***/
/***    XXXXXXXXXX  xx  xx  xx  xx  xx  xx  xx  xxXXXXXXXXXX   ***/
/***    XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX   ***/
/***    XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX   ***/
/***    XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX   ***/
/***    XXXXXXXXXXxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxXXXXXXXXXX   ***/
/***    XXXXXXXXXX  xx  xx  xx  xx  xx  xx  xx  xxXXXXXXXXXX   ***/
/***    XXXXXXXXXX  xx  xx  xx  xx  xx  xx  xx  xxXXXXXXXXXX   ***/
/***    |-------------------cc-----------------------|  ***/
/***  example for spreadsheet file (start in next line):       ***/
/***    (time)      (voltage)                                  ***/
/***  3.00000e-06 , 1.00                                       ***/
/***  3.00200e-06 , 1.01                                       ***/
/***  .....                                                    ***/
/*****************************************************************/
/*** RUN: Modtst7 [filename1[.csv] ... filename[.csv] ]       ***/
/*****************************************************************/
#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <math.h>
#define MAX_SAMPLES 5000
#define N_FSUB 32.0F    /* sidebands: 13.9838 MHz / 13.1363 MHz */
/* #define N_FSUB 28.0F /* sidebands: 14.0443 MHz / 13.0757 MHz */
float  pi;   /* pi=3.14.... */

/* Array for time and sense coil voltage vd*/
float vtime[MAX_SAMPLES]; /* time array  */
float vd[MAX_SAMPLES];    /* Array for different coil voltage */
```

```
/*************************************************************/
/***    Read CSV File  Function                            ***/
/***                                                       ***/
/***    Description:                                       ***/
/***    This function reads the table of time and sense coil ***/
/***    voltage from a File in CSV Format                  ***/
/***                                                       ***/
/***    Input: filename                                    ***/
/***                                                       ***/
/***    Return: Number of samples  (sample Count)          ***/
/***            0  if an error occurred                    ***/
/***                                                       ***/
/***    Displays Statistics:                               ***/
/***                                                       ***/
/***    Filename, SampleCount, Sample rate, Max/Min Voltage  ***/
/*************************************************************/
int readcsv(char* fname)
{
   float a,b;
   float max_vd,min_vd;
   int i;
   FILE     *sample_file;

   /************ Open File **********************************/
   if (!strchr(fname, '.'))
      {
               strcat(fname, ".csv");
      }

   if ((sample_file = fopen(fname, "r")) == NULL)
      {
           printf("Cannot open input file %s.\n",fname);
               return 0;
      }

   /*********************************************************/
   /* Read CSV File                                         */
   /*********************************************************/
   max_vd=-1e-9F;
   min_vd=-max_vd;
   i=0;

   while (!feof(sample_file))
      {
      if (i>=MAX_SAMPLES)
      {
          printf("Warning: File truncated !!!\n");
          printf("To much samples in file %s\b\n",fname);
          break;
      }
      fscanf(sample_file,"%f,%f\n", &a, &b);
      vtime[i] = a;
      vd[i] = b;
      if (vd[i]>max_vd) max_vd=vd[i];
      if (vd[i]<min_vd) min_vd=vd[i];
      i++;
      }
   fclose(sample_file);

   /************ Displays Statistics  ***********************/
   printf("\n***********************************************\n");
   printf("\nStatistics: \n");
   printf(" Filename    : %s\n",fname);
   printf(" Sample count: %d\n",i);
   printf(" Sample rate : %1.0f MHz\n",1e-6/(vtime[1]-vtime[0]));
   printf(" Max(vd)     : %4.0f mV\n",max_vd*1000);
   printf(" Min(vd)     : %4.0f mV\n",min_vd*1000);

return i;
}/*************** End ReadCsv **************/
```

```
/*****************************************************************/
/***    DFT : Discrete Fourier Transform                       ***/
/*****************************************************************/
/***    Description:                                           ***/
/***    This function calculate the Fourier coefficient        ***/
/***                                                           ***/
/***    Input: Number of samples                               ***/
/***    Global Variables:                                      ***/
/***                                                           ***/
/***    Displays Results:                                      ***/
/***                                                           ***/
/***     Carrier coefficient                                   ***/
/***     Upper sideband coefficient                            ***/
/***     Lower sideband coefficient                            ***/
/***                                                           ***/
/*****************************************************************/

void dft(int count)
{
   float c0_real,c0_imag,c0_abs,c0_phase;
   float c1_real,c1_imag,c1_abs,c1_phase;
   float c2_real,c2_imag,c2_abs,c2_phase;
   int   N_data,center,start,end;
   float w0,wu,wl;

   int i;

   w0=(float)(13.56e6*2.0)*pi;  /* carrier        13.56 MHz */
   wu=(float)(1.0+1.0/N_FSUB)*w0; /* upper sideband 13.98 MHz */
   wl=(float)(1.0-1.0/N_FSUB)*w0; /* lower sideband 13.14 MHz */

   c0_real=0;  /* real part of the carrier fourier coefficient */
   c0_imag=0;  /* imag part of the carrier fourier coefficient */
   c1_real=0;  /* real part of the up. sideband fourier coefficient */
   c1_imag=0;  /* imag part of the up. sideband fourier coefficient */
   c2_real=0;  /* real part of the lo. sideband fourier coefficient */
   c2_imag=0;  /* imag part of the lo. sideband fourier coefficient */

   center=(count+1)/2; /*  center address */

   /********** signal selection  ******************************/

   /*   Number of samples for two subcarrier periods  */

   N_data=(int)(0.5+2.0*N_FSUB/(vtime[2]-vtime[1])/13.56e6F);
          /* Note: (vtime[2]-vtime[1]) are the scope sample rate */

   start=center-(int)(N_data/2.0+0.5);
   end=start+N_data-1;

   /*****************    DFT ********************************/
   for(i=start;i<=end;i++)
      {
      c0_real=c0_real+vd[i]*(float)cos(w0*vtime[i]);
      c0_imag=c0_imag+vd[i]*(float)sin(w0*vtime[i]);
      c1_real=c1_real+vd[i]*(float)cos(wu*vtime[i]);
      c1_imag=c1_imag+vd[i]*(float)sin(wu*vtime[i]);
      c2_real=c2_real+vd[i]*(float)cos(wl*vtime[i]);
      c2_imag=c2_imag+vd[i]*(float)sin(wl*vtime[i]);
      }

   /*******************    DFT scale ***************************/
   c0_real=2.0F*c0_real/(float)(N_data);
   c0_imag=2.0F*c0_imag/(float)(N_data);
   c1_real=2.0F*c1_real/(float)(N_data);
   c1_imag=2.0F*c1_imag/(float)(N_data);
   c2_real=2.0F*c2_real/(float)(N_data);
   c2_imag=2.0F*c2_imag/(float)(N_data);

   /*************** absolute fourier coefficient     **********/
```

```
   c0_abs=(float)sqrt(c0_real*c0_real + c0_imag*c0_imag);
   c1_abs=(float)sqrt(c1_real*c1_real + c1_imag*c1_imag);
   c2_abs=(float)sqrt(c2_real*c2_real+c2_imag*c2_imag);

   /**************    Phase of fourier coefficient    **********/
   c0_phase=(float)atan2(c0_imag,c0_real);
   c1_phase=(float)atan2(c1_imag,c1_real);
   c2_phase=(float)atan2(c2_imag,c2_real);

   /**************  Result Display    ************************/
   printf("\n\nResults: \n");

   printf("Carrier        ");
   printf("Abs: %7.3fmV  ",1000*c0_abs);
   printf("Phase: %3.0fdeg\n",c0_phase/pi*180);

   printf("Upper sideband ");
   printf("Abs: %7.3fmV  ",1000*c1_abs);
   printf("Phase: %3.0fdeg\n",c1_phase/pi*180);

   printf("Lower sideband ");
   printf("Abs: %7.3fmV  ",1000*c2_abs);
   printf("Phase: %3.0fdeg\n\n",c2_phase/pi*180);
   printf("\n***********************************************\n");
   return;
}/*************** End DFT ***************/

/*************************************************************/
/***    MAIN  LOOP                                         ***/
/*************************************************************/
int main(unsigned short paramCount,char *paramList[])
{
   char fname[256];
   unsigned int  i,sample_count;
   pi = (float)atan(1)*4; /* calculate pi */

   printf("\n***********************************************\n");
   printf("\n****  ISO/IEC 10373-7 VICC Test Program    ****\n");
   printf("\n****  Version: 1.1     JUL 2000            ****\n");
   printf("\n***********************************************\n");

   /************* No Input Parameter             *****************/
   if (paramCount==1)
      {
      printf("\nCSV File name :");
      scanf("%s",fname);
      if (!strchr(fname, '.'))   strcat(fname, ".csv");
      if (!(sample_count=readcsv(fname))) return;

      dft(sample_count);
      }
   else
      {
      /************* Input Parameter Loop     ****************/
      for (i=1;i<paramCount;i++)
         {
         strcpy(fname,paramList[i]);

         if (!strchr(fname, '.'))   strcat(fname, ".csv");
         if (!(sample_count=readcsv(fname))) break;
         dft(sample_count);
         }
      }
   return;
}/********************** End Main  ************************/
```

Annex G
(normative)

Additional VICC test methods

G.1 VICC-test-apparatus and accessories

G.1.1 General

This clause defines the test apparatus and test circuits for verifying the operation of a VICC according to ISO/IEC 15693-2 and ISO/IEC 15693-3. The test apparatus includes the following:

— calibration coil (see 6.2);

— test VCD assembly (see 6.3);

— reference VICC (see 6.4);

— digital sampling oscilloscope (see 6.5).

Care shall be taken to ensure that the results are not affected by the RF performance of the test circuits.

G.1.2 Emulating the I/O protocol

The VICC-test-apparatus shall be able to emulate all protocols, which are required to test a VICC.

G.1.3 Generating the I/O character timing in reception mode

The VICC-test-apparatus shall be able to generate the I/O bit stream according to ISO/IEC 15693-2. These parameters will be described in each of the tests below.

G.1.4 Measuring and monitoring the RF I/O protocol

The VICC-test-apparatus shall be able to measure and monitor the timing of the logical low and high states of the RF Input/Receive line relative to the clock frequency. The VICC-test-apparatus shall be able to monitor the VICC subcarrier.

G.1.5 Protocol analysis

The VICC-test-apparatus shall be able to analyse the I/O-bit stream in accordance with protocol as specified in ISO/IEC 15693-2 and ISO/IEC 15693-3 and extract the logical data flow for further protocol analysis.

G.1.6 RFU fields and values

RFU fields should be constantly monitored during the testing and shall always be verified to contain the assigned default value. A test shall be FAIL and the tested VICC shall be declared non-compliant in case an RFU field is not set to its default value at any time.

Functional fields should be constantly monitored during the testing and shall always be verified to contain only functional values documented in the standard or proprietary values documented in the standard. A test shall be FAIL and the tested VICC shall be declared non-compliant in case a functional field is not set to said values (and thus is set to an RFU or restricted value) at any time.

G.1.7 Measuring timing

G.1.7.1 Protocol timing

G.1.7.1.1 VICC waiting time before transmitting its response after reception of an EOF from the VCD

a) **Test of Inventory command with 1 slot**

Precondition: None

Command: Inventory, 1 slot, mask length=0

Flag options to be tested: Single subcarrier and dual subcarriers,
low data rate and high data rate

To be measured: t_1

Defined in ISO/IEC 15693-3:2019, 9.2.

b) **Test of Inventory command with 16 slots**

Precondition: Lower 4 bits of the VICC UID shall be different from 0h. (VICC shall respond in a slot different from the first one)

Command: Inventory, 16 slot, mask length=0

Flag options to be tested: Dual subcarriers
High data rate

To be measured: t_1

Defined in ISO/IEC 15693-3:2019, 9.2.

c) **Test of all other commands having Immediate VICC reply**

Precondition: Command is supported by the VICC

Command: All supported commands having Immediate VICC reply time

Flag options to be tested: Dual subcarriers
High data rate

To be measured: t_1

Defined in ISO/IEC 15693-3:2019, 9.2.

d) **Test of all commands having Write alike VICC reply**

Precondition: Command is supported by the VICC, option flag setting is supported by the VICC

Command: All supported commands having Write alike VICC reply

Flag options to be tested: Dual subcarriers
High data rate
Option flag set and option flag not set

To be measured: twrite_alike_response

twrite_alike_response:

— Option flag not set
t_{1nom}+a multiple of 4 096/f_c ± 32/f_c
Less than 20 ms

— Option flag set
t_1 after EOF

Defined in ISO/IEC 15693-3:2019, 9.2, 9.6.

e) **Test of all commands supporting waiting time extension reply**

Precondition:	Command is supported by the VICC
Command:	All supported commands supporting waiting time extension reply
Flag options to be tested:	Single subcarrier High data rate Option flag set and option flag not set
To be measured:	t_response

t_response:

— t_{1nom}+a multiple of 4 096/f_c ± 32/f_c
Less than 20 ms

Defined in ISO/IEC 15693-3:2019, 9.9.

G.1.7.1.2 VICC modulation ignore time after reception of an EOF from the VCD

Precondition:	Lower 4 bits of the VICC UID shall be different from 0h. (VICC shall respond in a slot different from the first one)
Command:	Inventory, 16 slot, mask length=0
Flag options to be tested:	Dual subcarriers High data rate

An additional 10 % modulated EOF shall be transmitted from the VCD after the inventory command.

Timing of additional EOF: ~1ms, ~2ms, ~3ms after the EOF of the inventory command

To be measured: VICC responds in the correct slot ignoring the additional 10 % EOF

Defined in ISO/IEC 15693-3:2019, 9.3.

G.1.7.1.3 In-process reply

Precondition:	Command is supported by the VICC
Command:	All supported commands having In-process VICC reply
Flag options to be tested:	Dual subcarriers High data rate

To be measured: timing of Barker reply, timing of final reply

— Barker reply (maybe final response)
t_{1nom}+a multiple of 4 096/f_c ± 32/f_c
Less than 20 ms from EOF of last command or last Barker response

— Final reply
t_{1nom}+a multiple of 4 096/f_c ± 32/f_c
Less than 20 ms from EOF of last command or last Barker response

Defined in ISO/IEC 15693-3:2019, 9.8.2.1.

G.1.7.1.4 Security timeout

Precondition: Security timeout is supported by the VICC

Command sequence to be tested:

1) Security command with parameter(s) which result in a cryptographic error
2) Security command with valid parameters

To be measured: Within the security timeout there shall be no response of the VICC to a valid security command

— min 20 ms, max 200 ms

Defined in ISO/IEC 15693-3:2019, 9.7.

G.1.7.2 Test setup

See Figure 2.

G.1.7.3 Test procedure

— The test shall be performed at least using H_{min} and H_{max}. H field strengths between H_{min} and H_{max} can optionally be tested.

— The load modulation test circuit as described in G.1.7.2 shall be used.

— Test sequence:

  — Step 1: The RF power delivered by the signal generator to the test VCD antenna shall be adjusted to the required field strength and modulation waveforms as measured by the calibration coil without any VICC.

  — Step 2: The VICC under test shall be placed in the DUT position, concentric and aligned with sense coil a. The RF drive into the test VCD antenna shall be re-adjusted to the required field strength.

— VCD reference point for VICC timing measurements is the end of t_1 (t_2) in ISO/IEC 15693-2:2019, Figure 1 and Figure 2. The VICC response timing is counted from the start of the first rising edge of the load modulation (load modulation switch is closed).

— VICC reference point for VCD timing measurements is the last rising edge of the load modulation (load modulation switch is closed) in ISO/IEC 15693-2:2019, Figure 16 and Figure 17 corrected to the logical end of the EOF. The VCD timing is counted at the start of t_1 in ISO/IEC 15693-2:2019, Figure 1 and Figure 2.

G.2 General considerations

G.2.1 Testing of anticollision

G.2.1.1 General

These tests verify the correct implementation of the anticollision procedures as described in ISO/IEC 15693-3.

G.2.1.2 General test outline

Checking that the VICC responded appropriately and in the correct time requires to know its UID. Therefore the first step in the test procedure will be to acquire the UID of the VICC in the response of a valid Inventory 1 slot command with no mask.

An exhaustive test of the VICC response in each of the 16 slots of the Inventory 16 slots would require to master the UID of the VICC. This is considered as non-practical so the test will be limited to check the response in two deterministic slots and in one random slot.

For the 16-slots Inventory test the Test VCD shall mix 10 % and 100 % modulation EOF to switch to the next slot. Timings for sending the EOF shall be according to ISO/IEC 15693-3:2019, 9.4 and 9.5.

G.2.1.3 Inventory 1-slot test procedure

The AFI flag is always set to 0. The following steps shall be performed at an operating field strength between H_{min} and H_{max}:

a) Place the VICC into the field and adjust it.

b) Switch the RF operating field off for a minimum time for resetting a VICC (see ISO/IEC 15693-3).

c) Switch the RF operating field on.

d) Do a delay of 1 ms.

e) Send a valid Inventory command frame: 1 slot, Mask Length = '00' (no mask).

   1) The VICC shall respond with DSFID and UID.

   2) Test VCD acquires the UID.

f) Send a valid Inventory command frame: 1 slot, Mask Length = '01', Mask Value = '00000000'.

g) Send a valid Inventory command frame: 1 slot, Mask Length = '01', Mask Value = '00000001'.

   1) The VICC shall respond to one of the two commands in steps f) and g) depending on its UID.

   2) Test VCD check the VICC has responded in the correct slot with DSFID and UID.

h) Send a valid Inventory command frame: 1 slot, Mask Length = '3C', Mask Value = UID – (E).

   1) The VICC shall respond.

i) Send a valid Inventory command frame: 1 slot, Mask Length = '3C', Mask Value = UID' – (E).

   1) UID' means at least 1 bit mismatch versus the UID of the VICC under test (mask not matching).

   2) The VICC shall not respond.

G.2.1.4 Inventory 16-slots test procedure

The following steps shall be performed at an operating field strength between H_{min} and H_{max}:

a) Send a valid Inventory command frame: 16 slots, Mask Length = '00': Inventory command followed by 15 isolated EOFs.

   1) The VICC shall respond on one slot only depending on the value of the lowest nibble (b0 to b3) of its UID.

   2) Test VCD to check response in the correct slot.

b) Send a valid Inventory command frame: 16 slots, Mask Length = '3C', Mask Value = UID – (E): Inventory command followed by 15 isolated EOFs.

   1) The VICC shall respond on 15th slot (after the 14th EOF).

c) Send a valid Inventory command frame: 16 slots, Mask Length = '3C', Mask Value = UID' – (E): Inventory command followed by 15 isolated EOFs.

   1) UID' means at least 1 bit mismatch versus the UID of the VICC under test.

   2) The VICC shall not respond.

d) Send a valid Inventory command frame: 16 slots, Mask Length = '38', Mask Value = UID – (E0): Inventory command followed by 15 isolated EOFs.

   1) The VICC shall respond on the 1st slot (after the Inventory command).

e) Send a valid Inventory command frame: 16 slots, Mask Length = '38', Mask Value = UID' – (E0): Inventory command followed by 15 isolated EOFs.

   1) UID' means at least 1 bit mismatch versus the UID of the VICC under test.

   2) The VICC shall not respond.

G.2.2 Testing of optional commands

G.2.2.1 Use of test commands

G.2.2.1.1 General

There shall be one test command chosen by the test organization from the list of supported optional commands. The following tests shall be performed using all combinations of single subcarrier, dual subcarriers, low data rate and high data rate. The VCD shall use 100 % modulation. The VCD shall set the option flag to 0. The test command shall be tested at an operating field strength between H_{min} and H_{max}.

G.2.2.1.2 Test command in the Ready State

Table G.1 shows the test command and its response in the Ready State.

Precondition: Ready State with access to unprotected memory blocks.

Table G.1 — Test command in the Ready State

Step	VCD		VICC	Comment
1	Test command (non-addressed mode)	→		
		←	Response	

Table G.1 *(continued)*

Step	VCD		VICC	Comment
2	Test command (addressed mode [matching UID])	→		
			Response	
		←		
3	Test command (addressed mode [non-matching UID])	→		
			Mute	
		←		
4	Test command (select mode)	→		
			Mute	
		←		

G.2.2.1.3 Test command in the Selected State

Table G.2 shows the test command and its response in the Selected State.

Precondition: Selected State with access to unprotected memory blocks.

Table G.2 — Test command in the Selected State

Step	VCD		VICC	Comment
1	Test command (non-addressed mode)	→		
			Response	
		←		
2	Test command (addressed mode [matching UID])	→		
			Response	
		←		
3	Test command (addressed mode [non-matching UID])	→		
			Mute	
		←		
4	Test command (select mode)	→		
			Response	
		←		

G.2.2.2 All supported optional commands

G.2.2.2.1 General

Unless otherwise specified, these tests shall be run using single subcarrier, high data rate, addressed mode. The commands shall be tested at an operating field strength between H_{min} and H_{max}. Memory access ranges shall be specified by the manufacturer for each command. Responses shall be according to ISO/IEC 15693-3:2019, Clause 10.

G.2.2.2.2 Scenario G.1: Read single block command

Table G.3 shows the test scenario for the Read single block command.

Precondition: Read access to unprotected memory blocks.

Table G.3 — Scenario G.1: Read single block command

Step	VCD		VICC	Comment
1	Read single block command (block number x, option flag = 0)	→		
		←	Response(block x)[a]	
2	Read single block command (block number x, option flag = 1)	→		
		←	Response(block security status x, block x)[a]	

[a] Block x shall match the memory content of the requested blocks.

Data shall match the memory content of the requested block. This memory content and the block security status shall be specified by the manufacturer.

G.2.2.2.3 Scenario G.2: Write single block command

Table G.4 shows the test scenario for the Write single block command.

Precondition: Write access to unprotected memory blocks. The block is not locked.

Table G.4 — Scenario G.2: Write single block command

Step	VCD		VICC	Comment
1	Write single block command (block number x, data, option flag = 0)	→		
		←	Response	
2	Read single block command (block number x)	→		
		←	Response(block x)[a]	
3	Write single block command (block number, data, option flag = 1)	→		
	Isolated EOF	→		
		←	Response	
4	Read single block command (block number x, option flag = 0)	→		
		←	Response(block x)[a]	

[a] Block x shall match the memory content of the requested blocks.

G.2.2.2.4 Scenario G.3: Lock block command with option flag=0

Table G.5 shows the test scenario for the Lock block command with option flag=0.

Precondition: Write and Lock access to specified memory blocks.

Table G.5 — Scenario G.3: Lock block command with option flag=0

Step	VCD		VICC	Comment
1	Write single block command (block number x, data, option flag = 0)	→		
		←	Response	
2	Lock block command (block number x, option flag = 0)	→		
		←	Response	
3	Write single block command (block number x, data' , option flag = 0)	→		Data' is different than data in step 1
		←	Error Response	
4	Read single block command (block number x, option flag = 1)	→		
		←	Response(block security status x, block x)[a]	

[a] Block x shall match the memory content of [data].

NOTE This is an irreversible test case.

G.2.2.2.5 Scenario G.4: Lock block command with option flag=1

Table G.6 shows the test scenario for the Lock block command with option flag=1.

Precondition: Write and Lock access to specified memory blocks.

Table G.6 — Scenario G.4: Lock block command with option flag=1

Step	VCD		VICC	Comment
1	Write single block command (block number x, data, option flag = 0)	→		
		←	Response	
2	Lock block command (block number x, option flag = 1)	→		
	EOF	→		
		←	Response	

[a] Block x shall match the memory content of [data].

NOTE This is an irreversible test case.

Table G.6 *(continued)*

Step	VCD		VICC	Comment
3	Write single block command (block number x, data' , option flag = 0)	→		Data' is different than data in step 1
		←	Error Response	
4	Read single block command (block number x, option flag = 1)	→		
		←	Response(block security status x, block x)[a]	

[a] Block x shall match the memory content of [data].

NOTE This is an irreversible test case.

G.2.2.2.6 Scenario G.5: Read multiple blocks command

Table G.7 shows the test scenario for the Read multiple blocks command.

Precondition: Read access to unprotected memory blocks.

Table G.7 — Scenario G.5: Read multiple blocks command

Step	VCD		VICC	Comment
1	Read multiple blocks command (block number x, number of blocks n, option flag = 0)	→		
		←	Response(block x to block x+n-1)[a]	
2	Read multiple blocks command (block number x, number of blocks n, option flag = 1)	→		
		←	Response([block security status x, block x] to [block security status x+n-1, block x+n-1)[a]	

[a] Block x shall match the memory content of the requested blocks.

Data and block security status shall match the memory content of the requested blocks. The contents shall be specified by the manufacturer.

G.2.2.2.7 Scenario G.6: Write multiple blocks command

Table G.8 shows the test scenario for the Write multiple blocks command

Precondition: Write access to unprotected memory blocks. The blocks are not locked.

Table G.8 — Scenario G.6: Write multiple blocks command

Step	VCD		VICC	Comment
1	Write multiple blocks command (block number x, number of blocks n, blocks x to x+n-1, option flag = 0)	→		
		←	Response	
2	Read multiple blocks command (block number x, number of blocks n)	→		
		←	Response(block x to block x+n-1)[a]	
3	Write multiple blocks command (block number x, number of blocks n, blocks x to x+n-1, option flag = 1)	→		
	Isolated EOF	→		
		←	Response	
4	Read multiple blocks command (block number x, option flag = 0)	→		
		←	Response(block x to block x+n-1)[a]	

[a] Block x shall match the memory content of the requested blocks.

G.2.2.2.8 Scenario G.7: Select command with matched UID

Table G.9 shows the test scenario for the Select command with matched UID.

Precondition: The VICC is in the Ready State.

Table G.9 — Scenario G.7: Select Command with matched UID

Step	VCD		VICC	Comment
1	Select command (addressed mode[matching UID])	→		
		←	Response	

G.2.2.2.9 Scenario G.8: Select command without matched UID

Table G.10 shows the test scenario for the Select command without matched UID.

Precondition: The VICC is in the Ready State.

Table G.10 — Scenario G.8: Select command without matched UID

Step	VCD		VICC	Comment
1	Select command (addressed mode[non-matching UID])	→		
			Mute	
		←		

G.2.2.2.10 Scenario G.9: Reset to Ready command

Tested in G.3.2.

G.2.2.2.11 Scenario G.10: Write AFI command

Table G.11 shows the test scenario for the Write AFI command.

Precondition: The VICC is in the Ready State. AFI is not locked.

Table G.11 — Scenario G.10: Write AFI command

Step	VCD		VICC	Comment
1	Write AFI command (AFI, option flag = 0)	→		
			Response	
		←		

G.2.2.2.12 Scenario G.11: Lock AFI command

Table G.12 shows the test scenario for the Lock AFI command.

Precondition: The VICC is in the Ready State. AFI is not locked.

Table G.12 — Scenario G.11: Lock AFI command

Step	VCD		VICC	Comment
1	Lock AFI command (option flag = 0)	→		
			Response	
		←		
2	Write AFI command (AFI, option flag = 0)	→		
			Error Response	
		←		

G.2.2.2.13 Scenario G.12: Write DSFID command

Table G.13 shows the test scenario for the Write DSFID command.

Precondition: The VICC is in the Ready State. DSFID is not locked.

Table G.13 — Scenario G.12: Write DSFID command

Step	VCD		VICC	Comment
1	Write DSFID command (DSFID, option flag = 0)	→		
		←	Response	
2	Write DSFID command (DSFID, option flag = 1)	→		
	Isolated EOF	→		
		←	Response	

G.2.2.2.14 Scenario G.13: Lock DSFID command

Table G.14 shows the test scenario for the Lock DSFID command.

Precondition: The VICC is in the Ready State. DSFID is not locked.

Table G.14 — Scenario G.13: Lock DSFID command

Step	VCD		VICC	Comment
1	Lock DSFID command (DSFID, option flag = 0)	→		
		←	Response	
2	Write DSFID command (DSFID, option flag = 0)	→		
		←	Error Response	

G.2.2.2.15 Scenario G.14: Get system information command

Table G.15 shows the test scenario for the Get system information command.

Precondition: VICC is in the Ready State.

Table G.15 — Scenario G.14: Get system information command

Step	VCD		VICC	Comment
1	Get System Information command ()	→		
		←	Response[a]	

[a] The response shall match the declaration received from the manufacturer.

G.2.2.2.16 Scenario G.15: Get multiple block security status command

Table G.16 shows the test scenario for the Get multiple security status command.

Precondition: VICC is in the Ready State.

Table G.16 — Scenario G.15: Get multiple block security status command

Step	VCD		VICC	Comment
1	Get multiple block security Status command (block number x, number of blocks n)	→		
		←	Response(block security status * n)	

G.2.2.2.17 Scenario G.16: Extended read single block command

Table G.17 shows the test scenario for the Extended read single block command.

Precondition: Read access to unprotected memory blocks.

Table G.17 — Scenario G.16: Extended read single block command

Step	VCD		VICC	Comment
1	Extended read single block command (extended block number x, option flag = 0)	→		
		←	Response(extended block x)[a]	
2	Extended read single block command (extended block number x, option flag = 1)	→		
		←	Response(block security status, extended block x)[a]	

[a] Block x shall match the memory content of the requested blocks.

Block x shall match the memory content of the requested block. The contents shall be specified by the manufacturer.

G.2.2.2.18 Scenario G.17: Extended write single block command

Table G.18 shows the test scenario for the Extended write single block command.

Precondition: Write access to unprotected memory blocks. The block is not locked.

Table G.18 — Scenario G.17: Extended write single block command

Step	VCD		VICC	Comment
1	Extended write single block command (extended block number x, data, option flag = 0)	→		
		←	Response	
2	Extended read single block command (extended block number x)	→		
		←	Response(extended block x)[a]	

[a] Block x shall match the memory content of the requested blocks.