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Edition 1.0 2012-09

TECHNICAL SPECIFICATION

Process management for avionics – Electronic components for aerospace, defence and high performance (ADHP) applications – Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

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PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS FOR AEROSPACE, DEFENCE AND HIGH PERFORMANCE (ADHP) APPLICATIONS –

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FOREWORD

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- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC/TS 62686-1 which is a Technical Specification, has been prepared by IEC technical committee 107: Process management for avionics.

This Technical Specification cancels and replaces IEC/PAS 62686-1. It includes the following significant technical changes with respect to IEC/PAS 62686-1:

a) adoption and modification of STACK Specification S/0001 revision 14, *General requirements for integrated circuits and discrete semiconductors*;
b) addition of alternative IEC semiconductor test methods;
c) update of JEDEC semiconductor test methods;
d) update of Annex A additional JEDEC and IEC test information;
e) certification of the OCM according to ISO 9001;
f) addition of lead-free termination finish requirements;
g) addition of request for OCMs to make the data for device lifetime calculations available;
h) update of the IEC and JEDEC test methods for the following semiconductor wear-out mechanisms: TDDB, electro-migration, HCL and NBTI;
i) addition of request for OCMs to provide single event effects (SEE) data;
j) update of moisture sensitivity level (MSL) marking requirements.

The text of this Technical Specification is based on the following documents:

Enquiry draft	Report on voting
107/167/DTS	107/184/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62686 series, published under the general title *Process management for avionics – Electronic components for aerospace, defence and high performance (ADHP) applications*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

This part of IEC 62686 includes all the requirements of STACK Specification S/0001 revision 14 and contains revisions for alternative IEC qualification test methods and additional test information.

This Technical Specification complements IEC/TS 62564-1 which is used for ADHP applications when additional manufacturer's data is required beyond the publicly available manufacturer published datasheets (e.g. when additional thermal performance data is required for thermally challenging applications or when additional verification data are needed for example to comply with the requirements of RTCA DO-254/EUROCAE ED-80 for complex components for flight critical applications, etc.).

This Technical Specification can also be used to comply with the typical qualification requirements of IEC/TS 62564-1. Further guidance is given in IEC/TS 62239-1.

NOTE With the adoption of the STACK Specification S/0001 revision 14 it will be possible for all existing STACK certified manufacturers to be audited by IECQ under the new STACK-IECQ joint venture.

PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS FOR AEROSPACE, DEFENCE AND HIGH PERFORMANCE (ADHP) APPLICATIONS –

Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

1 Scope

This part of IEC 62686 defines the minimum requirements for general purpose "off the shelf" COTS (commercial off-the-shelf) integrated circuits and discrete semiconductors for ADHP (Aerospace, Defence and High Performance) applications.

This Technical Specification applies to all components that can be operated in ADHP applications within the manufacturers' publicly available datasheet limits in conjunction with IEC/TS 62239-1. It may be used by other high performance and high reliability industries, at their discretion.

ADHP application requirements may not necessarily be fulfilled by this specification alone. ADHP OEMs (original equipment manufacturers) may need to consider redesigning their products or conducting further testing to verify suitability in ADHP applications using their IEC/TS 62239-1 ECMP procedures. Alternatively a component in accordance with IEC/TS 62564-1 may be more suitable.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-3, *Semiconductor devices – Mechanical and climatic test methods – Part 3: External visual inspection*

IEC 60749-4, *Semiconductor devices – Mechanical and climatic test methods – Part 4: Damp heat, steady state, highly accelerated stress test (HAST)*

IEC 60749-5, *Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test*

IEC 60749-6, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-7, *Semiconductor devices – Mechanical and climatic test methods – Part 7: Internal moisture content measurement and the analysis of other residual gases*

IEC 60749-8, *Semiconductor devices – Mechanical and climatic test methods – Part 8: Sealing*

IEC 60749-9, *Semiconductor devices – Mechanical and climatic test methods – Part 9: Permanence of marking*

IEC 60749-14, *Semiconductor devices – Mechanical and climatic test methods – Part 14: Robustness of terminations (lead integrity)*

IEC 60749-15, *Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through hole mounted devices*

IEC 60749-17, *Semiconductors devices – Mechanical and climatic tests – Part 17: Neutron irradiation*

IEC 60749-19, *Semiconductor devices – Mechanical and climatic test methods – Part 19: Die shear strength*

IEC 60749-20, *Semiconductor devices – Mechanical and climatic test methods – Part 20: Resistance of plastic encapsulated SMDs to the combined effects of moisture and soldering heat*

IEC 60749-20-1, *Semiconductor devices – Mechanical and climatic test methods – Part 20-1: Handling, packing, labelling and shipping of surface-mount devices sensitive to the combined effect of moisture and soldering heat*

IEC 60749-21, *Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability*

IEC 60749-22, *Semiconductor devices – Mechanical and climatic test methods – Part 22: Bond strength*

IEC 60749-23, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-25, *Semiconductor devices – Mechanical and climatic test methods – Part 25: Temperature cycling*

IEC 60749-26, *Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)*

IEC 60749-29, *Semiconductor devices – Mechanical and climatic test methods – Part 29: Latch-up test*

IEC 60749-32, *Semiconductor devices – Mechanical and climatic test methods – Part 32: Flammability of plastic-encapsulated devices (externally induced)*

IEC 60749-33, *Semiconductor devices – Mechanical and climatic test methods – Part 33: Accelerated moisture resistance – Unbiased autoclave*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*

IEC 60749-38, *Semiconductor devices – Mechanical and climatic test methods – Part 38: Soft error test method for semiconductor devices with memory*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC/TS 62239-1, *Process management for avionics – Management plan – Part 1: Preparation and maintenance of an electronic components management plan*

IEC 62374, *Semiconductor devices – Time dependent dielectric breakdown (TDDB) test for gate dielectric films*

IEC 62374-1, *Semiconductor devices – Part 1: Time dependent dielectric breakdown (TDDB) test for inter-metal layers*

IEC 62415, *Semiconductor devices – Constant current electromigration test*

IEC 62416, *Semiconductor devices – Hot carrier test on MOS transistors*

IEC 62417, *Semiconductor devices – Mobile ion tests for metal-oxide semiconductor field effect transistors (MOSFETs)*

IEC/PAS 62483, *Test method for measuring whisker growth on tin and tin alloy finishes*

ISO 9001, *Quality management systems – Requirements*

ISO 14001, *Environmental management systems – Requirements with guidance for use*

ISO/TS 16949, *Quality management systems – Particular requirements for the application of ISO 9001:2008 for automotive production and relevant service part organizations*

AS/EN/JISQ 9100, *Aerospace series – Quality management systems – Requirements for aviation, space and defense organisations*

TL 9000, *Quality management system*[1]

STACK S/0001 revision 14, *General requirements for integrated circuits and discrete semiconductors*

EIA-471, *Symbol and label for electrostatic sensitive devices*

EIA-541, *Packaging material standards for ESD sensitive items*

ANSI/EIA-556, *Outer shipping container label standard*

JP001.01, *Foundry process qualification guidelines (Wafer fabrication manufacturing sites)*

JEP130A, *Guidelines for packing and labeling of integrated circuits in unit container packing*

JEP119, *A procedure for executing SWEAT*

JEP154, *Guideline for characterizing solder bump electromigration under constant current and temperature stress*

JESD6, *Measurement of small values of transistor capacitance*

JESD201, *Environmental acceptance requirements for tin whisker susceptibility of tin and tin alloy surface finishes*

[1] For the telecommunications industry.

JESD202, *Method for characterising the electromigration failure time distribution of interconnects under constant-current and temperature stress*

JESD22-A101, *Steady state temperature humidity bias life test*

JESD22-A102, *Accelerated moisture resistance – Unbiased autoclave*

JESD22-A103, *High temperature storage life*

JESD22-A104, *Temperature cycling*

JESD22-A108, *Temperature bias and operating life*

JESD22-A109, *Hermeticity*

JESD22-A110, *Highly accelerated temperature and humidity stress test (HAST)*

JESD22-A117, *Electrically erasable programmable ROM (EEPROM) program/erase endurance and data retention test*

JESD22-B100, *Physical dimension*

JESD22-B101, *External visual*

JESD22-B102, *Solderability*

JESD22-B105, *Lead integrity*

JESD22-B106, *Resistance to solder shock for through-hole mounted devices*

JESD22-B107, *Marking permanency*

JESD22-B116, *Wire bond shear test*

JESD46, *Customer notification of product/process changes by solid state suppliers.*

JESD47, *Stress test driven qualification of integrated circuits*

JESD48, *Product discontinuance*

JESD78, *IC Latchup test*

JESD85, *Methods for calculating failure rates in units of FITS*

JESD86, *Electrical parameters assessment*

JESD89, *Measurement and reporting of alpha particle and terrestrial cosmic ray-induced soft errors in semiconductor devices*

JESD94, *Application specific qualification using knowledge based test methodology*

JESD213, *Standard test method utilizing X-RAY-Fluorescence (XRF) for analyzing component finishes and solder alloys to determine Tin (Sn)-Lead (Pb) content*

JESD625, *Requirements for handling electrostatic discharge sensitive (ESDS) devices*

J-STD-020, *Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices*

J-STD-033, *Handling, packing, shipping and use of moisture/reflow sensitive surface mount-devices*

J-STD-609A.01, *Marking and labeling of components, PCBs and PCBAs to identify lead (Pb), lead-free (Pb-Free) and other attributes*

ANSI/ESDA/JEDEC JS-001, *Electrostatic discharge sensitivity testing – Human body model (HBM) – Component level*

MIL-STD-1580, *Destructive physical analysis (DPA) for electronic, electromagnetic and electromechanical parts*

UL94, *Tests for flammability of plastic materials for parts in devices and appliances*

AEC-Q100, *Stress test qualification for integrated circuits*

AEC-Q101, *Stress test qualification for automotive grade discrete semiconductors*

RTCA DO-254/EUROCAE ED-80, *Design assurance guidance for airborne electronic hardware*

3 Terms, definitions and abbreviations

For the purposes of this document, the following terms, definitions and abbreviations apply.

3.1 Terms and definitions

3.1.1
calendar days
continuous days, including weekends and holidays

3.1.2
container
outer shipping container consisting of one or more inner containers

3.1.3
customer
user
original equipment manufacturer (OEM) who procures integrated circuits and/or semiconductor devices compliant to this technical specification and uses them to design, produce, and maintain systems

3.1.4
data sheet
document prepared by the manufacturer that describes the electrical, mechanical, and environmental characteristics of the component

3.1.5
deviation
user agreement to allow the delivery of a shipping lot which does not fully meet the requirements of this specification

Note 1 to entry: Considered equivalent to concession for the purposes of this document.

3.1.6
device specification
document written by a user and agreed by the supplier or OCM

3.1.7
form
shape, arrangement of parts, visible aspect, mode in which a part exists or manifests itself, the material an item is constructed from

3.1.8
fit
qualified and competent, correct size and scale

3.1.9
function
work that an item is designed to do without degrading reliability

3.1.10
incoming lot
one or more shipments of a device, grouped together for the purpose of incoming inspection

3.1.11
inner container
box or bag containing devices, either in magazines or bulk packaged

3.1.12
magazine
shipping container that feeds into automatic placement machines

EXAMPLE Sticks, tubes, matrix trays, tape/reel, etc.

3.1.13
microcircuit
component
device
electrical or electronic device that is not subject to disassembly without destruction or impairment of design use and is a small circuit having a high equivalent circuit element density

Note 1 to entry: It is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function.

Note 2 to entry: This excludes printed wiring boards/printed circuit boards, circuit card assemblies and modules composed exclusively of discrete electronic components.

3.1.14
moisture sensitivity level
MSL
rating indicating a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering

3.1.15
original component manufacturer
OCM
company specifying and manufacturing the electronic component

3.1.16
room temperature
temperature identified at 25 °C ± 5 °C in a room

3.1.17
semiconductor device
electronic devices in which the characteristic distinguishing electronic conduction takes place with a semiconductor

EXAMPLE 1 Semiconductor diodes which are semiconductor devices having two terminals and exhibiting a nonlinear voltage-current characteristic.

EXAMPLE 2 Transistors which are active semiconductor devices capable of providing power amplification and having three or more terminals.

3.1.18
shipping lot
single lot of one or more containers received by a user

3.1.19
supplier
company identified by the logo or name marked on the device typically referred to as the original component manufacturer (OCM)

3.1.20
termination
element of a component that connects it electrically and mechanically to the next level of assembly

3.1.21
triboelectric charge
electrical charge generated by frictional movement or separation of two surfaces

3.2 Abbreviations

AC	alternating current
ADHP	aerospace, defense and high performance
AOQ	average out-going quality
AQEC	aerospace qualified electronic component
AQL	acceptable quality level
ASIC	application specific integrated circuit
BGA	ball grid array
BPSG	borophosphosilicate glass
CB	certifying body
CFC	chlorofluorocarbon
COTS	commercial off–the-shelf
CMOS	complementary metal oxide semiconductor
D	semiconductor device
DC	direct current
DRAM	dynamic random access memory
DLA	Defense Logistics Agency (see http://www.dscc.dla.mil/)
DPM	defects per million
ECMP	electronic component management plan
EHS	Environmental Health and Safety

EMAS	Eco-Management and Audit Scheme (established by the European Union)
ESD	electrostatic sensitive damage
FFF	form, fit and function
FIT	failures in time
h	hour
HAST	highly accelerated stress test
HCI	hot carrier injection
HTOL	high temperature operating life
IECQ	International Electrotechnical Commission Quality Assessment System for Electronic Components
IC	integrated circuit
I/O	input and output
IR	infra-red
LTB	last time buy
LTPD	lot tolerance percent defective
min	minute
MSL	moisture sensitivity level
NBTI	negative bias temperature instability
NVL	non-volatile memory operating life
OCM	original component manufacturer
OEM	original equipment manufacturer
PC	preconditioning
PCB	printed circuit board
PCN	product or process change notification
Pkg	package
QA	quality assurance
SDRAM	synchronous dynamic random access memory
SEE	single event effect
SEFI	single event functional interrupt
SEL	single event latchup
SEU	single event upset
SER	soft error rate
SMD	surface mount device
SRAM	static random access memory
Tamb	ambient temperature
TC	test code
THB	temperature humidity bias
Topmin	minimum operating temperature
Topmax	maximum operating temperature
UCL	upper control limit
VPR	vapour

4 Technical requirements

4.1 General

The supplier or original component manufacturer (OCM), as defined in 3.15 and 3.19, shall be Third Party ISO 9001 certified and shall provide the following minimum technical requirements. The OCM may use the test methods and methodologies specified herein which are based on IEC semiconductor test methods or any other equivalent test method for example JEDEC test methods (see 4.10.2.3 and Annex A). Proposed equivalent test methods, rationale and supporting data shall be reviewed and shall achieve the same end objectives as specified herein. Use of such equivalent tests shall not be considered to be deviations or waivers to the requirements of this specification.

Informative annexes are provided at the end of this specification and their content is subject to change. Users of this specification are encouraged to review the latest data available whenever referencing the content of these annexes:

- Annex A: test code information summarises all semiconductor test methods discussed herein;
- Annex B: cross-reference to STACK specification S/0001 revision 14;
- Annex C: Bibliography.

4.2 Procedures

4.2.1 General

The OCM shall have the following procedures:

- product discontinuance (4.2.2);
- ESD protection during manufacture (4.2.3);
- specification control (4.2.4);
- traceability (4.2.5).

4.2.2 Product discontinuance

Notification shall be in accordance with JESD48 or equivalent with the exception of timing as described in a) and b) below:

a) the OCM shall provide to the user a minimum of 12 months' notice of last order dates for single-source devices and 6 months for multi-sourced devices;

b) the OCM may give less than the specified notice period provided a mutually acceptable extension (up to the specification limit) is negotiated with any user needing a different period;

c) for custom ASIC devices, the normal procedure is to include discontinuation notice in the purchase contract.

4.2.3 ESD protection during manufacture

All integrated circuits and discrete semiconductors are considered to be static sensitive and shall be protected through the OCM's manufacturing operation. OCMs shall ensure that devices are not exposed to static damage and are not degraded or damaged due to static discharge. IEC 61340-5-1 and JESD625 are examples of suitable standards for ESD precautions in wafer fabrication and probe. OCMs holding current IECQ Certification for compliance with IEC 61340-5-1 shall be deemed to have satisfied this requirement.

4.2.4 Specification control

The OCM shall:

a) when applicable, have central or local record of the user's part number and specification, against the product to be delivered;

NOTE 1 This applies to direct sales and not to parts sold through distribution.

b) ensure the specifications on the purchase documents have been reviewed and accepted by personnel authorized to do so.

NOTE 2 This applies to custom and special orders only.

4.2.5 Traceability

Traceability shall be managed as follows:

a) the OCM shall have traceability for any device in a shipping lot through a route code, lot code or other marking on the device or magazine or inner container to identify the manufacturing route, e.g. groups of wafer lots, wafer fabrication location, assembly location, test location, date code and/or lot code;

b) the information needed to interpret the code shall be available;

c) the procedure shall be available for inspection during audit.

4.3 Product or process change notification (PCN)

4.3.1 General

The OCM shall provide the following:

- notification (4.3.2);
- notification details (4.3.3); and
- notifiable changes (4.3.4).

4.3.2 Notification

In the event of the OCM proposing or making a change to a device, then:

a) the OCM shall give at least 90 calendar day's written notice prior to shipping the changed product. The user will respond to confirm the date on which changed product shipments can begin (could be less than 90 calendar days), advise that changed product is not acceptable, or request further information;

b) for custom ASIC devices, change notification periods are normally specified in the purchase contract;

c) in an event beyond the control of the OCM where 90 calendar days' notice cannot be given, the OCM shall reach a mutually agreed lesser notice period with any user affected by the change or the IECQ CB that issued IECQ Certification.

4.3.3 Notification details

The PCN shall include the following items:

a) title of change;

b) OCM type number(s) affected;

c) OCM notification identification number;

d) estimated last order and shipment dates for unchanged devices to be supplied on request;

e) estimated earliest shipment date of changed devices;

f) manufacturing location and product line affected;

g) a thorough description of the proposed change;

h) means of distinguishing changed devices from unchanged devices. this may be a date code, lot code, date code range or distinguishing marking or feature that is visible to the user at point of receipt of shipment;

i) sufficient engineering and/or qualification test data, including details of any qualification test vehicle used and its applicability to the product change, shall be available on request to demonstrate that the change will not adversely affect device form, fit, function, quality or reliability, and that the changed product will continue to meet the specified requirements;

j) user part number of the affected device (preferred item but not mandatory).

4.3.4 Notifiable changes

JESD46 shall be used as a guide to changes requiring notification.

4.4 Shipment controls

4.4.1 General

The OCM shall have the following shipment controls:

- shipping container and date code marking (4.4.2);
- date code remarking (4.4.3);
- inner container formation (4.4.4);
- date code age on delivery (4.4.5);
- ESD marking (4.4.6);
- MSL (4.4.7);
- lead-free marking (4.4.8); and
- labels (4.4.9).

4.4.2 Shipping container and date code marking

The shipping container and date code marking shall be in accordance with JEP130A or an equivalent standard. The manufacturer's name, logo and/or trademark shall be marked on the shipping container where it is practical to do so.

4.4.3 Date code remarking

If the date of assembly and test are both marked, the test date can be remarked if the device is re-tested at a later date. If only one date is marked to represent the manufacturing date and initial electrical test it shall not be changed unless it is necessary to correct poor quality marking or incorrect information and provided that the time delta between the original mark and the remark is less than 6 weeks.

4.4.4 Inner container formation

It is preferred that the inner container contains only devices of the same die revision/stepping level.

It is preferred that devices shall also be from the same:

– wafer fabrication location;

– assembly site;

– outgoing QA electrical inspection site.

4.4.5 Date code age on delivery

Date code age on delivery shall be as follows:

a) the date codes of devices shall not be older than 24 months upon users' receipt date;

b) for custom ASIC devices, the date code age limits will normally be defined in the purchase contract;

c) if the OCM wishes to ship devices outside the specified limit, the deviation procedure should be used.

4.4.6 ESD marking

The symbols used and labelling shall be in accordance with EIA-471 or equivalent standard.

4.4.7 MSL

The labelling and shipping container shall be in accordance with J-STD-033 or equivalent standard.

4.4.8 Lead-free marking

The shipping container and date code marking shall be in accordance with J-STD-609A.01 or equivalent.

4.4.9 Labels

In general, labels shall include the requirements mentioned in Table 1 and exhibit:

a) human readable content: the content shown for each label in this section shall be available in human readable form on the outside of the relevant package;

b) machine readable content: bar codes for those items specified shall be included in 3 of 9 codes (bar code 39) as per ANSI/EIA-556 or equivalent compatible standard;

c) warning notice: any necessary warning notices or symbols to ensure the safety of the contents shall be included as appropriate.

Table 1 – Label requirements

Dry pack label:	**Bar code**
• Date of sealing and sealed life or expiration date.	
• Time and storage condition limits after opening.	
• Bake conditions if usage conditions after opening are violated.	
• Moisture sensitivity classification per J-STD-020 or per OCMs own classification provided a cross reference is provided at registration.	
Container label: this label is typically implemented as a shipping note or packing list attached to the outer container.	
• Delivery address.	
• Purchase order number.	*
• User part number.	*
• OCM device type number [a].	*
• The OCM's name [a].	
• Quantities enclosed of each device type [a].	*
Inner container label:	
• OCM device type number.	*
• User part number [b].	*
• Purchase order number [b].	*
• Quantity of devices.	*
• Date code.	*
• Lot number.	*
• Assembly location [b].	
• Test location [b].	
[a] For security reasons can be omitted with the agreement of the user.	
[b] Preferred but not mandatory.	

4.5 Electrical

4.5.1 General

Operating conditions shall be as defined in the device specification or data sheet, as explained in 4.5.2 to 4.5.7.

4.5.2 Electrical test

All shipped packaged devices shall have passed a production electrical test program, or in the case of user-specific devices, a test program approved by the user. Tested wafer or die products shall have an effective equivalent wafer probe test. Untested wafer and die products shall have met the OCMs minimum process control monitor (PCM) requirements. JEDEC test methods shall be used wherever possible.

4.5.3 Electrical parameter assessment

Test methods for assessing electrical parameter distributions (AC, DC, functional and timing) of devices should be in accordance with JESD86.

4.5.4 SDRAM memories

SDRAM memories should be designed and tested in accordance with JESD79.

4.5.5 Logic families

Logic families should be designed and tested in accordance with JESD36, JESD52, JESD76 or JESD80.

4.5.6 Power MOSFETs

Power metal-oxide-semiconductor field-effect transistors (MOSFETs) should be tested in accordance with JESD24.

4.5.7 Silicon rectifier diodes

Silicon rectified diodes should be tested in accordance with JESD282B.01, MIL-PRF-19500 or an equivalent standard.

4.6 Mechanical

4.6.1 General

Integrated circuits or discrete semiconductor package dimensions specified in industry standard outlines (e.g. JEDEC outlines), will be met as specified, if the package is stated as compliant with that outline.

4.6.2 Device or shipping container marking

4.6.2.1 General

All the specified markings on the device or shipping container shall be clearly legible.

4.6.2.2 Top surface

All of the following required markings shall be marked on the top side, except where otherwise indicated below:

a) pin 1 identifiable either by a mark or by reference to a physical feature of the device;

b) the OCM's name or logo;

c) the OCM part number or individual user part number as required;

d) date code of assembly or test. Formats YYWW, or YWW or YM are acceptable (Y=year numeral, W=week numeral, M=month character). If both assembly and test date codes are marked, the assembly code may be bottom marked;

e) a manufacturing route trace code. Top surface is preferred, but the device bottom surface may be used;

f) if both assembly and manufacturing route trace code are marked on the bottom surface, the manufacturing route trace code shall be marked below the assembly code.

4.6.3 Small packages

If the marking area available on the device is too small to do so, then the unit container is to include all the required marking.

4.6.4 Moisture sensitivity

The moisture sensitivity of all non-hermetic surface mount components shall be tested and classified according to J-STD-020. The MSL classification shall be available.

4.6.5 Robustness of hermetic seals

Seal shall not be compromised by any normal handling, testing or manufacturing processes.

4.6.6 Termination finishes

OCMs should make available on their web pages or datasheets (or otherwise), information pertaining to the leaded (Pb) and lead-free termination finish qualification testing, termination material, finish alloy composition, and (if used) heat treatment process of parts used relative to the RoHS directive. In addition, the following requirements shall be met:

a) thickness limits shall be met over 95 % of the termination surface. The OCM shall select appropriate measurement locations;

b) plating composition and thickness limits shall be available;

c) it is not necessary for solder dipping to cover the entire termination. The area covered should be appropriate to the type of package: e.g. J-bend packages (area below base plane); gull wing packages (center of bottom radius to trimmed edge of termination);

d) tin electroplate finishes shall be matt, dense, homogenous, free of co-deposited organic material and suitably treated to inhibit whisker growth. When applicable an appropriate tin whisker plan or process should be in place (for example accelerated tin whisker testing to JESD201 Class 2 limits or JESD22 A121 or IEC/PAS 62483) and be demonstrable. Documented results should be made available to the user upon request;

e) provide notification of changes, via the PCN process, to termination finish materials, thickness, or to plating process chemistry.

4.7 Audit capability

4.7.1 General

The OCM shall be able to carry out the following:

- internal quality audits (4.7.2); and
- sub-contract manufacturing (4.7.3)

4.7.2 Internal quality audits

The OCM shall periodically audit each internal location, to assess compliance with internal standards for the following areas listed below. Minimum Third Party certification shall be to ISO 9001. Avionics certification AS/EN/JISQ 9100 is preferred to the automotive ISO/TS 16949 certification. The following areas defined in Table 2 shall be addressed:

Table 2 – Internal quality audit requirements

Quality system	Calibration	Failure analysis
Shipment and container	Stores and dispatch	ESD control
Contract review	Customer service	Production test
Design management	Process control	Subcontract controls
Purchasing	Incoming materials	Wafer fabrication and probe
OCM audits	Documentation control	Assembly
Training	Product qualification	Reliability monitor

The results of these audits and the audit acceptance criteria shall be available for onsite inspection during an audit. The internal quality audit documentation shall be available upon request.

4.7.3 Subcontract manufacturing

The OCM shall qualify and periodically audit all subcontracted operations to a standard equivalent to the OCMs internal operations.

4.8 Quality assurance

4.8.1 General

The OCM shall have the following quality assurance system:

- quality system (4.8.2);
- sampling plans (4.8.3);
- failure analysis support (4.8.4); and
- outgoing quality (4.8.5).

4.8.2 Quality system

The OCM quality system shall meet the following requirements:

a) the OCM shall have an appropriate quality registration, i.e. one (or more) of ISO 9001, TL 9000, AS/EN/JISQ 9100, ISO/TS 16949, etc.;

b) the system shall ensure that the requirements of this specification are met;

c) the system shall provide for the prevention and ready detection of discrepancies and for timely and positive corrective action.

4.8.3 Sampling plans

Appropriate and statistically valid sampling plans shall be used and documented. The target for reliability qualification of microelectronics by accelerated ageing is an LTPD better than 3 %. This may be achieved by overstress testing of sample sizes exceeding 76 devices from the specific device population, with no failures permitted, or by invoking structural similarity and accumulating samples from other device types at the level of build being tested. For example, thermal cycling is intended to evaluate die and wire bonding and back-end assembly, and the desired LTPD may be achieved from structurally similar builds of similar metallization, die size and attachment, wirebond material diameter, process, and loops.

4.8.4 Failure analysis support

OCM failure analysis support shall meet the following requirements:

a) the OCM shall maintain an adequate failure analysis capability and provide a timely response to failures returned for failure verification or failure analysis;

b) representative samples of devices returned as failures, shall be analyzed and a failure analysis report issued to the originating user, typically within 30 calendar days of the receipt by the analytical facility of such returns;

c) for failure returns relating to a critical problem at a user, the failure analysis report shall typically be issued within 7 calendar days of receipt by the analytical facility.

4.8.5 Outgoing quality

4.8.5.1 General

Outgoing quality shall be measured as per 4.8.5.2 to 4.8.5.5.

4.8.5.2 DPM levels

The OCM shall measure average outgoing quality (AOQ) in defects per million from uniform manufacturing processes and the results shall be in accordance with Table 3. The measurement of outgoing quality via in process measurements is acceptable in principle. The number of defects will include all devices non-conforming to any functional, electrical, visual or mechanical specification requirement of a device.

4.8.5.3 DPM calculation

Measurement may be by any appropriate classification and method, e.g. individual devices or device families, package type and/or technology family, in process measurements.

4.8.5.4 Corrective action

If the outgoing quality levels given in Table 3 are not met, the OCM shall take root cause corrective action and issue a closure date for achieving the required DPM.

Table 3 – Outgoing quality

Device family		Maximum DPM
Electrical	Transistor count	
Discretes and integrated circuits	≤ 100 000	50
	< 1 000 000	100
	≥ 1 000 000	150
Programmable logic when supplied programmed and tested		100
Visual/mechanical		200
NOTE This information can be considered proprietary and confidential.		

4.8.5.5 Data reporting

AOQ data shall be compiled periodically and be available upon request.

4.9 Supplier performance monitoring by the user

4.9.1 General

The user reserves the right to decide upon the following:

- lot acceptance (4.9.2);
- suspension of deliveries (4.9.3);
- loss of approval (4.9.4);
- AQL figures (4.9.5);
- 100 % screening (4.9.6); and
- termination determination (4.9.7).

4.9.2 Lot acceptance

Users reserve the right to perform incoming lot acceptance on every lot received, using any incoming test as shown in Table 4 or the qualification test in Table 5.

Table 4 – Incoming test

Package type	Test per Table 5	Inspection level [a]	AQL %
All	Electrical test	II	0,065
All	External visual inspection	II	0,20

Package type	Test per Table 5	Inspection level [a]	AQL %
Hermetic only	Hermeticity fine	II	0,40
Hermetic only	Hermeticity gross	II	0,25
All	Dimensions	II	0,10
[a] See ANSI/ASQ Z1.4.			

4.9.3 Suspension of deliveries

The user may bring to the attention of the OCM any failure to meet a qualification or incoming test and to require the OCM to withhold further deliveries to that user until the cause of the failure has been identified and corrected.

4.9.4 Loss of approval

A failure of one or more shipping lots of a specific device to meet the requirements of this specification or the device specification may constitute grounds for loss of approval. The action taken will depend on the nature of the problem found.

4.9.5 AQL figures

The AQL/LTPD figures quoted are for the purpose of individual incoming lot rejection; they do not imply an overall acceptance quality level.

4.9.6 100 % screening

Users reserve the right to perform 100 % screening on individual shipping lots received and to reject any devices from the OCM which do not meet the special requirements specified in the contract.

4.9.7 Termination determination

The following procedures: X-ray fluorescence (XRF) spectroscopy per JESD213 or energy dispersive (X-ray) spectroscopy (EDS) per MIL-STD-1580 may be used for termination verification.

4.10 Qualification

4.10.1 General

The OCM shall manage the following:

- methodology (4.10.2); and
- test samples (4.10.3);
- qualification categories (4.10.4);
- maintenance of qualification standards (4.10.5);
- in-process test results (4.10.6);
- product monitor results (4.10.7);
- references (4.10.8);
- qualification report (4.10.9);
- archiving (4.10.10);
- qualification by similarity (4.10.11);
- similarity assessment (4.10.12).

4.10.2 Methodology

4.10.2.1 General

The OCM shall use appropriate methodologies to qualify new technology, new devices and device changes, to demonstrate that the device under qualification is capable of meeting the specified electrical, quality and reliability requirements, using qualification families as defined in JESD47.

4.10.2.2 Procedures and methods

Procedures and methods are per Table 5.

4.10.2.3 Alternate procedures

Alternate procedures and methods are acceptable as per 4.1 and are as follows:

a) qualification in conformity with JESD47, for integrated circuits and their generic families, providing the following, additional, items are addressed by the OCM:
   - ball shear testing on BGA packages,
   - electrical population drift calculations,
   - x-ray,
   - long term FIT-rate calculations,
   - electomigration; hot carrier injection; time dependent dielectric breakdown; and negative bias temperature instability,
   - MSL rating assessment,
   - marking permanency,
   - die shear strength,
   - thermal resistance,
   - flammability,
   - internal visual inspection;
b) qualification in conformity with AEC-Q100 for integrated circuits and their generic families providing the OCM address the following additional items:
   - the high temperature operating life (HTOL) test shall be 1 000 h minimum at temperature cycling equal to 125 °C,
   - soft error rate testing,
   - marking permanency,
   - x-ray,
   - electromigration; hot carrier injection; time dependent dielectric breakdown; and negative bias temperature instability,
   - non-volatile memory operating life,
   - thermal resistance,
   - flammability,
   - internal visual inspection;
c) qualification to AEC-Q101 for discrete semiconductors and their generic families providing the OCM address the following additional items:
   - latch-up,
   - steady state operating life,
   - high temperature blocking bias,

- high temperature bake,
- electromigration; hot carrier injection; time dependent dielectric breakdown; and negative bias temperature instability,
- temperature humidity bias,
- HAST,
- internal water vapour,
- flammability,
- internal visual inspection,
- x-ray,
- lid torque;

d) qualification to an application specific scheme should be created as per the methodology and guidance provided in JESD94. An application specific plan should address the subjects of concern contained in the preceding qualification schemes.

4.10.2.4 Risk analysis

A risk analysis shall be accomplished to determine the impact on reliability and quality.

4.10.2.5 Stress test driven qualification

The stress test driven qualification shall be performed and documented in stress test driven qualification plans.

4.10.2.6 Use of product similarity data

Perform testing and document the re-using of existing data based on product similarity arguments.

4.10.2.7 Use of reliability models

Perform and document the verified reliability models.

4.10.3 Test samples

4.10.3.1 General

The OCM shall use the test samples described below.

4.10.3.2 Test failures

The general acceptance level for all stress test qualification is zero rejects in the tested sample size.

Test failures attributed to extraneous factors not related to the qualification stress applied shall not be counted against acceptance criteria. If excessive failures from non-qualification test related mechanisms are generated, the test shall be repeated.

If a larger sample size than specified in Table 5 is used and failures allowed, then the result shall meet an LTPD = 3 % for specified sample size of 76. The target LTPD requirement is stated in 4.8.3. In Table 5, lower sample quantities are allowed where the particular stress tests are not intended for statistical extrapolation, but for characterisation or package evaluation.

4.10.3.3 Additional samples

Users reserve the right to take additional samples for a qualification test result confirmation.

4.10.3.4 Consolidation of lots

Where production volumes of a device are low and the sample sizes specified are not economically feasible from one manufacturing lot, consolidation of lots is permissible. If consolidation of lots is performed, the combining of parts shall follow the similarity rules as per 4.10.12 (similarity assessment).

4.10.3.5 Reduced sample sizes

The OCM's qualification procedures may allow devices to be released to the market after testing them to a qualification schedule which does not fully meet the requirements herein, in terms of reduced sample size, reduced test time etc. This is only acceptable providing test data continues to be accumulated as per 4.12 and corrective actions and or repeat testing is performed as necessary until the qualification level is reached or exceeded in a target of 90 calendar days. Where IECQ Certification has been issued for compliance with this specification, the IECQ CB shall decide on the acceptance of any reduced sample size.

4.10.4 Qualification categories

The qualification may be conducted on a specific device type. Alternatively qualification may be accomplished by using generic family qualification data providing similarity rules are followed (see 4.10.11).

4.10.5 Maintenance of qualification standard

Regular quality and reliability test results, that are obtained from a monitor program, but which are not related to any particular customer shipment, are an acceptable method of maintaining the qualification standard of this specification. It is desirable that the manufacturer maintains a regime of "maintenance of qualification" in order to ensure that reliability sensitive processes are routinely tracked and sample tested.

4.10.6 In-process test results

In-process test results shall be managed as follows:

a) if any of the inspection or package qualification tests are performed on a regular basis in the manufacturing line, these tests need not be repeated in new device qualification testing;

b) if qualification tests are not performed, manufacturing inspection results showing the current quality level shall be included in the qualification report. Manufacturing package test results shall be available.

Table 5 – Technology/family qualification and device qualification

Test code (TC) information see Annex A		Product family	Title	Test reference See 4.10.2 for more details	Number of lots for family qualification	Sample size per lot	Number of lots for device qualification
			ELECTRICAL				
TC6	(ET)	IC, D	Electrical test	JESD86/MIL883-M3012 or JESD6	3	50	1
TC7	(ED)	IC, D	Electrical distributions	JESD86/MIL883-M3012 or JESD6	3	30	1
TC16	(LU)	IC, D	Latch-Up	JESD78 or IEC 60749-29	1	6	1
TC5	(ESD)	IC, D	ESD – human body model	ANSI/ESDA/JEDEC JS-001 or IEC 60749-26	1	3	1
TC28	(SER)	IC	Soft error	JESD89 or IEC 60749-38 or IEC 60749-17	-	-	-
			PROCESS				
TC22	(OI)	IC, D	Time dependent dielectic breakdown (oxide integrity)	JP001.01 or IEC 62417	-	-	-
TC4	(EM)	IC, D	Electromigration	JP001.01, JEP119, JESD202, JEP154 or IEC 62415	-	-	-
TC9	(HCI)	IC, D	Hot carrier injection	JP001.01 or IEC 62416	-	-	-
TC40	(NBTI)	IC, D	Negative bias temperature instability	JP001.01 or IEC 62374 or IEC 62374-1	-	-	-
			ENDURANCE				
TC24	(PTC)	D	Power cycling	MIL883-M1037 or IEC 60749-34	3	76	1
TC29	(SSOL)	D	Steady state operating life	JESD22-A108 or IEC 60749-23	3	76	1
TC13	(HTGB)	D	High temperature gate bias	JESD22-A108	3	76	1
TC12	(HTBB)	D	High temperature blocking bias	MIL750-1048	3	76	1
TC14	(HTRB)	D	High temperature reverse bias	JESD22-A108	1	76	1
TC15	(HTOL)	IC	High temperature operating life	JESD 22-A108 or IEC 60749-23	3	76	1
TC21	(NVL)	IC	Non-volatile memory operating life	JESD22-A117	1	22	1
TC11	(HTB)	IC, D	High temperature bake	JESD22-A103 or IEC 60749-6	3	76	1

Test code (TC) information see Annex A		Product family	Title	Test reference See 4.10.2 for more details	Number of lots for family qualification	Sample size per lot	Number of lots for device qualification
			TEMPERATURE/HUMIDITY				
TC25	(RSH)	D	Resistance to solder heat	JESD22-B106 or IEC 60749-15 or IEC 60749-20	1	30	1
TC31	(THRB)	D	Temperature humidity reverse bias	JESD22-A101	1	76	1
TC30	(TC)	IC, D	PC + Temperature cycling	JESD22-A104 or IEC 60749-25	1	32	1
TC32	(THB)	IC, D	PC + THB: 85 °C / 85 % RH (or HAST) (plastic only)	JESD22-A101 or IEC 60749-4 or IEC 60749-5	1	76	1
TC32	(HAST)	IC, D	PC + HAST plastic only	JESD22-A110 or IEC 60749-4	1	76	1
TC1	(AC)	IC, D	PC + Autoclave (plastic only)	JESD22-A102 or IEC 60749-33	1	32	1
			MECHANICAL				
TC23	(PD)	IC, D	Package dimensions	JESD22-B100	1	5	1
TC27	(SD)	IC, D	Solderability (76 leads / 5 devices minimum)	JESD22-B102 or IEC 60749-21	1	76	1
TC36	(WV)	IC, D	Internal water vapour (hermetic only)	MIL883-M1018or IEC 60749-7	1	3	1
TC20	(MP)	IC, D	Marking permanency	JESD22-B107 or IEC 60749-9	1	3	1
TC2	(BS)	IC, D	Bond strength (76 wires / 5 devices minimum)	JESD22-B116 or IEC 60749-22	1	76	1
TC3	(DS)	IC, D	Die shear strength	MIL883-2019 or IEC 60749-19	1	5	1
TC34	(TR)	IC, D	Thermal resistance	Not specified	1	3	1
TC8	(FL)	IC, D	Flammability (plastic only)	UL94 or IEC 60749-32	-	-	-
TC8	(FL)	IC, D	Alternative flammability (plastic only)	IEC 60695-2-2	1	3	1
TC17	(LI)	IC	Lead integrity (applicable devices)	JESD22-B105 or IEC 60749-14	1	3	1
TC33	(TS)	D	Terminal strength	MIL750-M2036	1	3	1
TC18	(LT)	IC, D	Lid torque (hermetic only)	MIL883-M2024	1	5	1
TC19	(MS)	IC	Mechanical sequence (hermetic only)	See test in A.19	1	5	1
TC10	(HE)	IC, D	Hermeticity (hermetic packaging end point test only)	JESD22-A109 or IEC 60749-8	-	-	-
TC38	(MSL)	IC, D	Moisture sensitivity Level	J-STD020 or IEC 60749-20-1	-	-	-
TC39	(BST)	IC, D	Ball shear	JESD22-B117A or AEC-Q100-010	-	-	-
TC41	(TW)	IC,D	Tin whisker	JESD201	-	-	-

Test code (TC) information see Annex A	Product family	Title	Test reference See 4.10.2 for more details	Number of lots for family qualification	Sample size per lot	Number of lots for device qualification
		INSPECTION				
TC35a (VI)	IC, D	External visual inspection	JESD22-B101 or IEC 60749-3	1	25	1
TC35b (VI)	IC, D	Internal visual inspection	MIL883-M2010	1	5	1
TC37 (XR)	IC, D	X-Ray inspection (plastic only)	MIL883-M2012	1	5	1

4.10.7 Product monitor results

If any inspection or package qualification tests are performed on a regular basis in product monitor testing, these tests need not be repeated in new device qualification testing.

4.10.8 References

References are given for guidance only. Reference shall always be made to the appropriate test code information for full test details.

4.10.9 Qualification report

The qualification report shall be available upon request.

4.10.10 Archiving

The qualification report and the test specification (not test program), used in the qualification shall be archived for a minimum of 3 years.

4.10.11 Qualification by similarity

Qualification by similarity can be used as follows:

a) a change shall be qualified if there is a potential effect on performance, quality or reliability, or if there is any degree of uncertainty about the effect of the change;

b) guidance on the qualification tests, which the QCM should consider applying, for the various combinations of die, package and process changes, is shown in JESD47. The QCM shall perform tests defined in the qualification table that are appropriate, or relevant to the change;

c) upon request, the QCM shall provide data for any device transferred to a new process to prove that no design deficiencies (e.g. mechanical, electrical performance, reliability, single event effects etc.) were introduced by the process transfer.

4.10.12 Similarity assessment

4.10.12.1 General

The principle of similarity may be applied in qualification, qualification of changes and product monitor testing as follows:

- die changes (4.10.12.2);
- process/wafer fabrication changes (4.10.12.3);
- package/assembly changes (4.10.12.4).

4.10.12.2 Die changes

The QCM shall document and operate an appropriate set of die similarity rules or guidelines applied by appropriate engineering review.

4.10.12.3 Process/wafer fabrication changes

Devices to be assigned to a qualification family shall share the same critical processes and material elements.

4.10.12.4 Package/assembly changes

Package/assembly changes shall be managed as follows:

a) package families shall be grouped by configuration and materials of construction. In general, all members of the group that are equal to or smaller in dimensions and lead count can be considered as similar to a qualified package, provided the assembly process technology is identical;

b) packages should be qualified with the worst case configuration (e.g. the largest die) they are designed to carry that is currently in production. For custom ASIC's use of a "qualification die" is acceptable, such that die larger than the qualification die by +10 % by linear dimension are qualified, provided the package design maximum die size is not exceeded.

4.11 Reliability

4.11.1 General

The OCM shall ensure the following:

- operating reliability (4.11.2);
- failure criteria (4.11.3);
- corrective action (4.11.4);
- warranty (4.11.5);
- suspension of certification (4.11.6); and
- single event effects (SEE) (4.11.7).

4.11.2 Operating reliability

The OCM shall manage operating reliability as follows:

a) unless otherwise specified in the device specification, the failure rate of devices operating in systems at an ambient temperature of +55 °C shall not exceed the figures in Table 6. The OCM shall, upon request from the user make available FIT rate data to confirm application specific life expectancy. See 4.12.6 for production maturity factors;

b) results observed at a temperature other than +55 °C will be projected to this temperature, with 60 % confidence using an activation energy, appropriate to the failure mechanism observed. Refer to TC15 HTOL for calculation of acceleration factors and projected results shall show the 60 % confidence range. Alternatively results can be analyzed using JESD85 at higher confidence levels;

c) for custom devices the OCM shall on request provide a FIT rate including the confidence range and operating life prediction to the user (based on a demonstrable methodology) for the application and environmental conditions intended;

d) the OCM should provide upon request their device feature sizes under 100 nm and any mitigation strategies, tools or data for device lifetime calculations.

4.11.3 Failure criteria

Failure criteria shall consist of any of the following modes:

a) functional failure;

b) parameter limit failure;

c) intermittent faults due to the package pins, or the interconnect system, from the pins to the die surface, shall be regarded as failures;

d) transitory faults attributable to the device shall be regarded as failures.

4.11.4 Corrective action

If failures are detected in the reliability processes, the OCM shall investigate, determine root cause and take appropriate actions to achieve conformity to this specification or the OCM's internal requirements whichever is the most stringent.

4.11.5 Warranty

The reliability requirements in this specification apply to the general population of devices supplied. The warranty period and terms and conditions of sale for failure of individual devices within any warranty are not covered by this specification.

4.11.6 Suspension of certification

The user reserves the right to apply accelerated life test and to accumulate life test data on any device, starting with the life test performed for qualification. The reliability data accumulated shall show a device meets the specified requirements in Table 6.

Table 6 – Operating life failure rates

Operating life failure rates at T_{amb} 55 °C and 60 % UCL	Device complexity	FIT
This information may be considered proprietary.	Discrete transistors	5
	< 500 transistors	8
	< 5 000	25
	< 50 000	30
	< 1 000 000	100
	< 10 000 000	200
	< 100 000 000	200

4.11.7 Single event effects (SEE)

Single bit error rate for DRAM and SRAM are shown in A.28 for Test TC28 (SER). SEE data shall be made available upon request if available.

4.12 Product monitor

4.12.1 General

The OCM shall ensure the following:

- monitor programme (4.12.2);
- problem notifications (4.12.3);
- data reporting (4.12.4);
- samples (4.12.5);
- production maturity factors (4.12.6);
- device dissipation (4.12.7);
- corrective action (4.12.8);
- product monitor results (4.12.9); and
- accumulated test data (4.12.10).

4.12.2 Monitor programme

The monitor programme shall be as follows:

a) the OCM shall have a continuous monitor programme to demonstrate, that the requirements of this part of IEC 62686 are met, on an ongoing basis, for each manufacturing operation or product process;

b) statistical process control: the OCM shall control wafer production, assembly process and final test using statistical analysis. When anomalies are observed, parametric and yield data from probe and final tests shall be analyzed against in-line or electrical process control data. The root cause of the deviation shall be determined and the consequent corrective actions implemented;

c) Table 5 shows the minimum test requirements for a conventional stress driven monitor. The use of a failure mechanism driven approach to optimise reliability monitoring is encouraged. On-going qualification test data and accumulated reliability monitor test data may be assessed in a structured way to reduce reliability monitor testing when failure mechanisms are shown to be eliminated by process controls and to increase testing or introduce new tests when failures are detected.

4.12.3 Problem notification

The OCM shall have a process to notify the users and distributors in cases where failures were detected and where the possibility of failed parts may have been shipped or may be in the process of being shipped to the user.

NOTE This is usually part of the PCN system as described in JESD46 as a guide.

4.12.4 Data reporting

Reliability monitor data accumulated over the preceding two full quarters shall be available, at one month's notice.

4.12.5 Samples

Samples shall be selected as follows:

a) appropriate sample sizes shall be selected;

b) samples shall be randomly selected from representative package and process family devices;

c) all package types and all process families, but not necessarily all package/process combinations, shall be monitored;

d) package tests shall use the largest die size the package is designed to carry that is currently in production. Custom ASIC qualification die may be used, see similarity assessment (4.10.11);

e) sample lots will be added to the monitor at intervals appropriate for each test.

4.12.6 Production maturity factors

The FIT rates in Table 6 represent devices in mature production. The following maturity factors (MF) in Table 7 may be used to multiply the values in Table 6.

Table 7 – Production maturity factors

Production time (months)	0 to 12	12 to 24	24 and higher
Maturity factor (MF)	4	2	1

4.12.7 Device dissipation

Where the device dissipation in the oven is significantly less than in normal operation this shall be taken into account in FIT rate calculations.

4.12.8 Corrective action

Failure to meet the limits in Table 8 or the OCM's internal limits, whichever is the most stringent, shall trigger appropriate corrective action by the OCM

4.12.9 Product monitor results

Product monitor results shall meet the requirements of Table 8.

4.12.10 Accumulated test data

Accumulated test data can be analysed as follows:

a) failure rates and levels may be a rolling average with data accumulation period appropriate to the production quantity level;

b) for HTOL test, the minimum total sample size (SS) required over the data accumulation period, may be calculated using:

$$SS = \frac{Chi^2\ (B,c) \times 10^9}{2 \times FITS \times A \times t}$$

where

Chi^2 (60 %,0) = 1,83

Chi^2 (60 %,1) = 4,04

Chi^2 (60 %,2) = 6,21

FITS see Table 6

c is the number of failures;

B is the upper confidence limit;

A $A_T \times A_V$ (see A.15 for TC15);

t is the time under bias in oven.

Table 8 – Product monitor tests

Test codes	Title	Maximum failure
HTOL	Early life	a, b, d
HTOL	Long term life	b, e, f
NVL	Non-volatile memory operating life	0,5 %[c]
TC	Temperature cycling	0,5 %[c]
PC + THB or HAST	Preconditioned 85/85 or HAST (plastic package only)	0,5 %[c]

[a] Duration up to 168 h.

[b] Failure rate calculated as shown in Test HTOL.

[c] Failure levels are actual number of failures divided by the quantity tested.

[d] Early life FIT rate = 2 × (Table 6 value) × (production maturity factor in 4.12.6).

[e] Long term life FIT rate = 1 × (Table 6 value) × (production maturity factor).

[f] HTOL on devices may be substituted by appropriate wafer level reliability i.e. testing at the wafer level.

4.13 Environmental, health and safety (EHS)

4.13.1 General

The OCM shall ensure the following health and safety precautions are in place:

- EHS compliance (4.13.2);

- device handling (4.13.3); and
- device materials (4.13.4).

4.13.2 EHS compliance

The OCM shall be expected to comply with all applicable national, regional, state and local laws and regulations governing environment, health and safety. OCM registration to industry recognized EHS standards, such as ISO 14001, or EMAS, is encouraged, but not mandatory.

4.13.3 Device handling

Devices should not produce any toxic effects to personnel as a result of handling, storage or disposal, or when operated according to the OCM's data sheet.

4.13.4 Device materials

Materials used in the manufacture of devices should be non-flammable, and shall not emit harmful levels of toxic materials as a result due to electrical overload or fault within the device.

4.14 Shipping container

4.14.1 General

Shipping containers shall protect devices and address the following considerations.

4.14.2 ESD requirements

4.14.2.1 General

The OCM shall ensure that all shipping containers should be static safe (non-generating as a minimum) to safe guard sensitive products occupying the same manufacturing areas. The OCM shall also ensure the following:

- electrostatic properties (4.14.1.2);
- ESD protection (4.14.1.3);
- specification compliance after shipment (4.14.1.4);
- device orientation (4.14.1.5);
- user instructions (4.14.1.6);
- electrostatic shield (4.14.1.7);
- magazine surface resistivity (4.14.1.8);
- inner container surface characteristics (4.14.1.9).

4.14.2.2 Electrostatic properties

The electrostatic properties of the shipping container material shall be as specified after conditioning of 48 h at 23 °C ± 3 °C and 12 % RH ± 3 %. Any appropriate test method may be used; examples are contained in standard EIA-541. This test requirement may be met by a certificate of conformance from the shipping container material supplier.

4.14.2.3 ESD protection

All devices shall be supplied in suitable electrostatic protective shipping containers with electrostatic properties meeting the requirements of standard EIA-541 unless otherwise specified in this section.

4.14.2.4 Specification compliance after shipment

The method of packing for land, sea or air transportation shall adequately protect the device from being electrically or mechanically degraded or damaged in any way during transit.

4.14.2.5 Device orientation

Devices shall all have the same orientation within a magazine.

4.14.2.6 User instructions

Any special handling requirements or precautions (e.g. placing of desiccants; resealing of containers; maximum number of 24 h 125 °C bake cycles allowable) which shall be observed for storage or reshipment shall be stated on the packing and, where necessary, supporting documentation shall be supplied with each inner container.

4.14.2.7 Electrostatic shield

The inner container or magazine shall contain an electrostatic shield of surface resistivity less than 10^6 Ω/square.

4.14.2.8 Magazine surface resistivity

Packing material in direct contact with the device pins shall have a surface resistivity less than 10^{12} Ω/square.

4.14.2.9 Inner container surface characteristics

All surfaces of the inner container other than an electrostatic shield shall meet the following:

- Surface resistivity: 10^5 to 10^{12} Ω/square;
- Charge decay in 2 s: 5 kV to less than 100 V;
- Triboelectric charge: Not to exceed 100 V.

4.14.3 Magazine reuse

Tubes, trays or other magazines, which depend for their electrostatic properties on surface coatings, shall be limited to a defined number of load/unload cycles. The specified surface resistivity shall be met after the defined number of cycles and data shall be available to justify the limit chosen. Coated magazines may be “reset” to zero load cycles by a suitable recycling process, which includes recoating.

Magazines that utilize bulk material properties may be reused.

4.14.4 Tubes

4.14.4.1 General

The OCM shall ensure the following:

- cushioning material (4.14.3.2);
- partial tubes (4.14.3.3);
- marking access (4.14.3.4); and
- opening (4.14.3.5).

4.14.4.2 Cushioning material

Ceramic devices packaged in tubes shall have an adequate amount of cushioning material to ensure that the devices are not damaged as a result of movement within the tubes.

4.14.4.3 Partial tubes

Full tubes shall be shipped with a maximum of one partly-filled tube per inner container.

4.14.4.4 Marking access

The material of the tube shall be transparent or contain a slot to allow inspection of top markings.

4.14.4.5 Opening

Tubes shall be openable at either end unless otherwise specified to meet unique customer applications.

4.14.5 Trays

4.14.5.1 General

The OCM shall ensure the following:

- devices with MSL = 4 or higher (4.14.4.2);
- marking of bake temperature limit (4.14.4.3); and
- stacking of trays (4.14.4.4).

4.14.5.2 Devices with MSL of 4 or higher

For devices with a moisture sensitivity classification according to J-STD020 of 4 or higher, the tray shall have a bake capability of at least 125 °C.

4.14.5.3 Marking of bake temperature limit

Bake temperature limit shall be marked on the tray or the tray marked heatproof.

4.14.5.4 Stacking of trays

There shall be no more than 10 full trays to be stacked in height, plus one partial tray with one further tray as a cover.

4.15 Compliance with internal standards

This document does not exempt the OCM of their responsibility to meet their own internal company requirements.

Annex A
(informative)

Test code (TC) information

A.1 TC1 – Autoclave (AC)

Test method: JESD22-A102 condition C, for plastic packages only or IEC 60749-33 for 96 h. Solder preconditioning for non-hermetic SMD per test TC26 (PC).

NOTE Autoclave, whether biased or unbiased is sometimes used for testing plastic packaged devices. The test is a valid quality test but is a non-valid reliability test because of no known reliability data. Instead use HAST, JEDEC JESD22-A118 condition A, which is non-saturating and non-condensing, is the proven and preferred method for valid and known acceleration of ageing of electronics in humid environments.

A.2 TC2 – Bond strength, internal (BS)

Test method: Minimum bond strength as specified in JESD22-B116 for ball shear testing or MIL-STD-883 method 2011, test condition D for wire bond pull testing or IEC 60749-22. Recording of failure categories is not required. Plastic packages for example can be tested before encapsulation.

NOTE IEC 60749-22 uses metric units and defines methods A to G which cover a wider variety of test conditions than JESD22-B116.

A.3 TC3 – Die shear strength (DS)

Test method: MIL-STD-883 method 2019. Plastic packages for example can be tested before encapsulation.

Alternative test methods are:

- MIL-STD-883 method 2027, stud pull test (for integrated circuits (IC's));
- MIL-STD-750 method 2017, die attach integrity test (for discrete components);
- IEC 60749-19.

A.4 TC4 – Electromigration (EM)

Test methods to characterize the metallization system include JP001.01 and/or JEP119, JESD202, JEP154 or IEC 62415 and/or IEC 62418.

Details of test methods, results and the capability life demonstrated, for $< 0{,}1$ % failures at worst case operating temperature are to be available on request. The requirement to perform electromigration testing is not limited to sub-micron technologies. Larger geometries are subject to electromigration wear out mechanisms. Characterization data could be for the metallization and contact process as a whole, using accelerated current and temperature testing of test structures on the wafer rather than individual device types. Acceleration factors shall be justified by experimental data.

A.5 TC5 – Electrostatic discharge (ESD)

Test method: Human body model.

a) ANSI/ESDA/JEDEC JS-001 or IEC 60749-26;

NOTE ANSI/ESDA/JEDEC JS-001 superseded JESD22-A114 in 2010.

b) ESD withstanding voltage to be determined and be available;

c) ESD classification to be recorded in the qualification report.

Similarity: Sample testing among groups of similar pins is acceptable and for example the similarity basis can be stated in the qualification report. Users reserve the right to test any pin-to-pin combination and to reject on failure.

OCMs holding current IECQ certification for compliance with IEC 61340-5-1 are deemed to have satisfied this requirement.

A.6 TC6 – Electrical test (ET)

Test method: JESD86.

Qualification electrical test: the electrical test is performed at the worst still air ambient temperature in the range of T_{opmin} to T_{opmax}. The device shall be stabilized at the test temperature. Where the test is carried out at a temperature which is not the worst case then full guard banding allowance can be made.

Testing is as follows:

a) DC test to datasheet;

b) AC test to datasheet or correlated DC testing to guarantee the AC parameters;

c) special functional tests where applicable, e.g. pattern sensitivity etc.;

d) functional verification;

e) fault coverage target requirements for stuck at "1" and "0" are typically in excess of 95 %.

Population parameter drift: Where parameter drift assessment is specified in HTOL and HCI tests, a sample of $\geq$ 10 devices are to pass electrical test both before and after endurance testing and results of main parameters are to be data-logged.

f) individual devices are not required to be serialized;

g) adequate parameter stability confirmation is required;

h) reporting of statistical measures of population drift is required. The drift of the population mean for any parameter is to be less than 10 % of the initial population mean;

i) functional failures are to be excluded from calculation of mean values.

A.7 TC7 – Electrical distributions (ED)

Purpose: OCMs to verify the data on specified electrical-variables parameters on devices to be qualified per data sheet limits, and assess the device's capability to function within the data sheet limits over time and application environment (e.g. operating temperature range, voltage, input/output levels, etc.) in accordance with JESD86.

Input/output capacitance is one of the parameters evaluated for new process/design qualifications using MIL-STD-883 method 3012 or JESD6. The device bias is at nominal operating voltage. Capacitance measurements are made at all logic levels for digital devices and normal biased condition for analogue devices.

A.8 TC8 – Flammability (FL)

Flammability is only applicable to plastic devices.

Test methods: UL94 or IEC 60749-32 applicable.

The bulk material test is mandatory but the OCM could meet this test requirement by using material manufacturers test data. If bulk material is not available IEC 60695-11-5 needle flame is a suitable method for tests on individual devices.

A.9 TC9 – Hot carrier injection (HCI)

This is applicable to sub-micron MOS technologies where appropriate testing to evaluate long term intrinsic failure mechanisms for device/design related charge injection is carried out.

Test methods: JP001.01 or IEC 62417.

Details of test methods, results and the capability life demonstrated, for < 0,1 % failures is to be made available. Examples of appropriate methods are found in Table A.1.

Table A.1 – Conditions of the DC over voltage stress method of JP001.01 or IEC 62416 test

Absolute maximum V_{cc} for DRAM.	Maximum V_{cc} for other devices.
Duration 1 000 h.	
Dynamic operation.	End point: electrical test (ET). Population parameter drift.

A.10 TC10 – Hermeticity (HE)

Not applicable to non-hermetic packages.

Test methods: JESD22-A109 or MIL-STD-883 method 1014 or MIL-STD-750 method 1071 or IEC 60749-8. Note that IEC 60749-8 uses metric units, has condition E for weight gain gross leak testing and die penetrant gross leak testing

A.11 TC11 – High temperature bake (HTB)

Test methods: JESD22-A103 or IEC 60749-6 condition B for 1 000 h or JESD22-A103 condition C for 500 h for plastic packages.

JESD22-A103 condition E for 10 h or condition D for 72 h for ceramic packaged devices. Note that IEC 60749-6 does not contain these test conditions

Examines device metal/contact inter diffusion robustness.

A.12 TC12 – High temperature blocking bias (HTBB)

Test method: MIL-STD-750 method 1048, T_{amb} 150 °C ± 5 °C / 500 h or at 125 °C / 1 000 h at $V_{bias\ max}$ at which DC and AC parameters are guaranteed unless otherwise specified. Critical device blocking junction is reverse biased. Thermal shutdown is not allowed.

A.13 TC13 – High temperature gate bias (HTGB)

Test method: JESD22-A108, examines MOS Gate oxide capabilities. T_{amb} 150 °C ± 5 °C for 1 008 h at V_{cc} (maximum) which DC and AC parameters are guaranteed unless otherwise specified.

A.14 TC14 – High temperature reverse bias (HTRB)

Test method: JESD22-A108, examines junction capabilities. T_{amb} 150 °C ± 5 °C for 1 008 h at max rated junction temperature specified in the user/OCM specification with device reverse biased to 80 % of maximum breakdown voltage specification or max junction temperature to avoid thermal runaway. If $T_{amb} < 145$ °C due to device stability, actual T_{amb}, T_j and bias conditions shall be documented. Test before, at 504 h and 1 008 h.

NOTE Tj is the device semiconductor junction temperature and bias refers to the reverse voltage bias.

A.15 TC15 – High temperature operating life (HTOL)

A.15.1 General

Test method: JESD22-A108 or MIL-STD-883 method 1005 or IEC 60749-23 where a static or dynamic life test which best relates to the device type is applied.

a) devices are cooled to 55 °C or lower prior to the removal of bias;

b) interruption of bias for up to one minute for the purpose of moving the devices to cool down positions is not considered removal of bias;

c) following bias removal the devices are maintained at less than 30 °C ambient until tested;

d) electrical endpoint testing is normally be completed within 48 h of removal of bias.

End point measurements: electrical test TC6 (ET) including population parameter drift.

A.15.2 Qualification conditions

The qualification conditions are as follows:

a) 1 000 h at $T_{amb} \geq 125$ °C. Higher test temperatures for shorter test times could be used provided the stress is equivalent and anomalous failures do not result from the higher test temperature;

b) Maximum operating voltage;

c) If internal power dissipation causes T_j to exceed T_{jmax} or activate a thermal shutdown circuit, the test temperature could be reduced and the test time extended;

d) Use the field life simulated by the qualification test derived from using the temperature and voltage acceleration factors defined herein in the qualification report.

A.15.3 Test results assessment

Product monitor results accumulated from periods of accelerated life test could be used to assess early life and long term failure rates, using JESD85 or the following:

$$\text{FIT} = \frac{\text{Chi}^2\,(B,c) \times 10^9}{2 \times N \times t \times A_T \times A_V}$$

where

Chi^2 (60 %,0) = 1,83

Chi^2 (60 %,1) = 4,04

Chi^2 (60 %,2) = 6,21

B is the upper confidence limit;

c is the number of observed defects;

N is the number of devices tested;

A_V is the voltage acceleration factor;

A_T is the temperature acceleration factor;

t is the test duration of up to 168 h for early life calculations or total test duration minus early life period for long term life calculations.

A.15.4 Temperature acceleration factor

Use the activation energy indicated from relevant failure analysis data. Where no relevant data is available, an activation energy of 0,7 eV is to be used, but it shall be recognized that this will not take account of oxide failure mechanisms.

See Table A.2 for examples of temperature acceleration factors which use activation energy of 0,7 eV.

Table A.2 – Examples of temperature acceleration factors

Examples of A_T for E_a = 0,7 eV	T_{oven} °C	t h	T_{ja} °C	A_T	Field life years
$A_T = e^{\left[\left[\frac{E_a}{K}\right]\left[\frac{1}{T_{j\,sys}} - \frac{1}{T_{j\,oven}}\right]\right]}$	125	1 000	0	78	8,9
			15	55	6,3
			30	41	4,7
			45	31	3,6
			60	25	2,8
where	125	2 000	0	78	17,8
E_a is the activation energy;			15	55	12,6
K = 8,617 × 10^{-5} eV/K;			30	41	9,3
$T_{j\ sys}$ K = 273 + T_{ja} + T_{sys},			45	31	7,1
$T_{j\ oven}$ K = 273 + T_{ja} + T_{oven},			60	25	5,6
T_{sys} = 55 °C system ambient;	150	1 000	0	260	29,7
T_{ja} is the junction temperature rise due to power dissipation.			15	170	19,4
			30	117	1ESD
			45	83	9,5
			60	61	7,0

A.15.5 Supply voltage acceleration factor

The supply voltage acceleration factor is selected as follows:

- if a supply voltage higher than the nominal operating voltage is used, a voltage acceleration factor is to be used in FIT rate calculations;
- relationships are typically of the form shown below but any formula and constant values C can be used for which the OCM has supporting evidence available:

$$A_V = e^{C\,(V1-V2)}$$

where

A_V is the voltage acceleration factor;

C is a constant determined by the dielectric integrity data;

$V1$ is the stress voltage;

$V2$ is the operating voltage.

- supply voltage acceleration shall be used with circumspection and justified on a case-by-case basis.

A.16 TC16 – Latch-up (LU)

Latch up is applicable to CMOS technologies.

Test methods: EIA/JEDEC Standard EIA/JESD78 or IEC 60749-29, power supply overvoltage and current injection into the input and output (I/O) pins.

Test conditions used from Table A.3 are to be recorded in the qualification report.

Table A.3 – Test conditions

Failure criteria	1,4 × I_{nom} or I_{nom} + 10 mA whichever is greater or device no longer meets functional or parametric requirements.
Power supply over voltage (PSOV) pulse	1,5 × $V_{supply\ max}$
Positive current pulse	+(I_{nom}+100 mA) or 1,5 × I_{nom} whichever is greater in magnitude
Negative current pulse	–100 mA or –(0,5 × I_{nom}) whichever is greater in magnitude
NOTE I_{nom} is the measured DC supply current for each supply voltage pin with the device under test biased at the test temperature as defined in Clause 4 and Table 2 of JESD78.	

A.17 TC17 – Lead integrity (LI)

This is applicable to through hole mount IC's. It is not applicable to SMD and PGA (pin grid array).

Test methods: JESD22-B105 or MIL-STD-883 method 2004 condition B2 lead fatigue or IEC 60749-14. Note that IEC 60646-14 uses metric units.

Sample 15 leads on minimum of 3 devices. If package corner pins have reduced width or thickness, then at least 1 corner pin is to be tested on each device such that all corner pins are included in the sample.

Carry out end point hermeticity test for hermetic packages.

A.18 TC18 – Lid torque (LT)

Test method: MIL-STD-883 method 2024.

A.19 TC19 – Mechanical sequence (MS)

A.19.1 General

The same samples are to receive all the tests in the sequence.

This is applicable only to cavity packages and devices with bonds and solder joints not moulded in.

End point tests: External Visual inspection TC35 (VI), Hermeticity fine and gross TC10 (HE), Electrical test TC6 (ET).

A.19.2 Constant acceleration

Test method: MIL-STD-883 method 2001. Apply Y1 axis only. IEC 60749-36

A test condition appropriate to the package mass, area and perimeter length is to be selected.

The test condition used is to be made available.

A.19.3 Vibration (variable frequency)

Test method:

- JESD22-B103; or
- MIL-STD-883 method 2007 condition A; or
- IEC 60749-12.

Peak acceleration: 20 g.

A.19.4 Mechanical shock

Test method:

- JESD22-B104 condition B; or
- MIL-STD-883 method 2002 condition B; or
- IEC 60749-10, 5 pulses 1500 g, each pulse 0,5 ms duration.

A.20 TC20 – Marking permanency (MP)

This is not applicable to laser marking. The use of CFC solvents is not a requirement.

The sample "groups" can each consist of one device. Each group is tested with a different solvent.

Test methods: JESD22-B107 or MIL-STD-883 method 2015 or IEC 60749-9.

A.21 TC21 – Non-volatile memory operating life (NVL)

Test method: JESD22-A117.

Applicable to floating gate technology electrically programmable/erasable non-volatile memory devices including embedded memory. The write/erase and subsequent data retention properties of the device using a combination of write/erase cycling and high temperature bake testing is to be determined. Appropriate interim bake and electrical test points are selected by the OCM.

The test extends to the maximum number of write/erase cycles specified. The subsequent data retention bake of 150 °C for 1 000 h minimum is carried on the same sample devices unless otherwise notified.

Bake time can be reduced by using a higher temperature, e.g. 175 °C for 500 h, 200 °C for 72 h or 250 °C for 10 h. Conversely, if the test at 150 °C causes anomalous failure mechanisms, the test temperature can be reduced and the test time extended to provide an equivalent condition.

For each applicable technology the relationship between the number of write/erase cycles and data retention period (hours) is to be made available, see Table A.4.

Table A.4 – Relationship between write/erase cycle and data retention

Procedure for one write/erase test cycle	Procedure for data retention bake
a) Write the device with a suitable pattern.	a) Electrical test.
b) Electrical test (first and last cycles only).	b) Write the device with a suitable pattern.
c) Erase the device.	c) Bake at 150 °C for 1 000 h minimum.
d) Write the inverse of the pattern in (a).	d) Read and confirm data pattern still valid.
e) Electrical test (first and last cycles only).	e) Electrical test.
f) Erase the device.	

A.22 TC22 – Time dependent dielectric breakdown (oxide integrity) (OI)

Test method: JP001.01 or IEC 62417.

Appropriate testing to evaluate long term intrinsic failure mechanisms in semiconductor gate oxide systems and dielectric isolation material systems is to be carried out.

Details of test methods, results and the capability life demonstrated, for $<$ 0,1 % failures are to be made available.

A.23 TC23 – Package dimensions (PD)

Test method: JESD22-B100 or MIL-STD-883 method 2016, IEC 60749-3.

A.24 TC24 – Power cycling (PTC)

Test methods:

MIL-STD-883 M1037 (Power cycling only), Test at T_{amb} = 25 °C. Test duration based upon package size/type. Devices powered to ensure T_j = 100 °C (not to exceed absolute maximum ratings).

JESD22-A122 or IEC 60749-34.

Electrical test before, at midpoint and endpoint.

Examples of conditions:

- Small package (e.g. SMD SOTS, D-pak) duration 15 000 cycles, 2 min on/off.
- Medium package. (e.g. TO-220, D2-pak) duration 8 572 cycles, 3,5 min on/off.
- Large package. (e.g. TO-3, TO-247) duration 5 000 cycles, 5 min on/off.

If a T_j of 100 °C cannot be achieved, consider JESD22-A105 (power and temperature cycling) as an alternative method. Test is performed only on devices with maximum rated power > 1 W and T_j 40 °C. Apply 1 000 cycles of –40 °C to 125 °C. Thermal shutdown is not allowed.

A.25 TC25 – Resistance to solder heat (RSH):

Test methods:

- JESD22-B106, Test before and after RSH. SMD devices are to be fully submerged during test;
- IEC 60749-15; or
- IEC 60749-20.

A.26 TC26 – Solder preconditioning (PC)

This is not applicable to hermetic packages.

Test method: JESD22-A113 or IEC 60749-30:

a) moisture conditioning appropriate to the device moisture sensitivity classification followed by three reflow soldering operations in accordance with J-STD-020;

b) moisture conditioning and soldering operation(s) applied are to be stated in the qualification report;

c) the moisture conditioning requirement is to be as specified or an equivalent moisture weight gain specified;

d) if wave soldering capability is required by a device specification agreed with the OCM, it will be demonstrated by immersing the device in flux followed by immersion in solder at 260 °C for 10 s. This operation could include soldering devices onto a PCB with a preheat ramp rate of up to 10 °C/s. To avoid solder bridging problems on some fine pitch packages oil can be used in place of solder for wave soldering simulation.

A.27 TC27 – Solderability (SD)

Requirement:

Devices stored in the as received condition and shipping container are to retain solderability after delivery for a minimum of 12 months in “standard atmospheric conditions” of ambient temperature and relative humidity in the range 5 °C to 30 °C, 20 % to 70 % RH.

Test method and aging: industry standard dip and look test conditions and steam aging are given below as test references. These methods will not be suitable for all packages, e.g. fine pitch and chip scale and dry heat aging can be more suitable for some lead finishes. Any differences in test method and aging used should be noted during registration.

Dip and look test references:

Test method:	JESD22-B102 or MIL-STD-883-M2003 or IEC 60749-21.
Flux:	Non-activated flux.
Aging:	8 h steam.
THM (Through Hole Mount):	245 °C for 5 s.
SMD:	215 °C ± 2 °C for 5 s ± 1 s.
Palladium plated SMD:	The OCM can perform the test at 215 °C ± 2 °C for 10 s ± 1 s, but the user reserves the right to perform the test as specified and to reject on failure.

NOTE IEC 60749-21 uses metric units and defines lead-free solder in more detail than JESD22-B102.

A.28 TC28 – Soft error rate (SER)

Test methods: JESD89 including JESD89-1, JESD89-2 and JESD89-3 or IEC 60749-38 or IEC 60749-17.

This test applies to DRAM and SRAM devices only (not embedded memory). For SRAM references to refresh can be ignored.

Reporting: the number of errors detected, including SEFI and SEL and the following test parameters are to be stated in the qualification report. Appropriate parameter values are to be chosen by the OCM:

Sample size.	Refresh type, burst, etc.
Test duration (h).	Test temperature.

Sample size/test duration: for qualification, the number of device-hours shall be adequate to demonstrate that the soft single bit error rate at T_{amb} 55 °C and 90 % UCL does not exceed 20 FIT/Mbit for both DRAM and SRAM.

Recommended test conditions:	Recommended data pattern:
V_{cc} minimum specified for data retention.	Write and verify checkerboard once, then read/refresh continuously.
Maximum specified refresh interval (period)	Repeat with complementary checkerboard.
Test temperature 55 °C. Cycle time 500 ns.	Test with checkerboard and complementary pattern for approximate equal durations.

Accelerated testing: Accelerated testing using the “hot source” irradiation method is not acceptable as a substitute for system level soft error test.

A.29 TC29 – Steady state operating life (SSOL)

Test method: JESD22-A108 or IEC 60749-23.

Examine device power handling capabilities. T_{amb} for 1008 h. Device is biased statically to full power at ambient temperatures. Thermal shutdown is not allowed.

A.30 TC30 – Temperature cycling (TC)

Test methods:

- Solder preconditioning for non-hermetic SMD per test TC26 (PC);
- JESD22-A104 condition C, 500 cycles, –65 °C to +150 °C; or
- JESD22-A104 condition B, 1 000 cycles, –55 °C to +125 °C; or
- MIL-STD-883 method 1010 condition B, 1 000 cycles, –55 °C to +125 °C; or
- IEC 60749-25, 1 000 cycles, –55 °C to +125 °C.

1 min maximum transfer time. 10 min minimum dwell time if using MIL-STD-883 method 1010 or 1 min minimum dwell time if using soak mode 1 of JESD22-A104 or select an appropriate

dwell time based upon featuring and mass. Solder preconditioning to be applied for non-hermetic SMD per test code TC26 (PC).

End points: Hermeticity (hermetic devices only) test TC10 (HE).

Qualification electrical test TC6 (ET).

The OCM will apply the specified number of cycles. Alternative number of cycles and temperature extremes with $T_{min} \leq -40$ °C are acceptable if the OCM can show the stress level is equivalent.

A.31 TC31 – Temperature humidity reverse bias (THRB)

Test method: JESD22-A101. 1 000 h 85 °C / 85 % RH with device reverse biased at 80 % of rated breakdown voltage up to a maximum of 100 V or limit of chamber. Electrical test before at 500 h and 1 000 h.

A.32 TC32 – Temperature humidity bias (THB or HAST)

Solder preconditioning for non-hermetic SMD per test TC26 (PC).

Consider intermittent bias for cases where $T_j \geq 5$ °C above ambient.

End point: Qualification electrical test TC6 (ET).

Test methods:

Temperature Humidity Bias Test THB	Highly Accelerated temperature and humidity Stress Test HAST is considered to be a destructive test.
JESD22-A101 or IEC 60749-5	JESD22-A110 or IEC 60749-4
	Relative humidity: 85 % ± 5 %
	Temperature: 130 °C ± 2 °C
	Duration : 96 h

HAST shall not exceed 130 °C as above this value non-valid results have been known to occur, other HAST conditions with lower temperatures per JESD22-A110 can be used as an alternative to 85/85 THB test when the OCM has adequate evidence of correlation using those conditions. The conditions used shall be stated in the qualification report.

A.33 TC33 – Terminal strength (TS)

Test method: MIL-STD-750 method 2036 for diodes and transistors.

A.34 TC34 – Thermal resistance (Thermal Impedance) (TR)

Use any appropriate test method. Examples of methods are included here but not limited to:

- JESD531 for signal and regulator diodes,
- JESD313-B for conduction cooled power transistors,
- JESD51-1 and JESD51-2 for integrated circuits (natural convection),