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2007-02

Logic digital integrated circuits – Specification for I/O interface model for integrated circuit (IMIC version 1.3)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62404, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/746/DTS	47A/751/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

With an increase in speed of electronic systems, it becomes necessary to accurately predict electrical performance including noise in electronic systems with integrated circuits.

Simulators have been used for this purpose. Simulators need accurate models for describing electrical properties of integrated circuits. Semiconductor manufacturers and/or suppliers are required by their users to prepare device models for various simulation tools, some of which are not compatible with SPICE. In addition, since SPICE models contain proprietary process parameters, a non-disclosure agreement is typically required to obtain these from the vendor.

IBIS (I/O Buffer Interface Specification) has been proposed as a model for integrated circuits, which, approved as IEC 62014-1, has the following features:

- since electrical properties of I/O buffers are described in table format, disclosure of proprietary information such as process parameters is drastically reduced;
- it is easy to get IBIS models that are supported by many simulation tools;
- a public domain tool can convert SPICE models into IBIS models.

However, IBIS models seem to have the following problems:

- the modeling of power and ground currents is insufficient for accurate power and ground bounce analysis;
- since an IBIS model has only the final stage at output and input, it is difficult to model the effect of loading on circuit boards on output and input waveforms. The fixed model taken by IBIS has little flexibility for describing other circuitry;
- in order to simulate EMI with accuracy, more information such as material constant and three-dimensional structures is needed.

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

1 Scope

The following items are considered to standardize the electrical modeling of input signals, output signals, power supply and ground terminals of integrated circuits, in order to provide for analysis of electrical characteristics of equipment.

1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities.
2) To define more flexible description rules for electric circuits in order to provide more accurate analysis of printed circuit board.
3) To introduce the concept of modeling levels to exchange relevant data for each application.
4) To enhance electrical modeling for packages and modules.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62014-1:2001, *Electronic design automation libraries – Part 1: Input/output buffer information specifications (IBIS version 3.2)*

3 Terms and definitions

Under consideration

4 Outline

4.1 General

The outline of this model is shown in Figure 1.

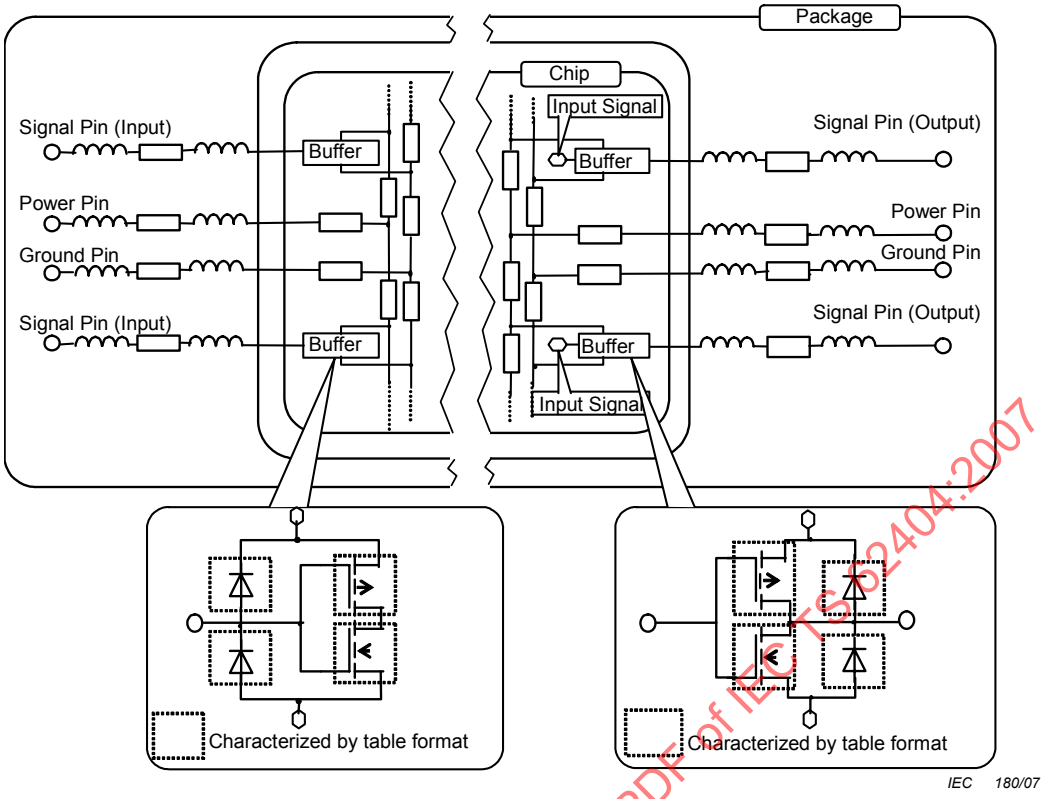


Figure 1 – Outline of the model

4.2 Covered range of model

The model is described as circuits covering the whole or a part of the I/0 buffers and the package.

4.3 Language for circuits

The circuits shall be described in extended SPICE format. The structure allows describing simple buffers, complex buffers, power and ground lines, packages and complex memory module boards in a unified format.

4.4 Device model

The characteristics of non-linear devices redescribed in one-dimensional, two-dimensional or three-dimensional table format.

4.5 Structure of model

The data of the model consists of integrated circuit, package and module portions. Therefore each portion can be generated independently.

4.6 Simulation

The netlist of printed circuit board and the I/O buffer model defined by this specification provides accurate circuit simulation results.

4.7 Relation to IBIS

Tools that can extract IBIS data from this model are possible to develop.

5 Model structure

The model shall describe the inside of ICs, packages and module boards as shown in Figure 2.

The models of IC, package and module board consist of the elements given in Table 1.

The data structures of IC, package and module board models are shown in Figure 3, Figure 4, and Figure 5, respectively.

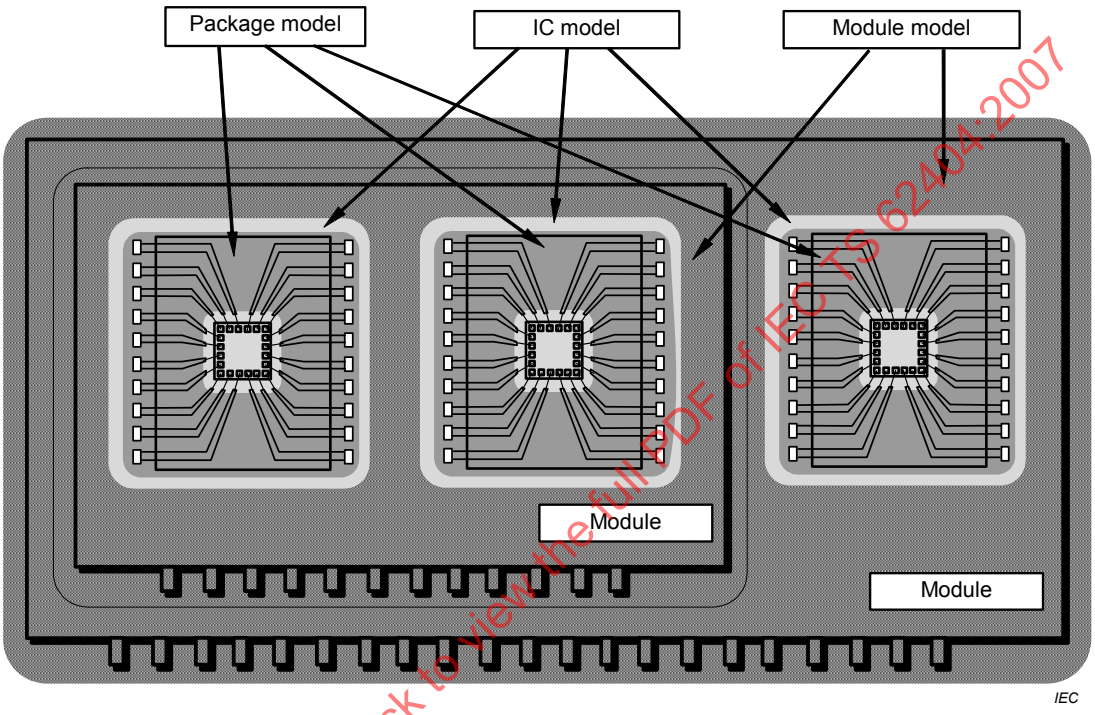


Figure 2 – Hierarchy of three models

Table 1 – Elements of model structures

File	Element	Description
IC model file	Header	IC type, model version, model level.
	External terminals	IC external terminals (package pins).
	Pad assignment	Connection between IC pads and package inner terminals.
	Circuit description	Internal circuits and their connections.
	Input stimulus assignment	Internal circuits and their stimuli to generate output waveforms.
	Input stimulus	Input waveforms.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	Package model reference	Name of the package model to be used.
Package model file	Header	Package name, model version, model level.
	Model name	List of models in package circuit model.
	Inner terminal	Cross-reference between internal terminals and package internal circuit model.
	Outer terminal	Cross-reference between external circuit and package internal circuit model.
	Circuit description	Internal circuits and their connections.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	Structure	Material, position, three-dimensional structures.
Module model file	Header	Module name, model version, model level.
	External terminals	External terminals (pins) of module.
	Circuit description	Internal circuits and their connections.
	Signal source	Internal circuits and their terminals to generate output waveforms at corresponding external terminals.
	Device model	Characteristics of non-linear circuits in one-dimensional, two-dimensional and three-dimensional table data. Non-linear devices are transistors, diodes and so on.
	IC/Module model reference	Names of IC/module model files and model names to be used.
	Structure	Material, position, three-dimensional structures.

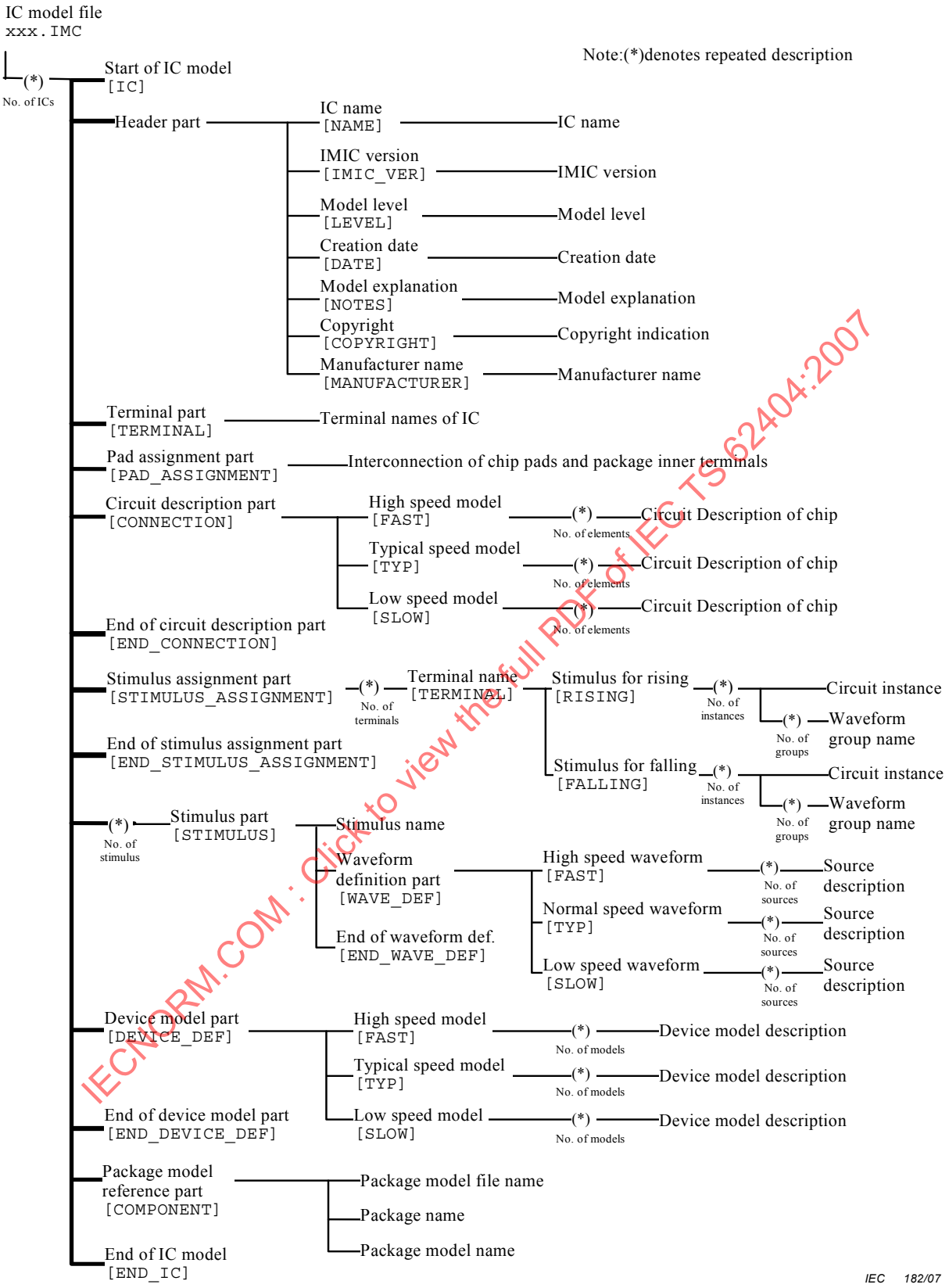


Figure 3 – Data structure of an IMIC model file for IC

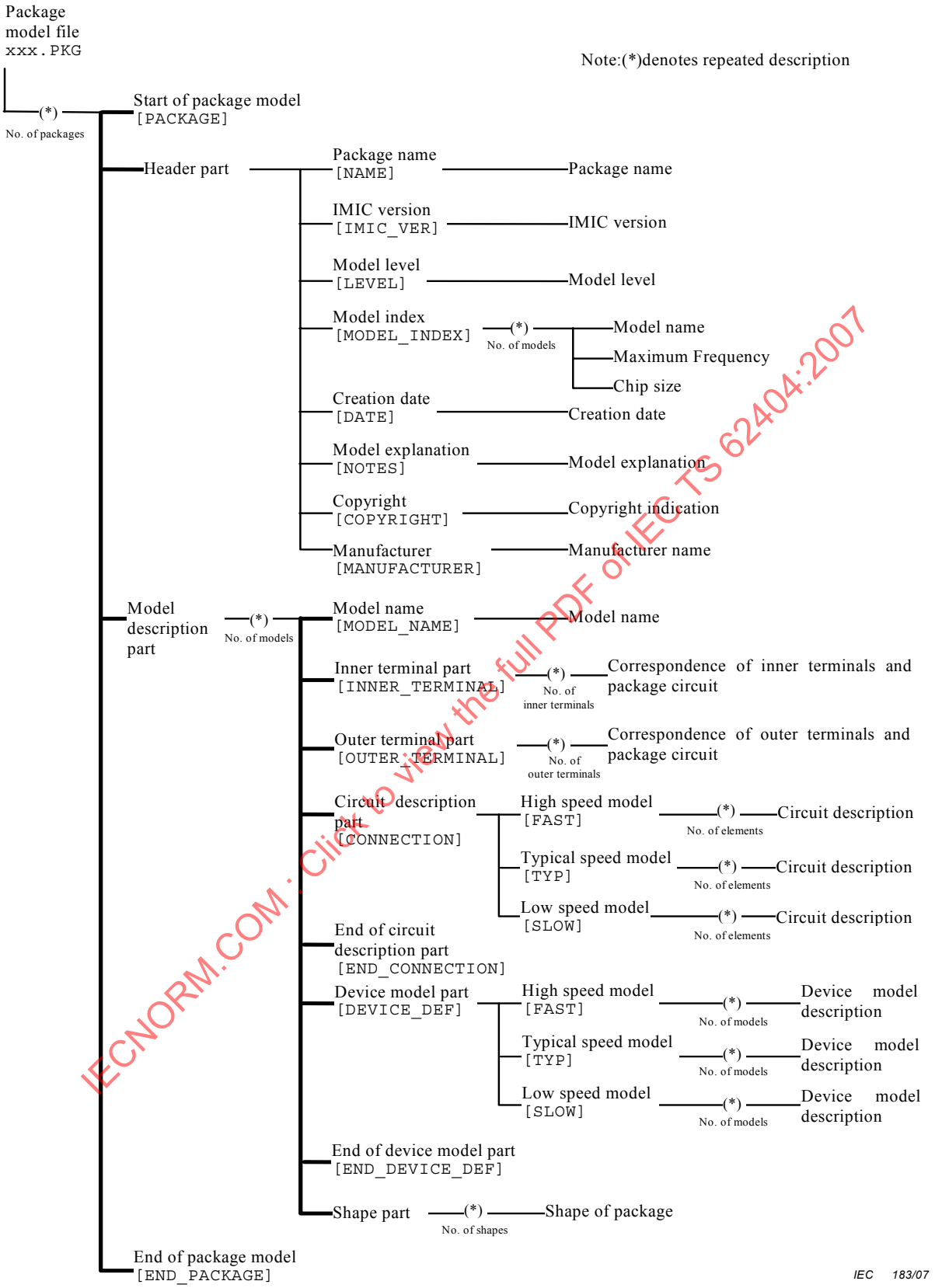


Figure 4 – Data structure of an IMIC model file for package

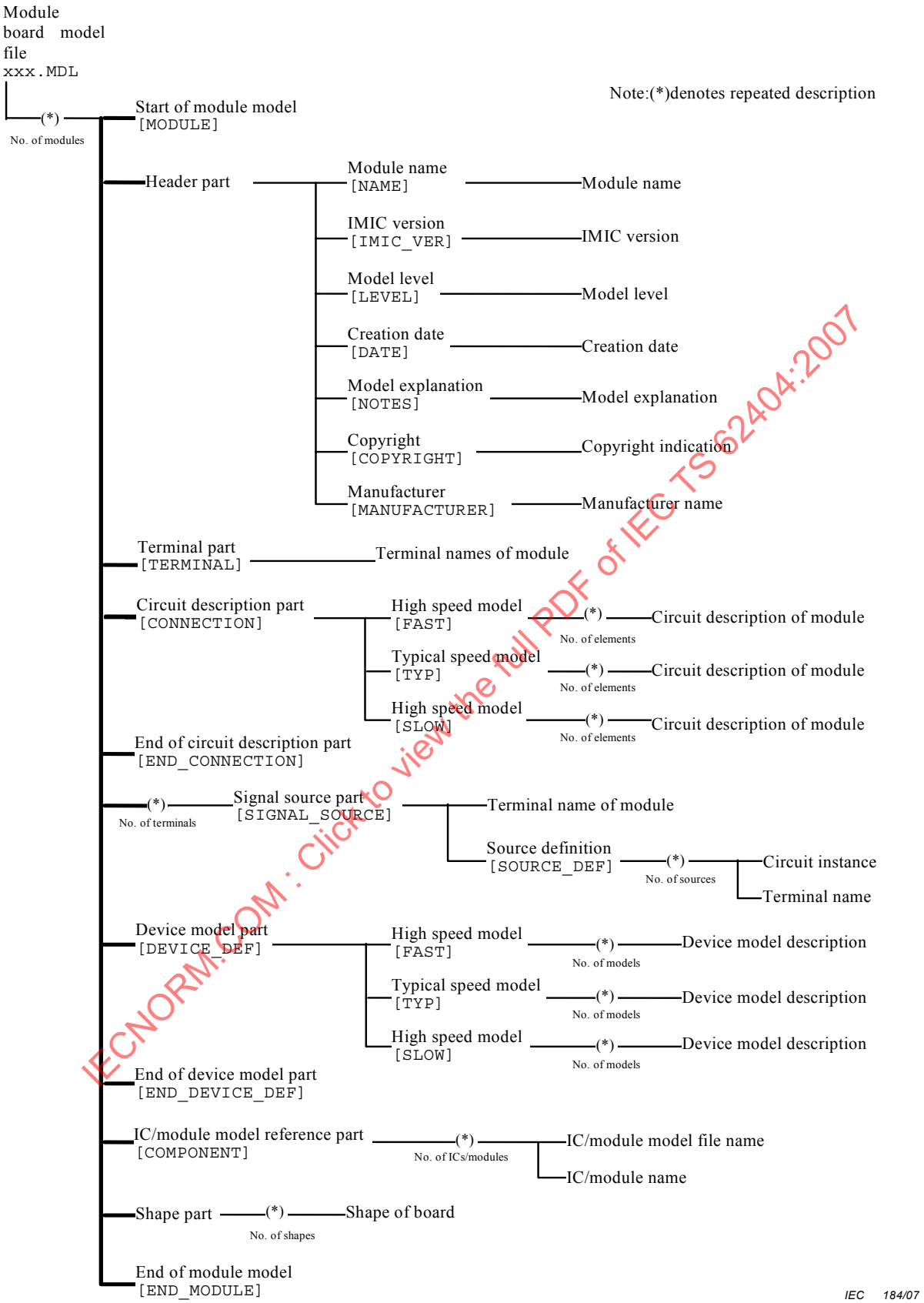


Figure 5 – Data structure of an IMIC model file for module

6 Detailed model description

6.1 Description rules

6.1.1 Characters

Recognition of characters in the model files is case insensitive. For instance, ‘M’ and ‘m’ are treated as the same character. It is recommended that all upper case or all lower case characters may be used.

6.1.2 Available characters

6.1.2.1 Available characters

A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, +, -, /, #, !, <, >, _ and %

6.1.2.2 Special characters

6.1.2.2.1 General

[ ]: Keywords

“ ‘: Equations

. : File Extension

Space, TAB: Delimiter

6.1.2.2.2 Example of equations

‘2.0*1+3’

“log(x)+2.3”

6.1.3 Keywords

6.1.3.1 General

Keywords shall be enclosed in square brackets, [ ], and shall be described from column 1 of the line. Tab or space cannot be used within [ ]. The detailed description shall be described on the same line and/or the following lines as the keyword. There are three types of keyword format:

6.1.3.2 Type-1

The detailed descriptions shall be placed between [*keyword*] line and [END_*keyword*] line.

Example:

[IC]

....

[END_IC]

6.1.3.3 Type-2

The detailed descriptions shall be placed next to the [*keyword*] line. There is no [END_*keyword*] line.

Example:

[TERMINAL]
SUBCKT ALVCH16244 SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG

6.1.3.4 Type-3

[*keyword*] shall be followed by the detailed descriptions on the same line. There is no [END_*keyword*] line.

Example:

[NAME] ALVCH16244

6.1.4 Numbers and numerical values

6.1.4.1 General

The decimal sign shall be "." (full-stop or period) on the line instead of "," (comma), against 6.6.8.1 of ISO/IEC Directives, Part 2, 2004 [1)] for the purpose of computer processing.

A scaling factor or scientific notation may be allowed. Either scaling factor or exponential expression may be used.

6.1.4.2 Scaling factor

T (tera) : 10^{12} G (giga) : 10^{9} MEG, X (mega) : 10^{6} K (kilo): 10^{3}

M (milli) : 10^{-3} U (micro): 10^{-6} N (nano): 10^{-9} P (pico): 10^{-12}

F (femto) : 10^{-15}

6.1.4.3 Scientific notation

Scientific notation shall use "E".

6.1.4.4 Examples

1.3X=1.3E6=1300K=1300E3=1300000

0.5U=5E-7=500N=500E-9=0.0000005

6.1.5 Comment

When the first letter on the line is asterisk "*", the rest of text on the line is deemed as a comment. When "$" appears anywhere on the line, the rest of text on the line is deemed as a comment.

6.1.6 Continuous lines

Any statement beginning with "+" is considered to be a continuation of the previous statement.

---

1) ISO/IEC Directives, Part 2, 2004: *Rules for the structure and drafting of International Standards*

6.1.7 Reserved node names

The reserved node names for ideal reference ground are 0, GND, GND! and GROUND. Therefore, these node names cannot be used as signal names.

6.1.8 Order of descriptions

Descriptions in the file shall be ordered as shown in Figures 3, 4, and 5, where items at the top of a solid vertical line are to be described at the beginning, and items at the bottom are to be described at the end. Items along horizontal line may appear in any order with respect to each other.

6.2 IC model file

6.2.1 File name

6.2.1.1 General

The name of the model file starts with any alphabetical or numerical characters, with .IMC as an extension.

6.2.1.2 Example

ALVCH16244.IMC

NOTE The limitation of file name length (number of characters) depends on operating system.

6.2.2 Start and end of model description

6.2.2.1 General

The description of one model shall be represented as the single IC model.

6.2.2.2 Start of IC model description

6.2.2.2.1 Description

[IC]

6.2.2.2.2 Explanation

The contents of the model follow with this description.

6.2.2.3 End of IC model description

6.2.2.3.1 Description

[END_IC]

6.2.2.3.2 Explanation

The description of the IC model shall be terminated by this keyword.

6.2.3 Header

6.2.3.1 General

IC type, model level etc. shall be described as the beginning statement of IC model.

6.2.3.2 IC type

6.2.3.2.1 Description

[NAME] arbitrary text

6.2.3.2.2 Explanation

This indicates the IC type identifier, which includes Product Number and/or Name.

This is used by simulators to assign the correct model for an IC in a design.

6.2.3.2.3 Example

[NAME] ALVCH16244

6.2.3.3 Model version

6.2.3.3.1 Description

[IMIC_VER] arbitrary text

6.2.3.3.2 Explanation

The version number of the IMIC specification shall be described. Currently, only version 1.3 is available. Parsers shall follow the appropriate syntax rules for the entire IC model.

6.2.3.3.3 Example

[IMIC_VER] 1.3

6.2.3.4 Model level

6.2.3.4.1 Description

[LEVEL] Integer

6.2.3.4.2 Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise.

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise.

Level 3: EMI (Electromagnetic Interference) model for the analysis of conducted electromagnetic emission noise. This level is not available in this version.

Detailed specification is explained in Clause 7.

6.2.3.4.3 Example

[LEVEL] 2

6.2.3.5 Date

6.2.3.5.1 Description

[DATE] date

6.2.3.5.2 Explanation

The model release date is described using any of the following formats.

– Day / Month name / Year Example: 23MAR98
– Month name Day, Year Example: MARCH 23, 1998

6.2.3.5.3 Example

[DATE] 23MAR98

6.2.3.6 Explanation of model

6.2.3.6.1 Description

[NOTES]

Arbitrary notes concerning the model shall be described if appropriate. This may be used for explanations of the origin, usage, and testing of the model, for example.

6.2.3.6.2 Explanation

Any comments can be described on the lines following [NOTES].

6.2.3.6.3 Example

[NOTES]
ELECTRICAL MODEL FOR ALVCH16244

6.2.3.7 Copyright

6.2.3.7.1 Description

[COPYRIGHT] arbitrary text

6.2.3.7.2 Explanation

Copyright holder and related terms shall be stated.

6.2.3.7.3 Example

[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED

6.2.3.8 Manufacturer

6.2.3.8.1 Description

[MANUFACTURER] arbitrary text

6.2.3.8.2 Explanation

Manufacturer is declared here.

6.2.3.8.3 Example

[MANUFACTURER] ZYX CORP.

6.2.4 Terminals

6.2.4.1 General

The external terminals of IC shall be defined. The external terminals are equivalent to the IC pins.

6.2.4.2 Description

[TERMINAL]

Arbitrary text

6.2.4.3 Explanation

The external terminals of the IC are defined.

The data begin on the line following [TERMINAL].

Signal names of external terminals at [PAD_ASSIGNMENT] shall be described.

The IC type name follows the string ".SUBCKT", and the names of terminals follow that.

6.2.4.4 Example

[TERMINAL]

.SUBCKT ALVCH16244 SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG

6.2.5 Pad assignment (see Figure 6)

6.2.5.1 General

The interconnections between chip pads and package inner terminals shall be described.

6.2.5.2 Description

[PAD_ASSIGNMENT]

Arbitrary text

6.2.5.3 Explanation

6.2.5.4 General

The interconnections between chip pads and package inner terminals are described.

The data begin on the line following [PAD_ASSIGNMENT].

Signal names of package inner terminals that are connected to chip pads shall be coincident with the signal names of the corresponding chip pads in ".SUBCKT" statement in [CONNECTION].

The data are given as subcircuit instance statements, starting with "X".

The subcircuit name of the top level ".SUBCKT" in [CONNECTION] shall appear after the terminal names at the end of this statement.

Following SPICE conventions, use of a particular node name (also known as a signal name) on both the chip instance and the package instance signifies a connection between these terminals.

NOTE If a chip pad is not connected to any package pad, the chip pad terminal shall be connected to signal "NO_CONNECTION". If a package inner terminal is not connected to any chip pad, the inner terminal shall be connected to signal "NO_CONNECTION".

6.2.5.5 Example

In the example below, the signal “SIG1I” is the first terminal of the CHIP connection to the first terminal of the PACKAGE.

[PAD_ASSIGNMENT]

XCHIP SIG1I SIG2I SIG3I SIG4I SIG5I SIG6I CHIP

XPACKAGE SIG1I SIG2I SIG3I SIG4I SIG5I SIG6I

+ SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG PACKAGE

[CONNECTION]

SUBCKT CHIP PAD1 PAD2 PAD3 PAD4 PAD5 PAD6

ENDS CHIP

<Package model file>

[CONNECTION]

SUBCKT PACKAGE L1I L2I L3I L4I L5I L6I

+ LEAD1 LEAD2 LEAD3 LEAD4 LEAD5 LEAD6 LEAD7 REFG

ENDS PACKAGE

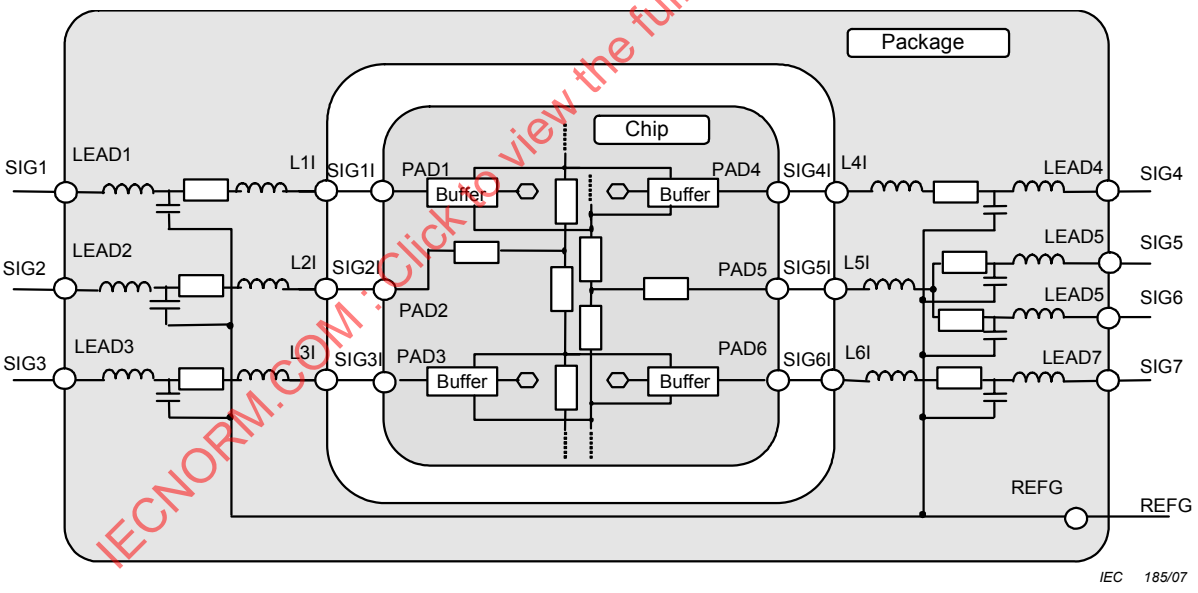


Figure 6 – Pad assignment

6.2.6 Circuit description (see example in Figure 7)

6.2.6.1 General

The elements of the internal circuit and their interconnections shall be described.

6.2.6.2 Description

[CONNECTION]

[FAST]

[TYP]

[SLOW]
[END_CONNECTION]

6.2.6.3 Explanation

6.2.6.3.1 General

The elements of internal circuit and their interconnections shall be described. The description is terminated with [END_CONNECTION].

Circuit descriptions with keywords are described after [CONNECTION].

These keywords are optional.

[FAST] Circuit description for the highest speed.

[TYP] Circuit description for typical speed.

[SLOW] Circuit description for the lowest speed.

The internal circuit of the chip contains the pad capacitance model statements.

The top level description of the internal circuit shall be described between ".SUBCKT" and ".ENDS".

".SUBCKT" shall be described together with subcircuit name of the top level circuit and pad signal names.

".ENDS" shall be described together with subcircuit name of the top level circuit.

The general circuit description is as follows.

Element_Name <Node_Name> [Value] [Model_Name] <[Parameter = Parameter_Value]>

Where, < > indicates repeatable, and [ ] indicates optional.

Available elements include the following: resistor, capacitor, inductor, mutual inductor, diode, MOS transistor, bipolar transistor, voltage-controlled voltage source, current-controlled current source, voltage-controlled current source, current-controlled voltage source, lossless transmission line, independent voltage source, independent current source, subcircuit call, and subcircuit description. The first character of each element statement denotes the element type. The model name shall be defined in the device description.

Each element description is as follows.

6.2.6.3.2 Resistor

Rxxxxxxx node1 node2 *value* or model_name

Where unit of *value* is ohm.

6.2.6.3.3 Capacitor

Cxxxxxxx node1 node2 *value* or model_name

Where unit of *value* is (F) Farad.

6.2.6.3.4 Self-inductor

Lxxxxxxx node1 node2 *value*

Where unit of *value* is (H) Henry.

6.2.6.3.5 Mutual-inductor

Kxxxxxxx lname1 lname2 *Coupling_coefficient*

Where lname1 and lname2 are self-inductance names.

6.2.6.3.6 Diode

Dxxxxxxx node1 node2 model_name AREA=*area_factor*

6.2.6.3.7 MOS transistor

Mxxxxxxx node1 node2 node3 node4 model_name L=*gate_length* W=*gate_width*
[+ AD=*drain_diffusion_area* AS=*source_diffusion_area*]
[+ PD=*perimeter_of_drain_junction* PS=*perimeter_of_source_junction*]
[+ NRD=*number_of_squares_of_drain_diffusion*]
[+ NRS=*number_of_squares_of_source_diffusion*]

Where the units of *gate_length*, *gate_width*, *perimeter_of_drain_junction*, *perimeter_of_source_junction* are meters, and those of *drain_diffusion_area* and *source_diffusion_area* are m^2.

AD, AS, PD, PS, NRD and NRS are optional. The default value for these is 0,0.

These values are not necessarily coincident with the real size of any chip dimension. Characteristics of individual transistors will be calculated by using equations with dependence of L, W, AD, AS, PD and PS, which are defined in the device model description.

It will be described in detail in 6.2.8.3.3.

6.2.6.3.8 Bipolar transistor

Qxxxxxxx node1 node2 node3 model_name AREA=*area_factor*

6.2.6.3.9 Voltage-controlled voltage source

Exxxxxxx node1 node2 POLY=*n* <cnode1 cnode2> <*k*>

Where cnode1 and cnode2 are controlling nodes and *k* is the list of polynomial coefficients.

6.2.6.3.10 Current-controlled current source

Fxxxxxxx node1 node2 POLY=*n* <vname> <*k*>

Where vname are voltage sources and *k* is the list of polynomial coefficients.

6.2.6.3.11 Voltage-controlled current source

Gxxxxxxx node1 node2 POLY=*n* <cnode1 cnode2> <*k*>

Where *cnode1* and *cnode2* are controlling nodes and *k* is the list of polynomial coefficients.

6.2.6.3.12 Current-controlled voltage source

Hxxxxxxx node1 node2 POLY=*n* <vname> <*k*>

Where vname are voltage sources and *k* is the list of polynomial coefficients.

6.2.6.3.13 Lossless transmission line

Txxxxxxx node1 node2 node3 node4 Z0=*characteristic_impedance* TD=*transmission_delay*

6.2.6.3.14 Independent voltage source

6.2.6.3.14.1 General

Vxxxxxxx node1 node2 [tranfun] [DC=]*dcvalue* [AC=*acmag*, [*acphase*]]

Where *dcvalue* is a value of DC voltage source, *acmag* is a magnitude value of AC voltage and *acphase* is a phase value of AC voltage.

Where tranfun is functional description of transient voltage source described below:

6.2.6.3.14.2 Pulse source function

PULSE *v1 v2* [*td* [*tr* [*tf* [*pw* [*per*]]]]]

Where *v1* is initial value, *v2* is pulse plateau value, *td* is delay time, *tr* is duration of the onset ramp, *tf* is duration of the recovery ramp, *pw* is pulse width, and *per* is pulse repetition period.

6.2.6.3.14.3 Sinusoidal source function

SIN *vo va* [*freq* [*td* [θ [φ]]]]

Where *vo* is voltage or current offset value, *va* is voltage or current amplitude, *freq* is frequency, *td* is delay time, θ is damping factor, and φ is phase delay time.

6.2.6.3.14.4 Exponential source function

EXP *v1 v2* [*td* [$\tau 1$ [*td2* [$\tau 2$]]]]

Where *v1* is initial voltage or current value, *v2* is pulsed value of voltage or current, *td* is rise delay time, *td2* is fall delay time, $\tau 1$ is rise time constant and $\tau 2$ is fall time constant.

6.2.6.3.14.5 Piecewise linear source function

PWL *t1 v1* [*t2 v2 t3 v3* …] [R [=repeat]] [TD=*delay*]

Where *vn* (*n*=1, 2, …) is voltage or current values, *tn* (*n*=1, 2, …) is segment time, repeat is the starting time of the waveform, which is to be repeated, and *delay* is delay time. R causes the function to repeat.

6.2.6.3.14.6 Single-frequency FM source function

SFFM *vo va* [*fc* [*mdi* [*fs*]]]

Where *vo* is voltage or current offset value, *va* is voltage or current amplitude, *fc* is carrier frequency, *mdi* is modulation index value and *fs* is single frequency.

6.2.6.3.15 Independent current source

Ixxxxxxx node1 node2 [tranfun] [DC=]*dcvalue* [AC=*acmag*, [*acphase*]]

Where *dcvalue* is a value of DC current source, *acmag* is a magnitude value of AC current and *acphase* is a phase value of AC current.

Where tranfun is functional description of transient current source described in 6.2.6.3.14.

6.2.6.3.16 Subcircuit call

Xxxxxxxx <node> subcircuit_name

6.2.6.3.17 Subcircuit definition

.SUBCKT subcircuit_name <node>

6.2.6.4 Example

```
[CONNECTION]
[TYP]
.SUBCKT CHIP OUT1 OUT2 VCC GND0 SUB
R1 VCC2 VCC1 1.0
R2 VCC1 VCC3 1.2
R3 GND2 GND1 1.1
R4 GND1 GND3 0.9
R5 VCC1 VCC 0.5
R6 GND1 GND0  0.5
C1 VCC2  SUB   1P
C2 VCC3  SUB   1P
X1 IN1 OUT1 VCC2 GND2 BUFFER
X2 IN2 OUT2 VCC3 GND3 BUFFER
.ENDS CHIP
.SUBCKT BUFFER IN OUT VCC GND0
M1 IN OUT VCC VCC PMOS L=1U W=10U
M2 IN OUT GND0 GND0 NMOS L=1U W=10U
D1 OUT VCC D AREA=2
D2 GND0 OUT D
.ENDS BUFFER
[END_CONNECTION]
```

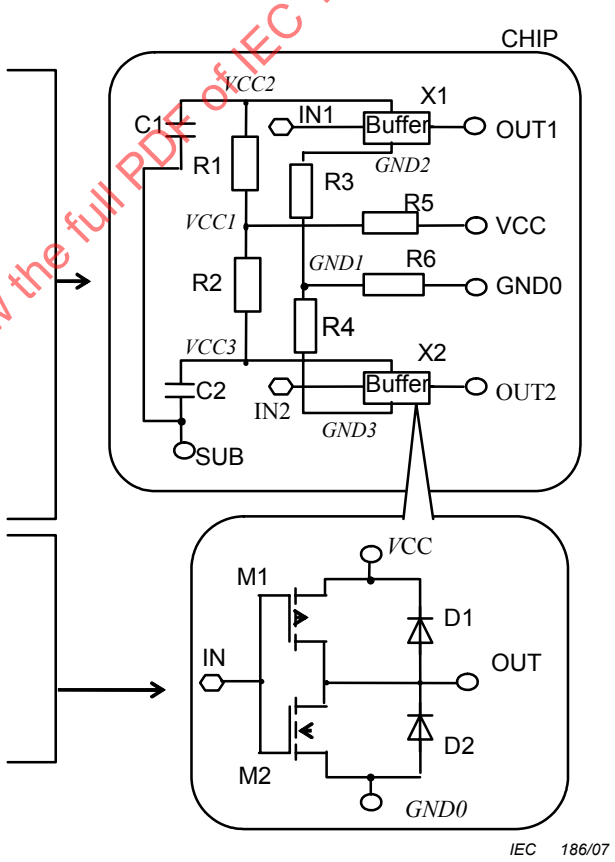


Figure 7 – Example of circuit description

NOTE The grounds of internal circuits of ICs are connected to package ground terminals.

6.2.7 Input stimulus (see Figure 8)

6.2.7.1 General

In order to describe the effect of loading on the output waveforms of buffer circuits, the input stimuli shall be defined both for rising and falling edges of the output buffer circuits.

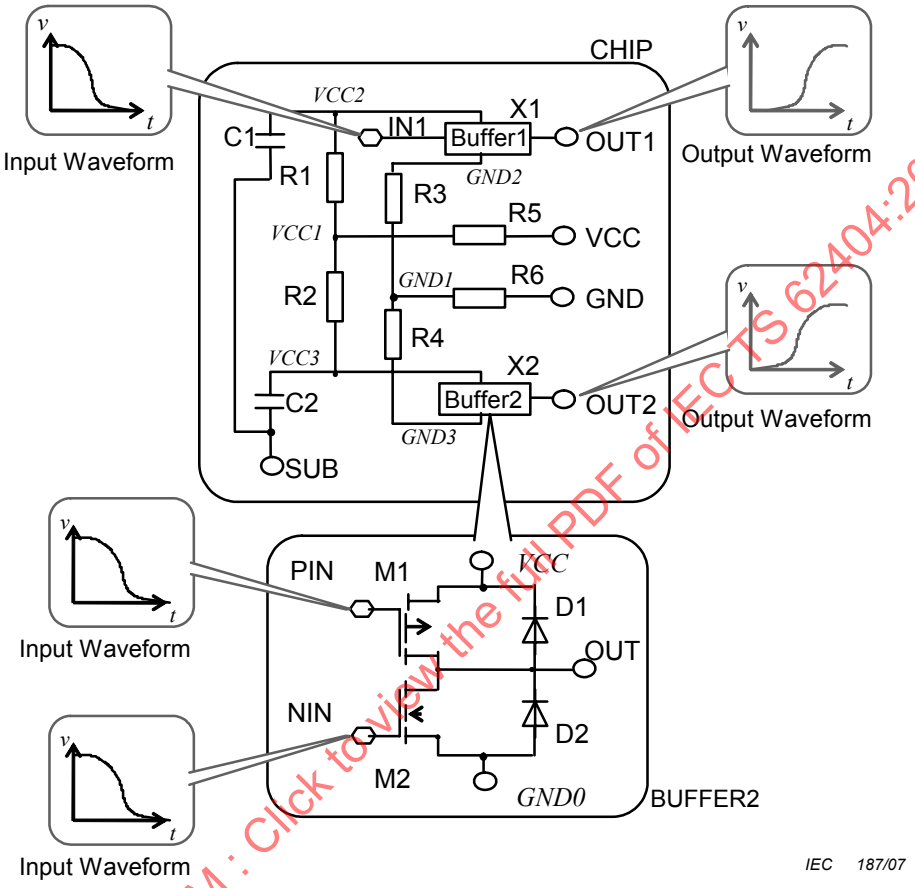


Figure 8 – Input stimulus

6.2.7.2 Input stimulus assignment

6.2.7.2.1 Description

[STIMULUS_ASSIGNMENT]

[TERMINAL] External terminal name of IC

[RISING]

[FALLING]

[END_STIMULUS_ASSIGNMENT]

6.2.7.2.2 Explanation

This defines the input stimulus names of output buffer circuits so that it can control the output waveforms of IC. The input stimulus section begins with [STIMULUS_ASSIGNMENT] and terminates with [END_STIMULUS_ASSIGNMENT]. The [STIMULUS_ASSIGNMENT] section contains one or more [TERMINAL] subsections, each defining the stimulus waveform to be applied for one chip pad terminal.

[TERMINAL] External terminal name of IC

The external terminal name of the IC shall match one of the signal names at the external terminals defined by the ".SUBCKT" in [TERMINAL]. Each [TERMINAL] section contains [RISING] and [FALLING] subsections to introduce separate stimulus waveforms to be used for rising and falling edges of the signal.

[RISING]

The input stimulus to control the rising waveforms of external terminals shall be defined following this keyword.

The first parameter is a reference name of the circuit with which the stimulus is provided.

For reference of the top hierarchy of the chip, the reference name shall be one of the items defined by [PAD_ASSIGNMENT].

For reference of the lower hierarchy level of the chip, the reference name shall be one of the subcircuit call names defined in [CONNECTION].

The other parameters are the names of waveforms defined by [STIMULUS]. These can be described in the same line such as:

Circuit_reference_name Stimulus_1 Stimulus_2 Stimulus_3…

[FALLING]

The input stimulus to control the falling waveforms of external terminals shall be defined following this keyword.

The first parameter is a reference name of the circuit with which the stimulus is provided.

For reference of the top hierarchy of the chip, the reference name shall be one of the items defined by [PAD_ASSIGNMENT].

For reference of the lower hierarchy level of the chip, the reference name shall be one of the subcircuit call names defined in [CONNECTION].

The other parameters are the names of waveforms defined by [STIMULUS]. These can be described in the same line such as:

Circuit_reference_name Stimulus_1 Stimulus_2 Stimulus_3…

6.2.7.2.3 Example

[STIMULUS_ASSIGNMENT]
[TERMINAL] OUT1
[RISING]
XCHIP WAVE1R
[FALLING]
XCHIP WAVE1F
[TERMINAL] OUT2
[RISING]
XCHIP.X2 WAVE2R
[FALLING]

XCHIP.X2 WAVE2F

[END_STIMULUS_ASSIGNMENT]

6.2.7.3 Input stimulus definition

6.2.7.3.1 Description

[STIMULUS] Stimulus Names

[WAVE_DEF]

[FAST]

[TYP]

[SLOW]

[END_WAVE_DEF]

6.2.7.3.2 Explanation

This defines the input stimuli of output buffer circuits so that they can control the output waveforms of the ICs.

Stimulus names shall be described after the [STIMULUS]. These are the names to be used for [WAVE_DEF]. Actual waveforms shall be described by the circuit statements following these keywords.

[FAST]: Definition of the highest speed.

[TYP]: Definition of the typical speed.

[SLOW]: Definition of the lowest speed.

These keywords are optional. Actual waveforms shall be defined from the next line of these keywords. The waveforms can be described using an independent voltage source or an independent current source (see 6.2.6.3.14 and 6.2.6.3.14.2). More than one stimulus can be described.

The description of actual waveforms is terminated with [END_WAVE_DEF].

6.2.7.3.3 Example

[STIMULUS] WAVE1R

[WAVE_DEF]

[FAST]

VIN1 IN1 GND PWL 0 3.3 4.8N 3.3 5.5N 0

[TYP]

VIN1 IN1 GND PWL 0 3.3 5N 3.3 6N 0

[SLOW]

VIN1 IN1 GND PWL 0 3.3 5.2N 3.3 6.4N 0

[END_WAVE_DEF]

[STIMULUS] WAVE2R

[WAVE_DEF]

[FAST]

VIN2 PIN GND PWL 0 3.3 2.8N 3.3 3.6N 0

VIN3 NIN GND PWL 0 3.3 2.6N 3.3 3.6N 0

[TYP]
VIN2 PIN GND PWL 0 3.3 3N 3.3 4N 0
VIN3 NIN GND PWL 0 3.3 3N 3.3 4N 0
[SLOW]
VIN2 PIN GND PWL 0 3.3 3.2N 3.3 4.3N 0
VIN3 NIN GND PWL 0 3.3 3.2N 3.3 4.3N 0
[END_WAVE_DEF]
[STIMULUS] WAVE1F
[WAVE_DEF]
[FAST]
VIN1 IN1 GND PWL 0 0 4.8N 0 5.6N 3.3
[TYP]
VIN1 IN1 GND PWL 0 0 5N 0 6N 3.3
[SLOW]
VIN1 IN1 GND PWL 0 0 5.2N 0 6.5N 3.3
[END_WAVE_DEF]
[STIMULUS] WAVE2F
[WAVE_DEF]
[FAST]
VIN2 PIN GND PWL 0 3.3 2.8N 3.3 3.6N 0
VIN3 NIN GND PWL 0 3.3 2.N 3.3 3.6N 0
[TYP]
VIN2 PIN GND PWL 0 3.3 3N 3.3 4N 0
VIN3 NIN GND PWL 0 3.3 3N 3.3 4N 0
[SLOW]
VIN2 PIN GND PWL 0 3.3 3.2N 3.3 4.4N 0
VIN3 NIN GND PWL 0 3.3 3.2N 3.3 4.4N 0
[END_WAVE_DEF]

NOTE The stimuli defined by [FAST], [TYP] and [SLOW] correspond to the characteristics of non-linear devices for [FAST], [TYP], and [SLOW] operating conditions, respectively. Thus, simulation for [TYP] stimulus shall use corresponding [TYP] non-linear characteristics of device models.

6.2.8 Device model

6.2.8.1 General

One-dimensional, two-dimensional or three-dimensional data of the characteristics of non-linear devices shall be described. Non-linear devices are those such as transistors, diodes, voltage dependent capacitors and so on.

The units to describe those device models comply with the SI units.

6.2.8.2 Description

[DEVICE_DEF]
[FAST]
[TYP]
[SLOW]

[END_DEVICE_DEF]

6.2.8.3 Explanation

6.2.8.3.1 General

This defines device models to be used in the definition of the internal circuit of the IC. The definition of the device model shall be terminated with [END_DEVICE_DEF]. The device model of the internal circuit shall be defined by using the following keywords after [DEVICE_DEF].

[FAST]: Definition of the highest speed.

[TYP]: Definition of the typical speed.

[SLOW]: Definition of the lowest speed.

These keywords are optional. General description of device models is as follows.

MODEL Model_name Model_type <[Parameter_name = *Parameter_value*]>

Where < > indicates repeatable and [ ] indicates optional.

6.2.8.3.2 **Diode model** (see Figures 9 and 10)

The Model_type shall follow with "MODEL=TABLE", "RS=*series_resistance_value*", "POINTS=*Number_of_data_points*" and <*Voltage_value*, *Current_value*, *Capacitance_value*>.

A set of numbers is composed of three values of parameters. If any parameters have the same value in every set of numbers, the parameters may be abbreviated from every set of numbers, adding "Parameter_name=*Parameter_value*" following "POINTS=*Number_of_data_points*".

Number_of_data_points is the number of sets of parameter values.

"RS=*series_resistance_value*" is optional. In default, RS=0,0.

Equivalent circuit

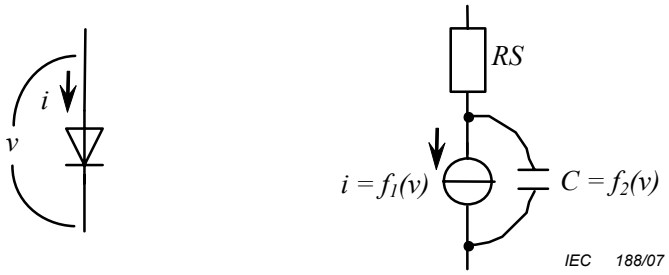


Figure 9 – Diode equivalent circuit

Example

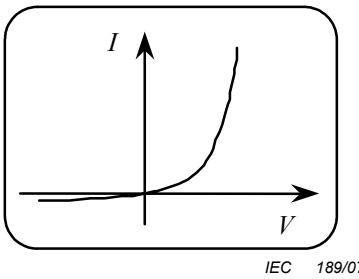


Figure 10 – Diode characteristics

```
[DEVICE_DEF]
[FAST]
MODEL DIODE D MODEL=TABLE
+ RS=3.2
+ POINTS=16
*      V       I       C
+    -2.0000   -2.9003P  371.8970F
+    -1.8000   -2.6102P  380.7287F
+    -1.6000   -2.3202P  391.3235F
+    -1.4000   -2.0302P  403.3597F
+    -1.2000   -1.7402P  415.3959F
+    -1.0000   -1.4501P  427.4321F
+ -800.0000M   -1.1601P  446.4778F
+ -600.0000M -870.0789F  467.8601F
+ -400.0000M -580.0526F  489.2424F
+ -200.0000M -290.0263F  510.6247F
+  0.   6.9045P  546.8902F
+  200.0000M   66.3353N  586.3105F
+  400.0000M   68.0767U  626.7824F
+  600.0000M   1.8949  667.2543F
+  800.0000M   481.9861  707.7262F
+  1.0000  116.2491K  748.1981F
[END_DEVICE_DEF]
```


6.2.8.3.3 **MOS transistor model** (see Figures 11 and 12)

6.2.8.3.3.1 General

The Model_type shall follow with "MODEL=TABLE", "L=*gate_length*", "W=*gate_width*", "AD=*drain_diffusion_area*", "AS=*source_diffusion_area*", "PD=*perimeter_of_drain_junction*", "PS=*perimeter_of_source_junction*" and "RSH=*drain_and_source_diffusion_sheet_resistance*".

AD, AS, PD, PS and RSH are optional. Default value for these is 0,0.

If any value is 0,0, the dependency equations corresponding to the value will not be used.

The dependency equations are described in detail in 6.2.8.3.9 and 6.2.8.3.10. In spite of these equations, it is highly recommended that MOS transistors for each gate length that is used should be modelled independently to obtain accurate simulation result.

Equivalent circuit

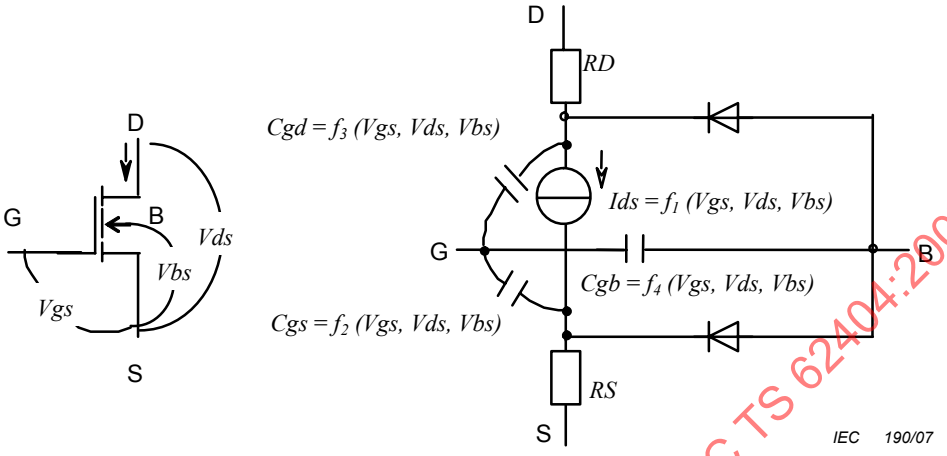


Figure 11 – NMOS transistor equivalent circuit

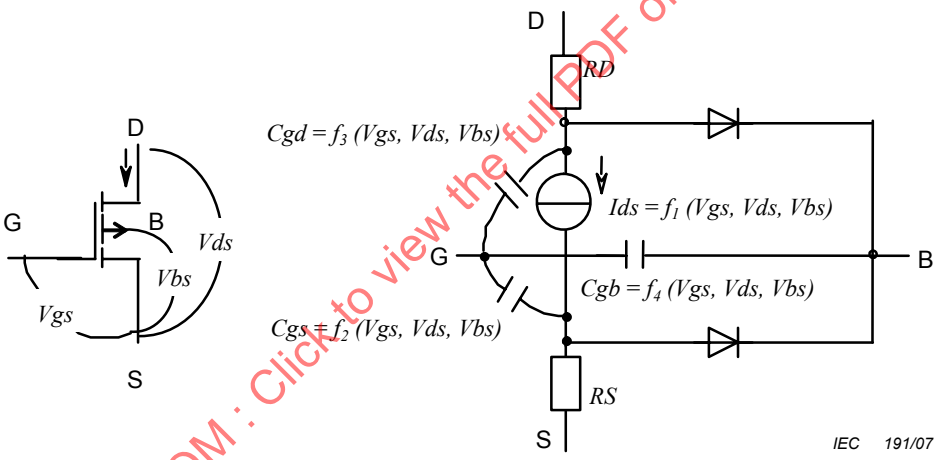


Figure 12 – PMOS transistor equivalent circuit

6.2.8.3.3.2 **Gate channel characteristics** (see Figure 13)

DC and capacitance characteristics of the gate channel of MOS transistors shall be described. "DATA=CHANNEL" shall be followed by "POINTS=*Number_of_data_points*", <*Gate-source_voltage_value* (*Vgs*), *Drain-source_voltage_value* (*Vds*), *Bulk-source_voltage_value* (*Vbs*), *Drain_current_value* (*Ids*), *Gate-source_capacitance_value* (*Cgs*), *Gate-drain_capacitance_value* (*Cgd*), and *Gate-bulk_capacitance_value* (*Cgb*)>.

A set of numbers is composed of seven values of parameters. If any parameter has the same value in every set of numbers, the parameter may be abbreviated from every set of numbers, adding "Parameter_name=*Parameter_value*" following "POINTS=*Number_of_data_points*".

For example, if *Vbs* is 0,0 in every set of numbers, "VBS=0.0" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 6 parameter values.

Number_of_data_points is the number of sets of parameter values.

Regarding the polarities of the values at the operation region of MOS transistor, all the parameters are positive for NMOS, *Vgs*, *Vds* and Ids are negative and *Cgs*, *Cgd*, and *Cgb* are positive for PMOS.

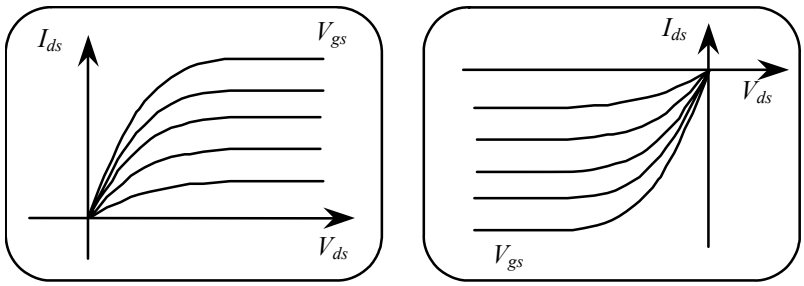


Figure 13 – Gate channel characteristics of MOS transistor

Example

```
[DEVICE_DEF]
[TYP]
MODEL MODEL1 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=30U PS=30U RSH=10.2
+ DATA=CHANNEL
+ POINTS=40
* Vgs   Vds  Vbs  Ids   Cgs   Cgd  Cgb
+ 0.0 0.095 0.2  2.0M  0.5N  0.5N 3.5N
+ 0.0 0.095 0.3  2.1M  0.7N  0.5N 4.0N
+ 0.2   2.1 0.2  2.0M  0.5N  0.5N 3.5N
+ 0.5   4.0 0.3  2.1M  0.7N  0.5N 4.0N
+ ...
MODEL MODEL2 PMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=90
+ VBS=0.0
*  Vgs   Vds    Ids   Cgs   Cgd  Cgb
+   0.0 -0.095  -2.0M  0.5N  0.5N 3.5N
+   0.0 -0.095  -2.1M  0.7N  0.5N 4.0N
+ -0.2   -2.1   -2.0M  0.5N  0.5N 3.5N
+ -0.5   -4.0   -2.1M  0.7N  0.5N 4.0N
+ ...
[END_DEVICE_DEF]
```

6.2.8.3.3.3 **Diode characteristics** (see Figure 14)

The DC and capacitance characteristics of diodes between source and substrate and between drain and substrate shall be described.

"DATA=DRAIN" for the characteristics of DC and capacitance between drain and substrate of diode shall follow with "POINTS=*Number_of_data_points*", <*Bulk-drain_voltage_value* (*Vbd*), *Bulk-drain_current_value* (*Ibd*), *Bulk-drain_capacitance* (*Cbd*) and *Sidewall_bulk-drain_junction_capacitance* (*Cbdsw*)>.

A set of numbers is composed of four values of parameters. If any parameter has the same value in every set of numbers, the parameter may be abbreviated from every set of numbers, adding "Parameter_name=*Parameter_value*" following "POINTS=*Number_of_data_points*".

For example, if *Cbd* is 1,2 pF in every set of numbers, "CBD=1.2P" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 3 parameter values.

Number_of_data_points is the number of sets of parameter values.

Regarding the polarities of the values for forward region of diode, all the parameters are positive for NMOS, *Vbd* and *Ibd* are negative and *Cbd* is positive for PMOS.

"DATA=SOURCE" for the characteristics of DC and capacitance between source and substrate of diode shall follow with "POINTS=*Number_of_data_points*", < *Bulk-source_voltage_value*(*Vbs*), *Bulk-source_current_value*(*Ibs*), *Bulk-source_capacitance*(*Cbs*) *and Sidewall_bulk-source_junction_capacitance* (*Cbssw*) >.

A set of numbers is composed of four values of parameters. If any parameter has the same value in every set of numbers, the parameter may be abbreviated from every set of numbers, adding "Parameter_name=*Parameter_value*" following "POINTS=*Number_of_data_points*".

For example, if *Cbs* is 1,2 pF in every set of numbers, "CBS=1.2P" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 3 parameter values.

Number_of_data_points is the number of sets of parameter values.

Regarding the polarities of the values for forward region of diode, all the parameters are positive for NMOS, *Vbs* and *Ibs* are negative and *Cbs* is positive for PMOS.

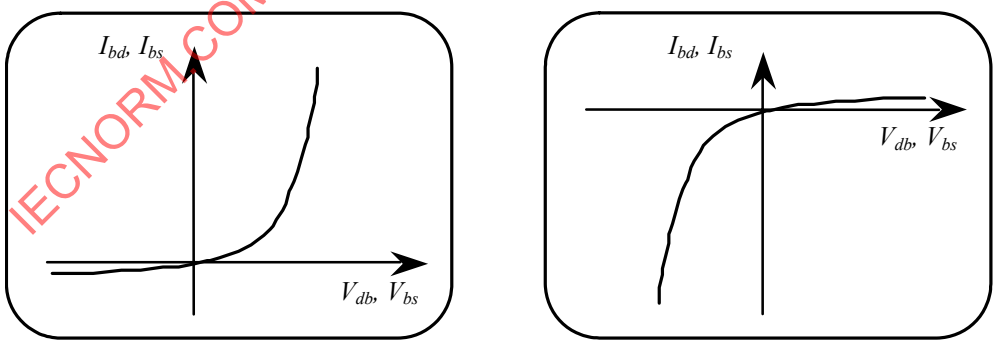


Figure 14 – Characteristics of diode in MOS transistor

Example

[DEVICE_DEF]

[SLOW]

MODEL MODEL1 NMOS MODEL=TABLE

+ L=0.8U W=10U AD=100P AS=100P PD=30U PS=30U RSH=10.2

```
+ DATA=CHANNEL
+ ...
+ DATA=DRAIN
+ POINTS=90
* Vbd    Ibd   Cbd    Cbdsw
+ -2.0  -0.095P 0.2P  0.01P
+  0.0   0.09M  0.3P   0.01P
+  0.6   4.0M   0.3P   0.012P
+ ...
+ DATA=SOURCE
+ POINTS=70
+ CBS=1.2P CBSSW=0.01P
* Vbs    Ibs
+ -2.0  -0.095P
+  0.0   0.09M
+  0.6   4.0M
+ ...
[END_DEVICE_DEF]
```

6.2.8.3.4 Bipolar transistor model (see Figures 15, 16 and 17)

The Model_type shall follow with "MODEL=TABLE", "POINTS=*Number_of_data_points*", "RB=*base_resistance_value*", <*Collector-emitter_voltage_value*(*Vce*), *Base-emitter_voltage_value*(*Vbe*), *Base_current_value*(*Ib*), *Collector_current_value*(*Ic*), *Collector-base_capacitance_value*(*Ccb*), *Collector-substrate_capacitance_value*(*Ccs*), and *Emitter-base_capacitance_value*(*Ceb*)>.

A set of numbers is composed of seven values of parameters. If any parameter has the same value in every set of numbers, the parameter may be abbreviated from every set of numbers, adding "Parameter_name=*Parameter_value*" following "POINTS=*Number_of_data_points*".

For example, if *Ccs* is 1,2 pF in every set of numbers, "CCS=1.2P" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 6 parameter values.

Number_of_data_points is the number of sets of parameter values.

"RB=*base_resistance_value*" is optional. In default, RB=0,0.

The signs of values are as follows. In the active region of a transistor, all values are positive for NPN and *Vce*, *Vbe* and *Ic* are negative and *Ccb*, *Ccs*, and *Ceb* are positive for PNP.

Equivalent circuit

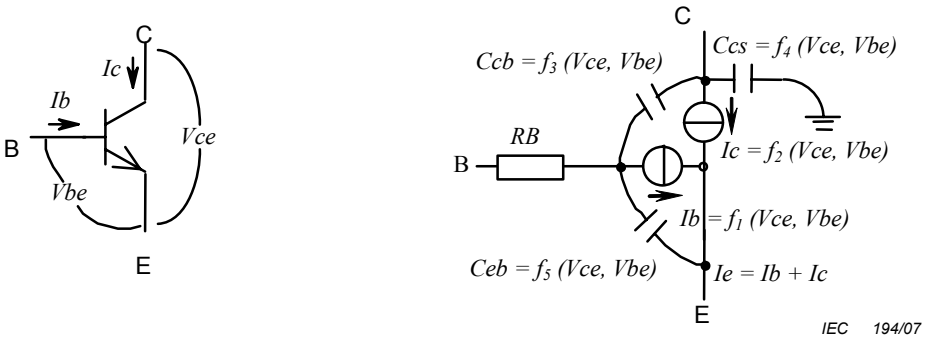


Figure 15 – NPN transistor equivalent circuit

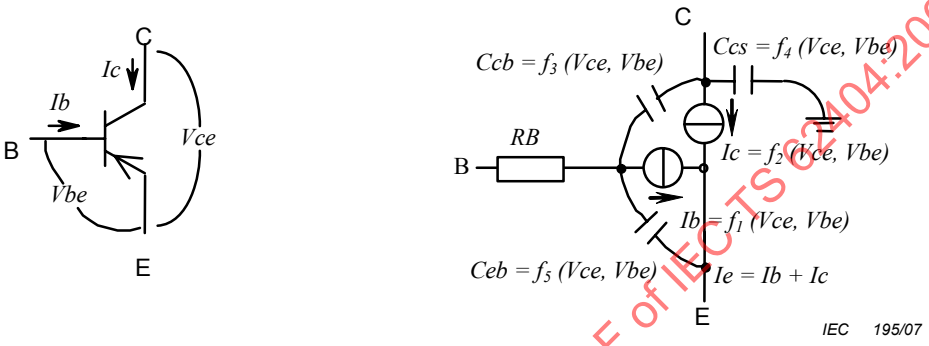


Figure 16 – PNP transistor equivalent circuit

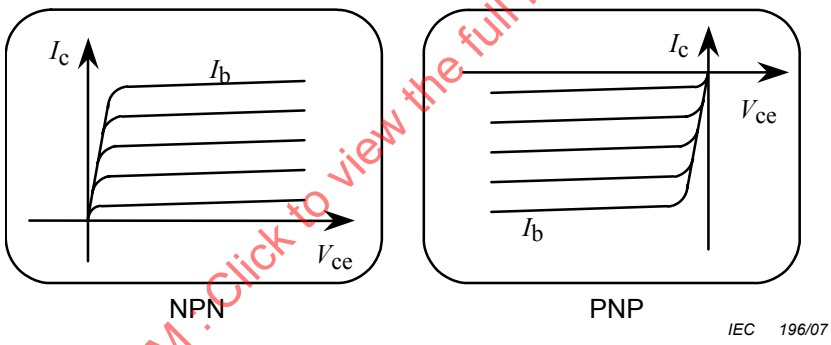


Figure 17 – Static characteristics of bipolar transistor

Example

```
[DEVICE_DEF]
[SLOW]
MODEL MODEL1 NPN MODEL=TABLE
+ RB=10
+ POINTS=70
* Vce  Vbe  Ib    Ic     Ccb   Ccs  Ceb
+ 0.0 0.2  0.1u  0.095M 0.36P 3.8P 0.85P
+ 0.2 0.2  2.0u   0.36M 0.36P 3.8P 0.85P
+ 0.5 0.2  9.0u   0.9M  0.4P  3.8P 0.85P
+ ...
.MODEL MODEL2 PNP MODEL=TABLE
+ RB=9.4
+ POINTS=70
```

```
+ CCS=3.8P
*  Vce  Vbe   Ib     Ic     Ccb   Ceb
+   0.0 -0.2  -0.1U  -0.095M 0.36P 0.85P
+ -0.2 -0.2  -2.0U  -0.36P  0.36P 0.85P
+ -0.5 -0.2  -3.5U  -0.4P   0.36P 0.85P
+ …
[END_DEVICE_DEF]
```

6.2.8.3.5 Example

```
[DEVICE_DEF]
[TYP]
MODEL DIODE D MODEL=TABLE
+ RS=3.2
+ POINTS=40
*  V      I      C
+ -0.5 -0.001P 0.2P
+  0.0  0.095M 0.2P
+  0.2  2.0M   0.2P
+  0.5  3.5M   0.2P
+ ...
.MODEL MODEL1 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=120
* Vgs   Vds  Vbs  Ids   Cgs   Cgd  Cgb
+ 0.0 0.095 0.2  2.0M  0.5N  0.5N 3.5N
+ 0.0 0.095 0.3  2.1M  0.7N  0.5N 4.0N
+ 0.2   2.1 0.2  2.0M  0.5N  0.5N 3.5N
+ 0.5   4.0 0.3  2.1M  0.7N  0.5N 4.0N
+ ...
+ DATA=DRAIN
+ POINTS=90
*  Vbd    Ibd   Cbd  Cbdsw
+ -2.0  -0.095P 0.2P  0.01P
+  0.0   0.09M  0.3P  0.01P
+  0.6   4.0M   0.3P  0.015P
+ ...
+ DATA=SOURCE
+ POINTS=90
+ CBS=1.2P CBSSW=0.01P
*  Vbs   Ibs
+ -2.0  -0.095P
+  0.0   0.09M
+  0.6   4.0M
+ ...
MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=120
+ VBS=0
* Vgs   Vds   Ids   Cgs   Cgd  Cgb
```

```
+ 0.0 0.095  2.0M  0.5N  0.5N 3.5N
+ 0.0 0.095  2.1M  0.7N  0.5N 4.0N
+ 0.2   2.1  2.0M  0.5N  0.5N 3.5N
+ 0.5   4.0  2.1M  0.7N  0.5N 4.0N
+ ...
+ DATA=DRAIN
+ POINTS=90
+ CBDSW=0.01P
*  Vbd    Ibd   Cbd
+ -2.0  -0.095P 0.2P
+  0.0   0.09M  0.3P
+  0.6   4.0M   0.3P
+ ...
+ DATA=SOURCE
+ POINTS=90
+ CBS=1.2P
*  Vbs   Ibs    Cbssw
+ -2.0  -0.095P  0.01P
+  0.0   0.09M   0.015P
+  0.6   4.0M    0.02P
+ ...
[END_DEVICE_DEF]
```

6.2.8.3.6 Data points

Number_of_data_points is the number of sets of parameter values. It shall be matched as the actual number of sets of parameter values in the device model description.

If the number is different from the actual number, the smaller one is effective.

For example, if *number_of_data_points* is smaller than the actual number, *number_of_data_points* sets of parameter values shall be used. If *number_of_data_points* is larger than the actual one, only whole sets of parameter values shall be used.

6.2.8.3.7 **Table data structure** (see Figure 18)

The Device Model shall be described as sets of parameters where current and capacitance are functions of terminal voltages. Terminal voltages are independent variables and current and capacitance are dependent variables. Values of each independent variable shall be selected according to variations of the dependent variables considering data size and accuracy. This specification does not require that independent variables are positioned on a regular grid. But from the simulation point of view, it is desirable that the data is positioned on a regular grid that does not necessarily have constant pitch.

In the case where the data is positioned on a regular grid, "GRID=YES" appears following "POINTS=*Number_of_data_points*". In the case where the data is not positioned on a regular grid, "GRID=NO" appears. The default is "GRID=YES".

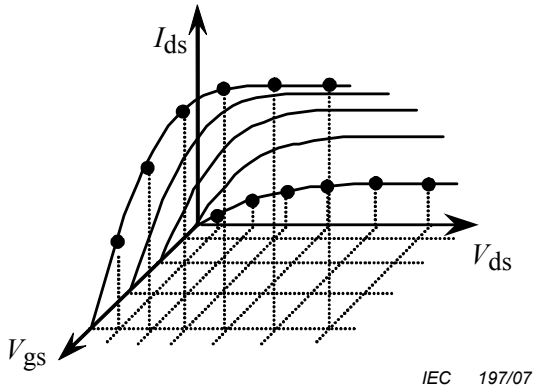


Figure 18 – NMOS characteristics on regular grid

6.2.8.3.8 MOS Transistor model with two-terminal switch (see Figure 19)

The DC characteristics of a MOS transistor model with a two-terminal switch can be considered to be the DC characteristics of *Vgs* and *Vbs* of the four-terminal model for a special case. Therefore, it is considered to be the characteristic of a four-terminal MOS model for the case of a fixed set of values for *Vgs* and *Vbs*. As a result, the model can be described as a one-dimensional model with only *Vds*. This table can easily represent the DC characteristics of IBIS 3.2 data (IEC 62014-1).

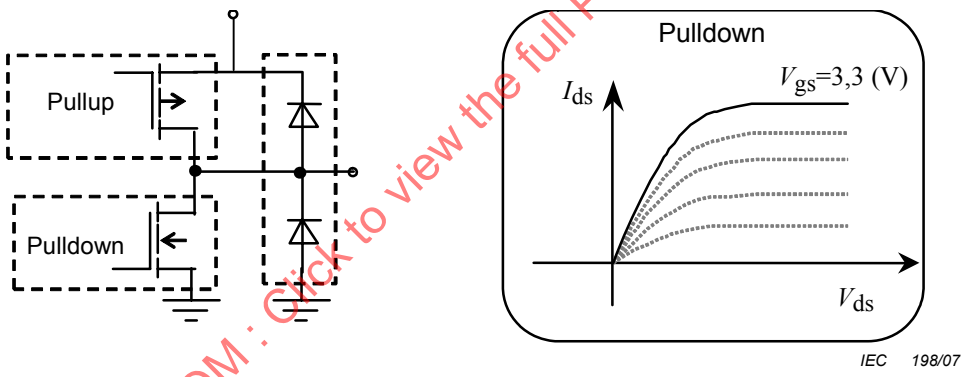


Figure 19 – MOS transistor model with two-terminal model

Example

```
MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=90
+ VGS=3.3 VBS=0
*  Vds   Ids   Cgs   Cgd  Cgb
+ 0.095 2.0M  0.5N  0.5N 3.5N
+ 0.095 2.1M  0.7N  0.5N 4.0N
+ 2.1   2.0M  0.5N  0.5N 3.5N
+ 4.0   2.1M  0.7N  0.5N 4.0N
+ ...
```

6.2.8.3.9 Dependency of L and W on characteristics of MOS transistor

The dependency of channel length L and channel width W on characteristics of a MOS transistor can be calculated by using the ratio of W/L.

The characteristics of the following MOS transistor can be calculated below.

Mxxxxxxx node1 node2 node3 node4 modelname L=Lr W=Wr

The drain current Ids' can be calculated by using the following equation with parameters L=Ld, W=Wd and Ids which are defined by .MODEL in [DEVICE_DEF], and L=Lr and W=Wr of the transistor descriptions which are defined by [CONNECTION].

$$I_{ds}' = I_{ds} * \frac{W_r}{W_d} * \frac{L_d}{L_r}$$

The gate-source capacitance Cgs', the gate-drain capacitance Cgd' and the gate-bulk capacitance Cgb' can be calculated by using the following equations.

$$C_{gs}' = C_{gs} * \frac{W_r}{W_d} * \frac{L_r}{L_d}$$

$$C_{gd}' = C_{gd} * \frac{W_r}{W_d} * \frac{L_r}{L_d}$$

$$C_{gb}' = C_{gb} * \frac{W_r}{W_d} * \frac{L_r}{L_d}$$

6.2.8.3.10 Dependency of AD and AS on diode characteristics of MOS transistor

The dependency of AD and AS on the characteristics of diodes in a MOS transistor can be calculated by using the ratio of AD or AS described in the circuit description, and that described in the device model.

The characteristics of the following MOS transistor can be calculated as shown below.

Mxxxxxxx node1 node2 node3 node4 modelname L=Lr W=Wr AD=ADr AS=ASr
+ PD=PDr PS=PSr

The bulk-drain diode current value Ibd' can be calculated by using the following equation with the parameters AD=ADd and Ibd which are defined by .MODEL in [DEVICE_DEF], and AD=ADr of the transistor descriptions which are defined by [CONNECTION].

$$I_{bd}' = I_{bd} * \frac{AD_r}{AD_d}$$

The bulk-source diode current value Ibs' can be calculated by using the following equation with the parameters AS=ASd and Ibs which are defined by .MODEL in [DEVICE_DEF], and AS=ASr of the transistor descriptions which are defined by [CONNECTION].

$$I_{bs}' = I_{bs} * \frac{AS_r}{AS_d}$$

The bulk-source diode capacitance Cbs' can be calculated by using the following equation with the parameters AS=ASd, PS=PSd, Cbs and $Cbssw$ which are defined by .MODEL in [DEVICE_DEF], and AS=ASr and PS=PSr of the transistor descriptions which are defined by [CONNECTION].

$$Cbs' = Cbs * \frac{ASr}{ASd} + Cbssw * \frac{PSr}{PSd}$$

The bulk- drain diode capacitance Cbd' can be calculated by using the following equation with the parameters AD=ADd, PD=PDd, Cbd and $Cbdsw$ which are defined by .MODEL in [DEVICE_DEF], and AD=ADr and PD=PDr of the transistor descriptions which are defined by [CONNECTION].

$$Cbd' = Cbd * \frac{ADr}{ADd} + Cbdsw * \frac{PDr}{PDd}$$

6.2.8.3.11 Junction resistance of MOS transistor

The junction resistance of MOS transistor of the following MOS transistor can be calculated as shown below.

Mxxxxxxx node1 node2 node3 node4 modelname L=Lr W=Wr NRD=NRD NRS=NRS

RD, RS can be calculated by using the following equation with the parameters RSH=RSH which is defined by .MODEL in [DEVICE_DEF], and NRD=NRD and NRS=NRS of the transistor descriptions which are defined by [CONNECTION].

RD = NRD x RSH

RS = NRS x RSH

NOTE The device characteristics defined by [FAST], [TYP], and [SLOW] correspond to those of the input stimulus.

Thus, a simulation for [TYP] stimulus shall use the corresponding [TYP] non-linear characteristics of the device.

6.2.9 Package model reference

6.2.9.1 Description

[COMPONENT]

6.2.9.2 Explanation

The file name and type of the package model for reference shall be assigned.

Parameters shall be described after [COMPONENT].

This keyword has three parameters on one line as package file name, package type name, and model name to be used.

The assigned package type and model name shall be described on the header of the package model.

6.2.9.3 Example

[COMPONENT]

*FILE_NAME PKG_NAME MODEL_NAME

PACKAGEA.PKG PACKAGE1 MODEL1

6.3 Package model file

6.3.1 File name

6.3.1.1 General

The name of the model file starts with any alphabetical or numerical characters, with .PKG as an extension.

6.3.1.2 Example

TSSOP48.PKG

NOTE The limitation of file name length (number of characters) depends on operating system.

6.3.2 Start and end of model description

6.3.2.1 General

One Model description shall be provided per package model.

6.3.2.2 Start of package model description

6.3.2.2.1 Description

[PACKAGE]

6.3.2.2.2 Explanation

The contents of the model follow this keyword.

6.3.2.3 End of package model description

6.3.2.3.1 Description

[END_PACKAGE]

6.3.2.3.2 Explanation

The description of the package model will be terminated by this keyword.

6.3.3 Header

6.3.3.1 Package type

6.3.3.1.1 Description

[NAME] arbitrary text

6.3.3.1.2 Explanation

This indicates the package type identifier, which includes Product Number and/or Name.

This is used by simulators to assign the correct model for a package in a design.

6.3.3.1.3 Example

[NAME] TSSOP48

6.3.3.2 Model version

6.3.3.2.1 Description

[IMIC_VER] arbitrary text

6.3.3.2.2 Explanation

The version number of the IMIC specification shall be described. Currently only version 1.3 is available. Parsers shall follow the appropriate syntax rules for the entire package model.

6.3.3.2.3 Example

[IMIC_VER] 1.3

6.3.3.3 Model level

6.3.3.3.1 Description

[LEVEL] Integer

6.3.3.3.2 Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise;

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise;

Level 3: EMI (Electromagnetic Interference) model for the analysis of conducted electromagnetic emission noise. This level is not available in this version.

6.3.3.3.3 Example

[LEVEL] 2

6.3.3.4 Model index

6.3.3.4.1 Description

[MODEL_INDEX]

6.3.3.4.2 Explanation

Package models shall be listed here. The package model name, upper frequency limit, and chip size in a line after [MODEL_INDEX]. Several lines of [MODEL_INDEX] entries are allowed. Frequency and chip size will be used to indicate the validity of the model for a particular usage or analysis. The parameters of frequency and chip size are optional.

6.3.3.4.3 Example

[MODEL_INDEX]

* MODELNAME FREQUENCY CHIPSIZE

MODEL1 50MHZ 10MM2

MODEL2 200MHZ 10MM2

6.3.3.5 Date

6.3.3.5.1 Description

[DATE] date

6.3.3.5.2 Explanation

The model release date is described using any of the following formats.

– Day / Month name / Year Example: 23MAR98
– Month name Day, Year Example: MARCH 3, 1998

6.3.3.5.3 Example

[DATE] 23MAR98

6.3.3.6 Explanation of model

6.3.3.6.1 Description

[NOTES]

Arbitrary notes concerning the model shall be described if appropriate. This may be used for explanations of the origin, usage, and testing of the model, for example.

6.3.3.6.2 Explanation

Any comments may appear in the lines following the keyword [NOTES].

The distance from surface of printed circuit board to reference ground shall be described. 0,0 mm, 0,152 mm and 1,588 mm are recommended as the distance if applicable.

6.3.3.6.3 Example

[NOTES]
TSOP 3 PIN PACKAGE ELECTRICAL CHARCTERISTICS MODEL
FOR ALVCH LCR3_SELF MODEL EXCLUDE MUTUAL ELEMENTS
HEIGHT TO REFERENCE GROUND IS 0.152 mm.

6.3.3.7 Copyright

6.3.3.7.1 Description

[COPYRIGHT] arbitrary text

6.3.3.7.2 Explanation

Copyright holder and related terms are stated.

6.3.3.7.3 Example

[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED

6.3.3.8 Manufacture

6.3.3.8.1 Description

[MANUFACTURER] arbitrary text

6.3.3.8.2 Explanation

The package manufacturer is declared here.

6.3.3.8.3 Example

[MANUFACTURER] ZYX CORP.

6.3.4 Model name

6.3.4.1 Description

[MODEL_NAME] arbitrary text

6.3.4.2 Explanation

This defines the model name which is used at [MODEL_INDEX] and/or [COMPONENT] of the IC model file.

6.3.4.3 Example

[MODEL_NAME] MODEL1

6.3.5 Terminals

6.3.5.1 **Inner terminals** (see Figure 20)

6.3.5.1.1 General

This defines the connections between the inner terminals and the equivalent circuits of package.

6.3.5.1.2 Description

[INNER_TERMINAL]

6.3.5.1.3 Explanation

This defines the connections between the inner terminals and the equivalent circuits of package.

Each line shall have only one inner terminal reference. The first parameter is inner terminal name. The second parameter is connected signal name of the equivalent circuit of the package.

6.3.5.1.4 Example

[INNER_TERMINAL]
LEAD1 NODE1
LEAD2 NODE2

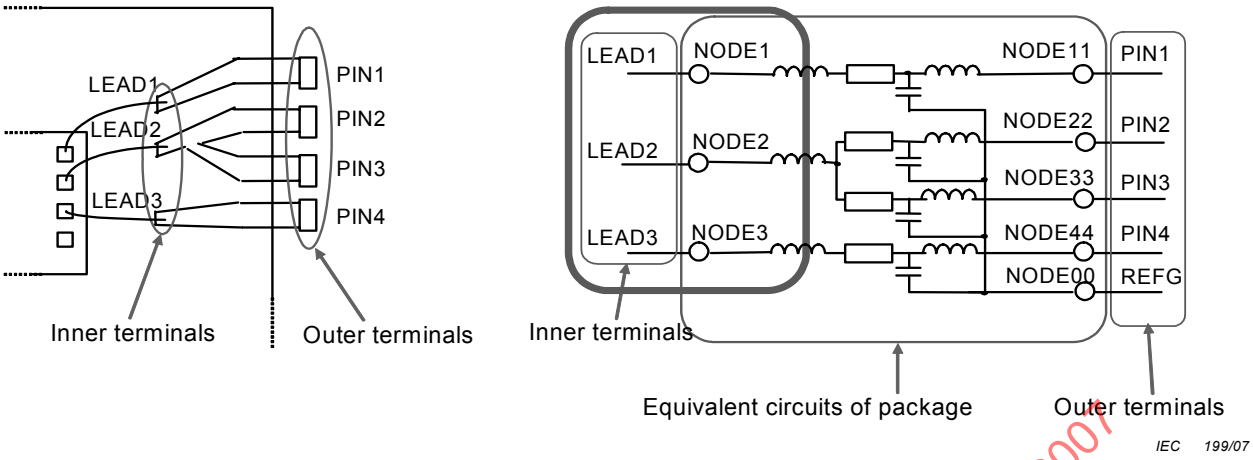


Figure 20 – Relationship between inner terminals and equivalent circuits of package

6.3.5.2 Outer terminals (see Figure 21)

6.3.5.2.1 General

This defines the connections between the outer terminals and the equivalent circuits of package.

6.3.5.2.2 Description

[OUTER_TERMINAL]

6.3.5.2.3 Explanation

This defines the connections between the outer terminals and the equivalent circuits of the package, and the relationship between reference ground and the equivalent circuits of the package. Each line shall have only one outer terminal reference. The first parameter is outer terminal name. The second parameter is the signal name of the equivalent circuit of the package, to which the outer terminal is connected.

The name of the reference ground terminal is "REFG". The reference ground is defined as a reference plane when electrical parameters of package are measured and/or simulated. The reference ground terminal has to be connected to the reference ground plane of printed circuit board.

Reference ground plane of printed circuit board can be excluded for EM extraction if interposer has reference plane inside. Then the reference plane inside the interposer that is "REFG" can be or cannot be connected to the reference plane in printed circuit board according to actual usage.

Reference plane of printed circuit board should be included for EM extraction if interposer contains no reference plane.

6.3.5.2.4 Example

[OUTER_TERMINAL]

PIN1 NODE11

PIN2 NODE22

...

REFG NODE00

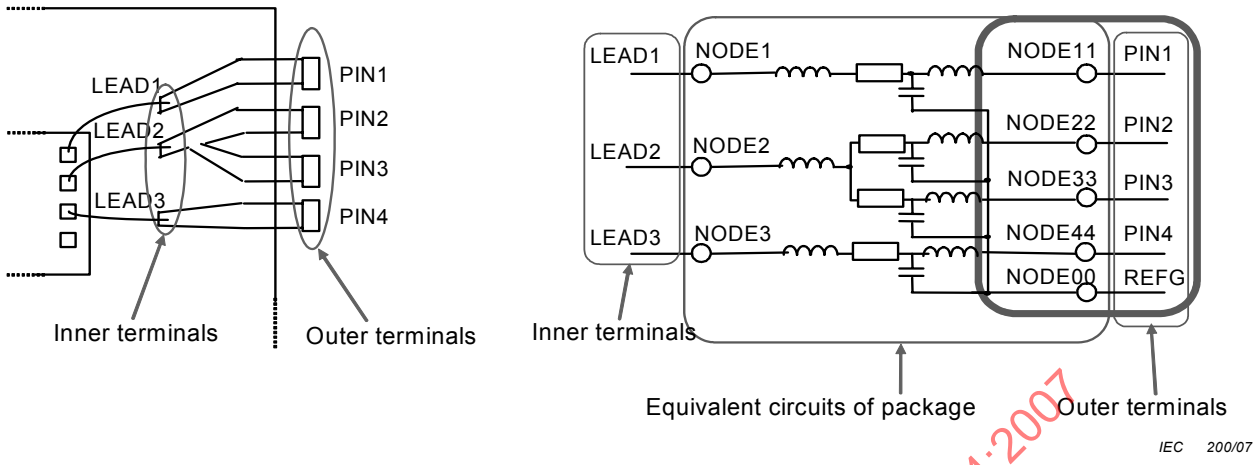


Figure 21 – Relationship between outer terminals and equivalent circuits of package

6.3.6 Circuit description

6.3.6.1 General

The elements of internal circuits and their interconnections shall be described.

6.3.6.2 Description

[CONNECTION]

[FAST]

[TYP]

[SLOW]

[END_CONNECTION]

6.3.6.3 Explanation

This defines the internal circuits of the package and wire bonding connections.

The format of the circuit description of the package follows the format of the IC model file.

NOTE The size of the package description may be huge due to coupling etc. If the package has symmetrical structures, the size of the model can be drastically reduced by defining the subcircuit for one portion, and then reference that subcircuit in the other portions. For example, a one-fourth model of the package or a hierarchical subcircuit of the package may reduce the size of model.

6.3.6.4 Example

Example for a one-fourth model is as follows.

[CONNECTION]

SUBCKT PKG IN1 IN2 IN3 IN4 IN5 IN6 IN7 IN8 IN9 IN10 IN11 IN12

+ OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10

+ OUT11 OUT12

+ IN24 IN23 IN22 IN21 IN20 IN19 IN18 IN17 IN16 IN15 IN14 IN13

+ OUT24 OUT23 OUT22 OUT21 OUT20 OUT19 OUT18 OUT17

+ OUT16 OUT15 OUT14 OUT13

+ IN25 IN26 IN27 IN28 IN29 IN30 IN31 IN32 IN33 IN34 IN35 IN36

+ OUT25 OUT26 OUT27 OUT28 OUT29 OUT30 OUT31 OUT32

```
+ OUT33 OUT34 OUT35 OUT36
+ IN48 IN47 IN46 IN45 IN44 IN43 IN42 IN41 IN40 IN39 IN38 IN37
+ OUT48 OUT47 OUT46 OUT45 OUT44 OUT43 OUT42 OUT41
+ OUT40 OUT39 OUT38 OUT37
+ REFG
XPKG_01
+ IN1 IN2 IN3 IN4 IN5 IN6 IN7 IN8 IN9 IN10 IN11 IN12
+ OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10
+ OUT11 OUT12  REFG  LCR
XPKG_02
+ IN24 IN23 IN22 IN21 IN20 IN19 IN18 IN17 IN16 IN15 IN14 IN13
+ OUT24 OUT23 OUT22 OUT21 OUT20 OUT19 OUT18 OUT17
+ OUT16 OUT15 OUT14 OUT13 REFG  LCR
XPKG_03
+ IN25 IN26 IN27 IN28 IN29 IN30 IN31 IN32 IN33 IN34 IN35 IN36
+ OUT25 OUT26 OUT27 OUT28 OUT29 OUT30 OUT31 OUT32
+ OUT33 OUT34 OUT35 OUT36 REFG  LCR
XPKG_04
+ IN48 IN47 IN46 IN45 IN44 IN43 IN42 IN41 IN40 IN39 IN38 IN37
+ OUT48 OUT47 OUT46 OUT45 OUT44 OUT43 OUT42 OUT41
+ OUT40 OUT39 OUT38 OUT37 REFG  LCR
ENDS PKG
SUBCKT LCR
+ 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
C000 26 25 3.08467E-13
C001 27 25 1.54055E-13
C002 28 25 1.18045E-13
C003 29 25 1.04291E-13
C004 30 25 1.0002E-13
C005 31 25 9.81234E-14
C006 32 25 9.24553E-14
C007 33 25 9.26352E-14
.......
......
R00m 36 61 0.000624821
L00b 12 50 5.1212E-10
L00n 24 62 5.1212E-10
R00b 37 50 0.000643131
R00n 37 62 0.000643131
ENDS LCR
[END_CONNECTION]
```

6.3.7 Device model

6.3.7.1 General

One-dimensional, two-dimensional or three-dimensional data of the characteristics of non-linear devices shall be described. Non-linear devices are those such as transistor, diode, voltage dependent capacitor and so on.

6.3.7.2 Description

[DEVICE_DEF]

[FAST]

[TYP]

[SLOW]

[END_DEVICE_DEF]

6.3.7.3 Explanation

This defines a device model to be used in the definition of the package.

The definition of device model shall be terminated with [END_DEVICE_DEF].

The format of the device model description of the package shall follow the same format as the IC model file.

6.3.8 Structures

The materials, positions, 3D-structures etc. of package shall be described if appropriate.

This is the future work item in this specification.

6.4 Module model file

6.4.1 File name

The name of the model file starts with any alphabetical or numerical characters, with .MDL as an extension.

6.4.1.1 Example

DIMM32MB.MDL

NOTE The limitation of file name length (number of characters) depends on operating system.

6.4.2 Start and end of model description

6.4.2.1 General

One Model description shall be provided as one module model.

6.4.2.2 Start of module model description

6.4.2.2.1 Description

[MODULE]

6.4.2.2.2 Explanation

The contents of the model follow this keyword.

6.4.2.3 End of module model description

6.4.2.3.1 Description

[END_MODULE]

6.4.2.3.2 Explanation

The description of the module model shall be terminated with this keyword.

6.4.3 Header

6.4.3.1 Module type

6.4.3.1.1 Description

[NAME] arbitrary text

6.4.3.1.2 Explanation

This indicates the module type identifier, which includes Product Number and/or Name.

This is used by simulators to locate the correct model for a module in a design.

6.4.3.1.3 Example

[NAME] DIMM32MB

6.4.3.2 Model version

6.4.3.2.1 Description

[IMIC_VER] arbitrary text

6.4.3.2.2 Explanation

The version number of the IMIC specification shall be described. Currently, only version 1.3 is available. Parsers shall follow the appropriate syntax rules for the entire module model.

6.4.3.2.3 Example

[IMIC_VER] 1.3

6.4.3.3 Model level

6.4.3.3.1 Description

[LEVEL] Integer

6.4.3.3.2 Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise;

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise;

Level 3: EMI (Electromagnetic Interference) model for the analysis of conducted electromagnetic emission noise. This level is not available in this version.

6.4.3.3.3 Example

[LEVEL] 2

6.4.3.4 Date

6.4.3.4.1 Description

[DATE] date

6.4.3.4.2 Explanation

The model release date is described using any of the following formats.

– Day / Month name / Year Example: 23MAR98
– Month name Day, Year Example: MARCH 23, 1998

6.4.3.4.3 Example

[DATE] 23MAR98

6.4.3.5 Explanation of model

6.4.3.5.1 Description

[NOTES]

Arbitrary notes concerning the model shall be described if appropriate. This may be used for explanations of the origin, usage, and testing of the model, for example.

6.4.3.5.2 Explanation

Any comments may appear on the lines following [NOTES].

6.4.3.5.3 Example

[NOTES]
MEMORY MODULE MODEL FOR 3.3V DDR x72 128MB DIMM

6.4.3.6 Copyright

6.4.3.6.1 Description

[COPYRIGHT] arbitrary text

6.4.3.6.2 Explanation

Copyright holder and related terms are stated.

6.4.3.6.3 Example

[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED

6.4.3.7 Manufacturer

6.4.3.7.1 Description

[MANUFACTURER] arbitrary text

6.4.3.7.2 Explanation

Manufacturer is declared here.

6.4.3.7.3 Example

[MANUFACTURER] ZYX CORP.

6.4.4 Terminals

6.4.4.1 General

The external terminals of the module shall be described. The external terminals are the equivalent of the module pins.

6.4.4.2 Description

[TERMINAL]

6.4.4.2.1 Explanation

This defines the external terminals of module. Description shall be started with the next line of keyword [TERMINAL].

The signal names of the external terminals of module shall be described. The keyword ".SUBCKT" is followed by the name of the module and the signal names of external terminals.

6.4.4.3 Example

[TERMINAL]

SUBCKT DIMM32MB SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG

6.4.5 Circuit description (see Figure 22)

6.4.5.1 General

The elements of the internal circuit and their interconnection shall be described.

The elements are ICs, modules and other elements including elements for interconnections on the module.

6.4.5.2 Description

[CONNECTION]

[FAST]

[TYP]

[SLOW]

[END_CONNECTION]

6.4.5.3 Explanation

This defines the elements of the internal circuits and their interconnection.

The format of the circuit description of module follows the format of the IC model file.

6.4.5.4 Example

[CONNECTION]

[TYP]

SUBCKT MODULE_TOP OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7
XLSI-A LAA LAB LAC LAD LAE LAF … LSI-A
XLSI-B LBA LBB LBC LBD LBE LBF … LSI-B
XLSI-C LCA LCB LCC LCD LCE LCF … LSI-C
XMODULE-A MAA MAB MAC MAD MAE MAF MAG MODULE-A
T1 LAA OUT1 Z0=2.3
T2 MAC OUT2 Z0=5.3
T3 LBA OUT3 Z0=1.3
T4 LBF OUT7 Z0=3.1
T5 LBF OUT7 Z0=2.1
…
[END_CONNECTION]

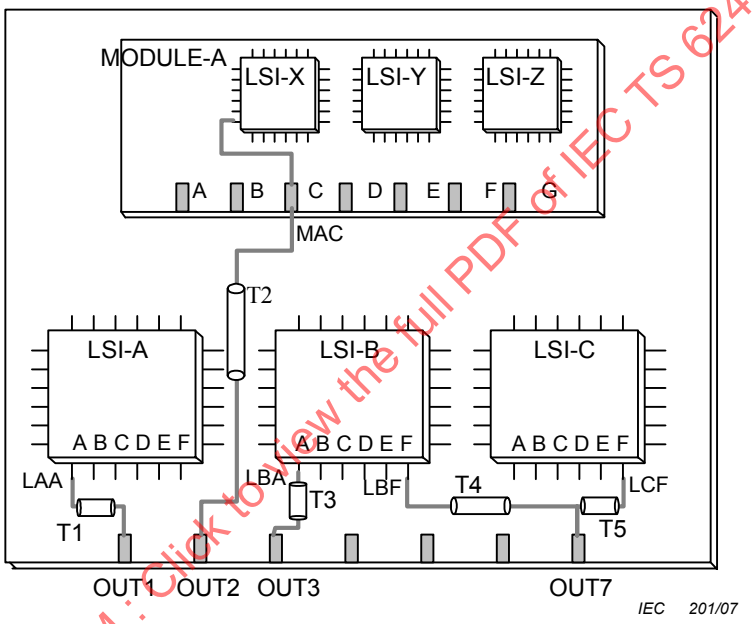


Figure 22 – Example of module circuit

6.4.6 Signal source (see Figure 23)

6.4.6.1 General

This defines the output terminals of ICs or modules on the module from which signal source stimuli are described to generate the desired waveforms at the output terminals of the module.

6.4.6.2 Description

[SIGNAL_SOURCE] Output terminal name

[SOURCE_DEF]

6.4.6.3 Explanation

The output terminal names of the module defined next to [SIGNAL_SOURCE] shall match the corresponding signal names defined as the external terminals of the module in the [TERMINAL].SUBCKT statement.

The [SIGNAL_SOURCE] section contains one [SOURCE_DEF] subsection, specifying ICs or modules on the module and their output terminals.

[SOURCE_DEF]

The signal sources for the output terminal of the module are defined by two parameters.

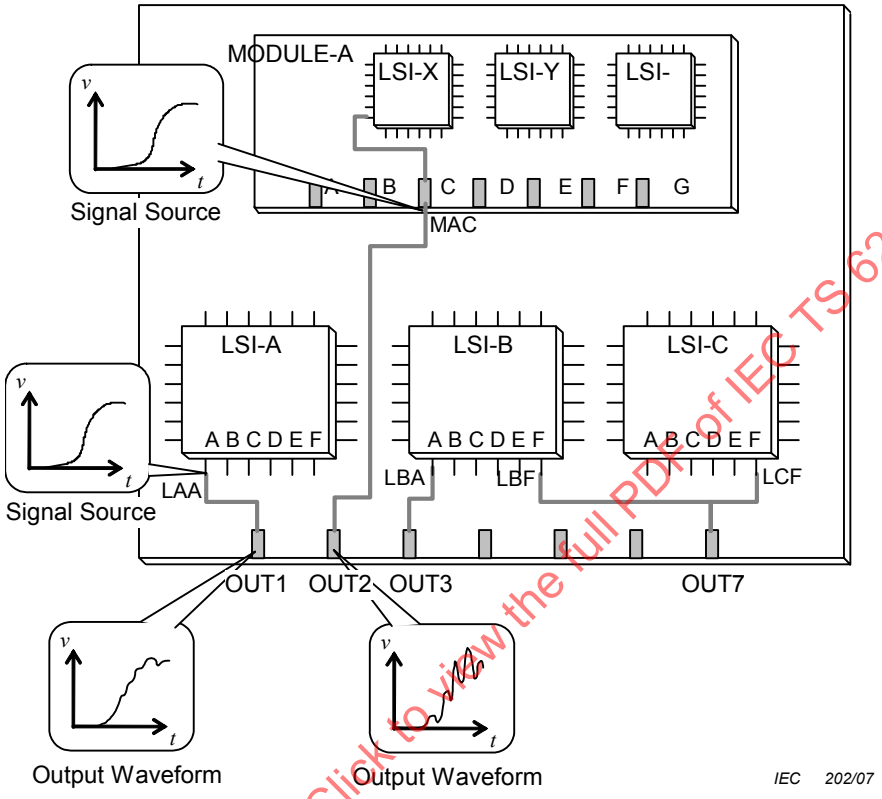
The first parameter is a subcircuit instance name for the IC or the module that provides the desired signal source stimulus. This instance name shall be defined in the [CONNECTION] section.

The second parameter is the external terminal name of the IC or the module defined by the first parameter. The external terminal name shall match one of the external terminals defined in the [CONNECTION] section.

These two parameters shall be described on one line.

6.4.6.4 Example

[SIGNAL_SOURCE] OUT1
[SOURCE_DEF]
XLSI-A LAA
[SIGNAL_SOURCE] OUT2
[SOURCE_DEF]
XMODULE-A MAC
[SIGNAL_SOURCE] OUT3
[SOURCE_DEF]
XLSI-B LBA
[SIGNAL_SOURCE] OUT7
[SOURCE_DEF]
XLSI-B LBF
XLSI-C LCF



NOTE 1 The signal source for output terminal “OUT1” of the module is terminal “LAA” of “LSI-A”.

NOTE 2 The signal source for output terminal “OUT2” of the module is terminal “MAC” of “MODULE-A”.

Figure 23 – Example of signal source of module

6.4.7 Device model

6.4.7.1 General

One-dimensional, two-dimensional or three-dimensional data of the characteristics of non-linear devices shall be described. Non-linear devices are those such as transistors, diodes, voltage dependent capacitors and so on.

6.4.7.2 Description

[DEVICE_DEF]

[FAST]

[TYP]

[SLOW]

[END_DEVICE_DEF]

6.4.7.3 Explanation

This defines the device models to be used in the definition of the module.

The definition of the device model shall be terminated with [END_DEVICE_DEF].

The format of the device model description of the module board shall follow the same format as the IC model file.

6.4.8 Module model reference

6.4.8.1 General

The relationships between the ICs and the module shall be described.

6.4.8.2 Description

[COMPONENT]

6.4.8.3 Explanation

This describes the file and the type names of the IC models to be referenced. It also describes the file and the type names of the module models to be referenced.

Parameters shall be described after the keyword [COMPONENT].

The first parameter is the file name of the IC model or module model. The second parameter is the model type of the IC model or module model.

These two parameters shall be described on one line.

The assigned IC type name and module type name shall be described on the header of IC model file and module model file, respectively.

6.4.8.4 Example

[COMPONENT]
*FILE_NAME IC_NAME
ALVCH16244.IMC ALVCH16244
DRAM16MX16.MDL DRAM16MX16

6.4.9 Structures

The materials, positions, 3D-structures etc. of package shall be described if appropriate.

This is the future work item in this specification.

7 Levels of models

The level of the models shall be set according to the purpose of the simulation. The purpose of simulation and the elements of model which are correspondent to level of models are described in Table 2 and Table 3 respectively.

Table 2 – Levels of models

Level	Object	Simulation
1	Signal Integrity (SI)	To analyze signal waveform. - Light load to simulator
2	Power Integrity (PI)	To analyze power/ground bounce. - Large size of circuits containing many parasitic LCRs - Heavy load to simulator
3	EMI	To analyze conducted electromagnetic emissions. (This level is not available in this version)

Table 3 – Required elements of model for each level

File	Item	Level 1	Level 2	Level 3
IC model	Header	Yes	Yes	Yes
	External terminals	Yes	Yes	Yes
	Pad assignment	Yes	Yes	Yes
	Circuit description Signal	Yes	Yes	Yes
	Power	No	Yes	Yes
	Input stimulus assignment	Yes	Yes	Yes
	Input stimulus	Yes	Yes	Yes
	Device model	Yes	Yes	Yes
	Package model reference	Yes	Yes	Yes
Package model	Header	Yes	Yes	Yes
	Model name	Yes	Yes	Yes
	Inner terminals	Yes	Yes	Yes
	Outer terminals	Yes	Yes	Yes
	Circuit description	Yes	Yes	Yes
	Device model	No	Yes	Yes
	Structures	No	No	Yes
Module model	Header	Yes	Yes	Yes
	External terminals	Yes	Yes	Yes
	Circuit description	Yes	Yes	Yes
	Signal source	Yes	Yes	Yes
	Device model	Yes	Yes	Yes
	IC/Module reference	Yes	Yes	Yes
	Structures	No	No	Yes