IEC TR 63037

Edition 2.0 2019-06
REDLINE VERSION

TECHNICAL REPORT

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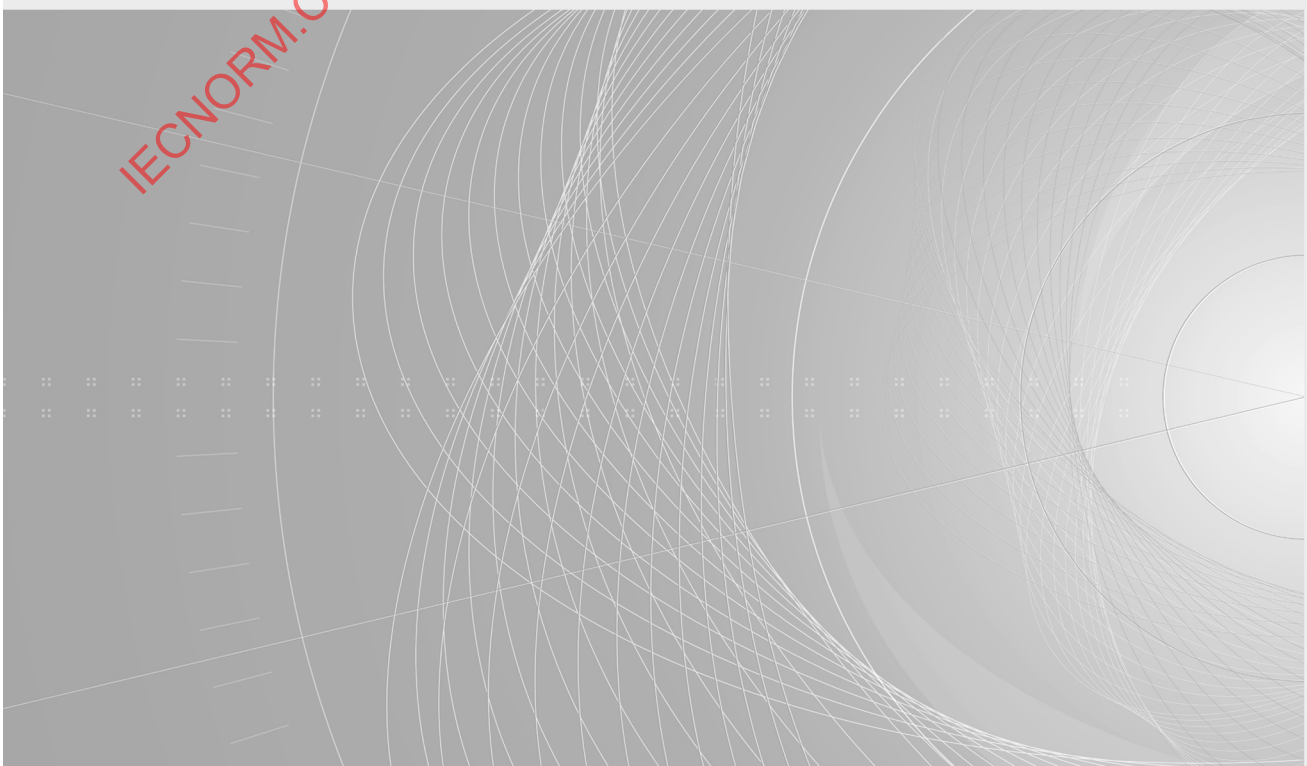
Electrical interface specifications for self ballasted lamps and controlgear in phase-cut dimmed lighting systems



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CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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ELECTRICAL INTERFACE SPECIFICATIONS FOR SELF BALLASTED LAMPS AND CONTROLGEAR IN PHASE-CUT DIMMED LIGHTING SYSTEMS

FOREWORD

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The main task of IEC technical committees is to prepare International Standards. However, a technical committee may propose the publication of a Technical Report when it has collected data of a different kind from that which is normally published as an International Standard, for example "state of the art".

IEC TR 63037, which is a Technical Report, has been prepared by IEC technical committee 34: Lamps and related equipment.

This second edition cancels and replaces the first edition published in 2016. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) emission of audible noise;
b) ghosting caused by issues that are not related to the power supply of the dimmer or synchronization;
c) stability of phase angle waveform (for the dimmer), including symmetry and stability tests;
d) flicker of light loads;
e) repetitive ring up voltage;
f) dimming range; and
g) number of switching cycles have been added.

The text of this Technical Report is based on the following documents:

Draft TR	Report on voting
34/517/DTR	34/583A/RVDTR

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

IMPORTANT – The "colour inside" logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this publication using a colour printer.

INTRODUCTION

This document describes the technical requirements for self-ballasted lamps and controlgear to work with phase-cut dimmers. For a complete picture of the technical requirements the user should also refer to IEC TR 63036 (see also IEC 60669-2-1:—,[1] Annex EE), the companion document that contains technical requirements and testing methods for phase-cut dimmers.

[1] Under preparation. Stage at the time of publication IEC AFDIS 60669-2-1:2019.

ELECTRICAL INTERFACE SPECIFICATIONS FOR SELF BALLASTED LAMPS AND CONTROLGEAR IN PHASE-CUT DIMMED LIGHTING SYSTEMS

1 Scope

~~This document specifies the electrical interface between phase-cut dimming equipment and lighting equipment, such as LED integrated lamps and light sources with external controlgear, with the intention of helping designers of both types of equipment to develop products that will work together properly.~~

~~This document describes both the dimming phase and the off phase. In addition to the specification of the interface, test procedures are given for testing the proper operation.~~

~~It may be expected that controlgear fulfilling the requirements of this document are also suited to be used with electronic switches that use a circuitry comparable with that of a phase-cut dimmer, but do not contain means for the adjustability of the phase-cut angle.~~

This document provides guidance to controlgear/integrated lamp designers for the development of products suitable to operate with future phase-cut dimmers. It describes the possible voltage signals and the expected response of the controlgear/integrated lamps.

This document describes the expected response of controlgear during all operation states of a phase-cut lighting system and provides a complete understanding of the requirements for phase-cut dimmers. The response of a phase-cut dimmer is described in IEC 60669-2-1:—, Annex EE.

This document specifies the system performance aspects and test procedures for the control by mains voltage phase-cut dimming of the brightness of mains operated electronic lighting equipment intended to be controlled by mains voltage phase-cut dimmers, such as LED integrated lamps and light sources with external controlgear.

Safety requirements are not covered by this document, but by respective product standards.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-845, *International Electrotechnical Vocabulary – Part 845: Lighting* (available at http://www.electropedia.org)

IEC 62504, *General lighting – Light emitting diode (LED) products and related equipment – Terms and definitions*

3 Terms, definitions, abbreviated terms and symbols

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-845 and IEC 62504 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
phase-cut dimmed lighting system
lighting system
combination of a phase-cut dimmer and one or more controlgear and light sources

Note 1 to entry: The term “lighting system” used in this document is an abbreviated form of "phase-cut dimmed lighting system".

3.1.2
off-state
state of a ~~phase-cut dimming~~ lighting system when no light is emitted

3.1.3
on-state
state of a ~~phase-cut dimming~~ lighting system when light is emitted

3.1.4
electrical interface
electrical parameters for supplying power and making exchange of information between the phase-cut dimmer and controlgear

3.1.5
phase-cut dimmer
dimmer
electronic switch connected in series with a load, that changes the supply voltage waveform applied to the load from the ~~pure~~ mains voltage waveform to a leading edge (forward phase) or a trailing edge (reverse phase) AC voltage waveform ~~or is capable of switching between both waveforms~~

Note 1 to entry: Some phase-cut dimmers are capable of switching their output between leading edge and trailing edge waveforms.

Note 2 to entry: The output voltage waveform of a phase-cut dimmer is applied to one or more loads. The conduction angle of the voltage waveform is adjustable.

Note 3 to entry: Within this document, where the term “dimmer” is used, the term “phase-cut dimmer” is meant.

3.1.6
two-wire phase-cut dimmer
phase-cut dimmer connected in series with a load that has no connection to neutral

3.1.7
three-wire phase-cut dimmer
phase-cut dimmer connected in series with a load that has ~~in addition~~ an additional connection to neutral

3.1.8
controlgear
~~device~~ one or more components between the ~~phase-cut dimmer~~ supply and one or more lamps which may serve to transform the ~~AC mains power~~ supply voltage, limit the current of the lamp(s) to the required value, provide starting voltage and preheating current, prevent cold starting, correct power factor or reduce radio interference

Note 1 to entry: Lamps may have integrated controlgear such as an integrated LED lamp. Any references to controlgear will include any such integrated lamps.

3.1.9
load side
connection from the output of the phase-cut dimmer to the supply input of one or more controlgear

3.1.10
conducting period
time period during which the phase-cut dimmer supplies power to a controlgear

3.1.11
non-conducting period
time period during which the phase-cut dimmer does not supply power to a controlgear

3.1.12
half-wave
positive or negative 180° of an AC sine wave starting and ending at the zero crossing point

3.1.13
phase angle
position within a half-wave expressed in degree, being in the range of 0° to 180°, referred to the beginning of the half-wave

3.1.14
reference minimum light output
RMLO
light output (luminous flux) produced by a lamp operated by a controlgear that is connected to mains voltage via a phase-cut dimmer set to a conduction angle of 40° ± 1°

3.1.15
maximum light output
MLO
light output (luminous flux) produced by a lamp operated by a controlgear that is directly connected to mains voltage

3.2 Abbreviated terms and symbols

To describe the electrical characteristics of the ~~phase-cut~~ electrical interface, the following ~~abbreviations~~ symbols are used:

~~α_x~~ α	Angle where the test voltage starts rising with the given slew rate SR as shown in Figure A.1. Subscripts L and 1 (see Table 20) refer to leading and end-of-transition, respectively.
~~β_x~~ β	Angle where the test voltage starts falling with the given slew rate SR as shown in Figure A.2. Subscripts T and 1 (see Table 20) refer to trailing and end-of-transition, respectively.
C_f	Filter capacitor to reduce high frequency disturbances
~~EC_CG~~	~~Equivalent circuit that represents a controlgear for phase-cut dimmer testing purposes~~
EC_D	Equivalent circuit that represents a phase-cut dimmer for controlgear testing purposes
I_{CG}	Current through the input terminals of the controlgear (see Figure 1)
I_{CG_pk}	Repetitive peak current of the controlgear in leading edge mode
I_{CG_SL}	Current-carrying capability of the controlgear with $V_{CG} \leq V_{SW}$ in leading edge mode
I_{CG_STH}	Current-carrying capability of the controlgear with $V_{CG} \leq V_{SW}$ in trailing edge mode

I_{CG_STL} Current-carrying capability of the controlgear with $V_{CG} > V_{SW}$ in trailing edge mode

I_D Current through the load side terminal of the phase-cut dimmer (see Figure 1)

I_{D_nc} Maximum current through the phase-cut dimmer during the non-conducting period, limited by the phase-cut dimmer

~~I_{EC_CG} Value of test current of EC_CG in the test circuit in Figure A.1~~

I_{PO} Minimum current carrying capability of the controlgear during the electronic off-state

I_{trans} Current sourced by the phase-cut dimmer during the transition from the conducting to the non-conducting state in trailing edge mode

n Required minimum number of controlgear connected with one phase-cut dimmer (named in phase-cut dimmer installation sheet)

P_{CG} Rated input power of the controlgear (as marked)

~~P_{max} Maximum permissible nominal load of phase-cut dimmer (according to installation sheet)~~

P_{min} Minimum nominal load required by the phase-cut dimmer (according to installation sheet)

~~R_R Resistance value of resistive load R of the test circuit of Figure 5 (according to 8.3.3), dependent on maximum permissible load of phase-cut dimmer P_{max}~~

SR Absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer switches off at time t_{s1} (see Figure 3)

SR_L Absolute value of the slew rate of the increase of the voltage across the input terminals of a controlgear in leading edge dimming mode when the phase-cut dimmer under test switches on (according to Clause 8)

SR_T Absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer under test switches off (according to Clause 8)

t_{HW} Time related to previous zero crossing of the mains to the subsequent zero crossing of the mains (duration of a half-wave)

t_s Time related to previous zero crossing of the mains when leading edge phase-cut dimmer reduces its impedance towards zero by activating its power switch

t_{s1} Time related to previous zero crossing of the mains when the trailing edge phase-cut dimmer increases its impedance towards infinite by deactivating its power switch

t_{s2} Time related to previous zero crossing of the mains when the voltage V_{CG} falls below V_{SW} in trailing edge method

t_{s3} Time related to previous zero crossing of the mains when the transition from the conducting period to the non-conducting period is finished

t_{SW} Time related to previous zero crossing of the mains when voltage V_{CG} crosses V_{SW}

t_t Transition time for trailing edge mode, equals $t_{s2} - t_{s1}$

V_{CG} Voltage across the input terminals of the controlgear (see Figure 1)

V_{CG_PK} Repetitive peak voltage across the terminal of the controlgear

V_D Voltage between the line side (L) and load side terminal of the phase-cut dimmer (see Figure 1)

V_M Mains voltage (rated nominal value)

V_{ME} Phase-cut voltage for testing purposes, sinusoidal part of the waveform ($\alpha 1$ to t_{HW}, 0 to β) equivalent to mains voltage

V_{PO} Lower limit for voltage across the input terminals of the controlgear to provide a current carrying capability I_{PO} during the electronic off-state

V_{SW} Voltage across the input terminals of the controlgear at the time that leads to disabling ($V_M(t) > V_{SW}$) or enabling ($V_M(t) < V_{SW}$), a current path having a current carrying capability of I_{CG_SL} or I_{CG_STH}

V_{test} Value of the test voltage of the test circuit in Figure 6 (according to 8.4)

$xx(t)$ Instantaneous values of current or voltage xx

Z_{CG} Impedance across the input terminals of the controlgear

Z_D Impedance between the line side (L) and the load side terminals of the phase-cut dimmer

Z_{D_max} Maximum impedance between the line side (L) and load side terminal of the phase-cut dimmer, defined by the technical properties of the phase-cut dimmer

Z_{D_min} Minimum impedance between the line side (L) and the load side terminal of the phase-cut dimmer, defined by the power properties of the phase-cut dimmer

4 General description

A phase-cut dimmer either cuts the mains voltage immediately after the zero crossing of the mains (leading edge) or towards the next projected zero crossing of the mains (trailing edge). The functionality of both methods can be implemented in one device (universal dimmers).

This document describes requirements for controlgear during the on-state of a ~~phase-cut dimming~~ lighting system. Specifications are provided dependent on the dimming method for the conducting period, the non-conducting period of the phase-cut dimmer and the transitions between the conducting and non-conducting period.

In addition, this document describes requirements for controlgear during the off-state of a ~~phase-cut dimming~~ lighting system. Specifications are provided independently from the dimming method.

This document addresses the following issues previously reported by consumers and authorities such as:

- emission of audible noise;
- ghosting caused by issues that are not related to the power supply of the dimmer or synchronization;
- stability of phase angle waveform (for the dimmer), including symmetry and stability tests;
- flicker of light loads;
- repetitive ring up voltage;
- dimming range;
- number of switching cycles.

5 General requirements

5.1 Voltage rating

This document applies to one or more of the following mains voltages:

100 V, 120 V, 200 V, 230 V, 277 V, according to IEC 60038.

5.2 Frequency rating

This document applies to one or more of the following mains frequencies:

50 Hz or 60 Hz, according to IEC 60038.

5.3 Marking of controlgear

~~The following information should be provided by the manufacturer on the product or in the accompanying instruction sheets.~~

Controlgear suitable for operating with a phase-cut dimmer, should be marked either on the product or in the product documentation with the following:

DIM

Controlgear and lamps with integrated controlgear should be marked with the reference minimum light output (RMLO) value, or the value should be given in the manufacturer's documentation.

The RMLO value should be in the form "DIM xx %" where xx is the RMLO value.

6 Description of the lighting system and its components

6.1 Wiring method

The wiring of the devices is in accordance with the installation rules given in IEC 60364 (all parts) and also with the national wiring rules applicable in the country where the devices are installed.

6.2 Wiring diagram

The wiring of the lighting system uses the traditional method of connecting the phase-cut dimmer to the mains and to the controlgear. Figure 1 is an example of a lighting system with one phase-cut dimmer and one or two controlgear.

Regarding the connections of the phase-cut dimmer shown in Figure 1, the drawn lines represent a two-wire installation and the dashed line represents the direct connection of the phase-cut dimmer to the mains which is used in three-wire installations.

The direct connection of the phase-cut dimmer to neutral (dashed line in Figure 1) will have consequences on the power supply requirement and synchronization with the phase-cut dimmer.

This document defines requirements that enable compatibility between phase-cut dimmer and controlgear in two-wire installations. However, all predications are also valid for three-wire phase-cut dimmers to ensure proper operation of controlgear.

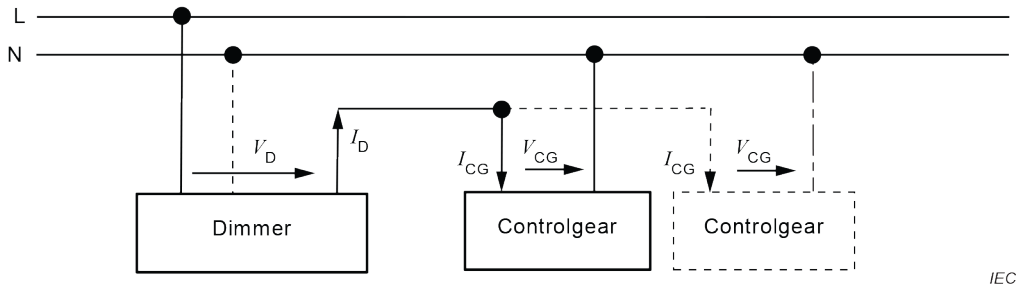


Figure 1 – Example of wiring diagram

7 ~~Electrical~~ Specifications

7.1 General

All information given in this document is related to a half-wave of the mains. Due to the polarity change between subsequent half-waves, all values ~~have to be~~ are regarded as absolute values.

The ~~phase-cut dimming~~ lighting system is either in an on-state or in an off-state. In an on-state, light sources ~~controlled~~ operated by the controlgear ~~being part~~ component of the ~~phase-cut dimming~~ lighting system emit light. In an off-state, light sources ~~controlled~~ operated by the controlgear ~~being part~~ component of the ~~phase-cut dimming~~ lighting system do not emit light.

The off-state may be realized as mechanical off-state by opening the current loop of the ~~phase-cut dimming~~ lighting system with mechanical means, for example a switch. For this case, no requirements need to be fixed.

Alternatively, the off-state may be realized as electronic off-state. In this case, the phase-cut dimmer increases its impedance (i.e. stops producing phase-cut) while continuing its operation, for example to keep its control interface activated. In this case, the connected controlgear are not energized sufficiently to operate a light source, but should provide a current path that allows the phase-cut dimmer to draw current continuously from the mains.

NOTE Applications that provide a connection to neutral allow using a three-wire device, enabling the usage of lamps that do not provide a current carrying capability according to 7.2 and 7.4.

During the on-state and the electronic off-state, it should be ensured that the phase-cut dimmer is supplied sufficiently with power and that the synchronization of the phase-cut dimmer and controlgear with the mains is ensured.

7.2 Electrical characteristics during the on-state of a ~~phase-cut dimming~~ lighting system

7.2.1 General

For the on-state of a ~~phase-cut dimming~~ lighting system, specifications are dependent on the dimming method, leading edge or trailing edge.

Each half-wave is divided into two periods, the conducting period and the non-conducting period of the phase-cut dimmer.

During the conducting period of the phase-cut dimmer, the mains voltage is applied to the controlgear. During the non-conducting period, the voltage between terminals of the phase-cut dimmer is almost equal to the mains voltage ($V_D \approx V_M$).

7.2.2 Electrical characteristics for leading edge dimming method

7.2.2.1 General

Starting from the mains zero crossing, the phase-cut dimmer remains in non-conducting state until its timing element activates the power switch at t_S. Afterwards, the phase-cut dimmer is supplying power to the load for the entire remaining part of the mains half-wave (see Figure 2).

To achieve synchronization with the mains and to control the phase-cut angle correctly, leading edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear has to be able to conduct a current I_{CG_SL}, which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

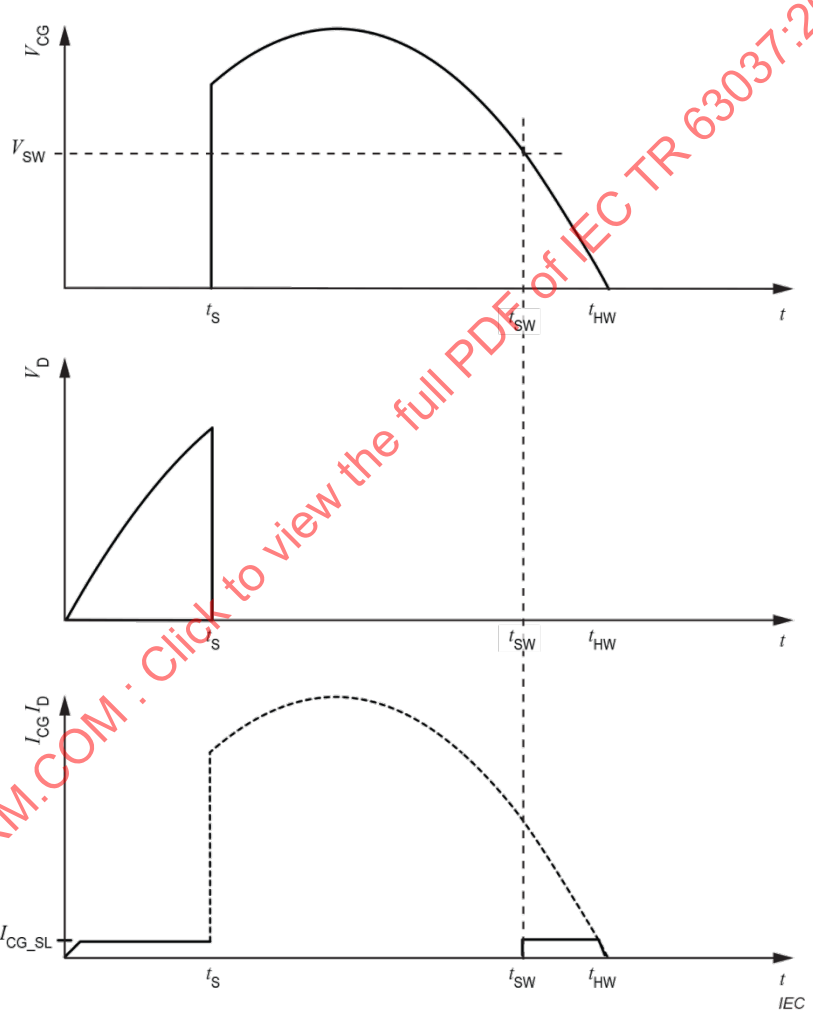


Figure 2 – Timing leading edge dimming method

7.2.2.2 Electrical characteristics during the non-conducting period

During the non-conducting period, the controlgear should comply with the electrical characteristics listed in Tables 1 to 5.

The non-conducting period starts at the zero crossing of the mains and ends at time t_S when the timing element of the phase-cut dimmer activates the power switch.

During this period, the controlgear should provide a current path with a minimum current-carrying capability of I_{CG_SL} as listed in Tables 1 to 5. At small input voltages of the controlgear when I_{CG_SL} cannot be reached due to the characteristics of its input circuitry (e.g. inrush current limiting elements), only its impedance Z_{CG} is defined as listed in Tables 1 to 5.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing an unsteady waveform (leading edge characteristic) for 100 ms.

NOTE This is for reducing power losses in the case where a controlgear is used without a phase-cut dimmer.

Table 1 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 22 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 13,8 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 165,6 mA

Table 2 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 26 V: P_{CG} < 12 W $I_{CG}(t)$ = I_{CG_SL} ≥ 11,5 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 138 mA

Table 3 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 43 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 6,9 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 82,8 mA

Table 4 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 40 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 6 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 72 mA

Table 5 – Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 60 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 5 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 60 mA

7.2.2.3 Electrical characteristics during the transition from the non-conducting to the conducting period

The transition from the non-conducting to the conducting state of the phase-cut dimmer starts at time t_s.

Starting from time t_s, the impedance Z_D of the phase-cut dimmer decreases until its minimum Z_{D_min} is reached. The voltage V_{CG} applied to the controlgear increases towards the instantaneous value $V_M(t)$ of the mains minus the voltage drop across the phase-cut dimmer.

The absolute value of the slew rate of the voltage change of V_D during the transition period does not exceed the values as listed in Table 6 when the phase-cut dimmer is connected to the marked maximum resistive load.

The slew rate should be calculated based on the measurement of the voltage slope of V_D by measuring the time (dt) between V_D = 0,8 · $V_D(t_s)$ and V_D = 0,1 · $V_D(t_s)$ and by calculating the differential voltage dV_D = [0,8 · $V_D(t_s)$] – [0,1 · $V_D(t_s)$].

When the voltage V_{CG} exceeds V_{SW}, the controlgear may deactivate its current carrying capability, thus possibly no current can flow through the controlgear.

NOTE Values of the slew rate represent a compromise between EMC, repetitive peak current in the controlgear and switching losses in the phase-cut dimmer power semiconductors.

Table 6 – Slew rate for voltage decrease across the phase-cut dimmer

V_M [V]	100	120	200	230	277
dV_D/dt [V/µs]	≤ 6,5	≤ 300	≤ 6,5	≤ 6,5	≤ 300

7.2.2.4 Electrical characteristics during the conducting period

During the conducting period, the controlgear should comply with the electrical characteristics listed in Tables 7 to 11.

During this period, full power is applied continuously to the controlgear from the phase-cut dimmer to allow power to be supplied to the controlgear. The values of peak current in Tables 7 to 11 apply at the maximum slew rate values given in Table 6.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the mains voltage.

At time t_{SW}, the input voltage V_{CG} of the controlgear falls below V_{SW}.

From time t_{SW} to the end of the period, the controlgear should provide a current path with a minimum current-carrying capability of I_{CG_SL}.

Table 7 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < 0,111 A/W
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 22 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 8 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < to be defined
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 26 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 9 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < 0,077 25 A/W
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 43 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 10 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < 0,077 25 A/W
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 50 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 11 – Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < to be defined
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 60 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

7.2.3 Electrical characteristics for trailing edge dimming method

7.2.3.1 General

Starting from the mains zero crossing, the phase-cut dimmer operates in conducting state until its timing element deactivates the power switch at time t_{s1}. Afterwards, the phase-cut dimmer is not significantly supplying power to the load for the entire remaining part of the mains half-wave (see Figure 3).

To achieve synchronization with the mains and to control the phase-cut angle correctly, trailing edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear has to be able to conduct a current I_{CG_STH}, which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

Since the negative voltage slope that is triggered by the switch-off of the power switch of the phase-cut dimmer is not only determined by the current I_{CG_STL} that is conducted by the controlgear, but also by the effective capacitance of the wiring and the capacitance being effective in parallel to the phase-cut dimmer, the sum of these capacitances has to be considered.

This document and all listed values are based on systems having a maximum capacitance of the wiring of 10 nF being effective in parallel to the controlgear.

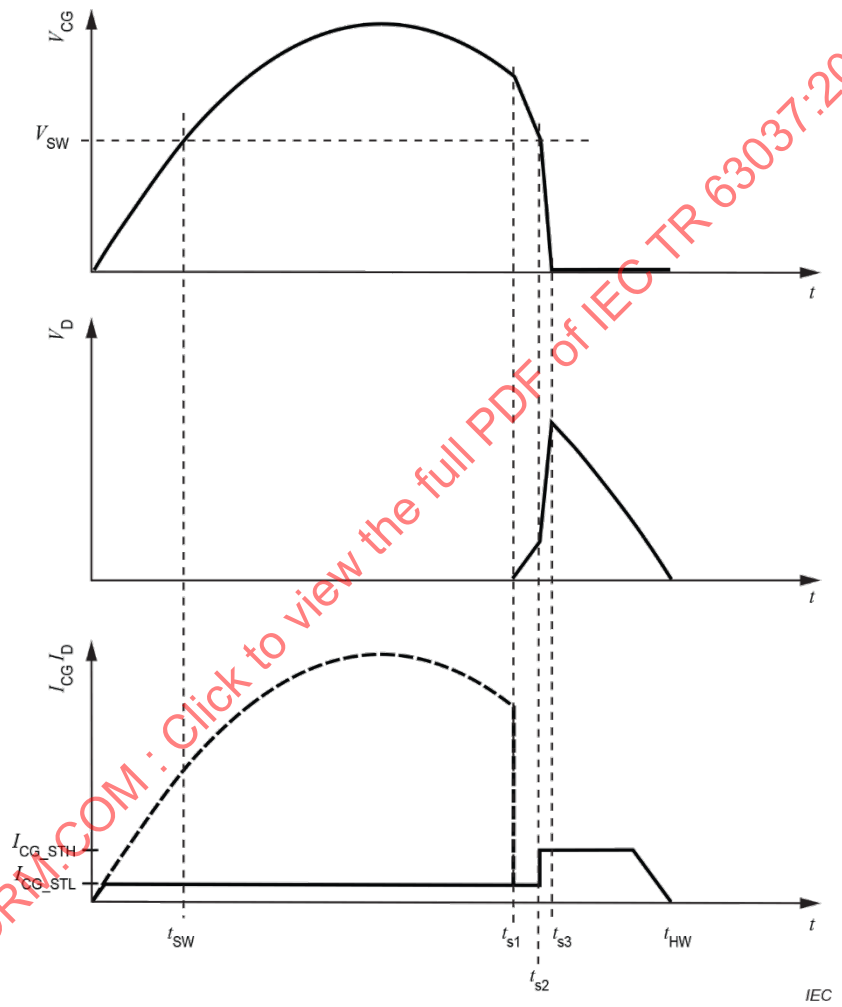


Figure 3 – Timing trailing edge dimming method

7.2.3.2 Electrical characteristics during the conducting period

The conducting period starts at the zero crossing of the mains and ends at time t_{s1} when the timing element of the phase-cut dimmer deactivates its power switch and the impedance of the phase-cut dimmer Z_D increases towards Z_{D_max}.

During the conducting period, the controlgear should comply with the electrical characteristics listed in Table 12.

During this period, the phase-cut dimmer continuously applies full power to the controlgear. Therefore, the impedance Z_D of the phase-cut dimmer remains continuously at its minimum value Z_{D_min}, independently from the current $I_D = I_{CG}$.

The impedance Z_D of the phase-cut dimmer is Z_{D_min} when the voltage $V_D(t)$ across the phase-cut dimmer is less than $0{,}1 \cdot V_M(t)$ during the entire conduction period.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the instantaneous value of the mains voltage.

From the zero crossing of the mains to time t_{s1}, the controlgear should provide a current path with a minimum current-carrying capability of I_{CG_STL} as listed in Table 12.

Since the current I_{CG_STL} is based on nominal data of a controlgear, a factor of 0,7 is inserted to account for the fact that the current drawn by the controlgear will have some distortion or displacement and may not be a perfect sine-wave or rectangular shape. Therefore the factor 0,7 introduces some margin for this. Additionally, in accordance with this document, the controlgear may not operate with its nominal wattage even at the maximum conduction angle.

Table 12 – Nominal mains voltage from 100 V to 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_{s1}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω V_{CG} > 6 V: $I_{CG}(t) = I_{CG\_STL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$

7.2.3.3 Electrical characteristics during the transition from the conducting to the non-conducting period

The transition from the conducting to the non-conducting state of the phase-cut dimmer starts at time t_{s1} and ends at time t_{s3}.

At time t_{s1}, the impedance Z_D of the phase-cut dimmer starts to increase towards Z_{D_max}. From time t_{s1} to t_{s2}, the phase-cut dimmer limits the current I_D.

The minimum value of $t_t = t_{s2} - t_{s1}$ should be as listed in Tables 13 to 17.

Since the controlgear provides a minimum current-carrying capability of I_{CG_STL} (see Tables 13 to 17), the voltage across the input terminals of the controlgear decreases towards zero and falls below the voltage V_{SW} at t_{s2} (see Figure 3).

NOTE 1 ~~This requirement is to~~ The minimum current-carrying capability ensures that parasitic capacities of the installation, the active capacity C_t between the terminals of the phase-cut dimmer (see Figure 3) and a capacitor that might be assembled inside the controlgear and which is connected directly with the mains terminals of the controlgear is discharged in a reasonable time to allow the phase-cut dimmer to supply itself sufficiently.

NOTE 2 The ratio between the values of the period t_{s2} to t_{HW} as given in Tables 13 to 17 for the different mains voltages is proportional to the ratio of the relevant mains voltages. The values of I_{CG_STH} scale inversely with the mains voltage. The value of V_{SW} scales directly with the mains voltage. The value of I_{D_nc} is always 10 % lower than the relevant I_{CG_STH}.

The slew rate SR should be calculated based on the measurement of the voltage slope of V_{CG} by measuring the time (dt) between $V_{CG} = 0{,}8 \cdot V_{CG}(t_{s1})$ and $V_{CG} = V_{SW}$ and by calculating the differential voltage d$V_{CG} = 0{,}8 \cdot V_{CG}(t_{s1}) - V_{SW}$.

When the voltage V_{CG} falls below V_{SW} (time t_{s2}), the controlgear should provide a minimum current-carrying capability of I_{CG_STH} as listed in Tables 13 to 17.

NOTE 3 The values of V_{SW} and I_{CG_STH} are selected to achieve a good compromise between the ability for the phase-cut dimmer to supply itself on one side and the appearing power loss in the controlgear on the other side.

NOTE 4 t_{s2} is defined by the time at which V_{CG} falls below V_{SW}. V_{CG} and I_D can be measured simultaneously with a 4-channel oscilloscope, and the value of I_D between t_{s1} and t_{s2} can be determined. The break in slope of V_D at t_{s2} (if such a break in slope exists) is not a criteria to define t_{s2}.

Table 13 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0,7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0,7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0,09$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0,108$ V/µs (60 Hz) when the ~~CG~~ controlgear is supplied by a current source driving $(2,8 \text{ mA} \cdot P_{CG})$ / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	$0 \text{ V} \leq V_{CG} \leq 3$ V: Z_{CG} not defined $3 \text{ V} < V_{CG} \leq 6$ V: ~~Z_{CG}~~ $V_{CG} \leq 1\,200\ \Omega$ $6 \text{ V} < V_{CG} < v_{SW} = 22$ V: $P_{CG} < 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 13,8 \text{ mA/W} \cdot P_{CG}$ $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 165,6$ mA

Table 14 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0,7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0,7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0,010\,5$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0,126$ V/µs (60 Hz) when the ~~CG~~ controlgear is supplied by a current source driving $(2,8 \text{ mA} \cdot P_{CG})$ / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	$0 \text{ V} \leq V_{CG} \leq 3$ V: Z_{CG} not defined $3 \text{ V} < V_{CG} \leq 6$ V: $Z_{CG} \leq 1\,200\ \Omega$ $6 \text{ V} < V_{CG} < V_{SW} = 26$ V: $P_{CG} < 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 11,5 \text{ mA/W} \cdot P_{CG}$ $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 138$ mA

Table 15 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0{,}7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0{,}175$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0{,}210$ V/µs (60 Hz) when the ~~CG~~ controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 43 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 6{,}9$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 82{,}8$ mA

Table 16 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0{,}7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0{,}2$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0{,}24$ V/µs (60 Hz) when the ~~CG~~ controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 40 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 6$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 72$ mA

Table 17 – Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0{,}7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0{,}245$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0{,}295$ V/µs (60 Hz) when the ~~CG~~ controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 60 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 5$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 60$ mA

7.2.3.4 Electrical characteristics during the non-conducting period

During the non-conducting period, the controlgear should comply with the electrical characteristics listed in Tables 13 to 17.

The non-conducting period ends at the next zero crossing of the mains at time t_{HW}.

During this period, the controlgear should provide a minimum current-carrying capability of I_{CG_STH} as listed in Tables 13 to 17. At small input voltages of the controlgear when I_{CG_STH} cannot be reached due to the characteristics of its input circuitry (e.g. inrush current limiting elements), only its impedance Z_{CG} is defined as listed in Tables 13 to 17.

During this period, the phase-cut dimmer limits the current I_D to $n \cdot I_{D\_nc}$ as ~~listed~~ indicated in IEC TR 63036, whereby I_{D_nc} is related to P_{min} of the phase-cut dimmer.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing trailing edge characteristics for 100 ms.

NOTE This is for reducing power losses in the case where a controlgear is used without a phase-cut dimmer.

7.3 Electrical characteristics during the off-state of a ~~phase-cut dimming~~ lighting system

The off-state of a ~~phase-cut dimming~~ lighting system is when no lamp connected with a controlgear is emitting light.

To set a controlgear in the off-state, the phase-cut dimmer increases its impedance Z_D until the controlgear is not sufficiently supplied with power to operate the lamp.

A phase-cut dimmer that needs no supply during the off-state of all connected controlgear may open the current loop of the system, for example by means of a mechanical switch.

A phase-cut dimmer that needs a power supply also during the off-state of all connected controlgear requires that the connected controlgear provide a current carrying capability,

although no lamp is operated (electronic off-state) in order to provide power to the electronic circuits within the dimmer to enable returning to the on-state when demanded.

If none of the connected controlgear is able to provide the current carrying capability due to insufficient power, the impedance Z_{CG} of the controlgear will increase.

The phase-cut dimmer may reduce its impedance Z_D to supply power to the connected controlgear in order to reestablish a current carrying capability that carries the needed supply current I_{D_nc}.

By reducing Z_D, the voltage V_D will decrease and the voltage V_{CG} will increase, thus all connected controlgear are energized and the requested current carrying capability is generated in the system to carry the required supply current I_D of the phase-cut dimmer.

The controlgear should provide a minimum current carrying capability of I_{PO} when the voltage V_{CG} is in the range of V_{PO} to V_{SW} (see Table 18). For voltages V_{CG} smaller than V_{PO} and higher than V_{SW}, the current carrying capability of the controlgear is not defined.

The controlgear should not operate the lamp when the voltage V_{CG} is below V_{SW}, and therefore no light should be emitted.

The phase-cut dimmer limits the current to a level that ensures that the voltage V_{CG} that is applied to the controlgear does not exceed V_{SW}.

Table 18 – Currents and voltages for controlgear during the electronic off-state

V_M [V]	100	120	200	230	277
V_{PO} [V]	15	15	30	30	30
I_{PO} [mA]	20	20	10	10	10
I_{PO_RMS} [mA]	8	8	4	4	4

NOTE The values of voltages and currents are instantaneous values except I_{PO_RMS}.

7.4 Audible noise

The total noise that is emitted by controlgear and lamps with integrated controlgear is radiated in all directions to the space surrounding these devices and can be characterized by the sound pressure level.

The preferred noise emission method to quantify the emitted noise is the A-weighted sound power level (LWA), expressed in decibels.

The principles of IEC 60704-1, ISO 3741 (reverberation method) and ISO 3744 (anechoic method) are adopted. Other existing standards (i.e. ISO 1996-1) could also be applied.

A controlgear or lamp with integrated controlgear that is operated at relevant operating conditions as defined in the test procedures should emit less than 30 dBA (long integration time).

7.5 Ghosting

Some applications use switching elements or dimmers that have a pilot light which requires a small amount of current in order to operate correctly.

Some controlgear may be inappropriate for these applications and their use will result in emitting light (ghosting) when the switch or dimmer is in the off-state.

The ghosting can be avoided by connecting at least one controlgear having properties as described in 7.3.

Controlgear complying with 7.3 provide a specific amount of current carrying capability in the electronic off-state without supplying sufficient power to connected lamps to produce light.

This amount of current is available to supply dimmers, electronic switches and pilot lights in mechanical switches.

7.6 Flicker of light output

Flicker is the perception of visual unsteadiness induced by a light stimulus whose luminance or spectral distribution fluctuates with time for a static observer in a static environment. The typical frequency range in which flicker is perceived is from a few Hz up to 80 Hz. Flicker may occur as a result of mains-voltage fluctuations, product design or system-level interactions (e.g. controlgear with an incompatible external dimmer).

Stroboscopic effects, which are defined by having frequencies above 80 Hz are out of the scope of this document. IEC TR 61547-1 describes methods for characterizing the variation of light output from the lamp (flicker) and recommends limits for the short-term flicker indicator, P_{st}. When operated on a stable phase-cut waveform, the flicker measurement of the illuminance, P_{st}^{LM}, should be less than 1.

7.7 Dimming range

Subclause 7.7 describes the relative brightness of lamps connected to integrated or external controlgear which are operated with the output voltage of a mains voltage phase-cut dimmer related to the adjusted conduction angle of the dimmer.

For determining the dimming response, the characteristic values MLO and RMLO, as defined in 3.1.14 and 3.1.15, are used.

The light output of a light source which is operated by an integrated or an external controlgear should depend on the conduction angle of the phase-cut dimmer as listed in Table 19 when the controlgear is operated at nominal mains voltage.

The light output of the lamp connected to the controlgear should be as listed in Table 19 when supplied by a phase-cut waveform with conduction angles as listed in Table 19.

Table 19 – Light output when connected to a dimmer

Conduction angle (°)	Light output
> 0 and < 35	Undefined
35 to 40	Stable light output of RMLO or less
40 ± 1	Stable light output of (10 to 25) % or less of MLO
40 to 120	Increasing from RMLO to (80 to 90) % of MLO or greater
> 120 and < 179	Not less than (80 to 90) % of MLO and not more than 110 % of MLO

7.8 Maximum number of cycles

Lamp cycling requirements are specified in IEC 62612.

LED module cycling requirements are specified in IEC 62717.

8 Test procedures

8.1 General

To test controlgear, the equivalent circuits EC_D ("synthetic dimmer") as defined in Annex B should be used.

8.2 Parameters

To simplify the description of the test setups and the test procedures, testing conditions for controlgear related to specific moments in time are defined in degree phase angles related to the mains zero crossings. Thus, a definition of different values for the moments in time such as t_{s1}, t_{s2} or t_{HW} is not necessary for different mains frequencies.

Table 20 – Parameters for testing purposes

V_M [V]	100	120	200	230	277
R_R	V_{M^2}/P_{max}	V_{M^2}/P_{max}	V_{M^2}/P_{max}	V_{M^2}/P_{max}	V_{M^2}/P_{max}
V_{test} [V]	0 to 23	0 to 23	0 to 45	0 to 45	0 to 45
V_1 [V]	8	8	8	8	8
SR_L [V/µs]	See Table ~~2~~6				
α_L	90°				
~~β_L~~	~~120°~~				
SR_T [V/ms]	200	200	200	200	200
~~α_T~~ β_T	120°				

8.3 Tests for leading edge dimmable devices

8.3.1 General

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical ~~behavior~~ response of controlgear during different periods of mains waveform according to 7.2.2.

A test circuit as shown in Figure 4 should be used to test the controlgear.

8.3.2 Test related to the non-conducting phase

Pre-condition: Controlgear applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.2 with the values of V_1, α_L and SR_L given in Table 20.
Test: Measure the current I_{CG} of the controlgear. Measure I_{CG} from 0° until $V_{CG} > V_{SW}$.
Expected results: 6 V ≤ V_{CG} ≤ V_{SW}: $I_{CG} \geq I_{CG\_SL}$ as listed in Tables 1 to 5. NOTE The controlgear ~~may~~ can deactivate its current-carrying capability during the non-conducting phase after it has not detected an input voltage waveform showing an unsteady waveform (leading edge characteristic) for one minute.

8.3.3 Test related to the conducting phase and to the transition from the non-conducting to the conducting phase

Pre-condition: Controlgear applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.2 with the values of V_1, α_L and SR_L given in Table 20.
Test: Measure the current I_{CG} of the controlgear. Measure I_{CG} from t_s (α_L) to t_{SW} and measure I_{CG} from t_{SW} to t_{HW}.
Expected results: from t_s to t_{SW}: $I_{CG} \leq I_{CG\_pk}$ (P_{CG}) from t_{SW} to t_{HW}: 3 V < V_{CG} ≤ 6 V: $I_{CG} \geq V_{CG} / Z_{CG}$ with Z_{CG} as listed in Tables 7 to 11. 6 V < V_{CG} < V_{SW}: $I_{CG} = I_{CG\_SL}$ as listed in Tables 7 to 11.

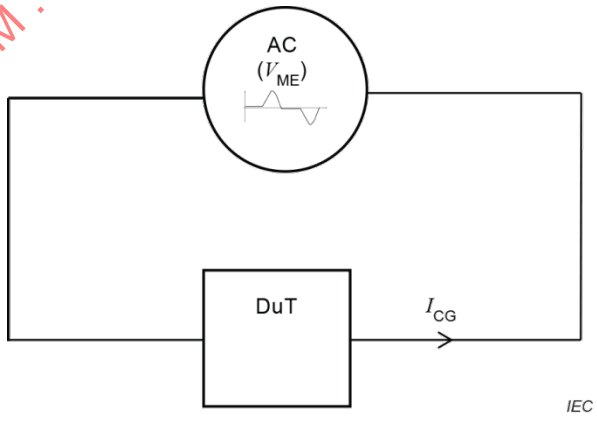


Figure 4 – Test setup for testing the conducting phase

8.4 Tests for trailing edge dimmable devices

8.4.1 General

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical ~~behavior~~ response of controlgear during different periods of mains waveform according to 7.2.3.

8.4.2 Test related to the conducting phase

An applicable test circuit is shown in Figure 4 .

Pre-condition: Controlgear applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.2 with the values of V_1, ~~α_T~~, $\beta°$ and SR_T given in Table 20.
Time related to last zero crossing: 0 to $V(t) < V_{SW}$
Test: Measure I_{CG} in dependence of the instantaneous value of the applied voltage.
Expected results: 3 V ≤ V_{CG} ≤ 6V: $I_{CG} \geq V_{CG} / Z_{CG}$ with Z_{CG} as listed in Table 12 $V_{CG} \geq 6$ V: $I_{CG} = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/V_M$ or $I_{CG} = I_{CG\_STL}(t) \geq (0{,}7 \cdot V_{CG}(t)) / (V_M^2 / P_{CG})$

8.4.3 Test related to the transition from the conducting phase to the non-conducting phase

The applicable test circuit is shown in Figure 5.

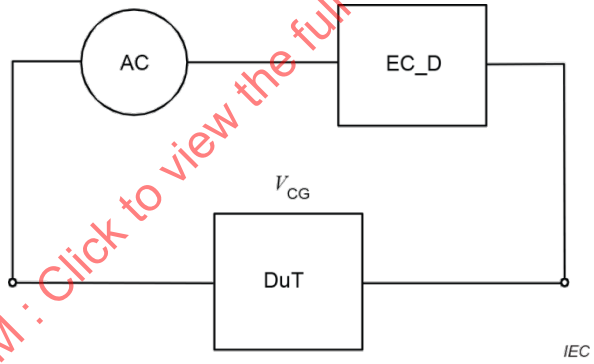


Figure 5 – Test setup for the transition from conducting to the non-conducting phase

Pre-condition: Controlgear connected to the EC_D according to Annex B, as shown in Figure 5, system powered with relevant mains voltage. Adjust the current I_D according to Annex B, as given in Tables 13 to 17.
Time related to last zero crossing: t_{s1} to t_{s2}.
Test: Measure $\lvert dV_{CG}/dt \rvert$ with a conduction angle of the EC_D of 90°, repeat this measurement with conducting angles of the EC_D of 60° and 120°.
Expected result: When the conduction angle of EC_D is terminated (t_{s1}), the voltage across the input terminals of the controlgear decreases with $\lvert dV_{CG}/dt \rvert \geq SR$, as listed in Tables 13 to ~~17~~18.

The slew rate SR should be calculated based on the measurement of the voltage slope of V_{CG} by measuring the time (dt) between $V_{CG} = 0{,}8 \cdot V_{CG}(t_{s1})$ and $V_{CG} = V_{SW}$ and by calculating the differential voltage $dV_{CG} = 0{,}8 \cdot V_{CG}(t_{s1}) - V_{SW}$.

8.4.4 Test related to the non-conducting phase

An applicable test circuit is shown in Figure 6.

Pre-condition: Controlgear applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.2 with the values of V_1, ~~α_L~~ β° and SR_L given in Table 20.
Time related to last zero crossing: t_{s2} to t_{HW}.
Test: Measure I_{CG} in dependence of the instantaneous value of the applied voltage.
Expected results: 6 V ≤ V_{CG} ≤ V_{SW}: $I_{CG} \geq I_{CG\_STH}$ 3 V ≤ V_{CG} < 6 V: $I_{CG} \geq V_{CG} / Z_{CG}$ with Z_{CG} as listed in Tables 13 to 17.

8.5 Tests for characteristics during electronic off-state

Tests concerning the electrical characteristics should ensure compliance of devices with this document in terms of electrical ~~behavior~~ response of controlgear during the electronic off-state of a ~~phase-cut dimming~~ lighting system according to 7.3.

A test circuit as shown in Figure 6 should be used to test the controlgear.

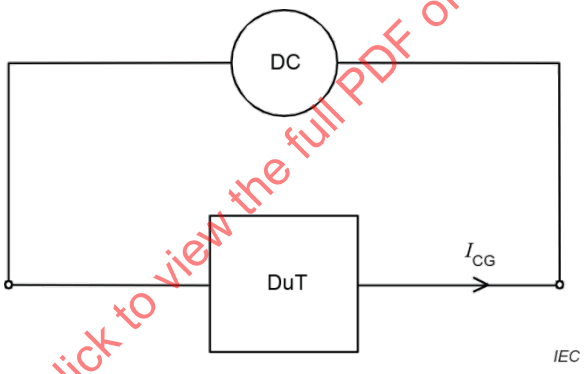


Figure 6 – Test setup for the non-conducting phase

Pre-condition: Controlgear connected to a controllable DC voltage source.
Test: Vary the voltage of the DC source within the range for V_{test} as given in Table 20 for the relevant mains voltage. Measure I_{CG} and record at which voltages in the range of V_{test} the current carrying capability is activated.
Expected results: Controlgear provides a current carrying capability I_{PO} at $V_{PO} \leq V_{PO} < V_{SW}$ as listed in Tables 1 to 5, Tables 7 to 11, and Tables 13 to ~~17~~18. Controlgear does not operate the lamp at $V_{CG} \leq V_{SW}$, no light is emitted.

8.6 Testing audible noise

8.6.1 General

Averaged over the microphone positions, the background noise level should be at least 6 dB below and preferably more than 15 dB below the sound pressure level to be measured.

8.6.2 Test setup

Only the device under test should be in the testing chamber while the synthetic dimmer should be outside the testing chamber.

Care should be taken to ensure that any auxiliary equipment (such as electrical conduits or cables) that is necessary for the operation of the appliance does neither radiate a significant amount of sound energy into the test environment nor change the sound output of the device under test.

To provide a correct measurement of noise, the manufacturer's instructions for the installation and use of the DUT as well as the test conditions should be taken into account.

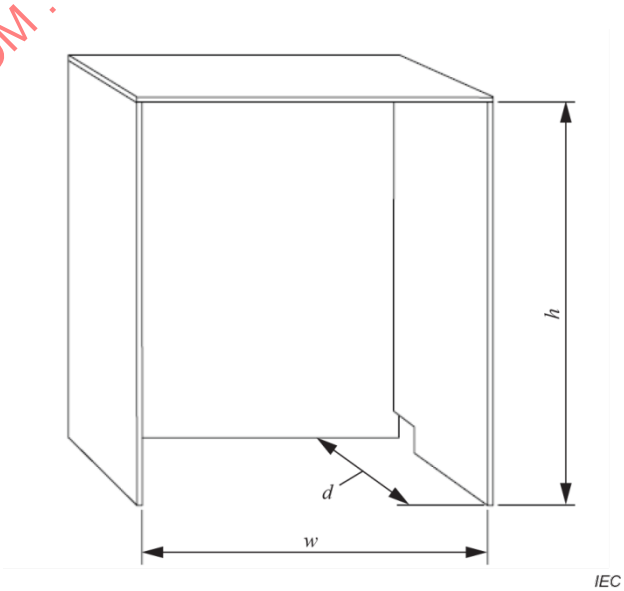
All products are mounted in an appropriate test enclosure according to Figure 7. The height of the lowest edge of the DUT from the floor should be fixed according to the manufacturer's instructions. On the front side of the enclosure, the DUT should be fixed in the middle of the horizontal plan. The test enclosure with the DUT should be placed in the anechoic chamber. Care should be taken that the base shelf does not transmit any noise to the DUT.

A DUT mounted on a metallic stand is placed on a stand constructed according to the manufacturer's instructions.

Wall-mounted DUTs, including their accessories, if any, are fastened or held by an appropriate fixture in close contact, without any resilient means other than those incorporated in the DUT.

Flush mounted products are built-in according to the manufacturer’s installation instructions.

In general, at least three microphone positions should be used. The use of a moving microphone along one specific direction will often be more convenient than the use of a number of fixed microphones. Instrumentation for measuring acoustical data fixed on the horizontal plane and on the same height is located on the floor so that the projection of the centre of its reference coincides with the projection of the centre of the reference of the DUT. The preferred value of the measurement distance L is 1 m. Three values of measurement should be done, one at the centre and the following next two values with an angle of 45° on each side of the DUT (see Figure 8).



h = 1 650 mm, w = 1 350 mm, d = 550 mm

Figure 7 – Test enclosure

The material of the enclosure is 19 mm thick untreated particle-board (chipboard) or untreated plywood, having a density between 600 kg/m^3 and 750 kg/m^3.

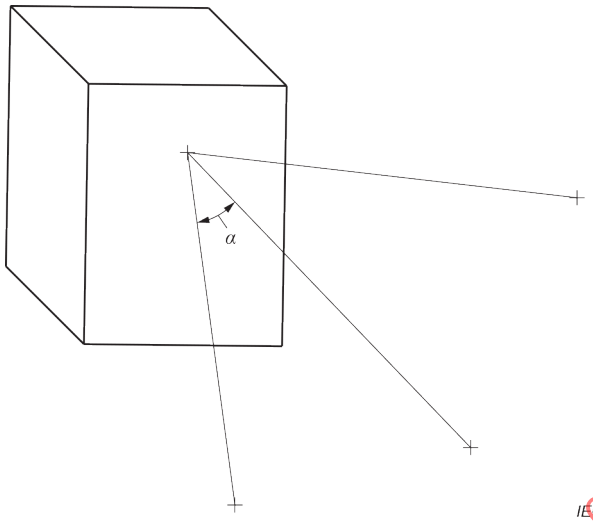


Figure 8 – Geometry of microphone placement in relation to the DUT

A lamp having an integrated controlgear should be equipped with a lampholder but not with a luminaire.

If the load connected to the controlgear can be modified (not a self ballasted lamp), the controlgear should be connected to the minimum and maximum load of the controlgear as declared by the manufacturer.

Only the device under test should be in the testing chamber and in the case where a controlgear is tested (no self ballasted lamp) the load should be outside the testing chamber.

The synthetic dimmer that operates the lamp or the controlgear should be outside the testing chamber.

8.6.3 Test procedures

To test the sound emission of a lamp with integrated controlgear, the following procedure should be followed:

1) Connect the lamp to the synthetic dimmer (using the lampholder). Turn on the synthetic dimmer adjusted to the maximum conduction angle.
2) Wait until thermal equilibrium is obtained in the lamp.
3) Adjust the synthetic dimmer to a conduction angle that leads to the maximum audible noise level emitted by the lamp.
4) Record the maximum sound pressure level.

To test the sound emission of a controlgear, the following procedure should be followed:

a) Connect the maximum load to the controlgear and turn on the synthetic dimmer adjusted to the maximum conduction angle.
a) Wait until thermal equilibrium is obtained in the controlgear.
b) Adjust the synthetic dimmer setting to produce the maximum audible noise level from the controlgear.
c) Record the maximum sound pressure level.
d) Connect the minimum load to the controlgear and repeat the test (if applicable).

8.7 Testing ghosting

To test ghosting of lamps, the controlgear that operates the lamp should be connected to a switching element and its light output should be observed.

Pre-condition: The controlgear is connected to a switch that is set in the off-state and limits the current to I_{PO} as described in IEC TR 63036:2016 or 7.3 of this document. The electrical conditions of 8.3 of IEC TR 63036:2016 or 7.3 of this document apply with V_{CG} less than V_{SW}.
Test: Measure the light output of the lamp. If the device under test is integrated, then its light output should be measured. If the device under test is a separated load, a current measurement from the controlgear to the load is an acceptable substitute for the light measurement.
Expected result: The light measurement (or current measurement) should be less than the measurement error of the measurement setup (statistically indistinguishable from zero).

8.8 Measurement method for determining flicker

The method of testing flicker is as follows:

Pre-condition: Controlgear applied to an AC test voltage source (V_{ME}) providing the relevant mains voltage according to Clause A.2 with the values of V_1, and SR_L given in Table 20.
Test: The equivalent dimmer circuit shown in Figure B.1 is used for this test. Before measuring flicker, resistor R20 is varied to get the right lamp current at a phase angle of 0°. Measure flicker according to IEC TR 61547-1 at α_L equal to 45°, 90° and 120° and by varying pulse generator V2 to get the right angle.
Expected result: Flicker value (P_{st}^{LM}) less or equal to 1.

8.9 Measurement method for determining dimming range

Measurement of the light output follows CIE S 025 and EN 13032-4.

Determination of MLO:

Pre-condition: Controlgear connected to an AC test voltage source providing a continuous sinusoidal waveform with the relevant nominal mains voltage as shown in Figure 5.
Test: Measure the light output.
Expected result: Record the light output as MLO.

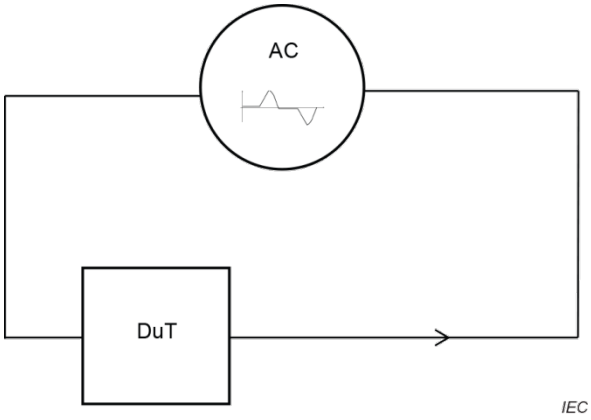


Figure 9 – Test setup for determination of RMLO

Determination of RMLO:

Pre-condition: Controlgear connected to an AC test voltage source (V_{ME}) as shown in Figure 9 providing the relevant nominal mains voltage according to Clauses A.1 or A.2 of IEC TR 63036:2016 or Annex A of this document, with the values of V_1= 0 V, β_L = 40° ± 1°.
Test: Measure the light output.
Expected result: Record the light output as RMLO.

Test for dimming range:

Pre-condition: Controlgear connected to an AC test voltage source (V_{ME}) as shown in Figure 9 providing the relevant nominal mains voltage according to Clauses A.1 or A.2 of IEC TR 63036:2016 with the values of V_1= 8 V, β_L = 35°, 45° and 120° and SR_L according to the values in Table 2 of IEC TR 63036:2016 or Clauses A.1 or A.2 of this document.
Test: Measure the light output.
Expected results: Light output relative to MLO should be as listed in Table 2.

Annex A
(informative)

Voltage shapes to be used for tests ~~in IEC TR 63037~~

A.1 General

A test AC voltage source (V_{ME}) with the waveform as shown in Figure A.1 or Figure A.2 should be used as indicated in the defined tests. The detailed settings for time and voltage should be set with an accuracy of ≤ 1 %. The internal resistance of this voltage source should not exceed 1 Ω.

A.2 Waveform description

0° to α°: constant voltage with the value V_1

α° to α_1°: constant slew rate (SR)

α_1° to 180°: sinusoidal voltage according to V_M

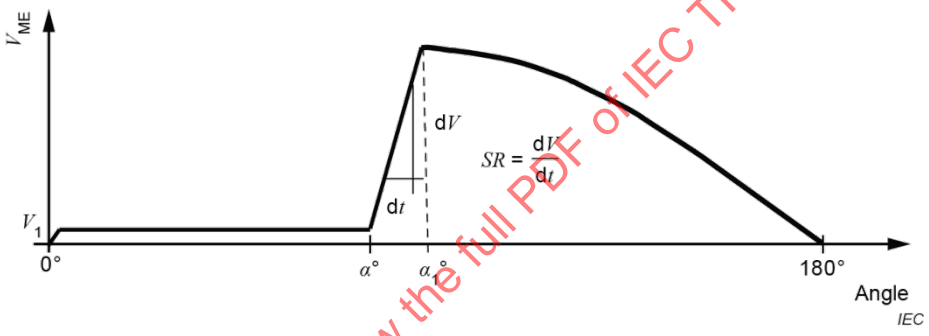


Figure A.1 – Waveform of AC voltage ~~source~~

0° to β°: sinusoidal voltage according to V_M

β° to β1°: constant slew rate (SR)

β1° to 180°: constant voltage with the value V_1

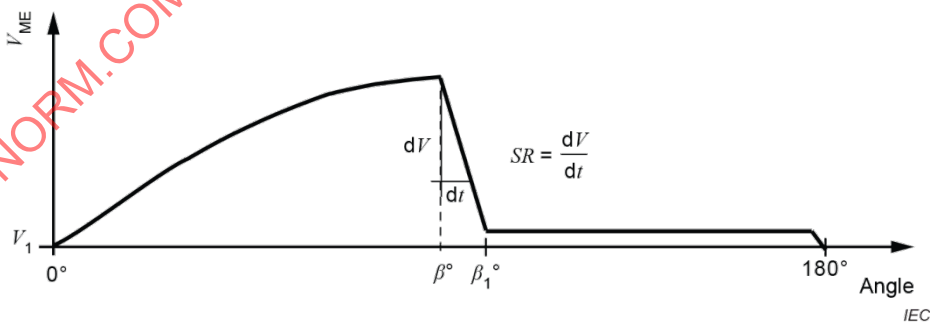


Figure A.2 – Waveform of AC voltage source

Annex B
(informative)

Equivalent phase-cut dimmer circuit

Figure B.1 shows the equivalent circuit EC_D for a phase-cut dimmer:

Components and values are only exemplary beside capacitance C2 which is mandatory, representing the maximum wiring capacitance.

V2 is a pulse generator that provides a control signal for the transistors T1 and T2 leading to conduction states of these two transistors in order that the correct phase angle is adjusted.

Adjust the current I_D ~~$= (U_{trans} \cdot P_{min})/W$~~ according to Tables 13 to 17 by varying resistor R20.

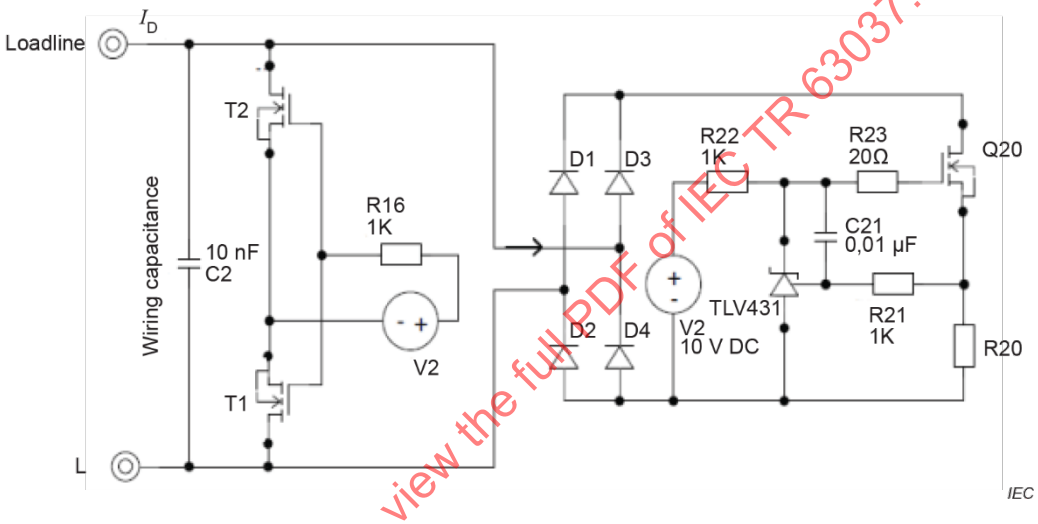


Figure B.1 – ~~Scheme~~ Schematic diagram of EC_D circuit

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IEC 60364 (all parts), *Low-voltage electrical installations*

IEC 60669-1, *Switches for household and similar fixed-electrical installations – Part 1: General requirements*

IEC 60669-2-1[2], *Switches for household and similar fixed electrical installations – Part 2-1: Particular requirements – Electronic switches*

IEC 60704-1, *Household and similar electrical appliances – Test code for the determination of airborne acoustical noise – Part 1: General requirements*

IEC TR 61547-1, *Equipment for general lighting purposes – EMC immunity requirements – Part 1: An objective light flickermeter and voltage fluctuation immunity test method*

IEC 62612, *Self-ballasted LED lamps for general lighting services with supply voltages > 50 V – Performance requirements*

IEC 62717, *LED modules for general lighting – Performance requirements*

IEC TR 63036:2016, *Electrical interface specification for phase-cut dimmer in phase-cut dimmed lighting systems*

ISO 3741, *Acoustics – Determination of sound power levels and sound energy levels of noise sources using sound pressure – Precision methods for reverberation test rooms*

ISO 3744, *Acoustics – Determination of sound power levels and sound energy levels of noise sources using sound pressure – Engineering methods for an essentially free field over a reflecting plane*

ISO 1996-1, *Acoustics – Description, measurement and assessment of environmental noise – Part 1: Basic quantities and assessment procedures*

CIE S 025, *Test method for LED lamps, LED luminaires and LED modules*

EN 13032-4, *Light and lighting – Measurement and presentation of photometric data of lamps and luminaires – Part 4: LED lamps, modules and luminaires*

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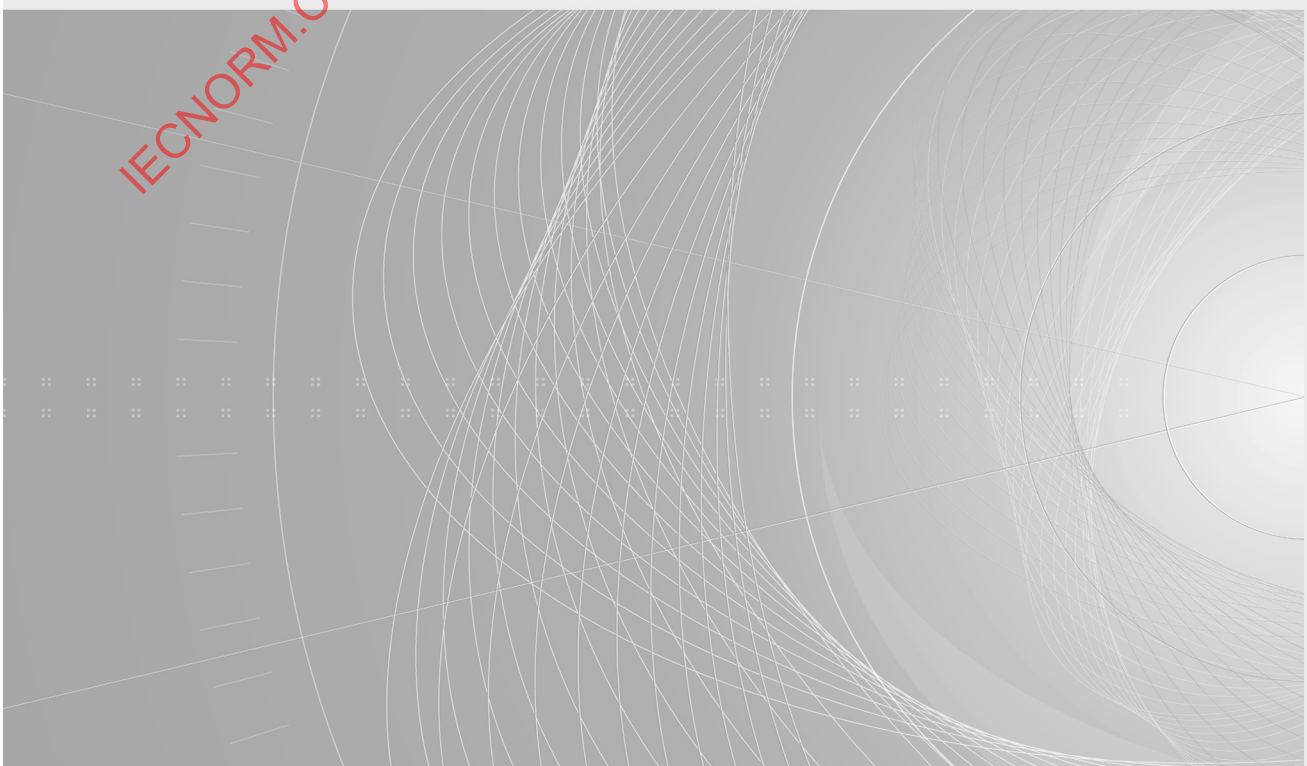
2 Under preparation. Stage at the time of publication IEC AFDIS 60669-2-1:2019.

IEC TR 63037

Edition 2.0 2019-07

TECHNICAL REPORT

Electrical interface specifications for self ballasted lamps and controlgear in phase-cut dimmed lighting systems



IEC TR 63037:2019-07(en)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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ELECTRICAL INTERFACE SPECIFICATIONS FOR SELF BALLASTED LAMPS AND CONTROLGEAR IN PHASE-CUT DIMMED LIGHTING SYSTEMS

FOREWORD

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IEC TR 63037, which is a Technical Report, has been prepared by IEC technical committee 34: Lamps and related equipment.

This second edition cancels and replaces the first edition published in 2016. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) emission of audible noise;
b) ghosting caused by issues that are not related to the power supply of the dimmer or synchronization;

c) stability of phase angle waveform (for the dimmer), including symmetry and stability tests;
d) flicker of light loads;
e) repetitive ring up voltage;
f) dimming range; and
g) number of switching cycles have been added.

The text of this Technical Report is based on the following documents:

Draft TR	Report on voting
34/517/DTR	34/583A/RVDTR

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

This document describes the technical requirements for self-ballasted lamps and controlgear to work with phase-cut dimmers. For a complete picture of the technical requirements the user should also refer to IEC TR 63036 (see also IEC 60669-2-1:—,[1] Annex EE), the companion document that contains technical requirements and testing methods for phase-cut dimmers.

[1] Under preparation. Stage at the time of publication IEC AFDIS 60669-2-1:2019.

ELECTRICAL INTERFACE SPECIFICATIONS FOR SELF BALLASTED LAMPS AND CONTROLGEAR IN PHASE-CUT DIMMED LIGHTING SYSTEMS

1 Scope

This document provides guidance to controlgear/integrated lamp designers for the development of products suitable to operate with future phase-cut dimmers. It describes the possible voltage signals and the expected response of the controlgear/integrated lamps.

This document describes the expected response of controlgear during all operation states of a phase-cut lighting system and provides a complete understanding of the requirements for phase-cut dimmers. The response of a phase-cut dimmer is described in IEC 60669-2-1:—, Annex EE.

This document specifies the system performance aspects and test procedures for the control by mains voltage phase-cut dimming of the brightness of mains operated electronic lighting equipment intended to be controlled by mains voltage phase-cut dimmers, such as LED integrated lamps and light sources with external controlgear.

Safety requirements are not covered by this document, but by respective product standards.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-845, *International Electrotechnical Vocabulary – Part 845: Lighting* (available at http://www.electropedia.org)

IEC 62504, *General lighting – Light emitting diode (LED) products and related equipment – Terms and definitions*

3 Terms, definitions, abbreviated terms and symbols

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-845 and IEC 62504 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
phase-cut dimmed lighting system
lighting system
combination of a phase-cut dimmer and one or more controlgear and light sources

Note 1 to entry: The term “lighting system” used in this document is an abbreviated form of "phase-cut dimmed lighting system".

3.1.2
off-state
state of a lighting system when no light is emitted

3.1.3
on-state
state of a lighting system when light is emitted

3.1.4
electrical interface
electrical parameters for supplying power and making exchange of information between the phase-cut dimmer and controlgear

3.1.5
phase-cut dimmer
dimmer
electronic switch connected in series with a load, that changes the supply voltage waveform applied to the load from the mains voltage waveform to a leading edge (forward phase) or a trailing edge (reverse phase) AC voltage waveform

Note 1 to entry: Some phase-cut dimmers are capable of switching their output between leading edge and trailing edge waveforms.

Note 2 to entry: The output voltage waveform of a phase-cut dimmer is applied to one or more loads. The conduction angle of the voltage waveform is adjustable.

Note 3 to entry: Within this document, where the term “dimmer” is used, the term “phase-cut dimmer” is meant.

3.1.6
two-wire phase-cut dimmer
phase-cut dimmer connected in series with a load that has no connection to neutral

3.1.7
three-wire phase-cut dimmer
phase-cut dimmer connected in series with a load that has an additional connection to neutral

3.1.8
controlgear
one or more components between the supply and one or more lamps which may serve to transform the supply voltage, limit the current of the lamp(s) to the required value, provide starting voltage and preheating current, prevent cold starting, correct power factor or reduce radio interference

Note 1 to entry: Lamps may have integrated controlgear such as an integrated LED lamp. Any references to controlgear will include any such integrated lamps.

3.1.9
load side
connection from the output of the phase-cut dimmer to the supply input of one or more controlgear

3.1.10
conducting period
time period during which the phase-cut dimmer supplies power to a controlgear

3.1.11
non-conducting period
time period during which the phase-cut dimmer does not supply power to a controlgear

3.1.12
half-wave
positive or negative 180° of an AC sine wave starting and ending at the zero crossing point

3.1.13
phase angle
position within a half-wave expressed in degree, being in the range of 0° to 180°, referred to the beginning of the half-wave

3.1.14
reference minimum light output
RMLO
light output (luminous flux) produced by a lamp operated by a controlgear that is connected to mains voltage via a phase-cut dimmer set to a conduction angle of 40° ± 1°

3.1.15
maximum light output
MLO
light output (luminous flux) produced by a lamp operated by a controlgear that is directly connected to mains voltage

3.2 Abbreviated terms and symbols

To describe the electrical characteristics of the electrical interface, the following symbols are used:

α	Angle where the test voltage starts rising with the given slew rate SR as shown in Figure A.1. Subscripts L and 1 (see Table 20) refer to leading and end-of-transition, respectively.
β	Angle where the test voltage starts falling with the given slew rate SR as shown in Figure A.2. Subscripts T and 1 (see Table 20) refer to trailing and end-of-transition, respectively.
C_f	Filter capacitor to reduce high frequency disturbances
EC_D	Equivalent circuit that represents a phase-cut dimmer for controlgear testing purposes
I_{CG}	Current through the input terminals of the controlgear (see Figure 1)
I_{CG_pk}	Repetitive peak current of the controlgear in leading edge mode
I_{CG_SL}	Current-carrying capability of the controlgear with $V_{CG} \leq V_{SW}$ in leading edge mode
I_{CG_STH}	Current-carrying capability of the controlgear with $V_{CG} \leq V_{SW}$ in trailing edge mode
I_{CG_STL}	Current-carrying capability of the controlgear with $V_{CG} > V_{SW}$ in trailing edge mode
I_D	Current through the load side terminal of the phase-cut dimmer (see Figure 1)
I_{D_nc}	Maximum current through the phase-cut dimmer during the non-conducting period, limited by the phase-cut dimmer
I_{PO}	Minimum current carrying capability of the controlgear during the electronic off-state
I_{trans}	Current sourced by the phase-cut dimmer during the transition from the conducting to the non-conducting state in trailing edge mode
n	Required minimum number of controlgear connected with one phase-cut dimmer (named in phase-cut dimmer installation sheet)
P_{CG}	Rated input power of the controlgear (as marked)

P_{min}	Minimum nominal load required by the phase-cut dimmer (according to installation sheet)
SR	Absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer switches off at time t_{s1} (see Figure 3)
SR_L	Absolute value of the slew rate of the increase of the voltage across the input terminals of a controlgear in leading edge dimming mode when the phase-cut dimmer under test switches on (according to Clause 8)
SR_T	Absolute value of the slew rate of the decrease of the voltage across the input terminals of a controlgear in trailing edge dimming mode when the phase-cut dimmer under test switches off (according to Clause 8)
t_{HW}	Time related to previous zero crossing of the mains to the subsequent zero crossing of the mains (duration of a half-wave)
t_s	Time related to previous zero crossing of the mains when leading edge phase-cut dimmer reduces its impedance towards zero by activating its power switch
t_{s1}	Time related to previous zero crossing of the mains when the trailing edge phase-cut dimmer increases its impedance towards infinite by deactivating its power switch
t_{s2}	Time related to previous zero crossing of the mains when the voltage V_{CG} falls below V_{SW} in trailing edge method
t_{s3}	Time related to previous zero crossing of the mains when the transition from the conducting period to the non-conducting period is finished
t_{SW}	Time related to previous zero crossing of the mains when voltage V_{CG} crosses V_{SW}
t_t	Transition time for trailing edge mode, equals $t_{s2} - t_{s1}$
V_{CG}	Voltage across the input terminals of the controlgear (see Figure 1)
V_{CG_PK}	Repetitive peak voltage across the terminal of the controlgear
V_D	Voltage between the line side (L) and load side terminal of the phase-cut dimmer (see Figure 1)
V_M	Mains voltage (rated nominal value)
V_{ME}	Phase-cut voltage for testing purposes, sinusoidal part of the waveform (α1 to t_{HW}, 0 to β) equivalent to mains voltage
V_{PO}	Lower limit for voltage across the input terminals of the controlgear to provide a current carrying capability I_{PO} during the electronic off-state
V_{SW}	Voltage across the input terminals of the controlgear at the time that leads to disabling ($V_M(t) > V_{SW}$) or enabling ($V_M(t) < V_{SW}$), a current path having a current carrying capability of I_{CG_SL} or I_{CG_STH}
V_{test}	Value of the test voltage of the test circuit in Figure 6 (according to 8.4)
$xx(t)$	Instantaneous values of current or voltage xx
Z_{CG}	Impedance across the input terminals of the controlgear
Z_D	Impedance between the line side (L) and the load side terminals of the phase-cut dimmer
Z_{D_max}	Maximum impedance between the line side (L) and load side terminal of the phase-cut dimmer, defined by the technical properties of the phase-cut dimmer
Z_{D_min}	Minimum impedance between the line side (L) and the load side terminal of the phase-cut dimmer, defined by the power properties of the phase-cut dimmer

4 General description

A phase-cut dimmer either cuts the mains voltage immediately after the zero crossing of the mains (leading edge) or towards the next projected zero crossing of the mains (trailing edge). The functionality of both methods can be implemented in one device (universal dimmers).

This document describes requirements for controlgear during the on-state of a lighting system. Specifications are provided dependent on the dimming method for the conducting period, the non-conducting period of the phase-cut dimmer and the transitions between the conducting and non-conducting period.

In addition, this document describes requirements for controlgear during the off-state of a lighting system. Specifications are provided independently from the dimming method.

This document addresses the following issues previously reported by consumers and authorities such as:

- emission of audible noise;
- ghosting caused by issues that are not related to the power supply of the dimmer or synchronization;
- stability of phase angle waveform (for the dimmer), including symmetry and stability tests;
- flicker of light loads;
- repetitive ring up voltage;
- dimming range;
- number of switching cycles.

5 General requirements

5.1 Voltage rating

This document applies to one or more of the following mains voltages:

100 V, 120 V, 200 V, 230 V, 277 V, according to IEC 60038.

5.2 Frequency rating

This document applies to one or more of the following mains frequencies:

50 Hz or 60 Hz, according to IEC 60038.

5.3 Marking of controlgear

Controlgear suitable for operating with a phase-cut dimmer, should be marked either on the product or in the product documentation with the following:

DIM

Controlgear and lamps with integrated controlgear should be marked with the reference minimum light output (RMLO) value, or the value should be given in the manufacturer's documentation.

The RMLO value should be in the form "DIM xx %" where xx is the RMLO value.

6 Description of the lighting system and its components

6.1 Wiring method

The wiring of the devices is in accordance with the installation rules given in IEC 60364 (all parts) and also with the national wiring rules applicable in the country where the devices are installed.

6.2 Wiring diagram

The wiring of the lighting system uses the traditional method of connecting the phase-cut dimmer to the mains and to the controlgear. Figure 1 is an example of a lighting system with one phase-cut dimmer and one or two controlgear.

Regarding the connections of the phase-cut dimmer shown in Figure 1, the drawn lines represent a two-wire installation and the dashed line represents the direct connection of the phase-cut dimmer to the mains which is used in three-wire installations.

The direct connection of the phase-cut dimmer to neutral (dashed line in Figure 1) will have consequences on the power supply requirement and synchronization with the phase-cut dimmer.

This document defines requirements that enable compatibility between phase-cut dimmer and controlgear in two-wire installations. However, all predications are also valid for three-wire phase-cut dimmers to ensure proper operation of controlgear.

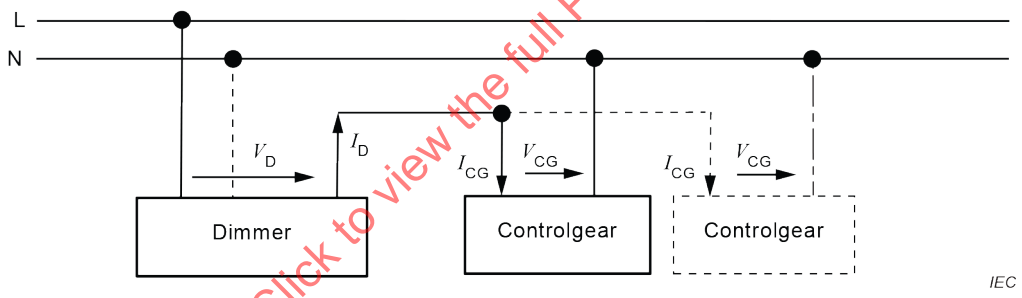

Figure 1 – Example of wiring diagram

7 Specifications

7.1 General

All information given in this document is related to a half-wave of the mains. Due to the polarity change between subsequent half-waves, all values are regarded as absolute values.

The lighting system is either in an on-state or in an off-state. In an on-state, light sources operated by the controlgear component of the lighting system emit light. In an off-state, light sources operated by the controlgear component of the lighting system do not emit light.

The off-state may be realized as mechanical off-state by opening the current loop of the lighting system with mechanical means, for example a switch. For this case, no requirements need to be fixed.

Alternatively, the off-state may be realized as electronic off-state. In this case, the phase-cut dimmer increases its impedance (i.e. stops producing phase-cut) while continuing its operation, for example to keep its control interface activated. In this case, the connected

controlgear are not energized sufficiently to operate a light source, but should provide a current path that allows the phase-cut dimmer to draw current continuously from the mains.

NOTE Applications that provide a connection to neutral allow using a three-wire device, enabling the usage of lamps that do not provide a current carrying capability according to 7.2 and 7.4.

During the on-state and the electronic off-state, it should be ensured that the phase-cut dimmer is supplied sufficiently with power and that the synchronization of the phase-cut dimmer and controlgear with the mains is ensured.

7.2 Electrical characteristics during the on-state of a lighting system

7.2.1 General

For the on-state of a lighting system, specifications are dependent on the dimming method, leading edge or trailing edge.

Each half-wave is divided into two periods, the conducting period and the non-conducting period of the phase-cut dimmer.

During the conducting period of the phase-cut dimmer, the mains voltage is applied to the controlgear. During the non-conducting period, the voltage between terminals of the phase-cut dimmer is almost equal to the mains voltage ($V_D \approx V_M$).

7.2.2 Electrical characteristics for leading edge dimming method

7.2.2.1 General

Starting from the mains zero crossing, the phase-cut dimmer remains in non-conducting state until its timing element activates the power switch at t_s. Afterwards, the phase-cut dimmer is supplying power to the load for the entire remaining part of the mains half-wave (see Figure 2).

To achieve synchronization with the mains and to control the phase-cut angle correctly, leading edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear has to be able to conduct a current I_{CG_SL}, which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

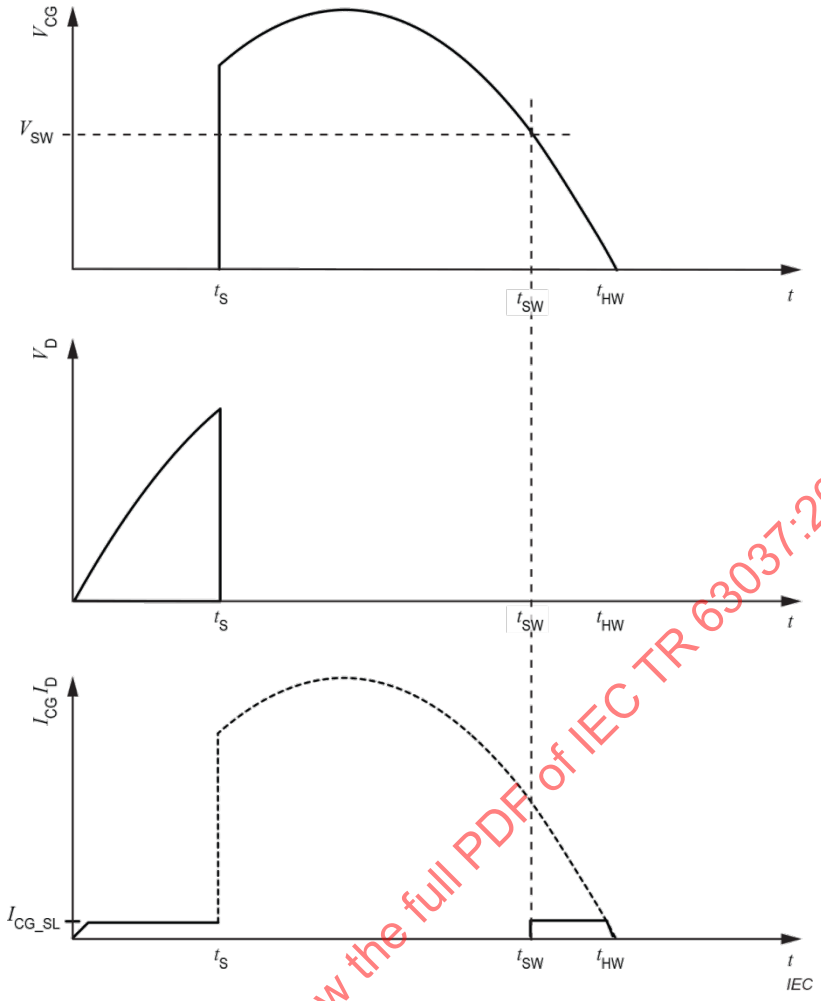

Figure 2 – Timing leading edge dimming method

7.2.2.2 Electrical characteristics during the non-conducting period

During the non-conducting period, the controlgear should comply with the electrical characteristics listed in Tables 1 to 5.

The non-conducting period starts at the zero crossing of the mains and ends at time t_S when the timing element of the phase-cut dimmer activates the power switch.

During this period, the controlgear should provide a current path with a minimum current-carrying capability of I_{CG_SL} as listed in Tables 1 to 5. At small input voltages of the controlgear when I_{CG_SL} cannot be reached due to the characteristics of its input circuitry (e.g. inrush current limiting elements), only its impedance Z_{CG} is defined as listed in Tables 1 to 5.

The controlgear may deactivate its current-carrying capability during the non-conducting period after it has not detected an input voltage waveform showing an unsteady waveform (leading edge characteristic) for 100 ms.

NOTE This is for reducing power losses in the case where a controlgear is used without a phase-cut dimmer.

Table 1 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 22 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 13,8 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 165,6 mA

Table 2 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 26 V: P_{CG} < 12 W $I_{CG}(t)$ = I_{CG_SL} ≥ 11,5 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 138 mA

Table 3 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 43 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 6,9 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 82,8 mA

Table 4 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 40 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 6 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 72 mA

Table 5 – Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_s	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 60 V: P_{CG} < 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 5 mA/W · P_{CG} P_{CG} ≥ 12 W: $I_{CG}(t)$ = I_{CG_SL} ≥ 60 mA

7.2.2.3 Electrical characteristics during the transition from the non-conducting to the conducting period

The transition from the non-conducting to the conducting state of the phase-cut dimmer starts at time t_s.

Starting from time t_s, the impedance Z_D of the phase-cut dimmer decreases until its minimum Z_{D_min} is reached. The voltage V_{CG} applied to the controlgear increases towards the instantaneous value $V_M(t)$ of the mains minus the voltage drop across the phase-cut dimmer.

The absolute value of the slew rate of the voltage change of V_D during the transition period does not exceed the values as listed in Table 6 when the phase-cut dimmer is connected to the marked maximum resistive load.

The slew rate should be calculated based on the measurement of the voltage slope of V_D by measuring the time (dt) between V_D = 0,8 · $V_D(t_s)$ and V_D = 0,1 · $V_D(t_s)$ and by calculating the differential voltage dV_D = [0,8 · $V_D(t_s)$] – [0,1 · $V_D(t_s)$].

When the voltage V_{CG} exceeds V_{SW}, the controlgear may deactivate its current carrying capability, thus possibly no current can flow through the controlgear.

NOTE Values of the slew rate represent a compromise between EMC, repetitive peak current in the controlgear and switching losses in the phase-cut dimmer power semiconductors.

Table 6 – Slew rate for voltage decrease across the phase-cut dimmer

V_M [V]	100	120	200	230	277
dV_D/dt [V/µs]	≤ 6,5	≤ 300	≤ 6,5	≤ 6,5	≤ 300

7.2.2.4 Electrical characteristics during the conducting period

During the conducting period, the controlgear should comply with the electrical characteristics listed in Tables 7 to 11.

During this period, full power is applied continuously to the controlgear from the phase-cut dimmer to allow power to be supplied to the controlgear. The values of peak current in Tables 7 to 11 apply at the maximum slew rate values given in Table 6.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the mains voltage.

At time t_{SW}, the input voltage V_{CG} of the controlgear falls below V_{SW}.

From time t_{SW} to the end of the period, the controlgear should provide a current path with a minimum current-carrying capability of I_{CG_SL}.

Table 7 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined $I_{CG\_pk}(P_{CG}) < 0{,}111$ A/W
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 22 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 8 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined $I_{CG\_pk}(P_{CG})$ < to be defined
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 26 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 9 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined $I_{CG\_pk}(P_{CG}) < 0{,}077\ 25$ A/W
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 43 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 10 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < 0,077 25 A/W
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 50 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

Table 11 – Nominal mains voltage 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
t_s to t_{SW}	Z_{CG} not defined I_{CG_pk} (P_{CG}) < to be defined
t_{SW} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 60 V: $I_{CG}(t) = I_{CG\_SL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_SL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/ P_{CG})$

7.2.3 Electrical characteristics for trailing edge dimming method

7.2.3.1 General

Starting from the mains zero crossing, the phase-cut dimmer operates in conducting state until its timing element deactivates the power switch at time t_{s1}. Afterwards, the phase-cut dimmer is not significantly supplying power to the load for the entire remaining part of the mains half-wave (see Figure 3).

To achieve synchronization with the mains and to control the phase-cut angle correctly, trailing edge phase-cut dimmers need to draw a current also during the non-conducting state.

Thus, the controlgear has to be able to conduct a current I_{CG_STH}, which allows synchronization of the phase-cut dimmer with the mains and ensures the supply of power to the phase-cut dimmer even in a two-wire installation.

Since the negative voltage slope that is triggered by the switch-off of the power switch of the phase-cut dimmer is not only determined by the current I_{CG_STL} that is conducted by the controlgear, but also by the effective capacitance of the wiring and the capacitance being effective in parallel to the phase-cut dimmer, the sum of these capacitances has to be considered.

This document and all listed values are based on systems having a maximum capacitance of the wiring of 10 nF being effective in parallel to the controlgear.

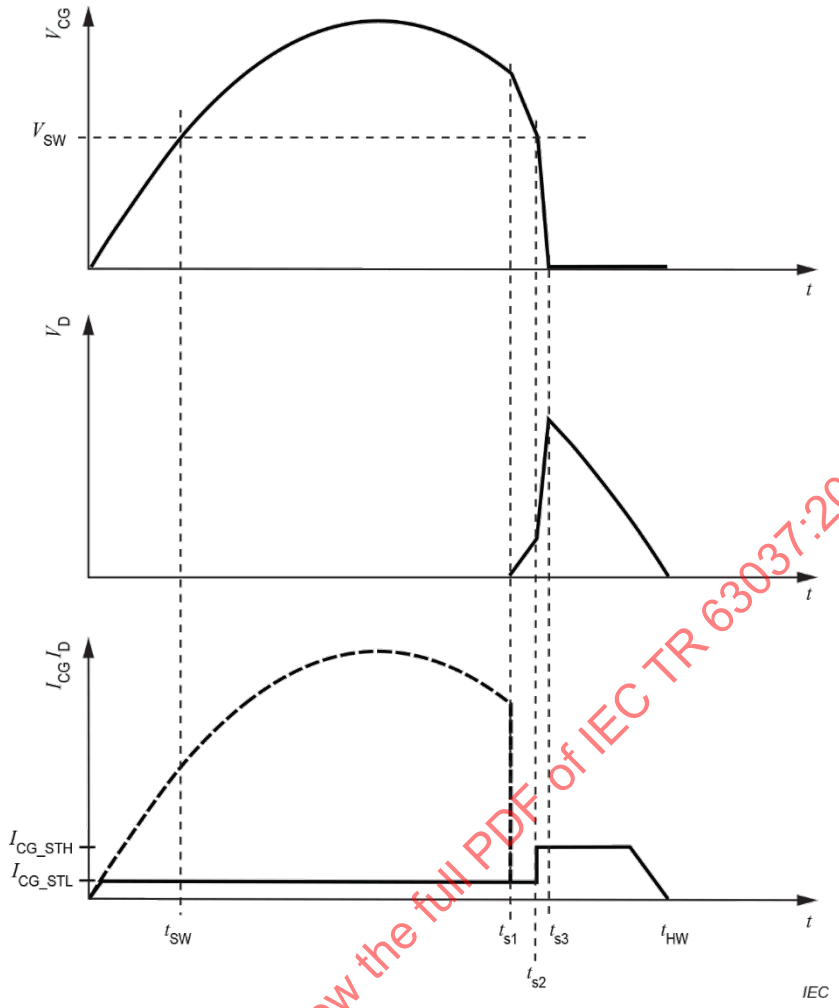

Figure 3 – Timing trailing edge dimming method

7.2.3.2 Electrical characteristics during the conducting period

The conducting period starts at the zero crossing of the mains and ends at time t_{s1} when the timing element of the phase-cut dimmer deactivates its power switch and the impedance of the phase-cut dimmer Z_D increases towards Z_{D_max}.

During the conducting period, the controlgear should comply with the electrical characteristics listed in Table 12.

During this period, the phase-cut dimmer continuously applies full power to the controlgear. Therefore, the impedance Z_D of the phase-cut dimmer remains continuously at its minimum value Z_{D_min}, independently from the current $I_D = I_{CG}$.

The impedance Z_D of the phase-cut dimmer is Z_{D_min} when the voltage $V_D(t)$ across the phase-cut dimmer is less than $0{,}1 \cdot V_M(t)$ during the entire conduction period.

Due to the low impedance of the phase-cut dimmer during the conducting period, the input voltage of the controlgear is almost equal to the instantaneous value of the mains voltage.

From the zero crossing of the mains to time t_{s1}, the controlgear should provide a current path with a minimum current-carrying capability of I_{CG_STL} as listed in Table 12.

Since the current I_{CG_STL} is based on nominal data of a controlgear, a factor of 0,7 is inserted to account for the fact that the current drawn by the controlgear will have some distortion or

displacement and may not be a perfect sine-wave or rectangular shape. Therefore the factor 0,7 introduces some margin for this. Additionally, in accordance with this document, the controlgear may not operate with its nominal wattage even at the maximum conduction angle.

Table 12 – Nominal mains voltage from 100 V to 277 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current, voltage and impedance limits
0 to t_{s1}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω V_{CG} > 6 V: $I_{CG}(t) = I_{CG\_STL} \geq (0{,}7 \cdot P_{CG})/ V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0{,}7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$

7.2.3.3 Electrical characteristics during the transition from the conducting to the non-conducting period

The transition from the conducting to the non-conducting state of the phase-cut dimmer starts at time t_{s1} and ends at time t_{s3}.

At time t_{s1}, the impedance Z_D of the phase-cut dimmer starts to increase towards Z_{D_max}. From time t_{s1} to t_{s2}, the phase-cut dimmer limits the current I_D.

The minimum value of $t_t = t_{s2} - t_{s1}$ should be as listed in Tables 13 to 17.

Since the controlgear provides a minimum current-carrying capability of I_{CG_STL} (see Tables 13 to 17), the voltage across the input terminals of the controlgear decreases towards zero and falls below the voltage V_{SW} at t_{s2} (see Figure 3).

NOTE 1 The minimum current-carrying capability ensures that parasitic capacities of the installation, the active capacity C_f between the terminals of the phase-cut dimmer (see Figure 3) and a capacitor that might be assembled inside the controlgear and which is connected directly with the mains terminals of the controlgear is discharged in a reasonable time to allow the phase-cut dimmer to supply itself sufficiently.

NOTE 2 The ratio between the values of the period t_{s2} to t_{HW} as given in Tables 13 to 17 for the different mains voltages is proportional to the ratio of the relevant mains voltages. The values of I_{CG_STH} scale inversely with the mains voltage. The value of V_{SW} scales directly with the mains voltage. The value of I_{D_nc} is always 10 % lower than the relevant I_{CG_STH}.

The slew rate SR should be calculated based on the measurement of the voltage slope of V_{CG} by measuring the time (dt) between $V_{CG} = 0{,}8 \cdot V_{CG}(t_{s1})$ and $V_{CG} = V_{SW}$ and by calculating the differential voltage d$V_{CG} = 0{,}8 \cdot V_{CG}(t_{s1}) - V_{SW}$.

When the voltage V_{CG} falls below V_{SW} (time t_{s2}), the controlgear should provide a minimum current-carrying capability of I_{CG_STH} as listed in Tables 13 to 17.

NOTE 3 The values of V_{SW} and I_{CG_STH} are selected to achieve a good compromise between the ability for the phase-cut dimmer to supply itself on one side and the appearing power loss in the controlgear on the other side.

NOTE 4 t_{s2} is defined by the time at which V_{CG} falls below V_{SW}. V_{CG} and I_D can be measured simultaneously with a 4-channel oscilloscope, and the value of I_D between t_{s1} and t_{s2} can be determined. The break in slope of V_D at t_{s2} (if such a break in slope exists) is not a criteria to define t_{s2}.

Table 13 – Nominal mains voltage 100 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0,7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0,7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0,09$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0,108$ V/µs (60 Hz) when the controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: $v_{CG} \leq 1\,200\ \Omega$ 6 V < V_{CG} < v_{SW} = 22 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 13,8$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 165,6$ mA

Table 14 – Nominal mains voltage 120 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0,7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0,7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0,010\,5$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0,126$ V/µs (60 Hz) when the controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: $Z_{CG} \leq 1\,200\ \Omega$ 6 V < V_{CG} < V_{SW} = 26 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 11,5$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq 138$ mA

Table 15 – Nominal mains voltage 200 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0,7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0,7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0,175$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0,210$ V/µs (60 Hz) when the controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 43 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 6,9$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq$ 82,8 mA

Table 16 – Nominal mains voltage 230 V; frequency 50 Hz or 60 Hz

Time related to previous zero crossing of mains voltage	Controlgear: current carrying capability
t_{s1} to t_{s2} $t_{s2} - t_{s1} \geq t_t$ $t_t = (1 / SR) \cdot V_M(t_{s1})$	$t = t_{s1}$: $I_{CG}(t) = I_{CG\_STL} \geq (0,7 \cdot P_{CG})/V_M$ or $I_{CG}(t) = I_{CG\_STL}(t) \geq (0,7 \cdot V_{CG}(t))/(V_M^2/P_{CG})$ $t_{s1} < t \leq t_{s2}$: $SR = \lvert dV_{CG}/dt \rvert \geq 0,2$ V/µs (50 Hz) $SR = \lvert dV_{CG}/dt \rvert \geq 0,24$ V/µs (60 Hz) when the controlgear is supplied by a current source driving (2,8 mA · P_{CG}) / W from t_{s1} to t_{s2}.
t_{s2} to t_{HW}	0 V ≤ V_{CG} ≤ 3 V: Z_{CG} not defined 3 V < V_{CG} ≤ 6 V: Z_{CG} ≤ 1 200 Ω 6 V < V_{CG} < V_{SW} = 40 V: P_{CG} < 12 W: $I_{CG}(t) = I_{CG\_STH} \geq 6$ mA/W · P_{CG} $P_{CG} \geq 12$ W: $I_{CG}(t) = I_{CG\_STH} \geq$ 72 mA