IEC TR 62878-2-8

Edition 1.0 2021-07

TECHNICAL REPORT

Device embedding assembly technology – Part 2-8: Guidelines – Warpage control of active device embedded substrate

IEC TR 62878-2-8:2021-07(en)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

ICS 31.180; 31.190

ISBN 978-2-8322-9953-1

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-8: Guidelines – Warpage control of active device embedded substrate

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IEC TR 62878-2-8, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
91/1649/DTR	91/1721/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-8: Guidelines – Warpage control of active device embedded substrate

1 Scope

This part of IEC 62878 describes a warpage control of active device embedded substrate along with parameters for determining warpage, which are useful during package assembly. Warpage results are explained using warpage driving force, resistance and neutral axis, for typical die embedded substrate, where the discrete active dies are placed in the core of substrate and interconnected to the substrate by direct Cu bonding. The same principles are applicable in other device embedded substrates. Even though the detailed structure of other device embedded substrates might be different, the origin and determination of the parameters of warpage are the same and thus the purpose of this report is to help engineers improve the warpage behaviours of their products by applying this principle.

2 Normative references

IEC 60194 (all parts), *Printed boards design, manufacture and assembly – Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
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3.1
warpage
deviation from uniform flatness of the substrate for the range of thermal conditions experienced during the package to board assembly

Note 1 to entry: Warpage during board assembly can cause the device terminals to have open or short circuit connections after the reflow soldering operation. Certain package types, such as BGAs (ball grid arrays), have been found to be more susceptible to component warpage [1][1].

Note 2 to entry: Package warpage depends on many factors including CTE mismatch between device constituents, assembly process, package design geometries, top and embedded die, substrate, etc. (x, y, & z). In addition, it can be related with use of IHS (integrated heat spreader), stiffener, or overmold (geometries and material choices include sealant/adhesives used), and other technology aspects of embedded design, embedded and external caps, use of GaA vs. SiO2, etc.

[1] Numbers in square brackets refer to the Bibliography.

4 Warpage driving force and resistance

4.1 General

Warpage of device embedded substrate can be related with many parameters which include properties, thickness, Cu ratio, routing and process history. The dimensions of embedded die including thickness, affect the warpage as well. Process history adds some variations by altering the material properties, and the residual stresses of constituents or interfaces between constituents. These parameters can be categorized into two groups, driving force and resistance.

4.2 Warpage driving force

The degree of warpage of device embedded substrate is proportional to the difference in CTE(coefficient of thermal expansion) of the materials and also to the temperature increase.

$$W \propto \Delta\alpha\Delta T$$

W: the degree of the warpage;

$\Delta\alpha$: the difference between the materials CTEs;

ΔT: the amount of the temperature change.

The direction of warpage can be defined by the direction of temperature change as Figure 1.

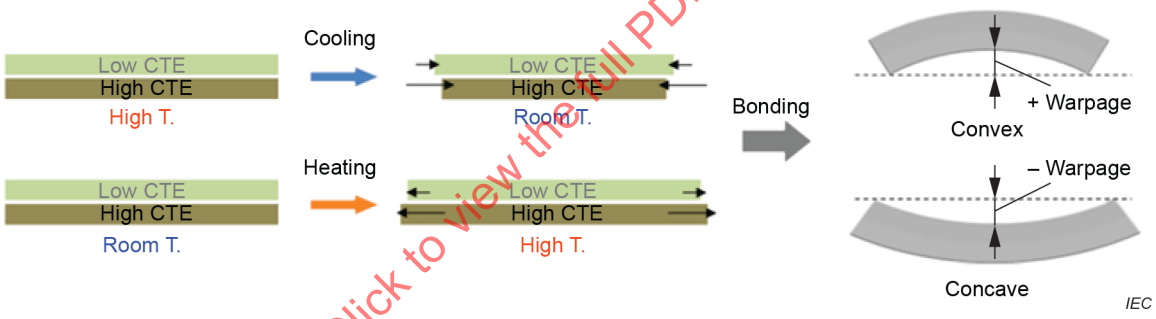
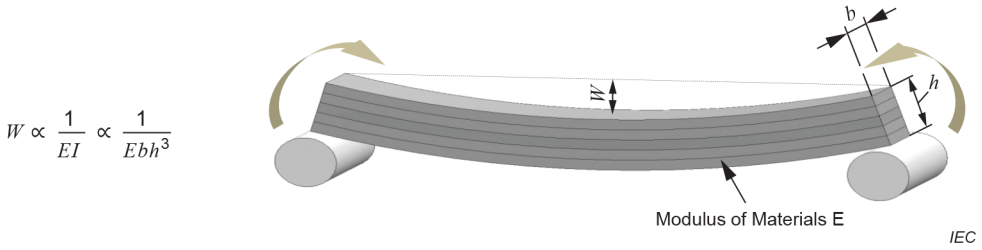


Figure 1 – Warpage behaviour of device embedded substrate during heating and cooling

4.3 Warpage resistance

Device embedded substrate warpage is inversely proportional to flexural rigidity, which is the Young's Modulus multiplied by geometrical moment of inertia. In case of the panel with fixed width of the beam (b), the warpage is proportional to the inverse of the panel thickness to the third power as shown in Figure 2.



Key

W: amount of the warpage;

E: Young's modulus;

I: geometrical moment of inertia;

EI: flexural rigidity;

b: width of the beam;

h: height of the beam.

Figure 2 – Relationship between warpage and rigidity

4.4 Determining parameters

Driving force for Warpage is the CTE mismatch between dielectric materials, circuit layer, embedded device, and solder resistor. While driving force is mainly related to CTE of each layer, the resistance to warpage is heavily dependent on the dimensions of each layer, the height of Si die and the ratio of the die to the panel area. The parameters determining warpage and their relationship are illustrated in Figure 3.

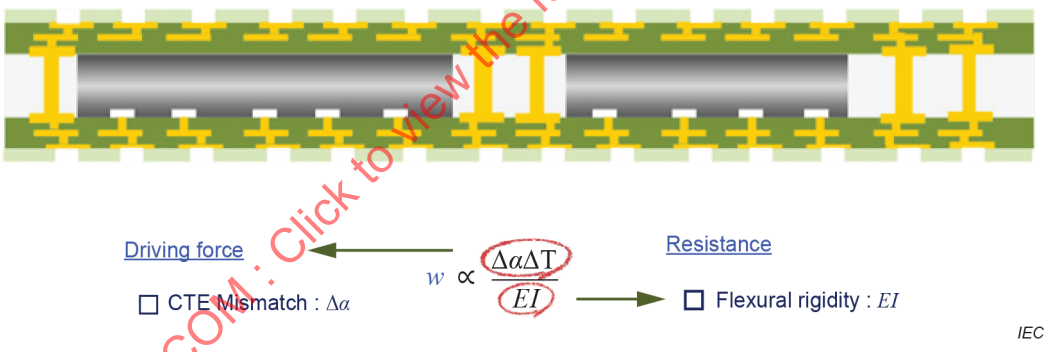
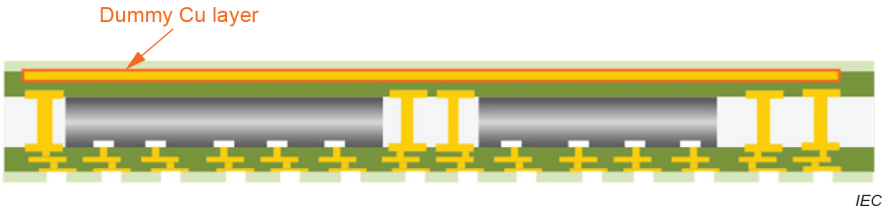
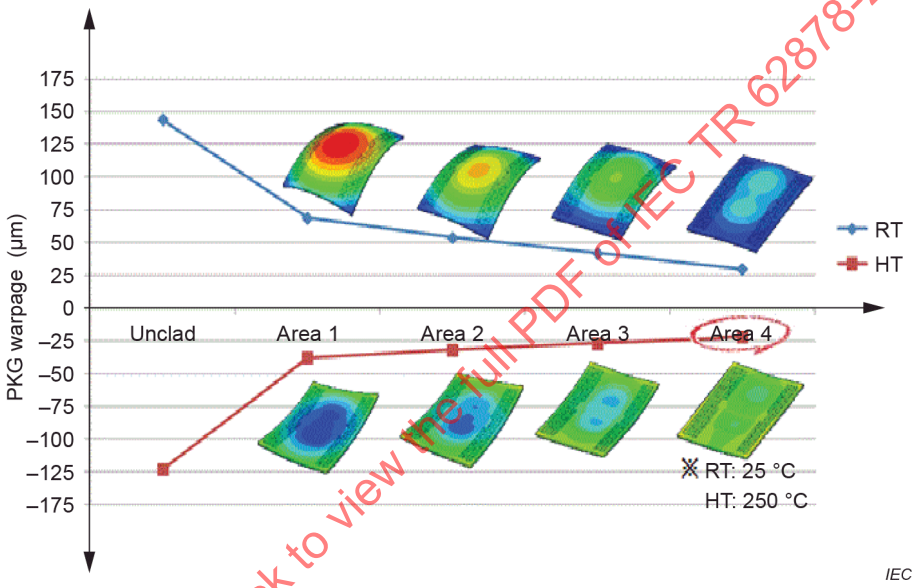


Figure 3 – Parameters determining warpage

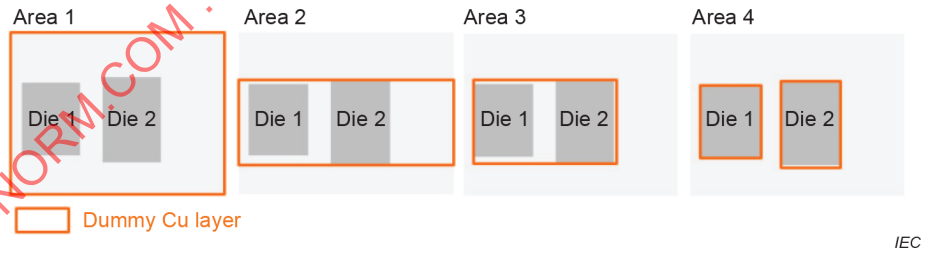
(a) Die embedded substrate without dummy Cu layer



(b) Die embedded substrate with dummy Cu layer



(c) Effects of dummy Cu design on warpage (simulation)



(d) Placements of dummy Cu layer

Figure 4 – Effects of dummy Cu design on warpage

A typical example is included in Figure 4, which shows the CTE mismatch. Without upper Cu layer, the CTE of lower part near dies including multi layers can be much higher than that of the upper part consisting of only thin dielectrics layer because the CTE of die is normally much lower. In that case the neutral axis is shifted to lower direction, which results in the high convex warpage at room temperature and the high concave warpage at high temperature. If the dummy Cu layer is added on the area above the dies, the warpage can be drastically reduced. The greatest reduction in warpage occurs where the dummy Cu layers are confined to the same areas as the die, because the warpage is mainly generated by the CTE difference between Si die and organic substrate

5 Guideline for warpage of active device embedded substrate

5.1 General

Active device embedded package, which is mainly composed of active device embedded substrate, is typically mounted on circuit board for mobile applications. If the package has significantly higher warpage, some failures will occur during assembly processes.

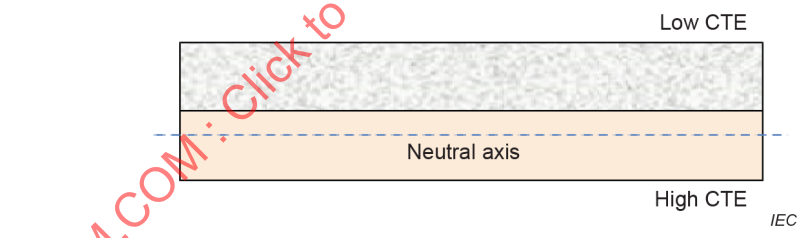
5.2 Rigidity

As described before, the degree of warpage is determined by the driving and resistance forces. Therefore, it is helpful to consider warpage of active device embedded substrate by considering their flexural rigidity and CTE balance along the z direction of the substrate.

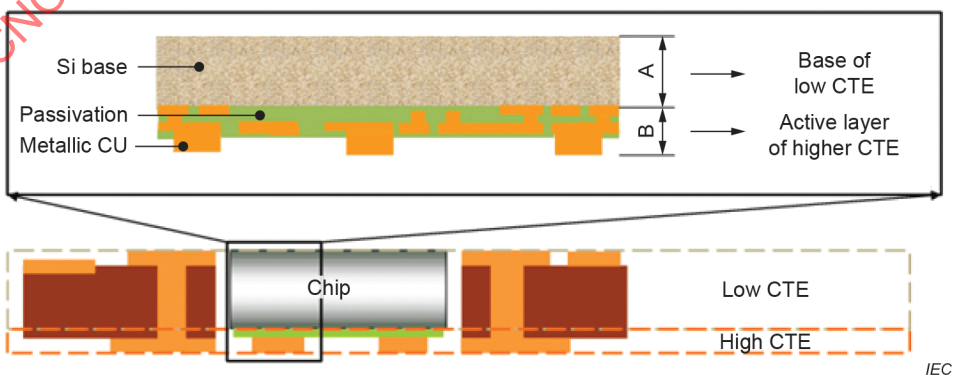
In case of the substrate with high flexural rigidity where the die portion and/or die thickness is high (typically in case of the die thickness above 200 um), the warpage sensitivity (the difference of warpage between low and high temperatures during heating and cooling) is very low, which can results in low warpage. On the contrary, in case of the substrate with low flexural rigidity when the die portion and/or die thickness is low (typically in case of the die thickness below 100 um), the warpage sensitivity is very high and if flexural rigidity is extremely low, the warpage may be much higher and it may not be easy to predict the warpage behaviour. Therefore, experimental verification becomes very important.

5.3 Neutral axis

The term of driving force can be best determined by understanding the location of neutral axis. This can be calculated from CTE and 3-dimensional distribution of substrate constituents as shown in Figure 5. The neutral axis is the plane where the stress causing the bending behaviour is zero and simply describes the balance of CTE along the z- axis of embedded substrate. If the neutral axis is placed above the central position of the embedded substrate, the CTE of the bottom part of embedded substrate is lower than the lower part of the substrate, which will result in the concave type of bending at high temperature upon heating.



(a) Neutral axis for die embedded substrate

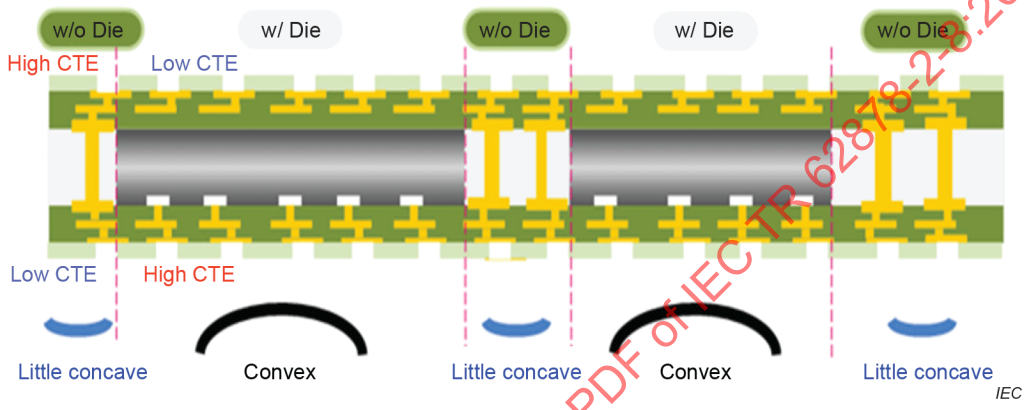


(b) An example of the case (a)

Figure 5 – Neutral axis of device embedded substrate

5.4 Typical example of low rigidity case

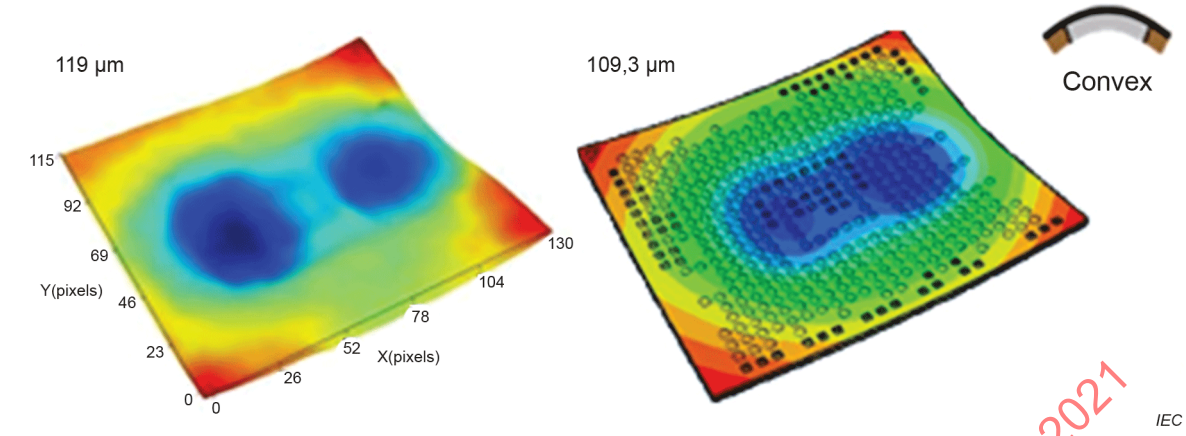
The cross-sectional view shown in Figure 6, shows a case of the active device embedded substrate, where multiple dies are embedded. The stack-up of embedded substrate results in a lower CTE on the upper side of die compared with the lower side of die. The reason is that the lower (active) part of die has higher CTE than the upper part. Therefore, an overall CTE of the upper part of die embedded substrate is lower than that of the bottom part even though the CTE balance is reversed for an unembedded substrate. The measured and the simulated warpages are shown in Figure 7. These were obtained for a thin substrate with thin die (Die thickness is 90 um and the total thickness is 220 um). The warpage was measured by means of shadow moiré [2], [3], [4] and the simulation was undertaken using FEM (Finite element model). The difference between the warpage at room temperature and the high temperature is greater than 200 um, which may be sufficient to cause failures during assembly.



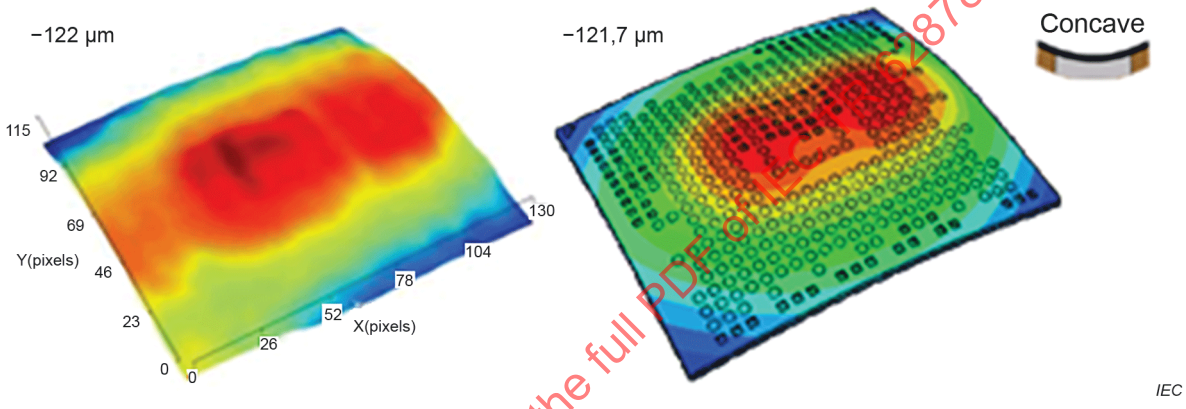
Substrate size: 11,5 × 13 mm^2; die size: 4,7 × 4,2 mm^2, 3,2 × 5,2 mm^2.

Total thickness: 220 um; die thickness: 90 um.

Figure 6 – Warpage behaviour of active device embedded substrate during heating and cooling



(a) Measured (left) and simulated (right) warpage results at 25°C

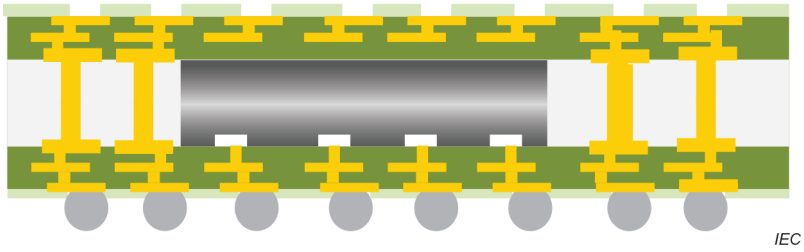


(b) Measured (left) and simulated (right) warpage results at 250°C

Figure 7 – Measured and simulated warpage results of die embedded substrates with low rigidity

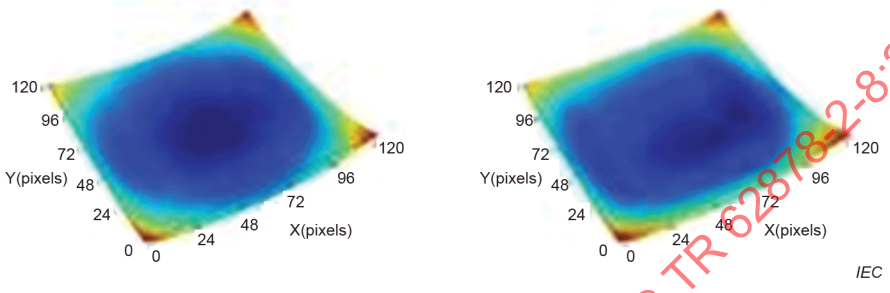
5.5 Typical example of high rigidity case

Figure 8 shows a high rigidity case where the die thickness and area ratio are high, and the resultant structure exhibits a very low level of warpage. The warpage can be drastically decreased as the thickness of die is increased, as shown in Figure 9.



PKG size: 12 × 12 mm2, total thickness: 490 um, die thickness 350 um

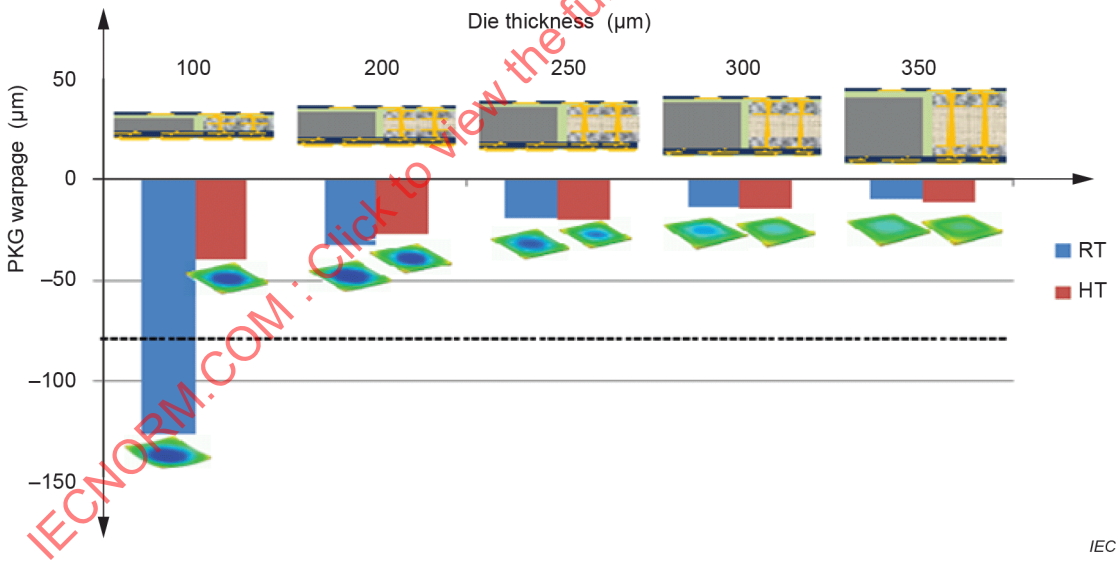
(a) Structure of die embedded package with high rigidity



NOTE The comparison between "high" and "low" rigidity examples cannot be compared directly as they are different designs.

(b) Low warpages (<10 um) of die embedded package at 25°C (left) and 250°C (right)

Figure 8 – Structure of die embedded package with high rigidity



R.T.: 25°C and H.T.: 250°C

Figure 9 – Simulated results on effect of die thickness on die embedded package warpage