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TECHNICAL REPORT

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AMENDMENT 1

High-voltage switchgear and controlgear – Part 306: Guide to IEC 62271-100, IEC 62271-1 and other IEC standards related to alternating current circuit-breakers

IEC TR 62271-306:2012-12/AMD1:2018-08(en)

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FOREWORD

This amendment has been prepared by subcommittee 17A: Switching devices, of IEC technical committee 17: High-voltage switchgear and controlgear.

The text of this amendment is based on the following documents:

DTR	Report on voting
17A/1161/DTR	17A/1169/RVDTR

Full information on the voting for the approval of this amendment can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this amendment and the base publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION to the Amendment

At the SC 17A meeting held in Delft (NL) in 2013, the decision was made form a new maintenance team (MT 57) with the task to amend/revise IEC 62271-306. The objective was to update the publication to amendment 2 of IEC 62271-100. Together with MT 34 (IEC 62271-1), MT 36 (IEC 62271-100) and MT 28 (IEC 62271-101) the decision was made to move some of the informative annexes to IEC 62271-306.

This amendment includes the following significant technical changes.

– Annex G of IEC 62271-1:2007 has been included;
– Annexes E, G, H, J, L and Q of IEC 62271-1:2007 have been included;
– I.2 of IEC 62271-100:2008 + A1:2012 has been included;
– Informative parts of Annex O of IEC 62271-100:2008 have been included;
– Former Clause 14 has been added to Clause 13;

– Clause 14 now has heading "Synthetic making and breaking tests". This clause contains annexes A, B, C, D and G of IEC 62271-101;
– Clause 9 has been restructured;
– 16.4 (No-load transformer switching) has been rewritten;
– Annex B has been expanded to include information about fully compensated transmission lines and cables;
– Annex D has been rewritten.

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1.2 Normative references

Replace the existing references to IEC 62271-100, IEC 62271-101 and IEC 62271-110 by the following new references:

IEC 62271-100:2008, *High-voltage switchgear and controlgear – Part 100: Alternating current circuit-breakers*
Amendment 1:2012
Amendment 2:2017

IEC 62271-101:2012, *High-voltage switchgear and controlgear – Part 101: Synthetic testing*

IEC 62271-110:2012, *High-voltage switchgear and controlgear – Part 110: Inductive load switching*

3.3 Capacitive current switching class C1 and C2

Replace the existing text of this subclause by the following new text:

Two classes are defined:

– Class C1: low probability of restrike;
– Class C2: very low probability of restrike.

IEC 60056 contained a definition of the term "restrike-free circuit-breaker". This definition was removed when the capacitive current switching requirements and test procedures were revised. The revised requirements and test procedures were first published in the first edition of IEC 62271-100 (published in 2001). The reason why the term "restrike-free circuit-breaker" was deleted from the standard was because it did not correspond to a physical reality.

The first edition of IEC 62271-100 introduced the term "restrike probability" during the type tests, corresponding to a certain probability of restrike in service, which depends on several parameters (see 9.4.6). For this reason, the term cannot be quantified in service.

The main differences in restrike performance between class C1 and C2 type tests are the number of tests shots and the allowable number of restrikes. Class C2 tests are performed on a pre-conditioned circuit-breaker. Pre-conditioning is done performing 3 breaking operations at 60 % of the rated short-circuit current. The pre-conditioning was derived based on CIGRE statistics and is considered to create interrupter wear that is broadly representative of long term service conditions.

The choice for the user between class C1 and C2 depends on:

– the service conditions;

– the operating frequency;

– the consequences of a restrike to the circuit-breaker or to the system.

Class C1 is acceptable for medium-voltage circuit-breakers and circuit-breakers applied for infrequent switching of transmission lines and cables.

Class C2 is recommended for capacitor bank circuit-breakers and those used on frequently switched transmission lines and cables.

The above given conditions are essential when choosing the circuit-breaker for a capacitive switching application, the needed performance class and the voltage factor should be known and demonstrated by the relevant type test. It is important to note that the performance class may vary for different capacitive current switching applications. For example, a circuit-breaker used to switch an overhead line may be tested for class C1 whereas the same circuit-breaker is tested in accordance with class C2 for capacitor bank switching.

6.1.3.1 TRVs for terminal faults

Delete the penultimate paragraph of this subclause.

Add, at the end of the existing 6.3, the following new subclauses, figures and tables.

6.4 General considerations regarding TRV

6.4.1 General

The purpose of 6.4 is to provide a background framework for some of the TRV requirements.

6.4.2 TRV waveshapes

In some cases, particularly in systems with a voltage 100 kV and above, and where the short-circuit currents are relatively large in relation to the maximum short-circuit current at the point under consideration, the transient recovery voltage contains first a period of high rate of rise, followed by a later period of lower rate of rise. This waveshape is generally adequately represented by an envelope consisting of three line segments defined by means of four parameters (see Figure 96).

The TRVs for terminal fault test-duties T100 and T60 represent cases where the major contribution of fault current is over transmission lines from multiple sources. The TRVs consist of the initial component at the fault bus and the additional component due to later arriving multiple reflected waves at the fault bus. The TRVs are overdamped (exponential) owing to the effect of the surge impedances of the lines and represented by four parameters to cover both of the above components. For terminal fault test duties T30 and T10 TRV cases, the fault current is from a single source and damping is determined by the involved circuit elements. The TRVs are underdamped (oscillatory) and thus represented by two parameters.

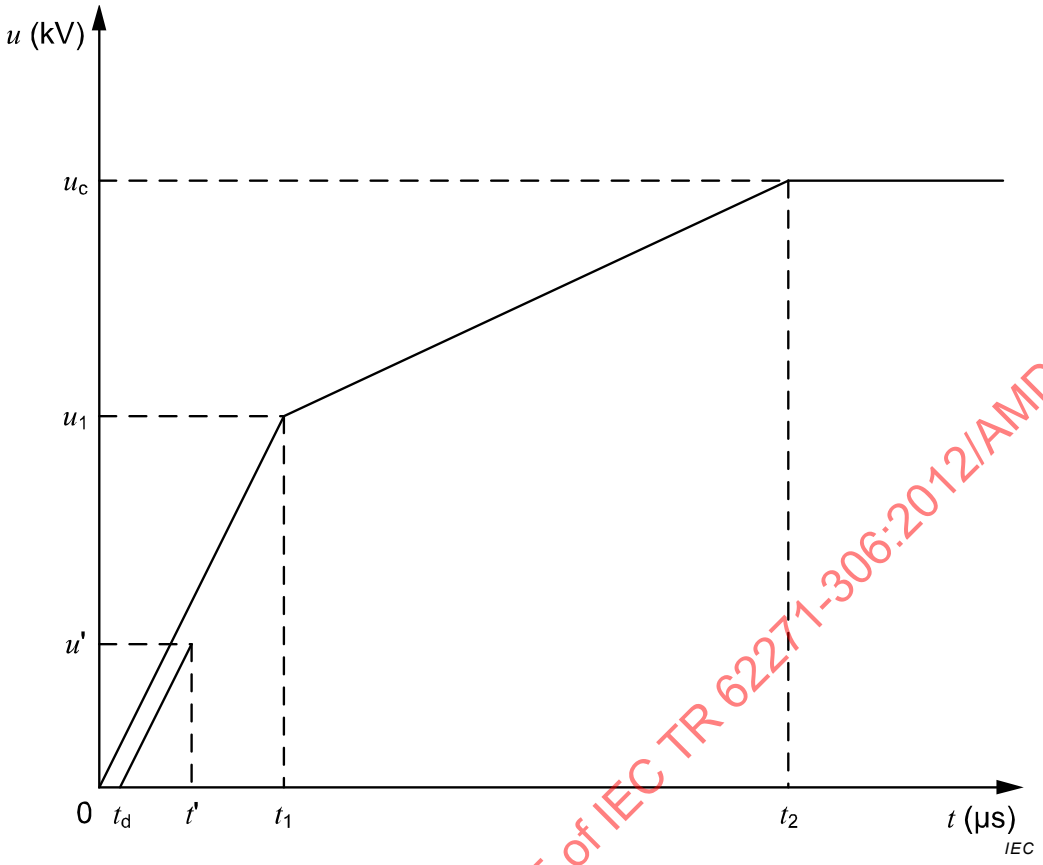


Figure 96 – Representation of a four-parameter TRV and a delay line

In other cases, particularly in systems with a voltage less than 100 kV, or in systems with a voltage greater than 100 kV in conditions where the short-circuit currents are relatively small in relation to the maximum short-circuit currents limited by transformers, the transient recovery voltage approximates to a damped single frequency oscillation. This waveshape is adequately represented by an envelope consisting of two line segments defined by means of two parameters (see Figure 97).

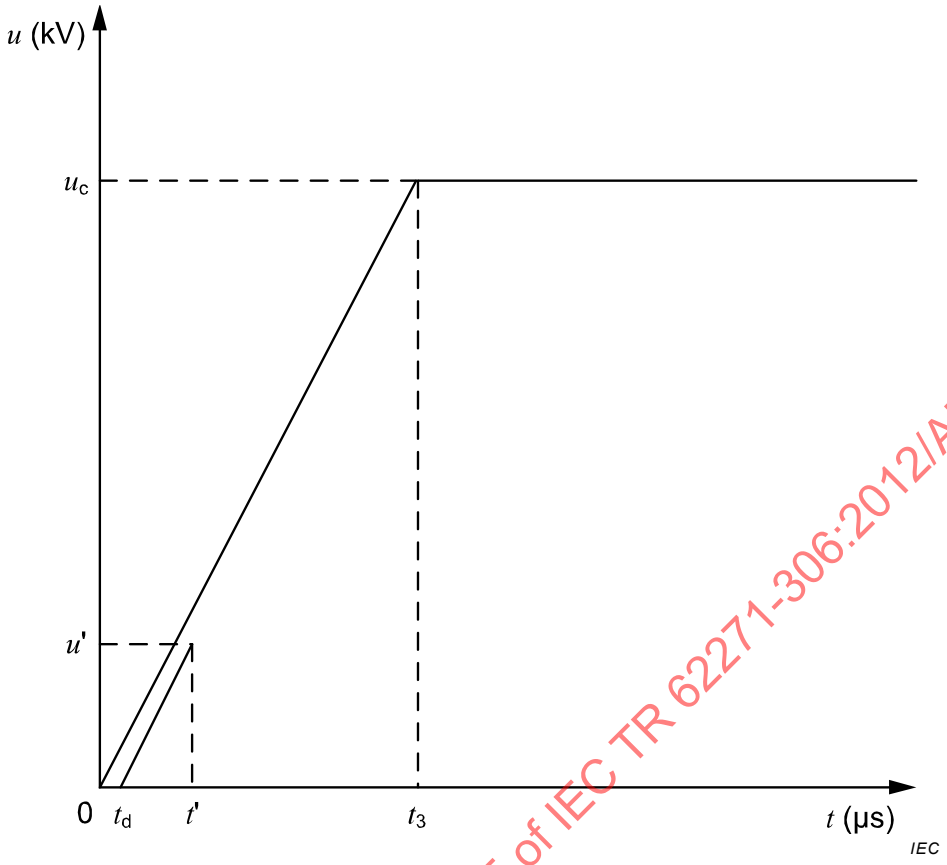


Figure 97 – Representation of a specified TRV by a two-parameter reference line and a delay line

Such a representation in terms of two parameters is a special case of representation in terms of four parameters.

The influence of local capacitance on the source side of the circuit-breaker produces a slower rate of rise of the voltage during the first few microseconds of the TRV. This is taken into account by introducing a time delay.

6.4.3 Earthing of the system

The system may be earthed in different ways depending on system voltage and application. The following definitions are used (Clause 3 of IEC 62271-100:2008 and as noted below):

solidly earthed (neutral) system (3.1.106 of IEC 62271-100:2008)
a system whose neutral point(s) is (are) directly earthed

[SOURCE: IEC 60050-601:1985, 601-02-25]

effectively earthed neutral system (3.1.128 of IEC 62271-100:2008)
system earthed through a sufficiently low impedance such that for all system conditions the ratio of the zero-sequence reactance to the positive-sequence reactance (X_0/X_1) is positive and less than three, and the ratio of the zero-sequence resistance to the positive-sequence reactance (R_0/X_1) is positive and less than one. Normally such systems are solidly earthed (neutral) systems or low impedance earthed (neutral) systems.

Note 1 to entry: For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

non-effectively earthed neutral system (3.1.129 of IEC 62271-100:2008)
system other than effectively earthed neutral system, not meeting the conditions given in 3.1.128 of IEC 62271-100:2008. Normally such systems are isolated neutral systems, high impedance earthed (neutral) systems or resonant earthed (neutral) systems

Note 1 to entry: For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

6.4.4 Power frequency recovery voltage and first-pole-to-clear factor

6.4.4.1 General

The first-pole-to-clear factor (k_{pp}) is a function of the earthing arrangements of the system. As defined in 3.7.152 of IEC 62271-100:2008, it is the ratio of the power frequency voltage across the interrupting pole before current interruption in the other poles, to the power frequency voltage occurring across the pole or poles after interruption in all three poles. For non-effectively earthed neutral systems, this ratio is or tends towards 1,5. For rated voltages less than 170 kV, such systems are quite common, particular within Europe and Japan.

For effectively earthed neutral systems, the realistic and practical value is dependent upon the sequence impedances of the actual earth paths from the location of the fault to the various system neutral points (the ratio X_0/X_1). The value used in IEC 62271-100 is taken to be ≤ 3 (see Equation (144)). The X_0/X_1 value is a standard value confirmed by system studies of various networks. Hence, for rating purposes, IEC 62271-100 considers two values for the three-phase short-circuit condition. These are adequate for the many, different, system earthing arrangements:

a) the non-effectively earthed, to cover all unearthed systems and those with some deliberate additional impedance in the neutral system. A standardised value for k_{pp} of 1,5 is used for all such systems;

b) all effectively earthed systems where it is accepted that some impedance exists. For standardization purposes for power systems operating at 800 kV and below the value for k_{pp} used is 1,3. For ultra-high-voltage (UHV) power systems operating above 800 kV, k_{pp} is 1,2 based on an X_0/X_1 ratio of 2.

For single-phase-to-earth faults in solidly or effectively earthed neutral systems, the pole factor k_{pp} is 1,0.

At transmission voltages, there has been an increase in interconnection and transformation, particularly in major urban systems. The high number of transformer neutrals connected effectively to earth causes the value of 1,3 to be questioned. Although this has been considered, the text of IEC 62271-100 does not take these developments into account. It is important for users with such systems to note that as k_{pp} decreases towards unity the value of the second-pole-to-clear factor will fall. In addition, the value of the phase currents will change. The three phases become three independent single-phases each with k_{pp} approaching 1,0. In general the users of such systems are aware of this possibility and of the need to consider the actual system conditions when assessing the suitability of their specified requirements and the test evidence they are offered against these.

For rated voltages higher than 800 kV, systems are characterized by long transmission lines and large transformers that contribute a relatively large part of the total short-circuit current. The first-pole-to-clear factor is function of the X_0/X_1 ratio that is in this case equal to or lower than 2,0, as a consequence k_{pp} is equal to or less than 1,2 and has been standardized to 1,2.

Where the ratio of three-phase to single-phase earth fault current is 1,0, k_{pp} is also 1,0. However, although this is normally assumed to be adequately covered by the use of the three-phase requirements and the associated k_{pp} of 1,2 or 1,3, it is important that evidence is provided to demonstrate the extended arc condition of the single-phase fault. In accordance with IEC 62271-100, a full extinguishing window shall be demonstrated.

It should be noted that in accordance with 6.108 of IEC 62271-100:2008, specific recovery voltage conditions are required to demonstrate the ability of a circuit-breaker to clear double earth faults.

Regarding earthing of the test circuit, reference is made to 6.103.3 of IEC 62271-100:2008.

6.4.4.2 Equations for the first, second and third-pole-to-clear factors

The equation for the first-pole-to-clear factor is:

$$k_{pp} = \frac{3X_0}{X_1 + 2X_0} \quad (144)$$

where X_0 is the zero sequence, and X_1 the positive sequence reactance of the system. Table 39 gives the k_{pp} values for various earthing arrangements based on the definitions given in 6.4.1.

Table 39 – First-pole-to-clear factors k_{pp}

Earthing arrangement	X_0/X_1	k_{pp}	System voltage
Solidly earthed	1	1	All
Effectively earthed	2	1,2	> 800 kV
Effectively earthed	3	1,3	≤ 800 kV
Non-effectively earthed	∞	1,5	≤ 170 kV
NOTE Calculation of k_{pp} for the effectively earthed case (X_0/X_1 = 3) gives k_{pp} = 1,286 which is then rounded to 1,3.			

Following interruption of the first pole, the remaining two phases continue to conduct fault current.

In systems with non-effectively earthed neutrals the second and third poles interrupt in series under the phase-to-phase voltage so that for the second and third pole,

$$k_p = \frac{\sqrt{3}}{2},$$

where k_p is the pole-to-clear factor of the individual poles.

In systems with effectively earthed neutrals the second pole clears with a pole-to-clear factor of,

$$k_p = \frac{\sqrt{3(X_0^2 + X_0X_1 + X_1^2)}}{X_0 + 2X_1} \quad (145)$$

NOTE In Equations (144) and (145) the resistances are neglected.

Equation (145) can be expressed as a function of the ratio $\alpha = X_0/X_1$:

$$k_p = \frac{\sqrt{3}\sqrt{\alpha^2 + \alpha + 1}}{2 + \alpha}$$

For the third-pole-to-clear in an effectively earthed system k_p = 1. Table 40 gives k_p for each clearing pole as a function of X_0/X_1 as appropriate.

Table 40 – Pole-to-clear factors for each clearing pole

X_0/X_1	Pole-to-clear factor		
Ratio	**First**	**Second**	**Third**
1	1,0	1,00	1,0
2	1,2	1,15	1,0
3	1,3	1,26*	1,0
∞	1,5	0,866	0,866
* Equation (145) assumes that system impedances are inductances only.			

The respective multiplying factors for the peak value of the TRV (u_c) are given in Table 6 of IEC 62271-100:2008. It is important to note that the amplitude factor is the same for each pole. The multiplying factors are as applied to the power frequency voltages.

6.4.4.3 Standardised values for the second- and third- pole-to-clear factors

As discussed above, IEC 62271-100 has standardised values for the second and third-pole to clear factors for three-phase testing. Subclause 13.3 deals with this topic in relation to demonstration of arcing times for these poles and the appropriate pole factors relevant to each opening pole. It is important to note that on systems where the neutral earthing is solid, both the first-pole-to-clear factor of 1,3 and the values provided above for second pole-to-clear factors are lower. This is likely to be a rare occurrence, generally associated with urban systems where there are numerous effectively earthed transformers in close proximity. Where such differences are significant, the user is generally aware that it may be necessary to specify system-specific requirements and tests (e.g. extinguishing window and single-phase short-circuit current).

Circuit-breakers are rated on the basis of their ability to interrupt a three-phase to earth fault in either an effectively or non-effectively earthed neutral systems. Taking the former case, the three poles clear in sequence:

- The first pole clears with k_{pp} given by Equation (144) leaving a two-phase to earth fault.
- The second pole clears with k_p given by Equation (145) leaving a single-phase to earth fault. For the case of a two-phase to earth, the k_{pp} for the first clearing pole is also given by Equation (145).
- Third pole with k_p = 1 which is also applicable to the single-phase to earth fault case.

Similar logic can be applied to faults in non-effectively earthed neutral systems. A summary of the pole-to-clear factors for the different fault cases is given in Table 41.

Table 41 – Pole-to-clear factors for other types of faults in non-effectively earthed neutral systems

Type of fault	First-pole-to-clear	Second-pole-to-clear	Third-pole-to-clear
Phase-to-earth	1	-	-
Two-phase not involving earth	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	-
Two-phase-to-earth	$k_p = \frac{\sqrt{3}\sqrt{\alpha^2+\alpha+1}}{2+\alpha}$	1	-
Three-phase not involving earth	1,5	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$

6.4.5 TRV characteristics

6.4.5.1 Terminal fault TRVs for rated voltages higher than 1 kV and less than 100 kV

6.4.5.1.1 General

Following the decision taken at the SC17A meeting in Beijing (CN) in October, 2002, IEC SC 17A/WG35 has prepared a proposal for the revision of TRVs for circuit-breakers rated above 1 kV and less than 100 kV.

This proposal used the input coming from former Working groups of CIGRE Study Committee A3 (Switching Equipment) that have studied the necessity to adapt the TRV requirements for circuit-breakers rated less than 100 kV. In 1983, a CIGRE SC A3 Task Force reported on Transient Recovery Voltages in Medium Voltage Networks. The results of the study have been published in Electra 88. Another CIGRE working group, WG 13.05, studied the TRVs generated by clearing transformer fed faults and transformer secondary faults. The results have been presented in Electra 102 (1985). In 1992, together with CIRED, CIGRE SC A3 created working group CC-03 to investigate again the definition of TRVs for medium voltage switchgear. The outcome of these investigations has been published in CIGRE Technical Brochure 134 (1998) and is in line with earlier studies.

The first edition of IEC 62271-100 (IEC 62271-100:2001) was amended in 2006 (Amendment 2) to include the new TRV values. The modifications can be summarized as follows:

a) In order to cover applications in all types of networks (distribution, industrial and sub-transmission) for rated voltages higher than 1 kV and less than 100 kV, and for standardization purposes, two types of systems and two classes of circuit-breakers are defined:
   - cable systems:

     cable-systems are defined in 3.1.132 of IEC 62271-100:2008;
   - line systems:

     line systems are defined in 3.1.133 of IEC 62271-100:2008;
   - Circuit-breaker class S1: circuit-breaker to be used in a cable system;
   - Circuit-breaker class S2: circuit-breaker to be used in a line system.

b) A particular test duty T30 is specified for the special case of circuit-breakers intended to be connected to a transformer with a connection of small capacitance (cable length less than 20 m), in order to verify their capability to interrupt transformer-limited faults. This is covered in Annex M of IEC 62271-100:2008.

In the general case where the capacitance of the connection is high enough, the normal test duty T30 demonstrates the capability to interrupt transformer-limited faults.

6.4.5.1.2 Terminal fault TRV for circuit-breakers in line systems

6.4.5.1.2.1 General

In North America, line systems are prevalent at 72,5 kV and below. Therefore, the TRV ratings as listed in Table 2 of ANSI C37.06-2000 were the basis to define the new Table 25 of IEC 62271-100:2008. The values for t_3 are 0,88 times the T_2 values specified in ANSI.

NOTE 1 The factor 0,88 is derived from a pure "1-cos"-waveshape multiplied with ½ amplitude factor. The standard TRV wave-shape "1-cos" in ANSI C37-06-2000 for rated voltages less than 100 kV did not coincide with the precise mathematical equation for parallel or series damped circuits, for which another ratio t_3/T_2 is applicable.

NOTE 2 TRV parameters are defined in the standard for rated voltages of 15 kV to 72,5 kV, for rated voltages less than 15 kV the TRV parameters can be derived using k_{pp} = 1,5, the values of amplitude factor, time t_3 and time delay given in 6.4.1.2.2.2, 6.4.1.2.2.3 and 6.4.1.2.2.4.

6.4.5.1.2.2 Amplitude factor

For T100, T60, T30 and T10 the following values were taken from ANSI C37.06-2000:

– 1,54 for T100;
– 1,65 for T60;
– 1,74 for T30;
– 1,8 for T10.

6.4.5.1.2.3 Time t_3

The rate-of-rise of recovery voltage (RRRV) is calculated using Equation (146),

$$\text{RRRV} = 0{,}4 U_r^{0{,}305} \tag{146}$$

Time t_3 for terminal fault is equal to $4{,}65 \times U_r^{0{,}7}$, with t_3 in µs and U_r in kV. Equation (146) was derived from the values given in Table 2 of ANSI C37.06-2000 for rated voltages 15,5 kV, 25,8 kV, 48,3 kV and 72,5 kV. The same equation is used for other rated voltages.

6.4.5.1.2.4 Time delay

The time delay in Table 25 of IEC 62271-100:2008 is derived using the following equation, t_d = 0,05 × t_3, as in the first edition of IEC 62271-100:2001 for rated voltages 48,3 kV – 52 kV and 72,5 kV. The equation has been extended to the lower rated voltages as no change in the initial part of the TRV wave-shape is expected (the initial part is exponential, even with the short line lengths that can be met in distribution and sub-transmission systems). This requirement is not judged excessive, as in the worst case (U_r = 15 kV), the time delay value of 2 µs is as specified for circuit-breakers with rated voltages higher than 72,5 kV.

It recognizes the fact that this time delay can be critical during short-line fault testing and test duty T100 with ITRV and has therefore to be taken into account. However, as shown in Tables 13 and 14 of the first edition of IEC 62271-100 published in 2001, such verification can be made when performing short-line fault tests. Therefore, as it is already the case for rated voltages higher than 38 kV, it is allowed to have a longer time delay during testing of T100, up to 0,15 × t_3, provided that short-line fault tests are performed. This possibility is indicated in Table 25 of IEC 62271-100:2008.

6.4.5.1.3 Terminal fault TRV for circuit-breakers in cable systems

6.4.5.1.3.1 Amplitude factor

For T60, the value of 1,5 in the first edition of IEC 62271-100:2001 is kept, due to the positive experience obtained.

For T30 and T10, the amplitude factor has been raised from 1,5 to respectively 1,6 and 1,7, as the contribution to TRV comes mainly from the voltage variation across transformer(s), which has low damping; this combined with source voltage results in a TRV with a relatively high amplitude factor.

For T100, the value of 1,4 in the first edition of IEC 62271-100 published in 2001 is retained owing to the positive experience with past editions of this standard.

6.4.5.1.3.2 Time delay

The time delay t_d is as given in the first edition of IEC 62271-100 published in 2001 for rated voltages less than 52 kV, t_d = 0,15 × t_3. The equation is generalized to all cable systems (rated voltage less than 100 kV).

6.4.5.1.4 Terminal fault TRV for rated voltages equal to or higher than 100 kV

6.4.5.1.4.1 Amplitude factor

The values of the amplitude factors are given in IEC 62271-100. These values were adopted into IEC 62271-100 as a result of system studies and generally remain acceptable.

6.4.5.1.4.2 Rate-of-rise of recovery voltage and time delay

The values for the rate-of-rise-of-recovery-voltage (RRRV) for the first-pole-to-clear, and the associated time delay values, were derived from system studies, supported by system tests performed in and before the mid-1970s. The values adopted (2 kV/µs etc.) have been shown by this work to be adequate for all developed systems, and are generally acceptable for others. IEC 62271-100 gives multipliers for the RRRV for the second and third poles-to-clear. These values were derived by calculation.

6.4.5.1.5 Basis for the current TRV values of test-duty T10

Test-duty T10 is detailed in IEC 62271-100 and represents the following cases:

– a transformer limited fault condition with the circuit-breaker under consideration clearing a fault on the remote side of the transformer.

  In such circumstances, the fault current is limited by the impedance of the transformer to a value, chosen for standardization purposes, of approximately 10 %. The value of 10 % is historic, having been established from system studies and modelling using the typical impedance values of transformers of standardised ratings.

  For this duty, the fault-current is limited by the value of the impedance of the transformer. The TRV is also dominated by the transformer characteristics which give it a (1-cos) wave-shape form. The values given in IEC 62271-100 for amplitude factor, time coordinates and delay line have been established from system studies and modelling during the 1960s and before. The present values are accepted as being adequate for the vast majority of systems;

– a long line fault for circuit-breakers having a rated voltage of 245 kV and above

  For rated voltages below 245 kV, k_{pp} = 1,5 in view of the fact that the contribution of transformers to the short-circuit current is relatively larger at smaller values of the short-circuit current. Additionally, a comparatively large number of transformers having an unearthed neutral are in service in earthed neutral systems. As the damping of the TRV oscillation on a high-voltage transformer is less than in a network, an amplitude factor of

1,7 has been standardised except for line systems, with a voltage reduction across the transformer of 10 % for voltages of 100 kV and above.

Thus, the TRV peak u_c for test-duty T10 is $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ with the following parameters:

a) for rated voltages below 100 kV:
   1) for circuit-breakers in cable systems
      k_{pp} = 1,5 and k_{af} = 1,7.
   2) for circuit-breakers in line systems
      k_{pp} = 1,5 and k_{af} = 1,8.
b) for rated voltages of 100 kV up to and including 170 kV:
   k_{pp} = 1,5 and k_{af} = 0,9 × 1,7 = 1,53.
c) for rated voltages of 245 kV up to and including 800 kV:
   k_{pp} = 1,3 and k_{af} = 1,76.
d) for rated voltages above 800 kV:
   k_{pp} = 1,2 and k_{af} =1,76.

6.4.6 Short-line fault TRV

6.4.6.1 General

Short-line fault (SLF) is a mandatory duty for circuit-breakers with rated voltages 15 kV and above that are directly connected to overhead lines. As specified already in IEC 62271-100:2001 for circuit-breakers rated 48,3 kV and above, the rated short-circuit current shall be higher than 12,5 kA (i.e. $I_{sc} \geq 16$ kA).

As it is considered that there are only few line systems below 15 kV, no short-line fault breaking capability is required for rated voltages below 15 kV. In the rare cases where a circuit-breaker with a voltage rating below 15 kV is directly connected to an overhead line, no short-line fault requirement is necessary as the line contribution to the TRV would be too low to produce a significant stress.

NOTE For class S2 circuit-breakers, short-line fault test-duty L90 is not required as it would lead to an unrealistic short length of faulted line.

The short-line fault test specified is regarded as covering three-phase short-line faults as well as two-phase and single-phase faults for the following reasons:

– the representative surge impedance, seen from the terminals of the clearing pole, is such that for all cases the RRRV for all three poles to clear is covered by the specified characteristics listed in Table 8 of IEC 62271-100:2008;
– the single-phase short-line fault test, with an interrupting window of (180°−dα), covers the requirement for the multi-phase fault cases for effectively-earthed and non-effectively earthed systems;
– the withstand of the peak value of TRV during three-phase fault interruption is demonstrated by terminal fault test duty T100.

6.4.6.2 Rated voltage less than 100 kV

6.4.6.2.1 General

In IEC 62271-100:2001, short-line fault requirements have been specified for circuit-breakers with a rated voltage of 52 kV and 72,5 kV, in the range of rated voltages considered in this edition, and directly connected to overhead-lines.

In IEC 62271-100:2008, short-line fault requirements are specified for class S2 circuit-breakers with a rated voltage of 15 kV and above and directly connected (with busbars) to overhead-lines, irrespective of the type of network on the source side.

As the network and substation topology and layout for 48,3 kV is identical to those of 52 kV and 72,5 kV systems, the short-line test duty for 48,3 kV is specified in a way similar to 52 kV and 72,5 kV.

For rated voltages of 15 kV to 38 kV, the characteristics and procedure are slightly different. As normally no equipment is connected to the line side of the circuit-breaker, the line characteristics are adapted to virtually no delay capacitance: $t_{dL} < 0,1$ µs. As the line length to the fault location should correspond to realistic distances, the test duty L_{90} has been dropped and the tolerances on the line length for L_{75} have been adapted.

Time t_3 and the amplitude factor of the supply circuit is the same as for terminal fault test-duty T100.

6.4.6.2.2 Rated voltage equal to or higher than 100 kV

The amplitude factor and the inherent value of the RRRV of the supply circuit are as specified for terminal fault test duty T100. During a SLF interruption the RRRV on the supply side is equal to the inherent value of RRRV for the supply circuit multiplied by the ratio of the SLF current divided by the rated short-circuit breaking current.

6.4.7 Out-of-phase TRV

Not enough system information is available to revise TRV parameters for breaking in the out-of-phase condition. CIGRE SC A3 has been asked to investigate the system and service conditions leading to out-of-phase current clearing. Therefore, the TRVs for out-of-phase breaking are basically unchanged.

The values of t_3 for out-of-phase are in all cases two times the value for terminal fault T100.

6.4.8 TRV for series reactor fault

Due to the very small inherent capacitance of a number of current-limiting reactors, the natural frequency of transients involving these reactors can be very high. A circuit-breaker installed immediately in series with such type of reactor will face a high-frequency TRV when clearing a terminal fault (reactor at supply side of circuit-breaker) or clearing a fault behind the reactor (reactor at load side of circuit-breaker). The resulting TRV frequency generally exceeds by far the standardized TRV values.

In these cases, it is necessary to take mitigation measures, such as the application of capacitors in parallel to the reactors or connected to earth. The available mitigation measures are very effective and cost efficient [125]. It is strongly recommended to use them, unless it can be demonstrated by tests that a circuit-breaker can successfully clear faults with the required high-frequency TRV.

Considering the economical aspect as well as service experience with TRV mitigation measures, there is no need for special requirements in IEC 62271-100 for circuit-breakers for this type of application.

More information is given in IEEE Std. C37.011 [126].

6.4.9 TRV for last clearing poles / tests circuit topology

In Table 2 of IEC 62271-100:2001, multipliers for transient recovery voltage values for second and third clearing poles are given for circuit-breakers with rated voltages higher than 72,5 kV.

Under NOTE 1, it is stated that for voltages equal to or lower than 72,5 kV, the values are under consideration.

For circuit-breakers with rated voltages equal to or lower than 72,5 kV, as not enough information is available to define values other than those specified for higher rated voltages, IEC SC17A has decided during its meeting in Montreal (CA), October 2003, to extend the validity of Table 2 to all rated voltages higher than 1 kV.

6.5 Calculation of TRVs

6.5.1 General

TRV parameters are defined as a function of the rated voltage (U_r), the rated first-pole-to-clear factor (k_{pp}) and the amplitude factor (k_{af}). k_{pp} is a function of the earthing of the system neutral. The rated values of k_{pp} are:

– 1,2 for terminal fault breaking by circuit-breakers with rated voltages higher than 800 kV in effectively earthed neutral systems;

– 1,3 for terminal fault breaking by circuit-breakers for rated voltages up to and including 800 kV in effectively earthed neutral systems;

– 1,5 for terminal fault breaking by circuit-breakers for rated voltages less than 245 kV in non-effectively earthed neutral systems.

6.5.2 Rated voltages less than 100 kV

A representation by two parameters of the prospective TRV is used for all test-duties.

– For circuit-breakers in cable systems.

  The TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ where k_{af} is equal to 1,4 for test-duty T100, 1,5 for test-duty T60, 1,6 for test duty T30 and 1,7 for test duty T10, 1,25 for out-of-phase breaking.

  Time t_3 for test-duty T100 is taken from Tables 24 and 43 of IEC 62271-100:2008 with IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017. Time t_3 for test-duties T60, T30 and T10 is obtained by multiplying the time t_3 for test-duty T100 by 0,44 (for T60), 0,22 (for T30) and 0,22 (for T10).

– For circuit-breakers in line systems.

  TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ where k_{af} is equal to 1,54 for test-duty T100 and the supply side circuit for short-line fault, 1,65 for test-duty T60, 1,74 for test duty T30 and 1,8 for test duty T10, 1,25 for out-of-phase breaking.

  Time t_3 for test-duty T100 is taken from Tables 25 and 44 of IEC 62271-100:2008 with IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017. Time t_3 for test-duties T60, T30 and T10 is obtained by multiplying the time t_3 for test-duty T100 by 0,67 (for T60), 0,40 (for T30) and 0,40 (for T10).

– Time delay t_d for test-duty T100 is $0{,}15\,t_3$ for cable systems, $0{,}05\,t_3$ for line systems, $0{,}05\,t_3$ for the supply side circuit for short-line fault.

– Time delay t_d is $0{,}15\,t_3$ for test-duties T60, T30 and T10 and for out-of-phase breaking.

– Voltage $u' = u_c/3$.

– Time t' is derived from u', t_3 and t_d according to Figure 97, $t' = t_d + t_3/3$.

6.5.3 Rated voltages from 100 kV to 800 kV

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test duties L_{90} and L_{75} and for out-of-phase test duties OP1 and OP2 and by two parameters for test-duties T30 and T10.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \times \sqrt{2/3}$

– Time t_1 for terminal fault test duties is derived from u_1 and the specified value of the rate of rise u_1/t_1. For test duties OP1 and OP2, t_1 is two times t_1 for test duty T100 and the rate of rise is derived from u_1 and t_1.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{2/3}$

where k_{af} is equal to 1,4 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 0,9 × 1,7 for test-duty T10, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to $4t_1$ for test-duty T100 and for the supply side circuit for short-line fault and between t_2 (for T100) and $2t_2$ (for T100) for out-of-phase breaking. Time t_2 is equal to $6t_1$ for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of Figure 96. Time delay t_d is 2 µs for test-duty T100, between 2 µs and $0{,}3t_1$ for test-duty T60, between 2 µs and $0{,}1t_1$ for test duties OP1 and OP2. Time delay is 0,15 t_3 for test-duties T30 and T10. For the supply side circuit for short-line fault the time delay is equal to 2 µs. When short-line fault tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 6.104.5.2 to 6.104.5.5 of IEC 62271-100:2008.

– Voltage $u' = u_1/2$ for test-duties T100 and T60 and the supply side for SLF and out-of-phase breaking, and $u_c/3$ for test-duties T30 and T10.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF and out-of-phase breaking, and in accordance with Figure 96; and from u', u_c/t_3 and t_d for test-duties T30 and T10 in accordance with Figure 97.

6.5.4 Rated voltages higher than 800 kV

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test duties L_{90} and L_{75} and by two parameters for test-duties T30, T10 and for out-of-phase test duties OP1 and OP2.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \times \sqrt{2/3}$

– Time t_1 for terminal fault test duties is derived from u_1 and the specified value of the rate of rise u_1/t_1.

– Time t_3 for out-of-phase test duties OP1 and OP2 is derived from u_c and the specified value of the rate of rise.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{2/3}$

where k_{af} is equal to 1,5 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 1,76 for test-duty T10, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to 3 t_1 for test-duty T100 and for the supply side circuit for short-line fault. Time t_2 is equal to 4,5 t_1 for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of rise u_c/t_3.

– Time delay t_d is 2 µs for test-duty T100, between 2 µs and 0,3 t_1 for test-duty T60. Time delay is 0,15 t_3 for test duties T30 and T10, 0,05 t_3 for test duties OP1 and OP2. For the supply side circuit for short-line fault the time delay is equal to 2 µs. When short-line fault

tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 6.104.5.2 to 6.104.5.5.

– Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF, and $u_c/3$ for test-duties T30, T10 and out-of-phase test duties.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF, and in accordance with Figure 96; and from u', u_c/t_3 and t_d for test-duties T30, T10 and out-of-phase test duties in accordance with Figure 97.

7.1.2 Technical comment

Replace the last paragraph of this subclause by the following:

As stated in 7.1.1, short-line faults tests apply to circuit-breakers directly connected to overhead lines. Direct connection is defined as a connection between the circuit-breaker and overhead line having a capacitance less than 5 nF. A time delay of more than 2 µs is obtained when a capacitance of 5 nF is added between the circuit-breaker and a line having a surge impedance of 450 Ω ($t_d = C \times Z = 5\times10^{-9} \times 450 = 2{,}25$ µs). It follows that the initial part of TRV is covered by terminal fault test duty T100s and the SLF test duty is not required in this case. For voltages lower than 52 kV, the situation is discussed in CIGRE Technical Brochure 134 [128] where it is recognised that the majority of connections to line circuits is made via cables, and in these systems SLF tests are generally not necessary. In the case of systems with overhead lines connected directly to the circuit-breaker without any length of cable, it is recommended to verify the SLF interrupting capability of the circuit-breaker.

7.5 Calculation of actual percentage of SLF breaking currents

Replace the title and content of this subclause by the following new title and content:

7.5 Test current and line length tolerances for short-line fault testing

The line reactance corresponding to the standardised line length can be calculated as follows:

$$X_{\text{L, stand}} = \frac{1 - \dfrac{I_{\text{L, stand}}}{I_{\text{sc}}}}{\dfrac{I_{\text{L, stand}}}{I_{\text{sc}}}} X_{\text{source}}$$

where

$I_{\text{L,stand}}$ is the short-line fault breaking current corresponding to the standardised line length;

I_{sc} is the rated short-circuit current;

$X_{\text{L,stand}}$ is the line reactance corresponding to the standardised line length;

X_{source} is the reactance corresponding to the rated short-circuit breaking current.

If the reactance of the line applied in practice differs from the reactance corresponding to the standardised line length within the tolerances of –20 % for L_{90} and ±20 % for L_{75} and L_{60}, as stated in 6.109.2 of IEC 62271-100:2008, the related current values can be calculated as follows:

$$I_{\text{L, act}} = \frac{U_{\text{r}}}{\sqrt{3}\left(X_{\text{L, act}} + X_{\text{source}}\right)}$$

where

$I_{\text{L,act}}$ is the short-line fault breaking current corresponding to the actual line length;

$X_{\text{L,act}}$ is the line reactance corresponding to the actual line length.

The actual line length is calculated considering the standardised line length and the percentage deviation of the actual line length from the standardised one:

$$I_{\text{act}} = I_{\text{stand}}\left(1+\frac{d}{100}\right)$$

where

l_{stand} is the standardised line length;

l_{act} is the actual line length;

d is the deviation of the actual line length from the standardised line length in percent.

The actual line reactance is calculated using the following equation:

$$X_{\text{L, act}} = X_{\text{L, stand}} \times \frac{I_{\text{act}}}{I_{\text{stand}}} = X_{\text{L, stand}}\left(1+\frac{d}{100}\right)$$

The actual percentage short-line fault breaking current $I_{\text{perc,act}}$ is determined by the following equation:

$$I_{\text{perc, act}} = \frac{I_{\text{L, act}}}{I_{\text{sc}}} \times 100 = \frac{I_{\text{perc, stand}}}{1+\frac{d}{100}\left(1-\frac{I_{\text{perc, stand}}}{100}\right)}$$

In Table 42 the actual percentage short-line fault breaking currents are stated for each standardised short-line fault breaking current $I_{\text{perc,stand}}$ taking the maximum tolerances for the line length into account.

Table 42 – Actual percentage short-line fault breaking currents

Standardised short-line fault breaking current $I_{\text{perc,stand}}$ %	Deviation of the line length d %	Actual short-line fault breaking current $I_{\text{perc,act}}$ %
90	**–20**	**91,8**
90	**0**	**90**
75	**–20**	**78,9**
75	**+20**	**71,4**
60	**–20**	**65,2**
60	**+20**	**55,5**

9 Switching of capacitive current

Replace the entire clause by the following new content:

9.1 General

Preferred values for capacitive current switching are given in Table 9 of IEC 62271-100:2008. The values include both de-energisation and energisation of capacitive loads as follows:

– shunt capacitor banks in single and parallel configurations;

– no-load cables in single and parallel configurations;

– no-load transmission lines.

The values given in Table 9 of IEC 62271-100:2008 for inrush current peak and frequency are not linked to the back-to-back capacitor bank breaking current.

Capacitive currents are typically in the order of up to a few hundred amperes and interruption is generally considered a light duty for a circuit-breaker. However, restriking is an issue since it may lead to undesirable overvoltages or high-frequency transients affecting power quality and also may cause damage to the interrupting unit or units. Circuit-breakers are therefore rated according to their restriking probability, i.e. restrike performance class C1 or C2 as discussed in 3.3.

Energisation of capacitive loads is usually associated with transient voltages and currents. Those transients are the following:

– inrush currents;

– overvoltages caused by the system response to the voltage dip when energizing capacitor banks;

– overvoltages caused by travelling waves on transmission lines and cables.

These transients also present power quality issues and some form of mitigation may be necessary as discussed later. IEC 62271-100 contains preferred values of inrush current magnitude and frequency, namely 20 kA peak and 4 250 Hz.

Type testing is designed to be representative of the service conditions up to the point of either clearing, reigniting or restriking. Because the actual value of overvoltage and transient response is totally system-dependent, tests cannot replicate these effects. By providing a means of assessing the likelihood of restrike occurrence, the user can determine what best suits their application. It is assumed that since capacitor switching is not the only source of overvoltage, other protection systems are employed and in the case of unacceptable power quality for sensitive electronic equipment, a sufficiently low number of likely events are selected. A separate study of actions relative to power quality on energisation should also be made.

In the selection of the rating for the circuit-breaker for capacitive current switching, the following needs to be considered:

a) application, i.e. capacitor bank (single or back-to-back), cable or transmission line;

b) power frequency of the network;

c) earthing situation of the network;

d) neutral earthing of the capacitor bank, i.e. solidly earthed or isolated;

e) presence of single or two phase-to-earth faults.

Based on the application, the required restrike performance class of the circuit-breaker can be chosen (C1 or C2) and also the mechanical endurance class (M1 or M2). Network earthing, presence of single and two phase-to-earth faults are important factors that determine the recovery voltage across the circuit-breaker, which, in turn, determines the test voltage of the circuit-breaker.

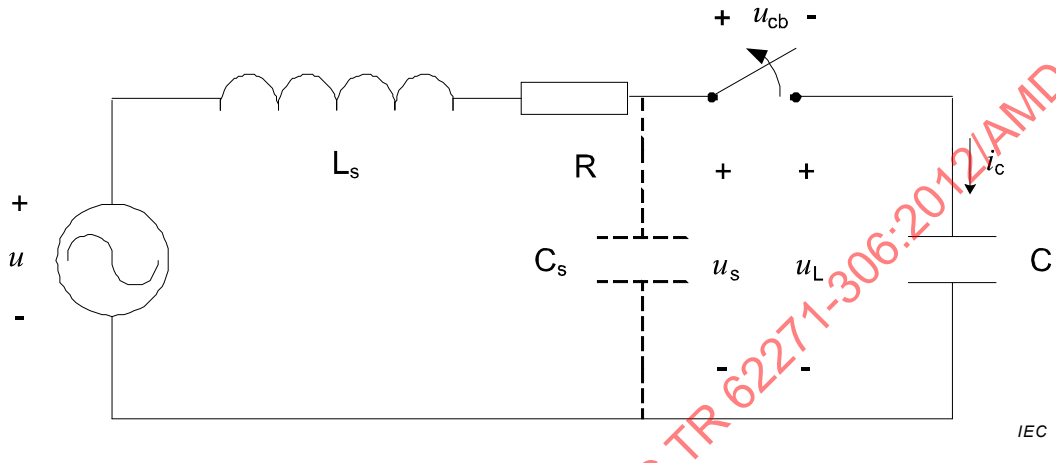
In 9.2, the general theory of capacitive current switching is given as well as the application and testing considerations.

9.2 General theory of capacitive current switching

9.2.1 De-energisation of a capacitive load

9.2.1.1 General

The single-phase equivalent circuit shown in Figure 98 may be used to illustrate the conditions when de-energising a capacitive load. The capacitive load is in this case represented by a concentrated capacitor.



Key

u	Source voltage (r.m.s.)	u_{cb}	Voltage across the circuit-breaker (r.m.s.)
L_s	Source inductance	u_L	Voltage across the capacitive load (r.m.s.)
R	Resistor representing the losses in the circuit	i_c	Capacitive current (r.m.s.)
C_s	Source side capacitance (stray capacitance)	C	Capacitive load (capacitor bank, transmission line or cable)
u_s	Source side voltage (r.m.s.)		

Figure 98 – Single-phase equivalent circuit for capacitive current interruption

9.2.1.2 Capacitive current

The capacitive current i_c flowing in the circuit is given by Equation (147):

$$i_c = \frac{\omega_s C \times u}{1 - \omega_s^2 L_s C} = \frac{\omega_s C \times u}{1 - \frac{\omega_s^2}{\omega_i^2}} \quad (147)$$

where

C is the capacitance of capacitor bank C (F).

$$\omega_s = 2\pi f_s ,$$

where

f_s is the system frequency (Hz).

$$\omega_i = \frac{1}{\sqrt{L_s C}} = 2\pi f_i ,$$

where

f_i is the inrush current frequency in Hz (see also 9.2.3);

L_s is the inductance of the source inductance L_s (H).

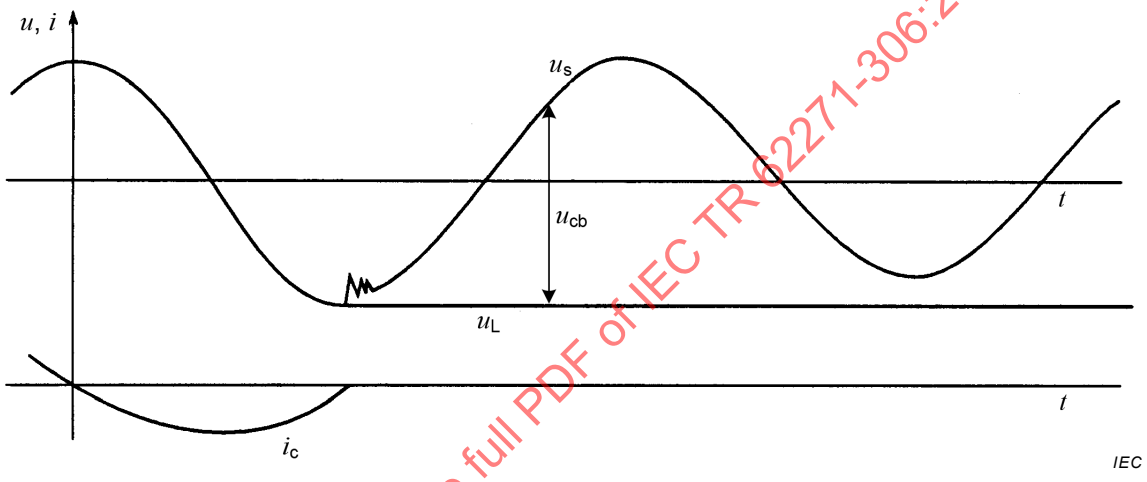
With $\omega_i >> \omega_s$, Equation (147) transforms to $i_c = \omega_s C \times u$.

In the determination of the power frequency capacitive current the influence of the resistance R is usually negligible and is ignored in Equation (147).

9.2.1.3 Recovery voltage

9.2.1.3.1 Recovery voltage in a single-phase circuit

Figure 99 shows the current and voltage shapes at interruption.



Key

i_c	Capacitive current
u_L	Voltage on the load side of the circuit-breaker
u_{cb}	Voltage across the circuit-breaker
u_s	Voltage on the source side of the circuit-breaker

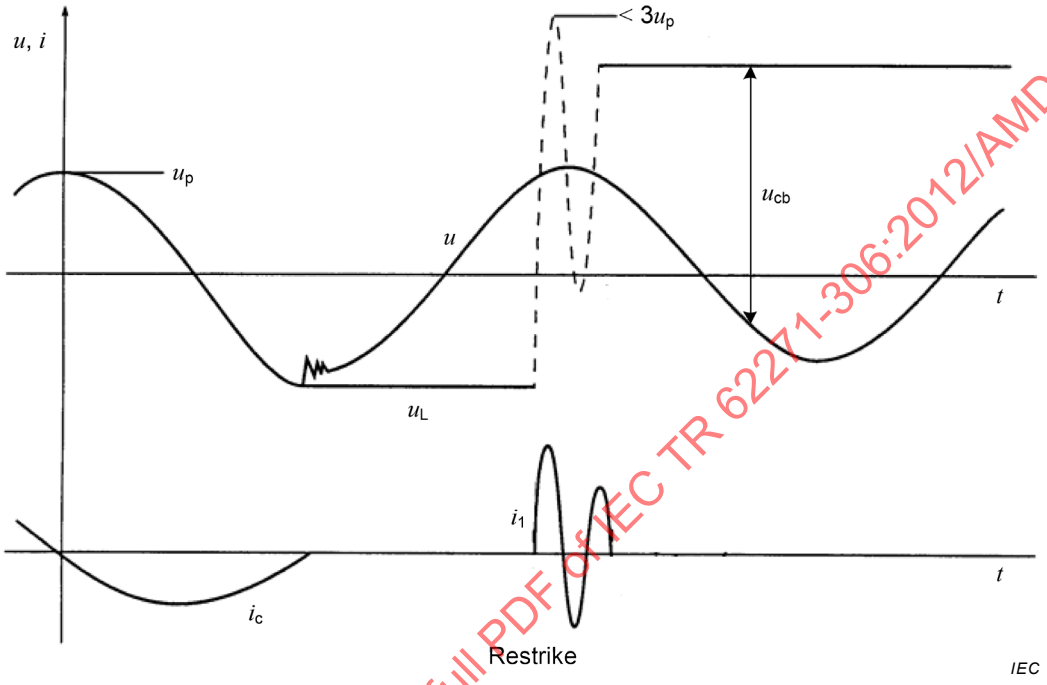
Figure 99 – Voltage and current shapes at capacitive current interruption

After interruption of the current, the supply side voltage u_s will be more or less unaffected. There is only a minor decrease in amplitude, associated with the removal of the capacitive load. The transition to the new amplitude value is associated with a slight oscillation, the frequency of which is determined by L_s and C_s.

The interruption of the current leaves a trapped charge on the capacitor bank. The voltage u_L will remain constant at the value it had at current zero (namely the peak value of the supply voltage).

Together with the low-current amplitude to be interrupted, the low initial rate-of-rise of the recovery voltage makes it relatively easy for the circuit-breaker to interrupt. Some circuit-breakers may interrupt even if the current zero occurs immediately after contact separation. Half a cycle after current zero, the recovery voltage increases to an amplitude of twice the peak value of the supply voltage. Consequently, a rated frequency of 60 Hz is more severe than 50 Hz. The circuit-breaker may then not be able to withstand the high value of the recovery voltage across a relatively small contact gap. Dielectric breakdown may occur between the contacts and the current is re-established between the contacts.

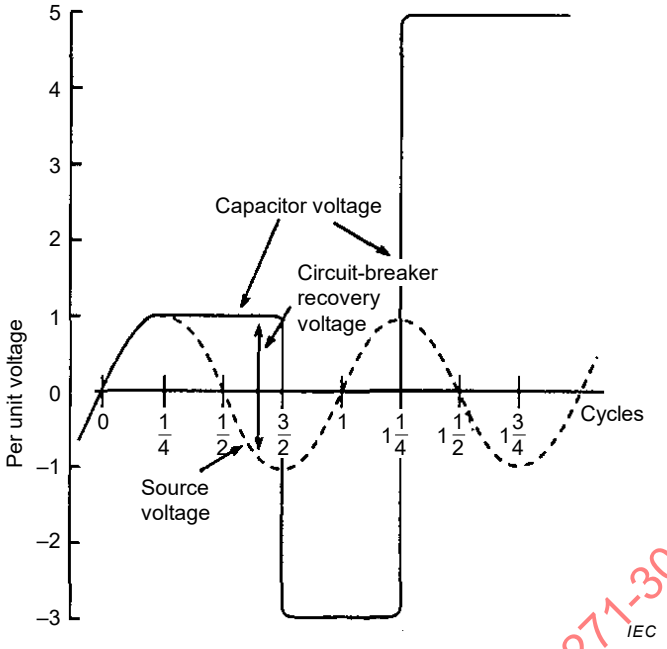
Figure 100 shows current and voltage wave shapes in a case where voltage breakdown occurs relatively close to the recovery voltage peak. The load side voltage will swing up to a voltage that ideally (without damping present) reaches three times the supply voltage peak u_p. The oscillation frequency of the current and voltage after the breakdown is determined by L_s and C (assuming $C >> C_s$). The circuit-breaker may interrupt the oscillatory current at one of its current zeros, with the result that the voltage across the capacitor may attain a new constant value, perhaps higher than before. Further breakdowns associated with even higher overvoltages across the load may then occur (Figure 101).



Key

u_p	Peak of the source voltage
i_c	Power frequency capacitive current
i_1	Restrike current through the circuit-breaker
u_L	Voltage on the load side of the circuit-breaker
u_{cb}	Voltage across the circuit-breaker

Figure 100 – Voltage and current wave shapes in the case of a restrike



Key

1 p.u. is the peak value of the phase-to-earth voltage

Figure 101 – Voltage build-up by successive restrikes

Voltage breakdowns at capacitive current interruption are divided into two categories:

1) Re-ignitions: Voltage breakdown during the first 1/4 cycle following current interruption.
2) Restrikes: Voltage breakdown 1/4 of a cycle or more following current interruption.

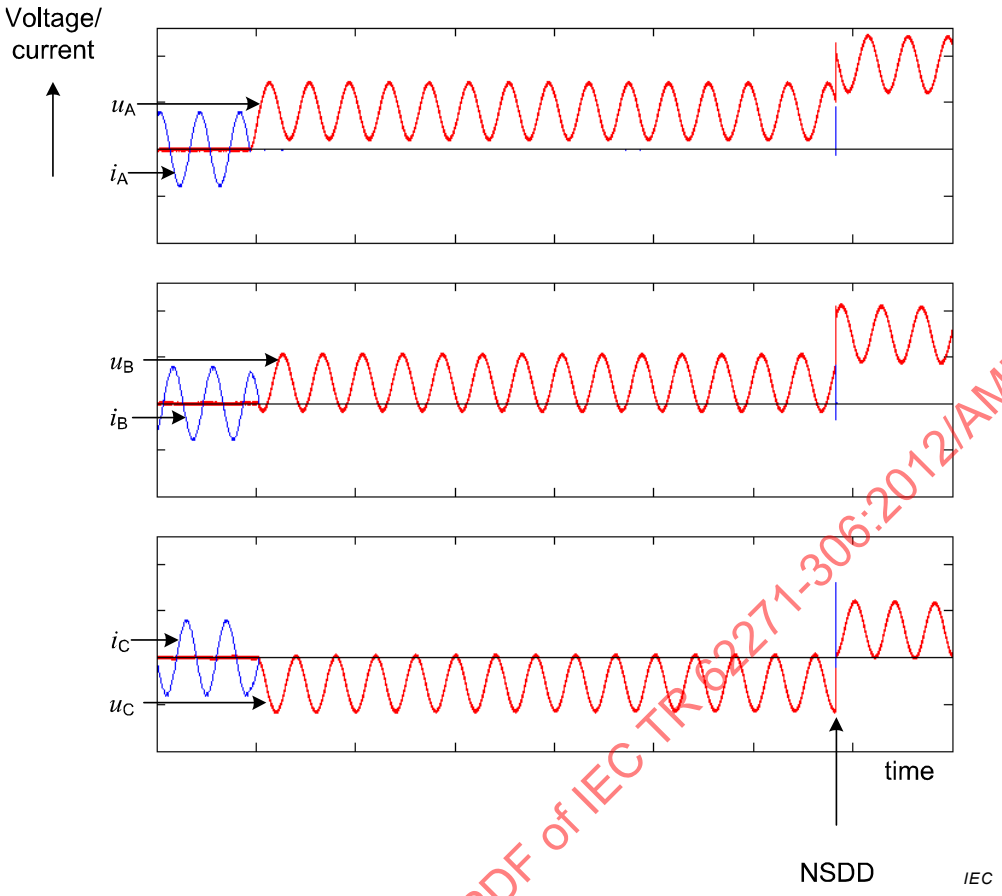
The definitions of re-ignition and restrike are valid only when the recovery voltage has a 1-cosine frequency waveshape.

Restrikes will lead to overvoltages across the capacitive load (maximum 3 p.u. for a single restrike, where 1 p.u. is the peak value of the phase-to-earth voltage) while re-ignitions will not produce any overvoltages (theoretically maximum 1 p.u.). Re-ignitions are acceptable but may cause power quality problems.

In reality, there are no restrike-free circuit-breakers. It would take an infinite number of test shots to verify this. For this reason, the concept of restrike performance was introduced in IEC 62271-100.

Another phenomenon, which has been observed predominantly on vacuum circuit-breakers, may occur during three-phase capacitive current and short-circuit breaking current tests, but also at lower currents and voltages. This phenomenon is known as a *non-sustained disruptive discharge* (NSDD).

An NSDD is defined as a disruptive discharge associated with current interruption that does not result in the resumption of power frequency current or, in the case of capacitive current interruption does not result in current at the natural frequency of the circuit. An NSDD is considered as a late local breakdown across the interrupter and leads to a resumption of high-frequency current. The high-frequency oscillation is determined by stray capacitance and inductance locally across the interrupter. An example of an NSDD is given in Figure 102.



Key

i_A, i_B, i_C	Currents in phase A, B and C, respectively
u_A, u_B, u_C	Voltages across the contacts of phase A, B and C, respectively

Figure 102 – Example of an NSDD during capacitive current interruption

9.2.1.3.2 Recovery voltage in a three-phase circuit

The recovery voltages in three-phase circuits are more complicated than in the single-phase case. Figure 103 shows as an example the recovery voltage of the first-pole-to-clear in a case with a non-effectively earthed capacitive load. Due to the neutral shift, the recovery voltage initially has a shape that will lead to a peak value equal to three times the supply voltage peak (dotted line). The neutral shift is then 1,0 p.u. When the two last poles interrupt 90 electrical degrees after the first, there is however, a discontinuity in the slope (the neutral shift remains at 0,5 p.u.) and the final peak value for the first-pole-to-clear is 2,5 times the supply voltage peak (see also 9.6).

NOTE The recovery voltage peak of a circuit-breaker having a non-simultaneity between poles of more than ¼ cycle will be 3 times the supply voltage peak.

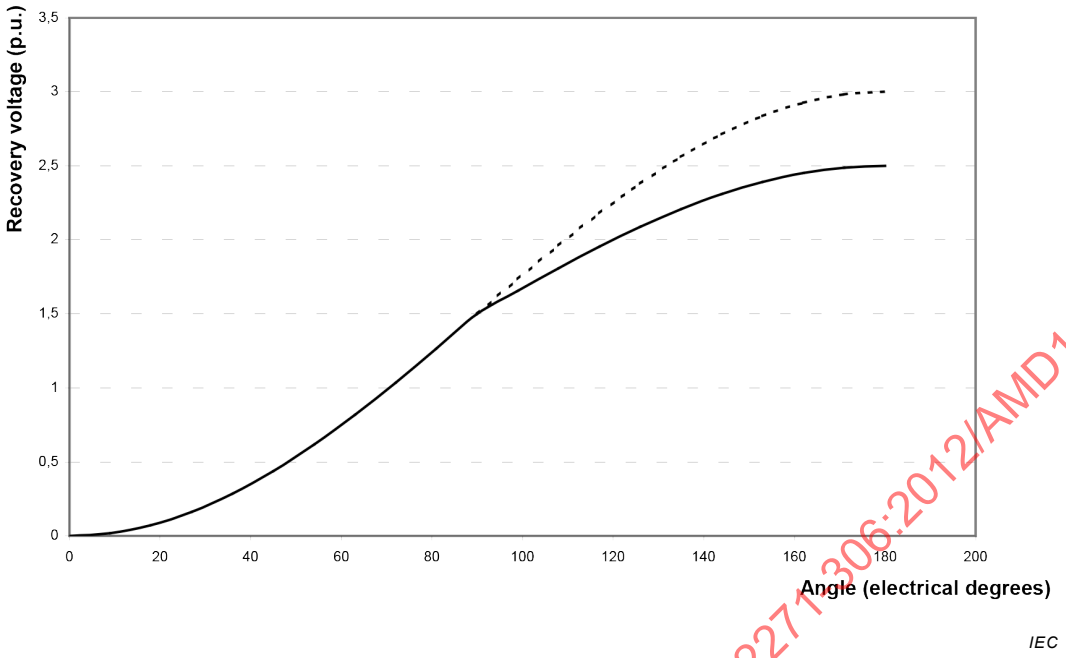


Figure 103 – Recovery voltage of the first-pole-to-clear at interruption of a three-phase non-effectively earthed capacitive load

9.2.2 Energisation of a capacitive load

With reference to Figure 98, L_s, R and C form a series RLC circuit. Applying a voltage u to such a circuit, the inrush current i can be calculated in general as follows:

$$u = Ri + L_s \frac{di}{dt} + \frac{q}{C}$$

Differentiating and treating u as a step voltage, i.e. energisation at the instant of the voltage peak:

$$\frac{d^2i}{dt^2} + \frac{R}{L_s}\frac{di}{dt} + \frac{1}{L_sC}i = 0 \qquad (148)$$

Equation (148) is a second order linear homogenous differential equation with three possible solutions depending on the degree of damping in the circuit. Taking $\alpha = R/2L_s$ and $\omega_0 = 1/\sqrt{L_sC}$, the three solutions are:

1) Overdamped $\alpha^2 > \omega_0^2$

$$i(t) = \frac{u}{L_s\sqrt{\alpha^2 - \omega_0^2}} e^{-\alpha t} \sinh\sqrt{\alpha^2 - \omega_0^2}\, t \qquad (149)$$

2) Critically damped $\alpha^2 = \omega_0^2$

$$i(t) = \frac{u}{L_s} te^{-\alpha t} \qquad (150)$$

3) Underdamped $\omega_0^2 > \alpha^2$

$$i(t) = \frac{u}{L_s\sqrt{\omega_0^2 - \alpha^2}} e^{-\alpha t} \sin\sqrt{\omega_0^2 - \alpha^2}\, t \quad (151)$$

The resistance value R_{cd} that results in critical damping is given by:

$$R_{cd} = 2\sqrt{\frac{L_s}{C}} \quad (152)$$

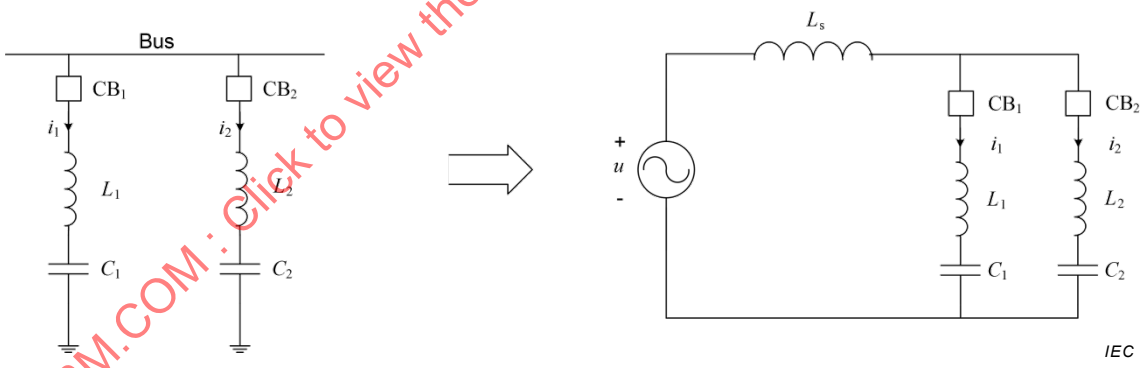
In most cases, the inrush current oscillation is underdamped and Equation (151) is of most interest. If closing resistors are applied to limit the inrush current, then Equation (149) or (150) may be applicable.

9.3 Capacitor bank switching

9.3.1 General

Since the use of capacitor banks for compensation purposes is increasing, it is common that more than one capacitor bank is connected to the same bus (back-to-back capacitor bank switching). This has no influence on the conditions at interruption. The current at closing, however, is affected to a high degree.

To describe the phenomena associated with capacitor bank switching, a general single-phase equivalent circuit is shown in Figure 104 showing a single-line diagram of the case where two capacitor banks (C_1 and C_2) are connected in back-to-back to a busbar. L_1 and L_2 represent the stray inductance (or stray inductance plus additional damping inductance). The inductance L_s of the source network will be several orders of magnitude higher than that of L_1 or L_2.



Key

CB_1	circuit breaker considered
CB_2	circuit breaker, open for single capacitor bank switching by CB_1, closed for back-to-back capacitor bank switching by CB_1
L_s	source inductance
L_1, L_2	inductance between capacitor bank 1 and 2 and bus, respectively
C_1, C_2	capacitor bank 1 and 2
i_1, i_2	capacitive currents
u	source voltage

Figure 104 – General circuit for capacitor bank switching

Single capacitor bank switching occurs when C_1 is switched and C_2 is not connected in the circuit described in Figure 104. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. The inductance L_1 can be disregarded here, since the value of the source inductance L_s>>L_1.

Back-to-back capacitor bank switching occurs when switching C_1, with C_2 being in service, or vice versa.

The conditions for single and back-to-back capacitor bank switching are given in 9.3.3.1 and 9.3.3.2. In some cases, energised capacitor banks in nearby substations may contribute to the inrush current such that a back-to-back situation occurs.

Especially, the second case may give rise to an inrush current of very high amplitude and frequency, which may have to be limited in order not to be harmful to the circuit-breaker, the capacitor banks and/or the network. The magnitude and frequency of this inrush current is a function of the following:

a) applied voltage (point on the voltage wave at closing); the magnitude will be maximum on closing at the voltage peak;

b) capacitance of the circuit;

c) inductance in the circuit (amount and location);

d) any charge on the capacitor bank at the instant of closing;

e) any damping of the circuit due to closing resistors or other resistances in the circuit.

It is assumed that the capacitor bank is discharged prior to energisation. This is a reasonable assumption, as capacitor units are fitted with discharging resistors that will discharge the capacitor bank. Typical discharge times are in the order of 5 min.

The transient inrush current to a single bank is less than the available short-circuit current at the capacitor bank terminals. It rarely exceeds 20 times the rated current of the capacitor bank at a frequency that approaches 1 kHz. Since a circuit-breaker shall meet the making current requirements of the system, transient inrush current is not a limiting factor in single capacitor bank applications. For this reason making tests with inrush current are not required for single-capacitor bank switching.

When capacitor banks are switched back-to-back, transient currents of prospective high magnitude and with a high natural frequency may flow between the banks on closing of the circuit-breaker. The effects are similar to that of a restrike on opening. This oscillatory current is limited only by the impedance of the capacitor bank and the circuit between the energised bank or banks and the switched bank. This transient current usually decays to zero in a fraction of a cycle of the system frequency. In the case of back-to-back switching, the component supplied by the source is at a lower frequency and so small that it may be neglected.

9.3.2 De-energisation of capacitor banks

De-energisation of capacitor banks follows the theory outlined in 9.2.2.

9.3.3 Energisation of capacitor banks

9.3.3.1 Single capacitor bank

Energising a single capacitor bank is equal to energisation of capacitor bank C_1 when capacitor bank C_2 is not connected in the circuit described in Figure 104. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. L_1 can be disregarded here, since the inductance of the source is several orders of magnitude higher than that of L_1 (i.e. L_s >> L_1). In this case, the peak of the inrush current ($i_{i\ peak}$) and inrush current frequency (f_i) are limited by the source impedance L_s.

A bank of shunt capacitors is considered single when the inrush current on energisation is limited by the inductance of the source and the capacitance of the bank being energised. A capacitor bank is also considered single if the maximum rate of change, with respect to time, of transient inrush current on energisation of an uncharged bank does not exceed the maximum rate of change of the rated short-circuit current at the voltage at which the current is applied. The limiting value is equal to

$$\left(\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}\right)_{\max} = \omega_\mathrm{s} I_\mathrm{sc}\sqrt{2} \tag{153}$$

where

$\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}$ is the rate of change of inrush current, A/s;

I_sc is the rated short-circuit current, in A r.m.s;

$\omega_\mathrm{s} = 2\pi f_\mathrm{s}$ is the angular frequency, in rad/s and f_s is the power frequency, in Hz.

Assuming that bank 1 is to be connected to the busbar and bank 2 is not connected, from Equation (151):

$$i_\mathrm{i} = \frac{\hat{u}}{L\sqrt{\omega_0^2 - \alpha^2}} e^{-\alpha t} \sin\left(\sqrt{\omega_0^2 - \alpha^2}\right)t \tag{154}$$

where $L = L_\mathrm{s} + L_1$ and $\omega_0 = 1/\sqrt{LC_1}$

If ω_0 >> α, then Equation (154) can be re-written in the simplified form:

$$i_\mathrm{i} = \frac{\hat{u}}{Z} e^{-\alpha t} \sin \omega_0 t \tag{155}$$

where $Z = \sqrt{\frac{L}{C_1}}$

The two quantities of interest for circuit-breaker application are the peak value of the inrush current $i_{\mathrm{i\ peak}}$ and its frequency f_i:

$$i_{\mathrm{i\,peak}} = \frac{\sqrt{2}u}{Z} \tag{156}$$

$$f_\mathrm{i} = \frac{1}{2\pi\sqrt{L_\mathrm{s}C_1}} \tag{157}$$

where $Z = \sqrt{\frac{L_\mathrm{s}}{C_1}}$ and $L_\mathrm{s} >> L_1$ is assumed.

9.3.3.2 Back-to-back capacitor bank switching

The inrush current of a single bank will be increased when other capacitor banks or parallel cables are connected to the same bus.

If, in Figure 104, bank 1 is connected to the busbar and initially uncharged bank 2 is to be connected, the inrush current associated with the charging of bank 2 is supplied by bank 1 (back-to-back switching).

Equations (156) and (157) are applicable and adjusted as follows:

$$i_{\mathrm{i}} = \frac{\sqrt{2}u}{Z_{\mathrm{eq}}} \tag{158}$$

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{L_{\mathrm{eq}}C_{\mathrm{eq}}}} \tag{159}$$

where $Z_{\mathrm{eq}} = \sqrt{L_{\mathrm{eq}} / C_{\mathrm{eq}}}$, $L_{\mathrm{eq}} = L_1 + L_2$ and $C_{\mathrm{eq}} = \frac{C_1 C_2}{C_1 + C_2}$

Equations (158) and (159) can be applied in general to multiple bank switching cases. Assume that bank C with series inductance L is to be switched in with banks C_1 to C_{n} and associated series inductances L_1 to L_{n} already in service. The simplified calculation procedure is as follows:

a) Ignore the capacitances and calculate L_{eq}

$$L_{\mathrm{eq}} = L + L'$$

where $L' = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \ldots\ldots \frac{1}{L_n}}$

b) Ignore the inductances and calculate C_{eq}

$$C_{\mathrm{eq}} = \frac{CC'}{C + C'}$$

where $C' = C_1 + C_2 + \ldots\ldots + C_n$

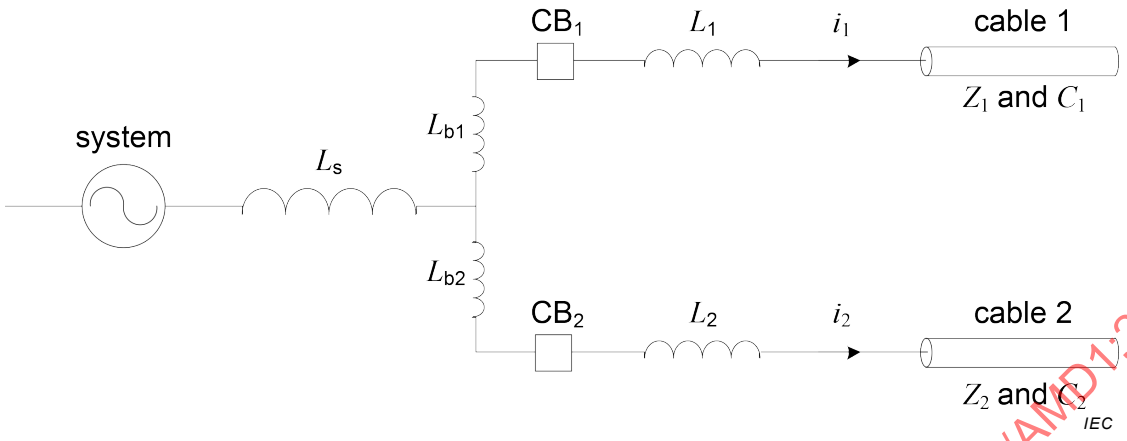
Typical amplitudes of the inrush currents for back-to-back energisation of capacitor banks are several kA with frequencies of 2 kHz to 5 kHz. Typical values are given in Table 9 of IEC 62271-100:2008. Capacitors can normally withstand amplitudes up to 100 times their rated current.

If the inrush current amplitude and frequency exceed those stated in Table 9 of IEC 62271-100:2008, it may be necessary to limit them. This can be done by insertion of additional series inductance in the circuit, or by using pre-insertion resistors (see 9.5.3). Another possibility is to use controlled switching.

9.4 No-load cable switching

9.4.1 General

To describe the phenomena associated with no-load cable switching, a general single-phase equivalent circuit is shown in Figure 105, showing the case where two cables (cable 1 and cable 2) are connected back-to-back to a system. The cables are represented by their capacitance C_1 and C_2 and their surge impedances Z_1 and Z_2, respectively.



Key

CB_1	circuit-breaker
CB_2	circuit-breaker, open for single cable switching, closed for back-to-back switching
L_s	source inductance
L_1, L_2	inductance between cables 1 and 2 and the bus
Z_1, Z_2	surge impedance of cables 1 and 2 (Ω)
C_1, C_2	capacitance of cables 1 and 2 (F)
L_{b1}, L_{b2}	inductance of the bus connecting the cables

Figure 105 – Typical circuit for no-load cable switching

Single cable switching occurs when cable 1 is switched and cable 2 is not connected in the circuit described in Figure 10. The circuit then consists of the source inductance L_s in series with the bus inductance L_{b1} and the inductance L_1 between bus and cable.

Back-to-back cable switching occurs when cable 1 is switched, with cable 2 being in service.

Three phase cables can be individually screened (Figure 106) or belted (Figure 107). As the equivalent circuits show, individually screened cables represent a load similar to earthed capacitor banks and belted cables a load similar to unearthed capacitor banks.

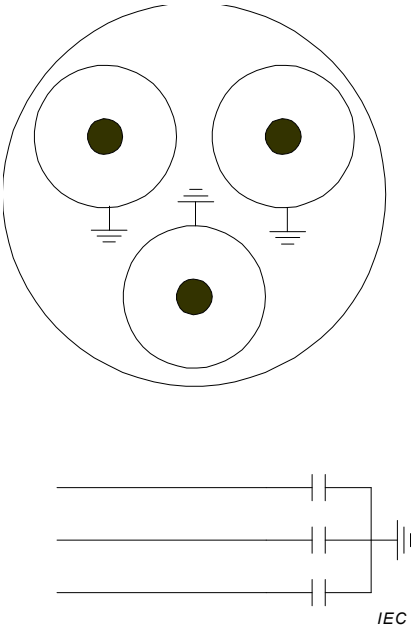


Figure 106 – Individually screened cable with equivalent circuit

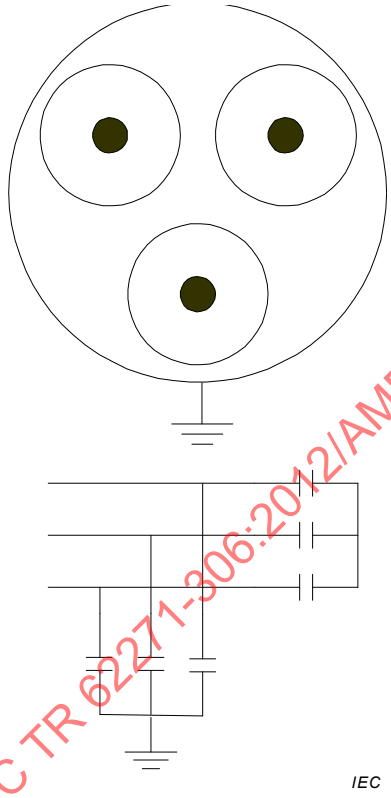


Figure 107 – Belted cable with equivalent circuit

9.4.2 De-energisation of no-load cables

9.4.2.1 General

A cable represents a distributed capacitive load. For de-energisation of a no-load cable, the principles discussed for capacitor bank switching are equally applicable with some variations as discussed later in Subclause 9.4.2. For example, in transient calculations, the cable surge impedance is applicable rather than its capacitance.

9.4.2.2 Cable charging current

The cable charging current is a function of the following characteristics:

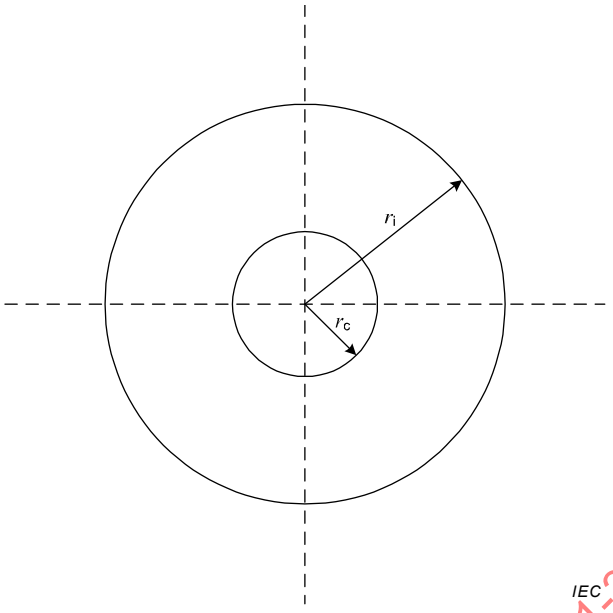
a) system voltage;

b) cable geometry;

c) insulation dielectric constant;

d) cable length.

The shunt capacitive reactance can be obtained from the cable manufacturer, or if the physical constants of the cable are known, the shunt capacitive reactance can be calculated. Figure 108 shows the cross-section of a high-voltage cable.



Key

r_c	Conductor radius (m)
r_i	Inside diameter of the shield

Figure 108 – Cross-section of a high-voltage cable

The shunt capacitance per unit length of a cable is expressed in Equation (160).

$$C = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln(\frac{r_i}{r_c})} \text{ F/m} \quad (160)$$

The series inductance per unit length of a cable is expressed in Equation (161).

$$L = \frac{\mu_0\mu_r}{2\pi}\ln(\frac{r_i}{r_c}) \text{ H/m} \quad (161)$$

For single-conductor and three-conductor shielded cables (for the different cable configurations see Figure 106 and Figure 107) the shunt capacitive reactance per km (X_c) can be written as shown in Equation (162).

$$X_c = \frac{1}{\omega_s C} = \frac{\ln(\frac{r_i}{r_c})}{l \times \omega_s \times 2\pi\varepsilon_0\varepsilon_r} (\text{M}\Omega) \quad (162)$$

Using the relationship $\ln(x) = 2{,}3\lg(x)$ and l = 1 000 m = 1 km, Equation (162) transforms to Equation (163).

$$X_c = \frac{6{,}58}{f_s\varepsilon_r}\lg\frac{r_i}{r_c} \text{ (M}\Omega \text{ per phase, see NOTE and Figure 108)} \quad (163)$$

where

f_s is the system frequency (Hz);

ε_0 is the dielectric constant of vacuum, $\varepsilon_0 = 8{,}85\times10^{-12}$ (F/m);

ε_r is the relative dielectric constant of cable dielectric material;

r_i is the inside radius of shield (mm);

r_c is the conductor radius (mm);

l is the cable length (m);

μ_0 is the magnetic permeability of vacuum, $\mu_0 = 4\pi \times 10^{-7}$ (H/m);

μ_r is the relative magnetic permeability of the cable dielectric material ($\mu_r \approx 1$);

ω_s is the angular power frequency, $\omega_s = 2\pi f_s$ (rad/s);

f_s is the power frequency (Hz);

ln is the natural logarithm based on e, $^{e}\log x$;

lg is the logarithm based on 10, $^{10}\log x$.

NOTE When using the quantity MΩ per phase per km, the shunt capacitive reactance in MΩ for more than 1 km decreases because the capacitance increases. For more than 1 km of cable, therefore, the value of shunt capacitive reactance as given above is divided by the number of km of cable.

Using the capacitive reactance, the cable charging current can be calculated and compared with the rated cable charging current of the circuit-breaker given in IEC 62271-100. If the calculation exceeds the rating, the manufacturer should be consulted. Before an application can be made, the inrush current rating should also be checked (see 9.4.3).

The surge impedance (Z) of a single-conductor and three-conductor shielded cables can be expressed using Equation (164).

$$Z = \sqrt{\frac{L}{C}} = \sqrt{\frac{\frac{\mu_0\mu_r}{2\pi}\ln(\frac{r_i}{r_c})}{\frac{2\pi\varepsilon_0\varepsilon_r}{\ln(\frac{r_i}{r_c})}}} = \sqrt{\frac{4\pi\times10^{-7}}{4\pi^2 8.85\times10^{-12}\varepsilon_r}}\times\ln(\frac{r_i}{r_c}) = \frac{138}{\sqrt{\varepsilon_r}}\times\log\left(\frac{r_i}{r_c}\right) \quad (\Omega) \qquad (164)$$

Typical values of ε_r range from 2,3 (polyethylene) to 4 (fluid impregnated paper); a typical value for Z is 50 Ω.

9.4.2.3 Recovery voltage

The recovery voltage is similar to that of a capacitor bank (see 9.2.2.3).

9.4.3 Energisation of no-load cables

9.4.3.1 General

A circuit breaker may be required to energize a no-load cable during its normal operating duties. Prior to energisation the cable is usually at ground potential, but can have a trapped charge from a previous switching operation. A cable may be switched from a bus that does not have other cables energized (single cable) or against a bus that has one or more cables energized (i.e. back-to-back cable).

The energisation of a cable by the closing of a circuit breaker will result in a transient inrush current. The magnitude and rate of change of this inrush current is a function of the following:

– applied voltage (including the point on the voltage wave at closing);

– cable surge impedance;
– cable capacitive reactance;
– inductance in the circuit (amount and location);
– any charges on the cable at the instant of closing;
– any damping of the circuit because of closing resistors or other resistance in the circuit.

The transient inrush current to a single cable is less than the available short-circuit current at the circuit breaker terminals. Because a circuit breaker shall meet the making current requirements of the system, transient inrush current is not a limiting factor in single cable applications.

When cables are switched back-to-back (that is, when one cable is switched while other cables are connected to the same bus), transient currents of high magnitude and initial high rate of change may flow between cables when the switching circuit-breaker is closed or restrikes on opening. This surge current is limited by the cable surge impedances and any inductance connected between the energised cable(s) and the switched cable. This transient current usually decays to zero in a fraction of a cycle of the system frequency. During back-to-back cable switching, the component of current supplied by the source is at a lower rate of change and so small that it may be neglected. Due to the very high damping of the inrush current, the switching of parallel cables usually does not represent a problem for modern circuit-breakers. Therefore no problems are expected for back-to-back cable configurations. The case of back-to-back cable switching is not addressed in IEC 62271-100.

Cables are considered being switched back-to-back if the maximum rate of change of transient inrush current on energizing an uncharged cable exceeds that specified for a single cable.

9.4.3.2 Single cable energisation

A cable is defined as single if the maximum rate of change, with respect to time, of transient inrush current on energizing an uncharged cable does not exceed the rate of change of current associated with the rated short-circuit current. This limiting value is numerically equal to

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max} = \omega_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} = 2\pi f_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} \qquad (165)$$

where

$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max}$ is the maximum rate of change of inrush current in A/s;

I_{sc} is the rated r.m.s. short-circuit current, in A;

$\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$ is the angular frequency in rad/s, where f_{s} is the power frequency in Hz.

By this definition, it is possible to have cable circuits that are physically back-to-back, but are considered single for application purposes provided a large inductance is located between the two cable circuits. The inductance should be large enough so that by itself it would limit fault current to a value less than or equal to the circuit-breaker rating.

In switching a single cable, if the source inductance is greater than 10 times the cable inductance, the cable can be represented as a capacitor. Otherwise, under transient conditions the cable can be represented by its surge impedance.

To calculate the inrush current for a single cable, Figure 105 may be used, with circuit-breaker CB_2 open.

$$i_{\mathrm{i}}(t) = \frac{U_{\mathrm{m}} - U_{\mathrm{t}}}{Z_1}\left[1 - \exp(-\frac{Z_1}{L}t)\right] \quad (166)$$

where

$$i_{\mathrm{i\,peak}} = \frac{U_{\mathrm{m}} - U_{\mathrm{t}}}{Z_1}$$

U_{m} is the crest of applied voltage;

U_{t} is the trapped voltage on the cable being switched;

f_{s} is the source frequency (power frequency);

i_{i} is the inrush current;

$i_{\mathrm{i\,peak}}$ is the peak of the inrush current;

Z_1 is the cable surge impedance;

L is the source inductance.

The initial rate-of-rise (di/dt at t = 0) of the inrush current is $\frac{U_{\mathrm{m}} - U_{\mathrm{t}}}{L}$. For application purposes, $i_{\mathrm{i\,peak}}$ should be compared to the value given in Table 9 of IEC 62271-100:2008.

The cable inrush current is not oscillatory in the usual frequency-related sense, but the initial slope can be used to determine an equivalent frequency that can be compared with the inrush frequency. In general,

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right) = 2\pi f_{\mathrm{i}} I_{\mathrm{i}} \quad (167)$$

where

$\left(\frac{\mathrm{d}i_i}{\mathrm{d}t}\right)$ is the rate-of-change of inrush current in A/s;

f_{i} is the inrush current frequency;

I_{i} is the peak inrush current.

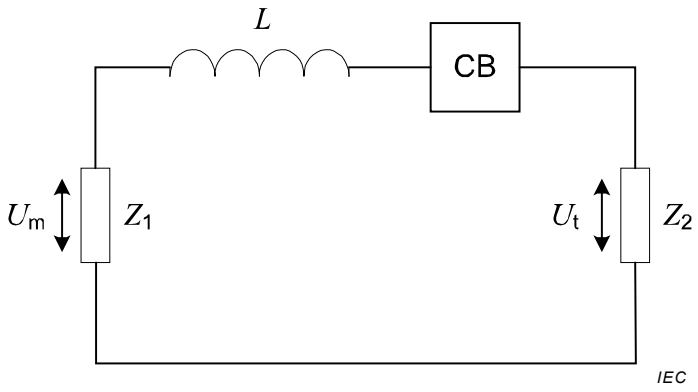
The equivalent frequency f_{eq} for a cable inrush current is then obtained as follows:

$2\pi f_{\mathrm{eq}} I_{\mathrm{i}} = \frac{U_{\mathrm{m}} - U_{\mathrm{t}}}{L}$ that gives $f_{\mathrm{eq}} = \frac{U_{\mathrm{m}} - U_{\mathrm{t}}}{2\pi L I_{\mathrm{i}}}$ and for proper circuit-breaker application, f_{eq} should be less than the preferred inrush current frequency.

9.4.3.3 Back-to-back cable energisation

Back-to-back cable switching occurs when cable 2 is in service and cable 1 is being energized in Figure 105. The values of the inductances of L_1, L_2, and L_{b1} and L_{b2} between the cables are often very small with respect to the inductance of L_{s}. In many cases they will be less than 1 % of the source inductance. They consist of the inductances from the cables to the circuit-breakers, the circuit-breaker inductances, and the bus inductance of the current path. Values of inductance depend upon the physical configuration and are hence site specific and unable to be standardized. However, a representative range is 0,66 µH to 1,0 µH per phase per m.

Neglecting the source contribution, the back-to-back cable switching case can be represented as shown in Figure 109.



Key

U_m	Crest of applied voltage
U_t	Trapped voltage on cable being switched
Z_1, Z_2	Cable surge impedance
L	Total inductance between cable terminals
CB	Circuit-breaker

Figure 109 – Equivalent circuit for back-to-back cable switching

The initial pulse of current has a front expressed as

$$i(t) = \frac{U_m - U_t}{Z_1 + Z_2}\left[1 - \exp\left(-\frac{Z_1 + Z_2}{L}t\right)\right] \quad (168)$$

Assuming that the $L/(Z_1 + Z_2)$ time constant is less than 1/5 of the travel time of the cable out and back, the initial crest of the inrush current is then $(U_m - U_t)/(Z_1 + Z_2)$, which for application should be less than the rated peak inrush current.

The peak inrush current when energizing a cable with another already connected to the bus is given by

$$i_{ipeak} = \frac{U_m - U_t}{Z_1 + Z_2} \quad (169)$$

and

$$f_{eq} = \frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}} \quad (170)$$

The inrush current when energizing a cable with an equal cable already connected to the bus is given by

$$i_{ipeak} = \frac{U_m - U_t}{2Z} \text{ (A)} \quad (171)$$

and

$$f_{eq} = \frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}} \text{ (Hz)} \quad (172)$$

Differentiating the expression for the current at t = 0 will give the maximum initial rate of change of the inrush current, in Equation (173).

$$\left(\frac{di}{dt}\right)_0 = \frac{U_m - U_t}{L} \text{ (A/s)} \quad (173)$$

This can reach extreme values since the magnitude of L can be arbitrarily small.

Additional inductance may be added in series with the inductances making up L to meet the preferred inrush frequency.

9.4.4 Compensated cable energisation

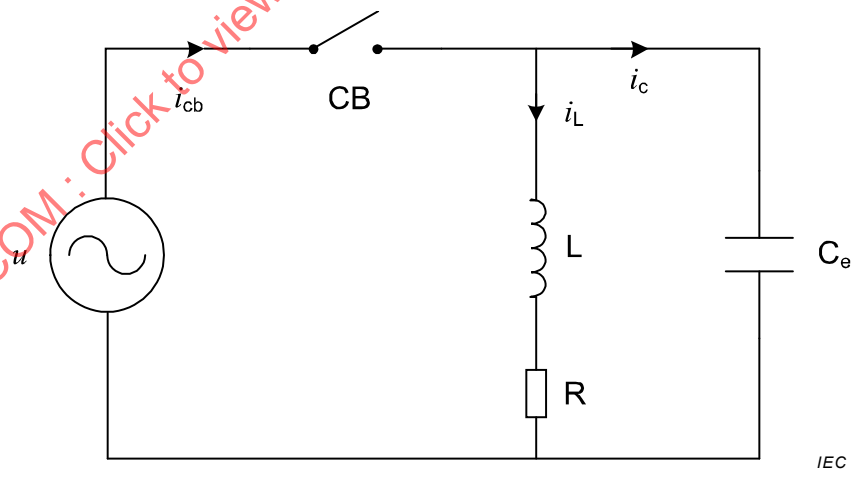
9.4.4.1 General

A circuit-breaker may be required to energise a no-load cable during its normal operating duties. Prior to energisation, the cable is usually at earth potential, but can have a trapped charge from a previous switching operation.

Besides these widely known effects, other phenomena may occur during cable energisation at rated voltages of 420 kV and above.

When operating the cable nearly fully compensated the phenomenon of delayed current zero crossings may occur. This phenomenon is similar to the one described at faults close to generators (see Annex B).

The simplified single-phase equivalent circuit is shown in Figure 110.



Key

u	Phase-to-earth voltage	R	Resistance to earth of compensating reactor
CB	Circuit-breaker	i_{cb}	Current through the circuit-breaker
C_e	Cable capacitance to earth	i_L	Current through the compensating reactor
L	Inductance to earth of compensating reactor	i_c	Current through the cable

Figure 110 – Equivalent circuit of a compensated cable

When energizing the compensated cable by closing the circuit-breaker, the current starts flowing in the cable (i_c, momentary value of the current is not continuous and may change suddenly) and in the reactor (i_L, momentary value of the current is continuous due to the fact that di/dt at a inductance is zero at the instant of closing the circuit-breaker). The sum of both currents flows through the circuit-breaker (i_{cb}).

Due to the fact that the instantaneous current value in the reactor before energizing and the current value directly after energizing shall be identical ($di/dt = 0$), a DC equalizing current flows depending on the making angle and the instantaneous value of the making voltage, respectively. The change of the current through the inductance when closing the circuit-breaker causes a magnetic field. Due to the continuity requirement, this magnetic field is compensated. The equalizing magnetic field causes the DC equalizing current.

If the circuit-breaker is closed at voltage maximum, the equalizing current is zero and when closing at voltage zero, the equalizing current is at its maximum due to the 90° phase shift between voltage and current for an inductance.

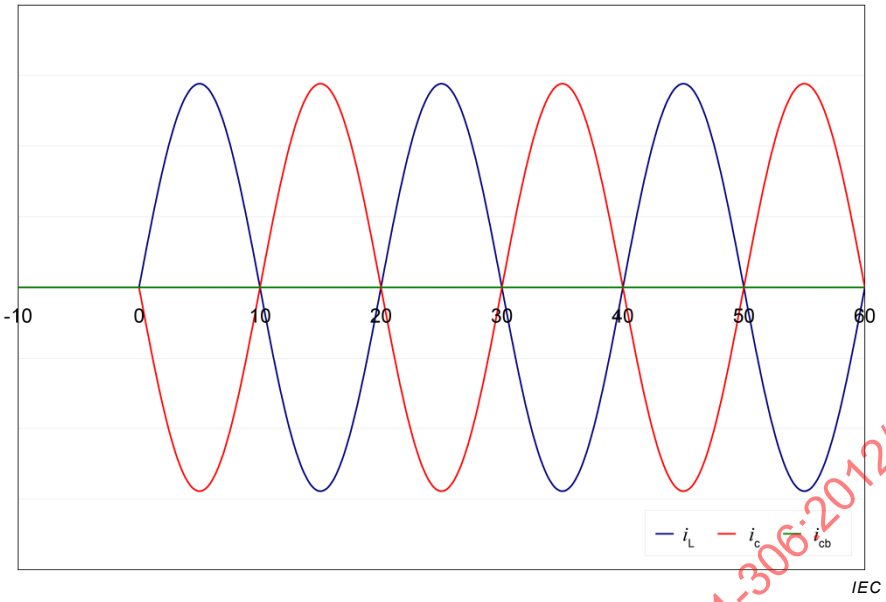
This DC equalizing is superimposed on the inductive AC current of the reactor to the total reactor current i_L. Due to the resistance of the reactor, the DC current decays over time.

The following two different cases are distinguished: fully compensated cables and partly compensated cables.

9.4.4.2 Fully compensated cables

When operating a fully compensated cable, the inductive AC current and the capacitive AC current will be of the same amount. Hereby the capacitive current i_c has the opposite sign of the inductive current i_L.

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 111 for making at voltage maximum and full compensation.

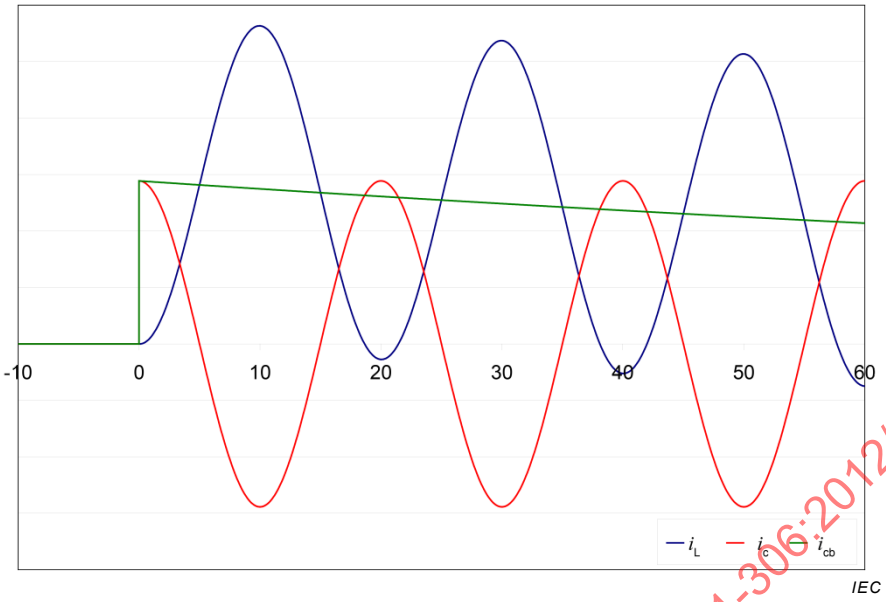


Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Dotted green line	Total current through the circuit-breaker i_{cb}

Figure 111 – Currents when making at voltage maximum and full compensation

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 112 for making at voltage zero and full compensation. The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.



Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 112 – Currents when making at voltage zero and full compensation

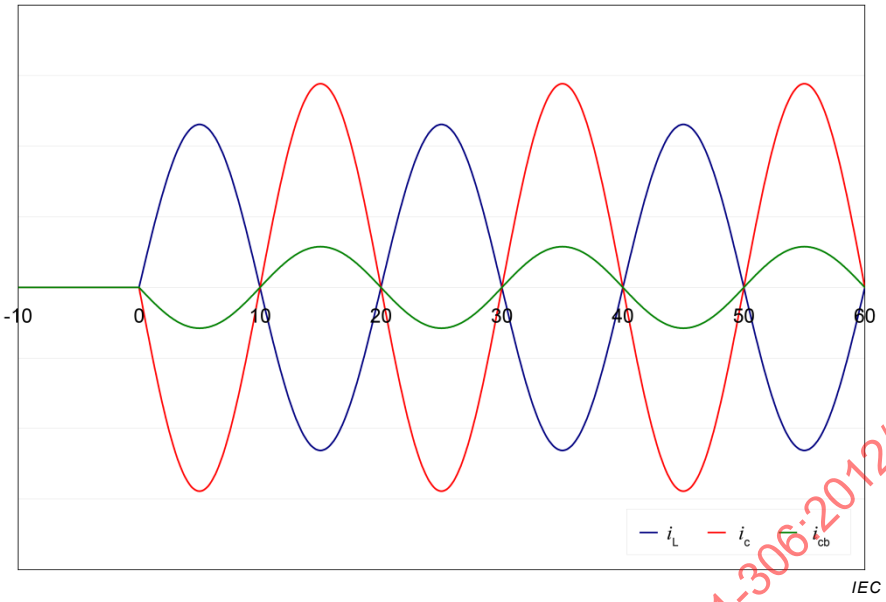
It can be seen that the inductive current i_L and the capacitive current i_c in both cases always show zero crossings.

In the case of making at voltage maximum, the current through the circuit-breaker for a fully compensated cable is zero due to the fact that the inductive current i_L and the capacitive current i_c have the same magnitude and opposite polarity.

In the case of making at voltage zero, the current through the circuit-breaker does not show zero crossings for several periods. If within this time period the circuit-breaker is tripped, it may have severe difficulties to interrupt the current. This will be described in detail further in this subclause.

9.4.4.3 Partly compensated cables

If the cable is partly compensated (undercompensated), the inductive AC current is smaller than the capacitive AC current. The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 113 for making at voltage maximum and partial compensation (e.g. 80 %).

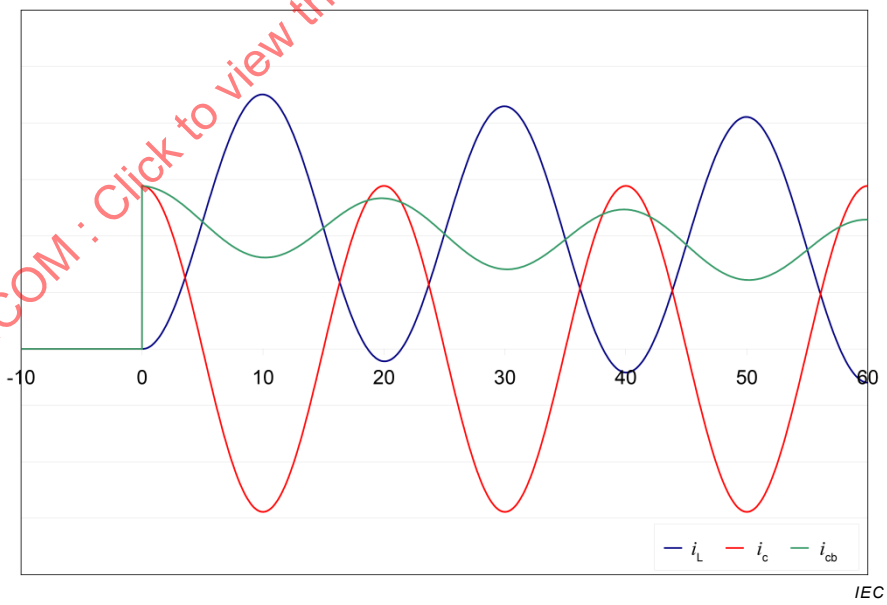


Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 113 – Currents when making at voltage maximum and partial compensation

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 114 for making at voltage zero and partial compensation (e.g. 80 %). The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.



Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 114 – Currents when making at voltage zero and partial compensation

Also, in the case of undercompensated operated cables, it can be seen that the inductive current i_L and the capacitive current i_c in all cases always show zero crossings.

In the case of making at voltage zero, the current through the circuit-breaker also does not show zero crossings for several periods even if the amplitude of the DC equalizing current is smaller due to the lower inductive current at partial compensation.

9.4.4.4 Summary

The amplitude of the DC equalizing current depends on the degree of compensation and the instant of making. The duration of the time period of missing current zero crossings depends on the X/R ratio, the damping of the compensation reactor and the degree of compensation.

In the past, the resistance of the compensation reactors was comparably high. Therefore the X/R ratio (related to the DC time constant τ) was low and the DC equalizing current was damped fast enough to create current zeros. Nowadays, the resistance of the compensation reactors is reduced further in order to minimize the ohmic losses.

The phenomenon of delayed current zero crossings may become problematic if the circuit-breaker is tripped during the time period of missing zero crossings. To solve this problem two basic approaches are possible:

a) prevention of the occurrence of currents with delayed zero crossings;

b) choice of a circuit-breaker suitable for the application.

To prevent currents with delayed zero crossings, the making should always occur around the voltage maximum in each phase. This can be done using controlled closing (point-on-wave closing). Controlled closing ensures that the making occurs in all phases at or near voltage maximum. The disadvantage of this method is the occurrence of switching overvoltages.

If the making at voltage zero cannot be prevented, the decay of the DC equalizing currents can be increased by using circuit-breaker types equipped with pre-insertion resistors. Owing to the additional resistance, the X/R ratio is decreased and hence the first zero crossing of the current i_{cb} occurs significantly earlier. The resistance value of the pre-insertion resistor should be dimensioned in a way that the first zero crossing occurs about 10 ms after making. In this case, a successful opening operation can also be ensured for the worst-case (e.g. opening command is already given during closing of the circuit-breaker). For each application an individual calculation should be performed due to the different parameters of reactor and network parameters as well as a different degree of compensation.

If no suitable resistance value can be determined or controlled switching is not possible, the current shows delayed zero crossings. Hence a suitable circuit-breaker type should be chosen to ensure a successful current interruption at all cases. The arc in the circuit-breaker during the breaking operation represents a non-linear resistance, which also leads to a decreased X/R ratio, and therefore to an earlier occurrence of zero crossings. With special tests, the parameters for an arc model can be determined for each circuit-breaker type. Using this arc model, the influence on the current i_{cb} can be determined. Depending on the amplitude and time constant of the DC equalizing current circuit-breaker types with high arc voltages may be necessary. Also with this method, for each application an individual calculation should be performed due to the different parameters of reactor and network parameters, different parameters of the circuit-breaker arc as well as a different degree of compensation.

9.5 No-load transmission line switching

9.5.1 De-energisation of uncompensated transmission lines

9.5.1.1 Line charging current

A no-load overhead line can generally be represented by a capacitance. In the case of short lines (< 200 km), this capacitance can be considered concentrated, but in the case of long

lines, it should be considered distributed. Typical capacitance values vary from 9 nF/km per phase for single conductor overhead lines to 14 nF/km per phase for four-conductor bundle overhead lines (see also [127]).

Owing to the distributed nature of the inductance and the capacitance of the line, the peak value of the power frequency voltage at the remote (or receiving) end is higher than that at the circuit breaker (sending) end of the line. This effect is called the *Ferranti effect*. For a line length of 500 km, the voltage increase is approximately 4 % and approximately 1 % for a line of 200 km. That is why the Ferranti effect is not considered for line lengths below 200 km.

Figure 115 gives an approximation of the line charging current per km of different line configurations at 60 Hz. If the estimated current is greater than 90 % of the preferred line current rating, a more accurate calculation based on the actual line configuration and methods similar to that discussed in Gabrielle, et al. [127] should be used.

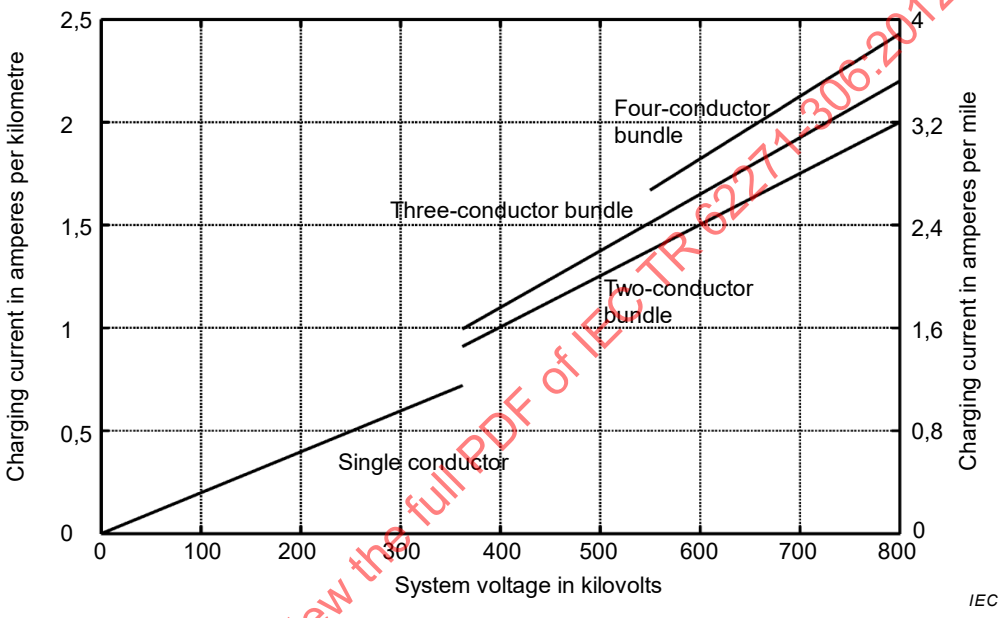


Figure 115 – RMS charging current versus system voltage for different line configurations at 60 Hz

From Figure 115, the capacitive reactance can be derived as follows.

Assume a system with a rated voltage of 245 kV, 60 Hz. The charging current is 0,5 A/km. The linear capacitive reactance X_C' is then:

$$X_C' = \frac{1}{\omega C'} = \frac{U}{I'} = \frac{245\,000\ \text{V}}{\sqrt{3} \times 0{,}5\ \text{A/km}} = 0{,}283\ \text{M}\Omega\,\text{km}\ ,$$

where

X_C' is the linear capacitive reactance of the line (MΩ km);

C' is the capacitance of the line (F/km);

I' is the charging current of the line (A/km);

U is the system voltage (kV).

For a 50 Hz system frequency, the corresponding value of X_C' would be

$$0{,}283 \times \frac{60}{50} = 0{,}34\,\mathrm{M\Omega\,km}$$

To calculate the reactance X_c of a line with a given length l, the linear reactance X_c' has to be divided by the length:

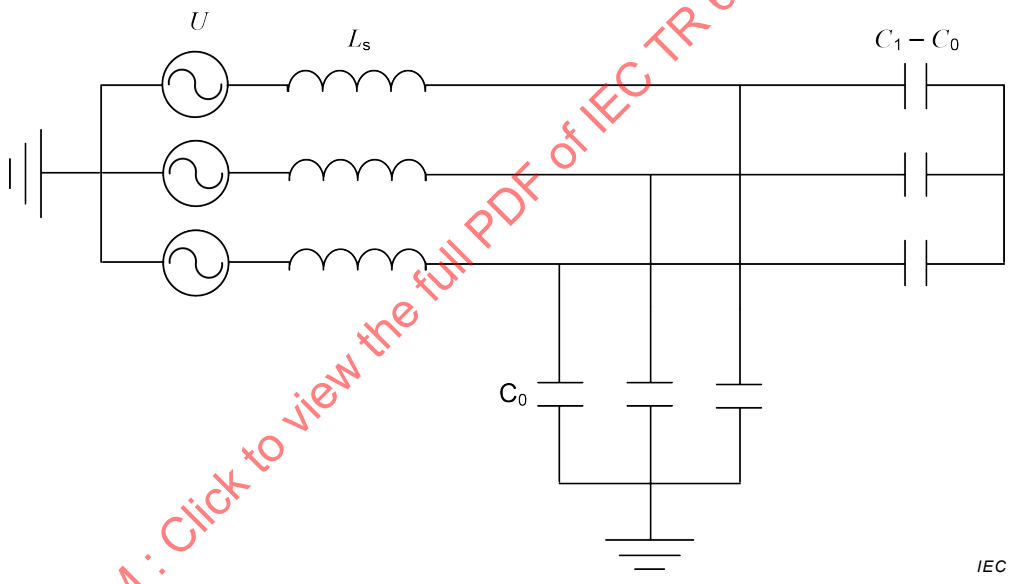
$$X_c = \frac{X_c'}{l}$$

Assume a length of 100 km for the example above. The reactance X_c is then:

$$X_c = \frac{X_c'}{l} = \frac{0{,}283\,\mathrm{M\Omega km}}{100\,\mathrm{km}} = 2{,}83\,\mathrm{k\Omega}\,.$$

9.5.1.2 Recovery voltage

Transmission lines have capacitance both between phases and to ground. Figure 116 shows a general circuit that can be used to analyse the phenomena associated with no-load transmission line switching.



Key

U	Source voltage
L_s	Source inductance
C_0	Zero sequence capacitance
C_1	Positive sequence capacitance

Figure 116 – General circuit for no-load transmission line switching

Overhead lines in transmission systems typically have C_1/C_0 ratios in the order of 2,0. Figure 117 shows the peak value of the recovery voltage in the first-pole-to-clear as a function of the capacitance ratio C_1/C_0 (positive to zero sequence capacitance). The recovery voltage peak is the differential voltage of the source and line sides, including the effects of coupled voltage on the first cleared pole. In this case Figure 117 shows that the recovery voltage peak is approximately 2,4 p.u. It follows that the voltage factor for single-phase testing to cover three-phase interruption is equal to 1,2. It has been assumed that the amplitude approaches 3 p.u. This is the case without capacitance to earth and delayed interruption of the second phase. An example of the voltages in such a case is given in

Figure 103. The other extreme, C_1 = C_0, is the case where each phase has capacitance to earth only. The recovery voltage peak is then 2 p.u. as in a single-phase case.

Overhead lines in transmission systems typically have capacitance both between phases and to earth. Figure 103 and Figure 117 assume that the second and third poles interrupt 90° after the first.

When the characteristics of the voltage in service (shape and peak value) are deviating from those of the test voltage, the restrike probability may increase. For example, if the line is compensated, the line side component is not a trapped voltage resulting from the trapped charge, but a voltage oscillating with a frequency determined by the compensating reactors and the line side capacitance (see 9.5.2).

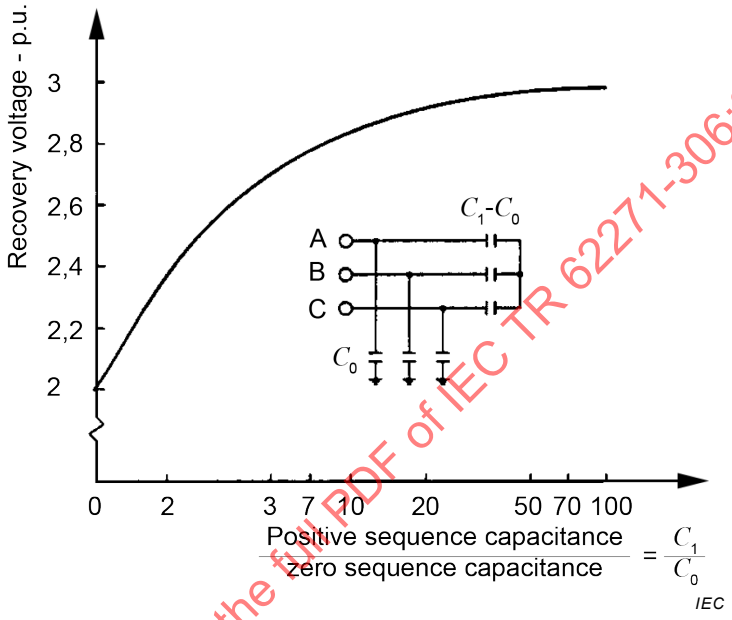


Figure 117 – Recovery voltage peak in the first-pole-to-clear as a function of C_1/C_0, delayed interruption of the second phase

If the C_1/C_0 ratio is greater than 2, higher voltages may be coupled to the first pole-to-clear, resulting in increased probability of restrike. In this case, the manufacturer should also be consulted since circuit-breaker designs are sensitive to both current magnitude and recovery voltage waveshapes.

9.5.2 De-energisation of compensated transmission lines

9.5.2.1 General

Long overhead lines are often compensated with shunt reactors to reduce the charging current of the line. The compensation factor (k_L) of an overhead line is given by the ratio of the capacitive reactance ($X_{C,line}$) to the inductive reactance ($X_{L,reactor}$) of the compensating reactor, in Equation (174):

$$k_L = \frac{X_{C,line}}{X_{L,reactor}} \quad (174)$$

If $X_{L,reactor}$ > $X_{C,line}$, the line is undercompensated, a line with $X_{L,reactor}$ < $X_{C,\ line}$ is called overcompensated.

9.5.2.2 Line charging current

The compensated line charging current is given by $I_{Lc} = I_c'(1 - k_L)$

where

I_{Lc} is the line charging current of the compensated line;

I_c' is the line charging current of uncompensated line;

k_L is the compensation factor.

Assuming a line compensated at 60 % (i.e. k_L = 0,60), the line charging current is $I_{lc} = I_c' \times (1 - 0{,}6) = 0{,}4 I_c'$, or 40 % of the uncompensated value.

9.5.2.3 Recovery voltage

If the line is compensated, the line side component of the recovery voltage is no longer a DC voltage, but an oscillation of which the frequency is determined by the compensating reactor and the line capacitance.

The resonant frequency is approximated by:

$$f_L \approx \frac{1}{2\pi\sqrt{LC}} = f_s \sqrt{\frac{X_{C,\,line}}{X_{L,\,reactor}}} = f_s \sqrt{k_L} \qquad (175)$$

where

f_L is the resonance frequency of the compensated line (Hz);

L is the inductance of the reactor (H);

C is the total capacitance of the line (F);

f_s is the system frequency (Hz);

k_L is the compensation factor.

In other words: the resonance frequency of a compensated line is dependent on the degree of compensation. Since the compensation usually is less than 1, this resonance frequency is less than the system frequency, resulting in a reduction of the rate-of-rise of the recovery voltage. Typical current and voltage waveshapes are given in Figure 118.

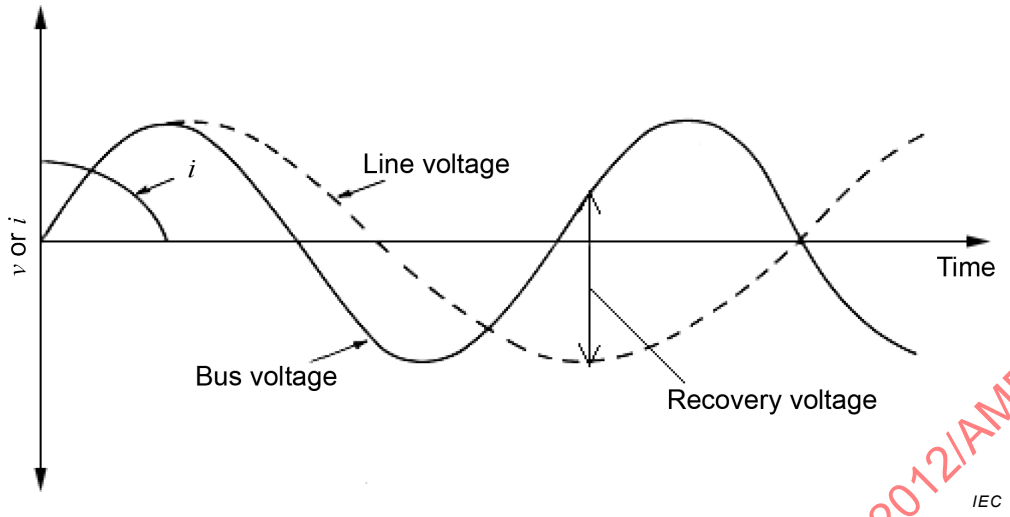


Figure 118 – Typical current and voltage relations for a compensated line

The first half-cycle of recovery voltage is, for this example, as shown in Figure 119. Compensation thus results in a decrease of the probability of restrike at a particular current. Under these conditions, improved performance may result, the circuit-breaker having a lower probability of restrike. The manufacturer should be consulted on applications which markedly alter the recovery voltage.

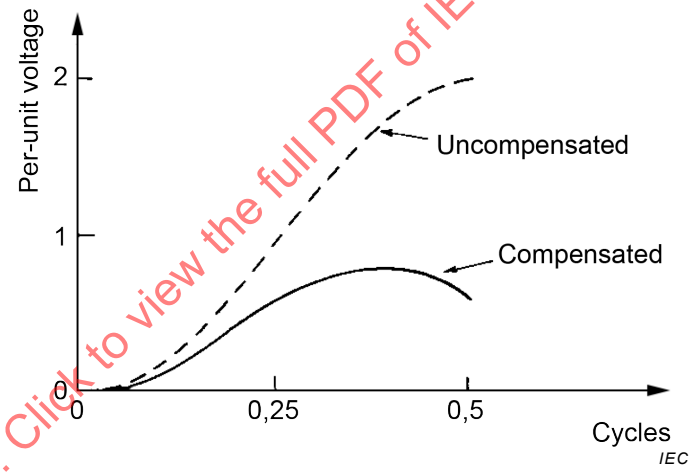


Figure 119 – Half cycle of recovery voltage

9.5.3 Energisation and re-energising transmission lines

9.5.3.1 General

For this case inrush currents are of no significance due to the high surge impedance of the lines. However, overvoltages are an issue due to travelling waves on the lines. Typically, the line is uncharged when being switched but voltage doubling is possible due to reflections from the open end of the line. A worst case can occur during high-speed reclosing when a restrike occurs at a source voltage peak of opposite polarity to the trapped charge on the line.

At voltages of 300 kV and above, mitigation measures are applied to limit the above switching overvoltages. The measures include opening resistors, metal oxide surge arresters and controlled switching.

When a transmission line is switched onto an energised network, a voltage wave is imposed on the line. The resulting phenomena are similar to those of energizing a cable. The imposed

wave will be reflected at the far end of the line and when the line is open at the far end (or terminated by a high-impedance load for high frequencies), the reflected wave results in doubling of the amplitude as shown in Figure 120.

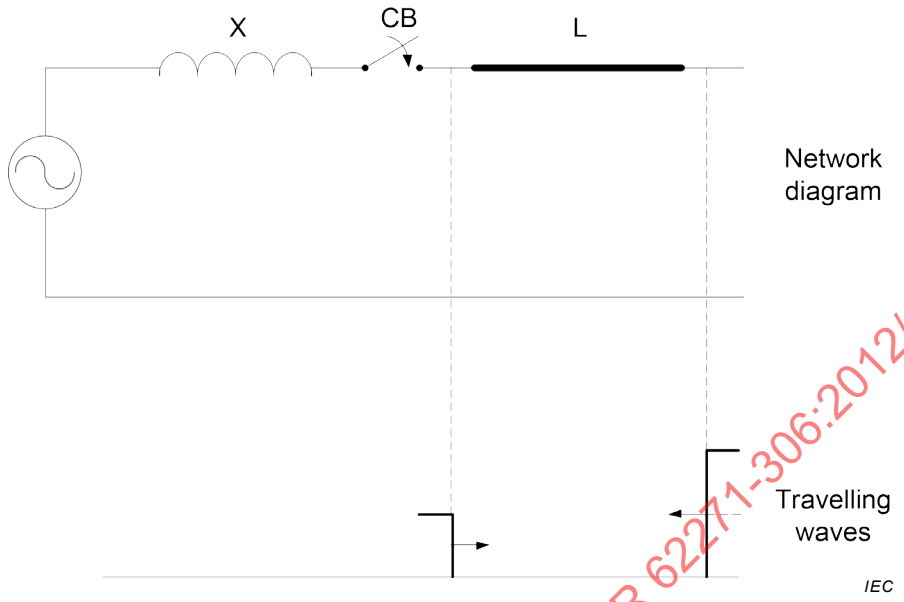


Figure 120 – Energisation of no-load lines: basic phenomena

An even higher voltage is obtained when the line has a trapped charge before being energized and the circuit-breaker happens to close at an instant when the polarity of the network voltage is opposite to that of the voltage that was present on the line. The voltage on the line can, after reflection of the wave, theoretically be up to three times the network voltage. This situation can occur in conjunction with auto-reclosing of a line.

Even higher voltages can develop on a three-phase line, when the three circuit-breaker poles are not closing simultaneously. A wave on one phase will then generate induced waves on the other phases and under unfavourable circumstances this can lead to a further rise in voltage on another phase.

9.5.3.2 Reclosing on a compensated transmission line

Similar phenomena as described under 9.4.4.2 also apply to fully compensated lines. Especially during reclosing of the healthy phases after the interruption of a single-phase short-circuit, the circuit-breaker may close at or near source voltage zero. This will result in delayed current zero crossings. Not all circuit-breakers may be suited for this application. For further information, refer to Annex B.

9.5.3.3 Long transmission line switching considerations

Overhead lines exceeding 200 km, even those of simple construction type, present a special case not covered by the requirements of 6.111.7 of IEC 62271-100:2008 or its notes. Where such long lines are to be switched, consideration should be given to the higher value of peak recovery voltage present on interruption. Some idea of the ability of a particular circuit-breaker for making and breaking of this requirement can be gained by considering any out-of-phase switching evidence that may exist. Such evidence will usually provide adequate demonstration of the elevated recovery voltage. For full compliance, evidence will be required to satisfy the capacitive current switching requirements of 6.111 of IEC 62271-100:2008, but to the elevated values required by the specific application.

Some users may be concerned about rare or occasional switching operations from one end on a series of long lines. This can occur during the early development stages of a system when

intermediate substations may not be fully equipped or may even be by-passed. In such cases, it may be appropriate to consider the out-of-phase capability in relation to the combined load presented by the series of lines. If satisfactory for the current and voltage conditions, then specific testing for the severe capacitive current switching duty of IEC 62271-100 would not be necessary at the enhanced levels of the extended line. They would be required for the switching duty of the individual lines of the series, as normal.

9.6 Voltage factors for capacitive current switching tests

Depending on the capacity of a high-power laboratory, capacitive current switching tests may be performed as three-phase tests or single-phase tests. For the higher voltages (362 kV, 420 kV, 550 kV and 800 kV), unit tests are generally carried out.

Especially when single-phase tests are made to cover three-phase application, the test voltage should reflect the application of the circuit-breaker in the field. One of the factors influencing this is the earthing situation of the network. The other is the presence of single or two-phase faults (see 9.8 of this document and Annex S of IEC 62271-100:2008/AMD2:2017.

Subclause 6.111.7 of IEC 62271-100:2008 gives the following voltage factors for single-phase test voltage (see Table 43). In accordance with IEC 62271-100, the test voltage measured at the circuit-breaker location prior to interruption shall not be less than the rated voltage $U_r/\sqrt{3}$ and the voltage factors given in Table 43.

Table 43 – Voltage factors for single-phase capacitive current switching tests

Voltage factor k_c	Application
1,0	Tests corresponding to normal service in solidly earthed neutral systems without significant mutual influence of adjacent phases of the capacitive circuit, typically capacitor banks with solidly earthed neutral and screened cables.
1,2	Test on belted cables and line-charging current switching [a] corresponding to normal service conditions in solidly earthed neutral systems with mutual influence of adjacent phases of the capacitive circuit for rated voltages 52 kV and above.
1,4	1. breaking during normal service conditions in systems having a non-effectively earthed neutral including screened cables [b]; 2. breaking of capacitor banks having a non-effectively earthed neutral; 3. test on belted cables and line-charging current switching [b] corresponding to normal service conditions in effectively earthed systems for rated voltages less than 52 kV;
NOTE 1 The voltage factors for line-charging current switching tests of 1,2 and 1,4 are applicable to single-circuit line construction. Requirements for multiple overhead line constructions may be greater than these factors. NOTE 2 The 1,4 factor is a compromise and is valid for breaking of capacitive currents in non-effectively earthed systems, where the second and third-pole-to-clear interrupt 90° after the first. NOTE 3 When the non-simultaneity of contact separation in the different poles of the circuit-breaker exceeds 1/6th of a cycle of rated frequency, IEC 62271-100 recommends to raise the voltage factor or to make only three-phase tests. Such circuit-breakers fall outside the scope of the standard. [a] Under the condition that the line can be replaced partly or fully by a concentrated capacitor bank. [b] When a significant capacitance to earth on the source side is present, the factor will be reduced.	

The voltage factor 1,4 is explained as follows (see Figure 121):

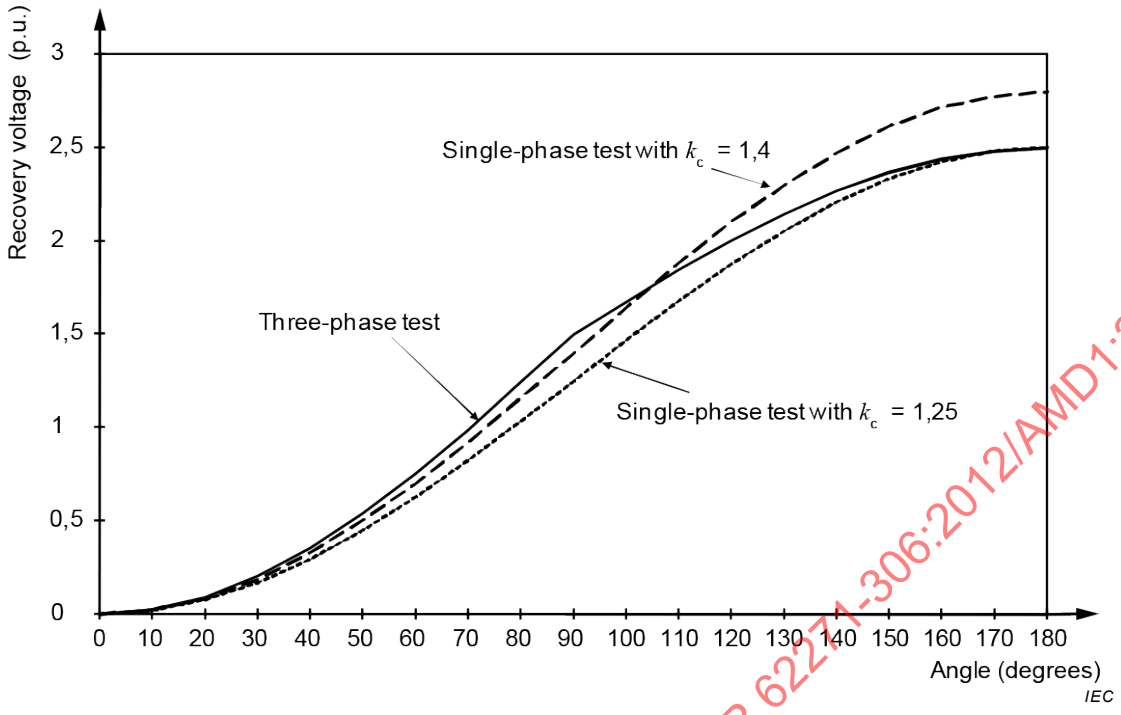


Figure 121 – Recovery voltage on first-pole-to-clear for three-phase interruption: capacitor bank with isolated neutral

When the current in the first pole is interrupted, the voltage across the circuit-breaker will rise as if the voltage factor would have been 1,5. When the second and third pole interrupt 90° later, there is a discontinuity and the recovery voltage across the first-pole-to-clear will follow a 1-cosine wave with a voltage factor of 1,25. The recovery voltage is indicated by the solid line in Figure 121. By using a voltage factor of 1,25 (dotted line in Figure 121), the initial portion of the recovery voltage across the first pole is not adequately covered. Using a voltage factor of 1,5 will result in too high a stress. A voltage factor of 1,4 as indicated by the dashed curve in Figure 121 is a compromise that adequately covers the actual recovery voltage.

Careful consideration should be given to these voltage factors when circuit-breakers are relocated to other parts of the system where the application is different from that of the original location.

As indicated in footnote a) to Table 43, the voltage factors given in Table 43 are associated with single circuit line constructions and are chosen to accommodate all known physical arrangements of the conductors of such circuits. Footnote b) to Table 43 indicates that energisation of the case of multiple overhead line constructions that have parallel circuits may require a voltage factor greater than 1,2 and 1,4. This is because such circuits are likely to have an enhancement to the line side residual voltage following interruption. This is associated with the coupling (pick-up) from the parallel circuit and may add a power frequency peak voltage of up to 0,2 p.u. This is dependent upon the geometry of the conductor systems of the two circuits.

In addition, the effect of these changes on the line side voltage, following interruption by the first-pole-to-clear, does affect the shape of the TRV across that opening pole. Consideration of this may require additional testing if the existing factor does not adequately cover the combined effects. Alternatively, the higher of the given values, e.g. 1,4 for 1,2, can be selected to encompass the specific waveshape.

On occasion, utilities have specified a voltage factor of 1,3 instead of 1,2 for double circuit lines.

9.7 General application considerations

9.7.1 General

The capacitive current switching capability of the circuit-breaker is depending on its rated voltage, rated frequency, the particular application (i.e. overhead line, capacitor bank, etc.) and the earthing conditions of the network.

Caution should be exercised when applying older circuit-breakers that have not been rated to IEC 62271-100.

9.7.2 Maximum voltage for application

The operating voltage should not exceed the rated voltage since this is the upper limit for operation.

9.7.3 Rated frequency

The rated frequency for circuit-breakers is 50 Hz or 60 Hz. As described in 9.2.1.3, a rated frequency of 60 Hz results in a more severe stress on the circuit-breaker, since the voltage peak occurs earlier (at 8,3 ms) than in the case of 50 Hz (10 ms).

Special consideration should be given when comparing tests performed at 60 Hz to cover 50 Hz requirements or vice versa. At lower frequencies, the capacitance current switching ability will be adequate. The switching capability demonstrated at 60 Hz covers the requirements for 50 Hz with the same voltage factor.

9.7.4 Rated capacitive current

9.7.4.1 General

The preferred values of the rated capacitive switching current are given in Table 9 of IEC 62271-100:2008. Not all actual cases of capacitive current switching are covered by that table. The values for lines and cables cover most cases, the values of the current for capacitor banks (single and back-to-back) are typical for some capacitor banks in service.

9.7.4.2 Overhead lines and cables

Depending on length, the no-load current of lines and cables may exceed that given in Table 9 of IEC 62271-100:2008.

The following may serve as an example: the no-load current of a two bundle conductor 550 kV transmission line is approximately 1,1 A/km at 50 Hz and 1,3 A/km for 60 Hz.

Without considering the Ferranti effect (see 9.5.3.3), the charging current of a 500 km line would be 605 A at 50 Hz and 715 A at 60 Hz. Ferranti rise on a 500 km line would increase the charging current by about 4 % at 50 Hz and 6 % at 60 Hz. This is not covered by Table 9 of IEC 62271-100:2008.

The higher current does not pose a problem for circuit-breakers of present design, since the higher current tends to increase the minimum arcing time resulting in a wider contact gap when the recovery voltage reaches its peak. The possible peak recovery voltage present on interruption could be a problem (see 9.5.3.3).

9.7.4.3 Capacitor banks

The same remark as given under 9.7.4.2 applies to capacitor bank currents. The current is dependent on the size of the capacitor bank and, in certain cases, the capacitor bank considered may have a current rating higher than that given in Table 9 of IEC 62271-100:2008. This does not pose a problem for circuit-breakers of present design.

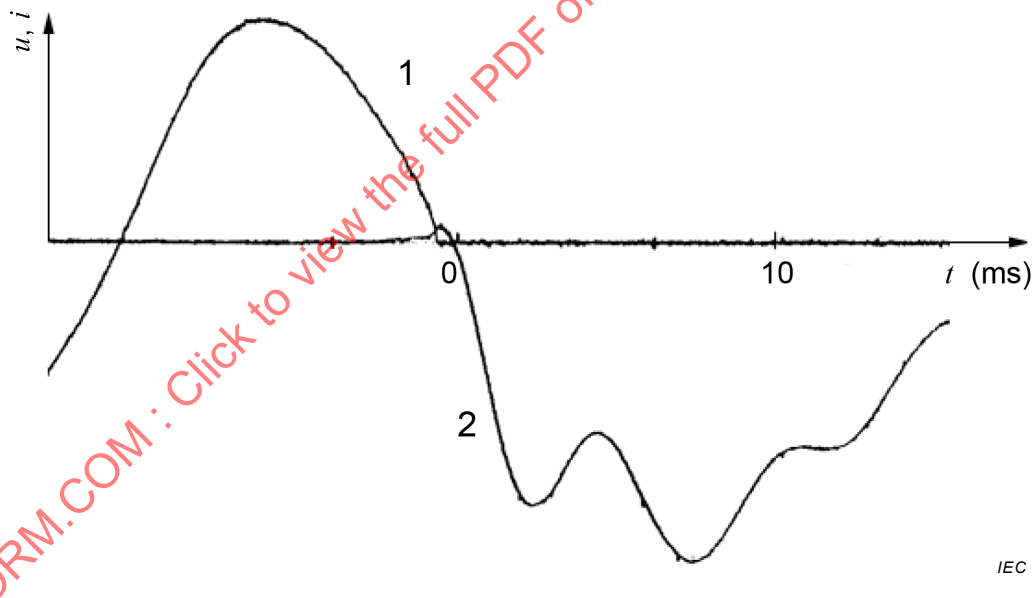
9.7.5 Voltage and earthing conditions of the network

Subclause 6.111.7 of IEC 62271-100:2008 gives the multiplication factors for single-phase tests for the different conditions, refer to 9.6. They range from 1,0 for solidly earthed systems to 1,7 for non-effectively earthed systems in the presence of single- or two-phase to earth faults.

Both user and manufacturer should be aware of these earthing conditions in order to specify the correct circuit-breaker suitable for the application.

Harmonic filter switching usually results in a recovery voltage that contains several harmonic components. The recovery voltage may have a shape as indicated in Figure 122. Careful system study should be done to define realistic requirements regarding the recovery voltage. In some cases, filter banks switching tests may need to be performed because capacitor bank switching tests do not cover the required recovery voltage waveshape. This needs to be considered when making the proper choice of circuit-breaker. From the voltage waveshape as indicated in Figure 122, it can be seen that the usual definition of re-ignition and restrike may no longer apply to a recovery voltage that does not have a 1-cosine waveshape.

In the case of a multi-frequency recovery voltage, the definition of re-ignition and restrike should be based on the amplitude of the breakdown voltage. If the amplitude is less than 1,0 p.u. of the system voltage, it is a re-ignition. If the amplitude is equal to or above 1,0 p.u. of the system voltage, it is a restrike. These definitions of restrike and re-ignition are generally acceptable but may lead to expensive solutions. More economical solutions may be obtained by permitting restrikes in a zone where tests have demonstrated that they are not harmful to the circuit-breaker.



Key

1 Current through circuit-breaker

2 Voltage across circuit-breaker

Figure 122 – Example of the recovery voltage across a filter bank circuit-breaker

9.7.6 Restrike performance

See 3.3.

9.7.7 Class of circuit-breaker

The choice of the class of circuit-breaker is discussed in 3.3.

9.7.8 Transient overvoltages and overvoltage limitation

9.7.8.1 General

An important consideration for application of circuit-breakers for capacitive current switching is the transient overvoltage that may be generated by restrikes during the opening operation. The transient overvoltage factor is defined as the ratio of the transient voltage appearing between a circuit-breaker disconnected terminal and the neutral of the disconnected capacitance during opening to the operating line-to-neutral crest voltage prior to opening.

The selection of the class (see 9.7.7) of circuit-breaker to be applied should be coordinated with the insulation capability of other components on the system.

9.7.8.2 Overvoltages

9.7.8.2.1 General

When switching capacitive currents, transients are generated. These transients are associated with the restrikes when de-energising a capacitive load and with energisation of capacitive loads. These transients may cause:

– insulation degradation and possible failure of the substation equipment;
– operation of surge arresters;
– interference in the control wiring of the substation;
– increase in step potentials in substations;
– undesired tripping or damage to sensitive electronic equipment.

The magnetic fields associated with high inrush currents during back-to-back energisation of either the no-load transmission line conductors or the earthing grid during back-to-back switching can induce voltages in control cables by both capacitive and electromagnetic coupling. These induced voltages can be minimized by shielding the cables and using a radial configuration for circuits (circuits completely contained within one cable so that inductive loops are not formed).

9.7.8.2.2 Switching of capacitor banks

9.7.8.2.2.1 General

The switching of capacitor banks is associated with voltage and current transients. As most modern circuit-breakers have a very low probability of restrike, the majority of the switching transients will be generated when energizing capacitor bank(s). The effects of the transients will exhibit themselves locally and at remote locations on the power system.

The high-frequency transient inrush current associated with back-to-back switching can stress other equipment in the circuit as well as the circuit-breaker. Wound-type current transformers will have turn-to-turn insulation stressed because of the high rates of rise of current and the resulting voltage that is developed across inductance in the circuit.

9.7.8.2.2.2 Local effects

– voltage transients resulting in dielectric stresses on nearby equipment;
– electrical, mechanical and electromechanical forces caused by the inrush current.

9.7.8.2.2.3 Remote effects

– transfer of capacitively coupled fast transients through transformer windings;
– reflections of travelling wave transients on open ended lines or transformer terminated lines;

– excitation of near resonant portions of the power system by the oscillatory transient frequency.

9.7.8.2.3 Switching of lines and cables

When energizing lines and cables, high overvoltages may be created depending on whether or not the line or cable was precharged as a result of a preceding breaking operation (i.e. in the case of an auto-reclosing). These overvoltages may result in damage of insulation.

9.7.8.3 Overvoltage limitation

There are several means available to reduce the overvoltages generated by the switching of capacitive currents:

– **current limiting reactors** are normally used to reduce the current transients associated with back-to-back switching. They do not limit the remote overvoltages.

– **pre-insertion resistors** limit the inrush current and remote overvoltages. It is a basic solution used on circuit-breakers. They are usually fitted on circuit-breakers and as such add to the complexity of the equipment. Depending on the design, the added complexity may or may not result in a reduced availability of the equipment (see also 9.7.16).

– **pre-insertion reactors** also limit the inrush current and remote overvoltages. They are usually fitted on circuit-switchers and their effect on complexity and availability of the equipment is sometimes equivalent to pre-insertion resistors, depending on the design of the devices.

– **controlled closing** reduces the magnitude of the inrush current depending on the point-on-wave of the voltage prior to the prestrike between the contacts. A simple way of reducing the transients is to let the circuit-breaker contacts close at a voltage zero. This method is called controlled closing. The controller also adds to the complexity of the equipment and can influence its availability.

9.7.9 No-load overhead lines

9.7.9.1 General

A circuit-breaker may be required to energise or de-energise a no-load transmission line during its normal operating duties. Prior to energisation, the line may or may not contain a trapped charge (see also 9.5.3). Consideration may need to be given to line energisation following load rejection (see [127]).

9.7.9.2 Line charging current

When considering the assigned line charging current rating, application is determined by the value of the line charging current. This current is a function of system voltage, line length, and line configuration (see also 9.5.1.1).

9.7.9.3 Compensated overhead lines

As described in 9.5.2 very long lines (> 200 km) are often compensated with shunt reactors to reduce the amount of charging current required of the system.

If the circuit-breaker rating is chosen based on I_{Lc}, the line could not be switched without the compensating reactor(s) connected. The voltage rise caused by the Ferranti effect and also the location of the reactor(s) will change the line current slightly.

9.7.9.4 No-load line recovery voltage

The line-charging breaking current rating is assigned on the basis of a standard recovery voltage associated with this type of circuit. For solidly earthed systems, the no-load line charging current switching tests require a maximum voltage of 2,4 times (see also 9.5.1.2) the rated phase-to-earth voltage across the circuit-breaker one half-cycle after interruption

(assumes C_1 = $2C_0$ where C_1 is the positive-sequence capacitance and C_0 is the zero-sequence capacitance). This is the difference voltage of the source and line sides, including the effects of coupled voltage on the first-pole-to-clear. The test voltage requires a 1-cosine waveshape.

For double circuit lines with higher voltage factors refer to 9.6.

Deviations from the test voltage characteristics may increase or decrease the probability of the circuit-breaker restriking. As described in 9.5.2, a compensated line will have a lower rate-of-rise of the recovery voltage, which will reduce the restrike probability.

9.7.10 Capacitor banks

9.7.10.1 General

A circuit-breaker may be required to switch a capacitor bank from a bus that does not have other capacitor banks energised (single) or against a bus that has other capacitor banks energised (back-to-back). In the application of circuit-breakers for capacitor switching duty, consideration should be given to the preferred single shunt capacitor bank switching current, preferred back-to-back shunt capacitor bank switching current, preferred transient inrush current, and preferred transient inrush current frequency (see also 9.3.2 and 9.2.2).

9.7.10.2 Capacitor bank current

Circuit-breakers are to be applied according to the actual capacitive current they are required to interrupt. The rating should be selected to include the following effects.

a) *Voltage.* The reactive power rating of the capacitor bank, in kvar, is to be multiplied by the ratio of the maximum service voltage to the capacitor bank nameplate voltage when calculating the capacitive current at the applied voltage. This ratio can be as large as 1,1, since capacitors can be operated continuously up to 10 % above the capacitor rated voltage.

b) *Capacitor tolerance.* The manufacturing tolerance in capacitance is −0 to +15 % with a more frequent average of −0 to +5 %. A multiplier in the range of 1,05 to 1,15 should be used to adjust the nominal current to the value allowed by tolerance in capacitance.

c) *Harmonic component.* Capacitor banks provide a low-impedance path for the flow of harmonic currents. When capacitor banks are non-effectively earthed, no path is provided for zero-sequence harmonics (third, sixth, ninth, etc.), and the multiplier for harmonic currents is less. A multiplier of 1,1 is generally used for a solidly earthed neutral bank and 1,05 for a non-effectively earthed neutral.

In the absence of specific information on multipliers for the above factors, it will usually be conservative to use a total multiplier of 1,25 times the nominal capacitor current at rated capacitor voltage for non-effectively earthed neutral operation and 1,35 times the nominal current for solidly earthed neutral operation.

9.7.10.3 Methods for calculating transient inrush currents

9.7.10.3.1 General

The capacitor bank being switched is assumed uncharged, with closing at a voltage crest of the source voltage. The current used should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the absence of specific information, a multiplier of 1,15 times normal capacitor current would give conservative results.

9.7.10.3.2 Single capacitor bank

A bank of shunt capacitors is considered single when the conditions described in 9.3.3.1 are fulfilled. Table 44 gives the equations that apply for calculation of the inrush current for single capacitor bank energisation, neglecting resistance.

Table 44 – Inrush current and frequency for switching capacitor banks

Duty	Quantity	Equation
Energisation of single bank	$i_{\text{i peak}}$ (A)	$\frac{\sqrt{2}U_{\text{r}}}{\sqrt{3}} \times \sqrt{\frac{C}{L_{\text{s}}}}$
	f_{i} (Hz)	$\frac{1}{2\pi\sqrt{L_{\text{s}}C}}$
Back-to-back switching	$i_{\text{i peak}}$ (A)	$\frac{\sqrt{2}U_{\text{r}}}{\sqrt{3}} \times \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}}$
	f_{i} (Hz)	$\frac{1}{2\pi\sqrt{L_{\text{eq}}C_{\text{eq}}}}$

Key

U_{r}: rated voltage (V)*
C: bank capacitance (F)*
L_{s}: source inductance (H)*
C_{eq}: equivalent capacitance (F)**
L_{eq}: equivalent inductance (H)**
* See 9.3.3.1.
** See 9.3.3.2.

9.7.10.3.3 Back-to-back capacitor bank

The inrush current of a single bank will be increased when other capacitor banks are connected to the same bus (see also 9.3.3.2).

Table 44 gives the equations for calculating inrush current and frequency for back-to-back capacitor bank switching, neglecting resistance. These equations are based on the theory described in 9.2.2.

A typical circuit for back-to-back switching is shown in Figure 123. The inductance in the circuit that limits the transient oscillatory current is composed of the inductance of the bus between switching devices, L_{bus}, the inductance between the switching device and the capacitor banks, L_1 and L_2, and the inductance of the capacitor banks, L_{c1} and L_{c2} and any additional reactance inserted. The total inductance between capacitor banks, $L_{\text{c1}} + L_1 + L_{\text{bus}} + L_2 + L_{\text{c2}}$, is very small with respect to the inductance of the source L_{s}. In most cases, the total inductance between capacitor banks will be less than 1 % of the inductance of the source, and the contribution of transient current from the source can be neglected.

The inductance of the bus can be calculated similar to a transmission line using values from tables available from suppliers of bus conductors for different bus configurations (see 9.7.10.3.4).

The inductance within the capacitor bank itself is not easy to obtain, but in general it is of the order of 10 µH for banks above 52 kV, and 5 µH for banks below 52 kV. Typical values of

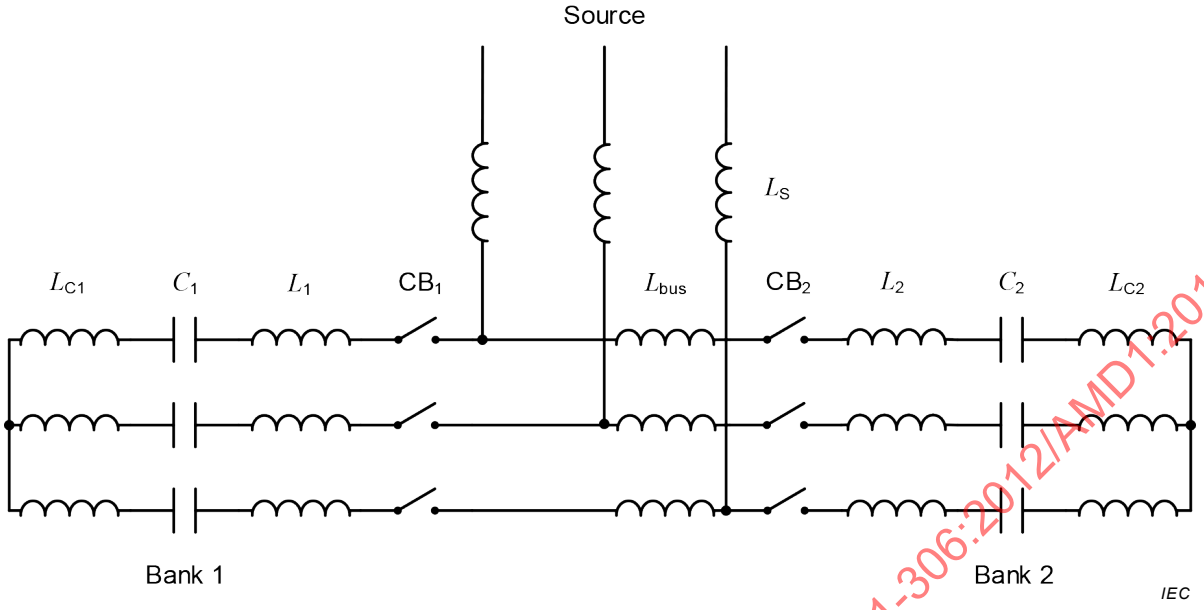
inductance per phase between back-to-back capacitor banks and bank inductance for various voltage levels are given in Table 45.

Table 45 – Typical values of inductance between capacitor banks

Rated maximum voltage (kV)	**Inductance per phase of busbar** (μH/m)	**Typical inductance between banks** [a] (μH)
17,5 and below	0,702	10 to 20
36	0,781	15 to 30
52	0,840	20 to 40
72,5	0,840	25 to 50
123	0,856	35 to 70
145	0,856	40 to 80
170	0,879	60 to 120
245	0,935	85 to 170

[a] Typical values of inductance per phase between capacitor banks. This does not include inductance of the capacitor bank itself. Values of 5 μH for banks below 52 kV and 10 μH for banks above 52 kV are typical for the inductance of the capacitor banks.

Inherent resistance of the circuit causes rapid decay of the transient current so that the first peak actually may only reach 90 % to 95 % of the maximum value calculated. These values are applicable to both solidly earthed or isolated capacitor banks and with Y or Δ connections. With a non-effectively earthed neutral, the current in the first two phases to close will be 87 % of calculated, but the current in the last phase will equal the value calculated. However, inherent resistance of the circuit will affect these currents by the factors indicated above.



Key

CB_1	circuit-breaker energizing capacitor bank 1
CB_2	circuit-breaker energizing capacitor bank 2
L_S	source inductance
C_1	capacitor bank 1
C_2	capacitor bank 2
L_{C1}, L_{C2}	capacitor bank inductance
L_1, L_2	bus inductance between switching device and capacitor bank
L_{bus}	inductance of bus between switching devices

Figure 123 – Typical circuit for back-to-back switching

The equations in Table 44 for back-to-back switching will give correct results when switching a bank against another bank. However, when switching against several other banks connected to the bus, the correct value of equivalent inductance to be used for the combination of banks connected to the bus is not easily obtained. For example, when switching a bank against three other banks energised on the bus, the calculated current will be too high if an inductance of $L/3$ is used. On the other hand, using a value of $3L$ will result in a current that is too low. If exact solutions cannot be made, conservative results should be used in calculating inrush currents by using the inductance divided by the number of capacitor banks, recognizing that the results will be 20 % to 30 % higher (see also 9.3.3.2). When more than two banks are installed on the same bus, a more exact calculation of the inrush current parameters is obtained using an electromagnetic transient program.

9.7.10.3.4 Considerations for transient inrush currents

The inrush currents of different types of compact multi-section banks with minimum spacing between the individual sections may differ by as much as 20 %. Consequently, these inrush currents can be reduced significantly by increasing the lengths (inductance) of the circuits between the sections.

Another effective measure to reduce transient inrush currents is to add inductance in the circuit between the capacitor banks.

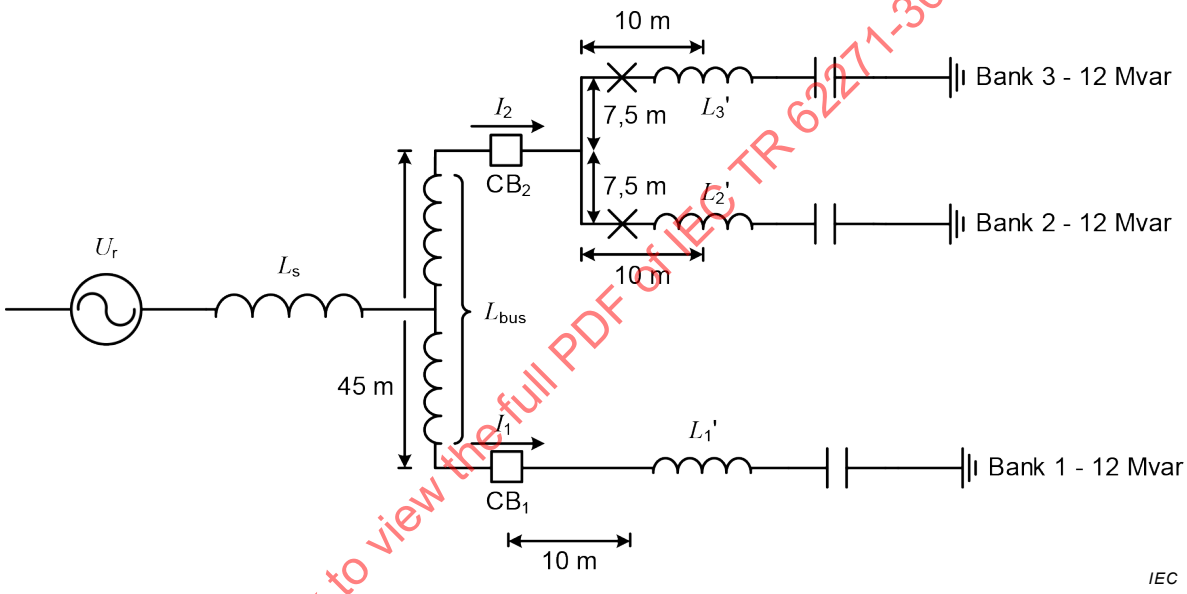
In IEC 62271-100:2001, the equivalency rule between the test performed and the service conditions was based on the product of inrush current peak and frequency, $i_{\text{i peak}} \times f_{\text{i}}$ (kAkHz). Calculations have shown that the arc energy during a making operation is independent of the inrush current frequency for cases where the pre-arcing time is greater than half a period of the inrush current frequency. This is usually the case for back-to-back

capacitor bank switching. For back-to-back capacitor bank switching, the arc energy during a making operation is only a function of the inrush current peak. On the other hand, it is well known that the shape of the wear on the arcing contacts as well as the effect of the pressure shock waves are somewhat frequency-dependent and should not be disregarded. Because of the latter, an upper tolerance of +130 % has been specified on the permissible inrush current frequency that can be used in service. In other words: the inrush current frequency used during the tests should not be lower than 77 % of the inrush current frequency foreseen in service. This concept is limited to inrush current frequencies up to 6 kHz since the information available for higher frequencies is limited.

Although circuit-breakers have usually been tested with inrush current peaks up to 20 kA and 4,25 kHz, system designers should endeavour to keep the inrush currents far below this value for system quality reasons.

The following example will illustrate the use of the equations in Table 44.

A 123 kV system is assumed as shown in Figure 124.



Key

U_r	123 kV (the rated capacitor bank voltage is 115 kV)
L_S	Source inductance is 3,77 Ω, 10 mH (f_s = 60 Hz)
L_1', L_2', L_3'	Inductance between circuit-breaker and capacitor bank; including inductance of capacitor bank
L_{bus}	Inductance of bus between switching devices
CB_1, CB_2	Circuit-breakers
	Short-circuit of source: 18 600 A at 123 kV

Figure 124 – Example of 123 kV system

The capacitor banks shown have a nominal rating of 12 Mvar (capacitors rated 100 kvar, 13,28 kV, 5 series sections with eight capacitors in parallel per phase). Nominal current per bank is 60 A. In determining the rating of the circuit-breaker required, the increase in current due to applied voltage, capacitance tolerance, and harmonics should be considered. The increase in current at maximum rated voltage is: maximum voltage to capacitor rated voltage = 123/115 = 1,07. Assume a positive tolerance of capacitors of +10 %, multiplier of 1,1 and assume a multiplier for harmonic content for a solidly earthed neutral bank of 1,1.

The total multiplier used to determine the single and back-to-back current rating is 1,07 × 1,1 × 1,1 = 1,29, giving a current of 1,29 x 60 = 78 A. With capacitor banks 2 and 3 energised, the current through CB_2 is 156 A.

The circuit-breakers intended for this duty have the following ratings: rated voltage 123 kV, rated current 1 600 A, rated short-circuit current 40 kA, rated single and back-to-back capacitive switching current 400 A.

The transient inrush current and frequency are calculated using the equations in Table 44. In the example, L_1', L_2' and L_3' are the inductances between the respective capacitor banks and the circuit-breakers, including the inductance of the capacitor bank. L_{bus} is the inductance of the bus between the circuit-breakers.

The inductance values in Table 45 can be used or values can be calculated for the actual bus configuration used. In the example given below, the added reactance between the circuit-breaker and capacitor bank is:

L_1' = 20,0 µH

L_2' = L_3' = 27,1 µH

The inductance of the busbar L_{bus} = 38,5 µH.

In determining inrush current and frequency, the currents I_1 and I_2 as used in Table 44 should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the example, the multiplier to be used is 1,07 × 1,1 = 1,18. The currents are I_1 = 60 × 1,18 = 71 A and I_2 = 71 A or 142 A, depending on whether bank 2 or 3 or both banks are energised.

Case I. Energisation of capacitor bank 1 with banks 2 and 3 not energised (single bank switching).

Bank capacitance C for calculation:

$$C = 1{,}1 \times \frac{\text{Mvar}}{\omega U_r^2}\,(\text{F}) \text{ with } U_r \text{ in kV} \rightarrow C = 1{,}1 \times \frac{12}{377 \text{ x } (115)^2} = 2{,}65\,\mu\text{F}$$

L_s = 10 mH

$$i_{ipeak} = \frac{\sqrt{2}\left(123 \times 10^3\right)}{\sqrt{3}} \times \sqrt{\frac{2{,}65 \times 10^{-6}}{10 \times 10^{-3}}} = 1\ 635\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{10 \times 10^{-3} \times 2{,}65 \times 10^{-6}}} = 977\ \text{Hz}$$

This is less than the maximum rate of change for a rated short-circuit current of 40 kA which is equal to $2\pi f_s \sqrt{2} I_{sc} = 21{,}3$ A/µs and therefore meets the requirements of single capacitor bank switching.

Case II. Energisation of bank 1 with bank 2 energised on the bus (back-to-back switching against an equal size bank).

$$C_{eq} = \frac{2{,}65}{2} = 1{,}325\,\mu\text{F}$$

L_{eq} = 20 + 38,5 + 27,1 = 85,6 µH

$$i_{ipeak} = \frac{\sqrt{2}(123\times10^3)}{\sqrt{3}} \times \sqrt{\frac{1{,}325\times10^{-6}}{85{,}6\times10^{-6}}} = 12\,495\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{85{,}6\times10^{-6}\times1{,}325\times10^{-6}}} = 14\,944\ \text{Hz}$$

The calculated back-to-back inrush current and frequency should be compared with the back-to-back switching capability listed in Table 5 of IEC 62271-100:2008. For a maximum voltage of 123 kV, the assumed rated values are 20 kA for the peak current and 4,25 kHz for the inrush current frequency. The calculated value of the inrush current peak is within this rating, the inrush current frequency exceeds that assumed and inductance should be added between the capacitor banks to reduce the inrush current frequency. Adding an inductance of 1 mH will limit the inrush current to 3,5 kA and the frequency to 4,18 kHz, both of which are below the assumed capability.

Case III. Energisation of bank 1 with banks 2 and 3 energised on the bus.

$$C_{eq} = \frac{(2{,}65+2{,}65)2{,}65}{(2{,}65+2{,}65)+2{,}65} = 1{,}76\ \mu\text{F}$$

$$L_{eq} = \frac{(27{,}1)}{2} + 38{,}52 + 20 = 72{,}07\ \mu\text{H}$$

$$i_{ipeak} = \frac{\sqrt{2}(123\times10^3)}{\sqrt{2}} \times \sqrt{\frac{1{,}76\times10^{-6}}{72{,}07\times10^{-6}}} = 15\,694\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{72{,}07\times10^{-6}\times1{,}76\times10^{-6}}} = 14\,131\ \text{Hz}$$

Of the calculated values of inrush current peak and frequency, the frequency of 14,1 kHz exceeds the assumed back-to-back switching capability of 4,25 kHz listed in Table 9 of IEC 62271-100:2008. As in the previous case of switching identical banks, adding an inductance of 0,71 mH will limit the inrush current peak to 4,7 kA and the inrush current frequency to 4,3 kHz, both of which are below the assumed back-to-back switching capability of a 123 kV circuit-breaker.

Based on the system and conditions studied, a circuit-breaker having the following ratings would be applied: rated short-circuit current of 40 kA and rated single capacitor bank switching current of 400 A. The assumed back-to-back rating of 20 kA and 4,25 kHz that goes with this rating will be exceeded unless additional inductance is added between the capacitor banks. A value of 0,71 mH is sufficient to keep within the assumed ratings available.

9.7.11 Switching through transformers

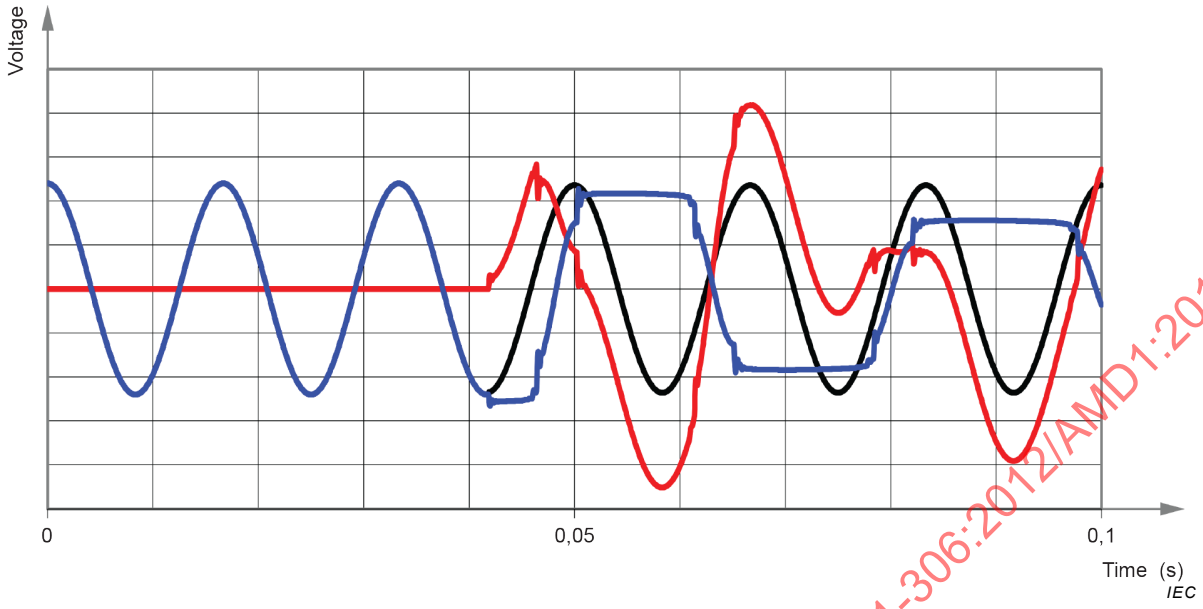
Circuit-breakers may be required in some applications to switch capacitors, lines, or cables through an interposed transformer. The current switched by the circuit-breaker will be N times the capacitor, line, or cable current on the other side of the transformer, where N is the transformer turns ratio.

Switching charging current through a transformer may be less difficult than switching the same current directly. The capacitive elements of the circuit will oscillate with the transformer inductance, which may also saturate, producing a less severe transient recovery voltage and

a lower probability of restrike. If a restrike should occur, the additional inductance will help to limit the inrush current. Saturation may also occur when de-energizing a remote transformer that is fed through a long cable. The stress on the transformer is not considered harmful.

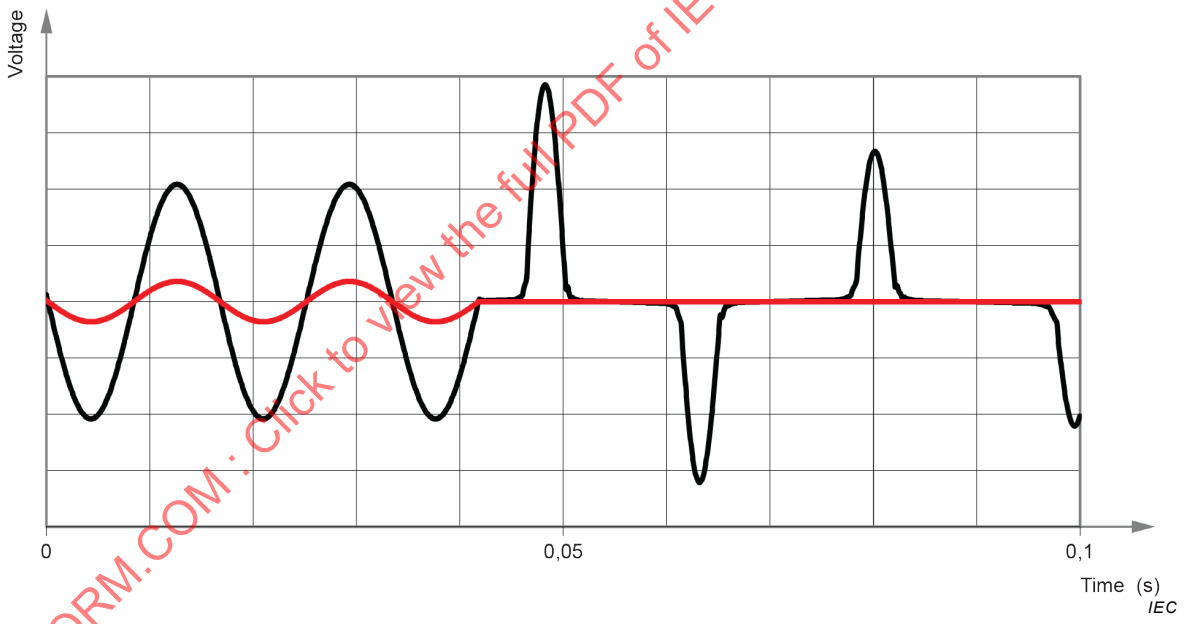
If the value of N is greater than 1, switching through a transformer will have the effect of increasing the current being switched. De-energizing no-load overhead lines with lower voltage circuit-breakers can result in effective line charging currents in the 750 A to 1 000 A range. The capacitive switching rating of circuit-breakers which may be exposed to this type of duty should be carefully checked before application is made.

Figure 125 shows the voltage and current relations that are the result of a single-phase simulation of capacitor switching through an interposed transformer. It can be seen that due to the reduced recovery voltage, the increased current is not a problem for the circuit-breaker.



Black line	Source voltage
Blue line	Voltage on the load side of the circuit-breaker
Red line	Voltage across the circuit-breaker

Figure 125a – Voltage relations



Black line	Capacitor bank current (low voltage side of the transformer)
Red line	Current through the circuit-breaker

Figure 125b – Current relations

Figure 125 – Voltage and current relations for capacitor switching through interposed transformer

9.7.12 Effect of transient currents

9.7.12.1 General

In the application of circuit-breakers in stations having banks of capacitors, it may be necessary to investigate the effects of transient currents and other special situations upon

circuit-breakers other than those specially equipped for and assigned to the routine capacitor switching.

The transient currents of capacitor banks may be considered in two aspects: the inrush currents energisation of the banks and the discharge currents into faults. Where the quantity of parallel capacitor banks installed in a station is large, the transient currents may have significant effects upon the circuit-breaker.

The transient currents may have large peaks and high frequencies which may affect circuit-breakers in the following ways:

a) a circuit-breaker may be subjected to a transient inrush current that exceeds its rating. This may occur with the circuit-breaker in the closed position or when closing into solidly earthed faults;

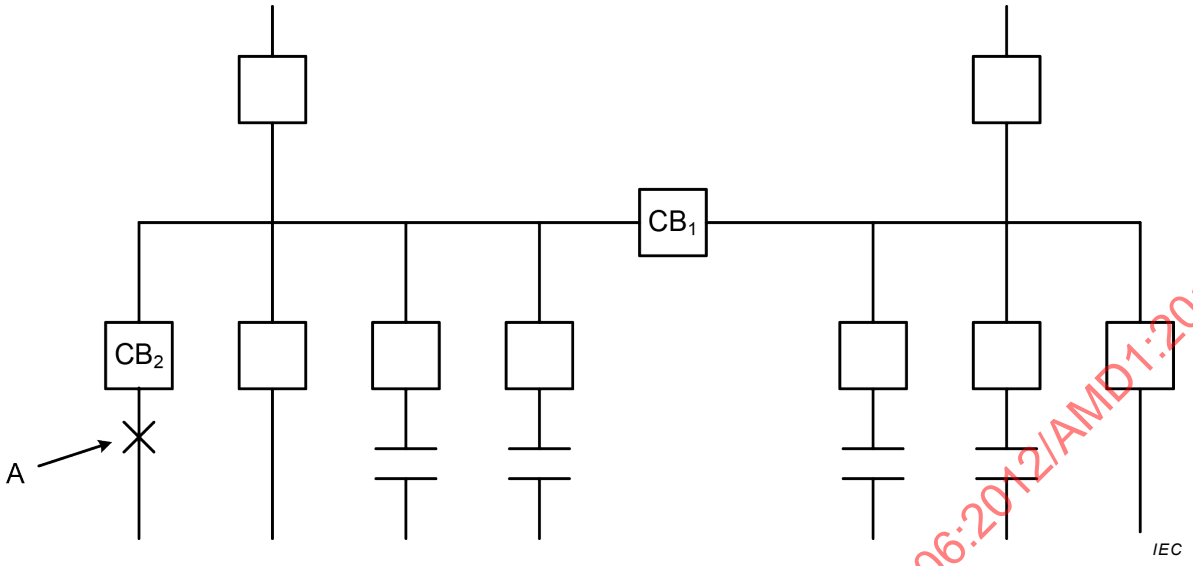
b) the transient inrush current may have sufficient magnitude and rate of change to flash over the secondaries of current transformers or the associated control wiring.

Circuit-breakers located in a position such as a tie circuit-breaker between bus sections (bus section or bus coupler) may be exposed to the transient inrush currents from energizing banks of capacitors when they are located on bus sections on both sides of the circuit-breaker (see Figure 126, CB_1).

The inrush current will seldom exceed the capability of the circuit-breaker. However, a check may be required to determine if the rate of change of inrush current will cause overvoltages on the secondary of current transformers on the circuit-breaker or in the current path between the capacitor banks.

9.7.12.2 Exposure to total capacitor bank discharge current

In a substation where parallel capacitor banks are located near or on a busbar, any circuit-breaker connected to the bus may be exposed during faults to the total discharge current of all the banks located behind the circuit-breaker. In Figure 126, CB_2 will be subjected to this total discharge current with a fault occurring at location A. The worst case, or highest capacitor discharge current, occurs with a bolted three-phase fault where capacitor banks are non-effectively earthed and for a case of a three phase-to-earth or a line-to-earth fault where capacitor banks are solidly earthed.



Key

CB_1, CB_2 Circuit-breakers

Figure 126 – Station illustrating large transient inrush currents through circuit-breakers from parallel capacitor banks

The total discharge current (peak) of all banks behind the circuit-breaker is equal to the algebraic sum of the individual banks of capacitors. Neglecting resistance, the discharge current of an individual capacitor bank is equal to:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{C}{L}} \tag{33}$$

where

$I_{\text{d peak}}$ is the crest value of discharge current;

U_{r} is the rated voltage;

C is the capacitance per phase of individual bank;

L is the inductance per phase between capacitor bank and fault location.

The inductance L is primarily made up of bus conductors and any additional inductance added to the bank for limiting the inrush currents.

If there are n capacitor banks of approximately equal capacitance and separated by an approximately equal inductance to the fault, then the total discharge current is approximately equal to the sum of the crest current of each bank or n times that of one bank. This is demonstrated as follows:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{Cn}{L/n}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} n \sqrt{C/L} \tag{177}$$

In addition to the checking of the crest current, it may be necessary also to check the rate of change of the discharge current with the manufacturer.

The transient discharge current passing through a circuit-breaker should also be examined for its effects upon the current transformers. The discharge currents may substantially exceed the magnitudes and the frequency of the inrush currents described in Table 9 of

IEC 62271-100:2008. This occurs because the contribution may come from a number of capacitor banks and is not limited by the inrush impedance seen when energizing a bank of capacitors.

9.7.13 Exposure to capacitive switching duties during fault switching

Where parallel banks of capacitors are located on bus sections in a station, caution should be exercised in the fault switching sequence so that the last circuit-breaker to clear is not subjected to a capacitive switching duty beyond its capability. This is especially a concern for a circuit-breaker used as a bus section tie circuit-breaker with capacitors located on both sides of the circuit-breaker as shown in Figure 126, CB_1.

The worst case occurs in a station where the bus section tie circuit-breaker is last to clear the bus for a fault that leaves one or more phases of the capacitor banks fully energised. In this situation, the bus tie circuit-breaker should be properly equipped and rated for the parallel switching of the capacitor banks remaining on the bus section to be de-energised. In the example of Figure 126, this means that the tie circuit-breaker should be capable of switching two banks of capacitors in parallel with two banks of capacitors on the source side. Another solution is to coordinate if possible the clearing times so that the tie circuit-breaker is always first to clear to avoid the capacitor switching duty.

9.7.14 Effect of load

The situation can occur where a circuit-breaker is called upon to switch a combination of a capacitive current and a load current. The circuit-breaker will have the required switching capability if the total current does not exceed the rated continuous current of the circuit-breaker and either

a) the power factor is at least 0,8 leading, or

b) the capacitive current does not exceed the rated capacitive switching current of the circuit-breaker.

Where the above conditions are exceeded, the capability and performance of the circuit-breaker is not defined by the standards and the manufacturer should be consulted. When the power factor is below 0,8 leading, the voltage may be sufficiently out-of-phase with the current to cause unacceptable restriking. The situation will be more severe if there is also a bank of capacitors located on the source side of the circuit-breaker.

9.7.15 Effect of reclosing

Up to twice normal inrush currents are possible when reclosing is applied to a circuit-breaker switching capacitive loads. When capacitor bank current is interrupted at or near a normal current zero, the voltage remaining on the bank may be near peak value. Reclosing a circuit-breaker against such a charged capacitor bank may produce high inrush current.

When a capacitor bank is connected to the load side of a feeder circuit-breaker equipped with automatic reclosing, high inrush currents can be avoided by isolating the capacitor bank from other loads after the circuit-breaker is tripped and before reclosing. The switching device used for regular capacitor bank switching can be employed for isolation. This technique is particularly recommended where other capacitor banks are connected to the same station bus.

A second technique to avoid high inrush currents during reclosing is to increase reclosing time delay. Normally, the discharge resistors inside each capacitor unit, or other deliberately introduced discharge devices will reduce residual voltage.

Discharge curves are available from the capacitor supplier and should be consulted where reclosing time is delayed.

9.7.16 Resistor thermal limitations

For capacitor bank circuit-breakers equipped with pre-insertion resistors, the thermal capability of the resistors should be considered in determining the time interval between capacitive current switching operations. The resistance value is related to the size of the capacitor bank and the pre-insertion resistors should normally have a thermal capability as defined by the rated operating sequence.

If capacitive current switching field tests are planned which exceed the number of operations as defined by the thermal capacity of the pre-insertion resistors, or which utilize a specially designed circuit-breaker, the manufacturer should be consulted regarding the frequency of operations.

9.7.17 Application considerations for different circuit-breaker types

9.7.17.1 General

The switching of capacitive current poses different stresses on the different types of circuit-breakers. Restrikes on opening and prestrikes on closing may or may not be a problem. The considerations given below are general and are based on experiences gained by laboratory tests, field tests and field experience.

9.7.17.2 Oil circuit-breakers

9.7.17.2.1 Restrikes

Depending on the design (contact speed, electrode shape, etc.), an oil circuit-breaker generally has long arcing times when interrupting. The restrike probability increases with increased current, because gas bubbles reduce the effective amount of oil between the contacts causing a reduction of the dielectric strength of the contact gap. These circuit-breakers deserve special consideration when used or relocated to a system where the line charging current exceeds the rating.

Some oil circuit-breakers are pressurized to reduce the size of the bubbles and therewith increasing the dielectric strength of the contact gap. Some oil circuit-breakers may be fitted with opening resistors, to reduce the effects of a restrike.

An oil circuit-breaker will normally not interrupt the high-frequency current associated with the restrike and the high arc impedance introduces an additional damping of the restrike current. This will reduce the risk for multiple restrikes.

Older contraction type oil circuit-breakers are known to produce multiple restrikes that may result in voltage escalation and subsequent development of an evolving fault.

9.7.17.2.2 Prestrikes

Oil circuit-breakers are especially sensitive to high-frequency prestrikes when energizing capacitor banks. The prestrikes cause a shock wave in the oil. As oil is not compressible, the shock wave causes mechanical stresses on the internal components of the breaking chamber. As a result of the exposure to these high mechanical stresses, the breaking chamber insulator may shatter and even stationary contacts may crack. Application of an oil circuit-breaker for capacitor bank switching requires a severe reduction of the inrush current frequency or special design of the oil circuit-breaker (e.g. using pre-insertion resistors).

Bulk oil circuit-breakers have been applied using a limitation of 20 kAkHz for over 30 years with no documented problems.

For minimum oil circuit-breakers, a value of 1 kAkHz is suggested.

9.7.17.3 Vacuum circuit-breakers

9.7.17.3.1 Restrikes

The voltage withstand of the contact gap of a vacuum circuit-breaker rises very fast and the restrike probability is low. When a restrike occurs, the contact gap is small and the vacuum circuit-breaker is usually capable of interrupting the high-frequency restrike current, which may result in voltage escalation.

9.7.17.3.2 NSDDs

NSDDs (see 9.2.1.3) are normally associated with vacuum circuit-breakers and are generally not a concern.

9.7.17.3.3 Prestrikes

The duration of the prestrike in a vacuum circuit-breaker is short. Shock waves are not a problem for this type of circuit-breaker.

The high-frequency discharge together with contact bouncing may lead to micro contact melting, especially when the arc is burning in the anode-spot mode (this occurs with currents higher than 10 kA). The breaking of welded points during a subsequent breaking operation with a very low current can damage the contact surface and this may reduce the dielectric withstand of the contact gap. However, a subsequent breaking operation with higher current may increase the dielectric withstand to its original condition. A subsequent no-load operation may flatten the micro spot resulting in an increased dielectric strength.

9.7.17.4 SF_6 circuit-breakers

9.7.17.4.1 Restrikes

The interrupting capacity of SF_6 circuit-breakers is limited by the recovery voltage, which means that the frequency and earthing conditions (i.e. whether the circuit is effectively or non-effectively earthed) are important factors in the determination of the capability of the circuit-breaker.

The capacity of clearing the high-frequency restrike current is low for puffer circuit-breakers and even lower for self-blast (or arc assisted) circuit-breakers. This also means that the risk for voltage escalation is low. However, a restrike may cause tracking and/or puncture of the insulating material between the contacts (e.g. nozzle, sleeve, etc.).

9.7.17.4.2 Prestrikes

The duration of the prestrike is depending on the voltage per breaking unit and the closing speed. In general this duration is short. Regarding the limit of inrush current peak and frequency there is referred to 9.7.10.3.4.

9.7.17.5 Air-blast circuit-breakers

9.7.17.5.1 Restrikes

In general, the restrike probability of an air-blast circuit-breaker is higher than that of an SF_6 circuit-breaker. The flashover characteristic of air has a wider scatter than that of SF_6. Air-blast circuit-breakers can interrupt the high-frequency discharge current, which means that they have a higher probability of multiple restrikes, which may lead to voltage escalation.

9.7.17.5.2 Prestrikes

The considerations given in 9.7.17.4.2 also applies to air-blast circuit-breakers.

9.8 Considerations of capacitive currents and recovery voltages under fault conditions

9.8.1 Voltage and current factors

Some requirements, general ratings and tests for capacitive current switching are based on switching operations in the absence of faults. The presence of a fault can increase the value of both the capacitive switching current and recovery voltage. This is recognized by IEC 62271-100 by the specification of two voltage factors when breaking in the presence of faults. These voltage factors are given in Annex S of IEC 62271-100:2008/AMD2:2017 and are 1,4 for effectively earthed systems and 1,7 for non-effectively earthed systems. Tests for these conditions are not mandatory. An example of such a fault is a circuit-breaker switching an overhead line that interrupts fault current in one phase and capacitive current in the other two phases.

The fact that the capacitive switching current increases in the presence of earth faults is recognized in Annex S of IEC 62271-100:2008/AMD2:2017, where the line and cable charging currents are multiplied by 1,25 for effectively earthed neutral systems and 1,7 for non-effectively earthed systems. The number of tests is reduced to reflect the fact that such operations do not occur frequently. The test procedure given in Annex S of IEC 62271-100:2008/AMD2:2017 is based on a class C1 test procedure (i.e. no pre-conditioning of the circuit-breaker) and is common for both class C1 and class C2 circuit-breakers.

For capacitor banks, the situation is different. No tests are required for switching of solidly earthed neutral single capacitor banks in solidly earthed neutral systems. Switching of non-effectively earthed neutral capacitor banks in solidly earthed neutral systems is not considered a normal system condition and no requirements or tests have been specified. Switching back-to-back is not considered a normal system condition and no requirements and tests have been specified.

9.8.2 Reasons for these specific tests being non-mandatory in the standard

In service, circuit-breakers have been successful in interrupting capacitive circuits under faulted conditions for a number of reasons. Principal reasons for successful operation include:

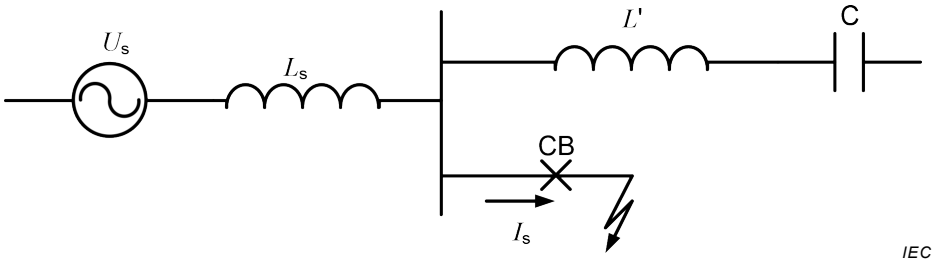
a) the probability of a fault occurring at minimum operating conditions of the circuit-breaker and its operating mechanism is extremely small;

b) the voltage factor used for single-phase tests is in excess of the service condition giving the tested circuit-breaker added margin;

c) laboratory tests are performed using a minimal voltage jump, resulting in short arcing times. This condition is more severe than the actual network condition where the voltage jump is generally higher.

9.8.3 Contribution of a capacitor bank to a fault

Consider the network situation given in Figure 126. A single line simplification is given in Figure 127. A fault has occurred on the line that is interrupted by the circuit-breaker (CB). The capacitance of the capacitor bank will modify the TRV across the circuit-breaker to a 1-cosine waveshape having a moderate rate-of-rise with a higher amplitude factor as compared to the case without the presence of the capacitor bank.



Key

U_s	Source voltage	CB	Circuit-breaker
L_s	Short-circuit inductance	I_s	Short-circuit current
L'	Busbar inductance		

Figure 127 – Fault in the vicinity of a capacitor bank

When the ITRV is negligible, the circuit-breaker will attempt to interrupt at the first available current zero following contact separation, resulting in a relatively small contact gap. As the recovery voltage increases across the gap, a re-ignition might occur and the capacitor bank will discharge into the fault through the circuit-breaker. The amplitude of the discharge current depends on the voltage across the circuit-breaker contacts at the time of re-ignition and the frequency of the discharge current is determined by the inductance between the capacitor bank and the fault location.

The high-frequency discharge current is superimposed on the fault current, which creates additional current zeros. Depending on the type of circuit-breaker (oil, air-blast, vacuum or SF_6), the high-frequency current may be interrupted causing high overvoltages. For further information refer to [128] and [129].

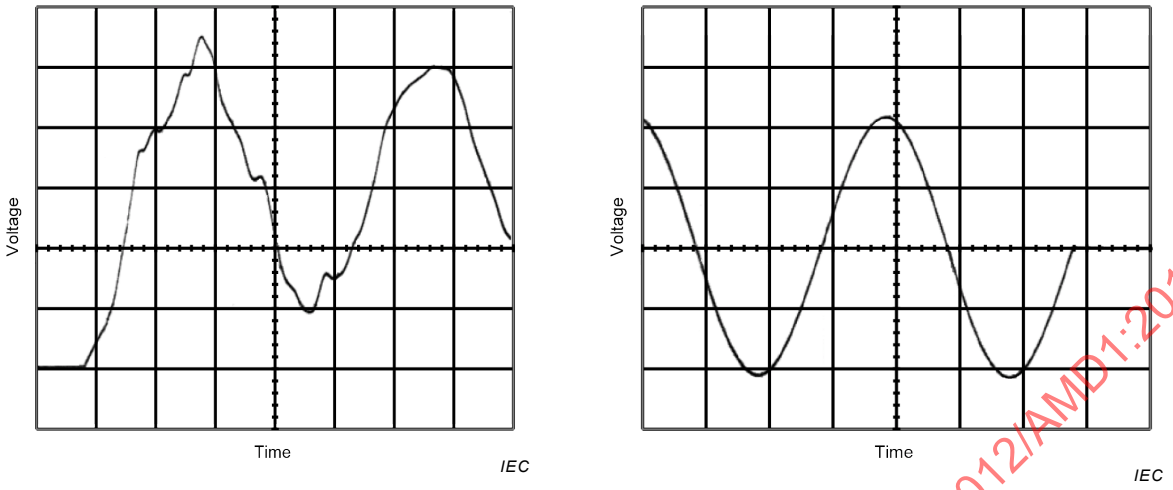
A similar situation may occur, when circuit-breaker CB closes into a fault. The capacitor bank discharges into the fault and depending on the magnitude of the inductance between the capacitor bank and the fault location, the discharge current can reach peak values and frequencies that exceed those given in Table 9 of IEC 62271-100:2008 (see also 9.7.12.2).

For these specific outrush cases the manufacturer should be consulted. For further treatment of this subject, see IEEE 1036 [130].

9.8.4 Switching overhead lines under faulted conditions

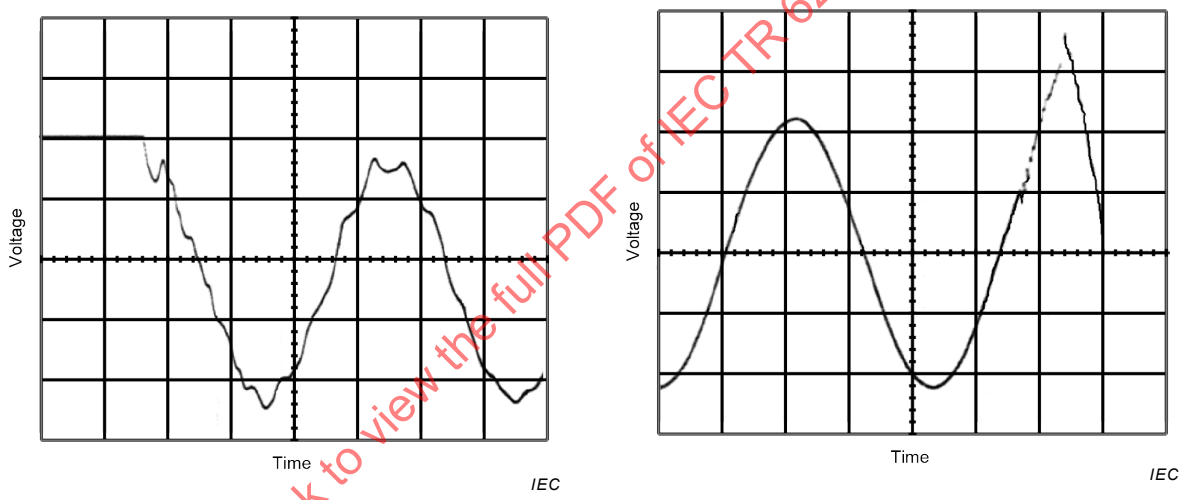
The voltages and currents that occur when switching a faulted transmission line are affected by the circuit parameters and the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage for switching an unfaulted transmission line as $2 \times 1{,}2 \times U_r \sqrt{(2/3)} = 2{,}4$ p.u. When switching a faulted line this value may be exceeded, as may be the rated capacitive switching current value as listed in Table 9 of IEC 62271-100:2008 (see also [131]).

When switching a no-load overhead line with a phase-to earth fault, the highest voltage occurs on the unfaulted phase, which interrupts prior to the faulted phase (see Figure 128). The highest current occurs on the last phase to interrupt when the faulted phase is the first to interrupt. The current for this case is not a sine wave but is distorted, as shown in Figure 129. Under these conditions, the voltages and currents may exceed those on which the design tests are based.



Maximum recovery voltage 2,74 × U_{max} (phase-to-earth) Maximum current 1,09 × rated current

Figure 128 – Recovery voltage and current for first-phase-to-clear when the faulted phase is the second phase-to-clear



Maximum recovery voltage 2,18 × U_{max} (phase-to-earth) Maximum current 1,77 × rated current

Figure 129 – Recovery voltage and current for last-phase-to-clear when the faulted phase is the first-phase-to-clear

For the phase-to-phase fault condition, the recovery voltage and capacitive current are less severe than for the two phase-to-earth fault condition, see also [130].

9.8.5 Switching capacitor banks under faulted conditions

9.8.5.1 General

The voltages and currents that can occur when switching a faulted capacitor bank depend upon the earthing conditions, whether the fault is to the bank neutral or to earth, and on the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage in switching an unfaulted shunt capacitor bank as 2,8 p.u. When switching a faulted bank, this value may be exceeded, as may the rated capacitive switching current value. In the following subclauses, a comparison is given between the recovery voltages and currents of a reference condition and two faulted conditions: a fault to neutral in the capacitor bank and a fault to earth in one phase.

NOTE The factor 2,8 for the maximum recovery voltage specified in IEC 62271-100 is valid when switching a non-effectively earthed capacitor bank where the second and third phases clear 90° after the first. This is true for modern circuit-breakers. For older circuit-breakers, where the second and third phases do not clear 90° after the first, this factor is 3,0.

9.8.5.2 Reference condition

9.8.5.2.1 General

The reference condition is illustrated in Figure 130. The neutral of the source and the capacitor bank may be solidly earthed and/or non-effectively earthed. The size of the capacitor bank is such that the current is equal to the preferred single capacitor bank current.

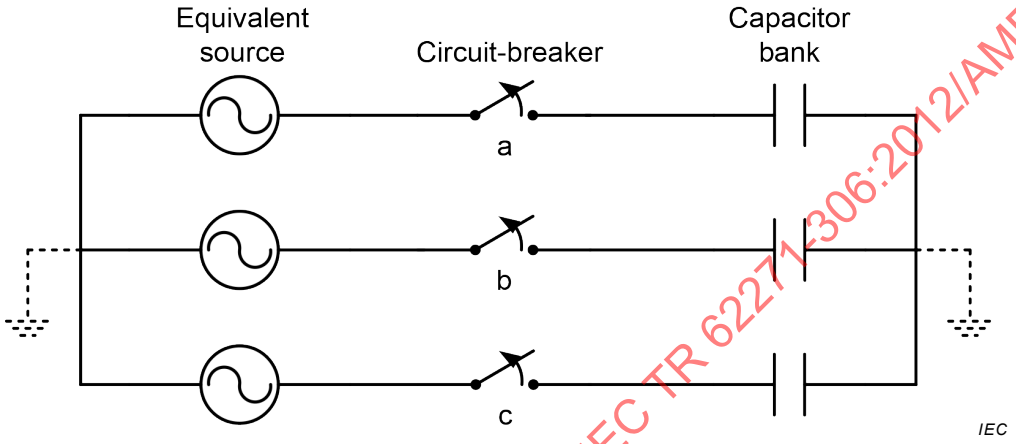


Figure 130 – Basic circuit for shunt capacitor bank switching

9.8.5.2.2 Recovery voltage

The highest recovery voltage (2,5 p.u.) is obtained in the first-pole-to-clear when either the neutral of the capacitor bank, the neutral of the source or both are non-effectively earthed and poles 2 and 3 clear 90° after the first.

The voltage across the last poles to interrupt when at least one of the neutrals (source or bank) is non-effectively earthed can reach $2 \times \sqrt{3} = 3{,}46$ p.u. However, the two phases are in series so that neither is stressed to more than 1,73 p.u.

9.8.5.2.3 Capacitor bank current

In all cases, the capacitor bank current does not exceed the preferred single capacitor bank current.

9.8.5.3 Fault to neutral in one phase (one capacitor bank phase short-circuited)

9.8.5.3.1 Recovery voltage

The highest recovery voltage ($2 \times \sqrt{3} = 3{,}46$ p.u.) is obtained when at least one neutral is non-effectively earthed and the first-pole-to-clear clears a healthy phase. This is in agreement with the voltage factor of 1,7 specified in IEC 62271-100. If the first-pole-to-clear interrupts an unfaulted phase, it is subjected to a recovery voltage of 3,46 p.u. until the second and third phases interrupt.

The highest recovery voltage in the remaining phases is 3,46 p.u., but it is shared by two poles in series.

9.8.5.3.2 Current

The highest capacitive current is obtained in the cases described under 9.8.5.3.1 when the faulted phase is the first-pole-to-clear and is equal to 3 times that of the reference case.

9.8.5.4 Fault to earth in one phase

For systems that are effectively earthed, the highest recovery voltage is obtained when the first-pole-to-clear interrupts a non-faulted phase. In this case, the maximum recovery voltage peak will be 2,8 p.u.

The most severe case is when the source is non-effectively earthed and the bank neutral is solidly earthed. If an unfaulted pole is the first to interrupt, the current may reach √3 times that of the reference condition and the recovery voltage 3,46 p.u. The remaining poles are subjected to the same current, but upon interrupting, share the 3,46 p.u. recovery voltage. When the faulted pole is the first-pole-to-clear, the current may be 3 times the rated current value and the recovery voltage $2 \times 1{,}25 \times \frac{U_r \sqrt{2}}{\sqrt{3}}$. The second pole to interrupt will have a lower current but a higher recovery voltage of $2 \times \sqrt{3} = 3{,}46$ p.u. which will be shared with the third pole. If the faulted pole reignites, one of the unfaulted poles will then interrupt and the conditions will be as previously described when an unfaulted pole was the first to interrupt.

9.8.5.5 Other fault cases

For phase-to-phase earth faults, or phase-to-phase non-effectively earthed faults, with the source solidly earthed and the bank neutral non-effectively earthed, recovery voltages and currents are no more severe than for the standard unfaulted condition.

9.8.6 Switching cables under faulted conditions

The normal frequency capacitive currents and recovery voltages on a faulted cable circuit will be the same as for a solidly earthed capacitor bank under faulted conditions.

9.8.7 Examples of application alternatives

Application options available are:

a) Use a circuit-breaker of a higher rating in those cases of earth faults on non-effectively earthed systems where the recovery voltage and current, or both, exceed the requirements of IEC 62271-100.

b) Reduce the capacitance of the existing capacitor bank size so that the current under faulted conditions does not exceed the rated capacitive switching current of the circuit-breaker.

c) Use a high-speed switch to earth the source or capacitor bank neutral before switching the capacitor bank under faulted conditions.

d) Use a Δ configuration for the capacitor bank instead of a non-effectively earthed Y.

9.9 Explanatory notes regarding capacitive current switching tests

9.9.1 General

Subclause 6.111 of IEC 62271-100:2008 deals with capacitive current switching tests. In the 1st edition of this standard, a new test procedure has been introduced for the two classes of capacitive current switching that deserve some explanation.

9.9.2 Restrike performance

See 9.7.6.

9.9.3 Test programme

In defining the test programme for these two classes, the following elements have been taken into account:

– the average number of operations per year carried out by circuit-breakers switching capacitive loads;

– the ability to reduce the number of tests by performing an increased number of switching operations at the minimum arcing time, usually the most difficult capacitive switching operation for circuit-breakers, thus keeping a high level of reliability;

– the recommendations of CIGRE working group A3.04. The expected restrike probability is exclusively related to the type tests.

The proposed number of tests may be questioned because of different assumptions for probability calculations. Nevertheless, these values represent a good compromise (which is the role of the standard where conflicting views exist), reflecting the needs of users (in response to market demand) and above all they avoid unrealistic demands. These tests are not reliability tests but type tests to demonstrate a satisfactory capacitive current switching capability of the equipment in service.

9.9.4 Characteristics of supply circuit

The paragraph concerning factor k_c/k_{pp} (from earlier versions of the standard) where k_c is the voltage factor as described in 9.6 and k_{pp} is the first-pole-to-clear factor has been deleted because there is neither use nor need for testing.

The variation of the power frequency voltage has been chosen as 5 % for test-duty 2 (LC2, CC2 and BC2) and 2 % for test-duty 1 (LC1, CC1 and BC1). These values are a compromise, taking limitations of testing laboratories into account. Considering the type test as a whole, because of the different stresses in the individual test-duties, any undue reduction of the electric stress during the tests is avoided. The actual values for the power frequency voltage variation (depending on the short-circuit power of the system and the capacitive load) is in the range of 1 % to 2 %.

9.9.5 Common features for class C1 and class C2 test-duties

The interval after final arc extinction, in which the voltage decay should not exceed 10 %, has been changed from 100 ms to 300 ms based on service conditions.

9.9.6 Specific feature for class C2 test-duties

Performing these capacitive current switching tests for class C2 equipment on a preconditioned circuit-breaker is, on the one hand, a recommendation of CIGRE working group A3.04; on the other hand, it draws closer to the real conditions of service, without prejudice as to whether this preconditioning improves the capacitive current switching performance of the circuit-breaker or not.

Close-open operations may be performed with no-load closing operations. In any case, the complete sequence should be tested in order to test the circuit-breaker during opening in a dynamic condition, i.e. during the motion of the fluid (if any) caused by the previous closing operation.

9.9.7 Class C1 and C2 test duties

The tolerance of the testing current values for test-duty 1 (LC1, CC1 and BC1) was increased from the old range 20 % to 40 % to the new range 10 % to 40 % in order to give more freedom during testing for combined test-duties for different applications.

The proposed test sequences have been tested in a laboratory (particularly the adjustment of the minimum arcing time by steps of 6°) and are well adapted to the philosophy of the tests.

Performing some tests at rated pressure is a more pragmatic approach to the notion of type testing, knowing that the circuit-breaker does not always stand under the worst functioning conditions.

9.9.8 Single-phase and three-phase line- and cable-charging current tests

In test-duty 2 of single-phase line-charging and cable-charging tests (LC2 and CC2), the tests are split into open operations and close-open operating cycles to follow more or less the actual service conditions. However, for practical reasons, owing to the small number of tests, in three-phase tests in test-duty 2 (LC2 and CC2), close-open operating cycles are performed exclusively.

9.9.9 Three-phase and single-phase line, cable and capacitor bank switching tests

Close-open operating cycles are important for capacitor bank switching because of the effect of inrush current. Close-open operating cycles are not significant for line- or cable-switching applications, therefore for line- and cable-switching tests, only a small number of close-open operations are requested (closing may be performed as a no-load operation).

A rough parity of the number of three-phase and single-phase tests has been maintained.

The mandatory order for capacitor bank switching tests (single- or back-to-back) is due to the necessity to introduce the effect of inrush current at the beginning of the tests.

9.9.10 Three-phase and single-phase capacitor bank switching tests

Because of the large number of operations in actual service compared with the limited number of operations during type testing, a high number (80 or 120 respectively) of close-open operating cycles is carried out in capacitor bank tests to simulate the wear in service even if the close-open operation is not the normal switching sequence.

For capacitor bank switching tests test-duty 1 (BC1) also needs to be performed, even if the actual service switching duty is always at 100 % nominal current, for the following reasons:

– the tests at 10 % to 40 % nominal current cover an increased number of actual currents;
– knowledge of the capacitive current switching performance is improved.

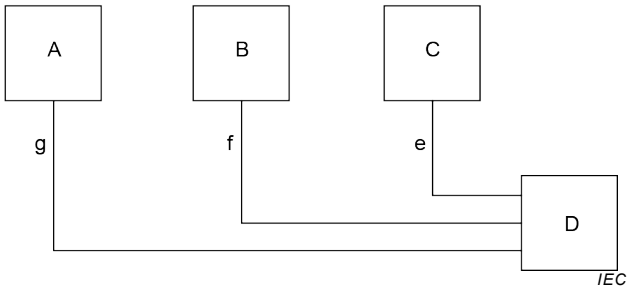
10.2 Testing

Replace the existing content of this subclause by the following new content:

10.2.1 General

To check the tightness characteristics for closed and sealed pressure systems for gas, the method generally used during type tests is to measure the leakage rate of the complete assembled circuit-breaker using a cumulative test method as mentioned in 6.8 of IEC 62271-1:2007. In case a measurement of the complete assembled circuit-breaker is not possible, the leakage measurement may be performed on parts, components or subassemblies. In such cases, the leakage rate of the total gas system is to be determined by summation of the component leakage rates as described in Figure 131.

Table 46 provides an overview of the different leakage detection methods and their sensitivity.



Example:

Gas-insulated metal-enclosed switchgear, single-phase encapsulated circuit-breaker compartments of the three phases connected to the same gas-system.

Leakage rate of the system:

Compartment A	9×10^{-6} Pa × m^3/s
Compartment B	9×10^{-6} Pa × m^3/s
Compartment C	9×10^{-6} Pa × m^3/s
Control box D (including valves, gauges, monitoring devices)	$2{,}3 \times 10^{-6}$ Pa × m^3/s
Piping e	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Piping f	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Piping g	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Complete system	$29{,}9 \times 10^{-6}$ Pa × m^3/s

Filling pressure	p_{re}: 700 kPa (relative)
Alarm pressure	p_{ae}: 640 kPa (relative)
Total internal volume	270 dm^3

$$F_{rel} = \frac{29{,}9 \times 10^{-6} \times 60 \times 60 \times 24 \times 365}{700 \times 10^{3} \times 270 \times 10^{-3}} = 0{,}5\ \%\ \text{per year}$$

$$t_r = \frac{\ln(p_{re} / p_{ae})}{\ln(1 + F_{rel}/100)} = \frac{\ln(700/640)}{\ln(1 + 0{,}005)} = 18\ \text{years}$$

NOTE F_{rel} is the leakage rate and t_r is the time between replenishment.

Figure 131 – Example of a tightness coordination chart, TC, for closed pressure systems

Table 46 – Sensitivity and applicability of different leak-detection methods for tightness tests

Measurement methodology	Sensitivity of leakage rate (best case)	Test result	Comments	Suitable for leakage rate determination		Suitable for major leaks detection
				High-voltage equipment	Medium-voltage equipment	
Vacuum/pressure increase test	100 P/h (approximately 10 kg/year of SF_6)	Qualitative	Normally used to verity equipment integrity before SF_6 filling	No	No	Yes if the cumulative test method is used
Infrared camera using BAGI (Backscatter/ Absorption Gas Imaging)	1 kg/year of SF_6 at a distance range of 35 m	Qualitative	Suitable for remotely determining the approximate location of major leaks	No	No	Yes
Bubble test with soap or special fluids	1 kg/year of SF_6	Qualitative	Simple and useful for determining the exact location of major leaks. Can also be used for other gases	No	No	Yes and for major leak localisation
Density monitoring (pressure drop)	600 g/year of SF_6 for an observation time of 1 year	Quantitative	Suitable for long term trend analysis of leakage detection or for equipment integrity test. Can also be used for other gases	No	No	Yes if the observation time is long enough
Infrared absorption spectroscopy	60 mg/year of SF_6 or 3 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type, routine and commissioning test. Not influenced by other common gases and water	Yes if the cumulative test method is used. Can be also used for minor leak localisation	Hardly suitable	Yes if the cumulative test method is used. Can also be used for major leak localisation
Negative ion capture detector (using corona discharge)	20 mg/year of SF_6 or 1 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type test, routine test, commissioning test and maintenance. Reading may be influenced by other gases and moisture content.	Yes if the cumulative test method is used Can be also used for minor leak localisation	Yes if the cumulative test method is used Hardly suitable for minor leak localisation	Yes if the cumulative test method is used. Can also be used for major leak localisation

Measurement methodology	Sensitivity of leakage rate (best case)	Test result	Comments	Suitable for leakage rate determination		Suitable for major leaks detection
				High-voltage equipment	Medium-voltage equipment	
Electron capture leak detector (using radioactive emitter)	2 mg/year of SF_6 or 0,1 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type test, routine test, commissioning test and maintenance. Reading may be influenced by other gases and moisture content.	Yes if the cumulative test method is used Can be also used for minor leaks localisation	Yes if the cumulative test method is used Hardly suitable for minor leak localisation	Yes if the cumulative test method is used. Can also be used for major leak localisation
Helium mass spectrometer	2 mg/year of SF_6 if checked by a calibration source	Quantitative	Type test and routine test. Can only be used with the cumulative test method	Yes Can also be used on equipment components	Yes	Yes. Cannot be used for leak localisation.
Photo-acoustic infrared spectroscopy	0,2 mg/year of SF_6 or 0,01 ppm_v	Quantitative	Type test and routine test. Can only be used with the cumulative test method	Yes	Yes	Yes. Cannot be used for leak localisation
See CIGRE Technical Brochure 430 [144] for more detailed information. NOTE 1 "minor leak" qualitatively indicates a leak having a leakage rate "L" in the order of the permissible leakage rate L_p ($L \approx L_p$). NOTE 2 "major leak" qualitatively describes leaks having at least one order of magnitude higher than the permissible leakage rate L_p ($L >> L_p$). NOTE 3 The "cumulative test method" can also be called "integral test".						

During routine tests, a cumulative test method is preferred but such a test may be impractical in industrial environments. For routine tests, as mentioned in 7.5 of IEC 62271-1:2007, a leak detection using a sniffing device may be used instead of using a cumulative test method. IEC 62271-1 specifies a minimum sensitivity of sniffing device of 10^{-8} Pa m^3/s.

This required minimum sensitivity corresponds to a single leak of less than 0,04 %/year for a typical 245 kV SF_6 circuit-breaker having an internal volume of 200 l filled at an absolute pressure of 0,5 MPa and if the moving speed of the sniffer detector around sealing joints is relatively slow, for instance, not exceeding 1 cm/s. Obviously, if the filling pressure, volume or moving speed of the leak detector are different, then the leakage rate sensitivity changes. Each case should be evaluated individually.

If a leak is detected when using a sniffing device, then the leakage rate cannot be quantified since this device is only giving an alert if a leak is detected. As mentioned in 7.5 of IEC 62271-1:2007, in the case of a detection of a leak with the sniffing device, the leakage rate should be then quantified by repeating the tightness test by using a cumulative test method. Only the cumulative test method can be used to quantify a leakage rate.

10.2.2 Cumulative test method and calibration procedure for type tests on closed pressure systems

10.2.2.1 Description of the cumulative test method

10.2.2.1.1 General

The cumulative test method is the recommended test method for the determination of gas leaks that can occur in closed pressure systems such as for SF_6 circuit-breakers. This method consists of erecting a relatively gastight enclosure (e.g. plastic tent or similar enclosure, see NOTE 2) around the complete test object or by erecting several smaller relatively gastight enclosures (plastic tents or similar enclosures, see NOTE 2) around each part, component or subassembly. The circuit-breaker should be filled as in service, at its rated filling pressure. The measurement consists of measuring the tracer gas content increase (e.g. SF_6) within the enclosure(s) during a sufficient time period. With today's available measuring equipment, a time period of 1 h is generally sufficient. If an enclosure(s) of small volume are used, then this measuring period can be reduced. For very large enclosures, this time period may need to be increased. As a rule of thumb, the time period should be long enough that the calculated tracer gas content in the enclosure for the maximum permissible leakage rate should be at least 3 times the minimum resolution of the measuring equipment. From the tracer gas content increase within the enclosure(s) during a given time period, then the annual leakage rate can be calculated. This method is considered to be very accurate and has been widely used during type tests on circuit-breakers at ambient, low and high temperatures.

The tightness of the enclosure should be demonstrated for the duration of the measuring time period. This can be done at the same time as the calibration of the enclosure.

The cumulative test method steps can be summarized as follows:

– install a relatively gastight enclosure(s) over the entire test object or over parts, components or subassemblies;
– pressurize the circuit-breaker at its rated filling pressure with its specified gas or gas mixture, pure SF_6 instead of gas mixture, or with a tracer gas such as helium;
– determine the enclosure(s) volume V_m (m^3);
– measure the tracer gas concentration C_0 (p.p.m_v. or cc/m^3) within the enclosure(s) at reference time t_0 (s);
– measure the final gas concentration C_1 (p.p.m_v. or cc/m^3) within the enclosure(s) at time t_1 (s);
– calculate the leak rate using the following equation:

$$F = V_m \times P_e \times \frac{\Delta C}{\Delta t} \times 10^{-6}$$

where

F is the leakage rate in m^3Pa/s;

V_m is the enclosure gas volume in m^3;

P_e is the atmospheric pressure in Pa;

ΔC is the tracer gas concentration increase (C_1-C_0) in p.p.m_v. during the measuring time period;

Δt is the measuring time period in seconds.

NOTE 1 A fan installed inside the enclosure helps to get an homogeneous gas tracer content within the enclosure. This recommendation applies mainly to large enclosure used around a complete circuit-breaker.

NOTE 2 The enclosure does not need to be as tight as a pressure vessel since the pressure within the enclosure is equal to the atmospheric pressure outside the enclosure. Thus, the air inside the enclosure (including traces of the tracer gas) is not forced to escape from the enclosure nor the air outside the enclosure is forced to enter within the enclosure.

10.2.2.1.2 Sensitivity, accuracy and calibration

The accuracy of the cumulative method depends on three main factors: sensitivity of the tracer gas detector, volume of enclosure and duration of the measuring period. For example, a minimum threshold sensitivity and resolution of 0,01 p.p.m_v is recommended when SF_6 is used as the tracer gas. Such gas detectors are commercially available.

NOTE 1 Infrared photo acoustic spectroscopy method is widely used to measure SF_6 concentration.

The uncertainty concerning the enclosure volume can be considerably reduced by using a suitable calibration technique. The recommended calibration procedure consists of injecting a known quantity of tracer gas into the enclosure.

NOTE 2 Experience gained from measurements showed that the estimation error of the enclosure volume is less than 10 %.

The enclosure volume (V_m in m^3) should be determined by calibration. A small tracer gas quantity, $V_{injected}$ (cm^3), is injected into the enclosure volume V_m. The injected gas quantity should be in the same order of magnitude than the gas quantity corresponding to the maximum allowable leakage rate.

The tracer gas concentration C_0 (p.p.m_v.) is measured before and after injection by the gas detector. The enclosure volume is then calculated as follows:

$$V_m = V_{injected} / \Delta C_0$$

This procedure should be repeated twice in order to get a better evaluation of the enclosure volume. The average value of the two measurements should be used as the enclosure volume V_m.

10.2.2.1.3 Test set-up and test procedure

For type test, the test object should be pressurized at its nominal filling pressure with its assigned gas mixture (if applicable). Nevertheless, industrial environments and local safety rules may force a deviation from service conditions. For instance, some tests could be performed using pure SF_6 instead of the assigned gas mixture, or other tracer gases such as helium may be used. All deviations from service conditions have to be carefully evaluated to see their impacts on the measurement sensitivity.

In order to have an effective test set-up, the following is recommended:

– the enclosure volume should be as small as possible in order to obtain a better sensitivity of the tracer gas concentration within the enclosure;

– a fan should be installed inside the enclosure in order to provide an homogeneous gas content within the enclosure;

– the gas detector device should be able to measure accurately 1/3 of the maximum allowable leakage rate.

For low and high ambient temperature tests, the following additional recommendations are given:

– Thermocouples should be installed at different heights along the test object inside the enclosure. The ambient temperature to be reached during test is the temperature measured inside the enclosure.

– Controllable electric heaters should be installed inside the enclosure in order to help to fulfill the temperature increase of 10 K/h specified during the low temperature test sequence. For the high-temperature test, the temperature decrease of 10 K/h within the enclosure can be met by making a temporary opening of the enclosure since the leak rate determination is not required during this test part of the test. Required temperature variations have to be met within the enclosure.

NOTE 1 One way to obtain the desired temperature inside the enclosure is to lower the ambient temperature in the climatic room such that it is slightly lower than the required temperature for low temperature test or slightly higher for high temperature test.

The maximum leakage rate (m^3Pa/s) based on acceptance leakage rate limit of 0,5 % per year (see 5.15.2 of IEC 62271-1:2007) is calculated as follows:

$$F = \frac{0{,}005 \times V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273\,\mathrm{K} + 20} - 101{,}3 \times 10^3 \right) \times \gamma}{365 \times 24 \times 60 \times 60}$$

where

F is the leakage rate in m^3Pa/s;

V_{to} is the circuit-breaker gas volume in m^3;

P_{to} is the circuit-breaker absolute filling pressure at T = 20 °C in Pa (see NOTE 2);

T_{test} is the ambient temperature during leakage measurement in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume.

NOTE 2 It is assumed only gas exceeding the atmospheric pressure can escape from the breaker. Other leakage mechanisms such as atomic migration through solid materials are considered to be negligible. The pressure correction for the test temperature is applied to the absolute gas pressure.

Finally, the leakage rate per year (%/year) can also be directly expressed by the following equation:

$$F_{year} = \frac{P_{atm} \times 365 \times 24 \times 60 \times 60 \times V_m \times \Delta C \times 10^{-6}}{V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273 + 20} - 101{,}3 \times 10^3 \right) \times \gamma \times t}$$

where

F_{year} is the leakage rate in %/year;

P_{atm} is the atmospheric pressure during measurement (a default value of 101,3 kPa can be used);

ΔC is the tracer gas concentration increase (C_1-C_0) in p.p.m_v. during the measuring time period;

V_m is the enclosure gas volume in m^3;

V_{to} is the circuit-breaker gas volume in m^3;

P_{to} is the circuit-breaker absolute gas pressure in Pa;

T_{test} is the ambient temperature during leakage measurement in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume;

t is the measuring time period in s.

10.2.2.1.4 Example: leakage rate measurement of a circuit breaker during low temperature test

The test object is filled with its gas mixture SF_6/N_2 at nominal filling pressure and ambient temperature. A relatively gastight enclosure is installed over the circuit-breaker. A calibration by injection method is performed in order to evaluate the enclosure volume.

Table 47 shows the results of a calibration of the enclosure.

Table 47 – Results of a calibration procedure prior to a low temperature test

Description	Quantity of SF_6 gas injected within the enclosure	Concentration of SF_6 gas measured within the enclosure	Variation of concentration of SF_6 gas within the enclosure	Calculated volume V_m
	(cm^3)	(p.p.m_v)	(p.p.m_v)	(m^3)
Before test	-	0,05	-	
First Injection	10	1,03	0,98	10,20
Second injection	10	2,06	1,03	9,71

Thus, the enclosure volume is considered to be the average value of the volumes determined with both injections e.g. 9,96 m^3.

Then, if a circuit-breaker having an internal volume of 0,375 m^3 filled with a gas mixture consisting of SF_6 and N_2 at an absolute pressure of 1,0 MPa and the SF_6/N_2 mixture is 30 % SF_6 and 70 % N_2, the 0,5 %/year permissible maximum leakage rate at ambient temperature (20 °C) corresponds to a maximum concentration of tracer gas within the enclosure during a measuring period of 1,0 h of:

$$\Delta C = \frac{F_{year} \times V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273 + 20} - 101{,}3 \times 10^3 \right) \times \gamma \times t}{P_{atm} \times 365 \times 24 \times 60 \times 60 \times V_m \times 10^{-6}}$$

$$\Delta C = \frac{0{,}005 \times 0{,}375 \times \left(1 \times 10^6 \times \frac{273 + 20}{273 + 20} - 101{,}3 \times 10^3 \right) \times 0{,}3 \times 3600}{101{,}3 \times 10^3 \times 365 \times 24 \times 60 \times 60 \times 9{,}96 \times 10^{-6}} = 0{,}057 \text{ p.p.m}_v.$$

Accordingly, if the same enclosure is used for the low-temperature test, the maximum allowable gas concentration increase for a measuring time period of 1 h at an ambient temperature of −25 °C will be:

$$3 \times F_{year} = 3 \times 0{,}057 \times \left(1 \times 10^6 \times \frac{273 - 25}{273 + 20} - 101{,}3 \times 10^3 \right) = 0{,}127 \text{ p.p.m}_v.$$

and accordingly at −50 °C

$$6 \times F_{year} = 6 \times 0{,}057 \times \left(1 \times 10^6 \times \frac{273 - 50}{273 + 20} - 101{,}3 \times 10^3 \right) = 0{,}226 \text{ p.p.m}_v.$$

It should be noted that the relative leakage rate of N_2 cannot be measured using this method. It may be higher than the value obtained by relating the leakage rate of N_2 to that of SF_6, i.e. $\Delta C(N_2) \neq \Delta C(SF_6) \times 0{,}7 / 0{,}3$.

10.2.2.2 Time between replenishment

With a given leakage rate F in %/year, the time between replenishments t_r is obtained from the following equation. t_r is the number of periods on which the leakage rate is defined (in this case 1 year):

$$t_r = \frac{\ln(p_{re} / p_{ae})}{\ln(1 + F/100)}$$

where

t_r is the time between replenishments;

p_{re} is the relative filling pressure in Pa;

p_{ae} is the relative alarm pressure in Pa;

F is the measured leakage rate in %/year.

11.2.2 Comparison of the mechanical characteristics

Add, after the first sentence of the first paragraph, the following new text:

The sensor used during the alternative drive tests should be of the same type as for the original operating mechanism. The position of the sensor should be at the same position as during the original test to allow a direct comparison of the travel curves. If it is not possible to use the same position or type of sensor during the alternative drive test, because the design of the alternative drive does not allow this, the manufacturer should provide a transfer function to calculate the corresponding travel characteristic for comparison. The evaluation of the transfer function should be explained in detail for easy check of validity. The position of the type and sensor for the record of the mechanical characteristics should be stated in the test report.

13 Terminal faults

Replace the entire clause, including its title, by the following:

13 Symmetrical and asymmetrical currents

13.1 General

This clause treats symmetrical and asymmetrical short-circuit currents and their arcing times.

Test requirements for symmetrical terminal fault conditions that are covered by short-circuit test duties T100s, T60, T30, and T10 are covered in 13.3. The asymmetrical duty T100a is covered in 13.4 and the various short-line fault and out-of-phase duties are considered elsewhere in this document.

The purpose of this clause is to provide a background framework for some of these requirements where it may not be clear from the latest revision of the standard, or from readily available text books, how they were derived. Aspects covered in this clause are those relating to the short-circuit current, particularly to the arcing time and the voltages, both power frequency and transient recovery voltage (TRV), associated with terminal faults.

13.2 Arcing time

The arcing time of a pole of a circuit-breaker is defined as the interval of time between the instant of the first initiation of an arc in a pole and the instant of arc extinction in that pole.

There are several possible methods to determine the arcing time.

a) Using the opening time of the circuit-breaker

When a tripping coil current signal is available, the arcing time is determined by subtracting the opening time from the break time of the pole considered.

b) Using a travel recorder

The arcing time is the duration between the contact separation point identified on the travel curve, and the instant of interruption. The instant of contact separation is determined during the no load measurements before the test.

c) Using amplified arc voltage

The arcing time is the duration between the contact separation, determined on the amplified arc voltage, and the instant of current interruption.

For gas circuit-breakers method b) is the preferred method. This method is considered more accurate as it eliminates the possible error in method a) due to mechanical scatter of the operating mechanism. For circuit-breakers having butt contacts, method c) is recommended.

13.3 Symmetrical currents

13.3.1 Demonstration of arcing time

Throughout IEC 62271-100 and related documents the terms arcing time and interrupting window are used, especially in relation to the interruption of short-circuit currents. To understand the requirements of the various subclauses of IEC 62271-100:2008, such as 6.102.10, it is necessary to understand the meaning of these terms and that of the terms minimum and maximum arcing time in particular.

The arcing time of a three-pole circuit-breaker is defined as the interval of time between the instant of first initiation of an arc (typically at contact separation) and the instant of final arc extinction in all three phases. Arcing time is measured in ms, or in electrical degrees (e.g. 10,0 ms at 50 Hz and 8,3 ms at 60 Hz are 180°). The shortest arcing time at which the circuit-breaker is able to interrupt is the minimum arcing time.

Depending on the point of contact separation and the particular current, the arcing time of a circuit-breaker will vary between this minimum value and a maximum value. The difference between these values is called the interrupting window (or more rarely the arcing window). Although different designs of circuit-breaker will be capable of interrupting with different duration of their interrupting windows there is a basic requirement which is applicable to all modern designs of circuit-breaker. For these circuit-breakers the minimum arcing time is short or relatively short, and in addition they have limited capability for prolonged arcing as their quenching period is also short.

The aim of each test-duty (e.g. T100s or T60) is to demonstrate the breaking capacity with any arcing time within this interrupting window. This requirement is fulfilled by demonstration of interruption at minimum, maximum and medium arcing time. The minimum and maximum arcing times cannot be demonstrated in a single valid test. In the case of fault interruptions involving three-phases, the minimum arcing time is obtained in one of the valid tests of a test-duty with the first-pole-to-clear and the maximum arcing time is obtained in another valid test with the last pole(s) to clear.

For single-phase faults the maximum arcing time is the period to the end of the interrupting window of the faulted phase, consisting of the minimum arcing time plus one loop of fault current minus 18°. This 18° is related to a deliberately specified step, of equal duration for 50 Hz and 60 Hz, giving a point of contact separation a short time later than that giving the minimum arcing time. At this setting the arcing time is too short for satisfactory clearance as a

minimum, by definition, and an additional loop i.e.180° will follow until the next current zero. Clearance at this later current zero results in the maximum arcing time and the end of the interrupting window. The specified step of 18° is the smallest practical value for such a step generally achievable at testing stations being 1 ms at 50 Hz and 0,8 ms at 60 Hz.

13.3.2 Demonstration of the arcing time for three-phase tests

In accordance with IEC 62271-100, each test-duty consists of demonstration of interruption within the interrupting window. This requirement is fulfilled by demonstration of interruption at minimum, maximum and medium arcing time, i.e. by three valid tests of each of the specified short-circuit test duties.

When three-phase symmetrical current tests are to be demonstrated using direct test techniques, the possible arcing times are automatically obtained by changing the setting of contact separation by a duration of 40° between each of the three required opening operations of the operating sequence (refer to 6.102.10.1.1 of IEC 62271-100:2008). In this way, taking into account that current passes through zero on one of the phases every 60°, the minimum arcing time is determined with a accuracy of less than 20°.

For synthetic testing the procedure is defined in IEC 62271-101.

13.3.3 Interrupting window and k_p requirements for testing

Separate procedures exist for tests performed in substitution for three-phase conditions by using a single pole of the circuit-breaker.

The procedure as defined is for circuit-breakers to be installed in systems with non-effectively earthed neutral and separately for those with effectively earthed neutrals. The relevant subclauses in IEC 62271-100:2008 are 6.102.10.2.1 and 6.102.10.2.2.

In accordance with IEC 62271-100, the required interrupting window shall be demonstrated for each condition in the case of interruptions with symmetrical currents, as for test duties T10, T30, T60, and T100s. (Note, this also applies to short-line fault and the out-of-phase test-duties OP1 and OP2). Whether the testing is for three-phase test requirements, or single-phase tests in substitution for the three-phase condition, it is important that the interrupting window and associated TRV are demonstrated for the relevant system condition. In the case of a single-phase test, the three tests of the duty are demonstrated on that single pole, as it is the representative sample of the circuit-breaker, as allowed in 6.102.2 of IEC 62271-100:2008.

The interrupting windows required by IEC 62271-100:2008 for circuit-breakers applied in a non-effectively earthed system are shown graphically in Figure 132. If contact parting is at the minimum arcing time ($t_{arc\ min}$) on one pole, then that pole clears at 0° in Figure 132 and is followed by the other two poles 90° later. The minimum three-phase arcing time is $t_{arc\ min}$ + 90°. If contact parting is now delayed by 18°, the first-pole-to-clear on one of the other two phases will interrupt the current at ($t_{arc\ min}$ – 18°) + 60° = $t_{arc\ min}$ + 42°. As before, the other two poles will clear 90° later giving a maximum three-phase arcing time of $t_{arc\ min}$ + 132°.

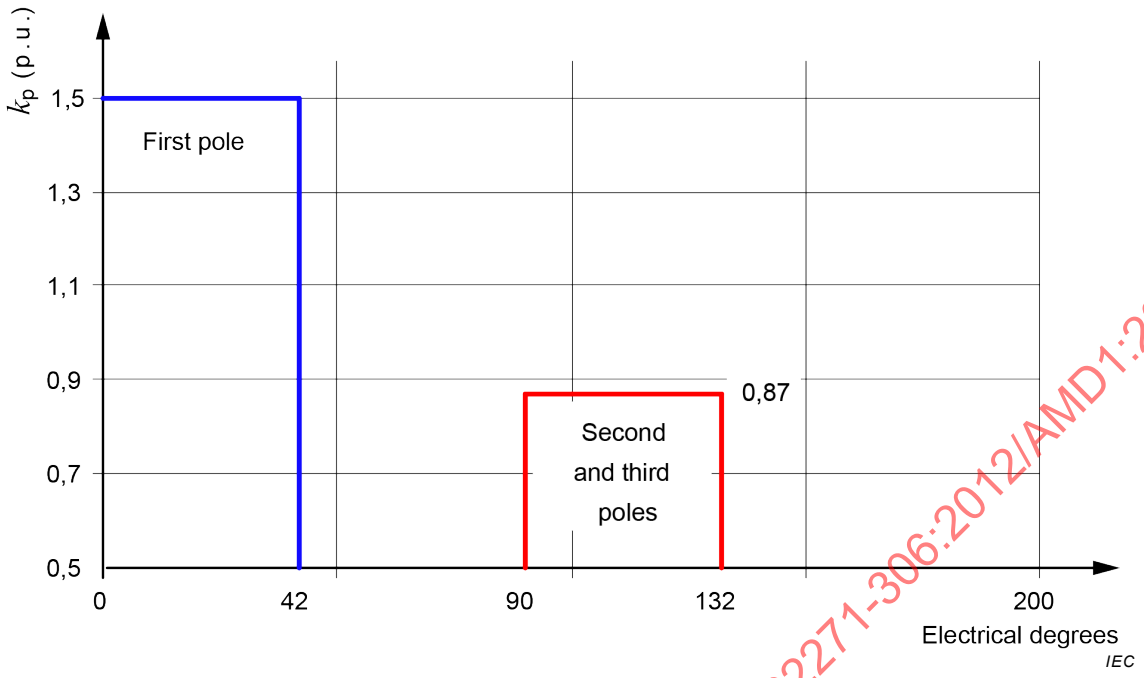


Figure 132 – Interrupting windows and k_p value for three-phase fault in a non-effectively earthed system

A practical example of this case is shown in Figure 133. In the upper trace, the blue phase clears first at the minimum arcing time of $t_{arc\ min}$ and the currents in the red and green each phase shift by 30° to become equal and opposite and are interrupted 90° later. In the lower trace, contact parting is delayed by 18° and the first suitable zero crossing for current interruption occurs on the red phase at ($t_{arc\ min}$ + 42° / 360° × T) ms, where T is the duration of one cycle of current (20 ms for 50 Hz and 16,7 ms for 60 Hz). The blue and green phases then clear at ($t_{arc\ min}$ (42° + 90°) / 360° × T)) ms.

The required interrupting windows for circuit-breakers applied in effectively earthed systems at 800 kV and below are shown in Figure 134 and at voltages above 800 kV are shown in Figure 135.

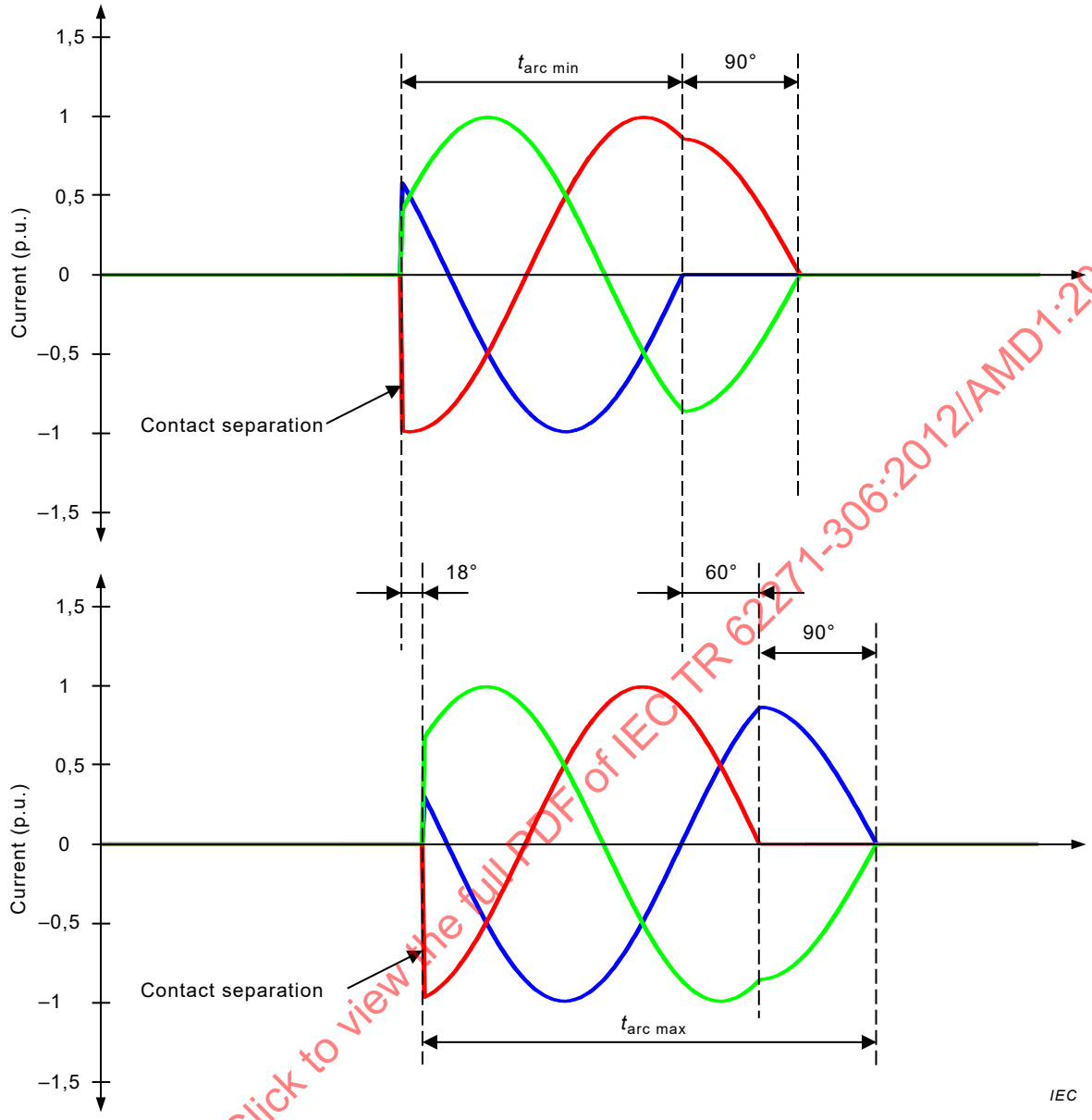


Figure 133 – Three-phase unearthed fault current interruption

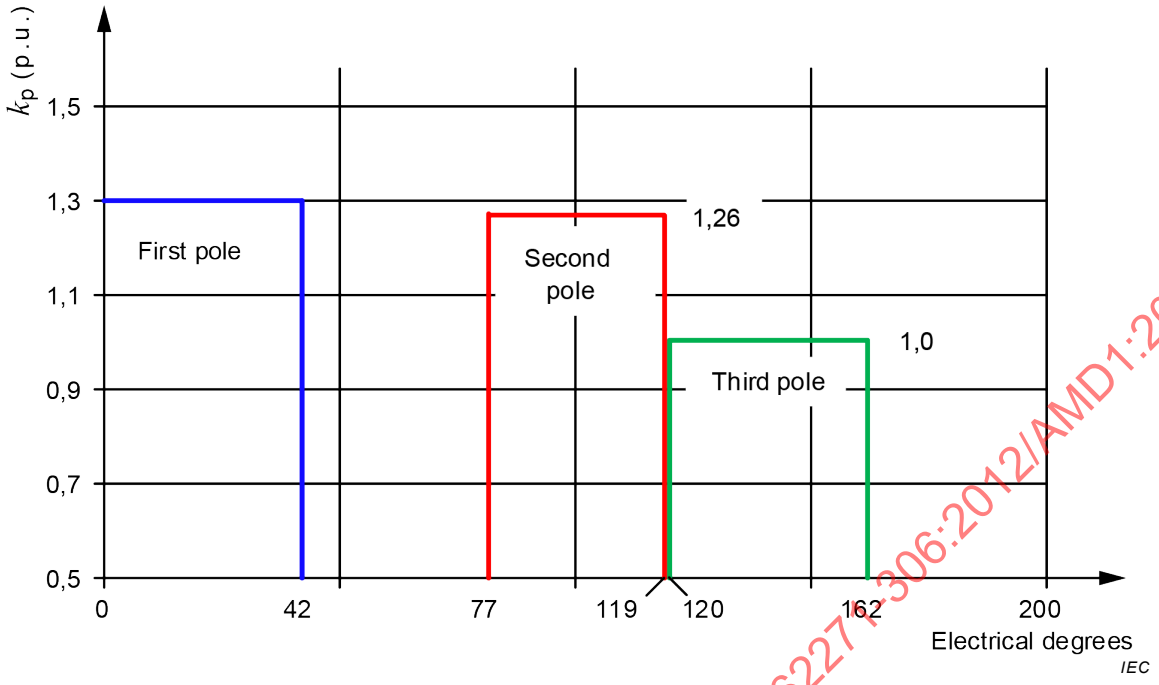


Figure 134 – Interrupting windows and k_p values for three-phase fault to earth in an effectively earthed system at 800 kV and below

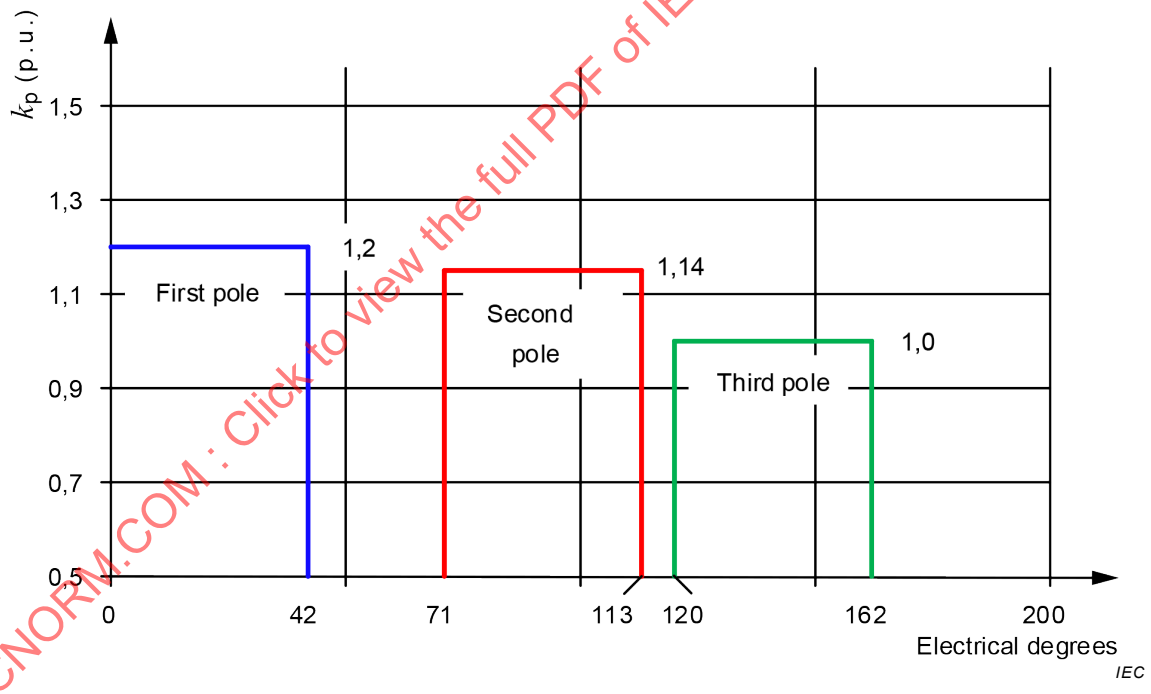


Figure 135 – Interrupting windows and k_p values for three-phase fault to earth in an effectively earthed system above 800 kV

Referring to Figure 134 and Figure 135, if contact parting is at the minimum arcing time on one pole, then that pole clears at 0° in either figure. The transition from a three-phase to a two-phase fault causes a phase shifting of the currents in the other phases and the second pole will clear at 77°. A further transition and phase shift results in the third pole clearing 43° later. The minimum three-phase arcing time is $t_{arc\ min}$ + ((77° + 43°) / 360°) × T = $t_{arc\ min}$ + 120° / 360° × T. If contact parting is delayed by 18°, the first-pole-to-clear will interrupt the current at ($t_{arc\ min}$ – 18° / 360° × T) + 60° / 360° × T, the second pole 77° / 360° × T later and the third pole 43° / 360° × T later still. The maximum three-phase arcing time is given by

$t_{arc\ max}$ = ($t_{arc\ min}$ – 18° / 360° × T) + 60° / 360° × T + 77° / 360° × T + 43° / 360° × T = $t_{arc\ min}$ + 162° / 360° × T. Figure 136 shows a simulation of a three-phase fault current interruption. The first-pole-to-clear interrupts the current at $t_{arc\ min}$ followed by the second and third poles at 77° and 43°, respectively. The phase shifting of the current at first and second pole clearing is obvious.

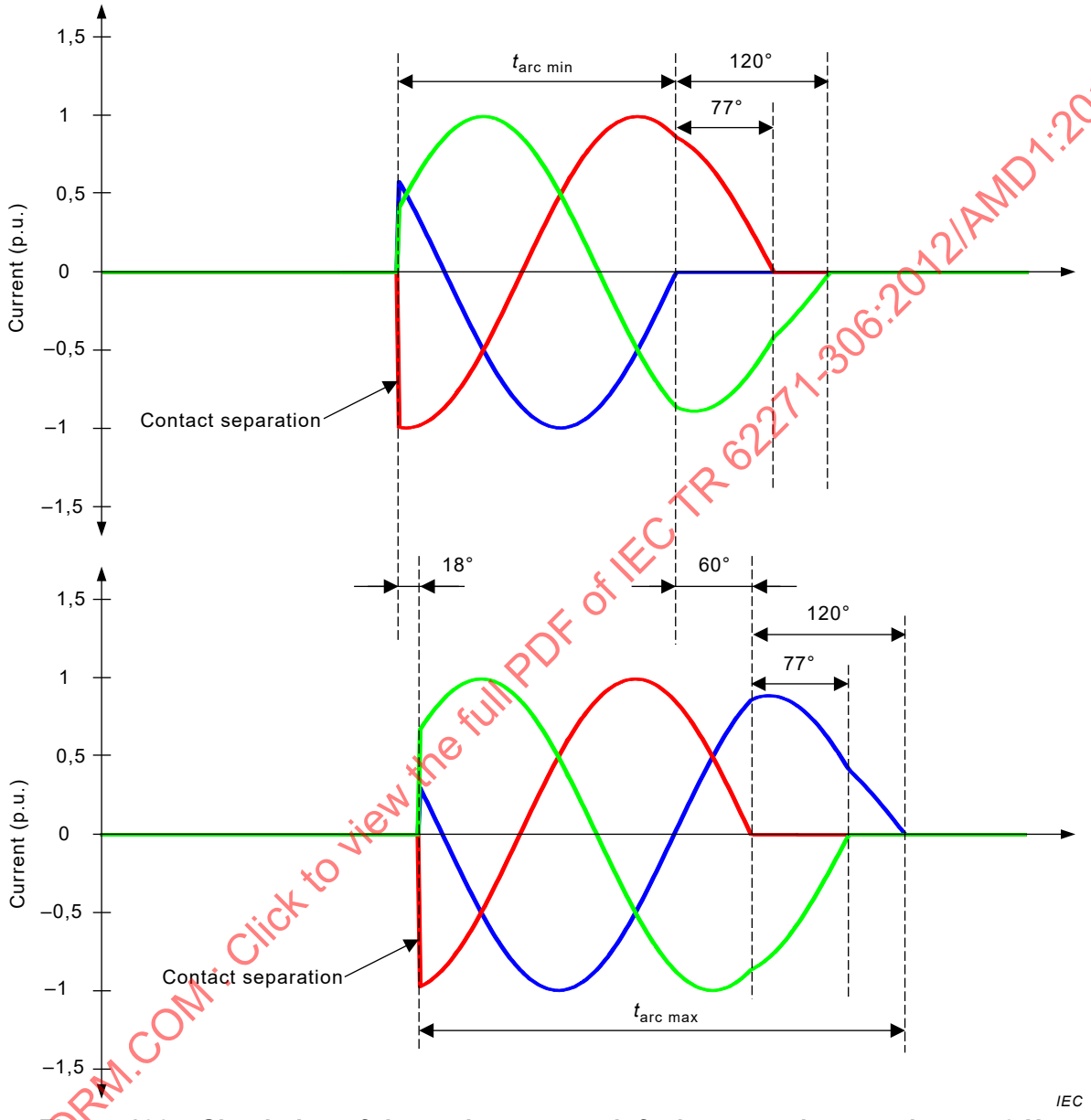


Figure 136 – Simulation of three-phase to earth fault current interruption at 50 Hz

13.3.4 Single-phase testing to cover three-phase testing requirements

As discussed in 13.3.3, Figure 132, Figure 134 and Figure 135 show the interrupting windows and associated k_p values for individual pole clearing of three-phase faults. From Figure 132, it is acceptable to perform a single-phase test with k_{pp} = 1,5 and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 132°. Likewise from Figure 134 and Figure 135, it is acceptable to perform a single-phase test with either k_{pp} = 1,2 or 1,3 as applicable and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 162°. These tests are acceptable because the test requirements for each pole are equalled or exceeded and this has the advantage that only three valid interruptions are required.

IEC 62271-100 recognizes that the testing described above is more onerous and allows that the tests be split into individual tests for each pole and earthing arrangement case (see

6.102.10.2.5 of IEC 62271-100:2008). For the non-effectively earthed case (Figure 132), two test series are: the first at k_{pp} = 1,5 and arcing time in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 42° and the second at k_p = 0,87 and arcing times in the range $t_{arc\ min}$ + 90° to $t_{arc\ min}$ + 132°. For the effectively earthed cases (Figure 134 and Figure 135), three test series are correspondingly required to address all three-pole clearing requirements.

13.3.5 Combination tests for k_{pp} = 1,3 and 1,5

For a requirement with a first-pole-to-clear factor of 1,3, it is possible to adapt the test procedure during tests for a factor of 1,5. In accordance with IEC 62271-100, two alternatives exist:

– For three-phase tests, if a complete series of test-duties demonstrating the circuit-breaker performance for k_{pp} = 1,5 is already performed, test-duties T100s and T100a shall be repeated with a test-circuit simulating the earthing condition of an effectively earthed neutral system. The repetition of test-duties T100s and T100a with a three-phase circuit for an effectively earthed neutral system can, as an alternative, be replaced by additional single-phase tests.

– For single-phase tests both conditions (k_{pp} = 1,5 and k_{pp} = 1,3) may be combined in one test series. The transient and power frequency voltages to be used shall be those applicable to a non-effectively earthed neutral system and the arcing times shall be those applicable to an effectively earthed neutral system.

  For test-duty T100a, the arcing times shall be those applicable to a non-effectively earthed neutral system.

13.3.6 Suitability of a particular short-circuit current rated circuit-breaker for use at an application with a lower short-circuit requirement

In accordance with 8.101 of IEC 62271-100:2008, circuit-breakers that have satisfactorily completed type tests for a combination of rated values (i.e. voltage, normal current, making and/or breaking current) are suitable for any application with lower service values (with the exception of frequency), without further testing.

The reason for this is related to the combination of the transient-recovery-voltage (TRV) requirements and the current values for the basic short-circuit test duties. This can be demonstrated by using the following example where a circuit-breaker tested for a rated voltage U_r of 420 kV, 50 kA rating is considered for an application requirement of 420 kV, 30 kA.

At 420 kV, the T100, T60, T30 and T10 duty TRV values are detailed in Table 26 of IEC 62271-100:2008 and reproduced in an abbreviated form below for convenience.

The circuit-breaker being considered satisfies the TRV peak and rate-of-rise etc. of the duties shown in the upper part of Table 48. Those for the application are shown in a similar form in the lower part of the table and are compared as illustrated by the arrows.

Table 48 – Example of comparison of rated values against application (U_r = 420 kV)

Duty for circuit-breaker (current)	**T100** (50 kA)	**T60** (30 kA)	**T30** (15 kA)	**T10** (5 kA)
TRV peak value	624	669	669	787
Rate of rise	2,0	3,0	5,0	7,0
		↓	↓ ↓	↓ ↓
Duty of application (current)	-	T100 (30 kA)	T60 (18 kA)	T30 (9 kA)	T10 (3 kA)
TRV peak value	-	624	669	669	787
Rate of rise	-	2,0	3,0	5,0	7,0

As can be seen from Table 48, the evidence from the upper part of the table provides significant overlapping evidence for the application shown in the lower part. This is the reason why 8.101 of IEC 62271-100:2008 is acceptable in this case.

Users should exercise due diligence in all cases and most particularly where the difference between the rating and the requirement is so great that the requirements of the application become far removed from the evidence provided by type testing. In such cases, discussions may be required with the supplier. Additional test evidence may be required.

13.4 Asymmetrical currents

13.4.1 Test procedure for test-duty T100a

13.4.1.1 General

A new test procedure was introduced for test-duty T100a in IEC 62271-100:2008/AMD:2017 in order to obtain a better correspondence between the test conditions during three-phase tests and single-phase tests made in substitution for three-phase tests (same amplitude of the major loop, arcing times, etc.). The new test procedure is based on the fact that the relevant major loop of current with full asymmetry to consider before current interruption for the two main test conditions depends on the capability of the circuit-breaker to interrupt after a minor loop of current with intermediate asymmetry. The two main test conditions are as follows:

– interruption of the first-pole-to-clear after a major loop of current with required asymmetry and longest arcing time;

– interruption of a last-pole-to-clear after a major extended loop of current with required asymmetry and longest arcing time in case the of k_{pp} = 1,5 or interruption of the second pole to clear after a major extended loop of current with the required asymmetry and longest arcing time in the case of k_{pp} = 1,3.

This consideration is explained in 13.4.1.2 using the case with k_{pp} = 1,5. In IEC 62271-100:2008, it is not considered necessary to prove interruption of the third-pole-to-clear in case of k_{pp} = 1,3 because the peak of the TRV, di/dt at current zero and the energy in the arc are lower than that of the second-pole-to-clear. The performance of the third-pole-to-clear is verified during test-duty T100s.

A definition has been introduced in IEC 62271-100:2008 to define the minimum clearing time of a circuit-breaker: it is the sum of the minimum opening time, minimum relay time (0,5 cycle) and the shortest arcing time of a minor loop interruption in the phase with intermediate asymmetry that starts with a minor loop at short-circuit current initiation. It will be illustrated by the examples in 13.4.1.2.

13.4.1.2 Basis for test-duty T100a

To illustrate the different cases of three-phase fault interruption presented hereafter the following parameters are chosen:

– rated frequency is 50 Hz, the relay time is 10 ms, k_{pp} = 1,5;

– opening time = 11,5 ms and the shortest arcing time (blue phase) is 5 ms;

– the minimum clearing time is then 10 + 11,5 + 5 = 26,5 ms.

Figure 137 illustrates a first case of three-phase fault interruption in which a first pole (blue phase) clears after minor loop of current with intermediate asymmetry. This is possible as the minimum clearing time is lower than the duration of 27 ms between initiation of the short-circuit current and passage through zero of current in the blue phase.

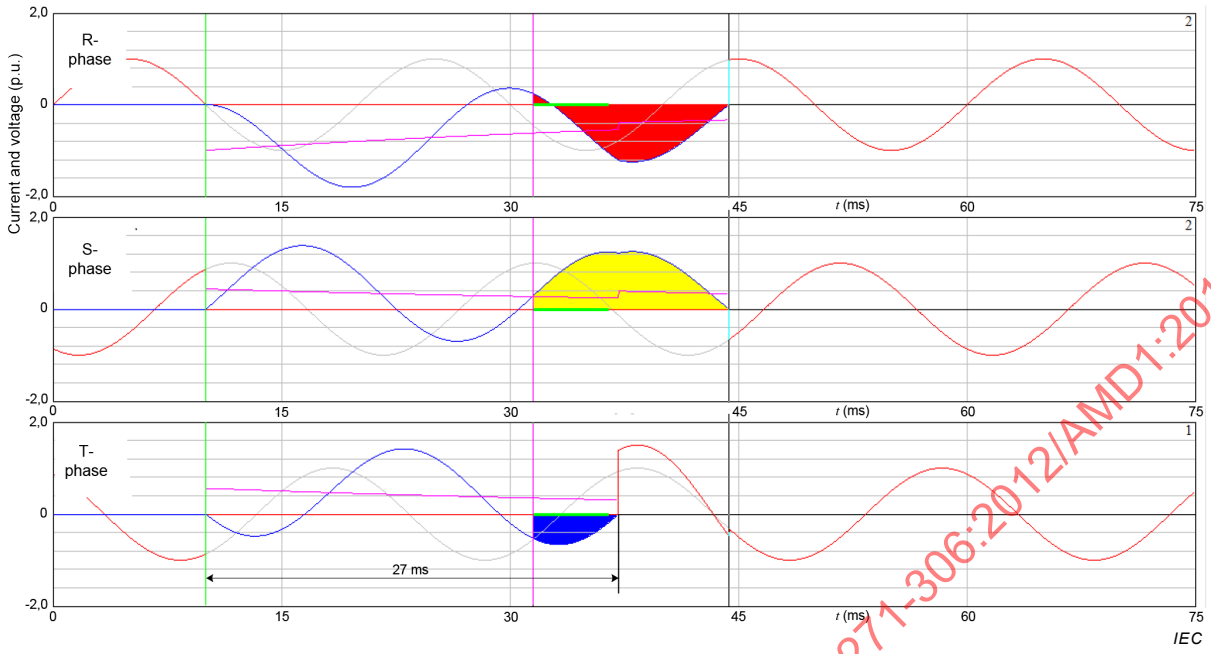


Figure 137a – Case 1 with k_{pp} = 1,5

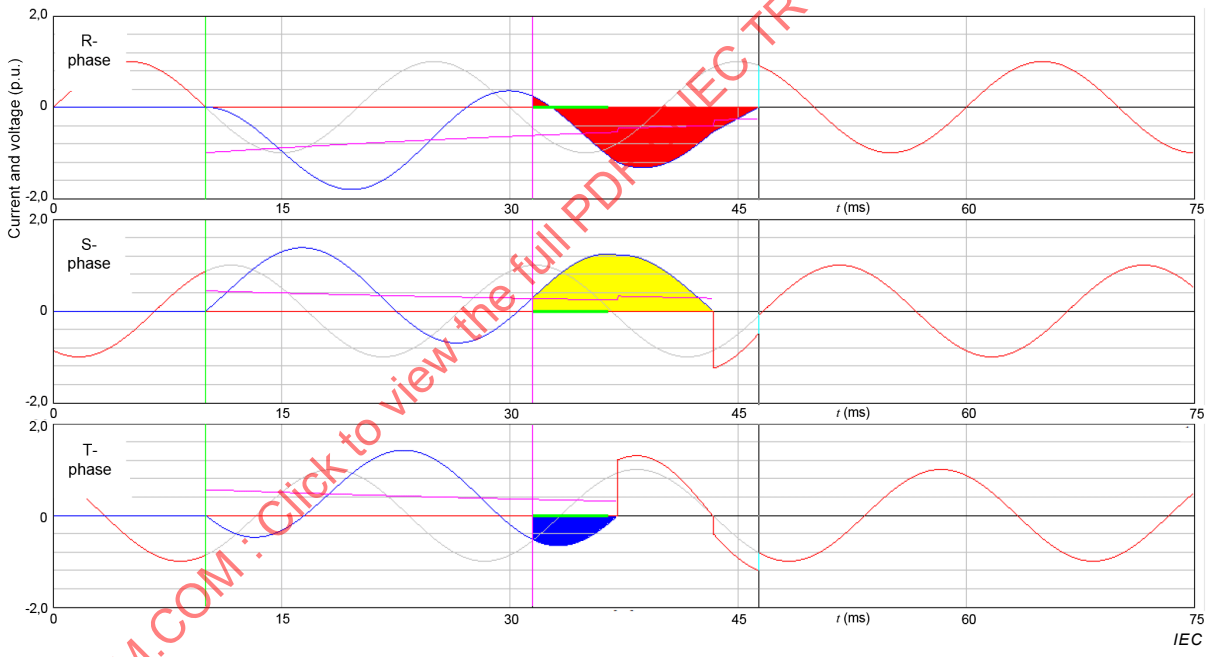


Figure 137b – Case 1 with k_{pp} = 1,3

Figure 137 – Case 1 with interruption by a first pole (blue phase) after minor loop of current with intermediate asymmetry

Figure 138 illustrates case 2 obtained when contact separation is delayed by 18° (1 ms at 50 Hz), a first pole interrupts after a major loop of current with intermediate asymmetry (yellow phase). For the case with k_{pp} = 1,5 a last pole clears a major extended loop with required asymmetry and the longest possible arcing time. For the case with k_{pp} = 1,3 the second pole clears a major loop with required asymmetry and the longest possible arcing time. This is one of the two breaking conditions for which interruption shall be proved.

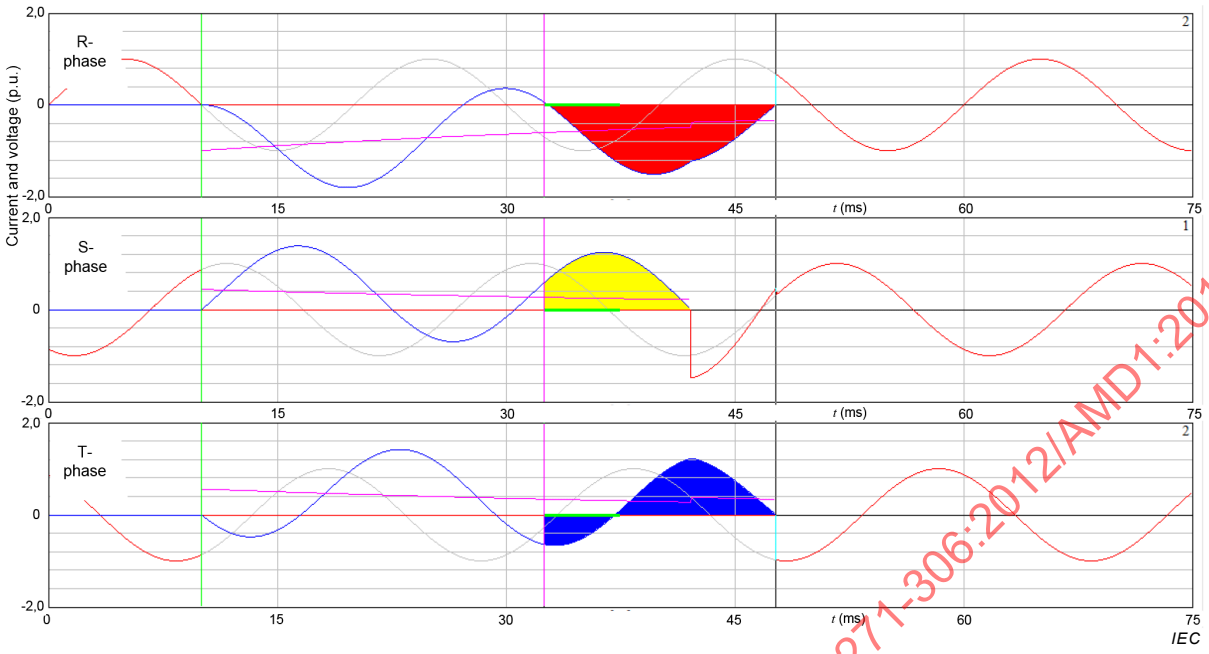


Figure 138a – Case 2 with k_{pp} = 1,5

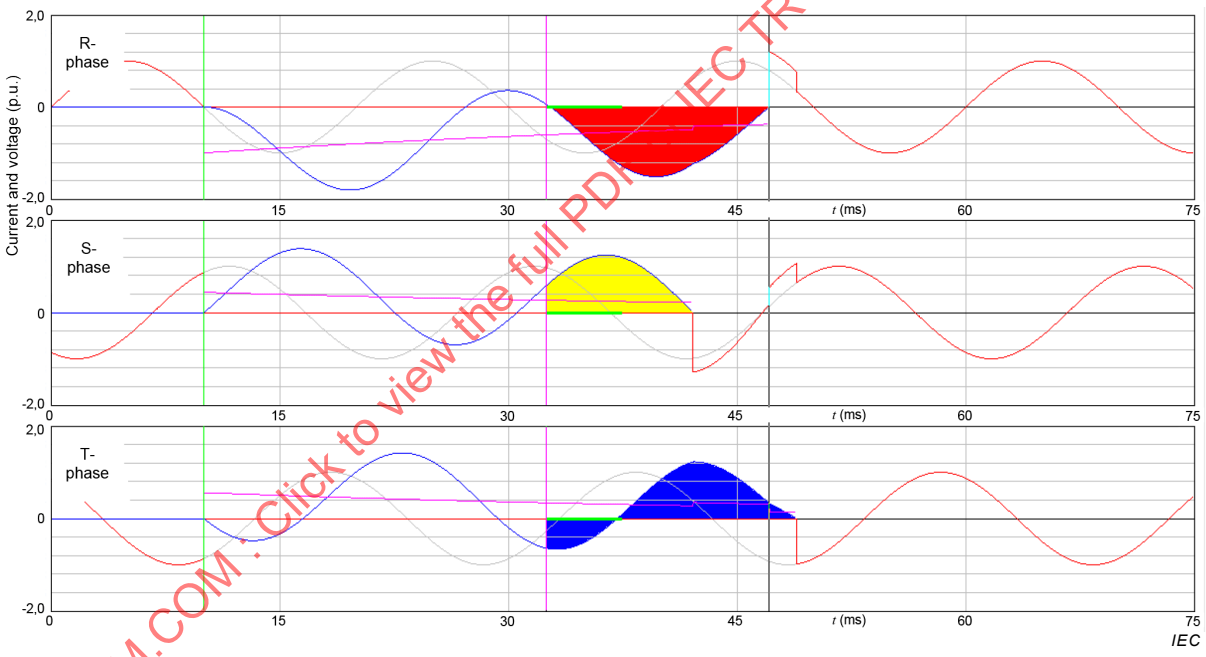


Figure 138b – Case 2 with k_{pp} = 1,3

Figure 138 – Case 2 with interruption of a last pole-to-clear after a major extended loop of current with required asymmetry and longest arcing time

Figure 139 illustrates case 3 obtained when contact separation is delayed by 72°, this test condition is less severe, as last pole that clears in the red phase with a major extended loop has a shorter arcing time.

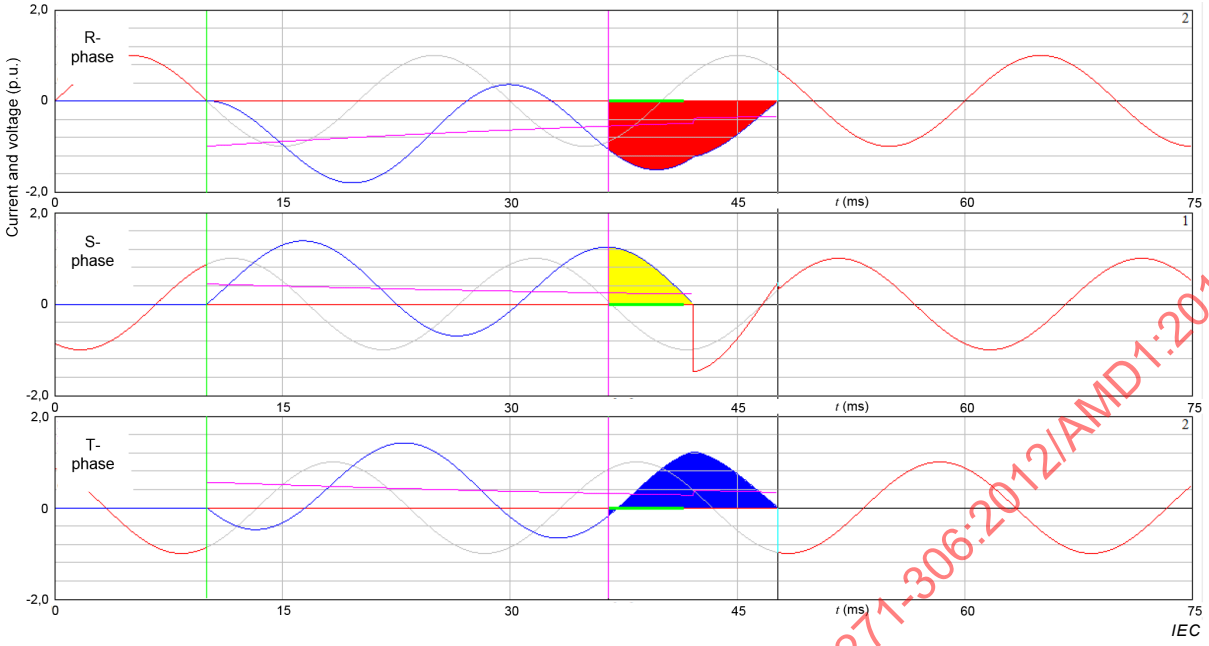


Figure 139 – Case 3 with interruption of a last pole-to-clear after a major extended loop of current with required asymmetry but not the longest arcing time

Figure 140 illustrates case 4 obtained when contact separation is further delayed by 18°. It shows that the first pole clears in the red phase after a major loop with required asymmetry and the longest arcing time for a first-pole-to-clear. It is the second breaking condition for which interruption shall be proved. It should be noted that the major loop with maximum asymmetry to consider for the first-pole-to-clear is the same as seen in case 2 (for a last-pole-to-clear). It is function of the minimum clearing time.

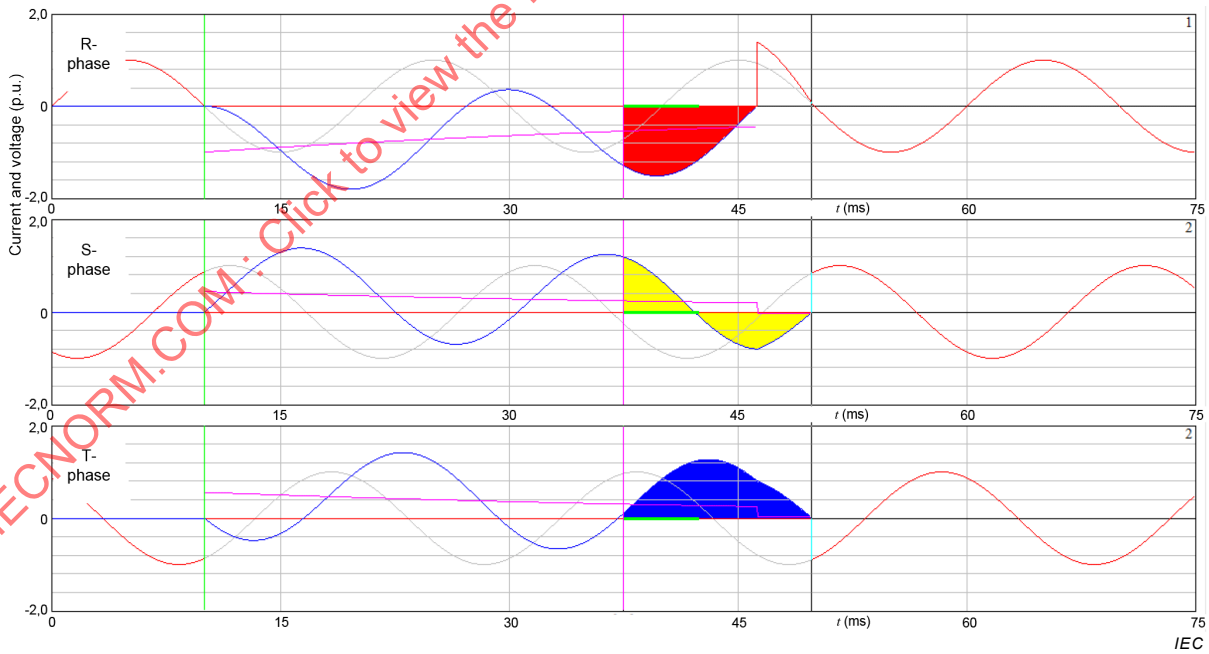


Figure 140 – Case 4 with interruption by the first pole in the red phase after a major loop of current with required asymmetry and the longest arcing time (for a first-pole-to-clear)

The case considered in this example corresponds to the first line of Table 41 in IEC 62271-100:2008/AMD2:2017, i.e. with a minimum clearing time in the interval higher than 10 ms and

equal to or lower than 27 ms. The other intervals of minimum clearing time given in Table 41 are the intervals between each possible instant of interruption after a minor loop in the blue phase.

13.4.2 Advice for the choice of the appropriate time constant

A DC time constant of 45 ms is adequate for the majority of actual cases except for rated voltages higher than 800 kV for which the standard DC time constant is 120 ms. Special case time constants, related to the rated voltage of the circuit-breaker, should cover such cases where the standard time constant 45 ms is not sufficient. This may apply, for example, to systems with very high rated voltage (for example 800 kV systems with higher X/R ratio for lines), to some medium voltage systems with radial structure or to any systems with particular system structure or line characteristics. Special case time constants have been defined, taking into account the results of the survey by CIGRE WG13.04 [139] .

When specifying a special case time constant, the following considerations should be taken into account:

a) The time constants referred to in IEC 62271-100:2008 are only valid for three-phase fault currents. The single-phase to ground short-circuit time constant is lower than that for three-phase fault currents.

b) For maximum asymmetrical current, the initiation of the short-circuit current has to take place at system voltage zero in at least one phase.

c) The time constant is related to the maximum rated short-circuit current of the circuit-breaker. If, for example, higher time constants than 45 ms are expected but with a short-circuit current lower than rated, such a case may be covered by the asymmetrical rated short-circuit current test using a 45-ms time constant.

d) The time constant of a complete system is a time-dependent parameter considered to be an equivalent constant derived from the decay of the short-circuit currents in the various branches of that system and is not a real, single time constant.

e) Various methods for the calculation of the DC time constant are in use, the results of which may differ considerably. Caution should be taken in choosing the right method.

f) When choosing a special case time constant, it has to be kept in mind, that the circuit-breaker is stressed by the asymmetrical current after contact separation. The time instant of contact separation corresponds to the opening time of the circuit-breaker and the reaction time of the protection relay. In this document, this relay time is one half-cycle of power frequency. If the protection time is longer this should be taken into account.

13.4.3 DC component during T100a testing

With the introduction of the special case time constants in IEC 62271-100:2001, the decisive parameters with their respective tolerances that should be followed during interruption of asymmetrical faults need to be defined in order to:

– be able to perform asymmetrical tests with a test circuit having a DC time constant different from the rated DC time constant of the rated short-circuit breaking current, because laboratories are not able to tune the DC time constant of the test circuit. For direct tests, when the DC time constant of the test circuit is higher than the rated DC time constant of the rated short-circuit breaking current, the resulting di/dt and TRV peaks are lower than those that can be seen in service conditions. The reverse situation is also true, mainly with the special case DC time constants (60 ms, 75 ms and 120 ms) introduced in IEC 62271-100:2001;

– be able to use the results obtained from one specific test to cover more than one DC time constant ratings. This concept of asymmetry equivalence may also help the user in establishing equivalence between system needs and the rating requirements.

A lot of calculations made confirm that the former concept of DC component at contact separation (for example IEC 60056 and the first edition of IEC 62271-100:2001) leads to stresses during the tests (including minor and major loop interruptions) being different from

those expected under service conditions. That is why IEC 62271-308 was published in 2002. IEC 62271-308 was incorporated in the first amendment to IEC 62271-100:2001.

The only way to obtain that equivalence is to introduce the concept of DC component at current zero. This concept is also applied in IEC 62271-101.

The maximum prospective DC component at current zero required during tests is determined by using the DC component given for the next complete current loop following the minimum interrupting time.

The parameters concerned by general equivalence criteria are:

a) the amplitude of the last current loop (both major loop or major extended loop);
b) duration of the last current loop (both major loop or major extended loop) before interruption;
c) arcing time;
d) di/dt at current zero;
e) TRV peak voltages, waveshape.

The three first points are linked to the arc energy.

To reach the equivalence according to this concept has led to a modification of some tolerances. For example, the tolerance (0 %, +10 %) on the symmetrical value of the test current has been changed in IEC 62271-100:2008/AMD2:2017 to +10 % and −10 % in order to be able to adjust the last current loop amplitude and duration to the required values. For some cases, it may be necessary to decrease or increase these values from the rated symmetrical short-circuit current.

With this procedure, depending on the actual test parameters, a specific test may cover several ratings if the applicable asymmetry criteria for each rating with their associated tolerances are met.

Annex A gives some guidance on how to use the asymmetry criteria.

13.5 Double earth fault

13.5.1 Basis for specification

This test requirement is limited to applications in non-effectively earthed systems.

In accordance with 6.108 of IEC 62271-100:2008, circuit-breakers applied in non-effectively earthed neutral systems shall be capable of clearing the short-circuit currents that may occur in the case of double earth faults i.e. earth faults on two different phases, one of which occurs on one side of the circuit-breaker and the other one on the other side.

Such a situation can occur if, after a single phase-to-earth fault, the two other phases stay energized long enough to allow another fault to earth to develop on another phase. This situation is unlikely to happen if the healthy phases are opened in a relatively short time after the occurrence of the initial fault. However, it may be provoked by the voltage elevation on healthy phases that is produced by the first fault to earth.

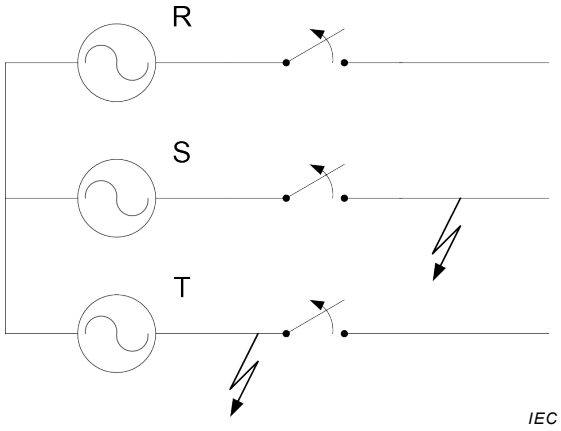


Figure 141 – Representation of a system with a double earth fault

Figure 141 illustrates the case where a fault is present in phase S. Due to the voltage increase on the healthy phases a fault develops on the other side of the circuit-breaker in phase T. The total fault current needs to be interrupted by pole S.

From Figure 141, it can be seen that one pole of the circuit-breaker is required to interrupt a short-circuit under phase-to-phase voltage. As the recovery voltage is higher than in other terminal fault test duties, this breaking condition could be more severe than a terminal fault T100 condition, but, as explained in 13.5.4, the short-circuit current is only 87 % of the rated short-circuit current.

This condition is not covered by test duty T100 and, since it has a low probability of occurrence, IEC 62271-100 requires only one breaking test to be performed. When this standard was established, it was considered that it is only necessary to test with the most severe condition of arcing time, i.e. with a long arcing time corresponding to a high energy content of the arc and with a moving contact position close to the fully open position.

13.5.2 Short-circuit current

The calculation of the short-circuit current is detailed in 13.5.4.

A symmetrical current is specified in testing, as in test duty T100s, because a symmetrical condition leads to the highest TRV peak possible when compared to the value specified for test duty T100.

13.5.3 TRV

The RRRV is the same as for terminal fault test duty T100s. The voltage factor for the double earth fault is $\sqrt{3}$, since the full phase-to-phase voltage is applied to one pole, whereas it is 1,5 for terminal fault. The di/dt is obtained by multiplying the di/dt value of T100s by $\frac{\sqrt{3}}{2}$. It follows that the rate of rise of recovery voltage is equal to the values of T100s multiplied by $\frac{\sqrt{3}}{1,5} \times \frac{\sqrt{3}}{2} = 1$

Specified TRVs with two parameters and four-parameters are determined from the RRRV and a pole-to-clear factor of $\sqrt{3}$. They are given in Table 28 of IEC 62271-100:2008.

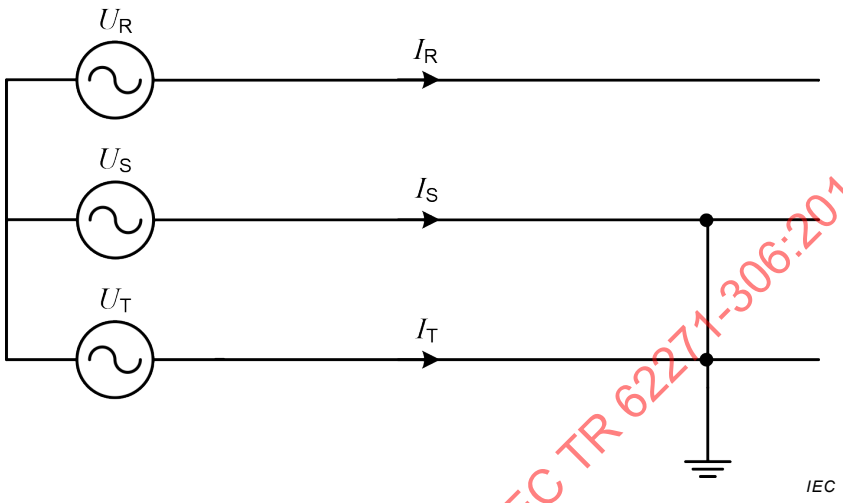
In the case of a two-parameter TRV, t_3 is derived from u_c and the RRRV.

In the case of a four-parameter TRV, u_1 and u_c are calculated on the basis of a pole-to-clear factor of $\sqrt{3}$, t_1 is derived from u_1 and the RRRV and $t_2 = 4 \times t_1$.

13.5.4 Determination of the short-circuit current in the case of a double-earth fault

Figure 142 shows a schematic representation of the fault case illustrated in Figure 141.

Phase supply voltage is U.



Key

U_R, U_S, U_T	Voltages in R, S and T-phase, respectively
I_R, I_S, I_T	Currents in R, S and T-phase, respectively

Figure 142 – Representation of circuit with double-earth fault

The circuit in Figure 142 is analysed using symmetrical components. The indices used are 0 for zero sequence component, 1 for the positive sequence component and 2 for the negative sequence component.

$I_R = 0 \quad \rightarrow \quad I_0 + I_1 + I_2 = 0$

$U_S = 0 \quad \rightarrow \quad U_0 + a^2 U_1 + a U_2 = 0$

$U_T = 0 \quad \rightarrow \quad U_0 + a U_1 + a^2 U_2 = 0$

with

$a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

$$U_1 = U - X_1 I_1 \tag{178}$$

$$U_2 = -X_2 I_2 \tag{179}$$

$$U_0 = -X_0 I_0 \tag{180}$$

this gives:

$-X_0 I_0 + a^2 (U - X_1 I_1) - a X_2 I_2 = 0$

$-X_0 I_0 + a (U - X_1 I_1) - a^2 X_2 I_2 = 0$

$I_1 + I_2 + I_0 = 0$

or,

$$a^2 X_1 I_1 + a X_2 I_2 + X_0 I_0 = a^2 U \quad (181)$$

$$a X_1 I_1 + a^2 X_2 I_2 + X_0 I_0 = a U \quad (182)$$

$$I_1 + I_2 + I_0 = 0 \quad (183)$$

Multiplying Equation (182) with "a" and subtracting Equation (181) leads to:

$$(1 - a) X_2 I_2 + (a - 1) X_0 I_0 = 0 \Rightarrow X_2 I_2 = X_0 I_0 \quad (184)$$

Multiplying Equation (181) with "a" and subtracting Equation (180) leads to:

$$X_1 I_1 (1\text{-}a) + (a\text{-}1) X_0 I_0 = (1\text{-}a) U \rightarrow X_1 I_1 - X_0 I_0 = U \quad (185)$$

A system of 3 equations with 3 unknown is obtained:

$$I_1 + I_2 + I_0 = 0 \quad (186)$$

$$X_2 I_2 = X_0 I_0 \quad (187)$$

$$X_1 I_1 - X_0 I_0 = U \quad (188)$$

Resolution of Equations (186), (187) and (188):

$$I_1 + \frac{X_0 I_0}{X_2} + I_0 = 0$$

$$I_0 \times \frac{X_2 + X_0}{X_2} = -I_1 \quad I_0 = -\frac{I_1 X_2}{X_2 + X_0}$$

$$X_1 I_1 + \frac{X_0 X_2}{X_2 + X_0} \times I_1 = U \text{ , or } I_1 \left(X_1 + \frac{X_0 X_2}{X_2 + X_0} \right) = U \Rightarrow I_1 = \frac{U}{X_1 + \frac{X_0 X_2}{X_2 + X_0}} \quad (189)$$

and

$$I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (190)$$

$$I_2 = -I_1 - I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (191)$$

The current in phase S is given by:

$I_S = I_0 + a^2 I_1 + a I_2$ with $a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

From Equations (190) and (191), and with the standard hypothesis $X_2 = X_1$:

$$I_S = -\frac{X_1 I_1}{X_1 + X_0} + a^2 I_1 - a\frac{X_0 I_1}{X_1 + X_0}$$

$$\frac{I_S}{I_1} = \frac{-X_1 + a^2 X_1 + a^2 X_0 - aX_0}{X_1 + X_0} = \frac{-X_1\left(3/2 + j\frac{\sqrt{3}}{2}\right) - jX_0\sqrt{3}}{X_1 + X_0}$$

Using the equation for I_1 given in Equation (188), the current for the double earth fault (I_{def}) is then:

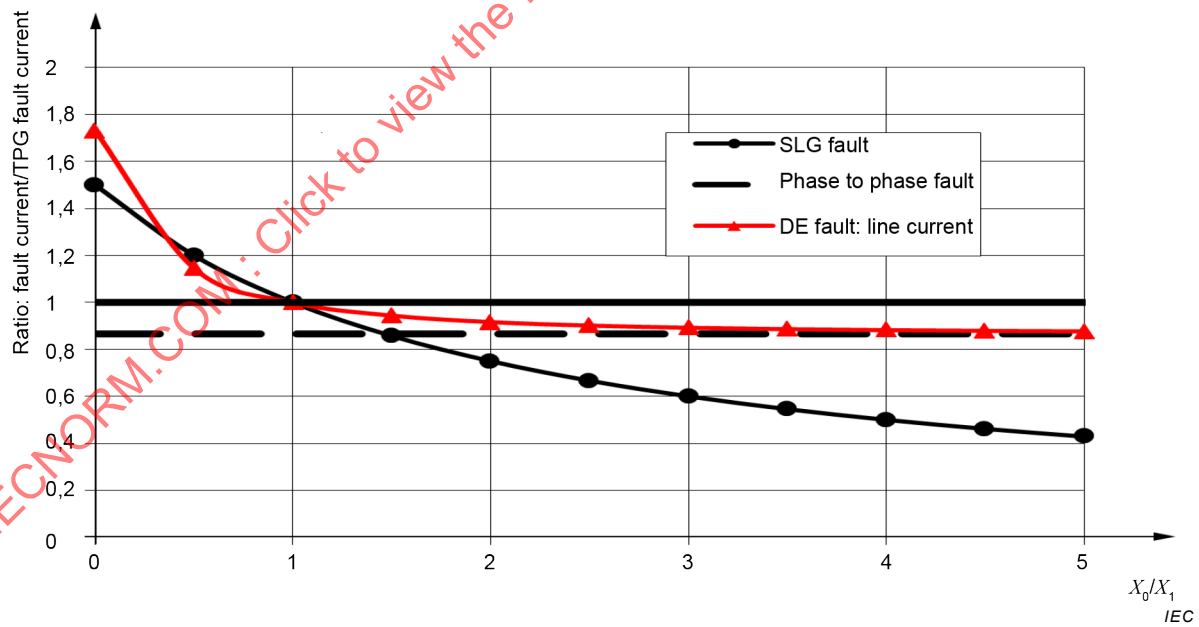
$$I_{def} = I_S = \frac{-U\sqrt{3}}{X_1 + 2X_0}\left(\frac{\sqrt{3}}{2} + \frac{j}{2} + j\frac{X_0}{X_1}\right)$$

For non-effectively earthed networks $X_0 >> X_1$, which gives:

$$I_{def} = -\frac{U\sqrt{3}}{X_1 + 2X_0} \times j\frac{X_0}{X_1} = -j\frac{U\sqrt{3}}{2X_1}$$

The three-phase short-circuit is given by $I_{sc} = U/X_1 \Rightarrow I_{def} = -j\frac{\sqrt{3}}{2} I_{sc}$, or $|I_{def}| = 0{,}87|I_{sc}|$.

Fault currents relative to the three-phase short-circuit current are shown in Figure 143 for this case and for other fault cases.



Key

SLG fault	Single-line to earth fault	TPG fault	Three-phase to earth fault
DE fault	Double earth fault	Solid line	Three-phase to earth current

Figure 143 – Fault currents relative to the three-phase short-circuit current

13.6 Break time

The break time of a circuit-breaker is the maximum interval between the instant of initialization of the opening operation (i.e. energizing of the trip circuit) and the instant of interruption of the current in all three phases during terminal fault test-duties T30, T60 and T100s under the following conditions:

– rated auxiliary supply voltage and frequency;

– rated pressures for operation, insulation and interruption;

– an ambient air temperature of (20 ± 5) °C.

The break time is defined based on the minimum arcing time because the longest recorded arcing time during the tests can be longer than under the actual field condition.

Terminal fault tests are carried out at the minimum auxiliary supply voltage and/or pressures for operation and/or interruption. For convenience of testing, the auxiliary supply voltage may be the rated or maximum value as long as it does not affect the making or breaking capability. (The operating times of some circuit-breakers may vary with the auxiliary supply voltage). In order to verify the break time during these test-duties, the maximum break time should be amended to take account of the lower auxiliary supply voltage and pressures as follows:

$$t_{\mathrm{bmax}} = t_{\mathrm{or}} + t_{\mathrm{am}} + t_{\mathrm{w}} - \frac{18^{\mathrm{o}}}{360^{\mathrm{o}}} \times T$$

where

t_{bmax} is the maximum determined break time;

t_{or} is the opening time under rated conditions (recorded during no-load operation at rated supply voltage and frequency of closing and opening devices and of auxiliary circuits, at rated pressure for operation and at a ambient temperature of 20 °C ± 5 °C)

t_{am} is the longest of the recorded minimum arcing times during test-duties T30, T60 and T100s;

$\frac{18^{\mathrm{o}}}{360^{\mathrm{o}}} \times T$ takes the uncertainty in the determination of the minimum arcing time into account;

T is one period of power frequency (20 ms for 50 Hz, 16,7 ms for 60 Hz) and t_{w} is the necessary interrupting window expressed in ms:

– for single-phase tests in substitution for three-phase conditions

  • non-effectively earthed neutral systems: t_{we} = 150 − dα

  • effectively earthed neutral systems: t_{we} = 180 − dα

– for three-phase tests

  t_{we} = 60 − dα

  t_{we} is expressed in electrical degrees

$$t_{\mathrm{w}} = \frac{t_{\mathrm{we}}}{360^{\mathrm{o}}} \times T$$

dα is the tripping impulse step in the search for the minimum arcing time, it is equal to 18 electrical degrees.

If the maximum break time determined according to this procedure exceeds the break time, the test-duty that has given the longest break time may be repeated with auxiliary supply voltage and pressure for operation and interruption at their rated values.

NOTE The break time during a make-break operation may be longer than that of a single break operation for some circuit-breaker designs. Such longer break times may impact system protection strategy and stability if the delay is longer than the relay time. Users should advise the manufacturer of the maximum allowable break time during make-break operations.

14 Double earth fault

Replace the entire clause, including its title, by the following new content:

14 Synthetic making and breaking tests

14.1 General

With the increasing voltage and current ratings of circuit-breakers, the total available short-circuit power of a high power laboratory has to be increased accordingly. The investments required to increase the short-circuit power are very high. In order to still be able to perform the correct type tests on circuit-breakers with the available short-circuit power, synthetic tests are performed.

Requirements for synthetic testing and examples of synthetic circuits are given in IEC 62271-101.

Generally a synthetic test circuit consists of separate current and voltage circuits (see Figure 144). During the high-current interval, the short-circuit current will be fed from a current circuit (source providing the necessary current at a reduced voltage). This reduced voltage should have an amplitude of sufficient magnitude to prevent the arc voltage from distorting the short-circuit current in such a way that the circuit-breaker is not stressed in the same way as under system conditions. For tests that need less power (e.g. capacitive current switching tests), some synthetic test circuits using a single source can also be used.

When the current is interrupted by the circuit-breaker under test (TB in Figure 144), the voltage circuit will give the correct voltage stresses across the contact gap. An auxiliary circuit-breaker (AB in Figure 144) is used to separate the voltage circuit from the current circuit, thus avoiding that the high-voltage from the voltage circuit stresses the current circuit.

The principle used for the making operation is similar. The voltage circuit first provides the correct voltage stress during the closing operation and as soon as the pre-arcing occurs, the current circuit will then provide the correct short-circuit current.

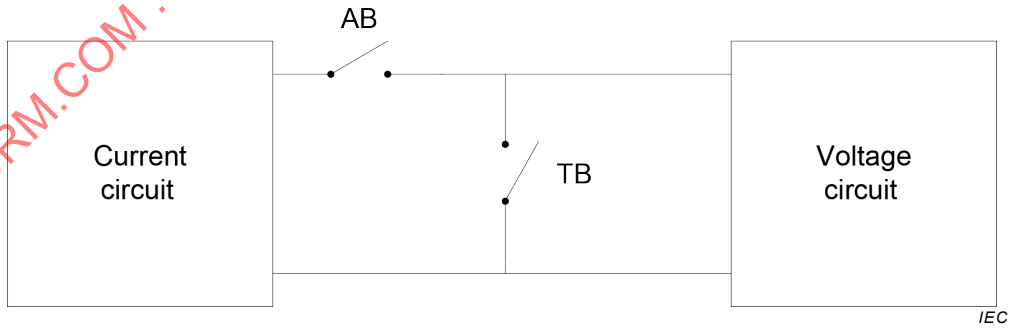


Figure 144 – Principle of synthetic testing

In order for a synthetic test to be valid, the following requirements should be met:

– the arc energy in the contact gap should be equal to that of a direct test;
– the di/dt at current zero should be in accordance with the current and frequency specified;
– the recovery voltage should appear immediately after current zero i.e. without delay;

– the prospective TRV should be at least equal to the required TRV;
– the voltage source should have a sufficient power to avoid excess damping of the transient process by the post arc current.

Synthetic testing allows in general testing at one particular arcing time per operation. In order to cover the full extinguishing window, it may be necessary to use re-ignition circuits.

14.2 Current injection methods

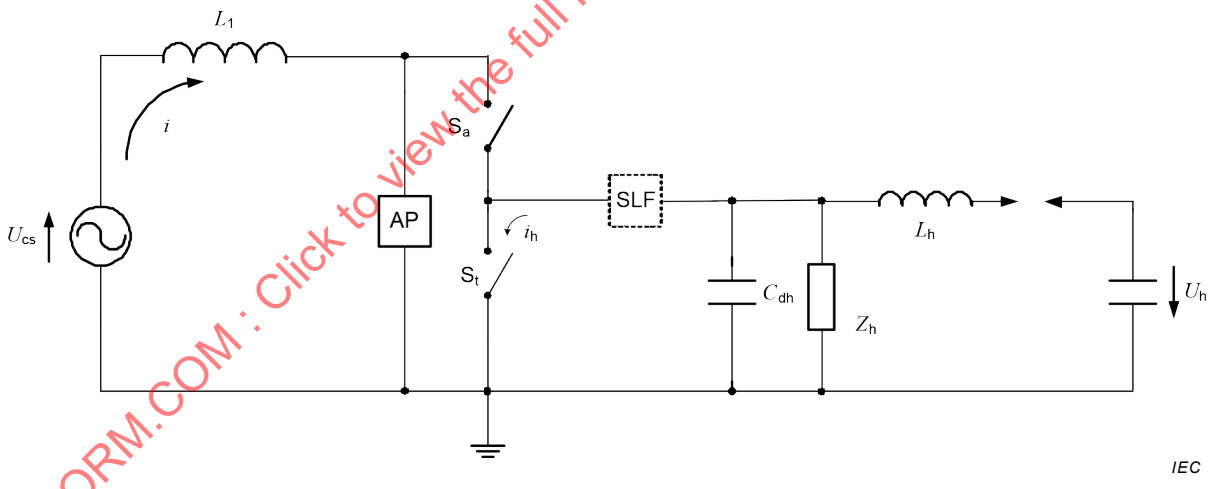
14.2.1 General

In a synthetic test circuit using current injection, the superposition of the currents takes place shortly before the zero of the power-frequency short-circuit current. A current of smaller amplitude but higher frequency, derived from the voltage circuit, is superimposed either in the test circuit-breaker or in the auxiliary circuit-breaker. The instant of switching in this injected current is selected by means of a current-dependent control circuit. This instant should be such that the character of the resulting current wave in the test circuit-breaker corresponds to that of the specified breaking current prior to the current zero during the interval of significant change of arc voltage.

In this way, the circuit-breaker under test is automatically connected into the voltage circuit after the interruption of the current in the auxiliary circuit-breaker, so there will be no delay between the current stress and the application of the voltage stress.

14.2.2 Current injection circuit with the voltage circuit in parallel with the test circuit-breaker (parallel circuit)

Figure 145 shows the simplified circuit diagram of a current injection circuit with the voltage circuit connected in parallel with the test circuit-breaker.



Key

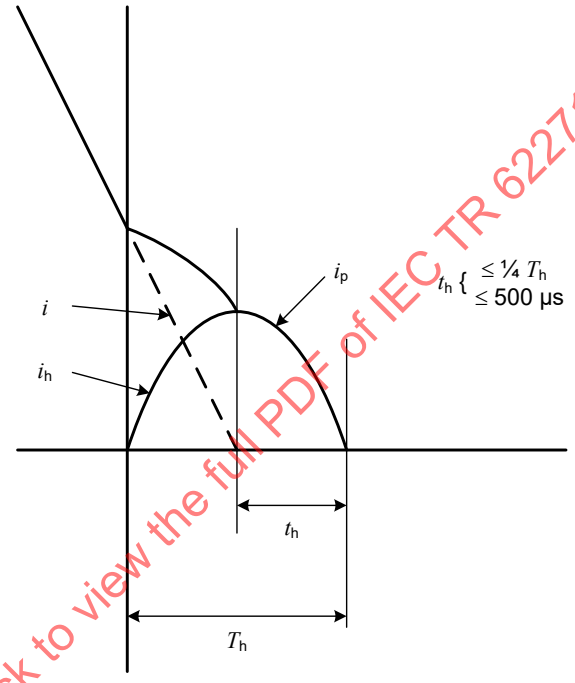
U_{cs}	voltage of current circuit	C_{dh}	capacitance for time delay of voltage circuit
L_1	inductance of current circuit	L_h	inductance of voltage circuit
AP	arc prolonging circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker	i	current of the current circuit
S_t	test circuit-breaker	i_h	injected current
Z_h	equivalent surge impedance of voltage circuit	SLF	short-line-fault circuit (for the corresponding tests)

Figure 145 – Typical current injection circuit with voltage circuit in parallel with the test circuit-breaker

The voltage circuit is switched in shortly before the zero of the power-frequency short-circuit current, prior to the interaction interval. At this time, the high-frequency oscillatory current i_h is superimposed on the power-frequency short-circuit current i, with the same polarity to give a resultant test current in the test circuit-breaker.

After the auxiliary circuit-breaker interrupts the power-frequency short-circuit current i, the test circuit-breaker is connected only to the voltage circuit and i_h is the only remaining current. The voltage circuit also provides the recovery voltage across the test circuit-breaker after the current is interrupted.

Figure 146 shows an example of injection timing. The two points of inflection typically indicate the start of the current injection in the test circuit-breaker and the interruption of the power-frequency short-circuit current by the auxiliary circuit-breaker. The waveshape of the transient recovery voltage can be adjusted by varying the values of Z_h and C_{dh} (Figure 145), to obtain compliance with the requirements of IEC 62271-100 (see 4.1.4 of IEC 62271-101:2012).



Key

i	current in the auxiliary circuit-breaker	T_h	duration of one period of the injected current
i_h	injected current	t_h	time during which the arc is fed only by the injected current
i_p	current in the test circuit-breaker		

Figure 146 – Injection timing for current injection scheme with the circuit given in Figure 145

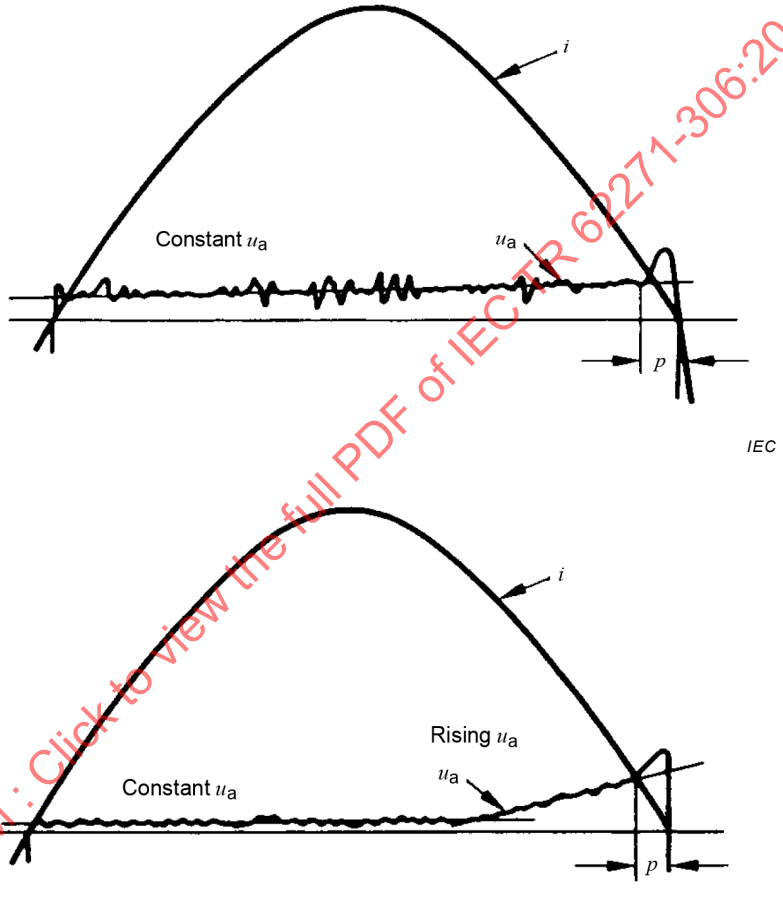
14.2.3 Current injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)

As the series current injection method is not used by laboratories, it is no longer under consideration.

14.2.4 Determination of the interval of significant change of the arc voltage

To determine the interval of significant change of the arc voltage that occurs immediately prior to current zero, the following method may be applied, dependent on individual arc voltage characteristics.

The arc voltages of circuit-breakers vary considerably in general shape. In many cases, the arc voltage is not steady but fluctuates about a mean value. This mean value is obtained by drawing a smooth curve in the middle, between the maximum and minimum arc voltage levels (Figure 147). This curve can be used to identify significant changes. The shape of mean arc voltage characteristics may also vary widely.



Key

i	current	p	interval of significant change of arc voltage
u_a	arc voltage		

Figure 147 – Examples of the determination of the interval of significant change of arc voltage from the oscillograms

Most circuit-breakers show a nearly constant or steadily rising arc voltage during the current loop, with an appreciable increase just prior to current zero. In such cases, it is not difficult to determine from the oscillogram the instant at which a significant change begins. For this purpose, it is preferable to use an oscillograph giving a relatively large deflection for the arc

voltage and having a time scale that is fast enough to enable the interval of significant change of arc voltage to be measured accurately.

In some cases, it may be difficult to determine the interval of significant change of arc voltage because

a) the arc voltage remains nearly constant or steadily rises during the current loop almost to the instant of current zero,

b) changes in the arc voltage occur considerably before the current zero.

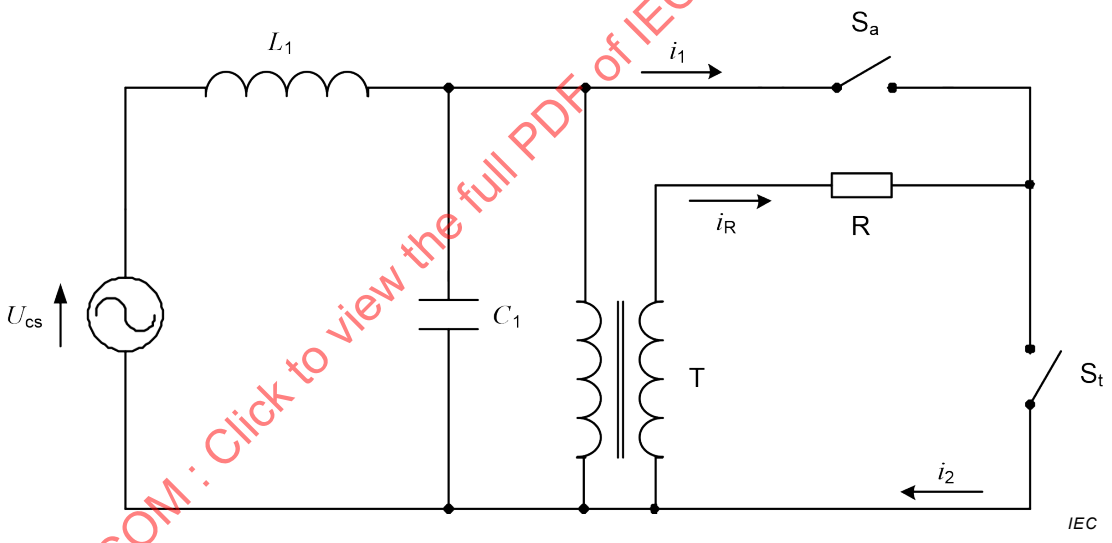
In these cases, an injection current frequency as low as possible should be used, taking account also of the requirements in 4.2.1 of IEC 62271-101:2012.

14.3 Duplicate transformer circuit

14.3.1 Principle of the method

In the duplicate test circuit (also known as the Skeats circuit), the current is supplied from a current circuit to the series combination of the auxiliary and the test circuit-breaker. The high voltage is applied to the test circuit-breaker via a resistance from a transformer (or auto-transformer), the primary of which is connected to the current circuit across the auxiliary and test circuit-breakers.

Figure 148 shows the principal layout of the circuit.



Key

U_{cs}	voltage of the current circuit	i_1	current through the auxiliary circuit-breaker
L_1	inductance of current circuit	i_2	current through the test circuit-breaker
C_1	capacitance of the current circuit which together with L_1 controls the first part of the TRV	i_R	current through resistor R
T	transformer	S_a	auxiliary circuit-breaker
R	phase-shifting resistor	S_t	test circuit-breaker

Figure 148 – Transformer or Skeats circuit

During the high-current interval, the arc voltages of the test and auxiliary circuit-breakers induce a current, i_R in the high-voltage circuit that adds to the current through the test circuit-breaker, $i_2 = i_1 + i_R$. The current in the auxiliary breaker will thus reach zero and interrupt

before the test circuit-breaker. If the arc voltages are assumed nearly constant, the test circuit-breaker current will go through zero at a time Δt after the interruption of the auxiliary breaker approximately given by:

$$\Delta t = \frac{n\,(u_{aa} + u_{at}) - u_{at}}{n \times \hat{u}_{cs}} \times \frac{L_2}{R}$$

where

n is the transformer ratio;

u_{aa}, u_{at} are the arc voltages in S_a and S_t, respectively;

$\hat{u}_{cs}$ is the voltage peak of the current circuit;

L_2 = $n^2 L_1$ + L_T (effective inductance in the high-voltage circuit);

L_T is the leakage inductance of T.

During the interval Δt, the rate of change of the current through the test circuit-breaker di_2/dt will approximately attain the value:

$$\frac{di_2}{dt} = -\frac{n \times \hat{u}_{cs}}{L_2} = -\frac{n\,\hat{u}_{cs}}{n^2 L_1 + L_T}$$

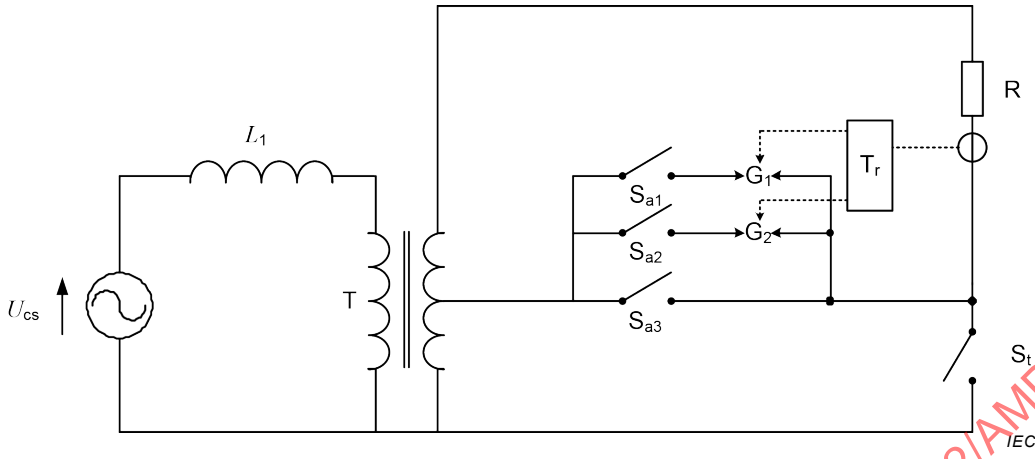
i.e. di_2/dt will be lower than the prospective uninfluenced value. This value is reduced by a factor of the same magnitude as the transformer ratio n.

By choosing the value R of the resistance R sufficiently large, the time interval Δt could be kept small. On the other hand, a high value will increase the damping of the TRV. For circuit-breakers with post-arc current, the value may be further restricted. Values of R in the range some kΩ are normally used, giving $\Delta t \leq 10$ μs.

The test circuit could be used when testing the dielectric recovery of a circuit-breaker. It could further be used for closing tests and could be extended to work with several full voltage applications.

14.3.2 Practical arrangement of the circuit

A practical circuit arrangement is shown in Figure 149. The circuit illustrated in Figure 149 can be used to apply full recovery voltage in three consecutive current zeros in an opening operation by opening the auxiliary circuit-breakers S_{a1}, S_{a2} and S_{a3} in turn. The spark gaps G_1 and G_2 are triggered to restore the current if the test circuit-breaker fails to interrupt in the first and second current zero respectively.



Key

U_{cs}	voltage of the current circuit	S_{a1}, S_{a2}, S_{a3}	auxiliary circuit-breakers
L_1	inductance of current circuit	S_t	test circuit-breaker
T	transformer	T_r	triggering circuit
R	phase-shifting resistor	G_1, G_2	triggered gaps

Figure 149 – Triggered transformer or Skeats circuit

Figure 149 can also apply full voltage stresses at both closing and opening in a CO operating cycle. The test circuit-breaker S_t closes against full voltage (S_{a1} is open) and, when it pre-strikes, one of the spark gaps, e.g. G_2, is triggered to make the current circuit (S_{a2} is closed). S_{a3} is closed before the opening of the test circuit-breaker and used as auxiliary circuit-breaker at the first current zero. If necessary, a second current zero could be tested by means of G_1 and S_{a1}.

In a similar manner the two opening operations in an auto-reclosing operation can be fully tested.

14.4 Voltage injection methods

14.4.1 General

In a synthetic test circuit using voltage injection, the current circuit provides the entire short-circuit current for the test circuit-breaker and also, after current zero, the first part of the transient recovery voltage.

By suitable choices of its voltage and natural frequency, the correct values of the power factor, current and first part of the TRV can be obtained.

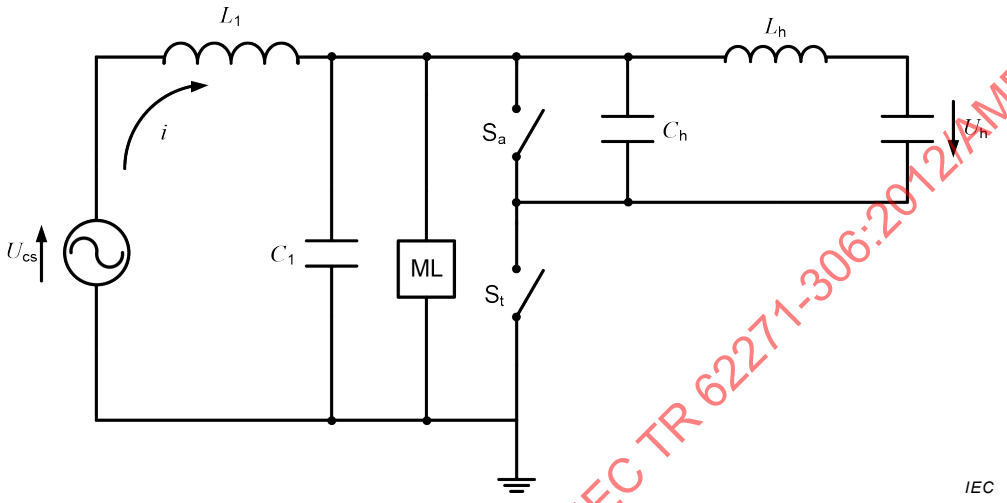
About the time of the first peak of the transient recovery voltage of the current circuit, the voltage circuit is switched in by means of a voltage-dependent control circuit in such a way that the specified transient recovery voltage is continued and so that there will be no delay between the current stress and the voltage stress.

A voltage injection test circuit is not valid for tests where attention is paid to the short-line fault tests and terminal fault tests with ITRV, because

– the source-side impedance does not correspond to network (or direct test circuit) conditions during the interaction interval;
– the di/dt deviates from the prospective value during a (short) time interval just before current zero.

14.4.2 Voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)

Figure 150 shows the simplified circuit diagram of a voltage injection circuit with the voltage circuit connected in parallel with the auxiliary circuit-breaker. The current circuit supplies the entire short-circuit current stress. A capacitor of suitable value is connected in parallel with the auxiliary circuit-breaker. After the current zero of the power-frequency short-circuit current, this capacitor transmits the entire transient recovery voltage of the current circuit to the test circuit-breaker, passing the necessary energy for the post-arc current.



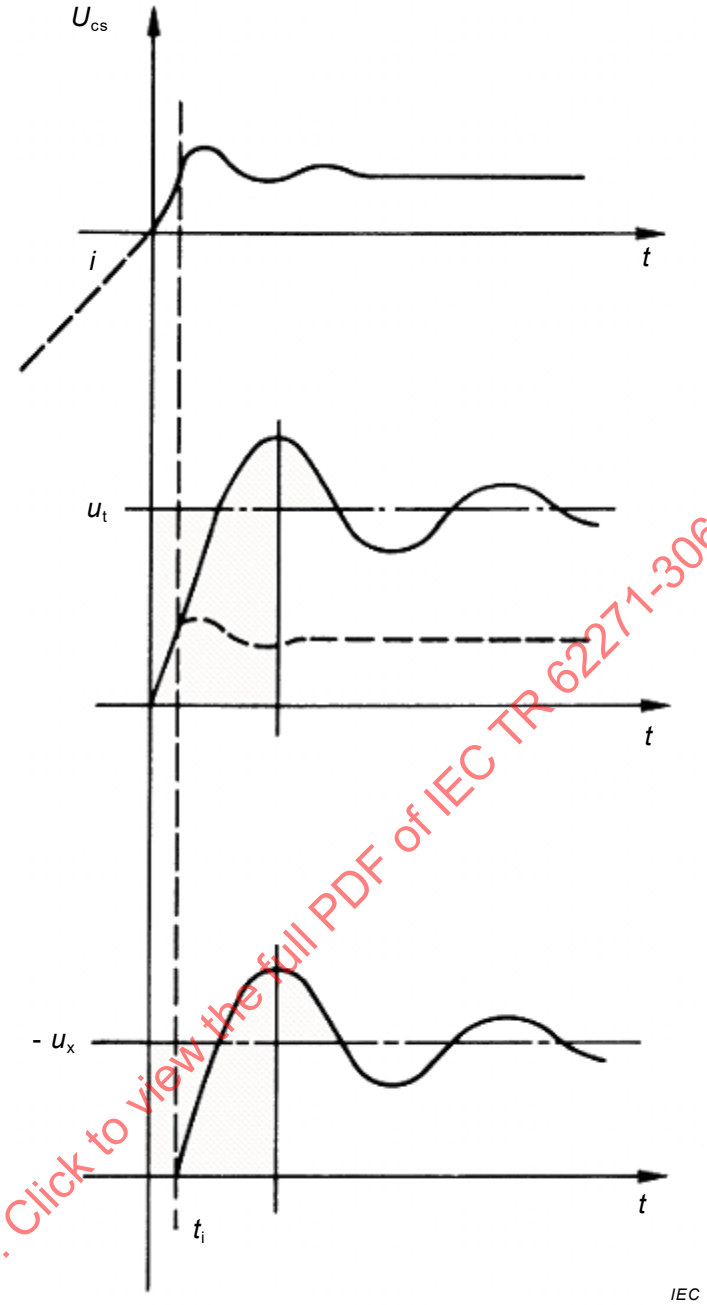
Key

U_{cs}	voltage of current circuit	S_t	test circuit-breaker
L_1	inductance of current circuit	C_h	capacitance of voltage circuit which together with L_h controls the major part of the TRV
C_1	capacitance of current circuit which together with L_1 controls the first part of the TRV	L_h	inductance of voltage circuit
ML	multi-loop reignition circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker	i	current of the current source

Figure 150 – Typical voltage injection circuit diagram with voltage circuit in parallel with the auxiliary circuit-breaker (simplified diagram)

About the time of the first peak of this transient voltage, the voltage circuit will be switched in and from this moment onwards the transient recovery voltages of both circuits are added together to form the transient recovery voltage across the test circuit-breaker.

Figure 151 shows the current in the test circuit-breaker and the waveshape of the voltage across the auxiliary circuit-breaker and test circuit-breaker. The auxiliary circuit-breaker is stressed only by the voltage of the voltage circuit. Both components of the voltage across the test circuit-breaker are superimposed to produce the transient recovery voltage, the waveshape of which can be adjusted by varying C_h and C_1 in conjunction with additional components – not shown in Figure 150 – to obtain compliance with the requirements of IEC 62271-100 (see 4.1.4 of IEC 62271-101:2012).



Key

i	power-frequency current in test and auxiliary circuit-breakers	u_t	voltage across test circuit-breaker
U_{cs}	TRV from current circuit	u_x	voltage across auxiliary circuit-breaker
		t_i	instant of voltage injection

Figure 151 – TRV waveshapes in a voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker

14.4.3 Voltage injection circuit with the voltage circuit in parallel with the test circuit-breaker

This voltage injection circuit is similar to the one described above except that the voltage circuit is in parallel with the test circuit-breaker instead of the auxiliary circuit-breaker. It is not in common usage.

14.5 Current distortion

14.5.1 General

Current distortion is a well-known factor that should be considered during synthetic testing. Subclauses 14.5.2, 14.5.3 and 14.5.4 give a basic analysis using simplified methods. In practice, digital calculations by computers may be more appropriate where various arc voltage waveshapes can be introduced.

14.5.2 Current distortion immediately prior to current zero

The interaction interval begins when the arc voltage starts to change significantly as the current approaches zero. The change of the arc voltage during this time influences the shape and the rate-of-change of the current immediately before current zero.

This deviation from the prospective current curve is caused by the distortion current, which mainly flows in the low time constant impedance, taking into account all parameters of the actual circuit.

The particular way in which the current approaches zero is responsible for the physical conditions of the medium between the arcing contacts of a circuit-breaker at current zero. The major interaction between circuit and circuit-breaker is caused by the arc voltage charging and discharging capacitances and influencing di/dt just before zero.

In a simplified circuit, as in Figure 152 representing a short-circuit in service or a direct test, the voltage u supplies an arc current i with the appropriate arc voltage u_a. Parallel to the arc is a capacitor C.

If it is assumed that the arc voltage u_a = 0, then a prospective short-circuit current i_p (see Figure 153) will flow through the arc, the magnitude and waveshape of this current being determined by the inductance L, the voltage u, the frequency of this voltage and the moment of current initiation.

If it is assumed that the supply voltage u = 0 and that an arc voltage exists, then the arc voltage will produce a current flow. This current i_d (see Figure 154) is the distortion current, which will flow partly as i_{dL} through the inductance L, and partly as i_{dC} through the capacitance C. For this condition, the following equations apply:

$$u_a - L \times \frac{d}{dt}(i_{dL}) = 0$$

and

$$C \frac{d}{dt}(u_a) - i_{dC} = 0$$

From these, the following equation for i_d can be obtained:

$$i_d = i_{dL} + i_{dC} = \frac{1}{L} \int u_a \, dt + C \times \frac{d}{dt}(u_a)$$

If both of the voltages, u and u_a are present (see Figure 155), then the resulting actual current is given by:

$$i = i_p - i_d$$

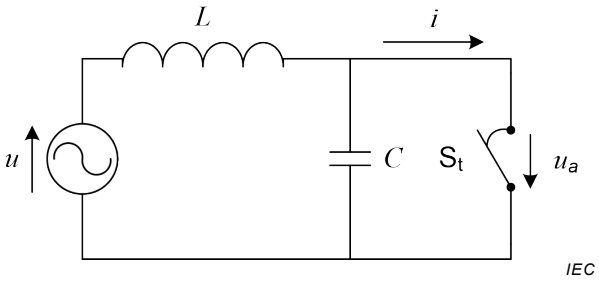


Figure 152 – Direct test circuit, simplified diagram

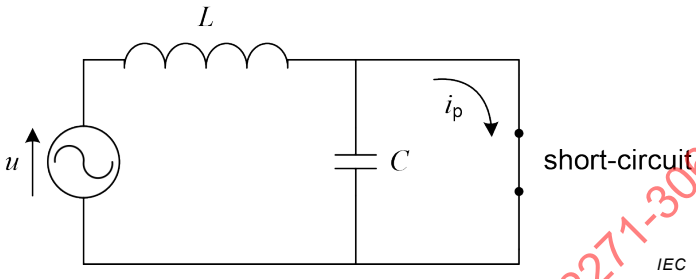


Figure 153 – Prospective short-circuit current flow

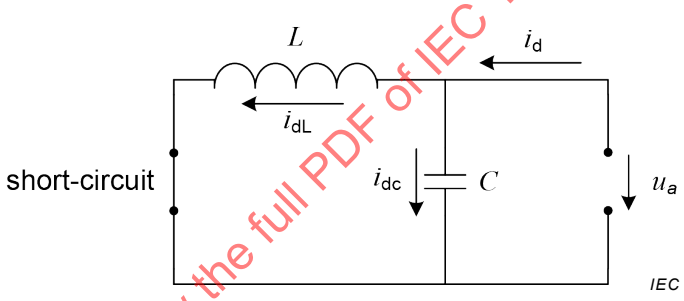
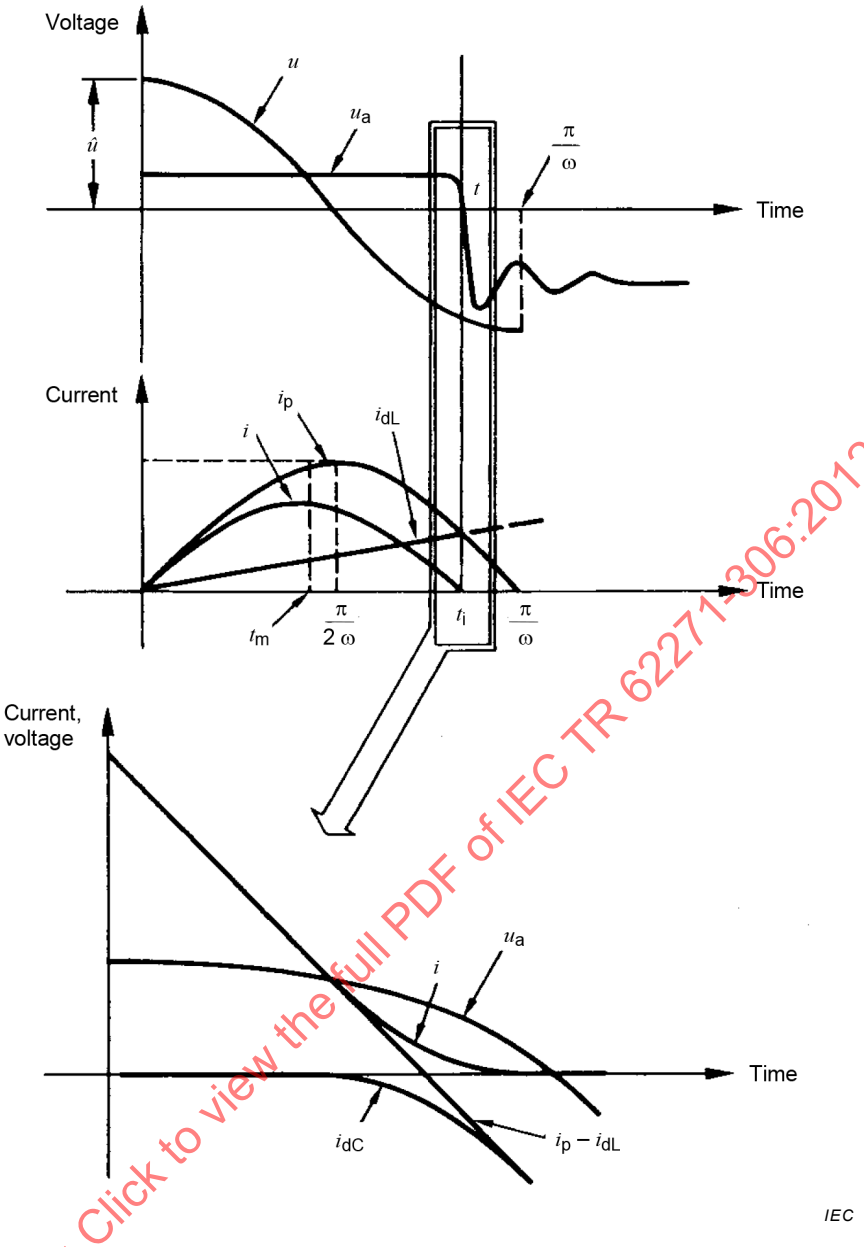


Figure 154 – Distortion current flow

Key to Figure 152, **Figure 153** and **Figure 154**

u	voltage supplying the direct circuit	C	capacitance of the full power direct circuit, together with L controlling the transient recovery-voltage of the circuit
u_a	arc voltage of circuit-breaker	S_t	circuit-breaker
L	inductance of the full power direct circuit, together with C controlling the short-circuit current	i	actual current
i_p	prospective short-circuit current	i_{dL}	distortion current through L
i_{dc}	distortion current through C	i_d	total distortion current



Key

u	voltage supplying the direct circuit	i_{dC}	distortion current through C
u_a	arc voltage of circuit-breaker	i	actual current
i_p	prospective short-circuit current	i_{dL}	distortion current through L
t_m	instant of peak value	t_i	duration of the actual current loop

Figure 155 – Distortion current

14.5.3 Current distortion during the high-current interval

14.5.3.1 General

During this interval, the arc voltage generates a distortion current i_d, in the circuit. i_d is superimposed on the total current.

By comparison with the prospective current, the resulting arc current exhibits distortion in four physical aspects: current amplitude, loop duration, arc-energy and di/dt.

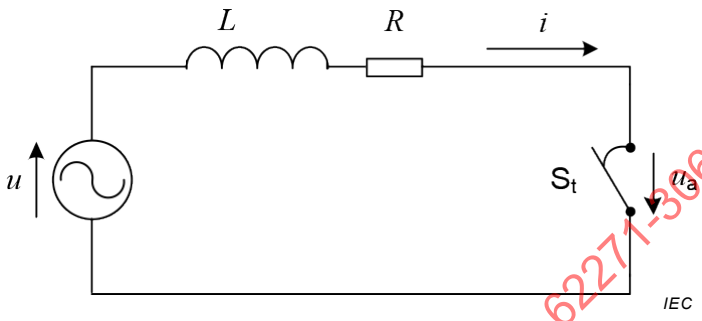
To evaluate the influence of the arc voltage, it is sufficient, in practice, to consider the current amplitude and the loop duration.

As a first approximation, two different arc voltage characteristics can be considered, namely:

a) a constant arc voltage $u_a = U_a$;

b) a linearly rising arc voltage $u_a = S \times t$, where S is the linear rate-of-rise of the arc voltage.

Since the current through the capacitor C (see Figure 152) will be small during this period of arcing, the simplified diagram of Figure 156 is adequate.



Key

u	voltage supplying the direct circuit	R	resistance of the direct circuit
u_a	arc voltage of circuit-breaker	i	actual current
L	inductance of the full power direct circuit, together with u controlling the short-circuit current		

Figure 156 – Simplified circuit diagram for high-current interval

14.5.3.2 Distortion during one loop of arcing related to a symmetrical current

The following equations are derived, where the resistance in Figure 156 is neglected since the effect of this during the single loop is negligible. Some results are given in Figure 157 and Figure 158.

Calculations are made based on the characteristics shown in Figure 157 and Figure 158.

$\hat{u} = \omega L \times \hat{i}_p$ peak value of voltage of current circuit

$\hat{i}_p$ peak value of prospective current

$\hat{i}$ peak value of actual current (reduced by arc voltage)

t_m instant of peak value $\hat{i}$

a) *Ratio of current amplitudes*

– for constant arc voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin(\omega \times t_m) - \frac{U_a}{\hat{u}} \times \omega\, t_m$$

– for linearly rising arc voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin(\omega \times t_m) - \frac{S\omega}{2\,\hat{u}} t_m^2$$

b) *Actual current loop duration* T_1 (reduced by arc voltage)

– for constant arc voltage

$$\sin(\omega T)_1 = \frac{U_a\,\omega}{\hat{u}}\,T_1$$

– for linearly rising arc voltage:

$$\sin(\omega T)_1 = \frac{S\omega}{2\,\hat{u}}\,T_1^2$$

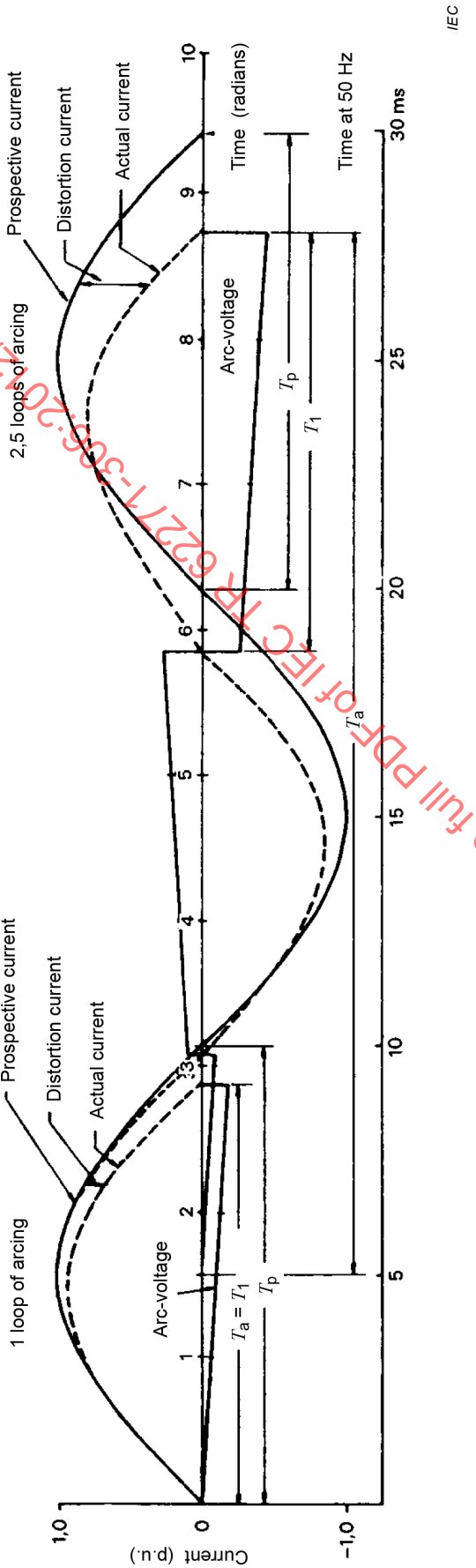
In Figure 159 and Figure 160, the relative reduction of current amplitude $\Delta i/\hat{\imath}_p$ and current loop duration $\Delta t/T_p$ are given as a function of ratio $U_a/\hat{u}$ for a constant arc voltage and of ratio $S\times T_a/2\times\hat{u}$ for a linearly rising arc voltage, respectively, where:

$\Delta i = \hat{\imath}_p - \hat{\imath}$,

$\Delta t = T_p - T_1$

T_p = prospective current loop duration

T_a = actual arcing time ($T_a = T_1$ for one loop of arcing, see Figure 157 and Figure 158).



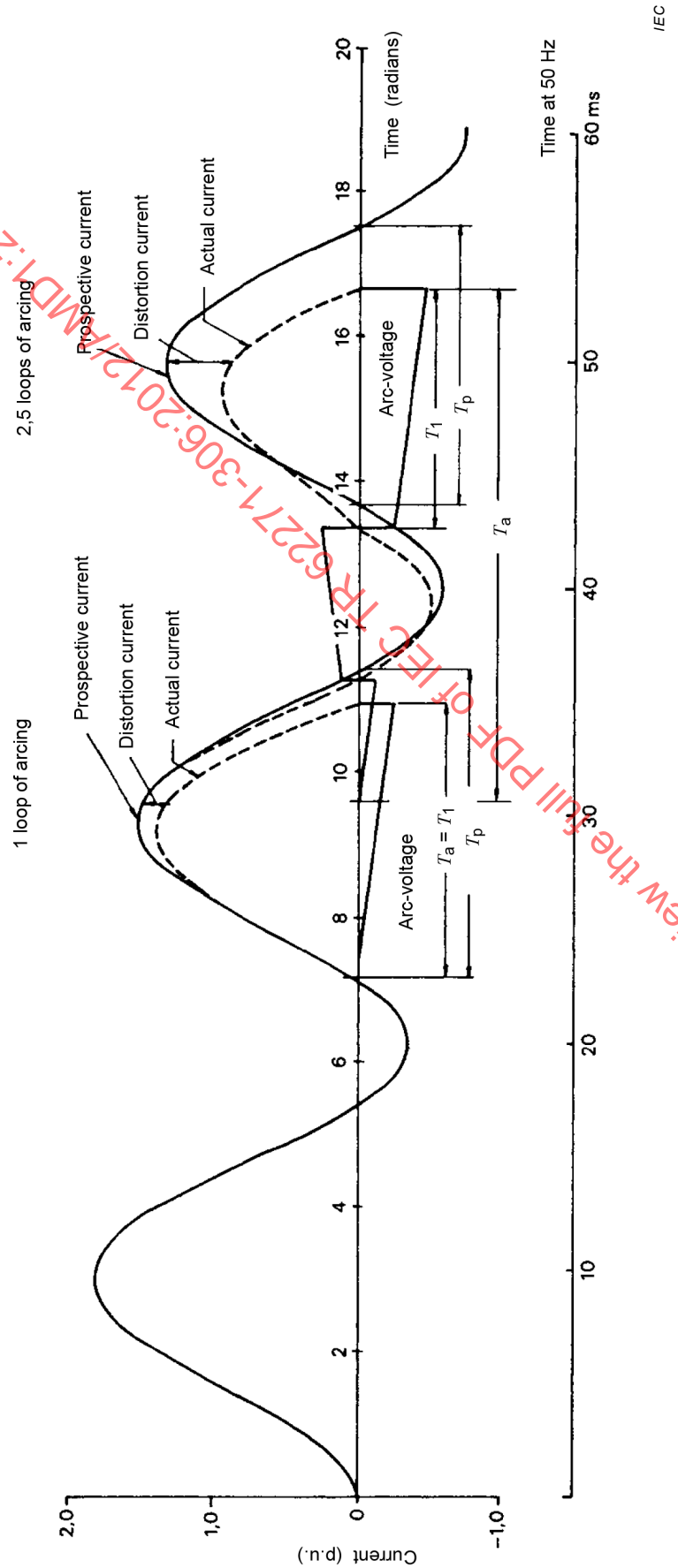
Key

T_a actual arcing time

T_p loop duration of the prospective current

T_1 loop duration of the actual current

Figure 157 – Current and arc voltage characteristics for symmetrical current and constant arc voltage



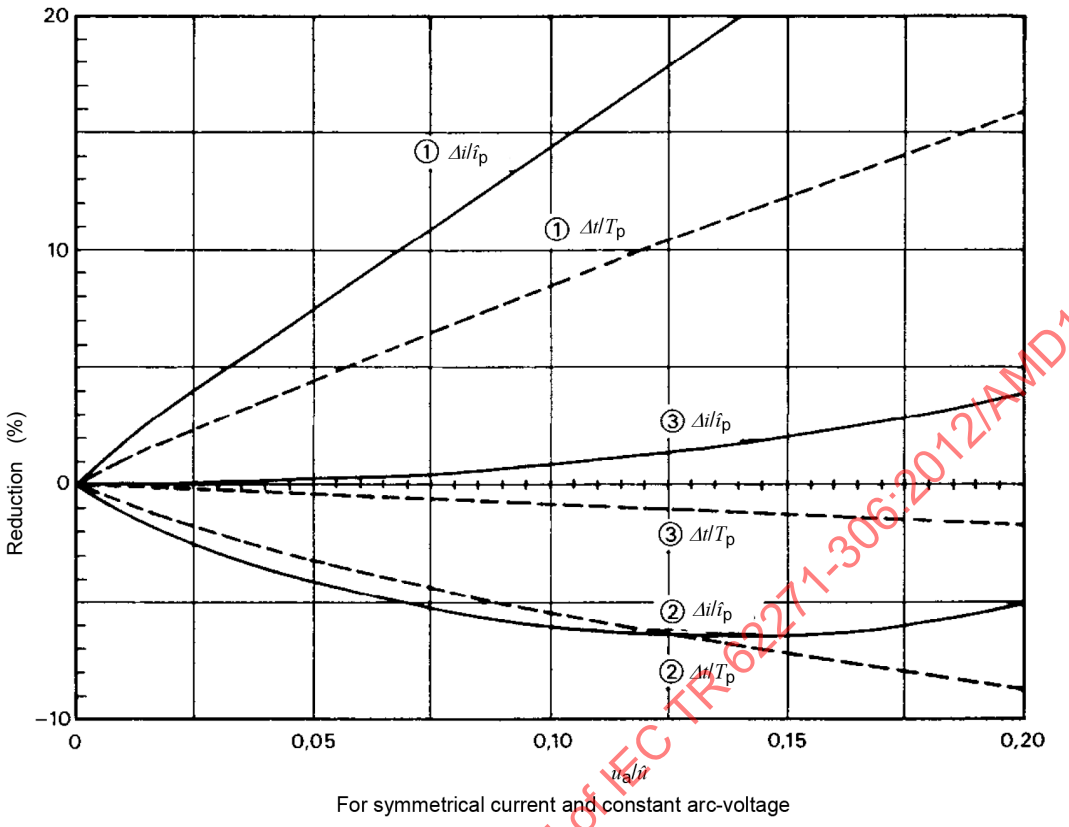
Key

T_a actual arcing time

T_p loop duration of the prospective current

T_1 loop duration of the actual current

Figure 158 – Current and arc voltage characteristics for asymmetrical current and constant arc voltage



① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 157.

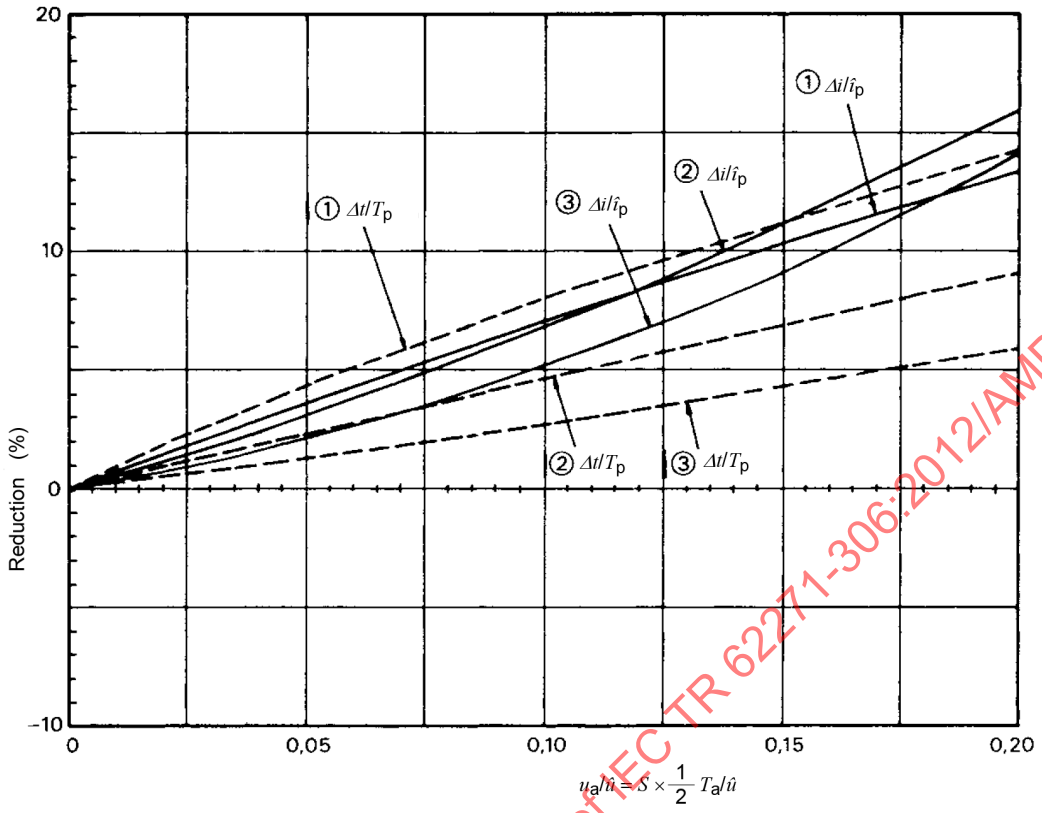
Key

$\Delta i/\hat{i}_p$ relative reduction of current amplitude

$\Delta t/T_p$ relative reduction of duration of current loop

$u_a/\hat{u}$ ratio of arc voltage to supply voltage

Figure 159 – Reduction of amplitude and duration of final current loop of arcing for symmetrical current and constant arc voltage



For symmetrical current and linearly rising arc-voltage

① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 157.

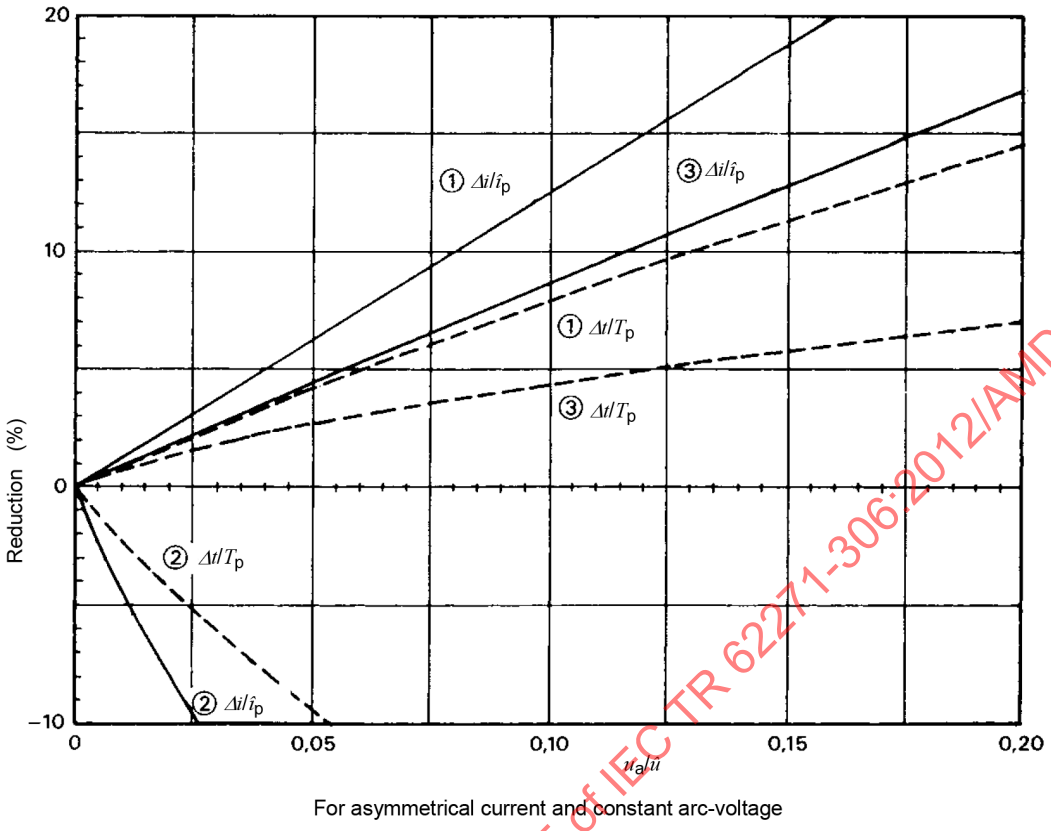
Key

$\Delta i/\hat{i}_p$ relative reduction of current amplitude

$\Delta t/T_p$ relative reduction of duration of current loop

$u_a/\hat{u}$ ratio of arc voltage to supply voltage

Figure 160 – Reduction of amplitude and duration of final current loop of arcing for symmetrical current and linearly rising arc voltage



① 1 loop of arcing

② 2 loops of arcing

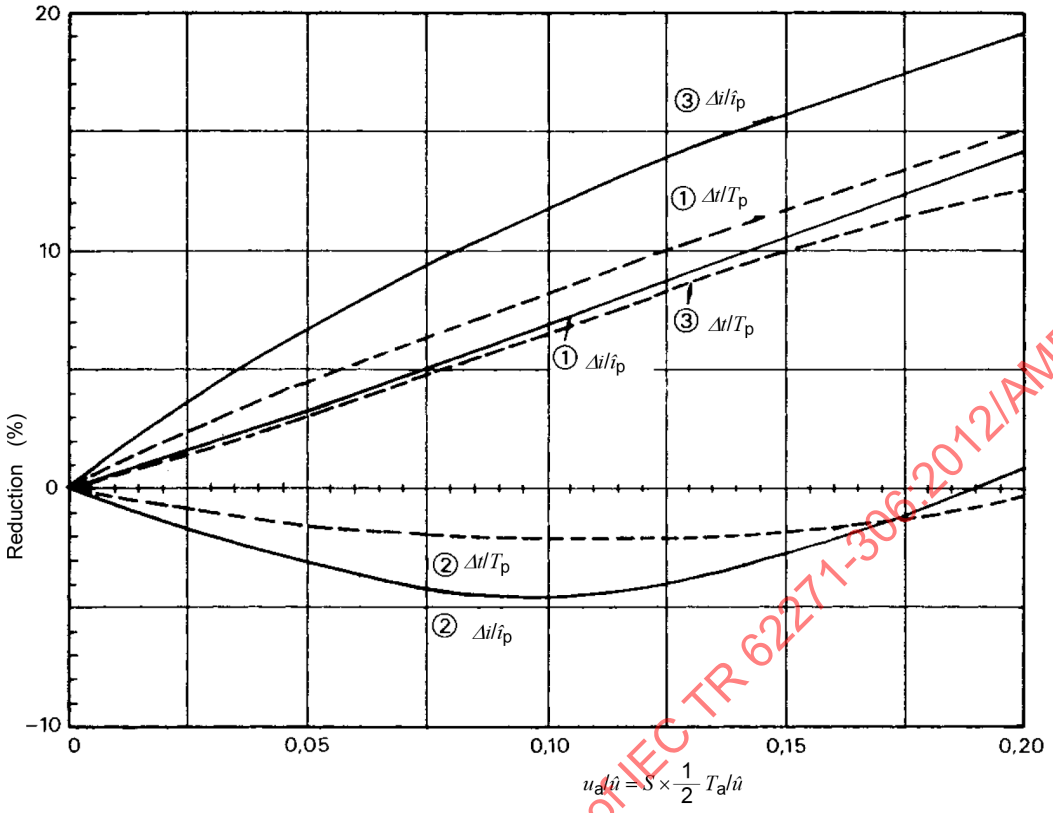
③ 2,5 loops of arcing

See Figure 158.

Key

$\Delta i/\hat{i}_p$	relative reduction of current amplitude	$u_a/\hat{u}$	ratio of arc voltage to supply voltage
$\Delta t/T_p$	relative reduction of duration of current loop		

Figure 161 – Reduction of amplitude and duration of final current loop of arcing for asymmetrical current and constant arc voltage



① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 158.

Key

$\Delta i/\hat{i}_p$	relative reduction of current amplitude	$u_a/\hat{u}$	ratio of arc voltage to supply voltage
$\Delta t/T_p$	relative reduction of duration of current loop		

Figure 162 – Reduction of amplitude and duration of final current loop of arcing for asymmetrical current and linearly rising arc voltage

14.5.3.3 Distortion in general case

The distortion currents in the case of both symmetrical and asymmetrical currents including more than one loop of arcing are obtained by the following equations which are applicable for the case of constant and linearly rising arc voltages. These calculations are based on a circuit as in Figure 156 where the L/R time constant of the supply impedance is introduced. The p.u. prospective current is given by:

$$i_p/\hat{i}_p = \sin(\omega t + \omega t_1 - \varphi) - \sin(\omega t_1 - \varphi) \times e^{-\frac{R}{L}t}$$

where

t is the time coordinate counting from the instant of current initiation;

t_1 is the time interval between the beginning of the positive voltage loop and current initiation;

φ is the arctan $\frac{\omega L}{R}$ for symmetrical current $\varphi = \omega t_1$.

The per unit distortion currents are

$i_d/\hat{i}_p = C$ for the first loop of arcing,
$i_d/\hat{i}_p = D - E$ for the second loop of arcing,
$i_d/\hat{i}_p = D - F + G$ for the third loop of arcing,

where C, D, E, F and G are defined as follows:

a) *for constant arc voltage*:

$$C = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t_{cs})}\right]$$

$$D = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t'_0 - t_{cs})}\right] e^{-\frac{R}{L}(t - t'_0)}$$

$$E = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t'_0)}\right]$$

$$F = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t''_0 - t'_0)}\right] e^{-\frac{R}{L}(t - t''_0)}$$

$$G = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t''_0)}\right]$$

where

$M = \frac{U_a}{\hat{u}}$ = the ratio between the arc voltage and the peak value of the power-frequency voltage

$$\cos\varphi = \frac{R}{\sqrt{R^2 + (\omega L)^2}}$$

where

t_{cs} is the instant of contact separation

t_0', t_0'' is the instants at the end of each current loop

b) *for linearly rising arc voltage:*

$$C = \frac{M}{\cos\varphi}\left[(t - t_{cs}) - \frac{L}{R}(1 - e^{-\frac{R}{L}(t - t_{cs})})\right]$$

$$D = \frac{M}{\cos\varphi}\left[(t'_0 - t_{cs}) - \frac{L}{R}(1 - e^{-\frac{R}{L}(t'_0 - t_{cs})})\right] e^{-\frac{R}{L}(t - t'_0)}$$

$$E = \frac{M}{\cos\varphi}\left[(t - t'_0) - \frac{L}{R}(1 - e^{-\frac{R}{L}(t - t'_0)}) + (t'_0 - t_{cs}) \times (1 - e^{-\frac{R}{L}(t - t'_0)})\right]$$

$$F = \frac{M}{\cos\varphi}\left[(t''_0 - t'_0) - \frac{L}{R}(1 - e^{-\frac{R}{L}(t''_0 - t'_0)}) + (t'_0 - t_{cs}) \times (1 - e^{-\frac{R}{L}(t''_0 - t'_0)})\right] e^{-\frac{R}{L}(t - t''_0)}$$

$$G = \frac{M}{\cos\varphi}\left[(t - t_0'') - \frac{L}{R}(1 - e^{-\frac{R}{L}(t - t_0'')}) + (t_0'' - t_{cs}) \times (1 - e^{-\frac{R}{L}(t - t_0'')})\right]$$

where

$$M = \frac{S \times T_a}{2\,\hat{u}}$$

Relative reductions of current amplitudes and loop durations related to the last arcing loop for some typical cases are given in Figure 159 to Figure 162.

For symmetrical current, values are given for constant arc voltage as a function of ratio $U_a/\hat{u}$ in Figure 159 and for linearly rising arc voltage as a function of the ratio $S \times T_a/2\hat{u}$ in Figure 160. For asymmetrical current, the corresponding results are given in Figure 161 and Figure 162.

For arcing times, three typical values, i.e. for 1, 2 and 2,5 loops, are introduced. In the case of asymmetrical current contact parting positions have been selected starting about 1,5 cycles after current initiation.

The modifying of arc voltage is much dependent on not only arc voltage but also arcing time and current asymmetry, therefore an exact evaluation for each case is necessary.

NOTE In order to be able to compare the curves relevant to either type of arcing, suitable values have been chosen for the arc voltages: the value at the last current zero for linearly rising arc voltage is twice the value U_a for the constant arc voltage.

14.5.4 Examples of estimation of the parameters of the distorted current

14.5.4.1 General

In the following, some examples of application of the methods of evaluation of the distorted current shown in 14.5.2 and 14.5.3 are given for the single pole test of a 123 kV circuit-breaker.

For the synthetic test examples, equal arc voltages and contact parting positions of both the test and the auxiliary circuit-breaker are assumed.

14.5.4.2 Symmetrical current test

14.5.4.2.1 Constant arc voltage

Direct test

Rated voltage U_r = 123 kV

Single pole test voltage $U_t = \frac{123 \times 1{,}3}{\sqrt{3}} = 92\,\text{kV}$

Mean value of constant arc voltage (last loop) U_a = 1 kV

Therefore: $\frac{U_a}{\hat{u}} = \frac{1}{92 \times \sqrt{2}} = 0{,}007\,7$

by calculation for one loop of arcing (see 14.5.3): $\frac{\Delta i}{\hat{i}_p} = -1{,}2\,\%$

and $\frac{\Delta t}{T_p} = -0{,}7\ \%$

Synthetic test

Current circuit voltage U_1 = 31 kV

Mean value of constant arc voltage (test and auxiliary circuit-breaker, last loop) $U_{as} = 2U_a$ = 2 kV

therefore: $\frac{U_{as}}{\hat{u}} = \frac{2}{31 \times \sqrt{2}} = 0{,}046$

from Figure 159 for one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -7\ \%$

and: $\frac{\Delta t}{T_p} = -4{,}5\ \%$

14.5.4.2.2 Linearly rising arc voltage

Direct test

Single pole test voltage U_t = 92 kV as above

Linearly rising arc voltage $\frac{S \times T_a}{2} = 3\ \text{kV}$

therefore: $\frac{S \times T_a}{2\hat{u}} = \frac{3}{92\sqrt{2}} = 0{,}023$

from Figure 160 for one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -1{,}7\ \%$

and $\frac{\Delta t}{T_p} = -2{,}2\ \%$

Synthetic test

Current circuit voltage U_1 = 31 kV as above

Linearly rising arc voltage (test and auxiliary circuit-breaker) $\frac{S \times T_a}{2} = 2 \times 3 = 6\ \text{kV}$

therefore: $\frac{S \times T_a}{2\hat{u}} = \frac{6}{31\sqrt{2}} = 0{,}137$

from Figure 160 for one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -10\ \%$

and $\frac{\Delta t}{T_p} = -11{,}2\ \%$

In the first example, the tolerances on the amplitude and the duration of the power-frequency current loop, in accordance with 4.1 of IEC 62271-101:2012, should not be exceeded during

the actual synthetic test. This depends, however, on the decrement of the AC component of the current being negligible.

In the second example, the current circuit voltage has to be increased or other measures as described in 4.1 of IEC 62271-101:2012 have to be taken because the tolerance on the loop duration is exceeded. Whilst tolerance on the current amplitude is apparently not exceeded, it might be exceeded in practice where there is likely to be some decrement of the AC component of the prospective current.

14.5.5 Asymmetrical current test

If the arc voltage is approximately constant or linearly rising, the curves in Figure 161 and Figure 162 can be used. The method of evaluation is similar to the one outlined for the symmetrical case. For example in case of constant arc voltage:

Direct test

Single pole test voltage $U_t = \frac{123 \times 1{,}3}{\sqrt{3}} = 92\,\text{kV}$ (as above)

Constant arc voltage U_a = 1 kV

therefore: $\frac{U_a}{\hat{u}} = \frac{1}{92 \times \sqrt{2}} = 0{,}0077$

for contact parting at around 1,5 cycles after current initiation and one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -1\%$

and: $\frac{\Delta t}{T_p} = -0{,}6\,\%$ (Figure 161)

Synthetic test

Current circuit voltage U_1 = 14,2 kV

Constant arc voltage (test and auxiliary circuit-breakers) U_a = 2 kV

therefore: $\frac{U_a}{\hat{u}} = \frac{2}{14{,}2 \times \sqrt{2}} = 0{,}10$

for the same situation as above: $\frac{\Delta i}{\hat{i}_p} = -12{,}6\,\%$

and $\frac{\Delta t}{T_p} = -8{,}0\,\%$ (Figure 161)

The actual arc voltage may not follow one of the simplified characteristics. In such a case, the current reduction during the synthetic test can be measured from actual oscillograms or calculated. The actual current of the direct test that is required to establish the synthetic test driving voltage can only be calculated.

For circuit-breakers having relatively low arc voltage (e.g. u_a = 2 % U_1), the modifying effect of the arc voltage on the current in the system or in the direct circuit is negligible. Therefore the specified prospective current is assumed as reference current.

NOTE If the opening of the auxiliary circuit-breaker is delayed in relation to the opening of the test circuit-breaker, or if an auxiliary circuit-breaker with a lower arc voltage is used, then its influence on the breaking current will be smaller than that of the test circuit-breaker.

14.6 Step-by-step method to prolong arcing

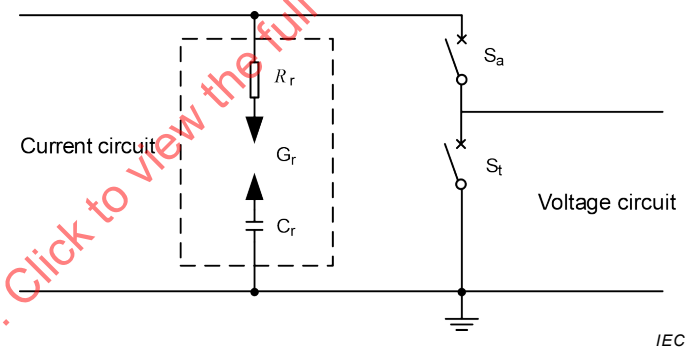
With this method, only one voltage source is used. The test circuit-breaker is artificially re-ignited by a special re-ignition circuit, or other means, in order to prolong arcing up to the current zero at which the voltage source is to be applied.

a) Method with a separate re-ignition circuit

A separate re-ignition circuit provides a rapidly rising pulse of current, of opposite polarity to that of the power-frequency current, approximately 10 µs before current zero. The current through the circuit-breaker is thus rapidly reversed and conduction in the arc gap is maintained for a further loop of power-frequency current. As an example, a re-ignition circuit is indicated in Figure 163. The corresponding current and voltage for a symmetrical current breaking tests is shown in Figure 164. Several such circuits may be used for prolonging the arcing through several loops of current. The re-ignition circuit can in principle be applied to re-ignite both test and auxiliary circuit-breaker. However, the need to re-ignite both circuit-breakers is usually avoided by suitably delaying the separation of the auxiliary circuit-breaker contacts.

b) Method with increased power-frequency circuit severity

In some cases, the arcing of the test circuit-breaker may be prolonged by increasing the rate-of-rise of the transient recovery voltage in the power-frequency current circuit. Whether this is effective or not depends upon the characteristics of the power-frequency current circuit and of the circuit-breaker under test.



Key

S_t	test circuit-breaker	C_r	capacitor for re-ignition circuit
S_a	auxiliary circuit-breaker	G_r	spark gap for closing re-ignition circuit
R	resistor for re-ignition circuit		

Figure 163 – Typical re-ignition circuit diagram for prolonging arc-duration

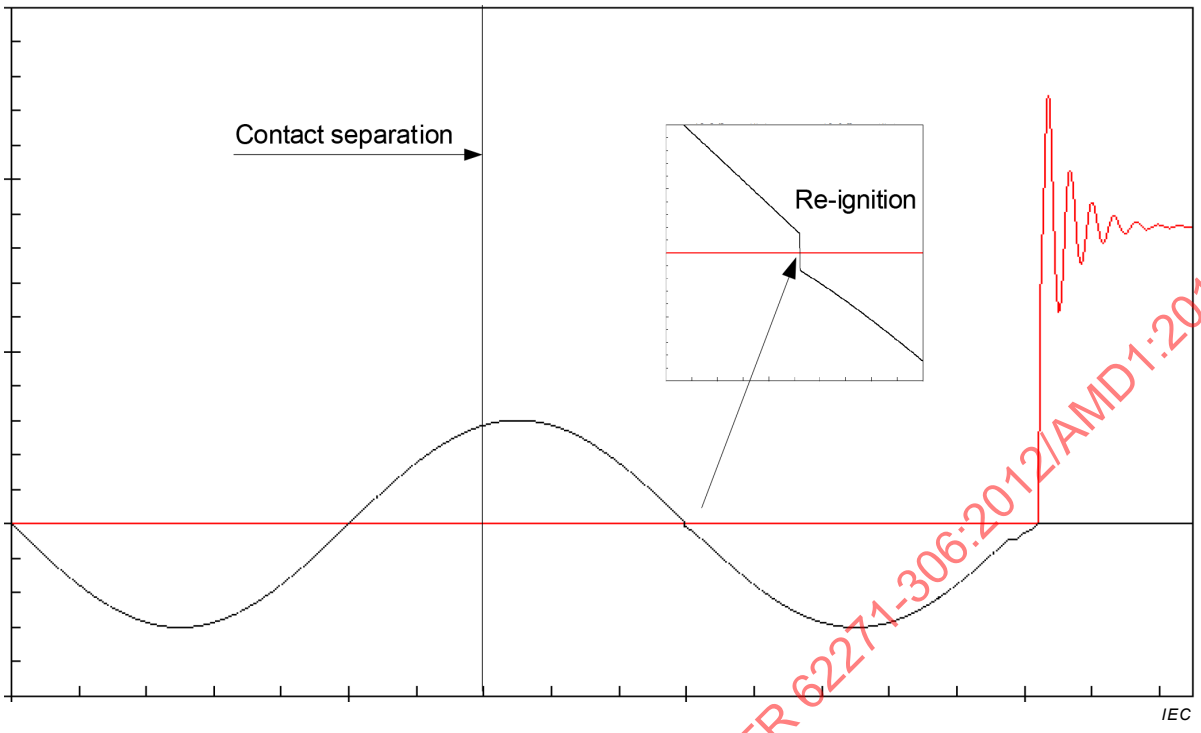


Figure 164 – Typical waveshapes obtained during a symmetrical test using the circuit in Figure 163

14.7 Examples of the application of the tolerances on the last current loop based on 4.1.2 and 6.109 of IEC 62271-101:2012

A few examples are given to show how the tolerances given in Annex B of IEC 62271-100:2008 are applied to the last current loop of test-duties T60, T100a and L90.

– T60, with a short-circuit rated current of 40 kA, with a rated frequency of 50 Hz:

  1) Final loop minimum amplitude: 0,9 × 0,6 × 40 × √2 = 30,5 kA;

  2) Final loop minimum duration: 0,9 × 10 = 9 ms.

– T100a, with a short-circuit rated current of 40 kA, with a rated frequency of 50 Hz, k_{pp} = 1,5, time constant of 45 ms, minimum clearing time between 27 ms and 47,5 ms, first-pole-to-clear:

  1) Final loop minimum amplitude: 0,9 × 1,33 × 40 × √2 = 67,7 kA;

  2) Final loop maximum amplitude: 1,1 × 1,33 × 40 × √2 = 82,8 kA;

  3) Final loop minimum duration: 0,9 × 12,2 = 11 ms;

  4) Final loop maximum duration: 1,1 × 12,2 = 13,4 ms.

– L90, with a short-circuit rated current of 40 kA, with a rated frequency of 50 Hz:

  1) Minimum value of (Final loop amplitude) × (final loop duration): 0,95 × (0,9 × 40 × √2) × 10 = 483,7 As;

  2) Final loop minimum amplitude: 0,95 × 0,9 × 40 × √2 = 48,4 kA;

  3) Final loop maximum amplitude: 1,1 × 0,9 × 40 × √2 = 56 kA;

  4) Final loop minimum duration: 0,9 × 10 = 9 ms.

There are no additional tolerances that can be applied.

Add, at the end of the existing 15.6, the following new subclauses:

15.7 Corrosion: Information regarding service conditions and recommended test requirements

15.7.1 General

The minimum requirement for switchgear and controlgear with regard to corrosion is that the function of the equipment should not be affected during the service life by corrosion under the conditions specified by the user. All bolted or screwed parts of the main circuit and of the enclosure should remain easy to disassemble, as applicable. In particular, galvanic corrosion of materials in contact should be considered because, for example, it may lead to the loss of tightness or increased contact resistance.

Corrosion might not only occur due to oxidizing gases, but also due to material incompatibility. An example is a connection made between bare aluminium or an aluminium alloy part and a silver coated part of the main circuit. Reference is made to [143] in the bibliography.

Due to the many variables involved, for example, design of equipment, service conditions, user maintenance practices, and the expected life of the equipment; standardized requirements and verification testing is left to agreement between the user and the manufacturer. In either case, however, the following guidelines should be followed.

Corrosion stresses are strongly dependant on the installation. The atmospheric conditions are important, but the installation should consider the solar and temperature variation, the air flow, etc.

NOTE When a surface becomes and remains wet, the two main factors involved in atmospheric corrosion are sodium chloride, mainly in marine environments, and sulphur dioxide, mainly in industrial environments. Occasionally, both of these factors apply at the same time.

15.7.2 Recommendation for minimum requirements

The basic function of switchgear and controlgear to be considered should include, but not be limited to, the following:

– the ability to withstand normal system voltage and carry rated continuous current;
– the continuity of earthing circuits;
– the ability to access or disassemble equipment as required to perform routine inspection and maintenance;
– the ability to provide minimum security against unauthorized access;
– the ability to provide for the safety of the user or the public as appropriate.

15.7.3 Recommended test requirements

The tests and test methods are related to the material used in the equipment and are recommended when required by the relevant equipment standard or by agreement between the user and the manufacturer.

Specific corrosion and humidity tests should be performed according to the relevant IEC standard, reference is made to IEC 60068-1 [132].

15.8 Electromagnetic compatibility on site

EMC site measurements are not type tests but may be performed in special situations:

– where it is deemed necessary to verify that actual stresses are covered by the EMC severity class of the auxiliary and control circuits, or

– in order to evaluate the electromagnetic environment, in order to apply proper mitigation methods, if necessary,

– to record the electromagnetically induced voltages in auxiliary and control circuits, due to switching operations both in the main circuit and in the auxiliary and control circuits. It is not considered necessary to test all auxiliary and control circuits in a substation under consideration. A typical configuration should be chosen.

Measurement of the induced voltages should be made at representative ports in the interface between the auxiliary and control circuits and the surrounding network, for example, at the input terminals of control cubicles, without disconnection of the system. The extension of the auxiliary and control circuits is described in 5.19 of IEC 62271-1:2007. Instrumentation for recording induced voltages should be connected as outlined in IEC 60816 [133].

Switching operations should be carried out at normal operating voltage, both in the main circuit and in the auxiliary and control circuits. Induced voltages will vary statistically and thus a representative number of both making and breaking operations should be chosen, with random operating instants.

The switching operations in the main circuit are to be made under no-load conditions. The tests will thus include the switching of parts of the substation but no switching of load currents and no fault currents.

The making operations in the main circuit should be performed with trapped charge on the load side corresponding to normal operating voltage. This condition may be difficult to obtain at testing, and, as an alternative, the test procedure may be as follows:

– discharge the load side before the making operation, to assure that the trapped charge is zero;

– multiply recorded voltage values at the making operation by 2, in order to simulate the case with trapped charge on the load side.

The switching device in the primary system should be operated at rated pressure and auxiliary voltage.

NOTE 1 The most severe cases, with regard to induced voltages, will normally occur when only a small part of a substation is switched.

NOTE 2 The most severe electromagnetic disturbances are expected to occur at disconnector switching, especially for GIS installations.

The recorded or calculated peak value of induced common-mode voltage, due to switching in the main circuit, should not exceed 1,6 kV for interfaces of the auxiliary and control circuits.

The note to 5.19 of IEC 62271-1:2007 gives guidelines for improvement of electromagnetic compatibility.

16.2.2 Chopping overvoltages

Replace the existing Equation (99) by the following new equation:

$$k_a = \sqrt{(k_{in} + 0{,}5)^2 + \left(\frac{i_c}{U_0}\right)^2 \frac{1{,}5L}{C}} - 0{,}5$$

Replace the existing Equation (102) by the following new equation:

$$k_a = \sqrt{(k_{in} + \kappa)^2 + NL(1+\kappa)\left(\frac{\lambda}{U_0}\right)^2 \left(\frac{C_P}{C_L} + 1\right)} - \kappa$$

Replace the existing Equation (103) by the following new equation:

$$k_a = \sqrt{\left(k_{in} + \kappa\right)^2 + \frac{1{,}5\, N\lambda^2 \left(1+\kappa\right)}{\omega Q}\left(\frac{C_P}{C_L}+1\right)} - \kappa$$

Replace the existing Equation (104) by the following new equation:

$$k_a = \sqrt{{k_{in}}^2 + \frac{1{,}5 N\lambda^2}{\omega Q}\left(\frac{C_P}{C_L}+1\right)}$$

16.2.6.3 Circuit-breaker selection

Replace the last sentence before item a) by the following new sentence:

From Equation (105) the second term under the root sign will be negligible and k_a can be taken as equal to k_{in}.

Delete the existing items a) to g).

16.2.7 Testing

Replace the last paragraph of this subclause by the following:

The individual test circuits and TRV parameters for all possible system and shunt reactor application and earthing conditions are given in 6.114 of IEC 62271-110:2012.

16.4 Unloaded transformer switching

Replace the existing content of this subclause by the following new content:

16.4.1 General

Unloaded transformer switching is an insignificant duty for circuit-breakers. The current to be interrupted is magnetizing current in the order of a few A at most and the associated transient recovery voltage is minimal as discussed below.

Owing to the enormous variations in transformer ratings and the non-linear behaviour of the core, it is not possible to model the switching of no-load transformers using linear components in a test laboratory. A test on an available transformer would only be valid for that transformer at the particular level of excitation used and would not be representative for other excitation levels on the same transformer, and certainly not for other transformers.

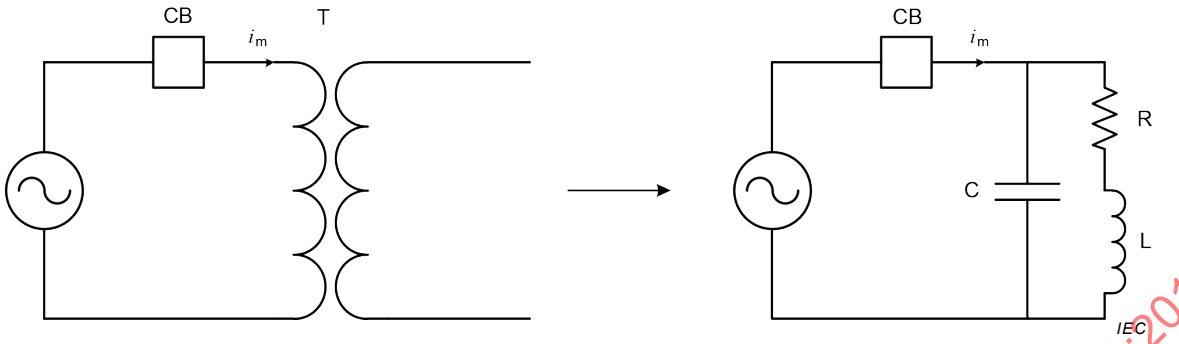
In summary, type testing for no-load transformers is not required for two reasons:

– the duty is less severe than any other switching duty;
– the duty cannot be correctly modelled in a test laboratory.

16.4.2 Transient recovery voltage calculation

Transformers can be oil-filled, dry-type or SF_6 gas filled. The basis for calculation of the transient recovery voltage for the unloaded switching case follows.

Circuit representation for unloaded transformer switching is shown in Figure 165.



Key

i_m	magnetising current
CB	circuit-breaker
T	transformer
R, L, C	equivalent circuit of the transformer

Figure 165 – Unloaded transformer switching circuit representation

The transformer can be represented as a source-free series RLC circuit. At current interruption, a voltage U remains on the capacitor, which then rings down to zero. The associated oscillation is underdamped with an amplitude factor usually not exceeding 1,3 p.u. at a frequency of a few hundred Hz as illustrated in Figure 166. The transient recovery voltage seen by the circuit-breaker is thus the difference between the source and transformer voltages and tends to be dominated by the former voltage due to the relative peaks not necessarily coinciding.

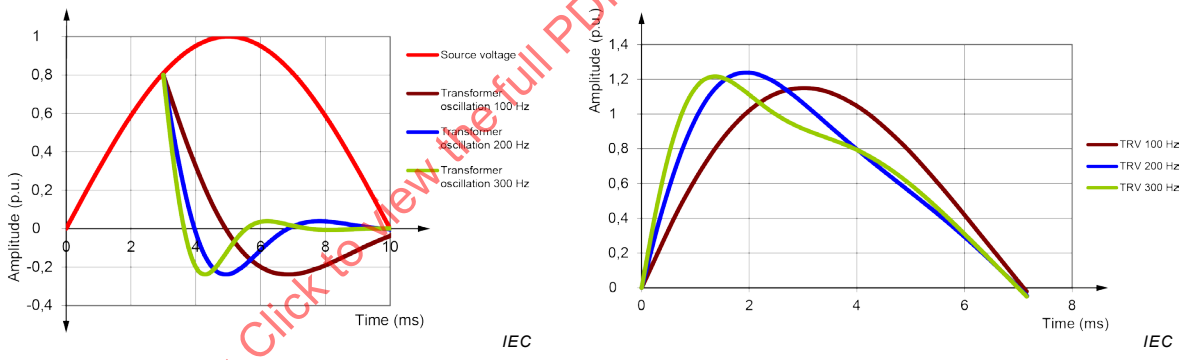


Figure 166 – Transformer side oscillation (left) and circuit-breaker transient recovery voltage (right)

The transformer side oscillation is described by the equation:

$$\upsilon = Ue^{-d_s t_g}\left(\cos\sqrt{1-d_s^2}\ t_g + \frac{d_s}{\sqrt{1-d_s^2}}\sin\sqrt{1-d_s^2}\ t_g\right) \quad (192)$$

where U is the initial voltage, d_s is the degree of damping in the circuit given by $d_s = R\Big/2\sqrt{\frac{L}{C}}$ and t_g is generic time in radians given by $t_g = t/\sqrt{LC}$, t being real time in s [134].

The parameters for the RLC circuit transformer representation can be approximated from the factory core loss measurements (R and L) and impulse voltage tests (C). The core losses P_o are given by:

$$P_o = U_o I_o \cos\phi \tag{193}$$

where P_o is in W, U_o is the r.m.s. applied voltage in V and I_o is the r.m.s. value of the magnetizing current in A. All three quantities being known, we can write

$$\cos\phi = \frac{P_o}{U_o I_o} \tag{194}$$

and

$$Z = R + j\omega L = \frac{U_o}{I_o}(\cos\phi + j\sin\phi) \tag{195}$$

giving

$$R = \frac{U_o}{I_o}\cos\phi \text{ and } L = \frac{U_o}{\omega I_o}\sin\phi \tag{196}$$

The value of C is calculated from the lightning impulse test wave shape time to peak T:

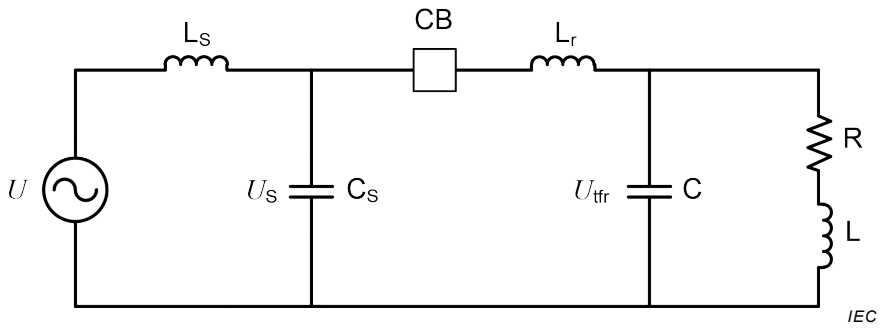
$$T = 2{,}5 \times R_s C_T \tag{197}$$

where R_s is the series resistance in the lightning impulse test circuit and C_T is the total load capacitance including any external front capacitors. If no front capacitors are used, $C_T = C$. As an alternative, the value of C may also be estimated from transformer winding dissipation factor measurements.

The frequency of the transformer side oscillation is given by:

$$f_{tfr} = \frac{1}{2\pi\sqrt{LC}} \tag{198}$$

When an unloaded transformer is de-energised by a circuit-breaker on the high-voltage side, it is very unlikely that any re-ignitions will occur. The re-ignition circuit loop involves the source side capacitance C_s, C and the combined inductance of the circuit-breaker, buswork and earth connections as shown in Figure 167.



Key

U	System voltage	CB	Circuit-breaker
L_s	Short-circuit inductance	L_r	Bus inductance
U_s	Source voltage	U_{tfr}	Voltage across the transformer
C_s	Source capacitance	C, R, L	Equivalent circuit of the transformer

Figure 167 – Re-ignition loop circuit

Re-ignitions take place in two stages. The re-ignition occurs at a certain voltage difference $U_s - U_{tfr}$ across the circuit-breaker (Figure 167). Initially, the two voltages will equalize at a voltage U_e dependent on the ratio C_s/C and then is followed by a second voltage excursion as the equalization voltage adjusts to the source voltage by way of an overvoltage transient U_{ov}. The magnitude of this transient is given by:

$$U_{ov} = U_s + \beta\left(\frac{U_s - U_{tfr}}{1 + C_s/C}\right) \tag{199}$$

where β is the damping factor of value < 1.

In reality, the value of U_{ov} can approach 3 p.u. with respect to earth at a low frequency dependent on the source inductance L_s and the ratio C_S/C.

The transient that causes difficulties for transformers is the equalization transient. While not high in terms of magnitude, its frequency is high given by:

$$f_e = \frac{1}{2\pi\sqrt{L_r\left(\frac{C_S C}{C_S + C}\right)}} \tag{200}$$

This frequency may coincide with the frequency of a possible internal resonance circuit within the transformer which, if triggered, may result in failure of the transformer. IEEE Std. C57.142 [135] contains more information about the interaction of the circuit-breaker, transformer and system.

In systems at ≤ 52 kV the use of dry type transformers is common. Such transformers are often switched with vacuum circuit-breakers. This case has certain similarities to motor switching including the fact that there is usually a length of cable between the circuit-breaker and the transformer [136]. The transformers can be treated, as for both shunt reactors and motors, as a capacitance in parallel with an inductance. The effective capacitance is much lower than for oil-filled transformers and is in the order of 200 pF to 500 pF. The inductance is the magnetizing inductance of the transformer and the magnetizing currents are typically in

the range 1 % to 3 % of rated full load current. For example, a 13,8 kV, 5 MVA transformer with 3 % magnetizing current would have a natural frequency of 3,8 kHz (C = 500 pF, L = 3,52 H) assuming that the core losses are insignificant.

16.4.3 Overvoltages

Overvoltages are not an issue when switching out high-voltage transformers using SF_6 gas circuit-breakers. However, vacuum circuit-breakers are now used up to 145 kV but no information is available on how they perform in this regard. In any case, transformers are always protected by a surge arrester for other reasons.

Studies have shown that the overvoltage level on switching unloaded dry-type transformers is dependent on the length of cable between the circuit-breaker and the transformer [137]. The results indicate that the longer the cable the lower the overvoltage level, but the overvoltage level tends to increase with increasing MVA for constant cable length. The highest overvoltages occur on multiple re-ignitions and voltage escalation to as high as 3,5 p.u.; interruption of inrush current can result in overvoltages in excess of 5 p.u. [138].

16.4.4 Overvoltage limitation

Overvoltage limitation is considered by reference to that for motor switching as discussed in 16.3.5.

Surge arresters: studies indicate that surge arresters applied at the transformer terminals are effective in limiting overvoltages to earth for transformers.

Surge capacitors: surge capacitors have the effect of reducing the surge impedance of the load and thereby the overvoltage levels [137].

RC dampers: effectiveness similar to that described for motor switching applications, i.e. will prevent multiple re-ignitions in vacuum circuit-breakers [136].

ZnO-RC dampers: effectiveness similar to that described for motor switching. Whether such devices have been applied in this context is unknown.

16.4.5 Circuit-breaker specification and selection

In most cases, circuit-breakers rated at 52 kV and below are specified and selected according to requirements other than unloaded transformer switching. The reason for this is that the circuit-breakers are taken to inherently have this capability with due regard to possible overvoltage limitation.

Add, before the existing Annex A, the following new clause:

17 Information and technical requirements relevant for enquiries, tenders and orders

17.1 General

This clause provides a list of useful technical information items in a tabular form to be considered for possible exchange between user and supplier during contracting stage.

When in the table "supplier information" is mentioned, this means that only the supplier needs to deliver this information.

Attention should be paid to the fact that such table should be complemented with information and characteristics relevant for the type of switchgear and controlgear considered; see product standards.

17.2 Normal and special service conditions (refer to Clause 2 of IEC 62271-1:2007)

		User requirements	Supplier proposals
Service condition	Indoor or Outdoor		
Ambient air temperature: Minimum Maximum	 °C °C		
Solar radiation	W/m^2		
Altitude	m		
Pollution	Class		
Excessive dust or salt			
Ice coating	mm		
Wind	m/s		
Humidity	%		
Condensation or precipitation			
Vibration	Class		
Induced electromagnetic disturbance in auxiliary and control circuits	kV		

17.3 Ratings and other system parameters (refer to Clause 4 IEC 62271-1:2007)

		User requirements	Supplier proposals
Nominal voltage of system	kV		
Highest voltage of system	kV		
Rated voltage for equipment (U_r)	kV		
Rated insulation levels phase to earth and between phases Rated short-duration power-frequency withstand voltage (U_d) Rated switching impulse withstand voltage (U_s) – phase to earth – between phases Rated lightning impulse withstand voltage (U_p)	 kV kV kV kV kV		
Rated frequency (f_r)	Hz		
Rated continuous current (I_r)	A	According single line	
Rated short-time withstand current (I_k)	kA		
Rated peak withstand current (I_p)	kA		
Rated duration of short circuit (t_k)	s		
Rated supply voltage of closing and opening devices and of auxiliary and control circuits (U_a)	V		
Rated supply frequency of closing and opening devices and of auxiliary circuits	Hz	DC or 50 or 60	
Type of system neutral earthing		Effectively or non-effectively	

17.4 Design and construction (refer to Clause 5 of IEC 62271-1:2007)

As required by the relevant standards.

		User requirements	Supplier proposals
Number of phases	Three- or single-phase encapsulation		
Mass of the heaviest transport unit			
Mounting provisions			
Type of gas-pressure or liquid-pressure system			
Overall dimensions of the installation			
Description by name and category of the various compartments			
Rated filling level and minimum functional level			
Low- and high-pressure interlocking and monitoring devices			
Interlocking devices			
Degrees of protection			
Arrangement of the external connections			
Accessible sides			
Volume of liquid or mass of gas or liquid for the different compartments			
Facilities for transport and mounting			
Instructions for operation and maintenance			
Specification of gas or liquid condition			

17.5 Documentation for enquiries and tenders

		User requirements	Supplier proposals
Scope of supply (training, technical and layout studies and requirements for co-operating cycle with other parties)			
Single-line diagram			
General arrangement drawings of substation layout			
Provisions for transport and mounting to be given by the user			
Foundation loading		Supplier information	
Gas schematic diagrams		Supplier information	
List of type test reports		Supplier information	
List of recommended spare parts		Supplier information	

Annex A (informative) – Consideration of d.c. time constant of the rated short-circuit current in the application of high-voltage circuit-breakers

Replace the existing annex by the following new annex:

Annex A
(informative)

Consideration of DC time constant of the rated short-circuit current in the application of high-voltage circuit-breakers

A.1 General

A time constant of 45 ms is generally adequate on systems rated 800 kV and below. For 1 100 kV and 1 200 kV systems, the standardized DC time constant has been defined as 120 ms mainly because the use of multi-conductor bundles on transmission lines. Alternative special case DC time constants, related to the rated voltage of the circuit-breaker, should cover cases where the standard DC time constant 45 ms is not sufficient. This may apply, for example, to systems with very high rated voltage (for example 800 kV systems having higher DC time constant for lines e.g. when multi-conductor bundles are used), to some medium voltage systems with radial structure or to any systems with particular system structure or line characteristics. Alternative special case DC time constants have been defined in 4.101.2 of IEC 62271-100:2008/AMD2:2017 of taking into account the results of the survey by CIGRE WG13.04 [139].

The choice of a single special case value of the DC time constant minimises the number of tests required to demonstrate the capability of the equipment.

For example, a test carried out on a circuit-breaker at 63 kA with a DC time constant of 45 ms does not automatically cover the performance of a circuit-breaker having a rating of 50 kA with a DC time constant of 75 ms, actual test parameters should be known in order to determine if the equivalency can be made.

Some general important aspects need to be considered. In order to state the equivalency of a certain circuit-breaker for another fault current rating and DC time constant, the following parameters have to be examined carefully in relation to the interrupting technology used:

a) amplitude of the last current loop before interruption;

b) duration of the last current loop before interruption;

c) arcing time window;

d) arc energy;

e) di/dt at current interruption;

f) TRV peak voltage u_c and first reference voltage u_1, as applicable.

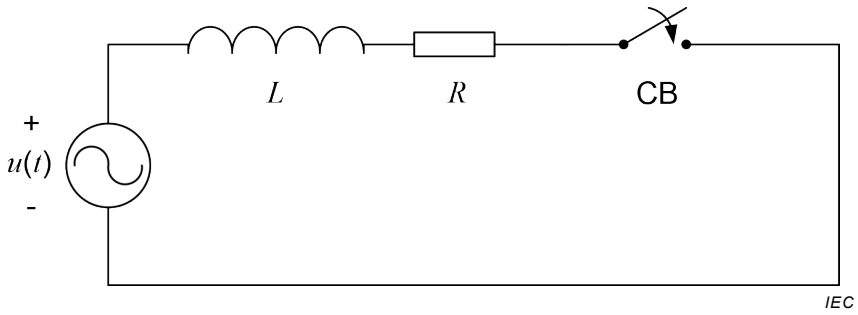
A.2 Basic theory

One of the duties that a circuit-breaker has to perform is to interrupt all short-circuit currents up to its rated short-circuit current. The short-circuit current may be symmetrical, partly asymmetrical or fully asymmetrical depending on the instant where the fault was initiated.

Asymmetrical currents occur in all type of inductive circuits and the level of asymmetry depends on the instant of fault initiation and the DC time constant (τ) of the circuit under evaluation.

NOTE The DC time constant of a circuit is sometimes expressed as the X/R ratio of a circuit, where $X = 2\pi f \times L$, where f is the power frequency in Hz and R represent the losses (Ω) in the circuit.

The simplified single-phase circuit shown in Figure A.1 illustrates the studied case.



Key

$u(t)$	Source voltage, $u(t) = U\sin(\omega t + \alpha)$	R	Losses in the circuit
L	Source inductance	CB	Circuit-breaker

Figure A.1 – Simplified single-phase circuit

In case of power systems ωL is generally $>> R$.

By using differential equations, the resulting current is:

$$I(t) = \frac{U}{Z} \times \left[\sin(\omega t + \alpha - \varphi) - e^{-t/\tau} \times \sin(\alpha - \varphi) \right] \quad \text{(A.1)}$$

where

U is the peak of the applied voltage $u(t)$;

Z is the circuit impedance: $Z = \sqrt{R^2 + \omega^2 L^2}$;

ω is the angular frequency: $2\pi f$;

α is the fault making angle (instant) on the applied sinusoidal voltage;

φ is the phase angle of the circuit impedance $\varphi = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\left(\frac{X}{R}\right)$;

τ is the DC time constant (L/R) of the circuit.

The resulting fault current has two components, the first part of the equation being the sinusoidal part and the second being the exponential decaying DC component.

From Equation (A.1), the DC component will be maximum when $\sin(\alpha - \phi) = 1$ or $\alpha - \phi = \pi/2$.

$$I(t)_{\max} = I\left[\sin(\omega t + \pi/2) - e^{-t/\tau} \right] \quad \text{(A.2)}$$

The peak value of the current will occur when $\sin(\omega t + \pi/2) = -1$ or $\omega t = \pi$ giving

$$I_{pk} = -I\left(1 + e^{-t/\tau}\right) \quad \text{(A.3)}$$

where $t = \pi/\omega$.

The maximum asymmetrical peak current is always obtained when the circuit-breaker is closed at 0° of the applied voltage (α= 0), which is not necessarily giving the maximum DC component. Equations (A.2) and (A.3) are approximate since the peak of the asymmetrical current does not occur exactly after π radians. However, the equations are accurate to at least two decimal places if the phase angle between the current peak and the zero of the applied voltage is less than 4° and therefore is suitable for the purpose.

Equations (A.2) and (A.3) are for the negative DC component case and, to obtain the positive DC component case, multiply the right side by –1. $I = U/Z$ and further equal to $\sqrt{2}$ times the symmetrical r.m.s. interrupting current rating of the circuit-breaker under consideration. The maximum peak current occurs when the circuit is made at a voltage zero crossing.

For the standardized DC time constants (45 ms and 120 ms) and the alternative special case DC time constants given in IEC 62271-100 (60 ms, 75 ms and 120 ms), the DC components in p.u. of the peak symmetrical current are shown in Figure A.2.

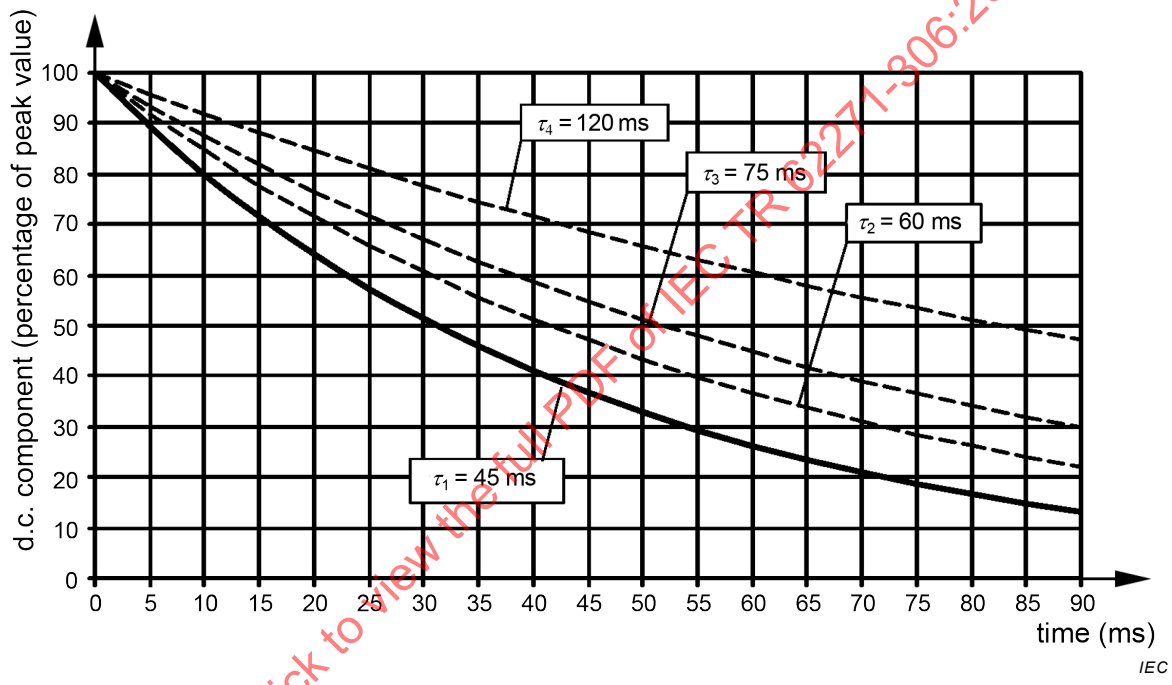


Figure A.2 – Percentage DC component in relation to the time interval from the initiation of the short-circuit for the standard time constants and for the alternative special case time constants (from IEC 62271-100)

Asymmetrical current related values of X/R and I_{peak} are power frequency dependent as summarized in Tables A.1 and A.2. The I_{peak} values in brackets are the recommended values used for standardization purposes in IEC 62271-100.

Table A.1 – X/R values

$\tau = L/R$	50 Hz		60 Hz	
ms	X/R	$\tan^{-1} X/R$	X/R	$\tan^{-1} X/R$
45	14	85,9	17	86,6
60	19	86,9	22,6	87,4
75	23,5	87,5	28,3	87,9
120	37,7	88,5	45,2	88,7

Table A.2 – I_{peak} values

$\tau = L/R$	I_{peak} (p.u.)	
ms	50 Hz	60 Hz
45	2,55 (2,5)	2,59 (2,6)
60	2,61 (2,7)	2,65 (2,7)
75	2,65 (2,7)	2,68 (2,7)
120	2,72 (2,7)	2,73 (2,7)

For a three-phase fault initiated simultaneously in the three phases, the DC component of the fault current at fault initiation of the most asymmetrical phase is always ranging from 87 % to 100 % whatever instant the fault is initiated on the applied voltage. This DC component range leads to an asymmetrical current peak ranging from 93,5 % to 100 % whatever instant the fault is initiated on the applied voltage.

The current equations for a three-phase fault initiated simultaneously on the three phases are:

$$I_{\varphi A}(t) = \frac{U}{Z} \times \left[\sin(\omega t + \alpha - \varphi) - e^{-t/\tau} \times \sin(\alpha - \varphi) \right] \quad \text{(A.4)}$$

$$I_{\varphi B}(t) = \frac{U}{Z} \times \left[\sin\left(\omega t + \alpha - \varphi - 2\pi/3\right) - e^{-t/\tau} \times \sin(\alpha - \varphi - 2\pi/3) \right] \quad \text{(A.5)}$$

$$I_{\varphi C}(t) = \frac{U}{Z} \times \left[\sin\left(\omega t + \alpha - \varphi + 2\pi/3\right) - e^{-t/\tau} \times \sin(\alpha - \varphi + 2\pi/3) \right] \quad \text{(A.6)}$$

In the first edition of IEC 62271-100 (and earlier editions of IEC 60056), the concept of DC component of the rated short-circuit current was used together with the asymmetry level at contact separation. At that time, a single unified standardized DC time constant of 45 ms was specified. With the introduction of new alternative special cases DC time constants, the concept of defining asymmetry level at contact separation has been changed to the concept of last current loop parameters since this is the important aspect to consider for arc energy and di/dt prior to interruption. This concept also allows performing tests on a circuit-breaker with a test circuit having a different time constant than the rated one and does also permit to validate more than one rating from the results obtained from a single T100a test series.

The considerations given in this subclause are based on the assigned ratings of the circuit-breaker and on the actual test parameters measured during the T100a test-duty.

The purpose of this subclause is to give guidance on how to use test results for validating other ratings with other DC time constants from a single test series results and to give guidance on how to modify the test parameters in order to obtain the required last current loop parameters. However, in doing this, the scope of this subclause is limited since the amplitude, duration and the di/dt at current zero all change as the DC time constant changes. A higher asymmetry results in a lower du/dt and peak value of the TRV, reducing the stress during the recovery process. This fact has been disregarded in the subclause dealing with equivalency and therefore the results can be considered conservative when the results obtained from a test series validating a lower DC time constant are used to validate an higher DC time constant rating. On the contrary, care should be exercised on the TRV parameters when the results obtained from a test series validating an higher DC time constant are used to validate a lower DC time constant rating. Annex I of IEC 62271-101:2012/AMD1:2017 gives the methodology for calculating TRV parameters during asymmetrical fault condition.

IEC 62271-100:2008/AMD1:2012 of introduces tolerances for testing purposes during the last current loop of arcing interval prior to interruption. A ±10 % tolerance is specified on both last current loop amplitude and duration. Then, the resulting product "$I \times t$", "I" being the peak value of the last current loop and "t" being the duration of the last current loop, will range between 81 % and 121 % of the required values.

The application of generator circuit-breakers breaking currents with delayed current zeros is beyond the scope of this document; this specific case is covered in IEC 62271-37-013 [145].

A.3 Network reduction

The rate of decay of the DC component is usually expressed as the DC time constant of the short-circuit current.

It should be noted that the DC time constant of the short-circuit current at the point of the fault is not the simple ratio of L/R typically obtained by network reduction short-circuit programs because each component of the network has its own DC time constant. Experience has shown that using the R and L values obtained by the typical network reduction short-circuit program will give the correct short-circuit current. However, the DC time constant based on the ratio of these values will generally be less than the correct value.

Transient calculation programs need to be used in order to obtain the correct DC time constant of a particular network location.

A.4 Special case time constants

With the publication of the first edition of IEC 62271-100 the concept of a circuit-breaker being able to deal with DC time constants other than the standard time constant of 45 ms was introduced for the first time. IEC 62271-100:2008 specifies additional "special cases time constants" of 60 ms, 75 ms and 120 ms in 4.101.2. In 4.101.2 b) of IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017, the following insight is provided:

– 120 ms for rated voltages up to and including 52 kV;
– 60 ms for rated voltages from 72,5 kV up to and including 420 kV;
– 75 ms for rated voltages 550 kV and 800 kV.

Moreover, IEC 62271-100:2008/AMD1:2012 introduces a second standardized DC time constant of the rated short-circuit current of 120 ms for circuit-breakers rated above 800 kV.

For application of circuit-breakers on power systems, IEC 62271-100 calls attention to the fact that not all applications fall within the confines of existing standards. The introduction of a special DC time constant value is a logical extension for the following reasons:

– the lower voltage circuit-breakers will frequently be applied close to generation or step down transformers or current limiting reactors which exposes the circuit-breakers in such locations to the much longer DC time constants;

– at the higher system voltages, bundled conductors may be used on transmission lines and the circuit-breaker again may be close to transformers. The bundled conductors and the transformer reactance will contribute to the higher DC time constant.

For the circuit-breaker application engineer, this raises the question of how to evaluate the individual applications. This annex tries to provide some guidance.

A.5 Guidance for selecting a circuit-breaker

A.5.1 General

To evaluate the effect of different DC time constants, some general observations can be made. For cases in which the actual short-circuit current is less but the DC time constant is greater, the di/dt of the current at current zero and the amplitude of current loops will be less than the rated values. The arc energy represented by the area under the major and the major extended current loop is probably one of the most important considerations. The amplitude and duration of the major and the major extended current loops are directly related to the DC time constant of the short-circuit current.

In an effort to evaluate the effect of different DC time constants, the standardized DC time constants of 45 ms and 120 ms, and special case DC time constants of 60 ms, 75 ms, 90 ms and 120 ms were examined.

IEC 62271-100:2008/AMD2:2017 introduces major changes for demonstration of arcing times during test-duty T100a. Both three-phase tests and single-phase tests in substitution of three-phase tests have been harmonized and are based on a three-phase fault condition. Tests on the minor current loop during single-phase test are not anymore required. Minimum clearing time ranges have been re-calculated based on the minimum clearing time (including relay time) and the zero crossings on the intermediate asymmetrical phase for which the minimum arcing time is defined. For practical reasons and because the DC component of the intermediate asymmetrical phase is relatively low, the minimum arcing time on the intermediate asymmetrical phase is considered to be the same as obtained during T100s and does not need to be re-demonstrated during T100a. It is acknowledged that for some circuit-breaker technologies the minimum arcing time obtained during T100s will be different that the one that would be obtained on the intermediate asymmetrical phase during T100a. For such cases, the required arcing times may not be obtained and additional tests up to a maximum of 6 tests are specified in order to demonstrate the required maximum arcing times.

IEC 62271-100 specifies criteria on the last current loop amplitude and duration. The important parameter to be considered is the arc energy from contact separation to interruption and the last current loop is of prime importance because generally most of the arc energy is within that last current loop, at least for modern circuit-breakers. The exact result would have been to compare the integral of the current waveshape from contact separation to current zero, but this type of calculation is not practical in test laboratories. Not all test laboratories have proper digital data acquisition systems or sufficient calculation tools to perform such calculation. Instead IEC 62271-100 asks to compare the parameters of the last current loop (I_{peak} and loop duration). Such measurements are easy to perform and can be done in all test laboratories without any specific constraints.

The methodology to evaluate the effect of different time constants is as follows:

a) Determine the last current loop parameters (amplitude and duration) obtained during T100a test series (last loops (major if tested single phase) or major and extended major current loop amplitudes and durations if tested three-phase.

b) Use Equations (A.4), (A.5) and (A.6) to find the current waveshapes of the specific case to be studied. Use an "α" of 0 rad. in order to obtain the full asymmetrical offset on one phase and resultant intermediate asymmetries on the two other phases.

c) Determine where the interruption will take place. The time sequence events in the operation of a circuit-breaker that always precede the actual interruption and tend to establish the most likely time for interruption are:

- relay time;
- circuit-breaker minimum opening time;
- minimum arcing time on the minor current loop of the intermediate asymmetrical phase starting with a minor current loop (as mentioned earlier, the minimum arcing time on the minor current loop of the intermediate asymmetrical phase is considered to be equal to the one found during T100s);
- The sum of the above times is defined in IEC 62271-100:2008/AMD2:2017 as the minimum clearing time. The major current loop of the full asymmetrical phase at a time after current initiation corresponding the end of the minimum clearing time range defined in Table 41 of IEC 62271-100:2008/AMD2:2017 for which the calculated minimum clearing time falls in is the current loop parameters for which the circuit-breaker should be able to interrupt.

Table 39 of IEC 62271-100:2008/AMD2:2017 has tabulated the last loop current parameters for standardized and alternative special cases DC time constants for both 50 Hz and 60 Hz systems.

Some assumptions have been taken:

a) The tolerance of ±10 % defined for both current amplitude and current loop duration is resulting in an allowable arc energy range during the arcing period. The arc voltage is assumed to be constant during the period of arcing. This allows the arc energy of the last current loop to be represented by the "$I \times t$" product;

   A smaller symmetrical fault current with a longer DC time constant (compared with the rated short-circuit-current and the standard time constant) has a larger percentage of DC component and the resultant di/dt is always less than the one associated with the highest rated short-circuit current. In such a case, the circuit-breaker should still be able interrupt at the normal current zero if it has met all other criteria;

b) If the arc energy represented by the "$I \times t$" product is less than 121 % of the standard wave, the interruption will be generally successful;

c) If the arc energy represented by the "$I \times t$" product is greater than 121 % of that of the standard interruption, the interruption could be unsuccessful.

Some circuit-breaker technologies use the arc energy as the main source of energy for current interruption. For such technologies, a lower arc energy may result in longer arcing times and the ability of interrupting lower current should be carefully evaluated. Care should be exercised in the evaluation of the minimum arcing time. The arc energy associated with minor current loops are lower for higher DC time constants that may result in a longer minimum arcing time and thus in a longer maximum arcing time.

The determination of the area X under the current curve may be obtained by solving Equation (A.7). This equation is the exact calculation method.

$$X = \int_{t_1}^{t_2} i(t)\mathrm{d}t \qquad \text{(A.7)}$$

where

$i(t)$ is the fully asymmetrical current $I_{\varphi A}(t)$ as given in Equation (A.4) for a making angle α = 0 rad;

t_1 is the time of contact separation;

t_2 is the time of current zero where interruption could occur.

As said before, this method cannot be easily used in test laboratories because it necessitates digital data acquisition systems with proper software, which are not always available. Instead, the comparison of the last current loop arcing energy by using the current loop parameters "$I \times t$" is a quite reasonable approximation (within 5 %) of the last current loop integral (see A.5.5).

The general guidance is to de-rate a circuit-breaker one class or approximately 80 % to deal with greater DC time constants. The question that should be answered is whether this is sufficient. For test purposes, IEC 62271-100 gives the following asymmetry criteria to be fulfilled when performing T100a:

– last current loop amplitude;
– last current loop duration;

Using the above methodology, the following cases were examined.

A.5.2 Case 1

Assumptions: Circuit-breaker ratings: I: 63 kA, τ = 45 ms and f = 60 Hz.

– relay time: 8,33 ms;
– minimum opening time: 17 ms;
– minimum arcing time (interruption on the minor loop of the intermediate asymmetrical phase starting with a minor loop): 8 ms;
– specific tests parameters recorded during T100a test-duty were exactly those associated with the rated values.

Table A.3 shows a comparison of the last major loop parameters for case 1 and for the first-pole-to-clear.

Table A.3 – Comparison of last major current loop parameters for the first-pole-to-clear, case 1

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	63	45	124,7	10,5	1 309
2	50	60	106,1/85,1	11,1/105,7	1 177/89,9
3	50	75	111,0/89,0	11,6/110,5	1 288/98,4
4	50	120	120,9/97,0	12,5/119,0	1 511/115,5

Particular points of Table A.3:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (63 kA and τ = 45 ms) had last current loop parameters equal to 100 % of the rated values as shown in the last three columns of row 1.

a) Row 1 provides the reference values for a 63 kA rating with τ = 45 ms as obtained during test duty T100a;

b) The 2nd row shows the requirements for a 50 kA rating with τ = 60 ms. The current amplitude is less than 90 % of the test current obtained at 63 kA. The current loop duration is within the tolerance given. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) In row 3, the rating is still 50 kA but the time constant has been increased to 75 ms. As for the second row, the current amplitude is slightly less than 90 % of the test current obtained at 63 kA. The current loop duration is within the tolerance given. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

d) In row 4, the rating is still 50 kA but the time constant has been further increased to 120 ms. Both current amplitude and current loop duration are with the tolerances prescribed by IEC 62271-100. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

The equivalence shown before should be carefully studied with the actual waveshape of the last current loop parameters used during tests for the demonstration of the reference rating (63 kA and τ = 45 ms). In accordance with IEC 62271-100 and IEC 62271-101 (in the case of synthetic testing), it is permissible to have the amplitude and the duration of the last current loop reduced by 10 % from the rated values. In such a case, the last current loop parameters for the first-pole-to-clear as shown in Table A.4 are obtained.

Table A.4 – Comparison of last major current loop parameters for the first-pole-to-clear, case 1: test parameters used for the reference case set at the minimum permissible values

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values and minimum tolerances	63	45	112,2 [a]	9,5 [b]	1 066
2	50	60	106,1/94,6	11,1/116,8	1 178/110,5
3	50	75	111,0/98,9	11,6/122,1	1 288/120,8
4	50	120	120,9/107,8	12,5/131,6	1 511/141,8
5	40	120	96,7/86,2	12,5/131,6	1 209/113,4

[a] Last current loop amplitude equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

[b] Last current loop duration equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

Particular points of Table A.4:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (63 kA and τ = 45 ms) had a last current loop parameters equal to 90 % of the rated values.

a) Row 1 provides the minimum permissible (90 %) reference values for a 63 kA rating with τ = 45 ms;

b) The 2nd row shows the requirements for a 50 kA rating with τ = 60 ms. The current amplitude is within the tolerance given. The current loop duration is more than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) The 3rd row shows the equivalence for a 50 kA rating with τ = 75 ms. The current amplitude is within the tolerance given. The current loop duration is more than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

d) As for the case shown in row 4, the rating is still 50 kA but the time constant has been increased to 120 ms. The current amplitude is still within the tolerance given. The current loop duration is significantly higher than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters exceeds the resulting tolerance derived from the criteria defined in IEC 62271-100, thus the interrupting capability cannot be assessed by the test done at 63 kA;

e) The last row shows the requirements for a 40 kA rating with τ = 120 ms. The current amplitude is lower than 90 % of the current obtained during the test at 63 kA. The current loop duration is more than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

From the above examples, it can be shown that the actual test parameters obtained during tests are of major importance to determine to which extent the reference test can be used to demonstrate the circuit-breaker ability to interrupt other fault currents with different DC time constants. From these examples, it has been shown that the one or two de-rating steps from the R10 series may be needed to cover lower short-circuit currents with higher DC time constants.

Finally, the comparison with the last major current loop parameters may be not enough to state if a particular circuit-breaker may be used for lower rated short-circuit current and higher DC time constant values. Some circuit-breaker technologies use the arc energy as the main source of energy for current interruption. Careful evaluation of the minimum arcing time needs to be done. Comparison of minimum arcing times obtained during T10, T30, T60 and T100s can be used as a tool to evaluate the increase of the minimum arcing time due to the reduced arc energy. If the minimum arcing times found during T10, T30 and T60 are not greater by more than a ¼ cycle from that measured in T100s, then it can be considered that a similar minimum arcing time on the minor loop than the reference case would be obtained. If this is the case, comparison of the last major current loop parameters to access circuit-breaker capabilities is sufficient. If not, additional tests may need to be performed to ensure that the minimum arcing time will not be significantly longer than the reference case.

A.5.3 Case 2

Assumptions: Circuit-breaker ratings: I = 20 kA, τ = 45 ms and f = 50 Hz.

– Relay time: 10 ms;

– Minimum opening time: 22 ms;

– Minimum arcing time (interruption after on the minor loop of the intermediate asymmetrical phase starting with a minor loop): 8 ms.

A comparison of the last loop parameters for the first-pole-to-clear is shown in Table A.5.

Table A.5 – Comparison of last major current loop parameters of the first-pole-to-clear, case 2

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	20	45	37,6	12,2	458,7
2	16	60	32,6/86,7	12,9/105,7	420,5/91,7
3	16	75	34,2/90,9	13,4/109,8	458,3/99,9
4	16	120	37,6/100	14,6/119,7	549,0/119,8
5	12,5	120	29,3/78,0	14,6/119,7	427,8/93,2

Particular points of Table A.5:

As mentioned in Table A.1, it should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (20 kA and τ = 45 ms) had a last current loop parameters equal to 100 % of the rated values as shown in the last three columns of row 1 of Table A.5.

a) Row 1 contains the reference values for 50 Hz, 20 kA rating;

b) In rows 2 to 5, it can be seen that a reduction of one step in the R 10 series will cover all cases for τ = 60 ms, 75 ms, 90 ms and 120 ms. For all these cases, the product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

As also mentioned for case 1, the applicability of a reference case to other fault currents and different DC time constants depends on the actual test parameters measured for the reference case. As an extreme case, if we consider that the last major current loop parameters during the reference test were at the minimum tolerance stated by IEC 62271-100 and IEC 62271-101, then the current loop parameters for the first-pole-to-clear of Table A.6 are obtained.

Table A.6 – Comparison of last major current loop parameters for the first-pole-to-clear, case 2: test parameters used for the reference case set at the minimum permissible values

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values and minimum tolerances	20	45	33,8 [a]	11,0 [b]	371,8
2	16	60	32,6/96,2	12,9/117,3	420,5/113,1
3	16	75	34,2/100,9	13,4/121,8	458,3/123,3
4	16	120	37,6/110,9	14,6/132,7	549,0/147,6
5	12,5	120	29,3/86,4	14,6/132,7	427,8/115,1

[a] Last current loop amplitude equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

[b] Last current loop duration equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

Particular points of Table A.6:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (20 kA and τ = 45 ms) had a last current loop parameters equal to 90 % of the rated values.

a) Row 1 provides the minimum permissible (90 %) reference values for a 20 kA rating with τ = 45 ms;

b) The 2nd row shows the requirements for a 16 kA rating with τ = 60 ms. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) The 3rd and the 4th rows show the equivalence for a 16 kA rating with τ = 75 ms and 120 ms. For these cases, the "$I \times t$" products calculated from the last current loop parameters exceed the resulting tolerance derived from the criteria defined in IEC 62271-100, and the reference rating does not demonstrate the performance of the circuit-breaker for these specific cases;

d) The last row shows the requirements for a 12,5 kA rating with τ = 120 ms. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

From the above examples, it can be shown, as for case 1, that the actual test parameters obtained during tests are again of crucial importance to determine to which extent the reference test can be used to demonstrate the circuit-breaker ability to interrupt other fault currents with different DC time constants. From these examples, it has been shown that the one or two de-rating steps from the R10 series may be needed to cover lower short-circuit currents with higher DC time constants.

A.5.4 Case 3

The examples given in A.5.2 and A.5.3 were based on single-phase tests or for the first-pole-to-clear loop parameters during three-phase tests. For three-phase tests on medium voltage circuit-breakers, very short minimum arcing times may be observed in particular for vacuum circuit-breakers. As an extreme example, Figure A.3 shows the resulting current curves for a circuit-breaker having a minimum arcing time of 1 ms.

For the first valid operation, the interruption occurs on phase A for which the asymmetry criteria is met.

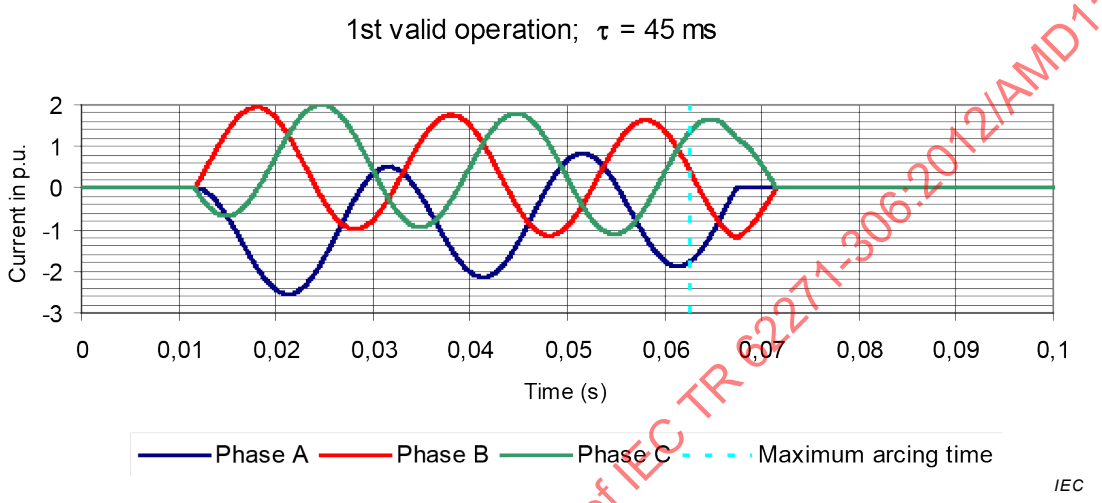


Figure A.3 – First valid operation in case of three-phase test (τ = 45 ms) on a circuit-breaker exhibiting a very short minimum arcing time

This example shows that the maximum possible arcing time on the asymmetrical phase is less than half of the major loop duration. The actual arcing time represents only 40 % of the major loop duration.

For the second test, the procedure given in IEC 62271-100 has been followed and the current oscillogram shown in Figure A.4 is obtained.

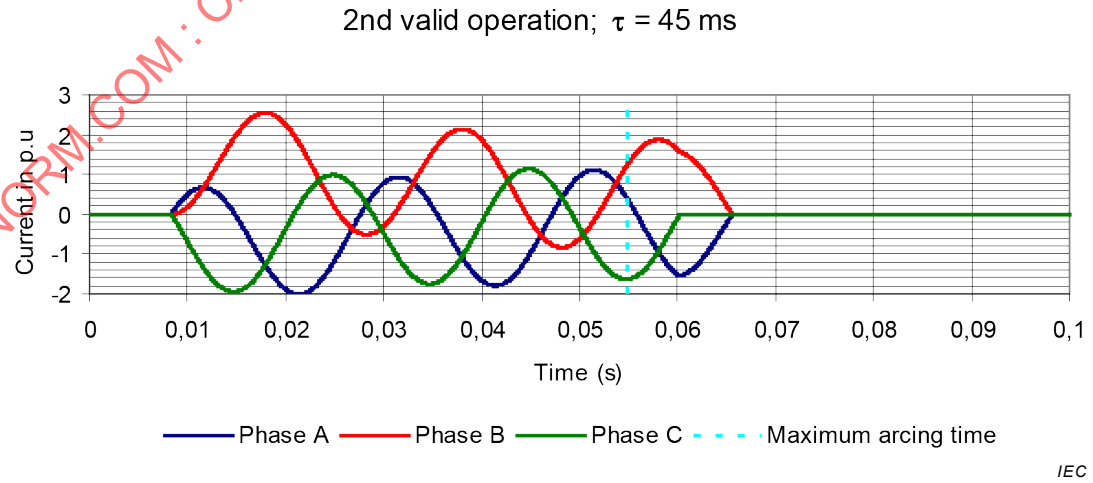


Figure A.4 – Second valid operation in case of three-phase test on a circuit-breaker exhibiting a very short minimum arcing time

The interruption occurs on phase B on an extended major current loop. This example shows that the maximum possible arcing time on the extended major loop is slightly less than the extended major loop duration. The actual arcing time represents 86 % of the extended major loop duration.

Finally, for the third valid operation, the curves of Figure A.5 are obtained:

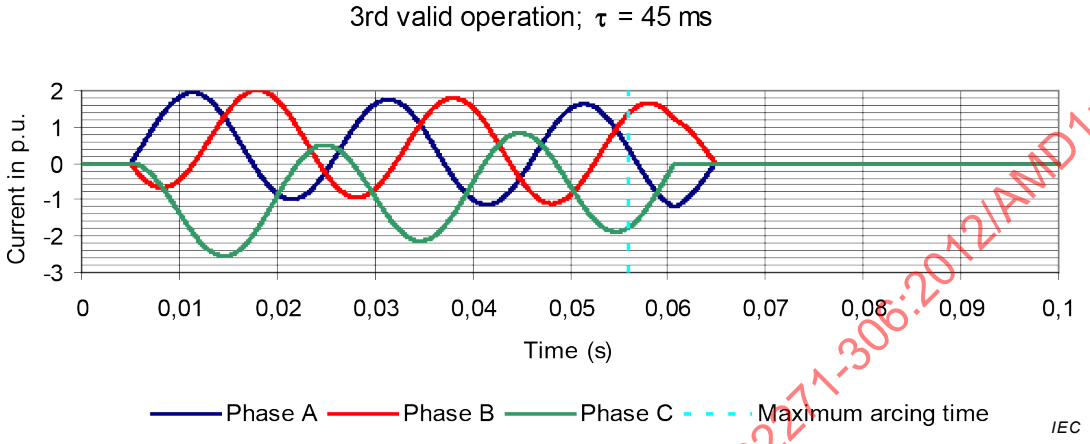


Figure A.5 – Third valid operation in case of three-phase test on a circuit-breaker exhibiting a very short minimum arcing time

The interruption occurs on phase C on a major current loop. Here also, as the first valid operation, the maximum possible arcing time on the asymmetrical phase is less than half of the major loop duration. The actual arcing time represents 46 % of the major loop duration.

The fact that this type of circuit-breaker exhibiting very short minimum arcing time does not see the full major and extended major loop, this raises the question if the "$I \times t$" method is still valid for such circuit-breakers. For the case shown before, the arc energy for the interruption on the major current loop will be not more than 50 % of the one calculated for the full major current loop. For the extended major loop, energy calculation has shown that 89 % of the relative full extended loop energy will be seen by the circuit-breaker.

Similar calculations have been done with a DC time constant of 120 ms and the results are very similar, mainly regarding the relative arc energy associated with the major extended current loop. For that particular case, the energy associated with the maximum possible arcing time represents 88 % of the total prospective arc energy of that current loop. For the other valid operations on the major current loop, the maximum arcing time window is slightly less than the 45 ms case (less than 40 % of the loop duration).

Because the relative arc energy associated with the extended major loop is quite close to 100 %, it is reasonable to use the same equivalency criteria ("$I \times t$" product) for circuit-breakers tested three-phase and exhibiting short minimum arcing times (e.g. < 3 ms).

A.5.5 Validity of the equivalence method prescribed by IEC 62271-100

IEC 62271-100 recommends a simple and practical way for the evaluation of the last loop parameters e.g. last loop current amplitude and last loop current duration. The resultant arc energy of the last current loop prior to interruption can be calculated by multiplying the loop amplitude by the loop duration to obtain a representative loop area ("$I \times t$" product) for comparison.

Table A.7 gives the results of the relative arc energy calculations for the different 60 Hz currents and DC time constants for interruption at the end of a major loop.

Table A.7 – 60 Hz comparison between the integral method and the "$I \times t$" product method

Row	Current rating kA r.m.s. symmetrical	Time constant ms	Area of the last major loop by the exact integral method As	Peak of last major loop I kA	Last loop duration ms	$I \times t$ As	Ratio: area of major loop	Ratio: product $I \times t$	Difference to integral method %
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
1	63	45	805,8	124,7	10,55	1 309	1	1	-
2	50	60	718,2	106,1	11,1	1 177	0,89	0,90	1,01
3	50	75	777,8	111,0	11,6	1 288	0,96	0,98	2,08
4	50	120	890,5	120,9	12,5	1 511	1,10	1,15	4,55
5	40	120	712,4	96,7	12,5	1 209	0,88	0,92	4,55
The ratio area of column (8) is derived from column 4 divided by 805,8 and the ratio area of column (9) from division of column (7) by 1 309.									

Similarly, Table A.8 gives the results of the relative arc energy calculation for the different 50 Hz currents and DC time constants for interruption at the end of a major loop.

Table A.8 – 50 Hz comparison between the integral method and the "$I \times t$" product method

Row	Current rating kA r.m.s. symmetrical	Time constant ms	Area of the last major loop by the exact integral method As	Peak of last major loop I kA	Last loop duration ms	$I \times t$ As	Ratio: area of major loop	Ratio: product $I \times t$	Difference to integral method %
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
1	63	45	893,2	118,5	12,2	1 446	1	1	
2	50	60	802,0	101,8	12,9	1 313	0,90	0,91	1,11
3	50	75	875,2	106,8	13,4	1 431	0,98	0,99	1,02
4	50	120	1 019,2	117,4	14,6	1 714	1,14	1,19	4,38
5	40	120	815,3	93,9	14,6	1 371	0,91	0,95	4,40
The ratio area of column (8) is derived from column 4 divided by 893,2 and the ratio area of column (9) from division of column (7) by 1 446.									

Particular points of Tables A.7 and A.8:

a) Row 1 is the reference case;

b) In rows 2 to 5, the "$I \times t$" method is compared to the exact integral method for determining the relative arc energy of the last major current loop prior to interruption;

c) Rows 2 to 5 show that the relative difference between the two methods remains below 5 %.

With a difference of less than 5 % for a DC time constant variation from 45 ms to 120 ms, it is shown that the "$I \times t$" method is fully adequate to extend test results for another current and DC time constant ratings. The integral method should be considered as the exact method to calculate the equivalent arc energy during the last current loop and also during the whole

arcing period but cannot be implemented in all test laboratories because of the different capabilities of the measuring system used. Therefore, the "$I \times t$" method was proposed to ease and speed up the result analysis after a test. "$I \times t$" is considered a reasonable approximation of the energy in the last major loop.

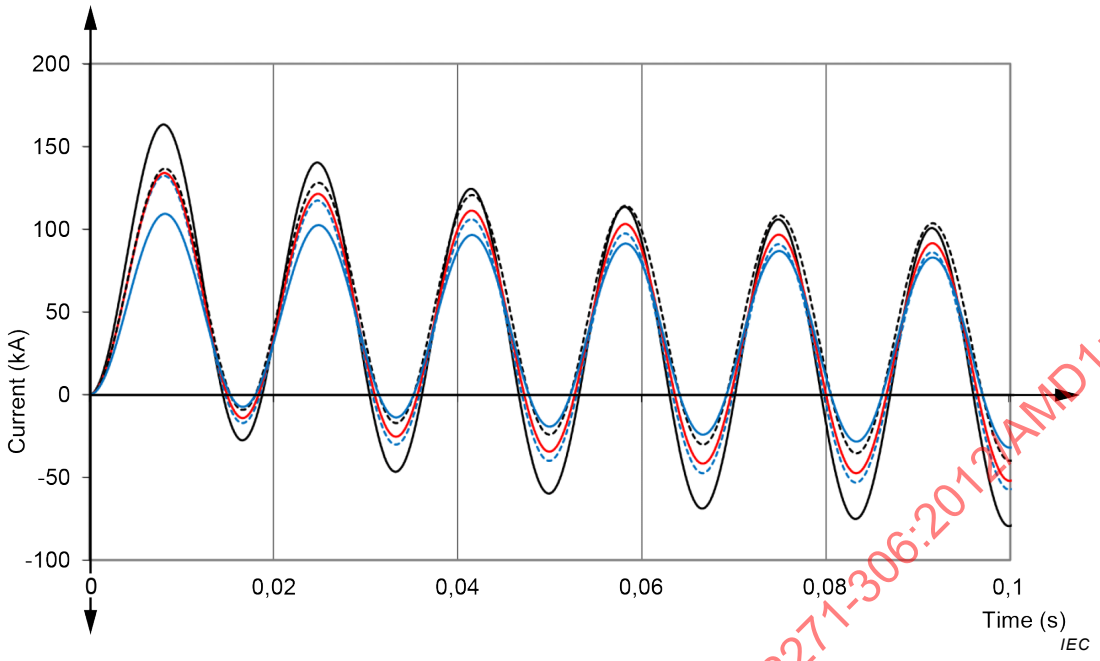
A.6 Discussion regarding equivalency

The method of analysis described for demonstrating the equivalency is not difficult to perform but access to the actual test results for the reference case is necessary. It should also be recognized that this investigation is only addressing a simultaneous three-phase fault case where one of the phases has always an offset ranging from 87 % to 100 % of the full DC offset depending on the point-on-wave initiation. It is the resulting current from that fully asymmetrical phase that has been compared. The fault currents that circulate in the other two phases will have significant reduced DC components and the ability of the circuit-breaker to interrupt these currents is not considered more difficult than those of all other test duties defined by IEC 62271-100.

This investigation supports the recommendation that if DC time constants greater than 45 ms are encountered on a system, the selection of a circuit-breaker rated one or two steps up (depending on actual test parameters for the reference case) in the R10 series above the expected system fault current for DC time constants up to 120 ms should be satisfactory. While the number of cases investigated is limited, the method can be applied to almost any combinations of three-phase fault currents and related DC time constants as a predictor of the maximum amount of energy involved.

Figure A.6 and Figure A.7 show selected plots for Case 1 and Case 2 of the currents with different DC time constants for both 60 Hz and 50 Hz respectively. An examination of the figures suggests that it is possible to use this method to evaluate different test combinations. For example one could use it to evaluate a test current at 50 Hz to show equivalence to a test current at 60 Hz. Since most such tests on high-voltage circuit-breakers will be done using synthetic circuits, the di/dt can be adjusted to the correct value at the time of interruption. By varying the amplitude of the current, the arc energy can be adjusted to be equivalent. For the manufacturer and/or user that knows the interrupting characteristics of a circuit-breaker, the outlined method is a useful tool for the evaluation of different interrupting capabilities under asymmetrical fault conditions.

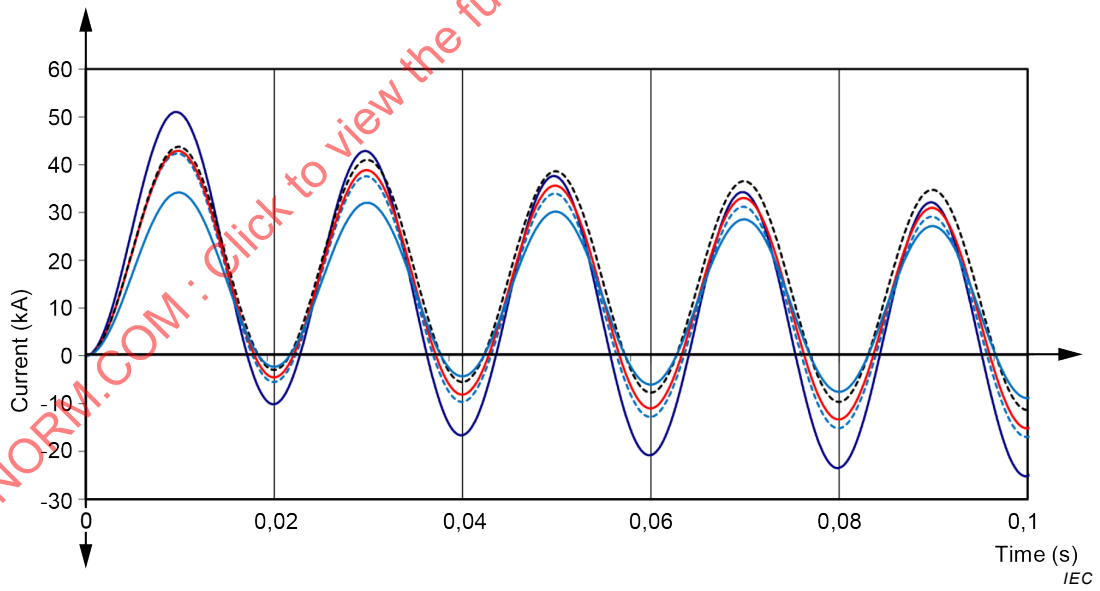
IEC 62271-100 recognizes the problems associated with testing circuit-breakers with different DC time constants. It is fundamental that the circuit-breaker sees the correct prospective di/dt and at the time of interruption. As mentioned earlier, if synthetic tests are conducted, this can be adjusted to the correct value. If direct tests are used, the current level is adjusted within the prescribed tolerance to have the associated di/dt at the time of interruption. One fundamental consideration that should be accounted for is the DC time constant of the test station whether direct or synthetic test are used. The effective arc energy level under the last current loop can be adjusted by selecting the initiation instant of the short-circuit current (e.g. asymmetry level) or by adjusting the current level or a combination of both to obtain the correct last current loop parameters (amplitude and duration). Clause A.7 gives examples of waveshape adjustments during testing.



Key

Black, solid	63 kA, τ = 45 ms
Blue, dashed	50 kA, τ = 60 ms
Red	50 kA, τ = 75 ms
Black, dashed	50 kA, τ = 120 ms
Blue, solid	40 kA, τ = 120 ms

Figure A.6 – Plot of 60 Hz currents with indicated DC time constants



Key

Dark blue, solid	20 kA, τ = 45 ms
Blue, dashed	16 kA, τ = 60 ms
Red	16 kA, τ = 75 ms
Black, dashed	16 kA, τ = 120 ms
Blue, solid	12,5 kA, τ = 120 ms

Figure A.7 – Plot of 50 Hz currents with indicated DC time constants

A.7 Current and TRV waveshape adjustments during tests

A.7.1 General

The examples given in this clause are based on standardized cases and give guidelines how to use the asymmetry criteria defined in IEC 62271-100:2008 in an actual test. It is usual that the DC time constant of the circuit-breaker is different than the DC time constant of the test circuit and some adjustments on the test parameters are necessary. Three different cases are given covering the major cases that may occur in test laboratories.

A.7.2 Three-phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current constant longer than the test circuit time constant

Rated voltage of the circuit-breaker:	24 kV
First-pole-to-clear factor:	1,5
DC time constant of the rated short-circuit breaking current:	120 ms
Test circuit time constant:	60 ms
Minimum arcing time during T100s:	7,5 ms
Minimum opening time:	32,5 ms
DC component at contact separation:	70,2 %
Minimum clearing time:	50 ms
Frequency:	50 Hz

The time constant of the test circuit differs from the DC time constant of the rated short-circuit breaking current. The adjustment method chosen in order to reach the required data is the pre-tripping method together with controlled closing.

NOTE 1 Controlled closing means the initiation of the test current at a chosen instant on the applied voltage in order to vary the initial DC component of the test current.

Table A.9 – Example showing the test parameters obtained during a three-phase test when the DC time constant of the test circuit is shorter than the DC time constant of the rated short-circuit current

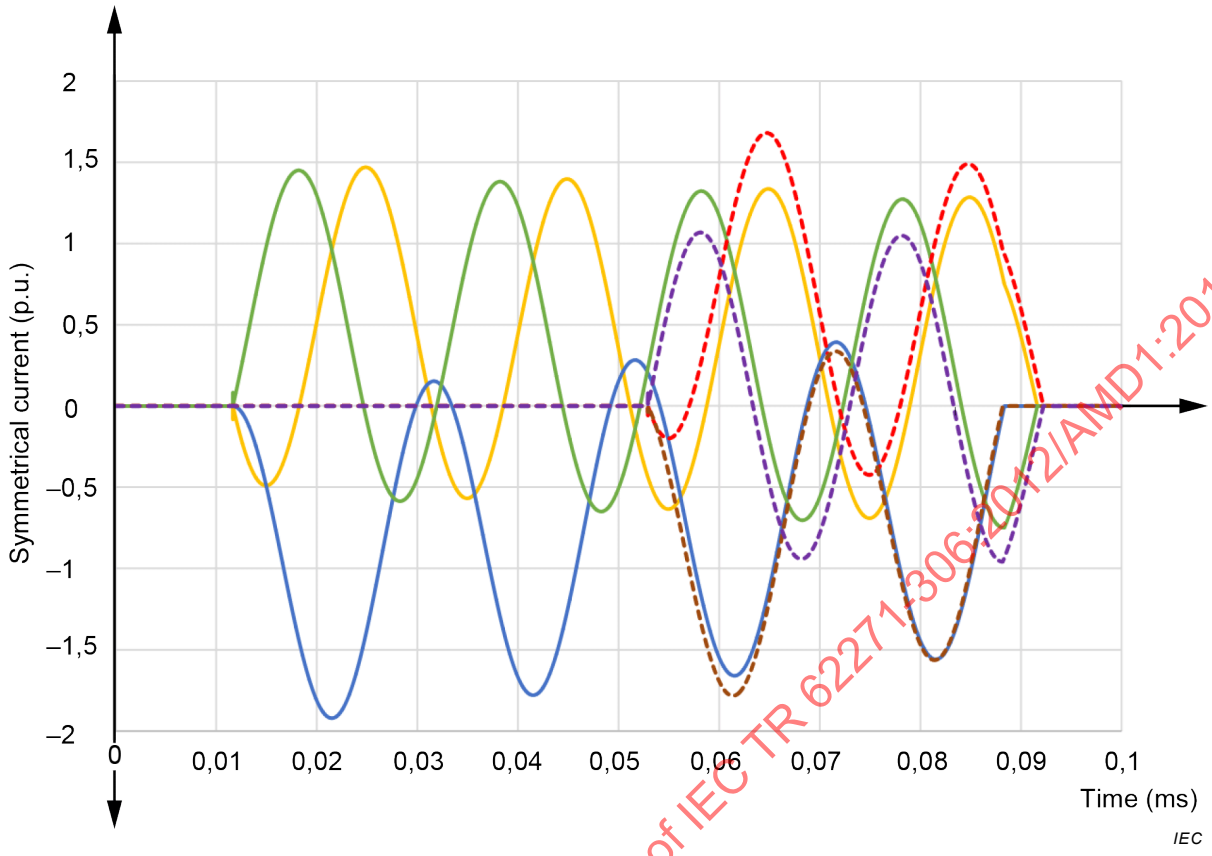
Parameters	Requirements (calculated values)		Test data when using pre-tripping and controlled closing methods		Deviation between required values and test values %
	Major loop with first clearing pole	Last-poles-to-clear major/minor loop [a]	Major loop with first clearing pole	Last-poles-to-clear major/minor loop [a]	
DC component at current interruption (%)	62,1		50,1		-19,3
di/dt at current interruption (%)	80,0		89,2		+11,5
Peak of the last current loop (p.u.)	1,56	1,28/0,75	1,56	1,48/0,95	0 +15,6/26,6[b]
Duration of the last current loop (ms)	13,8	12,7/7,45	13,8	14,1/8,8	0 +11/+17,8 [b]
Δt (ms) [c]		3,3		4,0	+21
I x t (p.u. ms)	21,53		21,53		0

[a] Values calculated for a non-effectively earthed neutral system using a network calculation program (see NOTE 2).

[b] Last-poles-to-clear.

[c] Δt is the time interval between the first-pole-to-clear and the last-poles-to-clear.

Result: It is possible to fulfil the requirements by using the pre-tripping and controlled closing options. In this particular case, the current initiation has been delayed by 2 cycles and the making angle has been moved from 0° to 22,5°. The TRV and di/dt values will be approximately 12 % higher than required. The arcing time for the last clearing poles will be slightly longer than the required one. The test data cover the required values. Tighter tolerances on the di/dt and on the TRV peak may be achieved by lowering test current and/or the TRV amplitude factor. The results are illustrated in Figure A.8.



Key

Solid yellow line	Required current in A-phase
Solid blue line	Required current in B-phase
Solid green line	Required current in C-phase
Dotted red line	Test circuit A-phase
Dotted brown line	Test circuit B-phase
Dotted purple line	Test circuit C-phase

NOTE Owing to the shorter time constant of the test circuit, the short-circuit current is initiated later (pre-tripping method and to choose the closing angle in a way to achieve the required DC component at current zero (controlled closing).

Figure A.8 – Three-phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current longer than the test circuit time constant

As seen in Table A.9, the ratings of the circuit-breaker given in A.7.2 are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified DC time constant of the rated short-circuit breaking current of 120 ms, it does not take into account the arcing time and the DC time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop.

NOTE 2 The easiest way to calculate the required three-phase or single-phase waveshape characteristics is by a network calculation program such as EMTP, MATHLAB, etc. The waveshape characteristics can also be calculated by hand from the fundamental three-phase or single-phase short-circuit current equations.