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TECHNICAL REPORT

colour inside

Process management for avionics – Electronic components capability in operation – Part 2: Semiconductor microcircuit lifetime

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IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS CAPABILITY IN OPERATION –

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FOREWORD

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IEC TR 62240-2, which is a Technical Report, has been prepared by IEC technical committee 107: Process management for avionics.

IEC TR 62240-2 adapts and modifies the GIFAS/2015/5022 document that has served as a basis for the elaboration of this Technical Report.

The text of this Technical Report is based on the following documents:

Draft TR	Report on voting
107/325/DTR	107/332/RVDTR

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

Electronic equipment for aerospace, defence and high performance (ADHP) applications integrate more and more commercial off the shelf (COTS) semiconductor microcircuits. These semiconductor microcircuits are above all designed and produced to address high volume and low cost markets such as consumer electronics, telecommunications or microcomputers, whose main requirements are basically cost, integration, performance and low consumption and for which the long term reliability in severe environments (for example vibration, thermal cycling, humidity and operating temperature) is not necessarily an imperative design criterion.

With semiconductor transistor feature size decrease, mainly from 90 nm transistor feature size, early wear-out can arise in COTS semiconductor microcircuits. For example, non-homothetic evolution of semiconductor microcircuit bias voltage and transistor feature size scaling have led to an increase of the electrical fields inside the semiconductor microcircuit and hence changes in classical failure and degradation modes or mechanisms. In addition new transistor architectures and technologies (for example fin field effect transistor (FinFET), fully depleted silicon on insulator (FD-SOI), etc.) and new materials (for example low-k dielectrics, high-k dielectrics, strain source/drain Si-Ge) have been introduced since the generation 90 nm to overcome the scaling issues, contributing potentially to the evolution of failure and degradation modes or mechanisms.

In this context, the lifetime of new generations of COTS semiconductor microcircuits may not meet the lifetime requirements of high performance, high reliability and long duration electronic applications (for example twenty years, thirty years or more). As a consequence, specific reliability assessment and maintenance plans are considered within the semiconductor microcircuit selection activities.

PROCESS MANAGEMENT FOR AVIONICS – ELECTRONIC COMPONENTS CAPABILITY IN OPERATION –

Part 2: Semiconductor microcircuit lifetime

1 Scope

This part of IEC 62240, which is a Technical Report, focuses on original equipment manufacturers (OEMs) using commercial off the shelf (COTS) semiconductor microcircuits for high performance, high reliability and long duration applications. This document supports OEMs in the preparation and maintenance of their semiconductor electronic component management plan (ECMP).

This document describes a process and a method for selecting digital semiconductor microcircuits by ensuring that their lifetime is compatible with the requirements of aerospace, defence and high performance (ADHP) applications (generally in connection with functional environments). Methods and guidelines are provided to assess the long term reliability of COTS semiconductor microcircuits in such applications; they mainly apply during the electronic design phase when selecting semiconductor microcircuits and assessing the application reliability.

Moreover, the document focuses on the intrinsic wear-out and the lifetime of COTS semiconductor microcircuits processed of less than or equal to 90 nm feature size (also called deep sub-micron (DSM) semiconductor microcircuits) and puts aside, at this time, packaging wear-out and random failure mechanisms. In this view, physics of failure (PoF) is at the heart of the approach.

NOTE 1 IEC 62239-1 can assist OEMs in the creation and maintenance of ECMPs.

NOTE 2 SAE ARP6338 can also help the OEM with regard to assessment and mitigation of early wear-out of life-limited semiconductor microcircuits.

NOTE 3 With the evolution of electronic technology and semiconductor microcircuits processed of less than or equal to 90 nm feature size, the current MIL-HDBK-217 handbook or FIDES guide become inappropriate as they are based for the time being on the assumption that the semiconductor electronic component exhibits a constant (random) failure rate and does not have life limits or exhibit wear-out.

Moreover, silicon itself has fundamentally very low failures in time (FIT) rates and the major failure modes are often in the packaging (for example housing, bond wires, etc.).

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1.1
acceleration model
equation for predicting time-to-fail as a function of operating stress

Note 1 to entry: An acceleration model shows how time-to-fail at a particular operating stress level can be used to predict the equivalent time-to-fail at a different operating stress level.

Note 2 to entry: An acceleration model is associated to one failure and degradation mode or mechanism. Acceleration models can be either defined for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

Note 3 to entry: An acceleration model is semi-empirical and is basically based on the physics of failure. Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

Note 4 to entry: The acceleration model is also defined as acceleration factor, for which the abbreviated term AF is used.

3.1.2
Bi-CMOS
bipolar CMOS
technology integrating two separate semiconductor technologies, bipolar junction transistor and CMOS transistor, in a single electronic component

3.1.3
cold redundancy
technique where one primary part is operational and the redundant one is in a backup mode

Note 1 to entry: The redundant part can also be called “cold” part and generally it is technically identical to the primary part.

Note 2 to entry: The “cold” part can be non-powered or in a standby mode and it is usually called upon only on failure of the primary part.

3.1.4
electronic equipment
functioning electronic device produced by the plan owner, which incorporates electronic components

Note 1 to entry: End items, sub-assemblies, line-replaceable units and shop-replaceable units are examples of electronic equipment.

[SOURCE: IEC 62239-1:2018, 3.20]

3.1.5
high-k dielectrics
material with a high dielectric constant “k” (as compared to silicon dioxide)

Note 1 to entry: High-k dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a semiconductor microcircuit. The implementation of high-k gate dielectrics is one of several strategies developed to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.6
lifetime
upper bound of period of time during which the COTS semiconductor component performs a required function without failure under stated conditions

3.1.7
low-k dielectrics
material with a small dielectric constant “k”, relative to silicon dioxide

Note 1 to entry: Low-k dielectric material implementation is one of several strategies used to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.8
NAND
Negative-AND
logic gate which produces, in digital electronics, an output that is false (0) only if all its inputs are true (1) and an output true (1) if one or both inputs are false (0)

[SOURCE: IEC 62239-1:2018, 3.22]

3.1.9
NOR
Negative-OR
logic gate which produces, in digital electronics, an output that is true (1) if both the inputs are false (0) and an output false (0) if one or both inputs are true (1)

[SOURCE: IEC 62239-1:2018, 3.23]

3.1.10
plan owner
original design authority responsible for all aspects of the design, functionality and reliability of the delivered equipment in the intended application and responsible for writing and maintaining their specific ECMP

[SOURCE: IEC 62239-1:2018, 3.26]

3.1.11
process node
specific semiconductor manufacturing process and its design geometry rules

Note 1 to entry: Generally, a smaller technology node means a smaller feature size, producing smaller transistors which are both faster and more power-efficient. Historically, the name “process node” referred to a number of different features of a transistor including the gate length as well as the first layer metal half-pitch. Most recently, due to various marketing practices and discrepancies among foundries, the name “process node” has lost the exact meaning it once held. Recent technology nodes below 90 nm refer purely to a specific generation of semiconductor microcircuits made in a particular technology; they do not correspond to any gate length or half pitch. Nevertheless the name convention has stuck and it is what the leading foundries call their nodes.

Note 2 to entry: Process node is also called technology node or simply node.

3.1.12
semiconductor microcircuit
semiconductor electronic component
electrical or electronic device that is not subject to disassembly without destruction or impairment of design use and that utilises the properties of semiconductor materials

Note 1 to entry: It is sometimes called electronic part or electronic piece part or electronic device or electronic component or integrated circuits. It refers to active electronic parts such as memories, microcontrollers, microprocessors, etc.

3.1.13
wear-out
phenomenon resulting in a permanent physical degradation of a semiconductor that can be quantified through a quasi-deterministic lifetime indicator

3.2 Abbreviated terms

ADHP	aerospace, defence and high performance
AF	acceleration factor
BEOL	back end of the line
BTI	bias temperature instability
COTS	commercial off the shelf (related to semiconductor microcircuits for the purposes of this document)
CMOS	complementary metal-oxide semiconductor
DDR	double data rate (memory)
DPA	deprocessing analysis
DRAM	dynamic random access memory
DSM	deep sub-micron
ECMP	electronic component management plan
EM	electro-migration
EOT	equivalent oxide thickness
FD-SOI	fully depleted silicon on insulator
FEOL	front end of the line
FinFET	fin field effect transistor
FIT	failures in time (number of failures that can be expected in one billion device-hours of operation)
FPGA	field programmable gate array
Ge	germanium
HCI	hot carrier injection
I/O	input/output
MRAM	magnetic random access memory
NMOS	N metal-oxide semiconductor
OCM	original component manufacturer (related to the COTS electronic components manufacturer)
OEM	original equipment manufacturer
PMOS	P metal-oxide semiconductor
PoF	physics of failure
Si	silicon
SDRAM	synchronous dynamic random access memory
SRAM	static random access memory
TDDB	time dependent dielectric breakdown
$TTF_{X\%}$	time to failure (or lifetime) for x % of samples

4 Lifetime assessment process and method

4.1 General

The aim of the method is twofold. In a first step, this method allows the assessment and determination of the lifetime of a COTS semiconductor microcircuit in a specific environment, and in the second step it provides the means for the OEM to select the right COTS semiconductor microcircuit according the electronic equipment reliability requirements.

The method is synthetized in the process flow of Figure 1.

Moreover, according to the level of information available from the OCMs and/or silicon foundries, three different paths can be considered:

– path and approach 1 (represented in yellow in Figure 1) where the OEM considers for its application the lifetime assessment of the COTS semiconductor microcircuit with regard to the lifetime specified and associated technical data provided by the OCM;

– path and approach 2 (represented in orange in Figure 1) where, in the absence of lifetime data specified by the OCM or if associated technical data are incomplete, the OEM conducts for its application its own lifetime assessment of the COTS semiconductor microcircuit, making a risk analysis and using the available technical data (for example, failure and degradation mechanisms, acceleration models, raw qualification test results) provided by the OCM;

– path and approach 3 (represented in burgundy in Figure 1) where, in case of unavailability or irrelevancy of OCM technical data, the OEM conducts for its application its own lifetime assessment of the COTS semiconductor microcircuit collecting potential technical data and considering the technology of the semiconductor microcircuit (including potential deprocessing analysis (DPA)).

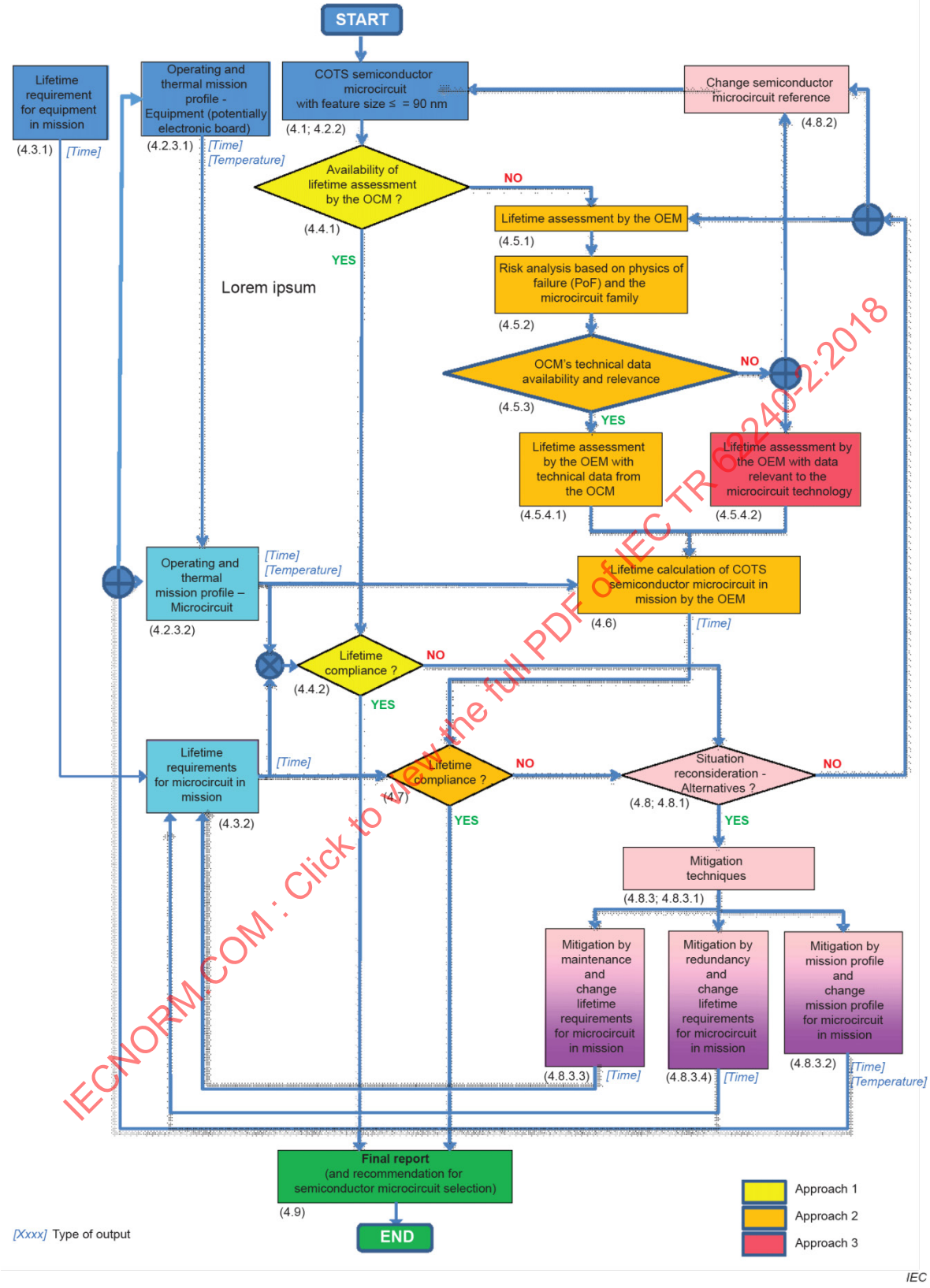

Figure 1 – Process flow for lifetime assessment and selection of COTS semiconductor microcircuits

4.2 Input data for the method

4.2.1 General

The input data for the method are as follows.

4.2.2 COTS semiconductor microcircuits and lifetime issues considerations

Wear-out and lifetime considerations need to be taken into account for electronic designs using COTS semiconductor microcircuits manufactured in 90 nm process nodes and below. This includes digital COTS semiconductor microcircuits such as SRAM, DRAM (SDRAM, DDR series), flash memories (NOR logic gate, NAND logic gate), MRAM, microcontrollers, microprocessors and FPGA. Analog or Bi-CMOS electronic components can also be concerned and a similar approach can be used.

The process node can be obtained from the original component manufacturer's datasheet or indicated on the part number marking or by contacting the OCM directly.

Intrinsic failures and degradations of semiconductor microcircuits which can impact wear-out are typically electro-migration (EM), time-dependent dielectric breakdown (TDDB), hot carrier injection (HCI), and bias temperature instability (BTI). Annex A provides more informative details.

4.2.3 Operating and thermal conditions

4.2.3.1 Operating and thermal mission profiles of the electronic equipment

The OEM usually obtains this information through the electronic equipment specification, standards, or customer requirements.

4.2.3.2 Operating and thermal mission profile of COTS semiconductor microcircuit

The semiconductor microcircuit mission profile is directly derived from the electronic equipment operation conditions (for example operating, thermal), see 4.2.3.1. In this sense, it is defined by the OEM. The mission profile at the COTS semiconductor microcircuit level lists all stresses applied on it during the mission life. Based on semiconductor physics of failure, the most critical stresses identified are typically the electrical bias current/voltage and the semiconductor microcircuit junction temperature by period of time. As an example, an operating and thermal mission profile of a semiconductor microcircuit implemented in an avionics equipment is provided in Annex B.

NOTE COTS semiconductor microcircuits already in use, under comparable mission profile, can provide valuable information for risk assessment and lifetime calculation.

However, the operating and thermal mission profile of COTS semiconductor microcircuits can potentially be reviewed in case of mitigation (see 4.8.3.1 and 4.8.3.2 related to mitigation of stresses by mission profile).

4.3 Lifetime requirements in mission

4.3.1 Lifetime requirements for electronic equipment in mission

The OEM obtains usually this information through the electronic equipment specification or customer requirements.

4.3.2 Lifetime requirement for COTS semiconductor microcircuit

The lifetime requirement for COTS semiconductor microcircuit in mission can be determined by the OEM from the electronic equipment life mission.

However the lifetime requirements for COTS semiconductor microcircuits can potentially be reviewed in case of mitigation (see 4.8.3.3 and 4.8.3.4, mitigation, respectively, by maintenance or redundancy).

NOTE As a first step, the lifetime requirements for COTS semiconductor microcircuits can be considered the same as the lifetime requirements for the electronic equipment.

4.4 Lifetime assessment for COTS semiconductor microcircuit based on the OCM information

4.4.1 Availability of lifetime assessment by the OCM

If the OCM specifies and supplies a COTS semiconductor microcircuit to the OEM with the expected lifetime under specific conditions, the OEM can check that the associated technical data are complete.

If the OCM's technical data are complete, the OEM keeps evidence of them.

Otherwise the OEM can itself assess the lifetime of the COTS semiconductor microcircuit (see 4.5).

Data are considered incomplete if one of the following information is missing:

- lifetime of COTS semiconductor microcircuit for x % of failed samples;
- test parameters for which the lifetime of the COTS semiconductor microcircuit has been estimated. Test parameters include test duration, number of tested samples, operating and thermal conditions.

4.4.2 Lifetime compliance

The OEM checks whether the COTS semiconductor microcircuit's expected lifetime under specific conditions provided by the OCM is relevant and acceptable for both the OEM's operating and thermal mission profiles and the mission's lifetime requirement.

If this lifetime is relevant and acceptable for its application, the OEM refers to 4.9 for editing the final report and providing recommendations with regard to the selection acceptance of the COTS semiconductor microcircuit.

If not, the OEM can reconsider the situation (see 4.8).

4.5 Lifetime assessment for a COTS semiconductor microcircuit processed by the OEM

4.5.1 Approach

In the absence of lifetime specified by the OCM for a COTS semiconductor microcircuit, the lifetime assessment can be carried out by the OEM either based on the OCM's technical data which can be available, and according to their relevance, or through a specific activity.

A partnership between the OEM and the OCM, and sometimes the foundry, can be necessary to obtain these technical data.

4.5.2 Risk analysis based on physics of failure (PoF) and the component family

COTS semiconductor microcircuits are designed with many functional blocks and technologies of transistors at silicon die level (for example I/O transistors, core transistors) that have their own kinetics of degradation. Because of this, a risk analysis is performed by the OEM to make a link between the type of semiconductor microcircuit (microprocessor, FPGA, DRAM, SRAM, flash, etc.) and the relevant failure mechanisms (EM, TDDB BEOL, TDDB FEOL, HCI, BTI, etc.) with the technological features involved (for example metal wire and transistor size).

The aim of this risk analysis is mainly to identify the relevant failure mechanism, putting aside the ones which are not likely to happen with respect to the physics of failure.

An example of risk analysis by COTS semiconductor microcircuit type is given in Annex C.

NOTE The OEM considers as many acceleration model assessments as test structures identified by the risk analysis (see 4.5.4).

4.5.3 OCM's technical data availability and relevance

Based on the semiconductor microcircuit process node qualification campaign and/or other specific tests, the OCM can determine, for a COTS semiconductor microcircuit, some reliability levels at given temperatures and extract some characteristics (for example failure and degradation mechanisms, acceleration factors) impacting the semiconductor microcircuit wear-out and hereafter the semiconductor microcircuit lifetime.

After that the OEM conducts the following tasks:

a) Collect all the technical data (for example qualification and/or raw tests results obtained under stressed conditions, failure and degradation mechanisms, acceleration models, etc.) which can contribute to the process and extrapolate the component lifetime from the OCM's tests conditions to the OEM's conditions as well as the failure mechanisms identified in 4.5.2.

b) Analyse their relevancy. In particular, if the raw test results are imported from product qualification report, check whether the test conditions are relevant enough to induce the stress corresponding to the failure mechanism described by the acceleration model. This verification is not needed if raw test results are derived from wafer foundry qualification.

c) Identify and document, according to a) and b), a credible path:

- acceleration models assessment with technical data from the original component manufacturer (see 4.5.4.1);
- acceleration models assessment conducted as a specific activity under the OEM's responsibility (see 4.5.4.2); or
- reconsideration of the choice of the COTS semiconductor microcircuit, selection of another semiconductor microcircuit reference (see 4.8.2) and restart of the process from the beginning.

NOTE As many acceleration model assessments and lifetime computations as test structures identified by the risk analysis are considered by the OEM (see 4.5.4).

4.5.4 Acceleration models assessment paths

4.5.4.1 Acceleration models assessment by the OEM with technical data from the OCM

If the technical data from the OCM are available and relevant (see 4.5.3), then the OEM can:

- either consider the acceleration models (if available) related to the failure mechanisms previously identified in 4.5.2; or
- extract the test data for defining the appropriate acceleration models.

The acceleration models will then be used into computations to determine the expected semiconductor microcircuit lifetime (see 4.6).

This approach is defined as default because the acceleration models provided by the OCM are developed specifically for the node/semiconductor microcircuit and hence include all the technological considerations.

4.5.4.2 Acceleration models assessment by the OEM as a specific activity

4.5.4.2.1 General

The OEM can make wear-out assessments when the technical data provided by the OCM are not sufficient, not relevant, are missing, not communicated, or if the acceleration models are not available.

4.5.4.2.2 Acceleration models relevant to the semiconductor microcircuit technology

Regarding the failure and degradation mechanisms identified during the risk analysis (see 4.5.2), the OEM can consider technical data (for example, tests results) and acceleration models coming from different sources, for example:

- public sources such as scientific publications;
- service providers' sources.

Nevertheless, both raw test results and acceleration models need to be appropriate to the COTS semiconductor microcircuit technology (at both back end of the line (BEOL) and front end of the line (FEOL) levels).

The OEM needs to demonstrate that all these data and acceleration models are credible and relevant.

As a consequence, the OEM carries out the following tasks:

– Get access to the BEOL and FEOL technology data including architecture, dimensions and materials. The list of technology parameters required is defined in Annex D. The technological data can be extracted by DPA or directly from the OCM data.

– Pick up or calibrate failure and acceleration models on experiment results in agreement with the technology of the COTS semiconductor microcircuit investigated. Some examples of generic acceleration models expressed by failure mechanisms are provided in Annex E.

The acceleration models will then be used in computations to determine the expected semiconductor microcircuit lifetime (see 4.6).

NOTE In service failure collection or reliability data related to the COTS semiconductor microcircuit and its technology or to a similar COTS semiconductor microcircuit and technology can help the demonstration.

4.6 Lifetime calculation of COTS semiconductor microcircuit in mission

The OEM uses the acceleration models into computations to determine the expected semiconductor microcircuit lifetime taking into account the application of the operating and thermal mission profiles including the environment and the derating conditions (see 4.2.3.2).

The OEM can refer to 4.7 to assess the results of the computation.

4.7 Lifetime compliance of COTS semiconductor microcircuit in mission

The OEM checks whether the COTS semiconductor microcircuit lifetime is acceptable with regard to the semiconductor microcircuit mission lifetime requirement (see 4.3.2).

In case of lifetime compliance, the OEM refers to 4.9 for editing the final report and the COTS semiconductor microcircuit selection can be accepted.

In case the COTS semiconductor microcircuit lifetime is not acceptable, the OEM reconsiders the situation (see 4.8).

4.8 Situation reconsideration and alternatives

4.8.1 General

If the lifetime computed for the COTS semiconductor microcircuit does not meet the lifetime requirement for the semiconductor microcircuit in mission (see 4.7) or if the COTS semiconductor microcircuit lifetime specified by the OCM is not compliant with both the semiconductor microcircuit mission profile and the lifetime requirements (see 4.4.2), the OEM can reconsider the situation and seek an alternative (see 4.8.2 and 4.8.3).

4.8.2 Semiconductor microcircuits change

The OEM has the possibility to reconsider the choice of the semiconductor microcircuit, to select another semiconductor microcircuit reference, and to restart the process from the beginning.

4.8.3 Lifetime mitigation solutions

4.8.3.1 General

Mitigation techniques can extend the COTS semiconductor microcircuit's operating life and hence the semiconductor microcircuit's lifetime.

Potential solutions to mitigate early wear-out effects are the modification of the operating and thermal mission profiles (see 4.8.3.2) or other mitigation dispositions such as the introduction of appropriate maintenance operations or redundancy actions (see 4.8.3.3 and 4.8.3.4).

The OEM needs to demonstrate the relevance of the applied mitigation solution (for example results from technical analysis, assessments and/or simulations; evolution of conditions related to the operating and thermal mission profiles or to the semiconductor microcircuit lifetime itself).

The mitigation dispositions identified in 4.8.3 are not limitative and, in any case, each one needs to be documented in the final report (see 4.9).

4.8.3.2 Mitigation of stresses induced by the operating and thermal mission profile

The mitigation by the operating and thermal mission profiles consists in decreasing the electrical and thermal stress factors by considering, if applicable, one or several of the following possibilities (non-limitative list):

- adjust temperature according to the dominant failure mechanism by carrying out for example passive and/or active cooling action at semiconductor microcircuit, electronic board, electronic equipment or system level;
- adjust the semiconductor microcircuit rate of solicitation regarding the failure mechanism;
- decrease the operating frequency;
- decrease the bias voltage.

With this lifetime mitigation, the operating and thermal mission profiles change at COTS semiconductor microcircuit level (see 4.2.3.2) and the OEM redoes a part of the process with a lifetime re-computation and lifetime compliance check (see Figure 1).

NOTE Adequate component derating, especially for voltage and temperature, can assist with the mitigation of stresses and can increase the predicted lifetime in the application. Derating standards include, for example, GEIA-STD-0008.

4.8.3.3 Mitigation by maintenance

Mitigation by maintenance can rely for example on:

– the development of embedded health monitoring techniques;

– the set up of pre-defined scheduled actions.

Mitigation by maintenance can be considered if the number of preventive maintenances n satisfies the following condition:

$$n \geq \frac{L_r}{L_c}$$

where:

L_r is the lifetime requirements for the COTS semiconductor microcircuit in mission; and

L_c is the lifetime calculation for the COTS semiconductor microcircuit in mission.

In this case, the lifetime requirements at semiconductor microcircuit level can be adjusted to the lifetime computed for the COTS semiconductor microcircuit in mission.

Hence, the OEM restarts the process from 4.3.2, considering then either 4.4.2 with regard to a COTS semiconductor microcircuit lifetime specified by the OCM or 4.7 when the lifetime has been assessed and computed by the OEM (see Figure 1).

4.8.3.4 Mitigation by redundancy

This kind of mitigation can be introduced by implementing, for example, cold redundancy at semiconductor microcircuit or electronic equipment level, or potentially at electronic board level.

Mitigation by redundancy can be considered if the number of redundancies m satisfies the following condition:

$$m \geq \frac{L_r}{L_c}$$

where:

L_r is the lifetime requirements for COTS semiconductor microcircuit in mission; and

L_c is the lifetime calculation for COTS semiconductor microcircuit in mission.

In this case, the lifetime requirements at COTS semiconductor microcircuit level can be adjusted to the lifetime computed for the COTS semiconductor component in mission.

Hence, the OEM restarts the process from 4.3.2, considering then either 4.4.2 with regard to a COTS semiconductor microcircuit lifetime specified by the OCM or 4.7 when the lifetime has been assessed and computed by the OEM (see Figure 1).

4.9 Final report

The OEM releases a final report using, for example, the template with the items mentioned in Annex F.

This report refers to all technical and demonstration data related to the COTS semiconductor microcircuit, and provides recommendations with regard to its selection acceptance.

5 Considerations with regard to semiconductor ageing level estimation for semiconductor microcircuits

During the past years, some specific techniques for monitoring semiconductor ageing have been investigated for reliability-critical applications. If these techniques are implemented by the OCM, they can be used to quantify and record the ageing level in real-time during the mission (more details provided for example in [2], [14][1]), and thereafter can be used to take adequate measures in a timely manner (for example semiconductor microcircuit replacement, dynamic voltage-frequency scaling, etc.).

However, for a COTS semiconductor microcircuit, the OEM cannot rely only on this type of function and possibility, especially without a lifetime assessment during the semiconductor microcircuit selection (by using this document, for example, and validating the relevance of the OCM ageing level estimation function). Indeed, if it turns out that the lifetime of the semiconductor microcircuit is not appropriate for the OEM's mission profile, the OEM will realize this during the mission and this will potentially be too late.

The semiconductor ageing monitoring technique and function as presented in [2] can be implemented by the OEM in an FPGA application, for example, and can be an additional source of ageing control.

NOTE This technique is not applicable for all non-programmable semiconductor microcircuits (memories, microcontrollers, microprocessors, etc.).

In any case, such semiconductor ageing monitoring technique and additional function need to be non-intrusive with regard to the operational function implemented into the semiconductor microcircuit and not lead, via their own ageing and a potential failure (for example oxide breakthrough by TDDB or EM problem) to a failure of the transistors used for the operational function (for example leakage current).

1 Numbers in square brackets refer to the Bibliography.

Annex A
(informative)

Failure and degradation mechanisms of COTS semiconductor microcircuits

By scaling technology feature sizes below 0,1 µm, current leakage, density and internal stresses (power per unit volume, electric field) within digital semiconductor microcircuits (for example SRAMs, DRAMS (SDRAMs, DDR series), flash memories (NOR logic gate, NAND logic gate), MRAM, microcontrollers, microprocessors and FPGA) have been greatly increased because the bias voltage and currents on one side, and the geometric features on the other side, have not been shrunk in a homothetic way by the same factor. As a consequence for these kinds of semiconductor microcircuits, internal electrical stresses have enhanced failure and degradation mechanisms and can impact both the reliability and operating life in the application environment.

Some failure and degradation mechanisms have been listed in Table A.1. This list is non-exhaustive with regard to semiconductor technologies and/or materials changes.

NOTE All the failure mechanisms listed in Table A.1 are triggered by the bias voltage and enhanced with temperature.

Table A.1 – Some failure and degradation mechanisms for COTS semiconductor microcircuits

Failure mechanism	Mode	Location	Catalyst factor
Electro-migration	Signals timing degradation due to the increase of the BEOL line resistivity	BEOL metal lines or interconnection	Current and high temperature
Inter/intra time dependent dielectric breakdown (TDDB BEOL)	• Increase of leakage currents • BEOL metal shortcut	• Inter-metallic BEOL oxides • Intra-metallic BEOL oxides	Bias voltage and high temperature
Gate dependent dielectric breakdown (TDDB FEOL)	Increase of leakage currents	Gate oxide	Bias voltage and high temperature
Hot carrier injection (HCI)	Signals timing degradation due to shift of transistors threshold voltage	Gate oxide (interface and volume)	Bias voltage and temperature
Bias temperature instabilities (BTI: NBTI, PBTI)	Signals timing degradation due to shift of transistors threshold voltage	Gate oxide (interface and volume)	Bias voltage and high temperature

As elements within an electronic equipment during operational usage, the semiconductor microcircuits will degrade away from their initial characteristics, and the time at which the semiconductor microcircuits fail intrinsically in the application is dependent on a complex function of a large number of factors, including technological features (size and material), deployment, environmental and application electrical stresses. Investigation of these effects in semiconductor microcircuits with geometric feature sizes below 0,2 µm has been carried out by the Aerospace Vehicle Systems Institute as part of projects AFE 17 [15] and AFE 71 [16]. Guidance on failure mechanisms and modelling is given in JEDEC JEP 122 [5] and DSIAC (formerly RIAC) publication “Physics of Failure Based Handbook of Microelectronics Systems” [11].

Derating the semiconductor microcircuit stressors can mitigate such mechanisms and can enable the improvement of both the semiconductor microcircuit reliability and its operating life capability. The derating may take several forms which include voltage derating, operating frequency reduction, part held in standby until the required reduction of power has dissipated, and environment improvement. Methods of thermal derating of semiconductor microcircuits are detailed in JEDEC JEP149 [6] and methods for determining the acceleration factors form testing are detailed in JEDEC JESD91 [9].

Standards and reference information which can be useful when addressing the wear-out requirement are: JEDEC JESD47 [8], JEDEC JESD91 [9], JEDEC JEP 122 [5] and DSIAC (formerly RIAC) publication “Physics of Failure Based Handbook of Microelectronic Systems” [11].

Moreover OCMs measure and control some of these failure mechanisms during semiconductor wafer process qualification according to JEDEC JP001 [7]. Nevertheless, currently, most OCMs control these failures mechanisms for only ten years of operation or less.

Annex B
(informative)

Example of operating and thermal mission profile for a COTS semiconductor microcircuit

Figure B.1 provides an example of thermal and operating mission profile for a COTS semiconductor microcircuit implemented in an electronic equipment located on the avionic bay of a civil aircraft.

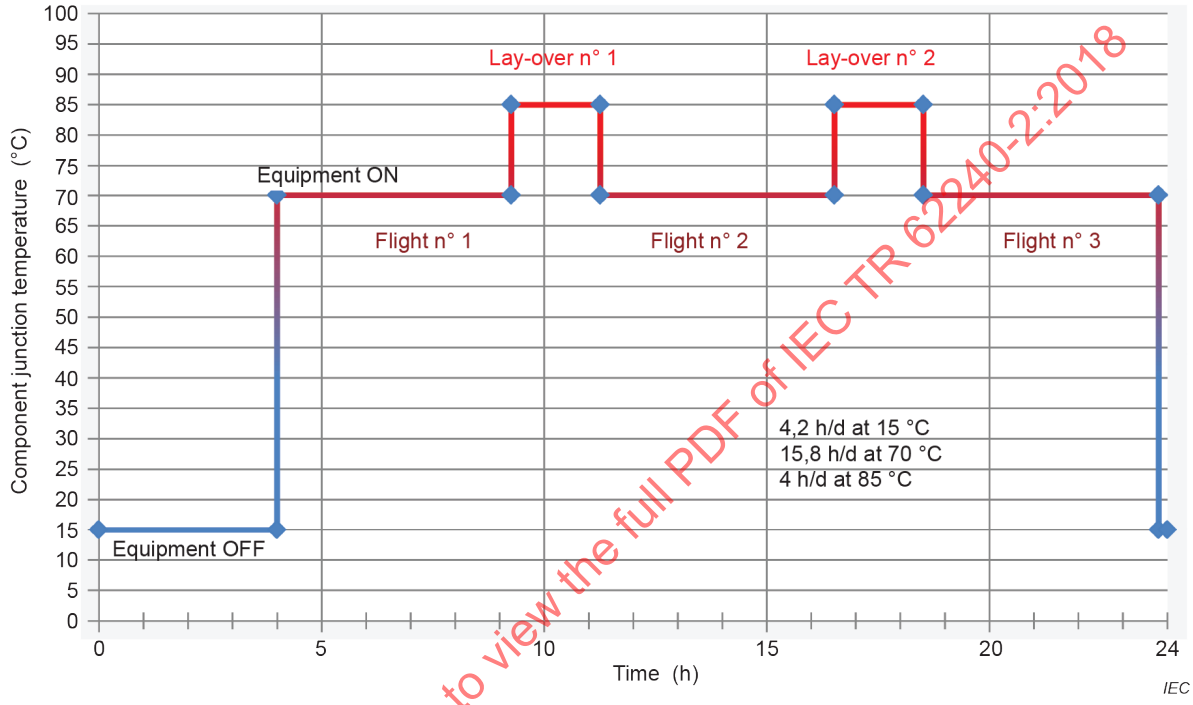

Figure B.1 – Example of thermal and operating mission profile for a semiconductor microcircuit implemented in an electronic equipment located on the avionic bay of a civil aircraft, assuming 30 °C of thermal dissipation

The conditions are:

- Electronic equipment “OFF”, semiconductor microcircuit “OFF”
  - daily operating profile: ground (4,2 h/d at 15 °C);
  - yearly operating profile: 350 days a year over 30 years.
- Electronic equipment “ON”, semiconductor microcircuit biased
  - daily operating profile: 3 flights a day (5,2 h each at 40 °C) and 2 lay-overs a day (2 h each at 55 °C);
  - yearly operating profile: 350 days a year over 30 years.

Annex C
(informative)

Risk of failure and degradation mechanisms according to the type of COTS semiconductor microcircuit

Table C.1 provides typical failure and degradation mechanisms according to the family and the structure of the COTS semiconductor microcircuits.

Table C.1 – Typical failure and degradation mechanisms according to the COTS semiconductor microcircuit family and structure

Failure mechanism	Semiconductor microcircuit structure		Semiconductor microcircuit family (< 90 nm process)				
			FPGA	Microprocessor	DRAM	Flash	SRAM
EM	Levels	Global	x	x	x	x	x
		Intermediate	x	x	NA	NA	NA
		Local	x	x	x	x	x
TDDB BEOL	Levels	Global	x	x	x	x	x
		Intermediate	x	x	NA	NA	NA
		Local	x	x	x	x (if low-k dielectrics)	NA
TDDB FEOL	I/O	NMOS	x	x	x	x	x
		PMOS	x	x	x	x	x
	Core	NMOS	x	x	NA	NA	x
		PMOS	x	x	NA	NA	x
	Capacitor	Oxide	NA	NA	x	NA	NA
HCI	I/O	NMOS	x	x	x	x	x
		PMOS	x	x	x	x	x
	Core	NMOS	x	x	x	x	x
		PMOS	x	x	NA	NA	x
BTI	I/O	NMOS	x	x	x	x	x
		PMOS	x	x	x	x	x
	Core	NMOS	x (if high-k dielectrics)	x (if high-k oxides)	NA	NA	x (if high-k dielectrics)
		PMOS	x	x	NA	NA	x

"x" means "is considered".

"NA" means "not applicable".

These typical failure mechanisms depend on lot of parameters, such as the semiconductor microcircuit family itself, semiconductor technology and process node, silicon junction structure, semiconductor microcircuit structure, interconnections, packaging, materials. Therefore, considering the evolution of the semiconductor (such as process node scaling, etc.) the importance of these parameters can change and, for example, one can either become negligible or cancel one another out. This confirms the interest of the lifetime assessment process and the method considered in this document.