TECHNICAL REPORT

IEC TR 61967-4-1

First edition
2005-02

**Integrated circuits –
Measurement of electromagnetic emissions, 150 kHz to 1 GHz –**

**Part 4-1:
Measurement of conducted emissions –
1 Ω/150 Ω direct coupling method –
Application guidance to IEC 61967-4**

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CONTENTS

FOREWORD 4

1 Scope 6
2 Normative references 6
3 Terms and definitions 7
4 Splitting ICs into *IC function modules* 9
4.1 Background 9
4.2 Benefits 9
4.3 IC function modules 9
4.4 Example matrix for splitting ICs into *IC function modules* 14
5 Workflow to perform IC EMC emission tests 15
5.1 Emission test philosophy 15
5.2 Flowchart of performing emission tests 15
6 Test configurations for *IC function modules* 16
6.1 EMC test recommendations for *IC function modules* 16
6.2 Port selection guide 16
6.3 Test networks at selected ports 18
6.4 Supply selection guide 22
6.5 Test networks at selected supplies 23
6.6 Parameter initialization of *IC function modules* for testing 24
6.7 Test parameter for performing conducted emission measurements 30
7 Test board layout recommendations 36
7.1 Common test board recommendations 36
7.2 150 Ω network on 2 layer and multi layer PCB 36
7.3 1 Ω network on 2 layer and multi-layer PCB 37
8 Test report 37

Annex A (normative) IEC 61967-4 test network modification 38
Annex B (informative) Trace impedance calculation 40
Annex C (informative) Examples for splitting ICs into *IC function modules* 42

Figure 1 – Common definition of an IC function module 8
Figure 2 – Flowchart of performing emission tests 15
Figure 3 – Test network for IC function module *line driver* 18
Figure 4 – *Symmetrical line driver* without termination (not required by bus system datasheet) 18
Figure 5 – *Symmetrical line driver* with termination required by bus system datasheet 19
Figure 6 – Test network for IC function module *line driver* 19
Figure 7 – Test network for IC function module *high side driver* 20
Figure 8 – Test network for IC function module *low side driver* 21
Figure 9 – Conducted emission measurement circuits for IC function module *supply* 23
Figure 10 – Layout recommendation 150 Ω network 36
Figure 11 – Layout recommendation 1 Ω network 37

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Figure A.1 – 150 Ω network, attenuation chart of some example capacitor values 38
Figure B.1 – Micro stripline 40
Figure B.2 – Symmetric stripline.....41
Figure B.3 – Offset stripline 41

Table 1 – Example matrix for splitting ICs into *IC function modules* 14
Table 2 – EMC test recommendations for *IC function modules*.....16
Table 3 – Test port selection table 17
Table 4 – Creating priority for a subset of *supply* modules.....23
Table 5 – *Driver* toggling definition.....24
Table 6 – Test initialization software module for *cores* containing a *CPU* 27
Table 7 –Test loop software module for *cores* containing a *CPU*.....29
Table 8 – Test procedure *driver switching noise, with CPU*.....30
Table 9 – Test procedure *driver switching noise, without CPU* 30
Table 10 – Test procedure *port internal crosstalk, with CPU*.....31
Table 11 – Test procedure *regional signal driver* supply noise, *with CPU* 31
Table 12 – Test procedure *regional signal driver* supply noise, *without CPU* 31
Table 13 – Test procedure *symmetrical line drivers, with CPU*.....32
Table 14 – Test procedure *symmetrical line drivers, without CPU* 32
Table 15 –Test procedure *high side drivers (without CPU)*.....32
Table 16 – Test procedure *low side drivers (without CPU)* 33
Table 17 – Test procedure *core supply, without CPU* 33
Table 18 – Test procedure *core to drivers* and *inputs* crosstalk, *without CPU*.....34
Table 19 – Test procedure *core supply, core with CPU*.....34
Table 20 – Test procedure *core* to *drivers* and *inputs* crosstalk, core with CPU, single *driver* or input port 35
Table 21 – Test procedure *core* to *drivers* and *inputs* crosstalk, with *CPU*, multiple *driver* or *input port* 35
Table 22 – Test procedure *oscillator* supply noise, *with CPU* 36
Table 23 – Test procedure *oscillator* supply noise, *without CPU* 36
Table A.1 – Limit frequencies of modified DC block capacitor values in 150 Ω network 39

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC EMISSIONS, 150 kHz TO 1 GHz –

Part 4-1: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method – Application guidance to IEC 61967-4

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IEC 61967-4-1, which is a technical report, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
47A/694/DTR	47A/702A/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

IEC 61967 consists of the following parts, under the general title *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz*

Part 1 General conditions and definitions

Part 2 Measurement of radiated emissions – TEM-cell method

Part 3 Measurement of radiated emissions – Surface scan method

Part 4 Measurement of conducted emissions – 1 Ω / 150 Ω Direct coupling method

Part 5 Measurement of conducted emissions – Workbench Faraday cage method

Part 6 Measurement of conducted emissions – Magnetic probe method

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
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- replaced by a revised edition, or
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INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC EMISSIONS, 150 kHz TO 1 GHz –

Part 4-1: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method – Application guidance to IEC 61967-4

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1 Scope

This technical report serves as an application guidance and relates to IEC 61967-4.The division of *IC types* into →*IC function modules* and the software modules for →*cores* with *CPU* can be used for Parts 3, 5 and 6 of IEC 61967 as well. This report gives advice for performing test methods described in IEC 61967-4 by classifying types of integrated circuits (ICs) and providing hints for test applications related to the IC type classification.

To obtain comparable results of IC emission measurements using IEC 61967-4, definitions are given which are in addition to the general conditions specified in IEC 61967-1 and IEC 61967-4. These definitions concern IC related operating modes, pins and →*ports* to be tested, test set-ups according IEC 61967-4, including description of load circuits and RF path, and IC related emission limits (or limit classes). Parts of the guidance provided by this technical report may be applicable to other parts of IEC 61967.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050(101), *International Electrotechnical Vocabulary (IEV) – Part 101: Mathematics*

IEC 60050(161:1990), *International Electrotechnical Vocabulary (IEV) – Part 161: Electromagnetic compatibility*
Amendment 2 (1998)

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 1: General conditions and definitions*

IEC 61967-2, *Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 2: Measurement of radiated emissions, TEM-cell method*[1]

IEC 61967-3, *Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 3: Measurement of radiated emissions, surface scan method*[2]

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method*

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1 In preparation.

2 To be published.

IEC 61967-5, *Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 5: Measurement of conducted emissions, Workbench Faraday Cage method*

IEC 61967-6, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 6: Measurement of conducted emissions – Magnetic probe method*

ISO 9141, *Road vehicle – Diagnostic systems – Requirements for interchange of digital information*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
analog
pertaining to the representation of information by means of a physical quantity which may at any instant within a continuous time interval assume any value within a continuous interval of values

NOTE The quantity considered may, for example, follow continuously the values of another physical quantity representing information.

[IEV 101-12-05]

3.2
core
→*IC function module* without any connection outside the IC via pins

NOTE The supply is connected via the *IC function module supply* to pins, signals to pins are connected via the *IC function module driver*.

3.3
common mode (CM) current
in a cable having more than one conductor, including shields and screens, if any, the magnitude of the sum of the phasors representing the currents in each conductor

[IEV 161-04-39]

3.4
digital
pertaining to the representation of information by distinct states or discrete values

[IEV 101-12-07]

3.5
differential mode (DM) current
in a two-conductor cable, or for two particular conductors in a multi-conductor cable, half the magnitude of the difference of the phasors representing the currents in each conductor

[IEV 161-04-38]

3.6
EMC pin type

3.6.1
global pin
signal carrier which comes from or leaves the application via a cable harness

NOTE The cable harness is an antenna for RF energy.

In general, there are series impedances (discrete components, PCB traces) and capacitances to an application's ground system in between the cable harness and the IC pin to reduce the IC pin's RF emission.

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3.6.2
local pin
signal carrier which does not leave the application via a cable harness

NOTE 1 It remains on the application PCB as a signal between two components with or without additional EMC components.

NOTE 2 In general, the PCB traces of these signals are as short as possible. Such a trace and the loop of the signal current is a smaller antenna for RF energy in comparison to the cable harness, so the ability of the antenna to radiate RF energy is smaller.

3.7
fixed function unit
FFU
functional core sub-unit of the →*IC function module 'Core'*, designed to perform one fixed function without instruction decode and execute capability

3.8
integrated circuit
IC
set of implemented →*IC function modules* in one die or package

3.9
IC type
IC with a characteristic set of functions built in

NOTE These functions are realized with →*IC function modules*.

3.10
IC function module
functional part of an IC with at least one function and its supply connection, if needed

3.10.1
passive IC function module
no supply system for function

3.10.2
active IC function module
dedicated supply connection needed for function

NOTE The supply connection is handled as a separate input/output pair as it has a dedicated EMC behavior.

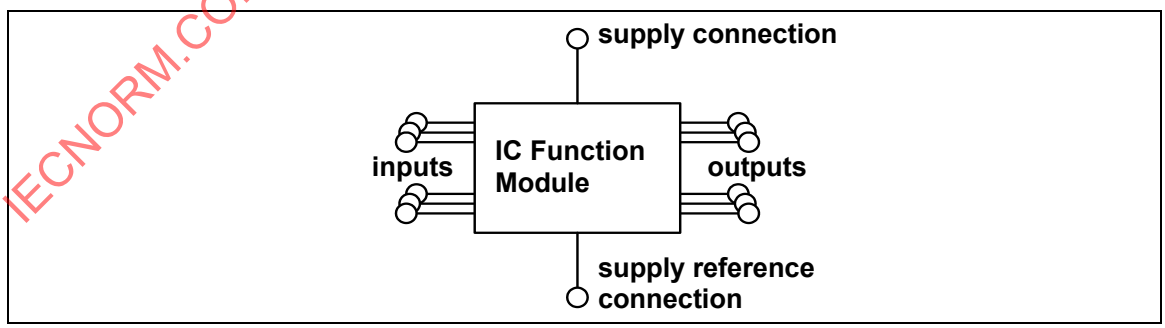

Figure 1 – Common definition of an IC function module

3.11
printed circuit board
PCB
piece of isolating material with fixed metal traces to connect electronic components

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3.12
port
functional set of minimum one *Driver* and/or minimum one *Input*

NOTE It is physically related to one →fixed function unit (FFU, see IC function module core). It is very useful to define this functional set of input and/or output IC function modules to get a common description of an interface between an IC and its circuit environment.

3.13
active port
port switched to a defined configuration or connected to *a →fixed function* unit and controlled during EMC measurements

3.14
inactive port
port switched to a defined configuration or connected to *a →fixed function* unit and remains in a defined static mode

3.15
test port
port selected for IC EMC tests

3.16
supply pin pairs
all supply voltage pins of the same supply voltage system with their related ground pin(s) of an IC supply module

4 Splitting ICs into *IC function modules*

4.1 Background

The functionality of an IC pin can be characterized as an *IC function module*. The defined set of *IC function modules* is sufficient to be combined to every kind of IC on the market. The advantage of this set of *IC function modules* is that it provides a description of EMC test set-ups and emission limit levels for each single *IC function module* with its characteristic EMC behaviour.

4.2 Benefits

– The number of test circuits is equivalent to the number of *IC function modules* independent from all IC types currently existing and future IC types (for examples for dividing actual IC types into IC function modules, see Annex C).
– The test circuit for each *IC function module* can be described precisely.
– Emission limits can be defined for each *IC function module*[3].

4.3 IC function modules

4.3.1 Port

The port is an interface between an IC and its circuit environment.

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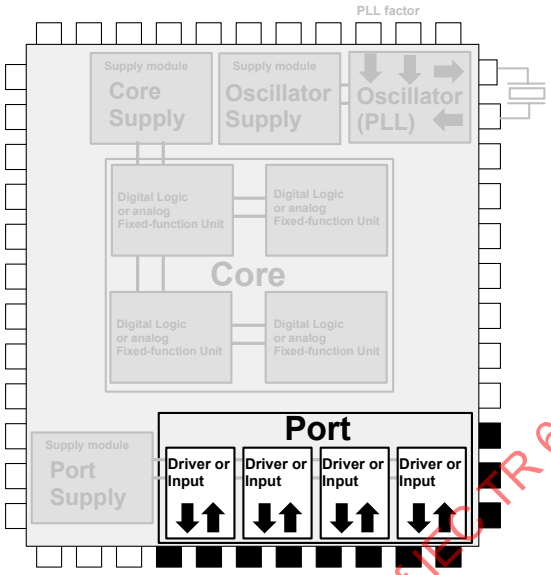
3 Limit definitions are not the target of IEC standardization. Limits have to be defined by the specific user groups, depending on application of EMC requirements in the business field concerned.

IC function modules comprising a set of at least one *IC function module 'Driver'* and/or one *IC function module 'Input'* are called *'port modules'.* If there is no driver implemented in the port or only 'local pin' defined *drivers* are implemented, the *port* is referred to as a 'local pin' type port. If 'global pin' defined *drivers* are implemented, the *port* is referred to as a 'global pin' port.



The *Port* can be a combination of eight kinds of *port modules*:

4.3.1.1 Line driver **EMC pin type: 'global'**

Drives signals into cables (signals leaving application to cable harness).

Examples: ISO 9141 outputs, LIN outputs.

4.3.1.2 Line receiver **EMC pin type: 'global'**

Receives signals from cables (signals get into application from cable harness).

Examples: ISO 9141 inputs, LIN inputs.

4.3.1.3 Symmetrical line driver ***EMC pin type: 'global'***

Drives differential signals into cables with two phase-correlated outputs (signals leaving application to cable harness).

Examples: CAN outputs, LVDS outputs.

4.3.1.4 Symmetrical line receiver ***EMC pin type: 'global'***

Receives differential signals from cables with two phase-correlated inputs cables (signals get into application from cable harness).

Examples: CAN inputs, LVDS inputs.

4.3.1.5 Regional signal driver ***EMC pin type: 'local'***

Drives signals into all other kind of lines than cables not leaving the application (application local signals).

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Examples: Digital signals: →*Ports* with inputs and outputs in 'Output mode', serial data outputs, clock outputs, status signal outputs.

Analog signals: operational amplifier outputs.

4.3.1.6 Regional Input **EMC pin type: 'local'**

Receives signals with any or discrete voltage level from all kinds of lines other than cables leaving the applications (local signals on application PCB).

Examples: Digital signals: →*Ports* with input and output modules in 'Input mode', serial data inputs, clock inputs, status signal inputs (not related to other IC function modules), interrupt inputs.

Analog signals: Input stages of operational amplifiers, input stages of ADCs.

4.3.1.7 High side driver **EMC pin type: 'global' or 'local'**

Drives power into loads. The current flows out of the driver. If driver and load are on same application PCB, the EMC pin type of the driver is 'local', if it is separated by a cable harness, the EMC pin type of the driver is 'global'.

Examples: High side switch, switched power supply current output (step down converter).

4.3.1.8 Low side driver **EMC pin type: 'global' or 'local'**

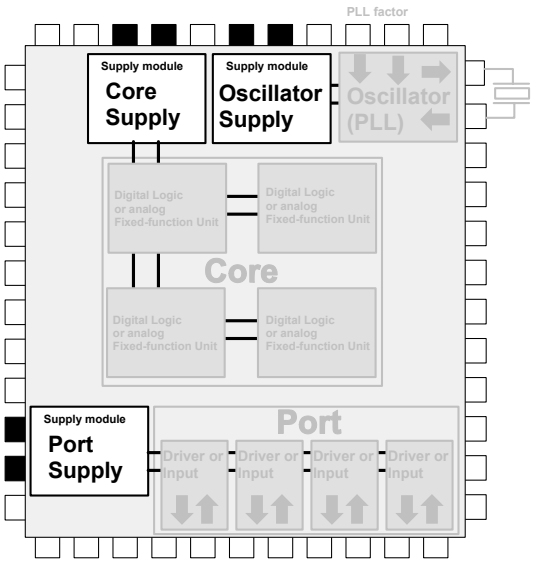
Drives power into loads. The current flows into the driver. If driver and load is on same application PCB, the EMC pin type of the driver is 'local', if it is separated by a cable harness, the EMC pin type of the driver is 'global'.

Examples: Low side switch, switched power supply current input (step up converter).

4.3.2 Supply

Distributes supply current to at least one IC function module.

An IC function module with at least one current input pin of same supply system and minimum one current output pin. It may contain active elements like voltage stabilization and/or passive elements such as internal charge buffering, current limiting series elements and other kinds of EMC filtering.



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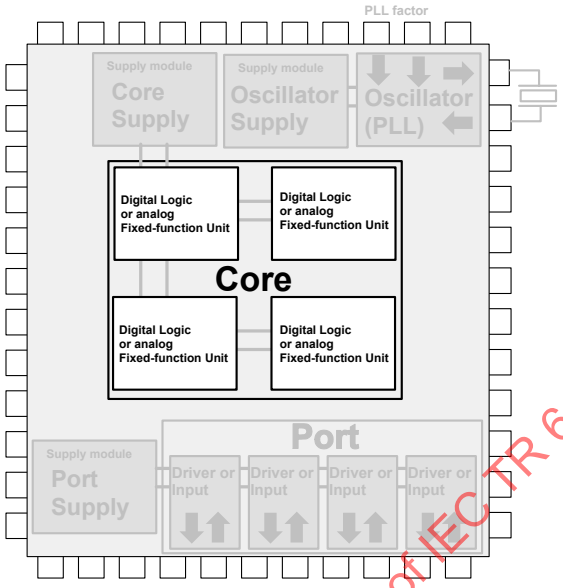
4.3.3 Core

A core is an IC function module without any connection outside of the IC via pins.

NOTE The supply is connected via the *IC function module supply* to pins. It contains a set of minimum one IC function sub-module as described below.



The core can be divided into two kinds of sub-modules:

4.3.3.1 Central processing unit (CPU)

A *CPU* decodes and executes instructions, can make decisions and jump to a new set of instructions based on those decisions.

Sub-units within the *CPU* decode and execute instructions (Sub-Unit *CU (Control Unit)*) and perform arithmetic and logical operations (Sub-Unit *ALU (Arithmetic/Logic Unit)*), making use of small number-holding areas called *registers*.

4.3.3.2 Fixed function unit (FFU)

Functional core sub-unit -> IC function module 'Core', designed to perform one analog, digital, or mixed-signal fixed function without instruction decode and execute capability

4.3.3.2.1 Digital logic fixed function unit

Functional core sub-unit, designed to perform one fixed core digital logic function without instruction decode and execute capability.

Examples: Clock distribution, Memory logic and arrays, Registers, Timer, Watchdog Timer, State Machines, Programmable Logic Arrays (PLA).

4.3.3.2.2 Analog fixed function unit

Functional core analog sub-unit, clocked or unclocked, designed to perform one fixed core analog function without instruction decode and execute capability.

Examples: Analog-to-digital-converter (ADC), Digital-to-analog-converter (DAC), Sample-and-hold-circuits, Switched capacitor filter, Charge Coupled Devices (CCDs).

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Dedicated analog fixed function unit: sensor element

A sensor element is a converter of an environmental value into an electrical value and therefore a FFU.

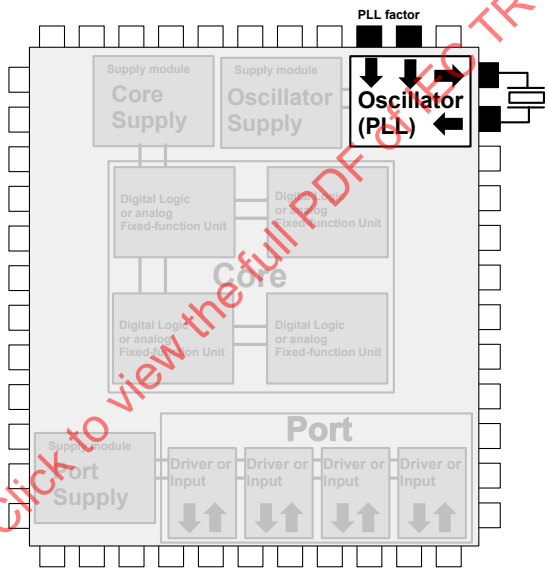
Examples: Hall sensor element for magnetic field sensing, E-field sensing, acceleration sensing. It can be combined with a precision amplifier (FFU), a supply module and a line driver to realize an IC type "sensor".

4.3.4 Oscillator

Generates a periodic signal.

NOTE This IC function module is a combination of *a fixed function module* of the *core* with *regional drivers* and *regional inputs*, but because of its EMC behaviour, it is dedicated to be defined as a separate IC function module.

A fixed-frequency oscillator may be part of a phase locked loop (PLL) circuit with voltage controlled oscillator (VCO), low pass filter, frequency divider and phase detection. All pins related to these circuits (for example divider, digital logic input pins) are part of this IC function module.



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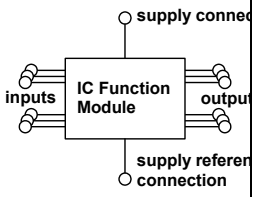
4.4 Example matrix for splitting ICs into *IC function modules*

Table 1 – Example matrix for splitting ICs into *IC function modules*

Functional module		Connection external circuit via pin									No pin			local external circuits
		Driver (outputs)					Inputs			Supplies	Core			Core/inputs
		Line driver	Symmetrical line driver	Regional signal driver	High side driver	Low side driver	Line receiver	Symmetrical line receiver	Regional input	All IC function module supplies	Digital fixed function unit	Analog fixed function unit	Central processing unit (CPU)	Oscillator
IC type examples														
Digital ICs	Microcontrollers			•					•	•	•	•	•	•
	RAM, ROM, bus drivers			•					•	•	•			
	Logic gate ICs			•					•	•	•			
Analog ICs	Operational amplifier	(•)	(•)	•					•	•		•		
	VCOs			•					•	•		•		•
	Sensor circuit	•	(•)	(•)						•		•		
Power driver	High side switch	(•)			•				•	•	•	(•)		(•)
	Low side switch	(•)				•			•	•	•	(•)		
	Bridge	(•)			•	•			•	•	•	(•)		
Interface driver	Symmetrical communication (e.g. CAN, LVDS)		•	•				•	•	•	•	(•)		(•)
	Asymmetrical communication (e.g. LIN, single wire CAN)	•		•			•		•	•	•	(•)		(•)
Voltage regulator, linear				(•)	•		•		(•)	•	(•)	(•)		
Voltage regulator, switch mode				(•)	•	(•)	•		(•)	•	(•)	(•)		(•)
ASICs		Any combination												

• = standard configuration
(•) = possible alternative configuration
NOTE For visual examples, see Annex C.

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5 Workflow to perform IC EMC emission tests

5.1 Emission test philosophy

The recommended order to test a DUT is to perform measurements from 'outside' to 'inside'. Highest priority have signals and supplies defined as EMC pin type 'global', see Definition 3.6.1.

5.2 Flowchart of performing emission tests

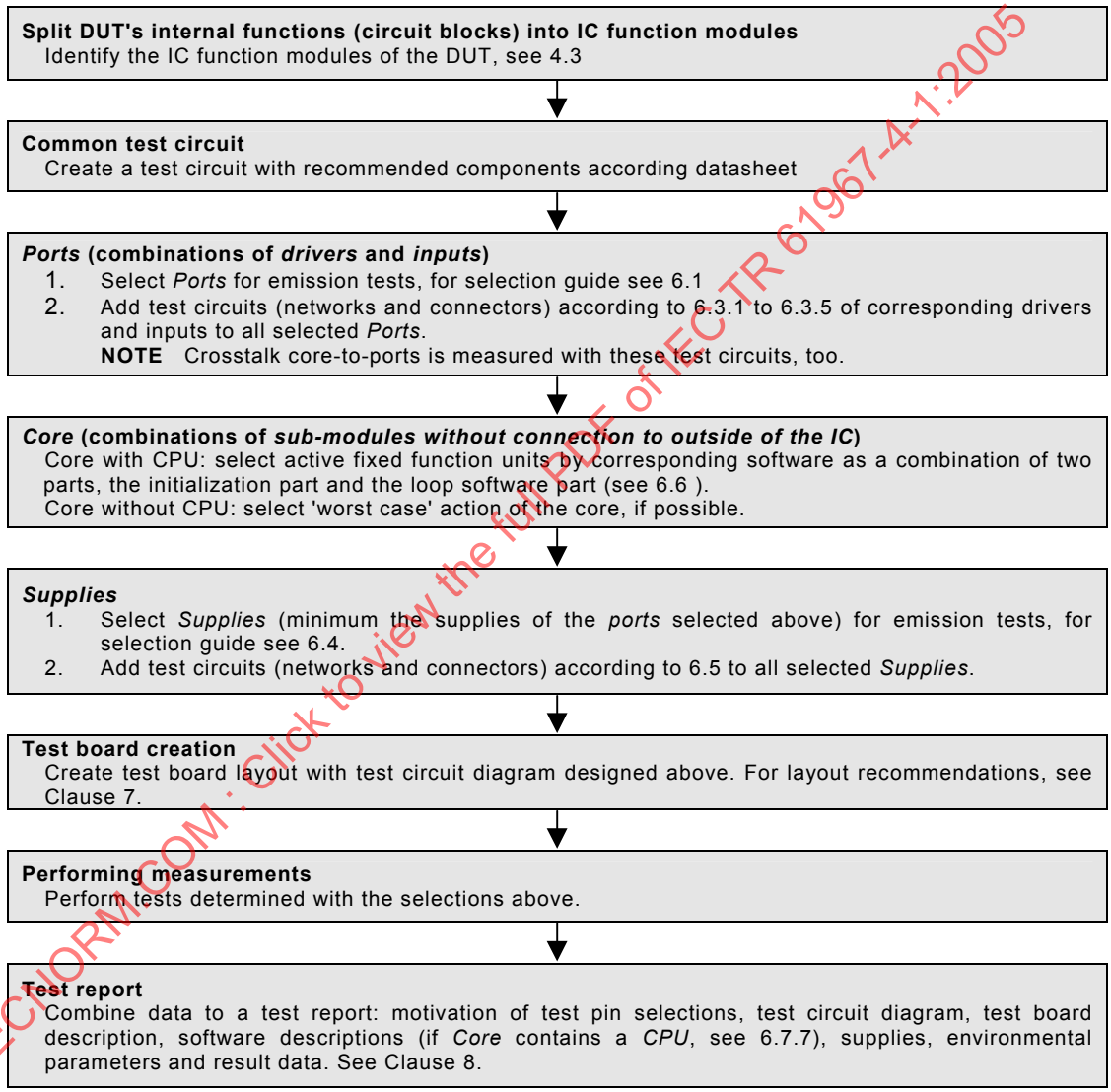

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Figure 2 – Flowchart of performing emission tests

6 Test configurations for *IC function modules*

6.1 EMC test recommendations for *IC function modules*

The following IC function modules should be tested for conducted emission:

Table 2 – EMC test recommendations for *IC function modules*

IC function module	EMC pin type		Test to be considered	Kind of coupling and emission output
	Local	Global		
Port IC function modules				
Line driver		•	Yes	Directly to driver pin
Line receiver		•	No	-
Symmetrical line driver		•	Yes	Directly to driver pins
Symmetrical line receiver		•	No	-
Regional signal driver	•		Yes	Directly to driver pin
Regional input	•		No	-
High side driver	•[1]	•[1]	Yes	Directly to driver pin
Low side driver	•[1]	•[1]	Yes	Directly to driver pin
Oscillator	•		Yes	Indirectly by crosstalk to pin
Core sub modules				
CPU	•		Yes	Crosstalk to driver pin
Digital Logic FFU	•		Yes	Crosstalk to driver pin
Analog FFU	•		No	-
Analog FFU *sensor element*	•		No	-
IC function modules supply				
All available *IC function module* supplies	•	•	Yes	Directly to supply pin
[1] EMC pin type depending on whether is a cable harness in between pin and load or not.				

6.2 Port selection guide

6.2.1 Test pin selection

At least one port should be prepared for measurement.

6.2.2 If more than one port is implemented into the IC:

The selection of a 'representative port' should be carried out according to the following priorities:

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Table 3 – Test port selection table

EMC risk	Item	Port selection	Testing kind of coupling
High	Minimum one driver of a port is EMC pin type 'global': - line driver - symmetrical line driver	All type 'global' driver pins	Direct coupling: Driver switching noise Indirect coupling: Crosstalk *driver to driver*[1]
High	Port slew rate and driver strength	Fastest port, base for selection: switch to 'multi-function' and fastest switching edges and/or select port with the highest driver capability	Driver switching noise
High	*Dedicated digital signals:*	*Examples*	Driver switching noise
	System clock outputs	CLOCK_OUTx	
	Serial communication outputs	SPI_CLOCK	
		SPI_MOSI	
	Parallel communication outputs	CLOCK	
		DATAx	
Medium	*Oscillator, digital FFU, CPU*	Use an already selected test port	Crosstalk *oscillator-to-port*

[1] More than one test network needed, for example see Figure 6, 'multiple driver port'.

For example:

In case of more than one multiple driver/input ports (e.g.: microcontroller):

Select the port, consisting of identical 4 or 8 or 16, ... I/O-drivers according following criteria:

a) The port with the shortest rising and falling time capability for emission measurements.

NOTE EMC functionality, e.g. voltage edge control, should be disabled for port selection.

b) Additionally this port should be the closest to the core of the microcontroller or where the highest crosstalk via supply and other noisy structures, for example clock distribution, is expected.

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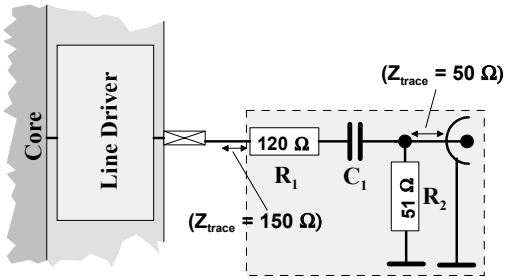
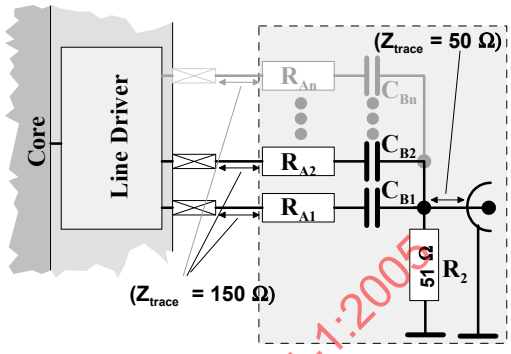
6.3 Test networks at selected ports

6.3.1 Line driver



Circuit A: Single *line driver* port



Circuit B: Multiple *line driver port

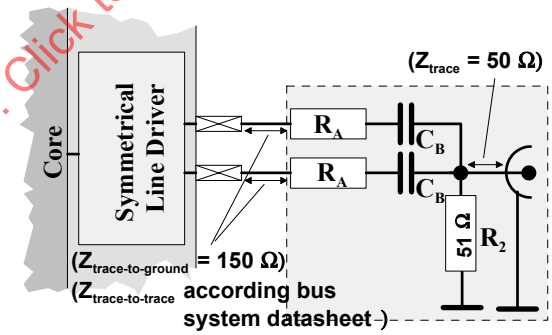
* Use circuit B, if more than one driver I to be tested simultaneously (means: all drivers are active) of a multiple *line driver* port, only suitable for sum emission measurement of all drivers.

C_1	6,8 nF or maximum load capacitance according to IC data sheet (see Annex A)
R_{A1}= R_{A2}=.. =R_{An}	$R_A\|_{\pm 5\%} = 120\Omega \cdot n$ *n* = number of *line drivers* Select a resistor according resistor standard set within the tolerance of 5 %
C_{B1}= C_{B2}=.. = C_{Bn}	$C_B\|_{\pm 5\%} = \frac{C_1}{n}$ *n* = number of *line drivers* Select a capacitor according to capacitor standard set within the tolerance of 5 %

Figure 3 – Test network for IC function module *line driver*

6.3.2 Symmetrical line driver

6.3.2.1 Bus system with separate termination*



CB_{1B}	6,8 nF or maximum load capacitance according to IC data sheet (see Annex A)	
RB_{AB}	Common bus systems	240 Ω
	Deviant definition: CAN	120 Ω
	NOTE The resistance matching tolerance shall be better than $10T^{-3T}$	
CB_{BB}	Common bus systems	6,8 nF
	Deviant definition: CAN	4,7 nF
	NOTE The impedance of both capacitors CB shall be small compared to RA, the matching tolerance may be not so tight as with the resistors. By default for CB a capacitance matching tolerance of better than 10-2 is sufficient.	

* Termination not part of the test network, but may be needed for the symmetrical line driver.

Figure 4 – *Symmetrical line driver* without termination (not required by bus system datasheet)

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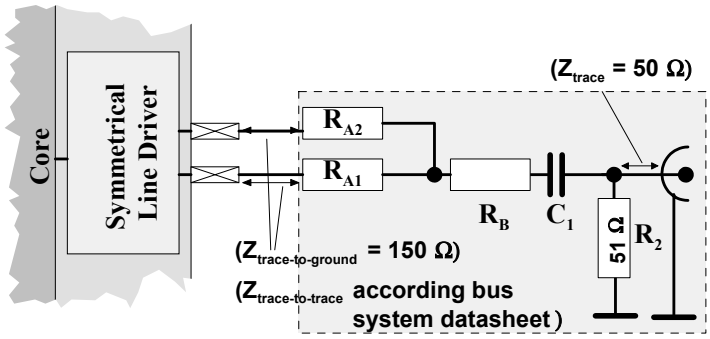
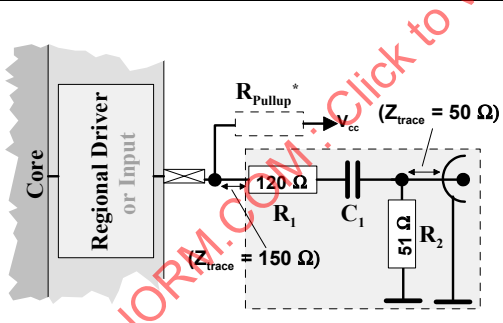
6.3.2.2 Bus system with termination used for test network



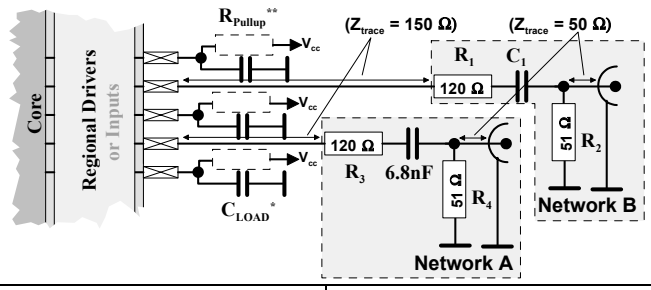
C_1	6,8 nF or maximum load capacitance according IC data sheet (see Annex A)		
R_{A1} = R_{A2}	Termination according bus system datasheet to the symmetrical star point (this point has no resulting current to reference ground, if there is no common mode current on lines)	**Examples:**	
		Bus system	R_{Ax}
		High speed CAN	30 Ω
		LVDS	50 Ω
		Airbag squib	e.g. 1 Ω
R_B	$R_B\|_{\pm 5\%} = 125\ \Omega - \frac{R_A}{2}$ Select a resistor according resistor standard set within the tolerance of 5 %	**Examples:**	
		Bus system	R_B
		High Speed CAN	110 Ω
		LVDS	100 Ω
		Airbag squib	130 Ω

Figure 5 – *Symmetrical line driver* with termination required by bus system datasheet

6.3.3 Regional signal driver



Single driver port



Network A	*Network B*
static output tests	toggle output tests

Multiple driver port, minimum test configuration

C_1, C_{Load}	6,8 nF or maximum load capacitance according IC data sheet (see Annex A)
R_{Pullup}	Digital signal: according IC data sheet, if it is needed for external pull up (default 3 300 Ω) at IC function module *input* Analog signal: signal connection to functional required circuit

Figure 6 – Test network for IC function module *line driver*

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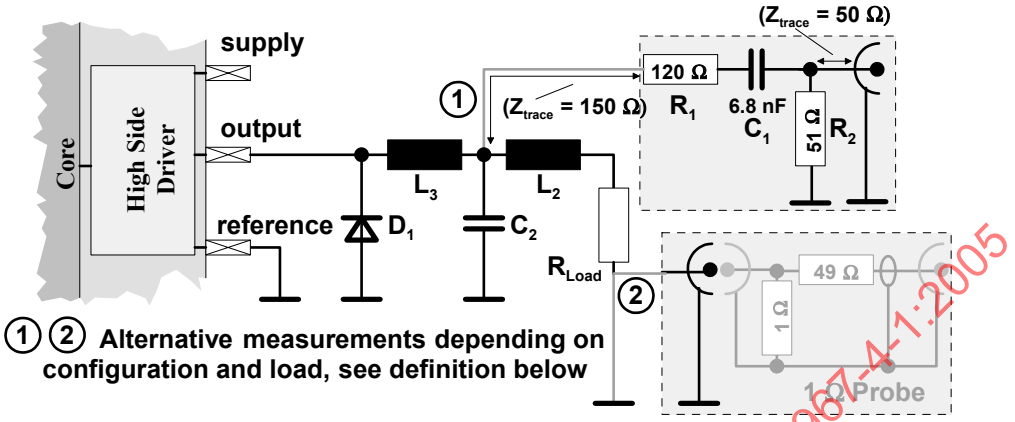
6.3.4 High side driver



Setup component variation				
Item	***Value***	***Placement depending on circuit type***		
		High side driver circuit	***Linear voltage regulator circuit***	***Switched mode power supply circuit***
L_{2}	5 µH	•	•	•
L_{3}	acc. IC data sheet	Shorted	Shorted	•
D_{1}	acc. IC data sheet			•
C_{2}	acc. IC data sheet		•	•
R_{Load}	According I_{mes}	•	•	•
		$I_{mes} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{ON150}}}$ (ΔT = 65 K, $I_{mes} \leq$ 10 A)	I_{mes} = 80% of I_{nom}	I_{mes} = 80% of I_{nom}
Test network	$R_{Load} \leq$ 30 Ω	1	1	1
	R_{Load} > 30 Ω	DC load current: 1 PWM load current: 2	1	1

Figure 7 – Test network for IC function module *high side driver*

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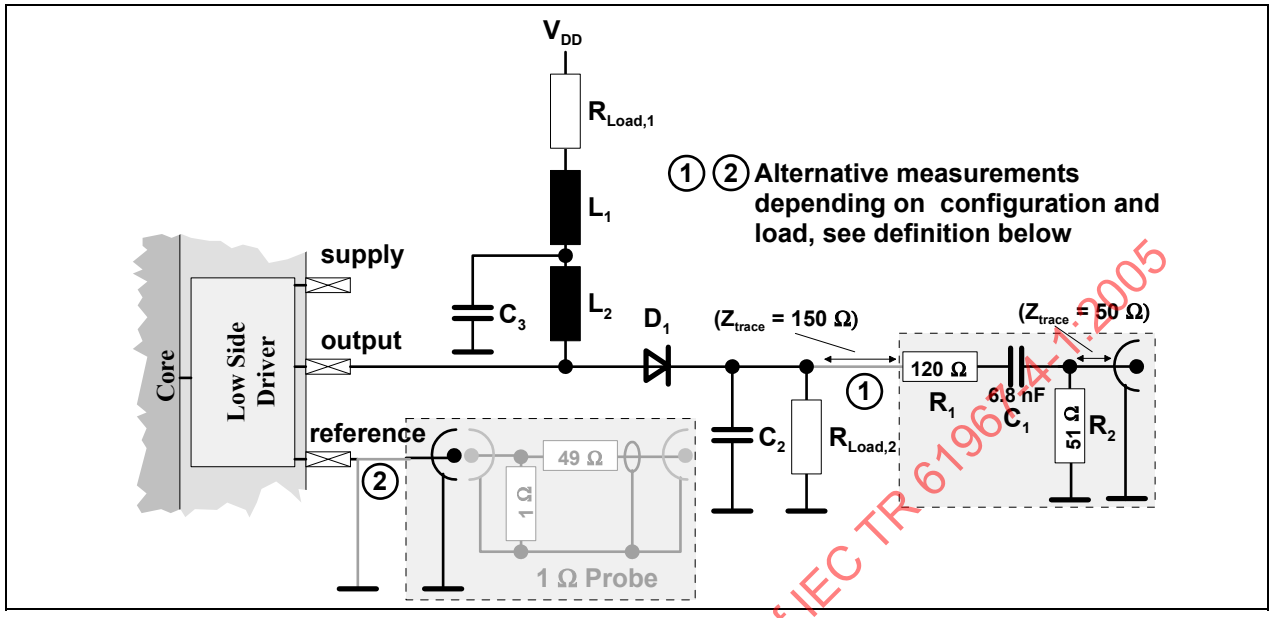
6.3.5 Low side driver



Setup component variation			
Item	***Value***	***Placement depending on circuit type***	
		Low side driver	***Boost converter***
C_2	acc. IC data sheet		•
C_3	acc. IC data sheet		•
L_1	5 µH	•	Optional
L_2	acc. IC data sheet	Shorted	•
D_1	acc. IC data sheet	Shorted	•
$R_{Load,1}$	According I_{mes}	•	Shorted
		$I_{mes} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{ON150}}}$ (ΔT = 65 K, $I_{mes} \leq$ 10 A)	
$R_{Load,2}$	According I_{mes}		•
			I_{mes} = 80 % of I_{nom}
Test network	$R_{Load} \leq$ 30 Ω	1	1
	R_{Load} > 30 Ω	DC load current: PWM load current:	1

Figure 8 – Test network for IC function module *low side driver*

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6.4 Supply selection guide

All supply pin pairs related to the supplied *IC function module* should be tested for conducted emission.

If decoupling capacitors are needed for functionality, they have to be added to the test circuit according to EMC PCB layout recommendations.

NOTE 1 If the number of supply voltage input pins is higher than the number of ground pins, the related ground pin for each supply voltage input pin should be shown in the result documents with an IC functional block/supply rail diagram. The related ground pin is the lowest impedance current path for the supply voltage.

NOTE 2 If more than one supply pin pair is connected internally, the IC supply concept should be shown in the result documents with an IC functional block/supply rail diagram.

All available supply voltage systems should be measured in 'worst case' operation mode.

Selection guide for test method variations:

There are four kinds of conducted emission measurement methods on supply pins:

Configuration A: 1 Ω method to measure the sum current in the common ground path method (Figure 9, Configuration A)

Configuration B: 150 Ω method to measure the sum disturbance voltage at all shorted supply input pins of one supply system (Figure 9, Configuration B)

Configuration C: 150 Ω method to measure the sum disturbance voltage at dedicated and shorted supply input pins of one supply system (Figure 9, Configuration C)

Configuration D: 150 Ω method to measure the disturbance voltage at each single supply input pin (Figure 9, Configuration D)

Use the 1 Ω method, if a sum current measurement is sufficient for characterizing the DUT. It is sufficient, if the result show emissions within a defined noise range. The definition of the allowed noise range depends on the kind of application.

NOTE 3 The reason for the used method should be mentioned in the test report. Test PCB layout recommendations for the conducted emission method can be found in Clause 7.

Each voltage input of one voltage supply system (same pin name, same IC function module *supply*) should be tested, if interconnection to a common supply line is 'electrically long'[4]. They have to be measured with a sum test point, if they can be connected in an 'electrically short'[5] way.

If a subset of the available number of *supply* modules have to be defined for reducing the amount of tests, choose the subset according following priority:

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4 'electrically long': If a trace is longer than the 20th part of the highest measuring frequency's wavelength. The factor '20' is a commonly used 'rule of thumb' considering wave guide in the dielectric PCB material

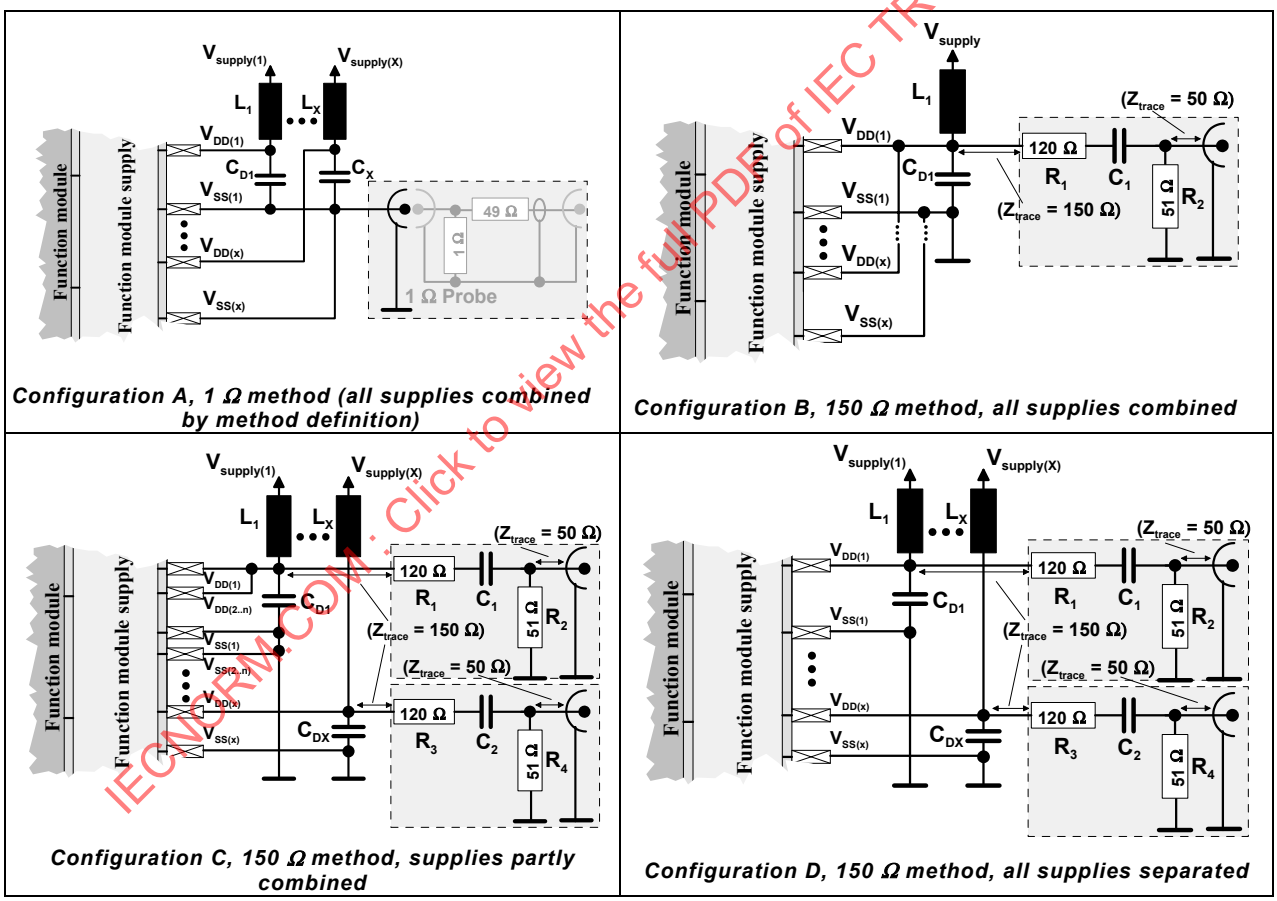
5 'electrically short': Trace shorter than $\frac{\lambda_{\text{highest test frequency}}}{20}$, see footnote above.

Table 4 – Creating priority for a subset of *supply* modules

Supplied IC function module	EMC risk
Oscillator	High
Core with *CPU*	High
Digital, clocked *core* without *CPU*	High
Ports containing 'global' *drivers*	High
Digital, unclocked *core* without *CPU*	Medium
Ports containing *regional drivers*	Medium
Analog *core* without *CPU*	Low

6.5 Test networks at selected supplies

Additionally to IEC 61967-4, at 150 Ω networks a 5 µH coil for supply impedance fixing is added:



Configuration A, 1 Ω method (all supplies combined by method definition)

Configuration B, 150 Ω method, all supplies combined

Configuration C, 150 Ω method, supplies partly combined

Configuration D, 150 Ω method, all supplies separated

Item	Value
$C_{D1}..C_{Dn}..C_{Dx}$	Supply decoupling capacitor acc. IC data sheet
$L_1..L_n..L_X$	5 µH independent of load current (no saturation effects)

Figure 9 – Conducted emission measurement circuits for IC function module *supply*

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6.6 Parameter initialization of *IC function modules* for testing

6.6.1 General port parameter definitions

Common *driver* output configuration

a) If no CPU is available:

If test pin is configurable, 'worst case' configuration should be used.

b) If a CPU is available:

All tested outputs with probing point must be configurable as:

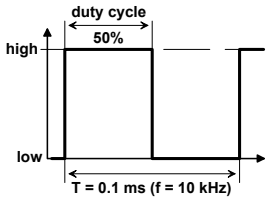
– static high
– static low
– toggling

All tested outputs without probing point must be configurable as toggling output.

Toggling outputs must be configurable to:

- Maximum possible toggling frequency related to the driving FFU according following definition:

Table 5 – *Driver* toggling definition

Kind of driving FFU and its output driver	Test toggling definition
Register output, CPU controlled	
System clock output	f = system frequency = $f_{max.}$, duty cycle: as fixed by FFU
Communication clock output	$f = f_{max.\ data\ rate}$ duty cycle: as fixed by FFU
Communication data output	$f = f_{max.\ data\ rate}$ Duty cycle: changing port pattern *'0101..'* to *'1010..'* and vice versa, if possible

- Various driver strengths and slew rates (if provided).

  In case of EMC improvement by controlling the rising and falling times perform several tests:

  Recommended: disable the improvement and

  optionally: enable it on for additional measurements.

Multiple driver and/or inputs port pin configuration

Three types of port pins are defined:

i) Input only:

to avoid floating, an internal or external pull up resistor is required.

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ii) Output without probing point:

Controlled by CPU: can be used for port toggle tests or remain static high if unused.
Connected to FFU: controlled by active FFU

iii) Output with probing point:

Must be connected to the adaptation network shown in IEC 61967-4 and therefore cannot be used as input or high speed output, if controlled by CPU.

All pins not used for testing have to be inactive (not toggling or floating), if controlled by CPU, else inactive by inactive FFU.

6.6.2 Test software (set of instructions) definitions for ICs containing a *core* with CPU

The software takes high influence on the emission level. It should include all functions which are necessary to operate different FFUs aiming at maximum functional and speed performance of the investigated IC type.

The following list describes how the software should be structured. Various *fixed function units* (*FFU*) and their corresponding input and output signals (e.g. RxD, TxD signals of CAN *FFU*, *FFU* analog-to-digital converter (ADC)) on the micro-controller must be able to be switched OFF/ON.[6] This can be realized for example by using an x-bit DIP switch on the PCB or by reloading new software.

All these features shall be implemented on board and by software, but not all combinations of measurements are recommended.

Details of the software are described below.

6.6.2.1 Common test pattern definitions

a) Inactive ports

Inactive ports should be switched to a non-toggling and non-floating mode.

b) Test loop time

The emission measurement dwell time should be, as a minimum, equal to the test software loop duration (see 6.6.2.3). (Taken from IEC 61967-1: the spectrum analyzer sweep period should be at least three orders of magnitude smaller than the software loop execution time (for example, sweep = 6 s, software loop ≤ 6 ms).)

c) System clock

The system clock is the internally used clock for data processing. It is generated by the *IC function unit oscillator* containing, as a minimum, a basic oscillator, optional a phased locked loop (PLL), voltage controlled oscillator (VCO) and a configurable clock tree divider and frequency multiplier. Measurements should use the maximum specified internal clock frequency while choosing maximum resonator frequency, if configurable. The resonator frequency, PLL multiplying factor and divider settings shall be documented.

d) Clock outputs

Drivers to distribute clock signals to external circuits are characteristically designed to drive a defined number of clock inputs. These drivers have a high EMC emission potential and should be switched at a maximum frequency and strongest driver strength mode. The clock outputs will be selected as active ports later.

e) Non-used fixed function units

Non-used *fixed function units* shall be disabled by software.

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6 The *fixed function unit*, its inputs and output signal drivers for interfacing with external circuits are called 'Core peripheral' in the microcontroller literature.

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f) Driver emission test

Measurements at drivers in static mode concern either switching noise of adjacent toggling drivers or core noise crosstalk from internal activity without toggling drivers.

g) I/O supply voltage

If several supply voltages are possible, the highest voltage shall be applied.

Recommendation:

Program (CPU) start Indication

A flashing LED indicating proper program start is driven by the test software for a short time after 'reset' signal release.

An overview of recommended tests and proposals for additional tests (for more detailed analysis) are given in the following part of this clause.

6.6.2.2 *IC* configurations by software and software modules for *cores* containing a *CPU*

In the following Tables 6 and 7, a set of software modules are described. Table 6 lists different initialization software modules. Each of these software modules arranges the IC with a *CPU core* to a defined emission test configuration described in the first three columns. Table 7 give a set of loop software modules which are running after initialization combined with one configuration described in Table 6.

NOTE Decisions made to realize the test software should be mentioned in the test report.

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Table 6 – Test initialization software module for *cores* containing a *CPU*

Emission configuration module			Description and definition of test initialization software module	
Number	**Name**	**Short description**		
C1	**Reference**	*'Worst case' setting*	System clock:	Frequency = f_{max}
			CPU:	Active
			FFUs:	All *fixed function units* active, *if available:* system clock output active
			Active ports:	All multifunction ports switched to FFU function
				Fastest slew rate of drivers
			Inactive ports:	All other ports
			Memory access:	Choose the memory access for the loop software module with highest emission potential (*high, medium, low*) available, for example:
				High Synchronous access from external memory (burst mode)
				Medium Asynchronous access from external memory
				Low Internal access from on-chip memory
C2	**1**	*Program execution with synchronous bus access/ system clock*	System clock:	Frequency = f_{max}
			CPU:	Active
			FFUs:	All *fixed function units* inactive, except the memory interface
			Active ports:	Buses
				Bus clock (system clock output active)
				Fastest slew rate of drivers
			Inactive Ports:	All other ports
			Memory access:	Memory access for the loop software module: Synchronous access from external memory (burst mode)
C3	**2**	*Program execution with asynchronous bus access/ system clock*	System clock:	Frequency = f_{max}
			CPU:	Active
			FFUs:	All *fixed function units* inactive, except the memory interface
			Active ports:	Buses
				fastest slew rate of drivers
			Inactive ports:	All other ports
				Bus clock (system clock output inactive)
			Memory access:	Memory access for the loop software module: asynchronous access from external memory
C4	**3**	*On-chip execution without system clock output*	System clock:	Frequency = f_{max}
			CPU:	Active
			FFUs:	All *fixed function units* inactive
			Active ports:	None
			Inactive ports:	All ports (buses and all other ports)
				Bus clock (system clock output inactive)
			Memory access:	Memory access for the loop software module: Internal access from on-chip memory

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Table 6 *(continued)*

Emission configuration module			Description and definition of test initialization software module
Number	**Name**	**Short description**	
C5	**Driver emission**	*Driver slew rate test*	System clock: Frequency = f_{max} CPU: Active FFUs: All *fixed function units* **in**active, except the FFU corresponding to a tested driver (if system clock output is available, its test is recommended) Active ports: Driver slew rate switched to I. Recommended**:** Fastest slew rate II. Optional**:** Slower slew rates Inactive ports: All other ports Memory access: Choose the memory access for the loop software module with **lowest** emission potential (*low, medium, high*) available, for example: *Low* Internal access from on-chip memory *Medium* Asynchronous access from external memory *High* Synchronous access from external memory (burst mode)
C6	**Oscillator**	*Idle (oscillator) mode*	System clock: Frequency = f_{max} CPU: Inactive ('wait' mode, 'hold' mode), if available FFUs: All *fixed function units* functionally **in**active and **un**clocked Active ports: None Inactive ports: All ports Memory access: Memory access for the loop software module: None
C7	**Clock tree**	*Active clock tree mode*	System clock: Frequency = f_{max} CPU: Maximum clock tree frequency in clock tree distribution Inactive ('wait' mode, 'hold' mode), if available FFUs: All *fixed function units* clocked, but functionally **in**active Active ports: None Inactive ports: All ports Memory access: Memory access for the loop software module: None
C8	**Single FFU**	*Test single FFU*	System clock: - Frequency = f_{max} CPU: - Minimum required activity FFUs: - All *fixedfunctioN units* **in**active, except the FFU under investigation Active ports: - Controlled ports by FFU under investigation Inactive ports: - All other ports Memory access: - Choose the memory access for the loop software module with lowest emission potential (*low, medium, high*) available, for example: *Low* Internal access from on-chip memory *Medium* Asynchronous access from external memory *High* Synchronous access from external memory (burst mode)

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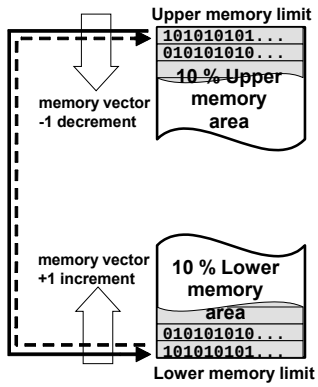
Table 6 *(continued)*

Emission configuration module			Description and definition of test initialization software module
Number	**Name**	**Short description**	
C9	*Reduced system frequency*	*On-chip execution at reduced system frequency*	System clock: - Frequency < f_{max} Combined with configuration modules C1..C8
NOTE 1 The measurement should start after finishing the initialization. NOTE 2 This table may be extended by further tests agreed between the customer and IC supplier.			

6.6.2.3 Test loop software module for *cores* containing a *CPU*

Table 7 –Test loop software module for *cores* containing a *CPU*

Emission software module		Description and definition of test loop software module	
Number	**Short description**		
S0	*Idle*	None	
S1	*Fastest instruction loop*	Label: jump(unconditional) label	
S2	*RAM copy*	Copied data range is equal or more than 10% of available RAM. Data pattern is alternating $AA.. and $55.. (length depending on data bus width) in consecutive RAM access. Source memory area and destination memory area should differ by the maximum number of address bits	
S3	*Driver output action*	Toggling driver outputs	
S4	*IEC increment*	(Taken from IEC 61967-1, Annex B): "This simple routine implements a counter function using a single 8-bit port. Every 100 µs, the port output is incremented or decremented. After 10 count cycles (256 ms) an LED output is complemented. This will provide a blinking light indication with a frequency of about 2 Hz. For consistency, equivalent loop times should be maintained."	
S5	*FFU dedicated software*	CPU runs at minimum required activity for FFU controlling, target is autonomous running mode of the FFU under investigation. All FFU parameters: Adjust to EMC 'worst case' condition	
NOTE Take care of software loop times according emission measurement dwell time.			

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6.7 Test parameter for performing conducted emission measurements

6.7.1 Ports: line drivers and regional signal drivers

6.7.1.1 Emission propagation path *driver switching noise*

6.7.1.1.1 Selection of test network

Single driver outputs:

Step by step all equipped *driver* outputs should be tested for conducted emission.

Multiple driver/input ports (e.g. microcontroller):

Step by step all *driver* outputs should be tested for conducted emission.

6.7.1.1.2 Test procedure

– Test software, if a *CPU* is implemented in *core* module

The following conducted emission measurement sequence should be performed:

Table 8 – Test procedure *driver switching noise, with CPU*

Test name	Test pin	Test software	
		Recommended	Optional
DRIVER_EDGE	**Toggle**	**C5-S3**	-

– *Core* without *CPU*

The following conducted emission measurement sequence should be performed:

Table 9 – Test procedure *driver switching noise, without CPU*

Test name	Test pin	Test condition driving FFU	
		Recommended	Optional
DRIVER_EDGE	**Toggle**	**FFU in EMC 'worst case' parameters, (e.g. with f_{max})**	-

6.7.1.2 Emission propagation path *port internal crosstalk*

6.7.1.2.1 Selection of test network

Only multiple driver/input ports (e.g. microcontroller):

Step by step all *driver* outputs equipped with Network B (see Figure 6) should be tested for conducted emission.

6.7.1.2.2 Test procedure

– Test software, if a *CPU* is implemented in *core* module

The following conducted emission measurement sequence should be performed:

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Table 10 – Test procedure *port internal crosstalk, with CPU*

Test name	Test port			Test software	
	Loaded pins*	Test pin	Unloaded pins	Recommended	Optional
IO_SUPPLY_LOW	Toggle	**Low**	High	**C5-S3**	-
IO_SUPPLY_HIGH		**High**			
IO_SUPPLY_INPUT*	Toggle	**Input**	High		
DRIVER_EDGE	Input	**Toggle**	Input		
* Additional test, if an *input* within a port is to be tested.					

6.7.1.3 Emission propagation path *supply*

6.7.1.3.1 Selection of test network

The supply pin(s) related to the *supply module* of the *driver* should be tested for conducted emission.

6.7.1.3.2 Test procedure

– *Core* with *CPU*:

The following conducted emission measurement sequence should be performed (if IC configuration available):

Table 11 – Test procedure *regional signal driver* supply noise, *with CPU*

Test name	Related *port*	Test software	
	Driver action	Recommended	Optional
DRIVER_SUPPLY	**Toggle**	**C5-S3**	-

– *Core* without *CPU:*

The following conducted emission measurement sequence should be performed:

Table 12 – Test procedure *regional signal driver* supply noise, *without CPU*

Test name	Related *port*	Test condition of *IC function module*	
	***Driver* action**	Recommended	Optional
DRIVER_SUPPLY	**EMC 'worst case' action**	***IC function module* with EMC 'worst case' parameters**	-

6.7.2 Ports: Symmetrical line drivers

6.7.2.1 Selection of test network

Step by step all equipped *driver* outputs should be tested for conducted emission.

6.7.2.2 Test procedure

– Test software, if a *CPU* is implemented in *core* module

The following conducted emission measurement sequence should be performed:

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Table 13 – Test procedure *symmetrical line drivers, with CPU*

Test name	Test pin	Test software	
		Recommended	Optional
SYM_DRIVER_CM	Toggle	C5-S3	-
NOTE Network depending on termination requirements, see 6.3.2.			

– Core without CPU

The following conducted emission measurement sequence should be performed:

Table 14 – Test procedure *symmetrical line drivers, without CPU*

Test name	Test pin	Test condition driving FFU	
		Recommended	Optional
SYM_DRIVER_CM	Toggle with f_{max}	FFU in EMC 'worst case' parameters	-
NOTE Network depending on termination requirements, see 6.3.2.			

6.7.3 Ports: high side driver – Emission propagation path driver switching noise and supply

6.7.3.1 Selection of test network

The test network is predefined by the load current, see Figure 7.

6.7.3.2 Test procedure

Table 15 –Test procedure *high side drivers (without CPU)*

Test variation depending on circuit type		High side driver circuit			Linear voltage regulator circuit	Switched mode power supply circuit
Maximum output	Test mode	DC ON			DC ON	80% power
	Test current	$I_{mes} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{ON150}}}$ (ΔT = 65 K, $I_{mes} \leq$ 10 A)			80% load current	80% load current
Minimum output	Test mode	–			–	Open load/ minimum load current
Special tests	Test mode	PWM			–	–
		Parameter	–	–		
		f_s	–	–		
		Duty cycle	–	–		
	Test current	$I_{mes} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{ON150}}}$ (ΔT = 65 K, $I_{mes} \leq$ 10 A)			–	–

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6.7.4 Ports: Low side driver

6.7.5 Emission propagation path driver switching noise and supply

6.7.5.1 Selection of test network

The test network is predefined by the load current, see Figure 8.

6.7.5.2 Test procedure

Table 16 – Test procedure *low side drivers (without CPU)*

Test modes	Detail description		
DC On	–		
DC Off / Standby	–		
PWM	**Parameter**	**Value**	**Examples**
	f_s	Typical	100 Hz, 10 kHz, 100 kHz
	Duty cycle	50%	–

Output	Current during test
Static output	$I_{mes} = \sqrt{\frac{\Delta T}{R_{th} \cdot R_{ON150}}}$ (ΔT = 65 K, $I_{mes} \leq$ 10 A)
PWM output	

6.7.6 *Core* without *CPU*, containing only fixed function units

6.7.6.1 Emission propagation path *core supply*

6.7.6.1.1 Selection of test network

The supply pin(s) related to the *supply module* of the *core* should be tested for conducted emission.

6.7.6.1.2 Test procedure

The following conducted emission measurement sequence should be performed:

Table 17 – Test procedure *core supply, without CPU*

Test number		*Test condition FFUs*	
		Recommended	**Optional**
CORE_SUPPLY		See note	–
NOTE The IC should be active with all functions in a 'worst case' condition. If the set of functions of the IC could vary by input parameters, the test set-up must be able to realize the 'worst case' of emission.			

6.7.6.2 Emission propagation path *crosstalk core* to *drivers* and *Inputs*

NOTE Core crosstalk and port supply coupling should be sufficiently tested at *active ports*.

6.7.6.2.1 Selection of test network

Select the driver, where the highest emission of the *fixed function module core* is expected. The reason for this selection should be stated in the test report.

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6.7.6.2.2 Test procedure

The following conducted emission measurement sequence should be performed:

Table 18 – Test procedure *core to drivers* and *inputs* crosstalk, *without CPU*

Test number		*Test condition FFUs*	
		Recommended	**Optional**
CORE_SUPPLY		See note	–
NOTE The IC should be active with all functions in a 'worst case' condition. If the set of functions of the IC could vary by input parameters, the test set-up must be able to realize the 'worst case' of emission.			

6.7.7 Core with CPU

6.7.7.1 Emission propagation path *core supply*

6.7.7.1.1 Selection of test network

The supply pin(s) related to the supply module of the *core* should be tested for conducted emission.

6.7.7.1.2 Test procedure

The following conducted emission measurement sequence should be performed:

Table 19 – Test procedure *core supply, core with CPU*

Test number		Test software	
		Recommended	**Optional**
CORE_SUPPLY		**C1-S2**	If available, 'worst case' of: C2-S2, C3-S2, C4-S2

6.7.7.2 Emission propagation path *crosstalk core* to *drivers* and *inputs*

6.7.7.2.1 Selection of test network

The emission of the core is measured indirectly by a crosstalk measurement through IC function modules *drivers* and *inputs*. This measurement is done in combination with testing *drivers*.

If more then one port is equipped as a test port, select the port closest to core according floorplan (see Table 3).

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6.7.7.2.2 Test procedure – Single driver and/or input port

The following conducted emission measurement sequence should be performed:

Table 20 – Test procedure *core* to *drivers* and *inputs* crosstalk, core with CPU, single *driver* or input port

Test name	Test pin (if output)	Test software	
		Recommended	Optional
CT_CORE_IO_LOW	Low	C1-S2	If available, 'worst case' of: C2-S2 C3-S2 C4-S2
CT_CORE_IO_HIGH	High		
If available: CT_CORE_IO_INPUT	Input		
NOTE Same test network configuration for conducted emission of →*Driver* noise, see 6.3			

6.7.7.2.3 Test procedure – Multiple *driver* and/or *input port*

The following conducted emission measurement sequence should be performed:

Table 21 – Test procedure *core* to *drivers* and *inputs* crosstalk, with *CPU*, multiple *driver* or *input port*

Test name	Test port			Test software	
	Loaded Pins*	Test Pin*	Unloaded Pins*	Recommended	Optional
CT_CORE_IO_LOW	Input	Low	Input	C1-S2	If available, 'worst case' of: C2-S2 C3-S2 C4-S2
CT_CORE_IO_HIGH		High			
If available: CT_CORE_IO_INPUT		Input			
* If output.					
NOTE Same test network configuration for conducted emission of →*Driver* noise, see 6.3.					

6.7.8 Oscillator

To obtain information concerning emission behaviour of the IC function module *oscillator*, it should be active all the time within the emission tests.

6.7.8.1 Emission propagation path *supply*

6.7.8.1.1 Selection of test network

The supply pin pair related to the *supply module* of the *oscillator* have to be tested for conducted emission, see 6.4.

6.7.8.1.2 Test procedure

– *Core* with *CPU*:

The following conducted emission measurement sequence should be performed (if IC configuration available):

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Table 22 – Test procedure *oscillator* supply noise, *with CPU*

Test name	Test software	
	Recommended	Optional
CLOCK_TREE	C7-S0	–
OSC	–	C6-S0

– Core without CPU:

The following conducted emission measurement sequence should be performed:

Table 23 – Test procedure *oscillator* supply noise, *without CPU*

Test name	Test condition of *IC function module*	
	Recommended	Optional
OSC	*IC function module* with EMC 'worst case' parameters	–

6.7.8.2 Emission propagation path *crosstalk* to other *IC function modules*

As the IC function module *oscillator* is recommended for all other clocked function modules in an IC with oscillator, it shall be tested indirectly within the measurement of other core IC function modules.

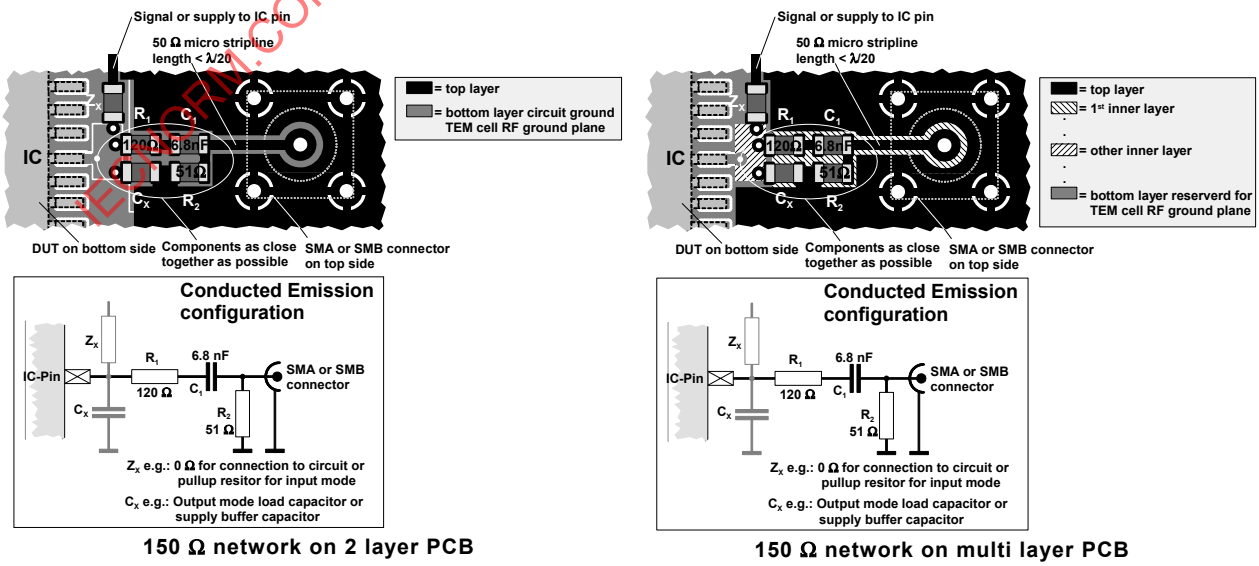
7 Test board layout recommendations

7.1 Common test board recommendations

The test board should be designed as described in IEC 61967-4. It is built with a minimum of two layers, one as a dedicated ground plane and impedant-defined 150 Ω striplines.

Optional: The test board should be able to combine different IC EMC test methods. To perform emission measurements with a TEM-cell, the test PCB recommendations described in IEC 61967-2 should serve as the base for creating a combination test board with 150 Ω/1 Ω networks.

7.2 150 Ω network on 2 layer and multi layer PCB



150 Ω network on 2 layer PCB **150 Ω network on multi layer PCB**

NOTE The impedance of signal island at the IC pin is not 150 Ω, but can be neglected as it is as small as possible.

Figure 10 – Layout recommendation 150 Ω network

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7.3 1 Ω network on 2 layer and multi-layer PCB

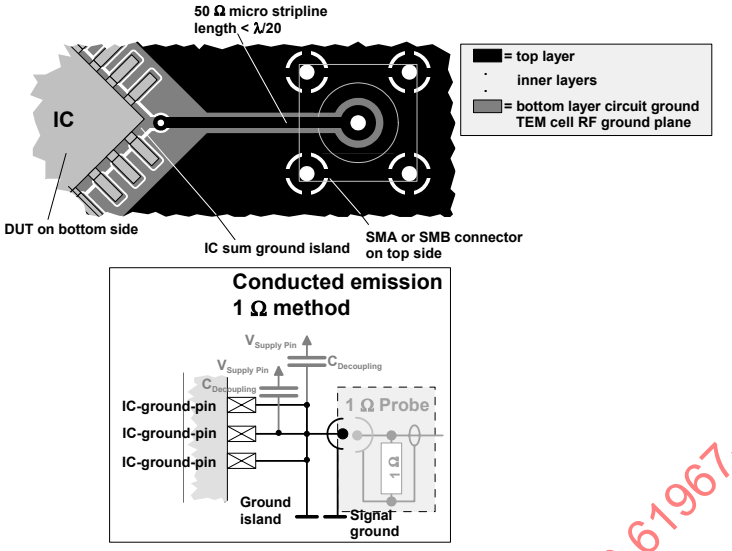

Figure 11 – Layout recommendation 1 Ω network

8 Test report

The following items should be in the test report:

– documentation of splitting the IC into *IC function modules*;

– documentation of test port selection, supply pin selection and supply test method selection;

– capacitor modifications of the test networks noted, with the valid frequency ranges marked in the result diagrams, see Annex A;

– schematic diagram of test board or reference to company internal database;

– layout of test board or parts of the layout or reference to company internal database;

– typical transfer characteristics of test circuits and test PCB traces;

– operation definitions of FFUs and implemented software modules in case of CPU availability;

– test equipment;

– result diagrams, scaled in *dBµV*.

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Annex A
(normative)

IEC 61967-4 test network modification

A.1 Calculation of new start frequency in case of modifying the coupling capacitor of the 150 Ω measuring network

Basis of calculation:

transfer ratio $_{\text{highpass voltage divider}}$ $a = \dfrac{U_{out}}{U_{in}} = \dfrac{Z_{in}}{Z_{out}}$; limit definition $a\big|_{-3dB} = \dfrac{1}{\sqrt{2}}$ (A.1)

Attenuation equation of 150 Ω network, see Figure A.1:

$$|a| = \left|\frac{U_{out}}{U_{in}}\right| = 20 \cdot \log \left| \frac{(51\Omega \| 50\Omega)}{\sqrt{(120\Omega + 51\Omega \| 50\Omega)^2 + \dfrac{1}{4\pi^2 f^2 C^2}}} \right|,$$

transfer ratio for: $f \to \infty$: $\left|a_{f\to\infty}\right| = -15.2\,\text{dB}$ (A.2)

Equation for limit frequency (highpass -3dB point)

$$f_{-3dB|_{MHz}} \approx \frac{1}{844\,\Omega \cdot C_{|\mu F}} \quad \text{(A.3)}$$

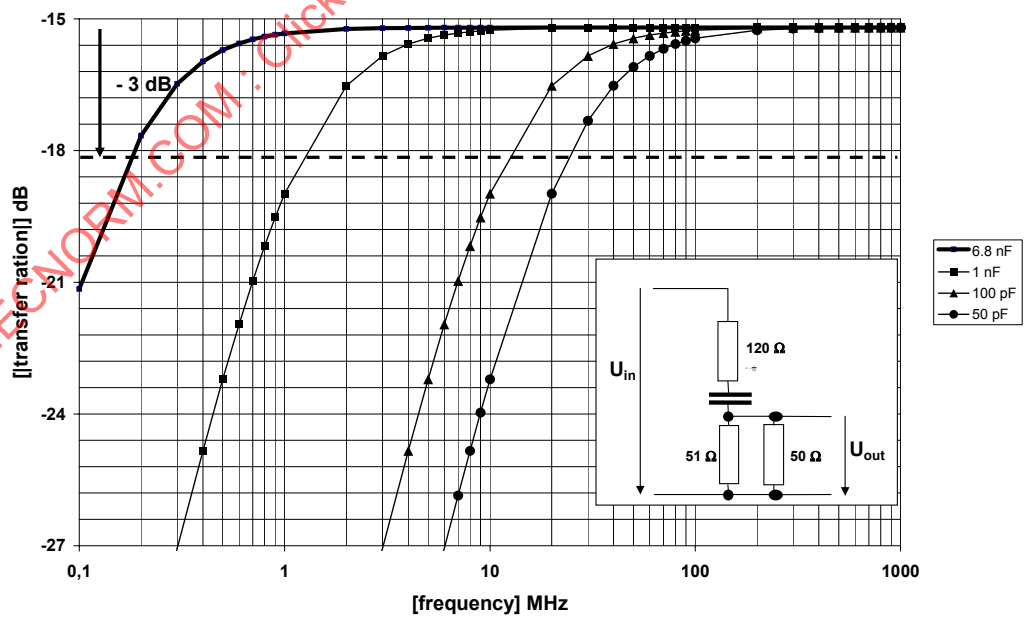

Figure A.1 – 150 Ω network, attenuation chart of some example capacitor values

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