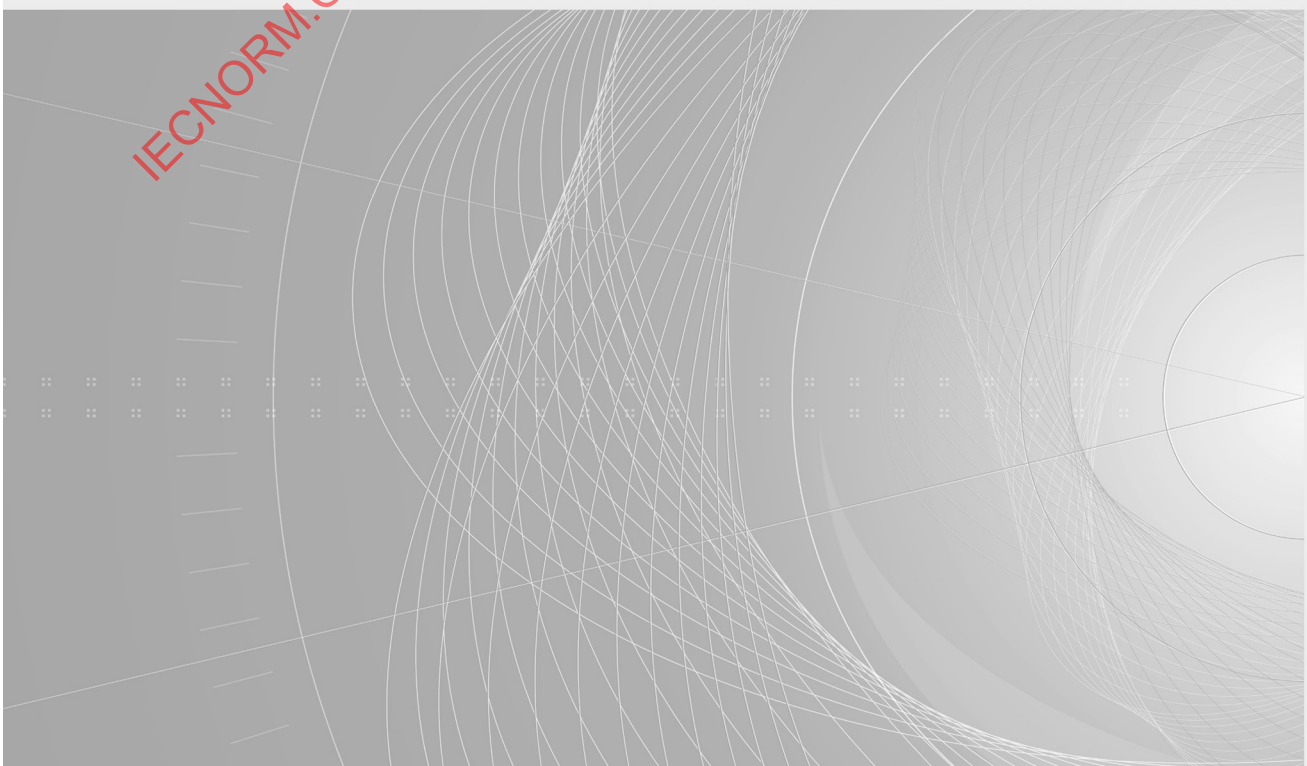
IEC TR 61643-03

Edition 1.0 2024-07

TECHNICAL REPORT

colour inside

Low-voltage surge protective devices – Part 03: SPD testing guide



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Low-voltage surge protective devices – Part 03: SPD testing guide

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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LOW-VOLTAGE SURGE PROTECTIVE DEVICES –

Part 03: SPD Testing Guide

FOREWORD

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IEC TR 61643-03 has been prepared by subcommittee 37A: Low-voltage Surge Protective Devices, of IEC technical committee 37: Surge Arrestors. It is a Technical Report.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
37A/XX/DTR	37A/XX/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 61643, published under the general title Low-voltage surge protective devices, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The "colour inside" logo on the cover page of this document indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

It has been assumed in the preparation of this document that the execution of its provisions is entrusted to appropriately qualified and experienced persons.

Throughout this document, when the “IEC 61643-x1 series” is mentioned, it refers to all parts of the IEC 61643 series of standards that deal with testing of SPDs, e.g. IEC 61643-01, IEC 61643-11.

This part of the IEC 61643 series addresses correct test execution and accurate interpretation of measurement results and is also intended to further enhance repeatability and comparability throughout different test laboratories and to establish an acceptable accuracy level for the test results obtained.

The new SPD classification T1 SPD, T2 SPD and T3 SPD is relating to the former test class oriented classification Class I tests, Class II tests and Class III tests.

LOW-VOLTAGE SURGE PROTECTIVE DEVICES –

Part 03: SPD Testing Guide

1 Scope

This part of IEC 61643, which is a Technical Report, applies to SPD testing in accordance with the IEC 61643-x1 series and for SPD coordination and system level immunity purposes.

It aims to provide guidance and helpful information for correct test execution and accurate interpretation of measurement results. It is also intended to further enhance repeatability and comparability throughout different test laboratories and to establish an acceptable accuracy level for the test results obtained.

The main subjects are:

– Test application
– Test arrangement/setup
– Probe application
– SPD coordination testing
– System level immunity testing

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

For the purposes of this document the normative references given in IEC 61643-01:— [1] and the following apply.

IEC 61643-01:—, *Low-voltage surge protective devices – Part 01: General requirements and test methods*

IEC 61643-11:—[2], *Low-voltage surge protective devices – Part 11: Surge protective devices connected to low-voltage power systems – Requirements and test methods*

IEC 61643-12:2020, *Low-voltage surge protective devices – Part 12: Surge protective devices connected to low-voltage power systems – Selection and application principles*

IEC 61643-41:—[3], *Low-voltage surge protective devices – Part 41: Surge protective devices connected to DC low-voltage power systems – Requirements and test methods*

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[1] Under preparation. Stage at the time of publication: IEC/ACDV 61643-01:2023.

[2] Under preparation. Stage at the time of publication: IEC/ACDV 61643-11:2023.

[3] Under preparation. Stage at the time of publication: IEC/ACDV 61643-41:2023.

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 61543-01:— apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

4 Correspondence between this document and the tests in IEC 61643-x1

Table 1 provides information on which clauses of this document should apply to certain tests from the IEC 61643-x1 series.

Table 1 – Correspondence between this document and the IEC 61643-x1 series

IEC 61643-03 clause reference	Relevance for test clauses in the IEC 61643-x1 series
5 Probe application – residual voltage measurements	9.1.1, Table 3, pass criterion D 9.3.4 measured limiting voltage, 9.3.5 operating duty test, 9.6.5.3 Measurement of voltage rate of rise d*u*/d*t*
6 Insulation resistance and dielectric withstand	9.3.7 Insulation resistance 9.3.8 Dielectric withstand
7 TOV testing	9.3.9 Behaviour under temporary overvoltages (TOVs)
7.1 TOV testing of SPDs for AC power systems	IEC 61643-11:—, 9.3.9.101 TOVs caused by faults in the high (medium) voltage system
7.2 TOV testing of SPDs for DC power systems	IEC 61643-41:—, 9.3.9 Behaviour under temporary overvoltages (TOVs)
8 Test application to SPDs with multiple components	General
Annex A Critical investigation on the impulse current specification for T1 SPDs when testing Metal Oxide Varistors	9.1.2 Impulse discharge current

5 Probe application – residual voltage measurements

5.1 Overview

Residual voltages measurements are very sensitive measurements due to the fact that they are carried out at high frequencies in presence of magnetic fields which may strongly interfere with the results of these measurements to such an extent that different measurements from one measurement to another one, or between different testing entities may not be comparable.

This clause intends to provide guidelines on testing techniques for making correct residual voltages measurements to limit these deviations and discrepancies.

5.2 General

According to the induction law, an alternating magnetic field induces a voltage into a conductor loop. The induced voltage depends on the loop size and the frequency and the amount of magnetic field. The intensity of a magnetic field decreases with increasing distance to its source.

The residual voltage is measured with 8/20 current impulses. The magnetic field generated by this 8/20 current impulse induces a voltage into the loop build up by the voltage measurement lines that are connected to the device under test. This voltage is added to the voltage drop between the two points where the measurement lines are connected to. This induced voltage depends on and is directly proportional to the size of the loop build by the voltage measurement lines and to the peak value of the 8/20 current impulse and may have values of several 10 V up to some kV. The wave shape of the induced voltage follows the derivative di/dt of the 8/20 current impulse and reaches its maximum at the beginning of the 8/20 current impulse. A zero crossing and therefore 0 V occurs at the crest value of the 8/20 current impulse. A typical waveshape of the induced voltage is shown in Figure 1.

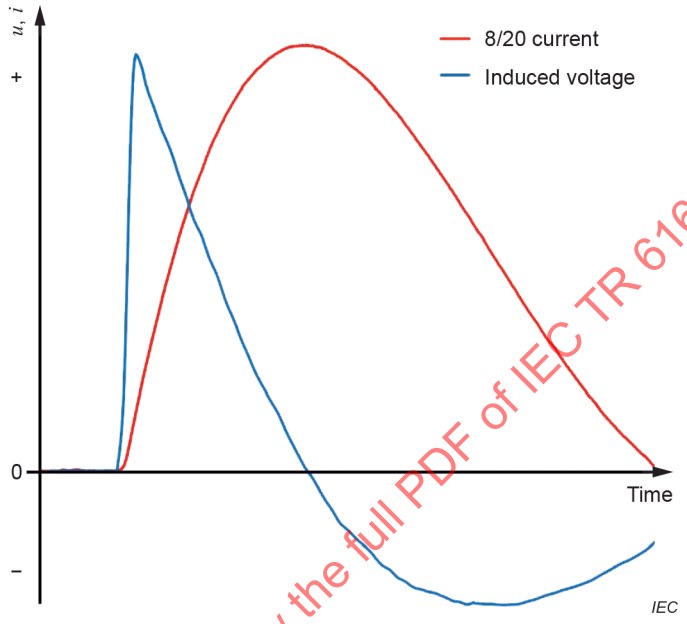


Figure 1 – 8/20 current impulse and induced voltage

In general, the test procedure to measure the residual voltage with 8/20 current impulses requires the connection of the voltage measuring system as close as possible to the SPD. This is caused by the fact that a voltage drop occurs along the length of a conductor when a current flows through. This voltage drop also influences the measured voltage between the two points to which the measurement lines are connected.

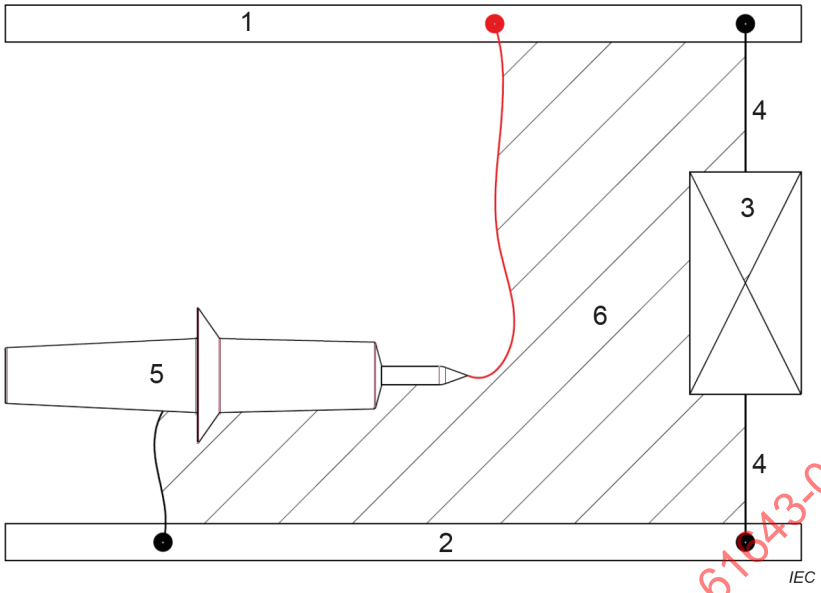
To show the influence of the loop size of the voltage measurement lines and the voltage drop of the conductors to the test sample when the 8/20 current impulse flows, three test arrangements are assumed.

Test arrangement A is given in Figure 2 and shows a large loop size of the voltage measurement lines that are connected far from the test sample.

Test arrangement B is given in Figure 3 and shows a smaller loop size of the voltage measurement lines that are connected directly to the test sample.

Test arrangement C is given in Figure 4 and shows a loop size as small as possible of the voltage measurement lines that are twisted and connected directly to the test sample.

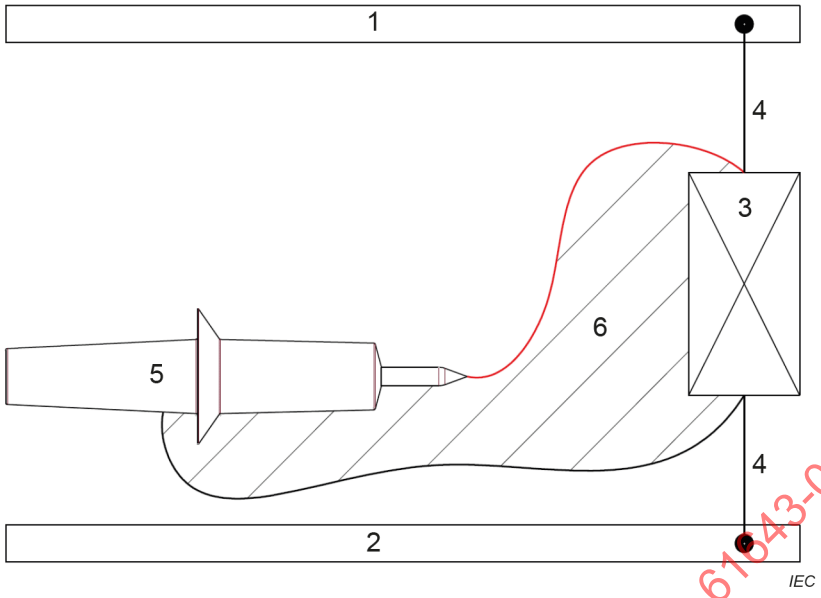
Figure 5 shows the measured voltage time behaviour of the test arrangements A, B and C during 8/20 current application when the device under test is a voltage limiting SPD.



Key

1 HV output connection of impulse current generator
2 Ground connection of impulse current generator
3 Device under test (SPD)
4 Conductor to connect the SPD to the impulse current generator
5 Voltage probe
6 Loop area created by the voltage measurement lines (hash shaded area)

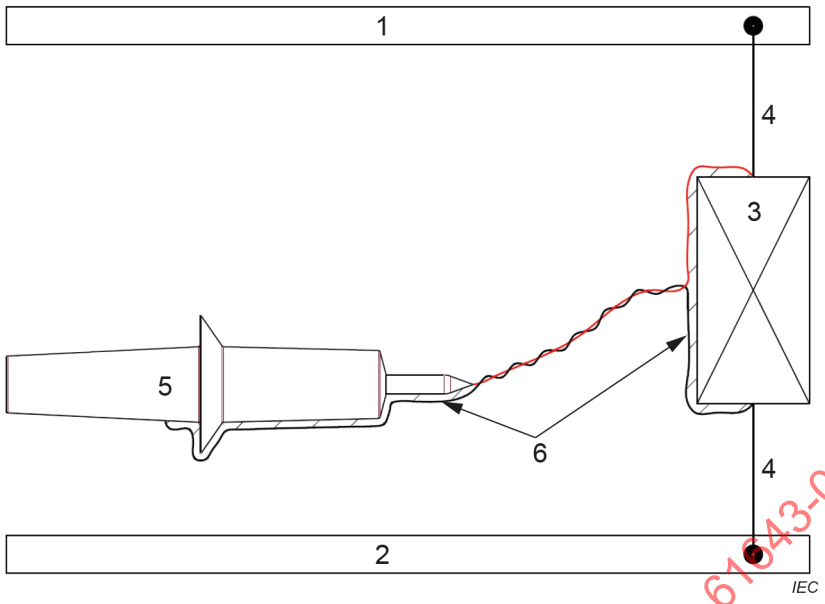
Figure 2 – Test arrangement A



Key

1 HV output connection of impulse current generator
2 Ground connection of impulse current generator
3 Device under test (SPD)
4 Conductor to connect the SPD to the impulse current generator
5 Voltage probe
6 Loop area created by the voltage measurement lines (hash shaded area)

Figure 3 – Test arrangement B



Key

1 HV output connection of impulse current generator
2 Ground connection of impulse current generator
3 Device under test (SPD)
4 Conductor to connect the SPD to the impulse current generator
5 Voltage probe
6 Loop area created by the voltage measurement lines (hash shaded area)

Figure 4 – Test arrangement C

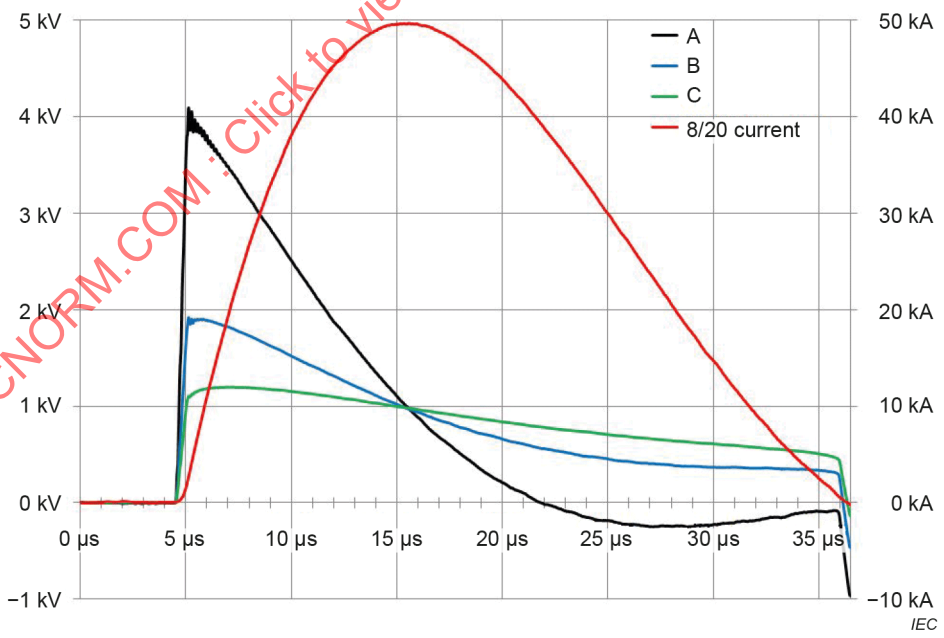


Figure 5 – Measured voltages of test arrangements A, B and C during 8/20 current application

5.3 Guidance for the test arrangement

5.3.1 General

The guidance for test arrangements to measure the residual voltage with 8/20 current impulses given in 5.3.2 and 5.3.3 may be applied if:

- it is unknown or it is assumed, that the influence of the magnetic field of the 8/20 current or the loop size of the measurement lines is too big, or
- the measured residual voltage exceeds the voltage protection level Up of an SPD defined by the manufacturer, or
- agreed or required by the manufacturer of the SPD.

The following two alternate test arrangements are proposed. Depending on the equipment available and as required by the manufacturer of the SPD one of these methods could be chosen.

In addition, the use of differential probes and/or a scope with isolated inputs should be considered.

5.3.2 Method 1: Voltage probe placed at a certain distance

If the design of the SPD and/or the size of the voltage probe does not allow to connect the voltage probes very close to the device under test (DUT) without creating a large loop area, the following test setup may be appropriate to minimize the loop build up by the measurement lines and the SPD itself.

The measurement lines connecting the voltage probe to the DUT should be as small as possible. Their insulation should be as small as possible but thick enough to withstand, when twisted together, the expected residual voltage. The measuring lines should be routed along the shortest distance between the connections of the DUT along the housing of the DUT. From the midpoint of the shortest distance between the connections of DUT, the measurement lines should be twisted with a twist rate of at least 30 twists per meter and routed at around 90° ±10° away from the axis created by the DUT and its conductors to the impulse current generator.

The shortest distance between the connections of DUT onto its housing may vary depending on the mode of protection under test. A typical example of an SPD having a single mode of protection is given in Figure 6. Two typical examples of a multimode SPD are given in Figure 8 and Figure 9.

Figure 7 shows a wrong routing of the measurement lines, where the loop between the measurement lines and the DUT is too large.

The voltage probe should be placed in a distance of 200 mm minimum up to 500 mm maximum away from the DUT.

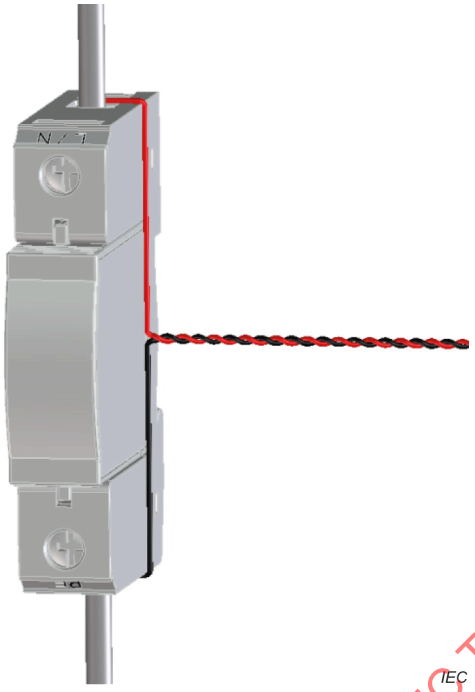
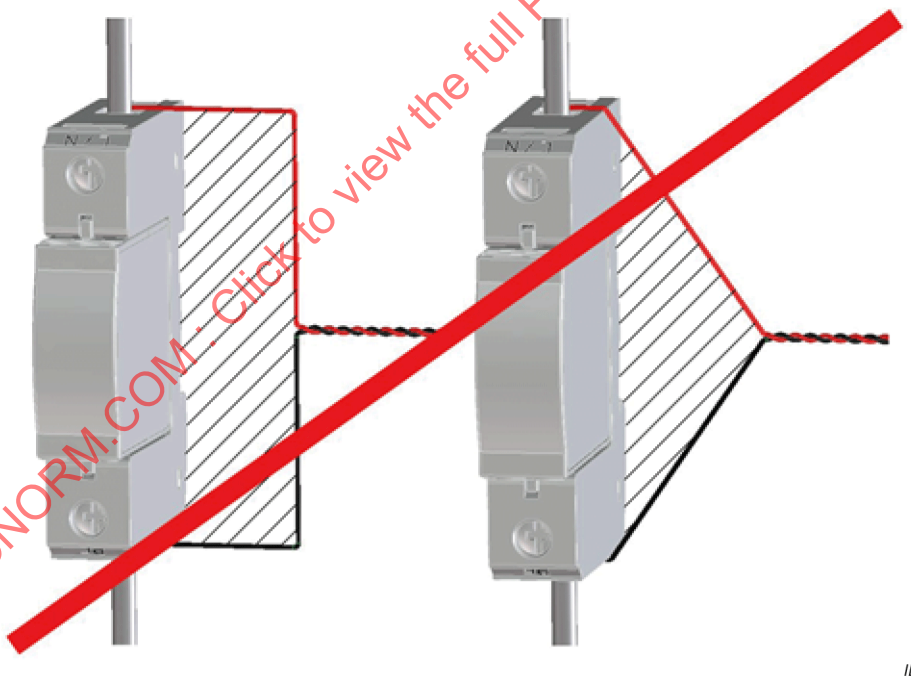


Figure 6 – Routing of the measurement lines of an SPD having a single mode of protection



Loop area created by the pigtails together with the voltage measurement lines (hash shaded area)

Figure 7 – Wrong routings of the measurement lines

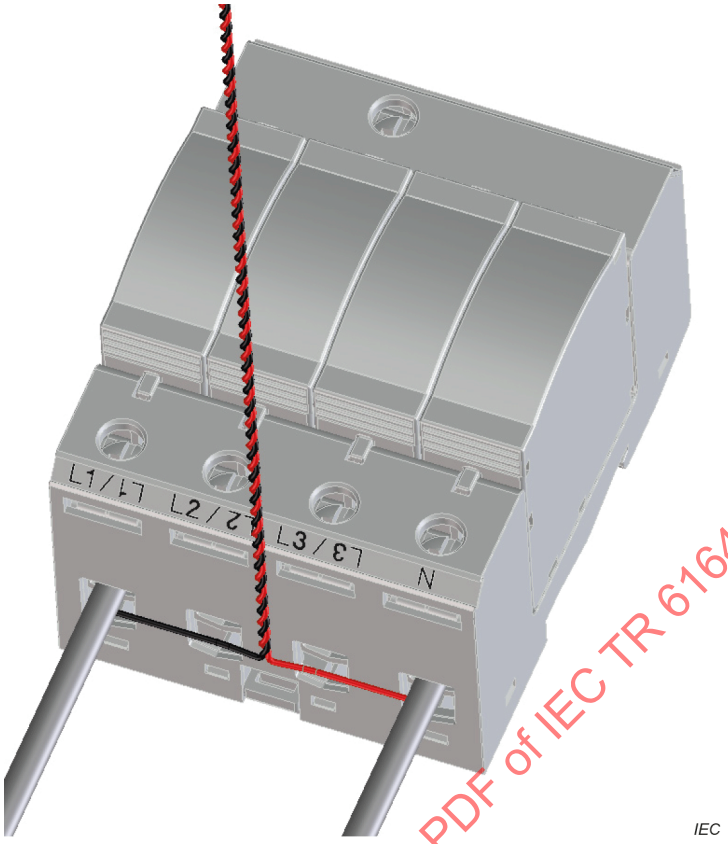


Figure 8 – Routing of the measurement lines of a multimode SPD, example 1

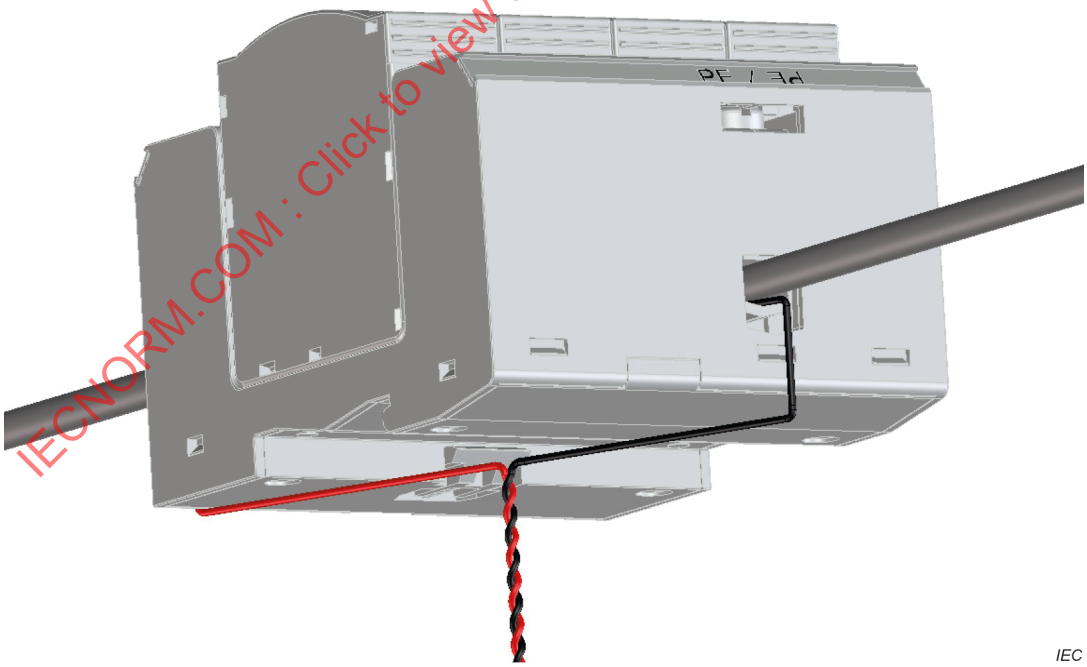


Figure 9 – Routing of the measurement lines of a multimode SPD, example 2

5.3.3 Method 2: Minimized loop of measurement lines

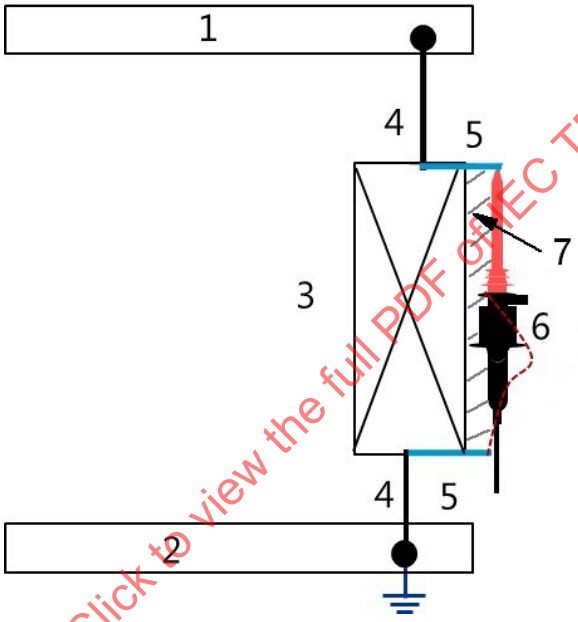
If the design of the SPD and the size of the voltage probe allows to connect the voltage probe directly or via short measurement lines placed close to the DUT the following test setup may be appropriate to minimize the loop build by the measurement lines and the SPD itself.

The voltage probe (with reduced dimensions) is placed as close as possible to the SPD. The voltage probe is either connected directly to the DUT or via a separate connecting wire which is as straight and as short as possible. It should be considered that the connecting wire itself is not part of the test circuit for the impulse current and no impulse flows through it.

To minimize the loop size even further, the ground connection wire 5 (connected to 4 on the ground side) should be twisted around the body of the voltage probe.

If possible, the voltage probe should be positioned in parallel to the impulse current flow through the SPD. Therefore the design of the SPD (single mode/ multimode) and the corresponding flow of surge current should to be considered.

Figure 10 shows an example for the application of method 2 to an SPD having a single mode of protection.



Key

1 HV output connection of impulse current generator

2 Ground connection of impulse current generator

3 Device under test (SPD)

4 Conductor to connect the SPD to the impulse current generator

5 Conductor to connect the SPD to the voltage probe

6 Voltage probe

7 Loop area created by the voltage measurement lines (hash shaded area)

Figure 10 – Example for the application of method 2 at an SPD having a single mode of protection

5.3.4 Combination of method 1 and method 2 for pigtail connections

Figure 11 describes the probe voltage connection for products with pigtail connections.

Figure 12 shows a wrong routing of the SPD pigtails together with the measurement lines, where the loop created by the SPD pigtails and the measurement lines is too large.

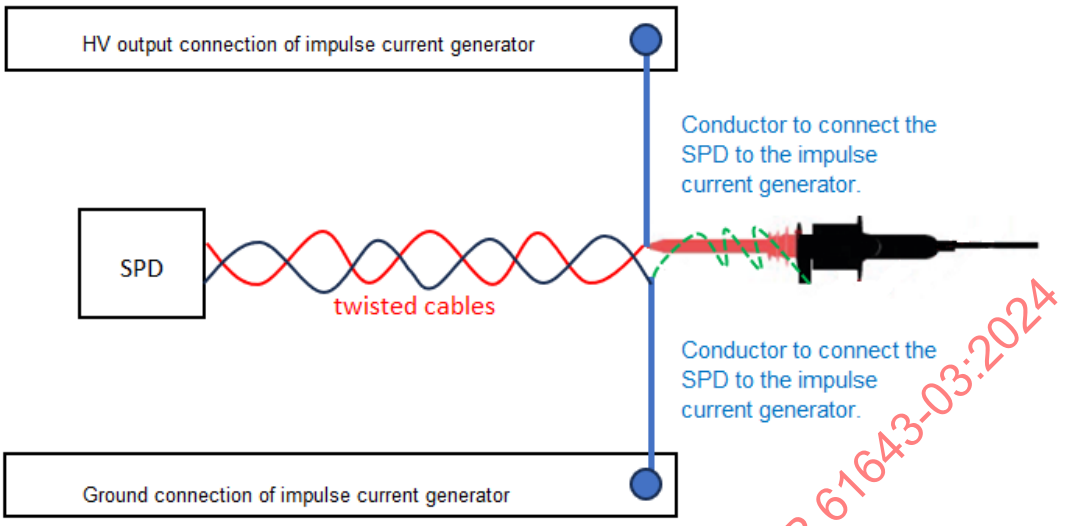
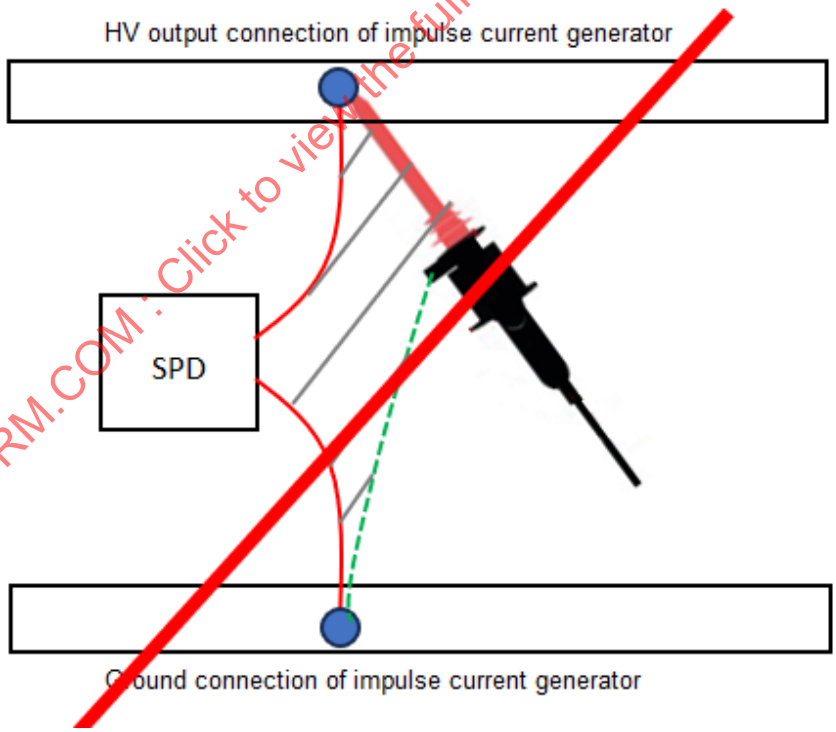


Figure 11 – Example for the application of method 1 and method 2 where the SPD is provided with pigtail connections



Loop area created by the pigtails together with the voltage measurement lines (hash shaded area)

Figure 12 – Wrong routings of the pigtails together with the measurement lines where the SPD is provided with pigtail connections

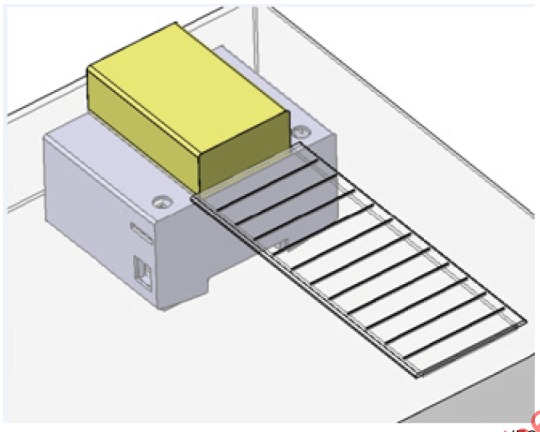
6 Insulation resistance and dielectric withstand

6.1 General

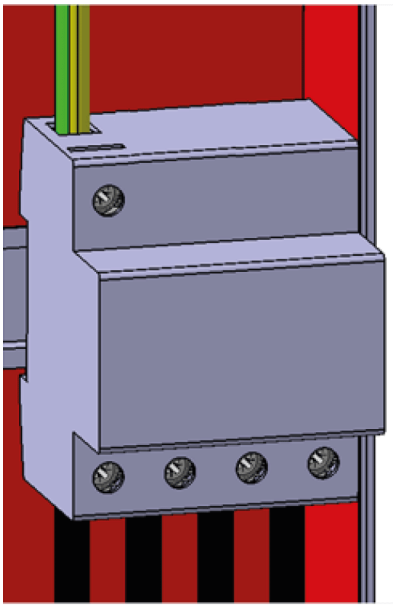
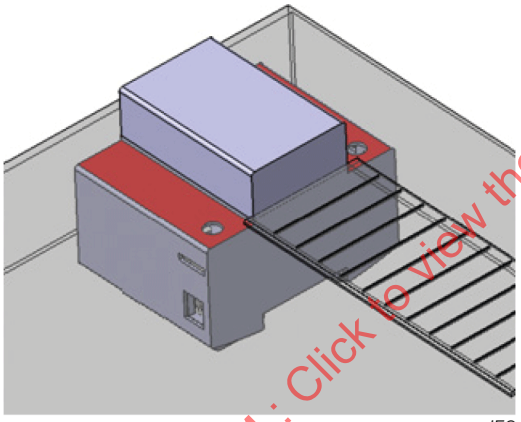
In this clause guidance is given on how to correctly perform the testing of the insulation resistance and the dielectric withstand of SPDs:

– between live parts and the SPD's body,
– between electrically separated circuits,
– between live parts of the SPD´s main circuits and live parts of any electrically separated circuit(s)
– between live parts of different electrically separated circuit(s)

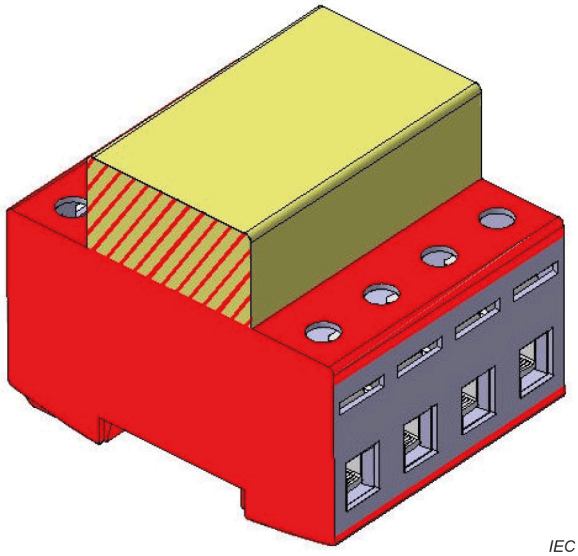
6.2 Surfaces which are touchable after installation as for normal use are as follows:

 IEC	**Normal use** means: Built in an enclosure including a cover. – only the **yellow marked surfaces** are touchable

6.3 Surfaces on which the SPD can be mounted or it can be in contact with metal surfaces:

 IEC	The SPD can be installed in a metallic cabinet or casing – **red marked surfaces** can be of metal or conductive material
 IEC	The cover could also be metallic or conductive – **red marked surfaces** of the SPD can be in contact with metallic or conductive parts

6.4 Conclusions:



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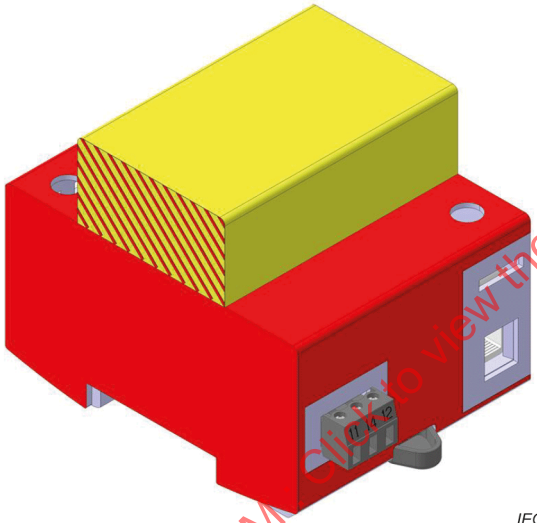


IEC

"Body" includes the **red** + **yellow** **marked surfaces** and the mounting surface.

The **red** + **yellow** **marked surfaces** are covered with metal foil for testing.

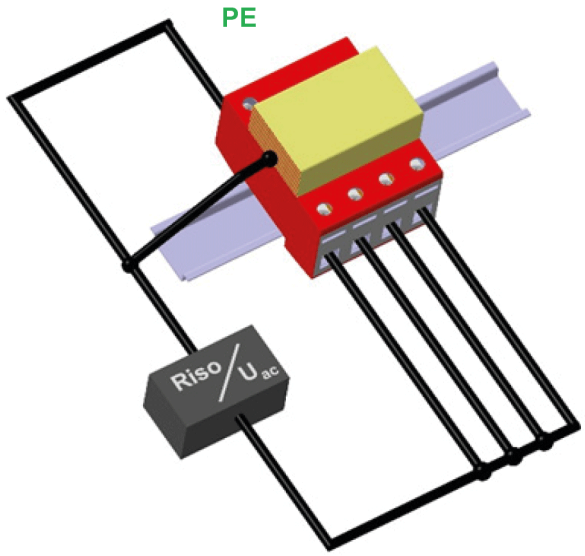
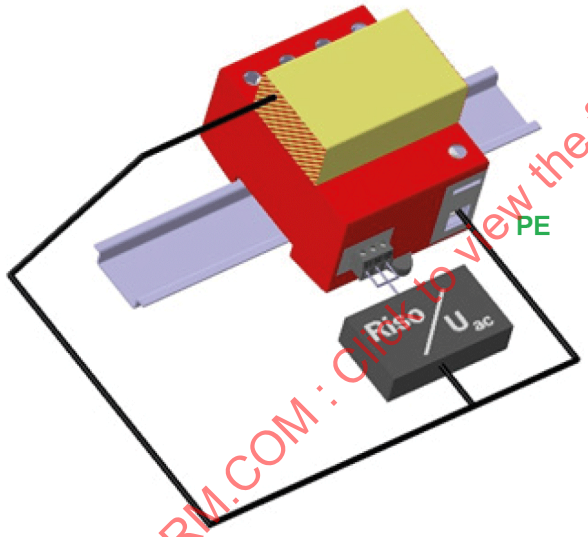
The metal foil also covers screw holes, but the foil is not pushed into the holes during the application of the test finger

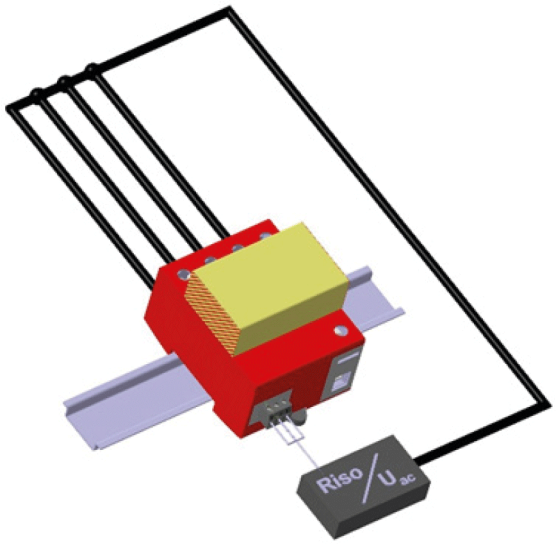
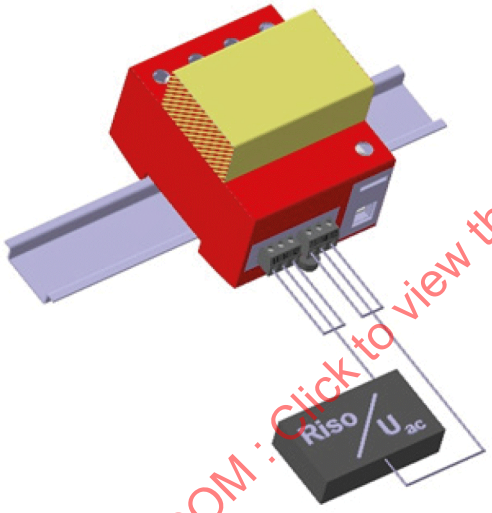
Sufficient distance is kept between the metal foil and the live terminal entrance(s) to ensure that no flashover occurs during testing.

The mounting surface including any recessed surface for mounting rails, or similar, are also covered with foil.

The PE terminal is connected to the metal foil.

6.5 Example of a test-set-up to measure the Insulation Resistance according to 9.3.7 and the Dielectric Withstand according to 9.3.8 of IEC 61643-01:—

 IEC	**Test according to 9.3.7.2, item a) of IEC 61643-01:—** Between all interconnected live parts of the SPD's main circuit(s) (all terminals being connected together, but excluding the PE, PEN or PEM terminals/connections) and the SPD's body.
 IEC	**Test according to 9.3.7.2, item b) of IEC 61643-01:—** Between all interconnected live parts from each electrically separated circuit, if there is any, and the SPDs body.

 IEC	**Test according to 9.3.7.2, item c) of IEC 61643-01:—** between all interconnected live parts of the SPD's main circuit(s) (all terminals being connected together, but excluding the PE, PEN or PEM terminals/connections) and all interconnected live parts of each electrically separated circuit, if there are any.
 IEC	**Test according to 9.3.7.2, item d) of IEC 61643-01:—** between all interconnected live parts of any electrically separated circuit and all interconnected live parts of all other electrically separated circuits, if there is more than one.
NOTE R_{iso}/U_{ac} insulation resistance test equipment	

7 TOV testing

7.1 TOV testing of SPDs for AC power systems

Figure 13 provides additional examples of test setups to IEC 61643-11 for use in testing SPDs for application in TT systems and for testing TOVs caused by faults in the high (medium) voltage system.

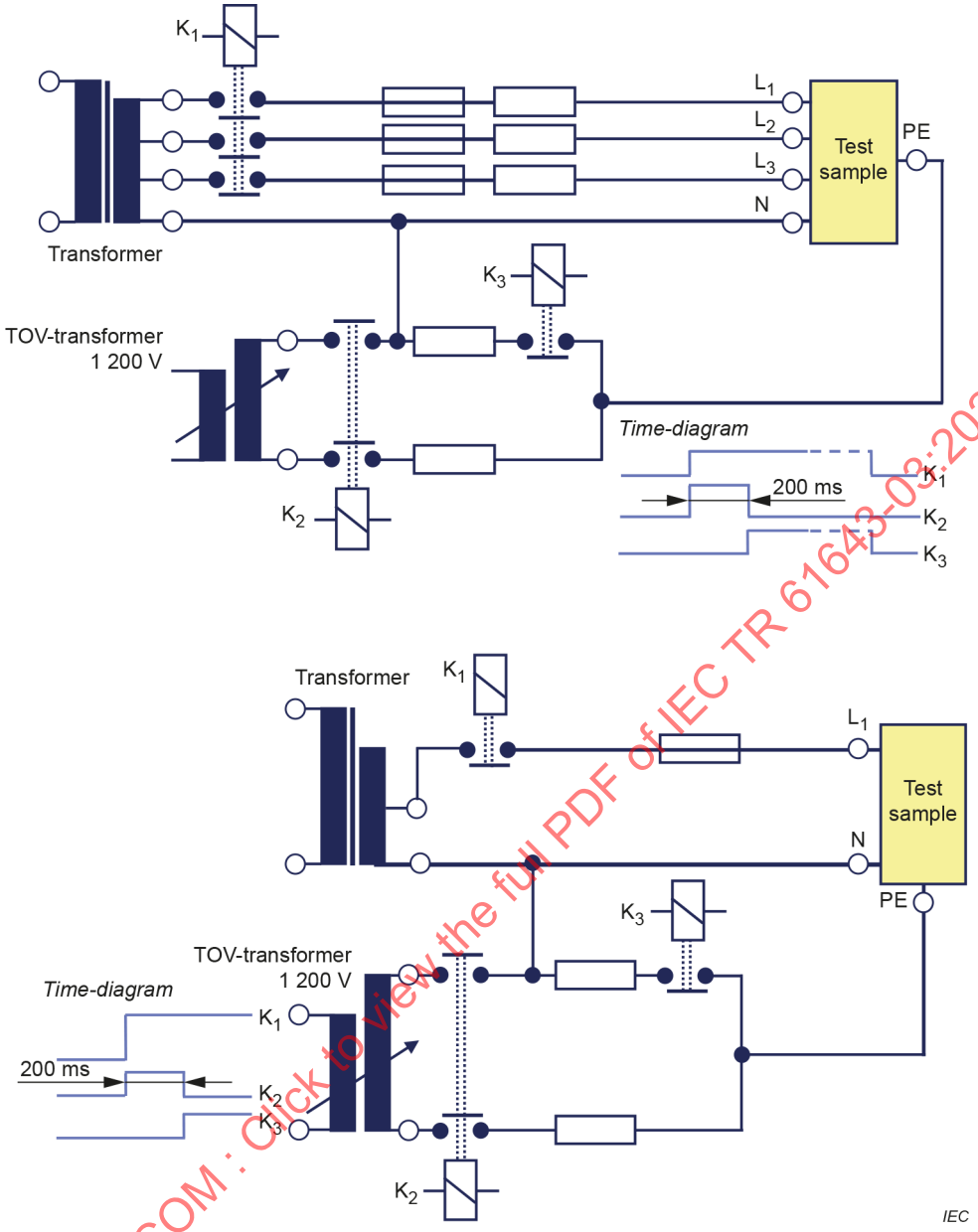


Figure 13 – Examples of a three-phase and single-phase test setup for use in testing SPDs for application in TT systems under TOVs caused by faults in the high (medium) voltage system

Figure 14 provides an additional example of a test setup to IEC 61643-11 for use in testing SPDs for application in IT systems and for testing TOVs caused by faults in the high (medium) voltage system. Figure 15 provides the corresponding vector diagram for the voltages in this test setup.

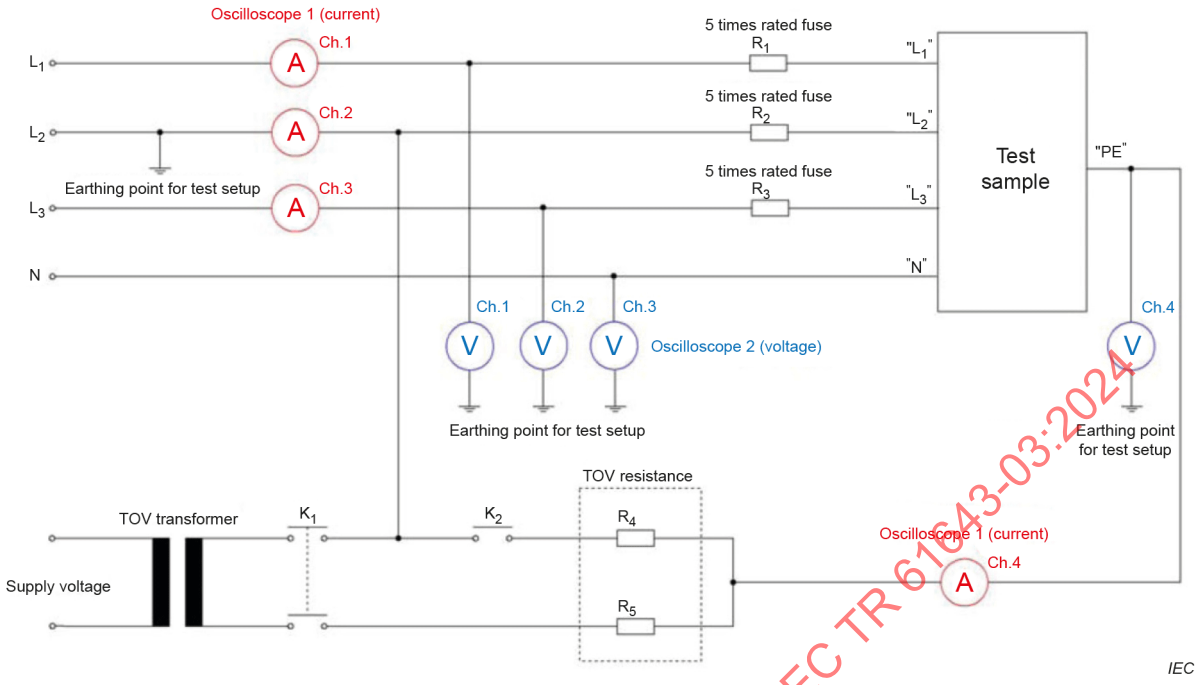


Figure 14 – Example of a three-phase test setup for use in testing SPDs for use in IT systems under TOVs caused by faults in the high (medium) voltage system

The earthing point for the example test setup is choosen to be located in phase L2 for measurement reference purposes and for protection considerations, to ensure that no point of the test setup exceeds 1 200 V RMS to earth. This earthing point may in principle be choosen anywhere depending on laboratory system configuration, but may have an influence on measurement setup.

This earthing point for the test setup has no relation to the earth fault simulation provided by the test setup.

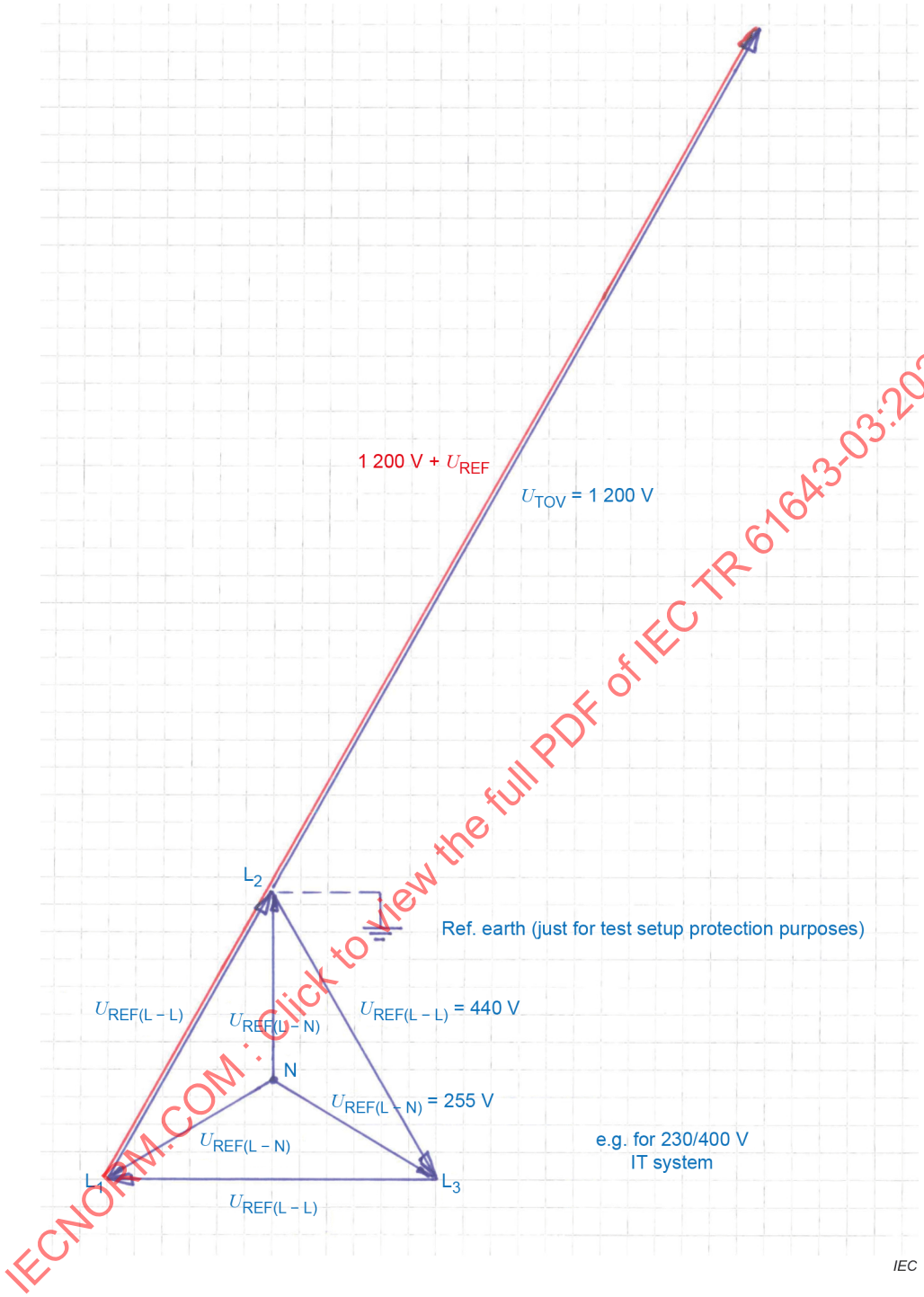


Figure 15 – Vector diagram for the voltages in the test setup in Figure 14

7.2 TOV testing of SPDs for DC power systems

Figure 16 provides an example of a test setup to IEC 61643-41:— for use in testing SPDs intended to be connected to a DC system, which is derived from an AC TT system without separation, under TOVs caused by faults in the high (medium) voltage system.

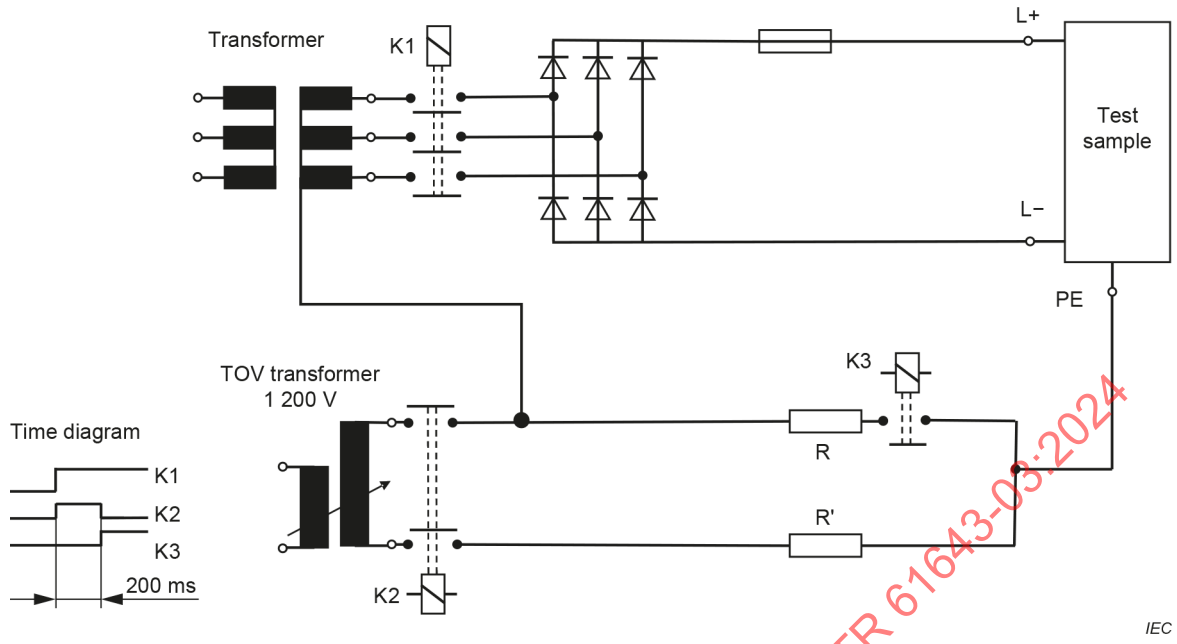


Figure 16 – Example of a test setup for use in testing SPDs intended to be connected to a DC system, which is derived from an AC TT system without separation, under TOVs caused by faults in the high (medium) voltage system

Figure 17 provides an example of a test setup to IEC 61643-41:— for use in testing SPDs intended to be connected to a DC TT system, which is derived from another earthed DC system, under TOVs caused by faults in the high (medium) voltage system.

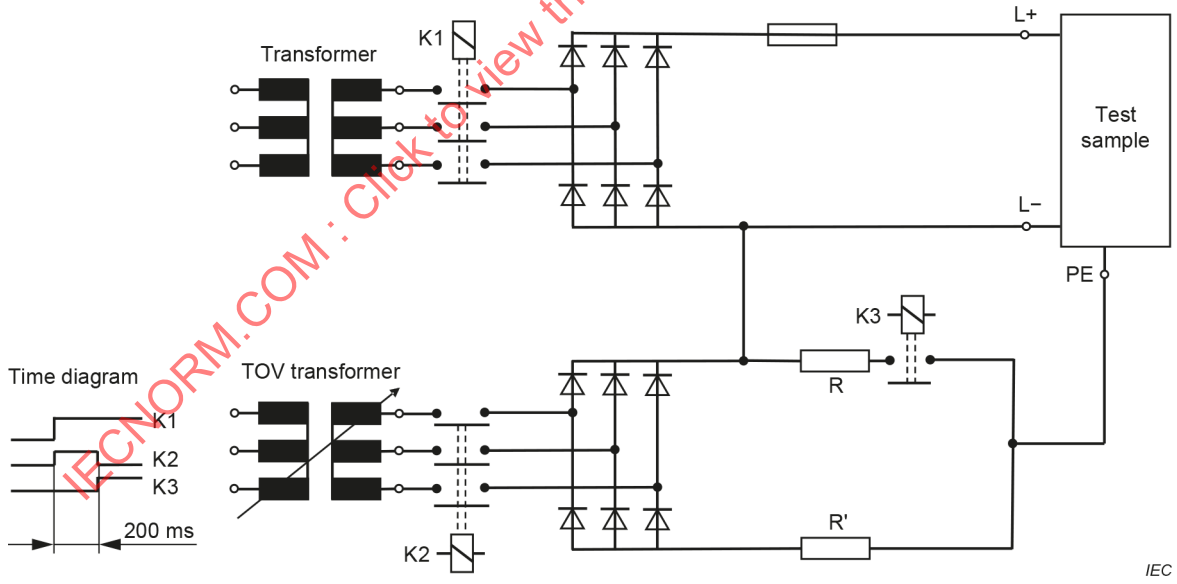


Figure 17 – Example of a test setup for use in testing SPDs intended to be connected to a DC TT system, which is derived from another earthed DC system, under TOVs caused by faults in the high (medium) voltage system

8 Test application to SPDs with multiple components

8.1 General

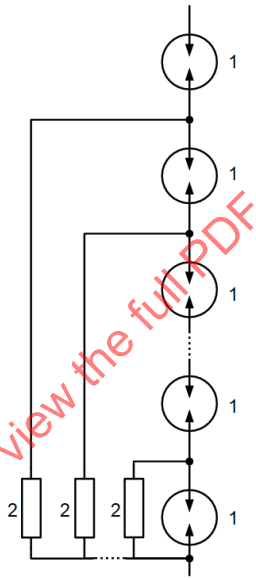
This clause provides guidance on which current paths are to be tested for certain examples of SPDs containing multiple components. For certain SPD constructions samples need to be

modified to allow this selective testing and specific sample preparation is necessary for SPDs with non-linear components connected in parallel.

The sample preparation requirements were developed based on the principle component arrangements mostly used within SPDs. Nowadays more and more complex SPD-circuitries appear in the market and questions arise on how to correctly apply these sample preparation requirements according to the original intentions. As this document only refers to non-linear components, but does not consider, if such components may take a significant fraction of the surge current or what could happen if such component fails, further guidance is needed. Such guidance is very difficult to provide in a general way as new circuit designs appear every now and then. Therefore the following examples are intended to guide the manufacturers and test engineers to take the most appropriate decision for sample preparation.

8.2 Example of a multiple series spark gap with resistive/capacitive trigger control

An example of multiple spark gaps in series with resistive/capacitive trigger control is shown in Figure 18.



Key

1 spark gaps

2 resistive or capacitive trigger control

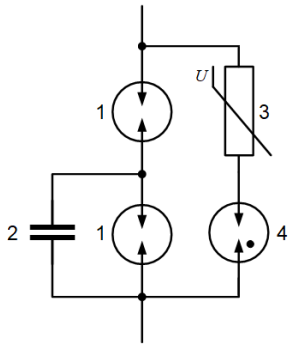
Figure 18 – Multiple series spark gap with resistive /capacitive trigger control

The series-connected spark gaps are the only non-linear components in this SPD and they represent the only current path which needs to be considered for testing.

The ohmic or capacitive voltage divider/trigger control circuitry does not constitute a separate current path in the meaning of Annex B, because it contains neither a non-linear component, nor does it take a significant fraction of current.

8.3 Example of a series spark gap with resistive/capacitive trigger control and with a parallel connected series connection of GDT + MOV(s)

An example of two spark gaps in series with resistive/capacitive trigger control and with a parallel connected series connection of GDT + MOV(s) is shown in Figure 19.



Key

1 spark gaps

2 resistive or capacitive trigger control

3 MOV(s)

4 GDT

Figure 19 – Series spark gap with capacitive trigger control

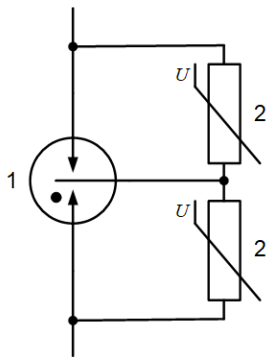
The two spark gaps connected in series constitute the main current path which needs to be considered for testing.

The parallel current path through the series connection of GDT and MOV(s) needs to be considered for separate testing, as the fraction of current passing through that series connection of GDT and MOV(s) is difficult, if not impossible, to determine and no limit for such current fraction is provided by this document.

The resistive/capacitive trigger control circuitry does not constitute a separate current path in the meaning of this document because it contains neither a non-linear component, nor does it take a significant fraction of current.

8.4 Example of a 3-electrode GDT with parallel MOV bypass/trigger control

An example of a 3-electrode GDT with parallel MOV bypass/trigger control is shown in Figure 20.



Key

1 GDT with 3 electrodes

2 MOVs "high energy" bypass

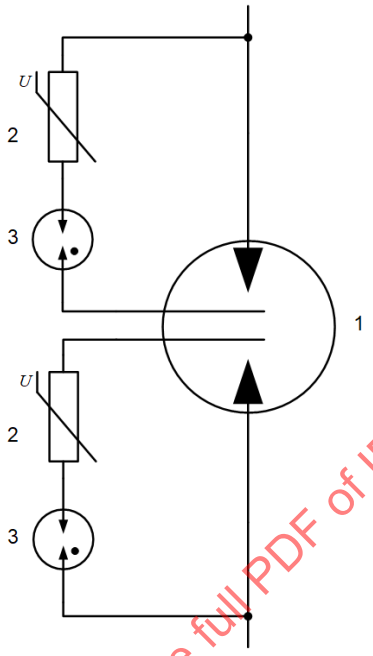
Figure 20 – 3-electrode GDT with parallel MOV bypass/trigger control

The 3-electrode GDT constitutes one current path which needs to be considered for testing.

The parallel current path through the series connection of MOVs needs to be considered for separate testing, as the significant fraction of current can be expected through that series connected MOVs until the GDT operates.

8.5 Example of a 4-electrode spark gap with GDT + MOV trigger control

An example of a 4-electrode spark gap with GDT + MOV trigger control is shown in Figure 21.



Key

1 Spark gap with 4 electrodes

2 MOVs

3 GDTs

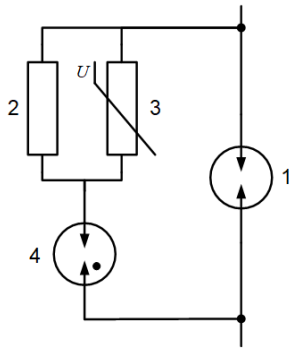
Figure 21 – 4-electrode spark gap with GDT + MOV trigger control

The 4-electrode spark gap constitutes the main current path which needs to be considered for testing.

The fractional parallel current path to single sections of this 4-electrode gap through the series connected GDT and MOV, although containing non-linear components, need not be considered for separate testing, as they do not constitute a parallel current path to the main component being the 4-electrode spark gap.

8.6 Example of a GDT with parallel connected series connection of GDT + MOV

An example of a Spark Gap in parallel with a series-connected GDT and MOV is shown in Figure 22.



Key

1 spark gap
2 resistor
3 MOV
4 GDT

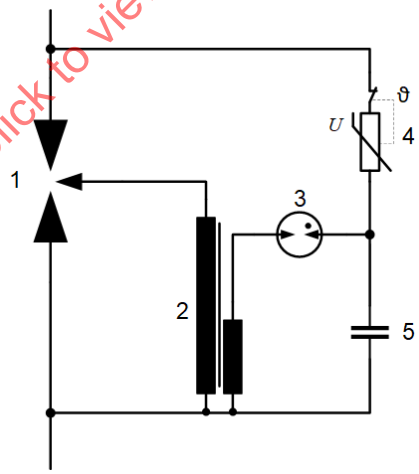
Figure 22 – GDT with parallel connected series connection of GDT + MOV

The spark gap constitutes one current path which needs to be considered for testing.

The parallel current path through the series connection of MOV plus GDT needs to be considered for separate testing, as a significant fraction of current can be expected through that series connection until the spark gap operates.

8.7 Example of a 3-electrode spark gap with trigger transformer

An example of a 3-electrode spark gap with trigger transformer is shown in Figure 23.



Key

1 spark gap with 3 electrodes
2 trigger transformer
3 GDT
4 MOV with thermal disconnect
5 capacitor

Figure 23 – 3-electrode spark gap with trigger transformer

The 3-electrode spark gap constitutes the main current path which needs to be considered for testing.

The parallel current path is limited in current by the trigger transformer and the capacitor and therefore needs not be considered for separate testing, as definitely no significant fraction of current needs to be expected through that circuitry.

9 SPD coordination testing

9.1 Energy coordination

Energy coordination is based on the maximum energy withstand of the second SPD. However, this energy is sometimes dependent upon the waveshape and the tests, as described in IEC 61643-12. Coordination is in most cases performed with only one waveshape (for example 8/20 for T2 SPDs). For this reason, it is better and easier to get this value E_{max} directly from the manufacturer (most of the time it is printed in the technical documentation).

Two values are necessary to define satisfactorily the energy withstand of an SPD:

– $E_{max\ S}$ for short-duration current waveshapes, for example, 8/20 (for T2 SPDs);

– $E_{max\ L}$ for long-duration current waveshapes, for example,10/350 (for T1 SPDs)

These two values $E_{max\ S}$ and $E_{max\ L}$ may be equal for some technologies.

The SPD is then characterized by two currents:

– I_n for short waves (as used for T2 SPDs) associated with the energy withstand $E_{max\ S}$ and

– I_{imp} for long waves (as used for T1 SPDs) associated with the energy withstand $E_{max\ L}$.

A simple SPD may then be tested as a T1 SPD and as a T2 SPD.

If I_{max} is declared by the manufacturer this value has to be considered for $E_{max\ S}$.

It is necessary to co-ordinate SPDs 1 and 2 using their maximum energy withstand E_{max} for the relevant surge waveshapes. That means that it is necessary to deal with two cases:

- coordination with long-duration waveshapes;
- coordination with short-duration waveshapes.

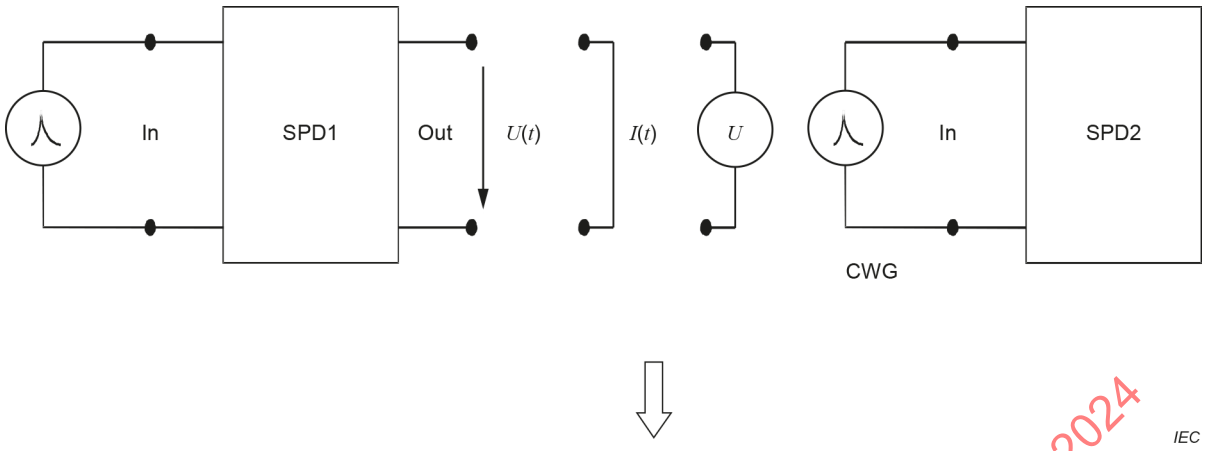
In general, coordination is easier to achieve with short waveshapes.

NOTE For switching SPDs it is necessary to deal also with a long front time. This matter is under consideration by the IEC.

9.2 Let-through energy (LTE) method

9.2.1 General

The energy coordination with standard impulse parameters, as described in IEC 62305-4, is a procedure to select and co-ordinate SPDs. The main advantage of this method is the possibility of considering an SPD like a black box (see Figure 24). Here, for a given surge at the input port not only the open-circuit voltage, but also an output current (for example, into a short circuit) is determined (principle of "let-through energy"). These output characteristics are converted into an equivalent "2 Ω-combination wave generator"-stress (open-circuit voltage 1,2/50, short-circuit current 8/20). The advantage is that there is no need for special knowledge of the internal design of the SPDs.



Conversion into a comparable standard impulse – 1,2/50, 8/20 with Z_i = 2 Ω.

U_{oc} SPD1/out ≤ U_{oc} SPD2/in

Key

U Load voltage

Figure 24 – LTE – Coordination method with standard pulse parameters

The aim of this coordination method is to make the input values of SPD2 (for example, discharge current) comparable to the output values of an SPD1 (for example, voltage protection level).

With stepped protection, it should be considered that the equivalent input hybrid impulse which can be discharged by the following SPD (without damage) is equal to, or higher than, the equivalent output hybrid impulse of the preceding SPD.

For reliable coordination, the equivalent hybrid impulse should be determined for the worst case of the stressing (I_{max}, U_{max}, let-through energy).

The worst case for the design of the decoupling element is given by a short circuit. But for coordination purposes this is too strenuous. It is more realistic to include a "load side voltage" (called hereafter "counter voltage").

The SPD downstream of a spark gap usually consists of a metal oxide varistors (MOV). The residual voltage of such an SPD is in any case higher than the peak value of the nominal power supply voltage (for example, in an AC system with a nominal voltage of 240 V the peak power voltage is $\sqrt{2}$ × 240 = 340 V, which is below the varistor voltage of the installed SPDs). This peak nominal power supply voltage corresponds to the lowest possible residual voltage of SPDs. Therefore, this peak voltage can be taken as the minimum possible counter voltage. Using the current in a short circuit instead of assuming a counter-voltage would result in an over-dimensioning of the decoupling element.

NOTE This method provides good results when the characteristics of SPD 1 are so different from those of SPD 2 that the surge conditions on SPD 2 are quasi impressed current conditions, for example in case of the coordination between a spark gap and an MOV, this condition is fulfilled.

Restrictions on the use of the method are as follows:

- to be sure to get a conservative result, the decoupling element should be included in the method as a part of the second SPD;
- to be sure to get a conservative result, the "counter-voltage" proposed should be equal to 0 where the second SPD contains a switching component;

- when the second SPD contains a switching component there is a possibility that the result is underestimated due to this method not being truly realistic in modelling the switching component. In such case, carefully consider the application of the method;
- the waveshape of the surge injected at the entrance of the installation should be considered as having a current waveshape and a voltage waveshape which are equal (10/350 or 8/20). The magnitude of the surge current i is in general known. The magnitude of a surge voltage U depends on the surge impedance of the system;
- the study should consider the tolerances on the SPD characteristics.

9.2.2 Method

The method described in this subclause in most cases gives a conservative value for the decoupling element (impedance) between the two SPDs. This means that, if such an impedance is installed between the two SPDs, the coordination will in most cases act better than predicted by the calculation.

The basis of this method is to represent the output of each SPD as an equivalent combination wave generator (CWG), defined by a no-load voltage U_{oc} 1,2/50 and a short-circuit current I_{sc} 8/20, the impedance of the generator being 2 Ω (U_{oc} = 2Ω × I_{sc}).

T3 SPDs are already tested by such a CWG. In the case of T2 SPDs it is necessary to consider that I_{sc} = I_n or I_{max} (if declared).

The upstream SPD may be tested as a T1 SPD in the case of direct lightning on the structure or as a T2 SPD.

The voltage at the output of each SPD will have in general a waveshape which is not directly connected to the waveshapes 1,2/50 and 8/20. It is then necessary to normalize the actual waveshapes in order to convert them in the 1,2/50 and 8/20 waves.

This is done by calculating the following values:

crest value of u = $\hat{u}$, $\int u\,dt$ and $\int u^2\,dt$ [$U(t)$ in Figure 22]

crest value of i = $\hat{\imath}$, $\int i\,dt$ and $\int i^2\,dt$ [$I(t)$ in Figure 22]

NOTE The same units are used in the formulae and in the tables.

These values are then used in Table 2.

Table 2 – Values to be calculated

Voltage	û	∫u dt	$\sqrt{\int u^2\,dt}$
Current	î	∫i dt	$\sqrt{\int i^2\,dt}$

The same table for a CWG with an amplitude of 1 V (Table 3) is:

Table 3 – Normalised division factors for a CWG

Voltage	1	70×10^{-6}	6×10^{-3}
Current	0.5	12×10^{-6}	2×10^{-3}

So dividing each cell of Table 2 by the equivalent cell of Table 3, we get a new table, Table 4:

Table 4 – Resulting calculation from Table 2 and Table 3

Voltage	û	∫u dt / (70 × 10^{-6})	$\sqrt{\int u^2 \, dt} / (6 \times 10^{-3})$
Current	î × 2	∫i dt / (12 × 10^{-6})	$\sqrt{\int i^2 \, dt} / (2 \times 10^{-3})$

The maximum value in Table 4 gives the value $U_{oc\ (CWG)}$, the equivalent value of U_{oc} of the CWG corresponding to the output of the SPD.

As soon as the downstream SPD has been tested as a T3 SPD with a CWG having a no-load voltage $U_{oc\ test}$ (or an equivalent CWG in case of T2 SPDs), it is possible to say immediately if the coordination is satisfactory. It is sufficient to check that $U_{oc\ test} > U_{oc\ CWG}$.

The value at the output of the SPD, for a given stress at the input, has to be calculated by using simulation software. It does not need to be calculated each time as such values may be calculated by the manufacturer. For each product, the manufacturer may calculate the output equivalent CWG impulse for a given stress (I_{imp} for T1 SPDs or I_n or I_{max} (if declared) for T2 SPDs or $U_{oc\ max}$ of the CWG for T3 SPDs) taking care both of the tolerances on the SPD characteristics and any blind spot (sometimes the most important stress at the output of the SPD is not given by the maximum values I_{imp}, I_n or I_{max} (if declared) and $U_{oc\ max}$ but for lower values).

9.3 Energy and voltage protection coordination method

9.3.1 General

In order to protect an electrical installation, the use of more than one SPD type is necessary depending on the overvoltage category of the equipment to be protected and on the wiring of the electrical installation (cable length, routing etc.). In this case effective SPD coordination should be examined to not overstress downstream SPDs and to limit the overvoltage level to a value lower than the withstand voltage of the equipment to be protected (this new criterion is called voltage protection level criterion and is described below). This subclause aims to provide few examples to achieve effective SPD coordination.

9.3.2 Coordination criteria

As presented above, coordination of SPDs requires the examination of two basic criteria, the energy criterion and the voltage protection level criterion.

Energy coordination can be achieved if, for all the values of the total incoming lightning/surge current, the portion of the energy that is dissipated through the upstream SPD is higher than the energy dissipated through the downstream SPD. Additionally, any elements between the upstream and the downstream SPDs should be able to withstand the same energy as the downstream SPDs.

Moreover, it is additionally proposed that the voltage protection level for the downstream SPDs should be equal or lower than the upstream SPDs, since they are situated nearer to the equipment to be protected, where more severe voltage protection is required.

The most significant parameters that should be considered during coordination of two SPDs are the following:

- SPD types (i.e. voltage switching – spark gap, voltage limiting – metal oxide varistor);
- characteristics of the SPD type (i.e. Sparkover voltage for spark gaps, maximum continuous operating voltage for MOVs, voltage protection level, maximum discharge current capability etc.);

- injected wave (i.e. 8/20, 10/350 etc.);
- type of the equipment to be protected (i.e. heavy inductive load, sensitive electronic etc.);
- separation distance between the two SPDs.

9.3.3 Coordination techniques

Prior to any coordination, certain steps should be followed to select the proper SPDs and the method of co-ordination between them.

- Step 1

  Identify the expected overvoltage level in absence of SPDs in order to select the type of SPD that will respond better. Reduction of fast overvoltages requires limiting SPDs rather than switching type. The identification of the overvoltages should be followed by the evaluation of the maximum energy of the prospective lightning/surge current in presence of an ideal SPD. Depending on the maximum energy level, the appropriate SPD type can be selected.

- Step 2

  Select upstream SPD according to the maximum energy that it can withstand.

- Step 3

  Select downstream SPD according to the desired voltage protection level of the equipment.

- Step 4

  For the selected SPDs both the energy and the voltage protection level criteria should be satisfied. This may be done mainly with the help of software simulations or with experimental testing. In this last case the following method could be used to check this out.

9.3.4 Coordination test

9.3.4.1 General

Coordination between SPDs is based on current sharing. Three parameters are defined as essential in establishing a coordination rule:

- the SPD themselves (one SPD is coordinated with another);
- the surge current at the entrance (fixed by upstream SPD's characteristics);
- The decoupling impedance *Z* between the 2 SPDs (the upstream and the downstream SPD).

The impedance *Z* between the two SPDs (in general an inductance) may be a physical one (a specific component inserted in the line to facilitate the sharing of the energy between the two SPDs) or represent the inductance of a length of cable between the two SPDs.

A SPD's coordination test can be performed by the SPDs manufacturer, by the installer or by the user.

Coordination of SPD is in most cases achieved if these two criteria are fulfilled:

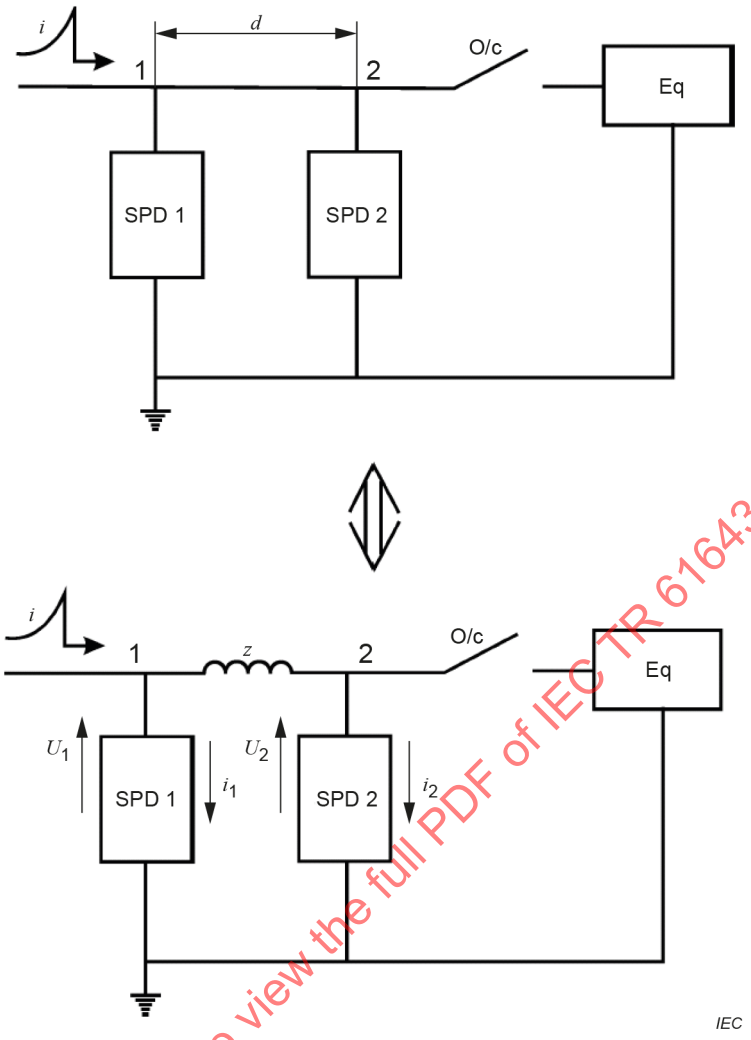
1) Energy co-ordination is achieved, if for all values of surge current from a minimum testing energy to a maximum testing energy (For T2 SPDs with 0,1, 0,25, 0,5, 0,75 and 1 time I_n and for T1 SPDs with 8/20 current impulses having a peak value equal to 0,1, 0,25, 0,5, 0,75 and 1 time I_{imp} and with 0,1, 0,25, 0,5, 0,75 and 1 time I_{imp} of the upstream SPD) the portion of energy, dissipated through SPD2 is lower or equal to its maximum energy withstand (E_{MAX2}).
2) Protection coordination is achieved, if for all values of surge current from a minimum testing energy to a maximum testing energy (For T2 SPDs with 0,1, 0,25, 0,5, 0,75 and 1 time I_n and for T1 SPDs with 8/20 current impulses having a peak value equal to 0,1, 0,25, 0,5,

0,75 and 1 time I_{imp} and with 0,1, 0,25, 0,5, 0,75 and 1 time I_{imp} of the upstream SPD) the residual voltage of SPD2 is lower or equal its declared voltage protection level U_p.

The testing with portion of the declared I_n or I_{imp} current is to explore if no blind spot up from low stress to maximum stress are existing. If I_{max} is declared for T2 SPDs I_n should be replaced by I_{max} and for T1 SPDs for the 8/20 current impulses the peak value should be equivalent to I_{imp}.

9.3.4.2 Test settings

SPDs arrangement for the coordination test is shown in Figure 25.



Key

Eq equipment to be protected in normal operation

O/c open circuit (equipment disconnected from supply)

i incoming surge

d distance between the connection points of SPD 1 and SPD 2

z impedance

1 Connection point of heading SPD (SPD 1)

2 Connection point of SPD 2

i_1 partial surge current through SPD 1

i_2 partial surge current through SPD 2

U_1 voltage drop across SPD 1

U_2 voltage drop across SPD 2

Figure 25 – SPDs arrangement for the coordination test

The connecting leads are disregarded and should be as short as possible and be similarly arranged for both SPDs. The external disconnectors, if any, are not considered in this coordination test.

When Z represents a physical impedance, the inductance of the line may be ignored due to its low value compared to Z. Z is then represented in a schematic way as in Figure 25 for both cases.

When Z represents the inductance of a length of cable between the two SPDs, the forward and return conductors have to be fixed following the manufacturer, installer or user declaration. If no specific arrangement, the forward and return conductors should not be twisted, at a distance of not more than 10 mm and creating a loop should be avoided.

The test should preferably be made on three sets of samples which have not been subjected previously to any tests.

Type of SPD coordination possibilities that may be tested under coordination procedure:

- Type 1 SPD coordinated with Type 2 SPD;
- Type 1 SPD coordinated with Type 3 SPD;
- Type 2 SPD coordinated with Type 2 SPD;
- Type 2 SPD coordinated with Type 3 SPD.

During the test, the SPD's system is energized at U_c with a short circuit current high enough to detect a failure of one of the SPDs under test (minimum 5 A). A current protection can be used in power supply branch, but not in surge current branch. If SPD 1 and SPD 2 are multi-mode SPDs for example with terminals for phase, neutral and ground (PE), all modes have to be tested L-N, N-PE and L-PE. In this case the remaining terminal(s) needs to be interconnected between SPD 1 and SPD 2.

When the upstream SPD is a T1 SPD, its declared I_{imp} is used for coordination procedure. If I_{max} is declared, the peak value for the 8/20 current impulses is equal to I_{imp} or I_{max}, whichever is greater.

When the upstream SPD is a T2 SPD, its declared I_n is used for coordination procedure. If I_{max} is declared, I_{max} is used for coordination procedure.

The coordination test procedure may be performed with 8/20 current impulses exceeding the discharge parameters of the downstream SPD only.

Positive current impulses are applied while the SPDs are energized to U_C at 60° after zero crossing in the positive voltage wave. The interval between the impulses should be long enough to allow the SPDs to cool down to ambient temperature.

Test procedure is summarized in Table 5, depending on the upstream SPD Type.

Table 5 – Test procedure for coordination

upstream SPD (SPD 1)	downstream SPD (SPD 2)	Test impulses
T1 SPD	T2 SPD or T3 SPD	with 8/20 current impulses having a peak value equal to 0,1, 0,25, 0,5, 0,75 and 1 time I_{imp} or I_{max} if declared, whichever is greater of the upstream SPD and with 0,1, 0,25, 0,5, 0,75 and 1 time I_{imp} of the upstream SPD
T2 SPD	T2 SPD or T3 SPD	with 0,1, 0,25, 0,5, 0,75, and 1 time In or I_{max} if declared, whichever is greater of the upstream SPD
NOTE The coordination test may be performed with 8/20 current impulses exceeding the discharge parameters of the downstream SPD only		

9.3.4.3 Conditions after test

Any follow current should be self-extinguished by the SPD and thermal stability be achieved after each impulse of the coordinated SPD test. Both the voltage and current records, together with a visual inspection, should show no indication of puncture or flashover of the samples. Mechanical damage should not occur during these tests.

The measured limiting voltage of the SPD2 should never exceed its declared U_P.

10 System level immunity testing

10.1 General

The following testing method can be used to evaluate overall system immunity level under lightning discharge conditions.

10.2 SPD discharge current test under normal service conditions:

a) Prior to the system level immunity test:

The immunity of the equipment to be protected should be determined. For equipment connected to power lines, IEC 60664-1 and IEC 61643-12 are used, and for equipment connected to telecom lines IEC 61643-22, ITU-T K.20, K.21 and K.45 are used.

The protection provided by the SPDs should be determined using test procedures described in the test and performance standards IEC 61643-x1.

b) The equipment to be protected should be tested with the SPDs installed per the manufacturer's instructions. The equipment should be energized at its nominal supply voltage and stressed with the nominal discharge current parameters rated for the SPD. Where applicable, additional circuits, such as communication lines, sensors, motors should be connected.

c) Figure 26 provides an example circuit of such an SPD discharge test under normal service conditions.

10.3 Induction test due to lightning currents:

a) Impulse currents should be injected into a metallic mounting plate in order to examine the behaviour of the complete system due to electromagnetic fields generated by the simulated lightning discharge.

b) The system under test is installed as realistically as possible. This simulated installation should include the equipment being protected; the installed SPDs and the real length and type of the interconnection lines.

c) The resulting induced impulse currents within the cabling of the complete system is monitored.

d) The characteristic and applicable values of the primary lightning current discharge should be as given in IEC 62305-1:2010, Table C.3.

e) Figure 27 provides an example of an induction test when T2 SPDs are installed on the power and control systems.

10.4 Recommended test classification of system level immunity (following IEC 61000-4-5):

This standard defines the following pass criteria:

a) Normal performance within limits specified by the manufacturers

b) Temporary loss of function or degradation of performance which ceases after the disturbance ceases and from which the equipment under test recovers its normal performance without operator intervention

c) Temporary loss of function or degradation of performance, the correction of which requires operator intervention

d) Loss of function or degradation of performance which is not recoverable owing to damage to hardware or software or loss of data.

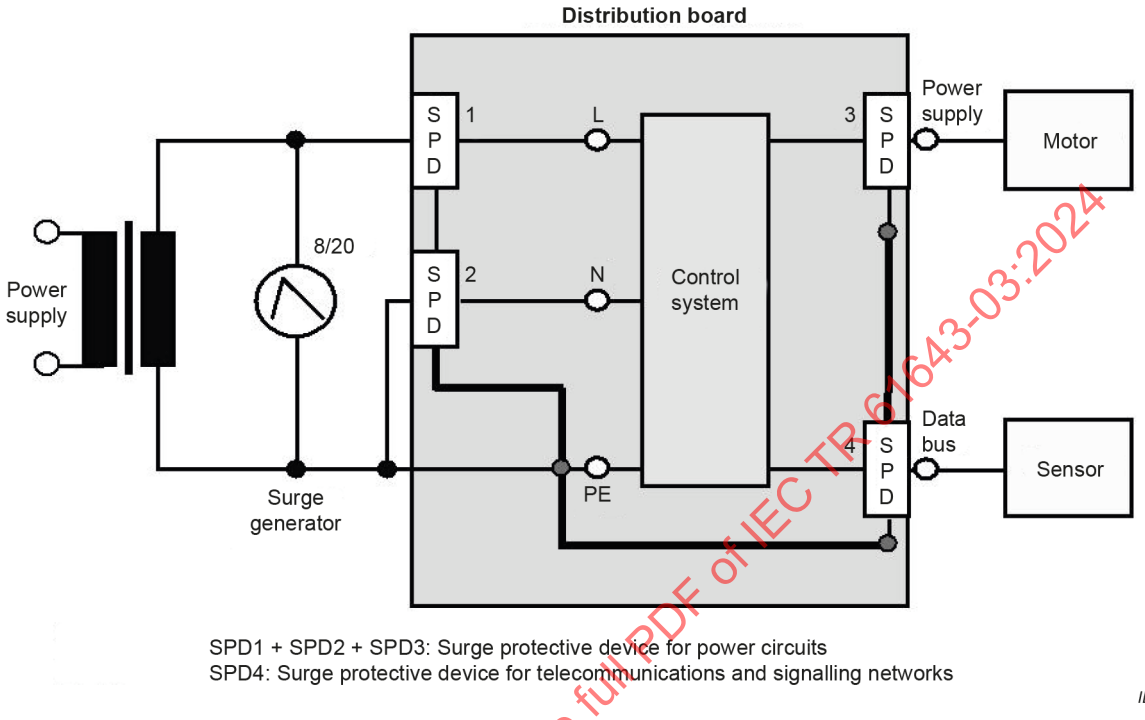


Figure 26 – Example of a circuit used to perform discharge current tests under normal service conditions

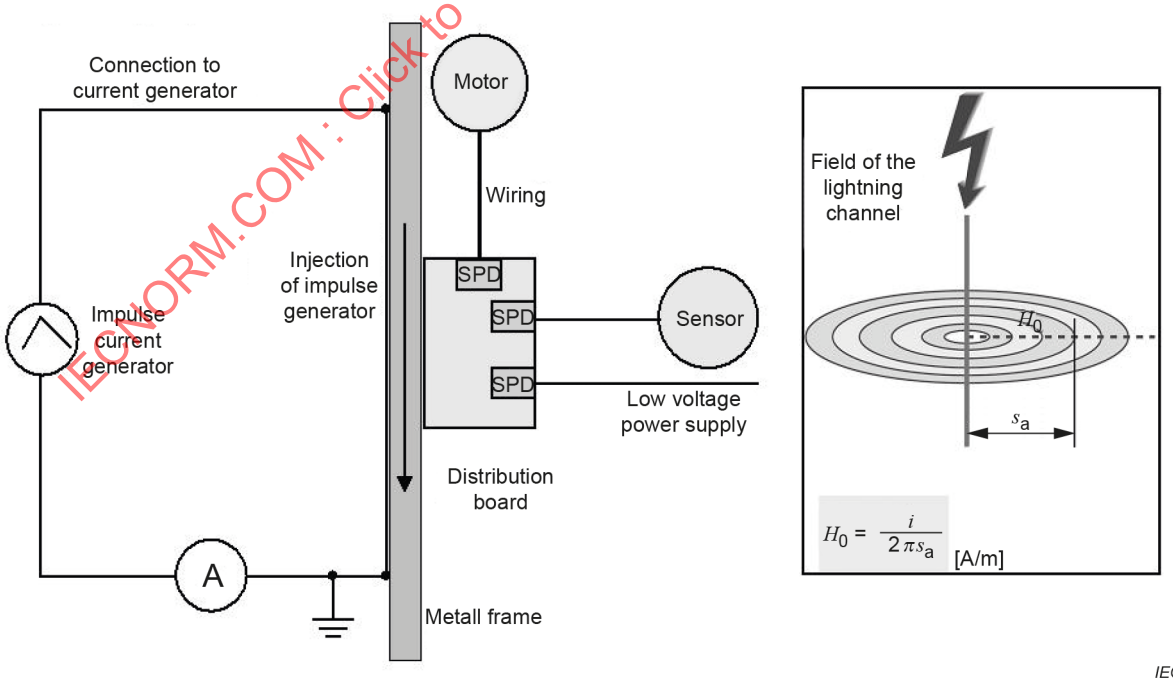


Figure 27 – Example circuit of an induction test due to lightning currents

Annex A
(informative)

Critical investigation on the impulse current specification for T1 SPDs when testing Metal Oxide Varistors

A.1 History and background

This annex contains the reprint of a report that resulted from comparison tests performed in 2006/2007 to gain a better understanding of the critical parameters when testing T1 SPDs containing metal oxide varistors.

NOTE The full report reference is provided in the bibliography.

A.2 General information

The standards IEC 61643-1 and EN 61643-11 are published and have been used for more than three years now. The impulse tests described for T1 SPDs within these documents are based on limited experience of some laboratories, who were able to perform such testing at the development stage of these test procedures. Since that time various generator designs have been developed and are in use within an increasing number of laboratories. These generators have been designed to meet the requirements given in the above mentioned standards.

Within the last two years some discussion started, initiated by inconsistent test results from different laboratories on some specific products. This resulted in the general question, if the generator description and tolerances given in the above mentioned standards are sufficient.

But whenever a detailed analysis started on the test results to be compared, it could quickly be shown that:

– the samples were taken from different batches/manufacturing lots
– the samples showed significant modifications in construction (electrode shape, connections etc.)
– the sample cooling between shots was not comparable etc.

Therefore, by end of year 2005, the idea came up to perform a comparative test on appropriate samples to find out, if the generator description and tolerances given are sufficient to provide comparable results, or if improvement is needed.

It was decided to use varistor samples (components with electrodes in epoxy coating) from a single batch and with very limited tolerance band, so that any influence of device construction can be eliminated as far as possible.

Further two different groups of samples were decided:

– single discs
– double blocks

to allow exclusion of influence of “varistor matching”, if consistency in results shows significant differences for single and double discs.

Every sample was individually assessed between and after the various steps of production at the manufacturing plant and was optically checked at CTI-Vienna. Samples were found to be homogenous and suitable for the program.

An interlaboratory comparison test (proficiency test program – PTP) with seven participants was carried out on a voluntary basis in 2006.

A.3 Test program and instructions

Reference standards are IEC 61643-1 Ed.2.0/2005 and EN 61643-11/2002 + A11/2006.

The sample connection was required to be done by avoiding any mechanical tension, excessive thermal stress or other stress to the samples.

Any dynamic stress on the samples and their connections due to passage of the test surge currents should have been prevented.

The tests were performed at normal ambient room temperature and conditions at 23 ± 5 °C.

The samples were required to cool down to less than 30 °C surface temperature after each surge application.

Samples have been considered as electrically or mechanically damaged if either the varistor voltage at 1 mA DC has decreased more than 10 % or if any mechanical destruction occurred.

Additional samples have been provided for adjustment puposes.

A.3.1 Detailed instructions

A.3.1.1 Initial measurements and checks

– Check the samples for any mechanical damage.

– Measurement of the varistor voltage at 1 mA d.c. in both polarities and at normal ambient room temperature, while the power source provides a smooth dc. voltage output.

A.3.1.2 Impulse tests single discs

– First sample:

  Test class I impulse currents (10/350) of positive polarity are applied to the sample, starting with 3 kA.

  This current is increased in steps of 1 kA till electrical and/or mechanical destruction occurs.

  The impulse current and the residual voltage at the sample are recorded.

  The $\int I*t$-value and the $\int I^2*t$-value are calculated

  After each impulse application the sample should cool down to less than 30 °C surface temperature and the measurement of the varistor voltage at 1 mA d.c. is repeated in both polarities. The time interval between the impuls applications is recorded.

– Second and third sample:

  Test class I impulse currents (10/350) of positive polarity are applied to the sample, starting with an impulse current 2 kA below the value, at which destruction of the first sample occurred.

  This current is increased in steps of 1 kA till electrical and/or mechanical destruction occurs.

  The impulse current and the residual voltage at the sample are recorded.

  The $\int I*t$-value and the $\int I^2*t$-value are calculated

  After each impulse application the sample should cool down to less than 30 °C surface temperature and the measurement of the varistor voltage at 1 mA d.c. is repeated in both polarities. The time interval between the impuls applications is recorded.

A.3.1.3 Impulse tests double blocks

– First sample:

Test class I impulse currents (10/350) of positive polarity are applied to the sample, starting with 6 kA.

This current is increased in steps of 2 kA till electrical and/or mechanical destruction occurs.

The impulse current and the residual voltage at the sample are recorded.

The $\int I^*t$-value and the $\int I^2*t$-value are calculated

After each impulse application the sample should cool down to less than 30 °C surface temperature and the measurement of the varistor voltage at 1 mA d.c. is repeated in both polarities. The time interval between the impuls applications is recorded.

– Second and third sample:

Test class I impulse currents (10/350) of positive polarity are applied to the sample, starting with an impulse current 4 kA below the value, at which destruction of the first sample occurred.

This current is increased in steps of 1 kA till electrical and/or mechanical destruction occurs.

The impulse current and the residual voltage at the sample are recorded.

The $\int I^*t$-value and the $\int I^2*t$-value are calculated

After each impulse application the sample should cool down to less than 30 °C surface temperature and the measurement of the varistor voltage at 1 mA d.c. is repeated in both polarities. The time interval between the impuls applications is recorded.

A.4 Details and results of interlaboratory comparison tests

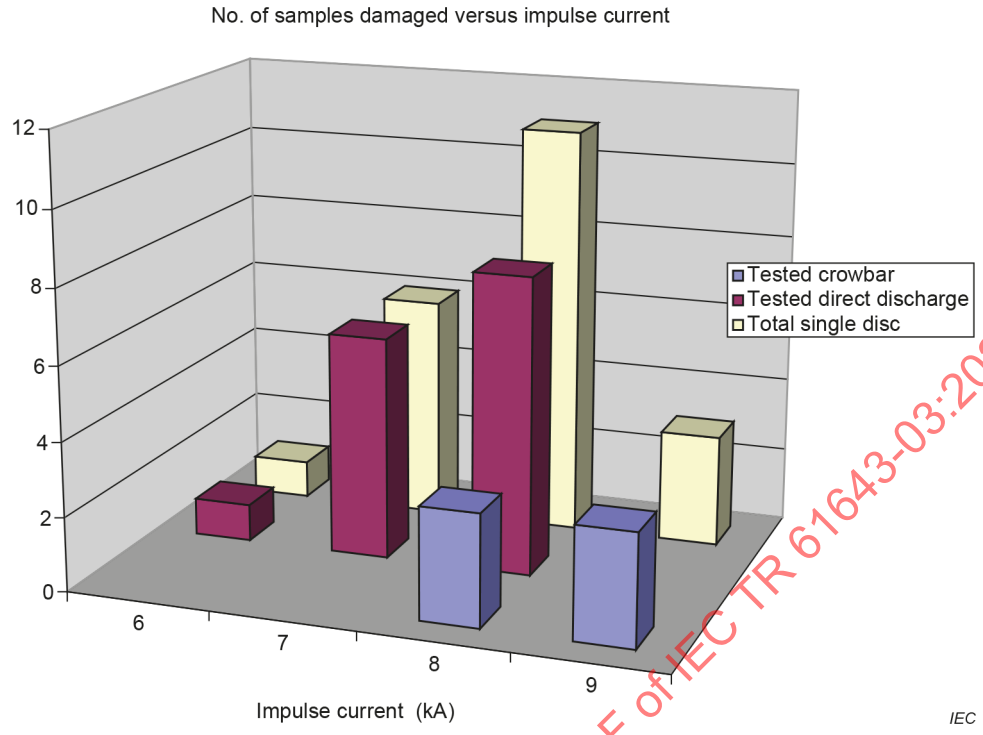
Four participants performed the tests using a so called direct discharge generator, one participant used a so called crowbar generator and two participants used a direct discharge generator arrangement up to a certain impuls current amplitude and a crowbar generator arrangement above that amplitude.

The direct discharge setups deliver almost a double exponential current waveshape through the sample and show approximate front times between 6 µs and 15 µs. The crowbar setups deliver almost a triangular current waveshape through the sample and show approximate front times between 21 µs and 45 µs.

Five participants used a Pearson current transformer and two participants used a coaxial shunt for impulse current measurements.

Six participants used voltage probes of various brands and one participant used a voltage devider.

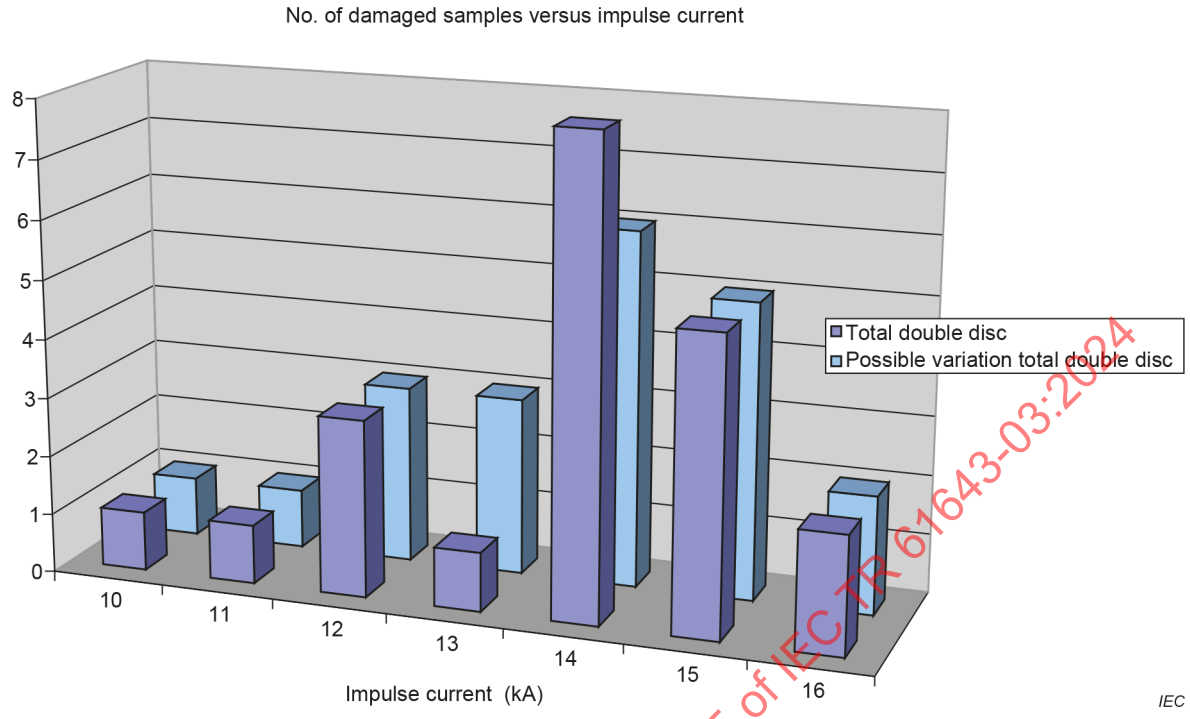
A.4.1 Single disc results

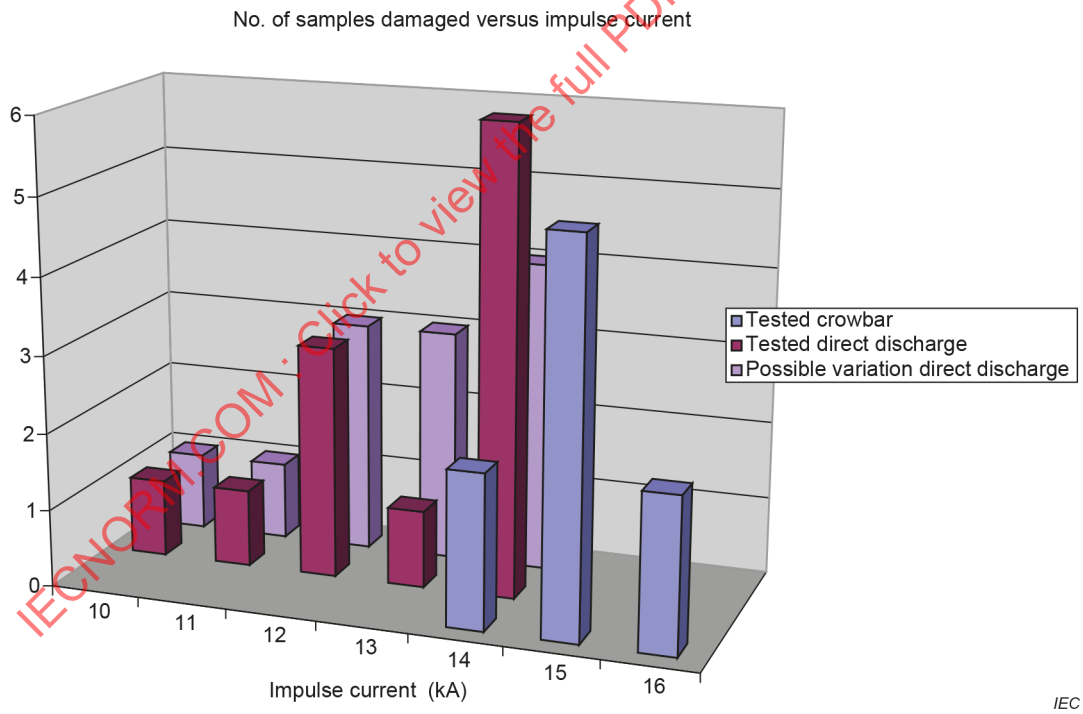


All samples (except one) tested with direct discharge generators did not show significant degradation before the last destructive impulse was applied.

All samples tested with crowbar generators showed degradation ≥7 % after the last impulse application before the destructive one.

A.4.2 Double block results





The data bars "Possible variation Total Double Disc" and "Possible variation direct discharge" refer to the fact that one laboratory skipped the tests at 13 kA on the double disc samples which possibly influenced the results towards two more damages at 14 kA.

All samples tested with direct discharge generators did not show significant (≤2 %) degradation before the last destructive impulse was applied.