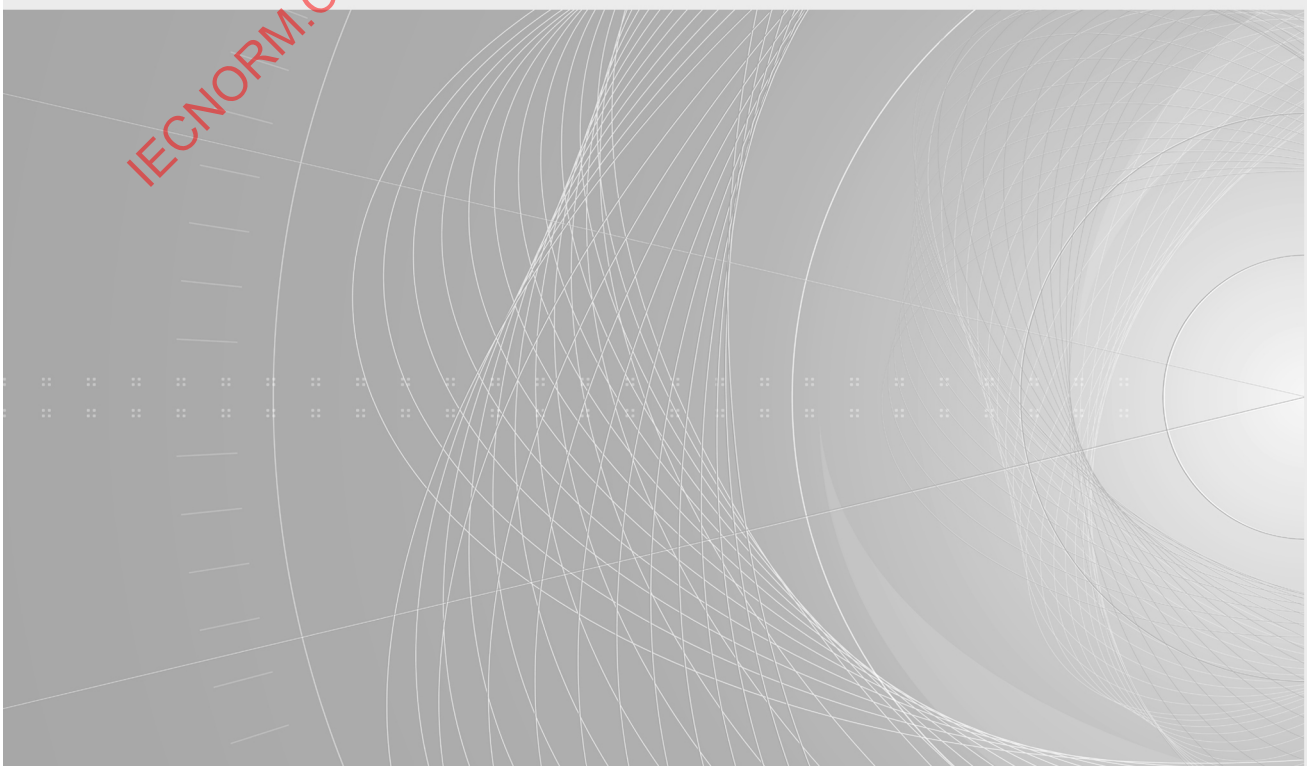
IEC TR 60146-1-2

Edition 5.0 2019-10

TECHNICAL REPORT

Semiconductor converters – General requirements and line commutated converters –
Part 1-2: Application guide



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Semiconductor converters – General requirements and line commutated converters –
Part 1-2: Application guide

INTERNATIONAL
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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR CONVERTERS – GENERAL REQUIREMENTS AND LINE COMMUTATED CONVERTERS –

Part 1-2: Application guidelines

FOREWORD

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IEC TR 60146-1-2, which is a Technical Report, has been prepared by IEC technical committee 22: Power electronic systems and equipment.

This fifth edition cancels and replaces the fourth edition published in 2011. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) addition of annexes concerning the applications of converter transformers and of fuses for overcurrent protection;

b) changes of calculation methods related the inductive voltage regulation and changes of description on transformer losses to be consistent with the latest transformer standards;

c) addition and updates of references based on the latest information.

The text of this Technical Report is based on the following documents:

Draft T	Report on voting
22/306/DTR	22/310/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 60146 series, under the general title *Semiconductor converters – General requirements and line commutated converters*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this standard may be issued at a later date.

SEMICONDUCTOR CONVERTERS – GENERAL REQUIREMENTS AND LINE COMMUTATED CONVERTERS –

Part 1-2: Application guidelines

1 Scope

This part of IEC 60146, which is a Technical Report, gives guidance on variations to the specifications given in IEC 60146-1-1:2009 to enable the specification to be extended in a controlled form for special cases. Background information is also given on technical points, which facilitates the use of IEC 60146-1-1:2009.

This document primarily covers line commutated converters and is not in itself a specification, except as regards certain auxiliary components, in so far as existing standards may not provide the necessary data.

This document will not take precedence on any product specific standard according to the concept shown in IEC Guide 108. IEC Guide 108 provides the information on the relationship between horizontal standards and product publications.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-551, *International Electrotechnical Vocabulary – Part 551: Power electronics* (available at www.electropedia.org)

IEC 60050-551-20, *International Electrotechnical Vocabulary – Part 551-20: Power electronics – Harmonic analysis* (available at www.electropedia.org)

IEC 60146-1-1:2009, *Semiconductor converters – General requirements and line commutated converters – Part 1-1: Specification of basic requirements*

IEC 60269-1:2006, *Low-voltage fuses – Part 1: General requirements*

IEC 60269-4:2009, *Low-voltage fuses – Part 4: Supplementary requirements for fuse-links for the protection of semiconductor devices*

IEC 60529, *Degrees of protection provided by enclosures (IP Code)*

IEC 60664-1, *Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests*

IEC 61148, *Terminal markings for valve device stacks and assemblies and for power conversion equipment*

IEC 61378-1:2011, *Convertor transformers – Part 1: Transformers for industrial applications*

IEC/IEEE 60076-57-129, *Power transformers – Part 57-129: Transformers for HVDC applications*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60146-1-1:2009, IEC 60050-551, IEC 60050-551-20 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

NOTE Several terms from IEC 60146-1-1:2009, IEC 60050-551, IEC 60050-551-20 are repeated here for convenience.

3.1 Terms and definitions related to converter faults

3.1.1
breakthrough
failure by which a controllable valve device or an arm consisting of such devices loses its ability to block voltage during the forward blocking interval

Note 1 to entry: See Figure 1a). Breakthrough can occur in rectifier operation as well as inverter operation and for various reasons, for example excessive junction temperature, voltage surges in excess of rated peak off-state voltage, excessive rate of rise of off-state voltage or spurious gate current.

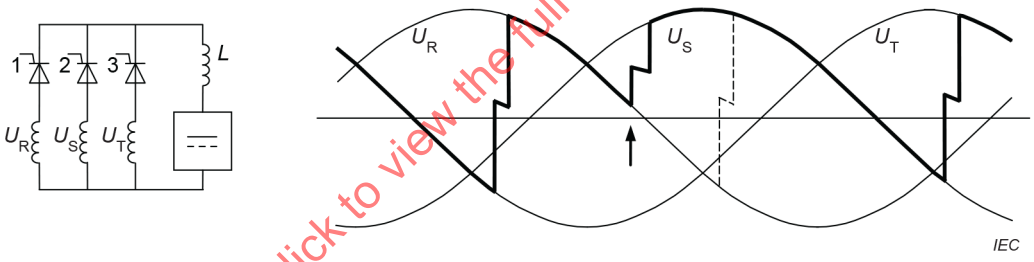


Figure 1a) Breakthrough in arm 2

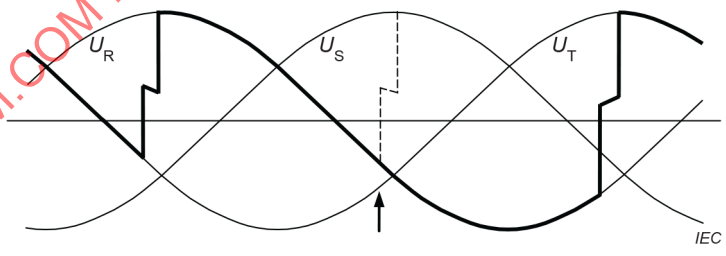


Figure 1b) Firing failure in arm 2

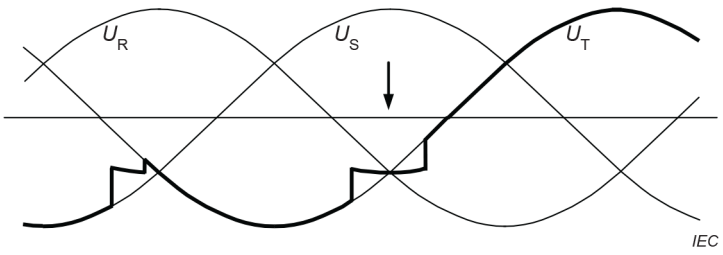


Figure 1c) Conduction through related to arm 3

Figure 1 – Voltages at converter faults

[SOURCE: IEC 60050-551:1998, 551-16-60, modified – Note 1 to entry has been added.]

3.1.2
false firing
firing of a latching valve device or an arm consisting of such devices at an incorrect instant

[SOURCE: IEC 60050-551:1998, 551-16-63]

3.1.3
breakdown
<of an electronic valve device or of a valve arm> failure that permanently deprives an electronic valve device or a valve arm of its property to block voltage

[SOURCE: IEC 60050-551:1998, 551-16-66]

3.1.4
firing failure
failure to achieve conduction in a latching valve device or an arm consisting of such devices during the conduction interval

Note 1 to entry: See Figure 1b).

[SOURCE: IEC 60050-551:1998, 551-16-65, modified – Note 1 to entry has been added.]

3.1.5
conduction through
situation where, in inverter operation, a valve arm continues conduction at the end of the normal conduction interval or at the end of the hold-off interval

Note 1 to entry: See Figure 1c).

[SOURCE: IEC 60050-551:1998, 551-16-64, modified – The definition has been rephrased, and Note 1 to entry has been added.]

3.1.6
commutation failure
failure to commutate the current from a conducting arm to the succeeding arm

[SOURCE: IEC 60050-551:1998, 551-16-59]

3.2 Terms and definitions related to converter generated transients

3.2.1
DC side transients
voltage transients produced by rapid changes of the DC voltage applied to the inductance and capacitance of the DC circuit

Note 1 to entry: See 7.4.

3.2.2
commutation transients on the line
voltage transients produced on the AC line after commutation

Note 1 to entry: See 7.4.

Note 2 to entry: The commutation transients are repetitive.

3.3 Terms and definitions related to temperature

3.3.1
thermal resistance
R_{th}
quotient of the difference between the virtual junction temperature and the temperature of a specified external reference point, by the steady-state power dissipation in the device under conditions of thermal equilibrium

Note 1 to entry: For most cases, the power dissipation can be assumed to be equal to the heat flow.

3.3.2
transient thermal impedance
Z_{th}
quotient of

a) variation of the temperature difference, reached at the end of a time interval between the virtual junction temperature and the temperature of a specified external reference point, and

b) step function change of power dissipation at the beginning of the same time interval causing the change of temperature

Note 1 to entry: Immediately before the beginning of this time interval, the distribution of temperature should have been constant with time.

Note 2 to entry: Transient thermal impedance is given as a function of the time interval.

3.3.3
virtual equivalent junction temperature
virtual junction temperature
T_j
virtual temperature of the junction of a semiconductor device

Note 1 to entry: The virtual junction temperature is not necessarily the highest temperature in the semiconductor device.

Note 2 to entry: Based on the power dissipation and the thermal resistance or transient thermal impedance that corresponds to the mode of operation, the virtual junction temperature can be calculated using a specified relationship.

[SOURCE: IEC 60050-521:2002, 521-05-15, modified – The symbol T_j has been added, as well as the notes to entry.]

3.3.4
virtual temperature
internal equivalent temperature
<of a semiconductor device> theoretical temperature which is based on a simplified representation of the thermal and electrical behaviour of the semiconductor device

[SOURCE: IEC 60050-521:2002, 521-05-14, modified – The notes to entry have been deleted.]

4 Application of semiconductor power converters

4.1 Application

4.1.1 General

Semiconductor power converters are used in most industries for the conversion of electrical power and also to facilitate the conversion of mechanical, chemical or other energy into electrical power and vice versa.

They also used in electrical power utilities for the supply source conditioning.

4.1.2 Conversion equipment and systems

Examples of applications of conversion equipment and systems are as follows, and not limited in these applications:

a) DC load, stabilized/adjustable voltage/current control;
b) AC power controllers (AC or DC output);
c) AC variable frequency:
   – line-commutated converters;
   – slip energy recovery;
   – machine-commutated converters;
   – self-commutated converters:
      • voltage stiff (voltage source);
      • current stiff (current source);
d) adjustable speed drives (covered by specific IEC standards, e.g. IEC 61800-1);
e) uninterruptible power systems (UPS, covered by specific IEC standards, e.g. IEC 62040-3);
f) chemical processes (electrolysis, electroplating, electrophoresis);
g) computer power supplies;
h) traction substations, railways, tramways, mines, electric vehicles;
i) telephone power supplies;
j) electromagnets, field supplies;
k) radio transmitter DC supplies;
l) arc furnace DC power supplies;
m) solar photovoltaic energy conversion.

4.1.3 Supply source conditioning (active and reactive power)

Examples of supply source conditioning are as follows, and not limited in these applications:

a) HV or MV systems (transmission and distribution, reactive power compensation);
b) LV systems (energy saving);
c) isolated, standby or dispersed generating plants;
d) DC or AC supplies particularly from solar, wind or chemical energy.

NOTE Some of the applications listed above are the subject of particular IEC publications now existing or in preparation.

4.2 Equipment specification data

4.2.1 Main items on the specification

See 6.6.2 of IEC 60146-1-1:2009 on rating plates.

4.2.2 Terminal markings

IEC 61148 shall apply.

4.2.3 Additional information

4.2.3.1 General

In addition to the essential data such as should appear on the rating plate as specified in IEC 60146-1-1:2009, the following list may prevent other important information being omitted from the specification, concerning the purchaser's requirements or the supplier's product.

4.2.3.2 Supply source

The following information is necessary to confirm the supply source conditions:

a) voltage and frequency (if applicable); range of rated values, unbalance, short time outage;
b) short-circuit power (or description of cables, lines and transformers): minimum, statistical average, maximum values;
c) other existing loads (motors, capacitors, furnaces, etc.);
d) limits of disturbances (reactive power, current harmonics, etc. prevailing or permitted);
e) type of earthing.

4.2.3.3 Output specification

The following information is required to design the converter connection and its control:

a) output voltage and frequency (if applicable);
b) required range of variation (continuous or stepwise);
c) voltage and/or current reversing capability (quadrant(s) of operation);
d) limits of permitted voltage/current/frequency variation;
e) character of load;
f) type of earthing;
g) distortion of the output waveforms.

4.2.3.4 Environment specification

The following information is required to design the cooling, structure, cubicle and so on of the converter:

a) temperate, tropical, arctic climates;
b) temperature, humidity, dust content (unless otherwise specified, IEC 60664-1, degree 1, is applicable);
c) unusual service conditions;
d) outdoor/indoor installation;
e) protection class (according to IEC 60529);
f) compliance with specific standards (IEC or others, including safety standards).

4.2.3.5 Electrical service conditions

The following information might be duplicated with above information, but should be given to confirm the details.

a) Supply bus category:
   – converter dedicated system (converters only);
   – general purpose system (includes AC motor loads);
   – high quality system (supplying loads with low immunity level such as computers, medical instrumentation etc.).

b) Immunity class of the equipment: a different immunity class may be selected for one or more parameters.

4.2.4 Unusual service conditions

4.2.4.1 General

For the normal service conditions, refer to IEC 60146-1-1:2009, 5.2.1. In case of unusual service conditions, a special agreement between purchaser and supplier should be made according to IEC 60146-1-1:2009, 5.2.4.

4.2.4.2 Cooling medium temperature difference

For the cooling medium temperature, it is noted that the temperature range of the normal service conditions is different between the converter and the transformer. Refer to IEC 61378-1:2011, 4.2, for the normal service conditions of the converter transformer.

4.2.4.3 Dust and solid particle content

For particular applications, the degree of pollution may be specified separately, according to IEC 60664-1 or other relevant IEC publications, for example specifying pollution classes other than degree 1 as specified in IEC 60664-1.

4.3 Converter transformers and reactors

IEC 61378-1 and IEC/IEEE 60076-57-129 shall be referred. IEC 61378-3 should be referred.

4.4 Calculation factors

4.4.1 General

Calculation factors are shown in Table 1 for each converter connection. For letter symbols and definitions, refer to 4.2 of IEC 60146-1-1:2009 and 4.6.2.

Table 1 – Connections and calculation factors *(1 of 4)*

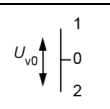
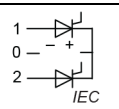
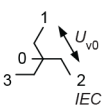
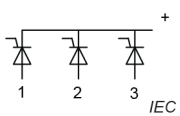
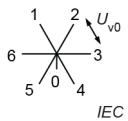
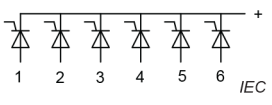
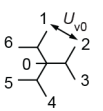
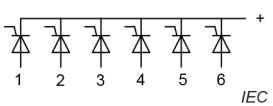
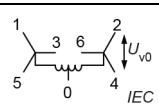
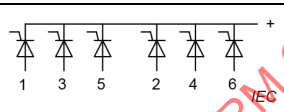
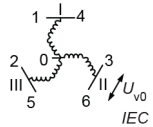
No.	Transformer connection		Converter connection	p [a]	q [a]	Line side fundamental current factor [b,d] I'_{1L} / I_d	Line side current factor [b] I'_L / I_d	Valve side current factor [c] I_v / I_d	$\frac{U_{di}}{U_{v0}}$	$\frac{U_{iM}}{U_{di}}$	$\frac{\delta q s}{g}$	Terminals to be short-circuited for short-circuit measurement [d]			Transformer guaranteed load losses [d]	Transformer guaranteed short-circuit impedance [d]
	Line side	Valve side										A	B	C		
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Single converter, single-way connections																
1				2	2	-	0,5	0,707 $\left(\frac{1}{\sqrt{2}}\right)$	0,450 $\left(\frac{\sqrt{2}}{\pi}\right)$	3,14 (π)	2		-	-	-	-
2				3	3	-	0,471 $\left(\frac{\sqrt{2}}{3}\right)$	0,577 $\left(\frac{1}{\sqrt{3}}\right)$	0,675 $\left(\frac{3}{\pi\sqrt{2}}\right)$	2,09 $\left(\frac{2\pi}{3}\right)$	3		-	-	-	-
3				6	6	-	0,816 $\left(\sqrt{\frac{2}{3}}\right)$	0,408 $\left(\frac{1}{\sqrt{6}}\right)$	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	2,09 $\left(\frac{2\pi}{3}\right)$	6		-	-	-	-
4				6	6	-	0,816 $\left(\sqrt{\frac{2}{3}}\right)$	0,408 $\left(\frac{1}{\sqrt{6}}\right)$	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	2,09 $\left(\frac{2\pi}{3}\right)$	6		-	-	-	-
5				6	3	$\frac{\sqrt{3}}{\pi\times\sqrt{2}}$ (≈ 0,390)	0,408 $\left(\frac{1}{\sqrt{6}}\right)$	0,289 $\left(\frac{1}{2\sqrt{3}}\right)$	0,675 $\left(\frac{3}{\pi\sqrt{2}}\right)$	2,42 $\left(\frac{4\pi}{3\sqrt{3}}\right)$	3/2	1-3-5	2-4-6	-	$\frac{P_A + P_B}{2}$	e_{XA} and e_{XB}
6				6	2	-	0,272 $\left(\frac{1}{3}\sqrt{\frac{2}{3}}\right)$	0,236 $\left(\frac{1}{3\sqrt{2}}\right)$	0,450 $\left(\frac{\sqrt{2}}{\pi}\right)$	3,14 (π)	2/3	-	-	-	-	-

Table 1 *(2 of 4)*

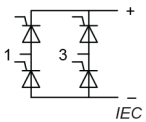
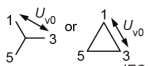
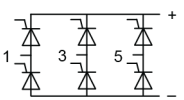
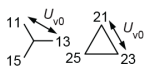
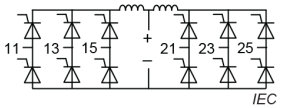
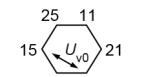
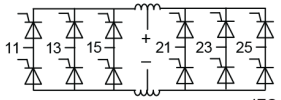
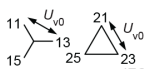
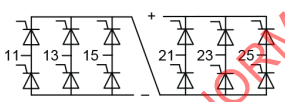
No.	Transformer connection		Converter connection	p [a]	q [a]	Line side fundamental current factor [b,d] I'_{1L} / I_d	Line side current factor [b] I'_L / I_d	Valve side current factor [c] I_v / I_d	$\frac{U_{di}}{U_{v0}}$	$\frac{U_{iM}}{U_{di}}$	$\frac{\delta qs}{g}$	Terminals to be short-circuited for short-circuit measurement [d]			Transformer guaranteed load losses [d]	Transformer guaranteed short-circuit mpedance [d]
	Line side	Valve side										A	B	C		
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Single converter, uniform double-way connections																
7				2	2	-	1	1	0,900 $\left(\frac{2\sqrt{2}}{\pi}\right)$	1,57 $\left(\frac{\pi}{2}\right)$	4	-	-	-	-	-
8				6	3	$\frac{\sqrt{6}}{\pi}$ ($\approx$0,78)	0,816 $\left(\sqrt{\frac{2}{3}}\right)$	0,816 $\left(\sqrt{\frac{2}{3}}\right)$	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	1,05 $\left(\frac{\pi}{3}\right)$	6	1-3-5			P_A	e_{XA}
9				12	3	$\frac{\sqrt{6}}{\pi}$ ($\approx$0,78)	0,789 $\left(\frac{1+\sqrt{3}}{2\sqrt{3}}\right)$	0,408 $\left(\frac{1}{\sqrt{6}}\right)$	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	1,05 $\left(\frac{\pi}{3}\right)$	3	11-13-15	21-23-25	11-13-15 and 21-23-25	P_C	e_{XA} and e_{XB}
10	Same as 9, but with two different transformers		Same as 9	12	3	$\frac{\sqrt{6}}{\pi}$ ($\approx$0,78)	0,789 $\left(\frac{1+\sqrt{3}}{2\sqrt{3}}\right)$	0,408 $\left(\frac{1}{\sqrt{6}}\right)$	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	1,05 $\left(\frac{\pi}{3}\right)$	3	11-13-15	21-23-25		P_A+P_B	e_{XA} and e_{XB}
11				12	3	-	0,789 $\left(\frac{1+\sqrt{3}}{2\sqrt{3}}\right)$	0,408 $\left(\frac{1}{\sqrt{6}}\right)$	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	1,05 $\left(\frac{\pi}{3}\right)$	3	-	-	-	-	-
12				12	3	$\frac{2\times\sqrt{6}}{\pi}$ ($\approx$1,559)	1,577 $\left(\frac{1+\sqrt{3}}{\sqrt{3}}\right)$	0,816 $\left(\sqrt{\frac{2}{3}}\right)$	2,70 $\left(\frac{6\sqrt{2}}{\pi}\right)$	0,524 $\left(\frac{\pi}{6}\right)$	12	11-13-15	21-23-25	11-13-15 and 21-23-25	P_C	e_{XA} and e_{XB}
13	Same as 12, but with two different transformers		Same as 12	12	3	$\frac{2\times\sqrt{6}}{\pi}$ ($\approx$1,559)	1,577 $\left(\frac{1+\sqrt{3}}{\sqrt{3}}\right)$	0,816 $\left(\sqrt{\frac{2}{3}}\right)$	2,70 $\left(\frac{6\sqrt{2}}{\pi}\right)$	0,524 $\left(\frac{\pi}{6}\right)$	12	11-13-15	21-23-25		P_A+P_B	e_{XA} and e_{XB}

Table 1 *(3 of 4)*

No.	Transformer connection		Converter connection	p [a]	q [a]	Line side fundamental current factor [b,d] I'_{1L} / I_d	Line side current factor [b] I'_L / I_d	Valve side current factor [c] I_v / I_d	$\frac{U_{di}}{U_{v0}}$	$\frac{U_{iM}}{U_{di}}$	$\frac{\delta q s}{g}$	Terminals to be short-circuited for short-circuit measurement [d]			Transformer guaranteed load losses [d]	Transformer guaranteed short-circuit impedance [d]
	Line side	Valve side										A	B	C		
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Single converter, non-uniform double-way connections																
14	IEC	U_{v0} 1 3 IEC	+ 1 3 – + 1 3 – IEC	2	2	-	$\sqrt{\frac{\pi-\alpha}{\pi}}$	$\sqrt{\frac{\pi-\alpha}{\pi}}$	0,900 $\left(\frac{2\sqrt{2}}{\pi}\right)$	1,57 $\left(\frac{\pi}{2}\right)$	-	-	-	-	-	-
15	or IEC	1 U_{v0} 3 5 or 1 U_{v0} 5 3 IEC	1 3 5 + – IEC	6	3	-	See 4.4.3	See 4.4.4	1,35 $\left(\frac{3\sqrt{2}}{\pi}\right)$	1,05 $\left(\frac{\pi}{3}\right)$	-	-	-	-	-	-
Double converter connections																
16	or IEC	1 3 6 2 b0 U_{v0} 5 a0 4 IEC	b0 1 3 5 2 4 6 a0 IEC	See connection No. 5												
17	or IEC	U_{v0} 6 3 5 0 4 IEC	1 3 5 2 4 6 1 3 5 2 4 6 IEC	See connection No. 5												
18	or IEC	or 11 21 U_{v0} 13 23 15 25 11 21 U_{v0} 15 13 25 23 IEC	11 13 15 21 23 25 IEC	See connection No. 8												
19	or IEC	U_{v0} 1 3 5 or 1 U_{v0} 5 3 IEC	1 3 5 1 3 5 IEC	See connection No. 8												

Table 1 *(4 of 4)*

[a] Refer to IEC 60146-1-1:2009, Table 2.
[b] Refer to transformer primary with voltage ratio 1.
[c] Refer to transformer secondary.
[d] IEC 61378-1:2011, Table 1, does not contain the information for the lines 1 to 4, 6, 7, 11, 14 and 15. Then, the cells which are not given relevant values are filled with hyphen "-". When the values are necessary, refer to the textbooks for the converter theory. Some information can be obtained from Annex C.

4.4.2 Voltage ratios

Table 1 gives the ratios:

column 10	column 11
$\frac{U_{di}}{U_{v0}}$	$\frac{U_{iM}}{U_{di}}$

where

U_{di} is the ideal no-load direct voltage;

U_{v0} is the no-load transformer valve winding voltage;

U_{iM} is the ideal crest no-load voltage, appearing between the end terminals of an arm neglecting internal and external voltage drops in valves, at no load. The ratio remains the same at light load current close to the transition current.

NOTE For connections No. 5, No. 11 and other connections employing interphase transformers, the ratio U_{iM}/U_{di} increases at no-load.

4.4.3 Line side transformer current factor

The quotient of the RMS value I'_L of the current on the line side and the direct current I_d is indicated in Table 1, column 8, on the assumption of smooth direct current, rectangular waveshape of the alternating currents and on the following voltage ratio for single or double-way connections:

$$\frac{U_L}{U_{v0}} = 1$$

where

U_L is the phase-to-phase voltage on the line side;

U_{v0} is the voltage between two commutating phases on the valve side.

For different values of the voltage ratio, the line side current is approximately:

$$I_L = I'_L \times \frac{U_{v0}}{U_L}$$

NOTE For connections 14 and 15, the line side current factor depends on the trigger delay angle α as follows:

$0 < \alpha < \frac{\pi}{3}$; $\quad \frac{I'_L}{I_d} = \sqrt{\frac{2}{3}} \approx 0{,}816$

$\frac{\pi}{3} < \alpha < \pi$; $\quad \frac{I'_L}{I_d} = \sqrt{\frac{\pi - \alpha}{\pi}}$

4.4.4 Valve-side transformer current factor

The quotient of the RMS value I_v of the valve-side current in each terminal of the transformer and the direct current I_d is indicated in Table 1, column 9.

NOTE For connections 14 and 15, the valve-side current factor depends on the trigger delay angle α as follows:

$0 < \alpha < \frac{\pi}{3}$; $\quad \frac{I_v}{I_d} = \sqrt{\frac{2}{3}} \approx 0{,}816$

$\frac{\pi}{3} < \alpha < \pi;$ $\frac{I_v}{I_d} = \sqrt{\frac{\pi - \alpha}{\pi}}$

4.4.5 Inductive direct voltage regulation due to transformer

Table 1, column 12, gives the parameter: $\frac{\delta qs}{g}$

The parameter is used to calculate the inductive voltage regulation due to the converter transformer as described in 4.7.2.4.

NOTE The ratio (d_{xtN}/e_{xN}) in IEC 60146-1-2:2011 was removed since it uses transformer impedance value which the converter transformer standards, IEC 61378 series, do not support. Furthermore, it is not evaluated to be practical to use since the ratio is too complicated to understand. In order to show the complexity, the ratio is analysed in Annex C just for information.

4.4.6 Magnetic circuit

The magnetic circuits corresponding to the connections supplied with three-phase currents in Table 1 are assumed to have three legs.

4.4.7 Transformer guaranteed load losses

The symbols P_A, P_B and P_C in column 16 indicate the losses measured in each short-circuit combination A, B or C in columns 13, 14 and 15, respectively (see IEC 61378-1:2011, 7.5.1).

The contents of columns 13 to 16 of Table 1 are provided for information purpose. For the loss of the converter transformer, IEC 61378 (all parts) should be referred to.

According to IEC 61378-1:2011, 5.2 and 6.1, the transformer guaranteed load losses is the load losses measured with the rated fundamental current in short-circuit conditions indicated in columns 13 to 15 of Table 1.

The actual load loss in service includes additional loss due to non-sinusoidal converter current. This value shall be calculated in accordance with IEC 61378-1:2011, 6.2. According to IEC 61378-1:2011, 6.1, "It is not guaranteed, but shall be provided by the transformer manufacturer for the purchaser".

4.4.8 Transformer guaranteed short-circuit impedance

The symbols e_{xA} and e_{xB} in column 17 show the transformer guaranteed short circuit impedance. e_{xA} is the inductive short-circuit impedance obtained by the short-circuit measurement A in column 13. e_{xB} is that obtained by the short-circuit measurement B in column 14. From these values, the commutating reactance X_t can be obtained used in the calculation for inductive voltage regulation of the transformer by the formula shown in 4.7.2.4 (see IEC 61378-1:2011, 7.2.1).

The contents of columns 13 to 15 and 17 of Table 1 are provided for information purpose. For the short-circuit impedance of the converter transformer, IEC 61378 (all parts) should be referred to.

4.4.9 Line side fundamental current factor

The contents of column 7 of Table 1 are provided for information purpose. For the line side fundamental current factor of the converter transformer, IEC 61378 (all parts) should be referred to.

NOTE By comparing this factor and "line side current factor" in column 8, it is noted that the definitions of rated current are found to be different between IEC 60146 (all parts) and IEC 61378 (all parts). For more detailed explanation, refer to Annex A.

4.5 Parallel and series connections

4.5.1 Parallel or series connection of valve devices

4.5.1.1 General

When diodes or thyristors are connected in series or parallel, precautions should be taken to ensure that all devices operate within rated values for voltage and current.

4.5.1.2 Current balancing of parallel connected valve devices

Unequal current distribution may be caused by differences in forward voltage or on-state voltage drop and by differences in thyristor turn-on time and trigger delay angles. Differences in the impedances of the parallel arms are also of considerable influence.

If factory matching of forward or on-state characteristics and turn-on time properties of the valve devices is used for current balancing, this should be stated by the equipment supplier.

4.5.1.3 Voltage division for series connected valve devices

Unequal voltage distribution may be caused by differences in reverse and off-state characteristics, differences in the turn-on instant for thyristors and differences in recovery charge.

4.5.2 Parallel or series connection of assemblies and equipment units

4.5.2.1 General

Precautions also should be taken when assemblies and equipment units are connected in series or parallel.

4.5.2.2 Parallel connection

When units are connected in parallel, it shall be considered if they are provided with means for voltage adjustment or not.

a) Units not provided with means for voltage adjustment

   In the case of equipment units designed for parallel connection, none of the parallel connected units shall exceed its rating when operating at total rated output.

   If the equipment is required to operate in parallel with other sources having dissimilar characteristics, the requirements for load-sharing should be specified separately.

b) Units provided with means for output voltage adjustment

   For such equipment, when required to operate in parallel the requirements for load sharing should be specified separately.

4.5.2.3 Series connection

When assemblies or equipment units are designed for series connection, precaution should be taken to ensure that each unit operates within its limits of rated voltages, even if the AC side is disconnected and the DC side is still connected to an active load.

In the case of series connection, the voltage to ground may be considerably higher than the voltage between the terminals. In this case, the insulation should be designed and tested accordingly.

4.6 Power factor

4.6.1 General

For converters with a pulse number of 6 or more, the total power factor is of limited interest. The value which is useful for normal purposes is the displacement factor $\cos\varphi_1$ of the fundamental wave.

The displacement factor $\cos\varphi_1$ is referred to the line side of the converter transformer.

For this reason, if a guarantee is required, it should, unless otherwise specified, refer to the displacement factor calculated under the assumption of both symmetrical and sinusoidal voltage.

The displacement factor for three-phase uniform thyristor connections should be determined by calculation from the measured reactances in accordance with 4.6.4.

For single-phase equipment exceeding 300 kW rated output, for equipment with non-uniform three-phase connections and for converters with sequential phase control, the method of determining the displacement factor is to be specified separately.

When a converter is operating in the rectifier mode, it is consuming active and reactive power from the AC system.

When a converter is operating in the inverter mode, it is delivering active power into the AC system but still consuming reactive power from it.

NOTE For many applications, i.e. rectifiers for small PWM (pulse width modulated) drives with small or no DC reactor, the ripple influences the total power factor very much.

4.6.2 Symbols used in the determination of displacement factor

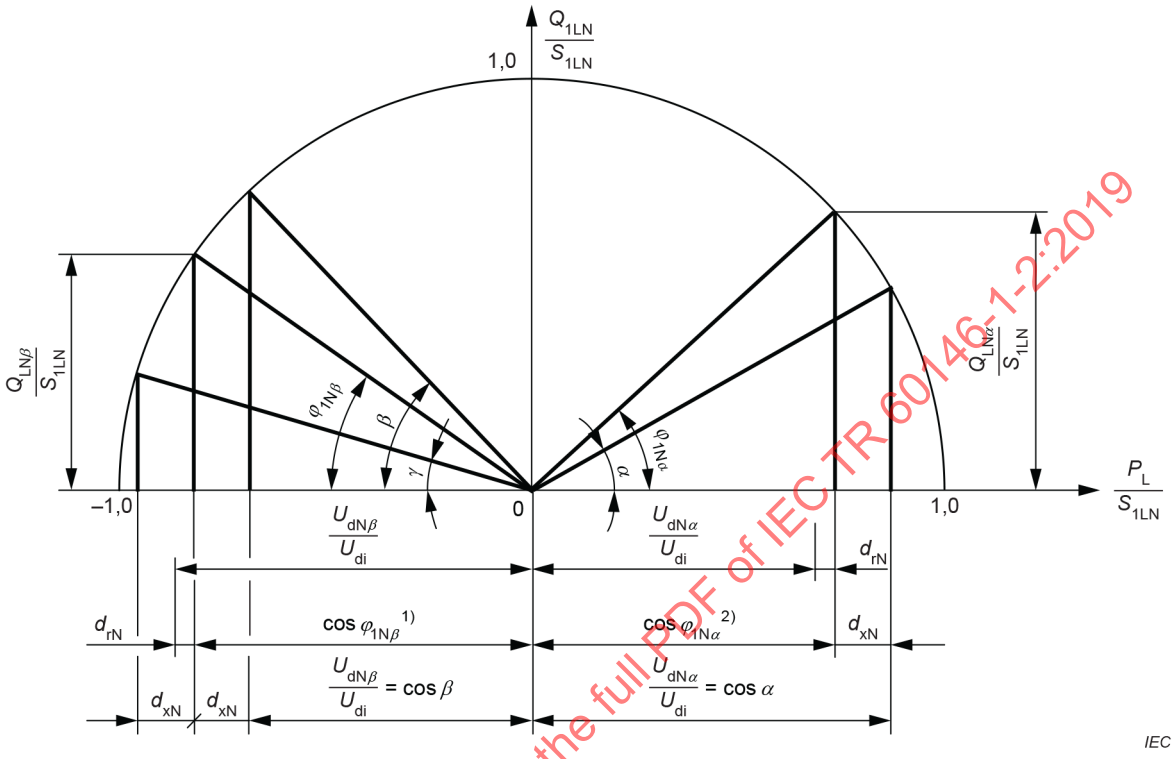
The letter symbols used in the determination of displacement factor are given in Table 2.

Table 2 – List of symbols used in the determination of displacement factor

Symbol	Quantity
$\cos\varphi_{1N}$	displacement factor at rated direct current for zero trigger delay angle
$\cos\varphi_{1N\alpha}$	displacement factor at rated direct current, for trigger delay angle α
d_{rN}	= d_{rtN} + d_{rbN}, total resistive direct voltage regulation at rated current in per unit of U_{di}
d_{xN}	= d_{xtN} + d_{xbN}, total inductive direct voltage regulation at rated current in per unit of U_{di}
d_{rbN}, d_{xbN}	resistive (resp. inductive), direct voltage regulation due to other components of the converter, for example valve reactors, line side reactors and transformers etc., if any, at rated direct current, in per unit of U_{di}
d_{rtN}, d_{xtN}	resistive (resp. inductive), direct voltage regulation due to the converter transformer at rated direct current, in per unit of U_{di}
d_{LN}	additional direct voltage regulation due to AC system impedance, expressed in per unit of U_{di}, at rated direct current I_{dN}, when the RMS voltage on line side terminals is kept constant
E_{dN}	DC motor counter e.m.f. at rated shaft speed and rated flux
f_{1N}	rated line frequency
I_{dN}	rated direct current
I_{LN}	Rated RMS current on line side (of converter or transformer if included)
I_{1LN}	RMS value of the fundamental component of I_{LN}
p	pulse number
P_{LN}	= $U_{dN} \times I_{dN} + P_{rN}$, active power on line side at rated direct current
P_{rN}	power losses in circuit resistance at rated direct current
Q_{1LN}	reactive power on line side at rated direct current, related to I_{1LN}
R_a	motor armature circuit resistance
R_C	system resistance of the supply source
R_{1SC}	short-circuit ratio reffered to the fundamental apparent power of the converter
S_{1LN}	= $U_{di} \times I_{dN} = U_{LN} \times I_{1LN} \times \sqrt{3}$, apparent power on line side at rated load, based on the fundamental component I_{1LN} of the line current
S_C	short-circuit power of the supply source
S_{tN}	transformer rated apparent power
μ	angle of overlap
U_{di}	ideal no-load direct voltage
U_{dN}	rated direct voltage
U_{drN}	total resistive direct voltage regulation at rated direct current
U_{dxN}	total inductive direct voltage regulation at rated direct current
U_{dpN}	ideal internal direct voltage at rated load excluding the total resistive direct voltage regulation
X_C	system reactance of the supply source
α	trigger delay angle of phase control in rectifier operation
β	trigger advance angle of phase control in inverter operation
γ	extinction angle of commutation for inverter operation
φ_{1N}	displacement angle (of fundamental component) of the line current at rated direct current (neglecting the transformer magnetizing current)
α	suffix for rectifier operation with the trigger delay angle α
β	suffix for inverter operation with the trigger advance angle β

4.6.3 Circle diagram for the approximation of the displacement factor $\cos\varphi_{1N}$ and of the reactive power Q_{1LN} for rectifier and inverter operation

The approximate displacement factor $\cos\varphi_{1N}$ and the approximate reactive power Q_{1LN} for a converter may be estimated by use of the circle diagram given in Figure 2.



1) $\cos\varphi_{1N\beta} = \frac{U_{dpN\beta}}{U_{di}} = \frac{P_{1N\beta}}{S_{1LN}}$

2) $\cos\varphi_{1N\alpha} = \frac{U_{dpN\alpha}}{U_{di}} = \frac{P_{1N\alpha}}{S_{1LN}}$

Figure 2 – Circle diagram for approximation of the displacement factor

4.6.4 Calculation of the displacement factor $\cos\varphi_1$

4.6.4.1 Displacement factor, at rated direct current, for zero delay angle $\cos\varphi_{1N}$

This is obtained, for the appropriate value of AC system reactance, from Figure 3 and Figure 4, respectively. If not otherwise stated, it is assumed that the RMS value of the line side terminal voltage is kept constant.

Figure 3 is used for 6-pulse connections.

Figure 4 is used for 12-pulse connections.

The values of α_p indicated in Figure 4 are those of the inherent delay angle which occurs in a 12-pulse connection in certain operating regions, even where no phase control is applied. For phase controlled converters, they represent the minimum delay angles that can exist under the indicated conditions.

4.6.4.2 Displacement factor $\cos\varphi_{1\alpha N}$, at rated direct current, for delay angle α

If there is phase control with trigger delay angle α, the corresponding value $\cos\varphi_{1N\alpha}$ may be calculated from the following formula, which is sufficiently accurate for practical purposes:

$$\cos\varphi_{1N\alpha} = \cos\alpha - (1 - \cos\varphi_{1N})$$

For the inverter range, the displacement factor may be obtained from the following formula:

$$\cos\varphi_{1N\beta} = \cos\beta + (1 - \cos\varphi_{1N})$$

For an inverter, the abscissa in Figure 3 and Figure 4 represents the inductive direct voltage increase at rated load in per unit of U_{di}.

4.6.4.3 Displacement factor at loads other than rated load, $\cos\varphi_{1\alpha}$

When using the curves of Figure 3 and Figure 4 for other loads than the rated load, the actual values of I_d, d_{xt} and d_{xb} are used to obtain the $\cos\varphi_1$ for the actual direct current I_d.

That is, the value:

$$d_{xt} + d_{xb} = (d_{xtN} + d_{xbN}) \times \frac{I_d}{I_{dN}}$$

is used to obtain $\cos\varphi_1$ from Figure 3 and Figure 4 respectively. Then:

$$\cos\varphi_{1\alpha} = \cos\alpha - (1 - \cos\varphi_1)$$

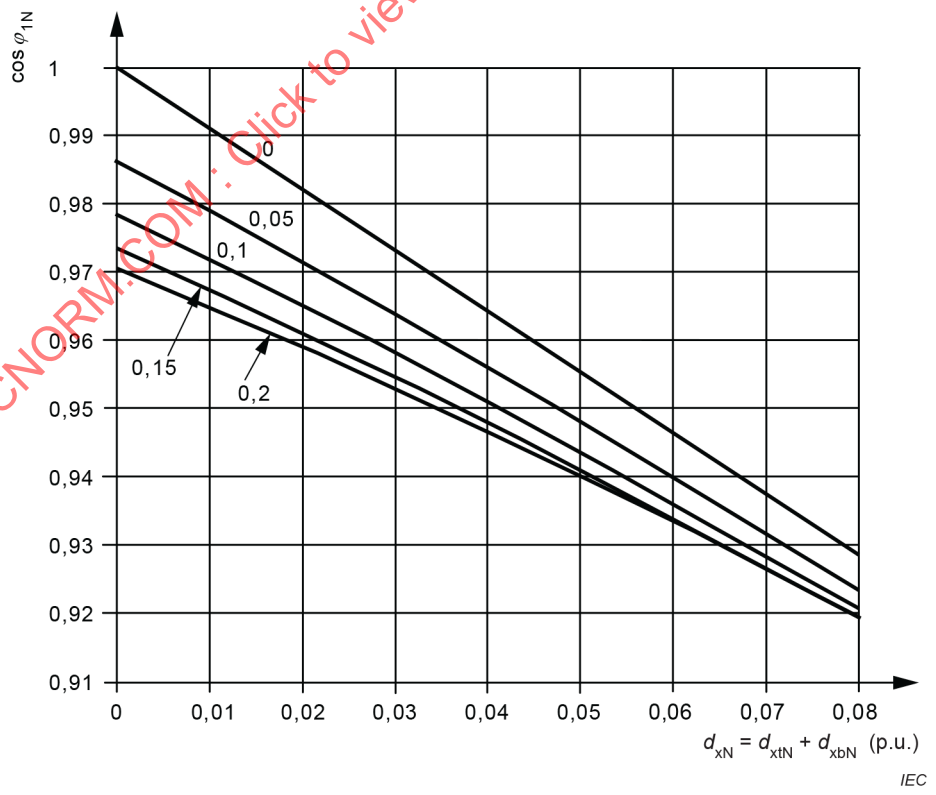


Figure 3 – Displacement factor as a function of d_{xN} for $p = 6$

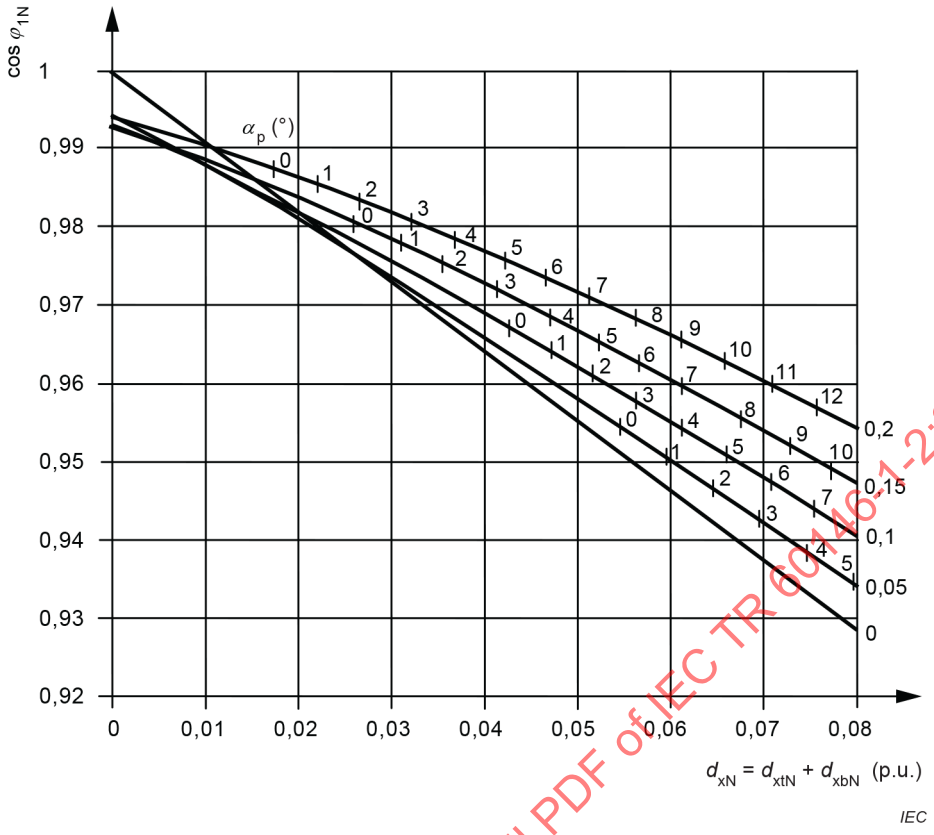


Figure 4 – Displacement factor as a function of d_{xN} for p = 12

NOTE The parameter for Figure 3 and Figure 4 is:

$$\frac{1}{R_{1SC}} = \frac{S_{1LN}}{S_C} = \frac{U_{di} \times I_{dN}}{S_C}$$

4.6.5 Conversion factor

For converters with a pulse number of 6 or more, the conversion factor and the power efficiency are almost equal (see IEC 60146-1-1:2009, 3.7.11 and 3.7.12).

The conversion factor should be given in addition to the power efficiency, especially for low power converters, for converters with pulse number of 6 or less if specified by the purchaser and in cases of applications where the power of the AC components of currents and voltages in the DC circuit is considered not to contribute to the useful power.

The conversion factor should always be determined by the input/output method for specified load conditions.

4.7 Direct voltage regulation

4.7.1 General

The voltage regulation of a single converter connected to a system that does not include power factor correction capacitors is mainly due to:

– resistive voltage regulation, i.e. the voltage regulation consequential of power loss within the converter;

– inductive voltage regulation due to commutation. Commutation distorts the voltage waveform at the terminals of semiconductor assemblies and change DC voltage that is basically made up of samples of the AC voltages;

– voltage regulation due to the impedance of the line and non-sinusoidal input currents of the converter that also distort the voltage waveform at converter terminals.

The ideal no-load direct voltage U_{di} could then be referred to the voltage of the infinite bus, i.e. voltage regulation shall include the effect of all impedances existing between such infinite power source and the AC terminals of the converter.

However, this document assumes the RMS line voltage to be constant at the AC terminals of the converter, not at infinite power source.

Thus the ideal no-load direct voltage U_{di} is referred to converter terminal voltage and the voltage regulation results from two contributions:

- the inherent direct voltage regulation, i.e. the voltage regulation of the converter itself (see 4.7.2 and IEC 60146-1-1:2009, 3.7.7);
- the additional direct voltage regulation due to the influence of AC system impedance on the waveform of converter terminal voltage (see 4.7.3).

When power factor correction capacitors are included in the system, the frequency behaviour influences the voltage waveform and the voltage regulation.

4.7.2 Inherent direct voltage regulation

4.7.2.1 General

The inherent voltage regulation is given by the sum of the direct voltage regulation produced by the transformer and other parts of the converter equipment, such as reactors, etc., plus the change with current of on-state voltage for thyristors and forward voltage for diodes.

It is assumed that the alternating voltage at the line side terminals of the converter is constant.

The voltage regulation should refer to the principal tap of the transformer. When a thyristor converter operates in the inverter range, the voltage regulation is adding to and gives an increase of the direct voltage.

The inherent voltage regulation should be calculated from the reactances and power losses of the components of the equipment. The voltage regulation may be determined by direct measurement in an input/output load test on the equipment if so preferred by the supplier.

For single-phase equipment, for equipment with non-uniform thyristor connections and for converters with sequential phase control, the method of determining the inherent voltage regulation will be specified.

4.7.2.2 Resistive direct voltage regulation due to converter transformer and interphase transformer

This regulation is given by the formula:

$$U_{drtN} = \frac{P_{rtN}}{I_{dN}}$$

where

P_{rtN} is losses in the transformer windings at rated direct current.

4.7.2.3 Resistive direct voltage regulation due to other components

Examples of such components are series-smoothing reactors, line side reactors, transductors, current balancing means, diodes, thyristors etc. Voltage drop by threshold voltage of valve devices is excluded.

This regulation is calculated from the formula:

$$U_{drbN} = \frac{P_{rbN}}{I_{dN}}$$

where

P_{rbN} is the losses in the components at rated direct current.

4.7.2.4 Inductive direct voltage regulation due to the converter transformer

The inductive voltage regulation can be calculated from the value of X_t by means of the following formula:

$$d_{xtN} = \frac{\delta \times q \times s}{2 \times \pi \times g} \times X_t \times \frac{I_{dN}}{U_{di}}$$

where

g is the number of sets of commutating groups between which I_{dN} is dvided;

I_{dN} is the rated direct current;

q is the commutation number;

s is the number of commutating groups in series;

U_{di} is the ideal no-load direct voltage;

δ is the number of commutating groups commutating simultaneously per primary.

The parameter below used in the formula is listed in Table 1, column 12.

$$\frac{\delta \times q \times s}{g}$$

X_t is the transformer commutating reactance measured according to IEC 61378-1:2011, 7.2. If the measured value of X_t is indicated in per unit (pu), it requires great attention to clarify the base of the per unit when converting the value from pu to ohm (or mili-Henry). It is noted that IEC 61378-1 defines the transformer capacity based on the fundamental component of the current. Refer to Annex A.

An alternative method to obtain the transformer inductive voltage regulation is indicated in IEC 61378-1:2011, 7.2.2.

The formula above for d_{xtN} indicates that the voltage regulation has linear characteristics to the DC load current. However, the formula can be applied when the assumptions listed below are fulfilled. For details, it is recommended to consult with textbooks of the line commutated converter theory. Refer to Bibliography.

a) Single commutation

The formula is derived based on the assumption that a single commutation takes place at an instant. In the case where multiple commutations take place, the characteristics of the voltage regulation changes from the line indicated by the formula. Such phenomena will

take place when the DC load current is sufficiently large and the commutation duration extends and overwraps to the next commutation.

b) No voltage induction from DC load current

In some kinds of converter circuit with 6-pulse operation, the voltage induction in valve side windings from the DC current may take place. However, it is noted that the converter circuits listed in Table 1 are free from such phenomena.

The voltage induction from the DC load current is explained taking the converter connection No.3 as an example.

In the converter circuit, the 6 arms conduct DC current in turn for 60° each. Namely, when one of arms conducts the load current, only one valve side winding in the transformer conducts the DC load current. The magnetic field induced in the core of this winding spread to the cores of the other phases when the cores are magnetically coupled among phases.

In the case where the line side windings are connected in delta as shown in Table 1, the current is also induced in the line side winding by the magnetic field and circulates within the delta-connected windings. The circulation current cancels the magnetic field induced by the DC current flowing in the valve side winding. Then, the valve side voltage is not affected by the magnetic field made by the DC current.

However, if the line-side windings are connected in star, it results in problem. Namely, the circulation current cannot flow in the line-side windings. Then, the magnetic field induced by the DC current cannot be cancelled out and induces the voltage in the windings of the other phases. The induced voltage superimposes to the AC voltage transferred from the line side winding. The induced voltage increases as the DC current increases. Then, the voltages across the arms are distorted and the conduction periods extend longer than 60°. Namely, the operation status is different from that of 6-pulse operation. It means that the phenomena affect the inductive voltage regulation and that the previous formula for d_{xtN} cannot be applied any more.

In summary, it should be noted that the winding connection or the magnetic design of the transformer affects the inductive voltage regulation and it is recommended to pay great attention to the transformer connection when calculating the inductive voltage regulation.

c) Constant DC current

The formula is derived based on the assumption that the DC current is kept ideally constant.

When the DC load is very light, in practice, the DC current is not constant and intermittent. Especially, when a DC capacitor or some parasitic capacitance is connected to the DC circuit with a light load, the DC current is likely intermittent. When the DC load has characteristics keeping DC voltage by itself, like batteries, DC motors or electrolysis, the intermittent current also likely appears. In such case, the DC voltage will be higher than the voltage estimated by the formula above.

Refer to IEC 60146-1-1:2009, 4.3.2.2.

4.7.2.5 Inductive direct voltage regulation due to other components

For example valve reactors, line side reactors, current balancing reactors, etc.

The symbols given in Table 3 are used in the calculation formulae.

Table 3 – List of symbols used in the calculation formulae

Symbol	Quantity
d_{xbLN}	inductive direct voltage regulation at I_{dN} due to line side reactors in per unit of U_{di}
d_{xbvN}	inductive direct voltage regulation at I_{dN} due to valve side reactors in per unit of U_{di}
U_{dxbLN}	inductive direct voltage regulation, corresponding to d_{xbLN}
U_{dxbvN}	inductive direct voltage regulation, corresponding to d_{xbvN}
X_{bL}	reactance per phase on line side of reactor, transformer etc.
X_x	reactance per phase on valve side of reactor, valve reactors etc.
I_{1L}	RMS value of the transformer fundamental primary phase current
I_{bN}	RMS current in reactor, corresponding to I_{dN}, calculated on the basis of rectangular current waveform
I_{dN}	rated direct current
U_{bN}	rated phase-to-phase voltage at the line side terminals of the reactor etc.
g	number of commutating groups between which I_{dN} is divided
p	pulse number
q	commutation number
s	number of commutating groups in series
δ	number of commutating groups commutating simultaneously per primary

a) For reactors, transformers etc., on the line side:

– For three-phase systems:

$$d_{xbLN} = \frac{\sqrt{3} \times I_{bN} \times X_{bL}}{U_{bN}} \sin\left(\frac{\pi}{p}\right) \text{ and } U_{dxbLN} = \frac{\sqrt{3} \times I_{bN} \times U_{di} \times X_{bL}}{U_{bN}} \sin\left(\frac{\pi}{p}\right)$$

– For single-phase systems:

$$d_{xbLN} = \frac{1}{\sqrt{2}} \times \frac{I_{bN} \times X_{bL}}{U_{bN}} \text{ and } U_{dxbLN} = \frac{1}{\sqrt{2}} \times \frac{I_{bN} \times X_{bL} \times U_{di}}{U_{bN}}$$

b) For valve side reactors:

$$d_{xbvN} = \frac{\delta \times q \times s}{2 \times \pi \times g} \times \frac{I_{dN} \times X_{bv}}{U_{di}} \text{ and } U_{dxbvN} = \frac{\delta \times q \times s}{2 \times \pi \times g} \times I_{dN} \times X_{bv}$$

The inductive direct voltage regulation due to other components is:

$$U_{dxbN} = U_{dxbLN} + U_{dxbvN}$$

4.7.2.6 Inherent direct voltage regulation of the converter

The direct voltage regulation at rated direct current due to converter transformer and interphase transformer (if any), is given by:

$$U_{dtN} = U_{drtN} + U_{dxtN}$$

The direct voltage regulation at rated direct current due to other components of the converter, is given by:

$$U_{dbN} = U_{drbN} + U_{dxbN}$$

The inherent direct voltage regulation at rated direct current, is given by:

$$U_{dtN} + U_{dbN} = U_{drtN} + U_{dxtN} + U_{drbN} + U_{dxbN}$$

4.7.3 Direct voltage regulation due to AC system impedance

4.7.3.1 Influence of AC system impedance on DC voltage regulation of the converter

Even if the converter terminal voltage RMS value is maintained constant, the AC system impedance causes an additional voltage regulation to appear on the DC terminals of the converter.

This is a consequence of changes in waveform of converter terminal voltages, due to non-sinusoidal currents drawn by the converter that influence the voltage regulation.

This influence depends on the pulse number and the ratio (R_{1SC}) of the short-circuit power of the source to the fundamental apparent power of the converter at rated direct current.

NOTE R_{SC} is referred to the rated apparent power in IEC 60146-1-1:2009. It is convenient to use R_{1SC} to calculate the influence of the AC system impedance.

4.7.3.2 Calculation of the additional direct voltage regulation U_{dLN} due to AC system impedance

Figure 5 gives the additional direct voltage regulation d_{LN} in per unit of U_{di} at rated direct current, due to AC system impedance. The corresponding voltage regulation U_{dLN} is:

$$U_{dLN} = d_{LN} \times U_{di}$$

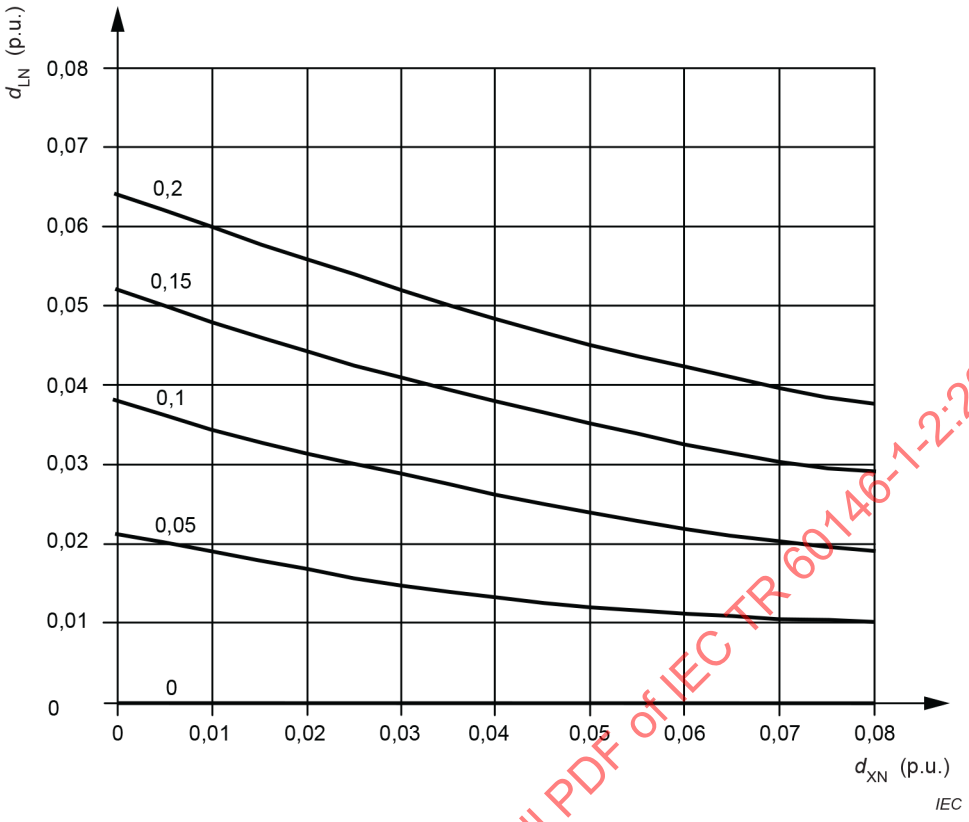
If not otherwise stated, it is assumed that the RMS value of the line side terminal voltage of the converter is kept constant.

When using the curves of Figure 5 for other loads than the rated load, the actual values of I_d, d_{xt} and d_{xb} shall be taken to obtain the actual regulation d_L and from this the actual additional regulation U_{dL}.

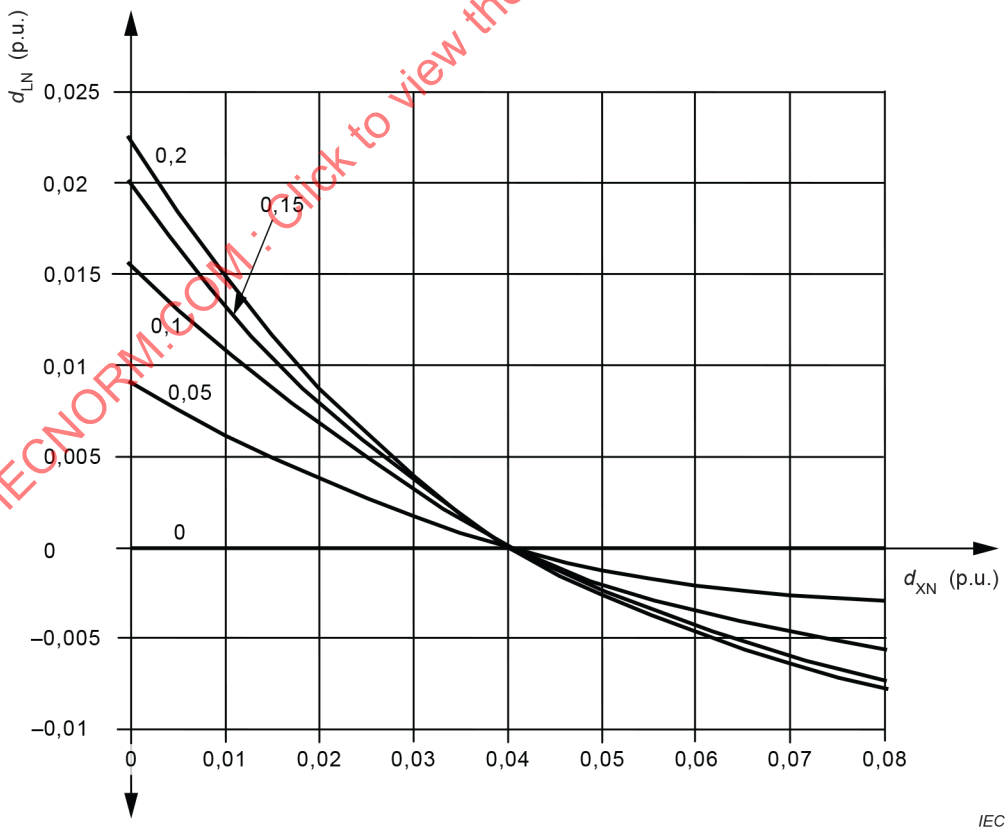
That is:

$$d_{xt} + d_{xb} = (d_{xtN} + d_{xbN}) \times \frac{I_d}{I_{dN}}$$

is used to enter the diagram of Figure 5.



a) d_{LN} for p = 6



b) d_{LN} for p = 12

Figure 5 – d_{LN} as a function of d_{xN} for p = 6 and p = 12

NOTE The parameter for Figure 5 is:

$$\frac{1}{R_{1SC}} = \frac{S_{1LN}}{S_C} = \frac{U_{di} \times I_{dN}}{S_C}$$

4.7.3.3 Measurement of the additional direct voltage regulation due to AC system impedance

A voltmeter on the DC side of the converter does not indicate the inherent voltage regulation (see 4.7.2) but a larger regulation.

The influence of the AC system impedance cannot be measured directly by a voltmeter indicating the RMS value on the AC voltage taken when the converter is on load.

The additional direct voltage regulation due to the AC system impedance can be measured with sufficient approximation by an appropriate measuring circuit using an auxiliary rectifier connected to the line side terminals of the converter, through a transformer if necessary.

This auxiliary rectifier have the same commutation number and pulse number as the converter and the ripple of its direct voltage have the same relative phase position to the AC network voltage as the ripple of the converter direct voltage.

The per unit change of the output voltage of the auxiliary rectifier during a change of the converter load represents the per unit change in the converter direct voltage due to the system impedance.

4.7.3.4 Influence on direct voltage regulation of other converters connected to the same system

If other converters are fed from the same AC system, these may cause an additional voltage regulation of the converter under consideration even in the case of constant RMS value of AC voltage at converter terminals.

To enable the supplier to take such conditions into consideration, the purchaser should indicate prior to order the power, connection, location and other main particulars of the other converters.

4.7.4 Information to be exchanged between supplier and purchaser about direct voltage regulation of the converter

To enable the supplier to calculate the effect of AC system impedance, the purchaser should give the AC system data before the order. When the system short-circuit power is given for this purpose, the value given should correspond to that configuration of the AC system for which the total voltage regulation is to be calculated.

The supplier should then indicate the following values:

– the inherent direct voltage regulation (see 4.7.2.6) of the converter

$$U_{dtN} + U_{dbN}$$

– the total voltage regulation of the converter, when the RMS value of the line side terminal voltage is kept constant

$$U_{dtN} + U_{dbN} + U_{dLN}$$

When values of system impedance are not given by the purchaser, the supplier should assume some specified finite value of the short-circuit power of the AC system or,

alternatively, should draw the purchaser's attention to Figure 5 by which the total voltage regulation can be calculated for any value of the AC system short-circuit power.

Sample calculations of voltage regulation are given in Clause 5.

4.8 Voltage limits for reliable commutation in inverter mode

To prevent commutation failure or conduction-through, the design shall take into consideration the required maximum current, the highest direct voltage and the lowest AC system voltage which may occur simultaneously. Both steady-state and transient conditions have to be taken into consideration.

If not otherwise specified, the converter, when operating as an inverter, shall be able to carry all rated current values according to the duty class, without conduction-through at the rated minimum AC system voltage.

Under transient conditions such as in the case of voltage dips due to distant faults in the AC system, a commutation failure may occur particularly at maximum DC voltage in the inverter mode.

The following means may be used together or separately to reduce commutation failures or their consequences:

– lowering current limit setting;
– higher secondary voltage;
– lowering limit setting for rate of change of current;
– fast DC circuit-breaker or magnetic contactor, to operate particularly in the inverter mode;
– higher setting of the under-voltage relay (within rated limits);
– gate pulse train (instead of short gating signals);
– AC filter on the synchronizing input to the trigger equipment to prevent disturbances on the gating angle.

These means may not prevent all of the commutation failures but they would greatly reduce their number in most applications.

Automatic restarting after a tripping may be specified separately, but strict precautions shall be taken for the safety of the operators.

4.9 AC voltage waveform

The deviation of line-to-neutral or line-to-line AC supply voltage from the instantaneous value of the fundamental wave (for example during commutation of power converters) may reach 0,2 p.u. or more of the existing crest value of the line voltage (Figure 6). Additional oscillations may appear at the beginning and at the end of each commutation.

Non-repetitive transients are mainly due to fault clearing and switching, as well as possible lightning strokes on overhead lines, which may have some effect on MV and LV systems.

The following values are given as examples only on the basis of the individual converter transformer characteristics and rating (S_{tN}).

a) Transient energy 400 S_{tN} J

NOTE 1 S_{tN} is expressed in MVA. The transient energy comes from the interruption of the transformer magnetizing current. The magnetizing current of the transformer is assumed to be 0,05 p.u. of its rated current.

b) Rise time (0,1 to 0,9 peak value) 1 µs

c) Repetitive peak value (U_{LRM} / U_{LWM}) 1,25 p.u.

d) Non-repetitive peak value (U_{LSM} / U_{LWM}) 2,0 .. 2,5 p.u.

NOTE 2 The peak value is given assuming a typical suppressor is used. Without suppressor, this value could be 10 p.u. or more.

e) Duration above 0,5 p.u. 3 .. 300 µs

If several converters without individual transformers are connected to the same bus, the suppressor circuits shall be coordinated with the common transformer.

U_{LRM} maximum instantaneous value of U_L, including repetitive over-voltages but excluding non-repetitive over-voltages

U_{LSM} maximum instantaneous value of U_L, including non-repetitive over-voltages

U_{LWM} maximum instantaneous value of U_L, excluding transient over-voltages

Figure 6 shows one non-repetitive transient with the amplitude U_{LSM} and the typical commutation notches of a 6-pulse power converter (connection No. 8, Table 1).

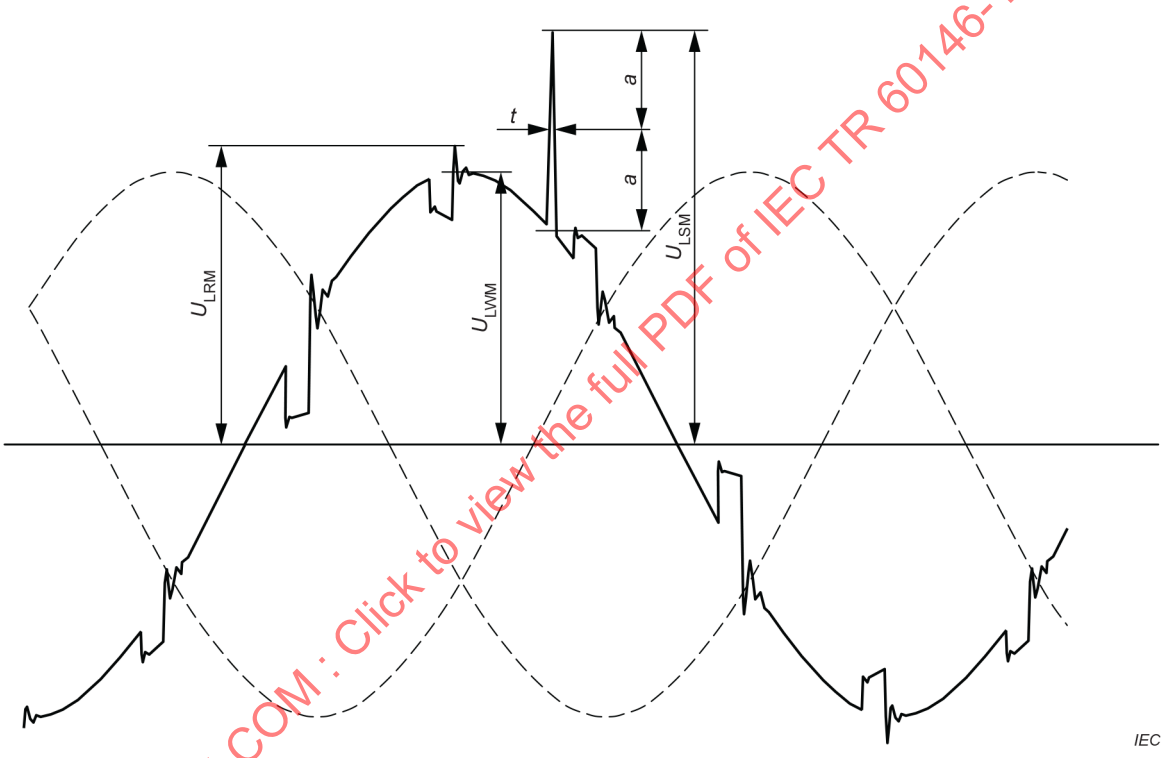


Figure 6 – AC voltage waveform

5 Application information

5.1 Practical calculation of the operating parameters

5.1.1 General

If a project requires the calculations to be performed a number of times, as an alternative to using the figures and formulae in 4.6 and 4.7, it is expedient to use a computer or at least a programmable calculator.

The formulae in 5.1.2 to 5.1.4 are sufficiently accurate for most cases, particularly for standard design converters.

For letter symbols, see 4.6.2 and IEC 60146-1-1:2009, 4.2.

5.1.2 Assumptions

The calculation implies that the following assumptions are valid:

– uniform connection;
– infinite smoothing inductance, i.e. negligible direct current ripple;
– pulse number $p = 6$; commutation number $q = 3$;
– negligible AC voltage unbalance;
– steady-state, i.e. constant direct voltage and current;
– angle of overlap μ less than $2\pi/p$.

5.1.3 Preliminary calculations

The fundamental apparent power is calculated as follows:

$$S_{1LN} = U_{di} \times I_{dN}$$

The inductive voltage regulation including the effects from the reactances of the supply source and the feeder cable or line is calculated as below based on the first formula shown in 4.7.2.4.

$$d_{xtN} = \frac{\delta \times q \times s}{2 \times \pi \times g} \times X_{sum} \times \frac{I_{dN}}{U_{di}}$$

where

X_{sum} = $X_t + X'_L + X'_C$, the sum of the reactances below:

X_t is the commutation reactance of the converter transformer seen from the valve side;

$X'_L = \left(\frac{U_{V0}}{U_L}\right)^2 X_L$ is the reactance of the cable or the line seen from the valve side through the converter transformer;

$X'_C = \left(\frac{U_{V0}}{U_L}\right)^2 X_C$ is the reactance of the supply source seen from the valve side through the converter transformer.

The formula above for d_{xtN} can be derived considering that the commutation current flows from the supply source to the converter through the reactances between them. In other words, the commutation reactance is calculated from the sum of the reactances. In the calculation, the values of reactances at the line side should be converted to those seen from the valve side of the converter transformer since the voltage regulation is calculated based on the values of the valve side.

NOTE The calculations using the ratio (d_{xtN} / e_{xN}) in IEC 60146-1-2:2011 was removed and replaced with the equivalent and simple calculations. The equivalency is shown in Clause C.7.

Resistive direct voltage regulation at rated current:

$$U_{drN} = \frac{P_{rN}}{I_{dN}}$$

where

P_{rN} is the power losses in circuit resistance at rated load. The loss caused by threshold voltages of valve devices is excluded.

$$d_{rN} = P_{rN}/(U_{di} \times I_{dN}) = P_{rN}/S_{1LN}$$

5.1.4 Calculation of the operating conditions

5.1.4.1 Direct voltage

With the assumptions of six-pulse uniform connection, the following formulae apply:

a) for rectifier:

$$U_{di} \times \cos\alpha = U_d + U_{TO} + (U_{drN} + U_{dxN}) \times \frac{I_d}{I_{dN}}$$

b) for inverter:

$$U_{di} \times \cos(\alpha + \mu) = U_d + U_{TO} + (U_{drN} - U_{dxN}) \times \frac{I_d}{I_{dN}}$$

where

U_{di} $= U_{v0} \times 3\sqrt{2}/\pi$;

U_{TO} is the sum of threshold voltages of all valve devices connected in series in any current path;

$\frac{I_d}{I_{dN}}$ is the per unit direct current.

In the common case of a converter for a DC motor drive, the value of U_d is the DC motor counter e.m.f. E_d (proportional to shaft speed and motor flux) plus the armature voltage drop at rated current.

$$U_d = E_{dN} \times \frac{E_d}{E_{dN}} + R_a \times I_{dN} \times \frac{I_d}{I_{dN}}$$

In this case, the resistive voltage regulation U_{drN} includes all the voltage regulation caused by the losses except the loss caused by threshold voltage of the valve devices: resistance of the valve devices, armature, DC and AC cables, smoothing inductor, transformer windings.

In other cases, U_d is the converter voltage at its DC terminals and then U_{drN} does not include the losses in the DC circuits outside of the converter (cables and load or source).

U_{dxN} includes all the voltage regulation caused by inductances in the AC circuit: transformer leakage reactance, line or anode reactance, cable reactance, supply system reactance, etc. (see 5.1.3).

In certain cases, not steady-state, the rate of current rise di/dt shall be provided for, by adding the term Ldi/dt to the converter DC voltage (L is the total inductance of the DC circuit).

NOTE In the case of a diode rectifier, $\alpha = 0$, $\cos\alpha = 1$, the angle of overlap μ is given by:

$$\cos\mu = 1 - 2 \times \frac{U_{dX}}{U_{di}}$$

The output voltage is given by:

$$U_d = U_{di} - (U_{dr} + U_{TO} + U_{dx})$$

5.1.4.2 Displacement angle

The following approximation gives a satisfactory result in most cases:

$$\cos\varphi_1 = \frac{U_d + U_{TO} + U_{drN} \times I_d / I_{dN}}{U_{di}}$$

A more accurate formula is:

$$\tan\varphi_1 = \frac{2\mu + \sin 2\alpha - \sin[2(\alpha + \mu)]}{\cos 2\alpha - \cos[2(\alpha + \mu)]}$$

NOTE Radians are used in the latter formula.

5.1.4.3 Rectifier and inverter operation

In rectifier operation, both current and voltage are considered as positive and also the active and reactive power.

In inverter operation, the current and reactive power are positive, the voltage and active power are negative.

As an example, Table 4 shows operating conditions and Table 5 shows operating points.

Table 4 – Example of operating conditions

	Value	Unit
E_{dN}	450	V
I_{dN}	1812	A
S_C	115	MVA
X_C / R_C	8	p.u.
S_{tN}	1,25	MVA
e_{xN}	0,055	p.u.
e_{rN}	0,012	p.u.
U_{LN}	400	V
U_{TO}	2,1	V
R_a	9,93	mΩ

Table 5 – Example of operating points

	Rectifying steady-state	Starting	Inverting	Unit
I_d / I_{dN}	1,03	1,6	1,175	p.u.
E_d / E_{dN}	1,055	0,0	–0,288	p.u.
U_{di}	540	540	540	V
U_{dx}	15,0	23,3	17,1	V
U_{dr}	5,2	8,1	5,96	V
α	23,2	83,4	98,3	° (degree)
μ	5,2	4,97	3,7	° (degree)
$\cos\varphi_1$	0,892	0,072	–0,176	–
φ_1	26,9	85,9	93,3	° (degree)
S_{1L}	1,01	1,57	1,15	MVA
P_L / P_{1L}	0,899	0,113	–0,213	MW
Q_{1L}	0,455	1,56	1,13	Mvar

5.2 Supply system voltage change due to converter loads

5.2.1 Fundamental voltage change

The voltage change may be estimated using the formula:

$$\frac{\Delta U}{U} \approx \frac{S_{1L}}{S_C} \times \cos\left[\tan^{-1}\left(\frac{X_C}{R_C}\right) - \varphi_1\right]$$

where

X_C is the reactance of the supply source;

R_C is the resistance of the supply source.

NOTE X_C / R_C can vary from 4 p.u. to 10 p.u.

5.2.2 Minimum R_{1SC} requirements for voltage change

The ratio of the short-circuit power of the supply source to the fundamental apparent power of the converter is:

$$R_{1SC} = \frac{S_C}{S_{1LN}}$$

The minimum R_{1SC} as regards the voltage regulation between no-load and peak load is:

$$R_{1SCmin} = \frac{S_{Cmin}}{S_{1Lm}} = \frac{\cos\left[\tan^{-1}\left(\frac{X_C}{R_C}\right) - \varphi_{1m}\right]}{\left(\frac{\Delta U_L}{U_L}\right)_m}$$

where

S_{1Lm} = $U_{di} \times I_{dMN}$;

I_{dMN} is the rated continuous direct current (maximum value).

EXAMPLE

Assume: X_C / R_C = 10; then $\tan^{-1}(X_C / R_C)$ = 84,29°

Assume: $\cos\varphi_{1m}$ = 0,1; then φ_{1m} = 84,26°

Hence: $\cos[\tan^{-1}(X_C / R_C) - \varphi_{1m}] \approx 1{,}0$

If: $(\Delta U_L / U_L)_m$ = 0,08

then: $R_{1SCmin} \approx 1{,}0 / 0{,}08 = 12{,}5$

5.2.3 Converter transformer ratio

The actual system voltage change may be approximated in two or more iteration steps.

In the first iteration, P_1, Q_1, φ_1 are calculated using the estimated secondary voltage corresponding to the on-load system voltage.

The voltage is then corrected to calculate the new values of P_1, Q_1, φ_1, $\Delta U_L/U_L$:

$$U_{L(n+1)} = U_{LN} \times \left[1 - \left(\frac{\Delta U_L}{U_L} \right)_n \right]$$

The new voltage change may be used for further iterations in order to optimize the transformer ratio and rating. However, other criteria may have to be considered such as the voltage changes due to other causes.

As an example of calculation, operating conditions shown in Table 6 is considered. The result of the iteration is shown in Table 7.

Table 6 – Example of operating conditions

Rated values		Value	Unit
DC voltage	U_{dN}	5 000	V
DC current	I_{dN}	2 200	A
DC circuit resistance	R_a	0,136	Ω
Transformer rating	S_{tN}	15	MVA
Short-circuit voltage			
Inductive component	e_x	0,085	p.u.
Resistive component	e_{rN}	0,008 7	p.u.
Secondary voltage	U_{LN}	5 080	V
Valve device threshold voltage drop	U_{TO}	38	V
Supply source short-circuit power (e_{xN} and e_{rN} include AC cables)	S_c	150	MVA

Table 7 – Result of the iteration

	Iteration		
	Initial	Final	Unit
U_L	5 080	4 745	V
U_{di}	6 860	6 408	V
I_d / I_{dN}	1,0	1,0	p.u.
E_d / E_{dN}	1,0	1,0	p.u.
U_{dx}	669	583	V
U_{dr}	66	57	V
α	32,7	27,6	° (degree)
μ	17,0	17,6	° (degree)
$\cos\varphi_1$	0,746	0,798	p.u.
φ_1	41,7	37,0	° (degree)
S_1	15,1	14,1	MVA
P_1	11,3	11,3	MW
Q_1	10,0	8,5	Mvar
$\Delta U / U$	0,076	0,066	p.u.

5.2.4 Transformer rating

The transformer current rating depends on the duty cycle.

The transformer rating increases with the system impedance.

At no-load, the supplied voltage defines the core size and number of turns and the wound conductor section is based on the current rating.

The transformer size also increases with $\tan\phi_1$.

Some increase of the transformer rating can be required to provide for large overloads with a high current rate of rise.

If the minimum control angle is high for reasons of response speed, the average displacement factor is lower and the transformer rating shall be increased.

For low to medium size converters, the DC side inductance may be small and the DC current ripple is high, requiring a higher current rating for the transformer.

The factor 0,816 ($\sqrt{2/3}$, Table 1, column 8) may become as high as 0,85.

5.3 Compensation of converter reactive power consumption

5.3.1 Average reactive power consumption

In most cases, the converter load duty cycle is variable with production requirements. It is, therefore, necessary to use a reference duty cycle selected as the most likely or most frequent.

The average active and reactive power consumption is calculated for each portion of the duty cycle. Table 8 shows an example.

Table 8 – Example of calculation results of active and reactive power consumption

	Constant acceleration	Steady-state	Constant deceleration	Unit
Duration	5	2	4,5	s
Q_{avg}	36	12,2	21,4	MVA
P_{avg}	18,5	13,9	–7,06	MW
S_{avg}	40,5	18,5	22,6	MVA
P_{avg} / S_{avg}	0,457	0,754	–0,313	p.u.
S_{rms}	41,6	18,5	23,1	MVA

Total cycle duration is 11,5 s ("forward" rolling speed).

$$Q_{avg} = (36 \times 5 + 12{,}2 \times 2 + 21{,}4 \times 4{,}5) / 11{,}5 = 26{,}15 \text{ Mvar}$$

$$P_{avg} = (18{,}5 \times 5 + 13{,}9 \times 2 - 7{,}06 \times 4{,}5) / 11{,}5 = 7{,}7 \text{ MW}$$

$$S_{RMS} = \sqrt{(41{,}6^2 \times 5 + 18{,}5^2 \times 2 + 23{,}1^2 \times 4{,}5)/11{,}5} = 32 \text{ MVA}$$

5.3.2 Required compensation of the average reactive power

The required compensation of the average reactive power is calculated using the required value and the formula:

$$Q_c = Q_{avg} - P_{avg} \times \tan\varphi_{req} = P_{avg} \times (\tan\varphi_{avg} - \tan\varphi_{req})$$

where

P_{avg}, Q_{avg} is the active and reactive power consumption;

$\tan\varphi_{avg}$ is the calculated $\tan\varphi_1$, without compensation;

$\tan\varphi_{req}$ is the required average $\tan\varphi_1$;

Q_c is the required reactive power compensation.

EXAMPLE

Using the data and results of the example in 5.2.2:

$\tan\varphi_{avg} = 26,15 / 7,7 = 3,4$

For: $\tan\varphi_{req} = 0,4$; $Q_c = 26,15 - 7,7 \times 0,4 = 23,1$ Mvar

It will be found that the reactive power compensation is too high during certain intervals of the duty cycle and too low in others. The succession of voltage changes may require some means of adjusting the compensation within closer limits of the required compensation.

NOTE The publications being prepared by TC 77 and its sub-committees are intended to give the acceptable limits of voltage changes as a decreasing function of their frequency of occurrence and also the acceptable limits as regards flicker.

5.3.3 Voltage fluctuations with fixed reactive power compensation

Capacitors used for power factor correction will supply more reactive power if the supply voltage increases and less if it decreases.

To account for this fact, an approximate method consists in deducting the capacitor bank rating from the system short-circuit power when calculating the voltage fluctuation.

EXAMPLE

Using the data of the previous example and S_C = 315 MVA

a) The no-load voltage change, with 23,1 Mvar power factor compensation, becomes:

$$\frac{\Delta U}{U} = \frac{23,1}{315\text{-}23,1} = 0,079\,1$$

b) Peak load corrected voltage: (acceleration at $2,3I_{dN}$ and $0,978U_{dN}$)

$$\frac{\Delta U}{U} = \frac{26,3 - 23,1 + 23,5/8}{315 - 23,1} = 0,021$$

The maximum voltage fluctuation is:

0,079 + 0,021 = 0,1 p.u.

NOTE The required $\tan\varphi_{req}$ can be non-optimal for minimizing the voltage changes due to the resistive voltage drop etc.

In the case of large fluctuating loads on relatively high impedance systems, the reactive power correction may have to be adjusted rapidly, although switched capacitor banks may be contemplated if the reactive power demand changes only two or three times per day.

Static switches or other means may be used for more frequent operations instead of conventional contactors or circuit-breakers, which may suffer mechanical wear, and the delay

time of the correction is such that the corrective action results in adding more voltage changes and making the flicker more objectionable.

5.4 Supply voltage distortion

5.4.1 Commutation notches

5.4.1.1 Notch area

The area of a commutation notch A_N, as observed between any two lines (principal notch of each half period), may be evaluated from:

$$A_N = \frac{U_{di}}{6 \times f_1 \times R_{1SC}}$$

EXAMPLE 1

f_1 = 60 Hz; U_{LN} = 460 V; R_{1SC} = 75; U_{di} = 621,2 V; A_N = 23 000 V·µs

If expressed in p.u. (line crest voltage × degrees):

$$A_E = \frac{180}{\pi \times R_{1SC}} \approx \frac{57{,}3}{R_{1SC}}$$

EXAMPLE 2

The same R_{1SC} gives A_E = 0,764 (p.u. × degrees).

5.4.1.2 Notch width

The notch width W_N may be calculated at the converter AC terminals neglecting the effect of stray capacitance and inductance. If all circuit capacitance is neglected, the notch width remains the same at other points of the supply circuit towards the infinite source, while the notch depth decreases.

The total width is expressed in angular measure and is equal to the angle of overlap μ.

Oscillations due to stray capacitance and inductance may appreciably change the shape of the commutation notches.

If identical converters are operated at approximately the same gating angle and supplied from the same source, they may be replaced by a single equivalent converter with a rating equal to the total rating and the same connection and pulse number. To get the equivalent commutation inductance, the individual inductances of the converters shall be connected in parallel and added to the common inductance.

5.4.1.3 Notch depth

The notch depth D_N at a given point is calculated by:

$$D_N = \frac{A_N}{W_N}$$

a) Converters with individual transformer

The amplitude of the commutation notches due to the converter under consideration at the points of connection of other converters depends on the impedance of the individual transformer which may be considered as an inductive element of the total commutation short-circuit power.

The notch depth decreases from 1,0 p.u. at the AC terminals of the converter assembly to zero at the level of the infinite source. The calculation is similar to that used for fault currents.

Table 9 shows an example of notch depth at the next conditions.

EXAMPLE

Supply source (50 Hz)	63 kV, 730 MVA
Main transformer	63/20 kV, 40 MVA, 0,125 p.u.
Feeder cable	20 kV, 0,32 mH/km, 130 m
Converter transformer	20/0,4 kV, 4,2 MVA, 0,07 p.u.

Table 9 – Example of notch depth

Voltage kV		**$1/S_c$** MVA^{-1}	**Short-circuit power** MVA	**Notch depth (α = 90°)** p.u.
63	Source	1/730	730	47,2/730 = 0,065
20	Transformer	0,125/40	222	47,2/222 = 0,213
20	Line	$2\pi \times 50 \times 0{,}32 \times 10^{-3} \times 0{,}13 / 20^2$	221	47,2/221 = 0,214
0,4	Conv. transformer	0,07 / 4,2	47,2	47,2/47,2 = 1,0

NOTE The notch depth in p.u. of crest voltage is independent of the converter load and is a maximum at α = 90° as assumed here; it varies as $\sin\alpha$.

b) Converters with a common transformer

In this case, the commutation inductance includes the inductance of the converter connecting cables which is the only individual inductance of each converter.

Consider at the next conditions.

Using the same supply source at the 20 kV level as in a) above, each converter is connected through a 150 m, 400 V cable to a 1,6 MVA, 20/0,4 kV transformer with 0,06 p.u. short-circuit voltage.

If the angle of overlap μ is small (2° to 5°) and the converters are used with non-correlated values of α, the commutation notch depth is calculated as before, only adding the 400 V cable impedance.

Table 10 shows the notch depth caused by one converter. The notch area also decreases from the converter to the infinite source but the width remains the same, if the effect of stray capacitance remains neglected.

If all the converters were operated at the same control angle and assuming equal impedance for all the converter lines, their impedances shall be paralleled for worst case conditions.

For example, if ten converters are connected to the same 400 V transformer and operate at the same time and the same control angle, the total short-circuit power would be increased to 19,4 MVA (instead of 7,34 MVA) resulting in greater notch depth as is shown in Table 11.

Table 10 – Example of notch depth by one converter with a common transformer

Voltage		$1/S_c$	Short-circuit power	Notch depth (α = 90°)
kV		MVA^{-1}	MVA	p.u.
63	Source	1/730	730	7,34/730 = 0,010 1
20	Transformer	0,125/40	222	7,34/222 = 0,033 1
20	Line	$2\pi \times 50 \times 0{,}32 \times 10^{-3} \times 0{,}13 / 20^2$	221	7,34/221 = 0,033 2
0,4	Conv. transformer	0,06 / 1,6	23,8	7,34/23,8 = 0,308
0,4	Cable	$2\pi \times 50 \times 0{,}32 \times 10^{-3} \times 0{,}15 / 0{,}4^2$	7,34	7,34/7,34 = 1,0

Table 11 – Example of notch depth by ten converters operating at the same time

Voltage		$1/S_c$	Short-circuité power	Notch depth (α = 90°)
kV		MVA^{-1}	MVA	p.u.
63	Source	1/730	730	19,4/730 = 0,027
20	Transformer	0,125/40	222	19,4/222 = 0,087
20	Line	$2\pi \times 50 \times 0{,}32 \times 10^{-3} \times 0{,}13 / 20^2$	221	19,4/221 = 0,088
0,4	Conv. transformer	0,06/1,6	23,8	19,4/23,8 = 0,815
0,4	Cable	$1/10 \times 2\pi \times 50 \times 0{,}32 \times 10^{-3} \times 0{,}15 / 0{,}4^2$	19,4	19,4/19,4 = 1,0

5.4.2 Operation of several converters on the same supply line

If several converters are connected to the same line, the interactions between the converters shall be considered, particularly in the design of the RC circuits connected in parallel to each valve device.

a) The losses in the damping RC circuits will increase with the number of converters. For a six-pulse bridge converter operating alone on the line, with RC circuits in the arms, the losses in the resistor due to commutation notches are in the worst case (that is with the trigger delay angle α = 90°):

$$P_{max} \approx 3{,}5 \times U_v^2 \times C \times f_1$$

where

C is the capacitance in one RC circuit;

U_v is the RMS voltage at the terminals of the converter assembly;

f_1 is the fundamental frequency;

P_{max} is the losses for one RC circuit.

In practice, the converters will operate with $\alpha \approx 90°$ only for short periods of time and the losses will then be much lower (exception: for example paper machines, when cooling of drying cylinders, may run for several hours at 0,02 p.u. to 0,05 p.u. speed). The following formula may be used:

$$P_{avg} \approx 3{,}5 \times U_v^2 \times C \times f_1 \times \sin^2\alpha$$

If several converters operate on the same line, the losses in the damping RC circuits of each converter will increase in proportion to the amplitudes and number of notches at its line terminals.

Therefore, the losses induced in a converter by notches originating from another converter are mainly dependent on the trigger delay angle of both converters, the possible overlap of commutations and the relative importance of individual impedances.

In most cases, it will cause no problem to connect up to 4 converters to the same line, if $\sin\alpha \leq 0{,}5$. If more converters shall be connected, the problem requires to be considered in detail.

b) The damping capacitor in the parallel connected converter will also increase the d*i*/d*t* stresses if the decoupling inductance between converters is low, which is the case if the connecting line is short and no line side reactor is included.

c) The converters will also cause a voltage drop in the line, which shall be considered in the converter specification. This is especially important if the converters shall be used in the inverter mode.

5.5 Quantities on the line side

5.5.1 RMS value of the line current

R.M.S value of the line current can be calculated as follows.

a) First approximation (neglecting overlap), see 4.4.3.

b) A more accurate formula may be used for a three-phase bridge connection when the trigger delay angle α and angle of overlap μ are known:

$$I_L^*(\alpha,\mu) = I_L \times \sqrt{1-3\psi(\alpha,\mu)}$$

where

I_L is the value by the first approximation;

$$\psi(\alpha,\mu) = \frac{\sin\mu \times [2+\cos(2\alpha+\mu)] - \mu \times [1+2\times\cos\alpha\times\cos(\alpha+\mu)]}{2\times\pi\times[\cos\alpha-\cos(\alpha+\mu)]^2}$$

using angles in radians.

The values of $I_L^*(\alpha,\mu)/I_L$ can be found in Table 12.

Table 12 – Values of $I_L^*(\alpha,\mu)/I_L$

	$I_L^*(\alpha,\mu)/I_L$				
μ degrees	α = 0°	α = 15°	α = 30°	α = 60°	α = 90°
5	0,994	0,993	0,993	0,993	0,993
15	0,983	0,979	0,979	0,979	0,979
25	0,972	0,966	0,965	0,965	0,965
35	0,960	0,953	0,951	0,950	0,950

c) When the relative DC side inductance is low, the real RMS value of the line current may become larger than what is calculated by the methods indicated in a) and b) due to the DC current ripple. See also 5.2.4, two last paragraphs.

5.5.2 Harmonics on the line side, approximate method for 6-pulse converters

5.5.2.1 General

At an early stage of the design, the formulae and Figure 7 of the following 5.5.2.2 and 5.5.2.3 may be used when the converter size is known by its transformer rating. Harmonics can be calculated easily by a computer simulation.

5.5.2.2 Current

The following formula can be used to calculate the harmonic current spectrum when the trigger delay angle α and the angle of overlap μ are known and direct current ripple can be neglected.

$$I_{h\alpha} = I_{1L} \times \frac{\sqrt{a^2 + b^2 - 2 \times a \times b \times \cos(2\alpha + \mu)}}{d}$$

where

$I_{h\alpha}$ is the harmonic current at the trigger delay angle α;

I_{1L} is the fundamental current;

h is the harmonic order;

$$a = \frac{1}{h-1} \times \sin\frac{(h-1) \times \mu}{2};$$

$$b = \frac{1}{h+1} \times \sin\frac{(h+1) \times \mu}{2};$$

$d = h \times \{\cos\alpha - \cos(\alpha + \mu)\}$ or

$d = 2 \times h \times d_x$.

Figure 7 shows results at some typical cases.

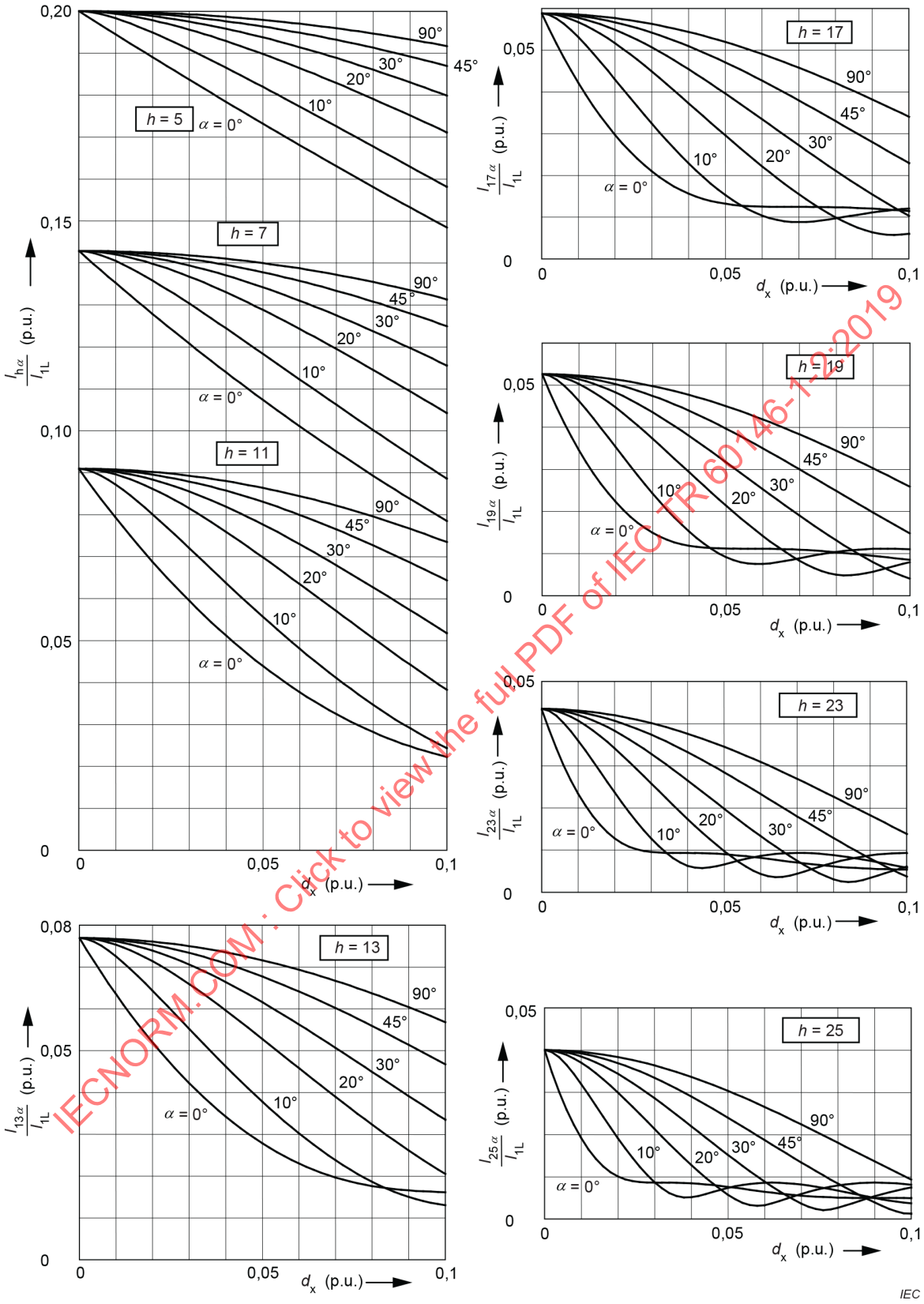
The fundamental current is given by:

$$I_{1L} = \frac{S_{1L}}{U_{LN} \times \sqrt{3}}$$

In the case of inverter operation, use extinction angle γ instead of trigger delay angle α. This chart assumes smooth direct current.

NOTE 1 Depending on the DC load circuit inductance, the direct current ripple can increase the 5^{th} harmonic current by 0,3 p.u. or more and the 11^{th} … $(6k - 1)$ to a lesser extent. The 7^{th} … $(6k + 1)$ is normally lowered.

NOTE 2 Other uncharacteristic harmonics can remain due to the supply voltage unbalance which prevents the expected cancellation.



Key

d_x inductive direct voltage regulation

α trigger delay angle (in the case of inverter operation, use extinction angle γ)

Figure 7 – Harmonic current spectrum on the AC side for p = 6

5.5.2.3 Voltage

The harmonic voltage $U_{h\alpha}$ is the product of the harmonic current $I_{h\alpha}$ and the harmonic impedance of the system Z_h:

$$U_{h\alpha} = Z_h \times I_{h\alpha}$$

The harmonic impedance of the system, in the absence of capacitor banks and long supply lines, may be approximated using the following formula applicable to transformers:

$$|Z_h| = \frac{U_{LN}^2}{S_C} \times \sqrt{\frac{1 + 1/(Q_s \times Q_p)^2 + 1/(h \times Q_s)^2}{1/Q_p^2 + 1/h^2}}$$

where

Q_s = X_s / R_s (about 8 p.u. to 12 p.u.);

Q_p = R_p / X_s (about 80 p.u. to 120 p.u,);

S_C = U_{LN}^2 / X_s;

R_s is the series resistance corresponding to the load losses;

R_p is the parallel resistance corresponding to the no-load losses;

X_s is the leakage reactance of the main transformers.

The following formula gives the relative harmonic voltage referred to the line-to-neutral voltage.

$$\frac{|U_{h\alpha}|}{U_{LN}/\sqrt{3}} = \frac{S_{1L}}{S_C} \times \frac{I_{h\alpha}}{I_{1L}} \times \sqrt{\frac{1 + 1/(Q_s \times Q_p)^2 + 1/(h \times Q_s)^2}{1/Q_p^2 + 1/h^2}}$$

5.5.3 Minimum R_{1SC} requirements for harmonic distortion

Harmonic distortion may be reduced by increasing the pulse number p of the converters. This is usually done by a combination of several basic 6-pulse converters.

The order of characteristic harmonics is given by:

$$h = k \times p \pm 1; \quad k = \text{positive integer}$$

Those harmonics that result to be characteristic for the basic 6-pulse converter units and non-characteristic for the complete converter usually are not completely cancelled and may reach 0,05 p.u. to 0,15 p.u. of the value for the basic 6-pulse converter.

Using the conservative value of 0,15 p.u. for non-characteristic harmonics, Q_s = 8 p.u., Q_p = 100 p.u., the following Table 13 has been calculated for different values of

$$\frac{S_{1L}}{S_C} = \frac{1}{R_{1SC}}$$

and p = 6 – 12 – 18 – 24.

It also gives the value of the lowest order characteristic harmonic and the notch area in p.u. × degrees (A_E at α = 90°).

Table 13 – Minimum R_{1SC} requirement for low voltage systems

THD [a]	*p* = 6			*p* = 12			p = 18			*p* = 24		
	R_{1SC}	A_E p.u. × deg.	U_5 p.u.	R_{1SC}	A_E p.u. × deg.	U_{11} p.u.	R_{1SC}	A_E p.u. × deg.	U_{17} p.u.	R_{1SC}	A_E p.u. × deg.	U_{23} p.u.
0,01	231	0,25	0,004 1	150	0,19	0,004 3	106	0,18	0,005 5	99	0,14	0,005 4
0,015	154	0,40	0,006 2	100	0,29	0,006 5	71	0,27	0,008 1	66	0,22	0,008 1
0,03	77	0,74	0,012 3	50	0,57	0,013 0	35	0,55	0,016 5	33	0,43	0,016 3
0,05	46	1,24	0,020 6	30	0,93	0,021 7	21	0,91	0,027 5	20	0,72	0,026 8
0,08	29	1,98	0,032 7	19	1,51	0,034 2	13	1,47	0,044 4	12	1,19	0,044 7
0,1	23	2,48	0,040 9	15	1,89	0,042 8	10	1,84	0,055 5	9	1,49	0,055 9

NOTE 1 For MV systems, use $R_{1SCmin} = 3 \times R_{1SC}$ as minimum requirement (resonance allowance).

NOTE 2 For HV systems, use $R_{1SCmin} = 2 \times R_{1SC}$ as minimum requirement (resonance allowance).

NOTE 3 Not to be used for systems with directly connected capacitor banks or filters.

NOTE 4 Use S_{1LN} for distortion corresponding to rated apparent power.

NOTE 5 Interpolation: $THD \times R_{1SC}$ = constant for a given *p*.

NOTE 6 The total harmonic distortion is given as the contribution of the converter to the existing distortion.

NOTE 7 The notch area is given for one single notch, without multiple commutation.

[a] *THD* = total harmonic ratio (total harmonic distortion)

5.5.4 Estimated phase shift of the harmonic currents

Using the simplifying assumption of a trapezoidal wave-shape, the phase shift is given by:

– for the fundamental current (see 5.1.4.2): φ_1

– for the harmonic current of order *h*:

$$\varphi_h = (1 \pm k \times p) \times \varphi_1 + k \times p \times \theta$$

where

k is a positive integer;

p is the pulse number;

θ is the transformer phase shift.

5.5.5 Addition of harmonic currents

If several converters are supplied from the same source, the harmonic components of like frequency may be added up vectorially if the phase relationship is known, including transformer phase shift, if any. However, minor fluctuation on design parameters, operating conditions, etc. may lead to a low accuracy in the calculated results, particularly for harmonic orders above 13^{th} or 17^{th} because the angle error is multiplied by k_p (for example 12 or 18). In the higher range of the harmonic spectrum, the uncharacteristic harmonics may well exceed the characteristic harmonics.

5.5.6 Peak and average harmonic spectrum

Harmonic currents are proportional to the fundamental current. Peak load harmonic currents and voltages and their effect, particularly on the crest voltage of capacitors, should be checked. But capacitors and other circuits elements are capable of short time overloads

particularly if their average overloading is moderate. Therefore, the RMS current in capacitors is allowed to exceed the capacitor rated current (for example 1,3 p.u. rated current, continuous duty).

5.5.7 Transformer phase shift

Using the appropriate transformer winding connections, the harmonic current phase shift may be used to virtually eliminate some of the harmonic currents. Table 14 shows examples.

Table 14 – Transformer phase shift and harmonic orders

Pulse number	Transformer phase shift degrees	Harmonic orders	
		Uncharacteristic	Characteristic
12	0 30	5-7, 17-19, ..	11-13, 23-25, ..
18	0 20 40	5-7-11-13, ..	17-19, 35-37, ..
24	0 15 30 45	5..19, 29..37	23-25, (47-49) ..
36	0 10 20 30 40 50	5..31, 41..	35-37

In actual transformer design, particularly for small numbers of turns, the exact cancellation is not possible and uncharacteristic harmonics may be expected to remain, up to 0,05 to 0,2 p.u. of the theoretical value for the equivalent 6-pulse connection with the same (total) rating.

Other factors such as direct current ripple, phase unbalance, also have an effect on the harmonic spectrum.

5.5.8 Sequential gating, two 6-pulse converters

In certain cases where minimizing reactive power consumption is considered essential, sequential gating of converters may be used with advantage:

– the reactive power consumption is considerably reduced for DC voltage values below 0,5 p.u. of the rated or maximum value. This is particularly useful for large reversing mills where the roll bite occurs at about half speed and the steady-state intervals are relatively short;

– the two 6-pulse converters may be fed from the same transformer YY or DD. The harmonic spectrum is nearer that of the 12-pulse connection than that of the 6-pulse connection, whenever:

$$\alpha_1 - \alpha_2 = 30°$$

However, these advantages may not be sufficient to compensate for the other consequences:

– for networks where short power outages are to be expected, the operation of the inverter section is impaired with possible tripping or fuse blowing;

– the harmonic spectrum is often similar to the 6-pulse connection typical spectrum: the reduction of the 5^{th}-7^{th}, 17^{th}-19^{th} … harmonics is valid only when $|\alpha_1 - \alpha_2| \approx 30°$. Therefore the harmonic filter, if any, shall be designed for it;

– the reduced reactive power demand would permit the capacitor rating to be lowered but the harmonic overloading may require some oversizing of the capacitors.

Therefore, it does not seem possible to give a simple rule in such cases and several alternatives may have to be compared in each case of application, depending on the supply system and operating conditions.

5.6 Power factor compensation and harmonic distortion

5.6.1 General

The use of power capacitor banks is increasingly necessary due to the energy saving policy:

a) the Supply Authority may specify a minimum power factor;

b) the power losses in cables and transformers are increased by the reactive power;

c) the transformers, cables, switchgear may be overloaded without compensation.

However, the use of capacitors should be studied carefully if converter loads are a significant part of the system load.

5.6.2 Resonant frequency

AC motor loads may significantly change the harmonic impedance and the chart in Figure 8 may be used at a preliminary stage of the design to find the estimated resonant frequency and amplification factor. The system impedance is assumed to be purely inductive/resistive (Q_s = 8 p.u., Q_p = 100 p.u.). The cable capacitance should be added to the capacitor bank.

5.6.3 Directly connected capacitor bank

From experience, the use of directly connected capacitor banks on the AC side of a converter without transformer is not recommended, particularly if the minimum operational AC motor load is small.

The power factor correction would be provided for preferably on the primary side of the converter transformer to avoid extremely high di/dt stresses on the semiconductors. Choke reactors may be used to minimize these stresses, but the harmonic currents may still overload directly connected capacitors, although the capacitor connecting cables introduce some reactance.

Care should be taken also in the case of radio interference filters which may suffer from harmonic current overloading.

5.6.4 Estimation of the resonant frequency

The resonant frequency of a capacitor bank with the system inductance is given by:

$$f_r = h_r \times f_1$$

where

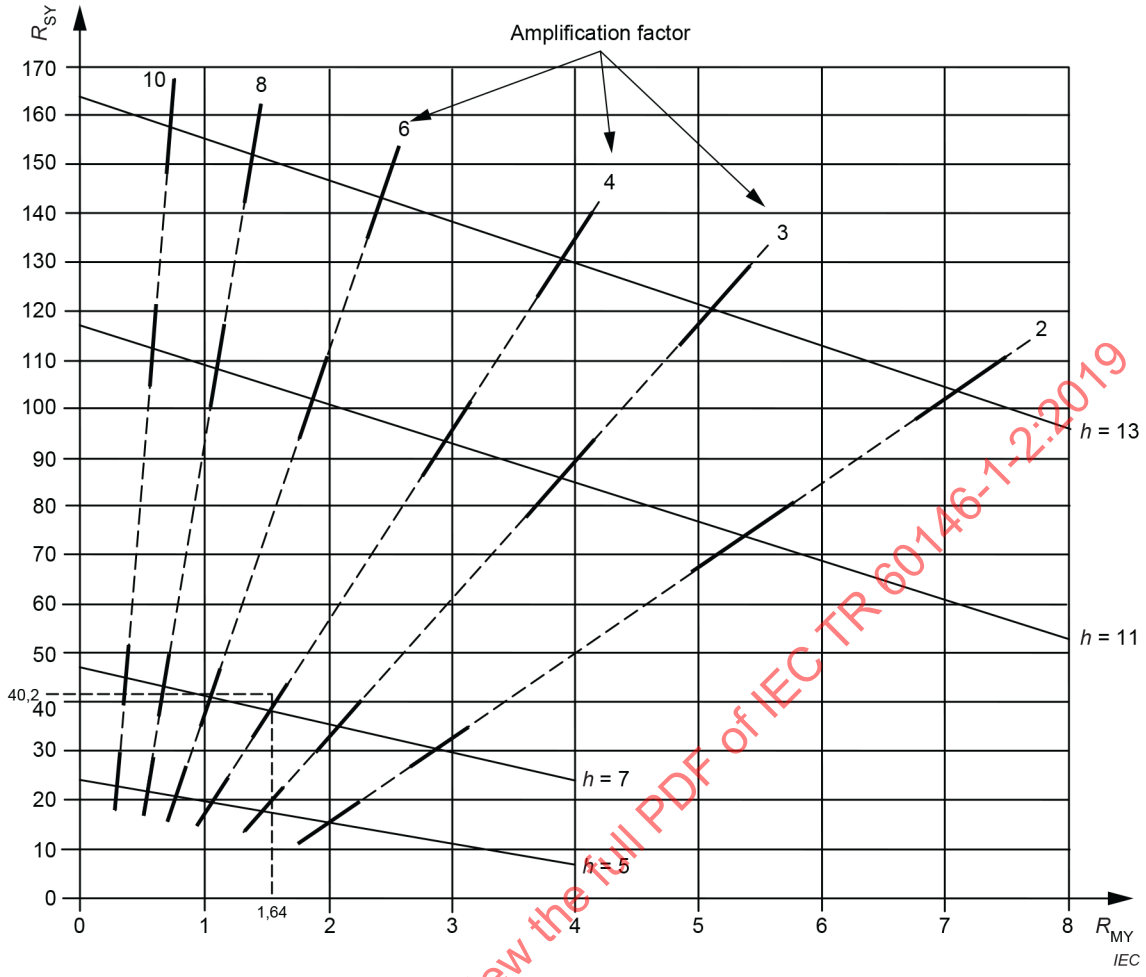
$f_r = \sqrt{S_C / Q_c}$;

Q_c is the capacitor bank rating.

If the AC motor load S_M is significant, use Figure 8

where

$$R_{SY} = \frac{S_C}{Q_c} \text{ and } R_{MY} = \frac{S_M}{Q_c}$$



NOTE The amplification factor value is only valid in the regions close to the intersections, not along the dotted part of the lines.

Figure 8 – Influence of capacitor rating and AC motor loads on the resonant frequency and amplification factor

EXAMPLE

Supply source:		92 MVA, 20 kV
AC motor/load:		1 MVA (total 850 kW, $\cos\varphi_N$ = 0,85)
Converter load:		500 kVA (400 kW DC motor)
Supply transformer:		2 MVA, 20/0,4 kV, e_{xtN} = 0,06 p.u.
Power factor correction:	AC motor:	250 kvar
	converter:	360 kvar
	total:	610 kvar
Short-circuit power at 400 V bus:		24,5 MVA

Expected resonant frequency:

$$f_r = \sqrt{\frac{24{,}5}{0{,}61}} \times f_1 = 6{,}34 \times f_1$$

Co-ordinates for use of the chart, Figure 8:

$R_{MY} = S_M / Q_c = 1 / 0,61 = 1,64$

$R_{SY} = S_C / Q_c = 24,5 / 0,61 = 40,2$

The corrected resonant frequency is found close to $7f_1$.

The amplification factor may be expected to be about 4.

The R_{1SC} is 24,5/0,5 = 49 and from Table 13 (6-pulse converter), the *THD* would be 0,05 p.u. and the 7th harmonic 0,02 p.u. but the amplification factor would give 0,02 × 4 = 0,08 p.u. for the 7th harmonic which may be acceptable for an in-plant bus bar, but not for a public network.

5.6.5 Detuning reactor

A detuning reactor should be adopted to prevent resonance.

a) A power capacitor is usually made of a number of parallel and series connected capacitor elements, made from aluminium foil wound with a dielectric film. The inductance of the capacitor gives a self-resonant frequency in the order of 10 kHz to 50 kHz.

b) In addition to this, the inductance of the connecting cables may introduce a lower resonant frequency, which may be as low as 2 kHz to 5 kHz depending on the length, size and arrangement of the cables. (The cable capacitance may be neglected against the capacitor bank up to several kilohertz).

c) In order to limit the inrush current, choke reactors are often used with about 50 μH or 60 μH inductance (MV system). However, the resulting series "tuning" frequency still remains in the order of 50 to 70 times the rated frequency for MV capacitor banks.

d) If the parallel resonant frequency is found to be close to one of the existing harmonics, it may be necessary to use a detuning reactor with a larger inductance than that of a choke reactor. For example, in the case of a 12-pulse converter, the residual 5th and 7th harmonics if amplified by a factor of 5 to 10 may result in capacitor overloading and other unwanted effects.

e) In such a case, a detuning reactor may be used to shift the resonant frequency to a lower value (below the 5th but not to coincide with the 4th nor the 3rd harmonic). Damping may be improved by an additional resistor.

f) The following formula may be used as a first approach:

$$\frac{1}{h_r'^2} = \frac{1}{h_a^2} + \frac{Q_c}{S_C}$$

where

h_r' f_1 is the new resonant frequency;

h_a f_1 is the tuning frequency;

Q_c is the capacitor rating;

S_C is the system short-circuit power at the capacitor bus-bars.

EXAMPLE

Q_c = 2,56 Mvar

h'_r = 4,25

S_C = 125 MVA

h_a = 5,35

$f_a = h_a f_1$

This is the required tuning frequency.

NOTE In this example, the tuning frequency is above the 5th harmonic, but if AC motor or other loads and several values of S_c have to be considered, the formula above and the chart Figure 8 may not be sufficient, particularly if the R_{1SC} factor is on the borderline of the required compatibility level.

5.6.6 Ripple control frequencies (carrier frequencies)

In most public networks, the remote control and monitoring (switchgear, voltage control, load flow parameters) are operated using a superimposed control voltage with a particular rated frequency which may be 175 Hz, 188 Hz, 595 Hz or other frequencies different from any significant harmonic of the power frequency.

In certain cases, the use of capacitor banks, possibly with choke or detuning reactor, will increase the system impedance at a particular frequency, which may amplify stray transients which could impair the ripple control system.

This problem should be examined in co-operation with the relevant authorities. The use of blocking filters may be contemplated, for preventing both the attenuation of the wanted signals and the amplification of stray transients in the frequency range of the ripple control system.

5.7 Direct voltage harmonic content

The RMS value of the harmonic component of order h, of the superimposed AC voltage (ripple components), referred to the no-load ideal DC voltage is calculated by the next formula. Figure 9 shows its results for $p = 6$.

$$U_h = \frac{U_{di}}{\sqrt{2}} \times \sqrt{e^2 + f^2 - 2 \times e \times f \times \cos(2\alpha + \mu)}$$

Harmonic order $h = k \times p$; with: p = pulse number; k = positive integer.

where

$$e = \frac{1}{h-1} \times \cos\frac{(h-1) \times \mu}{2};$$

$$f = \frac{1}{h+1} \times \cos\frac{(h+1) \times \mu}{2}.$$

NOTE A harmonic component of order $2f_1$ will appear if the AC side voltage is unbalanced. Its magnitude referred to U_{di} is approximately equal to the negative sequence voltage referred to the rated value (positive sequence).

Other non-characteristic harmonics will also arise if the gating signals are unevenly spaced over a period.

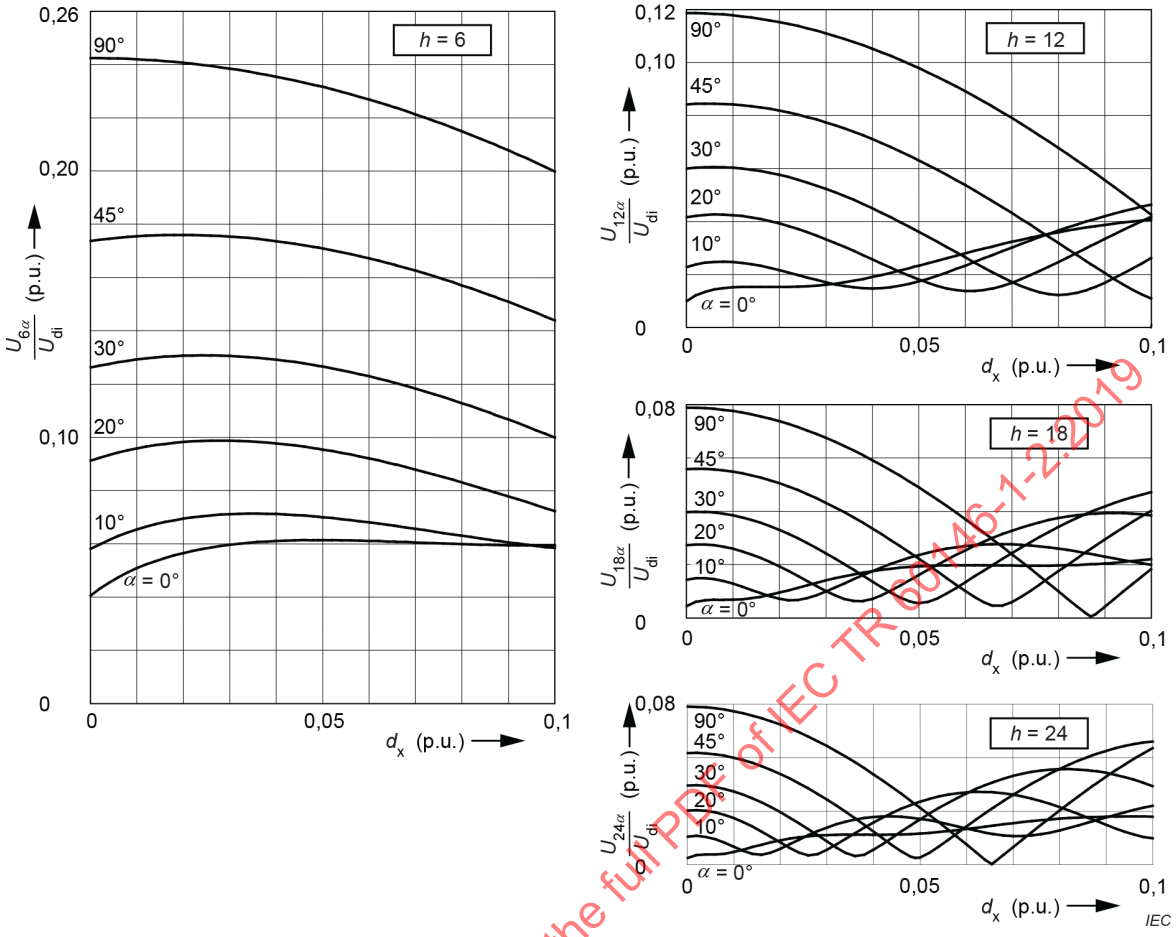


Figure 9 – Direct voltage harmonic content for $p = 6$

5.8 Other considerations

5.8.1 Random control angle

For the case of many converters used with uncorrelated duty cycles, the estimation of the reactive power demand and harmonic current spectrum may be based either on the worst case conditions or on the available data: type of industry, type of application or previous experience on similar applications.

The worst case approach leads to a higher safety margin, the usual result being increased size, cost and losses. It should not be used, unless the worst case conditions may exist with more than, for example 0,05 p.u. probability or for more than a few minutes per hour.

In most cases, the design should be based on the most likely conditions subject to checking that no damage would occur in the worst case conditions although the performance may not be achieved.

In certain cases, the optimum design requires the consideration of a number of alternatives.

5.8.2 Sub-harmonic instability

Cases of sub-harmonic instability have been recorded, some of them attributable to excessive harmonic distortion with variable wave deformation. This is a case of a converter being disturbed by itself due to the influence of unsuspected resonance of a capacitor bank with the system inductance. It may appear for a frequency up to that of the 4th harmonic, particularly for high performance, fast response control.

5.8.3 Harmonic filters

If no solution can be found with changing the resonant frequency or the capacitor rating and generally if the distortion is too high, a harmonic filter may be required.

This is outside the scope of this document.

5.8.4 Approximate capacitance of cables

If the system voltage is 15 kV or above, the cable capacitance may not be neglected particularly for extensive systems.

Table 15 was calculated using the average value of 0,32 μF/km to 0,25 μF/km depending on the insulation level and cable section.

Table 15 – Approximate kvar/km of cables

Supply frequency	System voltage kV									
Hz	6	10	13,8	15	20	25	30	63	90	150
50	3	8	16	19	33	51	73	317	643	1 770
60	4	11	20	22	42	65	92	391	784	2 121

5.9 Calculation of DC short-circuit current of converters

The steady-state value of some converter currents in case of short-circuit on the DC side of the converter can be evaluated using Table 16.

The table gives the ratio of the short-circuit current to the value of I_{dN}/e_{xN} for some of the connections listed in Table 16.

Table 16 – Short-circuit values of converter currents

Table 1 connection no.	Valve side current RMS p.u.	Arm current value			DC current average value p.u.
		RMS p.u.	Peak p.u.	Average p.u.	
1	0,71	0,71	1,41	0,45	0,90
2	0,74	0,74	1,15	0,55	1,65
3	0,33	0,33	0,66	0,21	1,27
5	0,29	0,29	0,58	0,18	1,10
6	0,22	0,22	0,44	0,14	0,85
7	1,00	0,71	1,41	0,45	0,90
8	0,82	0,58	1,15	0,37	1,10
9	0,40	0,28	0,56	0,18	1,07
12	0,80	0,56	1,12	0,36	1,07

5.10 Guidelines for the selection of the immunity class

5.10.1 General

As for electromagnetic compatibility, see IEC 60146-1-1:2009, 3.9, 4.3.3 and 5.4.1.

5.10.2 Converter Immunity class

The immunity classes A, B and C and immunity levels for each class are defined in IEC 60146-1-1:2009, 5.4.1.

a) Class A levels are used for converters intended to meet severe line conditions such as in the case of several converters directly connected to a common transformer (converter dedicated bus bar) with low R_{1SC}.

   Such converters may also be preferred for cases where the probability of exceeding class B or C levels is low but the consequences of a failure would be costly or dangerous or if other converters or disturbing loads are planned to be added in the future.

b) Class B levels are used for converters intended to meet the average conditions to be expected in most places, most of the time. They may be used on general purpose industrial systems, together with other types of loads such as AC motors.

   Such converters may also be used for severe line conditions, provided corrective means are used to improve these conditions (surge suppressors, isolating transformers, harmonic filters, static compensators) as required to keep the disturbance levels below class B immunity levels with a low enough probability of being exceeded to meet the required availability.

c) Class C levels are used for converters that may be used in the case of widely dispersed, low power units with a relatively large R_{1SC}, for non-critical functions, on systems with fairly constant load.

   These may be used on high quality systems provided their use on such systems does not appreciably change the disturbance levels.

5.10.3 Selection of the immunity class

The selection of the immunity classes of converters implies the assessment of their service conditions that are to be compared with the specified immunity levels of immunity classes. Therefore, a good knowledge is required of the operating conditions of the supply network.

It is assumed that the design of supply network follows good engineering practice with due regard to current carrying capability, short-circuit and overvoltage protection, power factor, etc.

It is also assumed that the network capacity is adequate to supply active and reactive power as required by the loads, including converters, within allowable voltage immunity levels. As a first step it is deemed necessary to get information on conventional network parameters such as frequency variations and AC voltage amplitude and unbalance at the most important junctions of the network, under steady-state and transient conditions. In so doing, consequences of non-linear behaviour of converters can be disregarded and only fundamental components of converter quantities taken into consideration.

Then, to complete assessment of electrical service conditions of converters, all aspects pertaining to voltage and current waveforms should be considered.

This will allow a good adaptation of converters to their final uses and to the electrical service conditions of their supply buses. But one should keep in mind that those conditions may vary with the number of loads connected, the supply bus connections, the variations observed on public network, etc.

Evaluation of the parameters of voltage and current distortion can be performed using information already given in this section.

An example is added in the following.

If a converter complies with immunity levels of a certain class, say B, converter generated disturbances, when added to existing disturbances on the line, shall not exceed the immunity

limits of the selected class (class B in this example). Therefore, transformers or AC reactors are usually needed, with the only possible exception of class A converters.

EXAMPLE

See the diagram of Figure 10 that shows a simplified diagram of power distribution for an industrial plant (below the dashed line) and the relevant elements of its supply network (above the dashed line).

Ratings and other relevant quantities are included in Figure 10.

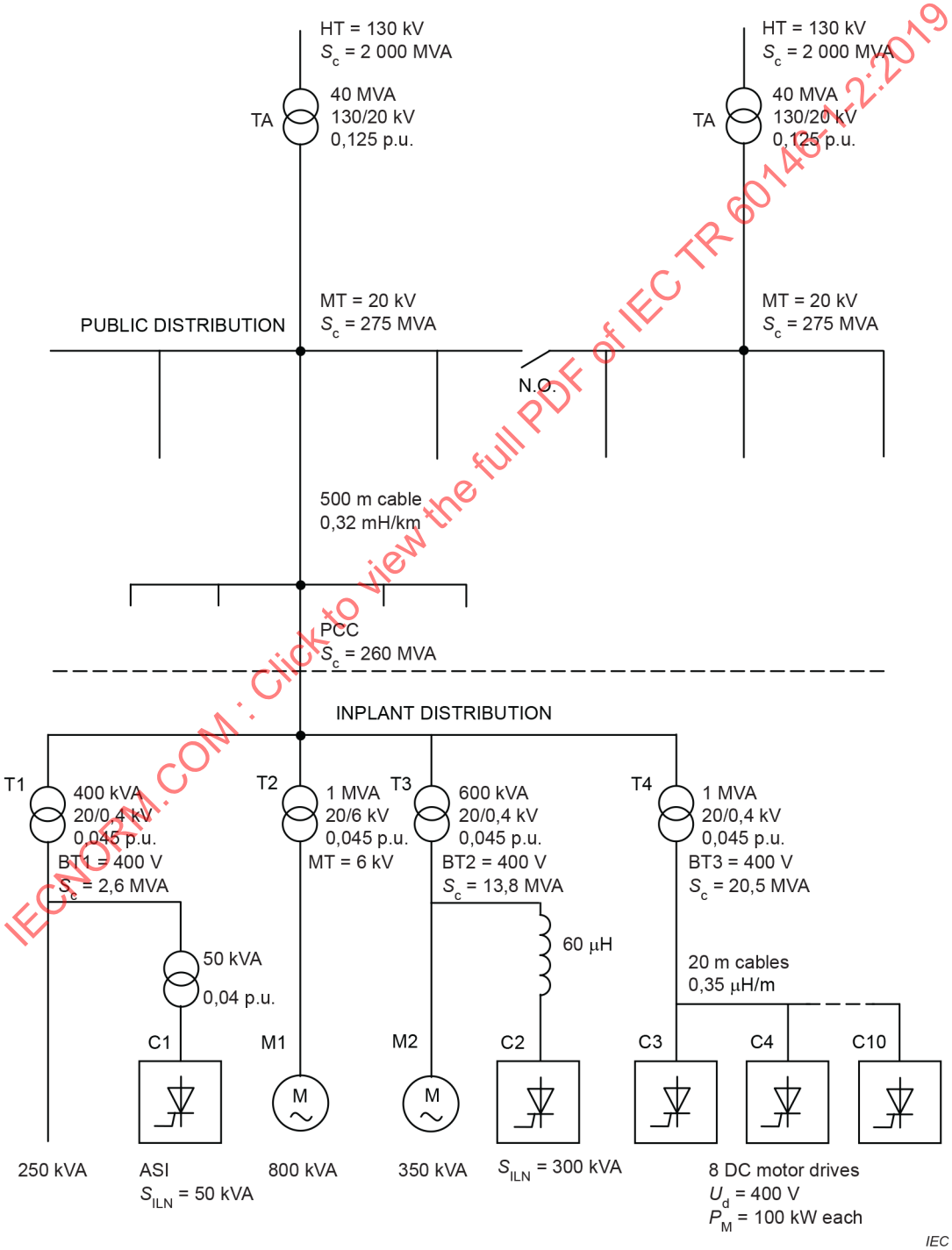


Figure 10 – Example of power distribution

NOTE 1 The HV to MV transformers (TA and TB) are never operated in parallel. In case of failure of one transformer the other can supply also the loads of the failed transformer within its overload capability (1,3 p.u.).This prevents any change of short-circuit power on public distribution network.

NOTE 2 The example does not include power factor correction capacitors, as usual in case of a first approach for evaluation of the severity of voltage distortion.

NOTE 3 The DC motor drives connected to LV3 bus-bar are assumed equivalent to a single converter with a diversity factor of 0,8.

NOTE 4 The example does not take into consideration the contribution to the short-circuit power from the AC motors.

Assumptions on types of lines:

MV	"public distribution" (outside user's premises) and "in-plant distribution";
LV1	"high quality line" for sensitive (low immunity) equipments and converters complying with immunity levels of class C, like C1;
LV2, MV1	"in-plant distribution line" for general purpose equipments and converters complying with immunity levels of class B, like C2;
LV3	"converter dedicated line" for converters complying with immunity levels of class A, like C3 to C10.

Converter classes

Converter C1:	class C
Converter C2:	class B
Converters C3 to C10:	class A.

Table 17 shows calculated data for the plant of Figure 10.

Table 17 – Calculated values for the example in Figure 10

	$1/S_C$	S_C	Total load	Converter load	Harmonic distortion	Notch depth	$\Delta U/U$
	MVA^{-1}	MVA	kVA	kVA	p.u.	p.u.	p.u.
Line 130 kV	$2\,000^{-1}$	2 000					0,007
Transformer TA 40 MVA	320^{-1}						
20 kV bus		275,8					
MV cable (0,32 mH/km)	$7\,957^{-1}$						
Point of common coupling		266,6	2 300	1 250	0,011[a]	0,1[b]	0,006
Transformer T_1	$8{,}9^{-1}$						
Line LV_1		8,6	300	50	0,0134	0,127	0,024
Transformer T_2	$1{,}25^{-1}$						
Converter terminals		1,09		50	0,106	1,0	
Transformer T_3	12^{-1}						
Line LV_2		13,76	600	300	0,05	0,38	0,03
Motor 350 kVA		2,275[c]	300				
Reactors 60 µH	$8{,}5^{-1}$						
Converter terminals		5,25		300	0,132	1,0	
Transformer T_4	$22{,}2^{-1}$						
Line LV_3		20,5	900	900	0,101	0,97	0,031
Cable 400 V 20 m, 8// (0,35 µH/m)	582^{-1}						
Converter terminals		20		900	0,104	1,0	

The calculated values of harmonic distortion, notch depth and voltage regulation $\Delta U/U$ take into consideration only the effect of the loads shown in Figure 10. The contribution of other loads that influence the MV bus should be added.

NOTE 1 As can be seen from the values of Table 17, converter loads can be tolerated without problems, thanks to the relative stiffness of PCC. In Table 17 the three figures that sum the total harmonic distortion and notch depth at PCC are the individual contributions of the three converter loads.

NOTE 2 AC reactors are necessary on the AC supply of converter C2 to avoid notch amplitude on LV2 exceeding the maximum allowable value for class B.

[a] 0,0004 + 0,0026 + 0,0078 = 0,0108

[b] 0,0041 + 0,02 + 0,075 = 0,1

[c] 0,35 × 6,5 = 2,275 (for $I_{start} / I_N = 6{,}5$)

6 Test requirements

6.1 Guidance on power loss evaluation by short-circuit test

6.1.1 Single-phase connections

Power losses can be determined from a direct measurement of input and output power at rated load or can be calculated from segregated loss measurements, at the option of the supplier.

6.1.2 Polyphase double-way connections

Short-circuit power losses may be measured by test methods A1, B or C (see 6.3).

6.1.3 Polyphase single-way connections

Short-circuit power losses may be measured by test methods A2 (modification of A1), B, C, D and E (see 6.3).

6.2 Procedure for evaluation of power losses by short-circuit method

The DC terminals of the stack or assembly shall be short-circuited and its AC terminals shall be supplied through sufficient reactance to cause the input current to be practically sinusoidal and at a voltage sufficient to cause the desired value of current to flow, at rated frequency. The input power shall be measured at the AC terminals of the stack or assembly. The accuracy of the watt-meters used should not be impaired by operating conditions, for example low voltage, stray magnetic fields, etc.

Two short-circuit tests shall be performed in quick succession at rated direct current I_{dN} and at $k \times I_{dN}$, where

$$k = \frac{FF_S}{FF_T}$$

where

FF_S is the form factor of arm current in real service (neglecting overlap);

FF_T is the form factor of arm current at test.

A first measurement of losses P_2 is made after reaching constant temperature at $k \times I_{dN}$. A second measurement of losses P_1 is made as quickly as possible after reducing the current to I_{dN}.

The losses P corresponding to rated direct current in normal service are calculated by means of the following formula:

$$P = \frac{k+1}{k} \times P_2 - k \times P_1$$

Where appropriate, the loss in the DC short-circuiting connections and shunts, if appreciable, shall be measured and deducted from P_1 and P_2.

The losses so evaluated are those expected in the case of negligible overlap.

The method is valid under the following assumptions (see also IEC 60146-1-1:2009, 7.4.1.1).

a) The forward voltage drop in the valves can be represented by a constant component (threshold voltage) plus a resistive component directly proportional to the current.

b) The difference between stray losses in normal operation and under test, due to different current waveforms, is compensated by larger RMS values of the test currents.

c) The inductance of the circuit on the DC side of the converter is negligible.

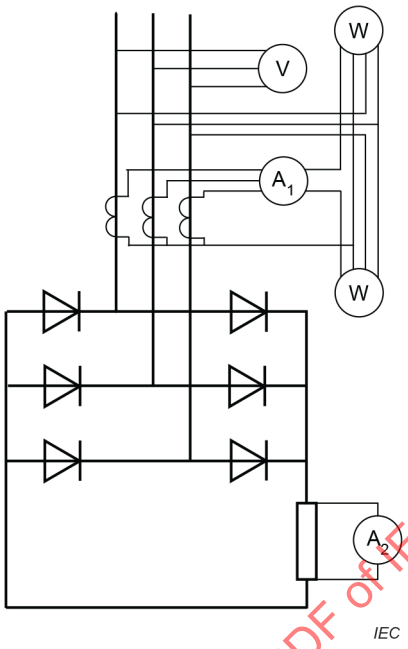
NOTE In double way connections, the inductance of the DC circuit can cause, through free-wheeling, DC output current larger than the corresponding AC current.

The test shall be performed in accordance with 6.3.1 to 6.3.6 according to the connection used. In all cases, the losses that will occur in service in voltage dividing resistors, damping circuits and surge diverters, if any, shall be calculated and added. In the case of thyristor converters, the control angle should be set at the minimum possible value.

6.3 Test methods

6.3.1 Method A1

This method is suitable for double-way connections. The test circuit is shown in Figure 11.



Key

A_1 AC ammeter indicating RMS values

A_2 DC ammeter indicating average values

V AC voltmeter indicating RMS values

W wattmeter

Figure 11 – Test method A1

This measurement shall be performed at 1,1 × I_{dN} and I_{dN} and the power loss in the assembly in service at rated direct current is taken to be:

$$P = 1{,}91 \times P_2 - 1{,}1 \times P_1$$

NOTE The form factor of arm current in real service (neglecting overlap) has the value $\sqrt{3} \approx 1{,}73$.

The form factor of a semi-sinusoidal waveshape, as in test, has the value $\pi/2 \approx 1{,}57$.

The value of k, ratio of form factors, is then $2\sqrt{3}/\pi \approx 1{,}1$. Therefore, the coefficients of the formula of 6.2 take the values shown.

The equation assumes essentially sinusoidal line current wave shapes on test.

If sinusoidal currents are not obtained, the multipliers for I_{dN}, P_2 and P_1 shall be determined by the method given in 6.2.

If the test apparatus does not permit adjustment of the currents to exact values specified above, then measurements should be taken at currents slightly above and below the specified values and the active power input obtained by interpolation between the measured wattmeter readings at these values.

6.3.2 Method B

This method is suitable for single and double-way connections.

In those cases where a complete converter, including transformer, is supplied by one manufacturer and when it is convenient to measure only the total converter losses, a method of measurement similar to A1 is used, but with the wattmeters connected on the line side of the transformer.

The transformer should have reached steady-state temperature corresponding to P_2 and the transformer copper losses should be corrected to reference temperature with specified temperature rise plus 20 K.

Measurements made under method B may be used as part of the transformer temperature rise determination.

6.3.3 Method C

This method is suitable for single and double-way connections.

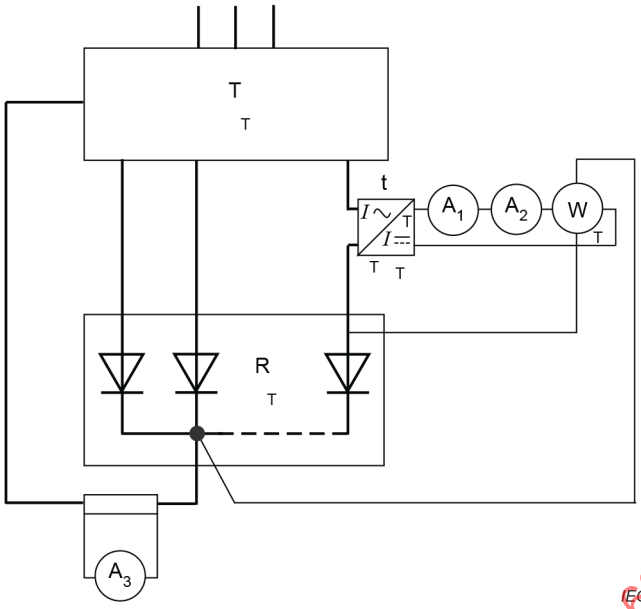
A calibrated test transformer may be used instead of the particular rectifier transformer of method B. The losses of the rectifier assembly are equal to P minus the losses of the test transformer.

The actual transformer may be calibrated and used as the test transformer when separate losses are required.

6.3.4 Method D

This method is suitable for single-way connections.

The test is performed as a short-circuit test with a circuit shown in Figure 12.



Key

R rectifier stack or assembly under test, having *n* arms (first, second and last are shown)

T rectifier transformer, either transformer for contract concerned or equivalent test

t DC current transducer of sufficient bandwidth

a current ratio of transducer "t"

W low-voltage wattmeter (resistance of current coil < *r* 1 000)

A_1 AC ammeter, indicating RMS values

A_2 DC ammeter, indicating average values

A_3 DC ammeter, indicating average values

I_1 RMS current indicated by A_1

I_2 average current indicated by A_2

I_3 direct current of stack or assembly, indicated by A_3

P power indicated by W

Figure 12 – Test method D

As a check on the current measurement in the rectifier arm, the relationship between the readings of ammeters A_2 and A_3 is verified.

Where the current rating of the rectifier is small enough, the transducer may be omitted and A_1, A_2 and W connected to measure the rectifier arm current directly.

The measurements are to be performed at average arm currents:

$$I_2 = \frac{I_{dN}}{n} \text{ and } I_2 = k \times \frac{I_{dN}}{n}$$

where

n is the number of rectifier arms in stack or assembly;

k = $\sqrt{3}/FF_T$ for polyphase 120° conduction;

k = $\sqrt{6}/FF_T$ for polyphase 60° conduction;

FF_T is the form factor of rectifier arm current in the test at $I_2 = I_{dN}/n$, as measured by ammeters A_1 and A_2.

$$FF_T = I_1/I_2$$

If P_1 and P_2 are the powers indicated by wattmeter W at average arm currents

$$I_2 = \frac{I_{dN}}{n} \text{ and } I_2 = k \times \frac{I_{dN}}{n}$$

respectively, then the power loss in the rectifier stack or assembly at rated direct current I_{dN} is taken to be:

$$P = n \times a \times \left(\frac{k+1}{k} \times P_2 - k \times P_1 \right)$$

where

a is the ratio of transducer t.

If the supplier certifies that the arms of the rectifier stack or assembly are substantially identical, then it could be regarded as sufficient if the test is done on only two arms, one near the middle of the assembly and one near the outside and the average of the losses is taken. The arms chosen should not be 180° apart and not on the same side of the interphase transformer if any.

All other losses in the assembly, not properly included in the loss measurement, shall be separately measured or calculated and added to P.

If the test apparatus does not enable the current to be adjusted to the exact values specified above, then measurements shall be taken at currents slightly above and below the specified values and the active power input at the specified current then obtained by interpolation between these measured values.

In heavy current assemblies, the arm loss measurements of methods D (Figure 12) and A2 (6.3.6) should be carried out by attaching the DC end of the wattmeter voltage lead to the junction between the arm and the duct (DC collector bar). The wattmeter then measures only "arm" losses.

The duct loss shall be obtained separately:

a) by calculation, or

b) by separate measurement.

A satisfactory method is to measure the average drop (in millivolts) along each section of the duct during a short-circuit test at rated current. The real service loss in each section of the duct is then given by:

$$P = U \times I \times (FF_S)^2$$

where

U is the voltage drop of section, average value;

I is the current of section, average value;

FF_S is the real service current form factor in section.

6.3.5 Method E

This method is suitable for single-way connections.

If one rectifier assembly can be completed by another assembly equal to it to form a double-way connection, the power loss measurement may be performed according to the method described in 6.3.1 (method A1).

In connecting two rectifier assemblies to form a double-way connection, care shall be exercised to avoid significant change of losses in the heavy current bus-bar connections (duct).

6.3.6 Method A2

This method is suitable for single-way connections.

Method A2 is substantially the same as method A1, with the DC transducers connected in the bars of a single commutating group of the single-way connection as shown in Figure 12 of method D.

The AC and DC ammeters shall be used, as in method D.

Measurements may be made successively on individual commutating groups and added. If tested in this manner, the temperature of the transfer agent should be adjusted to obtain approximately the same internal temperature as in normal operation.

7 Performance requirements

7.1 Presentation of rated peak load current values

All information on permissible peak loads should be given in terms of current, amplitudes, durations and repetition frequency or idle times. IEC 60146-1-1:2009, 6.4.3, is based upon this principle.

In cases where no suitable standard duty class can be found in IEC 60146-1-1:2009, Table 12, there are many possible ways in which peak load information can be given. The example in Figure 13 and Figure 14 below may serve the purpose to introduce the basic approach of presentation in the case of single peak loads and repetitive peak loads.

When the base load current I_b is less than I_{dMN}, peak loads of the value I_{p1} may be superimposed for the time t_p but only with long enough intervals to assure equilibrium temperatures to be obtained before each peak load.

Repetitive peak loads with the value I_{p2} may be superimposed for the time t_p with intervals equal to T. It is to be noted that the diagram for repetitive peak loads as given in the example is valid only for one single value of the base load I_b.

Whatever form of presentation is used, the cooling conditions shall be specified.

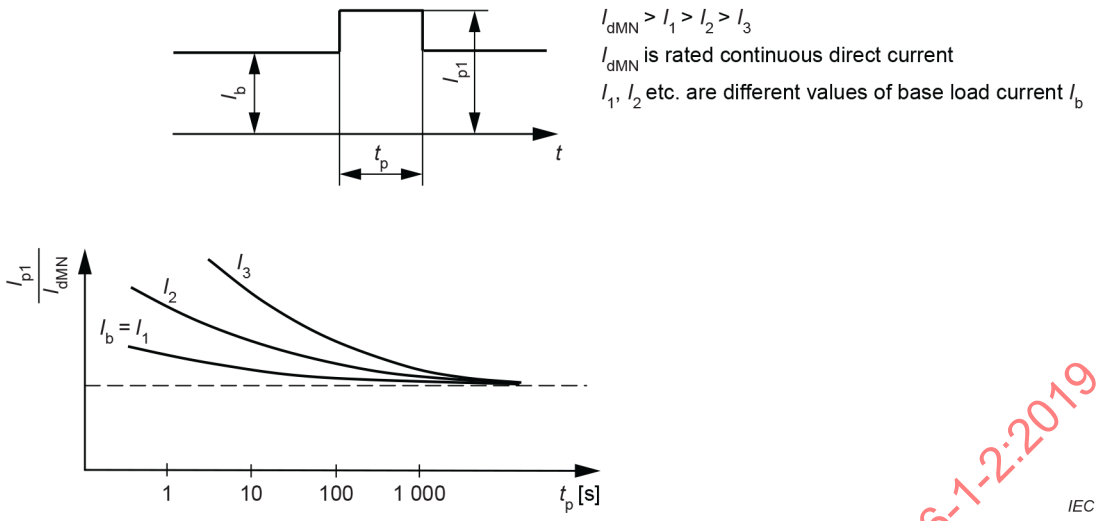


Figure 13 – Single peak load

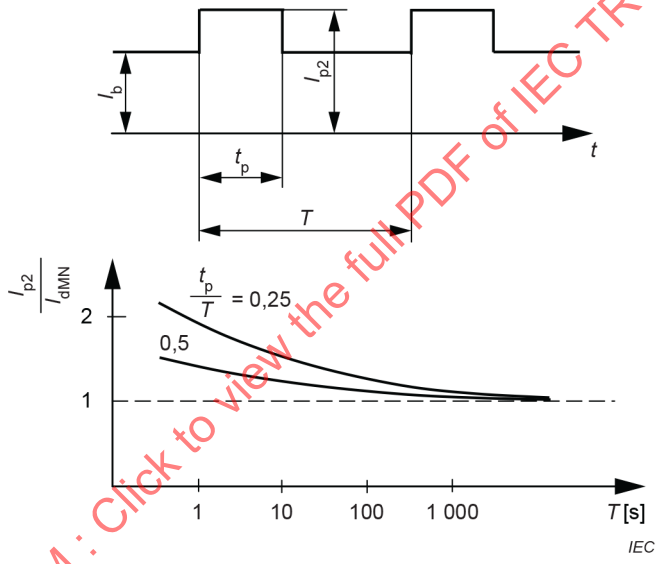


Figure 14 – Repetitive peak loads

7.2 Letter symbols related to virtual junction temperature

The letter symbols related to virtual junction temperature are given in Table 18.

Table 18 – Letter symbols related to virtual junction temperature

Symbol	Quantity
T_j	virtual junction temperature (see 3.3.3)
$T_{j(avg)}$	mean value of the virtual junction temperature over one period of the supply frequency
$T_{j(avg)n}$	$T_{j(avg)}$ referred to the instant t_n
ΔT_j	difference between the maximum instantaneous virtual junction temperature and $T_{j(avg)}$
$\hat{T}_j$	maximum instantaneous value of the virtual junction temperature
T_x	temperature in a specified external reference point x, for example the ambient temperature of a converter
P_{avg}	mean value of the on-state or forward power losses averaged over one period of the supply frequency
$\hat{P}$	maximum instantaneous value of the on-state or forward power losses
$\hat{P}_{avg}$	maximum instantaneous value of P_{avg}
P_M	mean value of $\hat{P}_{avg}$, averaged over one period of the load cycle
ΔP_ν	the step of power loss at the instant t_ν
k	number of power loss steps preceding the instant t_n
t_1	equivalent conducting period of one arm of a converter connection
t_p	equivalent pulse duration of the peak load pulse
f_{1N}	rated supply frequency
T	one period of the load cycle
T_{1N}	one period corresponding to the rated supply frequency
R_{th}	thermal resistance (see 3.3.1)
R_T	R_{th} corresponding to the interval T
Z_{th}	transient thermal impedance (see 3.3.2)
$Z_{n\nu}$	Z_{th} corresponding to the interval $t_n - t_\nu$
Z_{t1}	Z_{th} corresponding to the interval t_1
Z_T	Z_{th} corresponding to the interval T
Z_{t1+T}	Z_{th} corresponding to the interval $t_1 + T$
Z_{tp}	Z_{th} corresponding to the interval t_p

7.3 Determination of peak load capability through calculation of the virtual junction temperature

7.3.1 General

The calculation of the virtual junction temperature is the basis for determination of peak load capability of diode or thyristor stacks or assemblies, but generally such temperature is not the only quantity to be checked to assess peak load capability.

Due to the complexity of the duty cycles, it is often convenient to use computer programs to calculate virtual junction temperature for many applications, particularly for repetitive load duties, complex equivalent circuits of heat transfer paths or non-linear relationship between temperature rise and power loss.

A method for calculating virtual junction temperature is shown in 7.3.3 to 7.3.6.

The method is valid under the following assumptions:

a) The virtual junction temperature to be calculated depends only on power of the power semiconductor device under consideration.

   In other terms, each power semiconductor has its own heat transfer path to the cooling medium, really or virtually independent from the heat transfer paths of other power dissipating elements of the stack or assembly.

   NOTE 1 This does not hold true for example in those four quadrant assemblies in which power semiconductors belonging to forward and reverse sections share the same cooling bodies.

b) Thermal resistance and transient thermal impedance between the virtual junction and the reference point are independent from the temperature, that is a linear relationship exists between the temperature rise and the power loss.

   NOTE 2 This condition is generally not satisfied in the case of convection cooling.

c) Semiconductor power losses are mainly conduction losses; turn-on, turn-off and voltage dependent losses. The voltage dependent losses may have to be considered particularly in the case of self-commutated converters or heavy current line-commutated converters.

7.3.2 Approximation of the shape of power pulses applied to the semiconductor devices

The equivalent power losses with rectangular waveshape pulses are selected to have:

- the same peak value as the actual power pulse (see Figure 15a));
- a pulse duration adjusted to give the same average value as the actual power pulses (see Figure 15b)).

This method for approximating the power losses is applicable:

a) within a period of the supply frequency, i.e. equal to the conduction period of one converter circuit element;

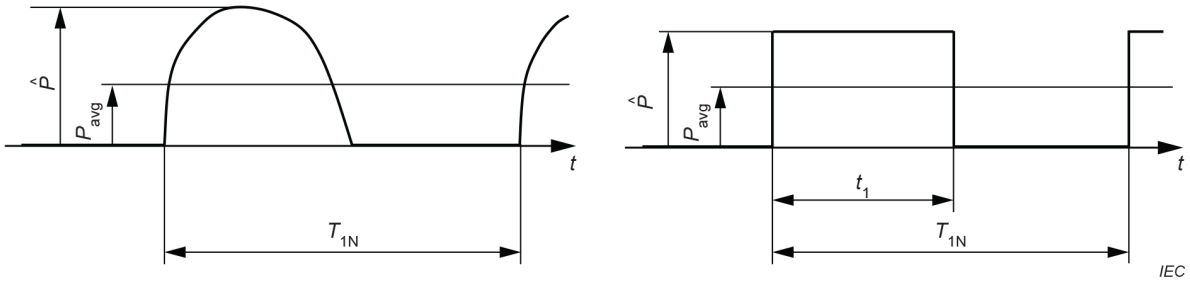
b) for the case when the load of a converter is cyclic with a period up to several minutes.

For case a)

$$t_1 = \frac{P_{\text{avg}}}{\hat{P}} \times T_{1\text{N}}$$

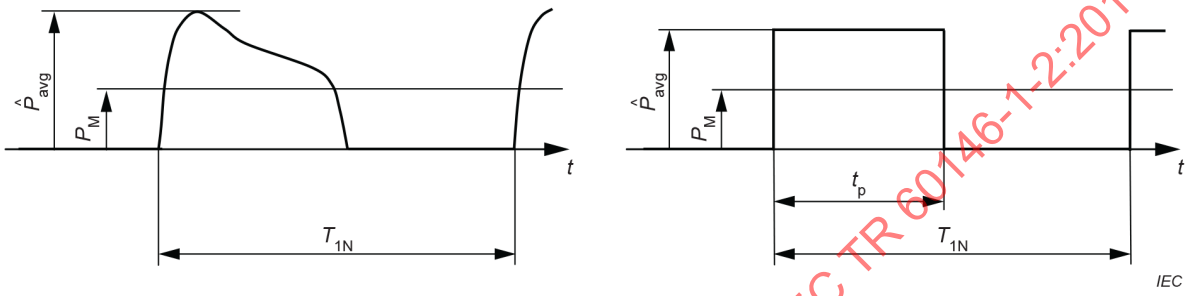
For case b)

$$t_p = \frac{P_{\text{M}}}{\hat{P}_{\text{avg}}} \times T$$



Actual power pulse **Approximated power pulse**

Figure 15a) One period corresponding to the rated supply frequency



Actual power pulse **Approximated power pulse**

Figure 15b) One period of the load cycle

Figure 15 – Approximation of the shape of power pulses

In some cases, especially for pulse durations longer than one second and for actual power loss pulses with shapes considerably diverging from rectangular waveform, it may be necessary to make up the approximated power pulse by several rectangular pulses of different amplitudes and durations to obtain a more accurate result. It is recommended that each of these pulses is selected to have the same duration and the same average value as the section of the actual power loss pulse it is substituting.

7.3.3 The superposition method for calculation of temperature

The method is based on the application of a transient thermal impedance curve. It is assumed that the power losses are represented as square wave pulses approximated according to 7.3.2.

The temperature difference T_n between two specified points A and B at the time t_n is given as the sum of temperature contributions from all power steps ΔP_ν preceding the time t_n.

$$T_{\mathrm{n}} = \sum_{\nu=1}^{n-1} \Delta P_\nu \times Z_{n\nu}$$

A positive power step gives a positive temperature contribution and a negative step gives a negative temperature contribution.

The method is exemplified in Table 19 (7.3.6).

7.3.4 Calculation of the virtual junction temperature for continuous load

7.3.4.1 General

Figure 16 shows an example of the power losses and the virtual junction temperature for continuous load. In this case, the virtual junction temperature varies with a frequency determined by the alternating line voltage.

The power loss approximated by the method given in 7.3.2 and the virtual junction temperature versus time are given by the diagram in Figure 16.

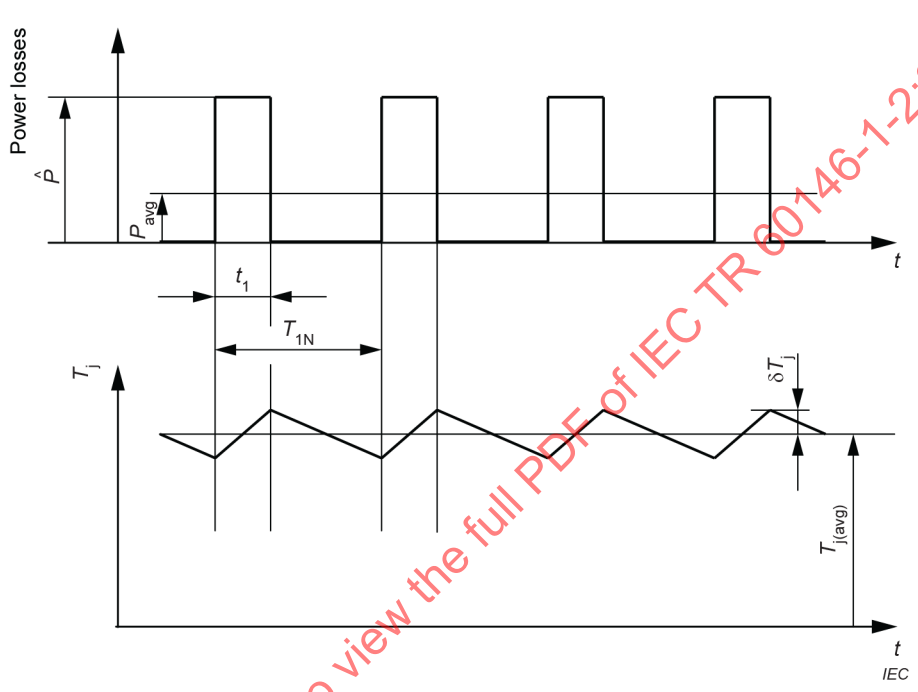


Figure 16 – Calculation of the virtual junction temperature for continuous load

7.3.4.2 Calculation of the mean value of the virtual junction temperature

The mean value of the virtual junction temperature is given by the formula:

$$T_{j(avg)} = T_x + P_{avg} \times R_{th}$$

7.3.4.3 Calculation of the maximum instantaneous virtual junction temperature

The maximum instantaneous virtual junction temperature within one cycle is calculated by the formula:

$$T_j = T_{j(avg)} + \Delta T_j$$

An accurate value of the temperature excursion ΔT_j can be calculated by the power pulse superposition method described in 7.3.3.

$$\Delta T_j = \frac{T_{1N}}{t_1} \times P_{avg} \times \left[\sum_{\nu=1}^{\frac{n}{2}} Z_{n(2\nu-1)} - \sum_{\nu=1}^{\frac{n-2}{2}} Z_{n(2\nu)} \right] - P_{avg} \times R_{th}$$

As ΔT_j normally is small compared to $\Delta T_{j(avg)}$, the following approximated formula is recommended:

$$\Delta T_j = \frac{T_{IN}}{t_1} \times P_{avg} \times \left[Z_{t_1} - Z_T + \left(1 - \frac{t_1}{T}\right) \times Z_{(t_1+T)} \right]$$

7.3.5 Calculation of the virtual junction temperature for cyclic loads

Figure 17 shows an example of the power losses and the virtual junction temperature for cyclic load. In this case, the virtual junction temperature varies with time at a frequency determined by the alternating voltage as described under 7.3.4 but also with a lower frequency determined by the load variations.

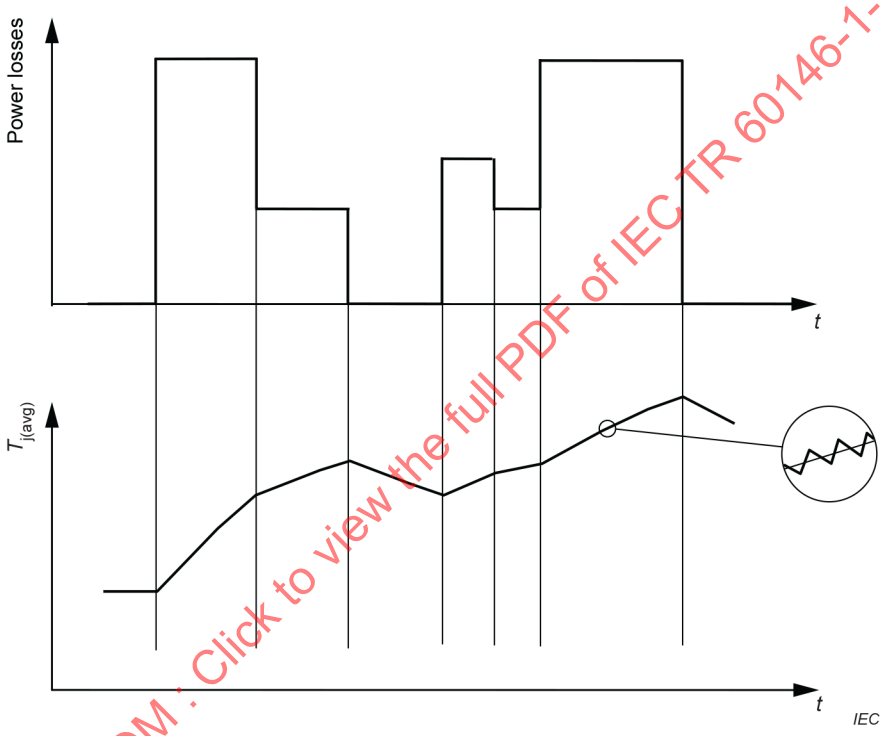


Figure 17 – Calculation of the virtual junction temperature for cyclic loads

The temperature excursion caused by the heating up of the junction during the conduction period and the cooling down is calculated in the same way as for continuous load according to 7.3.4. The mean value of the virtual junction temperature averaged over one cycle of the supply frequency at a certain time in the load cycle is calculated according to the method given in 7.3.4.2.

The mean virtual junction temperature at time t_n is thus given by:

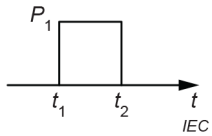
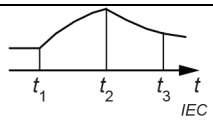
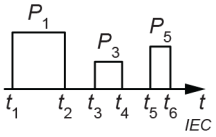
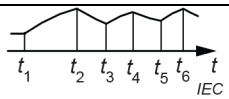
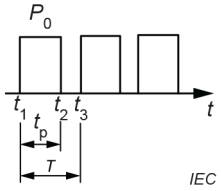
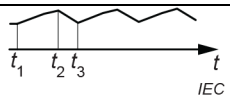
$$T_{j(avg)n} = T_x + \sum_{\nu=1}^{n-1} \left(\Delta P_\nu \times Z_{n\nu} \right)$$

The maximum instantaneous value of virtual junction temperature at time t_n is given by:

$$T_j = T_{j(avg)} + \delta T_j$$

7.3.6 Calculation of the virtual junction temperature for a few typical applications

Table 19 – Virtual junction temperature

Load condition	Power loss diagram	Mean virtual junction temperature diagram	Calculation formulae
Single load pulse			$T_{j(avg)2} = T_x + P_1 \times Z_{21}$ $T_{j(avg)3} = T_x + P_1 \times Z_{31} - P_1 \times Z_{32}$
Train of load pulses			$T_{j(avg)2} = T_x + P_1 \times Z_{21}$ $T_{j(avg)4} = T_x + P_1 \times Z_{41} - P_1 \times Z_{42} + P_3 \times Z_{43}$ $T_{j(avg)6} = T_x + P_1 \times Z_{61} - P_1 \times Z_{62}$ $+P_3 \times Z_{63} - P_3 \times Z_{64} + P_5 \times Z_{65}$ etc.
Long train of equal amplitude load pulses			$T_{j(avg)n} = T_x + \sum_{\nu=1}^{\frac{n}{2}} P_0 \times Z_{n(2\nu-1)} - \sum_{\nu=1}^{\frac{n-2}{2}} P_0 \times Z_{n(2\nu)}$ (n = even) $T_{j(avg)n} = T_x + \sum_{\nu=1}^{\frac{n-1}{2}} P_0 \times Z_{n(2\nu-1)} - \sum_{\nu=1}^{\frac{n-1}{2}} P_0 \times Z_{n(2\nu)}$ (n = odd) or approximated: $T_{j(avg)n} = T_x + P_0 \times \left[Z_{t_p} - Z_T + \left(1 - \frac{t_p}{T}\right) \times Z_{(T+t_p)} + \frac{t_p}{T} \times R_{th} \right]$ (n = even)

7.4 Circuit operating conditions affecting the voltage applied across converter valve devices

A converter valve device may be exposed not only to the AC line voltage but also to repetitive and non-repetitive voltages superimposed on the theoretical voltage across the valve device.

Figure 18a and Figure 18b) show examples of the voltage waveforms applied across an uncontrolled and controlled converter valve device respectively, assuming a commutating number q = 3 and a pulse number p = 6.

The voltages U_{RWM} and U_{DWM} are the crest values of the circuit voltage applied across the converter valve device.

The voltages U_{RRM} and U_{DRM} are repetitive voltage peaks applied across the converter valve device due to the properties of the semiconductor valve devices used in conjunction with circuit parameters such as inductances, RC-networks, etc.

The voltages U_{RSM} and U_{DSM} are non-repetitive voltage peaks applied across the converter valve device and may originate from operating circuit-breakers, atmospheric disturbances etc. This kind of voltage may be minimized by the provision of surge suppression components.

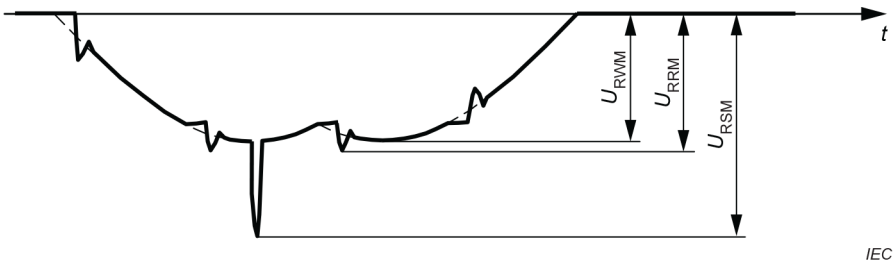


Figure 18a) Uncontrolled converter

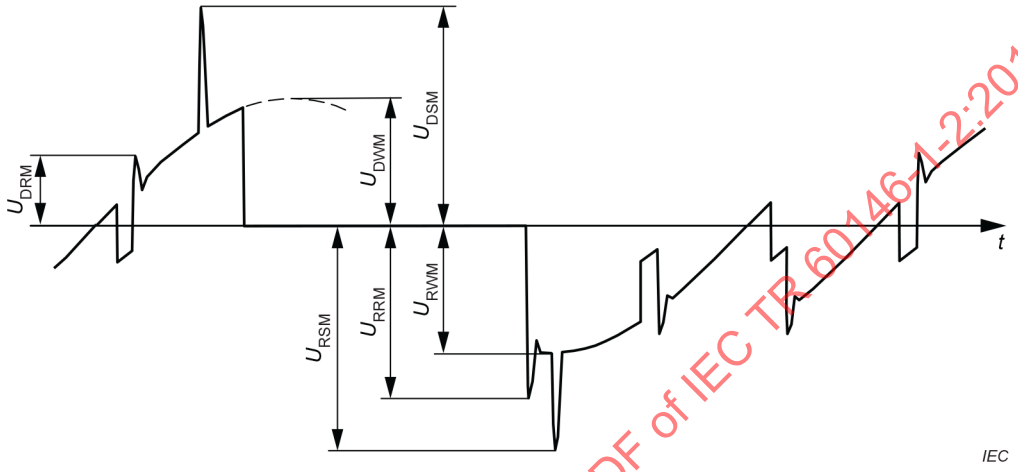


Figure 18b) Controlled converter

Figure 18 – Circuit operating conditions affecting the voltage applied across converter valve devices

In the design of converters, it shall be assured that the selected semiconductor valve devices have rated voltage values which exceed the protection level for each of the three kinds of voltages shown in Figure 18.

8 Converter operation

8.1 Stabilization

A converter may have an internally or externally closed loop control or other included means for stabilization of an output quantity (voltage, current, etc.).

If the converter has an internally closed loop control system, a reference value for this system is introduced into the converter electrically or mechanically or in any other way.

If the converter is a part of an external closed loop system, a control signal from this loop is introduced into the converter and the converter may be regarded as an amplifier forming a part of the total control system for which the equipment is designed.

8.2 Static properties

The static properties of the control system are those properties which are valid when the transients caused by sudden changes in set values or in quantities to be counter-acted have disappeared.

If the converter has internal stabilization means, its static properties should be specified for specified variations of all quantities (for example voltage on line side, AC system conditions,

character of load, etc.) which are to be counteracted. Such a specification should cover the setting range of the stabilized quantities for which the converter is designed.

If the converter is a part of an external closed loop system, the static properties should be given as the relation between the input signal and the output from the converter under stated conditions for those quantities (for example voltage on line side, AC system conditions, character of load, etc.) which may affect this relationship.

8.3 Dynamic properties of the control system

The dynamic properties of the control system could be given either as the response time to a step change or as the frequency response or in any other suitable way which may be agreed between supplier and purchaser.

The dynamic properties should be stated for changes in those quantities which mainly affect the output, especially for changes in set value or in control signal and for changes in load.

It is not necessary to state the dynamic properties of the control system for changes in those quantities which have only a minor influence on the output.

8.4 Mode of operation of single and double converters

8.4.1 Single converter connection

Because thyristors (reverse blocking triode thyristors) have an on state region only in one direction, it is impossible to reverse a current flow through a single thyristor converter. The direct voltage can, however, be reversed by phase control in uniform thyristor connections.

Figure 19 below shows the theoretical waveform of the direct voltage of a thyristor converter and the voltage over one arm of the thyristor connection during the transition from rectifier operation to inverter operation. The diagrams are based on a three phase bridge connection with a pulse number p = 6 and a commutation number q = 3. It is assumed that the direct current is constant and continuous over the entire operation range.

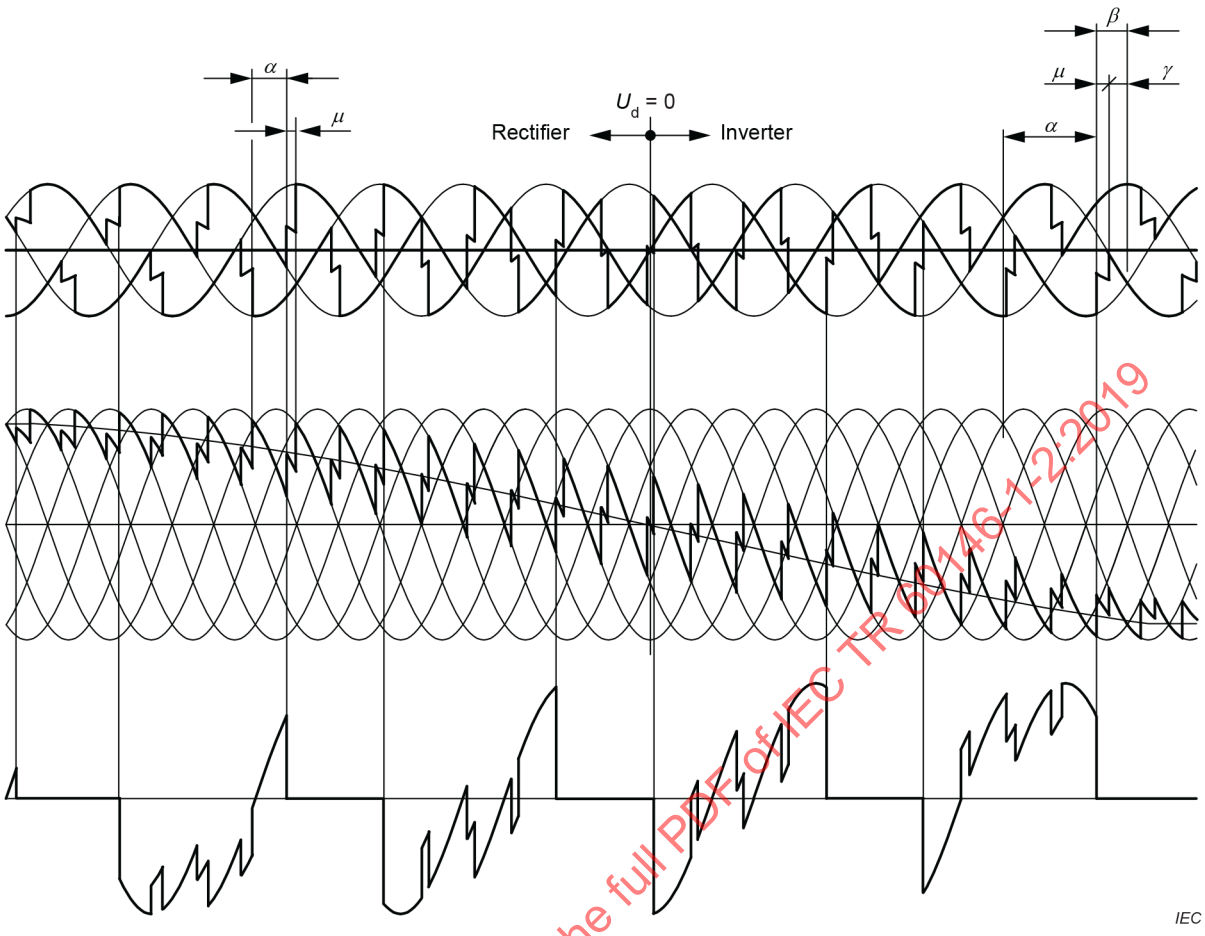


Figure 19 – Direct voltage waveform for various delay angles

The regulation curves, for example the mean value of the direct voltage as a function of the direct current, are shown in Figure 20. The curves are given for different trigger delay angles α between 0° and 150° and it is assumed that the reactance of the DC circuit is relatively small and that the converter has a back e.m.f. load.

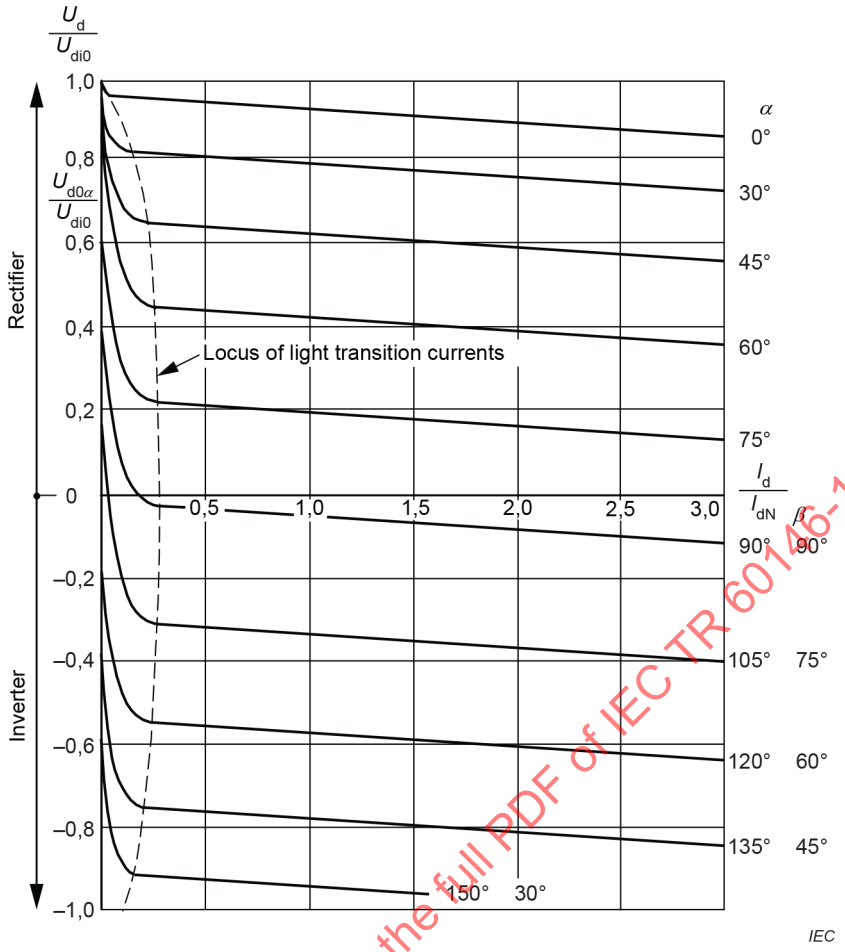


Figure 20 – Direct voltage for various loads and delay angles

When a thyristor converter is operating in the inverter range, it is necessary to limit the trigger delay angle to avoid conduction through (see 3.1.5). This is indicated in Figure 19 by the extinction angle γ which depends on the value of the trigger advance angle β and the angle of overlap μ and is determined by the relation:

$$\gamma = \beta - \mu$$

It is necessary to keep the extinction angle γ under all circumstances larger than the turn-off time of the thyristors. The necessary limitation of the trigger delay angle α or the trigger advance angle β may be calculated from the formula:

$$\cos\beta = \cos\gamma - 2 \times \frac{U_{dx}}{U_{di}}$$

where

U_{dx} is the total inductive direct voltage regulation.

8.4.2 Double converter connections and limits for rectifier and inverter operation

Theoretical regulation curves for a double converter connection for different control angles α_1 for one converter and α_2 for the other converter are shown in Figure 21. The curves are given for idealized conditions, assuming a high DC circuit inductance so that the transition current region can be neglected and the interaction between converters is also neglected.

The commutation limit lines indicated in Figure 21 give the highest admissible direct current in inverter operation, at which the critical value of the extinction angle γ is reached. If, for a given set of operating conditions (direct current, AC and DC voltages, etc.), the trigger delay angle α is increased beyond this limit, a conduction through will occur.

Although the working limit for a single converter in the rectifier operation region is given by the regulation curve for α = 0°, it may be necessary in a double converter connection to limit also the minimum value of the trigger delay angle to control direct current circulation.

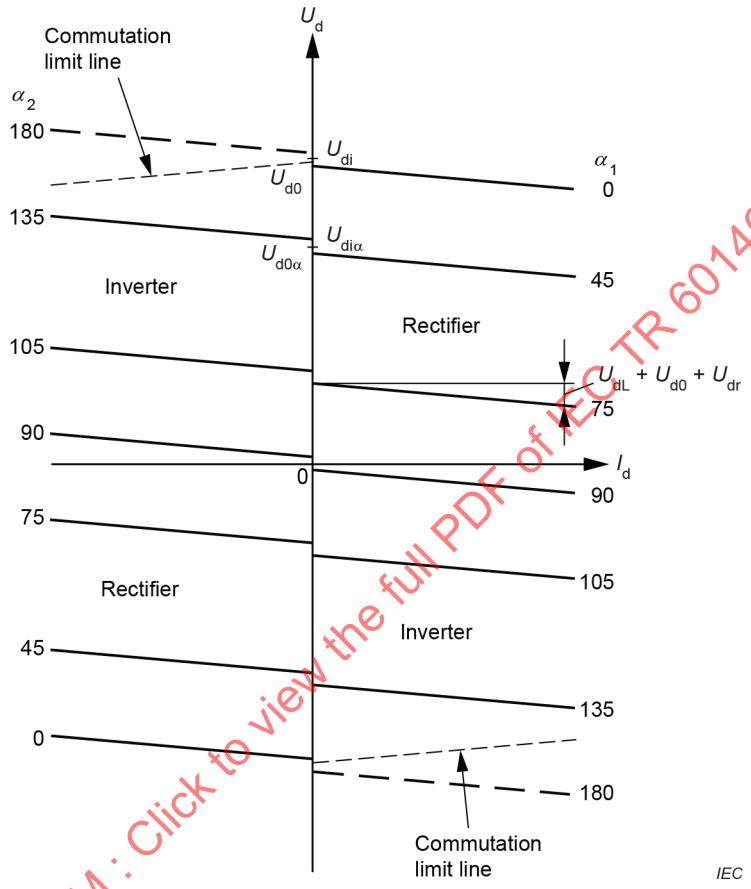


Figure 21 – Direct voltage limits in inverter operation

8.5 Transition current

When the direct current has decreased below the transition current value (IEC 60146-1-1:2009, 3.7.10), the voltage/current characteristics bend upwards. This is because the reactance of the DC circuit cannot maintain direct current over the entire period when the instantaneous value of the direct voltage is less than the counter e.m.f. voltage of the load. The direct current therefore becomes intermittent.

The waveforms of direct voltage and direct current under intermittent direct current conditions are shown in Figure 22. During those periods when the direct current is zero, the instantaneous value of the direct voltage is not given by the theoretical waveform as indicated by a dotted line in Figure 22, but by the counter e.m.f. voltage of the load. This means that the mean value of the direct voltage of the converter is higher than that obtained when the direct current is continuous.

The value of the transition current depends on the inductance of the DC circuit, the counter e.m.f. of the load and the value of the trigger delay angle α. It increases with decreasing DC circuit inductance, with increasing counter e.m.f. and with increasing trigger delay angle from 0° to 90° in the rectifier mode. It increases with decreasing DC circuit inductance, with

increasing e.m.f. of the load and with decreasing trigger delay angle in the inverter mode (see Figure 22).

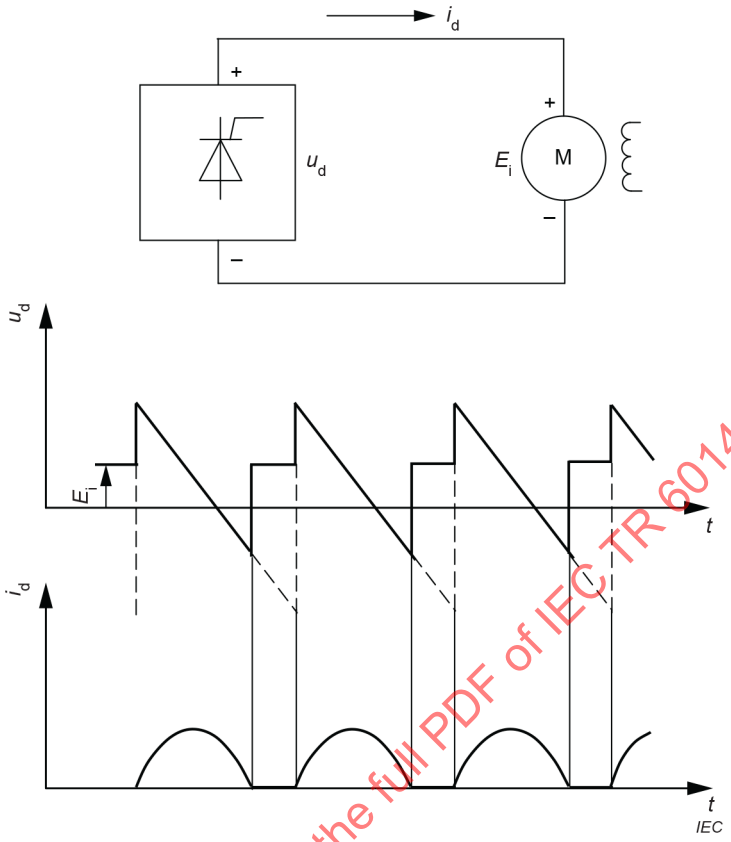


Figure 22 – Direct voltage at values below the transition current

8.6 Suppression of direct current circulation in double converter connections

8.6.1 General

In a double converter connection, it is necessary to take some precautions in order to limit direct current circulation. The most widely used methods are described in 8.6.2 to 8.6.4.

8.6.2 Limitation of delay angles

The trigger delay angles of the two converters are controlled so that the ideal direct voltage of the converter operating in the inverter mode is always higher than the direct voltage of the other converter operating in the rectifier mode. Because of the commutation limit line in the inverter mode as indicated in Figure 21, it is normally necessary to limit also the minimum value of the trigger delay angle to fulfil this requirement over the entire operation range.

8.6.3 Controlled circulating current

The trigger delay angles of both converters are controlled so that the circulating direct current is automatically controlled to a value appreciably smaller than rated direct current. The value of controlled circulating current can preferably be chosen slightly above the maximum transition current to avoid intermittent direct current.

8.6.4 Blocking of trigger pulses

A blocking signal inhibits all thyristor triggering pulses in one converter when the other is carrying current and vice versa. In that way, only one converter can operate at any time and no circulating direct current can occur between the two converters.

8.7 Principle of operation for reversible converters for control of DC motors

8.7.1 General

Figure 23 shows the sequence of operation of reversible converters serving a DC motor drive, for several types of circuits. The upper diagram shows motor speed plotted as a function of time. In the lower diagrams are indicated the operation of the converter as a rectifier and as an inverter. The operation of the basic converter circuits is also indicated in simplified form.

8.7.2 Motor field reversal

To brake the motor to standstill and then accelerate it in the reverse direction, the current is reduced to zero by phase control, the field current is reversed and the required braking current is adjusted by phase control for inverter operation. Subsequent transition from braking to acceleration in the reverse direction can be achieved smoothly by further continuous advance of phase control from inversion to rectification (see Figure 23a)).

8.7.3 Motor armature reversal by reversing switch

In this case, the sequence of operations is similar to that described in 8.7.2 except that the armature current is reversed by a reversing switch instead of reversing the field current (see Figure 23b)).

8.7.4 Double converter connection to motor armature

The motor armature is connected in parallel with two converters of opposite polarities. For each direction of the current in the motor armature, there is always a converter available to carry this current (see Figure 23c)).

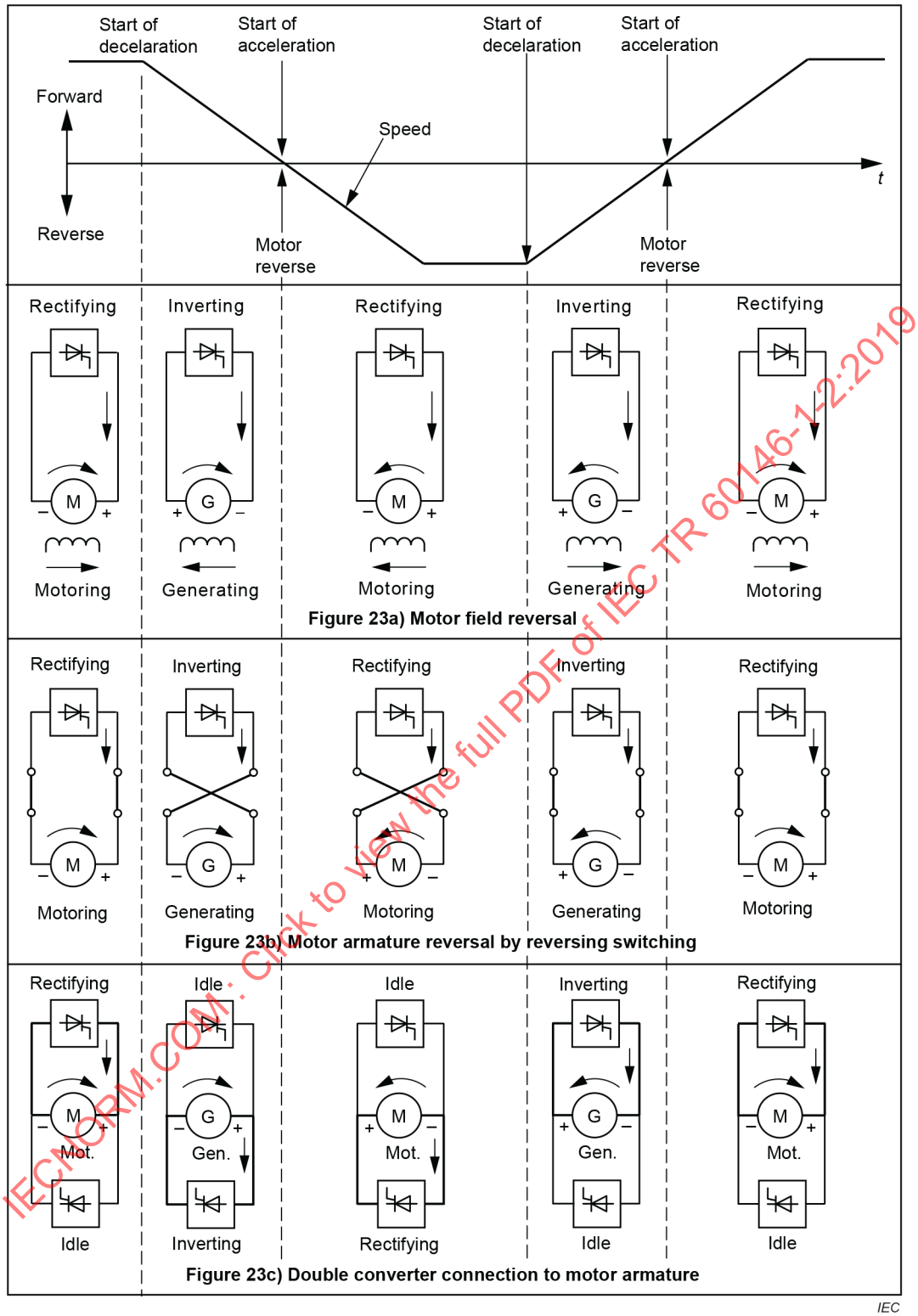


Figure 23 – Operating sequences of converters serving a reversible DC motor

9 Converter faults

9.1 General

Attention shall be paid to the instruction manual and any fault-finding charts provided by the supplier.