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PRE-STANDARD

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Device embedded substrate – Guidelines – Data format

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DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

FOREWORD

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IEC PAS 62878-2-5 was submitted by the JPCA (Japan Electronics Packaging and Circuits Association) and has been processed by IEC technical committee 91: Electronics assembly technology.

It is based on JPCA-EB02 (2011). It is published as a double-logo IEC / JPCA PAS.

The text of this PAS is based on the following document:	This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document
Draft PAS	Report on voting
91/1257/PAS	91/1264/RVD

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DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

1 Scope

This part of IEC 62878 defines the data format for active and passive devices embedded inside an organic board whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material. The basic structures, the terminology, reliability tests and a design guide are described in the "Standard of device embedded substrate", JPCA EB01, fourth edition.

A device embedded substrate contains device(s) in the board and is connected in a 3D way. Conventional 2D design technology using GERBER format cannot describe all the connection information in a device embedded substrate. We have several proposals to express 3D data formats but they cannot describe the structures given in EB01. The JPCA Committee for standardization of device embedded substrates has studied various formats and developed a format, FUJIKO V-1.0, which can express substrate design data in CAM data used in actual production. This Publicly Available Specification (PAS) described the FUJIKO data format.

Figure 1.1 shows the design flow of a device embedded substrate. The design data can be directly sent to a board manufacturing system using the FUJIKO format, or can be converted to CAM data and then be used in production. The data contain 3D information of coordinates and shapes of devices used. It is possible to check the status of device embedding in a board, and also make it a common knowledge in production know-how of a production line.

This PAS describes the expression of 3D data information, the concept of layers, the structure of board data, and definitions of information repeatedly used in design.
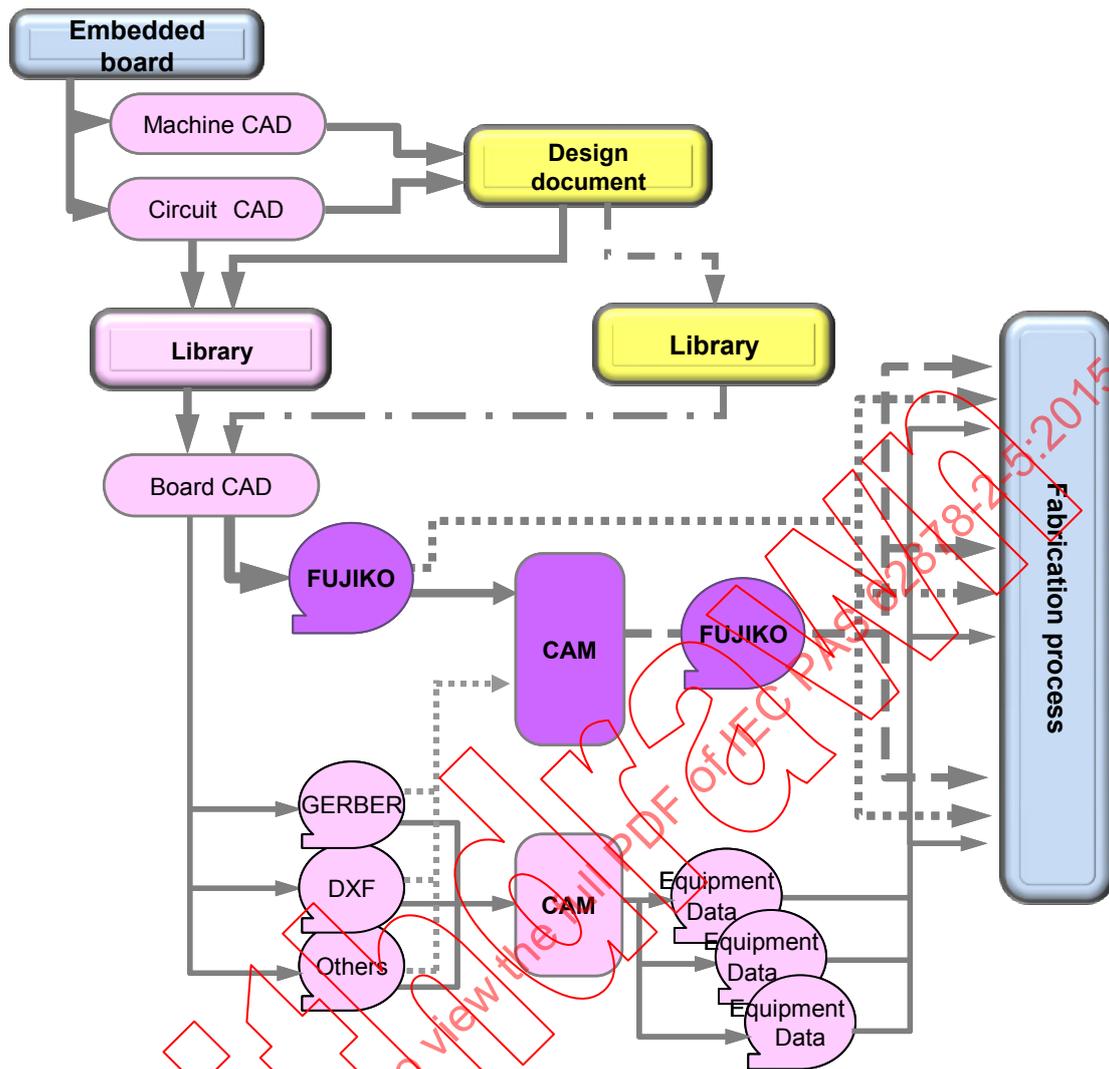
Figure 1.1 – Flow chart of design of device embedded substrate

1.1 Purpose

This file format describes the detailed 3D information of the following electronic circuit boards including device embedded substrate and SiP (system in package), and makes it possible to use necessary information from the stage of design to fabrication of products.

1.2 Applicable range

1.2.1 Product

It is possible to maintain the following design information of device embedded substrate as shown in Figure 1.2.

1) Information of inside device embedded substrate and surface mounting.

2) Assembly information of SiP (System in Package).
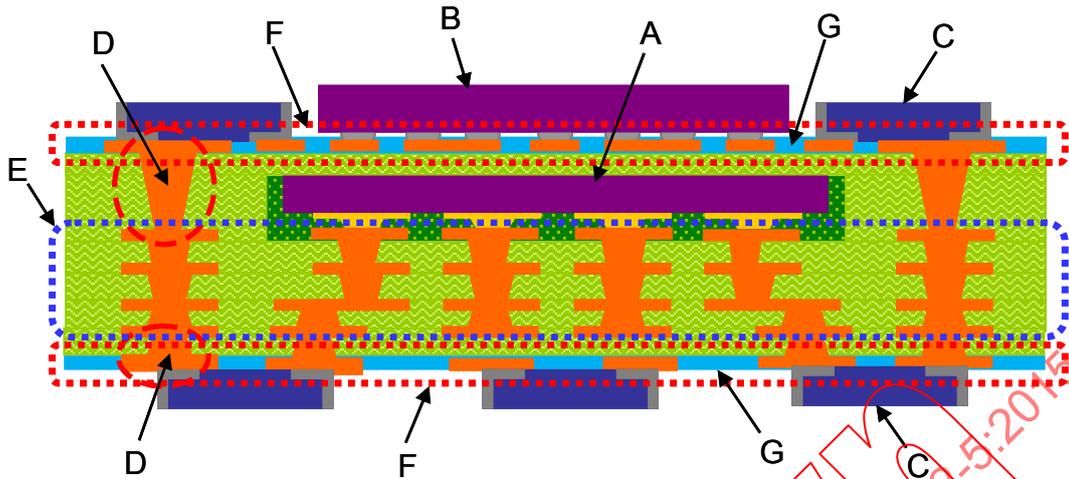
A	Embedded active device	E	Inner pattern
B	Surface mounted active device	F	Surface pattern
C	Surface mounted passive device	G	Solder resist
D	Layer connecting via		
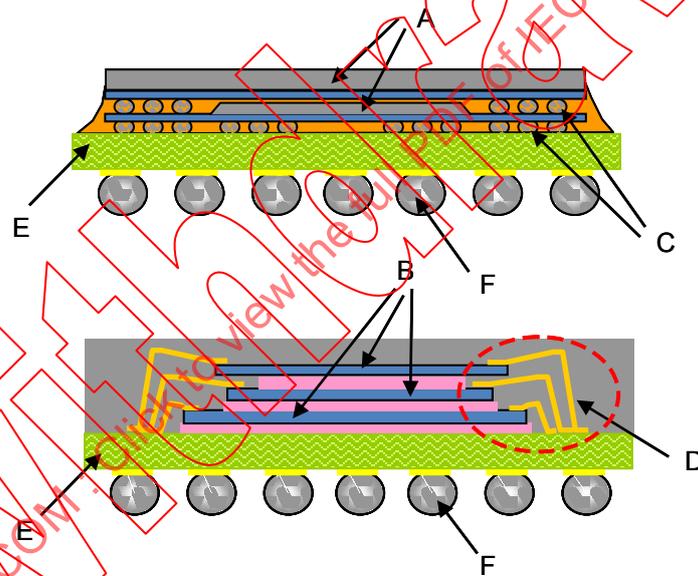
A	CSP	D	Wire bonding
B	Bare die semiconductor device	E	Interposer
C	Solder ball	F	Solder ball

Figure 1.2 – General concept of product

1.2.2 Process

The format describes maintained and available information of each stage in production as described in Figure 1.1

1) Design

2) Simulation

3) Substrate fabrication

4) Device embedding

5) Test.

Table 1.1 – Information required in production

Process	Holding data of	Data available for
Design	Circuit Components Shape of the board Board structure Design/Production rule (for check)	Limited condition Net list
Simulation	Circuit Characteristics of components Board properties (materials) Board structure Art work	Electrical properties Thermal properties Mechanical properties Electronic properties Additional information in production
Substrate fabrication	Art work Drilling Symbol marks Panel format	Equipment Additional information in production
Device embedding	Component shape Embedding position Interconnection terminals Symbol marks	Equipment Relative positions of component Component list
Test	Art work Component shape Component position Terminal information Marks	Electrical test equipment Video image inspection

1.3   Features

Data format has the following characteristics:

1) can contain the structure of the device embedding substrate specified inEB01;

2) can contain information of SiP in general (chip stack, PoP TSV, wire bonding, flip-chip, interposer, etc.);

3) design data of terminal positions of embedding device in a virtual layer specified in EB01;

4) information of internal structure of devices such as SiP which cannot be described as a structure of a device embedded substrate and of a terminal structure as 3D design data;

5) seamless keeping of design data of devices having different level such as SiP and of embedding substrate.

1.3.1   Maintenance of the device embedded substrate structure

It is possible to keep and illustrate the 3D structure of device embedded substrate as shown in Figure 1.3. It is also possible to check its 3D structure.
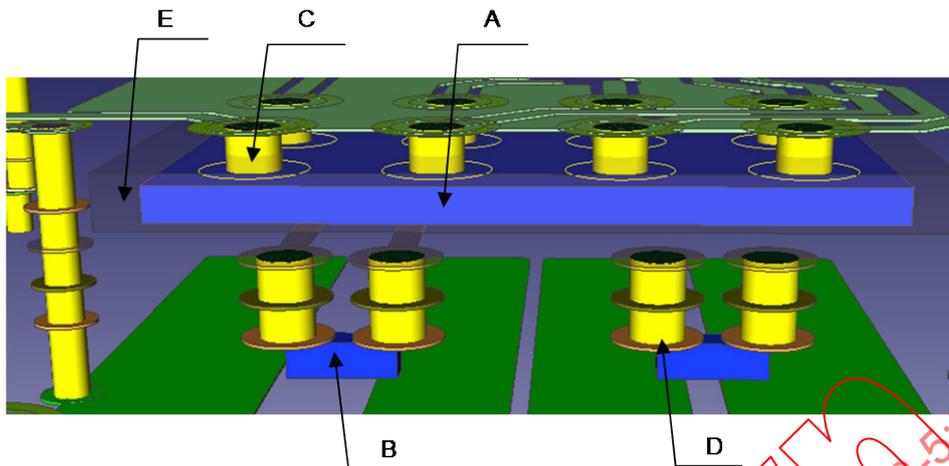
| A	Embedded active device	D	Pad connection
B	Embedded passive device	E	Space without board material
C	Via connection		

Figure 1.3 – Example of a structure of a device embedded substrate

1.3.2   Maintenance of SiP interposer structure

It is possible to keep and illustrate the 3D structure of SiP substrate as shown in Figure 1.4. It is also possible to check structures of flip-chip and wire bonding mounting.
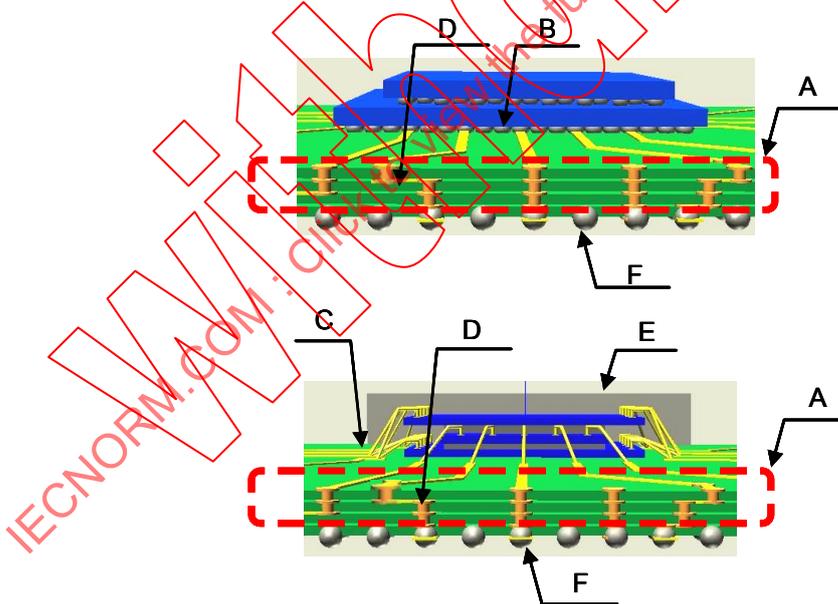
A	Interposer	D	Interposer
B	Flip-chip connection	E	Package
C	Wire bonding connection	F	Solder ball

Figure 1.4 – Examples of a structure of a SiP interposer

1.3.3   Maintenance of design data with a virtual layer of terminal positions of embedded device(s)

It is possible to keep the design data defined in EB01 of the terminal position of a via connection not on a conductor layer, but as in a virtual layer. It can be maintained in the structure shown in Figure 1.5.
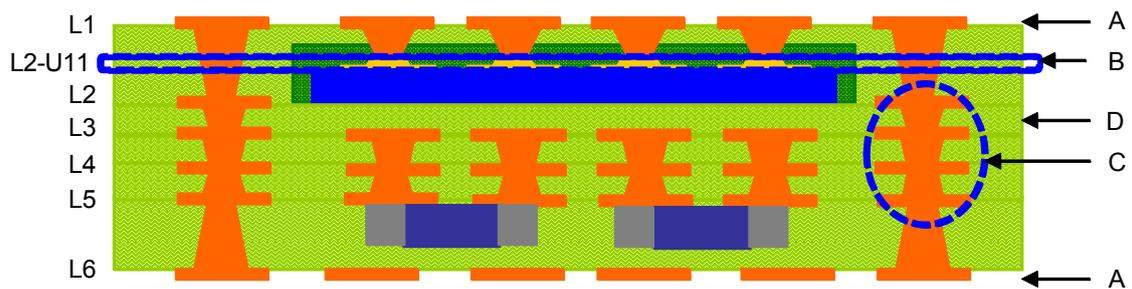
A	Surface conductor layer	C	Inner conductor
B	Virtual layer (connection position)	D	Insulation layer

Figure 1.5 – Example of a laying terminal position of an embedded device in a virtual layer

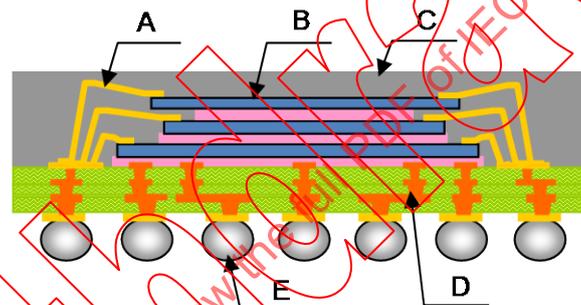### 1.3.4   Maintenance of terminal structure and embedded device structure including SiP

It is possible to keep the design data of the terminal position of such as SiP as shown in Figure 1.6.
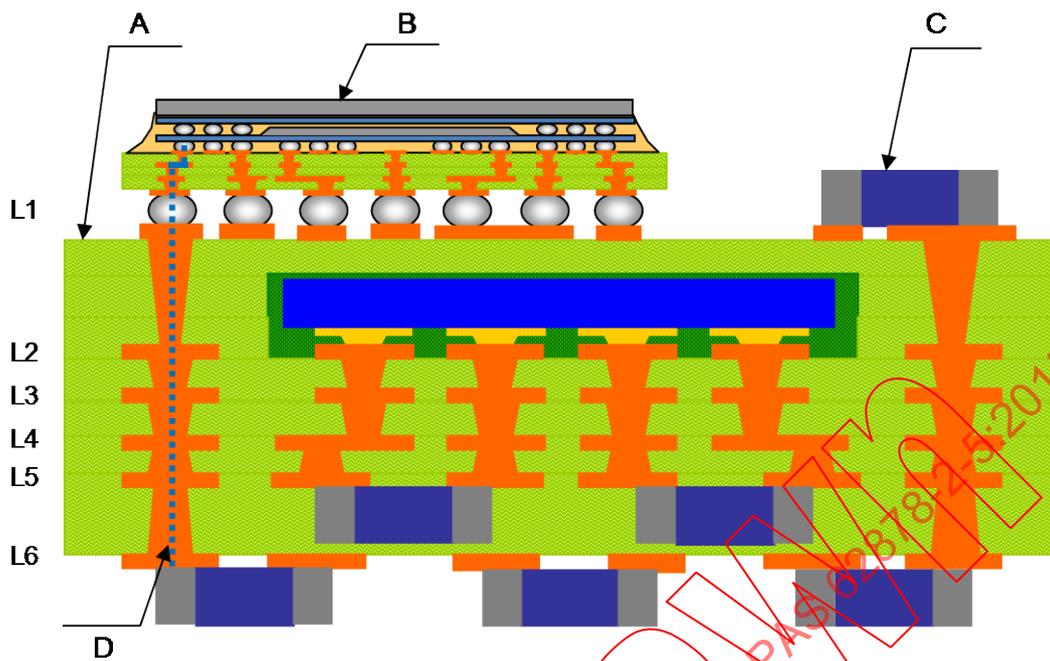

A	Bonding wire	D	Interposer
B	Chip stack	E	Solder ball
C	Package shape		

Figure 1.6 – Example of showing structures of device embedding and terminals

1.3.5   Seamless ownership of design data

It is possible to keep the design data of SiP and the device embedding substrate being made on different layers as shown in Figure 1.7.

| A | Substrate (Printed wiring board) | C | Surface mounted passive device |
| B | SiP | D | The same net |

Figure 1.7 – Example of showing structures of SiP and of a device embedding substrate

2   File description

2.1   File description summary

2.1.1   Types of data and their structure

1) Types of data

There are three types of data of substrate, definition and user defined data. Details of these data are shown in Table 2.1.

Table 2.1 – List of data

Type		Details	
Type name	**Content**	**Name**	**Content**
Board data	Basic structure elements of board data	Board information	Total data of board including embedding devices
		Layer map information	Layer combination information ofembedding devices and layers
		Device arrangement information	Position of devices and embedding layers
		Basic figure information	Available figure elements in board data There are ten (10) types of figures 1 Point 2 Area 3 Line 4 Text 5 Bonding wire 6 Semi-sphere 7 Rectangular prismoid 8 Via 9 Device 10 Group
		Net information	Device pin construction and wiring patterns
		Artwork information	Figure pattern other than wiring pattern
		Package information	Package figure information
		External terminal information	Figures and names of external terminals
		Internal terminal information	Figures and names of internal terminals
		User expandable information	Arbitrarily expandable data of the format user "Definition" = "Value" can be arbitrarily defined
Definition data	Definition of information which can be repeatedly used. It may be referred to from board data.	Layer definition	Shapes of layer construction, conductor layer(s) and insulation layer(s) – including scooped partsuch as a cavity
		Land definition	Shape of land (pad)
		Via definition	Diameter of via (pad stack) and landshape in each layer
		Device definition	Pin and package shape of embedding device
		Basic pattern information	Usable pattern elements in the defined data Types of figures are the same as in board data
		User expandable information	Arbitrarily expandable data of the format user "Definition" = "Value" can be arbitrarily defined

2)   Data structure

The data structure of FUJIKO is based on the board data shown in Figure 2.1. Repeatedly used data information is formalized and is possible to identify definition data. The data expandable by users can be added to the board data and definition data.
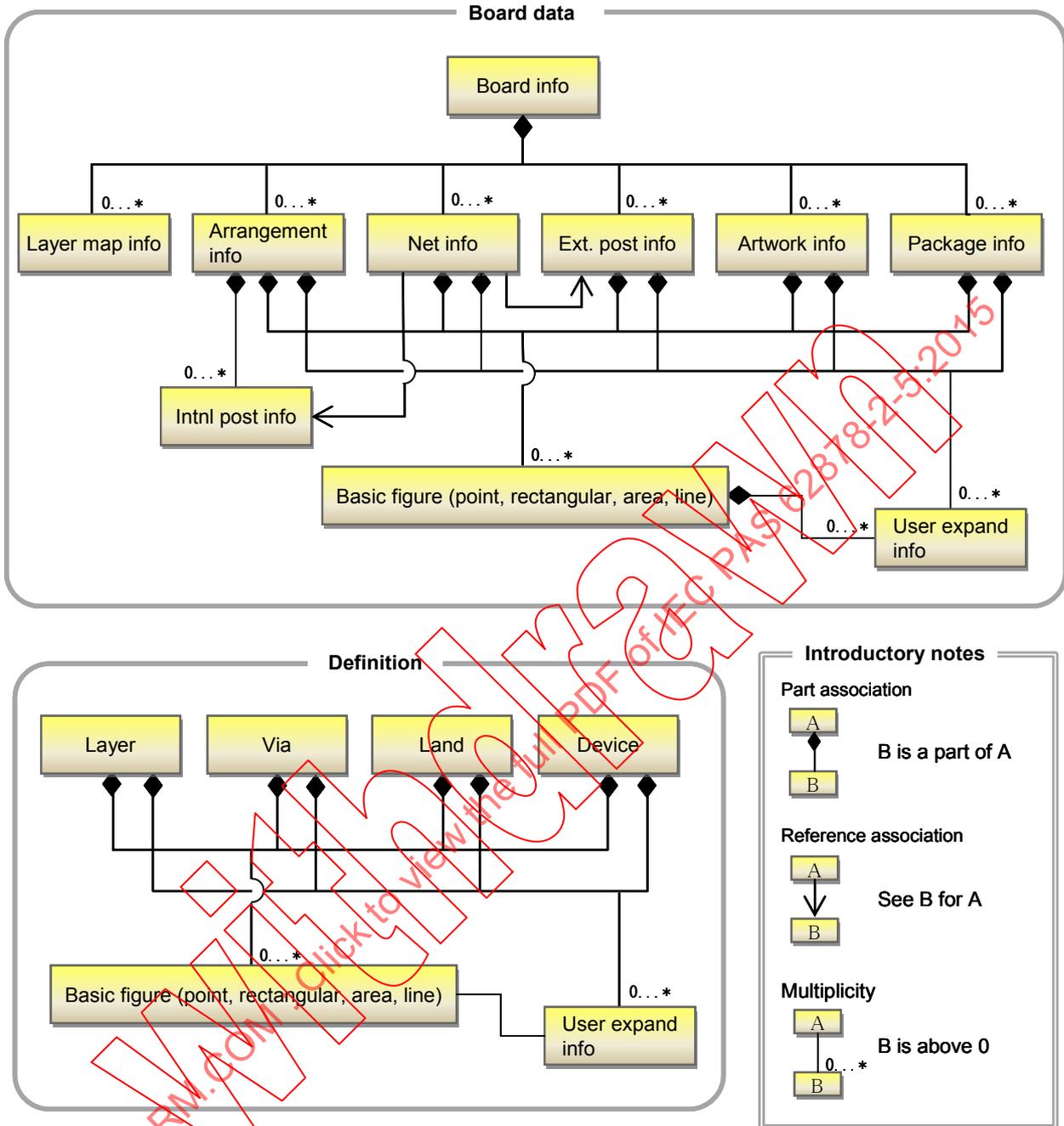
Figure 2.1 – Data structure

2.1.2 File structure

File structure is either of the following two methods.

1) Each definition data and board data are stored in one file as shown Figure 2.2 (recommended).

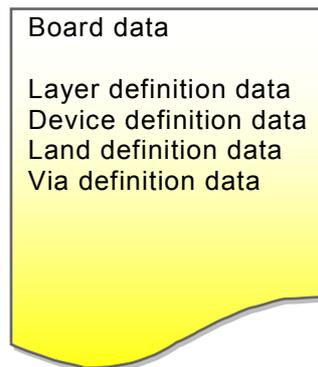2) Definition data are stored in a separate file as shown in Figure 2.3.

Board data

Layer definition data
Device definition data
Land definition data
Via definition data

Figure 2.2 – One file structure (recommended)

Board data

Layer definition data

Land definition data

Via definition data

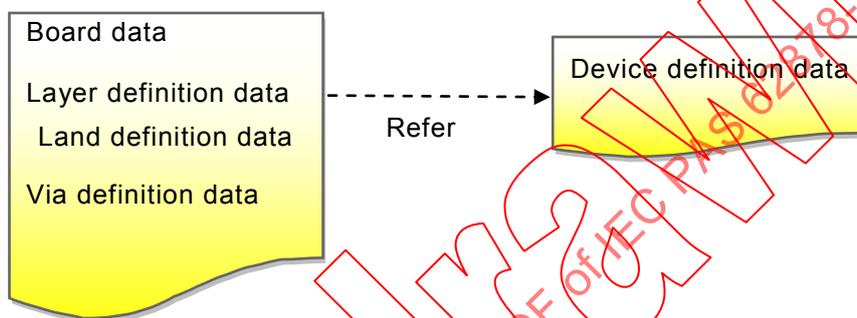Device definition data

Refer

Figure 2.3 – Two-File structure

2.2   3D expression

FUJIKO format is expressed in 3D coordinates. 3D coordinate expression is a space expressed by three diagonal axes, X, Y and Z.

2.2.1   Coordinates

The coordinates of this format are shown in Figure 2.4 and have the following definitions.

1) Rotation of an axis is anti-clockwise.

2) Selection of unit length may be selected from mm, μm and nm.

3) Directions of axes are horizontal direction for x-axis, side direction for y-axis and vertical (height/thickness) direction for z-axis.
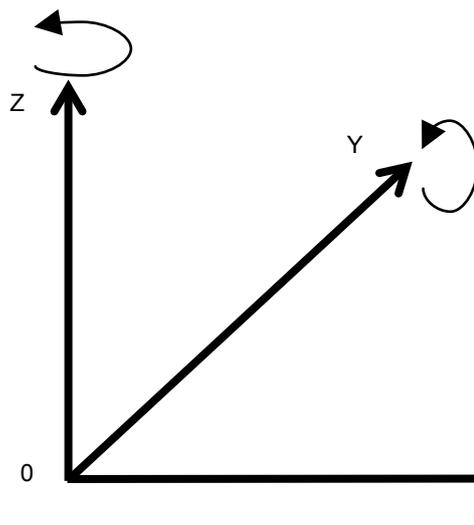
Figure 2.4 – Definition of coordinates

2.2.2   Position description

Specification of a 3D position is available as shown in Figure 2.5 to indicate layer structure and 3D coordination. Directions of axes can be expressed in horizontal direction for x-axis, side direction for y-axis and height direction for z-axis.
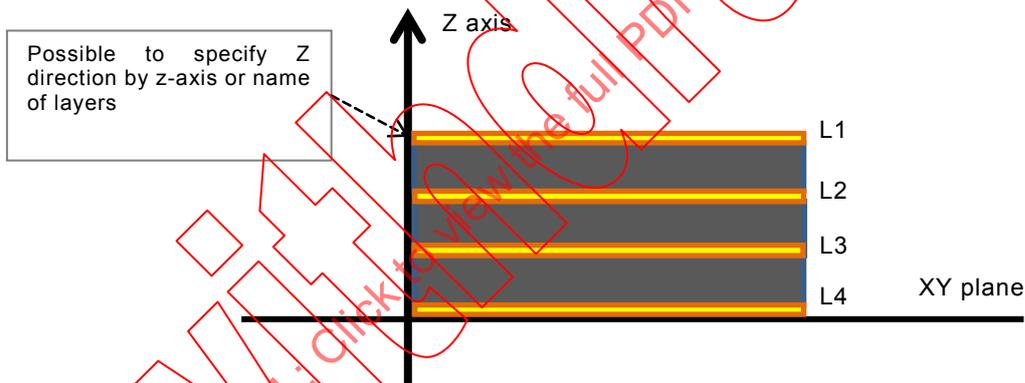
Figure 2.5 – Position definition

2.2.3   Relation between coordinate origin and board position

There is no specified relation between coordinates origin [(x, y, x) = (0, 0, 0)] and the board position as shown in Figure 2.6.
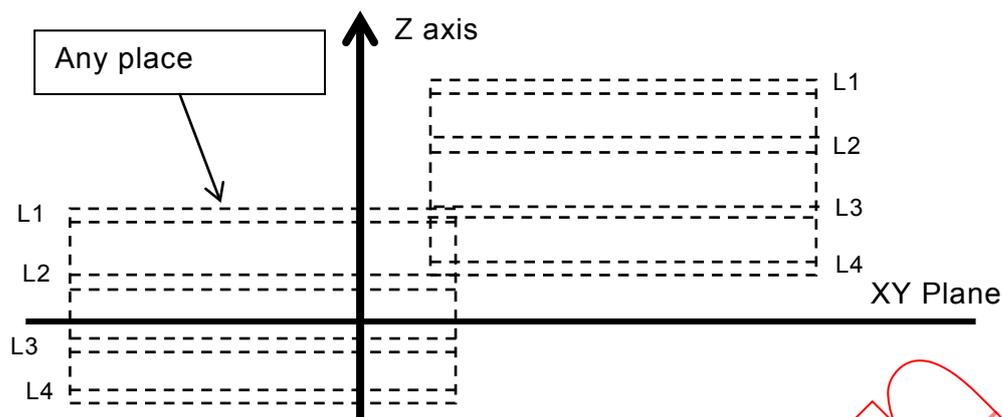
Figure 2.6 – Relation between coordinates and board position

2.3 Layer concept

There are two types of layers, conductor layer and virtual layer as illustrated in Figure 2.7. Characteristics of layers are explained below. The conductor layer is the layer coinciding with the terminals of an embedding component and a conducting layer. The conductor layer with internal posts that can be connected to the embedded device is the embedding layer. This concept is not applicable to embedding of a device which is not connected to a conductor layer, such as vias. A virtual layer is considered as a virtual conductor layer at interconnection points of an embedding component. This format can maintain coordinate data and design data in both of layer base and the 3D Z axis base design. It is recommended, however, that the data maintenance in the layer base in the case board structure is described within the description made in EB01. Use of 3D Z coordinate base can be used for describing design data such as for SiP which may not be an appropriate use of the above structure. The 3D Z coordinate base may not be appropriate to describe information necessary in the production process. Additional information transfer other than defined the present format data may be necessary between processes (among designs and design to production) and efficiency may be lowered in design and production.
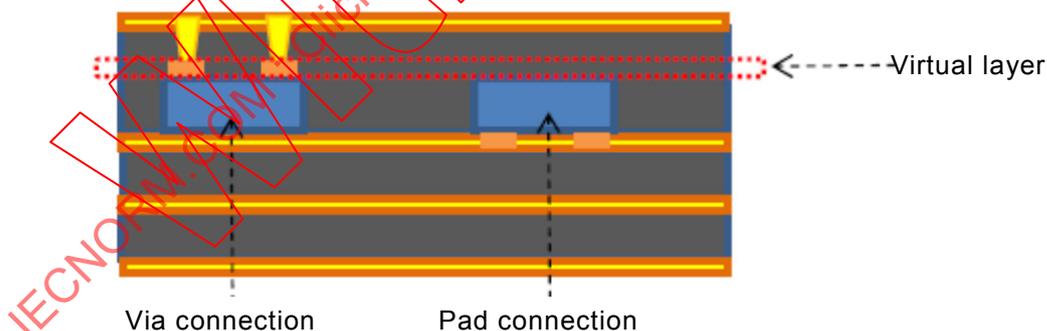

Figure 2.7 – Layer concept

2.4 Substrate data

Board data are to keep information of the basic elements of a device embedding substrate. There are the following nine types of information. Each type of the information is illustrated in the board data of Figure 2.1. Package information is held in case there is no internal connection information of embedded components.

1) Layer map information

2) Device arrangement information

3) Basic forms

4) Net information

5) Artwork information

6) Package information

7) External port information

8) Inside port information

9) User data expansion information

2.4.1   Layer map information

This information maintains the relation between inner and outer layers as devices are mounted and embedded, as shown in Figure 2.8 and Figure 2.9.

1) Information of mounting layers

The information shows connections in each mounting layer and mounting direction.
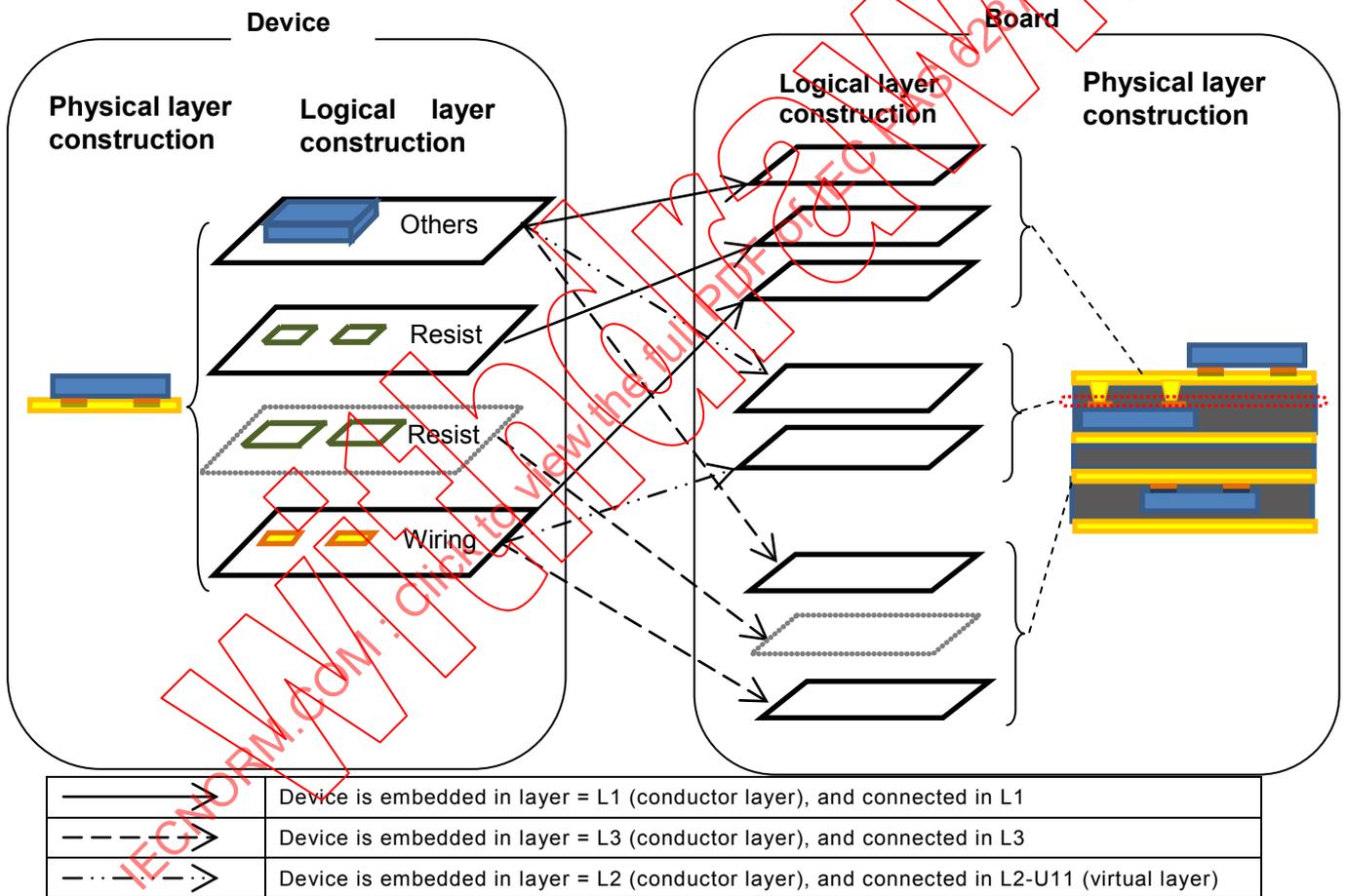
Figure 2.8 – Construction of mounting layers

2) Omission of mounting layers

Logic layers for embedding devices and for boards are combined in case the layer map information is omitted. It is possible only in the case where there is only one logic layer of the same type in one physical layer.
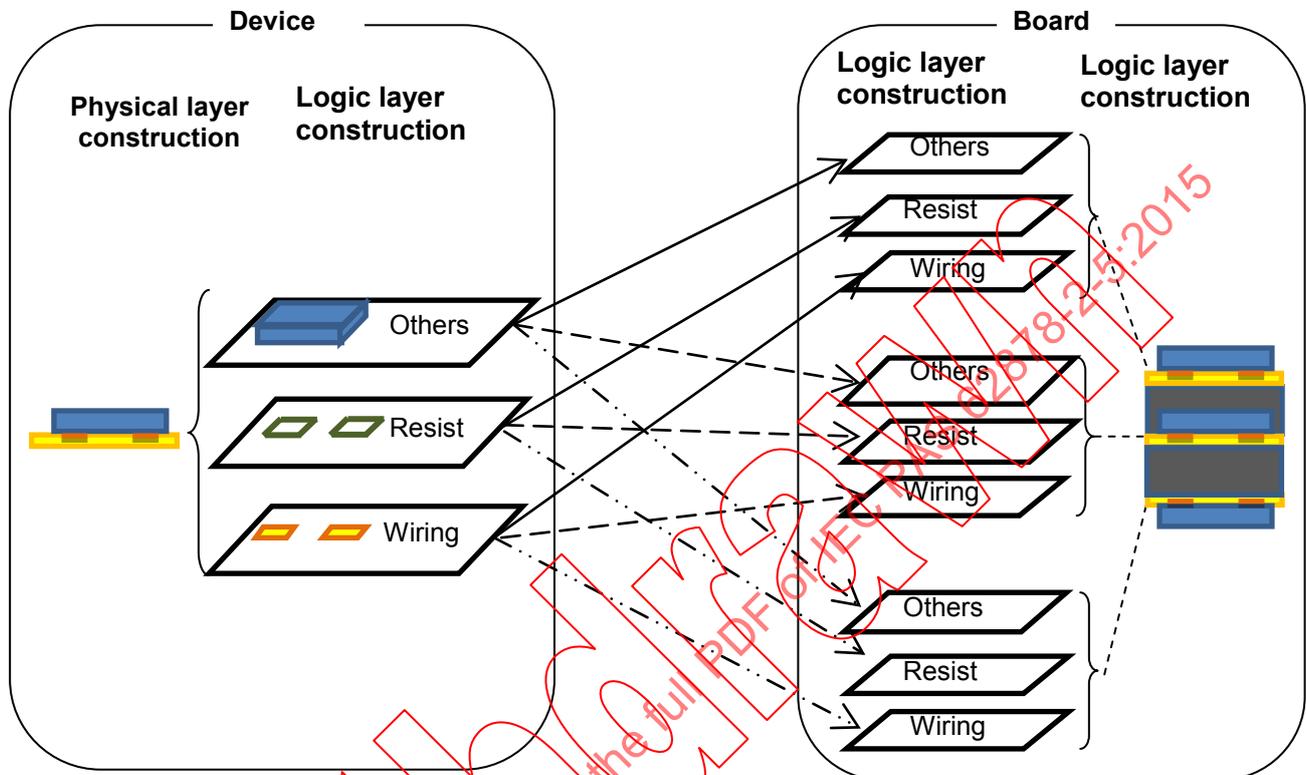

Figure 2.9 – Construction in the case of omission of mounting layers

2.4.2   Device arrangement information

The information has the position, figure and attribute of a device on a board. The external posts of a device become automatically internal posts (terminals) of a board.

1) Device attributes

   Name of a device on a board is the reference name of the device.

2) Device position attributes

   It is possible to specify the position in the following two ways (layer base design/3D coordinate design)

   a) XY coordinates/Z axis rotation/embedding layer/embedding direction/off-set/Connection terminal position in layer

   b) XYZ coordinates/XYZ axes rotation

3) Figure attributes

   Specified name of a device

2.4.2.1   Attribute of device position and arrangement

1) Layer definition

There are two ways of describing the vertical position of an embedded device for layer and Z axis. Details are shown in Figure 2.10 and Figure 2.11.
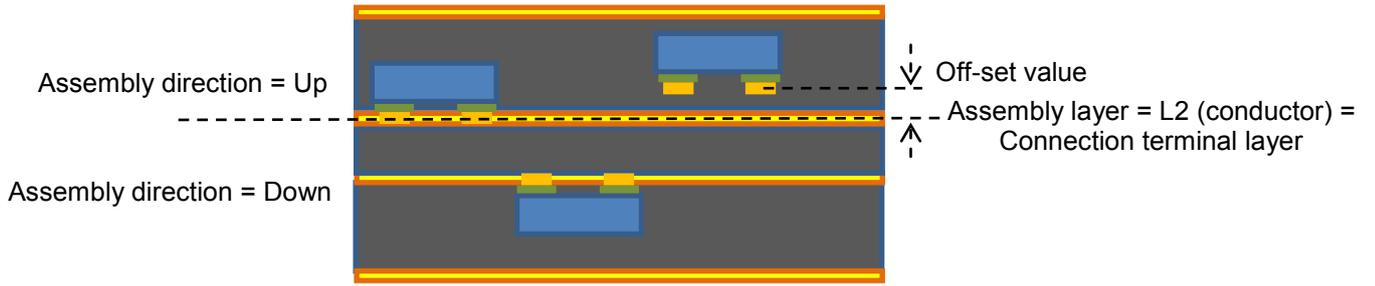
a) Pad connection

Assembly direction = Up

Off-set value

Assembly layer = L2 (conductor) =
Connection terminal layer

Assembly direction = Down

Figure 2.10 – Layer definition in pad connection

b) Via connection

Connection terminal layer =
L2-U11 (virtual layer)

Assembly layer = L2 =
(conductor layer)
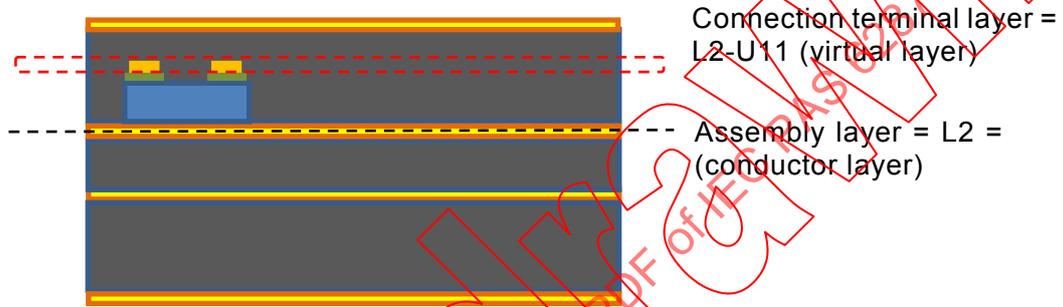
Figure 2.11 – Layer definition in via connection

2) Z coordinate definition

It is possible to use XYZ coordinates and XYZ axes rotation as the position specifying parameters.
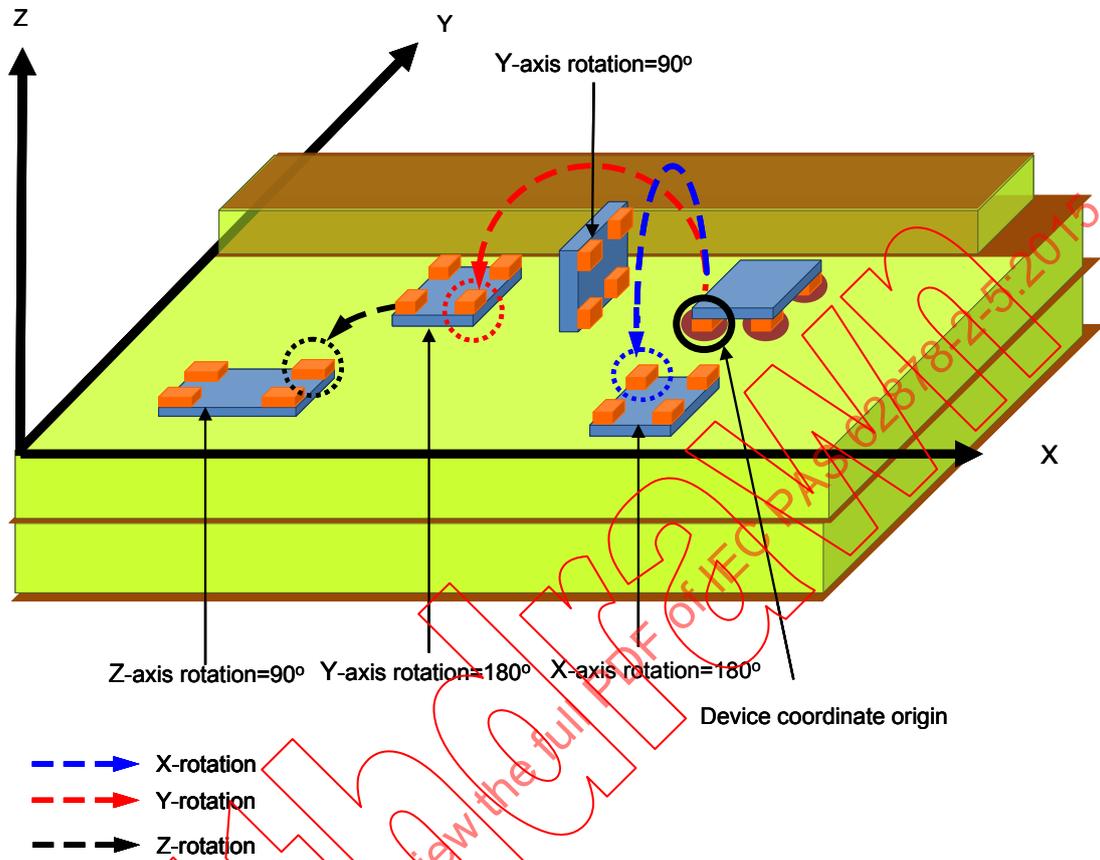

Figure 2.12 – XYZ axes rotation direction
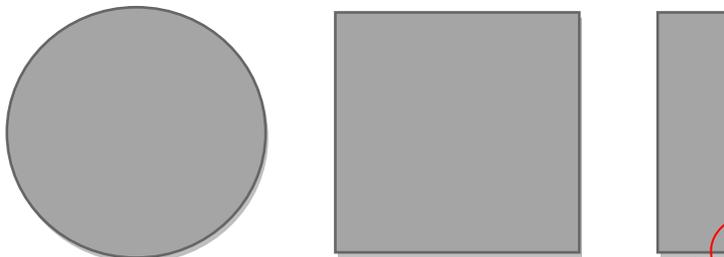
2.4.3   Basic figures

Figures of the following ten (10) types are available as figures in a board.

1) Point
2) Area
3) Line
4) Text
5) Bonding wire
6) Semi-sphere
7) Rectangular prismoid
8) Via
9) Device
10) Group

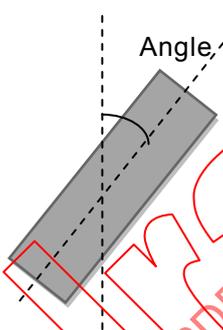**2.4.3.1   Point**

It is possible to specify round, angle and rectangular shapes as shown in Figure 2.13.

1) Shapes of round, square and rectangular
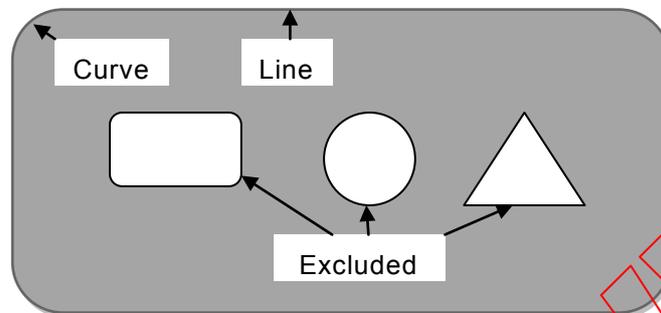
2) Rotation angle

Angle

3) Thickness

Figure 2.13 – Point

2.4.3.2   Area

Area can be specified as indicated in Figure 2.14.

1) It is a closed shape with many components and can specify line/curve as composing elements and excluded parts
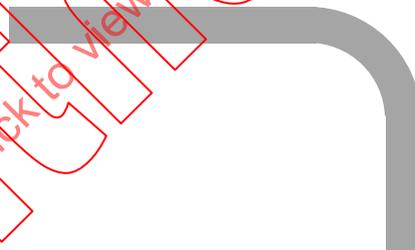

2) Thickness

Figure 2.14 – Area shapes

2.4.3.3   Line
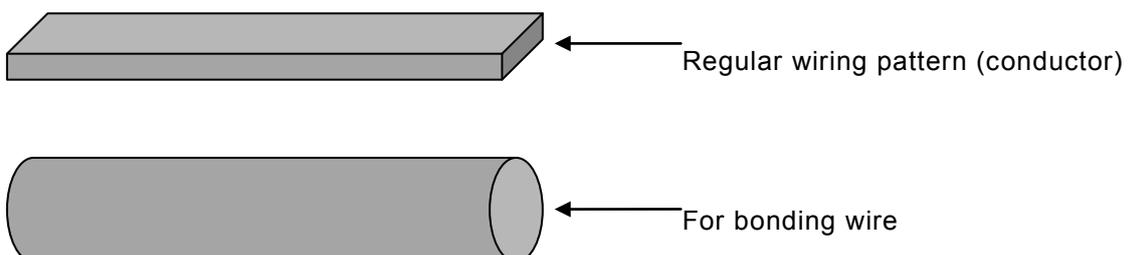
Line can be specified as indicated in Figure 2.15.

1) Can specify a continuous line having line and curve as composing g elements.

2) Can specify an extruded shape (round/angle).

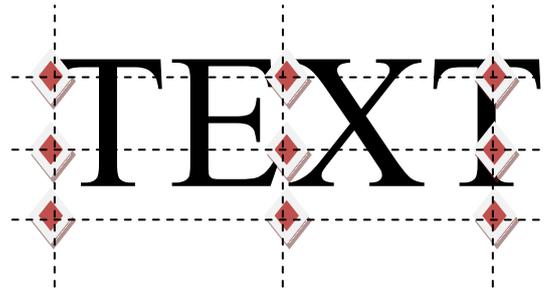3) Can specify types of cross sections (round or rectangular shape) and thickness

Regular wiring pattern (conductor)
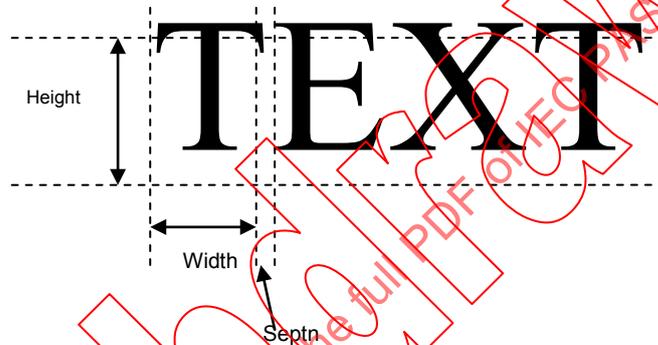
For bonding wire

Figure 2.15 – Area shapes

2.4.3.4   Text

Text is able to specify as indicated in Figure 2.16 with the origin of a letter, its height, with and separation and inclination.

1) Original points of letters

2) Letter height/width/separation

Height

Width

Septn

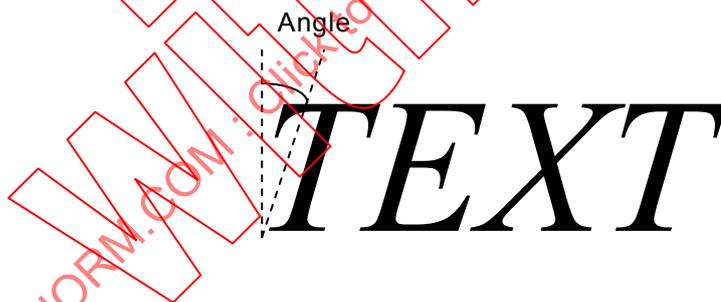3) Letter angle

Angle

TEXT

Figure 2.16 – Letter data

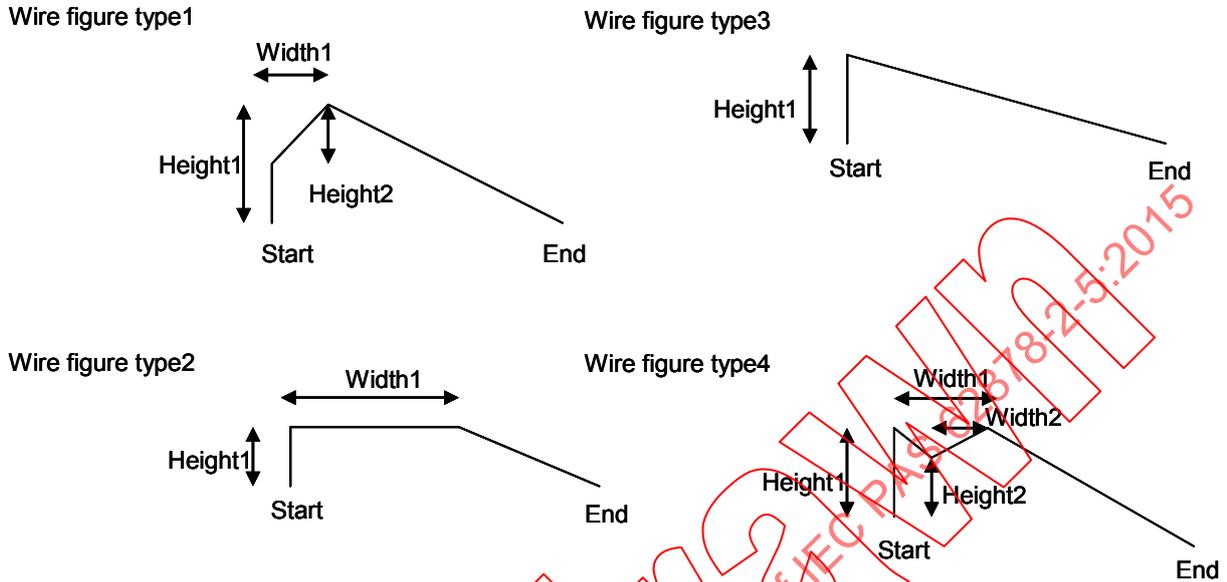4) Possible to maintain expanded patterns of vector font of text

Keep basic pattern "line" data

Figure 2.17 – Text shape

2.4.3.5   Bonding wire

Bonding wire is able to specify as indicated in Figure 2.18 for figure types 1 to 4.

Wire figure type1

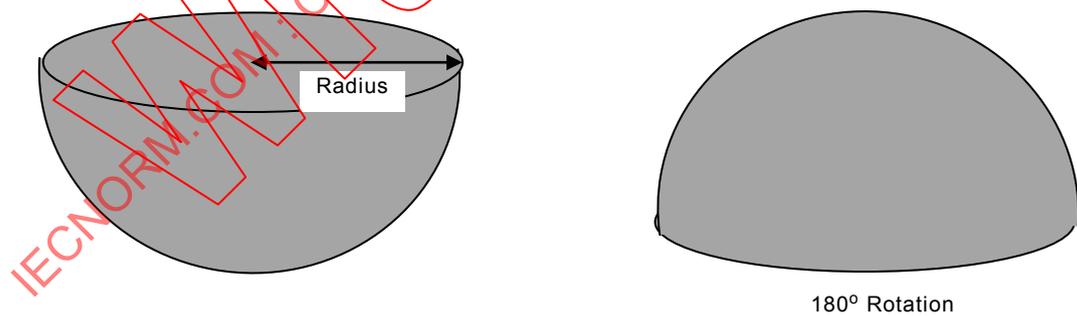Wire figure type3

Wire figure type2

Wire figure type4

Figure 2.18 – Bonding wire information

2.4.3.6   Semi-sphere

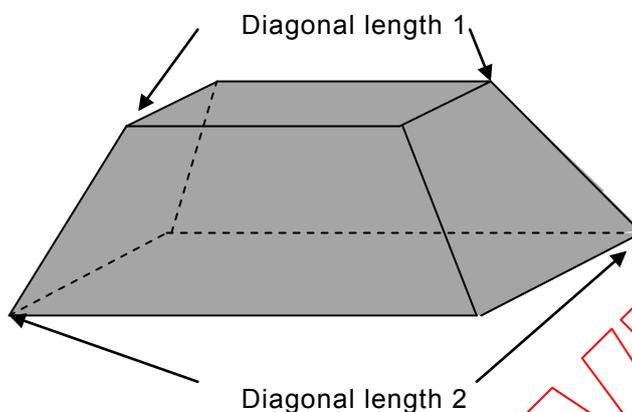Half ball is able to specify as indicated in Figure 2.19.

1) Radius
2) Rotation angle

Radius

180º Rotation

Figure 2.19 – Wire bonding shape

2.4.3.7 Rectangular prismoid

Rectangular cone is able to specify as indicated in Figure 2.20.

Diagonal length 1

Diagonal length 2

Figure 2.20 – Rectangular prismoid

2.4.3.8 Via

It is possible to specify the following three types of via as shown in Figure 2.21

1) Can specify via definition and refer to hole information and land information.
2) Can specify attributes of connection and un-connection for each layer.
3) Can specify grid positions of device mounting for numbers and separation of devices.

Figure 2.21 – Examples of via specification
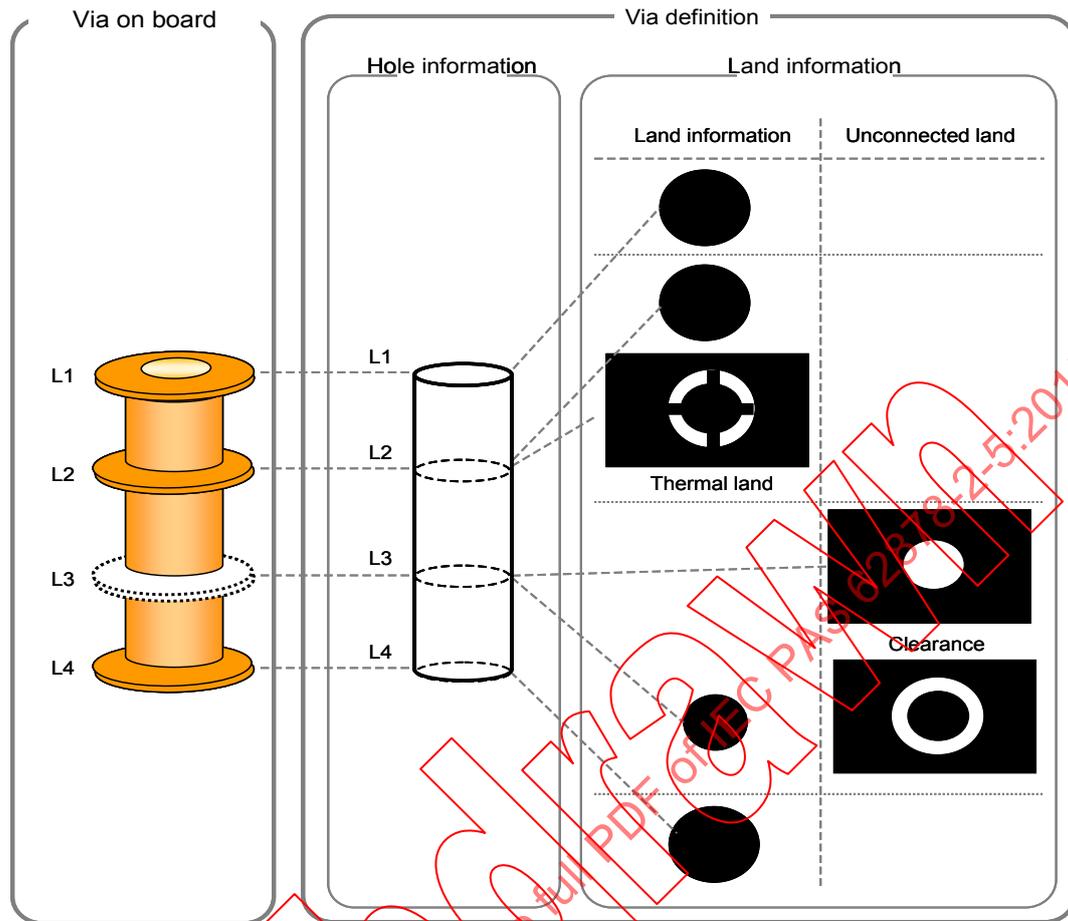
2.4.3.9 Device

It is possible to specify the following three types. Figure 2.22 shows examples.

1) Can specify names of device structure as attribute of the device.
2) Device figures can be arranged on a board as specified by device structure.
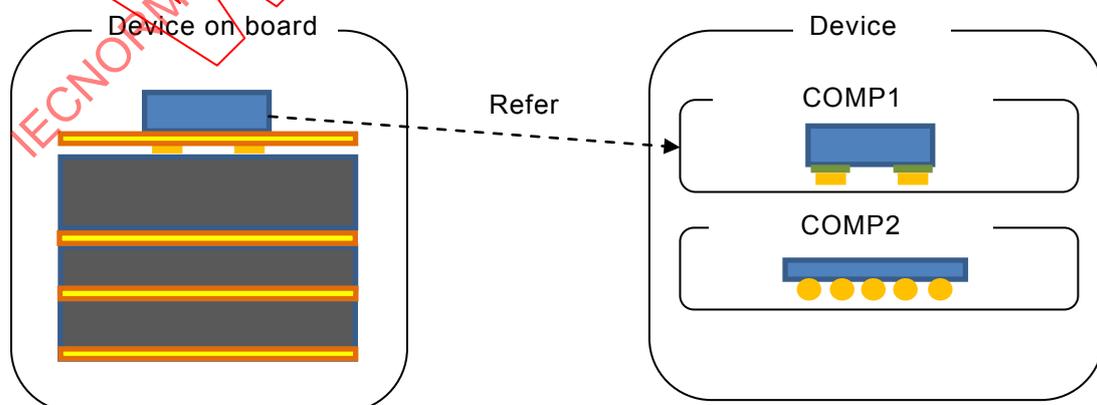3) Can specify grid positions of device mounting for numbers and separation of devices..

Figure 2.22 – Device definition

2.4.3.10   Group

Group is a combination of basic figures such as dimension lines as shown in Figure 2.23. It can be handled as one figure.

10.0

⌀ 5.0

Figure 2.23 – Example of group such as dimension lines

2.4.4   Net information

The net information maintains the connection terminal and wiring pattern information shown in Figure 2.24. Connection terminal information is the information giving interconnection between internal pads of a device or the connection of internal pads and external pads.

1) Connection pad information
   a) Names of internal pads
   b) Names of external pads
2) Wiring figures
   a) Point
   b) Area
   c) Line
   d) Bonding wire
   e) Semi-sphere
   f) Via
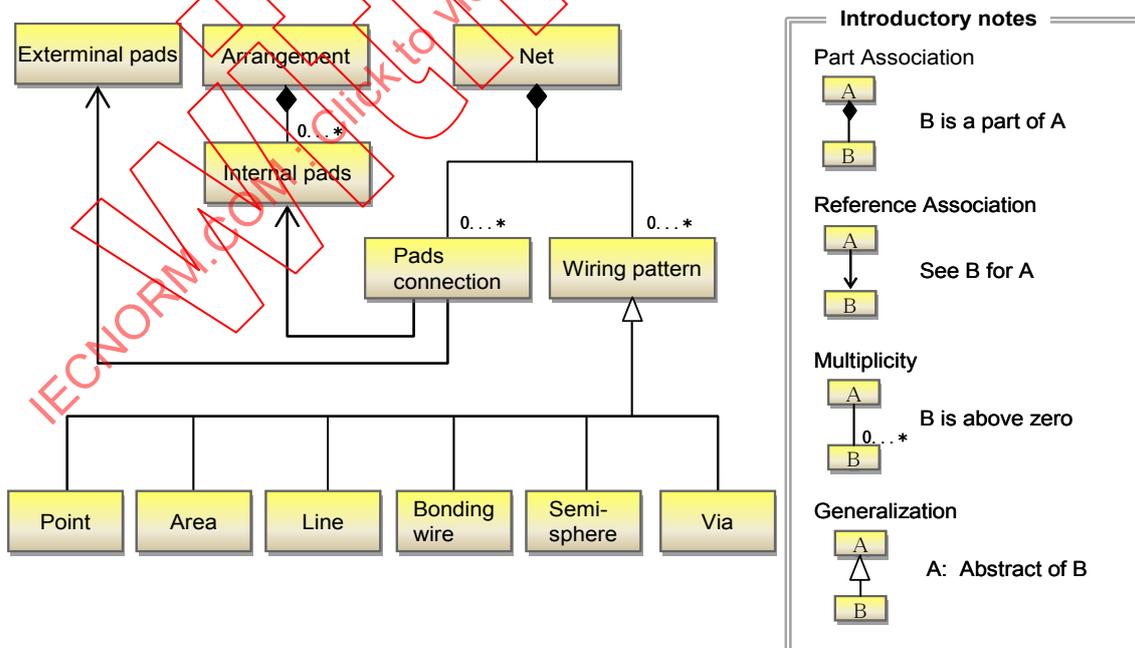
Figure 2.24 – Data structure of net information

2.4.5   Artwork information

Artwork information maintains artwork figure data on a board which are not included in the net information. Artwork figures include the following basic figures. Symbol mark, mold, spacer and remarks are also included in the information.

1) Point

2) Area

3) Line

4) Text

5) Bonding wire

6) Semi-sphere

7) Rectangular prismoid

8) Via

9) Device

2.4.6   Package information

The package information maintains the figures when the main structure has the package figure. Device package figure can use the following basic figures.

1) Point

2) Area

3) Line

4) Text

5) Semi-sphere

6) Rectangular prismoid

2.4.7   External port information

External points are the terminals of signals to supply electronic information from embedded devices and board to outside of the board. The point information maintains the shape and names of the external points the board structure has. The following shapes can be used for the information.

1) Point

2) Area

3) Line

4) Semi-sphere

5) Via

2.4.8   Internal port information

Internal ports are the terminals when a device is embedded to supply data to external ports. They connect the inside net of the board to outside world and have the same structure as the external ports.

2.4.9   User expansion information

The user expansion information illustrated in Figure 2.1 is possible to expand of definition data and board data. Property is expandable data by the user of the format. It is possible to apply this property to a part of definition data and board data. It is possible to select any combination of "definition name" = "data".

2.5   Defined data

Defined data are the definition of repeatedly used information. The definition data illustrated in Figure 2-1 contain the following four definitions.

1) Layer definition
2) Land definition
3) Via definition
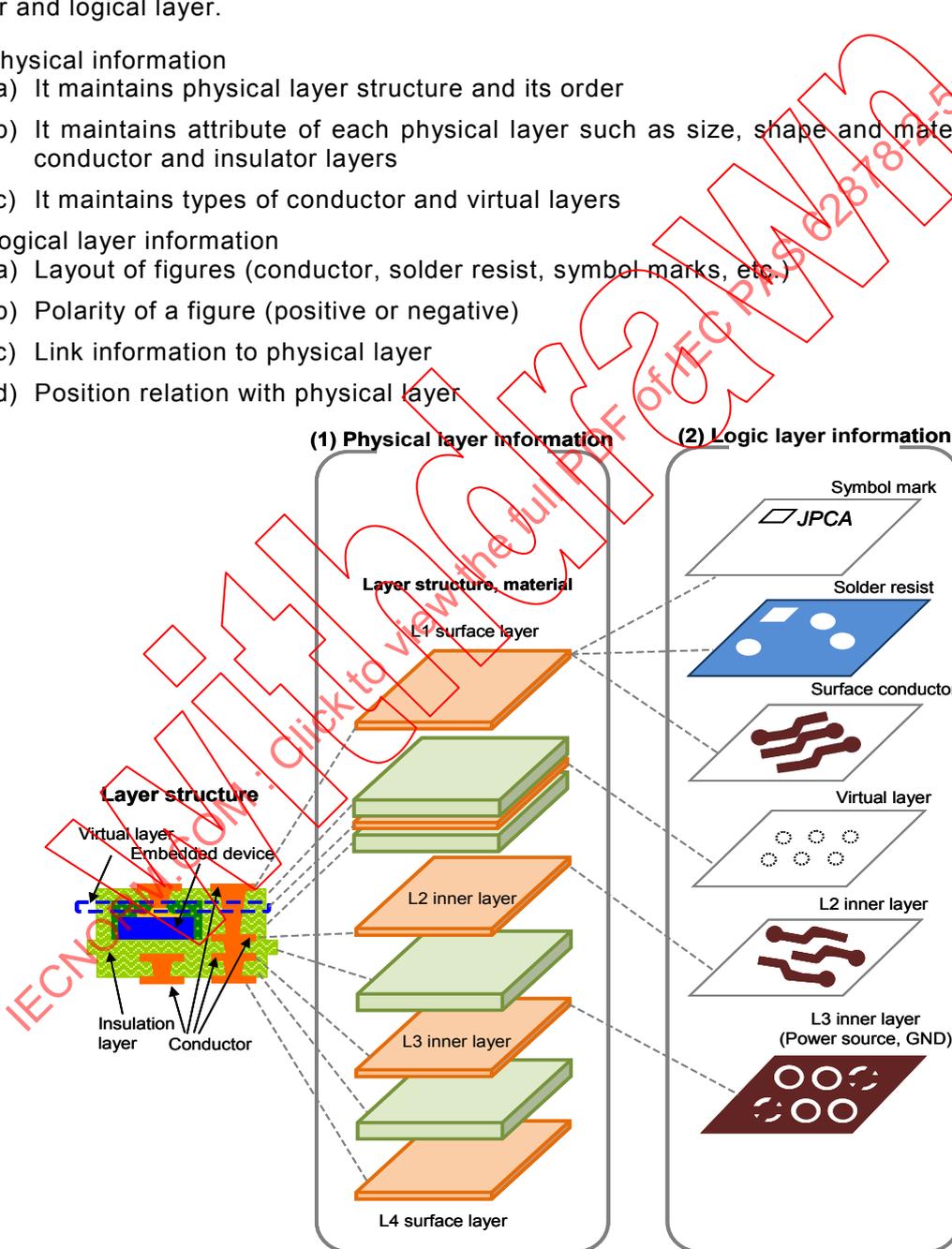4) Device definition

2.5.1   Layer definition

Layer definition includes the two types of information, physical information which gives physical figures and construction, and logical information which can be specified arbitrary necessary in design. The virtual layer is included in the physical information. It is also possible to link physical layer and logical layer.

(1)Physical information
    a) It maintains physical layer structure and its order
    b) It maintains attribute of each physical layer such as size, shape and material of both conductor and insulator layers
    c) It maintains types of conductor and virtual layers

(2)Logical layer information
    a) Layout of figures (conductor, solder resist, symbol marks, etc.)
    b) Polarity of a figure (positive or negative)
    c) Link information to physical layer
   d) Position relation with physical layer

Figure 2.25 – Relation of layer definition data

2.5.2   Land definition

It defines the land information used in device embedded substrate as shown in Figure 2.26.

1) It contains a land having more than one basic figure

2) It contains a land combined with positive and negative figures

3) It contains all the lands except a conductor land having resist
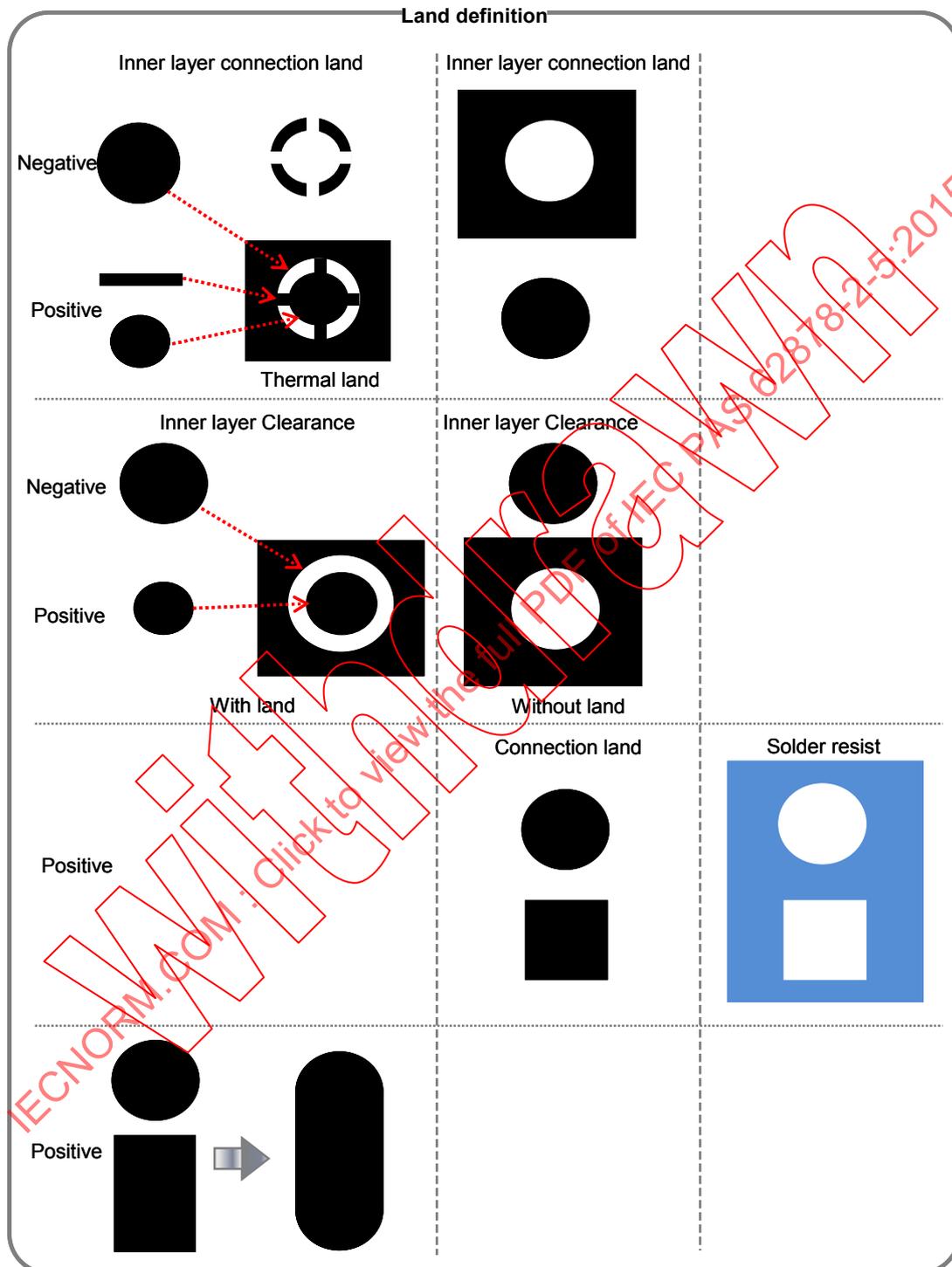
Figure 2.26 – Land definitions

2.5.3   Via definition

Via definition is the information of holes and lands used in a device embedded substrate as illustrated in Figure 2.27.

(1) Hole information