IEC/PAS 62686-1

Edition 1.0 2011-04

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

Process management for avionics – Aerospace qualified electronic components (AQEC) –
Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

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ELECTROTECHNICAL
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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE QUALIFIED ELECTRONIC COMPONENTS (AQEC) –

Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public.

STACK Specification S/0001 revision 14 *General Requirements for Integrated Circuits and Discrete Semiconductors* has served as a basis for the development of Part 1 of this publicly available specification.

IEC PAS 62686-1 has been processed by IEC technical committee 107: Process management for avionics.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
107/126/PAS	107/136A/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single 3-year period, following which it shall be revised to become another type of normative document, or shall be withdrawn.

A bilingual version of this publication may be issued at a later date.

PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE QUALIFIED ELECTRONIC COMPONENTS (AQEC) –

Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

1 Scope

This PAS defines the minimum requirements for general purpose 'off the shelf' COTS integrated circuits and discrete semiconductors for high reliability applications.

This PAS complements IEC/TS 62564-1. IEC/TS 62564-1 is to be used for high reliability applications where additional manufacturer's data is required beyond the publicly available manufacturer published datasheets, e.g. where additional thermal performance data is required for thermally challenging applications or when additional DO-254 verification data is needed for complex components for flight critical applications etc.

This PAS is to be used wherever possible for components that typically can be applied to operate in high reliability applications within the manufacturers publicly available datasheet limits. It is recommended that this PAS be used in conjunction with IEC/TS 62239 for avionics applications.

This PAS is identical to STACK Specification S/0001 revision 14 which is included in Annex A.

NOTE Adoption of the STACK Specification S/0001 revision 14 will enable all existing STACK Certified manufacturers to be audited by IECQ under the new STACK-IECQ joint venture.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60695-2-2, *Fire hazard testing – Needle flame test*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC/TS 62239, *Process management for avionics – Preparation of an electronic components management plan*

IEC/TS 62564-1, *Aerospace qualified electronic component (AQEC) – Part 1: Microcircuits*

STACK S/0001 revision 14, *General Requirements for integrated circuits and discrete semiconductors*

EN 100015-3, *Protection of electrostatic sensitive devices. Requirements for clean room areas*

EIA 471, *Symbol and Labels for Electrostatic Sensitive Devices (ESD)*

EIA 541, *Packaging materials for ESD sensitive items*

EIA 556, *Outer shipping container bar code label standard*

JP001.01, *Foundry process qualification guidelines*

JEP119, *Performing Standard Wafer level Electromigration Accelerated |Test (SWEAT)*

JEP130-A, *Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing (Tubes, Trays, and Tape and Reel)*

JEP138, *User guidelines for IR thermal imaging determination of die temperature*

JESD6 , *Measurement of small values of transistor capacitance*

JESD22-A101, *Steady state temperature humidity bias life test*

JESD22-A102 , *Accelerated moisture resistance unbiased autoclave*

JESD22-A103 , *High temperature storage life*

JESD22-A104 , *Temperature cycling*

JESD22-A108 , *Temperature bias and operating life*

JESD22-A109 , *Hermeticity*

JESD22-A110 , *Highly accelerated temperature and humidity stress test (HAST)*

JESD22-A113 , *Preconditioning of plastic surface mount devices prior to reliability testing*

JESD22-A114 , *Electrostatic Discharge Sensitivity (ESDS) testing Human Body Model (HBM)*

JESD22-A117 , *Endurance – Program/Erase cycle*

JESD22-A118 , *Accelerated moisture resistance – unbiased HAST*

JESD22-B100 , *Physical Dimension*

JESD22-B101 , *External visual*

JESD22-B102 , *Solderability test method*

JESD22-B103 , *Vibration, variable frequency*

JESD22-B104 , *Mechanical shock*

JESD22-B105, *Lead integrity*

JESD22-B106 , *Resistance to soldering heat*

JESD22-B107 , *Marking permanency*

JESD22-B116 , *Wire bond shear test*

JESD24, *Power MOSFETS*

JESD24-3, *Addendum No 3 to JESD24 – Thermal impedance measurements for vertical power mosfets (delta source-drain voltage method)*

JESD24-4, *Addendum No 4 to JESD24 – Thermal impedance measurements for bipolar transistors (delta base-emitter voltage method)*

JESD28, *Procedure for measuring N-Channel MOSFET hot-carrier degradation at maximum substrate current under DC stress*

JESD282, *Silicon rectifier diodes*

JESD313, *Thermal resistance measurements of conduction cooled power transistors*

JESD36, *Standard Description of Low-Voltage TTL-Compatible, 5 v Tolerant CMOS Logic Devices*

JESD46, *Customer notification of Product/Process changes by Semiconductor Supplier's*

JESD47, *Stress test driven qualification of integrated circuits*

JESD48, *Product Discontinuance*

JESD51-1, *Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)*

JESD51-2, *Integrated circuits thermal test method environmental conditions – natural convection (still air)*

JESD52, *Standard For Description of Low-Voltage TTL-Compatible CMOS Logic Devices*

JESD531, *Thermal resistance test method for signal and regulator diodes (forward voltage, switching method)*

JESD625, *Requirements for handling Electrostatic Discharge Sensitive devices*

JESD76, *Description of 1.8 V CMOS Logic Devices*

JESD76-1, *Standard Description of 1.2 V CMOS Logic Devices (Wide Range Operation)*

JESD76-2, *Standard Description of 1.2 V CMOS Logic Devices (Normal Range Operation)*

JESD76-3, *Standard Description of 1.5 V CMOS Logic Devices*

JESD78, *IC Latchup test*

JESD79, *Double Data Rate (DDR) SDRAM Specification*

JESD79-2, *DDR2 SDRAM Specification*

JESD79-3, *DDR3 SDRAM Standard*

JESD80, *Standard for Description of 2.5 V CMOS Logic Devices*

JESD86, *Electrical Parameter Assessment*

JESD89, *Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices*

JESD94.01, *Application Specific Qualification Using Knowledge Based Test Methodology*

JESD99, *Terms, Definitions and Letter Symbols for Microelectronic Devices*

J-STD-004, *Requirements for soldering fluxes*

J-STD-020, *Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices*

J-STD-033, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*

J-STD-035, *Acoustic microscopy for non-hermetic encapsulated electronic components*

MIL-STD-883, *Test methods standard microcircuits*

MIL-STD-750, *Test Method standards for semiconductor devices*

UL94, *Flammability of plastic materials for parts in devices and appliances, tests for*

AEC-Q100, *Stress Test Qualification for Integrated Circuit*

AEC-Q101, *Stress Test Qualification for Discrete Semiconductors, Customer Specific Requirements (ISO/TS-16949) Semiconductor Commodity – For use by the Semiconductor Suppliers*

3 Terms, definitions and abbreviations

For the purposes of this document, the following terms, definitions and abbreviations apply. When the following terms are used in *Italics*, they have the meaning defined in this clause.

3.1
calendar days
continuous days, including weekends and holidays

3.2
customer, user
original equipment manufacturer (OEM) who procures integrated circuits and/or semiconductor devices compliant to this PAS and uses them to design, produce, and maintain systems

3.3
data sheet
document prepared by the manufacturer that describes the electrical, mechanical, and environmental characteristics of the component

3.4
deviation
user agreement to allow the delivery of a *shipping lot* which does not fully meet the requirements of this *specification*

Considered equivalent to concession for the purposes of this document.

3.5
device specification
document written by a *user* and agreed by the *supplier*

3.6
form
shape, arrangement of parts, visible aspect, mode in which a part exists or manifests itself, the material an item is constructed from

3.7
fit
qualified and competent; correct size and shape

3.8
function
work to a specification that an item is designed to without degrading reliability

3.9
incoming lot
one or more shipments of a *device,* grouped together for the purpose of incoming inspection

3.10
inner box
a box or bag containing *devices,* either in *magazines* or bulk packaged

3.11
integrated circuit
microcircuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purpose of construction and commerce

3.12
limitation
requirement of this specification that is not met

3.13
magazine
sticks, tubes, matrix trays, tape/reel, etc.

3.14
microcircuit, component, device
electrical or electronic device, with a high circuit-element density, in which all or some of the circuit elements are inseparably associated and electrically interconnected (on one or more substrates, in a unique indivisible package) so that it is considered to be indivisible for the purpose of construction and commerce

3.15 outer box
outer shipping container, containing one or more *inner boxes*

3.16
room remperature
temperature of 25 ^{o}C ± 5 ^{o}C

3.17
semiconductor, device
electronic devices in which the essential electrical characteristic distinguishing electronic conduction takes place due to the flow of charge carriers within one or more semiconductor materials

This includes:

a) semiconductor diodes which are semiconductor devices having two terminals and exhibiting a nonlinear voltage-current characteristic, and

b) transistors which are active semiconductor devices capable of providing power amplification and having three or more terminals.

3.18
shipping lot
single lot of one or more *outer boxes* received by a *user*

3.19
supplier
the company identified by the logo or name marked on the device

3.20
termination
element of a component that connects it electrically and mechanically to the next level of assembly

3.21
triboelectric charge
electrical charge generated by frictional movement or separation of two surfaces

3.22
user
the general public using this IEC specification , STACK Members, IECQ Certification Bodies (CBs) or organizations authorized by the STACK Office to use this specification

3.23
waiver
written notice that a requirement of this *specification* no longer applies or is relaxed as requested during the registration process

If granted by the STACK Members, the *waiver* shall be documented on the Registration Certificate and is applicable to that individual *supplier* only.

4 Abbreviations

AQEC	Aerospace qualified electronic component
BPSG	Borophosphosilicate glass
COTS	Commercial off the shelf
CMOS	Complementary metal oxide semiconductor
DPM	Defects per million. It may also be referred as PPM (parts per million).
DSCC	Defence supply centre Columbus (see http://www.dscc.dla.mil/)

ECMP	Electronic component management plan
FFF	Form, fit and function
FIT	Failures in time
HAST	Highly accelerated stress test
HCI	Hot carrier injection
HTOL	High temperature operating life
LTB	Last time buy
LTPD	Lot tolerance percent defective
MSL	Moisture sensitivity level as defined in J-STD-20 relating to the packaging and handling precautions needed for semiconductors
NBTI	Negative bias temperature instability
PCN	Product change notification
SEE	Single event effect
SEU	Single event upset
SER	Soft error rate
THB	Temperature humidity bias
T_{op}min	Minimum operating temperature
T_{op}max	Maximum operating temperature

5 Technical requirements

The *supplier* shall provide the *user* requirements for quality, reliability and general requirements for integrated circuits and discrete semiconductors not otherwise governed by and supplied to Military Specifications, as stated in STACK S/0001 revision 14. STACK S/0001 specification revision 14 is included in Annex A.

NOTE 1 The required information is available to STACK Members by a method agreed during registration and to IECQ certified companies from their IECQ certification body (IECQ CB).

NOTE 2 Limitations may be identified during a certification audit where some of suppliers products do not meet the requirements of this specification due to marketing reasons. In that event, the supplier shall be noted as having limitations which shall be recorded in the audit report and on the certificate. These limitations are applicable to that individual supplier only.

Annex A
(normative)

STACK Specification S/0001 Issue 14

IEC QUALITY ASSESSMENT SYSTEMS FOR HIGH RELIABILITY INTEGRATED CIRCUITS AND DISCRETE SEMICONDUCTORS

IEC QUALITY ASSESSMENT SYSTEMS FOR HIGH RELIABILITY INTEGRATED CIRCUITS AND DISCRETE SEMICONDUCTORS

(IECQ System)

GENERAL REQUIREMENTS FOR INTEGRATED CIRCUITS AND DISCRETE SEMICONDUCTORS

JOINT COMPANY STANDARD

This is a Joint STACK INTERNATIONAL & IECQ
Specification issued by:
IECQ on behalf of both organisations
www.iecq.org
www.stackinternational.com
Tel: +44 (0) 1727 829100
Fax: +44 (0) 1727 821542

CONTENTS

1. INTRODUCTION

1.1 **Purpose and Scope:** This *specification* defines *user* quality, reliability and general requirements for *integrated circuits* and *discrete semiconductors*, not otherwise governed by and supplied to Military Specifications. Thus it forms the basis of the Stack Registration and Certification programs. Organizations complying with this specification may apply for assessment and certification under the International IECQ Process Approvals Scheme by contacting an approved IECQ Certification Body (CBs) listed at www.iecq.org.

1.2 **Use of Equivalent Tests:** To comply with the requirements of this *specification*, the *supplier may* use the test methods and methodologies specified herein or any other equivalent test method. Proposed equivalent test methods, rationale and supporting data *shall* be reviewed during the Registration and or Certification processes by the STACK members or the audit team (including the IECQ CB assessment Team) and shall achieve the same end objectives as specified herein. The *user* reserves the right to reject product failing to meet the test methods (or equivalent test methods) specified herein. Use of such equivalent tests shall not be considered to be *deviations* or *waivers* to the requirements of this *specification*.

1.3 **Liaison:** Enquiries relating to this *specification*, which concern product deliveries or orders, *shall* be addressed to the *user*. Enquiries relating to registration should be addressed to:

STACK International,
Tyttenhanger House,
Coursers Road,
Colney Heath,
St. Albans,
AL4 0PG,
U.K.
Tel: +44 (0)1727 829100
Fax: +44 (0)1727 821542

1.4 **Translation:** If translated into other languages the English language version of this *specification shall* prevail.

1.5 **Compliance with Internal Standards:** This document does not exempt the *suppliers* of their responsibility to meet their own company internal requirements.

2. REFERENCED STANDARDS

2.1 References to other documents form a part of this *specification* to the extent specified herein. Where no particular document revision is given the latest revision is intended. In case of conflict between this *specification* and the content of any referenced standard (excluding Section 19), the content of this *specification* defines the STACK requirement.

EN 100015-3	Protection of electrostatic sensitive devices. Requirements for clean room areas.
EIA 471	Symbol and Labels for Electrostatic Sensitive Devices (ESD).
EIA 541	Packaging materials for ESD sensitive items.
EIA 556	Outer shipping container bar code label standard.
IEC 60695-2-2	Fire hazard testing - Needle flame test.
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JEP130-A	Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing (Tubes, Trays, and Tape and Reel).
JEP138	User guidelines for IR thermal imaging determination of die temperature.
JESD6	Measurement of small values of transistor capacitance.
JESD22-A101	Steady state temperature humidity bias life test.
JESD22-A102	Accelerated moisture resistance unbiased autoclave.
JESD22-A103	High temperature storage life.
JESD22-A104	Temperature cycling.
JESD22-A108	Temperature bias and operating life.
JESD22-A109	Hermeticity.
JESD22-A110	Highly accelerated temperature and humidity stress test (HAST).
JESD22-A113	Preconditioning of plastic surface mount devices prior to reliability testing.
JESD22-A114	Electrostatic Discharge Sensitivity (ESDS) testing Human Body Model (HBM).
JESD22-A117	Endurance - Program/Erase cycle.
JESD22-A118	Accelerated moisture resistance - unbiased HAST.
JESD22-B100	Physical Dimension.
JESD22-B101	External visual.
JESD22-B102	Solderability test method.
JESD22-B103	Vibration, variable frequency.
JESD22-B104	Mechanical shock.
JESD22-B105	Lead integrity.
JESD22-B106	Resistance to soldering heat.
JESD22-B107	Marking permanency.
JESD22-B116	Wire bond shear test.
JESD24	Power MOSFETS
JESD24-3	Addendum No 3 to JESD24 - Thermal impedance measurements for vertical power mosfets (delta source-drain voltage method).
JESD24-4	Addendum No 4 to JESD24 - Thermal impedance measurements for bipolar transistors (delta base-emitter voltage method).
JESD28	Procedure for measuring N-Channel MOSFET hot-carrier degradation at maximum substrate current under DC stress.
JESD282	Silicon rectifier diodes.
JESD313	Thermal resistance measurements of conduction cooled power transistors.
JESD36	Standard Description of Low-Voltage TTL-Compatible, 5 v Tolerant CMOS Logic Devices.
JESD46	Customer notification of Product/Process changes by Semiconductor *Supplier's*.
JESD47	Stress test driven qualification of integrated circuits.
JESD48	Product Discontinuance.
JESD51-1	Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device).
JESD51-2	Integrated circuits thermal test method environmental conditions - natural convection (still air).
JESD52	Standard For Description of Low Voltage TTL-Compatible CMOS Logic Devices
JESD531	Thermal resistance test method for signal and regulator diodes (forward voltage, switching method).
JESD625	Requirements for handling Electrostatic Discharge Sensitive devices.
JESD76	Description of 1.8 V CMOS Logic Devices.
JESD76-1	Standard Description of 1.2 V CMOS Logic Devices (Wide Range Operation).
JESD76-2	Standard Description of 1.2 V CMOS Logic Devices (Normal Range Operation).
JESD76-3	Standard Description of 1.5 V CMOS Logic Devices.
JESD78	IC Latchup test.
JESD79	Double Data Rate (DDR) SDRAM Specification.
JESD79-2	DDR2 SDRAM Specification.
JESD79-3	DDR3 SDRAM Standard.

JESD80	Standard for Description of 2.5 V CMOS Logic Devices.
JESD86	Electrical Parameter Assessment.
JESD89	Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices.
JESD94.01	Application Specific Qualification Using Knowledge Based Test Methodology.
JESD99	Terms, Definitions and Letter Symbols for Microelectronic Devices.
J-STD-004	Requirements for soldering fluxes.
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices.
J-STD-033	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.
J-STD-035	Acoustic microscopy for non-hermetic encapsulated electronic components.
MIL-STD-883	Test methods standard microcircuits.
MIL-STD-750	Test Method standards for semiconductor devices.
UL94	Flammability of plastic materials for parts in devices and appliances, tests for.
AEC-Q100	Stress Test Qualification for Integrated Circuits.
AEC-Q101	Stress Test Qualification for Discrete Semiconductors
	Customer Specific Requirements (ISO/TS-16949) Semiconductor Commodity – For use by the Semiconductor Suppliers.

3. TERMS AND DEFINITIONS

3.1 For the purposes of this *specification,* when the following terms are used in *Italics* they have the meaning defined in this section:

Available:	The required information is available to STACK Members by a method agreed during registration and to IECQ Certified companies from their IECQ Certification Body (IECQ CB).
Calendar Days:	Continuous days, including weekends and holidays.
Deviation:	*User* agreement to allow the delivery of a *shipping lot* which does not fully meet the requirements of this *specification*. Considered equivalent to concession for the purposes of this document
Data Sheet:	A *device* specification written by the *device* manufacturer.
Device:	An *integrated circuit* or *discrete semiconductor*.
Device Specification:	A *device* specification written by a *user* and agreed by the *supplier*.
Discrete Semiconductor:	Applies to transistor, diode, or semiconductors of similar complexity.
DPM:	Defects per million may also be referred as PPM (parts per million)
Form/Fit/Function:	As defined in JESD46 i.e.:
Form -	Visual appearance including shape, color, marking and surface finish etc.
Fit -	External dimensions and associated tolerances etc.
Function -	Electrical, mechanical, thermal, and performance characteristics, etc.
Incoming Lot:	One or more shipments of a *device,* grouped together for the purpose of incoming inspection.
Inner Box:	A box or bag containing *devices,* either in *magazines* or bulk packaged.
Integrated Circuit:	A microcircuit is a small circuit having a high equivalent circuit element density which is considered as a single part composed of interconnected elements on or within a single substrate (silicon) to perform an electronic circuit function. (This excludes printed wiring boards (PWBs), circuit card assemblies (CCAs) and modules composed exclusively of discrete electronic parts.)

Limitation: It may be identified during a Certification Audit that some of a *suppliers* products do not meet the requirements of this *specification* due to marketing reasons. In that event, the *supplier* shall be noted as having *limitations* which shall be recorded in the audit report and on the Certificate. These *limitations* are applicable to that individual *supplier* only.

LTPD: Lot tolerance percent defective.

Manufacturing Lot: A definite quantity of *devices* tracked at each manufacturing operation. It is associated with a travel log and constitutes a group, homogeneously processed through all manufacturing operations under uniform manufacturing conditions.

May: Indicates a course of action which is permissible within the limits of this document.

Magazine: Sticks, tubes, matrix trays, tape/reel, etc.

MSL: Moisture Sensitivity Level as defined in J-STD-20 relating to the packaging and handling precautions needed for semiconductors.

PCN: Product Change Notification.

Outer Box: An outer shipping container, containing one or more *inner boxes.*

Room Temperature: 25 °C ± 5 °C

Shall: Indicates a requirement.

Should: Offers a guideline or recommendation that might be used or helpful to assure compliance to this document.

Shipping Lot: A single lot of one or more *outer boxes* received by a *user*.

Specification: This *specification* together with all other documents referred to as forming part thereof.

Supplier: The company identified by the logo or name marked on the *device*.

Termination: Method by which the *device* is attached to a board, includes leads, pads, balls, columns etc.

T_{op}min: Minimum operating temperature.

T_{op}max: Maximum operating temperature.

Triboelectric Charge: Electrical charge generated by frictional movement or separation of two surfaces.

User: STACK Members, IECQ Certification Bodies (CBs) or organizations authorized by the STACK Office to use this specification.

Waiver: A written notice that a requirement of this *specification* no longer applies or is relaxed as requested during the Registration process. If granted by the STACK Members, the *waiver* shall be documented on the Registration Certificate and is applicable to that individual *supplier* only.

3.2 Other common physical and electrical terms along with industry-standard symbols and abbreviations for the characterization, nomenclature, and classification of a *device should* be as described in JESD99.

4. ADMINISTRATION

4.1 Registration to this *Specification*:

4.1.1 STACK *Supplier* Registration or IECQ Registration is a formal *supplier* declaration that the *supplier's* standard qualification procedure, product monitor program and manufacturing processes are in compliance with this *specification* or that compliance will be achieved in a specified time and, that the other requirements of this *specification* will be met when *devices* are purchased to this *specification*. A *waiver may* be granted at the discretion of the STACK Membership or IECQ CBs. IECQ Certificate of Approval may be issued, to demonstrate compliance with this specification, by an IECQ CB according to IECQ Process Approvals requirements. Applications are to be lodged with IECQ CBs.

4.1.2 STACK Distributor Registration or IECQ Registration is a formal *distributor* declaration that the distributor's procedures will ensure the following requirements of this *specification* are met when parts are ordered to this *specification* for a *supplier* currently listed as registered on www.stackinternational.com. (All other requirements will be deemed the responsibility of the registered *supplier*.)

- Forwarding of product change and discontinuance notices received from the *supplier*.
- Date code age on delivery.

IECQ Certificate of Approval may be issued, to demonstrate compliance with this specification, by an IECQ CB according to IECQ Process Approvals requirements. Applications are to be lodged with IECQ CBs.

4.1.3 Suspension of STACK Registration / IECQ Registration can occur if it is determined that a Registered *supplier* is not fully compliant with this *specification,* or any *waivers* granted and if after due discussion, an agreement cannot be reached to resolve the problem. Registration / IECQ Registration may be suspended until the non-compliance is corrected or a corrective action plan has been agreed upon. Suspension of registration may have an impact on any certifications held.

4.2 STACK **Certification or IECQ Certification to the Specification:**

4.2.1 STACK *Supplier* or IECQ Certification is a formal audit by a team of STACK auditors or IECQ CBs, directed by a Lead Auditor who is responsible for closing out the audit to the requirements of this *specification*. The results of the audit *shall* be written up in an audit report, available to all STACK and IECQ Members, which *shall* contain details of any *limitations*, use of equivalent tests or processes approved during the audit by the Stack auditors and IECQ CBs. The audit checklist SP04 *shall* be used and shall be the basis of the audit report.
IECQ Certificate of Approval may be issued, to demonstrate compliance with this *specification*, by an IECQ CB according to IECQ Process Approvals requirements. Applications are to be lodged with IECQ CBs.

4.2.2 Suspension of STACK or IECQ Certification can occur if it is determined that a STACK or IECQ Certified *supplier* is not fully compliant with this *specification,* or accepted *limitations* if any and if after due discussion, an agreement cannot be reached to resolve the non-compliance. Certification may be suspended until the non-compliance is corrected or a corrective action plan has been agreed upon. Suspension of certification may have an impact on any registrations held.

4.3 **Proprietary Data:** Where the information provided for Registration or Certification purposes is considered proprietary, that information *shall* be disseminated from the *supplier* to the STACK members or IECQ CBs through the STACK or IECQ office. Non-Disclosure Agreements can be used, if required.

4.4 **Deviations:**

a) In the event that a *supplier* intends to deviate from the requirements of the purchase order, relevant specifications, or this *specification* for a custom part where the *user* is known, prior written consent must be obtained from the *user*. If *device* specific *deviation* procedures are otherwise specified, (e.g. in a Custom ASIC purchase contract) those requirements will apply.
b) In the event that a *supplier* deviates from the requirements of the purchase order, relevant specifications, standard *data sheet*, or this *specification* for an “off the shelf” catalogue part where the *user* is unknown, the *suppliers shall* distribute this information via their sales teams and/or on their web pages and to all franchised distributors.
c) Applications for *deviations* must contain the following information. If any item is not known at time of request, the request should be submitted with the remaining information to follow as soon as practicable:

Supplier type number
Description of deviation(s)
Quantities or time period affected
User part number
Cause of deviations.
Corrective actions being taken to overcome the deviation on subsequent deliveries, as required.

d) *Devices* subjected to application for a *deviation shall* be held at the *supplier's* premises pending reply unless otherwise instructed by the *user*.

4.5 **Updates to this Specification:**
Updates to this *specification* will be circulated to all STACK registered *suppliers* and IECQ Registered Suppliers. A period of time will be defined at each release date depending on the extent of the change to allow *suppliers* to formally accept the new issue.

5. PROCEDURES

5.1 Product Discontinuation: Notification *shall* be in accordance with JESD48 or equivalent with the exception of Timing as described in paragraphs 5.1.1, 5.1.2 below.

5.1.1 The *supplier shall* provide to the *user* a minimum 12 months notice of last order dates for single source *devices* and 6 months for multi sourced *devices*.

5.1.2 The *supplier may* give less than the specified notice period provided a mutually acceptable extension (up to the specification limit) is negotiated with any STACK Member needing a different period.

5.1.3 For custom ASIC's the normal procedure is to include discontinuation notice in the purchase contract.

5.2 **ESD Protection during Manufacture:** All *integrated circuits* and *discrete semiconductors* are considered to be static sensitive and *shall* be so protected through the *supplier's* manufacturing operation. *Suppliers shall* ensure that *devices* are not exposed to static damage and are not degraded or damaged due to static discharge. EN100015-3 and JESD625 are examples of suitable standards for ESD precautions in wafer fab and probe. Suppliers holding current IECQ Certification for compliance with IEC 61340-5-1 shall be deemed to have satisfied this requirement.

5.3 **Specification Control:** The *supplier shall*:
a) Have central or local record of the *users* part number and specification, against the product to be delivered.
b) Ensure the specifications on the purchase documents have been reviewed and accepted by personnel authorized to do so.

5.4 **Traceability:**
a) The *supplier shall* have traceability for any *device* in a *shipping lot* through a route code, lot code or other marking on the *device* or *magazine* or *inner box* to identify the manufacturing route, e.g.: groups of wafer lots, wafer fab location, assembly location, test location.
b) The information needed to interpret the code *shall* be *available*.
c) The procedure *shall* be available for inspection during audit.

6. PRODUCT OR PROCESS CHANGE NOTIFICATION (PCN)

6.1 **Notification:** In the event of the *supplier* proposing or making a change to a *device*, then:

a) The *supplier shall* give at least 90 *calendar days* written notice prior to shipping changed product. The *user* will respond to confirm the date that changed product shipments can begin (could be less than 90 *calendar days*), advice that changed product is not acceptable, or request further information.

b) For custom ASIC devices, change notification periods are normally specified in the purchase contract.

c) In an event beyond the control of the *supplier* where 90 *calendar days* notice cannot be given, the *supplier* shall reach a mutually agreed lesser notice period with any STACK Member affected by the change or the IECQ CB that issued IECQ Certification.

6.2 **Notification Details:** The *PCN shall* include the following items:

a) Title of change.
b) *Supplier* type number(s) affected.
c) *Supplier* notification identification number.
d) Estimated last order and shipment dates for unchanged *devices* to be supplied on request.
e) Estimated earliest shipment date of changed *devices*.
f) Manufacturing location and product line affected.
g) A thorough description of the proposed change.
h) Means of distinguishing changed *devices* from unchanged *devices*. This may be a date code, lot code, date code range or distinguishing marking or feature that is visible to the *user* at point of receipt of shipment.
i) Sufficient engineering and/or qualification test data, including details of any qualification test vehicle used and its applicability to the product change, *shall* be *available* on request to demonstrate that the change will not adversely affect *device form*, *fit*, *function,* quality or reliability, and that the changed product will continue to meet the specified requirements.
j) *User* part number of the affected *device* (preferred item but not mandatory).

6.3 **Notifiable Changes:** JESD46 shall be used as a guide to changes requiring notification.

7. SHIPMENT CONTROLS

7.1 Shipping container packaging and date code marking *shall* be in accordance with JEP130 or equivalent.

7.2 **Date Code Remarking:** If the date of assembly and test are both marked, the test date can be remarked if the *device* is re-tested at a later date. If only one date is marked to represent the manufacturing date and initial electrical test it shall not be changed unless it is necessary to correct poor quality marking or incorrect information and provided that the time delta between the original mark and the remark is less than 6 weeks.

7.3 **Inner Box Formation:**

a) It is preferred that the *inner box shall* contain only *devices* of the same die revision/stepping level.

b) It is preferred that *devices* shall also be from the same:
- wafer fab location.
- assembly site.
- outgoing QA electrical inspection site.

7.4 **Date Code Age on Delivery:**
a) The date codes of *devices shall* not be older than 24 months upon *users* receipt date.
b) For custom ASIC devices the date code age limits will normally be defined in the purchase contract.
c) If the *supplier* wishes to ship *devices* outside the specified limit, the *deviation* procedure *should* be used.

7.5 **ESD Marking:** Symbols used and labeling *shall* be in accordance with EIA471 or equivalent.

7.6 **MSL:** Labeling and packaging *shall* be in accordance with J-STD-033 or equivalent.

8. ELECTRICAL

8.1 **Operating Conditions:** *Shall* be as defined in the *device* specification or *data sheet*.

8.2 **Electrical Test:** All packaged *devices* shipped must have passed a production electrical test program, or in the case of *user*-specific *devices*, a test program approved by the *user*. Tested wafer or die products *shall* have an effective equivalent wafer probe test. Untested wafer and die products *shall* have met the *suppliers* minimum process control monitor (PCM) requirements. JEDEC test methods *shall* be used wherever possible.

8.2.1 Electrical Parameter Assessment: Test methods for assessing Electrical Parameter Distributions (ac, dc, functional and timing) of *devices should* be in accordance with JESD86.

8.2.2 SDRAM memories *should* be designed and tested in accordance with the JESD79 series of specifications.

8.2.3 Logic families *should* be designed and tested in accordance with the JESD36, JESD52, JESD76 or JESD80 series of specifications.

8.2.4 Power mosfets *should* be tested in accordance with the JESD24 series of specifications.

8.2.5 Silicon rectifier diodes *should* be tested in accordance with JESD282.

9. MECHANICAL

9.1 **Package Dimensions:** Package dimensions specified in industry standard outlines, (e.g. JEDEC outlines) will be met as specified, if the package is stated as compliant with that outline.

9.2 **Device or Packaging Marking:**
9.2.1 Legibility: All the specified markings on the *device or packaging shall* be clearly legible.

9.2.2 Top Surface: All of the following required markings *shall* be marked on the topside except where otherwise indicated below:
a) Pin 1 identifiable either by a mark or by reference to a physical feature of the *device.*
b) The *supplier's* name or logo.
c) The *supplier* type number or individual *user* part number as required.
d) Date code of assembly or test. Formats YYWW, or YWW or YM are acceptable. Y=year numeral, W=week numeral, M=month character. If both assembly and test date codes are marked the assembly code may be bottom marked.
e) A manufacturing route trace code. Top surface is preferred, but *device* bottom surface may be used.

9.2.3 Small Packages: If the marking area available on the *device* is too small to do so, then the smallest unit container is to include all the required marking.

9.3 **Moisture Sensitivity:** The moisture sensitivity of all non-hermetic surface mount components *shall* be tested and classified according to J-STD-020. The *MSL* classification *shall* be *available*.

9.4 **Robustness of Hermetic Seals:** Seal shall not be compromised by any normal handling, testing or manufacturing processes.

9.5 **Termination Finishes:** *Suppliers should* make available on their web pages or datasheets (or otherwise), information pertaining to the leaded (Pb) and lead-free *termination* finish qualification testing, *termination* material, finish alloy composition, and (if used) heat treatment process of parts used relative to the RoHS directive. In addition the following requirements *shall* be met:

a) Thickness limits *shall* be met over 95 % of *termination* surface. The *supplier* shall select appropriate measurement locations.
b) Plating composition and thickness limits *shall* be *available*.
c) It is not necessary for solder dipping to cover the entire *termination*. The area covered should be appropriate to the type of package: e.g. J bend packages – area below base plane; Gull wing packages – center of bottom radius to trimmed edge of *termination*.
d) Tin electroplate finishes must be dense, homogenous, free of co-deposited organic material and suitably treated to inhibit whisker growth.
e) Provide notification of changes, via the *PCN* process, to *termination* finish materials, thickness, or to plating process chemistry.

10. AUDIT CAPABILITY

10.1 **Internal Quality Audits:** The *supplier shall* periodically audit each internal location, to assess compliance with internal standards for the following areas listed below. Note, military or industry standards (e.g., ISO 9000, MIL-STD-883, AS9100, TS16949, etc...) or equivalent *shall* be adhered to:

• Quality System	• Calibration	• Failure analysis
• Shipment & Packaging	• Stores & Dispatch	• ESD Control
• Contract review	• Customer Service	• Production Test
• Design Management	• Process Control	• Subcontract Controls
• Purchasing	• Incoming Materials	• Wafer Fab & Probe
• *Supplier* Audits	• Documentation Control	• Assembly
• Training	• Product qualification	• Reliability monitor

The results of these audits and the audit acceptance criteria shall be available for onsite inspection during a STACK audit or IECQ CB audit. The internal quality audit documentation *shall* be *available* upon request.

10.2 **Sub Contract Manufacturing:** The *supplier shall* qualify and periodically audit all sub contracted operations to a standard equivalent to the *suppliers* internal operations.

11. QUALITY ASSURANCE

11.1 **Quality System:**

a) The *supplier shall* have an appropriate quality registration, e.g. one (or more) of ISO9000-2000, QS9000, TL9000, AS9100, TS16949, etc.., OR the *supplier shall* have established and documented a quality management system of equivalent standard.
b) The system *shall* ensure that the requirements of this *specification* are met.
c) The system *shall* provide for the prevention and ready detection of discrepancies and for timely and positive corrective action.

11.2 **Sampling Plans:** Appropriate and statistically valid sampling plans shall be used and documented. The target for reliability qualification of microelectronics by accelerated ageing is a *LTPD* better than 3 %. This may be achieved by overstress testing of sample sizes exceeding 76 *devices* from the specific *device* population, with no failures permitted, or by invoking structural similarity and accumulating samples from other *device* types at the level of build being tested. For example, thermal cycling is intended to evaluate die & wire bonding and back-end assembly, and the desired *LTPD* may be achieved from structurally similar builds of similar metallization, die size and attachment, wirebond material diameter, process, and loops.

11.3 **Failure Analysis Support:**

a) The *supplier shall* maintain an adequate failure analysis capability and provide a timely response to failures returned for failure verification or failure analysis.
b) Representative samples of *devices* returned as failures shall be analyzed and a failure analysis report issued to the originating *user*, typically within 30 *calendar days* of the receipt by the analytical facility of such returns.
c) For failure returns relating to a critical problem at a *user*, the failure analysis report shall typically be issued within 7 *calendar days* of receipt by the analytical facility.

11.4 **Outgoing Quality:**

11.4.1 *DPM* levels: The *supplier shall* measure Average Outgoing Quality (AOQ) in defects per million from uniform manufacturing processes and the results shall be in accordance with Table 1. The measurement of outgoing quality via in process measurements is acceptable in principle. The number of defects will include all *devices* non-conforming to any functional, electrical, visual or mechanical specification requirement of a *device*.

11.4.2 *DPM* calculation: Measurement may be by any appropriate classification and method, e.g. individual *devices* or *device* families, package type and/or technology family, in process measurements.

11.4.3 Corrective action: If the outgoing quality levels given in Table 1 are not met, the *supplier shall* take root cause corrective action and issue a closure date for achieving the required *DPM*.

Table 1 – Outgoing Quality

DEVICE FAMILY		Max DPM
Electrical	Transistor Count	
Discretes & Integrated Circuits:	<= 100k	50
	< 1000k	100
	>= 1M	150
Programmable logic when supplied programmed and tested		100
Visual/mechanical		200
NOTE If the *supplier* has provided other figures during registration or IECQ registration then those figures apply. This information will be considered proprietary and confidential to the STACK Members or in the case of IECQ registration the IECQ CB.		

11.4.4 Data reporting: AOQ data *shall* be compiled quarterly and be *available* upon request.

12. INCOMING INSPECTION

12.1 **Lot Acceptance:** *Users* reserve the right to perform *incoming lot* acceptance on every lot received, using any Incoming test in Table 2 or Qualification test in Table 3.

Table 2 – Incoming Test

Package Type	Test per Table 3	Insp. Level	AQL%
All	Electrical test	II	0.065
All	External Visual inspection	II	0.20
Hermetic only	Hermeticity fine	II	0.40
Hermetic only	Hermeticity gross	II	0.25
All	Dimensions	II	0.10

12.2 **Suspension of Deliveries:** The *user may* bring to the attention of the *supplier* any failure to meet a qualification or incoming test and to require the *supplier* to withhold further deliveries to that *user* until the cause of the failure has been identified and corrected.

12.3 **Loss of Approval:** A failure of one or more *shipping lots* of a specific *device* to meet the requirements of this *specification* or the *device* specification *may* constitute grounds for loss of approval. The action taken will depend on the nature of the problem found.

12.4 **AQL/LTPD Figures:** The AQL/*LTPD* figures quoted are for the purpose of individual incoming *lot* rejection; they do not imply an overall acceptance quality level.

12.5 **100 % Screening:** *Users* reserve the right to perform 100 % screening on individual *shipping lots* received and to reject to the *supplier* any *devices* which do not meet the specified requirements.

13. QUALIFICATION

13.1 **Methodology:** The *supplier shall* use appropriate methodologies to qualify new technology, new *devices* and *device* changes, to demonstrate that the *device* under qualification has the capability to meet the specified electrical, quality and reliability requirements, using Qualification Families as defined in JESD47:

13.1.1 Procedures and Methods are as per Table 3.

13.1.2 Alternate procedures and methods are acceptable as per Para. 1.2 (herein) and as follows:

a) Qualification to JESD47, for *integrated circuits* and their generic families, providing the following, additional, items are addressed by the *supplier*:
- Ball shear testing on BGA packages
- Electrical population drift calculations
- X-ray
- Long term FIT rate calculations
- Use of JP001.01 and/or JEP119 as the test method for Electomigration, Hot Carrier injection and Time dependent Dielectric Breakdown
- *MSL* rating assessment
- Marking Permanency
- Die Shear Strength
- Thermal Resistance
- Flammability
- Internal Visual Inspection

b) Qualification to AEC-Q100 for *integrated circuits* and their generic families providing the *supplier* address the following additional, items:
- The High Temperature Operating Life (HTOL) test *shall* be 1 000 hours minimum at TC=125 °C
- Soft error rate testing
- Marking permanency
- X-ray
- Use of JP001.01 and/or JEP119 as the test method for Electomigration, Hot Carrier injection and Time Dependent Dielectric Breakdown
- Non-volatile memory operating life
- Thermal resistance
- Flammability
- Internal Visual Inspection

c) Qualification to AEC-Q101 for discrete semiconductors and their generic families providing the supplier address the following additional items:
- Latch-up
- Steady State Operating Life
- High Temperature Blocking Bias
- High Temperature Bake
- Use of JP001.01 as the test method for Electromigration, Hot Carrier injection and Time Dependent Dielectric Breakdown
- Temperature Humidity Bias
- HAST
- Internal Water Vapour
- Flammability
- Internal Visual Inspection
- X-ray
- Lid Torque

d) Qualification to an Application Specific Scheme *should* be created as per methodology and guidance provided in JESD94. An application specific plan *should* address the subjects of concern contained in the preceding qualification schemes.

13.1.3 Accomplish Risk Analysis on the impact to Reliability and Quality.

13.1.4 Perform and document stress test driven qualification plans.

13.1.5 Perform and document the re-use of existing data based on product similarity arguments.

13.1.6 Perform and document the verified reliability models.

13.2 **Test Samples:**

13.2.1 Test Failures: The general acceptance level for all stress test qualification is zero rejects in the tested sample size. Test failures attributed to extraneous factors not related to the qualification stress applied shall not be counted against acceptance criteria. If excessive failures from non-qualification test related mechanisms are generated, the test shall be repeated. If a larger sample size than specified in Table 3 is used and failures allowed, then the result must meet an *LTPD* = 3 % for specified sample size of 76. The target *LTPD* requirement is stated in Section 11.2. In Table 3, lower sample quantities are allowed where the particular stress tests are not intended for statistical extrapolation, but for characterisation or package evaluation.

13.2.2 Additional samples: *Users* reserve the right to take additional samples for a qualification test result confirmation.

13.2.3 Consolidation of lots: Where production volumes of a *device* are low and the sample sizes specified are not economically feasible from one *manufacturing lot,* consolidation of lots is permissible. If consolidation of lots is performed, the combining of parts shall follow the similarity rules as per Paragraph 13.11 (Similarity Assessment).

13.2.4 Reduced sample sizes: The *supplier's* qualification procedures *may* allow *devices* to be released to the market after testing to a qualification schedule which does not fully meet STACK requirements, in terms of reduced sample size, reduced test time, etc. This is only acceptable providing test data continues to be accumulated as per Section 15 (Product Monitor) and corrective actions and or repeat testing is performed as necessary until the STACK qualification level is reached or exceeded in a target of 90 *calendar days*. Where IECQ Certification has been issued for compliance with this Specification, the IECQ CB shall decide on the acceptance of any reduced sample size.

13.3 **Qualification Categories:** The qualification *may* be conducted on a specific *device* type. Alternatively qualification *may* be accomplished by use of generic family qualification data providing similarity rules are followed, see Paragraph 13.10.

13.4 **Maintenance of Qualification Standard:** Regular quality and reliability test results, that are obtained from a monitor program, but which are not related to any particular customer shipment, are an acceptable method of maintaining the qualification standard of this *specification.* It is desirable that the manufacturer maintains a regime of 'Maintenance of Qualification' in order to ensure that reliability sensitive processes are routinely tracked and sample tested.

13.5 **In-Process Test Results:**

a) If any of the Inspection or Package qualification tests are performed on a regular basis in the manufacturing line, these tests need not be repeated in new *device* qualification testing.
b) If qualification tests are not performed, manufacturing inspection results showing the current quality level *shall* be included in the Qualification Report. Manufacturing package test results *shall* be *available*.

Table 3 – Technology/Family Qualification and Device Qualification

Test Code Information		Product family	TITLE	Test Reference See Paragraph 13.1 for more details	# of lots for Family Qual	SS per lot	# of lots for device Qual
			ELECTRICAL				
TC6	(ET)	IC, D	Electrical Test	JESD86/MIL883-M3012 or JESD6	3	50	1
TC7	(ED)	IC, D	Electrical Distributions	JESD86	3	30	1
TC16	(LU)	IC, D	Latch-Up	JESD78	1	6	1
TC5	(ESD)	IC, D	ESD – Human Body Model	JESD22-A114	1	3	1
TC28	(SER)	IC	Soft error	JESD89	-	-	-
			PROCESS				
TC22	(OI)	IC, D	Oxide Integrity	JP001.01	-	-	-
TC4	(EM)	IC, D	Electromigration	JEP119 or JP001.01	-	-	-
TC9	(HCI)	IC, D	Hot carrier injection	JP001.01	-	-	-
			ENDURANCE				
TC24	(PTC)	D	Power temperature cycling	MIL883-M1037	3	76	1
TC29	(SSOL)	D	Steady state operating life	JESD22-A108	3	76	1
TC13	(HTGB)	D	High temperature gate bias	JESD22-A108	3	76	1
TC12	(HTBB)	D	High temperature blocking bias	MIL750-1048	3	76	1
TC14	(HTRB)	D	High temperature reverse bias	JESD22-A108	1	76	1
TC15	(HTOL)	IC	High temperature operating life	JESD 22-A108	3	76	1
TC21	(NVL)	IC	Non Volatile memory operating life	JESD22-A117	1	22	1
TC11	(HTB)	D	High temperature bake	JESD22-A103	3	76	1
			TEMPERATURE/HUMIDITY				
TC25	(RSH)	D	Resistance to solder heat	JESD22-B106	1	30	1
TC31	(THRB)	D	Temperature humidity reverse bias	JESD22-A101	1	76	1
TC30	(TC)	IC, D	PC + Temperature cycling	JESD22-A104	1	32	1
TC32	(THB)	IC, D	PC + THB: 85°C/85%RH (or HAST) (plastic only)	JESD22-A101	1	76	1
TC32	(HAST)	IC, D		JESD22-A110	1	76	1
TC1	(AC)	IC, D	PC + HAST plastic only PC + Autoclave (plastic only)	JESD22-A102	1	32	1
			MECHANICAL				
TC23	(PD)	IC, D	Package dimensions	JESD22-B100	1	5	1
TC27	(SD)	IC, D	Solderability (76 leads / 5 devices min)	JESD22-B102	1	76	1
TC36	(WV)	IC, D	Internal water vapor (hermetic only)	MIL883-M1018	1	3	1
TC20	(MP)	IC, D	Marking Permanency	JESD22-B107	1	3	1
TC2	(BS)	IC, D	Bond Strength (76 wires/5 devices min)	JESD22-B116	1	76	1
TC3	(DS)	IC, D	Die Shear Strength	MIL883-2019	1	5	1
TC34	(TR)	IC, D	Thermal resistance	Not specified	1	3	1
TC8	(FL)	IC, D	Flammability (plastic only)	UL94	-	-	-
TC8	(FL)	IC, D	Alternative flammability (plastic only)	IEC 60695-2-2	1	3	1
TC17	(LI)	IC	Lead integrity (applicable devices)	JESD22-B105	1	3	1
TC33	(TS)	D	Terminal strength	MIL750-M2036	1	3	1
TC18	(LT)	IC, D	Lid torque (hermetic only)	MIL883-M2024	1	5	1
TC19	(MS)	IC	Mechanical sequence (hermetic only)	See Test	1	5	1
TC10	(HE)	IC, D	Hermeticity (hermetic pkg. end point test only)	JESD22-A109	-	-	-
TC38	(MSL)	IC, D	Moisture Sensitivity Level	J-STD020	-	-	-
TC39	(BST)	IC, D	Ball Shear	JESD22-B117A or AEC-Q100-010	-	-	-
			INSPECTION				
TC35a	(VI)	IC, D	External Visual Inspection	JESD22-B101	1	25	1
TC35b	(VI)	IC, D	Internal Visual Inspection	MIL883-M2010	1	5	1
TC37	(XR)	IC, D	X-Ray Inspection (plastic only)	MIL883-M2012	1	5	1

13.6 **Product Monitor Results:** If any Inspection or Package qualification tests are performed on a regular basis in product monitor testing, these tests need not be repeated in new *device* qualification testing.

13.7 **References:** are given for guidance only. Reference shall always be made to the appropriate Test Code information for full test details.

13.8 **Qualification Report:** The qualification report *shall* be *available* upon request.

13.9 **Archiving:** The qualification report and the test specification (not test program), used in the qualification *shall* be archived for a minimum of 3 years.

13.10 **Qualification by Similarity:**

a) A change must be qualified if there is a potential effect on performance, quality or reliability, or if there is any degree of uncertainty about the effect of the change.
b) Guidance on the qualification tests, which the *supplier should* consider applying, for the various combinations of die, package and process changes, is shown in Tables 1, 2 & 3 of JESD47. The *supplier shall* perform tests defined in the qualification table that are appropriate, or relevant to the change.
c) Upon request, the *supplier shall* provide data for any *device* transferred to a new process to prove that no design deficiencies (e.g. mechanical, electrical performance, reliability, single event effects etc.) were introduced by the process transfer.

13.11 **Similarity Assessment:** The principle of similarity *may* be applied in qualification, qualification of changes and product monitor testing.

13.11.1 Die Changes: The *supplier shall* document and operate an appropriate set of die similarity rules or guidelines applied by appropriate engineering review.

13.11.2 Process/Wafer Fab Changes: *Devices* to be assigned to a qualification family must share the same critical processes and material elements.

13.11.3 Package/Assembly Changes:

a) Package families shall be grouped by configuration and materials of construction. In general, all members of the group that are equal to or smaller in dimensions and lead count can be considered as similar to a qualified package, provided the assembly process technology is identical.

b) Packages *should* be qualified with the worst case configuration (e.g., the largest die) they are designed to carry that is currently in production. For custom ASIC's use of a "qualification die" is acceptable, such that die larger than the qualification die by +10 % by linear dimension are qualified, provided the package design maximum die size is not exceeded.

14. RELIABILITY

14.1 **Operating Reliability:**

a) Unless otherwise specified in the *device specification,* the failure rate of *devices* operating in systems at an ambient temperature of +55 °C shall not exceed the figures in Table 4. The *supplier shall*, upon request from the *user* make *available* FIT rate data to confirm application specific life expectancy. See Paragraph 15.5 for production maturity factors.
b) Results observed at a temperature other than +55 °C will be projected to this temperature, with 60 % confidence using an activation energy, appropriate to the failure mechanism observed. Refer to TC15 HTOL for calculation of acceleration factors; projected results shall show the 60 % confidence range.

c) For custom devices the *supplier shall* on request provide a FIT rate including the confidence range and operating life prediction to the *user* (based on a demonstrable methodology) for the application and environmental conditions intended.

14.2 **Failure Criteria:** Failure criteria shall consist of any of the following modes:
a) Functional failure.
b) Parameter limit failure.
c) Intermittent faults due to the package pins, or the interconnect system, from the pins to the die surface shall be regarded as failures.
d) Transitory faults attributable to the *device* shall be regarded as failures.

14.3 **Corrective Action:** If failures are detected in the reliability processes, the *supplier shall* investigate, determine root cause and take appropriate actions to achieve conformity to this *specification* or the *supplier's* internal requirements whichever is the most stringent.

14.4 **Warranty:** The reliability requirements in this *specification* apply to the general population of *devices* supplied. The warranty period and terms and conditions of sale for failure of individual *devices* within any warranty are not covered by this *specification*.

14.5 **Suspension of Certification:** The *user* reserves the right to apply accelerated life test and to accumulate life test data on any *device*, starting with the life test performed for qualification. If the reliability data accumulated shows a *device* does not meet the specified requirement in Table 4, certification may be suspended or revoked.

Table 4 – Operating Life Failure Rates

Operating Life Failure Rates @ Tamb 55 °C & 60 %UCL	Device Complexity	FIT
If the *supplier* has provided other figures during registration then those figures apply. This information will be considered proprietary and confidential to the STACK Members.	Discrete transistors	5
	<500 transistors	8
	<5K	25
	<50K	30
	<1M	100
	<10M	200
	<100M	200

14.6 **Single Event Effects (SEE):** Soft single bit error rate for DRAM and SRAM are shown in Test TC28 (SER). SEE data *shall* be made *available* upon request.

15. PRODUCT MONITOR

15.1 **Monitor Program:**
a) The *supplier shall* have a continuous monitor program to demonstrate that the requirements of this *specification* are met, on an ongoing basis, for each manufacturing operation or product process.
b) Statistical Process Control: The *supplier shall* control wafer production, assembly process and final test using statistical analysis. When anomalies are observed, parametric and yield data from probe and final tests *shall* be analyzed against in-line or electrical process control data. The root cause of the deviation shall be determined and the consequent corrective actions implemented.

c) Table 5 shows the minimum test requirements for a conventional stress driven monitor. The use of a Failure Mechanism Driven approach to optimise reliability monitoring is encouraged. Ongoing qualification test data and accumulated reliability monitor test data *may* be assessed in a structured way to reduce reliability monitor testing when failure mechanisms are shown to be eliminated by process controls and to increase testing or introduce new tests when failures are detected.

15.2 **Problem Notifications:** The *supplier shall* have a process to notify the *users* and distributors in cases where failures were detected and where the possibility of failed parts may have been shipped or may be in the process of being shipped to the *user*.
NOTE This is usually part of the *PCN* system as described in Section 6 with JESD46 as a guide.

15.3 **Data Reporting:** Reliability monitor data accumulated over the preceding two full quarters *shall* be *available*, at one month's notice.

15.4 **Samples:**
a) Appropriate sample sizes shall be selected.
b) Samples shall be randomly selected from representative package and process family *devices.*
c) All package types and all process families, but not necessarily all package/process combinations, *shall* be monitored.
d) Package tests shall use the largest die size the package is designed to carry that is currently in production. Custom ASIC qualification die may be used, see similarity assessment (Paragraph 13.10).
e) Sample lots will be added to the monitor at intervals appropriate for each test.

15.5 **Production Maturity Factors:** The FIT rates in Table 4 represent *devices* in mature production. Maturity factors (MF) may be used to multiply the values in Table 4.

Production time (months)	0 – 12	12 – 24	24+
Maturity factor (MF)	4	2	1

15.6 **Device Dissipation:** Where the *device* dissipation in the oven is significantly less than in normal operation, this shall be taken into account in FIT rate calculations.

15.7 **Corrective Action:** Failure to meet the limits in Table 5 or the *supplier's* internal limits, whichever is the most stringent, *shall* trigger appropriate corrective action by the *supplier.*

15.8 **Suspension of Certification:** Failure to meet the limits in Table 5 may lead to certification being suspended or revoked.

15.9 **Accumulated Test Data:**
a) Failure rates and levels may be a rolling average with data accumulation period appropriate to the production quantity level.

b) For HTOL test, the minimum total sample size (SS) required over the data accumulation period may be calculated using: $SS = \frac{\mathbf{Chi^2\ (B,c)\times 10^9}}{\mathbf{2\times FITS\times A\ \times t}}$

where
Chi^2 (60 %,0) = 1.83 FITS = see Table 4 A = A_T x A_V (see TC15)
Chi^2 (60 %,1) = 4.04 c = number of failures t = time under bias in oven
Chi^2 (60 %,2) = 6.21 B = upper confidence limit

Table 5 – Product Monitor Tests

Test Codes	Title	Max Failure	Notes
HTOL	Early life	Note 4	1, 2
HTOL	Long term life	Note 5	2, 6
NVL	Non-volatile memory operating life	0,5 %	3
TC	Temperature cycling	0,5 %	3
PC + THB or HAST	Preconditioned 85/85 or HAST (Plastic pkg. only)	0,5 %	3

Notes to Table 5:
1. Duration up to 168 h
2. Failure rate calculated as shown in Test HTOL.
3. Failure levels are actual number of failures divided by the quantity tested.
4. Early life FIT rate = 2 x Table 4 value x prod. Maturity factor (Paragraph 15.5).
5. Long term life FIT rate = 1 x Table 4 value x prod. Maturity factor.
6. HTOL on devices may be substituted by appropriate Wafer Level Reliability i.e. Testing at the wafer level

16. ENVIRONMENTAL, HEALTH AND SAFETY (EHS)

16.1 **EHS Compliance:** The *supplier shall* be expected to comply with all applicable national, regional, state and local laws and regulations governing environment, health and safety. *Supplier* registration to industry recognized EHS standards, such as ISO 14001, RC14001, or EMAS, is encouraged, but not mandatory.

16.2 **Device Handling:** *Devices should* not produce any toxic effects to personnel as a result of handling, storage or disposal, or when operated according to the *supplier's data sheet*.

16.3 **Device Materials:** Materials used in the manufacture of *devices should* be non-flammable, and shall not emit harmful levels of toxic materials as a result due to electrical overload or fault within the *device*.

17. SHIPMENT PACKAGING

17.1 **General:**

17.1.1 Electrostatic properties: Electrostatic properties shall be as specified after conditioning of 48 h at 23 °C ± 3 °C and 12 %RH ± 3 %. Any appropriate test method *may* be used, examples are contained in EIA 541. This test requirement *may* be met by a certificate of conformance from the material *supplier*.

17.1.2 ESD protection: All *integrated circuits* and some *discrete semiconductor* devices are considered to be static sensitive. All sensitive *devices* must be supplied in suitable protective packaging with electrostatic properties meeting the requirements of EIA 541 unless otherwise specified in this section.

17.1.3 Specification compliance after shipment: The method of packing for land, sea or air transportation *shall* adequately protect the *device* from being degraded in any way during transit.

17.1.4 Device orientation: *Devices shall* all have the same orientation within a *magazine*.

17.1.5 User instructions: Any special handling requirements or precautions (e.g.: placing of desiccants; resealing of containers; maximum number of 24 h 125 °C bake cycles allowable) which must be observed for storage or reshipment shall be stated on the packing and, where necessary, supporting documentation *shall* be supplied with each *inner box*.

17.1.6 Electrostatic shield: The *inner box* or *magazine* must contain an electrostatic shield of surface resistivity less than 10^6 ohms/square.

17.1.7 Magazine surface resistivity: Packing material in direct contact with the *device* pins *shall* have a surface resistivity less than 10^{12} ohms/square.

17.1.8 Inner box surface characteristics: All surfaces of the *inner box* other than an electrostatic shield *shall* meet the following:

Surface resistivity:	10^5 to 10^{12} ohms/square.
Charge decay in 2 s:	5 kv to less than 100 v.
Triboelectric charge:	Not to exceed 100 v.

17.2 **Magazine Reuse:**

a) Tubes, trays or other *magazines*, which depend for their electrostatic properties on surface coatings, shall be limited to a defined number of load/unload cycles. The specified surface resistivity shall be met after the defined number of cycles and data *shall* be *available* to justify the limit chosen. Coated *magazines* may be "reset" to zero load cycles by a suitable recycling process, which includes recoating.

b) *Magazines* that utilize bulk material properties may be reused.

17.3 **Tubes:**

17.3.1 Cushioning material: Ceramic *devices* packaged in tubes *shall* have an adequate amount of cushioning material to ensure that the *devices* are not damaged as a result of movement within the tubes.

17.3.2 Partial tubes: Full tubes shall be shipped with a maximum of one partly-filled tube per *inner box.*

17.3.3 Marking access: The material of the tube shall be transparent or contain a slot to allow inspection of top markings.

17.3.4 Opening: Tubes *shall* be openable at either end unless otherwise specified to meet unique customer applications.

17.4 **Trays:**

17.4.1 For *devices* with a moisture sensitivity classification according to J-STD-020 of 4 or higher, the tray *shall* have a bake capability of 125 °C min.

17.4.2 Bake temperature limit to be marked on tray or tray marked heatproof.

17.4.3 No more than 10 full trays to be stacked in height, plus 1 partial tray with one further tray as a cover.

18. LABELS

18.1 **General:**

18.1.1 Human readable content: The content shown for each label in this section *shall* be available in human readable form on the outside of the relevant package.

18.1.2 Machine readable content: Bar codes for those items specified shall be included in 3 of 9 code (bar code 39) per EIA556 or equivalent compatible standard.

18.1.3 Warning notices: Any necessary warning notices or symbols to ensure the safety of the contents shall be included as appropriate.

18.2 **Label Content:**

Dry pack label:		**Bar code**
a)	Date of sealing and sealed life or expiration date.	
b)	Time and storage condition limits after opening.	
c)	Bake conditions if usage conditions after opening are violated.	
d)	Moisture sensitivity classification per J-STD-020 or per *suppliers* own classification provided a cross reference is provided at registration.	
Outer box label: This label is typically implemented as a shipping note or packing list attached to the *outer box*. For security reasons, items d), e) & f) can be omitted with the agreement of the *user*.		
a)	Delivery address.	
b)	Purchase Order number.	*
c)	*User* part number.	*
d)	*Supplier device* type number.	*
e)	The *supplier's* name.	
f)	Quantities enclosed of each *device* type.	*
Inner box label:		
a)	*Supplier device* type number.	*
b)	*User* part number. (preferred but not mandatory)	*
c)	Purchase order number. (preferred but not mandatory)	*
d)	Quantity of *devices*.	*
e)	Date code.	*
f)	Lot number.	*
g)	Assembly location. (preferred but not mandatory)	
h)	Test location. (preferred but not mandatory)	

19. TEST CODE INFORMATION (For Reference only – See 1.2, 1.5, 2.1 and 4.3 herein).

TC1 – AUTOCLAVE (AC):
JEDEC JESD22-A102 Condition C for plastic packages only.
Solder preconditioning for non-hermetic SMD per test TC26 (PC).

NOTE Autoclave, whether biased or unbiased, is sometimes used for testing plastic packaged *devices*; the test may be a valid quality test but is a non-valid reliability test because of no known reliability data. Instead HAST, JEDEC JESD22-A118 Condition A, which is non-saturating and non-condensing, is the proven and preferred method for valid and known acceleration of ageing of electronics in humid environments

TC2 – BOND STRENGTH, INTERNAL (BS):
Minimum bond strength as specified in JESD22-B116 for ball shear testing or MIL-STD-883, Method 2011, Test condition D for wire bond pull testing.
Recording of failure categories is not required.
Plastic packages shall be tested before encapsulation.

TC3 – DIE SHEAR STRENGTH (DS):
MIL-STD-883, Method 2019.
Plastic packages shall be tested before encapsulation.
Alternative test methods are:
MIL-STD-883 Method 2027 Stud pull test (IC's)
MIL-STD-750 Method 2017 Die attach integrity test (discretes)

TC4 – ELECTROMIGRATION (EM):
The *supplier* shall perform appropriate testing to characterize the metallization system using JP001.01 and/or JEP119.
Details of test methods, results and the capability life demonstrated, for <0,1 % failures at worst case operating temperature, shall be *available* on request.
The requirement to perform electromigration testing is not limited to sub-micron technologies. Larger geometries are subject to electromigration wear out mechanisms.
Characterization data may be for the metallization and contact process as a whole, using accelerated current and temperature testing of test structures on the wafer rather than individual *device* types. Acceleration factors must be justified by experimental data.

TC5 – ELECTROSTATIC DISCHARGE (ESD):
Human body model
a) JESD22-A114.
b) The ESD withstanding voltage to be determined and be *available*.
c) ESD classification to be recorded in the Qualification Report.
Similarity: Sample testing among groups of similar pins is acceptable. The similarity basis shall be stated in the qualification report. *Users* reserve the right to test any pin-to-pin combination and to reject on failure.
Suppliers holding current IECQ Certification for compliance with IEC 61340-5-1 shall be deemed to have satisfied this requirement.

TC6 – ELECTRICAL TEST (ET):
Qualification electrical test
Electrical test is performed at the worst still air ambient temperature in the range of T_{op}min to T_{op}max. The *device* must be stabilized at the test temperature. If the test is carried out at a temperature which is not the worst case then full guard banding allowance shall be made.
The test shall include:
a) DC test to datasheet.
b) AC test to datasheet or correlated DC testing to guarantee the AC parameters.

c) Special functional tests where applicable, e.g. pattern sensitivity etc.
d) Functional verification.
e) Fault coverage targets for stuck at '1' & '0' *should* typically exceed 95 % or be as notified during registration.

Population Parameter Drift:
Where parameter drift assessment is specified in HTOL and HCI tests, a sample of >10 d*evices* shall pass Electrical Test both before and after endurance testing and results of main parameters shall be datalogged.
a) Individual *devices* are not required to be serialized.
b) Adequate parameter stability shall be confirmed.
c) Statistical measures of population drift shall be reported. The drift of the population mean for any parameter shall be less than 10 % of the initial population mean.
d) Functional failures may be excluded from calculation of mean values.

TC7 – ELECTRICAL DISTRIBUTIONS (ED):
Purpose: *Suppliers* to verify the data on specified electrical variables parameters on *devices* to be qualified per *data sheet* limits, and assess the *device's* capability to function within the *data sheet* limits over time and application environment (e.g. operating temperature range, voltage, input/output levels, etc.) in accordance with JESD86.
Input/output capacitance: shall be one of the parameters evaluated for new process/design qualifications using MIL-STD-883 Method 3012 or JESD6. The *device* shall be biased at nominal operating voltage. Capacitance measurements shall be made at all logic levels for digital *devices* and normal biased condition for analog *devices.*

TC8 – FLAMMABILITY (FL):
UL94. Applicable only to plastic devices.
The bulk material test is mandatory but the *supplier* may meet this test requirement by using material manufacturers test data. If bulk material is not available, IEC 60695-2-2 needle flame is a suitable method for tests on individual *devices*.

TC9 – HOT CARRIER INJECTION (HCI):
Applicable to sub-micron MOS technologies.
The *supplier* shall perform appropriate testing to evaluate long term intrinsic failure mechanisms for device/design related charge injection.
Details of test methods, results and the capability life demonstrated, for <0,1 % failures, shall be *available*.
Examples of appropriate methods are:
The DC over voltage stress method of JP001.01 or test under the following conditions:

Absolute max Vcc, for DRAM.	Maximum Vcc for other devices.
Duration 1 000 hours.	
Dynamic operation.	End point: Electrical Test-ET Population parameter drift.

TC10 – HERMETICITY (HE):
Not applicable to non-hermetic packages.
JESD22-A109 or MIL-STD-883, Method 1014 or MIL-STD-750 Method 1071

TC11 – HIGH TEMPERATURE BAKE (HTB):
JESD22-A103
Condition B for 1 000 hours or Condition C for 500 hours for plastic packages.
Condition E for 10 hours or Condition D for 72 hours for ceramic packaged devices. Examines device metal/contact inter diffusion robustness.