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ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

IPC-6012A
with Amendment 1

Qualification and Performance Specification for Rigid Printed Boards

IPC-6012A
with Amendment 1
July 2000

A standard developed by IPC

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

QUALIFICATION AND PERFORMANCE SPECIFICATION FOR RIGID PRINTED BOARDS

FOREWORD

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Draft PAS	**Report on voting**
91/210/PAS	91/236/RVD

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IPC-6012A with Amendment 1

Qualification and Performance Specification for Rigid Printed Boards

Developed by the Rigid Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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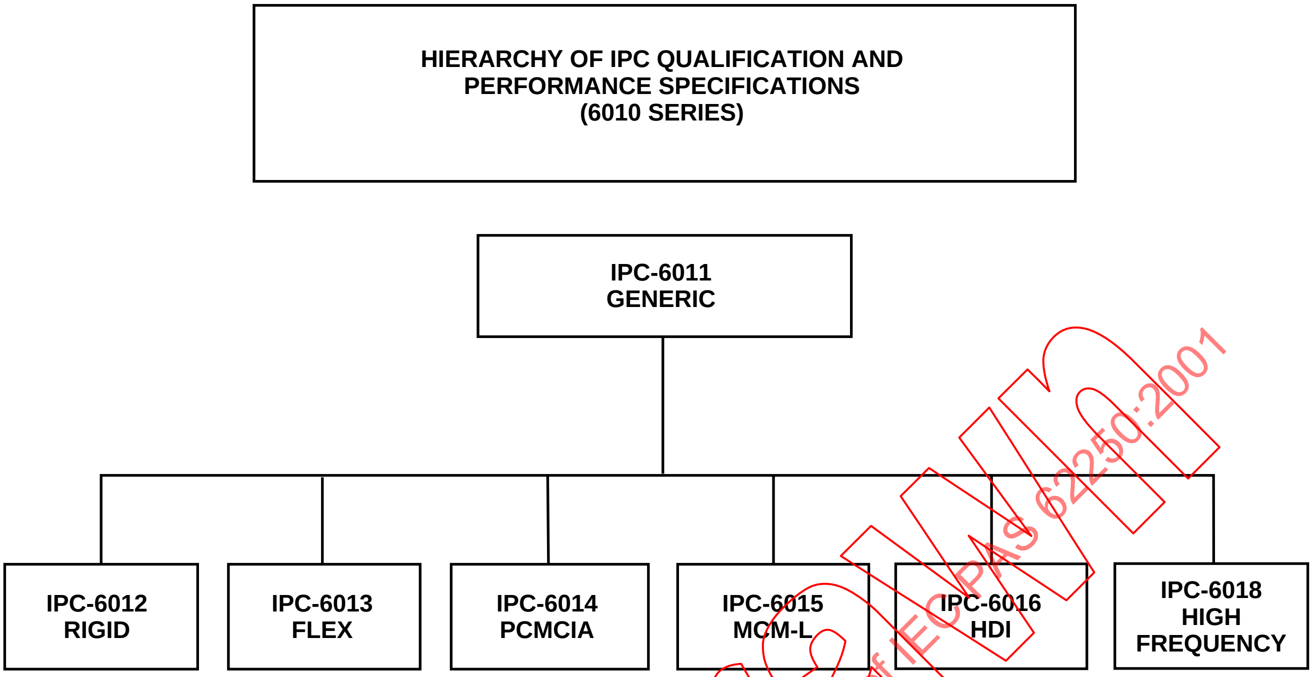

FOREWORD

This specification is intended to provide information on the detailed performance criteria of rigid printed boards. It supersedes IPC-RB-276 and IPC-6012 and was developed as a revision to those documents. The information contained herein is also intended to supplement the generic requirements identified in IPC-6011. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010).

Included in the set is the generic information, which is contained in the first document of the set. The generic specification is supplemented by one or multiple performance documents, each of which provide a specific focus on one aspect of the topic or the technology selected.

Failure to have all information available prior to building a board may result in a conflict in terms of acceptability.

As technology changes, a performance specification will be updated, or new focus specifications will be added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Rigid Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Table of Contents

Figures

Tables

Qualification and Performance Specification for Rigid Printed Boards

1 SCOPE

1.1 Scope This specification covers qualification and performance of rigid printed boards. The printed board may be single-sided, double-sided, with or without plated-through holes, multilayer with plated-through holes, multilayer with or without buried/blind vias, and metal core boards.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of rigid printed boards.

1.3 Performance Classification and Type

1.3.1 Classification This specification recognizes that rigid printed boards will be subject to variations in performance requirements based on end-use. The printed boards are classified by a Performance Class of 1, 2 or 3. Performance classes are defined in IPC-6011, Generic Performance Specification for Printed Boards.

1.3.2 Board Type Printed boards without plated-through holes (Type 1) and with plated-through holes (Types 2-6) are classified as follows:

Type 1—Single-Sided Board
Type 2—Double-Sided Board
Type 3—Multilayer board without blind or buried vias
Type 4—Multilayer board with blind and/or buried vias
Type 5—Multilayer metal core board without blind or buried vias
Type 6—Multilayer metal core board with blind and/or buried vias

1.3.3 Selection for Procurement For procurement purposes, performance class **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that he can fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is shown in IPC-D-325.

1.3.3.1 Selection (Default) The procurement documentation should specify the requirements that can be selected within this specification; however, in the event selections are not made in the documentation, Table 1-1 **shall** apply.

1.3.4 Material, Plating Process and Final Finish

1.3.4.1 Laminate Material Laminate material is identified by numbers and/or letters, classes, types as specified by the appropriate specification listed in the procurement documentation.

Table 1-1 Default Requirements

Category	Default Selection
Performance Class	Class 2
Material	Epoxy-Glass Laminate
Final Finish	Finish X (Electrodeposited tin-lead, fused or solder coated)
Minimum Starting Foil	1/2 oz. for all internal and external layers except Type 1 which **shall** start with 1 oz.
Copper Foil Type	Electrodeposited
Hole Diameter Tolerance Plated, components Plated, via only Unplated	 (±) 100 µm [0.0040 in] (+) 80 µm [0.0031 in], (-) no requirement, (may be totally or partially plugged) (±) 80 µm [0.0031 in]
Conductor Width tol.	Class 2 requirements per para. 3.5.1
Conductor Spacing tol.	Class 2 requirements per para. 3.5.2
Dielectric Separation	90 µm [0.0035 in] minimum
Lateral Conductor Spacing	100 µm [0.0040 in] minimum
Marking Ink	Contrasting color, nonconductive
Solder Resist	Not applied, if not specified
Solder Resist, specified	Class T of IPC-SM-840 if class not specified
Solderability Test	Category 2 of J-STD-003
Test Voltage, Insulation Resistance	40 Volts
Qualification not specified	See IPC-6011

1.3.4.2 Plating Process The copper plating process which is used to provide the main conductor in the holes is identified by one number as follows:

1 Acid copper electroplating only
2 Pyrophosphate copper electroplating only
3 Acid and/or pyrophosphate copper electroplating
4 Additive/electroless copper

1.3.4.3 Final Finish The final finish can be but is not limited to one of the finishes specified below or a combination of several platings and is dependent on assembly processes and end-use. Thickness, where required, **shall** be specified in the procurement documentation unless listed in Table 3-2. Coating thickness may be exempted in Table 3-2 (i.e., tin-lead plate or solder coating). Designators for final finish are as follows:

S	Solder Coating	(Table 3-2)
T	Electrodeposited Tin-Lead, (fused)	(Table 3-2)
X	Either Type S or T	(Table 3-2)
TLU	Electrodeposit Tin-Lead (unfused)	(Table 3-2)
G	Gold Electroplate for Edge Board Connectors	(Table 3-2)
GS	Gold Electroplate for Areas to be Soldered	(Table 3-2)
N	Nickel for Edge Board Connectors	(Table 3-2)
NB	Nickel as a Barrier to Copper-Tin Diffusion	(Table 3-2)
OSP	Organic Solderability Protector (tarnish and solderability protection during storage and assembly processes)	(Table 3-2)
C	Bare Copper	(Table 3-2)
SMOBC	Solder Mask over Bare Copper	
EN	Electroless Nickel	
EG	Electroless Gold	
IG	Immersion Gold	
IS	Immersion Silver	
IT	Immersion Tin	
TN	Tin-Nickel	
R	Rhodium	
P	Palladium	
TP	Tin Plating	
Y	Other	

2 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein. If a conflict of requirements exists between IPC-6012 and the listed applicable documents, IPC-6012 **shall** take precedence.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-DD-135 Qualification for Deposited Organic Interlayer Dielectric Materials for Multichip Modules

IPC-CF-148 Resin Coated Metal for Printed Boards

IPC-CF-152 Composite Material Specifications for Printed Wiring Boards

IPC-FC-232 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films

IPC-D-325 Documentation Requirements for Printed Boards, Assemblies, and Support Drawings

IPC-A-600 Acceptability of Printed Boards

IPC-AI-642 User Guideline for Automated Inspection of Artwork, Innerlayer and Unpopulated PWBs

IPC-TM-650 Test Methods Manual[2]

2.1.1D	03/98	Microsectioning
2.1.1.2	07/93	Microsectioning, Semi or Automatic Technique Microsection Equipment (Alternate)
2.3.15C	08/92	Purity, Copper Foil or Plating
2.3.25B	08/97	Detection and Measurement of Ionizable Surfact Contaminants
2.3.38B	08/97	Surface Organic Contaminant Detection Test
2.3.39B	08/97	Surface Organic Contaminant Identification Test (Infrared Analytical Method)
2.4.1D	08/97	Adhesion, Tape Testing
2.4.18.1	08/97	Tensile Strength and Elongation, In-House Plating
2.4.21D	08/97	Land Bond Strength, Unsupported Component Hole
2.4.22C	06/99	Bow and Twist
2.4.28.1C	03/98	Adhesion, Solder Resist (Mask), Tape Test Method
2.4.36B	08/97	Rework Simulation, Plated-Through Holes for Leaded Components
2.4.41.2	08/97	Coefficient of Thermal Expansion, Strain Gage Method
2.5.5.7	11/92	Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR
2.5.7C	08/97	Dielectric Withstand Voltage, PWB
2.6.1E	08/97	Fungus Resistance, Printed Wiring Materials
2.6.3E	08/97	Moisture and Insulation Resistance, Rigid Boards
2.6.4A	08/97	Outgassing, Printed Boards
2.6.5C	08/97	Physical Shock, Multilayer Printed Wiring

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[1] IPC, 2215 Sanders Road, Northbrook, IL 60062-6135.

[2] Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

2.6.7.2A	08/97	Thermal Shock, Continuity and Microsection, Printed Boards
2.6.8D	03/98	Thermal Stress, Plated-Through Holes
2.6.9A	08/97	Vibration, Rigid Printed Wiring

IPC-ET-652 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-QL-653 Certification of Facilities that Inspect/Test Printed Wiring Boards, Components and Materials

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-2221 Generic Standard on Printed Board Design

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures

IPC-7721 Repair and Modification of Printed Boards and Electronic Assemblies

IPC-100002 Universal Drilling and Profile Master Drawing

IPC-100047 Composite Test Pattern Basic Dimension Drawing-Ten Layer

IPC-100101 Master Drawing, Capability Test Board (Single Sided)

IPC-100102 Master Drawing, Capability Test Board (Double Sided)

IPC-100103 Master Drawing, Capability Test Board (Ten Layer Multilayer Board without Blind or Buried Vias)

2.2 Joint Industry Standards[1]

J-STD-003 Solderability Tests for Printed Boards

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

2.3 Federal[3]

QQ-A-250 Aluminum Alloy, Plate and Sheet

QQ-N-290 Nickel Plating

QQ-S-635 Steel

2.4 Other Publications

2.4.1 American Society for Testing and Materials[4]

ASTM B-152 Standard Specification for Copper Sheet, Strip, Plate and Rolled Bar

ASTM B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses

ASTM B-579 Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

2.4.2 Underwriters Lab[5]

UL 94 Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

2.4.3 National Electrical Manufacturers Association[6]

NEMA LI-1 Industrial Laminate Thermosetting Product

2.4.4 American Society for Quality Control[7]

H0862 Zero Acceptance Number Sampling Plans

3 REQUIREMENTS

3.1 General Printed boards furnished under this specification **shall** meet or exceed the requirements of IPC-6011 and the specific performance class as required by the procurement documentation. Descriptions and purposes of test coupons are documented in IPC-2221.

3.2 Materials Used in this Specification

3.2.1 Laminates and Bonding Material for Multilayer Boards Rigid metal clad laminates, rigid unclad laminates and bonding material (prepreg) should be selected from IPC-4101, IPC-FC-232, or NEMA LI-1. The specification sheet number, metal cladding type and metal clad thickness (weight) **shall** be as specified in the procurement

---

[3] Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.
[4] ASTM, 100 Barr Harbor Drive, West Conshohocken, PA 19428.
[5] Underwriters Lab, 333 Pfingsten Road, Northbrook, IL 60062.
[6] NEMA, 1300 North 17th Street, Suite 1847, Rosslyn, VA 22209.
[7] ASQC, 230 West Wells Street, Milwaukee, WI 53203.

documentation. When specific requirements such as the flammability requirements shown in UL 94 for laminate and bonding materials are required, it is necessary to specify those requirements in material procurement documents.

3.2.2 External Bonding Materials The material used to adhere external heat sinks or stiffeners to the printed board **shall** be selected from IPC-4101, IPC-FC-232 or as specified in the procurement documentation.

3.2.3 Other Dielectric Materials Photoimageable dielectrics should be selected from IPC-DD-135 and specified in the procurement documentation. Other dielectric materials may be specified in the procurement documentation.

3.2.4 Metal Foils Copper foil **shall** be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment and foil profile should be specified on the master drawing if critical to the function of the printed board. Resin coated copper foil **shall** be in accordance with IPC-CF-148. Resistive metal foil **shall** be in accordance with the applicable specification and the procurement documents.

3.2.5 Metal Core The metal core substrate **shall** be specified on the master drawing as shown in Table 3-1.

Table 3-1 Metal Core Substrate

Material	Specification	Alloy
Aluminum	QQ-A-250	As specified
Steel	QQ-S-635	As specified
Copper	ASTM-B-152 or IPC-4562	As specified
Copper-Invar-Copper	IPC-CF-152	As specified
Copper-Moly-Copper	IPC-CF-152	As specified
Other	As specified	

3.2.6 Metallic Platings and Coatings Thickness of the plating/coating **shall** be in accordance with Table 3-2. The copper plating thickness on the surface, in plated-through holes, via holes and in blind and buried vias **shall** be as specified in Table 3-2. Thickness of platings for a specific use is shown in Table 3-2. Final finishes selected from those listed in 1.3.4.3 or combinations required **shall** specify plating thickness except for fused tin-lead plating or solder coating which requires visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges; conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.5.4.6.

Note: The Category of solderability testing **shall** be specified by the user per J-STD-003; however, in the event it is not specified the supplier **shall** test to Category 2 (steam aging is not required).

3.2.6.1 Electroless Depositions and Conductive Coatings Electroless depositions and conductive coatings **shall** be sufficient for subsequent plating process and may be either electroless metal, vacuum deposited metal, or metallic or nonmetallic conductive coatings.

3.2.6.2 Additive Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification.

3.2.6.3 Tin-Lead Tin-lead plating **shall** meet the composition (50-70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected wherein the thickness specified in Table 3-2 applies.

3.2.6.4 Solder Coating The solder used for solder coating **shall** be Sn60A, Sn60C, Pb40A, Pb36A, Pb36B, Pb36C, Sn63A, Sn63C or Pb37A per J-STD-006.

3.2.6.5 Nickel Nickel plating **shall** be in accordance with QQ-N-290 Class 2, except the thickness **shall** be in accordance with Table 3-2.

3.2.6.6 Gold Plating Electrodeposited gold plating **shall** be in accordance with ASTM-B-488. Class and Type **shall** be specified in the procurement documentation. For Class 3 boards, gold plating **shall** be Type 1 or 3, Class 1.25.

Gold plating thickness on areas to be wire bonded **shall** be as specified in the procurement documentation (see IPC-6015, for example).

3.2.6.7 Other Other depositions such as bare copper, electroless nickel, immersion gold, immersion silver, palladium, rhodium, tin, 95Sn/5Pb etc. may be used provided they are specified in the procurement documentation.

3.2.6.8 Electrodeposited Copper When specified, electrodeposited copper platings **shall** meet the following criteria. Frequency of testing shall be determined by the manufacturer to ensure compliance.

a) When tested as specified in IPC-TM-650, Method 2.3.15, the purity of copper **shall** be no less than 99.50% for either pyrophosphate or acid copper.

b) When tested as specified in IPC-TM-650, Method 2.4.18.1, at ambient temperature using 50 - 100 µm [0.0020 in - 0.003937 in] thick samples, the tensil strength **shall** be no less than 36,000 PSI [248 MPa] and the elongation **shall** be no less than 12%.

3.2.7 Organic Solderability Preservative (OSP) OSPs are anti-tarnish and solderability protectors applied to bare copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating

Table 3-2 Final Finish, Surface[1] Plating Coating Requirements

Finish	Class 1	Class 2	Class 3
Gold (min) for edge-board connectors and areas not to be soldered	0.8 µm [0.00003 in]	0.8 µm [0.00003 in]	1.25 µm [0.00004921 in]
Gold (max) on areas to be soldered	0.8 µm [0.00003 in]	0.8 µm [0.00003 in]	0.8 µm [0.00003 in]
Nickel (min) for edgeboard connectors	2.0 µm [0.00008 in]	2.5 µm [0.00010 in]	2.5 µm [0.00010 in]
Nickel (min)[2] barrier to prevent formation of copper-tin compounds	1.0 µm [0.00004 in]	1.3 µm [0.00005 in]	1.3 µm [0.00005 in]
Unfused tin-lead (min)	8.0 µm [0.0003 in]	8.0 µm [0.0003 in]	8.0 µm [0.0003 in]
Fused tin-lead or Solder Coat	Coverage and Solderable	Coverage and Solderable	Coverage and Solderable
Solder Coat over Bare Copper	Coverage and Solderable	Coverage and Solderable	Coverage and Solderable
Organic Solderability Preservative	Solderable	Solderable	Solderable
Bare Copper	None	None	None
Surface and Holes			
Copper[1] (min. avg.)	20 µm [0.00079 in]	20 µm [0.00079 in]	25 µm [0.00098 in]
Min. thin areas[3]	18 µm [0.00071 in]	18 µm [0.00071 in]	20 µm [0.00079 in]
Blind Vias			
Copper (min. avg.)	20 µm [0.00079 in]	20 µm [0.00079 in]	25 µm [0.00098 in]
Min. thin area	18 µm [0.00071 in]	18 µm [0.00071 in]	20 µm [0.00079 in]
Low Aspect Ratio Blind Vias[4]			
Copper (min. avg.)	12 µm [0.00047 in]	12 µm [0.00047 in]	12 µm [0.00047 in]
Min. thin area	10 µm [0.00040 in]	10 µm [0.00040 in]	10 µm [0.00040 in]
Buried Vias			
Copper (min. avg.)	13 µm [0.00051 in]	15 µm [0.00060 in]	15 µm [0.00060 in]
Min. thin area	11 µm [0.00043 in]	13 µm [0.00051 in]	13 µm [0.00051 in]

[1] Copper plating thickness applies to surfaces and hole walls.

[2] Nickel platings used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

[3] For Class 3 boards having a drilled hole diameter < 0.35 mm [0.0138 in] and having an aspect ratio > 3.5:1, the minimum thin area copper plating in the hole **shall** be 25 µm [0.00098 in].

[4] Low Aspect Ratio Blind Vias refer to blind vias produced using a controlled depth mechanism (e.g., laser, mechanical, plasma or photo defined). All performance characteristics for plated holes, as defined in this document, **shall** be met.

storage, pre-assembly baking and sequential soldering processes impact solderability. Specific solderability retention requirement, if applicable, **shall** be specified in the procurement documentation.

3.2.8 Polymer Coating (Solder Resist) When permanent solder resist coating is specified, it **shall** be a polymer coating conforming to IPC-SM-840. (See requirements section on solder resist, 3.8.)

3.2.9 Fusing Fluids and Fluxes The composition of the fusing fluids and fluxes used in solder coating applications **shall** be capable of cleaning the tin-lead plating and bare copper to allow for a smooth adherent coating. The fusing fluid **shall** act as a heat transfer and distribution media to prevent damage to the bare laminate of the board.

Note: Fusing fluid compatibility should be confirmed with end users' cleanliness requirements due to the diverse interactions experienced at assembly soldering.

3.2.10 Marking Inks Marking inks **shall** be permanent, nonnutrient polymer inks, and **shall** be specified in the procurement documentation. Marking inks **shall** be applied to the board, or to a label applied to the board. Marking inks and labels must be capable of withstanding fluxes, cleaning solvents, soldering, cleaning and coating processes encountered in later manufacturing processes. If a conductive marking ink is used, the marking **shall** be treated as a conductive element on the board.

3.2.11 Hole Fill Insulation Material Electrical insulation material used for hole-fill for metal core printed boards **shall** be as specified in the procurement documentation.

3.2.12 Heatsink Planes, External Thickness and materials for construction of heatsink planes and insulation material **shall** be as specified in the procurement documentation.

3.3 Visual Examination Finished printed boards **shall** be examined in accordance with the following test method. They **shall** be of uniform quality and **shall** conform to 3.3.1 through 3.3.9.

Visual examination for applicable attributes **shall** be conducted at 1.75X (approx. 3 diopters); if the condition of a suspected defect is not apparent, it should be verified at progressively higher magnifications (up to 40X) to confirm that it is a defect. Dimensional requirements such as spacing or conductor width measurements require other magnifications and devices with reticles or scales in the instrument that allow accurate measurements of the specified dimensions. Other magnifications may be required by contract or specification.

3.3.1 Edges Nicks or haloing along the edge of the board, edge of cutouts and edges of nonplated-through holes are acceptable provided the penetration does not exceed 50% of the distance from the edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less. Edges **shall** be clean cut and without metallic burrs. Nonmetallic burrs are acceptable as long as they are not loose and/or do not affect fit and function. Panels which are scored or routed with a breakaway tab **shall** meet the depanelization requirements of the assembled board.

3.3.2 Laminate Imperfections Measling, crazing, blistering, delamination, and haloing **shall** be in accordance with IPC-A-600.

3.3.2.1 Foreign Inclusions Foreign inclusions **shall** be in accordance with IPC-A-600 with the exception that the inclusion has no maximum dimension.

3.3.2.2 Weave Exposure Weave exposure or exposed/disrupted fibers are acceptable for all Classes provided the imperfection does not reduce conductor spacing below the minimum. Refer to IPC-A-600 for more information.

3.3.2.3 Scratches, Dents, and Tool Marks Scratches, dents, and tool marks are acceptable provided they do not bridge conductors or expose/disrupt fibers greater than allowed in the paragraphs above and do not reduce the dielectric spacing below the minimum specified.

3.3.2.4 Surface Voids Surface voids are acceptable provided they do not: exceed 0.8 mm [0.0031 in] in the longest dimension; bridge conductors; or exceed 5% of the total board area.

3.3.2.5 Color Variations in Bond Enhancement Treatment Mottled appearance or color variation in bond enhancement treatment is acceptable. Random missing areas of treatment **shall not** exceed 10% of the total conductor surface area of the affected layer.

3.3.2.6 Pink Ring No evidence exists that pink ring affects functionality. The presence of pink ring may be considered an indicator of process or design variation but is not a cause for rejection. The focus of concern should be the quality of the lamination bond.

3.3.3 Plating and Coating Voids in the Hole Plating and coating voids **shall not** exceed that allowed by Table 3-3.

Table 3-3 Plating and Coating Voids Visual Examination

Material	Class 1	Class 2	Class 3
Copper	Three voids allowed per hole in not more than 10% of the holes	One void allowed per hole in not more than 5% of the holes	None
Finish Coating	Five voids allowed per hole in not more than 15% of the holes	Three voids allowed per hole in not more than 5% of the holes	One void allowed per hole in not more than 5% of the holes

Note 1: For class 2 product, copper voids **shall not** exceed 5% of the hole length. For class 1 product, copper voids **shall not** exceed 10% of the hole length. Voids **shall not** extend beyond 90° of the circumference.

Note 2: For class 2 and 3 product, finished coating voids **shall not** exceed 5% of the hole length. For class 1, finished coating voids **shall not** exceed 10% of the hole length. Voids **shall not** extend beyond 90° for class 1, 2 or 3.

3.3.4 Lifted Lands When visually examined in accordance with 3.3, the finished board **shall not** exhibit any lifted lands.

3.3.5 Marking Each individual board, each qualification board, and quality conformance test circuitry (as opposed to each individual test coupon) **shall** be marked in order to insure traceability between the boards/quality conformance test circuitry and the manufacturing history and to identify the supplier (logo, etc.). The marking **shall** be produced by the same process as used in producing the conductive pattern, or by use of a permanent fungistatic ink or paint (see 3.2.11), LASER marker or by vibrating pencil marking on a metallic area provided for marking purposes or a permanently attached label. Conductive markings, either etched copper or conductive ink (see 3.2.10) **shall** be considered as electrical elements of the circuit and **shall not** reduce the electrical spacing requirements. All markings **shall** be compatible with materials and parts, legible for all tests, and in no case affect board performance. Marking **shall not** cover areas of lands that are to be soldered. Refer to IPC-A-600 for legibility requirements. In addition to this marking, the use of bar code marking is permissible. When used, date code **shall** be formatted per the suppliers discretion in order to establish traceability as to when the manufacturing operations were performed.

3.3.6 Solderability Only those printed boards that require soldering in a subsequent assembly operation require solderability testing. Boards that do not require soldering do not require solderability testing and this **shall** be specified on the master drawing, as in the case where press-fit components are used. Boards to be used only for surface mount do not require hole solderability testing.

When required by the procurement documentation, accelerated aging for coating durability **shall** be in accordance with J-STD-003. The Category of durability **shall** be specified on the master drawing; however, if not specified, Category 2 **shall** be used. Test coupons or production boards to be tested **shall** be conditioned, if required, and evaluated for surface and hole solderability using J-STD-003.

When solderability testing is required, consideration should be given to board thickness and copper thickness. As both increase, the amount of time to properly wet the sides of the holes and the tops of the lands increases proportionately.

Note: Accelerated aging (steam aging) is intended for use on coatings of tin/lead, tin/lead solder or tin, but not other final finishes.

3.3.7 Plating Adhesion Printed boards **shall** be tested in accordance with the following procedure. The adhesion of the plating **shall** be tested in accordance with IPC-TM-650, Method 2.4.1, using a strip of pressure sensitive tape applied to the surface and removed by manual force applied perpendicular to the circuit pattern.

There **shall** be no evidence of any portion of the protective plating or the conductor pattern foil being removed, as shown by particles of the plating or pattern foil adhering to the tape. If overhanging metal (slivers) breaks off and adheres to the tape, it is evidence of overhang or slivers, but not of plating adhesion failure.

3.3.8 Edge Board Contact, Junction of Gold Plate to Solder Finish Exposed copper/plating overlap between the solder finish and gold plate **shall** meet the requirements of Table 3-4. The exposed copper/plating or gold overlap may exhibit a discolored or gray-black area which is acceptable. (See 3.5.4.3).

Table 3-4 Edge Board Contact Gap

	Max. Exposed Copper Gap	Max. Gold Overlap
Class 1	2.5 mm [0.0984 in]	2.5 mm [0.0984 in]
Class 2	1.25 mm [0.04921 in]	1.25 mm [0.04291 in]
Class 3	1.0 mm [0.031 in]	1.0 mm [0.031 in]

3.3.9 Workmanship Printed boards **shall** be processed in such a manner as to be uniform in quality and show no visual evidence of dirt, foreign matter, oil, fingerprints, tin/lead or solder smear transfer to the dielectric surface, flux residue and other contaminants that affect life, ability to assemble and serviceability. Visually dark appearances in nonplated holes, which are seen when a metallic or nonmetallic semiconductive coating is used, are not foreign material and do not affect life or function. Printed boards **shall** be free of defects in excess of those allowed in this specification. There **shall** be no evidence of any lifting or separation of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There **shall** be no loose plating slivers on the surface of the printed board.

3.4 Board Dimensional Requirements The board **shall** meet the dimensional requirements specified in the procurement documents. All dimensional characteristics such as board periphery, thickness, cutouts, slots, notches, and edge board contacts to connector key area **shall** be as specified in the procurement documentation.

Automated inspection technology is allowed (see IPC-AI-642).

3.4.1 Hole Size and Hole Pattern Accuracy The hole size tolerance and hole pattern accuracy **shall** be as specified in the procurement documentation. Nodules or rough plating in plated-through holes **shall not** reduce the hole diameter below the minimum limits defined in the procurement document.

3.4.2 Annular Ring and Breakout (Internal) The F coupon may be used to assess annular ring and breakout of internal lands by external visual inspection or radiographic (x-ray) techniques. If internal annular ring breakout is detected but the degree of breakout can not be determined, it **shall** be measured by horizontal microsection. The test coupon or production board used for the horizontal microsection **shall** be taken from the affected area and analyzed on the suspect layer(s). Requirements are shown in Table 3-5. Measurement for annular ring is from the inside of the drilled hole to the edge of the internal land as shown in Figure 3-1. Negative etchback is evaluated per 3.6.2.7. Buried vias are considered to be an external layer and are evaluated in process before multilayer lamination.

Internal registration may be assessed by nondestructive techniques such as patterns, probes and software which are configured to provide information on annular ring remaining and pattern skew. Prior to acceptance of the technique, microsectioning **shall** be used to verify correlation, and a calibration standard made for the probe technique which **shall** be used to periodically verify acceptability.

3.4.3 Annular Ring (External) The minimum external annular ring **shall** meet the requirements of Table 3-5. The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole, or unsupported hole, to the outer edge of the annular ring on the surface of the board. Plated-through holes identified as vias can have up to 90° breakout of the annular ring if it does not occur at the conductor and land intersection. (See Figure 3-2A and 3-2B).

Table 3-5 Minimum Internal and External Annular Ring

Characteristic	Class 1	Class 2	Class 3
Plated-through holes (see Figure 3-2A and 3-2B for land breakout and conductor width reduction at land)	180° breakout of hole from land is allowed when visually assessed[1]. For the external lands, the land/conductor junction is not reduced more than 30% of the minimum conductor width specified on the master drawing or the production master nominal.	90° breakout of hole from land is allowed when visually assessed[1]. For the external lands, the land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The conductor junction should never be less than 50 µm [0.0020 in] or the minimum line width, whichever is smaller.	The minimum external annular ring **shall not** be less than 50 µm [0.0020 in]. The minimum functional internal annular ring **shall not** be less than 25 µm [0.00098 in]. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.
Unsupported holes	No breakout at conductor junction.	No breakout allowed.	The minimum annular ring **shall not** be less than 150 µm [0.00591 in]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas.

[1] Minimum lateral spacing **shall** be maintained.

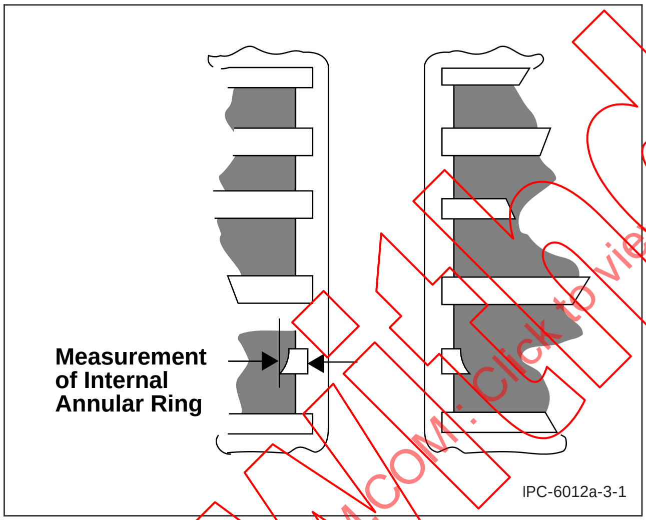


Figure 3-1 Annular Ring Measurement

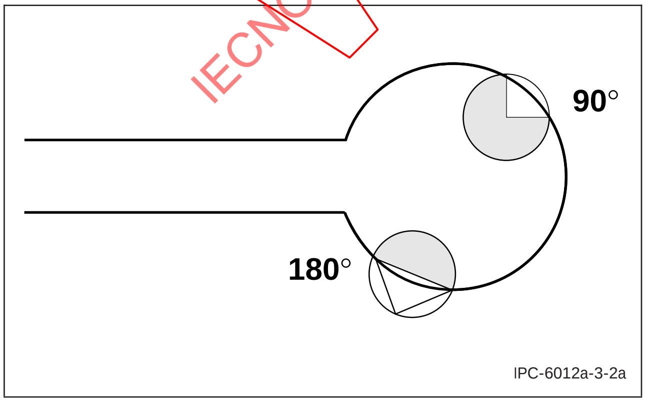


Figure 3-2A Breakout of 90° and 180°

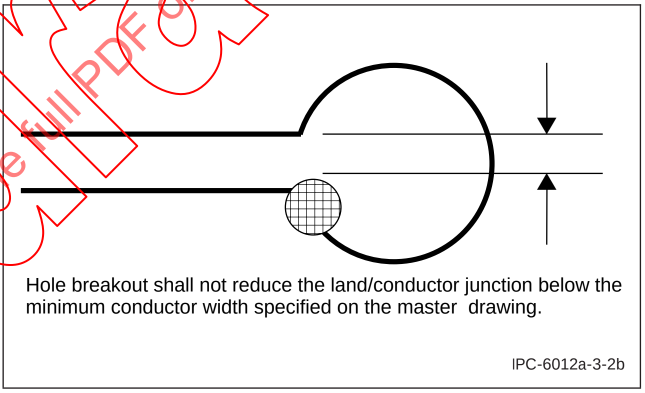


Figure 3-2B Conductor Width Reduction

3.4.4 Bow and Twist Unless otherwise specified in the procurement documentation, when designed in accordance with 5.2.4 of IPC-2221, the printed board **shall** have a maximum bow and twist of 0.75% for boards that use surface mount components and 1.5% for all other boards. Panels which contain multiple printed boards which are assembled on the panel and later separated **shall** be assessed in panel form.

Bow, twist, or any combination thereof, **shall** be determined by physical measurement and percentage calculation in accordance with IPC-TM-650, Method 2.4.22.

3.5 Conductor Definition All conductive areas on printed boards including conductors, lands and planes **shall** meet the visual and dimensional requirements of the following sections. The conductor pattern **shall** be as specified in the procurement documentation. Verification of dimensional attributes **shall** be performed in accordance with 3.3 and IPC-A-600. AOI inspection methods are allowed (see

Table 3-6 Plated-Through Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Copper voids	Three voids allowed per hole. Voids in the same plane are not allowed. No void **shall** be longer than 5% of board thickness. No circumferential voids allowed.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.
Plating folds/inclusions[2]	Must be enclosed	Must be enclosed	Must be enclosed
Burrs[2] and nodules[2]	Allowed if minimum hole diameter is met	Allowed if minimum hole diameter met	Allowed if minimum hole diameter met
Glass fiber protrusion	Allowed. See 3.6.2.10	Allowed. See 3.6.2.10	Allowed. See 3.6.2.10
Wicking	125 µm [0.00492 in] maximum	100 µm [0.00393 in] maximum	80 µm [0.00315 in] maximum
Innerlayer inclusions (inclusions at the interface between internal lands and through-hole plating)	Allowed on only one side of hole wall at each land location on 20% of available lands	None allowed	None allowed
Internal foil cracks[1]	"C" cracks allowed on only one side of hole provided it does not extend through foil thickness	None allowed	None allowed
External foil cracks[1] (type "A," "B" and "D" cracks)	"D" cracks not allowed. "A" and "B" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.
Barrel/Corner cracks[1] (type "E" and "F" cracks)	None allowed	None allowed	None allowed
Innerlayer separation (separation at the interface between internal lands and through-hole plating)	Allowed on only one side of hole wall at each land location on 20% of available lands	None allowed	None allowed
Separations along the vertical edge of the external land(s)	Allowed (see Figure 3-3) provided it does not extend beyond the vertical edge of the external copper foil		
Plating separation	Allowed at knee, maximum length 130 µm [0.00512 in]	None allowed	None allowed
Hole wall dielectric/ plated barrel separation	Acceptable provided dimensional and plating requirements are met	Acceptable provided dimensional and plating requirements are met	Acceptable provided dimensional and plating requirements are met
Lifted lands after thermal stress or rework simulation	Allowed provided the finished boards meet the visual criteria of 3.3.4		

[1] Copper crack definition: See Figure 3-4
"A" crack = A crack in the external foil
"B" crack = A crack that does not completely break plating (minimum plating remains)
"C" crack = A crack in the internal foil
"D" crack = A crack in the external foil and plating - complete break in foil and plating
"E" crack = A barrel crack in plating only
"F" crack = A corner crack in the plating only
[2] The minimum copper thickness in Table 3-2 must be met.

IPC-AI-642). Internal conductors are examined during internal layer processing prior to multilayer lamination.

3.5.1 Conductor Width and Thickness When not specified on the master drawing the minimum conductor width **shall** be 80% of the conductor pattern supplied in the procurement documentation. When not specified on the master drawing, the minimum conductor thickness **shall** be in accordance with 3.6.2.11 and 3.6.2.12.

3.5.2 Conductor Spacing The conductor spacing **shall** be within the tolerance specified on the master drawing. Minimum spacing between the conductor and the edge of the board **shall** be as specified on the master drawing. If minimum spacing is not specified, the allowed reduction in the nominal conductor spacings shown in the engineering documentation due to processing **shall** be 20% for Class 3 and 30% for Class 1 and 2 (minimum product spacing requirements as previously stated apply).

3.5.3 Conductor Imperfections The conductive pattern **shall** contain no cracks, splits or tears. The physical geometry of a conductor is defined by its width x thickness x length. Any combination of defects specified in 3.5.3.1 and 3.5.3.2 **shall not** reduce the equivalent cross sectional area (width x thickness) of the conductor by more than 20% of the minimum value (minimum thickness x minimum width) for Class 2 and 3, and 30% of the minimum value

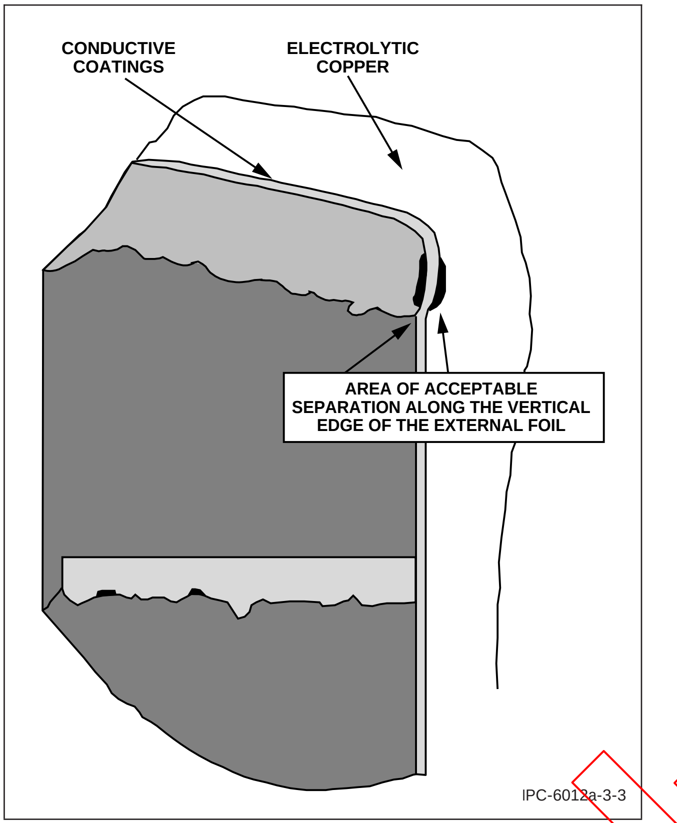


Figure 3-3 Separations at External Foil

for Class 1. The total combination of defect area lengths on a conductor **shall not** be greater than 10% of the conductor length or 25 mm [0.984 in] (for Class 1) or 13 mm [0.512 in] (for Class 2 or 3), whichever is less.

3.5.3.1 Conductor Width Reduction Allowable reduction of the minimum conductor width (specified or derived) due to isolated defects (i.e., edge roughness, nicks, pinholes and scratches) which exposes base material **shall not** exceed 20% of the minimum conductor width for Class 2 and 3, and 30% of the minimum conductor width for Class 1.

3.5.3.2 Conductor Thickness Reduction Allowable reduction of the minimum conductor thickness due to isolated defects (i.e., edge roughness, nicks, pinholes, depressions and scratches) **shall not** exceed 20% of the minimum conductor thickness for Class 2 and 3, and 30% of the minimum conductor thickness for Class 1.

3.5.4 Conductive Surfaces

3.5.4.1 Nicks and Pinholes in Ground or Voltage Planes Nicks and pinholes are acceptable in ground or voltage planes for Class 2 and 3 if they do not exceed 1.0 mm [0.0394 in] in their longest dimension and there are no more than four per side per 625 cm^2. For Class 1, the longest dimension **shall** be 1.5 mm [0.0591 in] with no more than six per side, per 625 cm^2.

3.5.4.2 Surface Mount Lands Defects such as nicks, dents, and pin holes along the edge of the land **shall not** exceed 20% of either the length or width of the land for Class 2 or Class 3 boards, or 30% for Class 1. Defects internal to the land **shall not** exceed 10% of the length or width of the land for Class 2 or Class 3 boards, or 20% for Class 1.

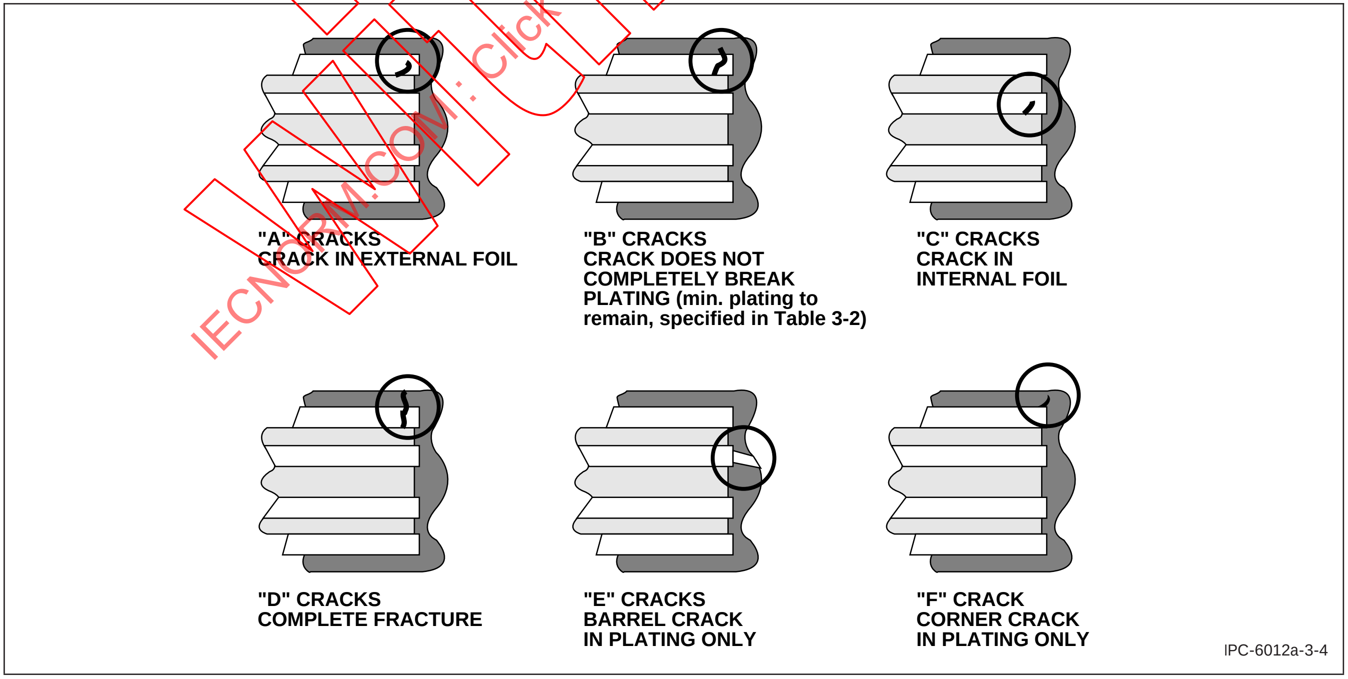


Figure 3-4 Crack Definition

3.5.4.3 Edge Board Connector Lands On gold or other noble metal plated edge board connector lands, except as noted below, the insertion or contact area **shall** be free of cuts or scratches that expose nickel or copper, solder splashes or tin-lead plating, and nodules or metal bumps that protrude above the surface. Pits, dents or depressions are acceptable if they do not exceed 0.15 mm [0.00591 in] in their longest dimension and there are not more than 3 per land and do not appear on more than 30% of the lands. The imperfection limits do not apply to a band 0.15 mm [0.00591 in] wide around the perimeter of the land including the insertion area.

3.5.4.4 Dewetting For tin, tin/lead reflowed, or solder coated surfaces, dewetting on conductors, areas of solder connection, and ground or voltage planes is allowed to the extent listed below:

a. Conductors and planes—permitted for all classes.

b. Individual areas of solder connection—Class 1–15%; Class 2–5%; Class 3–5%.

3.5.4.5 Nonwetting For tin, tin/lead reflowed or solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required.

3.5.4.6 Final Finish Coverage Final finish **shall** meet the solderability requirements of J-STD-003. Exposed copper on areas not to be soldered is permitted on 1% of the conductor surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor edges.

3.6 Structural Integrity Printed boards **shall** meet structural integrity requirements for thermally stressed (after solder float) evaluation test coupons specified in 3.6.2. Although the A and B coupons are assigned for this test, production boards may be used in lieu of the A/B coupons and are preferred for product that contains surface mount and vias or surface mount mixed with through-hole technology. Holes selected **shall** be equivalent to those specified for test coupons. The production boards and all other test coupons in the quality conformance test circuitry which contain plated-through holes **shall** be capable of meeting the requirements of this section. Structural integrity **shall** be used to evaluate test coupons or production boards from Type 2 through Type 6 boards by microsectioning techniques. Characteristics not applicable to Type 2 boards (i.e., requirements for innerlayer separations, innerlayer inclusions, and inner foil cracks) are not evaluated. Dimensional measurements that are only possible through the use of microsectioning techniques are also defined in this section. Blind and buried vias **shall** meet the requirements of plated-through holes.

The evaluation of all properties and requirements **shall** be performed on the thermally stressed test coupon and all requirements must be met; however, per supplier election, certain properties and conditions as defined in the following paragraph(s), which are not affected by thermal stressing, may be evaluated in a test coupon(s) that has not been thermally stressed.

a) When a supplier elects to evaluate the unstressed test coupon for the properties listed in (b), he may do so at any operation following the copper plating operation. If the board undergoes additional thermal excursions above the T_g (glass transition temperature) after copper plating, the unstressed test coupon being evaluated **shall** also be subjected to these thermal excursions.

b) The properties which are not affected by thermal stress are: copper voids, plating folds/inclusions, burrs and nodules, glass fiber protrusion, wicking, final coating plating voids, etchback, negative etchback, plating/coating thickness, internal and surface copper layer or foil thickness.

3.6.1 Thermal Stress Testing Test coupons or production boards **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.8.

Following stress, test coupons or production boards **shall** be microsectioned. Microsectioning **shall** be accomplished per IPC-TM-650, Method 2.1.1, or 2.1.1.2 on test coupons or production boards. A minimum of three holes or vias **shall** be inspected in the vertical cross section. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the three holes is within 10% of the drilled diameter of the hole.

Plated-through holes **shall** be examined for foil and plating integrity at a magnification of 100X ± 5%. Referee examinations **shall** be accomplished at a magnification of 200X ± 5%. Each side of the hole **shall** be examined independently. Examination for laminate thickness, foil thickness, plating thickness, lay-up orientation, lamination and plating voids, and so forth, **shall** be accomplished at magnifications specified above. Plating thicknesses below 1 µm [0.00004 in] **shall not** be measured using metallographic techniques.

Note: When agreed by user and supplier, alternate techniques may be used to supplement microsection evaluation.

3.6.2 Requirements for Microsectioned Coupons or Production Boards When examined in microsection, the test coupons or production boards **shall** meet the requirements of Table 3-6 and paragraph 3.6.2.1 through 3.6.2.16.

3.6.2.1 Plating Integrity Plating integrity in the plated-through holes **shall** meet the requirements detailed in Table 3-6. For Class 2 and 3 product, there **shall** be no separation of plating layers (except as noted in Table 3-6), no plating cracks, and internal interconnections **shall** exhibit no separation or contamination between plated hole wall and internal layers.

Metal core or thermal planes, when used as electrically functional circuitry, **shall** meet the above requirements when made from copper; but those made from dissimilar metals may have small spots or pits at their junction with the hole wall plating. Those areas of contamination or inclusions **shall** neither exceed 50% of each side of the interconnection, nor occur in the interface of the copper cladding on the core and the copper plating in the hole wall when viewed in the microsection evaluation.

3.6.2.2 Plating Voids Class 1 product **shall** meet the requirements for plating voids established in Table 3-6. For Class 2 and 3 product, there **shall** be no more than one void per test coupon or production board, and the following criteria must be met:

a. There **shall** be no more than one plating void per test coupon or production board, regardless of length or size.

b. There **shall** be no plating void in excess of 5 percent of the total printed wiring board thickness.

c. There **shall** be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

d. Circumferential plating voids are not allowed.

If a void is detected during evaluation of a microsection which meets the above criteria, resample in accordance with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or production boards have no plating voids, the product which the test coupon or production boards represent are considered acceptable; however, if a plating void is present in the microsections, the product **shall** be considered nonconforming.

3.6.2.3 Laminate Integrity For Class 2 and 3 products, there **shall** be no laminate voids in Zone B (Figure 3-5) in excess of 80 µm [0.00315 in]. For Class 1 products, voids allowed in Zone B (Figure 3-5) **shall not** exceed 150 µm [0.00591 in]. Multiple voids between two adjacent plated-through holes in the same plane **shall not** have a combined length which exceeds these limits. Cracks between two uncommon conductors in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

3.6.2.4 Laminate Cracks Laminate cracks in Zone A (Figure 3-5) are acceptable. Cracks which originate in Zone A and extend into Zone B or are entirely in Zone B **shall not** be in excess of 80 µm [0.00315 in] for Class 2 or 3 products, and 150 µm [0.00591 in] for Class 1 products. Multiple cracks between two adjacent plated-through holes in the same plane **shall not** have a combined length which exceeds these limits.

3.6.2.5 Etchback When specified on the master drawing, printed boards **shall** be etched back for the lateral removal of resin and/or glass fibers from the drilled hole walls prior to plating. The etchback **shall** be between 5 µm [0.00020 in] and 80 µm [0.00315 in] with a preferred depth of 13 µm [0.00051 in]. Shadowing is permitted on one side of each land. When no etchback is specified and the board manufacturer elects to use etchback, the manufacturer **shall** be qualified to perform etchback in his qualification test coupons or boards.

Caution: Etchback greater than 50 µm [0.00197 in] may cause folds or voids in the plating, which then may not meet the required copper thickness.

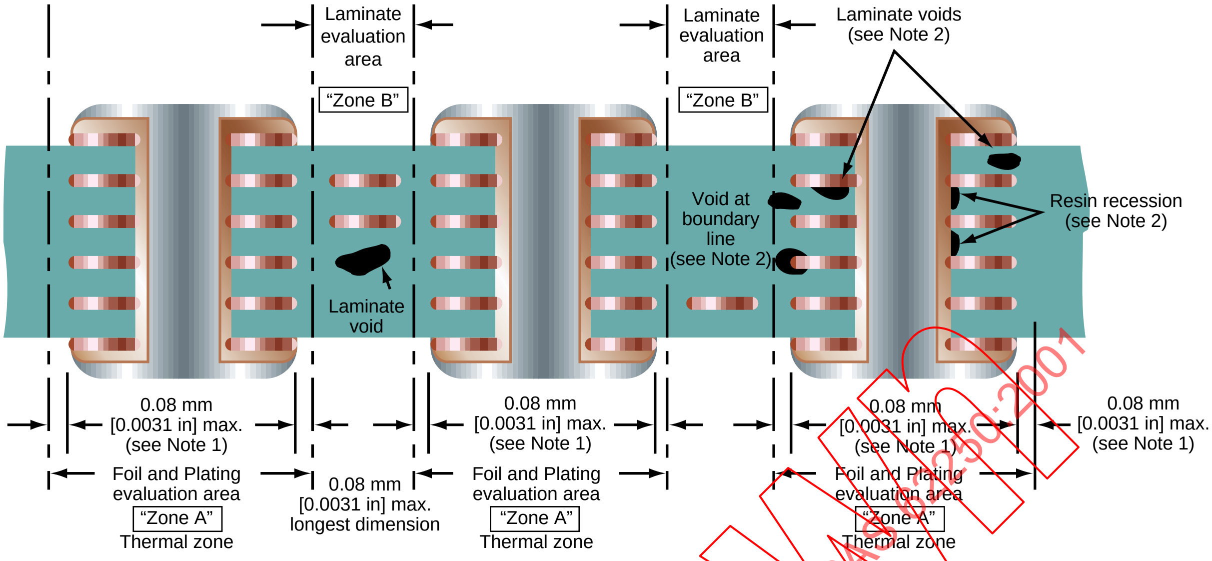
3.6.2.6 Smear Removal Smear removal is removal of resin debris which results from the formation of the hole. Smear removal **shall** be sufficient to meet the acceptability criteria for plating separation (see Table 3-6). Smear removal **shall not** be etched back greater than 25 µm [0.00098 in]; random tears or drill gouges which produce small areas where the 25 µm [0.00098 in] depth is exceeded **shall not** be evaluated as smear removal. Smear removal is not required of Type 1 or Type 2 boards.

3.6.2.7 Negative Etchback Negative etchback **shall not** exceed the requirements shown in Figure 3-6.

3.6.2.8 Annular Ring (Internal) Internal annular ring, if not determined by the techniques in 3.4.2, **shall** be measured by microsection to verify conformance to Table 3-5 as shown in Figure 3-1. For Class 2 boards, if internal annular ring breakout is detected in the vertical cross section, but the degree of breakout can not be determined, it **shall** be measured by horizontal microsection. The test coupon or production board used for the horizontal microsection **shall** be taken from the affected area and analyzed on the suspect layer(s). Requirements are shown in Table 3-5. Measurement **shall** be as shown in Figures 3-2A and 3-2B.

3.6.2.9 Lifted Lands Lifted lands are allowed on the thermally stressed microsection.

3.6.2.10 Plating/Coating Thickness Based on microsection examination, or on the use of suitable electronic measuring equipment, plating/coating thicknesses **shall** meet the requirements of Table 3-2, or as specified in the procurement document. Measurements in the plated-through hole **shall** be reported as an average thickness per side of the hole. Isolated thick or thin sections **shall not** be used for averaging. Isolated areas of reduced copper thickness due to glass fiber protrusions **shall** meet the minimum thickness requirements of Table 3-2 as measured from the end of the protrusion to the hole wall.



Notes:

1. The thermal zone extends 80 µm [0.08 mm] beyond the ends of each land.
2. Laminate defects in the Zone A areas are not evaluated on specimens which have been exposed to thermal stress or rework simulation.

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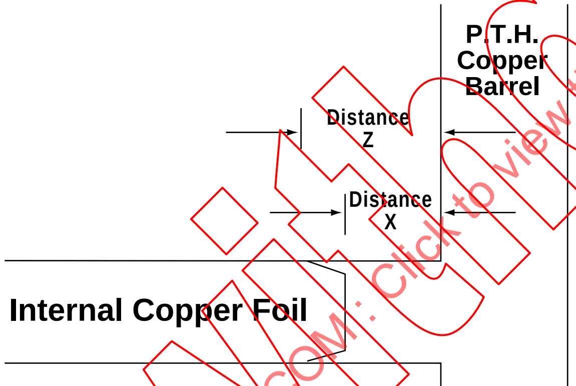
Figure 3-5 Typical Microsection Evaluation Specimen (Three Plated-Through Holes)



Distance "X" shall not exceed:
Class 1—25 µm [0.000984 in]
Class 2—25 µm [0.000984 in]
Class 3—13 µm [0.000512 in]
Distance "Z" shall not exceed:
90 µm [0.00354 in]

IPC-6012a-3-6

Figure 3-6 Negative Etchback

If copper thickness less than the minimum specified in Table 3-2 is detected in isolated areas, it should be considered a void and resample in accordance with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or production boards have no isolated areas of reduced copper thickness, the product which the test coupons or production boards represent are considered acceptable; however, if reduced copper thickness is present in the microsections, the product **shall** be considered nonconforming.

3.6.2.11 Minimum Internal Layer Copper Foil Thickness If the internal conductor thickness is specified by a foil weight, the minimum internal copper thickness after processing **shall** be in accordance with Table 3-7 for all classes. When the procurement documentation specifies a minimum copper thickness for internal conductors, the conductor **shall** meet or exceed that minimum thickness.

3.6.2.12 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-8. When the procurement documentation specifies a minimum copper thickness for external conductors, the test coupon or production board **shall** meet or exceed that minimum thickness.

3.6.2.13 Metal Cores The minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands and/or plated-through holes, and the metal plane **shall** be 100 µm [0.00394 in] (see Figure 3-7).

3.6.2.14 Dielectric Thickness The minimum dielectric spacing **shall** be specified in the procurement documentation.

Note: Minimum dielectric spacing may be specified to be 30 µm [0.00118 in]; however, low profile copper foils should be used and the voltages employed should be taken

Table 3-7 Internal Layer Foil Thickness After Processing

Copper Foil			
Designator	**Weight**	**Starting Thickness**	**Minimum**
E	1/8 oz	5 µm [0.00020 in]	3.5 µm [0.00014 in]
Q	1/4 oz	9 µm [0.00035 in]	6.0 µm [0.00024 in]
T	3/8 oz	12 µm [0.00047 in]	8.0 µm [0.00031 in]
H	1/2 oz	17 µm [0.00067 in]	12.0 µm [0.00047 in]
1	1 oz	35 µm [0.00138 in]	25.0 µm [0.00098 in]
2	2 oz	70 µm [0.00276 in]	56.0 µm [0.00220 in]
3	3 oz	105 µm [0.00413 in]	91.0 µm [0.00358 in]
4	4 oz	140 µm [0.00551 in]	122.0 µm [0.00480 in]
Above 4 oz			13 µm [0.00051 in] below minimum thickness listed for that foil thickness in IPC-4562

Table 3-8 External Conductor Thickness After Plating

Base Copper Foil			
Designator	**Weight**	**Starting Thickness**	**Minimum**
E	1/8 oz	5 µm [0.00020 in]	20.0 µm [0.00079 in]
Q	1/4 oz	9 µm [0.00035 in]	22.0 µm [0.00087 in]
T	3/8 oz	12 µm [0.00047 in]	25.0 µm [0.00098 in]
H	1/2 oz	17 µm [0.00067 in]	33.0 µm [0.00130 in]
1	1 oz	35 µm [0.00138 in]	46.0 µm [0.00181 in]
2	2 oz	70 µm [0.00276 in]	76.0 µm [0.00300 in]
3	3 oz	105 µm [0.00413 in]	107.0 µm [0.00421 in]
4	4 oz	140 µm [0.00551 in]	137.0 µm [0.00539 in]
For each succeeding ounce of copper foil, increase minimum conductor thickness by 30.0 µm [0.00118 in]			

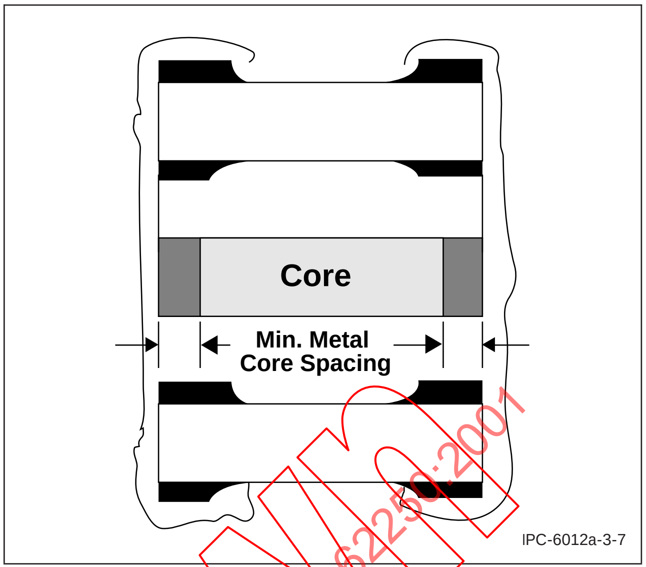


Figure 3-7 Metal Core to Plated-Through Hole Spacing

into consideration so as not to cause breakdown between layers. If the minimum dielectric spacing and the number of reinforcing layers are not specified, the minimum dielectric spacing is 90 µm [0.00354 in] and the number of reinforcing layers may be selected by the supplier. When the nominal dielectric thickness on the drawing is less than 90 µm [0.00354 in], the minimum dielectric spacing is 30 µm [0.00118 in] and the number of reinforcing layers may be selected by the supplier.

3.6.2.15 Resin Fill of Blind and Buried Vias There is no fill requirement for blind vias. Buried vias **shall** be at least 60% filled with the laminating resin for Class 2 and Class 3. They may be completely void of resin for Class 1.

3.6.2.16 Nail Heading No evidence exists that nail heading affects functionality. The presence of nail heading may be considered an indicator of process or design variation but is not a cause for rejection.

3.7 Other Tests

3.7.1 Metal Core (Horizontal Microsection) When specified, metal core printed boards which have clearance between the plated-through holes and the metal core **shall** require a horizontal microsection prepared to view the metal core/hole fill insulation. Test coupons or production boards **shall** have been subjected to thermal stress in accordance with 3.6.1 prior to microsectioning. Wicking, radial cracks, lateral spacing or voids in the hole-fill insulation material **shall not** reduce the electrical spacing between adjacent conductive surfaces to less than 100 µm [0.00394 in]. Wicking and/or radial cracks **shall not** exceed 75 µm [0.00295 in] from the plated-through hole edge into the hole-fill.

3.7.2 Rework Simulation

3.7.2.1 Through Hole Components When specified, printed boards or test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.4.36 and then microsectioned and examined in accordance with 3.6. Lifted lands are allowed.

3.7.2.2 Surface Mount Components When specified, 100% surface mount boards **shall** be tested in accordance with the procurement documentation.

3.7.3 Bond Strength, Unsupported Component Hole Land The unsupported component hole lands **shall** be tested in accordance with IPC-TM-650, Method 2.4.21. The unsupported component hole land **shall** withstand 2 kg or 35 kg/cm^2, whichever is less.

Calculations of land area of the unsupported hole do not include the area occupied by the hole.

3.8 Solder Resist (Solder Mask) Requirements When solder resist is required on printed boards, it **shall** meet the qualification/conformance requirements of IPC-SM-840. If a solder resist performance class is not specified for Class 1 or 2, IPC-SM-840 Class T **shall** be used. For Class 3 board performance, IPC-SM-840 Class H **shall** be used. The following other conformance requirements apply:

3.8.1 Solder Resist Coverage Solder resist coverage manufacturing variations resulting in skips, voids, and misregistration are subject to the following restrictions:

a. Metal conductors **shall not** be exposed in areas where solder resist is required. Touch up, if required to cover these areas with solder resist, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder resist.

b. In areas containing parallel conductors, solder resist variations **shall not** expose adjacent conductors unless the area between the conductors is purposely left blank as for a test point or for some surface mount devices.

c. Conductors under components **shall not** be exposed or **shall** be otherwise electrically isolated. If the component pattern is not readily apparent, the area covered by a component **shall** be shown in the procurement document.

d. Solder resist need not be flush with the surface of the land. Misregistration of a solder resist defined feature **shall not** expose adjacent isolated lands or conductors.

e. Solder resist is allowed on lands for plated-through holes to which solder connections are to be made provided the external annular ring requirements for that Class of products are not violated; resist **shall not** encroach upon the barrel of this type of plated-through hole. Other surfaces such as edge board connector fingers and surface mount lands **shall** be free of solder resist except as specified. Solder resist is allowed in plated-through holes and via holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled. Solder resist may tent or plug via holes and may be required for that purpose. Test points that are intended for assembly testing must be free of solder resist unless coverage is specified.

f. When a land contains no plated-through holes, as in the case of surface mount or ball grid array lands, misregistration **shall not** cause encroachment of the solder resist on the land or lack of solder-resist-definition in excess of the following:

  1) on surface mount lands misregistration **shall not** cause encroachment of the solder resist over the land area greater than 50 µm [0.00197 in] for a pitch of 1.25 mm [0.04921] or greater; and encroachment **shall not** exceed 25 µm [0.00098 in] for a pitch less than 1.25 mm [0.04921 in]; encroachment may occur on adjacent sides but not on opposite sides of a surface mount land.

  2) on ball grid array lands, if the land is solder-resist-defined, misregistration may allow a 90° breakout of the solder resist on the land; if clearance is specified, no encroachment of the solder resist on the land is allowed except at the conductor attachment.

g. Pits and voids are allowed in nonconductor areas provided they have adherent edges and do not exhibit lifting or blistering in excess of allowance in 3.8.2.

h. Coverage between closely spaced surface mount lands **shall** be as required by procurement documentation.

i. When design requires coverage to the board edge, chipping or lifting of solder resist along the board edge after fabrication **shall not** penetrate more than 1.25 mm [0.04921 in] or 50% of the distance to the closest conductor, whichever is less.

3.8.2 Solder Resist Cure and Adhesion The cured solder resist coating **shall not** exhibit tackiness, delamination, or blistering to the following extent:

- Class 1 does not bridge between conductors.
- Class 2 and 3 two per side, maximum size 0.25 mm [0.00984 in] in longest dimension, does not reduce electrical spacing between conductors by more than 25%.

Rework and touch up, if required to cover these areas with solder resist, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder resist. When tested in accordance with IPC-TM-650, Method 2.4.28.1, the maximum percentage of cured solder resist lifting from the G coupon **shall** be in accordance with Table 3-9.

3.8.3 Solder Resist Thickness Solder resist thickness is not measured unless specified in the procurement documents. If a thickness measurement is required, instrumental methods may be used or assessment may be made using a microsection of the parallel conductors on the E coupon.

Table 3-9 Solder Resist Adhesion

	Maximum percentage loss allowed		
Surface	**Class 1**	**Class 2**	**Class 3**
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid-tin)	50	25	10

3.9 Electrical Requirements When tested as specified in Table 4-4, the printed boards **shall** meet the electrical requirements detailed in the following paragraphs.

3.9.1 Dielectric Withstanding Voltage Applicable test coupons or production boards **shall** meet the requirements of Table 3-10, without flashover, or breakdown between conductors, or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between all common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

Table 3-10 Dielectric Withstanding Voltages

	Class 1	Class 2 and 3
Voltage For spacing 80 µm [0.00315 in] or greater	No requirement	500 Vdc +15, -0
Voltage For spacing less than 80 µm [0.00315 in]	No requirement	250 Vdc +15, -0
Time	No requirement	30 sec +3, -0

3.9.2 Electrical Continuity and Insulation Resistance Boards **shall** be tested in accordance with IPC-ET-652.

3.9.2.1 Continuity Printed boards and qualification test boards **shall** be tested in accordance with the procedure outlined below. There **shall** be no circuits whose resistance exceeds the values established in IPC-ET-652. Specialized circuitry consisting of long runs of very narrow conductors, or short runs of very large conductors may increase or decrease these values. The acceptability criteria for these specialized conductors must be specified in the procurement documentation.

A current **shall** be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors **shall not** exceed that specified in IPC-2221 for the smallest conductor in the circuit. For qualification, the test current **shall not** exceed one ampere. Boards with designed resistive patterns **shall** meet the resistance requirements specified on the master drawing.

3.9.2.2 Insulation Resistance Printed Boards or qualification test boards **shall** be tested in accordance with the following procedure. The insulation resistance between conductors **shall** meet the values established in IPC-ET-652.

The voltage applied between networks must be high enough to provide sufficient current resolution for the measurement. At the same time, it must be low enough to prevent arc-over between adjacent networks, which could induce defects within the product. For manual testing, the voltage **shall** be 200 volts minimum and **shall** be applied for a minimum of five seconds. When automated test equipment is used, the minimum applied test voltage **shall** be twice the maximum rated voltage of the board. If the maximum is not specified, the test voltage **shall** be 40 volts minimum.

3.9.3 Circuit/Plated-Through Shorts to Metal Substrate Printed boards **shall** be tested in accordance with 3.9.1 except that polarizing voltage of 500 volts (DC) **shall** be applied between conductors and/or lands and the metallic heatsink in a manner such that each conductor/land area is tested (e.g., using a metallic brush or aluminum foil).

The board **shall** be capable of withstanding 500 volts (DC) between circuitry/plated-through holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.

3.9.4 Moisture and Insulation Resistance (MIR) Test coupons **shall** be tested in accordance with the procedure outlined below. The test coupon **shall not** exhibit subsurface imperfections in excess of that allowed in 3.3.2. Insulation resistance **shall** meet the minimum requirements shown in Table 3-11 (at 500 volts DC). Noncomponent flush boards **shall** have a minimum requirement of 50 MΩ for all classes. Insulation resistance requirements in the as-received condition are detailed in special requirement section (see 3.11.9).

Table 3-11 Insulation Resistance

	Class 1	Class 2	Class 3
As received	Maintain electrical function	500 MΩ	500 MΩ
After exposure to moisture	Maintain electrical function	100 MΩ	500 MΩ

The moisture and insulation resistance for printed boards **shall** be performed in accordance with IPC-TM-650, Method 2.6.3. Conformal coating in accordance with IPC-CC-830 **shall** be applied to the external conductors prior to chamber exposure. Final measurements **shall** be made at room temperature within two hours after removal from the test chamber. All layers have a 100 ± 10 volts DC polarizing voltage applied during chamber exposure. Mealing of the conformal coating **shall not** extend more than 3 mm [0.12 in] from the edge of the test coupon or production board.

3.9.4.1 Dielectric Withstanding Voltage After MIR A dielectric withstanding voltage test **shall** be performed after moisture and insulation resistance in accordance with 3.9.1.

3.10 Cleanliness Printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.3.25 paragraph 4.0 Resistance of Solvent Extract Method. Equivalent methods may be used in lieu of the method specified; however it **shall** be demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the solution presently specified.

3.10.1 Cleanliness Prior to Solder Resist Application When a printed board requires a permanent solder resist coating, the uncoated boards **shall** be within the allowable limits of ionic and other contaminants prior to the application of solder resist coating.

When noncoated printed boards are tested per 3.10, the contamination level **shall not** be greater than an equivalent of 1.56 µg/cm^2 of sodium chloride.

3.10.2 Cleanliness After Solder Resist, Solder, or Alternative Surface Coating Application When specified, printed boards **shall** be tested per 3.10 and meet the requirements in the procurement documentation.

3.10.3 Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination When specified, inner layers **shall** be tested per 3.10 and meet the requirements of the procurement documentation.

3.11 Special Requirements When specified in the procurement documentation, some or all of the special requirements listed in this section (3.11) **shall** apply. A notation in the procurement documentation will designate which are required.

3.11.1 Outgassing Printed boards **shall** be tested in accordance with the procedure outlined below. The degree of outgassing **shall not** result in a total mass loss of more than 0.1%.

Mass loss **shall** be determined on test coupons or production boards of representative substrates when tested per IPC-TM-650, Method 2.6.4. Test substrates **shall** be approximately 1 cm^3 in volume. The substrates **shall** be placed in a vacuum chamber capable of achieving 7 x 10^{-3} Pa [5 x 10^{-5} mm Hg or torr] for 24 hours.

3.11.2 Organic Contamination Noncoated printed boards **shall** be tested in accordance with the procedure outlined below. Any positive identification of organic contamination **shall** constitute a failure.

The printed board **shall** be tested in accordance with IPC-TM-650, Methods 2.3.38 or 2.3.39. The first is a qualitative method in which very pure acetonitrile is dripped across the test coupon or production board and collected on a microscope slide. It is dried and compared with a slide having dried, uncontaminated acetonitrile on it for visual evidence of organic residue. If evidence of organic contamination is detected by this test, Method 2.3.39 is used to determine the nature of the contaminant by the use of infrared spectrophotometric analysis using the Multiple Internal Reflectance (MIR) method.

3.11.3 Fungus Resistance Completed boards or representative board sections from the lot **shall not** support fungus growth when tested as follows: The specimen(s) **shall** be tested in accordance with IPC-TM-650, Method 2.6.1.

3.11.4 Vibration The test coupon or production board **shall** pass the circuitry test in 3.9.2 following the vibration test procedure below and **shall not** exhibit bow or twist in excess of that allowed in 3.4.4 following testing.

The boards **shall** be subjected to both a cycling and resonance dwell test with the flat surface of the board mounted perpendicular to the axis of vibration in accordance with IPC-TM-650, Method 2.6.9.

Cycling test—The cycling test **shall** consist of one sweep from 20 to 2000 Hz performed in 16 minutes. Input acceleration over the 20 to 2000 Hz frequency range **shall** be maintained to 15 Gs.

Resonance dwell—Test coupons or production boards **shall** be subjected to a 30 minute resonance dwell with 25 Gs input or a maximum of 100 Gs output measured at the geometric center of the test coupon or production board. The test coupons or production boards **shall** be restrained from movement by fixturing on all four sides.

3.11.5 Mechanical Shock The test boards **shall** pass the circuitry test in 3.9.2 after being subjected to mechanical shock testing as follows.

The mechanical shock test **shall** be performed in accordance with IPC-TM-650, Method 2.6.5. The boards **shall** be subjected three times to a shock pulse of 100 Gs with a duration of 6.5 milliseconds in each of the three principal planes. The test coupons or production boards **shall** be restrained from movement by fixturing on all four edges.

3.11.6 Impedance Testing Requirements for impedance **shall** be specified on the master drawing. Impedance testing may be performed on a test coupon or a designated circuit in the production board. Time Domain Reflectometers

(TDR) are used for electrical testing, but for large impedance tolerances, mechanical measurements from a microsection utilizing a special test coupon can be used to calculate and verify impedance values. (See IPC-2221 for the equations for calculating impedance from the test coupon and IPC-TM-650, Method 2.5.5.7 for the test method using the TDR technique.)

3.11.7 Coefficient of Thermal Expansion (CTE) When boards that have metal cores or reinforcements with a requirement to constrain the thermal expansion in the planar directions, the Coefficient of Thermal Expansion **shall** be within ± 2 ppm/°C for the CTE and temperature range specified on the procurement documentation. Testing **shall** be by the strain gauge method in accordance with IPC-TM-650, Method 2.4.41.2. If agreed upon by user and supplier, other methods of determining the CTE may be used.

3.11.8 Thermal Shock When specified, printed boards or test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.6.7.2. An increase in resistance of 10% or more **shall** be considered a reject. After microsectioning, the boards or test coupons **shall** meet the requirements of Table 3-6 and Figure 3-4.

For polytetrafluoroethylene (PTFE) material types, the board or test coupon **shall** meet the circuitry requirements of 3.9.2 at room temperature after the 100th cycle and no microsectioning is required.

3.11.9 Surface Insulation Resistance (As Received) Test coupons **shall** be tested in accordance with the procedure outlined below. The insulation resistance **shall** be no less than that shown in Table 3-11.

Test coupons or production boards should be conditioned at 50 ± 5°C [122 ± 9°F] with no added humidity for a period of 24 hours. After cooling, the insulation resistance test **shall** be performed in accordance with the ambient temperature measurements specified in IPC-TM-650, Method 2.6.3.

3.12 Repair Repair of bare boards **shall** be as agreed upon between the user and supplier for each set of procurement documentation. (See IPC-7721.)

3.12.1 Circuit Repairs When agreed on between user and supplier, circuit repairs on Classes 1, 2, and 3 will be permitted. As a guideline, there should be no more than two circuit repairs for each 0.09 m^2 or less of layer area per side. Circuit repairs on any impedance controlled circuits **shall not** violate the impedance requirement and **shall** have the agreement of the user. Circuit repairs **shall not** violate the minimum electrical spacing requirements.

3.13 Rework Rework is permitted for all Classes. The touch-up of surface imperfections in the base material or removal of residual plating materials or extraneous copper will be permitted for all products when such action does not affect the functional integrity of the board.

4 QUALITY ASSURANCE PROVISIONS

4.1 General General Quality Assurance Provisions are specified in IPC-6011 and each sectional specification. The requirements specific to Rigid Boards are contained in this specification and include the Qualification Testing, Acceptance Testing and Frequency Quality Conformance Testing.

4.1.1 Qualification Qualification is agreed upon by the user and supplier (see IPC-6011). The qualification should consist of preproduction samples, production sample or test coupons (see IPC-6011) that are produced by the same equipment and procedures planned for the production boards. Qualification as agreed by the user may consist of documentation that supplier has furnished similar product to other users or to other similar specifications.

4.1.2 Sample Test Coupons Sample test coupons may be used for qualification or for on-going process control. Master drawings, databases, or phototools are available from IPC. For each type (see 1.3.2) the master drawing and phototool is listed as follows:

Type 1	Use surface layers of IPC-A-47
Type 2	Use surface layers of IPC-A-47
Type 3	Master Drawing IPC-100103, Phototool IPC-A-47

Note: IPC-100002 is the universal drilling and profile master drawing.

Table 4-1 specifies the test coupons on the sample used for qualification and process capability evaluations.

4.2 Acceptance Tests Use the C=0 Sampling Plan specified in Table 4-2 when ‘‘Sample’’ is indicated in Table 4-3. Acceptance testing **shall** be performed as specified in Table 4-3 to the requirements of this specification and IPC-6011 using either test coupons and/or production boards. The test coupons are described in IPC-2221 and indicate purpose of coupon and its frequency on a manufacturing panel.

4.2.1 C=0 Sampling Plan The C=0 Sampling Plan provides greater or equal protection for the Lot Tolerance Percent Defective (L.T.P.D.) protection at the 0.10 ‘‘consumer risk’’ level. The Index Values at the top of each sample size column associates to the A.Q.L. level. For a lot to be accepted, all samples (shown in Table 4-2) **shall** conform to the requirements. Disposition of rejected lots **shall** be fully documented. Contact the American Society for Quality Control for more information on sampling plans (H0862).

Table 4-1 Qualification Test Coupons

Test	Type 1	Types 2,3,5	Types 4,6	Board
Visual (5)	All	All	All	X
Solderability				
Surface (5)	M2,M5			
Hole (5)		S1,S6	S1,S6	
Dimensional (5)	All	All	All	X
Physical				
Plating Adhesion (5)	N1,N4,N5	N1,N4,N5	N1,N4,N5	
Bond Strength	A2,A3,A6	A2,A3,A6	A1,A3,A6	
Construction Integrity		A1,A4,A5	Design Req.	
PTH Prior to Stress		A1,A4,A5	Design Req.	
Additional Dimensions				
PTH After Stress				
Thermal Stress		B1,B4,B5	Design Req.	
Horizontal micro (Metal Core)		A1,B4,B5	A1,B4,B5	
Rework Simulation		B2,B3,B6	Design Req.	
Electrical Requirements				
DWV	E1,E4,E5	E1,E4,E5	E1,E4,E5	
Continuity	D1,D4,D5	D1,D4,D5	Design Req.	
Insulation Resistance	E2,E3,E6	E2,E3,E6	E2,E3,E6	
Environmental				
Thermal Shock	D2,D3,D6	D2,D3,D6	Design Req.	
Cleanliness (5)				X
Special Requirements (6)				
Outgassing				X
Organic Contamination				X
Fungus				X
Vibration				X
Mechanical Shock				
Impedance		H1,H2,H3		
Thermal Expansion				

Note 5 - Not technology dependent.
Note 6 - Additional test coupons required, to be agreed upon between user and manufacturer.

Table 4-2 C=0 Sampling Plan (Sample Size for Specific Index Value*)

Lot Size	Class 1			Class 2			Class 3			
	2.5*	4.0*	6.5*	1.5*	2.5*	4.0*	0.10*	1.0*	2.5*	4.0*
1-8	5	3	2	**	5	3	**	**	5	3
9-15	5	3	2	8	5	3	**	13	5	3
16-25	5	3	3	8	5	3	**	13	5	3
26-50	5	5	5	8	5	5	**	13	5	5
51-90	7	6	5	8	7	6	**	13	7	6
91-150	11	7	6	12	11	7	125	13	11	7
151-280	13	10	7	19	13	10	125	20	13	10
281-500	16	11	9	21	16	11	125	29	16	11
501-1200	19	15	11	27	19	15	125	34	19	15
1201-3200	23	18	13	35	23	18	125	42	23	18
3201-10,000	29	22	15	38	29	22	192	50	29	22
10,001-35,000	35	29	15	46	35	29	294	60	35	29

*Index Value is associated to the A.Q.L. value. If a particular product is determined to be "critical" by the user and a smaller index value is required, the user **shall** designate the requirement in the procurement document and should state the "critical" requirement on the master drawing.
**Denotes inspect entire lot.

Table 4-3 Acceptance Testing and Frequency

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Production Board	Test Coupon by Board	Class 1[1]	Class 2[1]	Class 3[1]	
Material	3.2.1- 3.2.12			Manufacturer's Certification			Verifiable certificate of compliance or SPC program
Visual							
Edges of board	3.3.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Laminate imperfections	3.3.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Voids in plated hole	3.3.3	X		Sample (4.0)	Sample (2.5)	Sample (1.0)	Per panel
Lifted lands	3.3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Marking and traceability	3.3.5	X	Coupons and board	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Workmanship	3.3.9	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Solderability							
Surface/Hole	3.3.6		C and A	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Dimensional							
Board dimensional	3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Hole pattern accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Minimum 10 evaluations per board
Annular ring and breakout (internal)	3.4.2		F	Not required	Sample (1.5) Type 3-6 only	Sample (1.0) Type 3-6 only	Per panel (4 coupons)
Annular ring (external)	3.4.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Bow & twist	3.4.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Solder resist coverage	3.8- 3.8.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Plating/coating thickness (electronic)	3.6.2.10	X	C	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Conductor Width							
Internal	3.5.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per internal panel layer
External	3.5.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Conductor Spacing							
Internal	3.5.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per internal panel layer (minimum 5 per layer set)
External	3.5.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Conductive Surfaces (Surface Only)							
Edge board contact, junction of gold plate to solder finish	3.3.8	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Production Board	Test Coupon by Board	Class 1[1]	Class 2[1]	Class 3[1]	
Nicks, dents, pinholes	3.5.4.1	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board
Dewetting/ nonwetting	3.5.4.4 3.5.4.5 3.5.4.6	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board
Edge board connector	3.5.4.3	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board
Surface mount	3.5.4.2	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Minimum 10 evaluations per panel
Physical							
Plating adhesion	3.3.7	X	C	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Solder resist cure & adhesion	3.8 3.8.2		G	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Structural Integrity After Stress Types 3-6 (Microsection)							
Plating integrity	3.6.2.1		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Laminate integrity	3.6.2.3		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Etchback/ negative etchback	3.6.2.5 3.6.2.7		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Annular ring (internal)	3.6.2.8		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Lifted lands	3.6.2.9		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Hole plating thickness	3.6.2.10		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Surface plating and conductor thickness	3.6.2.10 3.6.2.12		A,B,or C	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Conductor thickness (internal)	3.6.2.11		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Metal core spacing	3.6.2.13		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Dielectric thickness	3.6.2.14		A or B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel (1 coupon)
Resin fill of blind/buried vias	3.6.2.15		A or B	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Structural Integrity After Stress Type 2 (Microsection)							
Plating integrity	3.6.2.1		A or B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Laminate integrity	3.6.2.3		A or B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Lifted lands	3.6.2.9		A or B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Hole Plating thickness	3.6.2.10		A or B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel