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Guide for the standard probe pad sizes and layouts for wafer-level electrical testing

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INTERNATIONAL
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GUIDE FOR THE STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER-LEVEL ELECTRICAL TESTING

FOREWORD

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GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER-LEVEL ELECTRICAL TESTING

(From JEDEC Ballot JCB-96-27, formulated under the cognizance of JC14.2 Committee on Wafer-Level Reliability)

1 Scope

This guide applies to double- and single-column arrays of metal probe pads, on a semiconductor wafer or chip, that are electrically connected to one or more test structures.

The use of this guide will make necessary only two standard wafer-probe cards, one with a 1-by-16 and the other with a 2-by-16 standard array of probe tips to make contact with probe pads.

This guide is intended, in particular, to facilitate and expedite wafer-level electrical testing by laboratories participating in interlaboratory experiments conducted by JC-14.2 Committee.

This guide is intended, in general, to facilitate and expedite wafer-level electrical testing of test structures when using a wafer-probe card to make electrical contact to these structures.

The use of this guide will impose some restrictions on how test structures may be grouped within and near the area defined by the array of pads.

2 Introduction: significance and use

It is useful to have a standard for the size and layout of the probe pads of test structures that are to be electrically characterized or tested at the wafer level. Having such a standard design affords efficient and cost-effective use of wafer-probe stations because its widespread use leads to the need for a minimum number of probe cards and card changes to accommodate the various test structures that may need to be tested.

The use of a standard for the layout of probe pads is important for conducting interlaboratory experiments to evaluate or develop standard measurement methods that involve test-structure measurements or tests.

When a probe card required by a test structure is not readily available, manual probing is an option that presents significant potential for damage to the test structure. Damage to structures involved in interlaboratory experiments can lead to serious delays in the conduct and analysis of such experiments.

3 Design guides

The probe pads are designed to be probed by probe cards having one of two standard probe arrays: 16 probe tips arranged in a column at 160 μm intervals, and two such columns in a 2-by-16 arrangement where the separation of the two columns is dictated by the need to contact a parallel column of pads that have a center-to-center separation of 160 μm .

NOTE—An optimum separation of the two columns of probe tips may involve a somewhat greater separation than 160 μm to accommodate inward movements of the probes as they make contact with the metal pad.

3.1 Size of contact pads

The minimum pad size shall be 80 μm on a side.

NOTE—If the test structures are to be covered with a passivation film, the selection of the size of the opening in the passivation layer over the metal pad is left to the user. It is generally desirable to maximize this opening (without exposing the edges of the metal pad) to facilitate probing and wire bonding.

3.2 Double-column pad layout array

3.2.1 The pads shall be arranged in two columns and the center-to-center separation of the pads in both the horizontal and the vertical directions shall be 160 μm . See figure 1.

NOTE—If a pad size larger than 80 μm on a side is selected (see 3.1), adequate separation between adjacent pad edges should be provided to avoid possible short circuits between adjacent wire bonds (if used). Adequate separation between the pads and any adjacent-running features of the test structures should be provided for to reduce the possibility of damage to these features by accidental skidding of the probe off the pad.

3.2.2 The pads shall be numbered in 2-by-16 units as shown in figure 2.

NOTE—If a substrate contact is used in the test, the pad number of this contact should correspond to the probe pin that is electrically connected to the wafer stage of the probing station.

3.2 Double-column pad layout array (cont'd)

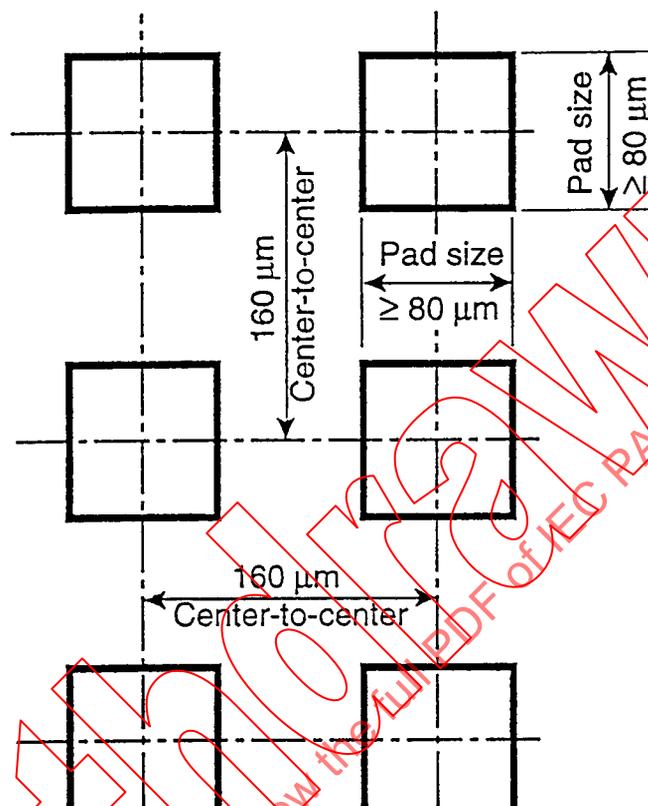


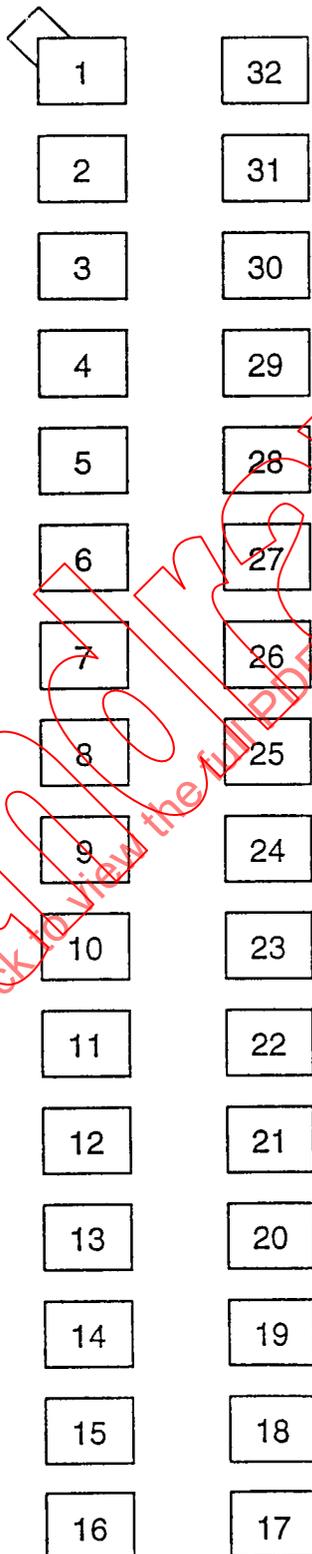
Figure 1 — Drawing a portion of a 2-by-16 array of bonding/probe pads

3.2.3 To avoid the possibility of confusion because of the 180° rotational symmetry, pad #1 shall be shaped differently from the other pads (as illustrated in figure 2) or some feature shall be included that makes pad #1 easily recognizable when using the optics of the probe station.

3.2.4 If the number of pad pairs is less than 16, space on the wafer should be free of features for the placement of a 2-by-16 probe card, where the probe tips are designed to contact the standard probe-pad array described in 3.2.1.

NOTE—To prevent contamination of the probe tips, it is recommended that a metal probe pad always be located where a probe would land on the wafer or chip.

3.2.5 If the number of pad pairs is larger than 16, the contacts for any one test structure must be contained completely within the first or within any subsequent set of 16 pad pairs that would serve to extend the column of pad pairs.

3.2 Double-column pad layout array (cont'd)**Figure 2 — Pad numbering scheme for a 2-by-16 unit**

3.3 Single-column pad layout array

3.3.1 The pads shall be aligned in one column and the center-to-center separation of the pads in the column shall be 160 μm . See 3.2.1 Note.

3.3.2 The pads shall be numbered in units of 16. See 3.2.2 Note.

3.3.3 To avoid the possibility of confusion because of the 180° rotational symmetry, pad #1 shall be shaped differently from the other pads (as illustrated in figure 2) or some feature shall be included that makes pad #1 easily recognizable when using the optics of the probe station.

3.3.4 If the number of pads is less than 16, space on the wafer shall be free of features for the placement of a 1-by-16 probe card designed to contact the line of pads described in 3. See 3.2.4 Note.

3.3.5 If the number of pads is larger than 16, the contacts for any one test structure must be contained completely within the first or within any subsequent set of 16 pads that would serve to extend the column of pads.

3.4 Separation of pad arrays on the wafer

If the pad arrays are to be replicated on the wafer or chip, they shall be spaced at regular intervals in either horizontal or vertical directions, or both.