**IEC/PAS 62202**

**Edition 1.0**
2000-11

# Failure mechanisms and models for silicon semiconductor devices

**PUBLICLY AVAILABLE SPECIFICATION**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

**Reference number**
**IEC/PAS 62202**

EIA/JEP122

# EIA/JEDEC PUBLICATION

# Failure Mechanisms and Models for Silicon Semiconductor Devices

## EIA/JEP122

FEBRUARY 1996

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT

# NOTICE

EIA/JEDEC Standards and Publications contain material that has been prepared, progressively reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.

EIA/JEDEC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchases, facilitating interchangeability and improvement of products, and assisting the purchaser is selecting and obtaining with minimum delay the proper product for his particular need. Existence of such standards shall not in any respect preclude any member or nonmember of JEDEC from manufacturing or selling products not conforming to such standards, nor shall the existence of such standards preclude their voluntary use by those other than EIA members, whether the standard is to be used either domestically or internationally.

EIA/JEDEC Standards and Publications are adopted without regard to whether their adoption may involve patents or articles, materials, or processes. By such action, EIA/JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the EIA/JEDEC Standards or Publications.

The information included in EIA/JEDEC Standards and Publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the EIA/JEDEC organization there are procedures whereby an EIA/JEDEC Standard or Publication may be further processed and ultimately becomes an ANSI/EIA Standard.

Inquiries, comments, and suggestions relative to the content of this EIA/JEDEC Standard or Publication should be addressed to the JEDEC Executive Secretary at EIA Headquarters, 2500 Wilson Boulevard, Arlington, VA 22201.

Published by

Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201

INTERNATIONAL ELECTROTECHNICAL COMMISSION

# FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES

## FOREWORD

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public and established in an organization operating under given procedures.

IEC-PAS 62202 was submitted by JEDEC and has been processed by IEC technical committee 47: Semiconductor devices.

| The text of this PAS is based on the following document: | This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document: |
|---|---|
| **Draft PAS** | **Report on voting** |
| 47/1507/PAS | 47/1539/RVD |

Following publication of this PAS, the technical committee or subcommittee concerned will investigate the possibility of transforming the PAS into an International Standard.

An IEC-PAS licence of copyright and assignment of copyright has been signed by the IEC and JEDEC and is recorded at the Central Office.

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
6) Attention is drawn to the possibility that some of the elements of this PAS may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

# FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES

## Contents

# FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES

## FOREWORD

This publication provides guidance in the selection of thermal activation energies used to estimate system failure rates for the Sum-of-the-Failure-Rates Method. It assumes that microcircuit failure mechanisms have statistically independent failure tendencies when stressed at accelerated test conditions.

# FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES

(From JEDEC Council Ballot JCB-94-73 formulated under the cognizance of JC-14 Committee on Quality and Reliability of Solid State Products)

## 1 Scope

This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum-of-the-Failure-Rates method.

## 2 Introduction

Accelerated tests are typically used to find and identify potential failure mechanisms in silicon semiconductor devices and to estimate the rate of their occurrence in electronic systems. The historical approach to investigating the relationship between a maximum stress failure rate and a system failure rate is to choose a single representative "equivalent" thermal activation energy for a given product or product group and use that number in the calculation of the acceleration factor for the device failure-rate estimation in the system application. While that approach has been generally accepted by the industry because of its simplicity and direct relationship to products, another method has been developed, the Sum-of-the-Failure-Rates method, that offers more knowledge of why devices fail.

For the Sum-of-the-Failure-Rates method, the failure rates of potential failure mechanisms are estimated separately and are then added together to generate the microcircuit failure rate estimate. The failure rate equation that represents this process is $\lambda_s = \Sigma\lambda_i = \lambda_1 + \lambda_2 + \ldots + \lambda_n$, where $\lambda_s$ represents the system failure rate for the microcircuit and $\lambda_i$ represents the failure rate for each failure mechanism.

## 2.1 Organization of this document

This publication is organized into three parts. The first consisting of sections 1 through 4, discusses the principles of classification and definitions needed to understand and use this publication. The second part consists of two tables of failure mechanisms. The first table can be visualized as a first order listing. It assigns thermal activation energies to general classifications of failure mechanisms. If a reliability engineer has only superficial knowledge of the physical processing employed and has no other way of obtaining the characteristics of the failure mechanism, but knows that the failure fails under one of the categories in table 1, then the selection of the typical value for thermal activation energy found in table 1 will provide the basis for a reasonable estimate of that failure mechanism's effect on the microcircuit failure rate. The second table adds more detail to some of the specific materials and processes listed in table 1 and assumes more knowledge of the specific process and material details is known. The activation energies in this table should provide a better estimate of the failure rate impact for a failure mechanism than would be achieved from a table 1 estimate. The third and final part is the annex where the technical rationale for the activation energy relationships and their mathematical relationships is explored. Bibliographical reference listings are supplied for each subject.

## 3 Definitions

The following terms will be used in the body of the text.

**acceleration factor (A):** The ratio of the measured failure rate at one stress condition to the failure rate of the same silicon semiconductor devices stressed at another condition.

**activation energy ($E_a$)[1]:** The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur. Examples are the energy needed by the molecule to take part in a chemical reaction, by an electron to reach the conduction band in a semiconductor, or by a lattice defect to move to a neighboring site.

**$A_f$:** The acceleration factor due to the presence of some stress (current density, electric field, humidity, temperature cycling, etc.).

---

[1] First Definition, (Van Nostrand's Scientific Encyclopedia, Sixth Edition, Van Nostrand Reinhold Company), p.31

**$A_T$:** The acceleration factor due to changes in temperature. The mathematical relationship or equation commonly used for microcircuits and other silicon semiconductor devices follows the format of the Arrhenius equation.

The most-often referenced acceleration factor is the acceleration factor due to changes in temperature ($A_T$). It is calculated as follows:

$$A_T = \frac{\lambda_t}{\lambda_s} = e^{-\frac{E_a}{\kappa}\left(\frac{1}{T_t}-\frac{1}{T_s}\right)} \qquad (1)$$

$E_a$ = activation energy in electron volts (eV).
$\kappa$ = Boltzmann's constant
$T_t$ = absolute temperature of test in kelvins.
$T_s$ = absolute temperature of system in kelvins.
$\lambda_t$ = failure rate at the accelerated temperature.
$\lambda_s$ = failure rate at the system temperature.

Other acceleration factors can be calculated for electrical, mechanical, environmental, and other stresses when those stresses affect the reliability of a device. Acceleration factors can be a function of one or more of the basic stresses. Many of these equations are found in annex A.

**apparent activation energy ($E_a'$):** Activation energy that is calculated using the principles of the physical relationship between stress and failure rate but is not directly related to a basic physical processes change. It may be based on too many possible physical "effects" that, when stressed as a unit, produce a cumulative effect. It is similar to the concept of an activation energy but measures the probability of not exceeding some measurable attribute. A plot of the reciprocal of absolute temperature (1/T(K)) versus the log of percent failed is linear.

**Boltzmann's constant ($\kappa$):** The constant $\kappa$ from the Maxwell-Boltzmann law of distribution of velocities. The average kinetic energy of a molecule is $3\kappa T/2$, where T is absolute temperature and $\kappa = 1.38 \times 10^{-23}$ joule per kelvin. In the Arrhenius equation, $\kappa = 8.62 \times 10^{-5}$ eV/K.

**failure mechanism:** The underlying cause of the failure (e.g., electromigration). Also see JESD29, "Failure-Mechanism-Driven Reliability Monitoring of Silicon Devices".

**failure mode:** The product attribute or manner in which a failure exhibits itself (e.g., open metal).

**failure rate (λ):** The ratio of the number of failures to the total number of hours a quantity of devices are on test ($\lambda_t$) or operating in the system ($\lambda_s$). For the constant failure rate (failure rate definition: λ = number of failures ÷ number of devices ÷ number of test hours). It is measured as failure per total hours on tests. For failure mechanisms with failure rates that are a nonlinear function of time, other analytical methods are required. Standard methods of reporting failure rates for semiconductor devices report failure rates as 1) percent failed per 1000 hours and 2) FITs.

**FIT:** Failures In Time or the fraction of the number of failures per billion ($10^9$) device-hours.

**potential failure mechanism:** A physical failure mechanism that (1) has been identified through physical experimentation to exist for similar products or (2) can be linked to these products through the scientific study of the product (process) physical characteristics and the physical requirement found to be necessary for the failure mechanism to occur. See JESD29.

**random defect:** A defect found in a failing device that does not occur in a manner consistent with normal process variation. It is not a normal part of the intrinsic population of a production run. The failure is attributed to defects during production.

**relative humidity:** The ratio of the amount of water vapor in the air to the maximum amount of water vapor air can hold at that temperature and pressure. It is calculated by comparing the vapor density (or vapor pressure) in the air to the value of saturated vapor density (or saturated vapor pressure) at that specific temperature and pressure.

## 4 Classification procedure

### 4.1 The basic thermal acceleration equation

When estimating acceleration due to temperature, it is customary to use the expression in equation 1. It is an adaptation of the Arrhenius equation and has been used to express both a single failure mechanism's sensitivity to temperature (i.e., its acceleration factor) and also a product's thermal acceleration factor. By measuring parametric change caused by temperature, activation energy in its physical sense can be estimated. When used to estimate the reliability of a product, as shown in equation 2, it is also being used to express that product's reliability with respect to temperature and as a function of time.

$$\lambda_s = \frac{\lambda_t}{A_T} = \frac{\lambda_0 e^{-\frac{E_a}{\kappa T_t}}}{A_T} \qquad (2)$$

where: $\lambda_0$ is the failure rate at base temperature (i.e., room temperature).

Equation 2 must be used with caution because this relationship only holds for systems in which the failure rate is constant. Even though very few practical situations exist in which the failure rate is truly constant. Nevertheless the assumption of constant failure rate is still commonly used. For product estimates using the Composite method, the parameter $E_a$ becomes an "apparent" activation energy $E_a{}'$

## 4.2 Other activation energy classifications

Often devices and their physical processes are sensitive to more than one combination of physical forces. These stresses may be encountered in a product's application and include electrical potential, moisture in the environment, extreme temperature cycling, and other forms of stress. Potential failure mechanisms do exist for a semiconductor device that is affected by multiple stresses. The reliability engineer has to consider that there may be more than the one activation energy equation for the failure mechanism to get the correct reliability estimate for the devices under study.

For example, two such mechanisms defined by multivariable equations or equation sets are dielectric or oxide breakdown and electromigration.

For dielectric breakdown, it is still not resolved to everyone's complete satisfaction whether the failure rate is directly proportional ($\varepsilon$-Model) to or inversely proportional ($1/\varepsilon$-Model) to the field strength across the oxide. These models are only two of several that appear in the literature. There is agreement that the thermal activation energy is a less-significant factor than field strength.

For metallization, some of the electromigration factors that have to be included are the composition of the metal, the passivation above and below it, its use as a long stripe, a short stripe or via, its granular structure, the number of metal layers, etc.

For mechanical stresses caused by temperature cycling, etc., they are typically modeled by power law forms, not Arrhenius. These failure mechanisms will not have a definable thermal activation energy. Annex A.4.2 provides additional discussion and references on mechanical stress.

## Table 1 — First order estimates semiconductor failure mechanism activation energies

| General Failure Mechanism Class | Activation energies Typ. (eV) | Min. (eV) | Max. (eV) | Other Factors/References (Note b) |
|---|---|---|---|---|
| Surface / Oxide | 1.0 | 0.75 | 1.40 | A.1 |
| Hot carriers | see A.2 | | | A.2 |
| Charge loss in dynamic memory | 0.6 | 0.50 | 1.30 | |
| Dielectric Breakdown | | | | γ = 3.2<br>A.3.1<br>A.3.2<br>Ref. a3-2 |
| field >0.04 micron thick | 0.3 | 0.20 | 1.0 | |
| field ≤0.04 micron thick | 0.7 | 0.28 | 1.0 | |
| Metallization Electromigration | | | | |
| Aluminum, alloys, and multi-layer Aluminum. See A.4 for details. | 0.6 | 0.5 | 0.7 | Current Density factor N=2.0<br>A.4.1 |
| Stress voiding | see A.4.2 | | | A.4.2 |
| Corrosion - Chlorine | 0.70 | 0.53 | 0.95 | |
| Corrosion - Phosphorus | 0.53 | 0.30 | 0.80 | |
| Wafer Fabrication | | | | |
| chemical contamination | 1.00 | 1.00 | 1.00 | |
| silicon/crystal defects | 0.50 | 0.30 | 0.50 | |

## Table 2 — Failure mechanisms/activation energies

| Failure Mechanism | (eV) | $J^{-N}$ | V | RH | Ref |
|---|---|---|---|---|---|
| Surface / Oxide | | | | | |
| Surface Inversion | 1.0 | No | Yes | Yes | |
| Mobile Ions | 1.0 | No | Yes | Yes | |
| Charge Accumulation | 1.0 | No | No | No | |
| Mobile Ion Diffusion | | | | | |
| Along Aluminum Lines | 1.0 | No | Yes | No | |
| Diffusion through PSG | 1.4 | No | Yes | No | |
| Bit-To-Bit spreading | 1.8 | No | Yes | No | |
| Charged Contamination | 1.0 | No | Yes | No | |
| Surface Charge spreading | 0.7 | No | No | No | |
| Charge Loss in Dynamic Memory | 0.6 | No | No | No | |
| Charge Loss in EPROMs | 1.0 | No | No | No | |
| Leakage in $SiO_2$ | 1.0 | No | No | No | |
| Inversion | 1.0 | No | No | No | |
| Refresh Degradation | 0.6 | No | No | No | |
| Dielectric Breakdown - Electric Field Induced | | | | | A.3 |
| General Relationship (Burn-in End of Life) | 0.7 | No | 3.2 | No | |
| Charge Trapping (EEPROMs) | 0.12 | Yes | Yes | No | |
| Dielectric Breakdown - Stress Induced. | | | | | |
| General Relationship | No | No | No | No | A.6 |
| Metal Corrosion - General | | | | | |
| General Assumption | 0.8 | No | No | Yes | A5 |
| Chlorine - In Plastic Pkge | 0.7 | No | No | Yes | A5 |
| Chlorine - In Water | 0.3 | No | No | Yes | A5 |
| Phosphorus | 0.53 | No | No | Yes | A5 |

| Failure Mechanism | (eV) | $J^{-N}$ | V | RH | Ref |
|---|---|---|---|---|---|
| Assembly Processes | | | | | |
| Intermetallics | | | | | |
| Bromide-induced | 1.0 | No | No | No | |
| Halide-induced | 0.5 | | | | |
| Chloride-induced | 0.8 | | | | |
| Wire Bond Failure | 0.75 | | | | |
| Wire Bond Failure (Wedge) | 0.45 | | | | |
| Wire Failure | 0.45 | | | | |
| Die Attach Failure | 0.30 | | | | |
| Scratched Passivation | | | | | |
| Die Cracked | 1.00 | | | | |
| Passivation Cracks | 0.45 | | | | |
| Contamination on Surface | 1.00 | | | | |

NOTES —

a. Industry sources show a range of values for many of these failure mechanism activation energies. The JEDEC committee has agreed upon a single value for each of these as a worst-case likely value for use as an industry suggestion to provide consistency and comparisons.

b. The references listed in this table that refer to annex A will be preceded by an A. Those that refer to one or more of the notes will list only the numbers.

c. In table 2, eV stands for thermal activation energy electron-volts, $J^{-N}$ denotes current density factors, V is used to denote any voltage or field factors, and RH is relative humidity in %.

## Annex A - Rationale

Some of the rationale behind the activation energies proposed follow in these notes and comments. In addition, each subject has a short bibliography attached to it to provide specific references on it. The subjects discussed are as follows:

A.1 Mobile Ions
A.2 Hot Electrons
A.3 Field Induced Dielectric Breakdown
A.4 Metallization
  A.4.1 Electromigration
  A.4.2 Stress Voiding
A.5 Metal corrosion
A.6 Mechanical Stress-Induced Dielectric Breakdown
A.7 EPROM Data Loss

### A.1 Comment - Mobile ions

The classification of mobile ions includes charges found in the silicon, at the silicon-oxide interface, in the dielectric oxides or the passivation oxides whose mobility increases as a function of temperature and whose ionic drift is towards opposite electrical charges, when they exist. What distinguishes these charges from other forms of oxide impurities is that they remain mobile after drifting and will "recover" after the bias is removed but will repeat the drift phenomenon when bias is reapplied. When the impurity density of the mobile ion is close enough to the density of the doped impurities that ionic drift towards an oppositely charged pole will "invert" (i.e., become the dominant doping impurity) the charge in a localized region of the microprocessor causing it to fail by conducting or leaking charges where it wasn't designed to occur. The result of the ionic drifting would be modified transistor characteristics that affect the circuit timing or total circuit function.

Ions that have been identified and studied include sodium, lithium and potassium. Mobile ions can be "passivated" (i.e., neutralized) by doping the surrounding oxide with oppositely charged ion such as phosphorus. The most plausible solution is to assure that the microcircuit processes keep their level of these ionic impurities low enough so that no level of overdoping is possible.

Other charges such as oxygen, hydrogen, etc., can initiate similar drift characteristics in the finished product but seldom will fail, recover through a bake, and then refail, as many times as the process is repeated, as truly mobile ions do.

As knowledge of these charges grew and the methods used to detect them in the process and in the materials used in processing microcircuits became more sophisticated, the mobile ion impact has diminished.

Sodium has been the most troublesome mobile ion. It is found everywhere and too often has corrupted process devices. It also has the lowest activation energy. In a pure form, sodium's lowest activation energy is about 0.7 eV. However, as reported in the literature[a1-11],[a1-3], the activation energy for the sodium ion ($Na^+$) is a function of the percentage of phosphorus doping in the oxide and the polarity of the applied bias. Reported values for the $Na^+$ ion are from 0.68 eV[a1-3] for oxides with no phosphorus impurities in them to 1.93 eV for the case where there was 8% $P_20_5$ concentrations (mol %) of impurities present[a1-11]. The recovery activation energy was reported[a1-11] to be 0.8 eV for sodium. In microcircuits, where the rate of occurrence is influenced by a number of variables, the consensus activation energy is 1.0 eV.

The following references are included to give more insight into how this failure mechanism has been treated over the years. They are arranged by date of publication.

**References:**

a1-1 **Evaluation of Modern Gate Oxide Technologies to Process Charging**, (Proceedings of the 31st Annual International Reliability Physics Symposium, 1993), pp. 255-261

a1-2 **Interface Degradation and Dielectric Breakdown of Thin Oxides Due to Homogeneous Charge Injection**, (27th Annual International Reliability Physics Symposium, 1989), pp. 17-21

a1-3 **MOS (Metal Oxide Semiconductor) Physics and Technology**, (Published by John Wiley & Son, 1982

a1-4 **Stability of MOSFET Devices with Phosphorus-Doped Oxide as Gate Dielectric**, (Solid State Science and Technology, December 1977), pp. 1897-1900

a1-5 **Charge Effects and Other Properties of the Si-$SiO_2$ Interface: The Current Understanding**, (The Third International Symposium on silicon Materials Science and Technology (Electrochemical Society) Philadelphia, PA, May 1977), pp. 1-18

a1-6 **Effect of Electron Trapping on IGFET Characteristics**, (Journal of Electronics Materials, Vol. 6, No. 2, 1977), pp. 65-76

a1-7 **Electron Trapping at Positively Charged Centers in $SiO_2$**, (Applied Physics Letters, Vol. 26, No. 5, March 1975), pp. 248-250 a1-8 **The Current Understanding of Charges in the Thermally Oxidized Silicon Structure,** (The Journal of the Electrochemical Society, Vol. 12, No. 6, 1974), pp. 198-205

a1-9 **ION Instabilities in MOS Structures,** (12th Annual International Reliability Physics Symposium, 1974), pp. 250-258

a1-10 **Interface Instabilities** (1974), (12th Annual International Reliability Physics Symposium, 1974), pp. 267-272

a1-11 **A Review of Instability Mechanisms in Passivation Films,** (8th Annual International Reliability Physics Symposium, 1970), pp. 1-8

a1-12 **Polarization Effects in Insulating Films on Silicon - A Review,** Transactions of the Metallurgical Society of AIME, Vol. 242, March 1968), pp. 512-523

## A.2 Comment - Hot carriers

The hot-carrier effect is a high-energy-carrier-induced transistor performance degradation. It arises from the high energy acquired by electrons and holes moving from source to drain in a MOSFET channel. The electric field accelerating the carriers has increased with each succeeding generation of process technology because transistor dimensions have scaled faster than operating voltages. The high energy of the channel carrier leads to a gradual shift in the transistor characteristics through generation of interface states and charge trapping in the gate oxide. As the transistor characteristics change, the overall circuit performance is degraded. Hot carrier effects are strongly accelerated by increasing operating voltage. Hot carrier effects are not described by a thermal activation energy, because these effects accelerate with decreasing temperature.

The temperature deceleration is small compared with the voltage acceleration, typically increasing by less than a factor of 10 as the temperature is increased from 0 to 100 °C.

**References:**

a2-1 **Temperature Dependence of Hot-Electron Degradation in Bipolar Transistors,** (IEEE Electron Device Letters, Vol. EDL-40, No. 9, September 1993), pp. 1669-1674

a2-2 **Dynamic Effects in Hot-Carrier Degradation and their Relevance for CMOS Operation,** (31st Annual Proceedings, International Reliability Physics Symposium, Tutorial, 1993), pp. 1a.1-1a.23

a2-3 **Temperature Dependence of Channel Hot-Carrier Degradation in N-Channel MOSFETs,** (Journal of Electron Devices, Vol. ED-37, April 1990), pp. 980- 992

a2-4 **The Effect of Channel Hot-Carrier Stressing on Gate-Oxide Integrity in MOSFETs,** (IEEE Transactions on Electron Devices, Vol. ED-35, No. 12, December 1988), pp. 2253-2257

a2-5 **Accelerated Testing of MOSFET Lifetime due to Hot Carrier Induced Degradation**, 27th Annual Proceedings, International Reliability Physics Symposium, Tutorial, 1987), pp. 7.1-7.22

a2-6 **A Model for Electric Field in Lightly Doped Drain Structures,** (IEEE Transactions on Electron Devices, Vol. ED-34, No. 7, July 1987), pp. 1509-1518

a2-7 **50-Å Gate-Oxide MOSFETs at 77 K,** (IEEE Transactions on Electron Devices, Vol. ED-34, No. 10, October 1987), pp. 2129-2135

a2-8 **Operation of CMOS Devices with a Floating Well,** (IEEE Transactions on Electron Devices, Vol. ED-34, No. 2, February 1987), pp. 335-342

a2-9 **Inversion-Layer Capacitance and Mobility of Very Thin Gate-Oxide MOSFETs,** (IEEE Transactions on Electron Devices, Vol. ED-33, No. 3, March 1986), pp. 409-413

a2-10 **Hot-Carrier Damage Mechanisms,** (26th Annual Proceedings, International Reliability Physics Symposium, Tutorial, 1986), pp. 1.1-1.21

a2-11 **Temperature Dependence of CMOS Device Reliability,** (24th Annual Proceedings, International Reliability Physics Symposium, 1986), pp. 175-182

a2-12 **Electrical Breakdown in Thin Gate and Tunneling Oxides,** (IEEE Transactions on Electron Devices, Vol. ED-32, No. 2, February 1985), pp. 413-422

a2-13 **Hot-Electron-Induced MOSFET Degradation - Model, Monitor, and Improvement,** (IEEE Transactions on Electron Devices, Vol. ED-32, No. 2, February 1985), pp. 375-385

a2-14 **Hot-Electron-Induced MOSFET Degradation at Low Temperatures,** (IEEE Electron Device Letters, Vol. EDL-6, No. 9, September 1985), pp. 450-452

a2-15 **Temperature Dependence of Hot-Electron-Induced Degradation in MOSFETs,** (IEEE Electron Device Letters, Vol. EDL-5, No. 5, May 1984), pp. 148-150

a2-16 **Impact Ionization of Electrons in Silicon (Steady State),** (Journal of Applied Physics, Vol. 54, No. 9, September 1983), pp. 5139-5144 a2-17 **Theory of Hot Electron Emission from Silicon into Silicon Dioxide,** (Journal of Applied Physics, Vol. 54, No. 9, September 1983), pp. 5145-5151

a2-18 **Generation of Interface States by Hot Hole Injection in MOSFETs** (IEEE Transactions on Electron Devices, Vol. ED-29, No. 5, May 1982), pp. 913-918

a2-19 **Behavior of the Si/SiO$_2$ Interface Observed by Fowler-Nordheim Tunneling,** (Journal of Applied Physics, Vol. 53, No. 1, January 1982), pp. 559-567

a2-20 **Hot-Electron Injection into the Oxide in N-Channel MOS Devices,** (IEEE Transactions on Electron Devices, Vol. ED-28, NO. 3, March 1981), pp. 328-340

a2-21 **Hot-Electron Emission in N-Channel IGFETs,** (IEEE Journal of Solid State Circuits, Vol. SC-14, No.2, April 1979), pp. 442-455

a2-22 **Leakage-Induced Hot Carrier Instability in Phosphorus-Doped SiO$_2$ Gate IGFET Devices,** (15th Annual Proceedings, International Reliability Physics Symposium, 1977), pp. 5-9

## A.3 Comment - Field-induced dielectric breakdown

Simple oxide dielectric breakdown is only slightly temperature-sensitive but is highly voltage-sensitive as the strength of the electric field approaches the dielectric strength of the oxide. Developing the acceleration factor for this family of mechanisms requires that the total dielectric breakdown acceleration factor $A_{ox}$ (for field-induced dielectric breakdown) be the product of the two acceleration factors $A_T$ (with temperature in kelvins) and $A_f$ (with field in MV/cm).

Two widely used models for dielectric breakdown, plus several others that are less widely used, are discussed in the literature. Users of the information contained in this document are encouraged to conduct experiments that determine $E_a$ for the particular process and operating conditions of interest. These experimental results are the best means by which the most accurate lifetime predictions are obtained.

### A.3.1 Proportional model (ε-Model)

It has been shown [a3-16] that the electric field acceleration factor ($A_f$) for SiO$_2$ is an inverse function of absolute temperature. It is also shown that the effective activation energy for SiO$_2$ stressing varies in a linear manner as a function of the difference between the field strength at the median ($t_{50}$) breakdown point for the intrinsic oxide and the test or operating stress field.

The equations for the field acceleration and the thermal acceleration factors are:

$$A_f = e^{\gamma(\varepsilon_t - \varepsilon_s)} \qquad (A.1)$$

$$A_T = e^{\frac{E_a}{\kappa}\left(\frac{1}{T_s} - \frac{1}{T_t}\right)} \qquad (A.2)$$

where

$A_f$ = the acceleration factor due to electric fields.
$A_T$ = the acceleration factor due to temperature.
$\gamma$ = the field acceleration parameter, which is temperature-dependent.
$\varepsilon_t$ = electrical field applied during the test.
$\varepsilon_s$ = electrical field during system operation.
$T_s$ = normal operating temperature in kelvins.
$T_t$ = test temperature in kelvins .
$E_a$ = activation energy due to temperature.

Since these are dependent factors, the expression for accelerated failure for field induced dielectric breakdown must be the product of the acceleration factor for temperature and voltage, as follows:

$$A_{ox} = A_T \times A_f \qquad (A.3)$$

That, by substitution, becomes

$$A_{ox} = e^{\gamma(\varepsilon_t - \varepsilon_s)} \cdot e^{\frac{E_a}{\kappa}\left[\frac{1}{T_s} \frac{1}{T_t}\right]} \qquad (A.4)$$

At $T_a = 125°C$, $E_a = 0.3$ eV and $\gamma = 7.4$ cm/MV for fields of 7.5 MV/cm. At fields below 5 MV/cm, more typical of systems operations, a value of 6.45 cm/MV is used for $\gamma$.

### A.3.2 Inverse proportional model (1/ε-Model)

In Modeling and Characterization of Gate Oxide Reliability [a3-9] it is proposed that the physical process that created the oxide filaments that lead to failure by the breakdown of the oxide were described by theory that requires the time to breakdown ($t_{bd}$) to be an inverse function of strength of field. In the proposed equation[a3-9], the electrical field acceleration factor ($A_f$) is the slope of the log of the time to breakdown ($t_{bd}$) versus $1/\varepsilon_{ox}$ and is equal to the expression

$$A_f = \frac{-(B+H)}{2.30\,\varepsilon^2_{ox}} \qquad \text{(A.5)}$$

where

$\varepsilon_{ox}$ = the value of the field stress on the oxide.

$B$ = the coefficient in the Fowler-Nordheim current density equation ($J \propto e^{-B/\varepsilon_{ox}}$), a value of 240 MV/cm.

$H$ = the coefficient in the hole generation current expression $ae^{-H/E_{ox}}$, a value of 80 MV/cm.

These parameters are fitted into the following expression for the intrinsic breakdown model due to field stress:

$$t_{bd} = \tau\, e^{\frac{(B_o+H_o)}{\varepsilon_{ox}}} = \tau \times e^{\frac{(B_o+H_o)(X_{ox}-\Delta X_{ox})}{V_{ox}}} \qquad \text{(A.6)}$$

In equation A.6, $X_{ox}$ and $X_{ox} - \Delta X_{ox}$ represent the thickness of the oxide ($X_{ox}$) and the change in oxide thickness ($\Delta X_{ox}$) due to defects. $V_{ox}$ is the voltage applied across the oxide. The field stress is a measure of the voltage ($V_{ox}$) applied across an oxide whose thickness is $X_{ox}$. ($B_0 + H_0$) is the value of B+H at room temperature. τ is the intrinsic breakdown time of the oxide.

To account for thermal factors, the model in reference [a3-9] expresses the temperature dependence of the factors B and H as shown in the next equation:

$$B + H = (B_0 + H_0) \cdot (M_1 + \frac{E_a'}{\kappa T}) \qquad \text{(A.7)}$$

In practice, the values of B + H may vary as a function of the oxide process, thickness, etc. $E_a'$ and $\kappa$ refer to the thermal characteristics of the Arrhenius Model, the thermal activation energy ($E_a$) and Boltzmann's constant ($\kappa$). $M_1$ is an adjustable fitting parameter.

By substitution, $t_{bd}$ becomes:

$$t_{bd} = \tau \times e^{\frac{(B_o + H_o)(M_1 + \frac{E_a'}{\kappa T})(X_{ox} - \Delta X_{ox})}{(V_{ox} - \frac{E_a'}{\kappa T})}} \qquad \text{(A.8)}$$

A value for effective $E_a$ ($E_a'$) is then:

$$E_a' = \frac{(B_o + H_o)(X_{ox} - \Delta X_{ox})E_a}{V_{ox}} - E_B \qquad \text{(A.9)}$$

$E_B$ is the constant for temperature dependence of the hole-generation coefficient.

### A.3.3 Other methods

Since the mid-eighties, other equations have been presented to address oxide thicknesses below 20 nm. It is not recommended that the above equations be applied to oxides of less than 20 nm unless experimental data has been generated to show their applicability to those oxides. The subject of oxide breakdown is very dynamic and will remain so for many more years. In response to a JEDEC ballot[2], it was pointed out that the $1/\varepsilon$-model does not yield a simple acceleration factor. A simple equation that can be used to calculate values of $t_{bd}$ at operating voltage:

$$t_{bd} = C \times \left(\frac{t_t}{C}\right)^{\frac{\varepsilon_t}{\varepsilon_s}} \qquad \text{(A.10)}$$

where C is a constant = $10^{-11}$ for silicon[3]. C is not a universal constant and has no verified processes or technology[3,4].

---

[2] **Comments to JC-14.1-91-122A,** Dec. 2, 1991.

[3] **Bimodal Lifetime Distributions of Dielectrics for Integrated Circuits,** (Qual. Reliab. Eng. Int. Vol. 7, No. 4, 1991) pp 299-305

[4] **Consistency of Lifetime Extrapolation Models Applied to ONO Triple Layers,** (Proceedings of 2nd ESREF, Bourdeaux 1991), pp 247-254

## References:

a3-1 **Hole Injection Oxide Breakdown Model for Very Low Voltage Lifetime Extrapolation,** (31st Annual Proceedings, International Reliability Physics Symposium, 1993), pp. 7-12

a3-2 **A Lifetime Projection Method Using Series Model and Acceleration for TDDB Failures of Thin Gate Oxides,** (31st Annual Proceedings, International Reliability Physics Symposium, 1993), pp. 1-6

a3-3 **$SiO_2$ TDDB Testing and Burn-In,** (30th Annual Proceedings, International Reliability Physics Symposium, Tutorial, 1992), pp. 5.1-5.32

a3-4 **Estimation of Thin-Oxide Reliability Using Proportional Hazards Models,** (IEEE Transactions on Reliability, Vol. 39, No. 3, August 1990), pp. 329-335

a3-5 **Projecting Gate Oxide Reliability and Optimizing Reliability Screens,** (IEEE Transactions on Electron Devices, Vol. ED-37, No. 7, July 1990), pp. 1643-1650

a3-6 **Time Dependent Dielectric Breakdown of 210Å Oxides,** (27th Annual International Reliability Physics Symposium, 1989), pp. 1-8

a3-7 **The Phenomenology of Dielectric Breakdown in Thin Silicon Dioxide Films: Al Cathodes and P-Type Si Anodes,** (Journal of Applied Physics, Vol. 66, No. 7, October 1989) pp. 3355-3370

a3-8 **A Study of the Breakdown Testing of Thermal Silicon Oxides and the Effects of Preoxidation Surface Treatment,** (27th Annual International Reliability Physics Symposium, 1989), pp. 9-16

a3-9 **Modeling and Characterization of Gate Oxide Reliability,** (IEEE Transactions on Electron Devices, Vol. ED-35, No. 12, December 1988), pp. 2268-2278 and, **Statistical Modeling of Silicon Dioxide Reliability,** (26th Annual Proceedings International Reliability Physics Symposium, 1988), pp. 131-138

a3-10 **High-Field-Induced Degradation in Ultra-Thin $SiO_2$ Films,** (IEEE Transactions on Electron Devices, Vol. 35, No. 12, December 1988), pp. 2259-2267

a3-11 **Oxide Reliability in VLSI Technology,** (24th Annual Proceedings, International Reliability Physics Symposium, Tutorial Notes, 1986), pp. 6.1-6.17

a3-12 **Electrical Breakdown in Thin Gate and Tunneling Oxides,** (IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, February 1985), pp. 333-341 a3-13 **A Quantitative Physical Model for Time-Dependent Breakdown,** (23rd Annual International Reliability Physics Symposium, 1985), pp. 24-31

a3-14 **Reliability of 6-10 mm Thermal $SiO_2$ Films Showing Intrinsic Dielectric Studies,** (IEEE Transactions on Electron Devices, Vol. ED-32, No. 11, November 1985), pp. 2485-2491

a3-15 **Thin Oxide Reliability**, IEDM 1985, Invited Paper, pp. 14.1

a3-16 **Acceleration Factors for Thin Gate Oxide Stressing**, (23rd Annual Proceedings, International Reliability Physics Symposium, 1985), pp. 1-5

a3-17 **A Non-Aging Screen to Prevent Wearout of Ultra-Thin Dielectrics**, (23rd Annual International Reliability Physics Symposium, 1985), pp. 6-10

a3-18 **Time-Dependent Dielectric Breakdown of Thin Thermally Grown $SiO_2$ Films.** (IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, February 1985), pp. 343-348

a3-19 **Low Field Time Dependent Dielectric Breakdown,** (17th Annual Proceedings, International Reliability Physics Symposium, 1979), pp. 8-12

a3-20 **Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown,** (17th Annual Proceedings, International Reliability Physics Symposium, 1979), pp. 1-7

a3-21 **Acceleration Factors for Thin Gate Oxide Stressing**, IRPS, pp 1-5, 1985.

a3-22 **The Dependence of the $SiO_2$ Defect Density on both the Applied Electric Field and the Oxide Thickness**, (Solid-State Science and Technology, Journal of the Electrochemical Society, October 1979), pp. 1771-1779

## A.4 Comments - Metallization

### A.4.1 Electromigration equation

$$MTTF = A \cdot J^{-N} \cdot e^{\left(\frac{E_a}{\kappa T}\right)} \qquad (A.11)$$

where

$A$ = Prefactor with complex dependence upon grain size, line structure and geometry, test conditions, current density, thermal history, etc.
$J$ = Current density

$N$ = 1 to 14 in literature. The accepted number today is N = 2 for current densities in the range of 1 to 2 X $10^6$ A/cm$^2$. However, variations in residual stress will cause N to range from 1 to 2.

Formula (A.11) which is referred to as the Black Formula inherently assumes a single activation energy $E_a$ independent of temperature and line width. This assumption is legitimate when the line width is much larger than the finite grain size of metallizations such that the effect of finite grain size on the mass diffusion mechanisms can be ignored. For the line width on the order of the median grain size or below, there has been no well-accepted model to predict the electromigration MTTF up to the moment of writing this document. However, two models, one based more on a statistical consideration [1] and another based more on a physical consideration [2,3], have been proposed.

Mechanical stress caused by thermal expansion mismatch can produce behavior resembling a temperature dependent activation energy. The greater the tensile stress the lower the apparent activation energy. The effect is most noticeable in narrow lines under thick passivation. This effect is process dependent and can produce errors on the order of 0.1 eV.

It must be stressed that the current density exponent (N) for electromigration failure is very sensitive to the failure mode. The growth of pre-existing voids results in N = 1 behavior whereas void nucleation results in N = 2 behavior. Which behavior will dominate is a function of the mechanical stress present in the conductor. Both have been observed in similar structures depending on processing variables. The use of the incorrect value for N can produce errors of orders of magnitude in failure rate or time to failure calculations.

Summarizations of a papers study conducted by a JC-14.1 Task Group member, performed in 1990, are in the following tables. A bibliography that references the papers from which this data was summarized is included at the end of this section . The papers with published dates of 1990 or earlier were used in preparing these tables.

## Table A.4.1 — Single Layer Aluminum Metallization (OPENS)

| Percent (%) Alloy | | | Typical Activation | | |
|---|---|---|---|---|---|
| Si | Cu | Ti | Energy (eV) | Exceptions | Comments |
| 0 | 0 | 0 | 0.48 | 0.84 | large grains |
| | | | | 1.2 | glassy large grains |
| | | | | 1.33-1.48 | bulk single xtal Al |
| | | | | 1.2→0.67 | 0.49→1.43 mA/cm² (J) |
| | | | | 0.64 | slow dep. rate |
| | | | | 0.71 | tested in $H_2$ |
| | | | | 0.41 | tested in He |
| ≤1.5 | 0 | 0 | 0.50 | 0.78 | PSG passivated |
| | | | | 0.27 | $Si_3N_4$ passivated |
| | | | | 0.52 | 0.75% Si |
| | | | | 0.58 | T >125°C |
| | | | | 0.40 | T <125°C |
| 1.5 | 0 | 0 | 0.72 | 0.65 | large Si nodules |
| | | | | 0.72 | medium Si nodules |
| | | | | 0.82 | small Si nodules |
| 0 | 0.5 | 0 | 0.70 | 0.70 | 2% & 5% Cu |
| 0 | 0 | ≤1.1 | 0.51 | | |
| 0 | 0 | ≤0.6 | 0.51 | | |
| 0 | 0 | >0.6 | 0.70 | | |
| 0.75 | 0.5 | 0 | 0.70 | | |
| 1 | 2 | 0 | 0.75 | | |

### Table A.4.2 — Multiple Layer Aluminum Metallization (OPENS) [Depends on underlayer thickness]

| Percent (%) Alloy | | | | | |
|---|---|---|---|---|---|
| Si | Cu | Ti | Underlayer | Typical Activation Energy (eV) | Exceptions & Comments |
| 0 | 0 | 0 | TiN | 0.55 | Migration experiment - 0.44 fine grain 0.5% Cu 1.21 large grain 0.5 Cu |
| 0 | 0 | 0 | W | 0.52 | Extrusions |
| <1 | 0 | 0 | W, W/Ti | 0.47 | ΔR |
| 0 | <2 | 0 | W, W/Ti | 0.70 | ΔR |
| 2 | 0 | 0 | Ti | 1.67 | |
| 0 | 0 | 0 | TiW | 0.53 | Extrusions |
| 0 | 0 | 0 | TiW | 0.61 | ΔR |
| 0 | <1 | 0 | TiW | 0.71 | ΔR |
| <1 | 0 | 0 | TiW | 0.49 | ΔR |
| 0 | 0 | 0 | PolySi | 0.53 | Opens |

**Table A.4.3 — Multilevel aluminum metallization contacts to metal and substrates**

| Percent (%) Alloy<br>Al | <br>Si | <br>Cu | Underlayer | Contact To | Typical Activation Energy (eV) | Exceptions | Comments |
|---|---|---|---|---|---|---|---|
| * | | * | | W | 0.9 | M2 → M1 | Opens |
| * | 1 | 0.5 | TiN/Ti | Al,1% Si, 0.5% Cu | 1.1 ±0.1 | M2 → M1 | Opens |
| * | 0.75 | 0.5 | | $T_aSi_2/P^+$Poly | 1.1 | M1 → Gate | Opens |
| * | 1 | | | $TiSi_2$/Poly | 0.85 | M1 → Gate | Nodules |
| * | 1 | | | Poly | 0.85 | M1 → Gate | Nodules |
| * | | 0.5 | | $P^+$Poly | 0.55 | M1 → Gate | Opens |
| * | 1 | | | Si | 0.85 | M1 → Si | Leakage |
| * | 1 | | W | Si | 0.5 | M1 → Si | Opens |
| * | 1 | | $TiSi_2$ | Si | 1.1<br>1.5 | M1 → Si<br>M1 → Si | Nodules<br>Spiking |

### A.4.2 Stress voiding

"Stress Voiding" is damage due to creep from stress caused by the combination of the mismatch in the thermal coefficients of expansion of metal and dielectric and the difference in the processing temperatures. Since the kinetics of failure processes are thermally activated, but the driving force for failure is inversely proportional to the temperature difference, a highly non-Arrhenius temperature dependence results. Although appearing to have an activation energy in some narrow temperature ranges, higher temperature can actually decrease the acceleration depending on certain difficult to control process parameters. The use of an Arrhenius relation for failure times can lead to dangerously optimistic predictions. Therefore, references to an activation energy for stress voiding will not be included in this document.

Additional information may be found in the referenced paper[5]. However, these values are offered as information at this time. *There is a significant alternative position that stress voids do not follow the Arrhenius thermal model very closely and are more likely to be detected through the use of accelerated temperature cycling methods and follow power law models.*

The metallization-voids phenomenon is another failure mechanism that must be better understood.

---

[5] **Measurement of Three Dimensional Stress and Modeling of Stress Induced Migration Failure in Aluminum Interconnections,** (28th annual proceedings, International Reliability Physics Symposium, 1990), pp. 221-229

## References:

a4-1 **AC Electromigration Characterization and Modeling of Multilayered Interconnects,** (Proceeds of the 31st Annual International Reliability Physics Symposium, 1993), pp. 311-316

a4-2 **Electromigration-Induced Failure and Reliability of Metallizations in Integrated Circuits**, (Journal of Applied Physics, Vol. 74, No. 2), pp. 983-987

a4-3 **Correlation Between Highly and Moderately Accelerated Electromigration Tests,** (IEEE Electron Device Letters, Vol. 14, No. 6, June 1993), pp. 277-279

a4-4 **Electromigration in Al(Cu) Two-Level Structures: Effect of Cu and Kinetics of Damage Formation,** (Journal of Applied Physics, Vol. 74, No. 2), pp. 969-978

a4-5 **High Resolution Observation of Void Motion in Passivated Metals under Electromigration Stress,** (Materials Reliability in MicroElectronics II Symposium), pp. 33-38

a4-6 [2] **The Effects of Temperature and Microstructure on the Components of Electromigration Mass Transport**, (Proceeds of the 31st Annual International Reliability Physics Symposium, 1993), pp. 304-310

a4-7 [3] **An Electromigration Model that Includes the Effects of Microstructure and Temperature on Mass Transport**, (Journal of Applied Physics, Vol. 73 (10), 15 May, 1993), pp. 4864-4902

a4-8 **Quick Tests for Electromigration: Useful but not Without Danger**, (Materials Reliability in MicroElectronics II Symposium, 1992), pp. 77-86

a4-9 **Finite Element Analysis os SWEAT Structure with a 3-D, Nonlinear Coupled Thermal-Electric Model,** (Proceeds of the 30th Annual International Reliability Physics Symposium, 1992), pp. 232-238

a4-10 [1] **The Electromigration Failure Distribution: The Fine-Line Case,** (Journal of Applied Physics, Vol. 69, Feb. 15, 1991), pp. 2117-2127

a4-11 **Barrier Metal Effects on Electromigration of Layered Aluminum Metallization,** (Proceedings of the Seventh International IEEE VLSI Multilevel Interconnection Conference, June 1990), pp. 133-141

a4-12 **Metal-Voiding Phenomenon in Al and its Alloys,** (Proceedings of the Seventh International IEEE VLSI Multilevel Interconnection Conference, June 1990), pp. 127-132