

IEC/PAS 62182

Edition 1.0
2000-09

Preconditioning of nonhermetic surface mount devices prior to reliability testing

IECNORM.COM: Click to view the full PDF of IEC/PAS 62182:2000

PUBLICLY AVAILABLE SPECIFICATION



INTERNATIONAL
ELECTROTECHNICAL
COMMISSION



Reference number
IEC/PAS 62182

IECNORM.COM: Click to view the full PDF of IEC PAS 62182:2000

Withdrawn

EIA/JEDEC STANDARD

Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

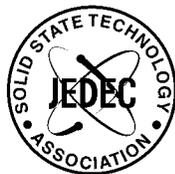
JESD22-A113-B

(Revision of Test Method A113-A)

MARCH 1999

ELECTRONIC INDUSTRIES ALLIANCE

JEDEC Solid State Technology Association



IECNORM.COM: Click to view the full PDF of IEC PAS 62182:2000

Withdrawn

INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING

FOREWORD

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public and established in an organization operating under given procedures.

IEC-PAS 62182 was submitted by JEDEC and has been processed by IEC technical committee 47: Semiconductor devices.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:

Draft PAS	Report on voting
47/1455/PAS	47/1488/RVD

Following publication of this PAS, the technical committee or subcommittee concerned will investigate the possibility of transforming the PAS into an International Standard.

An IEC-PAS licence of copyright and assignment of copyright has been signed by the IEC and JEDEC and is recorded at the Central Office.

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
- 3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
- 4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
- 5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
- 6) Attention is drawn to the possibility that some of the elements of this PAS may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

NOTICE

EIA/JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

EIA/JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

EIA/JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the EIA/JEDEC standards or publications.

The information included in EIA/JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an EIA/JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this EIA/JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
©ELECTRONIC INDUSTRIES ALLIANCE 1999
Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201-3834

"Copyright" does not apply to JEDEC member companies as they are free to duplicate this document in accordance with the latest revision of JEDEC Publication 21 "Manual of Organization and Procedure".

TEST METHOD A113-B

PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING

(From JEDEC Board Ballot JCB-98-101, under the cognizance of the JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Purpose

This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

NOTE — Correlation of moisture-induced stress sensitivity (per J-STD-020 and JESD22- A113) and actual reflow conditions used are dependent upon identical temperature measurement by both the semiconductor manufacturer and the board assembler. Therefore, it is recommended that the top of package temperature on the hottest moisture-sensitive SMD during assembly be monitored to ensure that it does not exceed the temperature at which the components are evaluated.

2 Apparatus

This test method requires as a minimum access to the following equipment.

2.1 Moisture chamber temperature

Moisture chamber(s) capable of operating at 85 °C/85% RH, 85 °C/60% RH, and 30 °C/60% RH. Within the chamber working area, temperature tolerance must be ± 2 °C and the RH tolerance must be ± 3 % RH. A chamber with 60 °C/60% RH capability is optional for accelerated soak conditions (See J-STD-020).

2.2 Solder reflow equipment

- (a) (Preferred) – 100% Convection reflow system capable of maintaining the reflow profiles required by this standard.
- (b) VPR (Vapor Phase Reflow) chamber capable of operating from 215 °C - 219 °C and/or (235 ±5) °C with appropriate fluids. The chamber must be capable of heating the packages without collapsing the vapor blanket and recondensing the vapor to minimize loss of the vapor phase soldering liquid. The vapor phase soldering fluid must vaporize at the appropriate temperature specified above.
- (c) Infrared (IR)/Convection solder reflow equipment capable of maintaining the reflow profiles required by this standard. It is recommended that this equipment use the IR to heat the air and not directly impinge upon the components under test.

NOTE — The moisture sensitivity classification test results are dependent upon the package body temperature, rather than board or lead temperature. Convection and VPR are known to be more controllable and repeatable than IR. When there are correlation problems between VPR, IR/Convection, and Convection, the Convection results shall be considered as the standard.

2.3 Optical Microscope

Optical Microscope (40x for external visual exam)

2.4 Electrical test equipment

Electrical test equipment capable of performing room temperature dc and functional tests.

2.5 Bake oven

Bake oven capable of operating at 125 +5/-0 °C.

2.6 Temperature Cycle Chamber

Temperature Cycle Chamber capable of operating as a minimum over the range of (-40 +0/-10) °C to (60 °C +10/-0) °C per JEDEC Test Method A104. Acceptable alternative test conditions and temperature tolerances are A through H of JEDEC Test Method A104, Temperature Cycling. This equipment is only required if Step 3.1.3 Shippability option is used.

3 Test Procedure

3.1 Steps

It is recommended that a prior evaluation be run according to J-STD-020, using similar devices, to determine which preconditioning sequence is appropriate, i.e. likely to pass. Other relevant moisture evaluation data may be consulted, or an arbitrary selection may be made. However, the soak sequence in step 3.1.5 must be consistent with the floor life information in Table 3.

3.1.1 Initial electrical test

Perform electrical dc and functional test to verify that the devices meet the room temperature data sheet specification. Replace any devices that fail to meet this requirement.

3.1.2 Visual Inspection

Perform an external visual examination under 40X optical magnification to ensure that no devices with external cracks or other damage are used in this test method. If mechanical rejects are found, corrective action must be implemented in the manufacturing process and a new sample must be drawn from product that has been processed with the corrective action.

3.1.3 Temperature cycling

Perform five (5) cycles of temperature cycle from $-40\text{ }^{\circ}\text{C}$ (or lower) to $60\text{ }^{\circ}\text{C}$ (or higher) to simulate shipping conditions. This step is optional.

3.1.4 Bake out

Bake the devices for 24 hours minimum at $125\text{ }^{\circ}\text{C} \pm 5\text{ }^{\circ}\text{C}$. This step is intended to remove all moisture from the package so that it will be "dry".

NOTES

- 1 This time may be modified if desorption data on the particular device being preconditioned shows that more or less time is required to obtain a "dry" package. Refer to J-STD-020 for procedures on running absorption and desorption curves.
- 2 If the preconditioning sequence is being performed by the semiconductor manufacturer, steps 3.1.1, 3.1.2, and 3.1.4 are optional since they are the supplier's risks. If the preconditioning sequence is being performed by the user, steps 3.1.7 through 3.1.9 are optional.

3.1 Steps (cont'd)

3.1.5 Soak conditions

The following soak conditions shall apply to the eight (8) levels shown in Table 3. Soak should be initiated within 2 hours of bake.

- (a) Subject Level 1 devices to 168 hours of 85 °C/85% RH.
- (b) Subject Level 2 devices to 168 hours of 85 °C/60% RH.
- (c) Subject Levels 2a through 6 to “Z” hours of 30 °C/60% RH. For use of accelerated testing at 60 °C/60% refer to J-STD-020.

Table 1 — Required Soak Times in Hours for Levels 2a - 6

Level	X	+	Y (Floor Life)	=	Z (Total Soak)
2a	24		672		696
3	24		168		192
4	24		72		96
5	24		48		72
5a	24		24		48
6	0		6		6

NOTES

- 1 X is manufacturer's exposure time (MET) and is the sum of the time between bake and dry pack plus the maximum time allowed out of the bag at the distributors
 - 2 Y is floor life of package after removal from dry pack bag
 - 3 Z is total required soak time in hours
- (d) The X values shown above are default values. If the semiconductor manufacturer's actual time between bake and bag plus the allowed time out of the bag at the distributor is greater than the default value, the actual time must be used. If the actual X value is less than 24 hours, the actual time may be used.

3.1.6 Reflow

Not sooner than fifteen (15) minutes and not longer than four (4) hours after removal from the temperature/humidity chamber, submit the devices to three cycles of the appropriate reflow conditions shown below. All temperatures refer to top surface of the package.

3.1 Steps (cont'd)

3.1.6 Reflow (cont'd)

Table 2 — Reflow Profiles

	Convection or IR/Convection	VPR
Average ramp-up rate (183 °C to Peak)	3 °C/second max.	10 °C/second max.
Preheat temperature 125(±25) °C	120 second max.	
Temperature maintained above 183 °C	60-150 seconds	
Time within 5 °C of actual peak temperature	10-20 seconds	60 seconds
Peak temperature range	(220 +5/-0) °C or (235 +5/-0) °C	215 - 219 °C or (235 +5/-0) °C
Ramp-down rate	6 °C/second max.	10 °C/second max.
Time 25 °C to peak temperature	6 minutes max	

NOTE — See J-STD-020 for appropriate peak temperature range.

The devices shall be allowed to cool at room ambient conditions for five (5) minutes minimum between VPR or IR cycles.

3.1.7 Flux application

After the reflow solder cycles are completed, allow the devices to cool at room ambient for 15 minutes minimum. Apply an activated water soluble flux to the device leads by bulk immersion of the entire parts in flux at room ambient for 10 seconds minimum.

3.1.8 Cleaning

Clean devices externally using multiple agitated deionized water rinses. No waiting time is required between flux application and cleaning.

3.1.9 Drying

Devices should be dried at room ambient prior to submission to reliability testing.

3.1.10 Final electrical test

Submit the devices to electrical dc and functional testing per the room temperature data sheet specification. (For the semiconductor manufacturer, this step is optional and may be omitted since it is a supplier's risk.) Any valid failures found at this point due to the preconditioning sequence indicate that the device may have been classified in the wrong level. Failure analysis should be conducted, and if appropriate, this device type should be reevaluated to determine the correct moisture sensitivity level. This would require resubmitting a sample to the correct level preconditioning sequence prior to reliability testing per 4.

4 Applicable Reliability Tests

SMDs should be subjected to the appropriate preconditioning sequence of this document prior to being submitted to reliability tests per JESD47 or the semiconductor manufacturers in-house reliability procedures.

5 Summary

The following details shall be specified in the applicable procurement documents:

- (a) Number of reflow cycles if other than three.
- (b) Type flux if other than Step 3.1.7.
- (c) Reliability tests if other than 4.
- (d) Test conditions and duration of reliability tests in 4.
- (e) Electrical test description, including test temperature(s).