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IC LATCH-UP TEST

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1 Scope

This specification covers the I-test and the overvoltage latch-up testing of integrated circuits.

1.1 Purpose

The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies. As used in this specification, latch-up is not related to a specific mechanism but is an electrical failure characteristic that occurs when a device is subjected to this test method.

1.2 Classification

The classification defines the latch-up test temperature. Latch-up testing classifications are defined as follows:

Class I - Latch-up testing performed at room temperature.
Class II - Latch-up testing performed at the maximum ambient rated temperature for the device.

If no classification is specified, class I testing shall be performed.

NOTE - Elevated temperature will reduce latch-up resistance, and class II testing is recommended for devices that are required to operate at elevated temperature.

1.3 Level

Level defines the failure criteria used during latch-up testing. Latch-up failure grades are defined as follows:

Level A - The failure criteria as defined in table 1.
Level B - Special failure criteria. Supplier shall provide definition of failure criteria used.

2 Definitions

The following terms and definitions apply to this test method.

2.1 Cool-down time

The period of time between successive applications of trigger pulses or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse. (See figures 2, 3, and 4 and table 2.)

2.2 DUT

The device under test.

2.3 GND (Ground)

The common or zero-potential pin(s) of the DUT.

NOTES

1 Ground pins are not latch-up tested.

2 A ground pin is sometimes called Vss.

2.4 Input pins

All address, data-in, control, V_{ref} and similar pins.

2.5 I/O (bi-directional) pins

Device pins that can be made to operate as an input or output or in a high-impedance state.

2.6 I_{supply}

The total supply current in each V_{supply} pin (or pin group) with the DUT biased as indicated in table 1.

2.7 I-test

A latch-up test that supplies positive and negative current pulses to the pin under test.

2.8 Latch-up

A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition.

NOTES

1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

2.9 Logic-high

A level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states.

NOTES

1 For digital devices, the maximum value of the high logic level voltage is used for latch-up testing.
2 For non-digital devices, the maximum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

2.10 Logic-low

A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states.

NOTES

1 For digital devices, the minimum value of the low logic level voltage is used for latch-up testing.
2 For non-digital devices, the minimum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

2.11 Maximum V_{supply}

The maximum operating voltage for operation within performance specifications.

NOTES

1 The maximum voltage is *not the absolute maximum voltage beyond which permanent damage is likely* .
2 Maximum refers to the magnitude of V_{supply} and can be either positive or negative.

2.12 "No Connect" pin

A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device.

NOTE - All "no connect" pins shall be left in an open (floating) state during latch-up testing.

2.13 Nominal I_{supply} (Inom)

The measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the test temperature as defined in section 4 and table 1.

2.14 Output Pin

A device pin that generates a signal or voltage level as a normal function during the normal operation of the device.

NOTE - Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

2.15 Preconditioned pin

A device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT.

2.16 Testing of dynamic devices

Latch-up trigger testing of a device in a known stable state, at the minimum-rated clock frequency applied to the device (see 4.2.3 for specified conditions).

2.17 Test condition

The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to the DUT during the latch-up test.

2.18 Timing-related input pin

A pin such as clock, crystal oscillator, charge pump circuit, etc., required to place the DUT in a normal operating mode.

NOTE - Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

2.19 Trigger pulse

The positive or negative current pulse (I-Test) or voltage pulse (V_{supply} overvoltage test) applied to any pin under test in an attempt to induce latch-up (see figures 2, 3 and 4).

2.20 Trigger duration

The duration of an applied pulse from the trigger source. (See figures 2, 3, and 4 and table 2.)

2.21 V_{supply} pin (or pin group)

All DUT power supply and external voltage source pins (excluding ground pins), including both positive- and negative-potential pins.

NOTES

1 Generally, it is permissible to treat equal potential voltage source pins as one V_{supply} pin (or pin group) and connect them to one power supply.
2 When forming V_{supply} pins (or pin groups), the combination of V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

2.22 V_{supply} overvoltage test

A latch-up test that supplies overvoltage pulses to the V_{supply} pin under test.

3 Apparatus and material

The apparatus required for this test method includes the following:

3.1 Latch-up tester

Test equipment capable of performing the tests as specified in this document. For devices requiring dynamic testing, the test equipment shall be capable of supplying timing signals and logic setup vectors required to control the I/O pin output states as specified in 4.2.3. The required timing signals and logic vectors may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate.

3.2 Automated test equipment (ATE)

A device tester capable of performing full functional and parametric testing of the device to the device specification requirements.

3.3 Heat source

Equipment capable of heating and maintaining the DUT at the maximum operating temperature specified in the device specification during the latch-up test.

4 Procedure

4.1 General latch-up test procedure

A sample group of six (6) devices shall be subjected to latch-up testing using the I-test and V_{supply} Overvoltage test. The use of a new sample group for each latch-up test type (I-test, and/or V_{supply} Overvoltage test) is also acceptable. All devices to be latch-up tested must have passed ATE testing to the device specification requirements. Before latch-up testing, the device continuity in the socket should be checked to avoid false latch-up failures. The latch-up test flow shall be as shown in figure 1. The devices to be tested shall be subjected to the test conditions specified in table 1 and table 2. All "no connect" pins on the DUT shall be left open (floating) at all times. All pins on the DUT, with the exception of "no connect" pins and timing related pins, shall be

latch-up tested. The Input, output and configurable I/O pins are to be tested with the I-test and the V_{supply} pins tested with the Overvoltage test. I/O pins shall be tested in all possible operating states or the worst case operating state (typically high impedance for configurable I/O pins). Dynamic devices shall be tested per 4.2.3. When a device is sufficiently complex that testing of all configurable I/O pins in the worst case condition is not practicable, the device should be conditioned with a set of vectors representative of the typical operation of the device as determined by engineering judgment. When an I/O pin cannot be tested in the high impedance state, the I/O shall be tested in a valid logic state. Untested pins and pins that could not be completely tested shall be recorded as specified in 4.2.5 and the user shall be informed of all I/O pins that were not tested or tested in all states. After latch-up testing, all devices must pass the failure criteria specified in section 5.

4.2 Detailed latch-up test procedure

4.2.1 I-test

The I-test shall be performed as follows:

1. The devices shall be subjected to the I-test as indicated in figure 1/table 1 and figures 2 & 3/table 2.
2. Bias the DUT as indicated in figure 5. All input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins, shall be tied to the maximum logic-high level specified in the device specification. Input pins used for preconditioning must be tested in their defined state (pins that are tied to a logic-high level to precondition the DUT can only be tested in the logic-high state; pins that are tied to a logic-low level to precondition the DUT can only be tested in the logic-low state). Allow the DUT to stabilize at the test temperature. Measure nominal I_{supply} (Inom) for each V_{supply} pin (or pin group, see 2.21) at this time.
3. Apply the positive current trigger (per table 1 for a duration as specified in table 2) to the pin under test.
4. After the trigger source has been removed, return the pin under test to the state it was in before the application of the trigger pulse, and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in 1.3, latch-up has occurred and power must be removed from the DUT. If latch-up has occurred, stop the test; the DUT has failed latch-up testing. Using a new part, return to step 1 and continue testing.
5. If latch-up has not occurred, after the necessary cool-down time (see table 2), repeat steps 3 & 4 for all pins to be tested (noting the exceptions stated in step 2).
6. Repeat steps 2 through 5 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the minimum logic-low level specified in the device specification.
7. Bias the DUT as indicated in figure 6 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins shall be tied to the maximum logic-high level specified in the device specification (noting the exceptions stated in step 2).
8. Apply the negative current trigger source below ground (per table 1 for a duration as specified in table 2) to the pin under test.

9. After the trigger source has been removed, return the pin under test to the state it was in before the application of the trigger pulse and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in 1.3, latch-up has occurred and power must be removed from the DUT. If latch-up has occurred, stop the test; the DUT has failed latch-up testing. Using a new part, return to step 1 and continue testing.
10. If latch-up has not occurred, after the necessary cool-down time (see table 2), repeat steps 8 & 9 for all pins to be tested.
11. Repeat steps 8 through 10 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the minimum logic-low level specified in the device specification (noting the exceptions stated in step 2).

4.2.2 V_{supply} overvoltage test

The V_{supply} overvoltage test shall be performed on each V_{supply} pin (or pin group) as indicated below. To provide a true indication of latch-up for given test conditions input pins configured as logic-high shall remain within the valid logic-high region as defined in the device specification (typically greater than 70% of the V_{supply} overvoltage test level). If input pin levels fall outside of the valid logic-high region, the device may change state causing a change in Inom and invalid test data. If a latch-up failure occurs when the input pin(s) fall outside of the valid logic-high region, engineering judgment must be used to determine whether the failure is a valid latch-up condition or a failure caused by a change in state.

1. The devices shall be subjected to the V_{supply} overvoltage test as indicated in figure 1/table 1 and figure 4/table 2.
2. Bias the DUT as indicated in figure 7. All input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins shall be tied to the maximum logic-high level specified in device specification. Input pins used for preconditioning must be tested in their defined state (pins that are tied to a logic-high level to precondition the DUT can only be tested in the logic-high state, pins that are tied to a logic-low level to precondition the DUT can only be tested in the logic-low state). Allow the DUT to stabilize at the test temperature. Measure nominal I_{supply} (Inom) for each V_{supply} pin (or pin group, see 2.21) at this time.
3. Apply the voltage trigger source (per table 1 for a duration as specified in table 2) to the V_{supply} pin (or pin group) under test.
4. After the trigger source has been removed, return the V_{supply} pin under test to the state it was in before the application of the trigger pulse and measure the I_{supply} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in 1.3, latch-up has occurred and power must be removed from the DUT. If latch-up has occurred stop the test; the DUT has failed latch-up testing. Using a new part, return to step 1 and continue testing.
5. If latch-up has not occurred, after the necessary cool-down time (see table 2), repeat steps 2 through 4 with all input pins, including bi-directional I/O pins in an input state or high impedance state, not used for preconditioning the I/O pins tied to the minimum logic-low level specified in the device specification (noting the exceptions stated in step 2).
6. Repeat steps 2 through 5 until each V_{supply} pin (or pin group) has been tested.

4.2.3 Testing dynamic devices

Devices that during normal operating conditions have a clock and/or other timing signal inputs may be latch-up tested in a static manner as indicated in 4.2.1 and 4.2.2. If the device does not show a stable I_{supply} (Inom) measurement or appears to latch up, the clock and /or other associated timing and control signals, as defined in the device specification, may be applied to the device during latch-up testing per 4.2.1 and 4.2.2. Unless otherwise specified, the clock pins and other associated timing pins used to place the device in a stable state shall not be latch-up tested while being used to stabilize the device.. The supplier shall maintain records indicating how the device was tested, as indicated in 4.2.5.

4.2.4 DUT disposition

Latch-up testing is potentially destructive. Devices used for latch-up testing shall not be used or considered as salable devices.

4.2.5 Record keeping

Data shall be recorded for each pin failure and shall include the test condition (clock frequency for dynamic devices, if used), vector set used for preconditioning, temperature, trigger condition, and latch-up I_{supply} current. Data shall also be recorded for all pins and operating states that could not be completely tested per 4.2.3. This information shall identify the pins, operating states, and reason for incomplete testing.

5 Failure criteria

A device that fails one or more of the following conditions is considered a failure:

1. Device does not pass the test requirements in 1.3.

2. Device no longer meets functional, parametric or I/V requirements of the device specification.

6 Summary

The following details shall be specified in the procurement document , if different from the requirements in this specification:

1 Class (I or II) per this document.
2 Sample size.
3 Trigger test conditions.
4 Latch-up test temperature.
5 Failure criteria (if not Level A per 1.3).
6 Pulse/Trigger conditions.
7 Vector set used to precondition the device.

TABLE 1 TEST MATRIX [7]

CLASS	TEST TYPE	TRIGGER POLARITY	CONDITION OF UNTESTED INPUT PINS	TEST TEMPERATURE (±2 °C)	V_{supply} CONDITION	TRIGGER TEST CONDITIONS [6]	FAILURE CRITERIA
I	I-TEST	POSITIVE see FIGURE 5	Max. Logic High [1]	Room temperature	Maximum operating voltage for each V_{supply} pin group per device specification	+(Inom + 100 mA) or 1.5X Inom, whichever is greater [3]	1.4 X Inom or Inom +10 mA whichever is greater [5]
			Min. Logic Low [1]				
		NEGATIVE see FIGURE 6	Max. Logic High [1]			-100 mA or -.5 X Inom, whichever is greater in magnitude [4]	
			Min. Logic Low [1]				
	V_{supply} OVER-VOLTAGE TEST	see FIGURE 7	Max. Logic High [1]			1.5 X max. V_{supply} [2]	
			Min. Logic Low [1]				
II	I-TEST	POSITIVE see FIGURE 5	Max. Logic High [1]	Maximum ambient operating temperature	Maximum operating voltage for each V_{supply} pin group per device specification	+(Inom + 100 mA) or 1.5X Inom, whichever is greater [3]	
			Min. Logic Low [1]				
		NEGATIVE see FIGURE 6	Max. Logic High [1]			-100 mA or -.5 X Inom, whichever is greater in magnitude [4]	
			Min. Logic Low [1]				
	V_{supply} OVER-VOLTAGE TEST	see FIGURE 7	Max. Logic High [1]			1.5 X max. V_{supply} [2]	
			Min. Logic Low [1]				

1. Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.

2. Current clamped at (Inom + 100 mA) or 1.5X Inom, whichever is greater. (Refer to 2.11 for max. V_{supply} definition.)

3. Voltage clamped at 1.5X max. logic high.

4. Voltage clamped at -.5X max. logic high.

5. If the trigger test condition reaches the voltage or current clamp limit and latch-up has not occurred, the pin passes the latch-up test. See paragraph 5 for complete failure definition.

6. The Inom value used for the trigger current calculation relates to the V_{supply} pin (or pin group) that supplies the I/O pin being tested.

7. The trigger conditions herein are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from this table, the trigger conditions used must be defined in the test results.

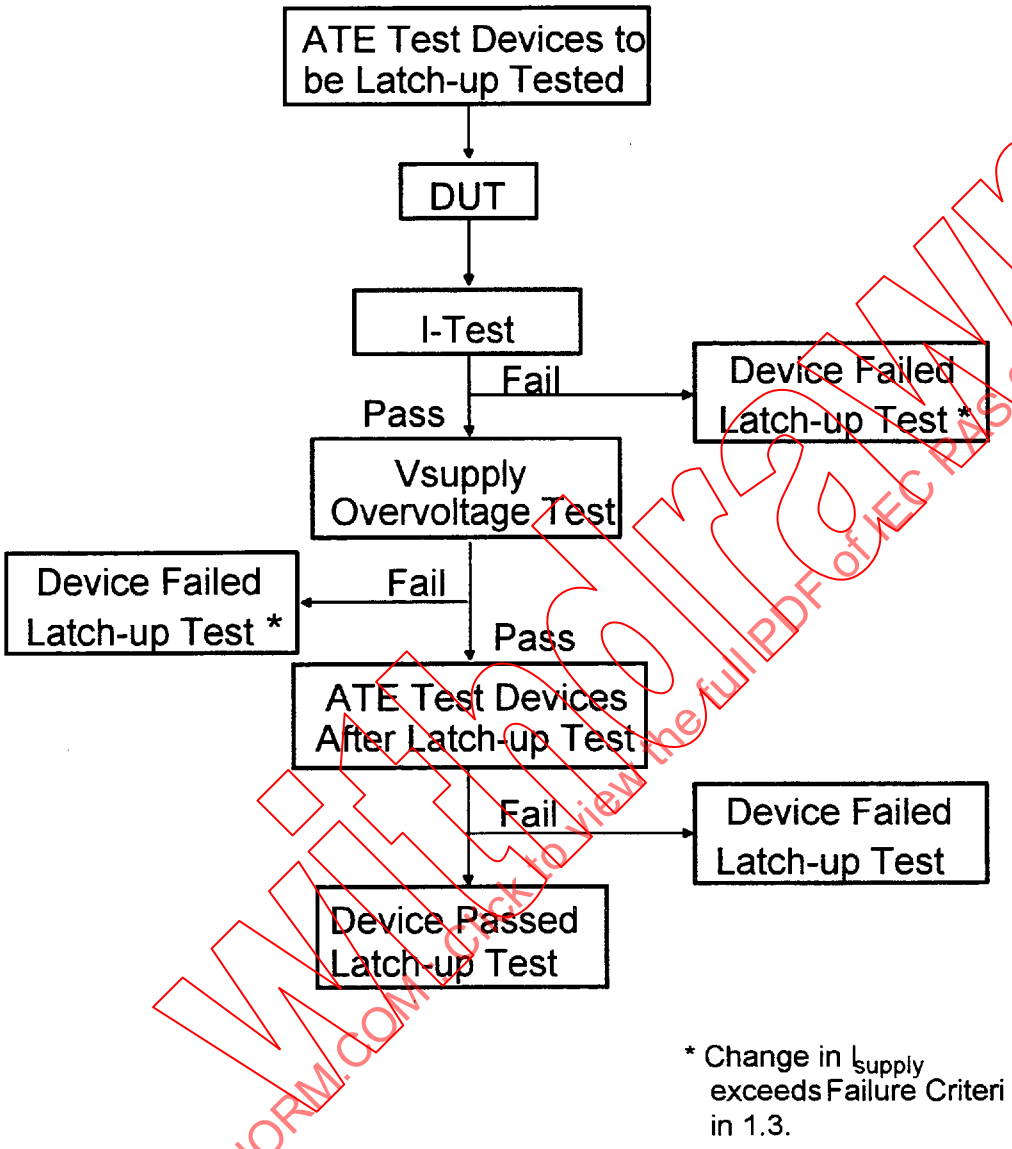
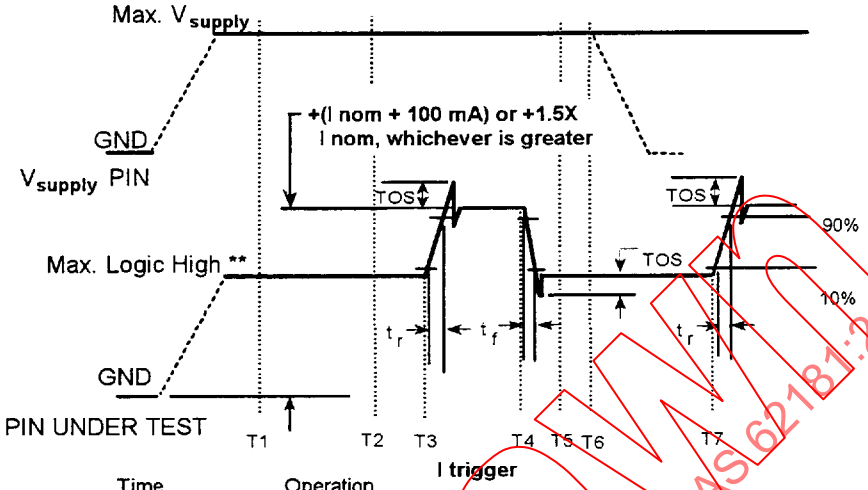


Figure 1 - Latch-up test flow

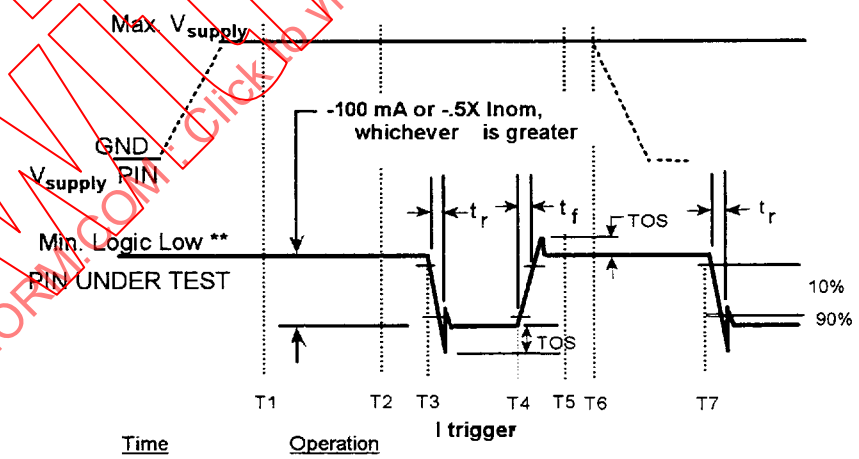


Time	Operation
T1 → T2	Measure nominal I_{supply} (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I_{supply} measurement. *
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from DUT.

* Note: The wait time shall be sufficient to allow for power supply ramp down and stabilization of I_{supply}

** Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.

Figure 2 - Test waveform for positive I-test

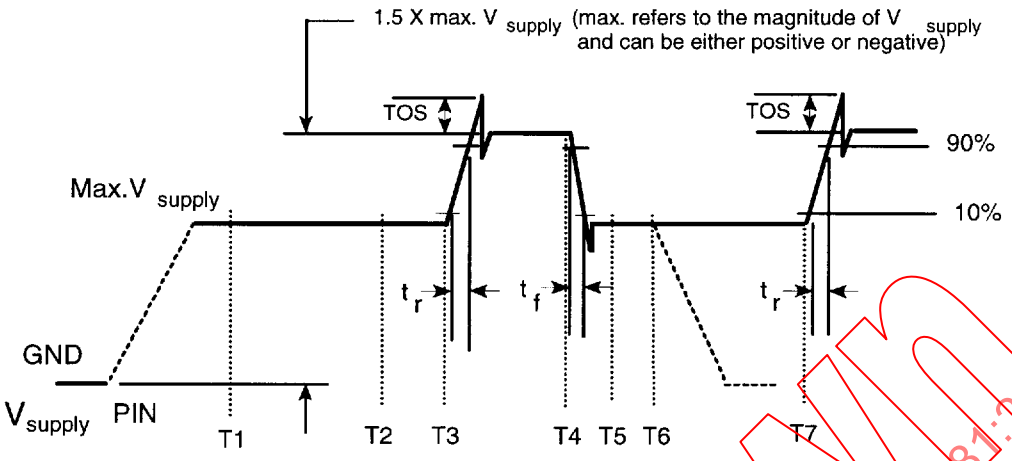


Time	Operation
T1 → T2	Measure nominal I_{supply} (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I_{supply} measurement. *
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from DUT.

* Note: The wait time shall be sufficient to allow for power supply ramp down and stabilization of I_{supply}.

** Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.

Figure 3 - Test waveform for negative I-test



Time	Operation
T1 → T2	Measure nominal I supply (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I supply measurement. *
T5	Measure I supply
T6	If any I supply ≥ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from

* Note: The wait time shall be sufficient to allow for power supply ramp down and stabilization of I supply

Figure 4 — Test waveform for V_{supply} overvoltage

Table 2 — Timing specifications for I-test and V_{supply} overvoltage test

SYMBOL	TIME INTERVAL	PARAMETER	LIMITS MIN	LIMITS MAX
t_r		trigger rise time	5 us	5 ms
t_f		trigger fall time	5 us	5 ms
Twidth	T3 → T4	trigger duration (width)	2xT_r	1 s
TOS		trigger over-shoot	± 5% of pulse voltage	
Tcool	T4 → T7	cool down time	≥ Twidth	
Tmeasure *	T4 → T5	waiting time before measuring I supply	3 ms	5 s

* Note: The wait time shall be sufficient to allow for power supply ramp down and stabilization of I_{supply} .