IEC-PAS 62085

Edition 1.0
1998-12

Implementation of Ball Grid Array and other High Density Technology

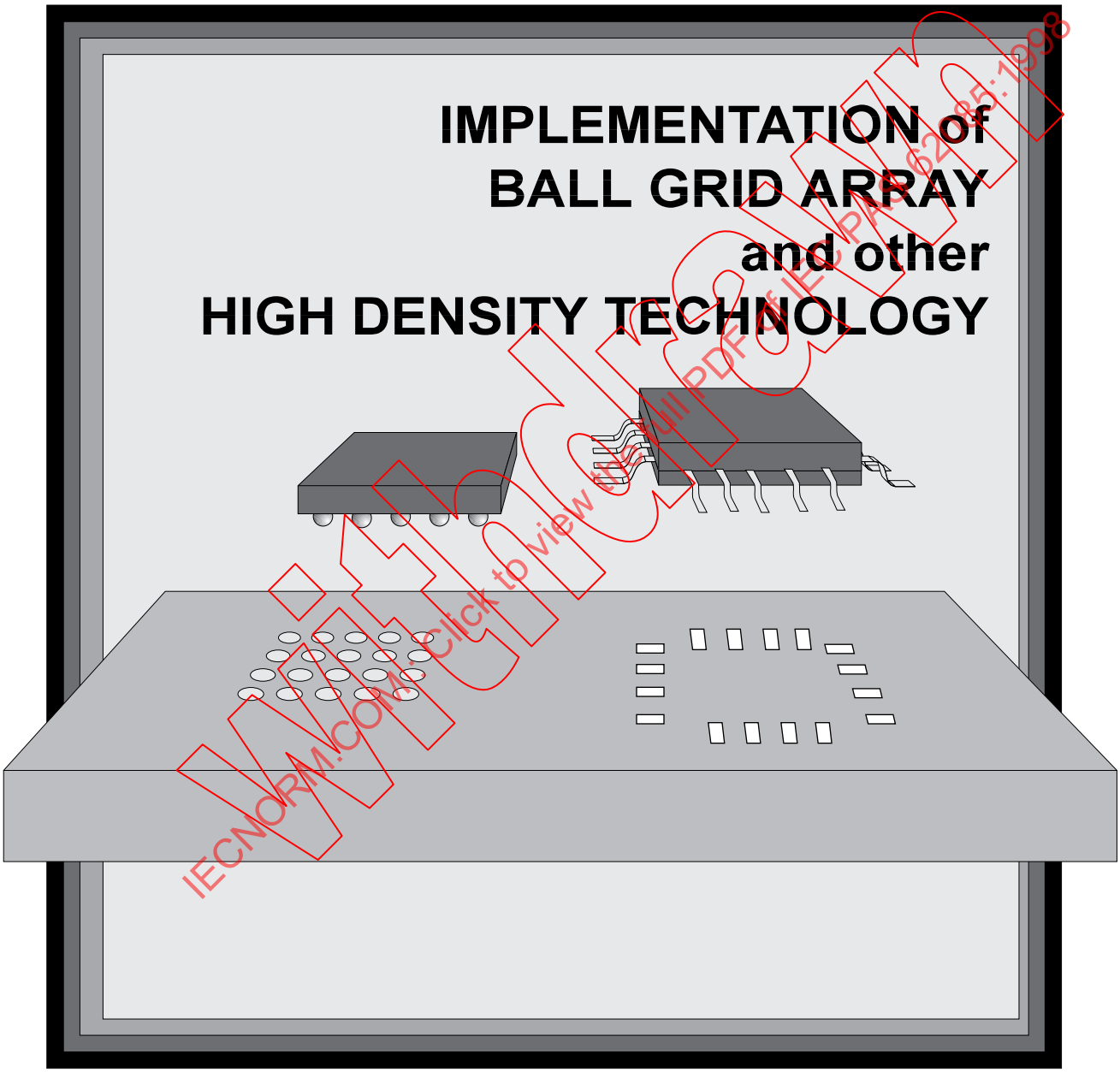
PUBLICLY AVAILABLE SPECIFICATION

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

Reference number
IEC/PAS 62085

J-STD-013
JULY 1996

JOINT INDUSTRY STANDARD



COORDINATED BY THE SURFACE MOUNT COUNCIL

IPC SEMATECH

INTERNATIONAL ELECTROTECHNICAL COMMISSION

IMPLEMENTATION OF BALL GRID ARRAY AND OTHER HIGH DENSITY TECHNOLOGY

FOREWORD

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IEC-PAS 62085 was submitted by the IPC (The Institute for Interconnecting and Packaging Electronic Circuits) and has been processed by IEC technical committee 91: Surface mounting technology.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:

Draft PAS	Report on voting
91/140/PAS	91/154/RVD

Following publication of this PAS, the technical committee or subcommittee concerned will investigate the possibility of transforming the PAS into an International Standard.

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J-STD-013 Implementation of ball grid array and other high density technology

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Material in this standard was voluntarily coordinated by the Surface Mount Council (SMC), and established by Technical Committees of IPC and EIA. Committee members of the two organizations contributed their time, knowledge and expertise to blend a cohesive report on the topic covered by this document. Proposals were sent to key individuals in each of the individual organizations for consensus. Meetings were held to resolve differences or conflicts prior to documenting the information in the final released version.

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Comments Welcome

The J-STD-013 is intended to serve as a roadmap for ball grid array and other high-density technology implementation.

In order to keep the document current, the Surface Mount Council welcomes comments from individuals reading the document, or implementing the suggested concepts.

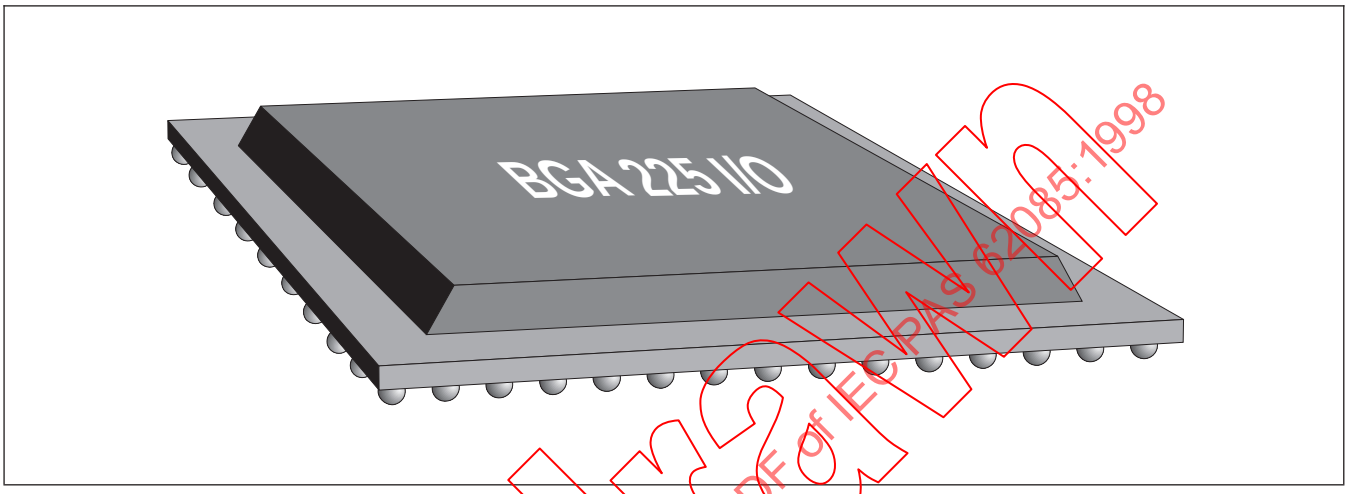
Comments may be sent to the EIA or IPC. All comments will be organized and sent to representatives of the Ad Hoc Committee responsible for the J-STD-013 for a yearly review and incorporation into the updating procedures.

Final Ballot Edition

The Surface Mount Council has authorized the special printing of this document in order to make the information available to industry experts for final ballot approval.

The official publication will be released for full industry circulation after the final editorial revision and completion of the balloting process by representatives of JEDEC. The results of those processes may initiate some changes. Once concensus has been reached, the official J-STD-013 will be printed and be supported by the three organizations, EIA, IPC, and JEDEC, and endorsed by Sematech and MCNC whose representatives participated and contributed to the development of this document.

J-STD-013
IMPLEMENTATION OF BALL GRID ARRAY AND OTHER HIGH-DENSITY TECHNOLOGY



About this Document

This document is intended to report on the work being done by a variety of organizations concerned with surface mounting of area array packages or other high pin count package configurations. The details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade association any comments or observations regarding details published in this document, or provide additional ideas and details that would serve the industry.

Section 8 of this document represents a listing of standards that are being developed, being updated, or need to be created in order to provide for the orderly implementation of Ball Grid Array, or other High-Density Technology. Members of the industry are invited to participate in the ongoing standardization process.

For additional information regarding material published herein or inquiries regarding the status of standardization activities, we urge you to contact the organization listed below.

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Acknowledgement

Any standard involving a complex technology draws material from a vast number of sources. While the principle members of the Ad Hoc committee are shown below, it is not possible to include all of those who assisted in the evolution of this document. To each of them, the members of the IPC and EIA extend their gratitude.

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A special note of appreciation goes to the representatives of Intel who provided resources for a great deal of information regarding the subject of this publication, and to Motorola whose engineering personnel provided copies of their BGA mounting methodologies.

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Implementation of Ball Grid Array and Other High Density Technology

1 SCOPE

This document establishes the requirements and interactions necessary for Printed Board Assembly processes for interconnecting high performance/ high pin count I/C packages. Included is information on design principles, material selection, board fabrication, assembly technology, testing strategy, and reliability expectations based on end-use environments.

The focus of the document is on design through testing issues related to Ball Grid Array and other high performance packages including fine pitch, ultra fine pitch and thru-hole PGA.

1.1 Purpose

The purpose of this document is to provide confidence in the Design through Testing processes to ensure that the final assembly will meet the intended goals for product performance. Reliability is established through end use environments that consider the performance requirements of assemblies that are used in electronic products in such markets as consumer, computer, telecommunication, commercial aircraft, industrial & automotive passenger compartment, military ground & ship, space (both LEO and GEO), military avionics, and automotive underhood electronics and the customary use of those equipments.

1.2 Categorization

The details contained herein are organized according to the various issues and are correlated to the specific high pin count, high performance type I/C packages. These include:

- BGA Ball Grid Array
- CBGA Ceramic Ball Grid Array
- CCGA Ceramic Column Grid Array
- TBGA Tab Ball Grid Array
- MBGA Metal Ball Grid Array
- PPGA Plastic Pin Grid Array
- PGA Pin Grid Array (Standard and Staggered Pins)
- SGA Stud Grid Array (Surface Mount Version of PGA)
- LGA Land Grid Array
  - * Plastic
  - * Ceramic
- QFP Quad Flat Pack
- CQFP Ceramic Quad Flat Pack
- SSOP Shrink Small Outline Package
- TSOP Thin Small Outline Package
- TQFP Thin Quad Flat Pack
- FQFP Fine Pitch Quad Flat Pack
- LQFP Low Profile Quad Flat Pack
- SVP Surface Vertical Package (Post Stand/ Lead Stand)

Organization of the information is initially provided in accordance to the specific processes (i.e. Design-Fabrication-Assembly-Test). Component information is organized with emphasis on area array type packages. Although there is some discussion of the peripheral format, the major emphasis is on the decision process that forces the manufacturing direction into the area array type package. Table 1-1 indicates the packages of choice in various integration of semiconductor technology. Usually the trade-offs switch from peripheral packages to array type packages at 208 pins or below 0.5 mm pitch on the peripheral package.

Table 1–1 Choice of Packages

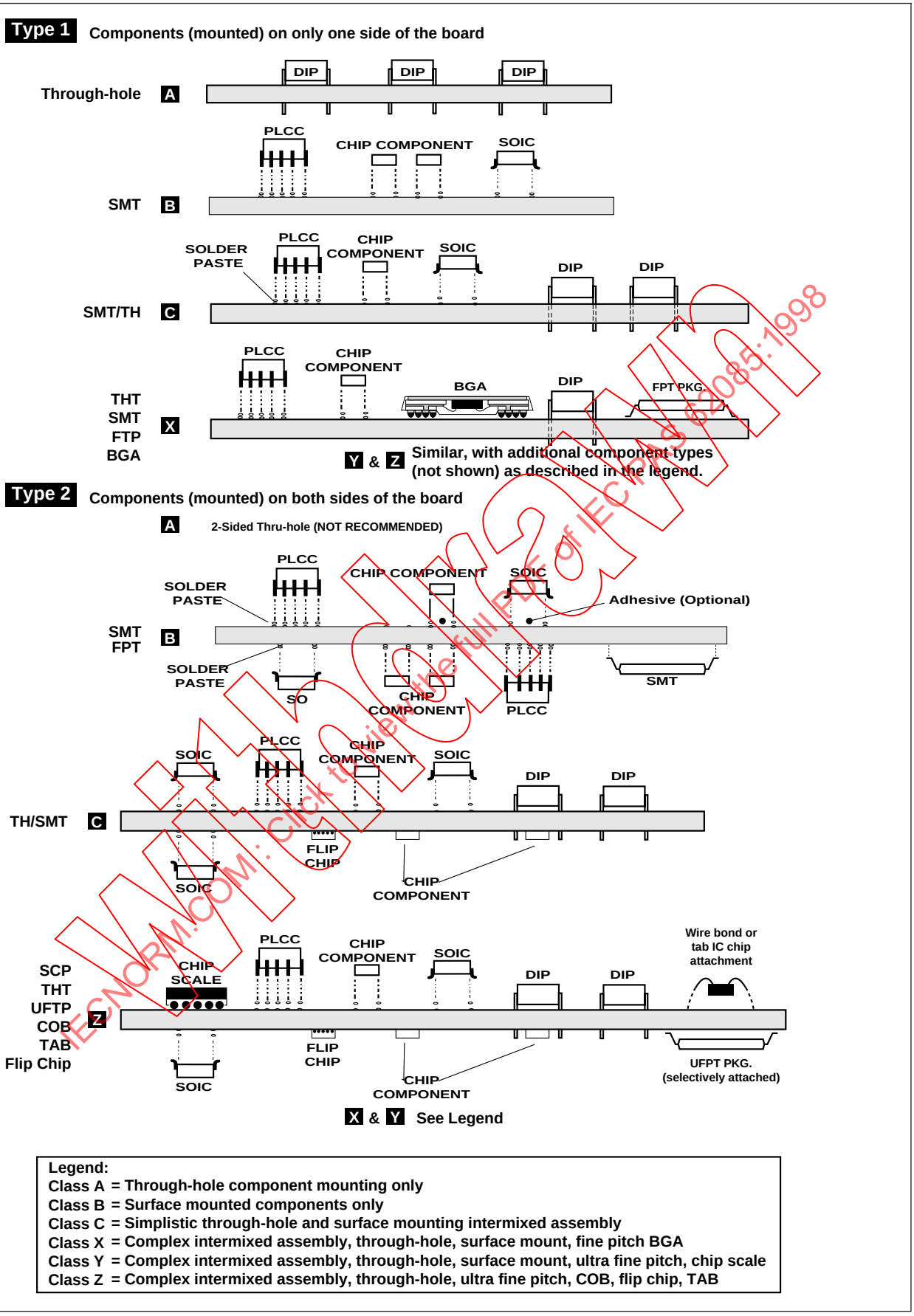
Semiconductor Integration	Number of Pins, Leads or Balls	Package Types
SSI	16-48	SOIC
MSI	48-156	QFP/PGA/BGA
LSI	156-256	BGA/QFP (0.5, 0.4, 0.3 mm pitch) and PGA
VLSI	256-500	BGA/PGA
ULSI	>500	BGA

1.3 Presentation

All dimensions and tolerances in this standard are expressed in metric units, with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off concept or the required precision. Users are cautioned to employ a single dimensioning system and not intermix millimeters and inches. Reference information is shown in parentheses ( ).

1.4 Producibility Levels

The Surface Mount Council, in their ‘‘Status of the Technology, Industry Activities and Action Plan’’ identified several levels of complexity based on manufacturing and assembly processes for electronic assembly. A differentiation was developed that correlated the ease with which an assembly process could place, and attach all the parts and test the final product. Letters were assigned to reflect progressive increases in sophistication of tooling, materials or number of processing steps.



Legend:
Class A = Through-hole component mounting only
Class B = Surface mounted components only
Class C = Simplistic through-hole and surface mounting intermixed assembly
Class X = Complex intermixed assembly, through-hole, surface mount, fine pitch BGA
Class Y = Complex intermixed assembly, through-hole, surface mount, ultra fine pitch, chip scale
Class Z = Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, TAB

Figure 1−1 Electronic Assembly Types

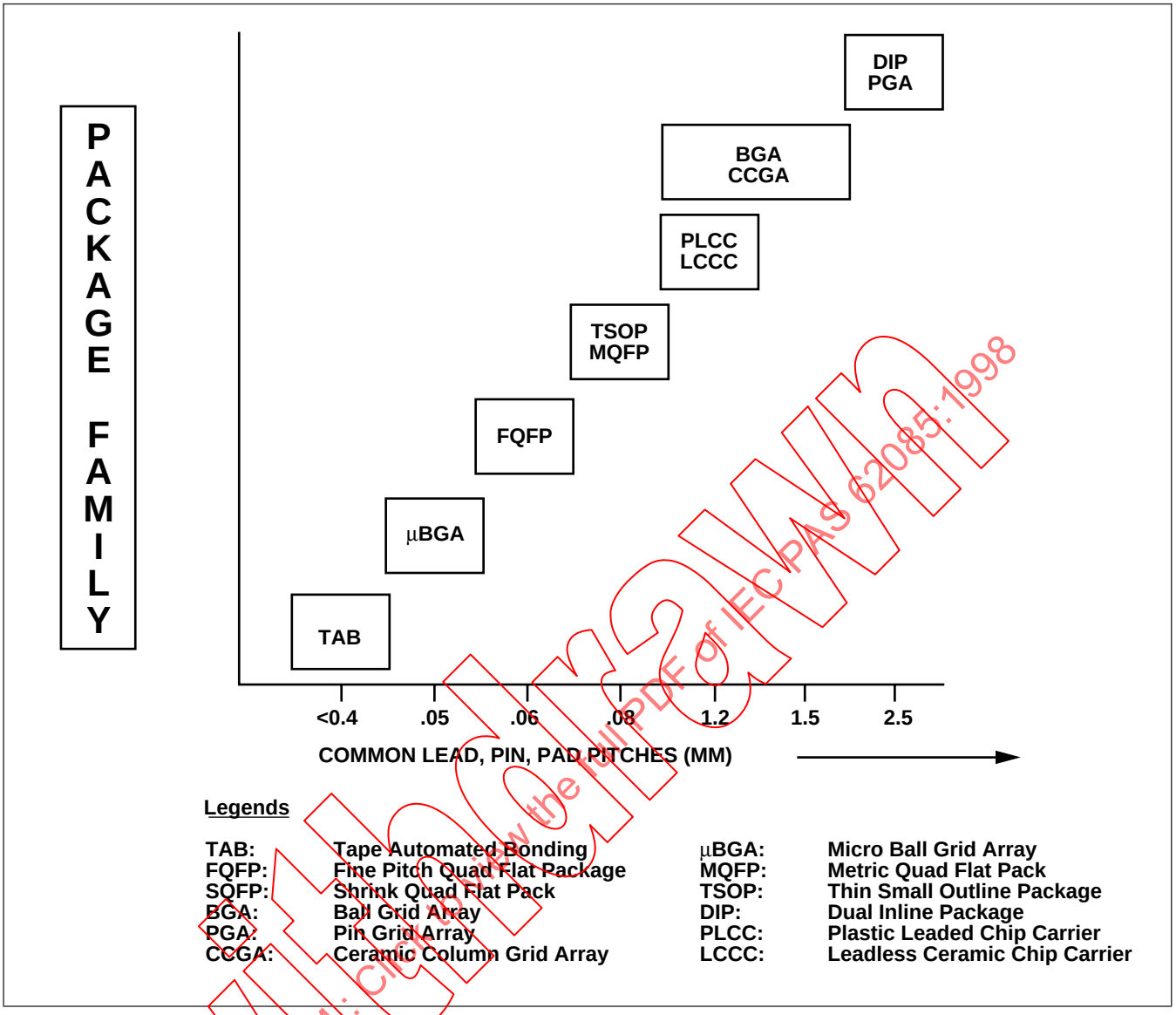


Figure 2−1 Common Lead Pitches in Package Family

The six classes identified were:

Class A = Through-hole component mounting only
Class B = Surface mounted Components only
Class C = Simplistic through-hole and surface mounting intermixed assembly
Class X = Complex intermixed assembly, through-hole, surface mount, fine pitch BGA
Class Y = Complex intermixed assembly, through-hole, surface mount, ultra fine pitch, chip scale
Class Z = Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, TAB

It should be noted that most of the applications for components in this document fall into the Class X or Y category.

In addition, a type designation signifies further sophistication describing whether components are mounted on one or both sides of the printed circuit board or interconnecting structure. Figure 1-1 shows some of the electronic assembly types where Type One has components mounted only on one side, while Type Two has components mounted on both sides. The definition of assembly types discussed in this publication would be Type 1X, 1Y, 2X and 2Y.

2 TECHNOLOGY OVERVIEW OF BOARD AND ASSEMBLY REQUIREMENTS

Continued emphasis on faster, smaller and lighter electronics systems is making component, board and system packaging more complex. The complexity is increased due to increasing use of surface mount packages, which are the key to miniaturization of electronics products. Most of the components on a typical mother board for desktop systems are 1.27 mm [0.050 in] pitch surface mount components with increasing use of fine pitch [0.65 mm and 0.5 mm pitch] packages. See figure 2-1 for various types of packages commonly used today on a typical printed board.

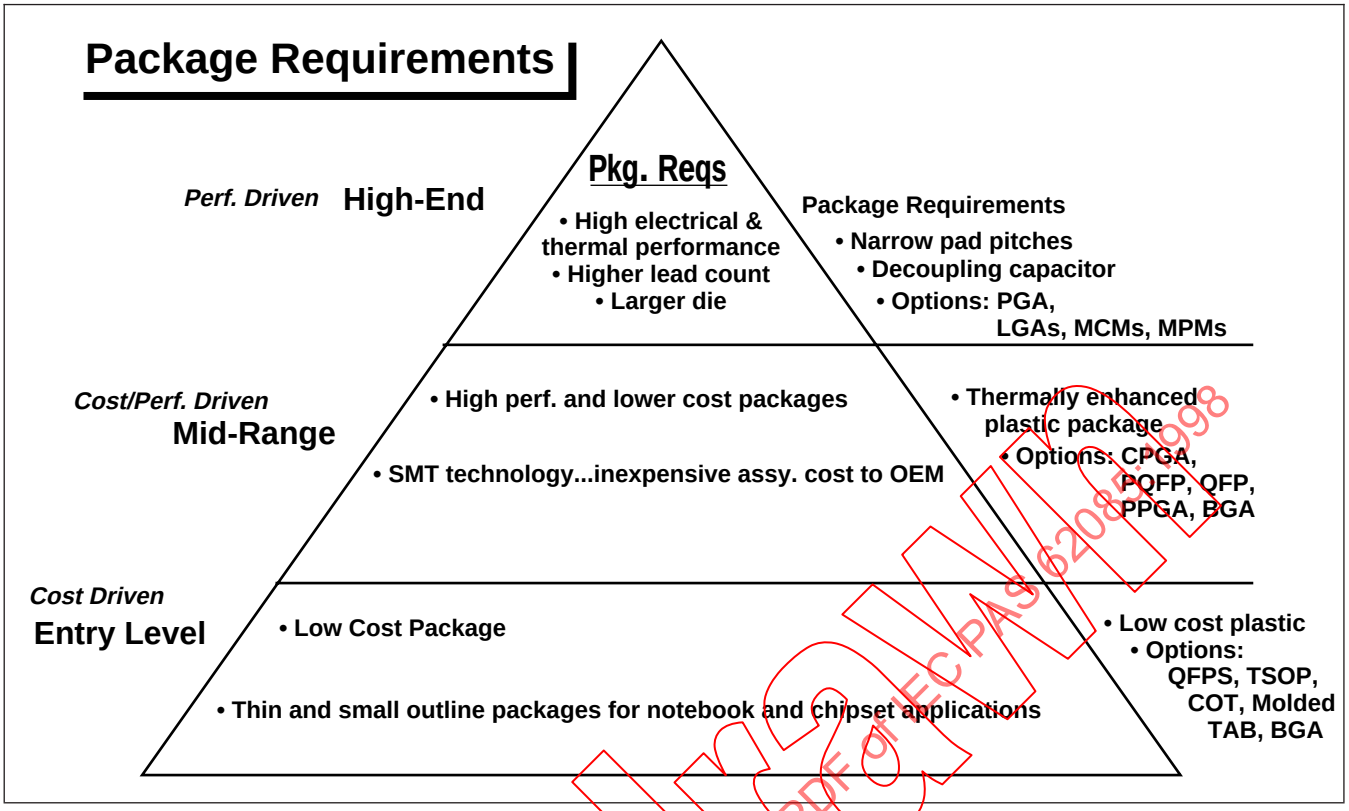


Figure 2−2 Component Packaging Requirements for Different Types of Systems

Lead pitch plays a critical role in the complexity of the manufacturing process. Demands on solder paste printing, pick-and-place accuracy, reflow, and rework become more precise. And since surface mounting generally requires automation for precision placement and paste printing, hundreds of assemblies may be built before a problem is discovered. Use of very fine pitch only compounds the problem in board manufacturing since with increased complexity, yields drop and rework becomes either more difficult or impossible. Thus, a design with parts with large I/O count (i.e. over 208), or below 0.5 mm pitch is the time to consider crossover from peripheral packages to array packages.

The combination of various drivers described in 2.1, will establish a dynamic cross-over point based on assembly capability (i.e. equipment precision), and relative state of the art, for each company mounting BGAs or QFPs.

2.1 The Drivers for Component Packaging

Component packaging in general, and microprocessor packaging in particular, drive the rest of board packaging issues. The driving forces for component packaging are thermal and electrical performance, real estate constraint and cost. As shown in Figure 2-2, the component packaging requirement varies for different types of systems. For example, the high end microprocessors run at higher frequencies and require thermally and electrically enhanced packages.

Enhancements are thermal vias, heat slugs, heat sink and fan heat-sink (fan mounted on heat sink) etc. and examples of electrical enhancements are multi-layer packages and in-package capacitance. Generally hermetic ceramic package are used for this application. For mid-range systems, performance is important but so is cost (not that cost is not important for high end systems.) Thermally enhanced, multilayer packages (Plastic PGA or QFP, BGA) may be appropriate for this application. For low end entry level and portable systems, cost and form factors are critical and generally surface mount packages such as QFP, TSOP and TAB are used.

2.1.1 The Thermal Drivers

With the introduction of new generations of microprocessors, power dissipation has continually moved upward. There is every indication that this will be true in the future. As speed increases, power goes up. This problem is somewhat mitigated, fortunately because die shrink is made possible by finer feature semi-conductor processes and the trend towards lower power supply voltages. For higher wattage packages, ceramic PGA (CPGA) packages have been commonly used, however, TBGA, Metal BGA and enhanced TBGA packages are gaining some attention. For the mid range systems, thermally enhanced plastic packages are being evaluated by the industry. An example of a thermally enhanced SMT plastic package is shown in Figure 2-3.

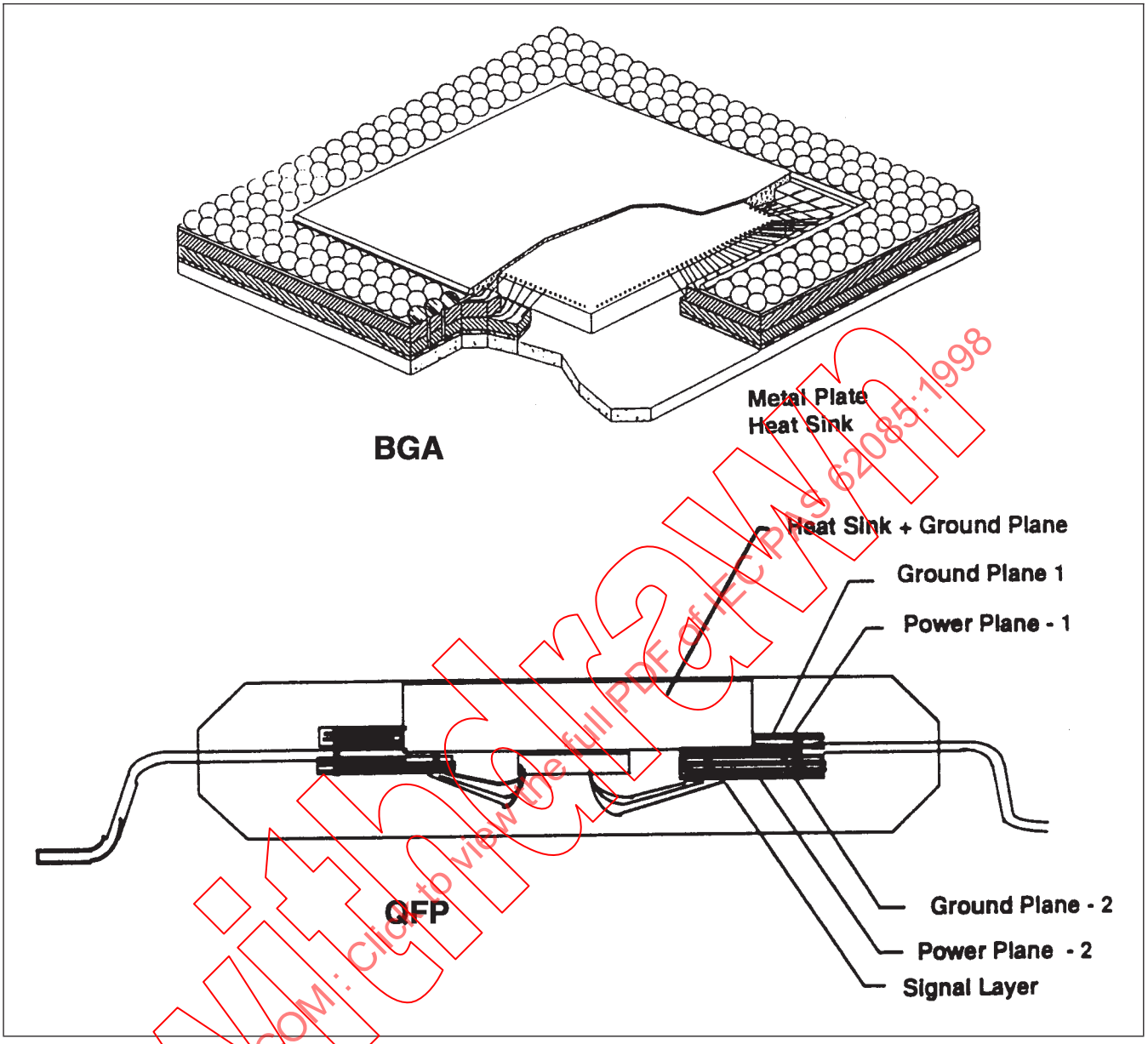


Figure 2–3 Thermally Enhanced Package

2.1.2 The Electrical Drivers

Increasing functionality and speed requires more power, a higher number of bond pads on the die and more pins on the package. Fortunately, even with the increase in bond pads, the pin count is kept to a minimum by using de-coupling capacitors in the package and on the die. In addition, by adding power and ground planes in the package, the number of pins can be further reduced. For example, if no electrical enhancement is used, the number of package pins will equal the number of die bond pads. If this was the case, the number of pins for some microprocessors would be staggering. By using in-package capacitance and multi-layer packages, the pin count is kept to a minimum. In enhanced plastic packages, the pin count is higher since addition of too many layers and in-package capacitance is generally not feasible. For example, a microprocessor that has 168 pins in a ceramic PGA, might require 196 pins in a plastic surface mount package.

2.1.3 The Real Estate Drivers

The real estate constraint is also one of the important driving forces in component packaging. This has been one of the main reasons for wide spread usage of surface mount devices which are not only smaller in size but facilitate component mounting on both sides of the board. Above certain pin counts, the pitch must drop to keep the body size within a practical range for manufacturing. For example, when the pin count increases above 84 pins, the pitches drop from 1.27 mm to 0.65 mm. However, if the pin count goes beyond 200 pins, finer pitches such as 0.4/0.3mm TAB or fine pitch QFPs become necessary which complicates the manufacturing process. An alternative to

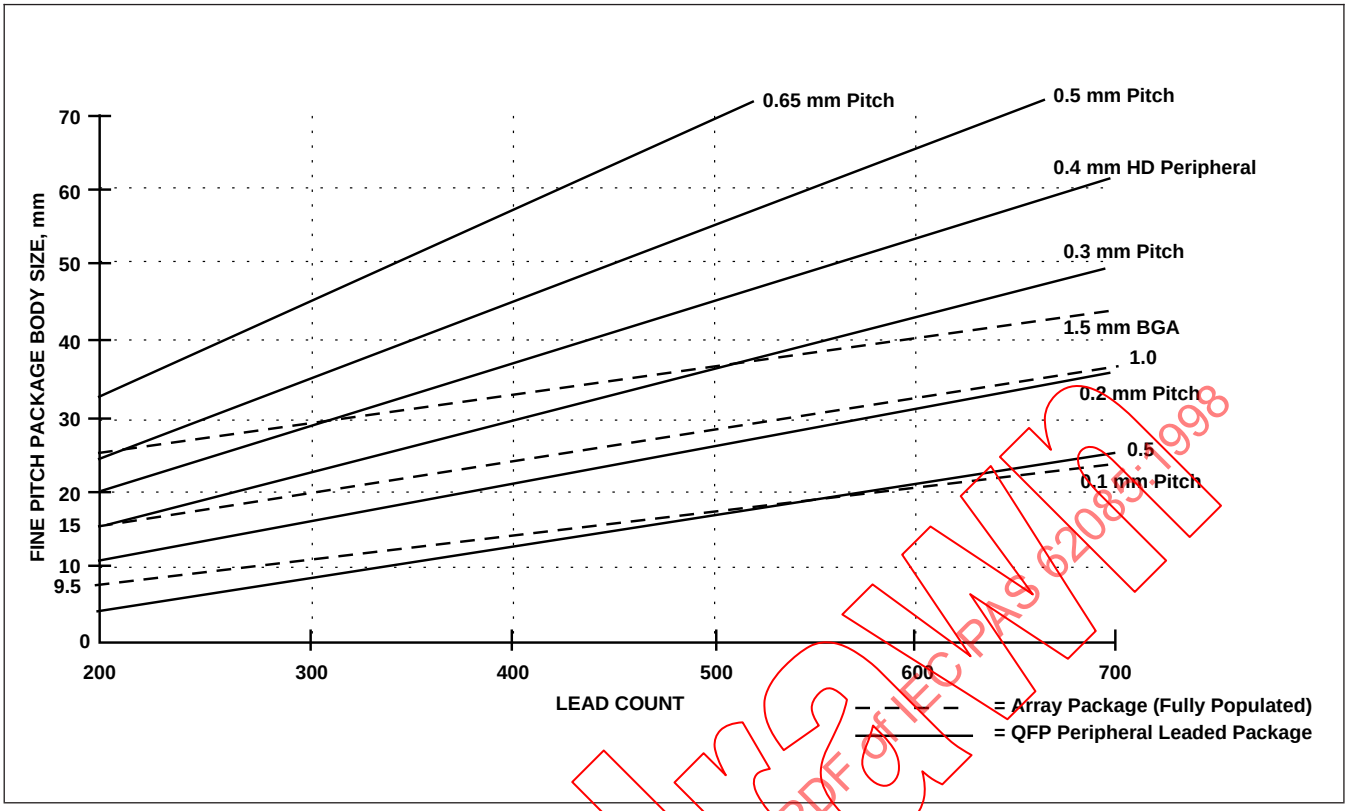


Figure 2−4 I/O Pitch Mounting Area Comparisons

finer pitches is larger body sizes, with the associated real estate penalties. Thus, the move to array type packages where the processes are more robust and provide assemblies with higher first pass yields. See figure 2-4.

2.1.4 Specific Package Drivers

There are generic package drivers such as cost, thermal and electrical enhancements, assembly yield, reliability, and real estate constraints. These relate to the package style and the ability of the form factor to fit into the main process for the product assembly.

Although not every integrated circuit is available in every package style, meeting the requirements of the assembly application become paramount. Package performance in both assembly and ability to withstand the end use environment are the main criteria for the selection. It is incumbent on the user to determine the requirements of the product's end use environment, and select the proper combination of package styles and the interconnecting substrate to be used.

The relationship of substrate and package is extremely important because the reliability of the joint, using a lead from a peripheral package, a ball for an array package, or a pin from a through hole package, determines the cyclic predicted failure rate that can be achieved.

2.1.4.1 Ball Grid Array (BGA) Drivers

A package known as the Ball Grid Array (BGA) has two main advantages over peripheral leaded packages. First, a BGA with a 1.5 mm ball pitch occupies less real estate than a 0.4 mm pitch QFP with 300 pins. The second advantage is that the BGA is easier to assemble than an equivalent fine pitch high lead count package.

The complexity of the board assembly increases dramatically with a reduction in lead pitch. Even at 0.5 mm pitch, considerable problems, such as lead bend, sweep and coplanarity are encountered.

Absence of fragile leads susceptible to handling damage helps make the BGA a much more robust package. Hence it provides much better manufacturing yield. There have been reports by some users that even today the yield of a BGA package is much better than that of 0.63 and 0.5 mm fine pitch peripheral lead packages. Currently BGAs are being used by several computer companies with very high assembly yields.

The BGA allows the use of conventional surface mount placement equipment, solder dispensing and reflow processes.

Companies using BGA are reporting major improvement in manufacturing efficiency. For example, a large multinational company using 0.5 mm pitch quad flat pack devices could not improve the assembly process defect ratio below 200 to 300 ppm. When the same product was redesigned using ball grid array packages, the defect factor dropped to 3 ppm (parts per million).

2.1.4.2 PGA Drivers

The Pin Grid Array (PGA) was the first area array package adapted for high pin count and high performance applications. Most packages are based on inch grid spacing [0.100 in].

Some of the advantages of a PGA are that it can either be socketed or directly soldered with minimum reliability concerns. Many OEMs directly solder PGAs to achieve lower cost even though they use sockets during development stages. Most important of all, socketing allows system upgrade by the end user without buying a whole new system. Tariff on the imported mother board also plays a role in favor of socketing PGAs. To minimize tariff on mother boards assembled overseas, processors (the most expensive component on the board), are inserted in the home country.

2.1.4.3 Fine Pitch Plastic Drivers

The primary driver for fine pitch is real estate constraint. In addition, there is significant cost saving in using FQFPs, in some cases well above 50 percent over PGA. In other cases, fine pitch plastic packages provide a lower profile package necessary for portable electronics. This fine pitch plastic package is also a common package for high pin count (over 100) ASIC (application specific integrated circuit) devices. In many cases, ASICs are used for reducing thermal load by combining 10 to 20 programmable logic array devices which would consume 5 to 10 watts each into a 2 to 4 watt single ASIC device. These packages allow thermal and electrical enhancements by use of heat slugs and multilayer boards while significantly reducing cost. However, package reliability and moisture susceptibility are some of the concerns that must be addressed before using thermally and electrically enhanced plastic packages.

2.2 Issues in Component Packaging

It should be noted that there are issues with every package option. Issues include:

- Package assembly
- Repair
- Susceptibility to moisture absorption
- Inspectability of final solder joint
- Handling of parts prior to assembly
- Handling of parts during assembly

Depending on pitch and contact density, BGA packages may require additional layers for conductor routing since it is more difficult to route area array land patterns than peripheral land patterns. Raising layer count will raise board cost.

Repair of BGAs may also be difficult. BGAs cannot be soldered by laser or hot bar processes. Since BGA solder joints cannot be inspected, one must primarily depend upon process control. The lack of inspectability of BGAs may not be a significant barrier for using the BGA if one considers the alternative of using an ultra fine pitch package. A quantum jump in surface mount manufacturing technology is required to establish a complete infrastructure for 0.4 mm and smaller pitch packages.

The major issues with fine pitch QFPs will be handling, lead coplanarity, paste printing and placement. Availability of boards with an even thickness of solder may also be a problem. It should be noted that there are issues with every package option. Issues include package assembly, repair, susceptibility to moisture absorption and inspectability of the final solder joint. Companies are still going through the learning curve with moisture susceptability of some plastic packages.

Handling of packages prior to and during the assembly operation must be approved. Solder may be applied by the board vendor by paste printing or plating or use of a protected copper surface may be necessary. Even if such a capability is developed, the yield differential between fine pitch QFP and BGA may remain.

There are some additional issues such as the foot length on gull wing leads to allow reflow and hot bar soldering of QFP especially if packages are shipped trimmed and formed. Hot bar or other equivalent processes may be required if the packages are susceptible to moisture induced package cracking. Additional handling incurred in moisture protected packages during baking and bagging may further compound the costs associated with using QFPs.

Finer pitches (below 0.4 mm) of high pin count devices may require the use of tape carrier packaging (TCP) or wire bonding of the chip to the device lead frame. Some have suggested skipping the QFP or plastic package altogether and moving directly to direct chip attach using TCP. Tape carrier packages will require the resolution of the same board and assembly related issues as fine pitch QFP. In addition, the technology for chip encapsulation needs to be defined. The lack of industry infrastructure for TCP is one of the major issues.

The Pin Grid Array has some problems as well. While it has served well for lower pin counts, it may not be the package of choice for higher pin counts with large heat sinks attached to it. The high pin count PGA packages used for high performance processors cannot afford to use a high inductance socket. The LGA package has a concern with socketing reliability since the LGA may require selectively gold plated lands on the PCB for connection. This adds to the cost of the board.

2.2.1 Future Considerations

Additional work is necessary for full acceptance of the processes. Figure 2-5 summarizes the issues that need to be resolved before new packages such as QFP, TCP and BGA are widely used by the industry. There is a mature infrastructure in place for dealing with PGA and QFP (0.65 mm

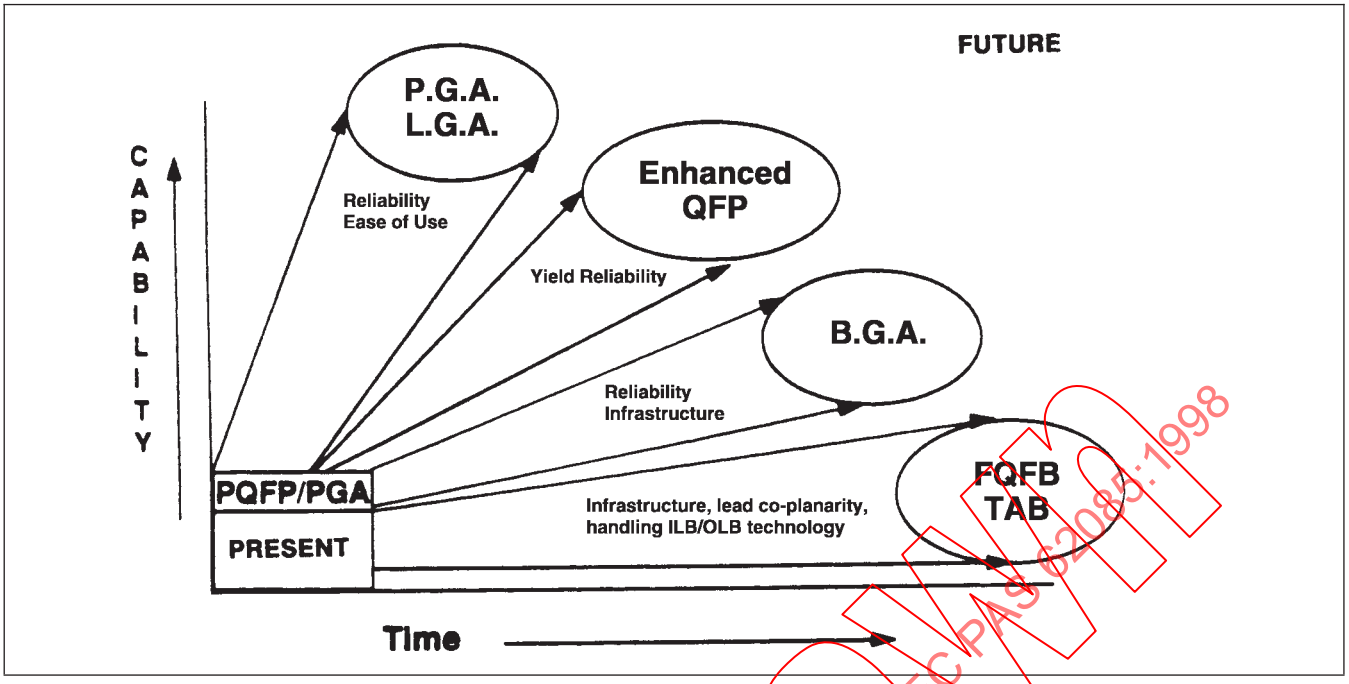


Figure 2−5 The Move from Present to Future Requirements

pitch and above) packages. They do not address all our needs, so we have to explore high pin count CPGAs, enhanced plastics, BGAs, TCP and QFP. In turning that vision into reality, there is much to be done. Here are some specific options: heat spreader or heat slug or some other form of thermal enhancement is needed for high power devices most likely to be packaged in ceramic PGAs. A multilayer thermally and electrically enhanced plastic package is needed for a lower cost option. This can be either in fine pitch QFP or BGA with a preference for BGA over fine pitch QFP packages.

As the performance and speed of microprocessors increase, pin counts increase. This trend will continue despite the fact that these packages will be electrically enhanced by using multilayer packages with in-package capacitance for decoupling. For cost reduction, thermally and electrically enhanced plastic QFP and BGA packages will become common.

To reduce board complexity and to increase manufacturing yield, ball grid array package use will become commonplace. Despite increased complexity in packaging and assembly, the primary driver will be cost. The winners will be those suppliers who not only meet the technical challenge to provide a solution, but do so at a continuously decreasing price.

2.3 Impact on Interconnecting (Printed Board) Technology

Printed boards must accommodate building intermixed component technology assemblies. Hot air solder leveling (HASL) is a commonly used process for applying solder to the top layers. The solder thickness on the lands of various types of packages on the same board vary widely from a low of 0.1 mm to a high of .25 mm. Too much solder thickness may result in solder opens due to coplanarity variation and too little solder may result in dewetting. In order to achieve a more uniform thickness, various other options such as plating, applying solder by screen printing or flattening solder after HASL are some of the options for the industry.

The other concern that the board industry must address are building four to six layer boards while keeping board thickness under 0.5 mm for PCMCIA (Personal Computer Memory Card Information Association) applications for the mobile market. It is also difficult to maintain bow and twist to a minimum in thin boards. Even for standard 1.5 mm thick boards, warpage needs to be kept under 0.5 percent as opposed to 1 percent now common.

The use of different packages impact layer count and board area. For example, peripheral fine pitch packages such as FQFP and TCP require more board area, but lower layer count. PGA and BGA packages require less board area, but higher layer count. One should also take into account the total area needed for routing. A BGA occupies less real estate, but could require additional layers for routing.

In addition to the type of package and its pin counts, conductor density also impacts layer count requirement. The number of conductors means the number of lines that can be routed between lands of a PGA on 2.5 mm centers with 1.2 mm lands leaving 1.3 mm for routing between lands. Four conductors for PGA means four lines can be routed between two lands. This is equivalent for a BGA that uses

0.65 mm via lands on 1.5 mm centers, allowing three conductors to be routed between the lands.

Effect of pin count on number of layers needed for routing (assuming only 10 percent for power and ground pins) for a BGA and PGA is shown in Figure 2-6. Note that using four conductor density (0.15 mm conductors and spaces) a PGA with 280 pins can be interconnected in four layers, but a BGA with the same pin count will require six layers.

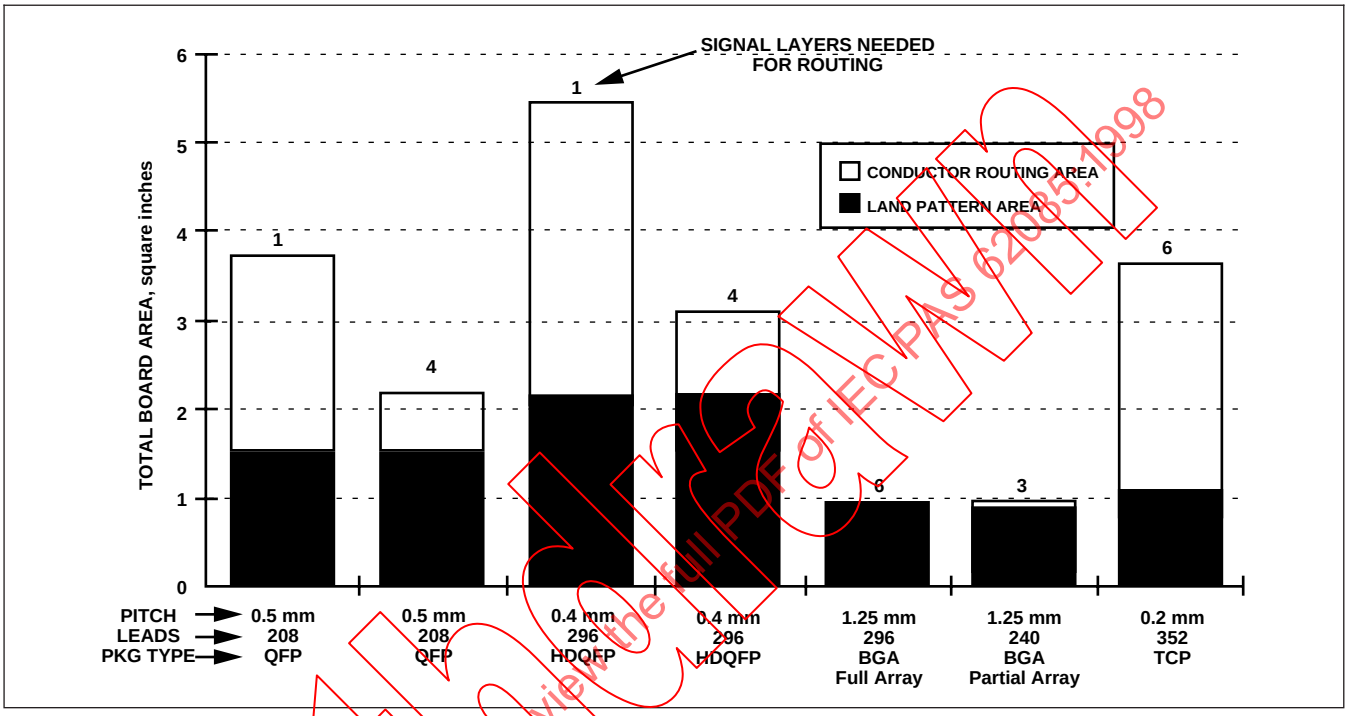


Figure 2−6 Board Routing Area Study

Via hole size, conductor density and layer count are important to keep in mind when selecting a package since they determine board cost. As shown in figure 2-7, board cost shoots up rapidly if the finished via hole size is reduced below .4 mm. Costs increase because drilling and plating yields begin to drop for small vias. It should also be noted that very fine via holes are also susceptible to cracking. One must maintain an aspect ratio of about 4:1 to ensure via hole reliability. Aspect ratio is defined as board thickness divided by preplated or drilled hole size.

As shown in figure 2-8, the layer count and conductor density impact board cost. Board cost dramatically increases if the layer count goes above 8. But in a very competitive market, layer count is kept as low as possible. For example, there is distinct shift from 6 to 4 layer boards. Existing 6 layer designs are being redesigned into 4 layers to lower cost.

2.4 Impact on Assembly

Component packaging not only affects the printed board design, its impact on the board assembly process is even more significant. With increased board complexity, as expected, defect rates climb dramatically. The major contributors to assembly defects are PCB (solderability, bow and twist, warpage and uneven solder on lands), components (lead coplanarity, lead pitch, solderability), and incapable assembly processes.

The effect of QFP lead pitch on solder defects is dramatic. As the lead pitch decreases, defects go up, due to the problems associated with a fragile lead (coplanarity, sweep, bend). This results in solder defects (shorts and opens). As the lead pitches drop below 0.65 mm, it becomes difficult or impossible to provide soldermask between lands, adding to solder bridging if a paste printing process is used. Also, for extremely fine pitch devices, it is difficult or impossible to determine how far off the leads are from target, even for the supplier. It is nearly impossible for some users since they are generally not set up with a method of determining lead or ball array coplanarity.

For the fine pitch package at or below 0.65 mm pitch, there may be significant solder opens primarily due to lead coplanarity as shown in Figure 2-9. The finer the contact pitch of a peripheral or area array package, the more susceptible it is to lead or ball damage, such as lack of coplanarity. And greater coplanarity deviation means more solder opens as shown in Figure 2-9, which shows how a minor coplanarity deviation causes an order of magnitude increase in solder defects.

Special solder paste with finer particles (20 to 45 microns), with higher viscosity and slower printing speed is needed for fine pitch packages. New methods of solder printing (slower speed) and laser cut stencils may be necessary.

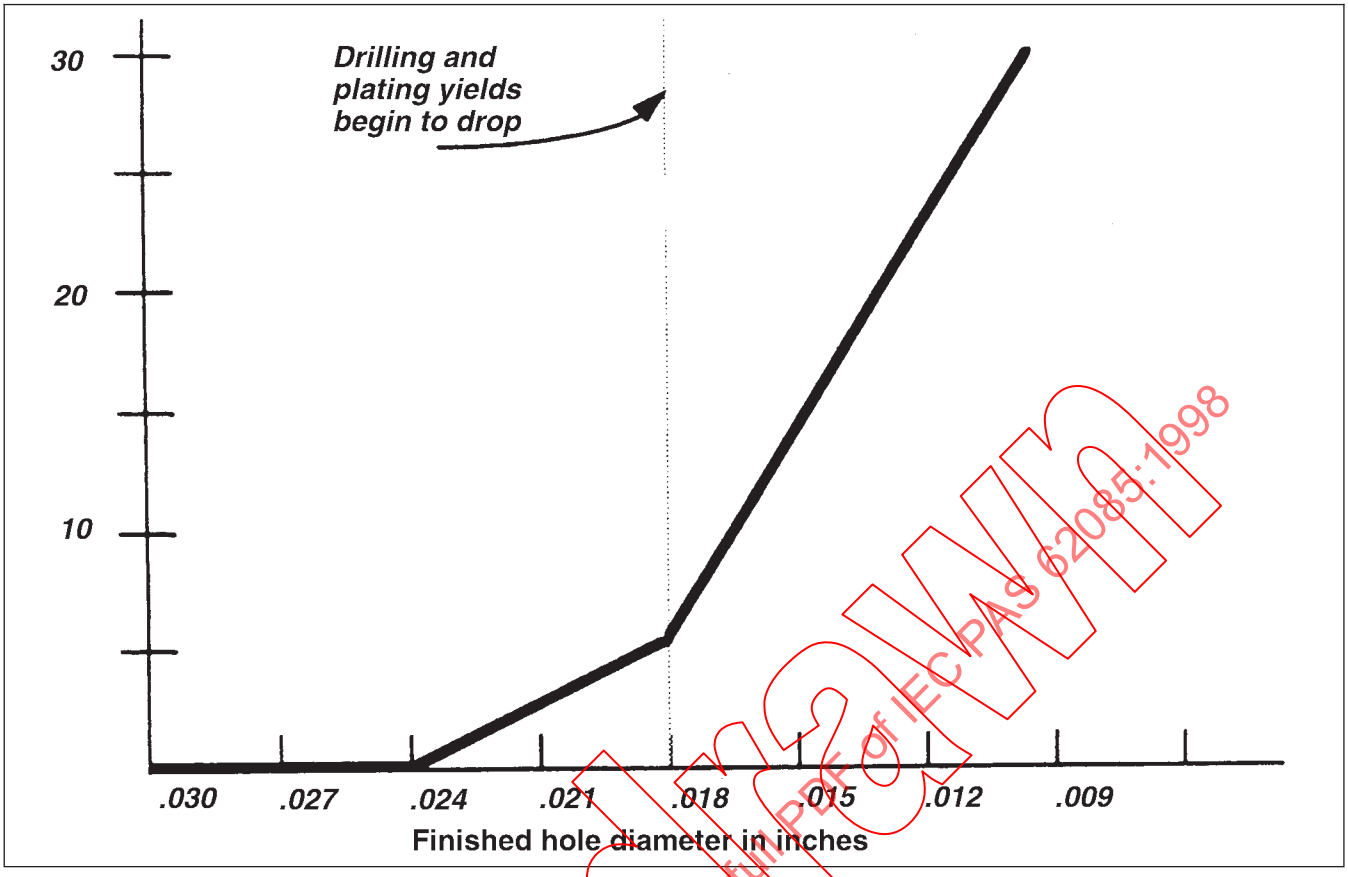


Figure 2−7 Typical Cost Curves − Cost vs. Finished VIA Hole

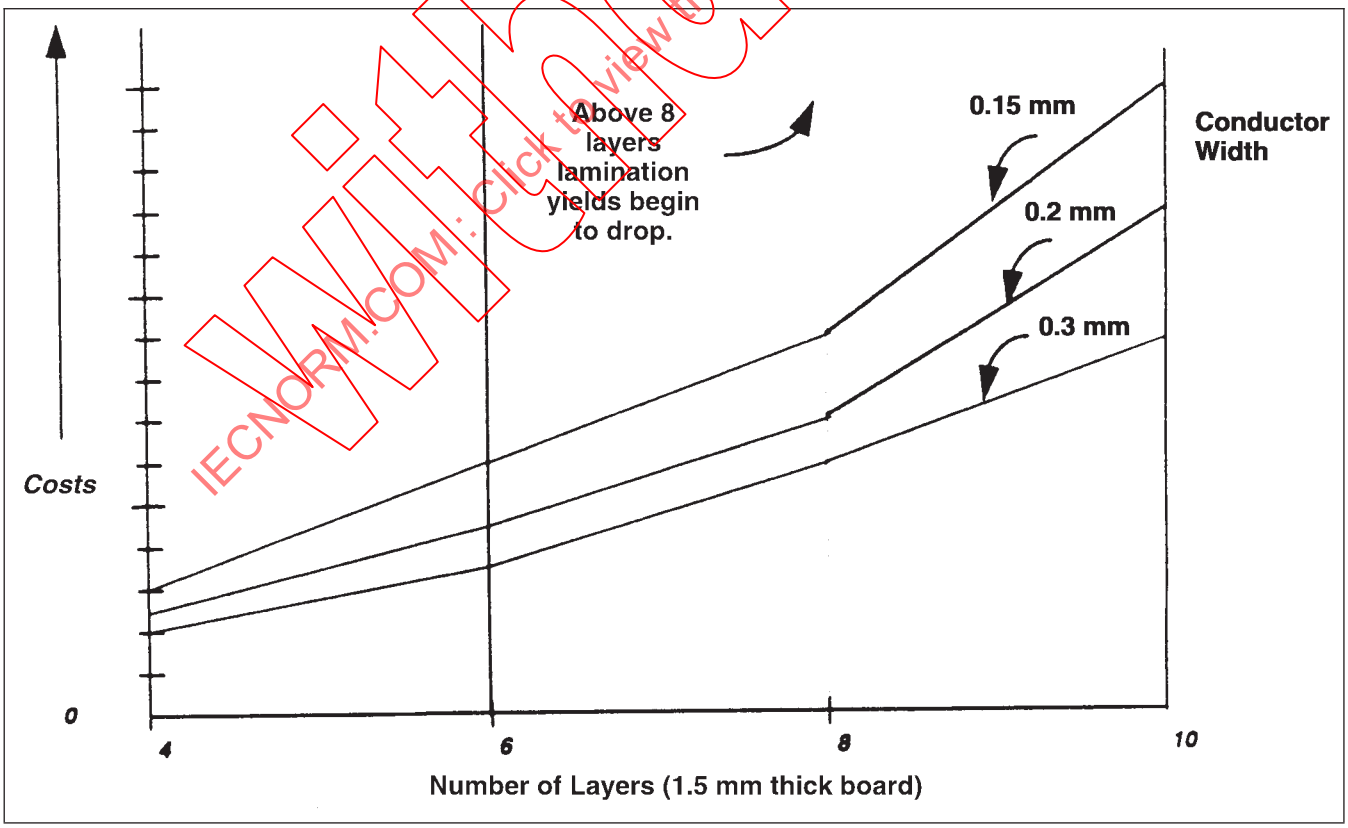


Figure 2−8 Typical Cost Curves − Cost vs. Number of Layers

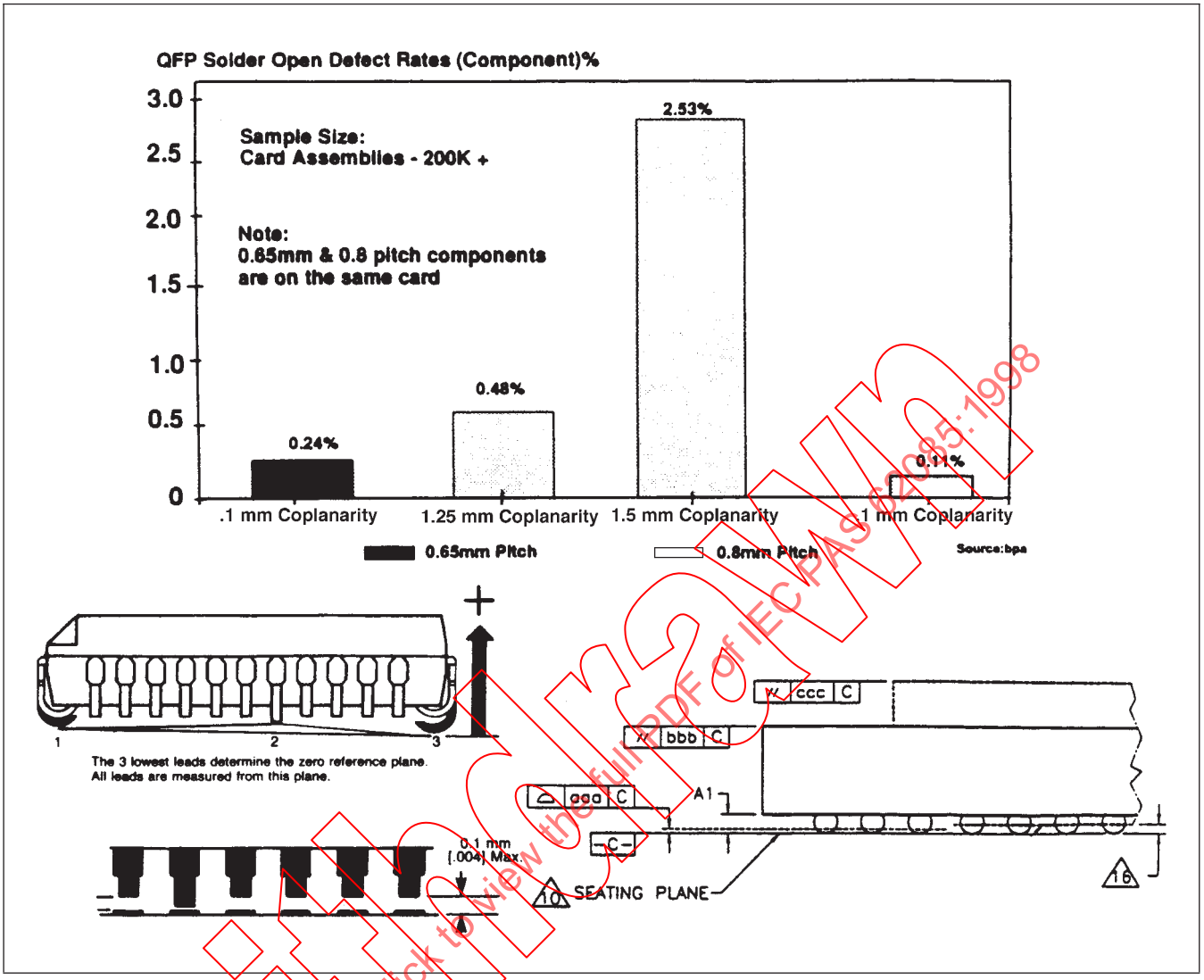


Figure 2–9 Coplanarity Example of QPF Solder Opens

These variables will be even more critical for pitches lower than 0.5 mm.

With emphasis on no clean or low active fluxes, it is becoming popular to use a neutral reflow environment such as nitrogen to achieve good soldering results. It is difficult to clean under these packages, since many have very low stand-off. Figure 2-10 shows the ability to clean under a package is determined by its area and stand-off from the board.

Some packages, especially EIAJ (Japanese) packages have zero stand-off. One cannot perform adequate cleaning under these packages.

Special cleaning consideration is required for a mixed assembly (one requiring wave soldering for through-hole components, after surface mount components have been reflow soldered). Cleanability can be assured only if vias under the packages are filled, or tented to prevent seepage of flux during wave soldering. Filling of vias is accomplished by temporary solvent soluable mask in the via or permanently by permanent solder mask or plating in the hole. Tenting is usually accomplished using a dry film soldermask.

2.5 Future Implementation Strategies

Increased performance and speed also mean that thermal enhancements such as heat sinks, heat spreader and heat slugs will become more common. Despite these thermal enhancements, higher airflow even in desktop systems will be needed. To ensure quietness in an office or home environment, noise dampening technologies may become essential for systems.

For cost reduction, thermally and electrically enhanced plastic packages will become common. For this to happen, however, the reliability concerns in such packages must be addressed. The complexity of board assemblies will increase because the packages of varying lead pitches, including through-hole will be used. Increasingly wider usage of finer pitch packages will compound this problem.

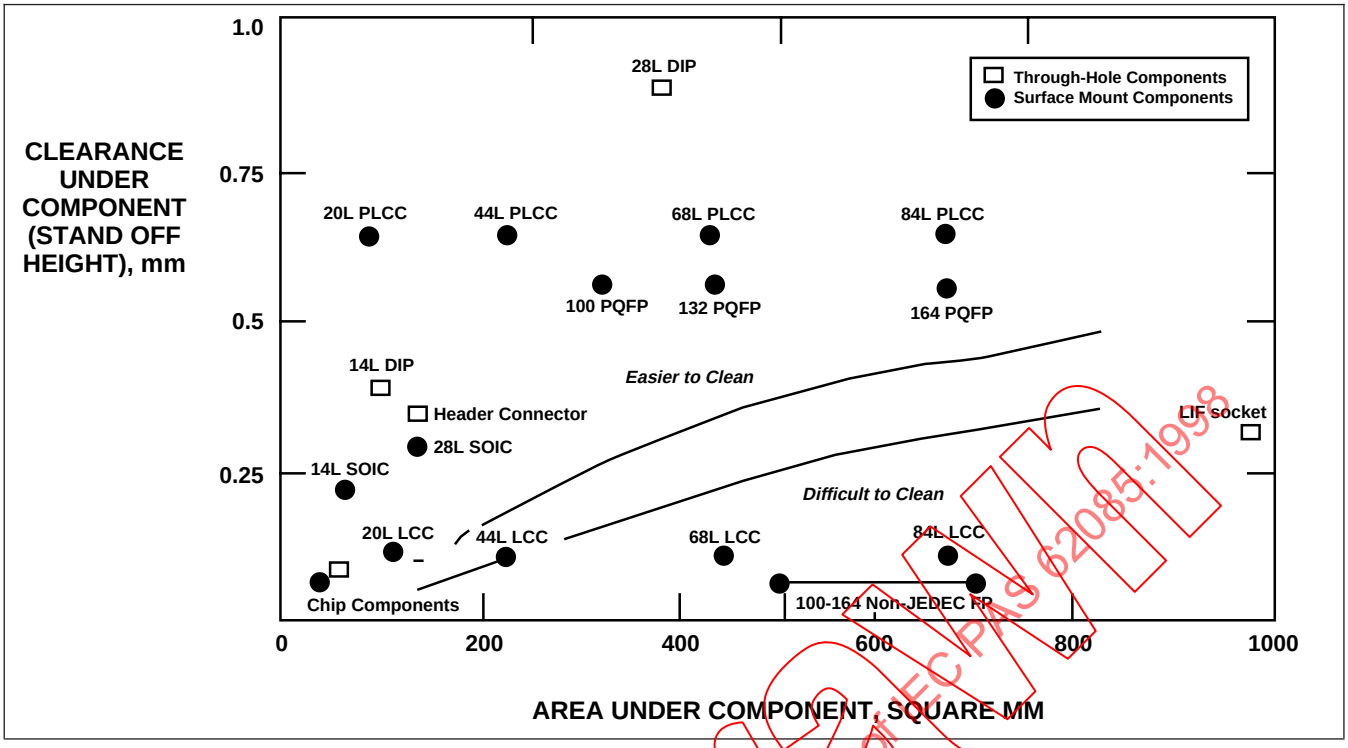


Figure 2−10 Stand-off vs. Cleanability

Some relief may be possible because ball grid array packages will become common, since they reduce process complexity for the user. The effect of complexity in general will be felt by the suppliers and users.

2.5.1 Complexity Matrix

With the advent of such I/C package styles as the Ball Grid Array (BGA), Land Grid Array (LGA), and Column or Ceramic Grid Array (CGA), electronic equipment designers are carefully reviewing their options. Array Surface Mount (ASM) has its benefits and its risks. Positioning tolerances are more liberal. However, quality is achieved through process control as opposed to visual inspection.

Figure 2-11 shows a complexity matrix for packaged parts with leads or terminations around their perimeter; figure 2-12 shows the relationship or evaluation of parts with their leads or terminations on the underside of the package in an array format.

The complexity matrices could help establish the parameters for definition of high pin count and fine pitch. Complexity is judged on a scale of 1 to 10, where 1 is easy and 10 is very difficult. The first number reflects design complexity. Although some designs are easy, others are more difficult because of the number of I/O's that are needed to be interconnected or the board real estate available for accomplishing the interconnection.

A second number in the matrices reflects the difficulty of manufacturing. Manufacturing includes both the manufacture and testing of the bare board as well as the manufacturing and testing of the completed assembly.

Pin Count \ Pitch	Std. Pitch 2.54 mm	Ultra Std. 1.0 mm	Fine Pitch .63/.5 mm	Ultra Fine Pitch .4/.3 mm	Very Ultra Fine Pitch .25 & Less mm
≤ 68	1-1	1-3	1-6	3-8	4-10
70 - 136	1-1	1-4	1-7	3-9	5-10
138 - 408	7-1	7-4	6-7	6-9	Not Practical
410 - 720	10-3	10-4		N O T	
720 - 1000			P R A C T I C A L		

Figure 2−11 Component Packages with Leads Around Perimeter

Pin Count \ Pitch	Std. Pitch 2.54 mm	Ultra Std. 1.0 mm	Fine Pitch .63/.5 mm	Ultra Fine Pitch .4/.3 mm	Very Ultra Fine Pitch .25 & Less mm
≤ 68	1-1	1-1	1-1	1-1	1-1
70 - 136	1-1	1-1	1-1	1-1	1-1
138 - 406	2-1	2-1	2-1	2-1	2-1
410 - 720	4-4	4-4	4-4	N O T	
720 - 1000	7-7	7-7	7-7	P R A C T I C A L	

Figure 2−12 Component Packages with Leads Underneath in Array Format

3 COMPONENT PACKAGES

Packages are essentially only one link in the varied and complex electric interconnect chain that has its beginning at the semiconductor wafer, where transistor feature size defines the first metal interconnecting process. Industry packaging interconnect schemes are varied to meet the electrical, mechanical, manufacturing, cost and reliability expectation of the I/C manufacturer and user applications.

The industry's first I/C packages were simple six-to-eight lead hermetic glass/ceramic or metal/ceramic packages. The assembly processes were restricted to socketing, thermal insertion, wave soldering or welding to the circuit board. Since that time, a multitude of package concepts and several assembly technologies and techniques have been developed, including the most recent development of surface mount technology. The options are a direct reflection of the manufacturing, application, performance and reliability expectations of both the devices and the circuits to which they are interconnected.

Each of the package options fulfills a unique circuit requirement with respect to I/C device and the interconnection application. These factors have therefore led to a proliferation of packaging options. Uniquely, as new package options are added, old ones have not become obsolete, resulting in an ever increasing number of available options. This section defines the interrelationship of the package options to the device and assembly and product requirements.

3.1 Component Identification

I/C packages are described in two basic lead or terminal classifications.

- Area Array
- Peripheral

Since this document is limited to high lead counts/high performance device packages, no definitions will be covered for packages that are effectively restricted to a maximum of 40 leads.

3.1.1 Area Array Component Types

Array lead packages are those types where the emanating terminations or leads are based on some form of grid network that positions the I/O into the output matrix. Originally starting as pins emanating from the package, this concept was an extension of the terminations of the chip contained in the package.

Beginning with four sets of rows around the periphery of the package or near the edge of package, it soon became apparent that additional rows could be added moving toward the center of the device. The concept continued until all available positions in the pin output matrix were occupied; thus the term pin grid array became synonymous with the image of the output pins. See figure 3-1.

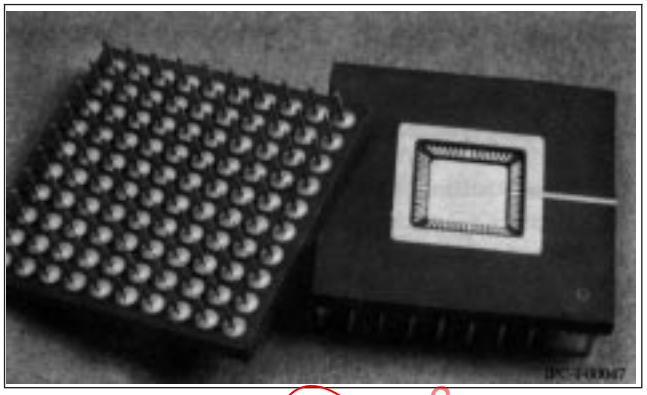


Figure 3–1 Pin Grid Array

Various perpetrations of area array type packages have evolved. The format is ideal for translating the chip bonding sites to the next level interconnect; however, increased use of surface mounting has become less desirable. Also there is a need to increase the utilization of the interconnecting real estate for making all electrical interconnections of the I/C package to the substrate.

Because of the move from through-hole technology, surface mount packages such as Land Grid Array, Ball Grid Array and Column Grid Array have evolved. Ball grid and stud grid array are intended to be close or soldered to the surface. The land grid array may also be soldered; however, in most instances it is a pressure bondable interconnection system that works well for connectors and other electrical and electronic parts.

The spacing of matrix or grid output lands is more forgiving than in the fine pitch peripheral type packages; therefore, the processes are achieving a higher yield (less solder bridging or solder skipping).

Area array packages offer some high density interconnection concepts without the penalties of density pitch. Six-sigma soldering can be achieved although proof through visual inspection is not possible. The desire to do visual inspection could be a detriment to future acceptance of the array type packages in either Ball Grid Array, Column Grid Array or Land Grid Array formats.

3.1.2 Peripheral Leaded Device Packages

Peripheral device packages are semiconductor device packages with terminals extending from one or more of the four sides of the package. The leads are formed in a shape that is compatible with printed board surface mount land pattern. Historically, the device packaging has been an evolutionary process that depends heavily upon the installed manufacturing base, materials, infrastructure of assembly equipment and cost effective piece-part suppliers. Peripheral lead packaging is most effective for smaller parts with a low lead count.

3.1.3 Component Marking

Most semiconductor I/C Packages are marked with a company logo and part number identification. The marking characteristics are extremely important and many times are related to the company who makes the part. The marking is significant advertisement that the product belongs to a particular company. Part number identification provides correlation to ordering or replacement of the part.

In addition, if the part family meets a standard such as defined by the Joint Electron Device Engineering Council (JEDEC), many times the registered and standard outline for the solid state and related product is identified by its particular standard number. Thus, as an example MS-016 might indicate that a particular part meets a standard outline. This assists in the evaluation of the land pattern in which the part belongs.

Another important element of marking is the location of pin #1 in the package device. The Peripheral packages many times have pin #1 identified with a small circle. Sometimes these marks are molded into the plastic body, thus assisting in the inspection and identification of properly placed and interconnected devices.

Sometimes, pin #1 is located in the center of the package, sometimes pin #1 is in one of the corners. In any event, this is an important piece of information. In addition to part number, there is usually an index area that may also be associated with the pin #1 marking. A similar condition exists for the Area Array Packages. In many instances, pin #1 is located in one of the corners. Figure 3-2 shows the difference between Peripheral and Area Array markings, and the pin wire bonding sequence from the point-of-origin.

3.2 Component Materials

The material and process technology steps used to manufacture or assemble the basic types of component packages differ only in detail. Package families in area array or peripheral format provide the functional specialization and diversity required for the user.

Material and construction attributes of individual family members are provided by the following package technologies:

- Cofired (Multilayer) Ceramics
- Pressed Ceramic
- Molded Plastic
- Laminated Printed Board

Not all combinations of package families (form, fit, function) and package assembly technologies are available in all forms. Nevertheless, multilayer structures have used the laminated ceramic approach in many products, as this has been most beneficial for leaded and leadless chip carriers and for various aspects of the array packages as well.

When single layer interconnection is feasible, pressed ceramic and molded plastic are used for the package family. This is normally accomplished in the leaded type packages; however, with the advent of the array packages and the SMT format, new ideas are being explored that use both single layer and multilayer organic substrates in the pressed and the molded plastic family.

In some cases, Ball Grid Arrays are being packaged using standard organic material substrates, such as BT resin or modified polyimide interconnection substrates systems and glass reinforcement. These standard printed board technologies provide a coefficient of thermal expansion

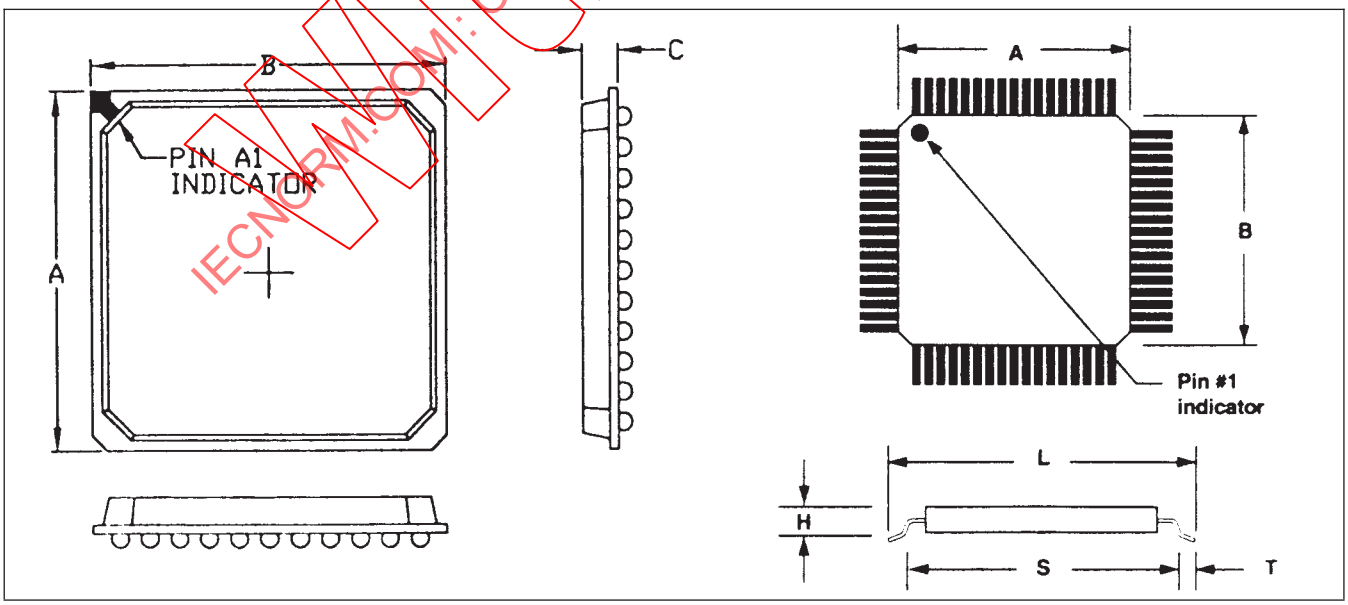


Figure 3–2 Example of Device Package Marking

between that of the component and the interconnecting structure resulting in a greatly reduced CTE mismatch.

During the development phase of the interconnecting strategy, it is important to consider all the variables such as temperature, material characteristics, package moisture content and package reliability under environmental stress due to the materials selected.

Component materials must be completely characterized before introduction to the assembly production line. Many experiments are necessary in the validation stage to provide cost-effective manufacturing processes.

3.2.1 Ball/Column Termination

The solder balls or solder columns form the electrical and mechanical bridge between the area array package and the next level assembly. The solder absorbs the stress between the package and the next level assembly caused by variations in the relative thermal expansion rates.

The solder composition of the area array bumps varies according to required mechanical and thermal properties. Common solder compositions include:

90 Pb−Sn
97 Pb−Sn
63 Sn−Pb
50 In−Pb
95 Pb−Sn

3.2.1.1 Bump Preparation

Bumps can be assembled into a solder-mask-defined area. They may be separately produced and attached through a fusing process, or they may be deposited and fused to form the round shape.

Usually a ball mask is attached to the underside of the part, and the bumps are plated to the size required where they represent a truncated cone, and a reflow process causes the final round diameter shape.

Electrodeposition offers a wider range of Sn-Pb compositions than evaporation and thus affords greater control over mechanical and thermal properties. Electrodeposition also produces smaller diameter balls.

A variety of solder paste compositions can be screen-printed. Here bumps are reflowed at lower processing temperatures, and improved compliance and failure life in some instances may result.

3.2.2 Termination Leads

Leads emanate from the I/C package and peripheral packages and must be formed in order to meet the final configuration. Lead forming is a two-fold assembly operation that bends and trims plated or solder dipped-leads to meet specified dimensional accuracy. Leads can be formed into three standard configurations: gull wing, ‘‘J’’ leads for surface mount packages, and straight form for through hole mounting. During the forming process extreme care is taken to expose the tin plating or solder coated leads to minimum stress and abrasion, thus ensuring maximum strength and reliability.

The lead finishes used on component packages are usually one of five basic lead finishes. These are:

- gold plate
- tin plate
- solder coating
- tin-lead plate
- palladium plating

Each type of lead finish offers advantages for specific applications and for internal and external processing.

3.2.3 Plating and Coating Technologies

3.2.3.1 Gold Plate

The gold plate finish is recommended for socket applications only. The packages most often involved are the ceramic laminated family, including pin grid arrays (PGA), side brazed dual-in-lines and its other cousins.

At one time gold was considered a universal superior lead finish because of its solderability and electrical and non-oxidizing properties. However, it has been determined that soldering gold-plated component leads directly into printed circuit boards has some clear disadvantages.

Excess gold in solder joints can result in the formation of a brittle alloy, causing the joints to fail over time and under high-vibration or board-flexing environments. Currently, requirements demand that a solder coat replace gold and direct soldering used for both leadless and leaded components. Gold plating remains the lead finish of choice however, for socketed units.

3.2.3.2 Tin Plate

Some leaded components are offered with tin plating. This is usually for selected ceramic type leaded packages. The tin-plating finish can be either directly soldered or socketed with non-gold socket contact finishes.

Tin offers the advantage of a slightly higher melting point (232 °C) than solder (180 °C), and it can be burned in at higher temperatures without melting. However, when compared to solder coating, tin plating does not age as well in long term storage from the stand-point of solderability. This may occur because tin plating is more porous than solder coating. In general, pure tin plating is more susceptible to tin whisker growth under certain mechanical and environmental conditions.

3.2.3.3 Solder Coat

Solder coat component leads offer the distinct advantage of the low melting point (183 °C), and resistance to aging. A

typical composition of solder coat is the eutectic alloy of 63% tin and 37% lead.

Base coatings are normally applied in the following sequence:

1. Clean the leads
2. Apply flux
3. Dip the leads into molten solder
4. Finish with hot water rinse.

Great care is taken to minimize any thermal shock to the package and die during solder joint processing and cleaning of the unit after coating.

The solder coat lead finish is usually available to most of the plastic and ceramic package family formats as well as all military packages. Solder coat lead finish is compatible with many types of assembly processes including wave soldering, infrared, hot air, and vapor phase reflow solder technologies.

3.2.3.4 Tin-Lead Plate

Tin-lead alloy is used extensively for plating leads. The plated elements, when reflowed, form an alloyed composition of approximately 85% tin and 15% lead, or 63% tin and 37% lead. The plating on the packages' copper lead frames, with the thickness of 5 µm minimum, provides full coverage of the copper without exposing any formed intermetalics to air. At the same time, solder plate produces a very solderable finish with a melting point for the 85/15 approximately 220 °C and for the 63/37 approximately 183 °C.

Leads plated with tin-lead alloy can be directly soldered using conventional reflow. Some products may also be socketed.

3.2.3.5 Palladium Plate

A palladium plated lead is composed of a copper base metal, a layer of nickel and a very thin layer of palladium. The key role of the palladium is to protect the underlying nickel plate from oxidation during the assembly process, as well as storage prior to use. Also, since the stitch bond is made directly to the nickel surface, through the palladium, instead of to silver, all silver is eliminated from the package. This eliminates the risk of silver migration causing extraneous electrical contacts.

Since palladium has a more consistant plating thickness, the advantages of fine pitch (0.5 mm or less) packaging becomes more obvious. The user can more accurately control the solder volume in the joint, thus solder bridging control is more easily obtained.

3.2.4 Process Comparisons

The information in figure 3-3 illustrates the process steps that usually occur for leads that are solder plated vs. those leads that have been solder coated. As can be seen from figure 3-3 there are several more steps in the solder coat process.

SOLDER PLATE	SOLDER COAT
Package Assembly	Package Assembly
Fixturing	Fixturing
Pretreatment	Pretreatment
Rinse	Rinse
Plate	Dry
Rinse	Fluxing
Dry	Preheat
Quality Assurance	Solder Coat
	Cool
	Rinse
	Dry
	Quality Assurance

Figure 3–3 Solder/Coating/Plating Process Comparison

3.2.5 Plastic Packages

The molded plastic package is normally a package made up of a copper alloy or alloy 42 lead frame, silvered-filled polymeric die attached adhesive, the silicon chip, gold bonding wires, and epoxy molding compound. Each of these components has a unique set of physical properties. The varying coefficients of thermal expansion present a challenge to maintain mechanical integrity of the bulk materials and interfaces between them.

Because of the different rates of expansion and contraction, stresses concentrate at the interfaces between materials during the temperature excursions typical of accelerated reliability testing and circuit-board mounting. When these stresses exceed interfacial strength between materials, loss of adhesion can occur. The presence of absorbed moisture in the molding compound exacerbates this phenomenon.

In order to prevent failure of the encapsulant during processing, testing, and end use, many different approaches are taken. From the material prospective, the supplier of the molding compound synthesizes the polymer to exhibit minimum moisture absorption. In addition, coupling agents are used to maximize adhesion between the epoxy matrix and silica filler to limit moisture ingress.

Optimization of other material properties such as flexure strength, module and toughness, ensures that the material can perform under severe moisture and temperature cycling conditions without the occurrence of cracking, which can lead to ingress of corrosion-causing contaminants. The molding compound contains the elastomeric toughening agents that curtail the growth of cracks, should they begin. These low stress materials also provide protection to the fragile chip surface for preventing cracking and shear

deformation of the thin film structures that make up the circuitry.

Careful package and process designs also ensure integrity of the molded package. Package engineers employ design features that provide robustness to the component by creating mechanical locks between the molding compound and chip lead frame. The material flows are designed to maximize adhesion and limit exposure to moisture during the manufacture, shipping and board mounting of the component.

3.2.6 Ceramic Packages

Ceramic packages are normally used when hermetic sealing is required. Hermetic sealing of I/C packages is used to seal the silicon electronic component from the external environment, specifically from water vapor and contamination that can shorten the lifetime of sensitive electronic devices.

3.2.6.1 Metal-filled Ceramic Packages

Two types of hermetic seals are normally used. One uses a hard solder precious metal brazing alloy (laminated ceramic package family) and the other a low melting-temperature glass (pressed ceramic package family).

The metal-sealed packages are of the laminate ceramic type and involve the brazing of a metal lid to gold-plated thick film seal ring on the ceramic. The glass-sealed packages utilize glass to create the seals between the pressed ceramic piece parts. The hermeticity of various sealing materials shows that metals provide the longer life time seal or impermeability, where as epoxies and silicon show the lowest opportunity for those characteristics. Thus, metal seals provide the highest level of hermeticity followed by glasses and ceramics.

The metal-sealed packages utilize a gold-tin eutectic hard solder to create the hermetic seal. The composition of the alloy is 80% gold and 20% tin and has a melting point of 280°C. This solder is chosen for its excellent wetting characteristics to the seal ring and lead materials, and is highly resistant to thermal fatigue. Seals created by the Au-Sn as well as its tin alloy can withstand thousands of thermal cycles without failure.

The gold-tin eutectic seal is made to a seal ring in the surface of aluminum oxide ceramic. The seal ring is composed of a tungsten thick-film that is fired to the ceramic material and plated with a thin nickel diffusion barrier and a gold over-plate. The gold over-plate prevents oxidation and provides a wettable surface for the solder.

The lid material is a gold-plated alloy 42 (a nickel-iron alloy with low thermal expansion) to which is attached an 80% gold and 20% tin alloy (eutectic composition) preform. The seal preform is attached by spot welding. The lid material is chosen for its stiffness and because the thermal expansion of alloy 42 is close to that of aluminum oxide ceramic.

3.2.6.2 Glass-Sealed Ceramic Packages

In glass-sealed packages, a ceramic lid is sealed to the base ceramic with a vitreous (non-crystallizing) lead based glass having a low melting temperature. The glasses chosen for hermetic sealing are lead-zinc borates that generally seal in the 415/450 °C range.

The glasses used in the industry have compositions in this range, with the final selection based on obtaining the lowest possible processing temperatures. As a result, the most commonly available seal glasses have very similar compositions. The glasses are highly resistant to chemical plating baths and have excellent thermal shock resistance. The variety of the glass that is used for package sealing also has high thermal expansion capability relative to the ceramic. To reduce thermally induced package stresses, it is necessary to reduce the thermal expansion of the glass by adding lower temperature expansion fillers. These fillers are chosen to be compatible with the lead glass and do not react during processing.

Because glasses all have similar composition, they have similar strengths. The glass used most often can be seen to have bending strength equivalent to other commonly used glasses. The fractured toughness is also found to be quite similar. It is expected that mechanical performance of sealed glass will be equivalent to other commonly used glasses.

3.2.7 Die Attach

Die attach is an important part of the component assembly process that ensure the parts performance requirements for the user. There are usually two types of die attach materials: adhesives (organic and in-organic) and hard solders (gold-silicon eutectic).

The choice of die attach materials depends on the specific applications and is compatible with the particular packaging technologies to insure the highest level of performance and reliability. Table 3-1 shows the relationship between the various packages and the die attachment material used and its type.

3.3 Heat Dissipation Techniques

Thermal management of the electronic system encompasses all the thermal processes and technologies that must be utilized to remove and transport heat from individual components to the system thermal sink in a controlled manner.

Thermal management has two primary objectives. The first is to insure that the temperatures of all components are maintained within both their functional and maximum

Table 3–1

Package	Die Attachment	Material Type
Pressed Aluminum Ceramic (Cerdip, Cerquad)	Silver-Filled Glass	Inorganic Adhesive
Laminated Aluminum Ceramic (PGA, CQFP, Side Brazed)	Gold Silicon Eutectic Silver-filled Cyanate Ester Silver-filled Glass	Hard Solder Organic Adhesive
Molded Plastic (Alloyed 42 Lead Frame)	Silver-filled Epoxy	Organic Adhesive
Molded Plastic (Copper Lead Frame)	Silver-filled Epoxy	Organic Adhesive

allowed limits. Functional temperature limits provide the temperature range within which the electrical circuits are expected to meet their specified performance requirements.

Operation outside the range may result in degraded machine performance or logic errors. The maximum allowable temperature limit is the highest temperature to which a component or part of a component may be safely exposed. Operation above the allowable temperature limit may result in actual physical destruction of the component or irreversible changes in its operational characteristics.

The second objective of thermal management is to ensure that distribution of component operating temperatures satisfies reliability objectives. Although failure to meet this objective may not be as readily apparent as failing to remain within maximum temperature limits, in the long run it can be equally costly.

Failure mechanisms encountered in electronic components are kinetic in nature and depend exponentially on device operations temperatures. The exact relationship between failure rate and temperature depends upon the packaging materials and processes and the failure mechanism in operation. This relationship can be illustrated (for changes in device characteristics resulting from chemical or diffusion processes) by using a normalized failure rate equation.

Relative heat flux levels of various devices and natural phenomena are shown in Figure 3-4. As seen from the figure, the heat flux at the die level is only about two orders of magnitude less than that on the surface of the sun. But the sun's surface temperature is 6000 °C, compared to a maximum chip operating temperature of 100°C for typical semiconductor devices. The challenge of thermal design is to continue to maintain die temperatures at acceptable operational temperature levels regardless of the increased power density. Operation of a device outside the specified temperature range can result in degraded machine performance or logic errors. Failure rates increase by a factor of two for every 10 °C increase in operating temperature; therefore, reliability concerns are a significant factor in thermal design.

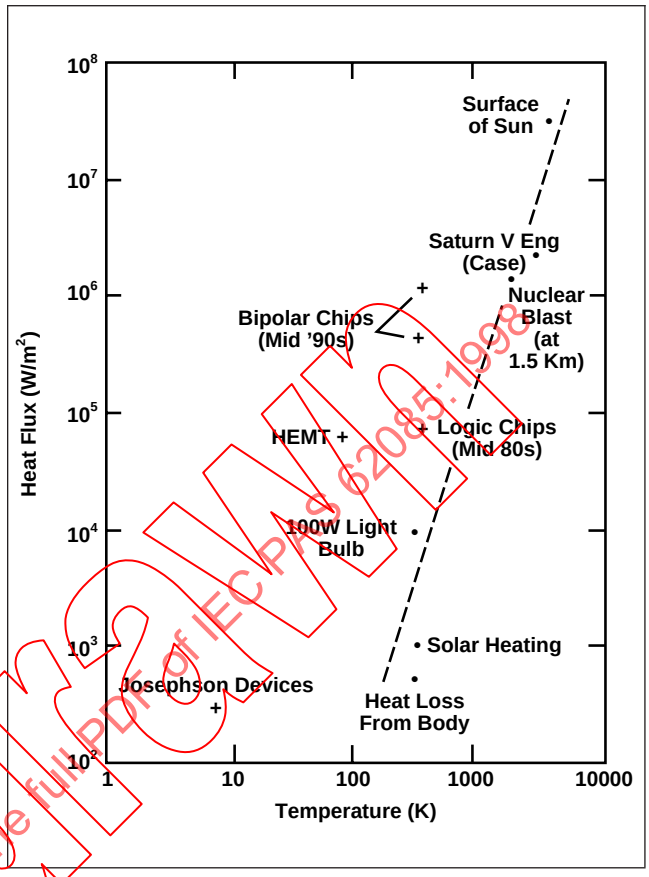


Figure 3–4 Temperature Differences Attainable as a Function of Heat Flux

Heat transfer through a given package can occur in various modes depending on the system environment. In mobile systems, fans are not typical and the heat must be dissipated from the component through heat flow channels that are narrow. In desktop environments, typically a system fan and a power supply fan exist and low air flow levels can be expected to aid more in the cooling process. In servers, additional degrees of freedom are available to provide room and increased airflow to address higher power dissipation.

The cooling technology selection must be made at an early stage of the design. Shown in figure 3-5 is a map that reflects the temperature difference necessary to support dissipation of heat (heat flux is defined as heat per unit exposed surface area of the package) to cooling technology assuming no enhancements have been made to the package (e.g., by addition of heat sink).

The temperature mapping in figure 3-5 can be used as a rough estimate to provide the designer with a starting point so that thermal requirements be accommodated in the design.

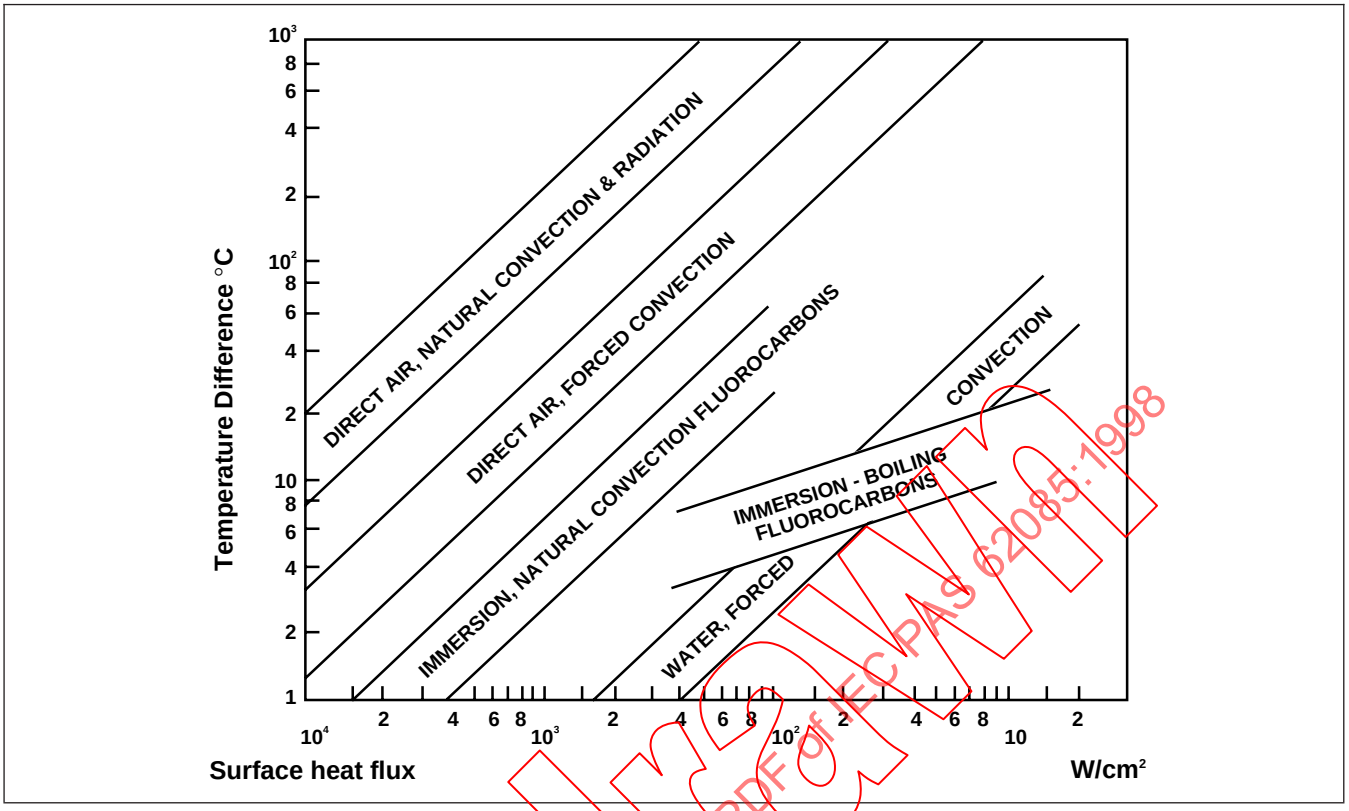


Figure 3−5 Heat Flux vs. Temperature Level

Example: Assume that it is necessary to determine the mode of cooling that would be appropriate for a 25 mm x 25 mm x 1.75 mm package (body only) dissipating 1.2 watts. The case temperature is to be maintained at 85 °C and the air temperature in the vicinity is expected to be 45 °C. The temperature difference available for cooling is (85 - 45) = 40 °C. The package of size has an approximate surface area of 8 cm^2, (including top surface area plus the four sides of the package); the bottom surface does not participate as it is not exposed to any cooling medium.

Package heat flux = 1.2/8 = 0.15 W/cm^2.

Then from figure 3-5 using 40 °C and a flux of 0.15 W/cm^2 it is easy to see that this part can be cooled by air under natural convection environment.

It must be noted that these estimates are based on gross simplifications and refinements are necessary in the later phases of implementation.

Heat transfer from a package assembled onto an interconnecting structure (e.g., printed board) can occur through various modes. These are described in the following paragraphs.

3.3.1 Conduction

Conduction is a process by which heat flows from a region of higher temperature to one of lower temperature within a medium (solid, liquid or gas) or mediums in direct physical contact. Multilayer printed boards with metal cores are an excellent way to remove the heat from the component. Thermal vias are positioned under the component and provide the thermal path to the heat sinking planes.

The fundamental feature of conduction is the transmission of thermal energy by direct molecular communications without appreciable displacement of the molecules.

In a one dimension form the Fourier law governing conduction can be represented by:

$$q = kA\,\Delta T/L$$

where: q = Heat flow rate (W)
k = Material thermal conductivity (W/m°C)
A = Cross sectional area (m^2)
$\Delta T/L$ = temperature gradient (°C/m)

The temperature difference resulting from the flow of a specified heat rate from a fixed cross section is thus related to the thermal conductivity of the material (k) and the path length (L). From an electrical analogy, if q and ΔT represent current and voltage respectively, L/kA is thermal resistance of the conduction path. While packages are made of a wide variety of materials and shapes, the process of heat dissipation from the junction to the surface(s) of the package is by conduction.

While the manufacturer sets the maximum or junction temperature limits, the component mounted on a board needs

to have a microenvironment that can satisfy the necessary condition for thermal control. Components are typically cooled by air and the heat transfer phenomenon for cooling the case of a package is described by convection.

3.3.2 Convection

Convection is a process of energy transport by the combined action of heat conduction, energy storage and mixing motion. It is a complex mechanism of energy transfer from a package surface to surrounding air. This process takes place in several steps. First, heat will flow by conduction from the package surface to immediate adjacent air molecules. The energy thus transferred will increase the temperature and internal energy of the air molecules. Due to the ability of air molecules to move more freely, the heated air molecules will move to a region of lower temperature of air where they will mix with the colder air and transfer part of the their energy to the colder fluid molecules. Note that unlike conduction, the flow in this case is of air as well as energy. The heat energy transferred from the package surface is stored in the fluid and is carried away as a result of mass motion. The effectiveness of heat transfer by convection depends largely upon the mixing motion of the air. The simplified relationship that captures this phenomena is commonly referred to as Newton's law of cooling as given below.

$$q^c = hcA(Ts - Ta)$$

where: q^c = convective heat flow rate from surface to ambient (W).
Δ =surface area (m^2)
Ts =Surface temperature (°C)
Ta = Ambient temperature (°C)
h^c = average convective heat transfer coefficient ($W/m^2\ ^\circ C$)

The above equation recast into an electrical analogy form results in the convective resistance definition as $1/h^cA$.

The role of convective heat transfer in keeping the package surface at the desired temperature is extremely important as it is the ultimate sink for the heat dissipated from the component. Observe in the definition of the resistance, the effect of the surface area of the package. In order to maximize the efficiency of heat removal from the package surface, the product of the heat transfer coefficient and the surface area has to be maximized. The determination of h^c requires the knowledge of fluid flow and is the focus of thermal research. The typical range of heat transfer coefficients as a function of fluid choice is presented in Table 3-2. Note that although the magnitudes for air are not as high as in liquids, the ease of use combined with simplicity in design promotes the use of air cooling as the primary mechanism in personal computers.

In the absence of a system fan to force air through, air still participates in the cooling of the packages via the convection currents set up due to density differences that arise in hot and cold air. This process is called natural convection. Under natural convection conditions, orientation of the heated surface with respect to gravity plays a significant role in the cooling. In general vertical surfaces are to be preferred to horizontal orientation. The heat transfer coefficient indicated above encompasses the natural convection regime.

3.3.3 Radiation

Thermal radiation is defined as the radiant energy emitted by a medium by virtue of its temperature, without the aid of any intervening media. The physical mechanism of radiation is not completely understood. Radiant energy is sometimes envisioned to be transported by electromagnetic waves, at other times by photons. Neither viewpoint completely describes the nature of all observed phenomena. The amount of heat transferred by radiation between two bodies at temperatures T1 and T2 is governed by the following expression:

$$q = \epsilon\sigma(T_1{}^4 - T_2{}^4)$$

where q = amount of heat transferred by radiation (W)
ϵ = emissivity ($0<\epsilon1$)
σ = Stefan-Boltzman constant, $5.67x10^{-8}$ (W/m^2K^4)
A = area (m^2)
F_{12} = Shape factor between surfaces 1 and 2 (A fraction of surface radiation seen by surface 2)
T_1, T_2 = surface temperatures of radiating surfaces

While radiation is an important cooling for space vehicles, natural convection environments can also benefit from radiation. To estimate the magnitude of radiational cooling to the convective cooling described earlier a radiation heat transfer coefficient can be calculated as follows:

$$h_r = \epsilon\sigma F_{12}(T_1^2+T_2^2)(T_1+T_2)$$

It is not uncommon to find the radiational contribution to be of the same order as convective cooling especially in natural convection cooled packages. Oversight of this aspect can result in expensive over-design of equipment. Note that the radiational process is nonlinear and the above definition of h_r linearizes the phenomenon and is applicable within moderate temperature ranges.

3.3.4 Thermal Impedance

The complex material tradeoffs for different package families makes it rather difficult for analyzing component details by simple 1D conduction analysis. In order to provide data for a wide variety of packages, the industry has adopted lumping the effects of materials within the package

Table 3−2 Transfer Coefficient as a Function of Fluid Choice

Primary Cooling Mechanism	Typical HTC Range (W/m2K)	Relative Effectiveness	Achievable Density	Complexity of Implementation
Natural Convection(air)	10	0.1	Low	Very Low
Forced Convection (air)	100	1.0	Medium	Low
Natural Convection (liquid)	100	1.0	Medium	Medium
Forced Convection (liquid)	1000	10.0	High	High
Boiling (liquid)	5000	50.0	High	High

by defining thermal impedance values. Under identical conditions, the package with lower impedance value provides a better thermal solution. The most commonly used ones are defined by the following relations:

$$\Theta_{ja} = (Tj - Ta)/P$$
$$\Theta_{jc} = (Tj - Tc)/P$$
$$\Theta_{ja} = \Theta_{jc} + \Theta_{ca}$$

where:

Θ_{ja} = Junction to ambient thermal resistance (°C/W)
Θ_{jc} = Junction to case thermal resistance (°C/W)
Θ_{ca} = Case to ambient thermal resistance (°C)
Tj = Maximum die temperature (°C)
Tc = Case temperature at a predefined location (°C)
P = Device power dissipation (W)
Ta = Ambient temperature (°C)

As can be seen from the above definitions, the various resistances are derived from experimental measurements. For the characterization of packages, temperature-sensitive parameter (TSP) method is most common. This method uses special test structures cut to the same size as the actual device, consisting of resistors and diodes. Resistors are used to simulate the device power dissipation, and the diodes located at different points on the chip surface provide junction temperature data. It is important to recognize that the lumping process of all the materials in a package requires that the location of the measurement of the case temperature be specified.

For single device packages, the manufacturer typically identifies the predominant heat flow path from the packages and chooses a location to identify the heat flow path. For example, in the case of cavity-down PGA packages the center of the top surface yields the highest case temperature. However, a cavity-up package at the same location would result in lower temperature due to the longer path to the device.

Another variable of importance is the definition of ambient temperature. For the data that is measured in air, it is typically defined as the unchanging temperature at a distance away from the package test section. Component data in earlier days have reported using a constant-temperature agitated bath. The applicability of such information to air cooled system environment is poor. In using component level data, the applicability of test conditions to the end user conditions should be carefully evaluated. The best source of data is one that replicates both the mounting configuration of the user and the airflow environment.

The data pertaining to the junction-to-case thermal resistance provides the end user with lumped effects of the material properties of the package and considerably decreases the need for detailed level models of conduction paths at the board and system level analysis.

3.3.5 Component Level Thermal Characteristics

The component provided by a manufacturer can be utilized in a variety of environments, and it is not possible for the vendor to provide data relating to all application configurations. However, certain information in the form of impedances are provided. These are typically provided both under conditions with still air and air velocities that cover a broad spectrum. As indicated in the description of the convection process, the area of a package has a significant impact on the thermal resistance of a package.

Shown in figure 3-6 are the typical junction-to-ambient resistance for different package families as a function of lead count. Note that packages of smaller size and made of lower conductivity material have higher resistance to heat flow under identical conditions. Observe that for a given package type, the thermal resistance decreases as the package size grows. The package resistance also serves the purpose of assisting the designer in evaluating package alternatives for the same function. Indirectly, given an environment in a system (e.g. fan-less system) one can use the thermal characteristic to determine to the first order whether the power dissipated by the component can be handled without addition of heat sinks or an alternative package style with better performance can be selected.

Package styles are numerous and the heat flow paths from the die are essentially different on each one of them. Use of copper lead frames, spreaders and slugs influence the package characteristics. In the use of data published by the component manufacturer, the effect of board conductance on the measurements provided, must be considered.

This is particularly important for fine pitch parts with copper lead frames. Based on layer count and copper content

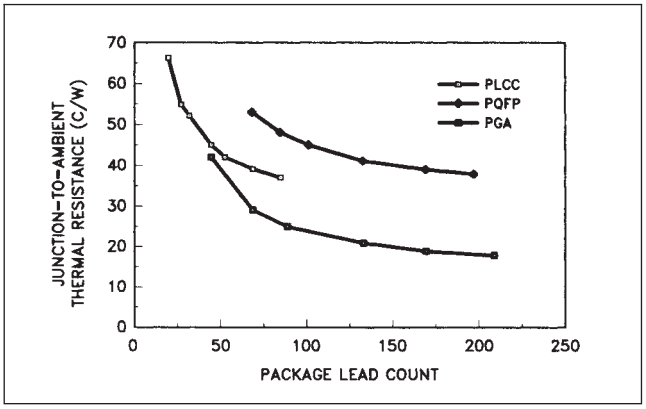


Figure 3−6 Effect of Package on Thermal Resistance of PLCC, PQFP, and PGA Packages

in the board the effective thermal conductivity can be computed for a specific design. Shown in figure 3-7 is the effect of board conductivity on the measured thermal resistance for PQFP package. As the effective board conductivity increases, the spreading resistance through the board reduces and the board participates to an increasing level in the heat removal from the package.

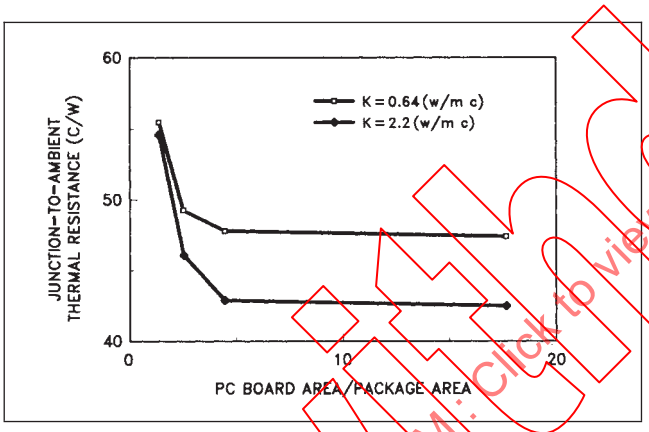


Figure 3−7 Effect of PC Board Material Size on Thermal Resistance of 132-Lead PQFP

Airflow tends to decrease the Θ_{ca} (i.e. the external resistance) and tends to have minimum influence on the internal resistance of the package. Such data is commonly published for a wide variety of packages in the vendor's data book. The data for a 168 lead cavity down package is presented in figure 3-8. In some cases, resistance values with heat sinks attached to the part are also presented. A well designed heat sink in conjunction with interface (attach material) can reduce the external resistance of the package by decreasing the external case-to-ambient resistance. This allows the designer to dissipate additional power from a device while maintaining the device temperature within prescribed limits. However, the penalty is increased volume. While data typically extends to high air flow rates, the acoustic limits established at the system level do not normally permit high air velocities to be attained.

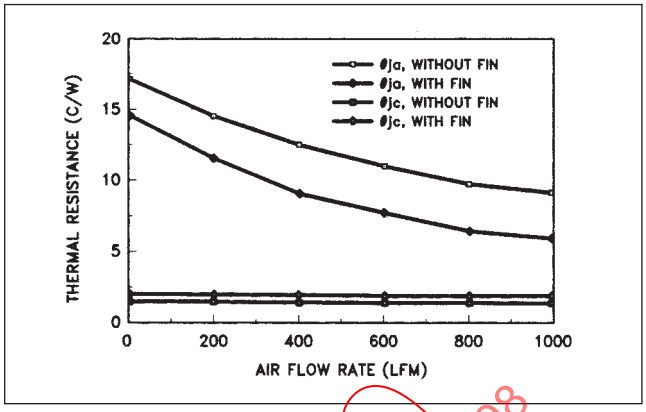


Figure 3−8 Effect of Air Flow Rate on Thermal Resistance of 168-Lead PGA Package

3.3.6 Board Level Thermal Management

In the context of a system, the various components are assembled to establish a board level product. In moving from a component level description to a board level analysis, the environment in which the board is employed has a major influence on the thermal design. To address the need for increased functionality, the separation distance between components is kept to a minimum within manufacturing limits. This is a sharp contrast to the test configuration in which individual packages are characterized.

For natural convection environments the local effects play a major role. Factors such as separation of cards and the inlet vents and orientation result in differing case temperature values for a given board. Recirculation patterns result in complex flow and thermal interactions when combined with nonuniform package geometries, and power dissipation is not amenable to generalized calculations. However, the correlations for plates having uniform spread out loading can serve as a rough guide to calculate temperature and heat transfer capabilities.

It must be noted that these correlations do not include the effects of radiation. It is often instructive to compute radiational contribution of the heat transfer coefficient to ascertain that an important effect is not ignored. Normally the radiational heat transfer between identical boards placed parallel and powered on (close approximation to the system's card environment) is minimal, as the temperature difference between the boards is negligible.

3.4 Handling and Storage

3.4.1 ESD

Electrostatic Discharge (ESD) protection is essential for handling almost all high performance packages. Damage to sensitive devices can result from failure to control the static electricity generated in simple human and machine movements. High voltages, in excess of 5,000 volts, can be generated by the rubbing of common materials: wood, plastics,

fabrics, in normal activities on the manufacturing floor. This electrical charge must be controlled because many components can be damaged by as little as 30 volts.

The threshold voltage where ESD damage can be sustained by a device has been divided into five categories by the Electrical Overstress/Electrostatic Discharge Association, Inc.

Class 0 0 to 199 volts
Class I 200 to 499 volts
Class II 500 to 1999 volts
Class III 2000 volts and above
Class IV no ESD sensitivity

Most high performance packages require class 0 ESD protection. The device manufacturer defines the ESD constraints on the device, and an ESD specification should be provided with the product data.

A standard symbol for ESD protection requirements, a hand superimposed on a triangle with a yellow/black format, provides universal recognition of this surface mount process requirement. The ESD Class can be printed on the hand near the wrist. This symbol can be used to identify areas and process machinery that must be ESD protected. Use of the symbol on the components is desirable, but marking space constraints often preclude this practice.

Printed board assemblies, containing electrostatic sensitive components (ESD) are marked with the circular symbol containing three inward pointing arrows. The ESD symbol may be marked or screened, using a permanent ink or label, able to withstand assembly processes, or etched in copper on the printed board. (See figure 3-9)

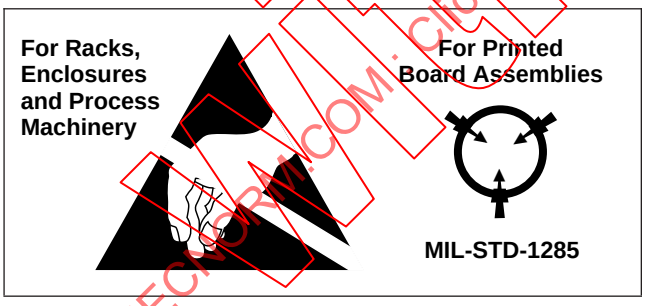


Figure 3–9 Standard ESD Symbols

3.4.1.1 ESD Control

ESD control consists of bleeding off any electrostatic charge through conductive paths to ground in all portions of the process equipment, part containers, and in the human interface. Many areas of the process equipment must be altered in construction or provided with a surface treatment to provide a conductive path for static charges. Air ionizers strategically located in the process area reduce static build-up. The human interface is a significant problem due to the static generating nature of most clothing, shoes, etc.

Control devices include static dissipative jackets or suits, grounding foot straps or foot wear, conductive floor finish, and wrist straps electrically connected to ground. It is preferable to have static dissipative (10^5 to $<10^{12}$ ohms per square) surface resistivity rather than conductive surfaces (0 to $<10^5$ ohms per square). Conductive surfaces may contribute to component damage by providing an excessively rapid discharge of an electrostatic charge. It is preferable to have the component in contact with static dissipative surfaces during handling, storage, and assembly. In addition, maintaining a moderate room humidity (30% to 50% R.H.) promotes static dissipation.

Measurement of ESD parameters is essential for working with sensitive components. Tools required for monitoring ESD include the electrostatic field meter that detects and measures the voltage and field strength associated with static charges on equipment, materials, and people. Additional testing is performed with surface resistivity meters to determine effectiveness of ESD coatings on equipment and facilities, charge plate monitor to evaluate air ionizers, and a personal grounding tester to measure the effectiveness of ESD protective equipment worn by personnel in the area.

All personnel in the area should receive training that describes the nature of ESD damage, the procedures necessary to prevent this damage, and care to be taken in handling sensitive components. One or more persons should be assigned to monitor the ESD control activities, procedures, training, and equipment for the production facility. This person or committee must have the responsibility and authority to enforce ESD controls.

3.4.1.2 Shipping Media

ESD-sensitive components must be shipped and stored in ESD-approved static dissipative containers and packing materials. The package must be opened on a static dissipative surface and ESD-controlled area. Components should be removed from the container with proper regard to ESD control in the work surface, containers, implements, and personnel. (See EIA-583 and EIA-541)

Proper labeling on shipping containers must be an essential part of the contract between the supplier and user. Internal part numbers, if used, must be assigned and clearly labeled at incoming inspection. Transfer of the part identification from the stock location, reel, tube, or tray to the feeder location on the process equipment is a prime source of error. Requiring that a second person check and sign off on all stock room transactions, machine set-ups, and part handling activities has proven effective in controlling these errors.

Moisture-sensitive components must be shipped in sealed moisture-resistant containers with an effective desiccant material included in the package. IPC-SM-786 provides information on handling moisture-sensitive components. In

many instances a label is provided as shown in figure 3-10 to indicate the effectiveness of the moisture resistant container.

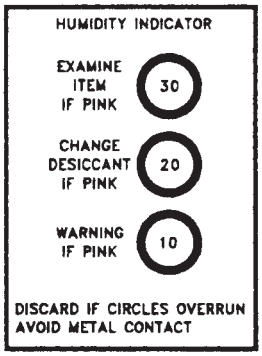


Figure 3−10 Moisture Level Indicator

3.4.1.3 Storage Environments

ESD considerations dictate that the stock room shelves must be static dissipative and properly grounded. All carts, benches, and work stations should be static dissipative and have grounding devices. This will ensure that all ESD sensitive components will be protected while being unpacked, counted, handled, and issued to the process station.

Plastic packages are often subject to moisture absorption. At reflow temperatures, the pressure build-up from the moisture causes cracks in the plastic body. Components with larger chips tend to be more sensitive to cracking. These cracks may easily escape detection if they are located in an area that is under the part. The concern is that flux and other process chemicals will be entrapped in the cracks and lead to reliability problems. Maintaining dry components (below 0.1% moisture by weight) eliminates the possibility of crack formation.

An acceptable practice is to store moisture-sensitive components (plastic packages) in unopened protective packages at room atmosphere. Once opened, the components must be stored in a dry chamber. The dry chamber must have an impermeable seal and a source of dry gas to fill and maintain the chamber atmosphere. Normally some bleed through is used to maintain chamber conditions. Dry nitrogen or dry compressed air of less than 1% R.H. may be used for the chamber atmosphere. A compressed air supply often has very low humidity when brought to atmospheric pressure but should be calibrated. A desiccator can be used but is not preferred because there is no circulation of the dry atmosphere to purge the chamber.

Parts that have moisture present because of improper shipment/storage or have been opened and allowed to absorb atmospheric water must be baked to remove moisture. Table 3-3 provides information and classification to six levels for floor life of desiccant packed components.

One option is to bake at high temperature, typically 125 °C ±5 °C for 24 hours at less than 50% Relative Humidity. This is the most expedient means of removing moisture from components, but it cannot be performed on parts in reels or other packaging that cannot withstand the temperature. In addition, components are limited to two bake cycles to prevent excessive growth of intermetallics and consequent reduction of solderability of the leads. Components must be cooled to room temperature prior to assembly to prevent viscosity reduction of the solder paste and subsequent solder bridges.

The second alternative is a low temperature bake at 40 °C +5 −0 °C for 192 hours at less than 5% Relative Humidity. These conditions can be used for components in reels or trays. There are no time limits for the exposure of components to this temperature. As in the high temperature bake, components must be cooled to room temperature prior to assembly.

The effectiveness of moisture removal or the amount of moisture in a component can be determined by measuring weight loss in successive bake cycles. When no weight loss is observed in two one-hour high temperature cycles, the components are free of moisture. The measurements must be accurate to better than 0.1% of the component weight.

If the components are not assembled in a reasonable amount of time, they must be stored in a dry atmosphere after baking. The length of time a part can be in room atmosphere after opening the moisture resistant container or removal from a bake cycle is dependent on room humidity, temperature and the characteristics of the component package. Since most process areas are controlled at a relative humidity of between 30% and 50% to minimize static problems, a typical allowable time for a component at room conditions is 8 days. At higher relative humidity, this time must be reduced. Exact limits can be determined by percent moisture measurements with the criterion of maintaining component moisture below 0.1%.

3.4.1.4 In-Process Handling and Control

ESD precautions must be taken during the handling of components, loading feeders, trays, etc.

A critical issue is part number control. Accidentally placing the incorrect component is a very common error. With fine pitch and high density components this error becomes increasingly serious due to difficulty in reworking these parts. Often a misplaced component must be scrapped during rework, or, in the worst case, the entire assembly may be damaged by the additional thermal exposure incurred by attempts to remove the incorrect part. A very effective method is to have a second person check and sign-off on all stockroom issues, feeder loads, and machine set-ups. The additional confirmation time is insignificant compared to the loss incurred by scrap of a fine pitch, high density

Table 3–3 Classification and Floor Life of Desiccant Packed Components

LEVEL	FLOOR LIFE (OUT OF BAG) AT BOARD ASSEMBLY SITE	MOISTURE EXPOSURE	
		°C/%RH	TIME (HRS)
1	UNLIMITED at ≤85% RH	85/85	168
2	1 YEAR at ≤30°C/60% RH	85/60	168
3	1 WEEK at ≤30°C/60% RH	30/60	168 + MET
4	72 HOURS at ≤30°C/60% RH	30/60	72 + MET
5	As Specified on Label: 24 or 48 hours at ≤30°C/60% RH	30/60	time on label + MET
6	Mandatory Bake Bake before use and once baked must be reflowed within the time limit specified on the label	30/60	time on label

component or board.

Lead integrity and coplanarity must be retained in all handling operations. Key areas are the support given in feeders, trays, and work areas. Support must be placed on the body of the component, never the leads. (See paragraph 4.3.2.)

In the case of plastic bodied components, part of the handling procedure must be to ensure that only moisture free components are assembled.

4 PACKAGE DETAILS

IC packaging as a rule has been developed to be compatible with most solder attachment technologies. Many of the multi-functional high performance devices are more difficult to handle in a manufacturing environment than some of their counterparts. The contact leads of fine pitch quad flat packs (QFPs) devices, for example, are very fragile having both high I/O and close lead spacing or pitch (<0.63 mm)

Plastic and ceramic area array package devices on the other hand have a wider contact pitch (>1.0 mm) and the chip scale and micro ball grid array package has established a 0.5 mm as the basic grid pitch.

As a general statement, the grid array package is more rugged and robust than the fine pitch device, and assembly processes yield on items like the BGA has proven to be superior to that of the gull wing fine leaded counterpart.

4.1 Area Array Package Description

The area array package is typically smaller, pin for pin, than the leaded alternatives. In addition, the ball contact is not easily damaged during assembly processes. Both BGA and micro BGA devices allow for depopulation of contacts to meet specific I/O requirements; however, the grid location conventions must be observed. Because of the higher lead density on the BGA and micro BGA component families, assembly specialists have found that both printed board quality and surface finish will directly affect the overall manufacturing process yields.

4.1.1 Physical Properties

The grid array device family includes square and rectangular package configuration and is furnished in either plastic or ceramic base materials. Base material serves as a mounting structure for attaching the die.

Depending on the physical characteristics of material for the plastic or ceramic BGA, flip chip or wire bond technologies may be employed for die attachment. Because the dye attachment structure is so rich in material, the dye bond or attachment site is generally centered with the conductor pads furnished to route the signal from the dye bond pads to the ball contact array matrix. Figure 4-1 provides an example of the plastic and ceramic BGA in top surface attach die to carry the down configuration.

The interface contact or grid is arranged in a uniform column and row format. The three standard basic spacing or pitch for the contacts are 1.0 mm, 1.25 mm and 1.5 mm. The contacts accommodate the electrical and mechanical interface between device and host interconnecting structure (PCB). The contact material will allow conventional reflow solder or other attachment processes.

The ball or column array device families are generally marked with the manufacturer's name or symbol, part number, date code and an orientation mark in the corner near contact 1-A. Method of marking is not defined.

Devices may be furnished in tube magazine, partitioned tray carrier or tape and reel packages. Tape and reel packaging is generally preferred for high volume assembly processing. However, if plastic array devices are specified, reels must be transported and stored in moisture-proof containers. For example, when plastic materials are exposed to the environment for a period of time, some plastics and laminates allow moisture absorption. The moisture may expand during reflow solder processes causing internal cracking and other physical damage.

The grid array devices are typically attached to the host interface structure using eutectic solder alloy. However, optional methods of attachment may include electrically conductive epoxy or polymer. Array package assembly

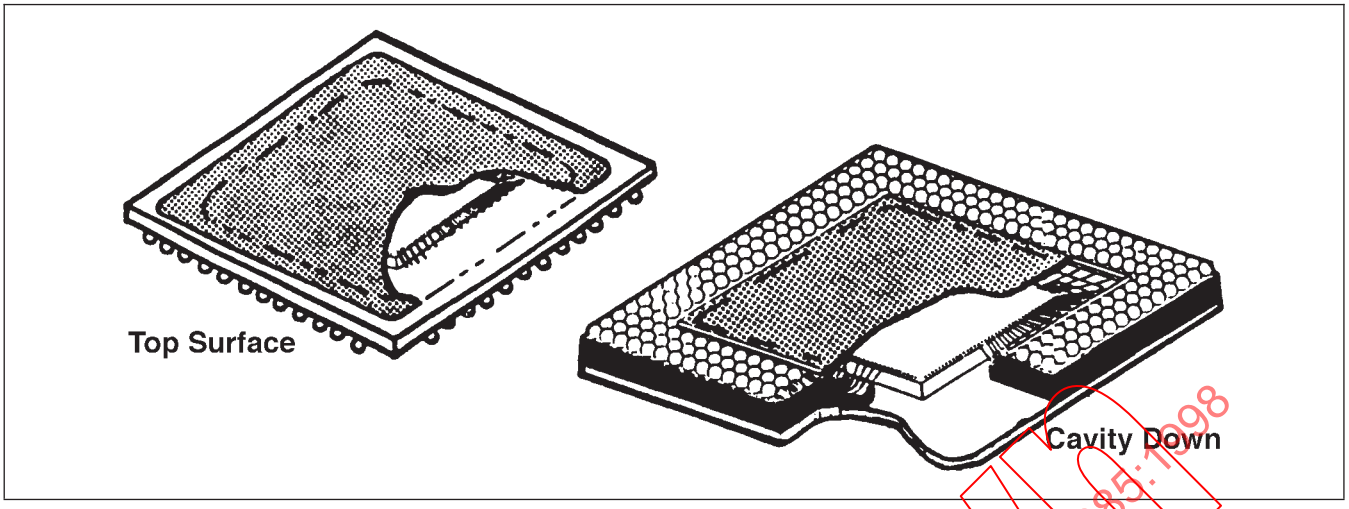


Figure 4–1 Ball Grid Array Devices Furnished with Die Mounted on Top Surface and Bottom Side for Cavity Down

should not require specialized equipment or processes beyond that currently in use for surface mount assembly.

4.1.2 Bump/Termination Layout

Both ball (or bump) and column contacts are standard for array package termination. The ball contact may be a preformed sphere attached to the device or formed on the surface by applying and reflowing a uniform volume of eutectic solder alloy paste. The paste material at each contact position, when liquefied, forms a somewhat spherical contact bump suitable for attachment to the host interconnect structure.

Column array contacts are cylindrical rods that are attached to the array pattern contact site as a final manufacturing step. Column contacts are primarily furnished on ceramic packages providing a compliant interface when attaching the device to a structure having a different temperature coefficient of expansion (TCE). The standoff height of column style packages shown in figure 4-2 is generally greater than the ball contact configuration.

Ball contacts are preferred for attaching plastic packages while columns provide a level of thermal compliance or flexibility needed when ceramic devices are attached to conventional laminated PCB structures.

The attachment site or land pattern geometry recommended for BGA and CGA devices are round with the diameter adjusted to meet contact pitch and size variation. The land pattern site can be the etched copper pattern with solder mask just outside the pad parameter or solder mask defined, an opening in the mask that is slightly smaller than the etched copper pad as compared in figure 4-3. Figure 4-3 shows the open etched copper land pattern compared to a solder mask defined land pattern.

When using the mask defined attachment site, the etched pattern size must be made slightly larger than the mask opening. Also note that physical shape of the solder fillet at the attachment site will be affected. The land pattern that is free of mask material will promote a uniform tapered slope or column profile while the mask defined land pattern promotes a controlled collapse of the ball profile during reflow processing. Column contact patterns should be free of mask material.

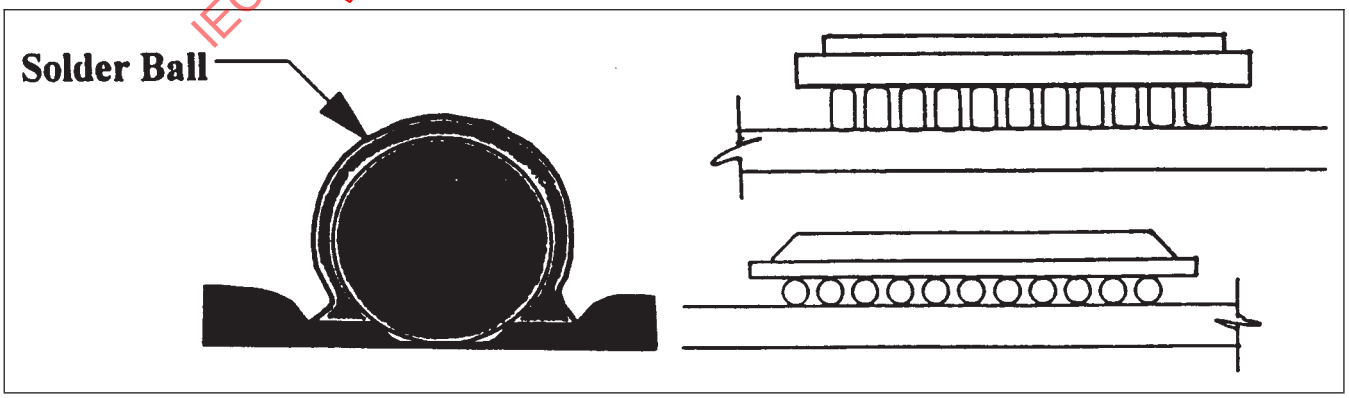


Figure 4–2 Stand Off Height

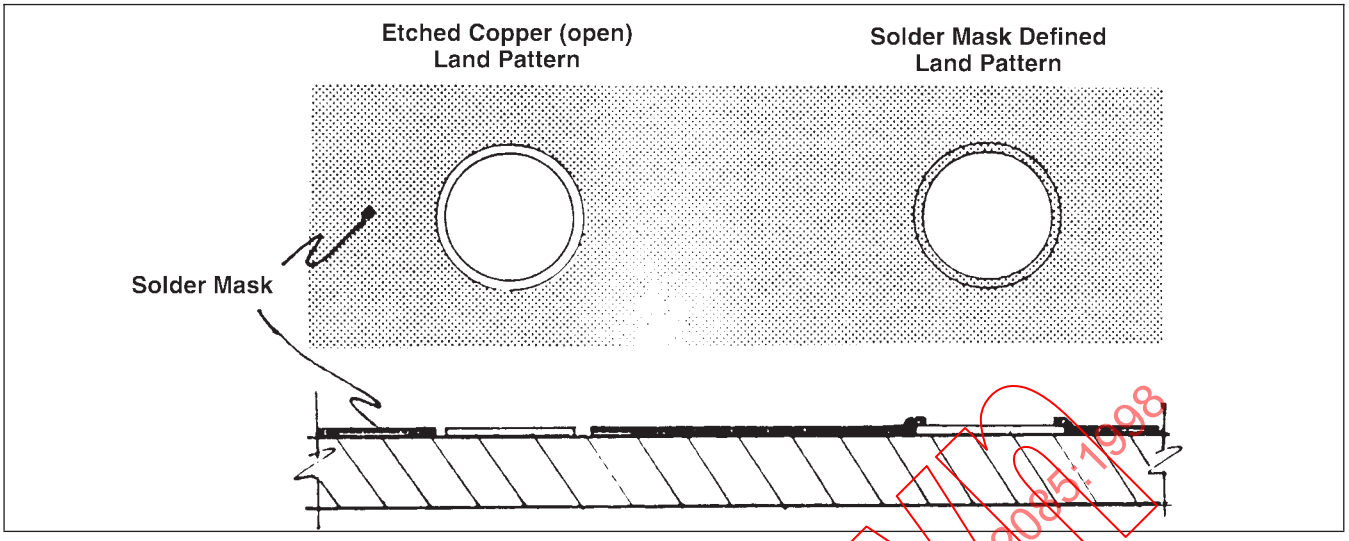


Figure 4–3 Land Pattern Comparisons

Because the land pattern array typically occupies most of the surface area under the device, signal routing for most of the contacts must be transferred to other layers of the host interface structure typical of that shown in figure 4-4.

4.1.3 Standardization

Array contact identification is standardized and is assigned by the column and row location. For example, A-1 contact is always at an outside corner position with alpha characters arranged in a vertical pattern from top to bottom. Numeric characters are assigned in a horizontal axis as shown in figure 4-5.

- MO-156 Ceramic Ball Grid Array (CBGA)
- MO-158 Ceramic Column Grid Array (CCGA)
- MO-163 Rectangular Plastic Ball Grid Array (R-PBGA)
- MO-157 Rectangular Ceramic Ball Grid Array (R-CBGA)
- MO-155 Rectangular Ceramic Column Grid Array (R-CCGA)

Registered outlines have been developed for a wide range of package configurations. Most of the registered package outlines define the features and physical limits related to a

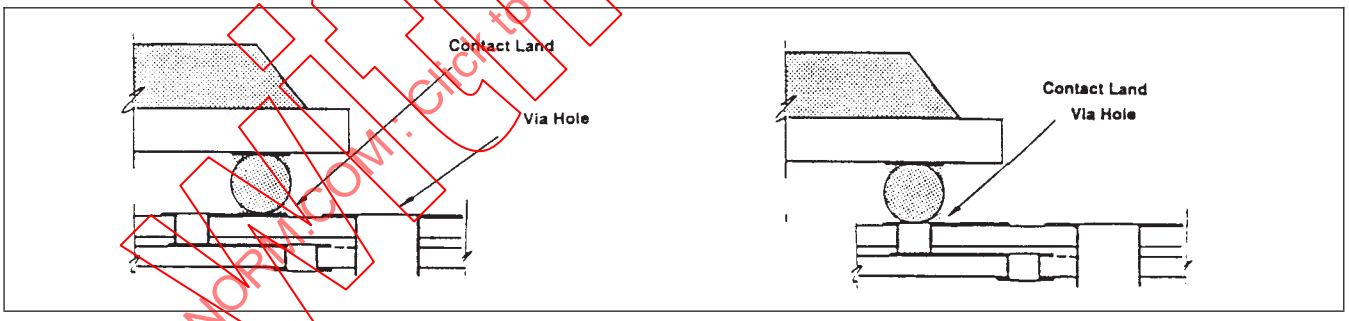


Figure 4–4 Signal Routing Approaches

Figure 4-6 shows the device specifications that illustrate the contact pattern when viewed from the bottom surface with A-1 at the upper right hand corner. The land pattern provided on the host substrate is opposite with A-1 contact to the left.

Sources for BGA and CGA standard documentation are provided by the Electronic Industries Association. EIA and JEDEC have registered outlines that deal with these documents and are published in JEDEC Publication 95. Some of the registered outlines for solid state and related products are:

- MO-151 Plastic Ball Grid Array (PBGA)

square shape having a symmetrical contact pattern array. The JEDEC MO-151 PBGA (plastic ball grid array) outline furnished in figure 4-6 specifies dimensional limits and tolerances for all physical features controlling the package.

4.2. BGA Types

Ball Grid Arrays come in a variety of configurations. Each has its purpose and application. Some are performance-driven to match the environment that they serve. Others are cost-effective to address the market sales profile.

The BGA device family includes square and rectangular

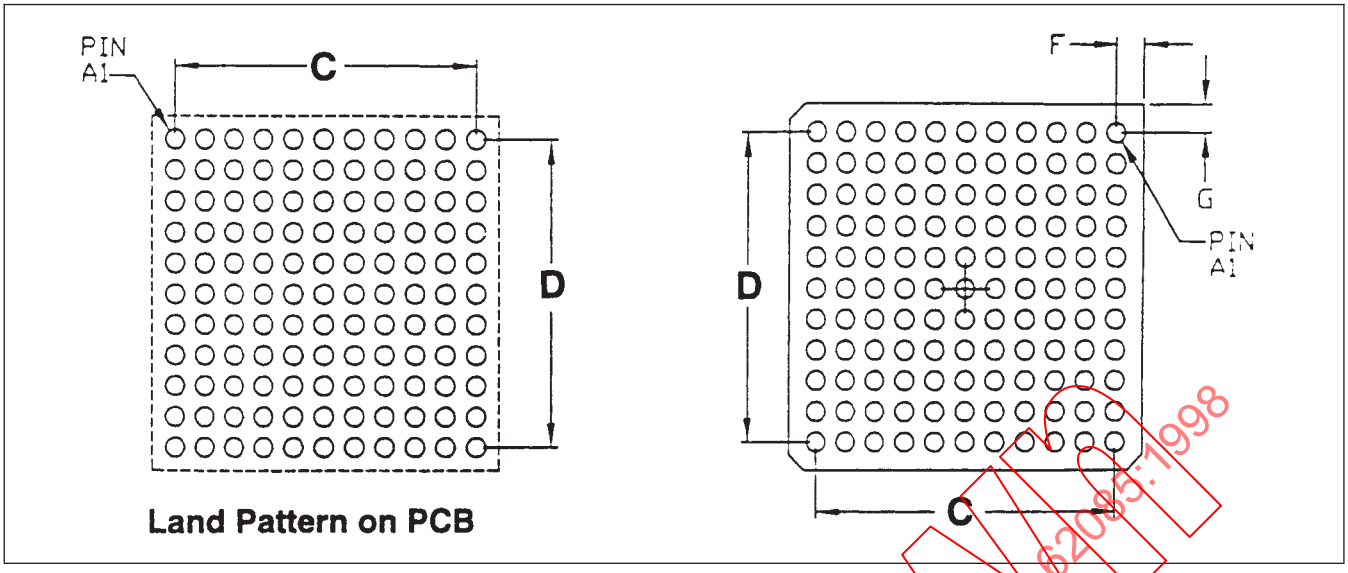


Figure 4–5 Contact Patterns

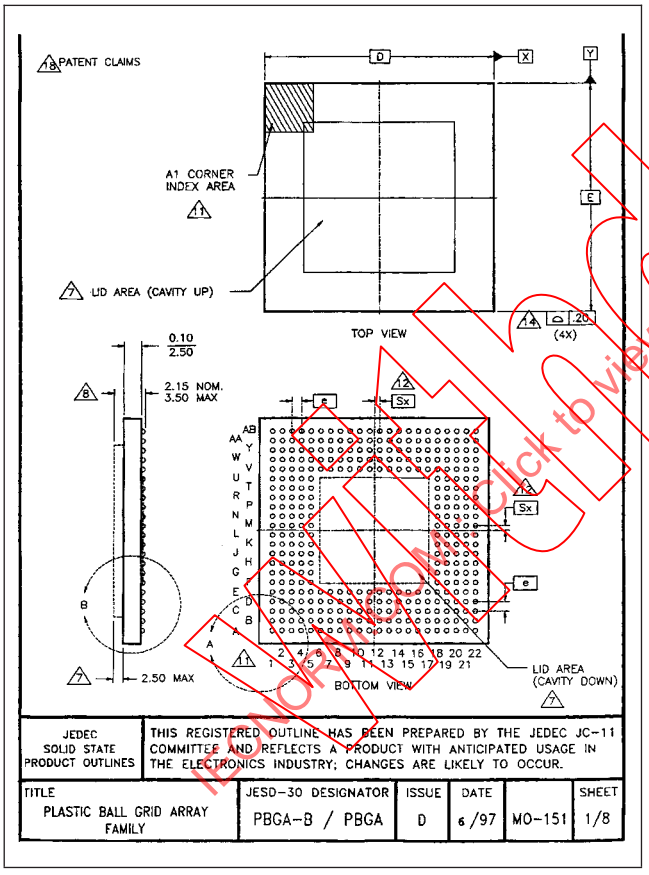


Figure 4–6 Physical Outline of BGA Package Specifications (Ref. JEDEC Publication No. 95)

package configurations and is furnished in either plastic or ceramic base materials. Base material serves as a mounting structure for attaching the die. Depending on the physical characteristics of material for the plastic or ceramic BGA, flip-chip or wire bond technologies may be employed for die attachment. Because the die attachment structure is a rigid material, the die bond or attachment site is generally centered with conductor paths furnished to route the signal from the die bond pads to the ball contact array matrix.

Figure 4-7 shows an example of cavity-up and cavity-down BGA chip mounting.

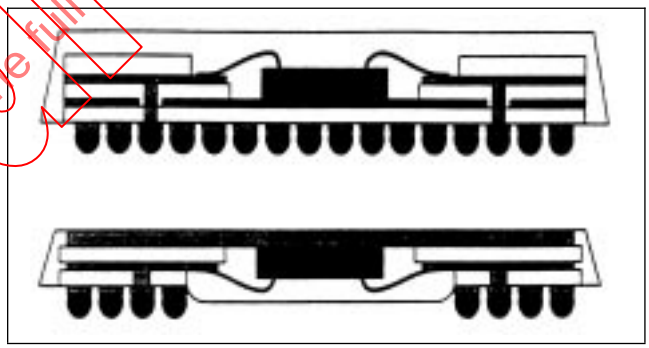


Figure 4–7 Cavity-up and Cavity-down Chip Mounting

4.2.1 Plastic BGA

This plastic BGA has the following characteristics:

- PCB laminate with higher TG (over 240 °C) epoxy resin (e.g. BT resin)
- Wire bond or flip chip interconnection
- Cavity up or down with fully populated or partially depopulated (cavity down) solder balls
- With or without heat slug (SuperBGA from Amkor as an example)
- 0.030 inch dia eutectic (63Sn/37Pb or 62Sn/36Pb/2Ag) solder balls

Figure 4-8 shows the cross section on the plastic BGA. The advantages of the plastic BGA are:

- Low cost and low profile package
- Eutectic solder balls ‘‘controlled collapse’’ and self align during reflow compensating for misplacement

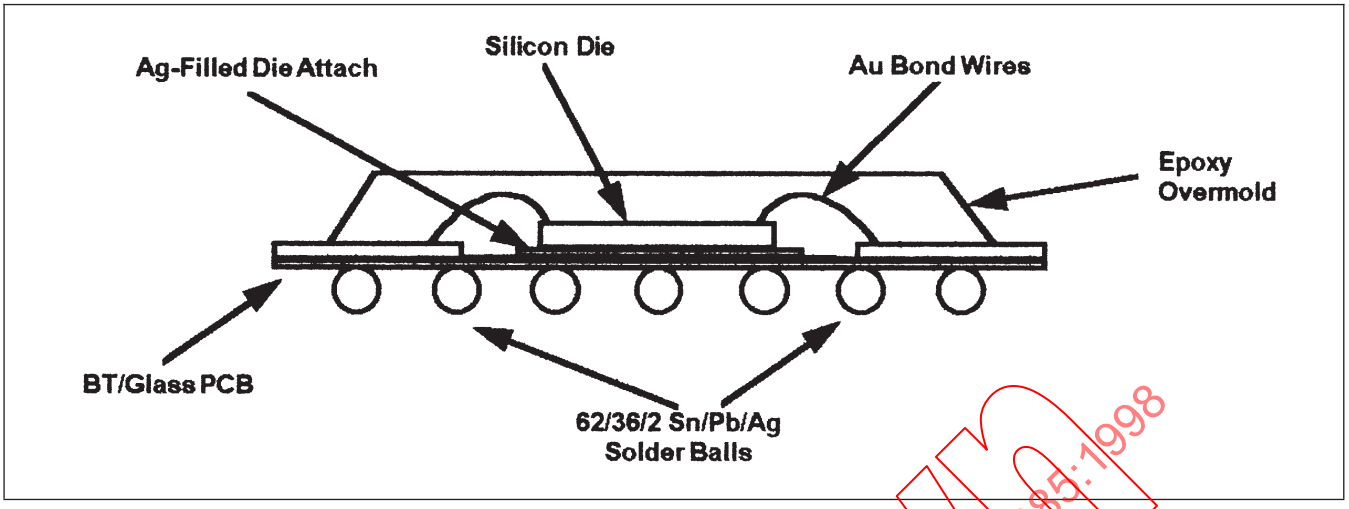


Figure 4–8 Plastic BGA Cross Section

and package/board coplanarity

- Unlike CBGA, non existent CTE mismatch problem between package and FR 4 PCB
- Unlike CBGA, depopulation of solder balls does not affect CTE mismatch related reliability

4.2.2 Thermally Enhanced BGA

Figure 4-9 shows a cross section view of the thermally enhanced BGA. The heat side added to the cavity down construction provides the thermal dissapation.[35]

4.2.3 Tab BGA

Tab BGA has the following characteristics:

- TBGA is a low cost, low profile IBM package
- Uses low dielectric substrate (polyimide) and 2 metal layer TAB type substrate (signal & ground)
- CTE mismatch issues non-existent since adhesive and flexible substrate take up strains. IBM reported no failures in 0-100 °C thermal cycling or 22,000 of power cycles (25-75 °C, 3W)
- Allows use of flip chip or TAB interconnection to lower die pitch than is possible in wire bond. This allows die shrinkage
- 0.63 mm [.025 in] dia balls (90 Pb/10Sn) welded to via lands at 1.25 mm pitch in 21 to 40 mm body size

Figure 4-10 shows a cross section of the TBGA. Some concerns are:

- Single wiring plane in substrate essentially limits TBGA to be a single chip package
- Requires gold bumped die

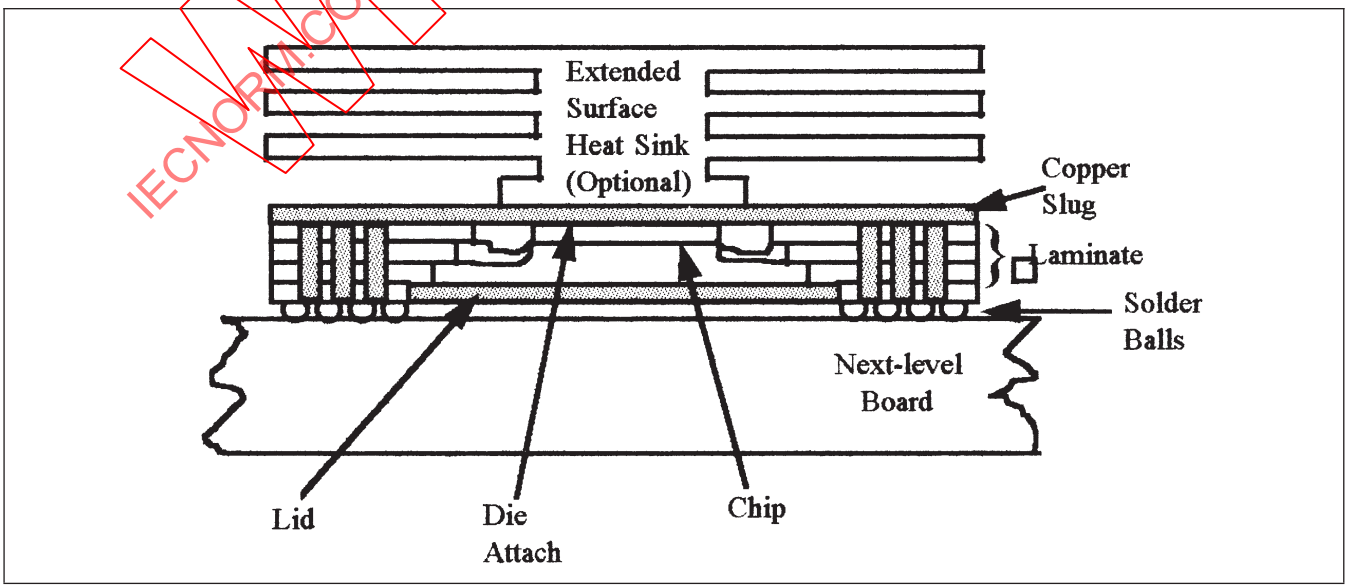


Figure 4–9 Thermally Enhanced BGA

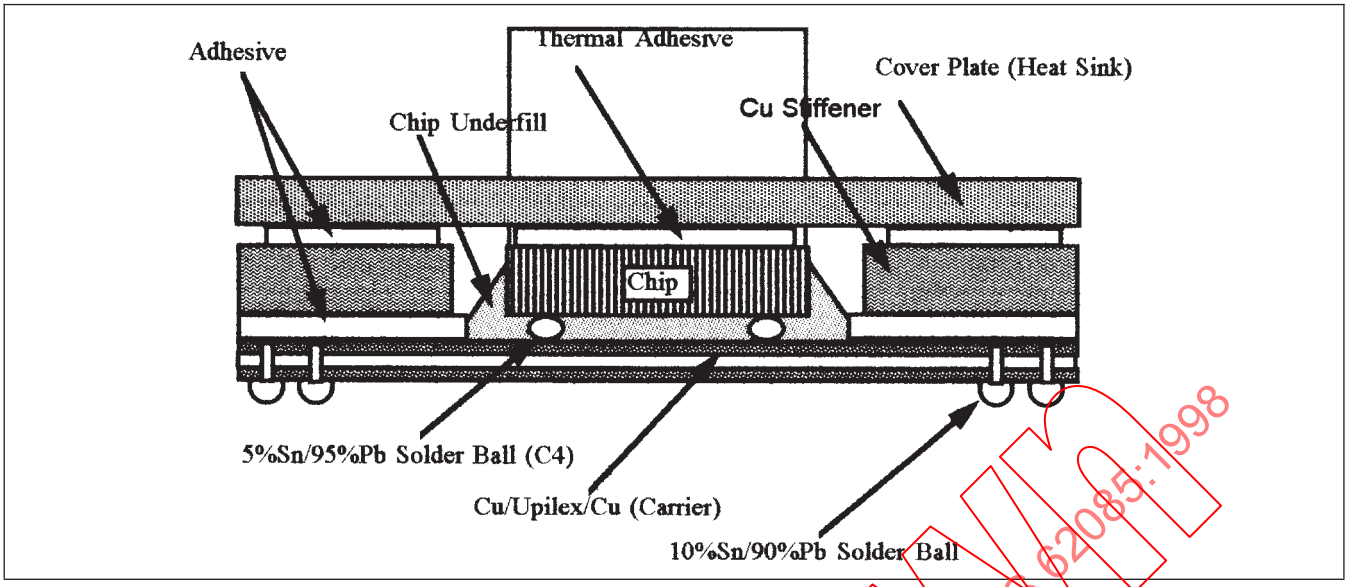


Figure 4–10 Cross-Section of a TBGA Package

- Moisture sensitive package since polyimide absorbs moisture

Typical electrical characteristics include:

- Total Capacitance (pF) 0.39 to 2.41
- Resistance (mOhm) 102-360
- Self Inductance (nH) 1.26-2.49
- Impedance (Ohm) 45-60

4.2.4 Mini BGA

The mini BGA was developed by Sandia Laboratories. Figure 4-11 shows the on-chip pad redistribution on the mini BGA.

4.2.5 Micro BGA

The micro BGA has the following characteristics:

- The micro BGA is an intermediate step between BGA and flip chip for complexity and density without the handling problems of bare die
- Slightly larger than die without the KGD problem since the die can be pretested
- Instead of fanning from chip to lead as in TAB, traces on flex circuit fan inward to the array of bumps underneath the die.

Figure 4-12 shows a cross section BGA

4.2.6 Ceramic Ball Grid Array (CBGA)

The ceramic BGA has the following characteristics:

- Flip chip or wire bonded die
- Cavity up (for cooling through board) or cavity down (air cooling)
- High temperature (90 Pb, 10 Sn) Solder balls 35 mils in diameter

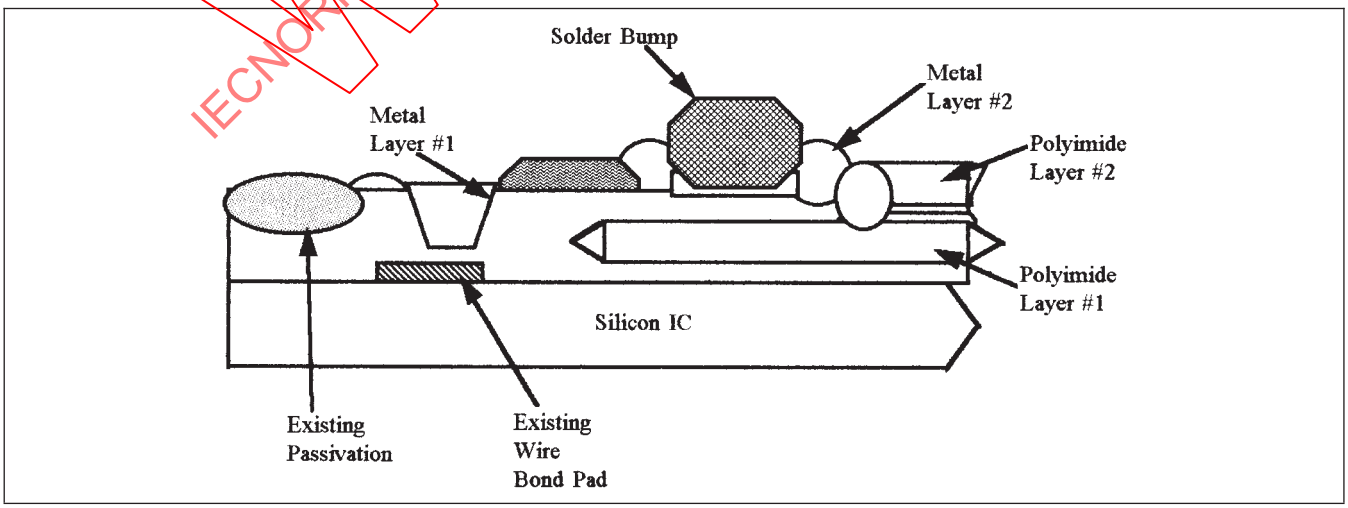


Figure 4–11 On-Chip Pad Redistribution (Sandia Mini BGA)

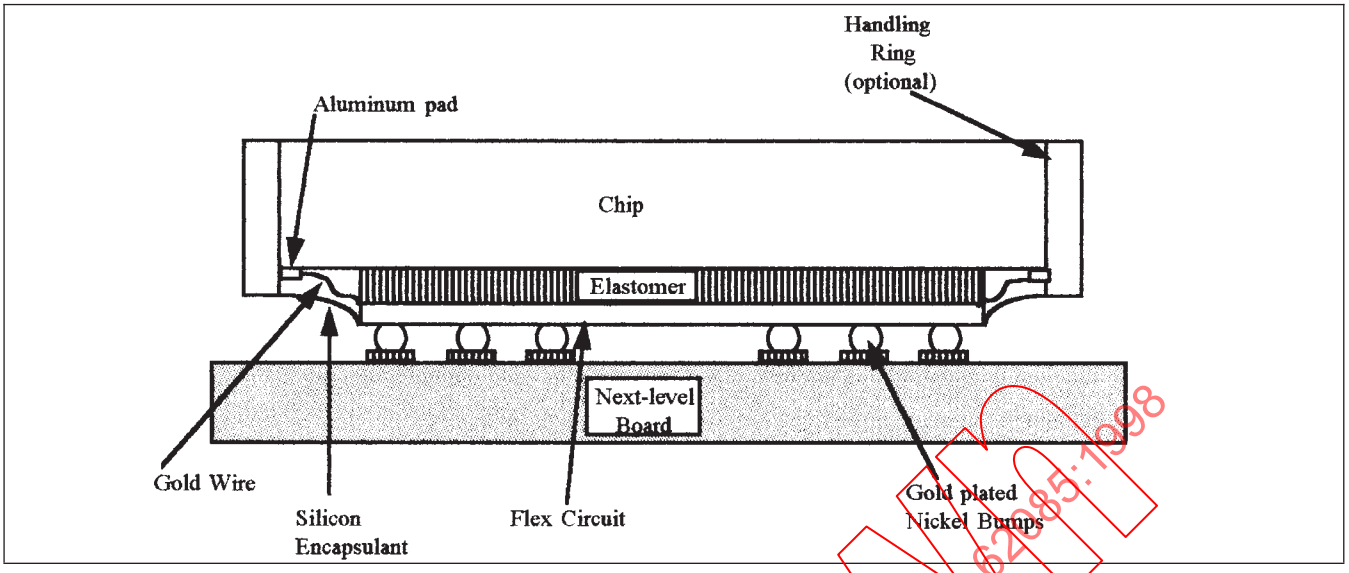


Figure 4–12 Micro BGA

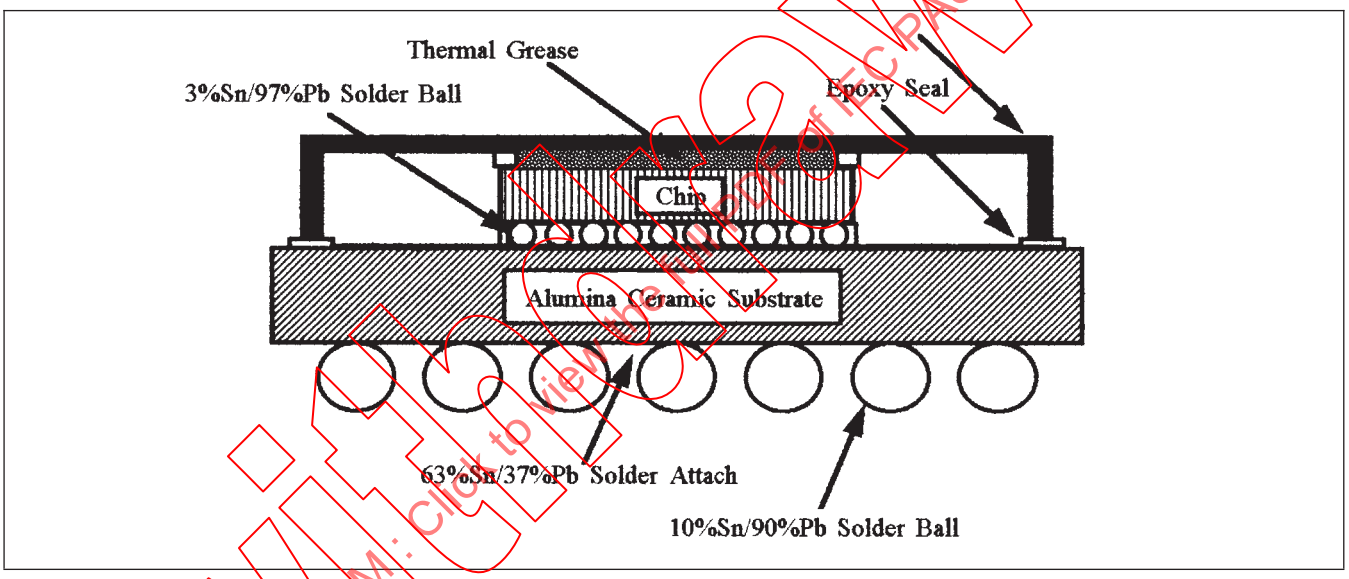


Figure 4–13 Cross-Section of CBGA

- Body size between 18 to 32 mm
- Fully populated (cavity up only) or custom depopulated
  - — Example: 603 power PC is in 21 mm body size at 1.27 mm pitch BGA package

Figure 4-13 shows a cross section of the CBGA

4.3 Material Decisions

The material checklist for BGA rests with the environment in which the part will be used. Characteristics include:

- Ceramic BGA (CBGA)
  aka SBC (solder ball connection (IBM)
- Ceramic Column Grid Array (CCGA)
  aka SCC (solder column connector)
- Plastic BGA (PBGA)
  aka OMPAC (over molded plastic pad array)
  SLICC (slightly larger than IC carrier)

Some of the issues for BGA are:

- Plastic package extremely moisture sensitive (PCB based substrate susceptible to delamination)
- No visual inspection (except outer row)
- Potentially difficult to rework
- Balls cannot be ‘‘dressed’’ for rework by most users (progress being made in this area)
- Lack of industry infrastructure especially in the areas of inspection and rework
- Process capability only a few OEMs and limited package suppliers
- Unresolved patent issues
- Concerns in large package planarity
- Popcorn related problems in PBGA (but not much different from PQFP bake and bag issue)

- Relatively unknown data and reliability limits
- New and expensive especially in low pin count
- Increases board layers count and hence cost

4.3.1 Thin Film Redistribution

- Redistribution of the peripheral bonding sizes must be resolved. This is sometimes accomplished by adding an insulating layer(s) and rewiring the lands to an array location.

4.3.2 Coplanarity

Coplanarity is a critical parameter in achieving sound solder joints. The maximum variation in coplanarity throughout a component's lead configuration is generally accepted to be 0.1 mm. A solder paste height for fine pitch components is usually about 0.15 mm. This provides very little margin of error for lead coplanarity with an average penetration of the lead into the solder paste of 65%. When leads are out of plane, unsoldered joints result because the solder paste cannot contact the high leads, or weakened joints may result from low solder joint cross-sectional area.

Coplanarity must be an acceptance criterion for component procurement, and incoming inspection of components may include AQL inspection for coplanarity characteristics or the supplier may be certified. Capability of placement machines to inspect for planarity is a highly desirable feature to accept/reject components on an individual part level.

A contributing factor to part coplanarity is the planarity of the circuit board pads. The finish on the circuit board is a key factor in achieving a flat mounting pad. Hot air solder level (HASL) surface has excellent solderability but the planarity of the pads varies with the thickness of the HASL coating. This variation may be as much as 0.075 mm, depending on board layout, pad design, and HASL process characteristics.

Solder or tin plated surfaces have planarity equivalent to the underlying copper surface, but plated solder is porous and tin coatings become difficult to solder with age. Copper antitarnish surfaces are now becoming available. This finish retains the planarity of the copper surface with good shelf life but may require some adjustment of the flux or solder paste to ensure solderability.

Solderability of components must be maintained by avoiding storage in corrosive atmospheres or excessive heat. Severe oxidation of the lead finish or formation of excessive intermetallics results in weak or incomplete solder joints. Humidity, in addition to causing plastic component body cracking, accelerates the degradation of the lead solderability.

In the case of leads with a solder finish over copper, exposure to temperatures of 125 °C adds approximately 0.5 µm copper-tin intermetallic per day. When the intermetallic thickness approaches the solder thickness, solderability is degraded. The high tin content on component leads being supplied by many manufacturers is more susceptible to this problem and often requires aggressive flux to achieve acceptable solder joints.

4.3.3 "Popcorning Effect" Failure

The plastic body BGA is a relatively open design that is far from hermetic and can readily take up water, etc. The "popcorn effect" is the term used to describe a catastrophic mechanical failure mode related to the abrupt vaporization of entrapped water in a nonhermetic package or component during a reflow soldering process. Design and materials choices exercised in developing the BGA packages should be subjected to repeated experiments where BGAs are preconditioned in water for hours prior to being removed and put through a standard reflow process (to well over 200°C). In addition, samples should be subjected to over 100 hours of 85/85 temperature and humidity under a bias voltage followed by 5 reflow cycles. If no failures occur, the results clearly demonstrate that BGA packages can be both stored and handled without having to provide special protection from either atmospheric or processing derived moisture.

Studies have been conducted on both shell and gel design BGAs which offer an effective approach to the design of packaging for extremely large chips where the problem of CTE mismatch is compounded by size. It appears that the choices of materials and design of an overmolded package also contribute to good long-term reliability, as measured in both corresponding reliability and thermal cycle tests and as will be experienced in service.

4.4 Area Array Selection Process

The decision process for the type of array to be used is based on many factors: performance of the package in its environment; relationship of the chip size to the BGA profile; the number of I/Os; and the routing of the interconnecting structure.

Table 4-1 shows an example from JEDEC 95, MO-151.

4.4.1 Device Outlines

The area array package outlines are documented and furnished in JEDEC publication 95. The overall outline specification for the array device allows a great deal of flexibility in lead pitch, contact matrix pattern and construction. The example shown in figure 4-14 illustrates two 225 I/O devices with a common package outline but with the variation of contact pitch and matrix.

Figure 4-14 illustrates comparisons between BGA devices having the same physical size and I/O count. One has a full contact array matrix, the other is furnished with a depopulated array with smaller contact-to-contact pitch.

Table 4–1
Array Population Example 1.50 mm Pitch
Ref. JEDEC Publication No. 95

D/E	e = 1.50								
	M1	N1	S1	VARIATION	M2	N2	S2	VARIATION	NOTE
7.00	4	16	0.750	CAA–1	3	9	0.000	CAA–2	
8.00	5	25	0.000	CBB–1	4	9	0.750	CBB–2	
9.00	6	36	0.750	CAB–1	5	25	0.000	CAB–2	
10.00	6	36	0.750	CBC–1	5	25	0.000	CBC–2	
11.00	7	49	0.000	CAC–1	6	36	0.750	CAC–2	
12.00	8	64	0.750	CBD–1	7	49	0.000	CBD–2	
13.00	8	64	0.750	CAD–1	7	49	0.000	CAD–2	
14.00	9	81	0.000	CBE–1	8	64	0.750	CBE–2	
15.00	10	100	0.750	CAE–1	9	81	0.000	CAE–2	
17.00	11	121	0.000	CAF–1	10	100	0.750	CAF–2	
19.00	12	144	0.750	CAG–1	11	121	0.000	CAG–2	
21.00	14	196	0.750	CAH–1	13	169	0.000	CAH–2	
23.00	15	225	0.000	CAJ–1	14	196	0.750	CAJ–2	
25.00	16	256	0.750	CAK–1	15	225	0.000	CAK–2	
27.00	18	324	0.750	CAL–1	17	289	0.000	CAL–2	
29.00	19	361	0.000	CAM–1	18	324	0.750	CAM–2	
31.00	20	400	0.750	CAN–1	19	361	0.000	CAN–2	
33.00	22	484	0.750	CAP–1	21	441	0.000	CAP–2	
35.00	23	529	0.000	CAR–1	22	484	0.750	CAR–2	
37.50	25	625	0.000	CAT–1	24	576	0.750	CAT–2	
40.00	26	676	0.750	CAU–1	25	625	0.000	CAU–2	
42.50	28	784	0.750	CAV–1	27	729	0.000	CAV–2	
45.00	30	900	0.750	CAW–1	29	841	0.000	CAW–2	
47.50	31	961	0.000	CAY–1	30	900	0.750	CAY–2	
50.00	33	1089	0.000	CBA–1	32	1024	0.750	CBA–2	
Notes:	4	5,13	12		4	5,13	12		
	1, 3, 15								
Ref.	11–489				11–489				
Issue	D				D				

Variations - 1.50 Pitch

4.4.2 Array Population

Contacts may be distributed in a uniform pattern with even or odd numbers of column and row array typical of that shown in figure 4-15. Depopulation of contact locations is permitted at the discretion of the device manufacturer.

Both even and odd column and row patterns are permitted in the JEDEC standards. Figure 4-16 compares the zone depopulated array pattern to the staggered array. Because contact position 1-A must be retained on all array packages, the staggered pattern must be developed using an odd number of contacts on both row and column.

4.5 Peripheral Lead Package Descriptions

Leaded I/Cs are either ceramic or plastic packages with terminations that extend beyond the package outlines. There, terminations typically space the body of the package from the interconnecting structure for reasons of cleaning, inspecting or accommodating differences in thermal expansion. The leads may be attached to the package body either before or after chip attachment.

In plastic leaded components, the primary packaging distinction concerns the point in which a chip is incorporated into the package. A premolded package is supplied as a leaded body with an open cavity for chip attachment. A post-molded body part typically has the chip attached to a lead frame with an insulating plastic body molded around the assembly. It is supplied by the manufacturer without apertures.

Leaded ceramic components may be similarly classified but with a difference in category. The distinction concerns the point at which leads, if desired, are attached to the ceramic body. A pre-leaded ceramic chip carrier is supplied with copper or Kovar leads brazed to metallization integral with the ceramic package. Typically, the package is supplied with an open cavity for chip attach. A metal or ceramic lid is epoxied, soldered, or attached with glass frit to provide a hermetic seal around the chip. After these steps, the leaded assembly is attached to the printed board.

A post-leaded ceramic chip carrier typically has leads soldered to metallization on the ceramic package after chip attachment. These leads may take the form of edge dips or solder columns. Incorporation of leads into the assembly typically occurs immediately prior to board attachment.

High lead-end coplanarity in surface-mounted lead chip carriers is an important factor in reliable solder attachment to the printed board. Coplanarity may be measured from the lowest three leads of a leaded package. Complanarity of 0.1 mm [0.004 in] maximum is recommended with 0.05 mm [0.002 in] preferred.

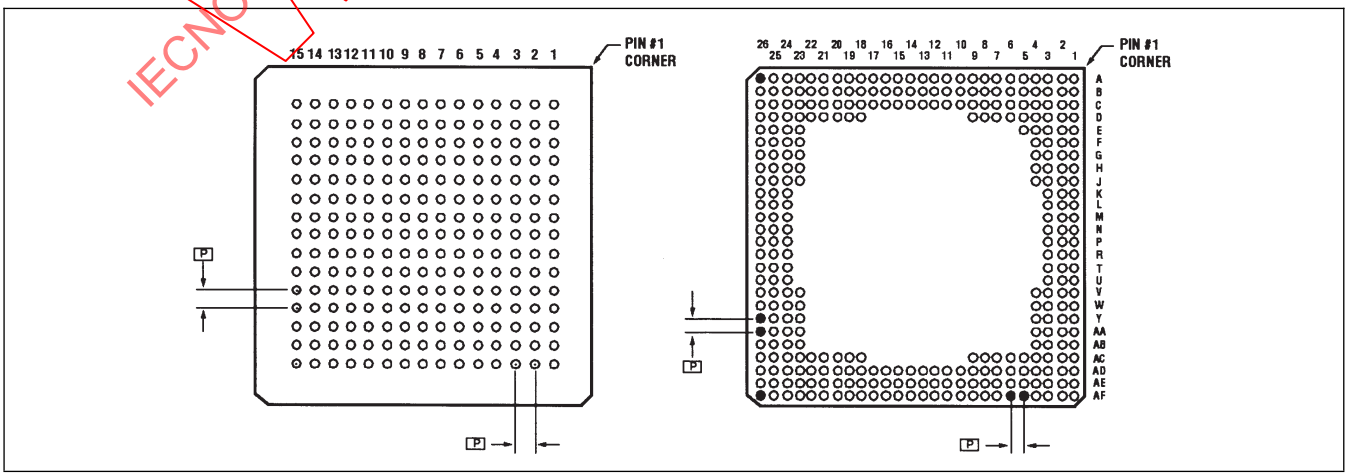


Figure 4–14 BGA Devices Having the Same Physical Size and I/O Count

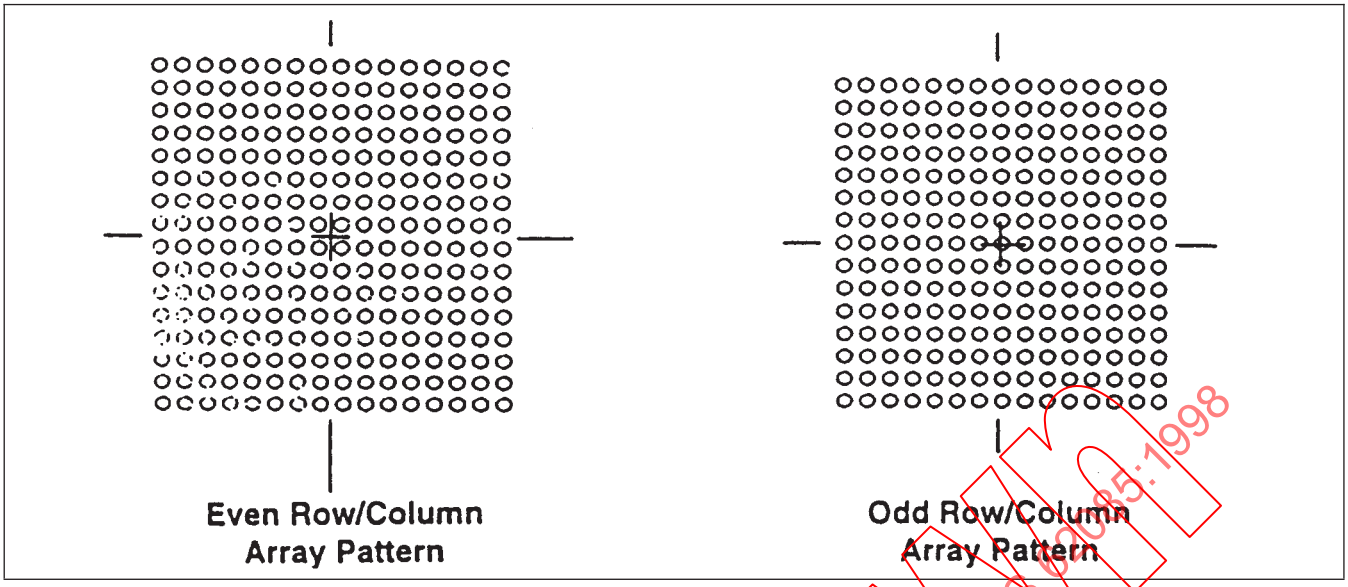


Figure 4–15 Both Even and Odd Column and Row Patterns Are Permitted in the JEDEC Standards

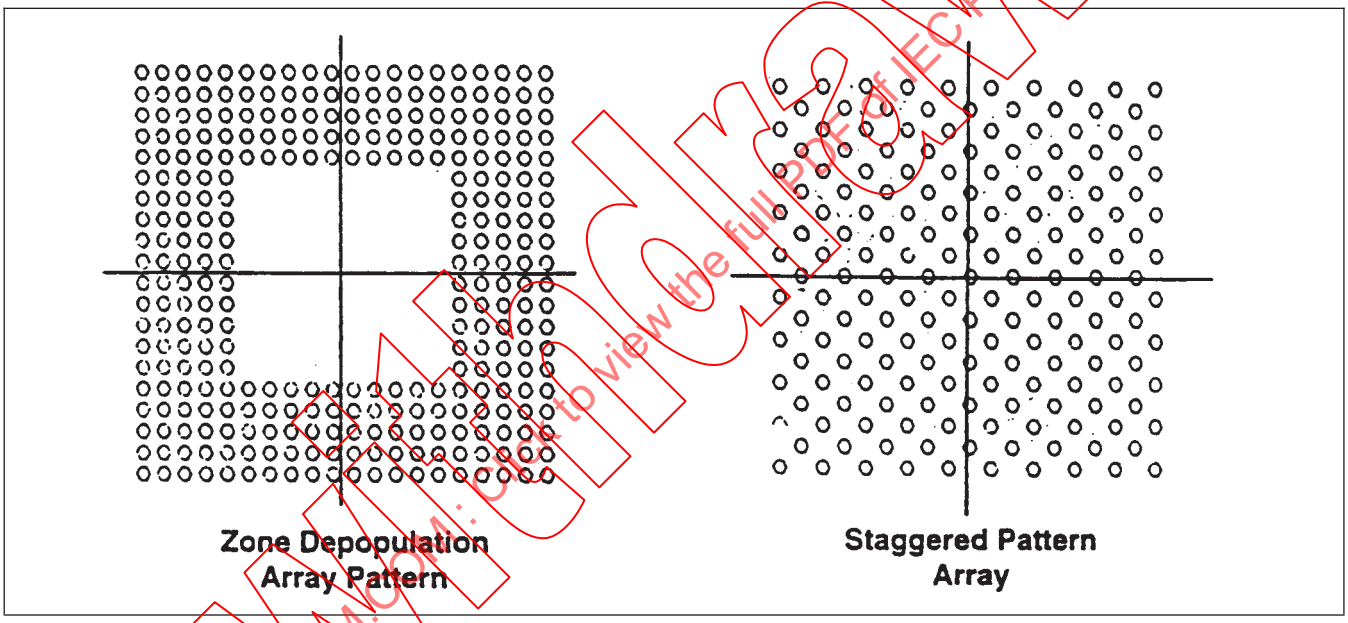


Figure 4–16 Depopulated and Staggered

4.5.1 Lead Pitch Parameters

The four-sided gull wing family is characterized by gull wing leads on four sides of a square or rectangular package. The family includes both molded plastic and ceramic case styles. The acronyms PQFP, Plastic Quad Flat Pack and CQFP, Ceramic Quad Flat Pack, are also used to describe the family.

There are several lead pitches within the family from 1.0 mm to 0.30 ram. High lead-count packages are available in this family that accommodate complex, high lead-count chips.

The PFQP and CQFP families of parts are generally marked with manufacturer's part numbers, manufacturer's name or symbol, and a pin #1 indicator. Some parts may have a pin #1 feature in the case shape instead of pin #1 marking. Additional markings may include date code/ manufacturing lot and/or manufacturing location.

Components may be provided in tubes but packaging tray carriers are preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity required for placement and soldering.

4.5.2 Standard SMT

Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0 °C or 70 °C) and nominal environmental protection. As with plastic DIPs, they have the

advantage of low cost as compared to ceramic packages. (See figure 4-17)

Premolded Plastic. The premolded plastic chip carrier was designed to be connected to the interconnecting substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

Postmolded Plastic. The postmolded plastic leaded chip carrier consists of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the premolded package which has an aperture for mounting microelectronic components, the postmolded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Electron Device Engineering Council defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of postmolded construction.

Postmolded packages that have J-lead configuration and are JEDEC standard MO-047, are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

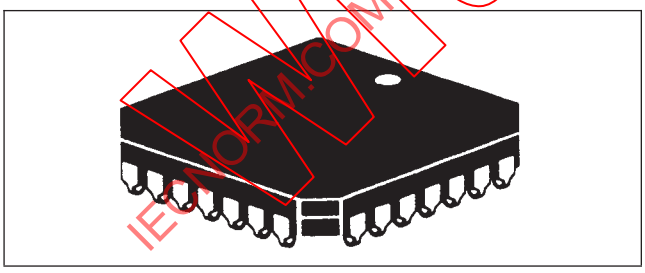


Figure 4–17 PLCC (Square)

4.5.3 Fine Pitch Packages

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

See figure 4-18. PQFPs have leads on a 0.635 mm pitch.

Leads should be solder-coated with a tin/lead alloy. The solder should contain from 58 to 90% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

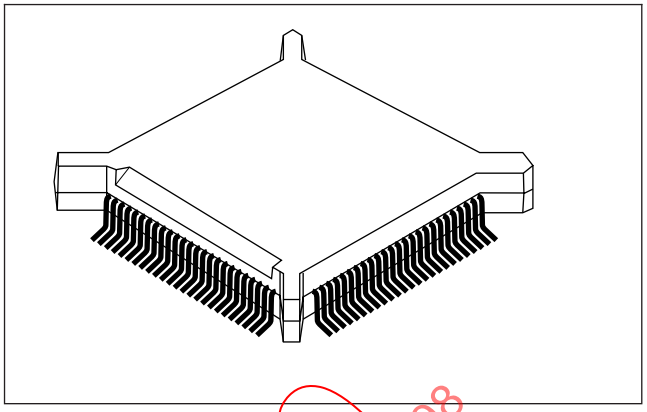


Figure 4–18 FQFP Construction

4.5.4 Ultra Fine Pitch Packages

The thin quad flat pack has been developed for applications requiring low height and high density. The TQFP, along with the TSOP components, are frequently used in memory card applications. The square TQFP family comes in 13 standard sizes, each of which sizes can come in either a 0.5, 0.4, or 0.3 mm pitch. There are therefore 39 configurations for square TQFPs. (See figure 4-19)

Two different pin counts are allowed for each package, both of which comply with the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1).

QFPs are also square and rectangular and come in larger pitches. Wherever applicable, the body sizes of the components and lead pitch usually dictates the relationships and pin numbers for SQFPs and QFPs that have the same body size.

Leads should be solder-coated with a tin/lead alloy. The solder should contain 58 to 90% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

4.6 Sockets

Sockets for PGA packages can be broadly classified in two categories, i.e., Zero-Insertion-Force (ZIF) and Low-Insertion-Force (LIF) sockets.

4.6.1 ZIF Sockets

Zero insertion force (ZIF) sockets usually depend on a lever- activated cam mechanism to engage and disengage the socket. The socket has two positions, i.e., actuated and open depending on the position of the level mechanism. Some sockets use a tool instead of a lever to actuate the socket. These sockets occupy minimum area and are

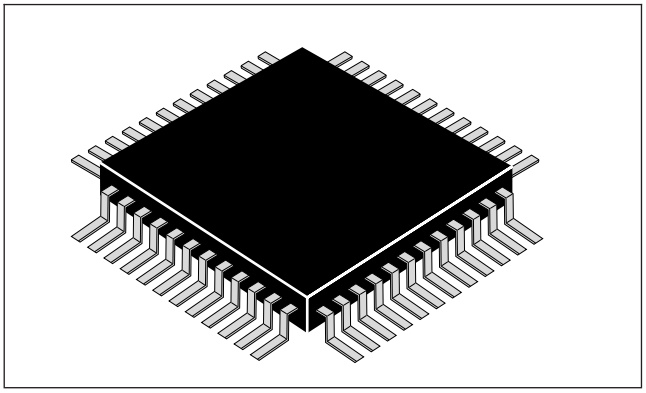


Figure 4–19 TQFP & QFP (Square)

known as tool actuated ZIF sockets or TAZ. The user inserts the Pin Grid Array package into the open socket using negligible force. The lever or the tool is used to either slide the package pins into the contacts or slide the contacts over the package pins. This operation requires a minimum of force. This socket type has been used in test/burn-in applications and for end user applications for upgrades. Traditionally the drawbacks associated with this type socket are the additional real estate required on the board (this is less of a problem with the TAZ socket), the greater socket cost and the occasional applications where the movement of the lever may be obstructed by the heat sink design.

4.6.2 LIF Sockets

The second category is the LIF sockets. There are two main variations in this socket type, i.e., the screw machined type and the stamped and formed type (sometimes referred to as the true LIF sockets). The difference between these two categories is that in the stamped and formed sockets, a single contact piece is embedded in a plastic housing as compared to the screw machined types, where the contact piece is a two-part assembly embedded in a plastic housing. The LIF sockets depend on a friction contact to provide adequate retention for the package in the socket. As the pin progresses to the socket it pushes open the contact. As a consequence, some force is required to completely insert the package in the socket.

Different manufacturers have different contact designs, the differences being the contact material, the surface finish and the number of tines that constitute the contact and the design of the socket. The total insertion force depends on a number of interacting factors such as the number of pins on the package, the alignment differences between the package and socket, the contact designs and the pin tip shape. The pin tip shape affects the insertion force in that different shapes encounter different forces during their progress into the contact. This effect of pin tip is most apparent when insertion force is measured for a stamped and formed socket with a two tine contact piece. The flat tipped pin, which sometimes also has a burr at its end, requires a significantly higher insertion force than the rounded pin tip shape or the conical pin tip shape. In the case of the more complex contact designs in the screw machined sockets, the effect of pin tip shape on insertion is not as apparent because it depends on other factors such as barrel diameter and the design and layout of the contact. The extraction forces required to remove the package from the socket are not a function of the pin tip shape, but depend on the contact design.

Earlier PGA packages had low pin counts and low power dissaproval. The reflow friction contact force was usually sufficient to hold the package in the socket during shock and vibration tests. As the pin counts increase and the power increases requiring larger heat sinks, the mass of the assembly held by the socket increases. This in turn makes it increasingly difficult to depend on friction contact alone to hold the package/sink assembly during shock and vibration. This may appear to require supplemental mechanical retention (e.g. clips) to hold the assembly in the socket.

5 INTERCONNECTING STRUCTURES

5.1 Interconnecting Structure Descriptions

At the heart of every electronic product are its active and passive components and their electronic interconnection structure. This ‘‘interconnection structure’’ is the conductor / insulator backbone that provides the basic infrastructural vehicle for interfacing and interconnecting the electronic systems component parts. Typically the complexity of a system is reflected in both its components and their interconnecting structures.

The interconnecting structure function has been perceived primarily as a simple electrical interconnect and was designed from a conductor routability (photo tooling) and schematic documentation perspective. However, as speed and frequency increase, the intrinsic electrical functional characteristics of the conductor-insulator structure become very significant.

Also, the interconnecting structure functional role to provide thermal, mechanical, chemical and optical requirements in addition to electrical functionality can no longer be trivialized.

Although great advancement in semiconductor technology has occurred in the past decade, it is of little consequence unless these sophisticated chips can work and talk to one another. To do this electronic communication economically and reliably requires a recognition of the importance of substrate design and the multifaceted interrelationships contained therein, and a viable industry infrastructure that can implement the design using state-of-the-art environmentally benign materials and processes.

Interconnecting structures can range from simple single-sided boards (one layer conductive pattern), to a double-sided (two layers of conductive patterns having each side interconnected by plated through-holes), to a multilayer (an intricate multiple three dimensional conductor - insulator network having thousands of plated through-holes along with blind and buried vias). Usually as performance demands increase, so does the density and complexity of the entire structure.

The steady advancement of electronic packaging technology continues to have a significant technological impact on the substrates used to interconnect today's electronic assemblies. This advance has created a technological need for finer circuit lines and spaces, smaller interconnection vias and plated thru-holes, lower dielectric constant materials, and more strenuous thermal management requirements as well as many other considerations.

The interconnection structures supporting today's advanced, first level electronic packages have become key limiting elements to the realization of the package's maximum performance potential. This section will review, in brief fashion, the choices that are available as packaging and interconnection structures from both materials and manufacturing technology perspectives.

Interconnection structures for electronic packages have evolved from the very simple to the extremely complex. Early circuits often employed metal chassis upon which the devices were mounted, insulated, and interconnected by point-to-point wiring. These simple techniques gave way to increasingly complex manufacturing schemes that were better suited to mass production. While the seeds for modern manufacturing technologies were planted in the early part of this century, they were not exploited until the late 1940s and early 1950s.

Continued advances in manufacturing technology have given rise to numerous alternative techniques for creating interconnection substrates, as will be shown. Many of the existing substrates are particularly well suited to meeting modern packaging's many technological demands. However, some are of greater value than others in differing applications.

The decision as to which of these technologies to use can be facilitated if the user has a better understanding of both the fundamentals that govern each of the technologies and of the individual strengths, weaknesses, and costs of each. The balance of this section is devoted to a discussion of the tradeoffs in the use of each technology through more detailed review.

There are a number of viable approaches to creating interconnection substrates. Each of these choices comes with its own set of advantages and disadvantages, and each substrate has its own set of constraints with respect to the assembly method that can be employed. Which interconnection structure-base material combination is the correct one is very much a matter of individual production requirements, and the final choice is normally arrived at by considering the trade-offs of conflicting needs. Following are brief descriptions of commonly used printed boards.

5.1.1 Rigid Printed Boards

Rigid printed boards (printed wiring and printed circuit) are the standard of the interconnection industry and as such are the most widely available interconnection method. These interconnection structures are available in an array of shapes, sizes and interconnection densities, from simple single-sided printed boards to complex multilayer structures such as MCM-L. Printed board technology is by far the most commonly chosen technology for interconnecting electronic devices. Printed wiring is also the oldest method used to create electronic interconnection structures, having been employed in that fashion since World War II.

Single-Sided Printed Boards

The first form of printed wiring board, the single-sided board, is still effective today for many applications. The advances in processing technology have made it possible to get extra use from single metal layer designs.

Double-Sided Printed Boards

Double-sided boards have two conductive metal layers normally interconnected by means of plated through holes; though eyelets and "Z" wires have also served in this capacity. As with single-sided boards, the fine line processing capabilities of today can in certain cases preempt the need for multilayer constructions.

Multilayer Printed Boards

Multilayer boards have three or more layers of circuitry. These are commonly used as the primary means of electronic interconnection in today's sophisticated computers. MLBs of more than 50 layers have been created to achieve the desired degree of interconnection.

Metal Core Printed Boards

Metal core printed boards have historically been used in cases where high power devices were employed and thermal management was of paramount importance. Such structures were commonly enameled or porcelain coated steel onto which the circuit pattern was applied. However, in the late 1970s and early 1980s with the advent of surface mount technology, the technique began to be used as a means of both extracting heat and managing the coefficient of thermal expansion of standard multilayer boards. Copper-clad invar and copper-clad molybdenum are two of the more commonly used core metals. They can also serve as functional ground and power layers, when designed properly, increasing their utility.

MCM-L Constructions

MCM-L circuits have much in common with standard printed boards. The major differences lie in the feature sizes (0.05 mm line and space) and the finish (wire bondable gold). MCM-L boards tend also to be small and use higher temperature laminates. They are arguably the most viable MCM alternative today because of the large potential vendor base.

The resins and reinforcements can be, and normally are, mixed and matched to create laminates that meet the specific needs of the circuit designer and user, an important advantage in the creation of today's complex circuits. Table 5-1 compares properties of some rigid substrates.

Table 5–1 Comparison of Selected Material Properties

Substrate Material	Coefficient of Thermal Expansion (X-Y) (PPM/°C)	Dielectric Constant	Glass Transition Temperature °C
Epoxy-Glass	17 - 18	4.2 - 5.0	120 - 130
High Temperature Epoxy-Glass	17 - 18	4.3 - 4.6	150 - 180
BT/Epoxy-Glass	15	4.0 - 4.2	185 - 195
Cyanate-Ester Glass	12 - 14	3.5 - 3.7	240 - 260
Epoxy-Aramid	6 - 9	3.7 - 3.9	120 - 130
Polyimide-Glass	14	4.0 - 5.0	240 - 250
Polyimide-Quartz	6 - 8	3.4 - 3.5	240 - 250

5.1.2 Flexible Printed Wiring Boards

A technological variant of the standard rigid printed board, flexible printed boards (also known as flex circuits) are interconnection structures that are created on flexible base materials. Like their rigid counterparts, they can range from simple single-metal layer devices to multilayer structures of great complexity.

Single-Sided Flex

Single-sided flex circuits are the simplest form of the technology. A single metal layer is employed and interconnected from one side. With a cover layer in place they are most commonly used for dynamic flex applications.

Double Access Flex

Double access flex circuits, like single flex, have only a single metal layer but the circuitry can be accessed from both sides due to special processing that provides opening through the base film.

Double-Sided Flex

Double-sided flex circuits allow greater density without greatly sacrificing either flexibility or adding greatly to substrate height. They can be used in certain dynamic applications if designed properly (e.g., single metal layer through the bend areas). Plated through holes are commonly used to provide connection from side to side.

Multilayer Flex

Multilayer flex circuits are most commonly found in more complex applications. Military applications are common. Special understanding of design is required to take greatest advantage of this useful technology. As with double-sided flex, multilayer flex designs can provide some dynamic capability, however, it is best reserved for intermittent flexing applications.

Rigid-Flex

Rigid flex boards are a hybridized form of printed board and offer the best of both worlds to the designer. Like multilayer flex, they are most often used in more complex constructions such as compact back panel bus systems.

The military and aerospace industries have been avid users of the technology for the enhanced reliability it can offer when compared to the complex wiring harnesses that rigid-flex commonly replaces.

5.1.2.1 Base Materials for Flexible Circuits

Base materials for flexible circuits have historically been quite varied. Among the unusual materials that have been pressed into service have been, epoxy composites, aramid fiber paper (DuPont's Nomex®) and fluoropolymers such as Teflon®. While these substrates for flexible circuit applications are available, polyester and polyimide are much more widely used.

5.1.2.2 Polyester Films

Polyester films are the most widely used for flexible circuit applications in terms of material volume, though not necessarily number of designs. They are pervasive in consumer products such as printers, membrane switches, calculators and dash panel displays. A typical polyester film consists of two joined layers, the base film, and a thin coating of uncured polyester adhesive. This material is in turn used to create the metal-clad laminate from which the flexible circuit is made.

Polyester is significantly lower in cost than polyimide. While having the needed electrical and mechanical performance characteristic for most applications, polyester is limited only by its inability to offer continuous service at temperatures much above 115 °C. While this may at first glance appear to eliminate polyester as a candidate for soldering applications, clever manufacturing processes have enabled certain OEM's to produce soldered polyester flexible circuits in mass quantities.

5.1.2.3 Polyimide Films

Polyimide films are normally viewed as the material of choice for high-end/ high performance flex circuit applications. Polyimide films are used in such diverse applications as disk drives, cameras, missile systems, video tape players and computer mice. Like polyester films, polyimide films for flex circuit applications normally consist of base film and adhesive, although adhesiveless forms are also available. Unlike polyester, many more adhesive choices are available, such as epoxy, acrylic, and polyimide. The most commonly used are acrylic-based thermosetting adhesives. Such adhesives allow polyimide flexible circuits to be soldered with relative ease.

Polyimide films offer excellent performance over a wide range of temperatures; from cryogenic to soldering temperatures. While the material tends to absorb more moisture than polyester, polyimide is at least equivalent in nearly every other performance category, from flexural endurance to tear strength. In addition, polyimide films offer a unique advantage, in that they can be chemically milled; an advantage well understood by manufacturers of TAB tape. This means that it is possible to create the equivalent of TAB bonding sites directly in the circuit. Admittedly, other methods can be used to create the same effect, most notably eximer CO_2 lasers, but such methods normally require a cleaning step to remove charred edges. Table 5-2 compares properties of common flexible substrates.

Table 5–2
Comparison of Selected Properties of Flexible Materials

Substrate Material	Coefficient of Thermal Expansion (PPM/°C)	Dielectric Constant	Tensile Strength (KPSI)
Polyester	27	3.1	20 - 35
Polyimide	20	3.5	25
Aramid Paper	22	2.0	11
FEP	80 - 105	1.9 - 2.2	4 - 7

5.1.2.4 Flexible Circuit Technology

Flexible circuit technology is one of the more interesting of the interconnecting substrates available for electronic assemblies, offering some unique capabilities not available from the other technologies. This is due to several factors. The substrate is flexible, normally quite thin, and almost always unreinforced. The combination of these elements provides the foundation for some rather unusual design capabilities, as will be pointed out shortly.

5.1.2.5 Flexible Circuit Capabilities

Flexible circuits are unique among interconnection methods. They can, at one time, offer weight and size reduction, elimination of wiring errors, and increased reliability, provide a three dimensional interconnection system, and reduce product cost. Related to common rigid printed wiring technology, flexible circuits can provide advantages other technologies are unable to offer. While flexible circuits share many of the same manufacturing processes as are used to produce rigid printed boards, and thus are subject to many of the same limits, they require an increased sensitivity on the part of the designer to mechanical concerns, such as bending, folding, flexural cycling, and strain relieving.

Machining, chemical processing and imaging of flexible circuits are substantially the same as for rigid boards; thus the process-imposed limitations for flexible circuits are nearly identical as those for rigid boards. In addition, new elements must be reckoned with; these being covercoating or coverlayer concerns and the intrinsically related matter of flexible circuit mechanics. The following brief introduction to these matters is offered to help facilitate entry to flexible circuit usage.

5.1.2.6 Coverlayer Limitations

Coverlayer or covercoat is the equivalent of a flexible solder mask. Like solder mask, the coverlayer serves to protect the circuit from the environment. However, with flexible circuits, it also serves to mechanically restrain circuit lands from lifting during soldering operations, and it allows the copper to be placed in the neutral axis of a bend. The latter item is of special importance in bending and flexing, as it protects the circuit from the premature failure that would occur in the coverlayer's absence.

Openings for interconnection in the coverlayer film can be produced by drilling, routing, cutting, punching, or lasing. The most common methods, especially in small quantity, are drilling and routing. These processes define certain feature design limits. For example, square corners are not a reasonable possibility for a round tool process. However, flexible circuit manufacturers often have a stock of creative solutions that can be applied to the problem if it is necessary.

Finally, eximer lasers, though somewhat costly to operate, can be used to photo-ablate the coverlayer from the surface of the lands. Such a process would yield a well-defined trough for solder paste and could facilitate assembly processes.

5.1.2.7 Bending and Flexing Limitations

While only a relatively small number of flexible circuits are designed for dynamic flexural applications, the vast majority (if not all) of flex circuits are bent, folded or flexed at some time during their life. This feature is usually taken advantage of during installation when the circuit is transitioned from a 2-dimensional circuit to a 3-dimensional interconnection system; thus understanding

of the design rules for bending and flexing is of considerable importance to the designer.

If the designer adheres to the practice of placing the copper circuit in the neutral axis (i.e. equivalent thickness of film are placed on both sides of the copper) then the following guidelines will serve. For single metal layer flexible circuits, the minimum bend radius should be 3 to 6 times the thickness of the circuit. For example, a typical single metal layer flexible circuit is approximately 0.15 mm thick, thus the minimum bend radius would be roughly 0.4-0.8 mm. With double-sided circuits and their added thickness, the factor is raised to 6-10 times the circuit thickness, and for multilayer, 10 or more times the thickness.

Obviously, as the package becomes thicker the stiffness of the circuit increases. Accordingly, the designer should attempt to keep layer counts down if bending is required. This is especially true for dynamic flexing, where minimizing both copper thickness and overall material thickness are key to creating a viable product. Dynamic flexural life is also very much influenced by bend radius. Best practice allows that the largest possible radius be provided but that it not be less than 40 or so times the circuit thickness.

Mainframe and supercomputer manufacturers thus pressed for a packaging technology that would incorporate:

- Low dielectric constant (<4.0) insulating materials
- Low resistivity conductors
- Tight tolerance line widths, spaces and dielectric thickness to achieve controlled characteristic impedances (Z°)
- Fine line width and pitch to obtain high interconnection wiring density such as are offered by TAB
- Multilayer structures to further increase wiring density and to create transmission line structures for high data speed

5.1.3 Encapsulated Discrete Wire Interconnection Boards

Discrete wiring boards are rigid, plane circuit boards with an embedded network of insulated wires as circuit conductors with plated-through hole and/or blind and/or buried via hole terminations or connections.

5.1.3.1 Wire Materials

The wire used is an insulated wire which meets or exceeds all of the requirements of J-W-1177/15, and has its size specified on the master drawing. The core conductor is composed of either copper conforming to the material requirements of QQ-W-343, copper-cadmium alloy conforming to the material requirements of MIL-W-82598, or as specified on the master drawing. The insulation is composed of cured, aromatic polyimide which exhibits a thermal rating of Class 220 when evaluated in accordance with ASTM D-2307.

5.1.3.2 Bonding Material

The bonding interlayer material for boards is also specified on the master drawing and is in accordance with IPC-L-109. Other bonding materials may be utilized providing they conform to the performance requirements of IPC-L-109. Sufficient bonding material must be used to provide for a minimum dielectric layer thickness specified between adjacent etched conductor layers.

5.1.3.3 Composite Metallic Material

When specified on the master drawing, composite metallic material is in accordance with IPC-CF-152. The type designation must be specified on the master drawing.

5.1.3.4 Adhesives

The adhesive used for bonding thermal planes are the same of a type as specified in 5.1.3.2. These materials provide for a minimum dielectric layer thickness as specified on the master drawing.

5.1.3.5 Copper Plating

Electrolytic copper plating deposit must meet the following requirements:

Purity—99.8% Cu minimum (for copper sulfate type plating solutions), or

99.5% Cu minimum (for pyrophosphate type plating solutions).

Elongation—6% minimum.

Tensile Strength—248184 KPa [36000 lb/in^2] minimum.

When tested the full build electroless copper deposit must meet the following requirements:

Purity—99.8% Cu minimum.

Elongation—6.0% minimum.

Tensile Strength—248184 KPa [36000 lb/in^2] minimum.

5.1.4 Nonorganic (Ceramic) Structures

The material most suitable for the particular application should be determined by examining the following properties of substrate materials:

Thermal Conductivity. The ability of a material to conduct heat away from critical circuit components. Normally measured as cal-cm/s-cm^2 °C. High thermal conductivity is desired.

Electrical Insulation. The ability of the material to insulate various circuit components from one another. Normally measured in ohm/cm. High resistivity is desired.

Mechanical Strength. The ability to withstand mechanical

shock. Young's modulus, flexular strength, tensile strength, and compressive strength are considered measures of mechanical strength. High strength is desired.

Refractory Property. The ability of a material to withstand high temperatures. Melting point is an indicator of this property. This property is usually desirable and absolutely mandatory for processes requiring heat treatment.

Chemical Susceptibility. The ability to withstand exposure to chemicals. It is very desirable for substrates to be inert to processing chemicals.

Weight. Weight may or may not be a consideration based on the application.

Metallizability. The ability of the material to be successfully metalized with thick-film, thin-film, or other metallization technique.

Cost. There are wide variations in the cost of substrate materials.

Table 5-3 provides information on some of the physical characteristics of non-organic substrates.

5.1.4.1 Alumina Substrates

Alumina substrates are made of polycrystalline $AL_2 0_3$ with small amounts of metal oxide glasses to achieve certain physical properties. Alumina is the most popular substrate material because it is readily available in sizes ranging from tiny chips to large area substrates, in thicknesses ranging from 0.25 to 1.25 mm or greater, and in a variety of shapes and designs. It is refractory, and the finished substrate can be drilled or cut with diamond tools or lasers.

5.1.4.2 Beryllia Substrates

Beryllia (polycrystalline BeO), with impurities for physical properties, is primarily used in applications requiring rapid heat removal from the circuit. Like alumina, beryllia substrates are available in a large variety of sizes, thicknesses, shapes and designs. Beryllia is less widely used than alumina due to its toxic nature in the powder form and its higher cost.

5.1.4.3 Coated Metal-core

Relatively new as a substrate, coated metal-core substrates, depending on the materials used, provide strength, shock resistance, a built-in ground plane, and relatively low cost for larger sized substrates. Prior to coating, the metal can be inexpensively shaped and punched to allow it to be used as a mounting bracket.

As a combination hybrid and discrete component mountingsurface, coated metal-core substrates can withstand such harsh environments as automobile engine compartments. Processing of coated metal-core substrates requires a low temperature firing, and pastes compatible with that condition.

Table 5-3 Physical Characteristics of Nonorganic Substrates

Material	Mechanical Integrity	Mechanical Stability and Flexible Strength	Thermal Conductivity (Cal-cm/S•cm^2-°C)	Thermal Expansion Coefficient (X 10^{-6}/°C)	Environmental Compatibility	Dielectric Constant
Alumina	Hermetic	Brittle 45-50K PSI	0.08-0.09	7.5-8.0	No Limit	K = 9-10
Beryllia	Hermetic	Brittle 33K PSI	0.59	8.5	No Limit*	K = 6.5
Coated metal-core	Hermetic	Shock Resistant	0.005	5.5 to 6.5**	No Limit	K = 5.4
Cofired multilayer ceramic	Hermetic	Brittle 55K PSI	0.035	6.0-7.4	No Limit	>10^{14} ohm-cm K = 7-9
Glass	Hermetic	Brittle	0.0018-0.0028	3.2-9.0	No Limit	K = 4.0-7.2
Quartz	Hermetic	Brittle	0.0045	8.0	No Limit	K = 3.8
Oxidized silicone	Hermetic	Brittle	—	—	No Limit	—
Sapphire	Hermetic	Brittle	0.0095	5.0	No Limit	K = 11-13
Ferrite	Hermetic	Brittle	—	—	Dry atmosphere	—
Organic film polyimides	Non-Hermetic	Flexible	0.00037	20	No High Temperatures	K = 3.5

*Material is very toxic.
**For coating only.

5.1.4.4 Glass Substrates

Glass substrates have limited applications due to their relatively low reliability and low processing temperatures. Their chief application is in display devices, specifically gas-discharge types. They are typically used in applications where cost is an important factor.

Glasses are mechanically sound, but brittle, and are subject to breakage if exposed to high impact forces. Glasses are usually not good thermal conductors and are not used where high heat dissipation is required. Glasses have very good surface finishes, very low warpages and cambers.

5.1.4.5 Quartz Substrates

Quartz is available in two forms: (1) fused quartz or silica, and (2) single-crystal quartz.

Fused Quartz. Fused quartz is similar to glass and is used in microwave applications because of its consistent dielectric constant and low rms surface finish. As with glass, it is a poor thermal conductor and cannot be used in high heat dissipation applications. It is very fragile, and extreme care must be exercised when it is handled. Its cost is moderate and the material is readily available from many sources.

Single-crystal Quartz. Single-crystal quartz is used in applications where an ordered crystal structure is necessary, e.g., in acoustic wave devices. The tensile strength of quartz varies according to the axis in which the crystal has been cut. The material is brittle and must be handled carefully. Its cost is generally considered to be exorbitant and, as with most crystals, its thermal conductivity is poor. However, single-crystal quartz does offer a very low rms surface finish and it exhibits little or no camber.

5.1.4.6 Oxidized-silicon Substrates

The use of oxidized-silicon wafer substrates overcomes some of the poor characteristics of glass. Such wafers have good surface quality, show excellent heat transfer characteristics, and can be scribed easily with a diamond tip.

Problems associated with ion migration, chemical attack and low mechanical strength are present in this material. Problems with capacitance, associated with the underlying silicon layer, can have a detrimental effect on circuit operating speed.

The primary use of this material is for thin-film precision resistor chips and networks.

5.1.4.7 Sapphire Substrates

Sapphire is used in microwave applications as a replacement for alumina substrates when a superior surface finish and low camber are required. Sapphire is an expensive single-crystal material ($\Delta L_2 0_3$) and is limited in size to the diameter of the boule from which it is cut.

The material is relatively strong but is a poor conductor of heat. The dielectric constant, as well as other mechanical and physical properties, will vary depending upon the crystal orientation. Therefore, care must be exercised to specify the proper crystal orientation.

5.1.4.8 Ferrite Substrates

Ferrites are typically used in microwave applications where a magnetic material is required. Circulators are one example of this application.

The material maintains a uniformity of substrate properties, e.g., dielectric constant and dissipation factor. Ferrites can be obtained with good surface finish qualities and low camber. However, they are brittle and highly susceptible to impact shock breakage.

5.2 Material Selection

Printed wiring is fundamentally a copper circuit pattern created on an insulating base. The insulating base (referred to as the base laminate) normally consists of an organic resin and a reinforcement of some type, most often with a copper foil surface. Many material choices in terms of both resin system and reinforcement method are available for the construction of base laminates.

The choice of resin system and reinforcement can have a significant impact on the performance of the finished product; thus understanding the relative merits of each is of some importance.

5.2.1 Reinforcement Material Properties

Reinforcement materials are the ‘‘backbone’’ of a laminate structure. They provide the strength and dimensional stability required to make the laminate a viable interconnection structure. They also contribute to the electrical properties of the laminate and can influence manufacturability if not selected with care. The following are some of the more common reinforcement materials used in making printed wiring laminates.

5.2.1.1 Fiberglass Cloth

Fiberglass cloth is the most common reinforcement material in use today. E-glass or electrical glass is the most frequently employed for this purpose, due to its very low content of soluble ionic components. E-glass is available in a variety of weave styles and thicknesses in order to meet the varied requirements of multilayer printed wiring products. In addition to E-glass, another type, S-glass or high strength glass, is also available. S-glass is lower in dielectric constant (values of 3.5 - 5.2 have been reported for S-glass versus values of 5.8 - 6.3 for E-glass) and may prove useful in certain high speed applications.

5.2.1.2 Quartz Cloth

Quartz cloth has been used as a reinforcement material in certain high performance applications, especially when tightly controlled dimensional tolerances and a low coefficient of thermal expansion is sought. Quartz cloth material is, however, very expensive and extremely difficult to drill, normally requiring diamond drill bits to process.

5.2.1.3 Aramid Fiber

Aramid fibers such as DuPont Kevlar® have been used either in woven cloth or chopped filler form when low thermal expansion rates in the X and Y axes are sought. The low dielectric constant of the material and light weight when compared to glass cloths makes it an attractive alternative for those applications where such a mix of properties is advantageous. A disadvantage of aramid fiber reinforced laminates is that they have a fairly high rate of thermal expansion in the Z direction below glass transition (~90 ppm/°C vs. ~60 ppm/°C for FR-4); consequently, plated through-hole reliability could be at risk if care is not exercised in design, manufacture and assembly. In addition, drilling and routing of the laminate can be difficult and thus costly due to the toughness of the aramid fibers, which leave small fibers on cut surfaces.

5.2.1.4 Fluoropolymer Fiber Cloths

Fluoropolymer fiber cloths are also available as a reinforcement for laminates. The fibers in such constructions are actually hollow, and laminates made from them can offer much lower dielectric constants that might normally be available. For instance, an epoxy resin based laminate made with this material would have a dielectric constant of 3.0 versus 3.5 -3.8 for conventional glass-based epoxy laminates.

5.2.2 Resin Types

The choice of resin system is of great importance to the performance of the board in terms of both electrical and mechanical requirements. Following are some of the more common resins and their applications.

5.2.2.1 Epoxy

Flame retardant epoxy (FR-4) has been the workhorse of printed board resins for many years. A thermoset resin (requiring heat to cure and harden), flame retardant epoxy has an excellent blend of properties that make it well suited to most electronic applications.

5.2.2.2 High Performance Epoxies

These resins were developed to fill a niche between more expensive high performance resins and the lower cost regular epoxies. These resins are often employed when higher temperature performance is required but cost is important as well. The operational temperatures of these resins are intermediate between epoxy and polyimide, yet their cost does not usually justify the added expense associated with the increased temperature capability of polyimide. The electrical properties of these resins are nearly identical to those of normal epoxy.

5.2.2.3 BT-Epoxy Blends

BT or bismalimide triazine/epoxy is another high temperature resin system with the added advantages of a relatively low coefficient of thermal expansion (approximately 70% of that for epoxy) and a lower dielectric constant when compared to normal epoxies (3.5 vs 3.0).

5.2.2.4 Polyimide

Polyimide resin offers the highest temperature resistance (Tg 260 °C) of all normally available resins for printed circuit manufacture. It is also the most favored for military applications where there is an anticipation that a product must go through several repair cycles, with the attendant thermal stresses, over the life of the product.

While the resin tends to be more costly and more demanding to process than other resins, it is well suited for thermosonic outer-lead bonding of TAB devices. The only major detraction of polyimide is that it has a greater tendency to absorb water than some of the other resins, causing changes in electrical properties, but its advantages tend to mute this deficiency.

5.2.2.5 Exotic Blends

Exotic blends are those materials that serve very specific application and thus see much lower usage. These materials tend to be more expensive though there are many exceptions. In some cases, materials are considered exotic only because of their more limited availability.

5.2.2.6 Cyanate ester

Cyanate esters, though somewhat costly, appear well suited to serve in applications where good electrical properties and good thermal performance are sought simultaneously. This is evidenced by the resin's low coefficient of thermal expansion (which is roughly equivalent to that of polyimide) and its low dielectric constant (2.9 vs. 3.0 for epoxy and 3.7 for polyimide). Cyanate ester resins also tend to be tougher, to offer better adhesion, and to be easier to process than some of the alternatives.

5.2.2.7 Fluoropolymers

Fluoropolymers, such as DuPont's Teflon®, offer the lowest dielectric constant values (2.0) of all normally available resin systems for printed wiring laminates. The material is also, however, quite soft, has a low Tg and also has a fairly large coefficient of thermal expansion, requiring extra effort in circuit design to accommodate its weaknesses.

5.2.3 Permanent Polymers (Solder Resist)

Permanent polymers are materials that become part of the printed board. They are usually used as a resist to protect the board from the action of a manufacturing or assembly process. They may also be used as a deterent of damaging the circuitry during the life of the equipment.

While technically not a substrate material, solder resist can play a substantial role in defining the properties of the finished product. Solder resist, or solder mask as it is also commonly known, is applied to the printed board both to protect the conductors from being soldered as the name implies and also to physically protect the surface from environmental damage after the assembly process has taken place. The material is available in both liquid and dry film forms. Printed board manufacturers differ in manufacturing approach and thus the type of solder resist used can vary between suppliers. Liquid, screen printed types are the ones most commonly specified and used. However, when the feature size requirements become more demanding, such as for BGA or fine pitch surface mount packaging, the use of photoimageable-type solder masks is often mandated.

5.2.4 Metallic Foils and Films

Copper is the most common metallic coating for printed board laminates. It is available in both foil and film forms. Among foils there are eight different recognized types of copper. These are broadly classed as either wrought (rolled) and annealed, or electrodeposited types. Special treatments are often applied to enhance the properties of the foil for such applications, as where high temperature ductility is required.

In addition to the foil types of copper, there are film-type copper coatings. These are typically deposited by vacuum processes such as sputtering and are normally very thin (i.e. less than 1 µm). These films can be plated up to the desired thickness with copper. This method also allows for the production of very fine line circuits.

5.3 Manufacturing Options

The construction of the printed board will more than likely be determined by the electrical impedance control required for the application, if any, and the need for module interconnections. With the increase in high lead count components and complicated support chips, six-and eight-layer structures with higher layer thickness tolerance can be expected. Thin and light wiring boards for portable computers and telecommunications are linked to thin cloth applications.

Six-layer structures on the order of 0.65 mm are in the market today in card form, and also provide a platform for emerging MCM-L technology. Conductor thicknesses and spacing control become more of an issue with thin cores because of the tight tolerances in the construction. Tradeoffs with manufacturing must be realized, in that thin cores with thin copper are difficult to handle and may affect yields.

Printed boards are available in an array of complexities from simple single-metal-layer circuits to high-layer-count multilayer interconnection structures. The processing of these products entails the use of many different manufacturing technologies, including numerically controlled drilling and routing, laser imaging, electroless and electrolytic plating, laminating, screen printing and photo imaging. The manufacture of printed boards can be extremely involved, and yields are sensitive to process complexity.

Printed boards are probably the most common interconnecting structure used for electronic assemblies, and can be expected to remain so for some time to come. Thus, it should prove useful to know some of the limitations of printed wiring technology.

Printed boards are created through the use of a diverse set of processes, mechanical, chemical, and photographic. Each of the processes has its own inherent limitations. In order to effectively design a printed board, some understanding of the limitations of those manufacturing processes used to produce printed wiring boards is most helpful. The following are some items of general concern that should be of interest to the designer of printed wiring boards.

5.3.1 Physical Parameters

Machined features consist primarily of holes, slots, and physical profiling of the board. In general, all machined features should be as large as possible, without violating the design's function. Holes, for instance, should not create an aspect ratio greater than 3 - 3.5 : 1 (thickness of board to hole diameter) for greatest ease of manufacture and best overall reliability. In special situations, holes with aspect ratios greater than 3.5 : 1 have been created but this will greatly increase cost. Also of note is the fact that plated through-holes with aspect ratios greater than 3.5: 1 have been shown to be more susceptible to damage during thermal cycling.

In addition to minimizing the aspect ratio, mechanically drilled holes should, if possible, be kept greater than 0.35 mm with 0.25 mm being considered a preferred minimum. Smaller drills are more delicate and less amenable to providing the economies that can be enjoyed by stack drilling. Additionally, very small drill bits are more expensive than larger diameter bits. However, with laser drilling, microvias of <0.125 mm [0.005 in] diameter are common but there are a limited number of suppliers with such capability.

Warp is an important concern for those attempting to mount today's most advanced electronic components onto

printed wiring substrates. Warp is measured by holding down three corners of the printed wiring board on a flat granite or other suitable surface and measuring the distance the fourth corner rises off the surface. The level of tolerance is an important consideration because of assembly conditions and for the reliability of the finished product, as residual strain from warp can fatigue the miniature solder joints created on today's micro devices.

5.3.2 Image Transfer

From the perspective of the designer and user, photoimaging is perhaps the most important manufacturing process in printed wiring production. It is the photoimaging process that normally holds the key to success or failure of the fine featured interconnect structures that today's high lead count components normally demand. Creating the images required for fine-line circuits is a highly demanding task and mandates scrupulous attention to detail and extreme cleanliness. The most successful printed board manufacturers have clean rooms for their imaging processes.

Recent advances in processing technology have led to breakthroughs. New electrophoretic photoresists are capable of producing very fine resolution of circuit features. Though these processes are known to be capable of producing features of less than 25 µm, current practical limitations on feature size are approximately 75 µm line and 75 µm space, (though some OEM's have demonstrated the ability to produce circuits with lines and spaces of 50 µm in limited production). This will be an important concern for some time to come as next generation designs will certainly demand ever finer features.

5.3.3 Feature characteristics (Size, Shape, Tolerances)

Features of high lead count components, whether area array or perimeter lead, need to be designed to optimize assembly yield. The placement tolerance for fine pitch can vary. Landing pads should be made as large as practicable to allow for tolerance at placement but at the same time discourage solder bridging at reflow.

5.4 Conductor Routing Methodologies

High lead count components create challenges in the design of printed wiring boards in two principal areas: component escape and component pitch. Component escape can be defined as the task of finding accessible connections to the printed board plated-through hole (PTH) grid. Component pitch helps to determine how close together high lead count components can be placed. Both area array and perimeter packages create design challenges for escape and pitch. The principal problem is one of a competition of printed board features in limited space.

5.4.1 Wiring Via Densities

The fundamental question to ask when trying to rout finer pitch components is whether or not there is a dense enough via grid to accept the required I/O and reference (or power). The need to increase via density below 2.5 mm to interstitial grids and move into the future to a 1.25 mm grid and less is a direct result of high lead count components.

The conventional plated through hole (used to escape straight 2.54 mm through hole components) is too large in diameter and has too large a land to allow enough wiring paths to escape many of the new fine pitch perimeter components, and many of the new ball grid array (BGA) packages.

Wiring vias on the order of .3-.5 mm diameter permits interstitial and straight 1.25 mm grid via density, and therefore increase the number of sites for component escape. Practical limitations in the current state of the art are important considerations, as drill expense, plating difficulties, and drill breakage escalate quickly with decreases in drill diameter. However, smaller vias will allow smaller lands, giving more room for circuit lines and spaces, thus increasing circuit routing paths.

Via density has a direct effect on component pitch in that the tighter the via density, the higher the escape rate per unit area of a printed wiring board. High via density will facilitate miniaturization in both supporting higher function components with more I/O, and also in compacting the I/O efficiently to the limits of the assembly technology used on high lead components. (See section 6)

Blind vias are a useful tool, especially in pad master designs and memory applications, where a pattern to link together memory modules can be achieved easily using blind vias. Benefits are the ability to free up wiring channels opposite the blind via, where normally there would be a hole and land.

In addition, back-to-back blind vias allow more flexibility for surface wiring than a single through via in that each blind via can have a distinct circuit associated with it. The blind via is not particularly useful in cases where a large number of signals must be escaped in many layers, such as with BGA packages. The through via is a good choice in these cases. (See figure 5-1)

Buried vias have very little impact on the escape problem. They may increase wiring opportunities module to module by allowing 90° turns within the laminate, and in that way may allow tighter component spacings than with conventional through or blind vias. For through vias to be effective, they must be small enough to allow sufficient wiring, a diameter .3-.5 mm and lower in the future.

The ultimate in via structure is the stacked via, where buried, blind and through vias may be placed as needed, and

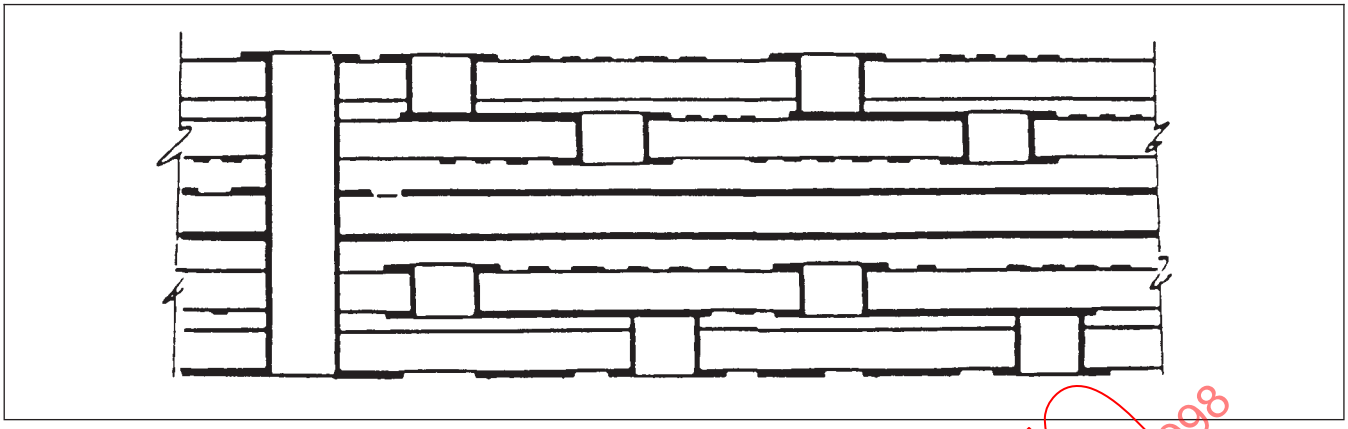


Figure 5−1 Multilayer Construction

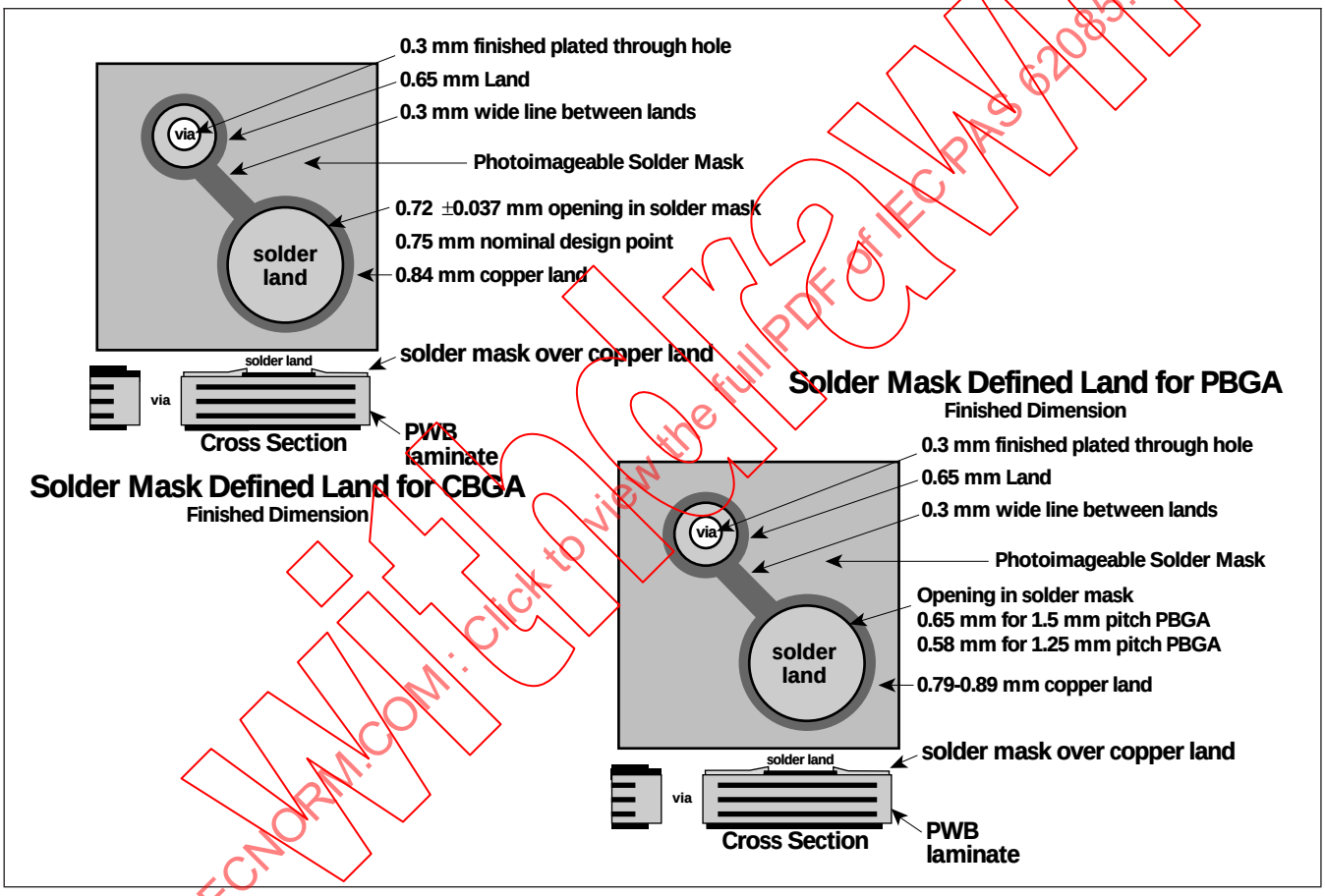


Figure 5−2 Solder Mask Defined Land Patterns for CBGA and PBGA

layers can be joined together at the composite, depending on the requirements of the particular design. The process challenges are for this kind of technology, as are the CAD/CAM systems needed to support random via placement and wiring.

Signal routing for high I/O BGA and µBGA device must be transferred through via holes to other circuit layers. Via holes, drilled and plated in the attachment site, are a consideration but, unless plugged or plated closed, will draw a significant volume of solder from the attachment site when liquified. It may be possible to compensate for the solder material migration, but the strength of the solder fillet will be compromised if a significant volume of the solder alloy is displaced from the attachment area.

Adding circuit layers to the rigid printed board adds cost. However, multilayer construction with via holes drilled and plated through all circuit layers is more economical than the sequential process steps needed for blind or buried via holes.

The board designer must weigh the efficiency gains of

sequential lamination versus the costs associated with fabrication process yield.

5.4.2 Conductors Geometries

The next design and manufacturing challenge is the connection of the chosen via grid. Internal lines and spaces will trend towards 100 µm, from today's standard of 125 µm, and in the future to 75 µm to take full advantage of the tighter via grids. Three lines per channel between vias area is a desirable design point because it permits flexibility in connection to the via or bypass to another point. In order to maintain manufacturing yields at this line density, thinner foils as low as ¼ oz. will be required. Electroless processes or very thin foils with copper plate may be required to execute these fine line designs.

As higher performance components become more common, high performance or electrically controlled carriers will also be needed to maintain communications. Designers will need to be concerned not only with conductor width and spacing but also with the tolerances associated with the design system and the artwork and circuitizing technologies.

Conductor spacings, less than 2X the line width, can be noisy if used in high speed applications. Manufacturing yields will also benefit by greater conductor spacing. The goal is to achieve three lines per channel with maximum spacing and very tight via densities.

Drilling via holes and plating in the attachment site are possible but, unless the hole is plugged or plated closed, the hole will draw a significant volume of solder from the attachment site when the solder is liquified. It may be possible to compensate for the material migration, but the uniform strength of the solder joint should not be compromised.

The detail shown in figure 5-2 is typical of an offset via pad and hole layout often adapted to conventional multilayer circuit board fabrication. The space provided between contact sites allows for a slightly smaller via pad and hole. To prevent the bridging of solder between via pads and adjacent attachment sites, via pad and hole coverage by solder mask material is recommended.

Figure 5-2 and 5-3 show that the via, land and hole are generally offset in the clear zone between device land pattern sites.

5.4.3 Signal Routing

Signal routing channels will be restricted by the space reserved between via land sites. The designer may choose

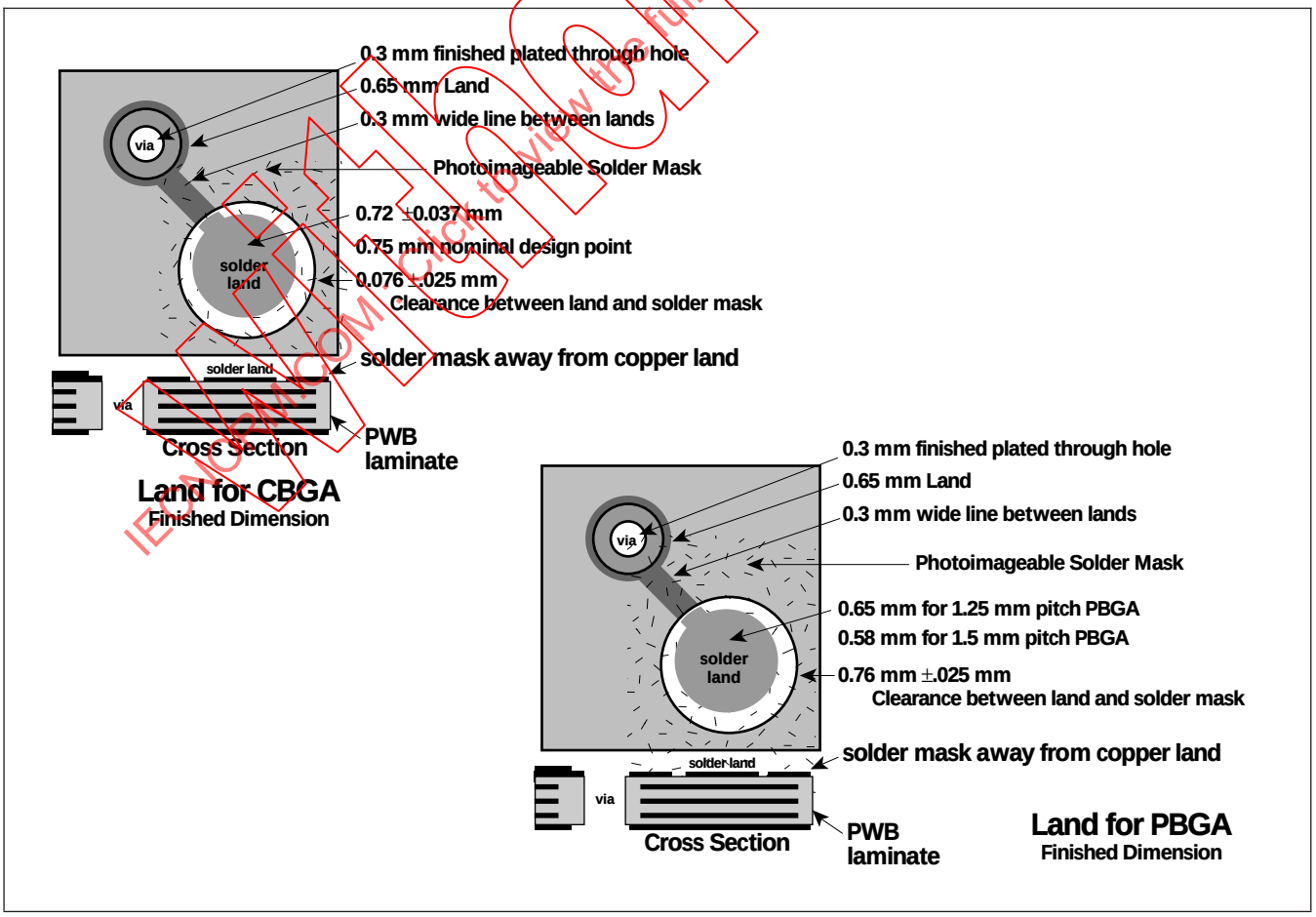


Figure 5–3 Land Defined Land Patterns for CBGA and PBGA

the maximum clearances, widest signal conductors and largest spacings, thereby maximizing fabrication yield and controlling PCB costs. If the design demands higher density circuit routing with finer conductor width and closer spacing, the board will be more difficult to manufacture, increasing overall product cost. The examples shown in Figure 5-4 and 5-5 compare routing paths possible by adjusting via land geometry and via hole size.

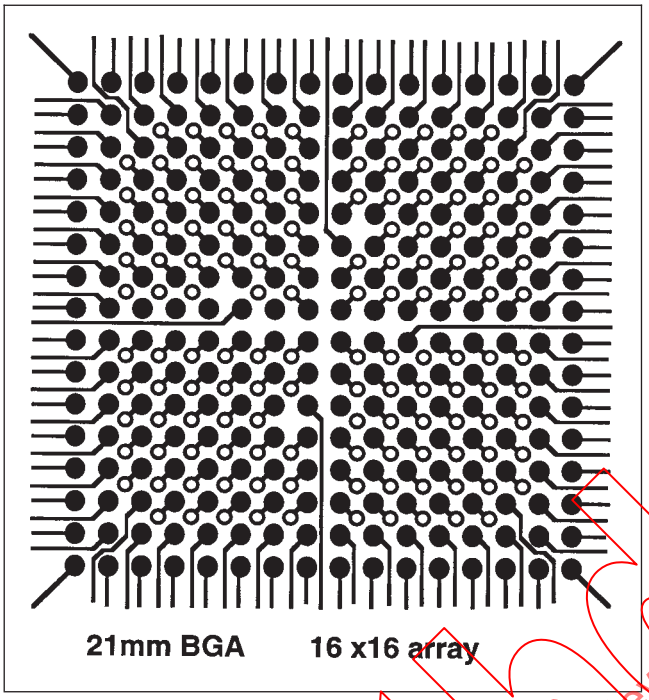


Figure 5–4 PWB Top Surface Including Vias

Figures 5-4 and 5-5 show routing paths between via land and holes that allow for the fabrication process capability of specific suppliers. Table 5-4 shows the number of escapes possible.

Rigid multilayer laminate structures will continue to be the primary material for surface mount applications. The designer must consider, when planning the circuit density, the impact of the physical structure of the interconnecting substrate and the finished cost. Adding more circuit layers will permit lower circuit density, but the added layers will increase the substrate thickness of the substrate and fabrication complexity.

5.4.4 Fine Line/Circuit Layer Trade-offs

Finer lines and spaces, although reducing the need for added circuit layers, may prove to be more costly due to the lower fabrication yield. Alternative fabrication techniques are available for preparing the interconnecting structure, and they may prove more economical for specific applications. The data furnished in table 5-5 may assist the designer in specifying signal routing complexity for conventional etched copper multilayer circuit structures.

If a solder mask defined land pattern is preferred, the land pattern diameter can be enlarged by 0.25 mm (.010 in) to facilitate registration of the smaller mask opening-to-land diameter.

5.5 Test Methodology

5.5.1 Electrical Continuity

Electrical Probing - Continuity testing should be capable of testing peripheral packages with pitches as fine as 0.3 mm. Automated optical inspection of both inner and outer layers is required for high density circuits.

5.5.2 Electrical High Frequency

A time domain reflectometer (TDR) is used to measure characteristic impedance. This measurement verifies an attribute needed for high frequency circuits. A coupon on the side of the board panel may provide this test circuit.

5.5.3 High Acceleration Stress Test

For high performance equipment product reliability is of greater importance than any other product characterization. Board manufacturers need to understand the product performance requirements, especially when evaluating the physical limits of materials, processes and structures used. More meaningful accelerated tests pertaining to the specific application must be defined.

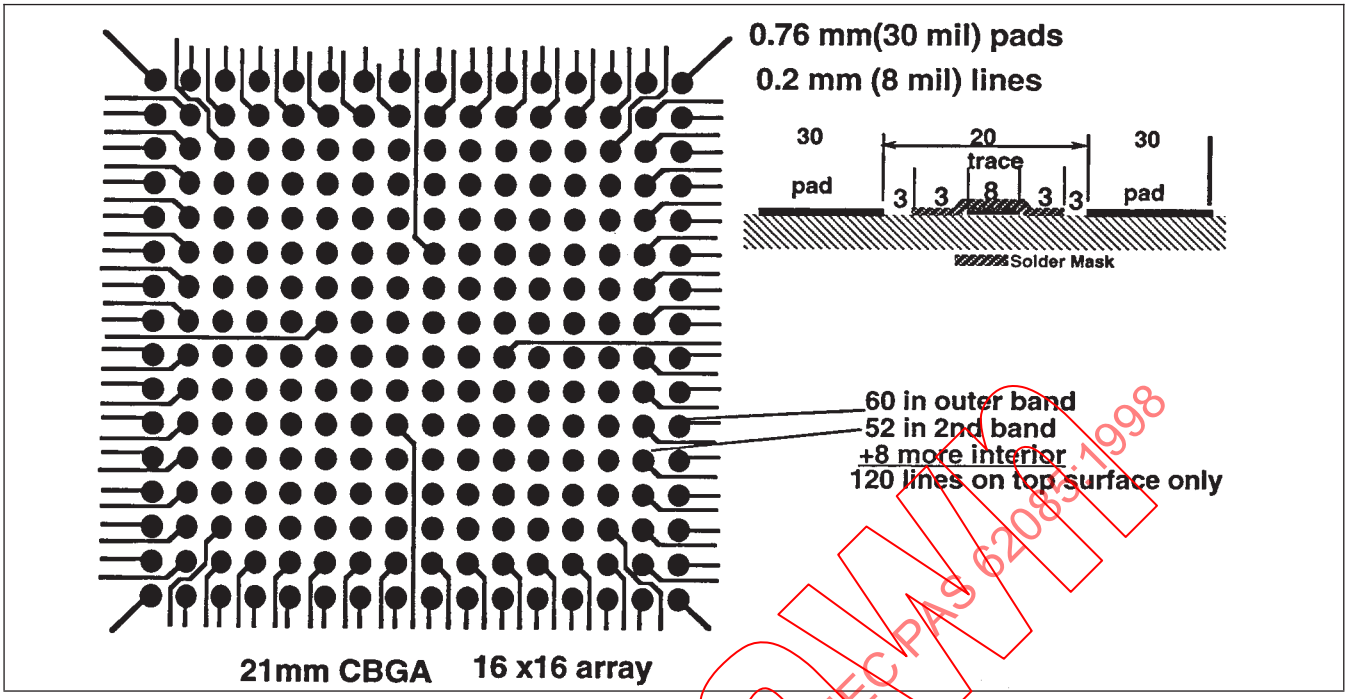


Figure 5–5 First Two Rows of the Array Escape on the Top Surface

Table 5–4 Number of "Escapes" Versus Array Size on Two PWB Layers

Two signal layer PWB's will be sufficient for BGA package escape for properly planned pinouts, even for very high lead counts.				
		Number of Traces between Vias		
		1	2	3
Array Size	Total Leads	○|○	○‖○	○‖‖○
14 x 14	196	192	196	196
16 x 16	256	236	256	256
19 x 19	361	272	316	352
21 x 21	441	304	356	400
25 x 25	625	368	436	496
31 x 31	961	464	556	640
35 x 35	1225	528	638	736

Table 5–5 Ball/Column Grid Array Signal Routing Guidelines

Contact Pitch	P	1.0	1.25	1.5	1.0	1.25	1.5
Contact Land	A	0.55 (.022)	0.65 (.026)	0.75 (.029)	0.55 (.022)	0.65 (.026)	0.75 (.029)
Via Land	B	0.61 (.024)	0.61 (.024)	0.61 (.024)	0.50 (.020)	0.50 (.020)	0.50 (.020)
Via Hole	C	0.33 (.013)	0.33 (.013)	0.33 (.013)	0.25 (.010)	0.25 (.010)	0.25 (.010)
Annular Ring	R	0.14 (.006)	0.14 (.006)	0.14 (.006)	0.12 (.005)	0.12 (.005)	0.12 (.005)
Signal Line	L	0.13 (.005)	0.13 (.005)	0.13 (.005)	0.10 (.004)	0.10 (.004)	0.10 (.004)
Air Gap	G	0.13 (.005)	0.13 (.005)	0.13 (.005)	0.10 (.004)	0.10 (.004)	0.10 (.004)
Signal Track	T	1	2	3	2	3	4

Note: Inches shown in () are approximate.

6 ASSEMBLY PROCESSES

Substrate level assembly of advanced, high pin count components is challenging. It requires a disciplined manufacturing organization, an established process capability, and excellent process control. A ''Design for Excellence'' philosophy is also essential.

Careful handling of the substrates and components during assembly is critical. An organized, clean and controlled factory is required for manufacturing these advanced assemblies. Various levels of cleanliness are required depending on the type of component being assembled. Not all factories must have clean room capability, but cleanliness and environment control are important.

Equipment with environment control may be required if an adequate process capability is to be achieved and maintained. For example, temperature and humidity control will enhance solder paste or adhesive performance.

A good material handling system is also required. As assembly density and component complexity increases proper handling of assemblies between processes becomes more critical. Improper handling can cause quality and reliability problems. Operator handling of assemblies during processing should be kept to a minimum.

A continuous flow assembly process is recommended for processing advanced assemblies, whether the operation is high or low mix, and low or high volume. Smooth, efficient processing of assemblies, with controlled handling between processes, will ensure that all processing variables are kept to a minimum. If a continuous flow operation is not possible, it is still necessary to provide a stable method for the transportation of assemblies between processes. This is typically done with high quality mobile carts. These carts, containing the assemblies, are moved through the factory to each required process.

6.1 Assembly Classification

Advanced assemblies with BGA components are classified as follows:

Single sided
- Type 1x (SMT, FP, BGA, TH)
- Type 1y (SMT, UFP, µBGA, TH)
- Type 1z (SMT, UFP, µBGA, TH)

Double sided
- Type 2x (SMT, FP, BGA, TH)
- Type 2y (SMT, UFP, µBGA, TH)
- Type 2z (SMT, UFP, µBGA, TH)

Legend:
SMT − standard surface mount components.
FP − fine pitch components.
BGA − ball grid array components.
TH − through hole components.
UFP − ultra fine pitch components.
µBGA − microball grid array components.

Figure 6-1 shows examples of Type 1 and Type 2 assemblies.

6.1.1 Process Flow, Type 1

The ideal printed circuit assembly would be single sided and 100% surface mount. However, this is not reality. Most assemblies are mixed technology, with 70% to 90% of the components surface mount. The through hole components are usually high pin count, high power packages and connectors.

Single sided, mixed technology assemblies are desirable because the through components can be mass soldered using a standard wave soldering process.

6.1.2 Process Flow, Type 2

Double sided printed circuit assemblies are more complex, and more difficult to manufacture. Double sided assembly creates two problems. First, two reflow cycles are required. Large components on the secondary side may drop off during the second reflow cycle. In this case a surface mount adhesive may be required to hold components in place. Due to their small size, resistor and capacitor type components are ideal for secondary side attachment.

Options for soldering through hole components include dual wave soldering, wave soldering using dedicated fixtures, selective soldering using dedicated nozzles, applying solder paste over plated-through-holes, and point to point soldering.

Figure 6-2 illustrates Type 1 and 2 surface mount process flow.

6.2 Assembly Materials

6.2.1 Surface Mount Adhesives

Surface mount adhesives are used to hold surface mount components in place during reflow or wave soldering, particulary if the assembly is doubled sided (type 2) . Careful evaluation is required to ensure that the proper adhesive is selected. The glass transition temperature (Tg) of the adhesive is a key element. Attaching components with adhesive also makes them difficult to rework.

Adhesives may also be used for other functions as well, such as improving thermal conductivity, to achieve certain dielectric properties, and encapsulation.

Surface mount adhesives are detailed in IPC-SM-817 ''General Requirements for Surface Mount Adhesives'', which classifies adhesives by grade of cure: heat only, UV or visible light and ambient cure. Test methods are described which detail methods for determining viscosity, working life, shear strength, peel strength, spread/slump, chemical resistance and many other characteristics. These

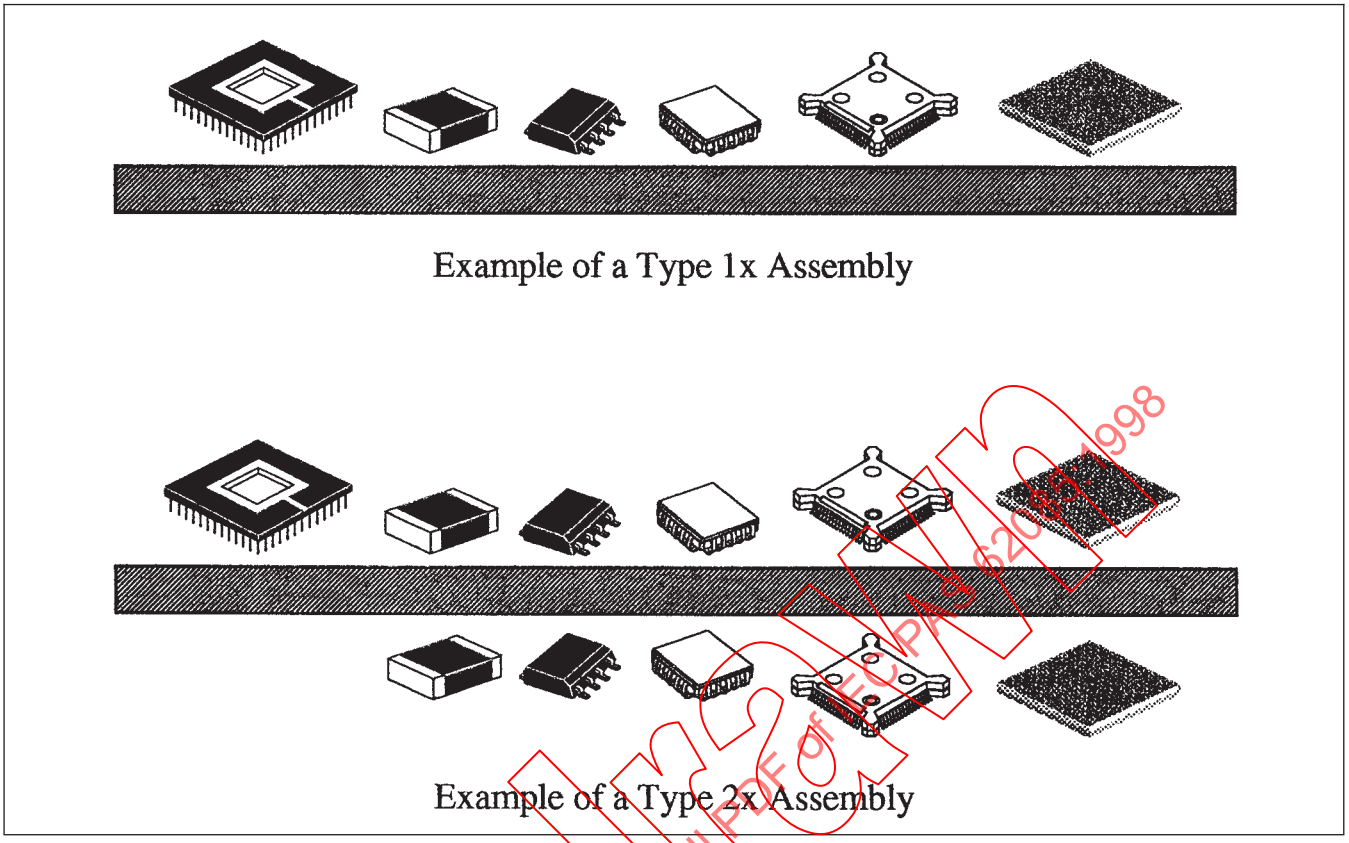


Figure 6–1 Assembly Classification Examples

adhesives can be either thermosetting or thermoplastic.

Surface mount adhesives are applied using dispensing or printing methods. (See 6.3.1)

6.2.2 Conductive Adhesives

Conductive polymer adhesives, developed over 50 years ago, are becoming a practicle means of attaching components. However, until recently, these materials have not been used to assemble electronic circuits. Through-hole mounted components do not work with conductive adhesives. The major problem has been that adhesives have a relatively high surface tension, which prevents the adhesive from wicking into plated-through holes. On the other hand, surface mounted components, which primarily use lap joints, are well suited to attachment with adhesive. Conductive adhesives are a possible replacement for lead solders. However, rework capability and long term reliability remain concerns.

Conductive adhesives are usually classified by their electrical conductivity, of which there are two classifications: isotropic and anisotropic. Isotropic adhesives conduct equally in all directions (the same as solder). Anisotropic adhesives conduct in only one direction (Z-axis).

Additional sub-classifications can be used, including thermosetting versus thermoplastic, and flexible versus rigid. Isotropic and anisotropic adhesives are available as pastes, which can be applied using standard printing and dispensing processes. (See 6.3). Anisotropic adhesives are also available as films, which can be applied manually or with customized equipment.

6.2.3 Soldering Fluxes

The flux type has a direct effect on soldering and cleaning capability. Soldering fluxes are used to prepare surfaces for soldering by removing minor surface contamination and oxidation. Two different flux systems are available: those that require cleaning and those that do not (no-cleans).

Flux systems that require cleaning include standard rosin chemistries that are cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, and water soluble chemistries that are cleaned with pure water or aqueous/saponifier solutions. No-clean (low solids/low residue) fluxes comprise a new generation of materials.

The amount of residue varies depending on the soldering process. Wave soldering tends to leave the least amount of residue because the solder wave scrubs most of the flux off the bottom of the substrate or printed board. Reflow soldering leaves small amounts of residue, while hand soldering can leave moderate to excessive amounts of residue. No-clean fluxes leave a film on the substrate that may cause electrical test probe contact problems. Testability issues must be addressed when considering a no-clean flux.

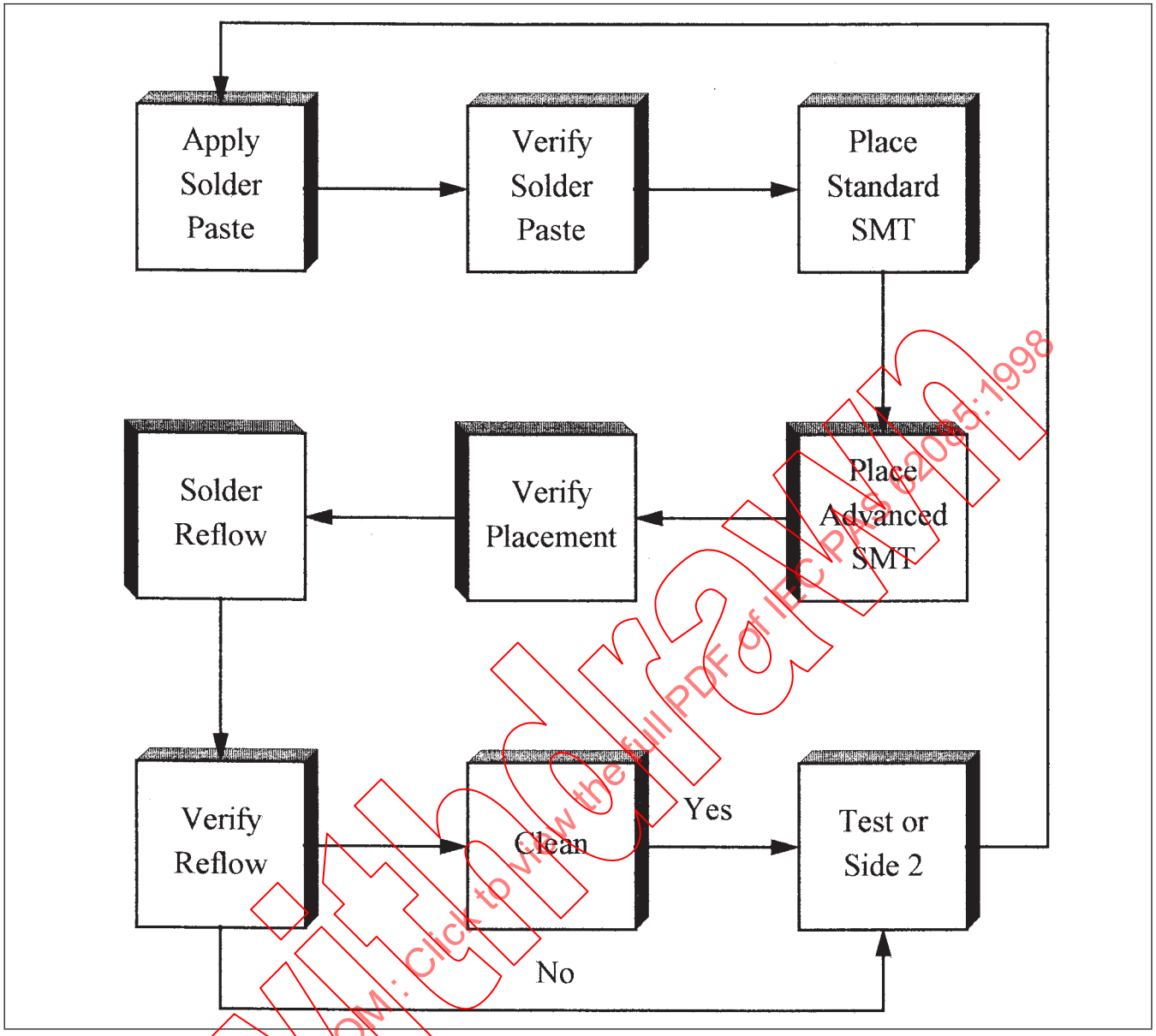


Figure 6–2 Simplified Process Flow for Type 1 and Type 2 Assemblies

The surfaces to be soldered should be carefully analyzed to determine what type of flux activity is required to properly prepare the surfaces for soldering. Fluxes are divided into three basic classifications. These classifications deal with the corrosive and conductive properties of the flux or flux residue in the uncleaned and/or cleaned condition.

Type ‘‘L’’ fluxes have a low activity level, type ‘‘M’’ fluxes have a moderate activity level, and type ‘‘H’’ fluxes have a high activity level. Type ‘‘H’’ fluxes must be used with some caution, the cleaning process must guarantee complete flux removal.

Fluxes are described in ANSI/J-STD-004 ‘‘Requirements for Soldering Fluxes.’’ This standard provides test methods for determining the corrosive and conductive properties of the flux or flux residue.

The requirements for liquid flux, paste flux, solder paste flux, solder preform flux adhesive and flux-cured solder are detailed so that each flux may be characterized by the manufacturer or user in order to determine its impact on the assembly process and product.

In addition, the new ANSI/J-STD-004 standard has added a 1 or 0 to the L, M or H descriptions to indicate the absence or presence of halides. Also, fluxes are further classified by their chemical constituents as an aid in purchasing requirements for military applications. Thus, they can be listed as RO (rosin), RE (resin), OR (organic) or IN (inorganic).

6.2.4 Solder Alloys

Solder alloys that are eutectic or near eutectic are preferred for reflow soldering with the 63Sn/37Pb, 60Sn/40Pb and

62Sn/36Pb/2Ag alloys most commonly used. The addition of 2% silver (Ag) helps limit silver migration (leaching) during reflow when silver bearing components and/or substrates are used.

Solder alloys that are eutectic or near eutectic are also preferred for wave soldering. The solder alloys 63Sn/37Pb and 60Sn/40Pb are the most commonly used. The 62Sn/36Pb/Ag alloy is not commonly used for wave soldering. Table 6-1 shows the melting, reflow and temperature characteristics of the three solder alloys.

Table 6−1 Solder Alloy Characteristics

Solder Alloy	Melting Temperature°C	Reflow Temperature Range°C	Wave Solder Temperature Range°C
Sn63	183	208-223	245-260
Sn60	183-189	214-229	245-260
Sn62	179	204-219	N/A

Other solder alloys would be considered if a step soldering process were to be used, or if it becomes necessary to limit the use of lead. Low temperature alloys usually contain bismuth (Bi) or indium (In). High temperature alloys usually contain higher amounts of lead.

For information on solder alloys see ANSI/J-STD-006 ''General Requirements and Test Methods for Soft Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications''. This standard has replaced QQ-S-571.

6.2.5 Solder Paste

Solder paste is a homogeneous mixture of a powdered metal alloy, a flux system and viscosity modifiers. The solder particles are of a specific size and shape.

Flux systems were described in 6.2.3. Viscosity modifiers include additives to control viscosity, tackiness, slump and drying rate. Solder pastes are used to provide solder for lands on substrates (solder bumping) or solder for the land/lead interface that forms the solder fillet between the component and the substrate. Solder paste application is a difficult process to implement and control.

The selection of two different solder paste alloys, one with a high melting temperature and one with a low melting temperature, can be used for double-sided surface mount assembly. This two step solder approach eliminates the need for adhesives but increases the demands on the printing, reflow and hand soldering processes.

Several companies have developed a process to ''solder bump'' selective areas on a substrate using a solder paste process. Solder paste is applied to the substrate at the fabrication stage. The solder paste is then reflowed, forming the solder bump. The substrate now contains sufficient solder to produce a solder joint. A flux paste is deposited on the land patterns during assembly. The components are placed into the flux paste, which holds the components in place on the bumped solder land patterns. The substrate is then reflowed, and the solder joints are formed.

Solder paste is described in ANSI/J-STD-005 ''General Requirements and Test Methods for Electronic Grade Solder Paste.'' Test methods are defined to determine viscosity, slump, tackiness, wetting, resistance to solder ball formation and shelf life.

Solder pastes are applied using one of two methods: dispensing or printing. (See 6.3.1)

6.3 Equipment Characteristics

6.3.1 Adhesive and Solder Paste Application

Two common methods are used to apply adhesives and solder pastes, dispensing and printing. The advantages and disadvantages of each method are listed below in table 6-2.

Table 6−2 Dispensing Method Comparisons

Method	Advantages	Disadvantages
Printing	Fast process Volume control	Flat surfaces only Material is exposed Thickness limitations Stencil fabrication
Dispensing	Irregular surfaces Volume control Material is enclosed	Slow process Dot size limitations Program generation

Both methods can be used to apply adhesive and solder paste, but dispensing has evolved as the preferred method for adhesive application and printing has evolved as the preferred method for solder paste application. Factors that influence the selection of an application process include the following:

- volume of material that needs to be applied
- size and shape of material that needs to be applied
- volume repeatability and control
- process cycle time
- flexibility

6.3.1.1 Dispensing

Dispensing is accomplished with equipment that ranges from simple hand held units to fully automatic dispensing systems. The dispensing equipment can be table mounted, stand alone, in-line with other equipment, or integrated into a placement system. Most automatic dispensing systems offer vision alignment using fiducial targets. (See 6.3.3). Material is usually dispensed from a preloaded 10 cc syringe.

6.3.1.2 Printing

Printing systems are available in three configurations: manual, semi-automatic, and fully automatic. The printing

equipment can be table mounted, stand alone, or in-line with other equipment. Many semi-automatic printers offer manual or semi-automatic vision alignment capability using fiducial targets. (See 6.3.3). Metal squeegee blades are recommended for fine pitch, ultra fine pitch and BGA printing.

Stencils are preferred over screens because of better image accuracy, volume control and longer service life. Stainless steel is the most widely used stencil material. Three methods are used to create stencil apertures: chemical etching, laser cutting, and electroforming. Chemical etching is the most common method used in stencil fabrication. Laser cutting and electroforming are used when small, precise apertures are required. Electropolishing is used with all three methods to produce a very smooth wall in the aperture. Table 6-3 compares the capabilities of the three fabrication methods.

Table 6−3 Stencil Creation Method Comparison

Capability	Laser	Electroformed	Chemical Etch
Aperture size	****	****	***
Aperture smoothness	*	****	****
Aperture shape	****	****	***
Stencil strength	****	**	****

Legend:
*Least Desirable
****Most desirable

Stencil aperture design is critical for fine pitch, ultra fine pitch and BGA components. The most important rule is to maintain a minimum aspect ratio (width to thickness) of 1.5 (W) to 1 (T). This ensures proper release of the solder paste from the aperture. This rule is illustrated in figure 6-3.

Stepped thickness stencils are one option for varying solder paste volume. The other option is aperture modification, in other words making the aperture smaller than the land pattern.

6.3.1.3 Surface Mount Adhesive Application

Two important variables apply for SMT adhesive application: adhesive quantity and location. Excessive adhesive and/or pattern misplacement will contaminate the solderable area to prevent good solder joint formation during soldering. Too little adhesive can allow components to move prior to the curing process, or allow components to move or fall off during the soldering process, resulting in misplaced or missing components. Surface condition is very important, as adhesives will not adhere to dirty, contaminated surfaces.

6.3.1.4 Solder Paste and Conductive Adhesive Application

Material registration and thickness variation are two important elements of this process. If the material is not applied to the correct location, bridges or opens may result. If the material is not thick enough, or if the thickness varies from location to location, opens may result, especially when dealing with components noted for lead coplanarity problems.

6.3.2 Placement

Placement of complex, high pin count components on substrates is a demanding process. It requires equipment with excellent accuracy and repeatability. This equipment consists of two types: flexible or dedicated placement systems.

6.3.2.1 Flexible Placement Systems

These overhead gantry-type systems can handle most standard surface mount components in addition to handling complex fine pitch and array components such as QFPs and BGAs. All of these systems can place components down to a lead pitch of 0.5 mm, with the more capable systems being able to handle lead pitches down to 0.4 mm. If the substrate is moved during placement the table movement must be very smooth and controlled. Component packaging format is tube, carrier tape and matrix tray. Feeders capable of on-line lead forming are available. Placement rates range from approximately 1,000 to 8,000 per hour for standard components, and 400 to 2,500 per hour for complex components. Vision alignment is the common and preferred choice for complex, high lead count components.

Global and local fiducial targets are recommended with this equipment (see 6.3.2.4).

6.3.2.2 Dedicated Placement Systems

This overhead gantry equipment is dedicated to handling complex, high pin count, fine pitch and array components such as QFPs, BGAs, TAB and flip chip. Use of these systems starts at a lead pitch of 0.4 mm, with some systems capable of handling lead pitches of 0.2 mm. These components require the most accurate and repeatable equipment available, with excellent process control. Component handling and placement accuracy are critical. Component packaging format is tube, carrier tape and matrix tray. Feeders capable of on-line lead forming are available. There is a limited selection of systems available, with placement rates ranging from several hundred to several thousand per hour. Component alignment is vision based. In addition to placement, some systems have the ability to do on-line soldering using a hot bar or laser process.

Global and local fiducial targets are recommended with this equipment (see 6.3.3).

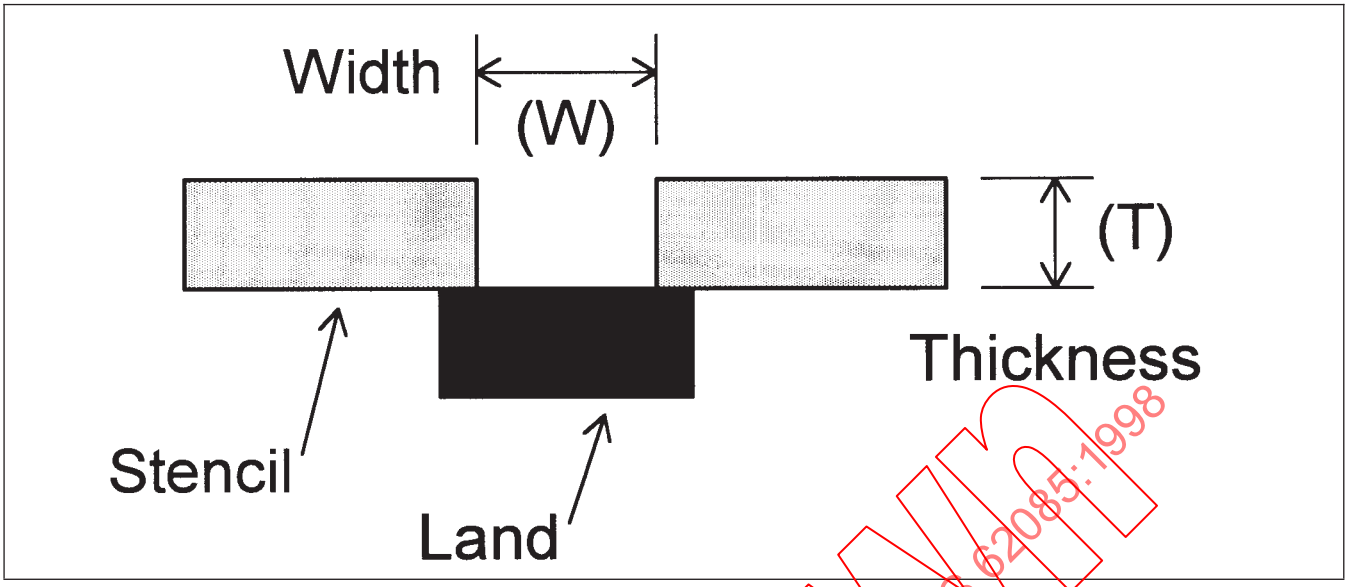


Figure 6−3 Stencil Opening Aspect Ratio

6.3.2.3 Vision Alignment Systems

Vision alignment, using either binary or gray scale imaging, determines the offset between the component center and the placement nozzle center. Figure 6-4 compares binary and gray scale imaging.

Binary imaging uses back lighting, which projects the outline of the component to a camera. This approach works well with peripheral lead components because the leads are projected as part of the outline. However, with area array components the camera sees the outline of the component, it does not see the balls. So, the tolerance between the component edge and the balls must be taken into account because this error will be part of the placement process.

Gray scale imaging uses front lighting along with a camera that is typically capable of up to 256 levels of gray scale imaging, which allows the camera to pick up surface features on the bottom of the component. This method is recommended for array type components. Gray scale imaging allows alignment based on ball location rather than outline location. This is important, because in some cases the position of the balls relative to the outside edge is not accurate enough for reliable placement using a binary system.

Important vision system issues are field of view (FOV), resolution, levels of gray scale (gray scale systems only), component lighting and processing speed. Lead coplanarity inspection capability is also recommended.

A third vision alignment method, which images a component from the side, is being introduced on some placement systems. Primarily intended for standard surface mount components, at this time it is not known whether these systems will be compatible with fine pitch and array type components.

6.3.2.4 Component Placement Requirements

Fine pitch components must be placed using a reliable vision alignment system. Binary vision systems work well with peripheral lead components. Gray scale systems can also be used. In either case the resolution and field of view (FOV) of the camera must be compatible with the pitch and size of the component.

Ball grid array components must also be placed using vision alignment. However, binary vision systems are of limited value with BGA components. The problem relates to the position of the balls relative to the edge of the package. In most cases the allowable error (tolerance) between the package edge and the center of the ball is too great for reliable placement using a binary system. Gray scale vision allows the user to directly align the balls to the lands, eliminating the error caused by edge alignment. A detailed tolerance analysis, such as the one shown in table 6-4, should be done to determine if the ball to outline tolerances will allow reliable placement with binary imaging.

On gray scale imaging systems lighting is important. Typically, plastic BGA components can use standard fine pitch lighting. However, to obtain the proper substrate to ball contrast on tape and ceramic BGA components different lighting may be necessary. Standard lighting illuminates from directly below the component. When contrast problems occur it is usually necessary to illuminate from an angle as well as from below.

6.3.3 Fiducial Targets

Global and local fiducial targets are recommended for placement applications. SMEMA 3.1 ‘‘Fiducial Mark Standard’’ describes a recommended fiducial.

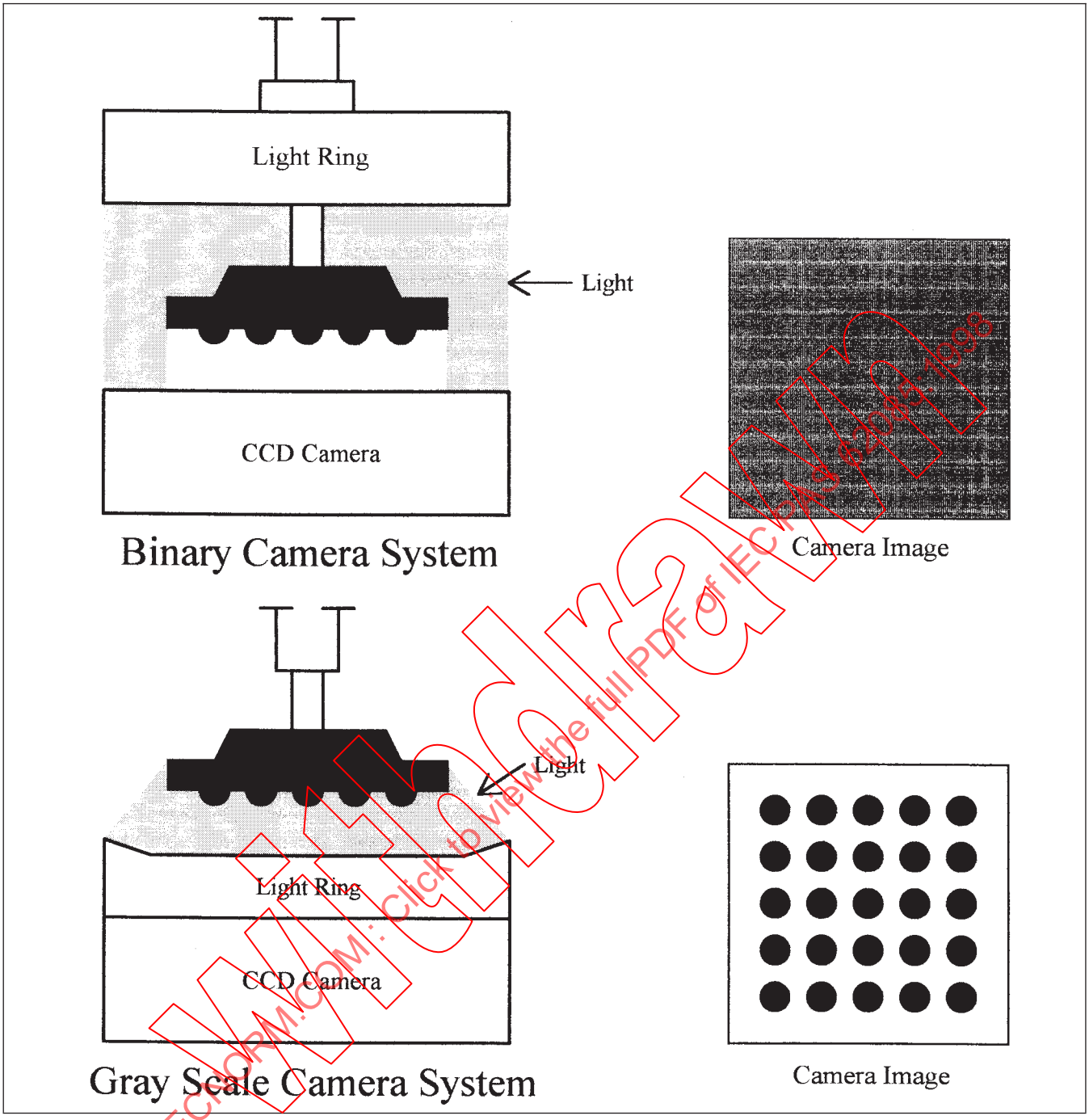


Figure 6−4 Binary and Gray Scale Image Comparison

6.3.3.1 Fiducial Marks

A Fiducial Mark is a printed artwork feature which is created in the same process as the circuit artwork. The fiducial and a circuit pattern artwork must be etched in the same step.

The Fiducial Marks provide common measurable points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of Fiducial Marks. These are:

A. Global Fiducials
Fiducial marks used to locate the position of all circuit features on an individual board. When a multi image circuit is processed in panel form, the Global Fiducials are referred to as Panel Fiducials when present for the panel.

B. Local Fiducials
Fiducial marks used to locate the position of an individual component.

A minimum of two global fiducial marks is required for

Table 6–4 Placement Capability - Binary Verses Gray Scale

Description	Binary Vision	Gray Scale Vision
Machine error	30 µm [0.0012 in]	30 µm [0.0012 in]
PCB error	56 µm [0.0022 in]	56 µm [0.0022 in]
Component error	447 µm [0.0176 in]	117 µm [0.0046 in]
3 Sigma process error	452 µm [0.0178 in]	132 µm [0.0052 in]
Maximum allowable error	297 µm [0.0117 in]	297 µm [0.0117 in]
CP	0.66	2.25
CPK	0.59	2.02

Notes:
1. Root-mean-square method of calculation.
2. Component type: tape ball grid array, 1.27 mm pitch.

correction of translational offsets (x and y position) and rotational offsets (theta position). These should be located diagonally opposed and as far apart as possible on the circuit or panel.

A minimum of two local fiducial marks are required for correction of non linear distortions (scaling, stretch and twist). These should be located in a triangular position as far apart as possible on the circuit or panel.

A minimum of two local fiducial marks are required for correction of translational offsets (x and y position) and rotational offsets (theta position). This can be two marks located diagonally opposed within the perimeter of the land pattern.

If space is limited, a minimum of one fiducial mark may be used to correct translational offsets (x and y position). The single fiducial should be located inside the perimeter of the land pattern with a preference for the center.

The minimum size for local, global or panel fiducials is 1.0 mm. Some companies have chosen a larger fiducial (up to 1.5 mm) for panel fiducials. It is a good practice to keep all fiducials the same size.

6.3.3.2 Fiducial Mark Design Specifications

The Surface Mount Equipment Manufacturers Association (SMEMA) has standardized on the design rules for fiducials. These rules are supported by the IPC and consist of:

A. Shape
The optimum fiducial mark is a solid filled circle.

B. Size
The minimum diameter of the fiducial mark is 1 mm [0.040 in]. The maximum diameter of the mark is 3 mm [0.120 in]. Fiducial marks should not vary in size on the same printed board more than 25 microns [0.001 in].

C. Clearance
A clear area devoid of any other circuit features or markings shall exist around the fiducial mark. The clearance area should be at least 2 times the radius of the fiducial mark.

D. Material
The fiducial may be bare copper, bare copper protected by a clear anti-oxidation coating, nickel or tin plated, or solder coated (hot air leveled).

The preferred thickness of plating or solder coating is 5 to 10 microns [0.0002 to 0.0004 in]. Solder coating should never exceed 25 microns [0.001 in]. If solder mask is used, it should not cover the fiducial or the clearance area. It should be noted that oxidation of a fiducial mark's surface may degrade its readability.

E. Flatness
The flatness of the surface of the fiducial mark should be within 15 microns [0.0006 in].

F. Edge Clearance
The fiducial shall be located no closer to the printed board edge than the sum of 5.0 mm [0.200 in] (SMEMA Standard Transport Clearance) and the minimum fiducial clearance required.

G. Contrast
Best performance is achieved when high contrast is present between the fiducial mark and the printed board base material.

It is good design practice to locate global or panel fiducials in a three point grid based datum system as shown in figure 6-5. The first fiducial is located at the 0.0 location. The second and third fiducials are located in the x and y directions from 0.0 in the positive quadrant. The global fiducials should be located on the top and bottom layers of all printed boards that contain surface mount as well as through hole components since even through hole assembly systems are beginning to utilize vision alignment systems.

All fine pitch components should have two local fiducials system designed into the component land pattern to insure that enough fiducials are available every time the component is placed, removed and/or replaced on the board. All fiducials should have a soldermask opening large enough to keep the optical target absolutely free of soldermask. If soldermask should get onto the optical target, some vision alignment systems may be rendered useless due to insufficient contrast at the target site.

The internal layer background for all fiducials must be the same. That is, if solid copper planes are retained under fiducials in the layer below the surface layer, all fiducials must have copper retained. If copper is clear under one fiducial, all must be clear.

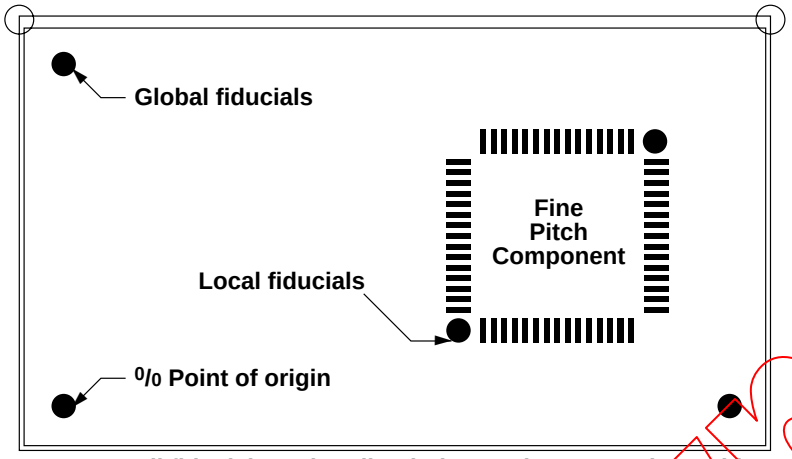


Figure 6−5 Fiducial Locations on a Printed Circuit Board

6.3.4 Soldering

Surface mount solder joint quality is of extreme importance because the solder joint must provide structural strength in addition to providing the electrical connection. For detailed solder joint information reference IPC-SM-782A, Surface Mount Land Patterns; ANSI/J-STD-001, Requirements for Soldered Electrical and Electronic Assemblies; and IPC-A-610, Acceptability of Printed Board Assemblies.

6.3.4.1 Surface Mount Soldering

Mass reflow soldering is used to form surface mount solder joints. A reflow system must do the following:

- Evaporate solder paste solvents
- Activate the flux and promote fluxing action
- Preheat the components and substrate
- Melt the solder and allow solder joints to form
- Cool the completed assembly

Four mass reflow methods have evolved, they are:

- Vapor phase (used primarily in special applications)
- Lamp infrared (declining in use)
- Panel infrared (declining in use)
- Forced gas convection (preferred method for most applications)

Forced gas convection has become the preferred choice for mass reflow because of its ability to heat assemblies uniformly. This method transfers greater than 90% of its energy to the substrate by convection. The rate at which heat is transferred is directly proportional to the difference in temperature between the heated air and the assembly. Convection system attributes include ease of profiling and low source temperatures.

The reflow time/temperature profile is very important. Although no industry standard/temperature profile has been developed some common rules can be applied: maintain a heating ramp rate of 0.5 to 2 °C/second, flux active time should range from a minimum of 30 seconds to a maximum of 120 seconds, remain above solder liquidus for 30 to 60 seconds, achieve a temperature of 25 to 40 °C above solder liquidus, and avoid being above the substrate Tg for more than about 3 minutes.

Profiling equipment capability has improved considerably in recent years. Profiling should be done to ensure proper reflow. Thermocouple location is a critical part of the profiling process. One thermocouple should be placed in a low density area, and another one should be placed in a high density area. The remaining thermocouples should be placed on critical components to ensure they are within the desired temperature limits.

6.3.4.2 Through Hole Soldering

Wave soldering is still the method of choice for soldering through hole components on single sided assemblies. On double sided assemblies the process is more complex, and in some cases wave soldering is not possible. There are creative alternatives.

Wave soldering can be used to solder double sided assemblies. However, plastic components may be damaged by the molten solder. It is recommended that only ceramic resistors and capacitors be subjected to wave contact. Secondary side components must be held in place with a surface mount adhesive.

Wave soldering may be possible using dedicated fixtures

that shield the surface mount components from the wave. The secondary side of the assembly must be designed to allow for this process. A clearance area of about 5 mm around the component is required.

The wave soldering time/temperature profile is important. Although no industry standard time/temperature profile has been developed some common rules can be applied: maintain a heating rate of 0.5 to 2 °C/second, preheat secondary side components to within 100 °C of the solder pot temperature, flux active time should range from a minimum of 30 seconds to a maximum of 120 seconds, use a solder dwell time of 1 to 2 seconds, and avoid being above the substrate Tg for more than about 3 minutes.

Selective soldering using a small solder pot and a dedicated nozzle is another option. These systems direct molten solder to specific component locations using the custom nozzle. A clearance area of about 3 mm around the component is required.

Some companies have been successful at printing solder paste over the plated-through-holes, and then inserting the through hole components in to the solder paste. The solder paste melts during reflow and forms a solder joint. However, proper solder joint formation is directly related to the hole and pin diameter, substrate thickness, and to some extent the pin length.

The last option is point to point contact soldering, done either by hand or with a robot. This method is quite slow. Typically, it is desirable only when the pin count is low.

6.3.5 Cleaning (General)

Cleaning the assembly after soldering is normally done to remove any corrosive residues that could degrade reliability and insulating residues that could interfere with probe testing. Military specifications have always required cleaning of activated fluxes, followed by ionic contamination testing to ensure that the remaining residues do not degrade the assembly. Cleaning is also required prior to conformal coating on military products. Many assemblers cleaned commercial product to military specification levels to guarantee field performance.

The cleaning process has received considerable attention in recent years because of the international effort to eliminate ozone depleting chemicals such as chlorofluorocarbons (CFCs) and 1,1,1-trichloroethane (TCA). These materials were used to remove the post-soldering residues from rosin and synthetic activated fluxes. Production of these materials ceased on 31 December, 1995 in accordance with the Montreal Protocol. Users may continue to use existing stocks of materials until they are exhausted, however the products must be labeled that they contain or were manufactured with an ozone depleting substance. In addition, the Department of Defense (DoD) and its contractors stopped using these materials at year end 1995.

Since there is cost associated with the purchase of new equipment and cleaning agents, manufacturers will choose one or more alternative flux and cleaning combinations based on the product they are building and the cost, performance and environmental impact of the possible options. The choice of an alternative cleaning method must be coupled with an understanding of the flux-type being used as described below. Companies presently cleaning their assemblies primarily to remove solder balls will be able to eliminate this process step by converting their printed board designs to solid solder deposit (SSD) designs. The SSD process, where the solder needed for assembly is applied, reflowed and cleaned at PWB fabrication, eliminates solder balling as an assembly level issue.

The cleaning handbook, IPC CH-65 ‘‘Guidelines for Cleaning of Printed Boards and Assemblies’’ contains additional information on many of these topics.

6.3.5.1 BGA Cleaning

The cleaning of BGAs is simplified by the reasonable stand-off heights of the present package designs. As packages grow in size and I/O (ball) count, while spacing drops, the distance from the board to package will decrease as the grid and balls become smaller. Successful cleaning in the mainframe computer industry on flip chip and similar attachment technologies was readily accomplished using organic solvents. 1,1,1-trichloroethane (a known ozone depleter) was often used to remove the non-activated or minimal activated flux residues from such soldering methods. Users implementing BGA designs will have the best chance for success by starting with cleaning agents that mimic the physical properties of 1,1,1-trichloroethane. Studies conducted to assess the penetration and drainage of cleaning agents were accomplished by attaching the BGA devices to glass plates, reflowing, and then passing them through a candidate cleaning process. Visual inspection allows the various cleaning agents and attachment fluxes or solder pastes to be ranked in order of ease of removal. A short list of soldering materials and cleaning agents can then be developed for long term temperature - humidity - bias testing prior to a decision on the materials and processes to be implemented on the shop floor.

6.3.5.2 Solvent Cleaning Technology

Low surface tension/low viscosity organic solvents probably offer the greatest long term flexibility for cleaning present and future BGA designs. Often the pure solvents do not have sufficient solvency power to attack the baked-on residues from attachment temperatures exceeding the standard tin/lead eutectic alloy. Solvent blends and azeotropes have been developed that do have the required solvent power while retaining the desired physical properties that enhance penetration, rinsing, draining and drying.

Examples of such materials are the cychlohexane/2-propanol azeotrope wash followed by 2-propanol rinsing and evaporative drying, fluorocarbon inerted organic solvent wash, rinse and dry, fluorocarbon/organic mechanical emulsion wash followed by fluorocarbon rinsing and drying, in addition to the new HCFC-225/trans dichloroethylene azeotrope (with and without methanol for better removal of ionics) vapor defluxing; and HydroFluoroCarbons (HFCs), HydroFluoroEthers (HFEs) or Volatile Methyl Siloxanes (VMSs) with trans dichloroethylene or similar solvency enhancing materials. An example would be the HFE (Hydrofluoroether) Cosolvent Process. Certain processes that now use PerFluoroCarbons (PFCs) as either inerting or rinsing agents will be converted to the environmentally preferred hydrogen containing fluorocarbons (HFEs, HFCs) as soon as these materials are commercially available. The cyclohexane/2-propanol azeotrope wash followed by 2-propanol rinse has been found to be very effective in cleaning ultra high density high speed computer printed board assemblies.

6.3.5.3 Aqueous BGA Cleaning Technology

As long as stand-offs remain in the 0.1 to 0.5 mm range (depending on the package size) and higher, aqueous cleaning will be a viable cleaning option. Aqueous cleaning in the 0.05 mm standoff range can be done with high pressure in-line equipment. Any problems encountered will usually be in the rinsing and drying steps. Water soluble fluxes and solder pastes are formulated with higher levels of more active and potentially corrosive materials than rosin fluxes. These formulations provide good soldering with low defect levels, but rigorous cleaning in a powerful aqueous (or aqueous/saponifier) process, with or without neutralizers, is required. Aqueous processes may work on first generation 1.25 mm pitch BGA designs, but attempts to clean finer pitch designs may be compromised by the rinsing and drying issues inherent in aqueous systems.

Rosin-based flux and solder paste residues can be removed using either:

1. Semi-aqueous solutions or 5-10% semi-aqueous solvent-in-water emulsions or
2. Aqueous solutions of alkaline organic or inorganic saponifiers.

Synthetic activated (SA) based flux and solder paste residues can be removed with the same materials, excluding saponifiers. The semi-aqueous process involves two steps: (1) an organic liquid is used to dissolve and remove the rosin or synthetic activated flux residues, and (2) water is used to rinse away the remaining organic material by first forming a solvent-in-water emulsion of the cleaning agent and soil, which is then removed along with any soluble contaminants in sequential standard aqueous rinses and then dried. One major advantage of this method is the excellent ability of the semi-aqueous material to get under low profile components and its excellent solvency for flux residues. Formulation of the cleaning agent with the proper surfactant to enhance rinsing has been successfully qualified for mainframe CPU-BGA cleaning on 0.2 mm standoff devices; incorporating three different solder alloys and fluxes. The early concerns about flash point and combustability have been dealt with by the materials suppliers with second and third generation products that have flash points above 95 °C and by the equipment suppliers who have incorporated various suppression devices and alarms. Large automated 2-propanol cleaning systems are now used routinely by the industry. Decanters, which are internal settling tanks for the emulsion phase in semi-aqueous systems, allow the separation of the emulsion into the organic semi-aqueous material, which is returned to the wash tank, and water, which is returned to the rinse sections; thus automatically recycling both the organic cleaning agent and the water. The environmental impact of this cleaning material and process is minimal.

Aqueous saponifiers have been in use for many years in the cleaning of through-hole assemblies. The saponifier is required for rosin flux removal, but it is also used in reduced concentration with water soluble flux to remove finger prints and other residues that can not be removed by pure water. This method can also be used with some no-clean fluxes and solder pastes. However, saponifiers have a pH of approximately 10.5 to 11.0 and so the effluent from the cleaner must be properly neutralized before disposal to municipal sewer. The traditional mono ethanolamine based organic saponifiers place a very high biological oxygen demand (BOD) on the waste treatment system, which is regulated in most localities. The new inorganic saponifiers have more environmentally benign waste streams. (See IPC-AC-62 and IPC-SA-61).

6.3.5.4 Ultrasonic Cleaning

Ultrasonic cleaning was not accepted for many years due to early reports of damage to component wire bonds from the 25 MHz ultrasonic cleaning systems used to clean metal case transistors. The development of better wire bonding technology, plastic encapsulated components (which tended to dampen the harmonics) and the move to the less aggressive 40 Khz cleaning frequency greatly reduced the risk of damage from ultrasonic cleaning processes. The virtual elimination of harmonics by ‘‘sweep frequency’’ ultrasonics has now allowed even very delicate components and very high packaging density PWAs to be cleaned quickly, efficiently and without damage. Assessment of the effect of ultrasonics on various components can be performed using IPC-TM-650 Methods 2.6.9.1 and 2.6.9.2 for components that are loose in a basket and components soldered to the printed board.

6.3.5.5 No-Clean BGA Concepts and Processes

In BGA applications where a non-corrosive rosin based flux or paste is used the flux residue may not need to be removed. Such no-clean assembly of BGA designs will be most successful when the printed board and the BGA package are both solderable and clean, which is defined as free of any processing residues that could lower the SIR below 10^{12} when measured on the IPC-B-24 SIR comb pattern at 85 °C/85%RH. The incoming printed boards can be easily tested for polyglycols which are known to degrade SIR using IPC-TM-650, Methods 2.3.38 and 2.3.39. Low residue soldering fluxes are preferred for the attachment process, with the best balance of soldering and freedom of electrical effects being achieved when the residue is equal to or less than 20% of the applied flux.

Another approach to eliminating cleaning has come in the form of ‘‘controlled atmosphere soldering’’. This category includes both wave and reflow soldering under a nitrogen or mixed non-oxygen containing environment, in addition to the use of plasmas to pre-clean the surfaces and eliminate the use of flux and therefore flux residues altogether.

A cleaning handbook is available, IPC-CH-65, Guidelines for Cleaning of Printed Boards and Assemblies.

6.3.5.6 Cleanliness Testing

Solvent extraction testing is the common method used for determining the cleanliness of a completed assembly. A solution of 75% isopropyl alcohol and 25% deionized water is used to remove contaminates. The tester measures the ionic conductivity of the contaminates and displays the results in micrograms of sodium chloride per square inch. (See IPC-TM-650, method 2.3.26.1)

The equipment available today includes dynamic and static variations, as well as elevated temperature capabilities, volume variability, etc. The challenge of removing flux residues from underneath low profile surface mount components has created large variations in the measurements from one instrument to another.

6.3.5.7 Stencil Cleaning

Stencil cleaning can be readily accomplished with cleaning agents matched to the flux used in the attachment step solder paste. Semi-aqueous systems, either as pure solvent followed by a water rinse or as a 5-20% emulsion of the semi-aqueous cleaning agent in water followed by a water rinse, are quite effective in cleaning rosin or synthetic activated flux solder paste from either brass or stainless steel stencils. High pH (alkaline) saponifers can attack brass stencils, so their use for this application should be minimized. Water soluble flux solder paste can be removed with water systems, although the emulsion systems can be used to remove other soils such as fingerprints. The effluent from stencil cleaners of any type should be carefully monitored for heavy metals such as lead, since solder paste is washed off the stencils in this process.

6.3.5.8 Maintenance Cleaning

BGA designs may often be in high value use products that are returned periodically from the field for engineering upgrades, modifications, reconfiguration or repair. These printed board assemblies need to be cleaned in a maintenance cleaning system to remove the oils, soot, fingerprints or other air-borne particulate that accumulates over time. These contaminants should be removed prior to any testing to ensure accurate test and subsequent action data. Emulsion systems containing 5-10% of a semi-aqueous cleaning agent have been qualified for such cleaning, since such emulsions are very compatible with the wide range of materials of construction found in a completed assembly.

6.3.6 Rework

Rework is done to an unacceptable end product to make it acceptable. Rework is not a substitute for proper assembly and quality control techniques. Every effort should be made to solder the component correctly the first time. Reworking FP and BGA components is difficult. Rework should be avoided unless the solder joint is completely unacceptable.

Individual solder joints can be reworked without removing the component. If the component must be removed the rework process consists of component removal, land preparation, solder and flux application, component placement and solder reflow. Land preparation is one of the most important aspects of rework. Old solder must be removed, and fresh solder must be added.

Rework equipment is expensive and complex. In most cases computer controlled, vision aided rework equipment is recommended. Computer controlled systems allow time/temperature profile development and storage. The vision system is used to align the leads or balls to the substrate. Hot air nozzles are used to concentrate the heat needed for solder flow. Automatic handling mechanisms are used to remove and replace the component.

Operator training is critical. They must be trained to use the rework equipment, and they must be trained to understand workmanship standards, such as ANSI/J-STD-001. Only trained, proficient operators should be allowed to rework components.

6.4 Package Attachment Process Details

6.4.1 Substrate Preparation

Substrates must be handled carefully. The condition of the attachment area is of prime concern. The surface must be kept in a solderable condition. This means the substrate

must be protected from contaminates such as dirt and finger prints. Organic coatings are more sensitive to contamination, especially acids and oils from finger prints.

6.4.2 Component Preparation

Components must be packaged properly in either matrix trays or tape and reel. Care must be taken to avoid package and lead damage. Solderability of attachment points must be maintained. Moisture sensitive components must be handled and stored properly. (See IPC-SM-786, Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages).

6.4.3 Heat Sink Attachment

Heatsinks of various sizes and shapes are attached to complex packages to aid in removing heat. Most heat sinks are made from aluminum, which is anodized to protect the aluminum surface. Thermally conductive plastics have also been used.

The simplest, and best method for attaching heatsinks is to have a package that is designed for a clip on heatsink. A thermally conductive grease is applied between the heatsink and component. The heatsink is held in place by a metal clip that can be easily removed to allow rework.

Attaching heatsinks with an adhesive is also possible, but more difficult. A flexible, thermally conductive adhesive is required. The adhesive must be flexible to compensate for the difference in the thermal coefficient of expansion between the heatsink and the component. The bonding surfaces must be very clean. The anodizing should be removed from the heatsink bonding surface. The thickness of the adhesive must be controlled depending on the thermal characteristics of the adhesive, and the rate of heat transfer that is required.

A third option is the use of a thermally conductive, double sided tape. The tape can be pre-cut to the correct size. A minimum force must be applied to the tape to achieve mating of the tape surface to the component and heatsink surfaces.

Another option is to fill the area between the bottom of the component and the top of the substrate with a thermally conductive adhesive.

6.4.4 Process Control

Some level of process control is recommended for each assembly process. Process control is the strategy that relates product specifications to process capability and process repeatability. To control the process, one must understand the assembly process and how each variable contributes to product quality. Process control requires a stable process that is performed exactly the same way each time it is done. Ball grid array technology forces the implementation and use of good process control.

Currently, the goal is to establish a system that encourages continuous improvement starting with at least a 3 sigma process capability, the future goal is to establish and maintain a 6 sigma process capability. A common mistake involves statistical process control (SPC). Gathering and displaying statistical data is not all there is to process control. SPC is one of the tools used to help evaluate processes and keep them in control. Process control is a combination of product specifications, process capability, process standardization, data collection (SPC) and failure analysis.

For guidance reference IPC-PC-90, General Requirements for Implementation of Statistical Process Control, which provides guidelines for implementing process control.

Automated optical inspection (AOI) is an evolving technology. Currently, AOI suppliers are focusing on three areas: inspection after solder paste printing, inspection after component placement, and inspection after wave and reflow soldering. Currently, automated inspection is capital intensive, however, lower cost AOI inspection tools are becoming available.

Electrical testing is used to evaluate the quality and functionality of the electronic assembly. In-circuit Test (ICT) and Functional Test (FT) are the two common approaches. ICT is used to detect faults caused by the manufacturing process and also to isolate the majority of bad components. FT is used to detect device faults on the assembly at speed. Another approach is to place a simplified in-circuit tester at the end of the assembly line and use it as a manufacturing defect analyzer (MDA). The product is tested immediately after assembly. Problems are relayed quickly back to manufacturing so corrective action can be taken while the product is being assembled.

AOI and electrical test equipment should be used to determine process capability and as a process control tool. They should never be used to simply inspect product. During production fine pitch solder joints are very difficult to inspect, and ball grid array solder joints are impossible to inspect. The process must be capable of producing an acceptable solder joint without visual inspection.

6.4.5 Process Comparison

Surface mount component attachment is a complex process. As the component pin count increases the complexity of the assembly process increases. In general terms, the complexity of the various surface mount processes can be compared as shown in table 6-5.

6.5 Assembled Board Test

Rather than providing information on assembled board test in general, this section points out areas where testing boards with high performance, high pin count I/C packages differs from testing boards with conventional SMT and THT packages. It is assumed that the reader is familiar

Table 6–5 Surface Mount Processes Comparison

Process	SMT	FPT	BGA
Printing	**	****	***
Placement	**	***	****
Reflow	**	***	***
Cleaning	**	**	***
Rework	**	****	****

Legend
*Least complex
****Most complex

with assembled board test techniques, including in-circuit ATE and functional test.

6.5.1 Test Strategy

High performance, high pin count I/C packages pose challenges, particularly with access, to existing test strategies. However, their inclusion on boards generally does not require a different test strategy altogether. For example, if in-circuit ATE followed by functional test is working successfully on conventional SMT boards, in-circuit ATE followed by functional test will likely meet the needs of testing boards with high pin count I/C packages. In other words, the changes in test required for assembled board test are evolutionary, rather than revolutionary.

6.5.2 In-Circuit ATE Access

Conventional SMT boards generally must provide access points for contact by an ATE bed-of-nails fixture. One access point for each network is required. This point may be a THT lead (if the board has THT components), a via (used for conductor routing), an edge finger contact, or a designed-in Test Point. Various CAD tools are now available to locate and identify access points for test. Some can even add test points to networks that would not otherwise be accessible.

Different types of high performance, high pin count I/C packages have different impacts on ATE access.

6.5.2.1 Through Hole Mounted Array Packages

The through hole mounted array packages, such as CPGA and PPGA, typically require few additional access points. Each lead protrudes through the board, and may be able to serve as the access point for its network. It may not be possible to use every lead as a test target though, because the concentration of spring probes on a 2.54 mm (or smaller) grid may impose a greater force than can be overcome by atmospheric pressure, in a vacuum actuated fixture.

A mechanical fixture, or a vacuum fixture with a pushdown lid, may be used to provide greater down force. However, care must be taken to avoid excessive board bowing, which may result and cause damage to the board. Lower force spring probes can be used to alleviate these problems. Preferably, some of the networks connected to the through hole mounted array package can be probed at access points other than the leads of the device.

6.5.2.2 Surface Mounted Array Packages

The surface mounted array packages, such as BGA and chip scale packages, seem to require many more additional access points when compared to through hole mounted array packages, since no part of the package protrudes to the secondary side. However, conductors from the mounting lands of the device must be routed to other places on the board.

Because of the density of these lands, the routing cannot be done on one layer and usually involves many layers. Unless blind and buried vias are used, this routing usually results in a pattern of through hole vias, visible from the secondary side. If properly planned for, these vias may be usable as ATE test access points. Of course, they must be exposed, that is, not covered with secondary side components, or tented or filled with soldermask.

If vias are used for test access points, the density of spring probes must be considered, just as it was for through hole mounted array packages. Again, it is preferable to use only some of the points near the device, and find alternative points for the remaining networks. If the device routing vias cannot be used at all, then alternating points must be found, away from the high pin count device. This may mean finding vias elsewhere on the network and designating them as test points. If the board includes through hole mounted devices or edge finger contacts, then these can be used as test access points.

6.5.2.3 Peripheral Packages

The impact of peripheral packages such as PQFPs and CQFPs on ATE access is very similar to the impact of surface mounted array packages. They often have regular patterns of routing vias, which can be considered for access. Unlike the surface mounted array packages, the peripheral packages have leads exposed on the primary side. However, their small size renders them useless as ATE access points, even if a double-sided fixture is considered for other reasons.

Packages with leads on only two sides instead of four, such as TSOPs and SSOPs, generally do not have regular patterns of routing vias, like PQFPs and CQFPs. For these parts, all their networks must be probed at random vias found elsewhere on the board.

6.5.3 Locating Open Solder Joints at ATE

Traditional in-circuit test techniques, even with high-fault-coverage ICT models for each device, have difficulty distinguishing between an open SMT joint and a device problem. This is because the response that the tester can observe, at the bed-of-nails, is identical for both kinds of faults. On older boards, a handheld probe could be used to touch each lead on the device in question, to determine if there was an open. The scratch probe is grounded, and whether the tester does not see the network go to ground, it knows that the joint is the problem, and it can therefore indict only the joint, and not the entire device.

But scratch probing is impractical on all high performance, high pin count packages. Either the leads (if they exist at all) are not exposed, or they are too fragile to consider scratch probing. Without the scratch probe, the tester can only indict the entire device, leaving the debug person to determine whether the cause of the test failure is a joint or a device. This can result in good devices being replaced, when the real problem is solder joint opens. This increases costs and hides assembly process information (the opens defect rate) that might be used to improve the assembly process.

The unpowered opens feature of some ATE systems should be considered when using high performance, high pin count I/C packages. With this method, the presence of an electrical connection between the board and the device's leadframe can be verified separately from the operation of the silicon chip in the package. This testing is performed during the unpowered portion of the test (before power is applied to the board), and therefore does not require that a high-fault-coverage ICT model be developed for each I/C, just to check for open solder joints. The method has some limitations. For example, the device must have at least a minimal lead frame, as a signal must be capacitively coupled from the network on the board to a sensor plate in the fixture. Also, a grounded plane, heat spreader, or heat sink above the lead frame will prevent proper operation. Despite these and other limitations, unpowered opens test can be useful for many boards using high performance, high pin count I/C packages.

6.5.4 Functional Test

The GO/NO-GO portion of functional test is typically unaffected by the addition of high performance, high pin count I/C packages, because connection to the test environment is usually made through the product's designed-in interfaces, such as connectors and feature sockets. However, if a board fails the GO/NO-GO test, then it must be manually debugged. The same is true if a board fails ATE test. The following section addresses this manual debug. The same concerns apply if the GO/NO-GO portion of functional test does require manual access, such as when a frequency must be measured and verified.

6.5.5 Manual Access for Debug (at ATE or Functional Test)

In most test strategies, boards that fail at any test step must be debugged and repaired. Some manufacturing defects can be found visually. The through hole mounted array packages and the peripheral packages are easier to inspect visually, since the leads and joints are exposed. The surface mounted array packages pose a much greater problem, because the joints are hidden. Alternative inspection methods may be needed, such as x-ray radiography or x-ray laminography.

Boards that are not repaired after a visual check require manual debug. This is usually performed by a skilled technician, using a digital voltmeter (DVM), an oscilloscope, and possibly a logic analyzer or other instrument. All these devices require physical contact to be made to the networks of the board. Different types of high performance, high pin count I/C packages have different impacts on manual access for debug.

6.5.5.1 Through Hole Mounted Array Packages

Through hole mounted array packages, such as CPGA and PPGA, provide secondary side access for manual probing with scopes, DVMs, or logic analyzers, although the probes must be held, one at a time, against the pins. The pattern of leads must be approached in mirror image, although mirrored pin maps can be created to simplify this. Test leads can also be temporarily soldered to the secondary side pads, to reduce the problem of holding leads in place.

PGAs in sockets can also be adapted with a breakout adapter, that inserts between the package and the socket. This allows hands-free primary side access, for plugging in large numbers of logic analyzer probes. Breakout adapters require a certain amount of space on the board and system to use, but can usually be made to work.

6.5.5.2 Surface Mounted Array Packages

The surface mounted array packages present the same problem for manual debug probing that they do for inspection: the leads (if any) and the joints are obstructed by the device.

This means that the networks involving the package must be manually probed at alternative points. If a network goes to a conventional SMT component, or a THMT component, or a connector, it can be probed there. If not, it must be probed at a via. The via identified as an ATE access point might be used for this purpose. If a map of probe points is created for ATE, it might be very useful for manual debug.

As described earlier, the ATE access point may be a random via used in routing the network, or it may be part of a regular pattern of vias placed near the package, to help

route all its signals away. Standardizing this regular via pattern for each package size and type will help manual debuggers get familiar with the pattern.

6.5.5.3 Peripheral Packages

Peripheral packages, such as PQFPs and CQFPs, have exposed leads that might be usable for manual probing. They are very small and fragile, but an experienced person may be able to probe an individual pin. However, if the probe slips, a short may result, causing damage to the board. Also, it is very difficult to locate the correct lead/pad to probe, since the lead pitch is so small.

Some peripheral packages have available adapters that can be held against one whole side of a device, with test probes attached. These have a comb shape on one side, intended to prevent shorting of adjacent pins.

If leads cannot be safely probed with either of these methods, then alternative points must be found, either on other devices, or at the regular pattern of routing vias, or at random vias, just as they were for surface mounted array packages.

7 DESIGN FOR RELIABILITY (DfR)

The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the developmental phase of the product. There exists a misconception in the industry, that quality manufacturing is all that is required to assure the reliability of an electronic assembly.

While of course, consistent high quality manufacturing—and all that this implies in terms of Design for Manufacturability (DfM), Design for Assembly (DfA), Design for Testability (DfT), etc.—is a necessary prerequisite to assure the reliability of the product, only a Design for Reliability (DfR) can assure that the design—manufactured to good quality—will be reliable in its intended application.

Thus, adherence to quality standards is necessary but not sufficient. For example, solder joint quality in the U.S. is generally measured against criteria in both IPC-A-620, Acceptability of Electronic Assemblies with Surface Mount Technologies, for overall workmanship and ANSI/J-STD-OO1, Requirements for Soldered Electrical and Electronic Assemblies. However, meeting these criteria does not assure reliable solder connections, only quality solder connections.

To clarify the difference between the two requires an explanation and a definition of reliability. Reliability is defined in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, by:

Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

In the short term, reliability is threatened by infant mortality failures due to insufficient product quality; these infant mortalities caused by defects can be eliminated prior to shipping by the use of appropriate screening procedures. Long term failures are the result of premature wear-out damage caused by inadequate designs of the assembly.

It is for this reason that IPC-D-279, Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies, is being developed.

7.1 Damage Mechanisms and Failure of Solder Attachments

The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical thermal, and electrical interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachment, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the printed board and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the printed board.

The characteristics of these three elements—component, substrate, and solder joint—together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

7.1.1 Solder Joints and Attachment Types

Solder joints are anything but a homogeneous structure. A solder joint consists of a number of quite different materials, many of which are only superficially characterized. A solder joint consists of: (1) the base metal at the printed board, (2) one or more intermetallic compounds (IMC)—solid solutions—of a solder constituent—typically tin (Sn)—with the board base metal, (3) a layer from which the solder constituent forming the board-side IMC(s) has been depleted, (4) the solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations, (5) a layer from which the solder constituent forming the component-side IMC(s) has been depleted, (6) one or more IMC layers of a solder constituent with the component base metal, and (7) the base metal at the component.

The grain structure of solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. The

grain growth process is thus an indication of the accumulating fatigue damage. At the grain boundaries contaminants like lead oxides are concentrated; as the grains grow these contaminants are further concentrated at the grain boundaries, weakening these boundaries. After the consumption of ~25% of the fatigue life micro-voids can be found at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks grow and coalesce into macro-cracks leading to total fracture as is schematically shown in figure 7-1.

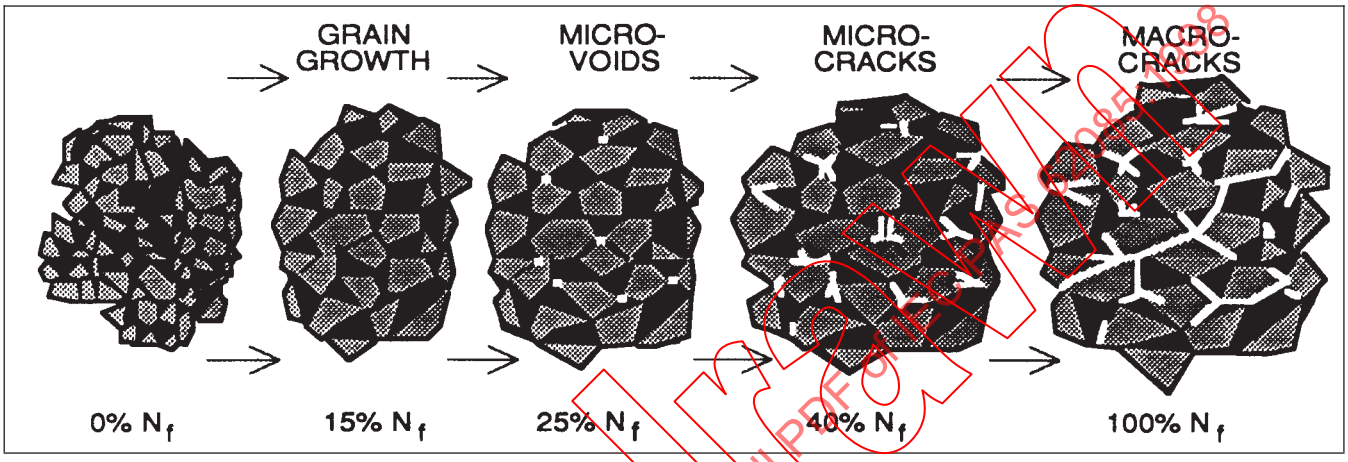


Figure 7−1 Description of the Effects of the Accumulating Fatigue Damage in Solder Joint Structure [Ref. A-2: 1].

Surface mount solder attachments exist in a wide variety of designs. The major categories are leadless and loaded solder attachments. Among the leadless solder joints a differentiation has to be made between those without fillets, e.g., Flip-Chip C4 (Controlled Collapse Chip Connection) solder joints, BGAs with C5 (Controlled Collapse Chip Carrier Connection) solder attachments, BGAs with high-temperature solder (e.g., 10Sn/90Pb) balls, and CGAs with high-temperature solder columns; and solder joints with fillets, e.g., chip components, Metal Electrode Face components (MELFs), and castellated leadless chip carriers. The loaded solder attachments differ primarily in terms of their compliancy and can be roughly categorized into components with super-compliant leads {L_D<~9 N/mm (~50 lb/in)}, compliant leads (~9 N/mm<L_D<~90 N/mm and non-compliant leads {(L_D>~90 N/mm (~500 lb/in)}.

The different surface mount solder attachment types can have significantly different failure modes. Solder joints with essentially uniform load distributions, e.g., Flip-Chip, BGA, CGA, show behavior as illustrated in figure 7-1]. Solder joints with non-uniform load distributions, e.g., those on chips components, MELFs, leadless chip carriers, and all leaded solder joints, show localized damage concentrations with the damage shown in Figure 7-1 preceding an advancing macro-crack.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches [Refs. A-2: 1-6], and are made of a material, solder, that itself has often properties significantly different than the bonding structure materials, causing local thermal expansion mismatches [Refs. A-2:4, 7].

The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment. In table 7-1 guidelines as to the possible use environments for nine of the more common electronic applications are illustrated [Refs. A-2: 8, 9]. However, it needs to be emphasized, that the information in table 7-1 should serve only as a general guideline; for some use categories the description of the expected use environment can be rather more complex [Ref. A-2: 9].

7.1.2 Global Expansion Mismatch

The global expansion mismatches result from differential thermal expansions of an electronic component or connector and the printed board to which it is attached via the surface mount solder joints. These thermal expansion differences result from differences in the CTEs and thermal gradients as the result of thermal energy being dissipated within active components.

Global CTE-mismatches typically range from $\Delta\alpha$~2 ppm/°C (1 ppm=lx10^6) for CTE-tailored high reliability assemblies to ~14 ppm/°C for ceramic components on FR-4 printed boards. CTE-mismatches of $\Delta\alpha$ <2 ppm/~C are not achievable in reality as a consequence of the variability of the CTE values of the materials involved on both components and printed boards.

Global thermal expansion mismatches typically are the largest, since all three parameters determining the thermal expansion mismatch—the CTE-mismatch, $\Delta\alpha$, the temperature swing, ΔT, and the acting distance, L_D—are large.

This global expansion mismatch will cyclically stress, and

Table 7−1 Realistic Representative Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics by Use Categories [Ref. A-2: 10]

	WORST - CASE USE ENVIRONMENT						Accept
Use Category	Tmin °C	Tmax °C	ΔTmax(1) °C	T_D hrs	Cycles/ year	Years of Service	Failure Risk, %
1. Consumer	0	+60	35	12	365	1-3	~1
2. Computers	+15	+60	20	2	1460	~5	~0.1
3. Telecomm	−40	+85	35	12	365	7-20	~0.01
4. Commercial Aircraft	−55	+95	20	12	365	~20	~0.001
5. Industrial & Automotive Passenger Compartment	−55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1
6. Military Ground & Ship	−55	+95	40 &60	12 12	100 265	~5	~0.1
7. Space leo geo	−40	+85	35	1 12	8760 365	5-20	~0.001
8. Military a Avionics b c Maintenance	−55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	~10	~0.01
9. Automotive -Underhood	−55	+125	60 &100 &140	1 1 2	1000 300 40	~5	~0.1

& = in addition

(1) ΔT represents the maximum temperature swing, but does not include power dissipation effects for components; for reliability estimations the actual local temperature swings for components and substrate, including power dissipation should be used.

thus fatigue, the solder joints. The cyclically cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically a corner joint, of the component causing functional electrical failure that is initially intermittent.

7.1.3 Local Expansion Mismatch

The local expansion mismatch results from differential thermal expansions of the solder and the base material of the electronic component or PWB to which it is soldered. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions [Refs. A-2: 4, 7].

Local CTE-mismatches typically range from Δα~7 ppm/°C with copper to ~18 ppm/°C with ceramic and ~20 ppm/°C with Alloy 42 and Kovar™. Local thermal expansion mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller—in the order of hundreds of µm (tens of mils).

7.1.4 Internal Expansion Mismatch

An internal CTE-mismatch of ~6 ppm/°C results from the different CTEs of the Sn-rich and Pb-rich phases of the solder. Internal thermal expansion mismatches typically are the smallest, since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension—in the order of less than 25 µm (<1 mil) [Ref. A-2: 11].

7.1.5 Solder Attachment Failure

The failure of the solder attachment of a component to the substrate to which it is surface mounted is commonly defined as the first complete fracture of any of the solder joints of which the component solder attachment consists.

Given that the loading of the solder joints is typically in shear, rather than in tension, the mechanical failure of a solder joint is not necessarily the same as the electrical failure. Electrically, the mechanical failure of a solder joint results, at least initially, in the occasional occurrence of a short-duration (<1 µs) high-impedance event during either a mechanical or thermal disturbance. From a practical point of view, the solder joint failure is defined as the first observation of such an event.

For some applications this failure definition might be inadequate. For high-speed signals with sharp rise times signal deterioration prior to the complete mechanical failure of a solder joint might require a more stringent failure definition. Similarly, for applications which subject the electronic assemblies to significant mechanical vibration and/or shock loading, a failure definition that considers the mechanical weakening of the solder joints as the result of the accumulating fatigue damage might be necessary.

7.2 Reliability Prediction Modeling

7.2.1 Creep-Fatigue Modeling

It has been experimentally shown [Refs. A-2: 2,4, 12, 13] that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation [Ref. A-2: 14] developed for more typical engineering metals. For practical reasons and as the direct consequence of the time-dependent stress-relaxation/creep behavior of the solder at typical use environments (see table 7-1), the specialized case of the Coffin-Manson equation requires reversion to the more general strain-energy relationship of Morrow [Ref. A-2: 15]; it also requires that the cyclic strain energy be based on the total possible thermal expansion mismatch and that the exponent is a function of temperature and time to provide a measure of the completeness of the stress-relaxation process. The Engelmaier-Wild solder creep-fatigue equation [Refs. A-2: 1-6, 9, 12], subject to some caveats listed later, relates the cyclic visco-plastic strain energy, represented by the cyclic fatigue damage term, AD, to the median cyclic fatigue life for both isothermal-mechanical and thermal cycling [Ref. 16]

$$N_f(50\%) = \frac{1}{2}\left[\frac{2\epsilon'_f}{\Delta D}\right]^{\frac{1}{c}} \qquad \text{[Eq \#1]}$$

where

ϵ'_f = fatigue ductility coefficient, =0.325 for eutectic and 60/40 Sn/Pb solder (for other solders the value of E'_f is expected to be somewhat different).

Solder, uniquely among the commonly used engineering metals, readily creeps and stress-relaxes at normal use temperatures; the rate of creep and stress-relaxation is highly temperature- and stress-level-dependent. Thus, the cyclic fatigue damage term, ΔD, for practical reasons, has to be based on the total potential damage at complete creep/stress relaxation of the solder. For cyclic conditions that do not allow sufficient time for complete stress relaxation ΔD is larger than the actual fatigue damage. The temperature- and time-dependent exponent, c, compensates for the incomplete stress relaxation and is given by

$$c = -0.442 - 6x10^{-4}\,\overline{T}_{S_j} + 1.74x10^{-2}\ln\left(1 + \frac{360}{t_D}\right) \qquad \text{[Eq \#2]}$$

where

T_{S_j} = mean cyclic solder joint temperature

t_D = half-cycle dwell time in minutes.

The half-cycle dwell time relates to the cyclic frequency and the shape of the cycles and represents the time available for the stress-relaxation/creep to take place.

Equations #1 and #2 come from a generic understanding of the response of SM solder joints to cyclically accumulating fatigue damage resulting from shear displacements due to the global thermal expansion mismatches between component and substrate. These shear displacements cause time-independent yielding strains and time-, temperature-, and stress-dependent creep/stress relaxation strains. These strains, on a cyclic basis, form a visco-plastic strain energy hysteresis loop which characterizes the solder joint response to thermal cycling and whose area, given as the damage term ΔD, is indicative of the cyclically accumulating fatigue damage. Hysteresis loops in the shear stress-strain plane have been experimentally obtained [Refs. A-2: 13, 17-19].

7.2.2 Statistical Failure Distribution and Failure Probability

While the physical parameters define the median cyclic fatigue life from physics-of-failure considerations, solder attachment failures for a group of identical components will follow a distribution like all fatigue results which typically is best described by a Weibull statistical distribution [Ref. 20]. Given the statistical distribution, the fatigue life at any given failure probability can be predicted as long as the slope of the Weibull distribution is known. Thus, the fatigue life of surface mount solder attachments at a given acceptable failure probability, x, is —assuming a two-parameter (2P) Weibull statistical distribution—given by

$$N_f(x\%) = N_f(50\%)\left[\frac{1n(1-0.01x)}{1n(0.5)}\right]^{\frac{1}{\beta}} \qquad \text{[Eq \#3]}$$

where

β = Weibull shape parameter or slope of the Weibull probability plot; typically β≈3 for fatigue tests, from low-acceleration tests of stiff leadless solder attachments β≈4 and ≈2 for compliant leaded attachments.

Experimentally, β can be found to be quite variable with more severely accelerated reliability tests resulting in tighter failure distributions and thus giving larger values for β. Values of β in the range of 1.8 to 9.0 have been observed.

There is some, unfortunately as yet inadequate, evidence that for lower failure probabilities a three-parameter (3P) Weibull distribution, postulating a failure-free period prior to first failure [Refs. A-2: 21, 22], may be applicable. From physics-of-failure and damage mechanism considerations, a failure threshold as provided by a 3P-Weibull distribution makes sense, since the fatigue damage in the solder joints has to accumulate to crack initiation and complete crack propagation. While the 2P-Weibull distribution may be overly conservative for designs to very small acceptable failure probabilities (~x<0.1%), a too liberal choice of the failure-free period is definitely non-conservative. This area requires more work.

Also, when designing to low failure probabilities, the variability in the quality of the solder joints may no longer be negligible; also solder joints with latent defects that made it into the field will have in impact on the actual failure experience of a product in the field.

7.2.3 Damage Modeling

The assessment of the cyclically accumulating fatigue damage is not a straight-forward task. While Eq. #1 is widely used, the question of how to best quantify the cyclic fatigue damage is still hotly debated. The choices are primarily between more complex finite-element analyses (FEA), which can give more detailed information and can include second-order effects, but require a large number of not fully-supported assumptions [Ref. A-2: 23]; and closed-form empirically-based relationships of the first-order design parameters, which cannot include second-order effects and have use limitations due to their simple nature, but allow, due to their simple form, a direct assessment of the impact of the primary design parameters as well as design trade-offs.

The following cyclic fatigue damage terms are of the simplified closed-form type and should be utilized with the application caveats that follow [Refs. A-2: 1-6, 9, 12, 16, 24].

The cyclic fatigue damage term for leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength and cause plastic yielding of the solder, is

$$\Delta D(\text{leadless}) = \left[\frac{F L_D \Delta(\alpha\Delta T)}{h}\right]^2 \qquad \text{[Eq \#4]}$$

For solder attachments with leads compliant enough, so that the solder joint stresses are below the yield strength and thus bounded by it, the cyclic fatigue damage term is

$$\Delta D(\text{leaded}) = \left[\frac{F K_D \Delta(\alpha\Delta T)]^2}{(133\ \text{psi})Ah}\right] \qquad \text{[Eq \#5]}$$

where for metric units the scaling coefficient is 919 kPa instead of 133 psi. Equations #4 and #5 contain the design parameters that have a first-order influence on the reliability of SM solder attachments. They are

A = effective minimum load bearing solder joint area;

F = empirical ''non-ideal'' factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, different solder crack propagation distances, brittle IMCs, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. #1 through #5; 1.5>F> l.0 for ball/column-like leadless solder joints (C4, C5, BGAs, CGAs), 1.2>F>0.7 for leadless solder joints with fillets (castellated chip carriers and chip components), F≈1 for solder attachments utilizing compliant leads;

h = solder joint height, for leaded attachments h=½ of solder paste stencil depth as a representative dimension for the average solder thickness;

K_D = ''diagonal'' flexural stiffness of constrained, not soldered, corner-most component lead, determined by strain energy methods [see Refs. A-2: 25-28] or FEA;

L_D = distance between component center and the most remote component solder joint measured from the component solder joint pad center; L_D is sometimes referred to as the distance from the neutral point (DNP); for most packages the most remote component solder joint will experience the most severe cyclic loading, but for packages with non-uniform CTEs, e.g., PBGAs, other solder joints may be most stressed;

T_C, T_S = steady-state operating temperature for component, substrate (T_C>T_S for power dissipation in component) during high temperature dwell;

$T_{C,0}$, $T_{S,O}$ = steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,O}$

$T_{S,O}$; = (1/4)(T_C+T_S+$T_{C,O}$ +$T_{S,O}$), mean cyclic solder joint temperature;

$\alpha_{C,}$ α_S = CTEs for component, substrate;

ΔD = potential cyclic fatigue damage at complete stress relaxation;

ΔT_C = T_C−$T_{C,O}$, cyclic temperature swing for component;

ΔT_S = T_S−$T_{S,O}$, cycling temperature swing for substrate (at component);

$\Delta(\alpha\Delta T)$ = $|\alpha_S\Delta T_S - \alpha_C\Delta T_{C|}$, absolute cyclic expansion mismatch, accounting for the effects of power dissipation within the component as well as temperature variations external to the component;

$\Delta\alpha$ = $|\alpha_C - \alpha_S|$, absolute difference in CTEs of component and substrate, CTE-mismatch, because of the inherent variability in material properties $\Delta\alpha<2\text{x}10^{-6}$ should not be used in calculating reliability.

7.2.4 Caveat 1 — Solder Joint Quality

The solder joint fatigue behavior and the resulting reliability prediction equations, Eqs. #1 through #5, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the IMC layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the 'weakest link' in the surface mount solder attachments. Such layered structures could be: metallization layers that have weak bonds to the underlying base material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing a proper metallurgical bond of the solder to the underlying metal; brittle IMC layers too thick due to too many or improperly long high temperature processing steps.

Some material choices can lead to lower quality and weaker solder joints because the material is more difficult to wet with solder. The nickel/iron alloys, Kovar™ and Alloy 42, fall into this material category. The resulting lower solder joint quality results in solder joint pull strength values for solder joints to Alloy 42 leads that are significantly below those of copper leads. Alloy 42 leads, even when etched or pre-reflowed at temperatures higher than can be tolerated by the component, show a substantial reduction in the solder joint pull strength relative to copper. In the worst instance, the leads from one Alloy 42 manufacturer have a pull strength of less than half of those with more typical Alloy 42 and are essentially non-wettable.

Early failures of the solder attachments of components with Alloy 42 lead frames and leads during accelerated testing [Refs. A-2: 29-33] and manufacture [Ref. A-2: 34] have been documented.

Solder joints which have solder joint heights (gaps) of h<50 to 75µm also require special attention. For solder joints that thin, the gap is essentially filled with intermetallic compounds and those solder metals that do not go into solution with the base metals to form the IMCs. Therefore Eqs. #1 and #2 do not apply because these gaps are not filled with solder [Ref. A-2: 35]. These materials do not creep as readily, if at all, at the prevailing temperatures and are typically more brittle, but much stronger than solder. Thus, fatigue lives are longer than would be predicted from Eqs. #1 and #2 unless overstress conditions occur.

On the other hand, the fatigue lives of solder attachments can be underestimated by Eqs. #1 through #4 if the component is underfilled with a load-bearing substance, e.g., epoxy [Ref. A-2: 36]. Components that are glued-down to the substrate result in higher solder joint fatigue reliability, since the solder joints are loaded in compression when the adhesive contracts on cooling from the solder reflow temperatures. Covercoats can either increase or decrease solder joint fatigue lives depending on the properties of the covercoat and when and how it is applied. Parylene™ has been found to increase the solder joint fatigue life by about a factor of three.

In general, caution might be indicated in all instances where the predicted life is less than 1000 cycles, because the severe loading conditions producing such short lives are likely to produce different damage mechanisms or/and failure modes.

7.2.5 Caveat 2 — Large Temperature Excursions

Solder joints experiencing large temperature swings which extend significantly both below and above the temperature region bounded by −20°C to +20°C, in which the change from stress- to strain-driven solder response takes place, do not follow the damage mechanism described in Eqs. #1 and #2 [Ref. A-2: 37]. The damage mechanism is different than for more typical use conditions and is likely dependent on a combination of creep-fatigue, causing early micro-crack formation, and stress concentrations at these micro-cracks causing faster crack propagation during the high stress cold temperature excursions, as well as recrystallisation considerations.

7.2.6 Caveat 3 — High-Frequency/Low-Temperatures

For high-frequency applications, f>0.5 Hz or t_D<l s, e.g., vibration, and/or low temperature applications, T_C< 0°C, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson [Ref. A-2: 14] fatigue relationship might be more appropriate. This relationship is

$$N_f(50\%) = \frac{1}{2}\left[\frac{2\epsilon_{f'}}{\Delta\gamma_p}\right]^{\frac{1}{c}} \qquad \text{[Eq \#6]}$$

where $\Delta\gamma_p$ is the cyclic plastic strain range and c ≈ −0.6.

It has to be noted, that the determination of $\Delta\gamma_p$ depends on the expansion mismatch displacements and the separation of the plastic from the elastic strains.

For loading conditions of this character, it is possible that high-cycle fatigue behavior may be observed.

7.2.7 CAVEAT 4 — Local Expansion Mismatch

For applications for which the global thermal expansion mismatch is very small, e.g. ceramic-on-ceramic or silicon-on-silicon (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equations #4 and #5 do not address the local thermal expansion mismatch. This reliability problem needs to be assessed using an interfacial stress analysis [Ref. A-2: 38] and appropriate accelerated testing.

Suhir [Ref. A-2: 38] has shown that the interfacial stresses resulting from the local expansion mismatch follow

$$\tau \propto L\,(\alpha_{Solder} - \alpha_{Basr})(T_{max} - T_{min}) \qquad \text{[Eq \#7]}$$

where L is the wetted length of the solder joint. In addition, besides substantial shear stresses at the interface between the solder joint and the base material to which it is wetted, even larger peeling stresses occur. Both of these stresses are proportional to the parameters given in Eq. #7.

However, since in most applications, the local expansion mismatch results in contributory damage to the more important damage caused by the global expansion mismatch, this contra-indication can be ignored without suffering catastrophic consequences.

From the available experimental data, the damage term, to be used in Eq. #1, for the local expansion mismatch alone is

$$\Delta D(\text{local}) = \left[\frac{L\Delta\alpha\Delta T}{L_0}\right] \qquad \text{[Eq \#8]}$$

where the parameters are the same as in Eq. #8 and L_0=0.004 in. (0.1 mm), a scaling wetted length. The local expansion mismatch is then treated as an additional loading condition (see 7.2.10 & 7.2.11).

7.2.8 Caveat 5 — Very Stiff Leads

Equations #4 and #5 differentiate between surface mount solder attachments that are leadless and those with compliant leads. Leadless solder attachments presume substantial plastic strains due to yielding prior to creep and stress relaxation. Equation #5 assumes that the compliant leads prevent stresses in the solder joints to reach levels where substantial yielding, and thus plastic strains prior to creep and stress relaxation, can take place.

For very stiff, non-compliant leads (e.g., SM connector headers, through-hole components converted to SM components), perhaps at lead stiffness K_D>~90 N/mm (~500 lb/in), the stress calculated in Eq. #5 can exceed the yield strength of the solder. Since yielding will not permit stresses significantly higher than the yield strength, these calculated stress ranges will overestimate the cyclic fatigue damage and thus result in substantially underpredicted fatigue lives. To prevent this analytical error, the stress range in Eq. #5 needs to be bounded by the yield strength of solder in shear.

Under these circumstances, Eqs. #4 and #5 will provide lower and upper bounds for the reliability estimates, respectively. The higher the lead stiffness, the closer the expected results will be towards the results given by Eq. #4 for the leadless—'infinitely stiff leads'—solder attachments.

7.2.9 Caveat 6 — Very Soft Leads/Very Large Expansion Mismatches

Equation #5 also assumes that the compliant leads will store the thermal expansion mismatches as elastic strain energy, but will not plastically deform thermselves; thus, all the thermal expansion mismatch is assumed to result in loading of the solder joints.

The loading conditions resulting from the plastic deformation of the leads, either because they are very soft and/or the thermal expansion mismatch is large, are not covered by these assumptions. For very soft, highly-compliant leads (e.g., QFPs) and/or for very large thermal expansion mismatches (e.g., ceramic MCMs on FR-4) resulting in strain ranges $\Delta\gamma$>~10%, the damage estimates in Eq. #5 can be substantially in error, because the assumptions underlying Eq. #5 are violated.

Under these circumstances, the full displacements will not be transmitted to the solder joints, because the leads will accommodate displacements by plastic deformations of the lead material. The strain range that can be accommodated by creep and stress relaxation in the solder joints can be significantly exceeded by the displacements resulting from very large thermal expansion mismatches and the cyclic fatigue damage would be significantly overestimated. Under these conditions FEA is required to determine the split in the accommodation of the displacements between the lead and the solder joint.

Very high thermal expansion mismatches occur primarily in accelerated testing and in extraordinary environments like storage and transport for products that are designed for benign operating environments.

7.2.10 Multiple Cyclic Load Histories

The loading histories over the life of a product frequently include many different use environments and loading conditions [Refs. A-2: 39, 40]. Multiple cyclic load histories (e.g., "Cold" temperature fatigue cycles combined with higher temperature creep/fatigue cycles (see table 7-1) combined with vibration and local expansion mismatches) all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative—this assumption underlies Eqs. #1 and #2 as well—and that the simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule [Ref. A-2: 41] can be applied.

Frequently the initial reliability objective is stated as an allowable net cumulative damage ratio (CDR). The CDR is calculated as the sum of the ratios of the number of occurring load cycles to the fatigue life at each loading condition and is:

$$CDR = \sum_{j=1}^{j} \frac{N_j}{N_{fj}} < 1 \qquad \text{[Eq \#9]}$$