IEC/IEEE 62659

Edition 1.0 2015-09

INTERNATIONAL STANDARD

Nanomanufacturing – Large scale manufacturing for nanoelectronics

IEC/IEEE 62659:2015-09(en)

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue
New York, NY 10016-5997
United States of America
stds.ipr@ieee.org
www.ieee.org

About the IEC
The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About the IEEE
IEEE is the world's largest professional association dedicated to advancing technological innovation and excellence for the benefit of humanity. IEEE and its members inspire a global community through its highly cited publications, conferences, technology standards, and professional and educational activities.

About IEC/IEEE publications
The technical content of IEC/IEEE publications is kept under constant review by the IEC and IEEE. Please make sure that you have the latest edition, a corrigendum or an amendment might have been published.

IEC Catalogue - webstore.iec.ch/catalogue
The stand-alone application for consulting the entire bibliographical information on IEC International Standards, Technical Specifications, Technical Reports and other documents. Available for PC, Mac OS, Android Tablets and iPad.

IEC publications search - www.iec.ch/searchpub
The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,…). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished
Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and also once a month by email.

Electropedia - www.electropedia.org
The world's leading online dictionary of electronic and electrical terms containing more than 30 000 terms and definitions in English and French, with equivalent terms in 15 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IEC Glossary - std.iec.ch/glossary
More than 60 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

IEC Customer Service Centre - webstore.iec.ch/csc
If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: csc@iec.ch.

IEC/IEEE 62659

Edition 1.0 2015-09

INTERNATIONAL STANDARD

Nanomanufacturing – Large scale manufacturing for nanoelectronics

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 07.030; 25.020

ISBN 978-2-8322-2915-6

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

_____

NANOMANUFACTURING – LARGE SCALE MANUFACTURING FOR NANOELECTRONICS

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation.

   IEEE Standards documents are developed within IEEE Societies and Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. IEEE develops its standards through a consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of IEEE and serve without compensation. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards. Use of IEEE Standards documents is wholly voluntary. IEEE documents are made available for use subject to important notices and legal disclaimers (see http://standards.ieee.org/IPR/disclaimers.html for more information).

   IEC collaborates closely with IEEE in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees. The formal decisions of IEEE on technical matters, once consensus within IEEE Societies and Standards Coordinating Committees has been reached, is determined by a balanced ballot of materially interested parties who indicate interest in reviewing the proposed standard. Final approval of the IEEE standards document is given by the IEEE Standards Association (IEEE-SA) Standards Board.

3) IEC/IEEE Publications have the form of recommendations for international use and are accepted by IEC National Committees/IEEE Societies in that sense. While all reasonable efforts are made to ensure that the technical content of IEC/IEEE Publications is accurate, IEC or IEEE cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.

4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications (including IEC/IEEE Publications) transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC/IEEE Publication and the corresponding national or regional publication shall be clearly indicated in the latter.

5) IEC and IEEE do not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC and IEEE are not responsible for any services carried out by independent certification bodies.

6) All users should ensure that they have the latest edition of this publication.

7) No liability shall attach to IEC or IEEE or their directors, employees, servants or agents including individual experts and members of technical committees and IEC National Committees, or volunteers of IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board, for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC/IEEE Publication or any other IEC or IEEE Publications.

8) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.

9) Attention is drawn to the possibility that implementation of this IEC/IEEE Publication may require use of material covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. IEC or IEEE shall not be held responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patent Claims or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility.

International Standard IEC/IEEE 62659 has been prepared by IEC technical committee 113, Nanotechnology standardization for electrical and electronic products and systems, in cooperation with the Standards Committee of the IEEE Nanotechnology Council[1], under the IEC/IEEE Dual Logo Agreement.

The text of this standard is based on the following documents:

FDIS	Report on voting
113/271/FDIS	113/280/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The IEC Technical Committee and IEEE Technical Committee have decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

[1] A list of IEEE participants can be found at the following URL: http://standards.ieee.org/downloads/62659/62659-2015/62659-2015_wg-participants.pdf

INTRODUCTION

In order to fully benefit from the cost, performance, and flexibility of new electronics products manufactured on a large-scale, industries accustomed to the purchase, use, and engineering of continuum materials need to grow to embrace appropriate new practices at the nanoscale. The purpose of this International Standard is to enable the quick, low-risk adoption of nanomaterials into large-scale electronics manufacturing. In addition a best set of common practices for use by semiconductor fabricators will be delineated.

The description of nanomaterials to be incorporated into the electronics process can be described in terms of: composition (material), density, purity, size/dimensions, properties such as electrical characteristics (conductive, non-conductive, and semiconductive), associated media (delivery medium), fabrication, surface functionalization, particle size distribution, surface area, shape, and degree of aggregation and agglomeration, etc.

These standards for the characterization of nanomaterials also provide an opportunity to help ensure consistency in metrics and measurement methods when specifying or producing nanomaterials for electronics applications. This is important when multiple vendors or technology partners are involved.

NANOMANUFACTURING – LARGE SCALE MANUFACTURING FOR NANOELECTRONICS

1 Scope

This International Standard provides a framework for introducing nanoelectronics into large scale, high volume production in semiconductor manufacturing facilities through the incorporation of nanomaterials (e.g. carbon nanotubes, graphene, quantum dots, etc.). Since semiconductor manufacturing facilities need to incorporate practices that maintain high yields, there are very strict requirements for how manufacturing is performed. Nanomaterials represent a potential contaminant in semiconductor manufacturing facilities and need to be introduced in a structured and methodical way.

This International Standard provides steps employed to facilitate the introduction of nanomaterials into the semiconductor manufacturing facilities. This sequence is described below under the areas of raw materials acquisition, materials processing, design, IC fabrication, testing, and end-use. These activities represent the major stages of the supply chain in semiconductor manufacturing facilities.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

None.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
nanoscale
size range from approximately 1 nm to 100 nm

Note 1 to entry: Properties that are not extrapolations from a larger size will typically, but not exclusively, be exhibited in this size range. For such properties the size limits are considered approximate.

Note 2 to entry: The lower limit in this definition (approximately 1 nm) is introduced to avoid single and small groups of atoms from being designated as nano-objects or elements of nanostructures, which might be implied by the absence of a lower limit.

[SOURCE: ISO/TS 80004-1:2010, 2.1]

3.2
nanotechnology
application of scientific knowledge to manipulate and control matter in the **nanoscale** (3.1) in order to make use of size- and structure-dependent properties and phenomena, as distinct from those associated with individual atoms or molecules or with bulk materials

Note 1 to entry: Manipulation and control includes material synthesis.

[SOURCE: ISO/TS 80004-1:2010, 2.3]

3.3
nanoelectronics
electronic devices that incorporate **nanoscale** (3.1) materials, processes and properties

3.4
nanomanufacturing
intentional synthesis, generation or control of **nanomaterials** (3.6), or fabrication steps in the **nanoscale** (3.1), for commercial purposes

[SOURCE: ISO/TS 80004-1:2010, 2.11]

3.4.1
bottom-up nanomanufacturing
processes that use small fundamental units to create larger functionally rich structures or assemblies

3.4.2
hybrid nanomanufacturing
combination of additive and subtractive controlled processing to create an intentional nanoscaled structure

3.4.3
top-down nanomanufacturing
processes that create structures at the nanoscale from macroscopic designs

3.5
nanomanufacturing process
ensemble of activities to intentionally synthesize, generate or control **nanomaterials** (3.6), or fabrication steps in the **nanoscale** (3.1)

[SOURCE: ISO/TS 80004-1:2010, 2.12]

3.6
nanomaterial
material with any external dimension in the nanoscale or having internal or surface structure in the **nanoscale** (3.1)

Note 1 to entry: This generic term is inclusive of nano-object and nanostructured material.

[SOURCE: ISO/TS 80004-1:2010, 2.4]

3.7
nano-object
material with one, two or three external dimensions in the **nanoscale** (3.1)

Note 1 to entry: Generic term for all discrete nanoscale objects.

[SOURCE: ISO/TS 80004-1:2010, 2.5]

3.8
nanostructure
composition of inter-related constituent parts, in which one or more of those parts is a **nanoscale** (3.1) region

Note 1 to entry: A region is defined by a boundary representing a discontinuity in properties.

[SOURCE: ISO/TS 80004-1:2010, 2.6]

3.9
nanofibre
nano-object (3.7) with two similar external dimensions in the **nanoscale** (3.1) and the third dimension significantly larger

Note 1 to entry: A nanofibre can be flexible or rigid.

Note 2 to entry: The two similar external dimensions are considered to differ in size by less than three times and the significantly larger external dimension is considered to differ from the other two by more than three times.

Note 3 to entry: The largest external dimension is not necessarily in the nanoscale.

[SOURCE: ISO/TS 27687:2008, 4.3]

3.10
nanoparticle
nano-object (3.7) with all three external dimensions in the **nanoscale** (3.1)

Note 1 to entry: If the lengths of the longest to the shortest axes of the nano-object differ significantly (typically by more than three times), the terms nanofibre or nanoplate are intended to be used instead of the term nanoparticle.

[SOURCE: ISO/TS 27687:2008, 4.1]

3.11
nanowire
electrically conducting or semi-conducting **nanofibre** (3.9)

[SOURCE: ISO/TS 27687:2008, 4.6]

3.12
nanosheet
freestanding nanofilm

3.13
graphene
single layer of carbon atoms with each atom bound to three neighbours in a honeycomb structure

Note 1 to entry: It is an important building block of many carbon nano-objects.

[SOURCE: ISO/TS 80004-3:2010, 2.11]

3.14
nanotube
hollow **nanofibre** (3.9)

[SOURCE: ISO/TS 27687-2008, 4.4]

3.15
nanorod
solid **nanofibre** (3.9)

[SOURCE: ISO/TS 27687-2008, 4.5]

4 Abbreviations

The following abbreviations are used in this standard:

CNT – Carbon nanotube

HDL – Hardware description language

ATE – Automatic test equipment

5 Nanomaterials incorporation into electronics fabrication

5.1 General

Nanomanufacturing processes follow three general methods of production: bottom-up nanomanufacturing, top-down manufacturing and a hybrid version of these two methods, each based on the location of the initiating material. See Figure 1.

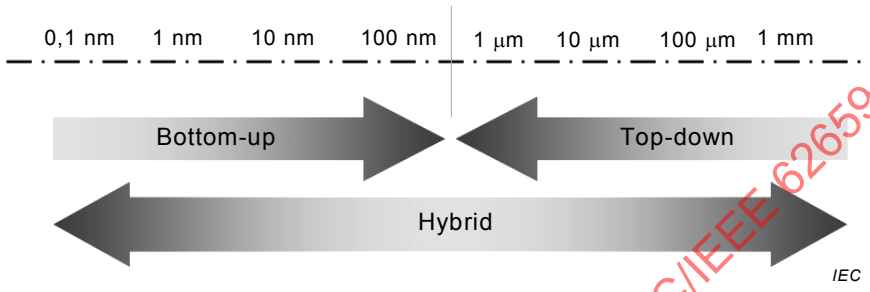

Figure 1 – Relationship between bottom-up, top-down and hybrid device fabrication processes for nanoelectronics over length scales

Tables 1 and 2 describe representative workflows for the creation of nanoelectronics within the two most common manufacturing processes. Incorporation of nanomaterials into electronics fabrication may utilize a hybrid process in which creation of nanoelectronics employs a combination of elements of both of these workflows.

Table 1 – Bottom-up process for nanoelectronics

Workflow	Processing
Desired pattern defined using lithographic technique	Desired pattern developed in seed planting software tool to produce the seed positions
Functionalized surface	Seed layer is produced on substrate layer
Functional surface generation and growth	The desired pattern described by functional surface allows seeds to grow and assemble. Additive raw material grown from functionalized surface
Completed pattern	Finished device

Table 2 – Top-down process for nanoelectronics

Workflow	Activity
Raw material coating of substrate	Material added to substrate
Desired pattern defined using lithographic technique	Desired pattern developed
Pattern etched	The desired pattern described by lithographic process and excess material selectively removed; patterning and etching repeated as necessary
Completed pattern	Finished device

A workflow for nanomaterials incorporation into electronics fabrication is highlighted in Table 3, comparing a CNT electronics workflow to that of a CMOS workflow.

Table 3 – Comparison of CMOS processes with exemplary CNT electronics process

Workflow	CNT electronics	Si CMOS electronics
Raw materials acquisition	CNT in grams	Wolframite/Sheelite (Tungsten ore) in metric tonnes
Materials processing	CNT in 1 L or 4 L aqueous solutions	150 mm, 200 mm or 300 mm W targets for sputter deposition
Design	Full custom layout;	Multi-core microprocessor synthesized from HDL;
IC fabrication	0,15 µm CMOS line	45 nm, 200 mm wafer Si CMOS foundry
Testing	Semi-automatic wafer probe stations	High throughput ATE
End-use	Solid-state data recorder module	Mainboard with chipset for notebook computers

The primary areas for elucidation to move from start to product include: raw materials, processed materials, IC fabrication processes, design and test and end-user systems. Each area has specific requirements and function which has dependencies based upon the end-user system requirements. This document will provide a framework for the elucidation of generic approaches to describe these systems with the goal to coalesce with other standards activities wherever a common thread or shared methodology can be exploited.

5.2 Raw materials acquisition

Raw materials use for nanoelectronics at the large scale falls into four primary categories: nanoparticles, nanowires, nanotubes and nanosheets, which may include zero-dimensional nanomaterials, one-dimensional nanomaterials, two-dimensional nanomaterials or three-dimensional nanomaterials, either separately or in combination or as a mixture. Nanotubes are distinct from nanowires because of the hollow nature of a tubular structural motif versus the solid form of a wire. Several IEC and IEEE efforts, for example IEC 62624/IEEE Std 1650 and IEC PAS 62565-2-1, have focused on delineation of various aspects of nanotube generation and description. Those efforts will be incorporated as references for this effort.

Some of the key features of raw carbon nanotube materials examination include sourcing, growth conditions including gas control, temperature control, substrate choice and control, diameter (and chirality) control, length control, surface functionalization, contamination measurement from catalysts in the case of nanotubes and additional carbon contamination as well. These are detailed in IEC PAS 62565-2-1.

In the case of nanoparticles the synthesis methodologies are quite diverse and the focus will be on monodispersity, composition control, surface functionalization and contamination.

In the case of nanowires, the synthesis will focus on methods which specify gas concentrations, temperature control, substrate choices, diameter control, length control, surface functionalization and contamination. All of these raw materials generation methodologies require close examination of safety conditions during growth, harvesting safety and waste stream handling and monitoring. IEC PAS 62565-1 shall be the model for the future nanowire blank detail specification.

In the case of nanosheets, the synthesis will focus on providing monatomically layered carbon atoms with a specified stacking of one or more layers. Controlled growth will focus on methods which specify gas concentrations, temperature control, substrate choices, and contamination.