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Format for LSI-Package-Board Interoperable design –

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2401 (2019)	91/1869/FDIS	91/1887/RVD

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IEEE Standard Format for LSI-Package-Board Interoperable Design

Developed by the

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 7 November 2019

IEEE SA Standards Board

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Abstract: A method is provided for specifying a common interoperable format for electronic systems design. The format provides a common way to specify information/data about the project management, netlists, components, design rules, and geometries used in the large-scale integration-package-board designs. The method provides the ability to make electronic systems a key consideration early in the design process; design tools can use it to seamlessly exchange information/data.

Keywords: common interoperable format, components, design analysis, design rules, geometries, IEEE 2401™, large-scale integration (LSI), netlists, packages for LSI circuits, printed circuit board, project management, Verilog-HDL

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IEEE Introduction

This introduction is not part of IEEE Std 2401-2019, IEEE Standard Format for LSI-Package-Board Interoperable Design.

To deal with the increasing difficulty of design and the cost competitiveness of the global market, and to shorten the development term, innovative design methodologies should be implemented. It has been difficult to achieve the optimization of an entire set of large-scale integration (LSI), package, and board (LPB) using individual design processes for each LPB part.

One possibility for optimization is to have a certain section design the whole LPB; however, gathering knowledge and integrating the design environment of each LPB part is difficult. Dedicated professional technicians of individual LPB parts, who have the best knowledge and performance of their own part's design tools, intend to create design optimization by having proper interoperable information exchanges among all LPB parties. In order to achieve a design that optimizes the balance between cost and performance, information about and the results of design should be well shared among cooperating LPB design sections.

The standard format of LSI package board interoperable design (hereinafter called *LPB Format*) was developed to make it easier to exchange information among LPB design departments, so that optimal design will be carried out quickly.

The LPB interoperable design process has the following issues:

- Netlist not unified on each LPB
- Complexity of the representation of the relationship as a whole arrangement of the LPB
- Differences in how to give the design constraints, lack of design information, and many discrepancies in design rules
- Databases not unified in each LPB, or among different vendors
- No unified terms

Various problems caused by these issues include the following:

- A large effort is required for conversion of formats.
- The occurrence of conversion errors and connection errors is difficult to detect because there is a lack of the information needed to do so.
- It takes a long time to gather information, resulting in a long period of design and analysis.
- It is difficult to make optimal design changes because the entire verification process is difficult.
- Electronic design automation (EDA) tool cost increase because of additional development required to support multiple formats.
- It is time consuming for designers to communicate their intentions in a way that others understand.

Based on this analysis, the interface LPB Format has been developed which can address these issues.

As the one of the case studies of the LPB interoperable design process, the power distribution network (PDN) should be designed with information about the other LPB parts to reduce the noise (see Figure i).

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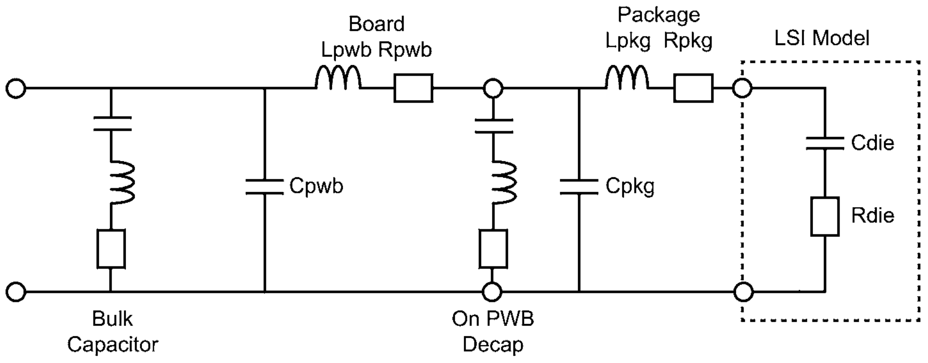

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Figure i—Power distribution network

Resonance is caused by a capacitance and inductance present in the various parts in the LPB PDN. Impedance at the resonant frequency will be extremely large. If each part of the overall LPB design is not accurately simulated in the PDN model, the power supply circuit cannot be correctly designed (see Figure ii).

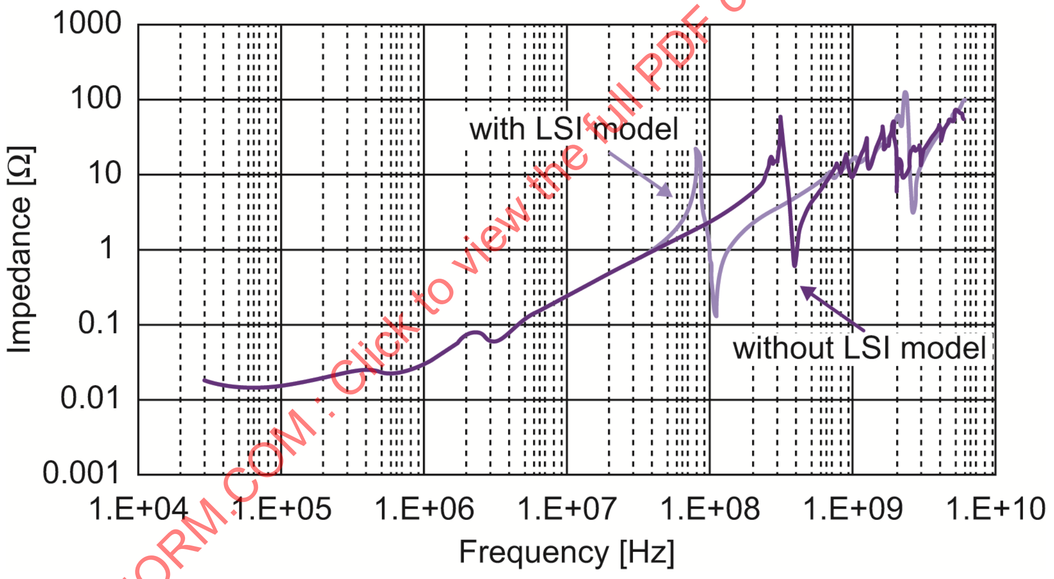

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Figure ii—Example of PDN impedance

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In order to run properly, this simulation should align a variety of information, such as the circuit model of power distribution network (PDN) of LSI, shape information about the package and board, electrical parameters of materials, and models of the components. It is difficult to make an efficient design when the specification or format of the design information is different in each part of the LPB, and the necessary parameters are not shared. When the format of the interface methods and models of the simulation are not consistent, the setup time and the cost of design/verification are enormous, which has become a barrier to cooperation in LPB design. The LPB Format will be evolved to create a mutual interface to enable a more efficient co-design environment.

IEEE Standard Format for LSI-Package-Board Interoperable Design

1. Overview

1.1 Scope

This standard defines a common interoperable format that will be used for the design of a) large-scale integration (LSI), b) packages for such LSI, and c) printed circuit boards on which the packaged LSIs are interconnected. Collectively, such designs are referred to as *LSI-Package-Board (LPB)* designs. The format provides a common way to specify information/data about the project management, netlists, components, design rules, and geometries used in LPB designs.

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1.2 Purpose

The general purpose of this standard is to develop a common format that LPB design tools can use to exchange information/data seamlessly, as opposed to having to work with multiple different input and output formats.

1.3 Key characteristics of the LSI-Package-Board Format

The LPB Format will facilitate the exchange of design information. This functionality provides the ability to plan the entire design at an early stage. In effect, post-design analysis will be possible throughout the entire LPB design process. Analysis of each part of the design can be examined in relation to all other parts of the design to determine the optimal point to give feedback for appropriate design changes throughout the LPB. This will promote the overall optimization of the design process.

The LPB Format is constructed out of the following five formats (see Figure 1):

a) Project Management (M-Format)

b) Netlist (N-Format)

c) Component (C-Format)

d) Design Rule (R-Format)

e) Geometry (G-Format)

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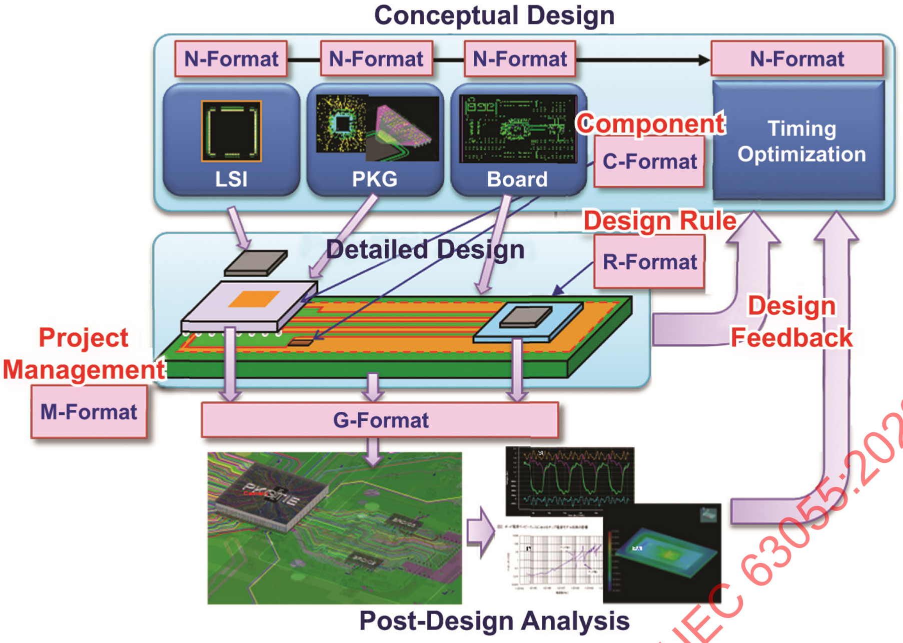

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Figure 1—LPB Format

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Design time can be shortened by using the LPB Format. Traditionally, design starts immediately after separate planning for each individual component of the LPB. Therefore, information exchange among the separate design processes is limited. Trying to adjust the detailed design of one component to the detailed design of another component makes the entire design period take longer. Optimization also tends to be a separate process for each component of the LPB. By using the LPB Format for distributed information, each LPB engineer will be able to have the same understanding of the challenges at an early stage. As a result, adjustments at the conceptual design stage can be made, before detailed designs are developed. By making clear the overall LPB product specifications, the design target can be decided, and so the duration of individual designs can be shortened. Use of the LPB Format also helps to reduce the number of design iterations, because the design quality is enhanced. The designers can collect all information for simulation using the LPB formats, thereby reducing production time. The LPB Format can enable the entire analysis easily, so that sufficient verification can be done and the quality of the products can be improved. As a result, the period of adjustment in the set can be shortened and the time to market can be accelerated. With the LPB Format, the design method for one product can be applied to the design environment for next product in development.

1.4 Contents of this standard

The organization of the remainder of this standard is as follows:

- Clause 2 provides references to other applicable standards that are presumed or required for this standard.
- Clause 3 defines terms and acronyms used throughout the different specifications contained in this standard.
- Clause 4 describes the concepts of the LPB Format.
- Clause 5 describes the language basics for the LPB Format and its commands.
- Clause 6 describes common elements in the M-Format, C-Format, and R-Format.

- Clause 7 describes the M-Format.
- Clause 8 describes the C-Format.
- Clause 9 describes the R-Format.
- Clause 10 describes the N-Format.
- Clause 11 describes the G-Format.

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IEEE Std 1364™, IEEE Standard for Verilog® Hardware Description Language.[3, 4]

3. Definitions, acronyms, and abbreviations

3.1 Definitions

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antipad: The clearance **hole** between a **via** and a no-connect metal layer, mainly used on the printed circuit **board** and large-scale integration (LSI) **package**. The shape of the antipad is mainly determined by the limit on the printed circuit board or LSI package manufacturing and is defined by the **padstack** in the R-Format file.

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ball: *See:* **solder ball**.

ball grid array (BGA) package: A type of surface-mount **package** with one face covered (or partly covered) with **solder balls** arranged in a grid pattern.

board: The printed circuit board or printed wiring board.

bonding finger: The metal electrode on the surface of an large-scale integration (LSI) **package**. It connects the **bonding wire** to the routing pattern on the LSI package. In LSI-Package-Board (LPB) Format files, the shape of the bonding finger is defined by the **padstack** in the C-Format file.

bonding wire: A metal wire for connecting the **die** and **bonding finger**. In large-scale-integration-Package-Board (LPB) Format files, the shape of the bonding wire is defined in the R-Format file.

clock: The signal used in a synchronous circuit. All synchronous circuits use a clock signal to synchronize different parts of the circuit. In most cases, the part is register or flip-flop. The clock is distributed from a single source to registers or flip-flops and is required to arrive at all such parts at the same time.

common mode impedance: The impedance of a single transmission line when the two lines in a pair are driven with signals of the same amplitude and same polarity. Common (even) and differential (odd) modes are the two main modes of propagation of the signal through a coupled line pair.

component: A physical and logical construction having inputs to outputs. Large-scale integration (LSI) package or die and passive parts such as capacitors and connectors are called components.

component hole: A **hole** used for the attachment of component terminations to the printed **board** as well as for any electrical connection to the conductive pattern. *See also:* **hole**.

delay: The time interval between a step function change of the input signal level and the instant at which the magnitude of the output signal passes through a specified value that is close to its initial value. The switching time of the transistor and the propagation time of the signal through wiring.

die: A separated part (or whole) of a wafer intended to perform a function or functions in a device. A small block of semiconducting material, on which a given functional circuit is fabricated.

differential mode impedance: The impedance of a single transmission line when the two lines in a pair are driven with signals of the same amplitude and opposite polarity. Common (even) and differential (odd) modes are the two main modes of propagation of the signal through a coupled line pair.

differential signal: Differential signaling. A method of transmitting information electrically with two complementary signals sent on two paired wires, called a *differential pair*.

drill: The drill to be used when drilling the **via** hole connecting the layers of a multilayer printed circuit **board**.

driver: *See:* **sender**.

finger: *See:* **bonding finger**.

flipchip: A die that is flipped over so that its metal wiring faces down in order to mount the die to external circuitry (e.g., a circuit board or another chip or wafer).

flipchip pad: The contact pad of the **flipchip** surface.

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guard shield: A barrier or enclosure provided for mechanical protection, which may also have the function of a screen, called a *GND shield* when put on a ground (GND) conductor. Its purpose is to limit the electromagnetic interference from other signals.

hole: Used for the conductive connection between each layers and for mounting components. *See also:* **component hole**, **landless hole**, **mounting hole**, **plated-through hole**, and **via hole**.

inout: A **port** having the function of both input and output. It is an input port where electromagnetic energy or signals may be received from an external circuit or device. It is an output port where electromagnetic energy or signals may be supplied to an external circuit or device.

land: The conductive pattern used for joining and connecting parts, the conductive pattern for surface mount pads and hole-mounted components, and the conductive pattern that covers a via hole.

landless hole: A **plated-through hole** without **land**. *See also:* **hole**.

line: A device connecting two points for the purpose of conveying electromagnetic energy between them. Electromagnetic energy may be extracted from or supplied to a line at an intermediate point. Examples of lines are two-wire line, polygon line, coaxial line, and waveguide.

mounting hole: A **hole** used for the mechanical mounting of a printed **board** or for mechanical attachment of components to the printed board. *See also:* **hole**.

net: The relative position of the ideal elements representing an electric network. The label in between interconnection of terminals. Although it is defined on the same hierarchy, there are also cases that indicate the connection regardless of hierarchy (for example, global net definition).

package: An enclosure for one or more die, film elements, or other components, that allows electrical connection and provides mechanical and environmental protection. Types of packages include quad flat package (QFP), ball-grid array (BGA), wafer-level chip-scale package (WLCSP), multi-chip module (MCM), package on package (PoP), etc.

package mold: Protection of die by resin against stress, external force, water, static electricity, and foreign substances. A package mold contains resin, silica, carbon, and flame-retardant material.

package substrate: The same as that of a printed circuit board. It carries large-scale integration (LSI) and electrically connects **solder balls** with LSI.

pad: A metal electrode on the surface of a die, large-scale integration (LSI) package, or printed circuit **board**.

padstack: The combination of layers that constitute a **pad**.

physical design rule: A series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.

pin: A contact element intended to make electric engagement on its outer surface for mating with the inner surface of another contact element.

plated-through hole: A **hole** in which metal is deposited on the wall. *See also:* **hole**.

port: Access point or points to a module where signals may be supplied or received. The port may be physical, or conceptual as in circuit nodes.

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power domain: A collection of instances that are treated as a group for power-management purposes. The instances of a power domain typically, but do not always, share a primary supply set. A power domain may also have additional supplies, including retention and isolation supplies.

receiver: A device that receives signals for interpretation and action.

reference point: A location with respect to which the dimension coordinates and placement of a shape are fixed.

sender: A device that generates and terminates signals. *Syn:* **driver**.

single-ended signal: A signal used for single-ended signaling, which is the method of transmitting signals over electrical connections. One electrical connection carries a varying voltage that represents the signal.

skew: A variation of a delay time by propagation of a signal, or an amount of gaps of the delay time between a reference signal and an object signal.

solder ball: A spherical solder that is used in the large-scale integration (LSI) package of a **ball grid array (BGA)** type and provides the contact between the **package** and the printed circuit **board**. The **pins** of the BGA package are placed in a grid pattern. Balls are mounted on each pin and used to solder the BGA to the printed circuit board. The internal circuit in a BGA exchanges signals and power with an external circuit on a printed circuit board through the ball. The shape of the ball is defined in the R-Format file.

stacked via: A structure that places a **via** on another via. *See also:* **via**.

sub-circuit: A sub-circuit expresses a specific circuit as one unit.

terminator: A device fitted to the end of a cable to ensure electrical connection with other parts of the system and to maintain the insulation up to the point of connection.

typ: An abbreviation of “typical,” used to express a representative or standard value.

via: One of the conductive parts forming a contact in between layers.

via hole: The conduction connectivity made through a **hole** in between layers. *See also:* **hole**.

void: A **hole** or cutout on a plane.

3.2 Acronyms and abbreviations

ACIS	A generic 3D modeling kernel developed by Spatial Corporation
ASCII	American Standard Code for Information Interchange
BGA	ball grid array
CPIP	Chip-Package Interface Protocol
dc	direct current
DDR	double data rate
DDR-SDRAM	double data rate synchronous dynamic random-access memory

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DEF	Design Exchange Format
DXF	Drawing Exchange Format
EDA	electronic design automation
EMI	electromagnetic interference
GDS (GDS II)	Graphic Database System
GND	ground
HDL	hardware description language
IBIS	Input/output Buffer Information Specification
IBIS-ISS	IBIS Interconnect SPICE Subcircuit
IC	integrated circuit
ICEM	integrated circuit emission model
ICIM	integrated circuit immunity model
IEC	International Electrotechnical Commission
IGES	Initial Graphics Exchange Specification
I/O	input output
JEDEC	Joint Electron Device Engineering Council
JEITA	Japan Electronics and Information Technology Industries Association
JTAM	Japan Electronics and Information Technology Industries Association (JEITA) Thermal Accurate Model
LPB	LSI, package, and board; LSI-Package-Board
LSI	large-scale integration
MD5	message digest algorithm 5
NG	no good
PCB	printed-circuit-board (adjective)
PCIe	Peripheral Component Interconnect Express
PI	power integrity
PKG	package
PKI	public key infrastructure

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POP, PoP	package on package
PWB	printed wiring board
RMS	root mean square
SAT	Standard ACIS Text file
Si2	Silicon Integration Initiative
SI	signal integrity
SMA	subminiature version A
SMD	surface mount device
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
STEP	Standard for the Exchange of Product model data
URI	Uniform Resource Identifier
VHDL	Very High Speed Integrated Circuits Hardware Description Language
XML	Extensible Markup Language
Xtal	crystal

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4. Concept of the LPB Format

4.1 Technical background

The design margin for timing and noise is decreasing due to the higher speed of systems and the low voltage of the interface and power supply. Also, balancing design for both cost and performance is increasingly becoming important for cost competitiveness. In a conventional design, the large-scale integration (LSI), package and board (LPB) are designed with margin in accordance with individual design guidelines. However, it becomes difficult to provide design guidelines for each LPB part separately with the decreased design margin. Therefore, deciding the design target needs the cooperation of the designers of each part of the LPB. In other words, the innovation of deciding design guidelines by using simulation technology is needed in the system design process. To perform this task, a rapid and accurate simulation environment is necessary.

4.2 Conventional design

In conventional design, LPB design and sign-off analysis were performed for each design criterion. In other words, only partial optimization was done, so whole-system optimization and analysis was not performed at the initial design stage. The result was a lack of observation of physical phenomena throughout the whole system, appropriate design changes on each design site separately, and excessive estimation for design margin. These significantly influenced the quality and cost of the final product.

4.3 Common problems at the design site

4.3.1 Misunderstanding among designers

Misunderstanding among designers can occur when different designers perceive the same word to have different meanings, designers use the different words to describe the same phenomenon, and designers have different subjectivities, such as viewing the design from the top or bottom. These cases occur even if designers are in the same office, with the result that many designers have a bitter experience.

4.3.2 Lack of information for system design

Limitations and design margins among the LSI, package, and board may not be assumed at the time of the design of the individual components. Also, designers may face big obstacles after connecting individual components because they are uncertain about the limitations and margins of the others. For example, designing the package or board (wiring) will be difficult because of lack of information about the LSI pad assignment, the package ball assignment, and the part location on the board.

4.3.3 Waste of time that should be used for design

Because input and output formats are different for each electronic design automation (EDA) vendor, in some cases the designer needs to convert the format at the time of the delivery of the data from the different EDA vendors. Problems occur when the designer lacks information at the time of format conversion and has to make up for its lack later. In addition, the pin name and net names may be different for every LSI circuit, package, and board. The designer needs to adjust those data and spend painful time in correction.

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4.4 Concept of LPB interoperable design

Interoperable design is the solution method for the problems with using conventional individual design methods for each LPB part. It is defined as the style that each LPB section uses to cooperate and design. At first, the designer makes minimum design guidelines to satisfy the product’s performance standards by designing through the whole LPB using the interoperable design. After that, the designer designs each part individually in accordance with the design guidelines. After each individual design is completed, the designer performs a simulation for integrating that part with the whole LPB, confirms the performance of all products, and provides feedback on the designs for all other parts accurately.

4.5 Value creation by LPB interoperable design

4.5.1 Effects of LPB interoperable design

LPB interoperable design is an appropriate method of design throughout a whole system for signal integrity and power integrity among LPB components. This technology is a solution for the problems discussed in 4.3. Use of LPB interoperable design makes it is possible to get the effect described in the following subclauses.

4.5.2 Reduction of development cost and time by design flow without iteration

When the designer finally connects the parts designed by partial optimization, an unexpected lack of design margin sometimes occurs. The designer then needs to discover which part of the LPB is causing the margin bottleneck. As a result, the designer may not only spend a lot of time but also need additional recovery costs for creating the needed design margin. In such cases, it is possible to reduce the development cost and time by starting LSI design, package design, and board design with each designer sharing information and cooperating from the point that the LSI design begins. Figure 2 compares conventional design flow and LPB interoperable design flow. The LPB interoperable flow reduces development costs and time.

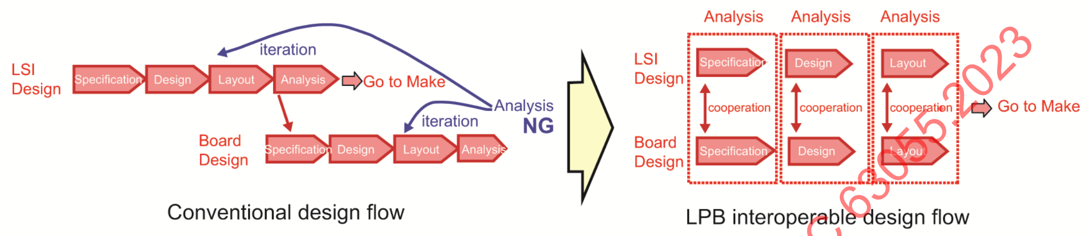

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Figure 2—Conventional design flow versus LPB interoperable design flow

4.5.3 Reduction of system total cost

In conventional design, because a designer designs each part of the LSI, package, and board separately with individual margins, the design margin of the product as whole system sometimes becomes excessive when all the parts are finally connected. It is possible to reduce the total cost using LPB interoperable design because the design margin for the whole design is controlled and held in total, including reduction of the number and cost of the parts used in the design. Figure 3 compares the design margins of conventional design flow and LPB interoperable design flow.

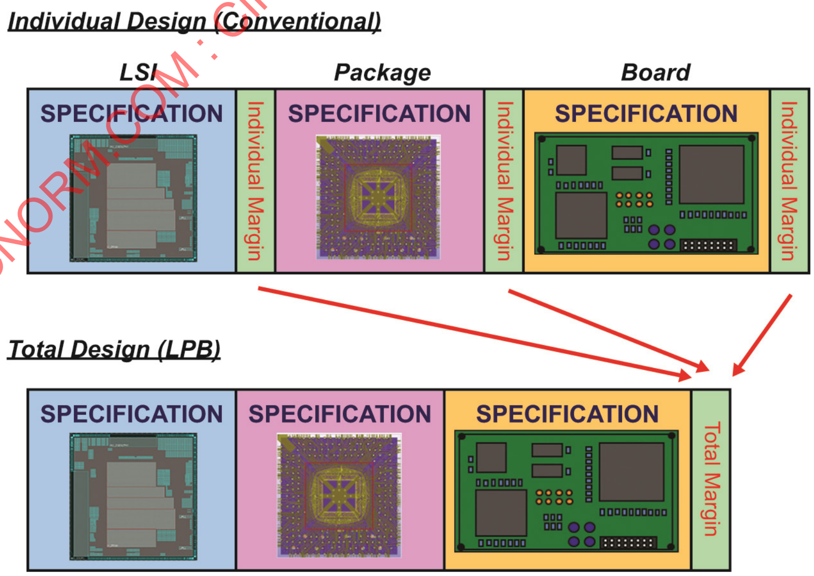

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Figure 3—LPB interoperable design can control design margin

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4.6 LPB Format

LPB Format solves the problems in conventional design methodologies, improves product quality, and reduces design time. LPB Format is a common language for describing the information required for design and verification. It reduces the preparation time of EDA tools in design teams. Furthermore, LPB can enable the sharing of ideas beyond the design teams. It can become a medium for information distribution in the supply chain. It prevents misunderstanding of design information and improves the information flow in the whole industry. As the result, quality, cost, and delivery time (QCD) will be improved.

4.7 Summary of LPB Format files

4.7.1 General

Figure 4 shows one example of how design information is exchanged using the LPB Format. In this example, three types of designers exist: the LSI designer, the package designer, and the board designer. All designers exchange design information using LPB Format standard files. By unifying the notation of the files for exchanging design information, it is possible to prevent misunderstandings and to automate the design tool settings.

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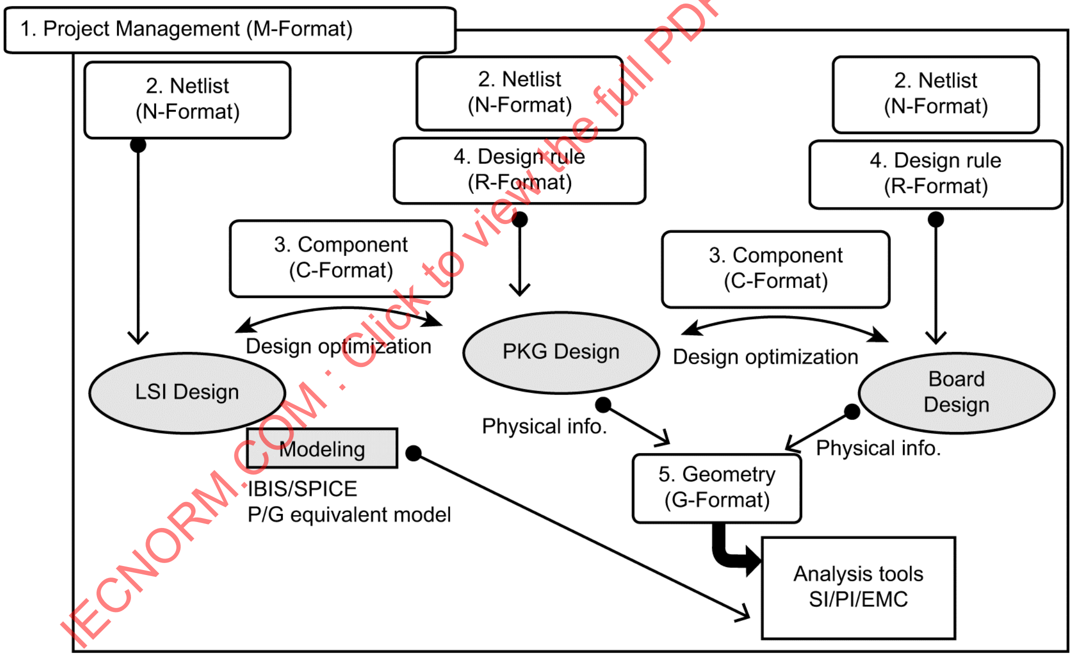

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Figure 4—Example of exchanging design information using the LPB Format

4.7.2 C-Format

The first purpose of C-Format is to give a unified notation to the outer specifications for parts, such as the LSI, package, socket, and so forth. The outer specification is the information needed in order to use the parts, as follows:

- Physical shape of the parts
- Name and type of signal to be input to and output from the parts
- Input/output (I/O) specification, such as the physical shape and position of pins, or swappable pin definitions
- Design constraints, such as the upper limit of the delay or skew
- Design specifications, such as the input impedance of pins or power consumption

By unifying the notation with C-Format, it is possible to exchange information without misunderstanding. For example, a board designer should understand the specifications delivered from several LSI vendors and should set up the design tools based on this understanding. Human error may occur during this process if the specifications are described by each vendor's own notation. Using C-Format instead of the vendor's own notations, it is possible to set up the design tool automatically and to prevent human error due to misunderstanding. Figure 5 shows an example of the information flow of LSI specifications using C-Format. The LSI specifications are all provided by C-Format even if the vendors are different. The board designer can understand the LSI specifications by reading only one notation, and design tools can automatically set up themselves by entering C-Format.

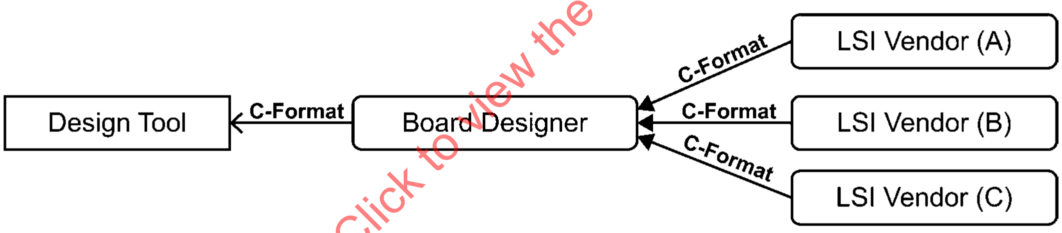

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Figure 5—Example of information flow of LSI specifications using C-Format

Unified notation also smoothly circulates information about specification changes. Figure 6 shows an example of interoperable design flow. A board designer and a LSI designer are collaborating. The information about the pin assignment of the LSI package is provided by the LSI designer. When the board designer wants to change the pin assignment of the LSI package, he or she modifies the provided C-Format file and returns it to the LSI designer. The use of C-Format prevents misunderstanding about the specification change and prevents human error that can occur due to specification changes.

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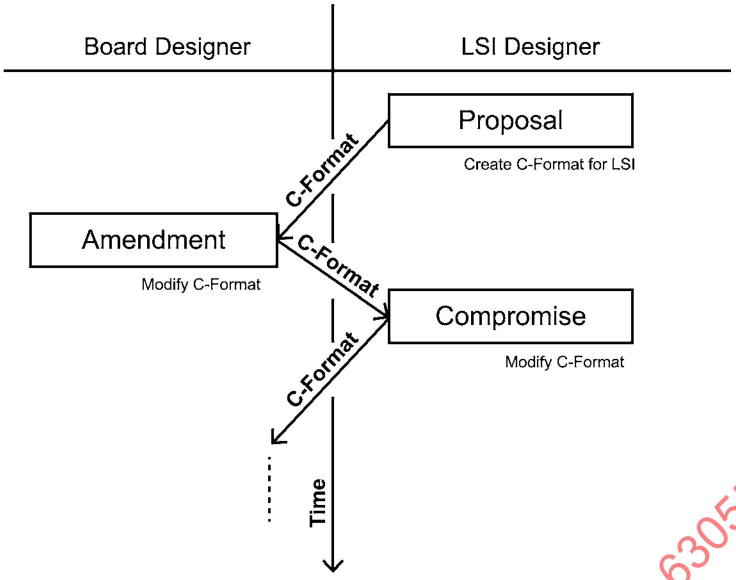

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Figure 6—Example of interoperable design flow with C-Format

The second purpose of C-Format is to provide a unified interface to a simulation model such as a Simulated Program with Integrated Circuit Emphasis (SPICE) netlist, Input/output Buffer Information Specification (IBIS), S-parameters, etc. C-Format wraps these simulation model files and gives cross-references between the nodes of the simulation model and the physical ports of the parts. Simulation tools can plug in the simulation model automatically by entering the wrapped model file. Figure 7 shows an example of exchanging simulation models. Model files are provided with the C-Format file.

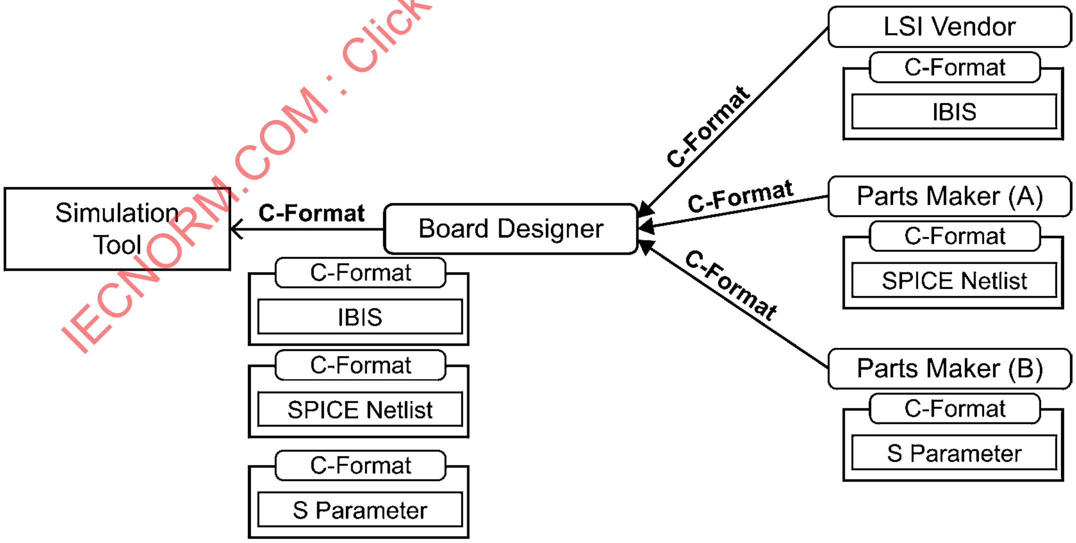

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Figure 7—Example of exchanging simulation models with C-Format

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The third purpose of C-Format is to provide connection points to merge multiple layout data. C-Format wraps layout data files, such as Graphic Database System (GDS) II, and gives cross-references between ports in the C-Format file and objects in the layout data file. For example, when the C-Format file wraps a GDS II file, ports in C-Format are associated with the coordinates/layers in the GDS II file. When the C-Format file wraps a G-Format file, ports in the C-Format file are associated to the pin in the G-Format file. This feature can be used to merge two or more layout data designed by different design houses. Such situations can occur when the board designer wants to analyze the board with package layout data. The board designer receives the wrapped package layout data from the package designer and enters it in the analysis tools. The analysis tools can find the connection points using the cross-references defined in the C-Format file and merge the layout data of the printed circuit board and the package.

The fourth purpose of C-Format is to support the floorplan of the printed circuit board and package. C-Format includes placement information about parts. This feature can be used to communicate the floorplan information from the system designer to the board designer. Figure 8 shows an example of design flow when the system designer requests a printed circuit board design to the board designer. At the beginning of the work, the printed circuit board designer can set up the design tools based on the provided C-Format file. By unifying the notation of the floorplan, it is possible to exchange floorplan information without misunderstanding, and to set up the design tool automatically.

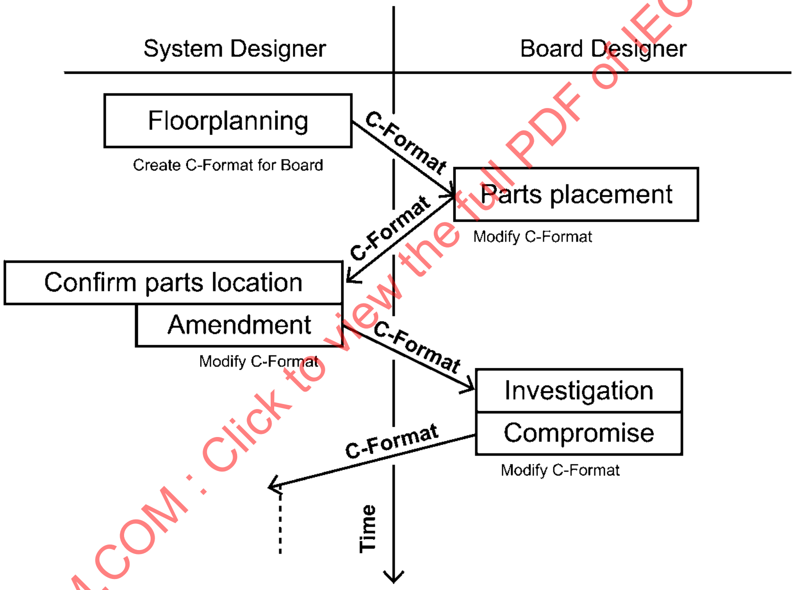

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Figure 8—Example of design flow between system designer and board designer

4.7.3 R-Format

The first purpose of R-Format is to unify the notation of the design rules of the printed circuit board and the package. The following design rules are defined in R-Format:

- Layer stackup of the package and the printed circuit board
- The thickness of the conductive layer/insulating layer
- The material used for each layer
- The material parameters, such as conductivity, dielectric constant, or loss tangent

- Line width and line space
- Via spacing
- Shape of vias

Normally, manufacturers of printed circuit boards and packages provide the design rules using their own notations. The designer has to understand the design rules described in several notations and set up the design tools, with the risk that human error may occur. However, using a unified notation such as R-Format makes it possible to set up the design tool automatically and to prevent misunderstanding. Figure 9 shows an example of exchanging design rules using R-Format. All manufacturers provide design rules using the R-Format unified notation. Design tools can set up themselves automatically by entering R-Format.

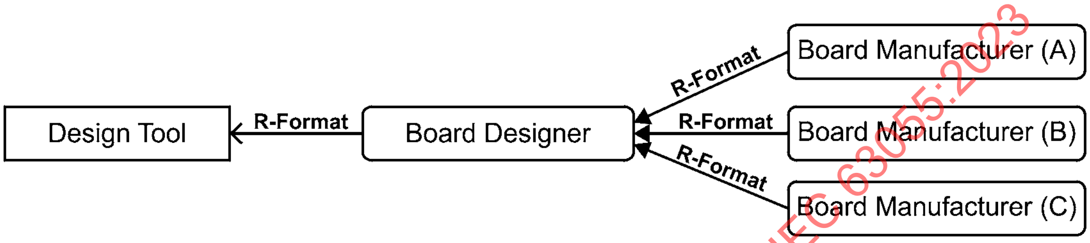

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Figure 9—Example of exchanging design rules with R-Format

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The second purpose of R-Format is to define the physical design constraints of the printed circuit board and the package. *Physical design constraints* mean the height limitation of mounted parts and the non-default design rule area.

4.7.4 G-Format

The purpose of G-Format is to unify the notation of the layout data of the layer stack-up structure, such as the printed circuit board or package. It is possible to exchange the layout data seamlessly between analysis tools and layout tools by the unified notation of the layout data. The G-Format file includes the following geometric information:

- Printed circuit board
- Layer stackup and physical parameters of the material
- Shape and location of the mounted parts
- Shape and location of the pins
- Route or pattern of the nets
- Shape and location of the vias
- Shape of the bonding wires

Figure 10 shows an example of exchanging layout data using G-Format. Analysis tools can set up by only entering G-Format if all layout tools output G-Format files.

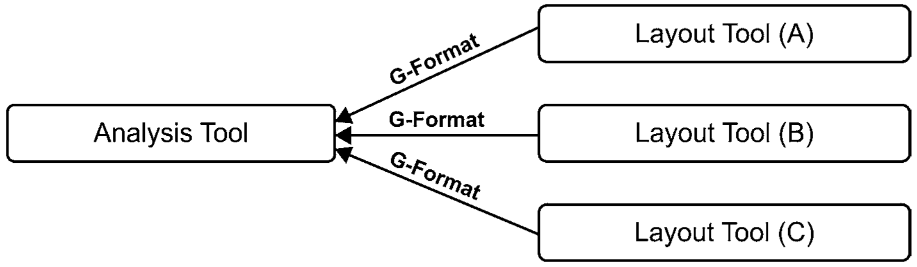

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Figure 10—Example of exchanging layout data with G-Format

4.7.5 N-Format

The purpose of N-Format is to unify the notation of the netlist that is used to design the printed circuit board and the package, where *the netlist* means the connectivity information between parts mounted on a printed circuit board or package. N-Format conforms to Verilog hardware description language (HDL) (IEEE Std 1364™[6]) and adds keywords to identify power and ground nets. Unifying notation of the netlist makes it possible to exchange the netlist seamlessly between circuit design tools and layout tools. For example, when the circuit designer orders the board design from the board designers, the circuit designers should exchange the netlist.

If the netlist is represented using several notations, there is a risk that human error may occur when entering the connectivity between parts into the design tools. However, by using the unified notation for netlist, it is possible to prevent human errors when setting up the design tools because all design tools can set up the connectivity between parts by supporting only one notation for the netlist file. Figure 11 shows an example of design flow using the N-Format file. The circuit modification is exchanged using N-Format.

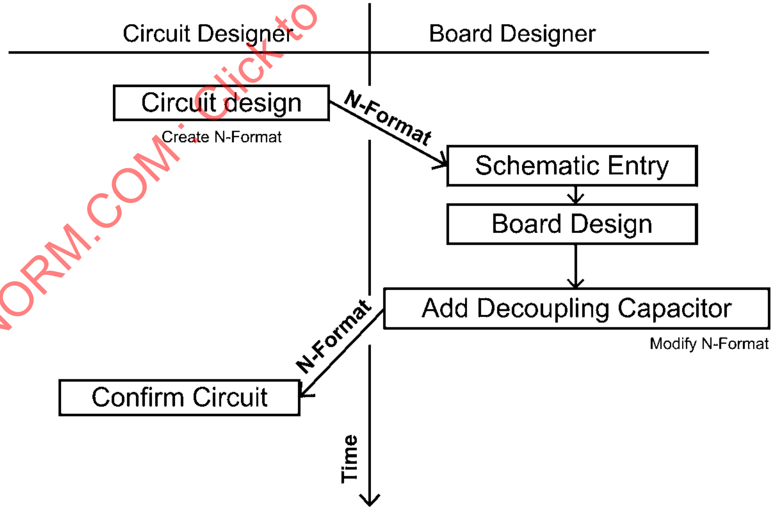

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Figure 11—Example of design flow with N-Format

[6] Information on references can be found in Clause 2.

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4.7.6 M-Format

LPB Format files are continuously updated in accordance with the design progress. The purpose of M-Format is to manage the version of each file to prevent errors when exchanging LPB Format files.

5. Language basics

5.1 General

This subclause describes the conventions used in the syntax definitions of the LPB M-Format, C-Format, and R-Format.

5.2 Typographic and syntax conventions

The following list describes the syntax conventions:

`text`

The `monospace` font is used to indicate the attributes or elements that shall be typed literally.

`italic`

The *`italic`* font is used to indicate the user-defined information for which shall be substituted a name or value.

|

Vertical bars separate possible choices for a single attribute or element. They take precedence over any other character.

[ ]

Brackets denote optional attributes or elements. When used with vertical bars, they enclose a list of choices.

[ ]…

Brackets followed by three dots indicate that there shall be specified zero or more attributes or elements. When used with vertical bars, they enclose a list of choices.

{ }…

Braces followed by three dots indicate that there shall be specified one or more attributes or elements. When used with vertical bars, they enclose a list of choices.

…

Three dots indicate that the previous value could be repeated.

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All of the strings in the M-Format, C-Format, and R-Format are case sensitive.

NOTE—All code examples in this standard are written in monospace font.[7]

5.3 Character information

Unless otherwise noted, only ASCII characters, as defined in ANSI Standard X3.4-1986, shall be used in LPB Format file. The use of characters with codes greater than hexadecimal 0x7E is not allowed. Also, ASCII control characters (those numerically less than hexadecimal 0x20) are not allowed, except for tabs or in a line termination sequence.

5.4 Notation of the floating point number

The following format is used to denote floating point numbers.

```
[-|+]<mantissa>[{e|E}[-|+]<exponent>]
```

`<mantissa>`

An integer or fractional number. Only numeric character (0 to 9) and decimal separator character (period) shall be used.

`<exponent>`

Only integer shall be used for the exponent (the power of 10). Shall not contain a decimal separator character.

5.5 File naming definitions

The following defines a rule of file referencing.

- **directory**: A location for storing files on a hierarchical file system.
- **root directory**: A standard designation for the root of a file system. In Windows, it includes the driver letter (line C:) and in Linux, it includes the root slash (/).
- **current directory**: A directory that holds current LPB Format file.
- **path**: A route to a specific file that is represented by a sequence of root directory (optional) and directories.
- **absolute path**: An absolute path is a path that starts from the root directory of a file system. It locates the specified file regardless of the current directory.
- **relative path**: The relative path is not starting from root directory. It locates a file relative to the current directory.
- **file reference**: A reference to a file, expressed as either a simple file name or including relative or absolute path. Simple file name means that the file is located in the current directory.

[7] Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

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6. Common elements in M-Format, C-Format, and R-Format

6.1 General

This clause provides commonly used elements in M-Format, C-Format, and R-Format.

M-Format, C-Format, and R-Format use the World Wide Web Consortium standard for the XML version 1.0 [B21]. M-Format, C-Format, and R-Format are structured by several elements. The name of an element is enclosed in triangular brackets `< >`.

```
 <element_name>
```

An element can contain multiple elements as its children. An element start with `<element_name>` and end with `</element_name>` if the element contains children.

```
 <element_name>....</element_name>
```

If an element does not contain children, the element simply expresses as `<element_name/>`. The order of elements is defined by syntax rule of M-Format, C-Format, and R-Format.

An element can have one or more attributes. An attribute is represented by name, and a value enclosed in double quotation. Attribute values shall be numeric value or string value. Numeric value shall be notated according to the rules defined in 5.4. Unless restricted by keyword, string value is free strings.

```
  attribute_name="attribute_value"
```

The attributes can appear in any order and shall be unique.

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6.2 The <extensions> element

6.2.1 General

The `<extensions>` element is a container of the user's own extension. It is used to add the user's own specifications to M-Format, C-Format, and R-Format. All user extensions are defined using the namespace (Name spaces in XML 1.0 [B16]). Any description can be added to user extension area as long as they accord to the XML format. The user extension declaration has the following syntax.

```
<extensions xmlns:user_prefix="URI">
    {<user_prefix:user_own_tag {user_own_attribute="any_string"}… />}…
</extensions>
```

If multiple users add the their own specifications individually, the keywords might conflict with each other. Use the namespace identified by URI reference to prevent the keyword conflicting. The most important thing of URI is that it is unique. The users who use user extension area can guarantee the uniqueness of the URI by registering the domain name included in URI to internet domain management organization. It is the responsibility of the user extension to guarantee the uniqueness of the string used after the domain name. The LPB Format use the URI as an identifier. Including a specific domain name is an idea to ensure uniqueness of URI strings. The URI specified here can be fictitious as long as it is unique. Only graphic characters in ANSI Standard X3.4-1986 (codes 0x21 to 0x7E) shall be used for URI.

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6.2.2 Example

The following is an example of the `<extensions>` element in use.

```
<header project="test project" design_revison="1.1">
    <extensions xmlns:A="http://www.A.com">
        <A:own_user_area1 myattribute1="xxx" myattribute2="yyy"/>
        <A:own_user_area2 myattribute3="xxx" myattribute4="yyy"/>
    </extensions>
    <extensions xmlns:B="http://www.B.com">
        <B:own_user_area1 myattribute1="xxx" myattribute2="yyy"/>
        <B:own_user_area2 myattribute3="xxx" myattribute4="yyy"/>
    </extensions>
</header>
```

6.3 The <header> element

6.3.1 General

The `<header>` element defines the management information of the M-Format, R-Format, and C-Format files.

```
<header
             project="project_name"
             design_revison="revision_number"
             [permission="edit_permission"]
             [date="date"]
             [author="owner_of_this_document"]
             [email="email_address"]
             [company="company_name"]
             [comment="any_comment"]
>
             [<extensions> element]…
</header>
```

By processing the `<header>` element, you can get the project name (`project`), creation date (`date`), information about the author (`author`, `email`, and `company`), and a control number (`design_revision`).

6.3.2 Attribute definitions

The attributes of the `<header>` element are defined as follows.

`project`

> This attribute specifies the name of the project. All LPB Format files in a project shall have the same project name.

`design_revision`

> This attribute specifies the revision number of each LPB Format file. The revision number shall be increased appropriately when modifying the LPB Format file.

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`permission`

This attribute specifies the edit permission of each LPB Format file. The value shall be one of the following:

`EDITABLE`	Permit editing.
`LOCKED`	Prohibit editing.

If `permission` attribute is not specified, `EDITABLE` is set as the default.

`date`

This attribute specifies the creation or modification date of the LPB Format file.

`author`

This attribute specifies the name of the author of the LPB Format file.

`email`

This attribute specifies the email address of the author.

`company`

This attribute specifies the organization to which the author of this design file belongs.

`comment`

This attribute specifies an arbitrary text string used as a comment.

6.3.3 Element content

The `<header>` element can contain the following element:

`<extensions>`

6.3.4 Example

The following is an example of the `<header>` element in use.

```
<header
    project="JEITA_LPB_SAMPLE_PROJECT"
    design_revision="1.3"
    date="20190101"
    permission="LOCKED"
    author="yyyyy xxxxx"
    email="xxxx@jeita.jp"
    company="JEITA"
    comment="This is a sample code of LPB format."
 >
    <extensions xmlns:LPB_FORUM="http://www.lpb-forum.com">
       <LPB_FORUM:header_ext comment="this is a sample of user extension area"/>
    </extensions>
</header>
```

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6.4 The <global> element

6.4.1 General

The <global> element defines the unit system, basic shapes, and padstack to be used throughout the R-Format and C-Format files.

```
<global>
             <unit> element
             [<shape> element]…
             [<padstack_def> element]…
             [<extensions> element]…
</global>
```

The scope of the defined variables is limited to the file in which it is declared. The content of the <global> element consists of one <unit> element and one or zero <shape> and <padstack_def> elements.

6.4.2 Element contents

The <global> element can contain the following elements:

```
     <unit>
     <shape>
     <padstack_def>
     <extensions>
```

6.4.3 The <unit> element

The <unit> element defines the unit system to be used in LPB Format file.

```
<unit>
             [<distance> element]
             [<angle> element]
             [<area> element]
             [<time> element]
             [<resistance> element]
             [<capacitance> element]
             [<resistivity> element]
             [<temperature> element]
             [<voltage> element]
             [<current> element]
             [<power> element]
             [<inductance> element]
             [<frequency> element]
             [<impedance> element]
             [<thermal_conductivity> element]
             [<specific_heat_capacity> element]
             [<density> element]
             [<thermal_diffusivity> element]
             [<coefficient_of_thermal_expansion> element]
             [<dynamic_viscosity> element]
             [<extensions> element]…
</unit>
```

The value for each indicates how the numbers in the LPB Format file shall be interpreted.

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6.4.3.1 Element content

6.4.3.1.1 The <distance> element

The `<distance>` element defines length units to be used in the LPB Format file.

```
<distance unit="length_unit"/>
```

The *`length_unit`* shall be one of the following values:

`pm`	picometers
`nm`	nanometers
`um`	micrometers
`mm`	millimeters
`m`	meters
`inch`	inches
`mil`	mil

If `<distance>` element is not specified, `m` is set as the default.

6.4.3.1.2 The <angle> element

The `<angle>` element defines a unit system for angles.

```
<angle unit="unit_of_angle"/>
```

The *`unit_of_angle`* shall be either of the following values:

```
degree
radian
```

If `<angle>` element is not specified, `degree` is set as the default.

6.4.3.1.3 The <area> element

The `<area>` element defines a unit of area.

```
<area unit="unit_of_area" />
```

The *`unit_of_area`* shall be one of the following values:

`pm2`	square picometer
`nm2`	square nanometer
`um2`	square micrometer
`mm2`	square millimeter
`m2`	square meter
`i2`	square inch

If `<area>` element is not specified, `m2` is set as the default.

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6.4.3.1.4 The <time> element

The `<time>` element defines a unit of time in seconds.

```
<time unit="unit_of_time" />
```

The *`unit_of_time`* shall be one of the following values:

`ps`	picosecond
`ns`	nanosecond
`us`	microsecond
`ms`	millisecond
`s`	second

If `<time>` element is not specified, `s` is set as the default.

6.4.3.1.5 The <resistance> element

The `<resistance>` element defines a unit of resistance.

```
<resistance unit="unit_of_resistance" />
```

The *`unit_of_resistance`* shall be one of the following values:

`fohm`	femtoohm
`pohm`	picoohm
`nohm`	nanoohm
`uohm`	microohm
`mohm`	milliohm
`ohm`	ohm
`kohm`	kiloohm
`Mohm`	megaohm
`Gohm`	gigaohm

If `<resistance>` element is not specified, `ohm` is set as the default.

6.4.3.1.6 The <capacitance> element

The <capacitance> element defines a unit of capacitance.

```
<capacitance unit="unit_of_capacitance" />
```

The *`unit_of_capacitance`* shall be one of the following values:

`fF`	femtofarad
`pF`	picofarad
`nF`	nanofarad
`uF`	microfarad
`mF`	millifarad
`F`	farad
`kF`	kilofarad

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`MF`	megafarad
`GF`	gigafarad

If `<capacitance>` element is not specified, `F` is set as the default.

6.4.3.1.7 The <resistivity> element

The `<resistivity>` element defines a unit of resistivity.

```
<resistivity unit="unit_of_resistivity" />
```

The *`unit_of_resistivity`* shall be one of the following values:

`fohmm`	femtoohm meter
`nohmm`	nanoohm meter
`pohmm`	picoohm meter
`uohmm`	microohm meter
`mohmm`	milliohm meter
`ohmm`	ohm meter
`kohmm`	kiloohm meter
`Mohmm`	megaohm meter
`Gohmm`	gigaohm meter

If `<resistivity>` element is not specified, `ohmm` is set as the default.

6.4.3.1.8 The <temperature> element

The `<temperature>` element defines a unit system for temperature.

```
<temperature unit="unit_of_temperature" />
```

The *`unit_of_temperature`* shall be either of the following values:

`C`	celsius
`K`	kelvin

If `<temperature>` element is not specified, `C` is set as the default.

6.4.3.1.9 The <voltage> element

The `<voltage>` element defines a unit of voltage.

```
<voltage unit="unit_of_voltage" />
```

The *`unit_of_voltage`* shall be one of the following values:

`pV`	picovolt
`nV`	nanovolt
`uV`	microvolt
`mV`	millivolt

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V	volt
kV	kilovolt

If <voltage> element is not specified, V is set as the default.

6.4.3.1.10 The <current> element

The <current> element defines a unit of electric current.

```
<current unit="unit_of_current" />
```

The *unit_of_current* shall be one of the following values:

pA	picoampere
nA	nanoampere
uA	microampere
mA	milliampere
A	ampere
kA	kiloampere

If <current> element is not specified, A is set as the default.

6.4.3.1.11 The <power> element

The <power> element defines a unit of power consumption.

```
<power unit="unit_of_power" />
```

The *unit_of_power* shall be one of the following values:

pW	picowatt
nW	nanowatt
uW	microwatt
mW	milliwatt
W	watt
kW	kilowatt

If <power> element is not specified, W is set as the default.

6.4.3.1.12 The <inductance> element

The <inductance> element defines a unit of inductance.

```
<inductance unit="unit_of_inductance" />
```

The *unit_of_inductance* shall be one of the following values:

fH	femtohenry
pH	picohenry
nH	nanohenry

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`uH`	microhenry
`mH`	millihenry
`H`	henry
`kH`	kilohenry

If `<inductance>` element is not specified, `H` is set as the default.

6.4.3.1.13 The <frequency> element

The `<frequency>` element defines a unit of frequency.

```
<frequency unit="unit_of_frequency" />
```

The *`unit_of_frequency`* shall be one of the following values:

`uHz`	microhertz
`mHz`	millihertz
`Hz`	hertz
`kHz`	kilohertz
`MHz`	megahertz
`GHz`	gigahertz

If `<frequency>` element is not specified, `Hz` is set as the default.

6.4.3.1.14 The <impedance> element

The `<impedance>` element defines a unit of impedance.

```
<impedance unit="unit_of_impedance" />
```

The *`unit_of_impedance`* shall be one of the following values:

`fohm`	femtoohm
`pohm`	picoohm
`nohm`	nanoohm
`uohm`	microohm
`mohm`	milliphm
`ohm`	ohm
`kohm`	kiloohm
`Mohm`	megaohm

If `<impedance>` element is not specified, `ohm` is set as the default.

6.4.3.1.15 The <thermal_conductivity> element

The `<thermal_conductivity>` element defines a unit of thermal conductivity.

```
<thermal_conductivity unit="unit_of_thermal_conductivity" />
```

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The `unit_of_thermal_conductivity` shall be one of the following values:

`W/(m*K)`	$\frac{\text{watt}}{(\text{meter} \times \text{kelvin})}$
`W/(cm*K)`	$\frac{\text{watt}}{(\text{centimeter} \times \text{kelvin})}$

If `<thermal_conductivity>` element is not specified, `W/(m*K)` is set as the default.

6.4.3.1.16 The <specific_heat_capacity> element

The `<specific_heat_capacity>` element defines a unit of specific heat capacity.

```
<specific_heat_capacity unit="unit_of_thermal_specific_heat_capacity" />
```

The `unit_of_specific_heat_capacity` shall be one of the following values:

`J/(g*K)`	$\frac{\text{joule}}{(\text{gram} \times \text{kelvin})}$
`J/(kg*K)`	$\frac{\text{joule}}{(\text{kilogram} \times \text{kelvin})}$

If `<specific_heat_capacity>` element is not specified, `J/(kg*K)` is set as the default.

6.4.3.1.17 The <density> element

The `<density>` element defines a unit of density.

```
<density unit="unit_of_density" />
```

The `unit_of_density` shall be one of the following values:

`kg/m3`	$\frac{\text{kilogram}}{\text{cubic meter}}$
`g/m3`	$\frac{\text{gram}}{\text{cubic meter}}$
`g/cm3`	$\frac{\text{gram}}{\text{cubic centimeter}}$

If `<density>` element is not specified, `kg/m3` is set as the default.

6.4.3.1.18 The <thermal_diffusivity> element

The `<thermal_diffusivity>` defines the unit of the coefficient of thermal diffusivity.

```
<thermal_diffusivity unit="unit_of_thermal_diffusivity">
```

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The *unit_of_thermal_diffusivity* shall be one of the following values:

m2/s	$\frac{\text{square meter}}{\text{seconds}}$
cm2/s	$\frac{\text{square centimeter}}{\text{seconds}}$

If <thermal_diffusivity> element is not specified, m2/s is set as the default.

6.4.3.1.19 The <coefficient_of_thermal_expansion> element

The <coefficient_of_thermal_expansion> defines the unit of the coefficient of thermal expansion.

```
<coefficient_of_thermal_expansion
unit="unit_of_coefficient_of_thermal_expansion">
```

The *unit_of_coefficient_of_thermal_expansion* shall be one of the following values:

1/K	$\frac{1}{\text{kelvin}}$
1/C	$\frac{1}{\text{celcius}}$

If <coefficient_of_thermal_expansion> element is not specified, 1/K is set as the default.

6.4.3.1.20 The <dynamic_viscosity> element

The <dynamic_viscosity> defines the unit of dynamic viscosity.

```
<dynamic_viscosity unit="unit_of_dynamic_viscosity">
```

The *unit_of_dynamic_viscosity* shall be one of the following values:

kg/ms	$\frac{\text{kilogram}}{\text{meter seconds}}$
Pas	pascal seconds $\left(\text{Pas} = \frac{\text{kilogram}}{\text{meter seconds}}\right)$
P	poise $\left(\text{P} = \frac{0.1\ \text{kilogram}}{\text{meter seconds}}\right)$
cP	centi poise $\left(\text{cP} = \frac{0.001\ \text{kilogram}}{\text{meter seconds}}\right)$

If <dynamic_viscosity> element is not specified, kg/ms is set as the default.

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6.4.3.2 Example

The following is an example of the `<unit>` elements in use.

```
<unit>
  <distance unit="um" />
  <angle unit="degree" />
  <area unit="um2" />
  <time unit="ps" />
  <resistivity unit="ohmm"/>
  <temperature unit="C" />
  <voltage unit="V" />
  <capacitance unit="pF" />
  <resistance unit="mohm" />
  <power unit="mW" />
  <inductance unit="nH" />
  <frequency unit="MHz" />
  <impedance unit="ohm" />
  <thermal_conductivity unit="W/(m*K)" />
  <specific_heat_capacity unit="J/(kg*K)" />
  <density unit="kg/m3" />
</unit>
```

6.4.4 The <shape> element

6.4.4.1 General

The `<shape>` element defines basic shapes those are referenced by other attributes and elements, such as a `<padstack_def>` element.

```
<shape>
             [<rectangle> element]…
             [<circle> element]…
             [<polygon> element]…
             [<extensions> element]…
</shape>
```

The scope of the defined shapes is limited to the file in which it is declared. The content of the `<shape>` element consists of zero or more `<rectangle>`, `<circle>`, and/or `<polygon>` elements.

6.4.4.2 Element content

The `<shape>` element can contain the following elements:

```
<rectangle>
<circle>
<polygon>
<extensions>
```

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6.4.4.3 The <rectangle> element

6.4.4.3.1 General

The `<rectangle>` element defines the shape of the rectangle with width, height, and rotation angle.

```
<rectangle
              id="identifier"
              width="width"
              height="height"
              [angle="rotation_angle"]
/>
```

The reference point of the defined rectangle is the center of rectangle. It is used for rotation and placement position of the rectangle.

6.4.4.3.2 Attribute definitions

The attributes of the `<rectangle>` element are defined as follows.

`id`

This attribute specifies the unique identifier that is used to reference the shape separately from other attributes and elements.

`width`

This attribute specifies the width of the rectangle. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

`height`

This attribute specifies the height of the rectangle. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the center of the rectangle. If an angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the `<angle>` element in the `<unit>` element.

6.4.4.3.3 Example

The rectangle shape in Figure 12 is represented by the following code:

```
<rectangle id="bfrect10" width="12" height="6"  angle="30"/>
```

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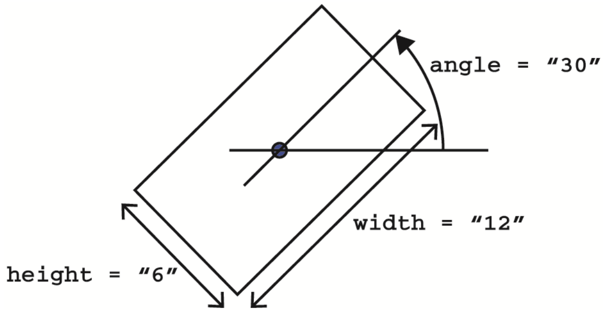

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Figure 12—Example of a rectangle shape

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6.4.4.4 The <circle> element

6.4.4.4.1 General

The `<circle>` element defines the shape of a circle by diameter.

```
<circle
              id="identifier"
              diameter="diameter"
/>
```

The reference point of the circle is at the center.

6.4.4.4.2 Attribute definitions

The attributes of the `<circle>` element are defined as follows.

`id`

This attribute specifies the unique identifier that is used to reference the shape separately from other attributes and elements.

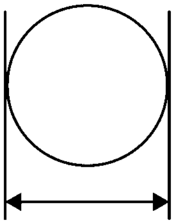
`diameter`

This attribute specifies the diameter of the circle. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

6.4.4.4.3 Example

The circle shape in Figure 13 is represented by the following code:

```
<circle id="viapad12" diameter="12"/>
```



diameter = "12"

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Figure 13—Example of a circle shape

6.4.4.5 The <polygon> element

6.4.4.5.1 General

The `<polygon>` element defines the shape of a closed polygon.

```
<polygon
              id="Identifier"
              points="x1, y1, x2, y2, x3, y3, x4, y4…"
              [angle="rotation_angle"]
/>
```

The reference point of the polygon is set to (0, 0).

6.4.4.5.2 Attribute definitions

The attributes of the `<polygon>` element are defined as follows.

`id`

This attribute specifies the unique identifier that is used to reference the shape separately from other attributes and elements.

`points`

This attribute specifies a sequence of at least four points to generate a closed polygon. The last point and first point shall be the same. Points are separated by commas (`,`), and each point is a pair of XY coordinates separated by a comma (`,`). The unit of distance is defined by the `<distance>` element in the `<unit>` element.

`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the polygon. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the `<angle>` element in the `<unit>` element.

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6.4.4.5.3 Example

The polygon shape in Figure 14 is represented by the following code:

```
<polygon id="X1" points="5,3,3,4,-3,2,-1,-3,4,-1,5,3"/>
```

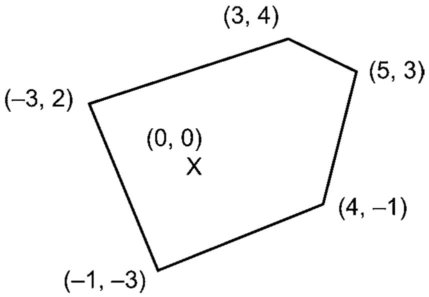

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Figure 14—Example of a polygon shape

The polygon shape in Figure 15 is represented by the following code:

```
<polygon id="X2" points="5,3,3,4,-3,2,-1,3,4,-1,5,3" angle="30"/>
```

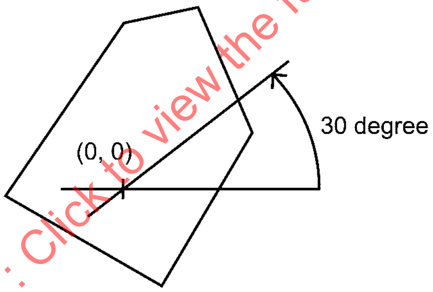

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Figure 15—Example of the rotation of a polygon shape

6.4.4.6 Example

The following is an example of the `<shape>` elements in use.

```
<shape>
  <rectangle id="R1" width="100" height="10" />
  <circle id="C1" diameter="20" />
  <polygon id="P1" points="-10,-10,10,-10,10,10,-10,10,-10,-10" />
  <circle id="VLLPAD" diameter="500" />
  <circle id="VSLPAD" diameter="400" />
  <circle id="VLSPAD" diameter="700" />
  <circle id="VSAPAD" diameter="600" />
  <circle id="SHP.10" diameter="200" />
  <rectangle id="SHP.21" width="7500" height="10900" />
  <polygon id="SQRT" points="10,10,20,10,20,20,10,20,10,10" />
</shape>
```

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6.4.5 The <padstack_def> element

6.4.5.1 General

The <padstack_def> element defines padstacks that are used by other attributes and elements.

```
<padstack_def>
             {<padstack> element}…
             [<extensions> element]…
</padstack_def>
```

The <padstack_def> element consists of one or more <padstack> elements and zero or more <extensions> elements.

6.4.5.2 Element contents

The <padstack_def> element can contain the following elements:

```
<padstack>
<extensions>
```

6.4.5.3 The <padstack> element

6.4.5.3.1 General

The <padstack> element defines the geometrical description of each pin or via of the printed wiring board (PWB) or package.

```
<padstack
             id="identifier"
>
             {<ref_shape> element}…
             [<extensions> element]…
</padstack>
```

The reference point of the padstack is at local origin (0, 0). The scope of the padstack definitions is limited to the file in which it is declared. The content of the <padstack_def> element consists of one or more <ref_shape> element and zero or more <extensions> elements.

6.4.5.3.2 Attribute definition

The attribute of the <padstack> element is defined as follows.

id

This attribute specifies the unique identifier that is used to reference the padstack from other attributes and elements.

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6.4.5.4 Element contents

The `<padstack>` element can contain the following elements:

```
<ref_shape>
<extensions>
```

6.4.5.4.1 The <ref_shape> element

6.4.5.4.1.1 General

The `<ref_shape>` element references the shape that constructs a padstack.

```
<ref_shape
                shape_id="identifier_of_referenced_shape"
                [type="shape_type"]
                [x="x_coordinate" y="y_coordinate"]
                [angle="rotation_angle"]
                [layer="shape_placed_layer"]
                [pad_layer="pad_placed_layer"]
/>
```

The referenced shape shall be defined at the `<shape>` element in the same file.

6.4.5.4.1.2 Attribute definitions

The attributes of the `<ref_shape>` element are defined as follows.

`shape_id`

This attribute specifies the identifier of the predefined shape that is defined at the `<shape>` element. The referenced shape shall be defined at the `<shape>` element in the same file.

`type`

This attribute specifies how the shape is used. Figure 16 shows an example when the shape is used for via structure. The value shall be one of the followings:

`Antipad`	Used as a shape of clearance, or antipad
`NonConnection`	Used as a shape of the nonconnection land
`Land`	Used as a shape of the normal land
`Drill`	Used as a shape of the drill; the outside diameter of the via
`Hole`	Used as a shape of the hole; the inside diameter of the via
`SolderMask`	Used as a shape of the solder mask
`Resist`	Used as a shape of solder resist

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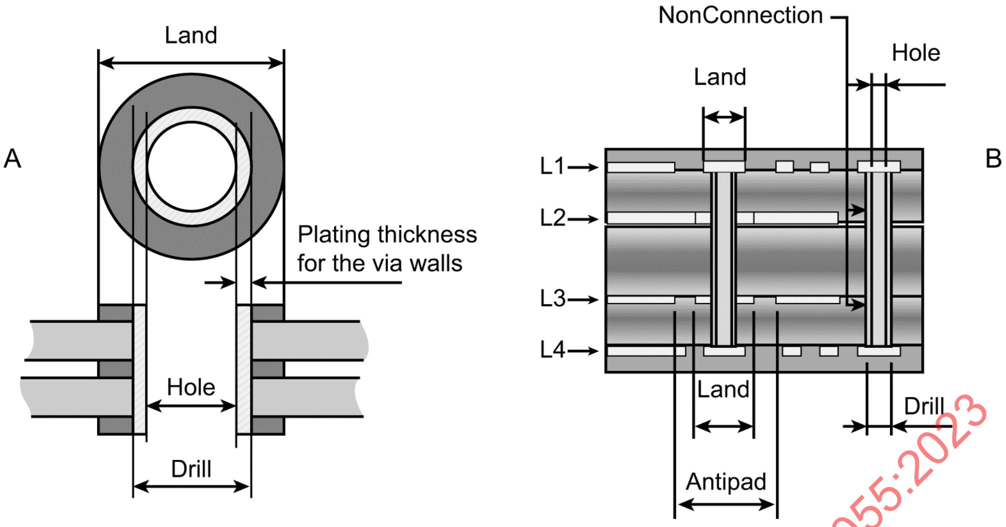

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Figure 16—Example of via structure

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x
y

These attributes specify the location of the reference point of the shape with respect to the local origin. The x and y attributes specify the x-coordinate and y-coordinate, respectively. If these attributes are not specified, zero is set as the default. The unit of the coordinate is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the shape. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

layer

This attribute specifies the name of the layer defined in the R-Format on which the shape is placed.

pad_layer

This attribute specifies the placement side of the shape as shown in Figure 17. The pad_layer attribute is used exclusively by the C-Format. The value shall be one of the following:

TOP	The shape is placed on the top side.
BOTTOM	The shape is placed on the bottom side.
FOOTPRINT	The shape is used as a footprint.

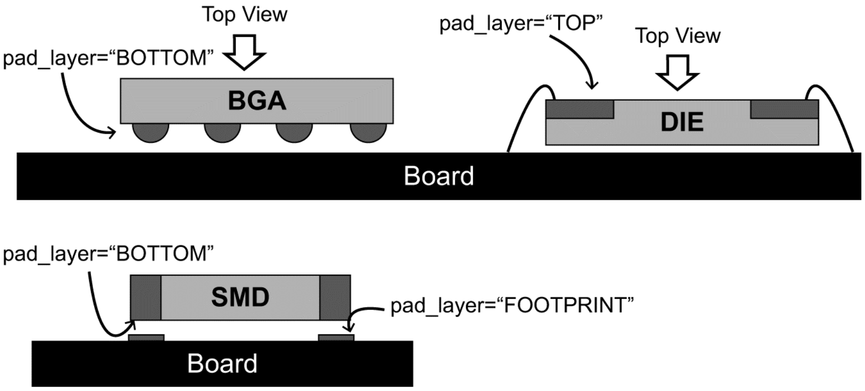

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Figure 17 —Explanatory drawing of `<pad_layer>`

6.4.5.5 Example

The following is an example of the `<padstack>` elements.

```
<padstack_def>
  <padstack id="smallvia>
     <ref_shape shape_id="VLLPAD"/>
     <ref_shape shape_id="VLAPAD"/>
     <ref_shape shape_id="VDRILL"/>
     <ref_shape shape_id="VHOLE"/>
     <ref_shape shape_id="VLLPAD"/>
     <ref_shape shape_id="VLAPAD"/>
     <ref_shape shape_id="VDRILL"/>
     <ref_shape shape_id="VHOLE"/>
  </padstack>
  <padstack id="ball>
     <ref_shape shape_id="SHP.10"
                x="0" y="0" angle="0" pad_layer="BOTTOM"
     />
  </padstack>
</padstack_def>
```

7. M-Format

7.1 M-Format file structure

The content of the M-Format file consists of one `<header>` element, zero or more `<include>` elements, zero or one `<current_phase>` elements, and one or more `<class>` elements. The elements shall be specified in the following order:

```
<LPB_MFORMAT version="2020">
             <header> element
             [<include> element]…
             [<current_phase> element]
             {<class> element}…
             [<extensions> element]…
</LPB_MFORMAT>
```

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7.2 The <include> element

7.2.1 General

The `<include>` element specifies other M-Format files to be included.

```
<include
             MFORMAT="name_of_M_format_file"
/>
```

7.2.2 Attribute definition

The attribute of the `<include>` element is defined as follows.

MFORMAT

> This attribute specifies the name of the M-Format file to be included. When this attribute does not contain a directory name, it means the M-Format file exists in the current directory. When this attribute contains a relative path, it means the M-Format file exists in that relative place from the current directory. Also, this attribute may use an absolute path from the root directory.

7.2.3 Example

The following is an example of the `<include>` element in use.

```
<include MFORMAT="LPBFMT-PKG.xml" />
<include MFORMAT="ydir/zdir/LPBFMT-PKG2.xml" />
<include MFORMAT="/TOPDIR/xdir/LPBFMT-SOC.xml" />
```

7.3 The <current_phase> element

7.3.1 General

A purpose of MFormat is to manage the versions of LPB Format files that are used in several design phases. One MFormat can include those versions of LPB Format files. The `<current_phase>` element is used to declare the current design phase. Applications that handle MFormat shall select LPB Format files for the design phase.

```
<current_phase  name="current_design_phase" />
```

7.3.2 Attribute definition

The attribute of the `<current_phase>` element is defined as follows:

name

> This attribute specifies the design phase name that is defined by `phase_name` attribute in `<class>` element.

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7.3.3 Example

The following example includes three design phases. The current design phase is "step03_cad". The application shall select the LPB Format files that are used in "step03_cad" design phase.

```
<?xml version="1.0" ?>
<LPB_MFORMAT version="2020">
    <header project="myproj01"
            design_version="1.0"
            date="2018-06-17 13:00:00"
            author="Mr.X"
            company="JEITA/SDTC/LPBSC/2020TG" />
    <current_phase name="step03_cad"/>
    <class name="myboard"
           phase_name="phase03_cad"
           comment="cad design ongoing"
           date="2018-06-14 13:00">
    .... .... .... .... .... .... .... .... ....
    .... .... .... .... .... .... .... .... ....
    </class>
    <class name="myboard"
           phase_name="phase02_sim"
           comment="si/pi simulation was ok"
           date="2018-06-07 13:00">
    .... .... .... .... .... .... .... .... ....
    .... .... .... .... .... .... .... .... ....
    </class>
    <class name="myboard"
           phase_name="phase01_fs"
           comment="feasibility study done"
           date="2018-06-01 13:00">
    .... .... .... .... .... .... .... .... ....
    .... .... .... .... .... .... .... .... ....
    </class>
```

7.4 The <class> element

7.4.1 General

The <class> element binds the related files which form a functional module, such as an LSI, package, or printed circuit board.

```
<class
             [name="class_name"]
             [phase_name="design_phase_name"]
             [date="date"]
             [comment="comment_text"]
>
             [<CFORMAT> element]
             [<RFORMAT> element]…
             [<GFORMAT> element]…
             [<NFORMAT> element]…
             [<OtherFile> element]…
             [<ref_class> element]…
             [<extensions> element]…
</class>
```

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7.4.2 Attribute definition

The attributes of the `<class>` element are defined as follows.

`name`

This attribute specifies the name of the class.

`phase_name`

This attribute specifies the design phase name. The LPB Format files defined in this `<class>` mean that they are used in the design phase specified here.

`date`

This attribute specifies the date when the class is defined or modified.

`comment`

This attribute specifies the comment string.

7.4.3 Element content

The `<class>` element can contain the following elements:

```
<CFORMAT>
<RFORMAT>
<GFORMAT>
<NFORMAT>
<OtherFile>
<ref_class>
<extensions>
```

7.4.4 Example

The following is an example of the `<class>` element in use.

```
<class
    name="LPB_SAMPLE_CLASS"
    phase_name="Final_Design_Rev.1.0"
    date="20190331"
    comment="PWB"
>
    <CFORMAT
        comment="C-Format"
        file_name="CFMT_TOP.xml"
        design_revision="1.0"
        MD5="646da9ae5d90e6b51b0a578badae372f"
    />
    <RFORMAT
        comment="R-Format"
        file_name="RFMT_TOP.xml"
        design_revision="1.0"
        MD5="6ede01b9fed673b6619cffb5f96e1acf"
    />
    <GFORMAT
        comment="G-Format"
```

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```
        file_name="GFMT_TOP.xfl"
        MD5="6ede01b9fed672cfa746974210d68e96"
    />
    <NFORMAT
        comment="N-Format"
        file_name="NFMT_TOP.v"
        MD5="ee620bf842fb6646da9ae5d90e6b51b0"
    />
    <ref_class
        commnet="Parts"
        file_name="./lib/LPB_PARTS.xml"
        class_name="parts_lib"
    />
</class>
```

7.4.5 The <CFORMAT> element

7.4.5.1 General

The <CFORMAT> element specifies a file of the LPB-component format (C-Format).

```
<CFORMAT
                [comment="comment_text"]
                file_name="name_of_C_format_file"
                design_revision="revision_number"
                [MD5="MD5_checksum"]
/>
```

7.4.5.2 Attribute definitions

The attributes of the <CFORMAT> element are defined as follows.

comment

This attribute specifies a comment string.

file_name

This attribute specifies the name of the C-Format file.

design_revision

This attribute specifies the revision number of the C-Format file.

MD5

This attribute specifies a message digest algorithm 5 (MD5) checksum for the C-Format file.

7.4.5.3 Example

The following is an example of the <CFORMAT> element in use.

```
<CFORMAT comment="C-Format" file_name="CFMT_TOP.xml"
  design_revision="1.0" MD5="5c34a4dd1bb48484e1e93eb5e23b3094" />
```

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7.4.6 The <RFORMAT> element

7.4.6.1 General

The `<RFORMAT>` element specifies a file of the LPB-rule format (R-Format).

```
<RFORMAT
             [comment="comment_text"]
             file_name="name_of_R_format_file"
             design_revision="revision_number"
             [MD5="MD5_checksum"]
/>
```

7.4.6.2 Attribute definitions

The attributes of the `<RFORMAT>` element are defined follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the R-Format file.

`design_revision`

This attribute specifies the revision number of the R-Format file.

`MD5`

This attribute specifies an MD5 checksum for the R-Format file.

7.4.6.3 Example

The following is an example of the `<RFORMAT>` element in use.

```
  <RFORMAT comment="R-Format" file_name="RFMT_TOP.xml"
    design_revision="1.0" MD5="4d16098ad69f0a153387d6430a25806a" />
```

7.4.7 The <GFORMAT> element

7.4.7.1 General

The `<GFORMAT>` element specifies a file of the LPB-geometry format (G-Format).

```
<GFORMAT
             [comment="comment_text"]
             file_name="name_of_G_format_file"
             [MD5="MD5_checksum"]
/>
```

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7.4.7.2 Attribute definitions

The attributes of the `<GFORMAT>` element are as follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the G-Format file.

`MD5`

This attribute specifies a MD5 checksum for the G-Format file.

7.4.7.3 Example

The following is an example of the `<GFORMAT>` element in use.

```
  <GFORMAT comment="G-Format" file_name="GFMT_TOP.xfl"
    MD5="b3fed15159e9fbefdf67b603395eaf4c" />
```

7.4.8 The <NFORMAT> element

7.4.8.1 General

The `<NFORMAT>` element specifies a file of the LPB-netlist format (N-Format).

```
<NFORMAT
              [comment="comment_text"]
              file_name="name_of_N_format_file"
              [MD5="MD5_checksum"]
/>
```

7.4.8.2 Attribute definitions

The attributes of the `<NFORMAT>` element are defined as follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the N-Format file.

`MD5`

This attribute specifies a MD5 checksum for the N-Format file.

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7.4.8.3 Example

The following is an example of the <NFORMAT> element in use.

```
<NFORMAT comment="N-Format" file_name="NFMT_TOP.v"
  MD5="343490687786f1420958e9aed2f2895b" />
```

7.4.9 The <OtherFile> element

7.4.9.1 General

The <OtherFile> element specifies the names of user-defined files.

```
<OtherFile
                [comment="comment_text"]
                file_name="name_of_format_file"
                [MD5="MD5_checksum"]
/>
```

7.4.9.2 Attribute definitions

The attributes of the <OtherFile> element are defined as follows.

comment

This attribute specifies a comment string.

file_name

This attribute specifies the name of a user-defined file.

MD5

This attribute specifies an MD5 checksum for the user-defined file.

7.4.9.3 Example

The following is an example of the <OtherFile> element in use.

```
<OtherFile comment="Power Model" file_name="DDRPowerModel.sp"
MD5="7ca273b0993527d8df5deed246b8fbff" />
```

7.4.10 The <ref_class> element

7.4.10.1 General

The <ref_class> element is used to reference the related other <class> elements, such as the mounting components corresponding to the board design. It specifies the class name that is defined by the name attribute in <class> element.

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```
<ref_class
             [comment="comment_text"]
             [file_name="name_of_MFormat_file"]
             class_name="reference_class_name"
>
             [<extensions> element]…
</ref_class>
```

7.4.10.2 Attribute definitions

The attributes of the `<ref_class>` element are defined as follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the M-Format file to be referenced. When this attribute is specified, the scope to search the related classes is expanded to the specified M-Format file.

`class_name`

This attribute specifies the class name to refer to the related other classes, such as the mounting components corresponding to the board design.

8. C-Format

8.1 C-Format file structure

The content of the C-Format file consists of one `<header>` and `<global>` element, one or more `<module>` elements, one or zero `<component>` element, and zero or more `<extensions>` elements. These elements shall be specified in the following order:

```
<LPB_CFORMAT version="2020">
             <header> element
             <global> element
             {<module> element}…
             [<component> element]
             [<extensions> element]…
</LPB_CFORMAT>
```

8.2 The <module> element

8.2.1 General

The module is the basic design unit of items such as a die or LSI package. The `<module>` element encapsulates the geometry information, design constraints, I/O interface, and electrical model of a module.

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```
<module
             name="name_of_module"
             [type="module_type"]
             [shape_id="identifier_of_referenced_shape"]
             [x="x_coordinate"   y="y_coordinate"]
             [angle="angle"]
             [thickness="thickness"]
             [ref_rule_name="referenced_design_rule_name"]
>
             [<size_code> element]
             [<socket> element]…
             [<guideline> element]
             [<specification> element]
             [<surrounding_characteristics> element]
             [<blockage> element]
             [<component> element]
             [<keepaway> element]
             [<reference> element]…
             [<extensions> element]…
</module>
```

The content of the `<module>` element consists of zero or more `<socket>`, `<reference>`, and `<extensions>` elements, and one or zero `<guideline>`, `<specification>`, `<surrounding_characteristics>`, `<blockage>`, `<keepaway>`, and `<component>` element.

The `<socket>` element defines the I/O ports and design constraints.

The `<specification>` element defines the specification for the module itself, such as power consumption. The `<surrounding_characteristics>` element defines the physical specification of three-dimensional structure such as thermal conductivity.

The `<reference>` element associates the port defined in the `<socket>` element with electrical node or physical data that are defined in other files. For example, the `<reference>` element can provide the position for the I/O node of SPICE that does not have physical information.

8.2.2 Attribute definitions

The attributes of the `<module>` element are as follows:

`name`

This attribute specifies the module name that is used to reference the module from other attributes and elements. The module name shall be unique in the same C-Format file.

`type`

This attribute specifies the module type. The value shall be one of the followings:

LSI	Large-scale integration
PKG	Package
PWB	Printed wiring board or printed circuit board
C	Capacitor
R	Resistor
L	Inductor
OTHER	Other type

If it is not specified, `OTHER` is set as the default.

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shape_id

This attribute specifies the identifier of the predefined shape to define the boundary shape of the module. The specified shape shall be defined at the <shape> element in the same file.

x
y

These attributes specify the location of the reference point of the shape with respect to the local origin. The x and y attribute specify the x-coordinate and y-coordinate, respectively. The module is placed at the specified point (see Figure 18). If these attributes are not specified, zero is set as the default. The unit of the coordinates is defined by the <distance> element in the <unit> element.

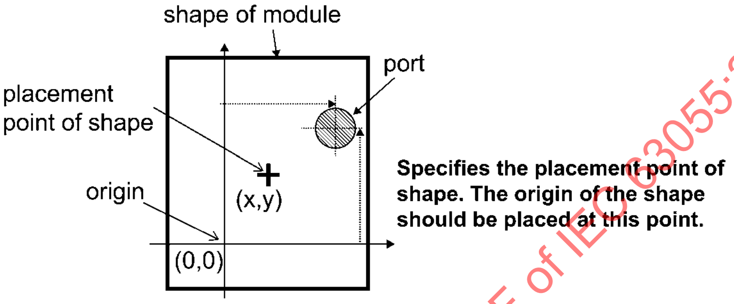
shape of module
port
placement
point of shape
origin
(x,y)
(0,0)
Specifies the placement point of shape. The origin of the shape should be placed at this point.

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Figure 18—Example of the shape of the module and its placement

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the shape as shown in Figure 19. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

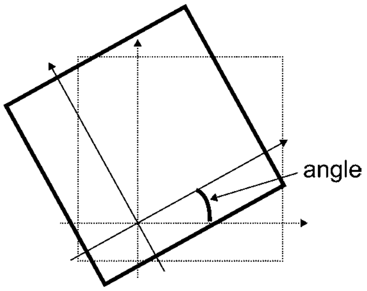

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Figure 19—Explanatory drawing of the rotation of a module

thickness

This attribute specifies the thickness module without pin or solder-ball, as shown in Figure 20. If the thickness is not specified, zero is set as the default. The unit of the coordinate is defined by the <distance> element in the <unit> element.

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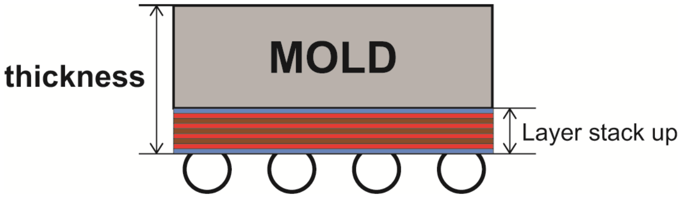

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Figure 20—Explanatory drawing of the `thickness` attribute of the module

`ref_rule_name`

> This attribute specifies the name of design rule to apply to this module which is defined by `<Physicaldesign>` element in R-Format.

8.2.3 Example

The following is an example of the `<module>` element in use.

```
<global>
    <shape>
        <rectangle id="PFGBABODY"   width="1200"  height="1200" />
        <circle id="B500" circle="500" />
    </shape>
    <padstack_def>
         <padstack id="BGABALL" type="BALLPAD">
             <ref_shape shape_id="B500" x="0" y="0" />
         </padstack>
    </padstack_def>
</global>
<module  name="BGA" type="PKG"
              shape_id="PFBGABODY" x="0" y="0" thickness="540">
   <socket  name="BGAIO" >
      <default>
          <port_shape padstack_id="BGABALL" />
      </default>
      <port id="A1" x="-1100" y="-1100" />
      <port id="A2" x="-1000" y="-1100" />
   </socket>
</module>
```

8.2.4 The <size_code> element

8.2.4.1 General

The `<size_code>` element defines the size of surface mount device (SMD). The size of SMD is indicated by a code, such as 0603. This code contains the width and height of the package. It is given in imperial or metric units.

```
<size_code
             [metric="metric_size_code"]
             [imperial="imperial_size_code"]
/>
```

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8.2.4.2 Attribute definition

The attributes of the `<size_code>` element are defined as follows.

`metric`

This attribute specifies the size code is given in metric units.

`imperial`

This attribute specifies the size code is given in imperial units.

8.2.4.3 Example

```
<module name="MAG2096xp" type="C"
        shape_id="smd0603" x="0" y="0" thickness="0.45">
   <size_code imperial="0201" metric="0603"/>

   .. .. .. .. .. .. ..

</module>
```

8.2.5 The <socket> element

8.2.5.1 General

The `<socket>` element defines the I/O ports and design constraints.

```
<socket
             name="socket_name"
>
             [ <default> element ]
             { <port> element }…
             [ <portgroup> element ]…
             [ <powerdomain_group> element ]…
             [ <swappable_port> element ]…
             [ <swappable_group> element ]…
             [ <port_assignment> element ]…
             [ <frequency> element ]…
             [ <constraint> element ]…
             [ <extensions> element ]…
</socket>
```

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The port definition includes not only logical information but also geometrical information. The logical information includes the signal direction, name, and type. The geometrical information includes the shape and location of the port, like a footprint. The design constraints provide constraints to route the signal connecting the module.

The `<socket>` element can contain the following elements:

```
<default>
<port>
<portgroup>
<powerdomain_group>
<swappable_port>
```

```
<swappable_group>
<port_assignment>
<frequency>
<constraint>
<extensions>
```

The <port> element defines the I/O port, and the <default> element defines the default shape for ports. Each port can have a different shape, but if all ports have the same shape, the <default> element can be used.

The <portgroup> element defines sets of ports that are referred to by other elements in the same file.

The <powerdomain_group> element defines the power domain of the signals that move in and out from the port of the module. The <swappable_port> and <swappable_group> elements define sets of swappable ports to each other, like double data rate 3 synchronous dynamic random access memory (DDR3 SDRAM) data bus bytes. The <frequency> element defines the operating frequency for signals that move in and out from the port of the module. The <constraint> element defines the design constraints, such as limitation of skew.

Figure 21 shows examples of sockets. In the case of a BGA package, the socket is a set of solder balls. A <module> element may have multiple <socket> elements. Diagram (b) in Figure 21 shows an example of a printed wiring board. In this example, the one card edge and the two connectors are defined as the socket.

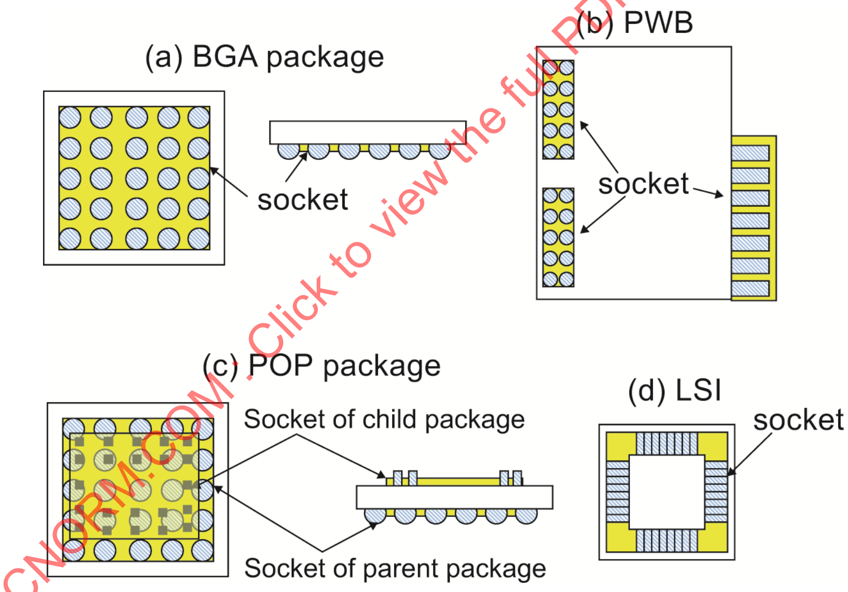

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Figure 21 —Explanatory drawing of the structure of sockets and modules

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8.2.5.2 Attribute definition

The attribute of the <socket> element is defined as follows.

name

This attribute specifies the socket name that is used to reference the socket from other attributes and elements. The socket name shall be unique in the same C-Format file.

8.2.5.3 Element content

The `<socket>` element can contain the following elements:

```
<default>
<port>
<portgroup>
<powerdomain_group>
<swappable_port>
<swappable_group>
<port_assignement>
<frequency>
<constraint>
<extensions>
```

8.2.5.4 The <default> element

8.2.5.4.1 General

The `<default>` element defines the default shapes for the port that are used when the shape is not defined in the `<port>` element.

```
<default>
             [<port_shape> element]
             [<ball_shape> element]
             [<extensions> element]…
</default>
```

The content of the `<default>` element consists of zero or one `<port_shape>` and `<ball_shape>` elements, which define the pad and solder ball shape, respectively.

8.2.5.4.2 The <port_shape> element

8.2.5.4.2.1 General

The `<port_shape>` element defines the default pad shape for the I/O port.

```
<port_shape padstack_id="identifier_of_referenced_padstack" />
```

The default is used when the `padstack_id` is not defined in the `<port>` element.

8.2.5.4.2.2 Attribute definition

The attribute of the `<port_shape>` element is defined as follows.

`padstack_id`

> This attribute specifies the identifier of the predefined padstack that is used to define the default pad shape. The referenced padstack shall be defined at the `<padstack_def>` element in the same file.

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8.2.5.4.2.3 Example

The following is an example of the `<port_shape>` element in use.

```
<global>
  <shape>
    <circle id="circ_3" diameter="1500" />
    <circle id="circ_4" diameter="750" />
  </shape>
  <padstack_def>
    <padstack id="PAD.4" >
      <ref_shape shape_id="circ_3" type="Land"
            x="0" y="0" pad_layer="TOP" />
      <ref_shape shape_id="circ_4" type="Hole"
            x="0" y="0" pad_layer="TOP" />
      <ref_shape shape_id="circ_3" type="Land"
            x="0" y="0" pad_layer="BOTTOM" />
      <ref_shape shape_id="circ_4" type="Hole"
            x="0" y="0" pad_layer="BOTTOM" />
    </padstack>
  </padstack_def>
</global>
<module name="LPB_2012_SAMPLE" type="PWB" shape_id="SHAPE.1"
             x="0" y="0" angle="0" >
  <socket  name="SMA_X1" >
    <default>
      <port_shape padstack_id="PAD.4" />
    </default>
    <port id="1" x="1570.7" y="32293.2" />
    <port id="2" x="-429.3" y="34293.2" />
    <port id="3" x="-429.3" y="30293.2" />
    <port id="4" x="3570.7" y="30293.2"/>
    <port id="5" x="3570.7" y="34293.2"/>
  </socket>
</module>
```

8.2.5.4.3 The <ball shape> element

8.2.5.4.3.1 General

The `<ball_shape>` element defines the default solder ball shape for the I/O port of the BGA package.

```
<ball_shape ball_name="name_of_referenced_ball" />
```

The default is used when the solder `ball_name` is not defined in the `<port>` element.

8.2.5.4.3.2 Attribute definition

The attribute of the `<ball_shape>` element is defined as follows.

`ball_name`

> This attribute specifies the name of the ball that is used to define the default shape of the solder ball. The referenced ball is defined at the `<ball_def>` element in the R-Format file.

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8.2.5.4.3.3 Example

The following is an example of the `<ball_shape>` element in use.

```
<ball_shape ball_name="BGA_BALL" />
```

8.2.5.5 The <port> element

8.2.5.5.1 General

The `<port>` element defines the logical and geometry information for a port of the module.

```
<port
       [id="identifier"
              [padstack_id="identifier_of_referenced_padstack"]
              [ball_name="name_of_reference_ball"]
              [x="x_coordinate" y="y_coordinate"]
              [angle="angle"]
       ]
       [name="port_name"
              [direction="signal_direction"]
              [type="port_type"]
       ]
>
              [<impedance> element]
              [<delay> element]
              [<voltage> element]
              [<max_current> element]
              [<dumping> element]
              [<decap> element]
              [<extensions> element]
</port>
```

The logical information is the port name, signal direction, and signal type. These are defined by the `name`, `direction`, and `type` attributes, respectively. The geometry information is the port identifier, port shape, and location. These are defined by the `padstack_id`, `ball_name`, `x`, `y`, and `angle` attributes. The `<port>` element can have both logical and geometry information or it can have only one type of information.

The content of the `<port>` element consists of zero or one `<impedance>`, `<delay>`, `<voltage>`, `<max_current>`, `<dumping>`, `<decap>`, and `<extensions>` elements. The actual impedance and delay are defined by `<impedance>` and `<delay>` elements. The `<voltage>` and `<max_current>` element are used to define the output voltage and current of voltage regulator or logic IC. The `<dumping>` and `<decap>` elements are used to define how to place dumping resistance and decouping capacitor.

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8.2.5.5.2 Attribute definitions

The attributes of the `<port>` element are defined as follows.

`id`

> This attribute specifies the unique identifier that is used to reference the port from other attributes and elements. The identifier shall be unique in the `<socket>` element. Normally, the `id` follows the Joint Electron Device Engineering Council's (JEDEC's) naming convention. In the case of a BGA package, the `id` might be A1, A2, A3, etc.

padstack_id

This attribute specifies the identifier of a predefined padstack to define the shape of the port. The referenced padstack shall be defined at the <padstack_def> element in the same file. If the padstack_id is not specified, the default shape that is defined in the <default> element is used.

ball_name

This attribute is used for BGA packages. Specify the name of the ball to define the shape of the solder-ball. The referenced ball is defined at the <ball_def> element in the R-Format file. If the ball_name is not specified, the default shape that is defined in the <default> element in the same <socket> element is used.

x
y

These attributes specify the location of the reference point of the referenced padstack with respect to the local origin of the module. The x and y attributes specify the x-coordinate and y-coordinate, respectively. The unit of the coordinates is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin of the module. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

name

This attribute specifies the name of a port. Normally, the port name is the same as the signal that inputs/outputs from the port. The same name can be used for different ports. For example, the ports that connect to the same ground plane can have the same port name.

direction

This attribute specifies the signal direction for a port as shown in Figure 22. The value shall be one of the followings:

in	Port that accepts signals coming in to the module
out	Port that drives signals out of the module
inout	Port that can accept signals going either in or out of the module; power and ground types of port shall be inout.

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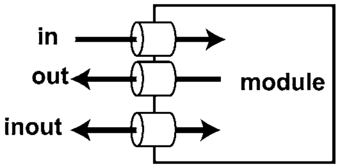

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Figure 22—Explanatory drawing of the relation of in/out/inout ports and signal direction

`type`

This attribute specifies the port type for a port. The value shall be one of the followings.

`power`	Port is used for power distribution network
`ground`	Port is used for ground distribution network
`signal`	Port is used for signal net
`floating`	Port shall not be connected to any net
`dontcare`	Port does not have any logical meanings, such as thermal ball
`through`	Port that goes completely across the module, namely, feed-through
`thermal`	Port is used for thermal network in kelvin
`thermal_c`	Port is used for thermal network in celsius

The signal direction of `floating`, `dontcare`, and `through` ports is ignored.

8.2.5.5.3 Element content

The `<port>` element can contain the following elements:

```
<impedance>
<delay>
<voltage>
<max_current>
<dumping>
<decap>
<extensions>
```

8.2.5.5.4 Example

The following is an example of the `<port>` element in use.

```
<port id="A1" x="-12500" y="12500" direction="input">
    <impedance typ="50"/>
    <delay typ="100"/>
</port>

<port id="A2" x="-11500" y="12500" direction="output">
    <impedance typ="50"/>
    <delay typ="100"/>
</port>
```

8.2.5.5.5 The <impedance> element

8.2.5.5.5.1 General

The `<impedance>` elements define the actual I/O impedance for the port.

```
<impedance typ="port_impedance" />
```

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8.2.5.5.5.2 Attribute definition

The attribute of the `<impedance>` element is as follows.

`typ`

> This attribute specifies the magnitude of the port's actual load impedance. The unit of impedance is defined by the `<impedance>` element in the `<unit>` element.

8.2.5.5.6 The <delay> element

8.2.5.5.6.1 General

The `<delay>` element defines the actual backward delay and the forward delay, which are the delays from the input port to the internal logic and vice versa.

```
<delay typ="port_delay"/>
```

8.2.5.5.6.2 Attribute definition

The attribute of the `<delay>` element is defined as follows.

`typ`

> This attribute specifies an actual delay of the port. The unit of delay is defined by the `<time>` element in the `<unit>` element.

8.2.5.5.7 The <voltage> element

8.2.5.5.7.1 General

The `<voltage>` element defines the rated output voltage of voltage regulator IC or logic IC.

```
<voltage
             typ="power_voltage"
             [ripple_rate="ripple_rate"]
/>
```

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8.2.5.5.7.2 Attribute definition

The attributes of the `<voltage>` element are defined as follows.

`typ`

> This attribute specifies the rated output voltage. In case of voltage regulator IC, this attribute expresses the voltage of output voltage pin. In case of logic IC, this attribute expresses signal voltage of output pin. The unit of voltage is defined by the `<voltage>` element in the `<unit>` element.

`ripple_rate`

This attribute defines the ripple rate of output voltage for voltage regulator IC.

8.2.5.5.8 The <max_current> element

8.2.5.5.8.1 General

The `<max_current>` element defines the maximum output current of voltage regulator IC or logic IC.

```
<max_current typ="maximum_current_consumption" />
```

8.2.5.5.8.2 Attribute definition

The attribute of the `<max_current>` element is defined as follows.

`typ`

This attribute defines the maximum output current. In case of voltage regulator IC, this attribute expresses the maximum output current at rated output voltage. In case of logic IC, this attribute expresses the maximum current value that can be taken out from the output port. The unit of current is defined by the `<current>` element in the `<unit>` element.

8.2.5.5.9 The <dumping> element

8.2.5.5.9.1 General

The `<dumping>` element defines the placement range and resistance of the dumping resistor from the port.

```
<dumping
             distance="distance_to_resistor"
             resistance="resistance"
/>
```

8.2.5.5.9.2 Attribute definition

The attributes of the `<dumping>` element are defined as follows.

`distance`

This attribute specifies the placement range of the dumping resistor from the port. The specified value is the acceptable maximum distance from the port to the dumping resistor. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

`resistance`

This attribute specifies the resistance value of the dumping resistor. The unit of resistance is defined by the `<resistance>` element in the `<unit>` element.

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8.2.5.5.10 The <decap> element

8.2.5.5.10.1 General

The <decap> element defines the placement range and value of the decap capacitor from the port.

```
<decap
             distance="distance_to_capacitor"
             capacitance="capacitance"
/>
```

8.2.5.5.10.2 Attribute definition

distance

This attribute specifies the placement range of the decap capacitor from the port. The specified value is the acceptable maximum distance from the port to the decap capacitor. The unit of distance is defined by the <distance> element in the <unit> element.

capacitor

This attribute specifies the capacitance value of the decap capacitor. The unit of capacitance is defined by the <capacitance> element in the <unit> element.

8.2.5.6 The <portgroup> element

8.2.5.6.1 General

The <portgroup> element defines groups of ports that are referenced by other elements in the same file.

```
<portgroup
             name="port_group_name"
>
             [<mustjoin/>]
             [<differential/>]
             [<ref_port> element]…
             [<ref_portgroup> element]…
             [<extensions> element]…
</portgroup>
```

A port can belong to multiple groups if necessary. The groups can nest into other groups. It is possible to create a new port group by combining several port groups.

8.2.5.6.2 Attribute definition

The attribute of the <portgroup> element is defined as follows.

name

This attribute specifies the name of the port group that is used to reference the group from other attributes and elements. The group name shall be unique in the <socket> element.

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8.2.5.6.3 Element content

The `<portgroup>` element can contain the following elements:

```
     <mustjoin>
     <differential>
     <ref_port>
     <ref_portgroup>
     <extensions>
```

8.2.5.6.4 Example

The following is an example of the `<portgroup>` element in use.

```
<portgroup name="ADD">
      <ref_port name="AD0" />
      <ref_port name="AD1" />
      <ref_port name="AD2" />
      <ref_port name="AD3" />
</portgroup>

<portgroup name="DIGITAL_GND">
    <mustjoin/>
    <ref_port name="CORE_GND" />
    <ref_port name="IO_GND" />
</portgroup>

<portgroup name="ANALOG_GND">
    <mustjoin/>
    <ref_port id="A1" />
    <ref_port id="A2" />
</portgroup>

<portgroup name="GND">
    <ref_portgroup name="DIGITAL_GND" />
    <ref_portgroup name="ALALOG_GND" />
</portgroup>
```

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8.2.5.6.5 The <mustjoin> element

If `<mustjoin/>` is contained in the `<port group>` element, the port in the group shall be connected together.

```
<mustjoin/>
```

8.2.5.6.6 The <differential> element

If `<differential/>` is contained in the `<port_group>` element, the port in the group is differential signal.

```
<differential/>
```

8.2.5.6.7 The <ref_port> element

8.2.5.6.7.1 General

The `<ref_port>` element refers to the port that makes up the group.

```
<ref_port
                { id="identifier_of_referenced_port" |
                 name="name_of_referenced_port" }
                 [polarity="polarity"]
/>
```

The port shall be specified with either the name (`name`) or the identifier (`id`). The referred port shall be defined in the same `<socket>` element.

8.2.5.6.7.2 Attribute definitions

The attributes of the `<ref_port>` element are defined as follows.

`id`

This attribute specifies the identifiers of the predefined ports that make up the group. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `id` attribute shall not be used with the `name` attribute.

`name`

This attribute specifies the names of the predefined ports that make up the group. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `name` attribute shall not be used with the `id` attribute. If multiple same-name ports exist, these ports belong to the same group.

`polarity`

This attribute specifies the polarity of the differential signal.

`NEGATIVE`	Negative signal
`POSITIVE`	Positive signal

8.2.5.6.8 The <ref_portgroup> element

8.2.5.6.8.1 General

A port group can nest into another port group. The `<ref_portgroup>` element refers to the other port group.

```
<ref_portgroup
               name="name_of_referenced_port_group"
/>
```

The referenced port group shall be defined in the same `<socket>` element.

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8.2.5.6.8.2 Attribute definition

The attribute of the `<ref_portgroup>` element is defined as follows.

`name`

> This attribute specifies the name of the predefined port group that makes up the nested group. The specified port group shall be defined in the same `<socket>` element.

8.2.5.7 The <powerdomain_group> element

8.2.5.7.1 General

The `<powerdomain_group>` element defines the power domain of the signals that move in and out from the port of the module.

```
<powerdomain_group
             {port_name="name_of_referenced_port" |
             port_id="identifier_of_referenced_port" |
             group_name="name_of_referenced_port_group"}
             [min="minimum_voltage"]
             [typ="typical_voltage"]
             [max="maximum_voltage"]
             {pwr_port_name="name_of_referenced_power_port" |
              pwr_port_id="identifier_of_referenced_power_port" |
              pwr_group_name="name_of_referenced_power_port_group"}
             [pwr_min="minimum_power_voltage"]
             [pwr_typ="typical_power_voltage"]
             [pwr_max="maximum_power_voltage"]
             {gnd_port_name="name_of_referenced_ground_port" |
              gnd_port_id="identifier_of_referenced_ground_port" |
              gnd_group_name="name_of_referenced_ground_port_group"}
             [gnd_min="minimum_ground_voltage"]
             [gnd_typ="typical_ground_voltage"]
             [gnd_max="maximum_ground_voltage"]
             [ripple_rate="ripple_rate"]
>
             [<ref_portgroup> element]
             [<ref_port> element]
             [<extensions> element]…
</powerdomain_group>
```

For example, in the case of analog-digital mixed design, this element specifies the analog power/ground and analog signals that make up the power domain in order to distinguish them from the digital. The port shall be specified with either the port name (`port_name`), port identifier (`port_id`), or port group name (`group_name`). The referenced port or port group shall be defined in the same `<socket>` element.

8.2.5.7.2 Attribute definitions

The attributes for the `<powerdomain_group>` element are defined as follows.

`pwr_port_name`

> This attribute specifies the name of the power port that defines the voltage level of the power domain. The referenced power port shall be defined at the `<port>` element in the same `<socket>` element, and the port type shall be `power`. The `pwr_port_name` attribute shall not be used with the `pwr_port_id` and `pwr_group_name` attributes.

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pwr_port_id

This attribute specifies the identifier of the power port that defines the voltage level of the power domain. The referenced power port shall be defined at the <port> element in the same <socket> element, and the port type shall be power. The pwr_port_id attribute shall not be used with the pwr_port_name and pwr_group_name attributes.

pwr_port_group

This attribute specifies the name of the power port group that defines the voltage level of the power domain. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The type of the ports that belong to the group shall be power. The pwr_group_name attribute shall not be used with the pwr_port_name and pwr_port_id attributes.

gnd_port_name

This attribute specifies the name of the ground port that defines the voltage level of the power domain. The referenced ground port shall be defined at the <port> element in the same <socket> element, and the port type shall be ground. The gnd_port_name attribute shall not be used with the gnd_port_id and gnd_group_name attributes.

gnd_port_id

This attribute specifies the identifier of the ground port that defines the voltage level of the power domain. The referenced ground port shall be defined at the <port> element in the same <socket> element, and the port type shall be ground. The gnd_port_id attribute shall not be used with the gnd_port_name and gnd_group_name attributes.

gnd_port_group

This attribute specifies the name of the ground port group that defines the voltage level of the power domain. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The type of the ports that belong to the group shall be ground. The gnd_group_name attribute shall not be used with the gnd_port_name and gnd_port_id attributes.

pwr_typ

This attribute specifies the typical power voltage level. The voltage perturbation is specified by min and max attributes. The unit of voltage is defined by the <voltage> element in the <unit> element.

pwr_min
pwr_max

These attributes specify the power voltage perturbation level. The pwr_max and pwr_min attributes are the maximum and minimum power voltage, respectively. The unit of voltage is defined by the <voltage> element in the <unit> element.

gnd_typ

This attribute specifies the typical ground voltage level. The voltage perturbation is specified by min and max attributes. The unit of voltage is defined by the <voltage> element in the <unit> element.

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gnd_min
gnd_max

These attributes specify the ground voltage perturbation level. The gnd_max and gnd_min attributes are the maximum and minimum ground voltage, respectively. The unit of voltage is defined by the <voltage> element in the <unit> element.

ripple_rate

This attribute defines the allowable ripple rate of the power domain.

For backward compatibility, the following attributes were still remained. But using the following attributes is not recommended. In future revisions of this standard, the following attributes will be removed.

port_name

This attribute specifies the name of the power or ground port that defines the voltage level of the power domain. The referenced power or ground port shall be defined at the <port> element in the same <socket> element, and the port type shall be power or ground. The port_name attribute shall not be used with the port_id and group_name attributes.

port_id

This attribute specifies the identifier of the power or ground port that defines the voltage level of the power domain. The referenced power or ground port shall be defined at the <port> element in the same <socket> element, and the port type shall be power or ground. The port_id attribute shall not be used with the port_name and group_name attributes.

group_name

This attribute specifies the name of the port group that defines the voltage level of the power domain. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The type of the ports that belong to the group shall be power or ground. The group_name attribute shall not be used with the port_name and port_id attributes.

typ

This attribute specifies the typical voltage level. The voltage perturbation is specified by min and max attributes. The unit of voltage is defined by the <voltage> element in the <unit> element.

min
max

These attributes specify the voltage perturbation level. The max and min attributes are the maximum and minimum voltage, respectively. The unit of voltage is defined by the <voltage> element in the <unit> element.

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8.2.5.7.3 Element content

The <powerdomain_group> element can contain the following elements:

```
<ref_portgroup>
<ref_port>
<extensions>
```

8.2.5.7.4 Example

The following is an example of the `<powerdomain_group>` element in use.

```
<portgroup name="DDR_DIG"/>
  <ref_port name="PL1"/>
  <ref_port name="PL2"/>
  <ref_port name="PL3"/>
  <ref_port name="PL4"/>
</portgroup>

<powerdomain_group  pwr_port_name="DCDC"  pwr_typ="2.5"
                    gnd_port_name="PGND"  gnd_typ="0.0">
    <ref_portgroup name="DDR_DIG"/>
</powerdomain_group>
```

8.2.5.7.5 The <ref_portgroup> element

8.2.5.7.5.1 General

The `<ref_portgroup>` element refers to the signal port group that belongs to the power domain.

```
<ref_portgroup
             name="name_of_referenced_port_group"
/>
```

The referenced port group shall be defined in the same `<socket>` element.

8.2.5.7.5.2 Attribute definition

The attribute of the `<ref_portgroup>` element is defined as follows.

`name`

> This attribute specifies the name of the predefined signal port group that belongs to the power domain. The ports that are included in the same group belong to the same power domain. The specified port group shall be defined in the same `<socket>` element.

8.2.5.7.6 The <ref_port> element

8.2.5.7.6.1 General

The `<ref_port>` element refers to the signal port that belongs to the power domain.

```
<ref_port
             { id="identifier_of_referenced_port" |
               name="name_of_referenced_port" }
/>
```

The port shall be specified with either the name (`name`) or the identifier (`id`). The referenced port shall be defined in the same `<socket>` element.

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8.2.5.7.6.2 Attribute definitions

The attributes of the `<ref_port>` element are defined as follows.

`id`

This attribute specifies the identifiers of the predefined signal port that belongs to the power domain. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `id` attribute shall not be used with the `name` attribute.

`name`

This attribute specifies the name of the predefined signal port that belongs to the power domain. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `name` attribute shall not be used with the `id` attribute. If multiple same-name ports exist, these ports belong to the same power domain.

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8.2.5.8 The <swappable_port> element

8.2.5.8.1 General

The `<swappable_port>` element defines sets of swappable ports, such as DDR3 data bus bytes.

```
<swappable_port>
             <ref_port> element
             {<ref_port> element}…
             [<extensions> element]…
</swappable_port>
```

The `<swappable_port>` element contains two or more `<ref_port>` elements. The nets that are connected to the swappable ports that are defined by the `<ref_port>` element can replace each other in the connection. For example, if the swappable CK_N and CK_P shown in Figure 23 are connected to n1 and n2, respectively, you can swap the connection of CK_N and CK_P.

8.2.5.8.2 Element content

The `<swappable_port>` element contains the following elements:

```
<ref_port>
<extensions>
```

8.2.5.8.3 Example

The swappable ports shown in Figure 23 are represented by the following code:

```
<swappable_port>
   <ref_port name="CK_N" />
   <ref_port name="CK_P" />
</swappable_port>
```

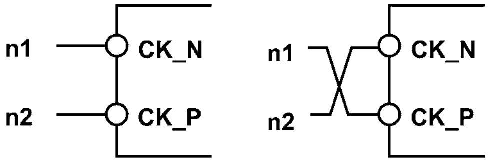

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Figure 23—Example of swappable ports

8.2.5.8.4 The <ref_port> element

8.2.5.8.4.1 General

The `<ref_port>` element refers to the ports that make up the swappable port group.

```
<ref_port
             {id="identifier_of_referenced_port" |
              name="name_of_reference_port" }
/>
```

The port shall be specified with either the name (`name`) or the identifier (`id`) attribute. The referenced port group shall be defined in the same `<socket>` element.

8.2.5.8.4.2 Attribute definitions

The attributes of the `<ref_port>` element are as follows.

`id`

> This attribute specifies the identifier of the predefined ports that make up a set of swappable ports. The specified ports shall be defined at the `<port>` element in the same `<socket>` element. The `id` attribute shall not be used with the `name` attribute.

`name`

> This attribute specifies the names of the predefined ports that make up a set of swappable ports. The specified ports shall be defined at the `<port>` element in the same `<socket>` element. The `name` attribute shall not be used with the `id` attribute.

8.2.5.9 The <port_assignement> element

8.2.5.9.1 General

The port_assignment is used to define the signals to be assigned to the physical ports.

```
<port_assignment>
             {<ref_port_by_id> element}…
             {<ref_port_by_name> element}…
             [<extensions> element]…
</port_assignment>
```

The physical ports are defined by port element with `id` attribute. On the other hand, the signal that is assigned to the physical port is defined by the `name` attribute in the port element. The port element without `name` attribute means that a signal has not been assigned yet. The port element without an `id` attribute means that physical ports have not been defined for the signal. The `<port_assignment>` consists of the following two elements:

```
<ref_port_by_id>
<ref_port_by_name>
```

A `<ref_port_by_id>` element refers a port by id attribute, thus a physical port is referred. A `<ref_port_by_name>` element refers a port by name attribute, thus a signal is referred. The implication of the `<port_assignment>` is that the referred signals can be assigned to the physical ports, the referred signals shall not be assigned to other physical ports, and other signals shall not be assigned to the referred physical ports.

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8.2.5.9.2 The <ref_port_by_id>

8.2.5.9.2.1 General

The <ref_port_by_id> element defines physical ports for which signal have not been assigned yet.

```
<ref_port_by_id id="identifier_of_referenced_port"/>
```

This element refers a unique <port> element in the same <socket> element by id attribute. If the referred <port> element is already assigned to a signal, the assignment shall be regarded as tentative.

8.2.5.9.2.2 Attribute definition

The attribute for the <ref_port_by_id> element is defined as follows.

id

> This attribute specifies the identifier of the predefined. The specified ports shall be defined at a <port> element in the same <socket> element.

8.2.5.9.3 The <ref_port_by_name>

8.2.5.9.3.1 General

The <ref_port_by_name> element defines a signal that has not yet been assigned to a physical port.

```
<ref_port_by_name name="name_of_reference_signal"/>
```

This element refers one or more <port> elements in the same <socket> element by specifying a signal name. If the signal is already assigned to one or more physical ports in the <socket> element, the assignment shall be regarded as tentative.

8.2.5.9.3.2 Attribute definition

The attribute for the <ref_port_by_name> element is defined as follows:

name

> This attribute specifies a signal name that shall be used as the name attribute value in the <port> element in the same <socket> element.

8.2.5.9.4 Example

```
<socket name="example_socket1">
  <port id="A1" x="0" y="0" shape_id="port_shape1"
     name="sig1" direction="in"/>
  <port id="A2" x="1" y="0" shape_id="port_shape1"
     name="sig3" direction="out"/>
  <port id="A3" x="1" y="1" shape_id="port_shape1"
     name="sig2" direction="in"/>
  <port id="A4" x="0" y="1" shape_id="port_shape1"
     name="sig4" direction="out"/>
```

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```
<port_assignment>
    <ref_port_by_id id="A1"/>
    <ref_port_by_id id="A2"/>
    <ref_port_by_name name="sig1"/>
    <ref_port_by_name name="sig3"/>
</port_assignment>
<port_assignment>
    <ref_port_by_id id="A3"/>
    <ref_port_by_id id="A4"/>
    <ref_port_by_name name="sig2"/>
    <ref_port_by_name name="sig4"/>
</port_assignment>
```

8.2.5.10 The <swappable_group> element

8.2.5.10.1 General

The <swappable_group> element defines sets of swappable port groups.

```
<swappable_group>
             <ref_portgroup> element
             {<ref_portgroup> element}…
             [<extensions> element]…
</swappable_group>
```

The port groups in the same <swappable_group> element are swappable by a group unit (see Figure 24 and Figure 25). The <swappable_group> contains two or more <ref_portgroup> elements. The nets that are connected to the swappable port groups defined by <ref_portgroup> element can replace each other in the connection by group unit. If the port count matches in the all <ref_portgroup> elements, the order of the nets shall be maintained in the replacement.

8.2.5.10.2 Element content

The <swappable_group> element contains the following elements:

```
<ref_portgroup>
<extensions>
```

8.2.5.10.3 Example

The swappable group shown in Figure 24 is represented by the following code:

```
<portgroup name="R_CHANNEL">
   <ref_port name="RAD1" />
   <ref_port name="RAD2" />
   <ref_port name="RAD3" />
</portgroup>
<portgroup name="L_CHANNEL" />
   <ref_port name="LAD1" />
   <ref_port name="LAD2" />
   <ref_port name="LAD3" />
</portgroup>

<swappable_group>
   <ref_portgroup name="R_CHANNEL" />
   <ref_portgroup name="L_CHANNEL" />
</swappable_group>
```

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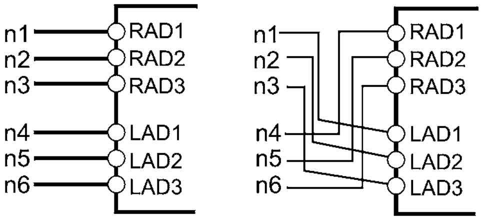

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Figure 24—Example of a swappable group

The swappable group shown in Figure 25 is represented by the following code:

```
<portgroup name="RCHA_1">
   <ref_port name="RAD1" />
   <ref_port name="RAD2" />
</portgroup>
<portgroup name="RCHA_2">
   <ref_port name="RAD3" />
   <ref_port name="RAD3" />
</portgroup>
<portgroup name="R_CHANNEL" />
   <ref_portgroup="RCHA_1" />
   <ref_portgroup="RCHA_2" />
</portgroup>
<portgroup name="L_CHANNEL" />
   <ref_port name="LAD1" />
   <ref_port name="LAD2" />
   <ref_port name="LAD3" />
   <ref_port name="LAD4" />
</portgroup>
<swappable_group>
   <ref_portgroup name="R_CHANNEL" />
   <ref_portgroup name="L_CHANNEL" />
</swappable_group>
```

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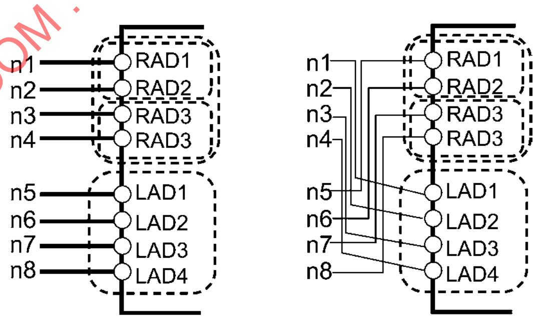

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Figure 25—Example of a swappable group

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8.2.5.10.4 The <ref_portgroup> element

8.2.5.10.4.1 General

The `<ref_portgroup>` element refers to two or more port groups.

```
<ref_portgroup
             name="group_name_of_reference_port"
/>
```

The ports belonging to the referenced groups can be swapped. For example, if the following two port groups, `AGRP` and `BGRP`, are swappable groups, ports `A0` and `B0`, `A1` and `B1`, and `A2` and `B2` are swappable, respectively.

```
<portgroup name="AGRP">
   <ref_port name="A0" />
   <ref_port name="A1" />
   <ref_port name="A2" />
</portgroup>

<portgroup name="BGRP">
   <ref_port name="B0" />
   <ref_port name="B1" />
   <ref_port name="B2" />
</portgroup>
```

8.2.5.10.4.2 Attribute definition

The attribute for the `<ref_portgroup>` element is defined as follows.

`name`

> This attribute specifies the name of the predefined port groups that make up a set of swappable ports. The specified port groups shall be defined in the same `<socket>` element.

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8.2.5.11 The <frequency> element

8.2.5.11.1 General

The `<frequency>` element defines the minimum, typical, and maximum operating frequencies for signals that move in and out of the port of the module.

```
<frequency
             { port_name="name_of_reference_port" |
              port_id="identifier_of_reference_port" |
              group_name="identifier_of_reference_port_group" }
             min="minimum_frequency"
             [typ="typical_frequency"]
             max="maximum_frequency"
>
             [<extensions> element]…
</frequency>
```

The port shall be specified with either the port name (`port_name`), port identifier (`port_id`), or group name (`group_name`).

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8.2.5.11.2 Attribute definitions

The attributes of the `<frequency>` element are defined as follows.

`port_name`

> This attribute specifies the name of a predefined port for inputting and outputting a signal that defines the operating frequency. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_name` attribute shall not be used with the `port_id` nor `group_name` attributes.

`port_id`

> This attribute specifies the identifier of a predefined port for inputting and outputting a signal that defines the operating frequency. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_id` attribute shall not be used with the `port_name` nor `group_name` attributes.

`group_name`

> This attribute specifies the name of a group that includes ports for inputting and outputting a signal that defines the operating frequency. The ports included in the specified group are operating at the same frequency. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. The `group_name` attribute shall not be used with the `port_name` nor `port_id` attributes.

`typ`

> This attribute specifies the typical frequency. The frequency perturbation is specified by `min` and `max` attributes. The unit of frequency is defined by the `<frequency>` element in the `<unit>` element.

`min`
`max`

> These attributes specify the frequency perturbation. The `max` and `min` attributes are the maximum and minimum frequencies, respectively. The unit of frequency is defined by the `<frequency>` element in the `<unit>` element.

8.2.5.11.3 Example

The following is an example of the `<frequency>` element in use.

```
  <frequency port_name="FKBCLK" min="50" max="55" />
```

8.2.5.12 The <constraint> element

8.2.5.12.1 General

The `<constraint>` element defines the design constraints, such as limitation of skew.

```
<constraint>
              [<impedance> element]
              [<delay> element]
              [<skew> element]
              [<guard_shield> element]
              [<extensions> element]…
</constraint>
```

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The <constraint> element consists of one or more <impedance>, <delay>, <skew>, and <guard_shield> elements.

8.2.5.12.2 Element content

The <constraint> element can contain the following elements:

```
<impedance>
<delay>
<skew>
<guard_shield>
<extensions>
```

8.2.5.12.3 The <impedance> element

8.2.5.12.3.1 General

The <impedance> element defines the minimum, typical, and maximum characteristic impedances for the port that requests impedance matching.

```
<impedance
             { port_name="name_of_reference_port" |
              port_id="identifier_of_referenced_port" |
              group_name="name_of_reference_port_group"  }
             [type="impedance_type"]
             [min="minimum_impedance"]
             typ="typical_impedance"
             [max="maximum_impedance"]
/>
```

The port shall be specified with either the port name (port_name), port identifier (port_id), or group name (group_name) attribute.

8.2.5.12.3.2 Attribute definitions

The attributes for the <impedance> element are defined as follows.

port_name

> This attribute specifies the name of a predefined port for inputting and outputting a signal that requests impedance matching. The specified port shall be defined at the <port> element in the same <socket> element. The port_name attribute shall not be used with the port_id nor group_name attributes.

port_id

> This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests impedance matching. The specified port shall be defined at the <port> element in the same <socket> element. The port_id attribute shall not be used with the port_name nor group_name attributes.

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group_name

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests impedance matching. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The group_name attribute shall not be used with the port_name nor port_id attributes.

type

This attribute specifies the type of the characteristic impedance. The value shall be one of the followings:

single	Single-ended signal
differential	Differential mode impedance
common	Common mode impedance

If the type attribute is not defined, single is set as the default.

typ

This attribute specifies the typical impedance value. The impedance perturbation is specified by the min and max attributes. The unit of impedance is defined by the <impedance> element in the <unit> element.

min
max

These attributes specify the impedance perturbation. The max and min attributes are the maximum and minimum impedance values, respectively. The unit of impedance is defined by the <impedance> element in the <unit> element.

8.2.5.12.3.3 Example

The following is an example of the <impedance> element in use.

```
<portgroup name="CK">
   <ref_port port_name="CK_N" />
   <ref_port port_name="CK_P" />
</portgroup>
<constraint>
 <impedance port_name="DQ1" type="single" min="45" typ="50" max="55" />
 <impedance port_id="A1" type="single" typ="50" />
 <impedance group_name="CK" type="differential" typ="100" />
</constraint>
```

8.2.5.12.4 The <delay> element

8.2.5.12.4.1 General

The <delay> element defines the minimum, typical, and maximum delay values for the port that requests a timing constraint.

```
<delay
             { port_name="name_of_referenced_port" |
```

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```
               port_id="identifier_of_referenced_port" |
               group_name="name_of_referenced_port_group"}
              [min="minimum_delay"]
              typ="typical_delay"
              [max="maximum_delay"]
/>
```

The port shall be specified with the port name (`port_name`), port identifier (`port_id`), or group name (`group_name`) attribute.

8.2.5.12.4.2 Attribute definitions

The attributes of the `<delay>` element are defined as follows.

`port_name`

> This attribute specifies the name of a predefined port for inputting and outputting a signal that requests a timing constraint. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_name` attribute shall not be used with the `port_id` nor `group_name` attributes.

`port_id`

> This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests a timing constraint. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_id` attribute shall not be used with the `port_name` nor `group_name` attributes.

`group_name`

> This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests a timing constraint. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. The `group_name` attribute shall not be used with the `port_name` nor `port_id` attributes.

`typ`

> This attribute specifies the typical delay value. The delay time perturbation is specified by `min` and `max` attributes. The unit of delay is defined by the `<time>` element in the `<unit>` element.

`min`
`max`

> These attributes specify the delay time perturbation. The `max` and `min` attributes are the maximum and minimum delay values, respectively. The unit of delay is defined by the `<time>` element in the `<unit>` element.

8.2.5.12.4.3 Example

The following is an example of the `<delay>` element in use.

```
<portgroup name="BUS">
   <ref_port port_name="SIG1" />
   <ref_port port_name="SIG2" />
```

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```
   <ref_port port_name="SIG3" />
</portgroup>
<constraint>
 <delay port_name="CLK" min="10" typ="12" max="15" />
 <delay port_id="D3"  typ="5" />
 <delay group_name="BUS"  min="50" typ="55" max="60"/>
</constraint>
```

8.2.5.12.5 The <skew> element

8.2.5.12.5.1 General

The <skew> element defines the skew constraint for signals that input and output from the specified port.

```
<skew
             { port_name="name_of_port" |
              port_id="identifier_of_port" |
              group_name="name_of_port_group" }
             [ reference_port_name="name_of_referenced_port" |
             reference_port_id="identifier_of_referenced_port" ]
             [min="minimum_time"]
             [max="maximum_time"]
/>
```

The port shall be specified with either the port name (port_name), port identifier (port_id), or group name (group_name) attribute.

When the reference signal is specified, the skew constraint is defined by a maximum time (max) and a minimum time (min). In this case, the specified maximum and minimum times are based on the propagation time of the reference signal that inputs or outputs from the specified reference port (reference_port_name, reference_port_id). The propagation time of signals having a skew constraint is required to be between the minimum time and the maximum one (see Figure 26).

```
<portgroup name="skewset1">
 <ref_port name="port1" />
 <ref_port name="port2" />
 <ref_port name="port3" />
</portgroup>
<skew group_name="skewset1" reference_port_name="port0"
     min="-5" max="10"/>
```

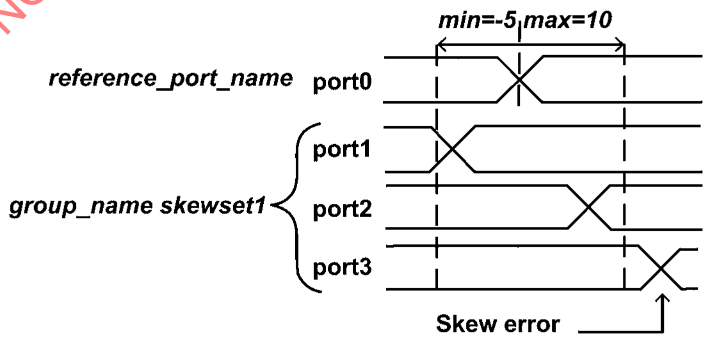

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Figure 26—Sample of skew constraint with min and max attributes

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When the reference signal is not specified, the skew constraint is defined by either the maximum time (max) or minimum time (min). If the maximum time is defined, a signal having the fastest propagation time is used as the reference signal (see Figure 27).

```
<portgroup name="skewset2">
 <ref_port name="port4" />
 <ref_port name="port5" />
 <ref_port name="port6" />
</portgroup>
<skew group_name="skewset2" max="5" />
```

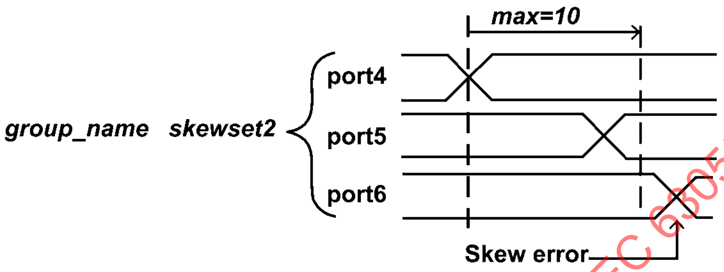

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Figure 27 —Sample of skew constraint with only max attribute

If only a minimum time (min) is defined, a signal having the slowest propagation time is used as the reference signal (see Figure 28).

```
<portgroup name="skewset3">
 <ref_port name="port7" />
 <ref_port name="port8" />
 <ref_port name="port9" />
</portgroup>
<skew group_name="skewset3" min="-10" />
```

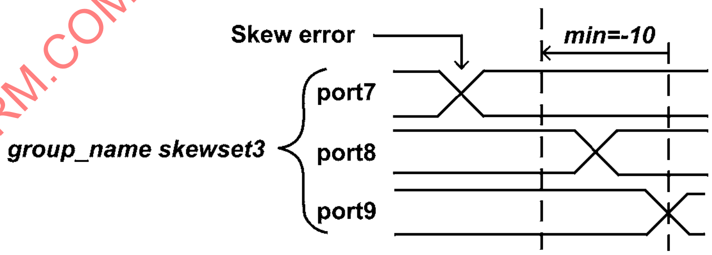

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Figure 28 —Sample of skew constraint with only min attribute

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8.2.5.12.5.2 Attribute definitions

The attributes of the `<skew>` element are defined as follows.

`port_name`

> This attribute specifies the name of a predefined port for inputting and outputting a signal that requests a skew constraint. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_name` attribute shall not be used with the `port_id` nor `group_name` attributes.

`port_id`

> This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests a skew constraint. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_id` attribute shall not be used with the `port_name` nor `group_name` attributes.

`group_name`

> This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests a skew constraint. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. The `group_name` attribute shall not be used with the `port_name` nor `port_id` attributes.

`reference_port_name`

> This attribute specifies the name of a predefined port for inputting and outputting a reference signal for a skew constraint. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `reference_port_name` attribute shall not be used with the `reference_port_id` attribute.

`reference_port_id`

> This attribute specifies the identifier of a predefined port for inputting and outputting a reference signal for a skew constraint. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `reference_port_id` attribute shall not be used with the `reference_port_id` attribute.

`min`
`max`

> The `max` and `min` attributes specify maximum and minimum skew time, respectively. Set a positive value for the max attribute and a negative value for the min attribute. When a reference signal is specified by `reference_port_name` or `reference_port_id` attribute, `min` and `max` attributes shall be used together. When a reference signal is not specified, either `min` or `max` attribute shall be used. The unit of minimum and maximum skew time is defined by the `<time>` element in the `<unit>` element.

8.2.5.12.5.3 Example

Assume that a semiconductor designer delivers a chip with a differential skew constraint. The following code is an example of a differential skew constraint of 10 ps provided by a semiconductor designer. The package designer routes differential signal according to this constraint.

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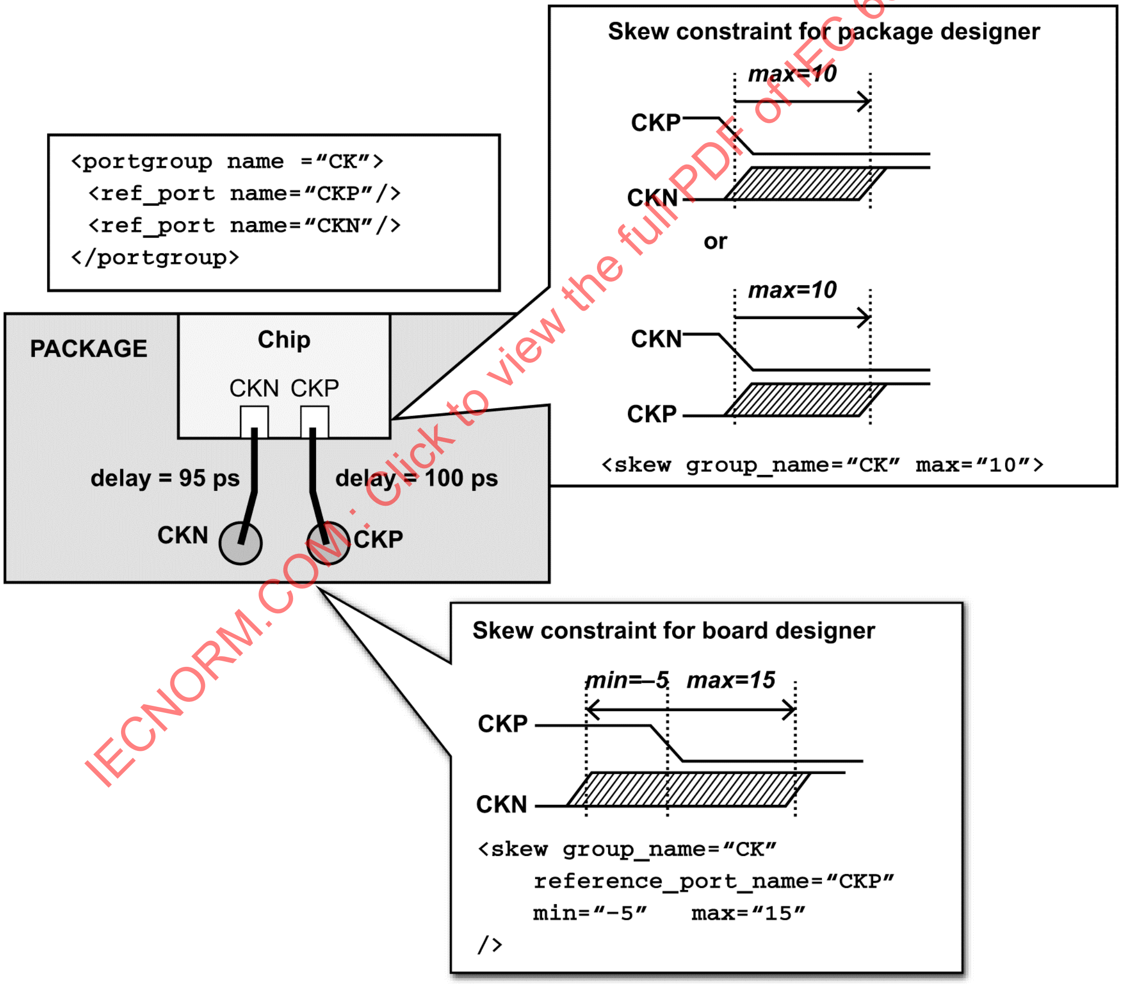
```
<portgroup name="CK">
   <ref_port name="CKP" />
   <ref_port name="CKN" />
</portgroup>
<skew group_name="CK"  max="10" />
```

If the package designer routes CKP with 100 ps delay and CKN with 95 ps delay, the minimum and maximum skew constraints based on CKP for board designers are −5 ps and 15 ps respectively. The following code and Figure 29 are examples of the skew constraint for the board designer.

```
<portgroup name="CK">
   <ref_port name="CKP" />
   <ref_port name="CKN" />
</portgroup>
<skew group_name="CK" reference_port_name="CKP" min="-5" max="15"
/>
```



```
<portgroup name ="CK">
 <ref_port name="CKP"/>
 <ref_port name="CKN"/>
</portgroup>
```

```
<skew group_name="CK" max="10">
```

```
<skew group_name="CK"
    reference_port_name="CKP"
    min="-5"   max="15"
/>
```

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Figure 29—Example of a skew constraint for a differential clock

8.2.5.12.6 The <guard_shield> element

8.2.5.12.6.1 General

The <guard_shield> element defines a signal used for a shield, and signals requiring a shield.

```
<guard_shield
              { port_name="name_of_port_requiring_shield" |
               port_id="identifier_of_port_requiring_shield" |
               group_name="name_of_port_group_requiring_shield" }
              { shieldnet_port_name="name_of_port_using_shield"  |
               shieldnet_port_id="identifier_of_port_using_shield"  |
               shieldnet_port_group_name="name_of_port_group_using_shield" }
/>
```

For example, in the case of analog-digital mixed design, it would be better to shield the analog signal by analog ground. The <guard_shield> element is used to define the combination of shielding signals.

8.2.5.12.6.2 Attribute definitions

The attributes of the <guard_shield> element are defined as follows.

port_name

> This attribute specifies the name of a predefined port for inputting and outputting a signal that requests a shield. The specified port shall be defined at the <port> element in the same <socket> element. The port_name attribute shall not be used with the port_id nor group_name attributes.

port_id

> This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests a shield. The specified port shall be defined at the <port> element in the same <socket> element. The port_id attribute shall not be used with the port_name nor group_name attributes.

group_name

> This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests a shield. The specified port group shall be defined at the <portgroup> element in the same <socket> element. If multiple ports with the same name exist, the signals that input or output from these ports shall be shielded. The group_name attribute shall not be used with the port_name nor port_id attributes.

shieldnet_port_name

> This attribute specifies the name of a predefined port for inputting and outputting a signal that is used for shielding. The specified port shall be defined at the <port> element in the same <socket> element. The shieldnet_port_name attribute shall not be used with the shieldnet_port_id nor shieldnet_port_group_name attributes.

shieldnet_port_id

> This attribute specifies the identifier of a predefined port for inputting and outputting a signal that is used for shielding. The specified port shall be defined at the <port> element in the same <socket> element. The shieldnet_port_id attribute shall not be used with the shieldnet_port_name nor shieldnet_port_group_name attributes.

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`shieldnet_port_group_name`

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that is used for shielding. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. If multiple ports with the same name exist, any signals that are input or output from these ports can be used for shielding. The `shieldnet_port_group_name` attribute shall not be used with the `shieldnet_port_name` nor `shieldnet_port_id` attributes.

8.2.5.12.6.3 Example

The example of a guard shield in Figure 30 is represented by the following code. VSS is the guard net and CLK is the shielded net:

```
<guard_shield port_name="CLK" shieldnet_port_name="VSS" />
```

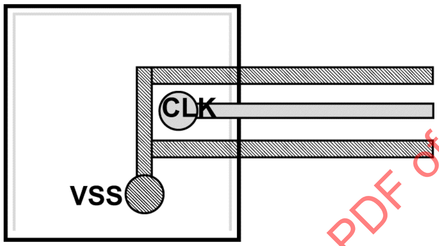

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Figure 30 —Example of a guard shield for a clock signal

8.2.6 The <guideline> element

8.2.6.1 General

The `<guideline>` element defines the guideline about the wiring design inside the `<module>`. The `<net>` element is introduced under the `<netgroup>`, and it has the `name` attribute. The `<net name>` is corresponding to the wire name in N-Format which defines net inside the module.

```
<guideline>
              [<netgroup> element]…
              [<impedance> element]…
              [<delay> element]…
              [<skew> element]…
              [<width> element]…
              [<length> element]…
              [<clearance> element]…
              [<gap> element]…
              [<enclosure> element]…
              [<keepout> element]…
              [<extension> element]…
</guideline>
```

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8.2.6.2 Element content

The `<guideline>` element can contain the following elements:

```
     <netgroup>
     <impedance>
     <delay>
     <skew>
     <guard shield>
     <width>
     <length>
     <clearance>
     <gap>
     <enclosure>
     <keepout>
     <extension>
```

8.2.6.3 The <netgroup> element

8.2.6.3.1 General

The `<netgroup>` element defines a group of nets like a BUS signal. And it is also used to define differential signals and connections of the same voltage groups.

```
<netgroup
             name="net_group_name"
>
             [<mustjoin/>]
             [<differential/>]
             [<ref_net> element]…
             [<ref_netgroup> element]…
             [<extensions> element]…
</netgroup>
```

8.2.6.3.2 Attribute definition

The attributes of the `<netgroup>` element are defined as follows.

`name`

> This attribute specifies the netgroup name that is used to refer the netgroup from other attributes and elements. The name shall be unique in the individual C-Format file.

8.2.6.3.3 Element content

The `<netgroup>` element can contain the following elements:

```
     <mustjoin>
     <differential>
     <ref_net>
     <ref_netgroup>
     <extensions>
```

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8.2.6.3.4 The <mustjoin> element

When the `<mustjoin>` element is specified, nets in the group must be connected together in the module.

```
<mustjoin/>
```

8.2.6.3.5 The <differential> element

Which `<differential>` element is specified indicates nets in the group that make up the differential signal.

```
<differential/>
```

8.2.6.3.6 The <ref_net> element

8.2.6.3.6.1 General

The `<ref_net>` element specifies the nets which make up the `<netgroup>`. The `<ref_net>` is corresponding to the wire in N-Format.

```
<ref_net
             name="net_name"
             [polarity="polarity"]
/>
```

The `<ref_net>` element can be referred from one or more groups.

8.2.6.3.6.2 Attribute definitions

The attributes of the `<ref_net>` element are defined as follows.

`name`

> This attribute specifies the net name that is used to refer the net from other attributes and elements. The `name` is corresponding to the wire name in the module of N-Format. The net name shall be unique in the individual C-Format file.

`polarity`

This attribute specifies the differential signal polarity. The `polarity` shall be one of `POSITIVE` or `NEGATIVE`.

8.2.6.3.6.3 Example

The following is an example of the <netgroup> in use to define the `<netgroup>`.

```
<netgroup name="CLOCK">
   <differential/>
   <ref_net name="CKN" polarity="NEGATIVE" />
   <ref_net name="CKQ" polarity="POSITIVE"/>
</netgroup>
```

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```
<netgroup name="ADDRESS">
   <ref_net name="RADDR0" />
   <ref_net name="RADDR1" />
   <ref_net name="RADDR2" />
   <ref_net name="RADDR3" />
   <ref_net name="RADDR4" />
   <ref_net name="RADDR5" />
   <ref_net name="RADDR6" />
   <ref_net name="RADDR7" />
</netgroup>

<netgroup name="GND">
   <mustjoin/>
   <ref_net name="GND1"/>
   <ref_net name="GND2"/>
</netgroup>
```

8.2.6.3.7 The <ref_netgroup> element

8.2.6.3.7.1 General

The `<ref_netgroup>` element is used to describe the nest structure of `<netgroup>`.

```
<ref_netgroup name="name_of_referenced_netgroup" />
```

8.2.6.3.7.2 Attribute definitions

The attribute of the `<ref_netgroup>` element is defined as follows.

`name`

> This attribute specifies the netgroup name that is used to reference the netgroup from other attributes and elements. The netgroup name shall be unique in the individual C-Format file.

8.2.6.3.7.3 Example

```
   <netgroup name="ADDRESS_G0">
      <ref_net name="RADDR0" />
      <ref_net name="RADDR1" />
      <ref_net name="RADDR2" />
      <ref_net name="RADDR3" />
   </netgroup>
      <netgroup name="ADDRESS_G1">
      <ref_net name="RADDR4" />
      <ref_net name="RADDR5" />
      <ref_net name="RADDR6" />
      <ref_net name="RADDR7" />
   </netgroup>
   <netgroup name="ADDRESS">
      <ref_netgroup name="ADDRESS_G0"/>
      <ref_netgroup name="ADDRESS_G1"/>
   </netgroup>
```

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8.2.6.3.8 The <impedance> element

8.2.6.3.8.1 General

The `<impedance>` element defines the minimum, typical, and maximum characteristic impedance for the net that requests impedance matching.

```
<impedance
              {net_name="name_of_referenced_net" |
               group_name="name_of_referenced_net_group"  }
              [type="impedance_type"]
              [min="minimum_impedance"]
              typ="typical_impedance"
              [max="maximum_impedance"]
/>
```

The net shall be specified with either the net name (`net_name`) or group name (`group_name`) attribute.

8.2.6.3.8.2 Attribute definitions

The attributes for the `<impedance>` element are defined as follows.

`net_name`

This attribute specifies the name of the net to be the target of the impedance matching. The net is defined in N-Format file.

`group_name`

This attribute specifies the netgroup name to be the target of the impedance matching. The `group_name` is corresponding to the `name` attribute of the `<netgroup>` element.

`type`

This attribute specifies the type of the characteristic impedance. The value shall be one of the followings:

`single`	Single-ended signal
`differential`	Differential mode impedance
`common`	Common mode impedance

If the `type` attribute is not specified, `single` is set as the default.

`typ`

This attribute specifies the typical impedance value. The acceptable impedance is specified by the `min` and `max` attributes. The unit of impedance is defined by the `<impedance>` element in the `<unit>` element.

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min
max

These attributes specify the acceptable impedance. The max and min attributes are the maximum and minimum impedance values, respectively. The unit of impedance is defined by the <impedance> element in the <unit> element.

8.2.6.3.8.3 Example

```
<guideline>
   <netgroup name="CLOCK">
      <differential/>
      <ref_net name="CKN" polarity="NEGATIVE"/>
      <ref_net name="CKP" polarity="POSITIVE"/>
   </netgroup>
   <impedance net_name="DQ1"  type="single"  min="45" typ="50" max="55" />
   <impedance net_name="RESET"  type="single" typ="50" />
   <impedance group_name="CLOCK"  type="differential"  typ="100" />
</guideline>
```

8.2.6.3.9 The <delay> element

8.2.6.3.9.1 General

The <delay> element defines the minimum, typical, and maximum delay value for the net that requests a timing constraint.

```
<delay
             {net_name="name_of_referenced_net" |
              group_name="name_of_referenced_net_group"}
             [min="minimum_delay"]
             typ="typical_delay"
             [max="maximum_delay"]
/>
```

The net shall be specified with the net name (net_name) or group name (group_name) attribute.

8.2.6.3.9.2 Attribute definitions

The attributes of the <delay> element are defined as follows.

net_name

This attribute specifies the name of the net to be the target of delay constraint. The net is defined in N-Format file.

group_name

This attribute specifies the netgroup name to be the target of delay constraint. The group_name shall be corresponding to the name attribute of the <netgroup> element.

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typ

This attribute specifies the typical delay value. The acceptable delay time is specified by min and max attributes. The unit of delay is defined by the <time> element in the <unit> element.

min
max

These attributes specify the acceptable delay time. The max and min attributes are the maximum and minimum delay values, respectively. The unit of delay is defined by the <time> element in the <unit> element.

8.2.6.3.9.3 Example

```
<guideline>
   <netgroup name="BUS">
      <ref_net name="SIG1" />
      <ref_net name="SIG2" />
      <ref_net name="SIG3" />
   </netgroup>
   <delay net_name="CLK" min="10" typ="12" max="15" />
   <delay net_name="D3"  typ="5" />
   <delay netgroup="BUS"  min="50" typ="55" max="60"/>
</guideline>
```

8.2.6.3.10 The <skew> element

8.2.6.3.10.1 General

The <skew> element defines the skew constraint for signals that input and output from the specified net.

```
<skew
             {net_name="name_of_net" |
              group_name="name_of_net_group" }
             [reference_net_name="name_of_net_to_be_base_delay"]
             [min="minimum_time"]
             [max="maximum_time"]
/>
```

The net shall be specified with either the net name (net_name) attribute or group name (group_name) one.

When the reference net is specified, the skew constraint is defined by a maximum time (max) and a minimum time (min). In this case, the specified maximum and minimum times are based on the propagation time of the reference net (reference_net_name). The propagation time of nets having a skew constraint is required to be between the minimum time and the maximum time (see Figure 31).

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```
<netgroup name=“skewset1”>
 <ref_net name=“net1” />
 <ref_net name=“net2” />
 <ref_net name=“net3” />
</netgroup>
<skew group_name=“skewset1” reference_net_name=“net0”
     min=“-5” max=“10”/>
```

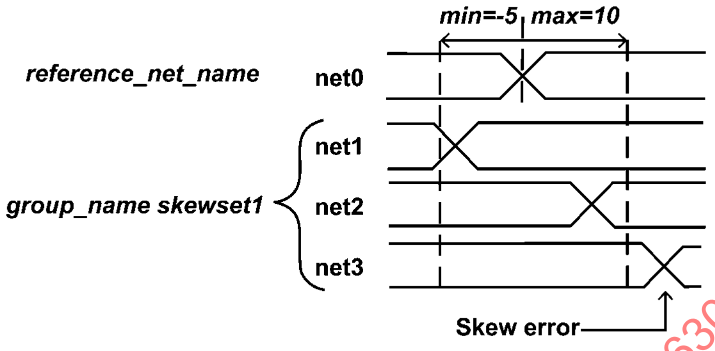

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Figure 31 —Sample of guideline for skew constraint with min and max attributes

When the reference net is not specified, the skew constraint is defined by either the maximum time (`max`) or the minimum time (`min`). If the maximum time is defined, a signal having the fastest propagation time is used as the reference net (see Figure 32).

```
<netgroup name=“skewset2”>
 <ref_net name=“net4” />
 <ref_net name=“net5” />
 <ref_net name=“net6” />
</netgroup>
<skew group_name=“skewset2” max=“10”/>
```

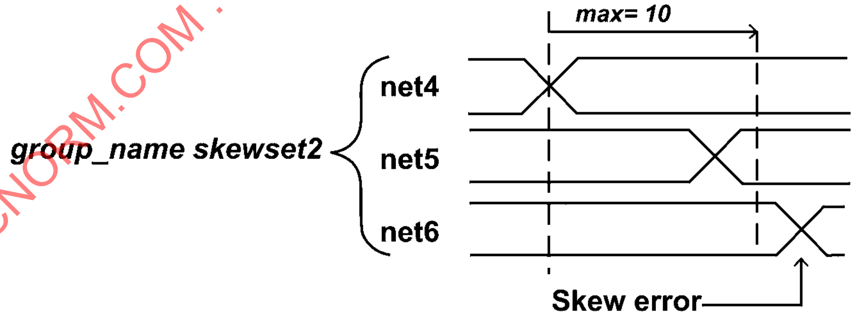

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Figure 32 —Sample of guideline for skew constraint with only `max` attribute

If only a minimum time (`min`) is defined, a net having the slowest propagation time is used as the reference net (see Figure 33).

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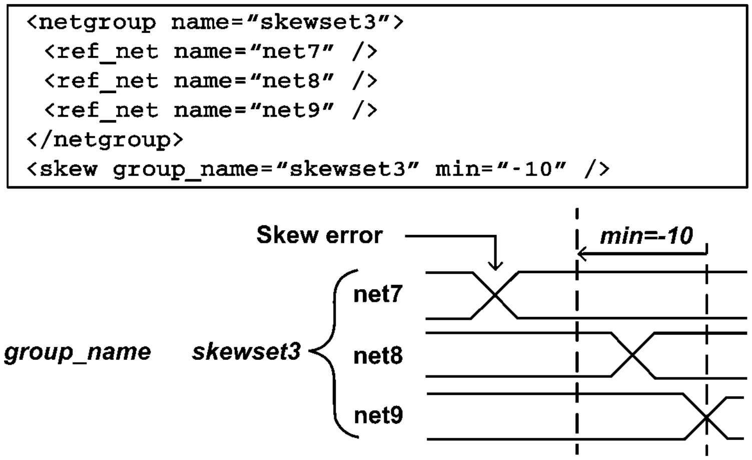

```
<netgroup name="skewset3">
 <ref_net name="net7" />
 <ref_net name="net8" />
 <ref_net name="net9" />
</netgroup>
<skew group_name="skewset3" min="-10" />
```

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Figure 33—Sample of guideline for skew constraint with only `min` attribute

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8.2.6.3.10.2 Attribute definitions

The attributes of the `<skew>` element are defined as follows.

`net_name`

> This attribute specifies the net name to be the target of this `<skew>` constraint. The `net_name` attribute shall be specified with `reference_net_name` to define base delay.

`group_name`

> This attribute specifies the netgroup name to be the target of skew constraint. All the nets which belong to the group shall be under the skew constraint.

`reference_net_name`

> This attribute specifies the net to be used as base delay for the skew constraint.

`min`
`max`

> The `max` and `min` attributes specify maximum and minimum skew, respectively. Set a positive value for the max attribute and a negative value for the min attribute. When a reference net is specified by the `reference_net_name` attribute, the `min` and `max` attributes shall be used together. When a reference net is not specified, either `min` or `max` attribute shall be used. The unit of minimum and maximum skew is defined by the `<time>` element in the `<unit>` element.

8.2.6.3.10.3 Example

```
<netgroup name="skewset1">
   <ref_net="net1" />
   <ref_net="net2" />
```

```
       <ref_net="net3" />
    </netgroup>
    <netgroup name="skewset2">
       <ref_net="net4" />
       <ref_net="net5" />
       <ref_net="net6" />
    </netgroup>
    <netroup name="skewset3">
       <ref_net="net7" />
       <ref_net="net8" />
       <ref_net="net9" />
    </netgroup>

    <skew group_name="skewset1" reference_net_name="net0" min="-5" max="10" />
    <skew group_name="skewset2" max="10" />
    <skew group_name="skewset3" min="-10" />

    <netgroup name="CK">
       <differential/>
       <ref_net="CKP" polarity="POSITIVE"/>
       <ref_net="CKN" polarity="NEGTIVE"/>
    </netgroup>
    <skew group_name="CK"  max="10" />
    <skew group_name="CK" reference_net_name="CKP" min="-5" max="15" />
```

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8.2.6.3.11 The <guard_shield> element

8.2.6.3.11.1 General

The `<guard_shield>` element defines a signal used for a shield, and signals requiring a shield.

```
<guard_shield
             {net_name="name_of_net_requiring_shield" |
              group_name="name_of_net_group_requiring_shield" }
             {shieldnet_net_name="name_of_net_using_shield"  |
              shieldnet_net_group_name="name_of_net_group_using_shield" }
/>
```

For example, in the case of analog-digital mixed design, it would be better to shield the analog signal by analog ground. The `<guard_shield>` element is used to define the combination of shielding nets.

8.2.6.3.11.2 Attribute definitions

The attributes of the `<guard_shield>` element are defined as follows.

`net_name`

This attribute specifies the net name which requires a guard shield. The `net_name` shall be corresponding to a wire name of the module in N-Format.

`group_name`

This attribute specifies the netgroup name which requires guard shield. All the nets belonging to the netgroup require guard shield. The `group_name` shall be corresponding to a `<netgroup>` definition. Either `net_name` or `group_name` shall be used to specify the shielding target.

`shieldnet_net_name`

This attribute specifies signal name to be used to form guard shield pattern. The `shieldnet_net_name` shall be corresponding to a wire name of the module in N-Format.

`shieldnet_net_group_name`

This attribute specifies the netgroup name to be used to form guard shield pattern. The `shieldnet_net_group_name` shall be corresponding to a `<netgroup>`.

Either `shieldnet_net_name` or `shieldnet_net_group_name` shall be used to specify signal name which forms guard shield.

8.2.6.3.11.3 Example

The example of a guard shield in Figure 34 is represented by the following code. VSS is the guard net and CLK is the shielded net:

```
<guard_shield net_name="CLK" shield_net_name="VSS"/>
```

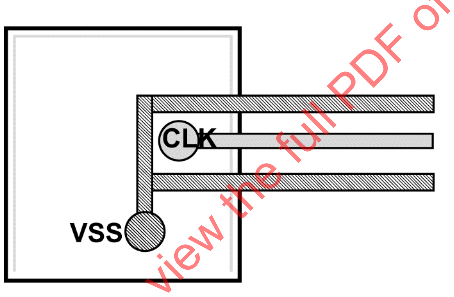

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Figure 34—Example of guideline for guard shield for a clock signal

8.2.6.3.12 The <width> element

8.2.6.3.12.1 General

The `<width>` element defines line width to be used for wiring.

```
<width
                {net_name="net_name" |
                 group_name="net_group_name"}
                [min="minimum_width"]
                [max="maximum_width"]
                [layer="layer_name"]
/>
```

This element can specify the constraint for a wiring width to a `<net>` or a `<netgroup>`. The width constraint can be layer dependent.

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8.2.6.3.12.2 Attribute definitions

The attributes of the `<width>` element are defined as follows.

`net_name`

> This attribute specifies the net name to which the constraint shall be applied. The `net_name` shall be corresponding to the wire name of the module in N-Format.

`group_name`

> This attribute specifies the netgroup name to which the constraint shall be applied. The `group_name` shall be corresponding to `<netgroup>` definition.
>
> Either `net_name` or `group_name` shall be used to specify the target to which the constraint would be applied.

`min`
`max`

> The `max` and `min` attributes specify maximum and minimum width, respectively. The unit of minimum and maximum width is defined by the `<distance>` element in the `<unit>` element.

`layer`

> This attribute specifies the wiring layer to which the width constraint shall be applied. When the `layer` is not specified, constraint shall be applied to all wiring layers.

8.2.6.3.12.3 Example

```
<width net_name="net1" min="100" layer="L1"/>
<width net_name="net1" min="110" layer="L2"/>
<width net_name="net1" min="110" layer="L3"/>
<width net_name="net1" min="100" layer="L4"/>
```

8.2.6.3.13 The <length> element

8.2.6.3.13.1 General

This element specifies the absolute length constraint for wiring of a net or a netgroup. The element can specify a layer dependence of the constraint.

```
<length
              {net_name="net_name" |
               group_name="net_group_name"}
              [min="minimum_length"]
              [max="maximum_length"]
              [layer="layer_name"]
/>
```

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8.2.6.3.13.2 Attribute definitions

The attributes of the `<length>` element are defined as follows.

`net_name`

This attribute specifies the net name to which the constraint shall be applied. The `net_name` shall be corresponding to the wire name of the module in N-Format.

`group_name`

This attribute specifies the netgroup name to which the constraint shall be applied. The `group_name` shall be corresponding to a `<netgroup>`.

Either `net_name` or `group_name` shall be used to specify the target to which the constraint would be applied.

`min`
`max`

The `max` and `min` attributes specify maximum and minimum length, respectively. The unit of minimum and maximum length is defined by the `<distance>` element in the `<unit>` element.

`layer`

This attribute specifies the wiring layer to which the length constraint shall be applied. When the `layer` is not specified, the length constraint means the total length regardless of the wiring layer.

8.2.6.3.14 Example

```
<netgroup name="group1">
   <ref_net name="net4" />
   <ref_net name="net5" />
</netgroup>
<length group_name="group1" min="30000" max="30300" layer="L2"/>
```

8.2.6.3.15 The <clearance> element

8.2.6.3.15.1 General

This element specifies the clearance constraint for wiring of a net or a netgroup, that is the spacing between different nets or different netgroups (see Figure 35). The element can specify a layer dependence of the constraint.

```
<clearance
             {net_name="net_name" |
              group_name="net_group_name"}
             [min="minimum_clearance"]
             [max="maximum_clearance"]
             [layer="layer_name"]
/>
```

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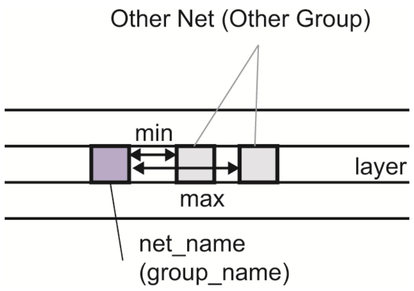

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Figure 35—Example of guideline for clearance constraint

8.2.6.3.15.2 Attribute definitions

The attributes of the `<clearance>` element are defined as follows.

`net_name`

This attribute specifies the net name to which the constraint shall be applied. The `net_name` shall be corresponding to the wire name of the module in N-Format.

`group_name`

This attribute specifies netgroup name to which the constraint shall be applied. The `group_name` shall be corresponding to a `<netgroup>`.

Either `net_name` or `group_name` shall be used to specify the target to which the constraint would be applied.

`min`
`max`

The `max` and `min` attributes specify maximum and minimum clearance, respectively. The unit of minimum and maximum clearance is defined by the `<distance>` element in the `<unit>` element.

`layer`

This attribute specifies the wiring layer to which the constraint shall be applied. When the `layer` is not specified, the constraint shall be applied to all wiring layers.

8.2.6.3.15.3 Example

The following example is a clearance constraint that requires net AA to be routed with a space wider than 10 µm from other nets in layer L1 and L4, and wider than 11 µm from other nets in layer L2 and L3.

```
<clearance net_name="AA" min="100" layer="L1"/>
<clearance net_name="AA" min="110" layer="L2"/>
<clearance net_name="AA" min="110" layer="L3"/>
<clearance net_name="AA" min="100" layer="L4"/>
```

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8.2.6.3.16 The <gap> element

8.2.6.3.16.1 General

This element specifies the gap constraint for the wiring of a net or a netgroup, the spacing between same net or nets belonging to the same net group (Figure 36). The element can specify a layer dependence of the constraint.

```
<gap
             {net_name="net_name" |
              group_name="net_group_name"}
             [min="minimum_gap"]
             [max="maximum_gap"]
             [layer="layer_name"]
/>
```

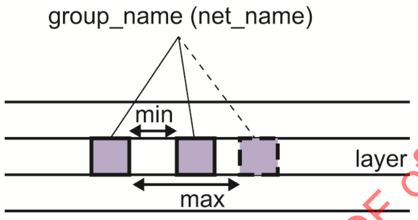

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Figure 36—Example of guideline for gap constraint

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While the `<clearance>` focuses on the spacing for “a net to another net” or “a netgroup to another netgroup” the `<gap>` focuses on intra-net or intra-netgroup spacing.

8.2.6.3.16.2 Attribute definitions

The attributes of the `<gap>` element are defined as follows.

`net_name`

> This attribute specifies the net name to which the constraint shall be applied. The `net_name` shall be corresponding to the wire name of the module in N-Format.

`group_name`

> This attribute specifies the netgroup name to which the constraint shall be applied. The `group_name` shall be corresponding to a `<netgroup>`.
>
> Either `net_name` or `group_name` shall be used to specify the target to which the constraint would be applied.

`min`
`max`

> The `max` and `min` attributes specify maximum and minimum gap width, respectively. The unit of minimum and maximum gap is defined by the `<distance>` element in the `<unit>` element.

layer

This attribute specifies the wiring layer to which the constraint shall be applied. When the layer is not specified, the constraint shall be applied to all wiring layers.

8.2.6.3.17 Example

The following example is a gap constraint that requests to route nets belonging to group AA with space of 10 µm to 12 µm.

```
<gap group_name="AA" min="10" max="12" />
```

8.2.6.3.18 The <enclosure> element

8.2.6.3.18.1 General

The <enclosure> element is used to specify the rule to cover the wiring metal with a metal plane in another layer. It enables to instruct the stripline structure or the microstripline structure to a wiring design. The element can specify the layer dependence of the constraint.

```
<enclosure
                {net_name="net_name" |
                 group_name="net_group_name"}
                [min="minimum_enclosure"]
                [layer="layer_name"]
                [upper_layer="name_of_upper_layer"]
                [lower_layer="name_of_lower_layer"]
                [upper_net="name_of_upper_net"]
                [lower_net="name_of_lower_net"]
/>
```

8.2.6.3.18.2 Attribute definitions

The attributes of the <enclosure> element are defined as follows.

net_name

This attribute specifies the net name which requires a stripline structure or microstripline structure. The net_name shall be corresponding to a wire name of the module in N-Format.

group_name

This attribute specifies the netgroup name on which the constraint shall be applied. The group_name shall be corresponding to a <netgroup>.

Either net_name or group_name shall be used to specify the target on which the constraint would be applied.

min

The min attribute specifies the minimum overhang length to cover the specific net's wires by a metal plane. The unit of minimum overhang is defined by the <distance> element in the <unit> element.

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`layer`

This attribute specifies the wiring layer to which the constraint shall be applied to wiring metals on the specified layer only. When the `layer` is not specified, the constraint shall be applied to all wiring layers.

`upper_layer`

When `upper_layer` attribute is specified, the upper side of the wiring metal shall be covered with the metal plane on the layer specified by this attribute.

`lower_layer`

When `lower_layer` attribute is specified, the lower side of the wiring metal shall be covered with the metal plane on this attribute-specified layer.

`upper_net`

The `upper_net` attribute specifies the net to cover the upper side of the wiring metal. If this attribute is not specified, any nets can be used to cover one.

`lower_net`

The `lower_net` attribute specifies the net to cover the lower side of the wiring metal. If this attribute is not specified, any nets can be used to cover one.

8.2.6.3.19 Example

```
<enclosure group_name="net_group1" min="50"
         upper_layer="L1" lower_layer="L3"
         upper_net="SG1" lower_net="SG1"/>
```

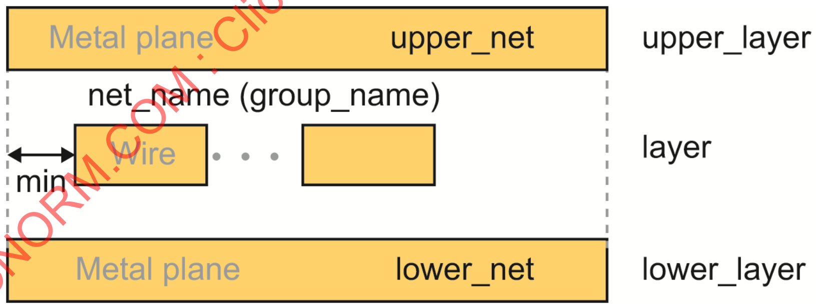

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Figure 37—Example of guideline for enclosure constraint

8.2.6.3.20 The <keepout> element

8.2.6.3.20.1 General

This element is used to specify the wiring and metal prohibition area which exists in adjacent layers of a specific net’s wiring. The element can specify a layer dependence of the constraint.

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```
<keepout
             {net_name="net_name" |
              group_name="net_group_name"}
             [min="minimum_overhang"]
             [ref_layer="layer_name"]
             [target_layer="UPPER|LOWER|ALL"]
>
             [<target_layer> element]…
             [<extensions> element]…
</keepout>
```

8.2.6.3.20.2 Attribute definitions

The attributes of the `<keepout>` element are defined as follows.

`net_name`

> This attribute specifies the name of the net which requires the wiring and metal prohibition area at its wiring pattern’s adjacent layers. The `net_name` shall be corresponding to the wire name of the module in N-Format.

`group_name`

> This attribute specifies the name of the net group which requires the wiring prohibition area at its wiring pattern’s adjacent layers. The `group_name` shall be corresponding to the `<netgroup>`.

`min`

> The `min` attribute specifies the minimum overhang for the wire prohibition area. The shape of the wire prohibited area is an extension of the routing area of a specified net or netgroup by the distance defined by `min` attribute. The unit of `min` is defined by the `<distance>` element in the `<unit>` element.

`ref_layer`

> This attribute specifies the wiring layer of the specific nets given by `net_name` or `group_name`. The `ref_layer` should be specified by the name which is defined in R-Format.

`target_layer`

> This attribute specifies layers to which the wiring and metal prohibition area will be applied. The `target_layer` must be one of the following: `UPPER`, `LOWER`, or `ALL`. The `UPPER` specifies all relative upper layers other than the `ref_layer`. The `LOWER` specifies all relative lower layers other than the `ref_layer`. The `ALL` specifies all layers except the layer specified by `ref_layer`.

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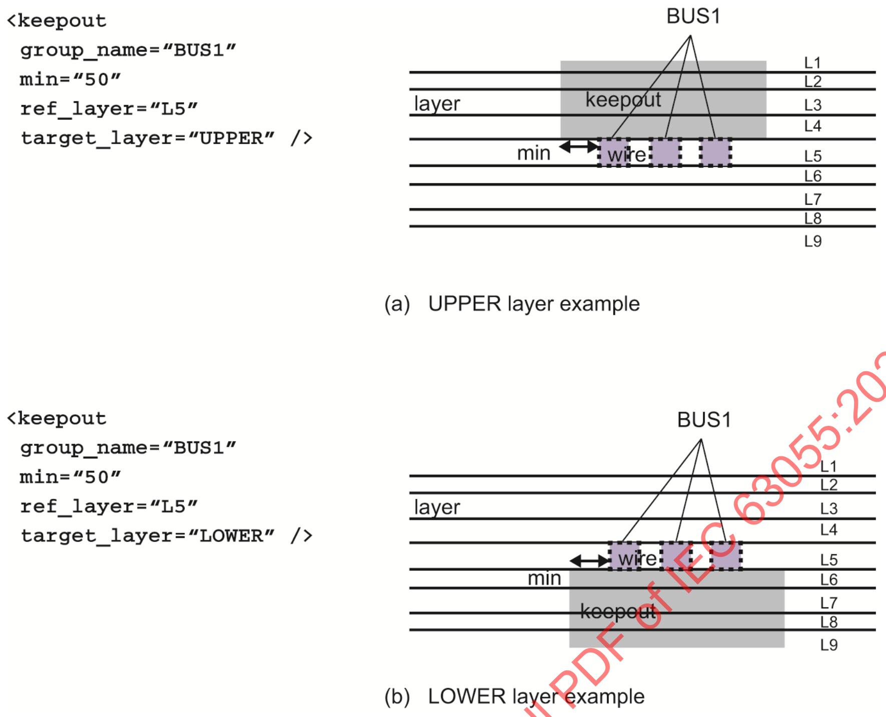
8.2.6.3.20.3 Example



```
<keepout
 group_name="BUS1"
 min="50"
 ref_layer="L5"
 target_layer="UPPER" />
```

(a) UPPER layer example

```
<keepout
 group_name="BUS1"
 min="50"
 ref_layer="L5"
 target_layer="LOWER" />
```

(b) LOWER layer example

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Figure 38 —Example of guideline for keepout constraint

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8.2.6.3.20.4 The <target_layer> element

8.2.6.3.20.4.1 General

The `<target_layer>` element specifies the wiring and metal prohibition layer. It is allowed to be used plural times under one `<keepout>`.

```
<target_layer
          ref_layer="name_of_target_layer"
/>
```

8.2.6.3.20.4.2 Attribute definition

The attribute of the `<target_layer>` element is as follows:

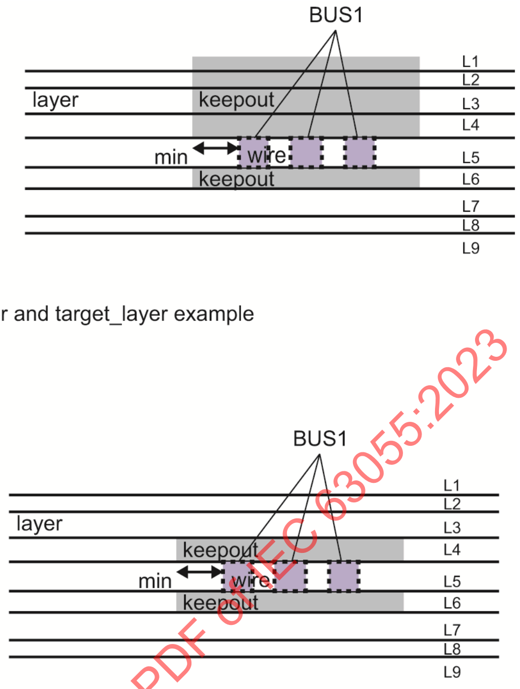
`ref_layer`

This attribute specifies the target layer on which the wiring and metal prohibition should be applied.

8.2.6.3.20.4.3 Example

```
<keepout
 group_name=“BUS1”
 min=“50”
 ref_layer=“L5”
 target_layer=“UPPER”>
 <target_layer  ref_layer=“L6”/>
</keepout>
```

```
<keepout
 group_name=“BUS1”
 min=“50”
 ref_layer=“L5” >
 <target_layer  ref_layer=“L4” />
 <target_layer  ref_layer=“L6” />
</keepout>
```



(a) UPPER layer and target_layer example

(b) Multiple target_layer example

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Figure 39—Example of guideline for keepout constraint with target_layer spcification

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8.2.7 The <specification> element

8.2.7.1 General

The <specification> element defines the specifications for the module itself, such as power consumption.

```
<specification>
             [<power> element]
             [<resistance> element]
             [<capacitance> element]
             [<inductance> element]
             [<extensions> element]…
</specification>
```

8.2.7.2 Element content

The <specification> element contains the following elements:

```
     <power>
     <resistance>
     <capacitance>
     <inductance>
     <extensions>
```

8.2.7.3 The <power> element

8.2.7.3.1 General

The <power> element specifies the power consumption of the module.

```
<power
             [min="minimum_power_consumption"]
             typ="typical_power_consumption"
             [max="maximum_power_consumption"]
/>
```

8.2.7.3.2 Attribute definitions

The attributes of the <power> element are defined as follows.

typ

> This attribute specifies the typical power consumption. The unit of power consumption is defined by the <power> element in the <unit> element.

min
max

> These attributes specify the perturbation of power consumption. The max and min attributes are the maximum and minimum power consumption, respectively. The unit of power is defined by the <power> element in the <unit> element.

8.2.7.3.3 Example

The following is an example of the <power> element in use.

```
<specification>
      <power typ="1.0" />
</specification>
```

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8.2.7.4 The <resistance> element

8.2.7.4.1 General

The `<resistance>` element specifies the resistance of the module.

```
<resistance
              [min="minimum_resistance"]
              typ="typical_resistance"
              [max="maximum_resistance"]
/>
```

The resistance, capacitance, and inductance that are defined in `<resistance>`, `<capacitance>`, and `<inductance>` element is a connected series.

8.2.7.4.2 Attribute definitions

The attributes of the `<resistance>` element are defined as follows.

`typ`

> This attribute specifies the typical resistance. The unit of resistance is defined by the `<resistance>` element in the `<unit>` element.

`min`
`max`

> These attributes specify the perturbation of resistance. The `max` and `min` attributes are the maximum and minimum resistance, respectively. The unit of resistance is defined by the `<resistance>` element in the `<unit>` element.

8.2.7.4.3 Example

```
<specification>
      <resistance typ="1.0" />
</specification>
```

8.2.7.5 The <capacitance> element

8.2.7.5.1 General

The `<capacitance>` element specifies the capacitance of the module.

```
<capacitance
              [min="minimum_capatitance"]
              typ="typical_capatitance "
              [max="maximum_capatitance "]
/>
```

The resistance, capacitance, and inductance that are defined in `<resistance>`, `<capacitance>`, and `<inductance>` element is a connected series.

8.2.7.5.2 Attribute definitions

The attributes of the `<capacitance>` element are defined as follows.

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typ

This attribute specifies the typical capacitance. The unit of capacitance is defined by the `<capacitance>` element in the `<unit>` element.

min
max

These attributes specify the perturbation of capacitance. The `max` and `min` attributes are the maximum and minimum capacitance, respectively. The unit of capacitance is defined by the `<capacitance>` element in the `<unit>` element.

8.2.7.5.3 Example

```
<specification>
      <capacitance typ="1.0" />
</specification>
```

8.2.7.6 The <inductance> element

8.2.7.6.1 General

The `<inductance>` element specifies the inductance of the module.

```
<inductance
             [min="minimum_inductance"]
             typ="typical_inductance "
             [max="maximum_inductance "]
/>
```

The resistance, capacitance, and inductance that are defined in `<resistance>`, `<capacitance>`, and `<inductance>` element is a connected series.

8.2.7.6.2 Attribute definitions

The attributes of the `<inductance>` element are defined as follows.

typ

This attribute specifies the typical inductance. The unit of inductance is defined by the `<inductance>` element in the `<unit>` element.

min
max

These attributes specify the perturbation of inductance. The `max` and `min` attributes are the maximum and minimum inductance, respectively. The unit of inductance is defined by the `<inductance>` element in the `<unit>` element.

8.2.7.6.3 Example

```
<specification>
      <inductance typ="1.0" />
</specification>
```

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8.2.8 The <surrounding_characteristics> element

8.2.8.1 General

The <surrounding_characteristics> element provides information on physical properties of a three-dimensional mass of a material, denoted as the surrounder here, in which the module is placed. The shape of the surrounder is assumed to be a rectangular box shape.

```
<surrounding_characteristics
             depth="depth"
             width="width"
             height="height"
             x="x_coordinate"
             y="y_coordinate"
             z="z_coordinate"
             [thermal_conductivity="thermal_conductivity"]
             [emissivity="emissivity"]
             [specific_heat_capacity="specific_heat_capacity"]
             [density="density"]
             [power="power_consumption"]
>
             [<extensions> element]…
</surrounding_characteristics>
```

8.2.8.2 Attribute definitions

The attributes of the <surrounding_characteristics> element are defined as follows.

depth

> This attribute specifies the depth (size along Y axis) of the surrounder. The unit of depth is defined by the <distance> element in the <unit> element.

width

> This attribute specifies the width (size along X axis) of the surrounder. The unit of width is defined by the <distance> element in the <unit> element.

height

> This attribute specifies the height (size along Z axis) of the surrounder. The unit of height is defined by the <distance> element in the <unit> element.

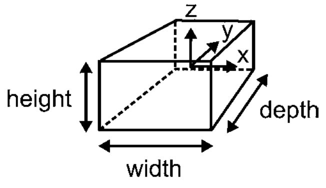

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Figure 40 —Explanatory drawing of the depth, width, and height attributes of the <surrounding_characteristics> element

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x
y
z

These attributes specify the X, Y, and Z coordinates of the center point of the surrounder. The unit of `coordinate` is defined by the `<distance>` element in the `<unit>` element.

thermal_conductivity

This attribute specifies the thermal conductivity of the surrounder. The unit of `thermal_conductivity` is defined by the `<thermal_conductivity>` element in the `<unit>` element.

emissivity

This attribute specifies the emissivity of the surrounder.

specific_heat_capacity

This attribute specifies the specific heat capacity of the surrounder. The unit of `specific_heat_capatity` is defined by the `<specific_heat_capacity>` element in the `<unit>` element.

density

This attribute specifies the density of the surrounder. The unit of `density` is defined by the `<density>` element in the `<unit>` element.

power

This attribute specifies the power consumed by the surrounder. The power consumed by the module is excluded. The unit of `power` is defined by the `<power>` element in the `<unit>` element.

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8.2.8.3 Example

The following is an example of the `<surrounding_characteristics>` element in use.

```
<surrounding_characteristics
    depth="150000" width="150000" height="250000"
    x="50000" y="40000" z="100000"
    thermal_conductivity="0.02"
    emissivity="0.05"
    specific_heat_capacity="1005"
    density="1.293"
    power="0.0" />
```

8.2.9 The <blockage> element

8.2.9.1 General

The blockage is a two-dimensional region where placement or routing is prohibited. The `<blockage>` element defines a collection of such prohibited areas.

```
<blockage>
             [<placement> element]…
             [<routing> element]…
             [<extensions> element]…
</blockage>
```

8.2.9.2 Element content

The <blockage> element can contain the following elements:

```
<placement>
<routing>
<extensions>
```

8.2.9.3 The <placement> element

8.2.9.3.1 General

The <placement> element defines a region where any child module shall not be placed intruding beyond the boundary of the region.

```
<placement
             shape_id="identifier_of_referenced_shape"
             [x="x_coordinate"]
             [y="y_coordinate"]
             [angle="angle"]
             [mount="mount_type" |
              {ref_layer="name_of_referenced_layer"
               [attach="side_to_be_attached"]}
             ]
             [stack="stack_level"]
/>
```

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8.2.9.3.2 Attribute definitions

The attributes of the <placement> element are defined as follows.

shape_id

> This attribute specifies the identifier of the predefined shape to define the boundary shape of the blockage area. The specified shape shall be defined at the <shape> element.

x
y

> These attributes specify the location of the reference point of the referenced shape with respect to the local origin of the module. The x and y attributes specify the x-coordinate and y-coordinate, respectively. The unit of the coordinates is defined by the <distance> element in the <unit> element. Zero is used as default when omitted.

angle

> This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the shape. If an angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

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`mount`

This attribute specifies the layer of substrate in which the placement blockage area is to be provided. A child module shall not be placed on the inside of a blockage area provided at the specified layer. The keyword for this attribute shall be one of the following (see Figure 41).

`TOP`	The placement blockage area is provided at the top layer of substrate.
`BOTTOM`	The placement blockage area is provided at the bottom layer of substrate.
`MIDDLE`	The placement blockage area is provided at all internal layers of substrate except top and bottom layer.

Either `mount` attribute or `ref_layer` attribute shall be present.

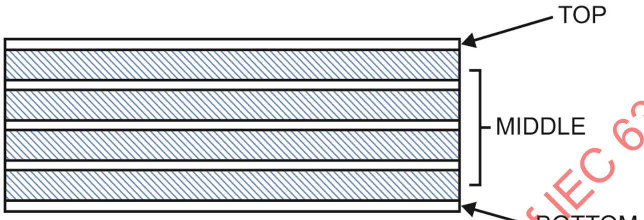

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Figure 41 —Explanatory drawing of mount layer for placement blockage area

`ref_layer`

This attribute specifies a specific layer of the substrate by referring the name defined in the R-Format that is combined in an M-Format. If this attribute is specified, a child module shall not be placed on the inside of the blockage area provided at the specified layer. Either `mount` attribute or `ref_layer` attribute shall be present.

`attach`

This attribute is used with `ref_layer` attribute and specifies the layer side of placement blockage. The available variable is `ABOVE` or `BELOW` (see Figure 42). If `ABOVE` is specified, the placement blockage is constructed above the specified layer. If `BELOW` is specified, the placement blockage is constructed below the specified layer.

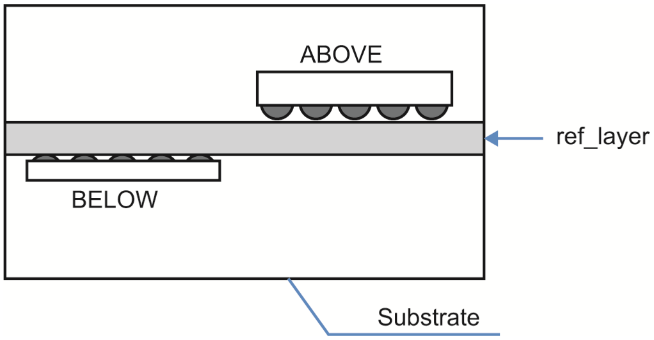

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Figure 42 —An example for explaining mount side when layer is specified

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stack

This attribute specifies the “stack level” of a child component placement (See Figure 47 for the concept of stack attribute). This blockage is effective only to the child components placed with the specified stack level. If this attribute is omitted, it means that the stack level is one as default.

8.2.9.3.3 Example

```
<placement shape_id="1" x="0" y="0" angle="0" mount="TOP"/>
```

8.2.9.4 The <routing> element

8.2.9.4.1 General

The <routing> element defines a region where any substrate routing object shall not be placed intruding beyond the boundary of the region. The routing object refers to the metallic material used for routing, such as traces, vias, and planes.

```
<routing
              shape_id="identifier_of_referenced_shape"
              [x="x_coordinate"]
              [y="y_coordinate"]
              [angle="angle"]
              [mount="mount_type"|
                ref_layer="name_of_referenced_layer"]
/>
```

8.2.9.4.2 Attribute definitions

The attributes of the <routing> element are defined as follows.

shape_id

This attribute specifies the identifier of the predefined shape to define the boundary shape of the blockage area. The specified shape shall be defined at the <shape> element in the same file.

x
y

These attributes specify the location of the reference point of the referenced shape with respect to the local origin of the module. The x and y attributes specify the x-coordinate and y-coordinate, respectively. The unit of the coordinates is defined by the <distance> element in the <unit> element. Zero is used as default when omitted.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the shape. If an angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

mount

This attribute specifies the layer of substrate in which the routing blockage area to be provided. A substrate routing shall not go through the inside of the blockage area provided at the specified layer. The keyword for this attribute shall be one of the following (see Figure 43).

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`TOP` The routing blockage area is provided at the top layer of substrate.

`BOTTOM` The routing blockage area is provided at the bottom layer of substrate.

`MIDDLE` The routing blockage area is provided at all internal layers of substrate except top and bottom layer.

Either `mopunt` attribute or `ref_layer` attribute shall be present.

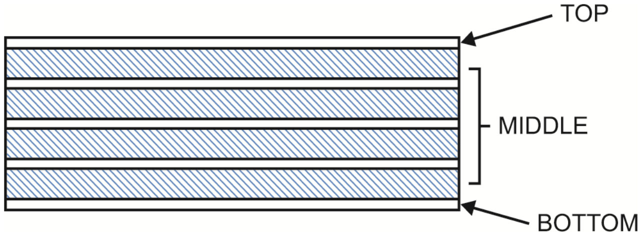

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Figure 43 —Explanatory drawing of mount layer for routing blockage area

`ref_layer`

This attribute specifies a specific layer of the substrate by referring the layer name defined in the R-Format that is combined in a M-Format. If this attribute is specified, a substrate routing shall not go through the inside of the blockage area provided at the specified layer. Either `mopunt` attribute or `ref_layer` attribute shall be present.

8.2.9.4.3 Example

```
<routing mount="TOP" shape_id="1" x="0" y="0" angle="0"/>
```

8.2.10 The <component> element

8.2.10.1 General

The `<component>` element instantiates child modules and bondwires.

```
<component
             [ref_rule_name="name_of_reference_rule"]
>
             [<placement> element]…
             [<bondingwire> element]…
             [<extensions> element]…
</component>
```

8.2.10.2 Attribute definitions

The attribute for the `<component>` element is defined as follows:

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ref_rule_name

This attribute specifies a design rule that shall be applied to placing child modules and bondwires, by identifying the name defined in <Physicaldesign> element in the R-Format that is combined in an M-Format.

8.2.10.3 Element content

The <component> element contains the following elements:

```
<placement>
<bondingwire>
<extensions>
```

8.2.10.4 The <placement> element

8.2.10.4.1 General

The <placement> element defines how to place the module.

```
<placement
             ref_module="name_of_referenced_module"
             inst="instance_name"
             [symbol="name_of_symbol"]
             [distance="unit_of_length"]
             [angleunit="unit_of_angle"]
             [scale="geometrical_scale"]
             [x="x_coordinate"]
             [y="y_coordinate"]
             [z="z_coordinate"]
             [flip="flip_type"]
             [angle="rotation_angle"]
             [mount="mount_type" |
              ref_layer="name_of_referenced_layer"
              [attach="layer_side_to_be_attach"]
             ]
             [stack="order_of_loading"]
             [ref_rule_name="name_of_referenced_rule"]
             [sizing="sizing"]
/>
```

8.2.10.4.2 Attribute definitions

The attributes of the <placement> element are defined as follows.

ref_module

This attribute specifies the module to be placed, by referring the name attribute of the module.

inst

This attribute specifies the instance name of a child module. The instance name shall be unique in the parent module.

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symbol

This optional attribute specifies an alias name of the module to be placed.

distance

This attribute specifies the unit of the x/y coordinate. If this attribute is not specified, the unit that is defined at the <distance> element in the <unit> element is used. The value shall be one of the followings:

pm	picometer
nm	nanometer
um	micrometer
mm	millimeter
m	meter

angleunit

This attribute specifies the unit of an angle. If this attribute is not specified, the unit that is defined at the <angle> element in the <unit> element is used. The value shall be either of the following:

degree
radian

scale

This attribute specifies the scale rate of distance. The scale rate shall be more than zero. If this attribute is not specified, 1.0 is used as the default.

x
y

These attributes specify the location of the reference point of the module. The x and y attributes specify the x-coordinate and y-coordinate, respectively. The unit of the coordinates is defined by the <distance> element in the <unit> element.

z

This attribute specifies the z-coordinate of the module, namely, the height of the module from the top layer as shown in Figure 44. If this attribute is not specified, zero is set as the default. The unit of the coordinates is defined by the <distance> element in the <unit> element.

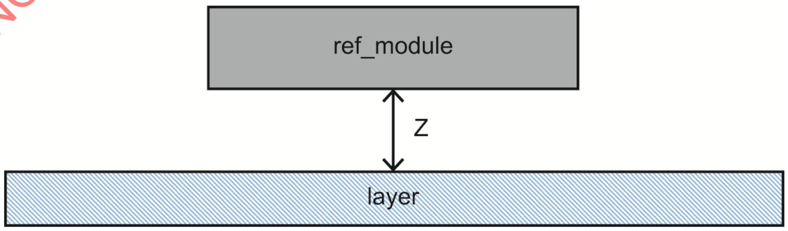

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Figure 44—Explanatory drawing of the z-coordinate of a module

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`flip`

This attribute specifies the type of flip. The value shall be either of the following:

`X`	X-flip reversing the X axis
`Y`	Y-flip reversing the Y axis

Figure 45 shows examples of an `X-flip` and a `Y-flip`.

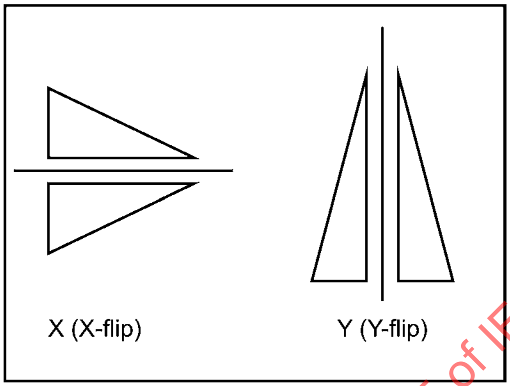

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Figure 45—Explanatory drawing an X-flip and a Y-flip

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`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the module. If an angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the `<angle>` element in the `<unit>` element.

`mount`

This attribute specifies the mount side of the module placement. The value shall be either of the following when the mount layer is not specified (see Figure 46).

`TOP`	The module is placed on the top side of the substrate.
`BOTTOM`	The module is placed on the bottom side of the substrate.
`MIDDLE`	The module is embedded inside the substrate.

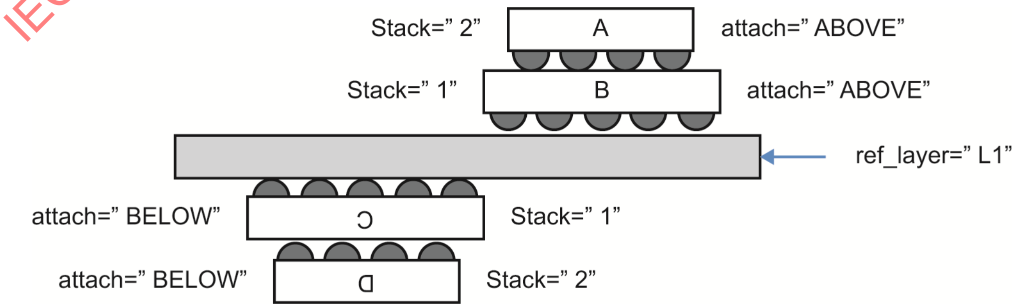

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Figure 46—An example for explaining mount side when layer is not specified

ref_layer

These attributes specify the *mount layer,* a substrate conductive layer on which the module is mounted directly or indirectly through another module that is mounted on the layer.

Attribute ref_layer specifies the mount layer by the layer name defined by the name attribute in the <layer> element in R-Format.

attach

This attribute is used with ref_layer attribute and specifies the layer side of the module placement. The available keyword is ABOVE or BELOW (see Figure 42). If ABOVE is specified, the component is placed above the specified layer. If BELOW is specified, the component is placed below the specified layer. If it is not specified, ABOVE is set as the default.

stack

This attribute specifies a positive integer, called *stack level*, to define the stacking order in Z-direction among child modules. For two modules A and B (C and D), A (D) is defined to be above (below) B (C) in Z-direction if all of the following conditions hold (Figure 47).

1) The mount attribute of A and B are the same, or ref_layer and attach attribute of A and B are the same,
2) The shapes of A and B overlap in X-Y plane beyond touching, and
3) The stack level of A is larger (smaller) than that of B, if their mount attribute is TOP or MIDDLE (BOTTOM) , or their attach is ABOVE (BELOW).

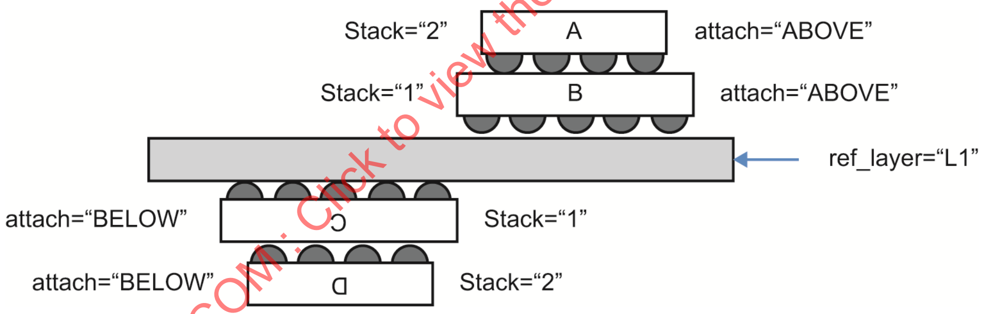

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Figure 47 —An example for explaining stack attribute

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The following sample code expresses the state of Figure 47.

```
<placement ref_module="CAP1" inst="A" x="10" y="10"
           ref_layer="L1" attach="ABOVE" stack="2" />
<placement ref_module="CAP2" inst="B" x="10" y="10"
           ref_layer="L1" attach="ABOVE" stack="1" />
<placement ref_module="CAP3" inst="C" x="-10" y="-10"
           ref_layer="L1" attach="BELOW" stack="1" />
<placement ref_module="CAP4" inst="D" x="-10" y="-10"
           ref_layer="L1" attach="BELOW" stack="2" />
```

ref_rule_name

This attribute specifies a design rule that is applied specifically to the region under the placed module. The design rule is referred by the name attribute of <Physicaldesign> element in R-Format.

`sizing`

> This attribute specifies the *sizing width,* which is positive (negative) number to enlarge (shrink) the shape of the module by the distance value.

8.2.10.4.3 Example

The following is an example of the `<placement>` element in use.

```
<component>
  <placement ref_module="CAP0603B" inst="C10"
            x="-8584.7" y="-4104.9" mount="BOTTOM" />
  <placement ref_module="CAP0603B" inst="C11"
            x="-8584.7" y="-6355.9" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C12"
            x="26092.5" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C13"
            x="30005.4" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C14"
            x="34659.6" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C15"
            x="40178.8" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="RAS8" inst="RAS8_RN2"
            x="25477.7" y="15729.6" angle="270" mount="TOP" />
  <placement ref_module="RAS8" inst="RAS8_RN4"
            x="43929.3" y="6225.3" angle="270" mount="TOP" />
  <placement ref_module="REGULATOR" inst="REGULATOR"
            x="-12598" y="10183.9" mount="TOP" />
  <placement ref_module="SOC_PKG" inst="SOC"
            x="400" y="-6500" mount="TOP" />
  <placement ref_module="XTAL" inst="XTAL"
            x="-6285.9" y="26473" mount="TOP" />
</component>
```

8.2.10.5 The <bondingwire> element

8.2.10.5.1 General

The `<bondingwire>` is used to define bonding wire placement, starting and ending points, layer, and the bonding wire rule.

```
<bondingwire
             bw_id="identifier"
             [bw_rule_name="name_referenced_bonding_wire_rule"]
             [bw_shape="name_of_referenced_bondingwire_shape"]
             x1="x_coordinate_of_start_point"
             y1="y_coordinate_of_start_point"
             inst1="instance_name_of_start_point"
             ref_layer1="name_for_reference_end_layer"
             x2="x_coordinate_of_end_point"
             y2="y_coordinate_of_end_point"
             inst2="instance_name_of_end_point"
             ref_layer2="name_of_reference_end_layer"
             [loop="loop_direction"]
/>
```

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8.2.10.5.2 Attribute definitions

The attributes of the <bondingwire> element are defined as follows.

bw_id

This attribute is a character string, defining an identification (ID) of the bondingwire. The ID should be unique in <component> element.

bw_rule_name

This attribute specifies the design rule for the bondingwire. The design rule is referred by the name attribute of <Physicaldesign> element in R-Format.

bw_shape

This attribute specifies the shape of bondingwire. The shape is referred by the name attribute of <bondingwire_def> element in R-Format.

x1
y1

These attributes specify the coordinates of the starting point of bondingwire. The unit of the coordinates is defined by the <distance> element in the <unit> element.

inst1
ref_layer1

These attributes specify the layout object that is attached with the bondingwire at its starting point.

If the bondingwire is attached to child module, its instance name is referred by the attribute inst1. If the bondingwire is attached to substrate layer, the layer is specified by its name defined in R-Format using attribute ref_layer1. Either inst1 or ref_layer1 shall be present.

x2
y2

These attributes specify the coordinates of the ending point of bondingwire. The unit of the coordinates is defined by the <distance> element in the <unit> element.

inst2
ref_layer2

These attributes specify the layout object that is attached with the bondingwire at its ending point.

If the bondingwire is attached to child module, its instance name is referred by the attribute inst2. If the bondingwire is attached to substrate layer, the layer is specified by its name defined in R-Format using attribute ref_layer2. Either inst2 or ref_layer2 shall be present.

loop

This attribute specifies whether the bonding wire is convex upward or convex downward in Z-direction.

TOP	The bondingwire is convex upward in Z-direction.
BOTTOM	The bondingwire is convex downward in Z-direction.

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8.2.10.5.3 Example

```
<component ref_rule_name="bondingwire_rule">
     <bondingwire bw_id="WB1" bw_shape="WBOND1"
            x1="4.0" y1="1.0" inst1="U1"
            x2="6.0" y2="1.0" ref_layer2="L1"
            loop="TOP" />
     <bondingwire bw_id="WB2" bw_shape="WBOND2"
            x1="1.0" y1="2.0" inst1="U2"
            x2="2.0" y2="2.0" inst2="U1"
            loop="TOP" />
     <bondingwire bw_id="WB3"
            bw_rule_name="bondingwire_rule_b" bw_shape="WBONDB"
            x1="3.0" y1="3.0" inst1="U3"
            x2="6.0" y2="3.0" ref_layer2="L3"
            loop="BOTTOM" />
</component>
```

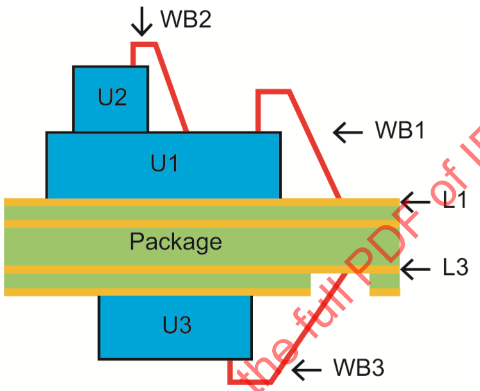

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Figure 48 —An example of bonding wire

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8.2.11 The <keepaway> element

8.2.11.1 General

The <keepaway> element defines a region around this module, where other modules shall not be placed in the region.

```
<keepaway
            shape_id="identifier_of_referenced_shape"
            x="x_coordinate"
            y="y_coordinate"
            [angle="angel"]
            [objective_layer="keep_away_area"]
>
            [<extensions> element]…
</keepaway>
```

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8.2.11.2 Attribute definition

The attribute of the <keepaway> element is defined as follows:

shape_id

This attribute specifies the identification number of the predefined shape.

x
y

These attributes specify the coordinates of the shape origin with respect to the module origin. The unit of the coordinates is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the rotation angle of the shape. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

objective_layer

This attribute specifies the effective range in Z-direction.

SAME	The keepaway is effective to the same mount side of the substrate/layer.
OPPOSITE	The keepaway is effective to any other parts.
ALL	The keepaway is effective to all parts.

8.2.11.3 Element content

The <keepaway> element can contain the following element:

<extensions>

8.2.11.4 Example

```
<keepaway shape_id="PFBGABODY" x="0" y="0" objective_layer="ALL"/>
```

8.2.12 The <reference> element

8.2.12.1 General

The <reference> element is used to make a relationship between the module in C-Format and an electrical, thermal, or geometrical model file. While referring an electrical or thermal file, the <reference> element defines the connection procedure between ports in the <socket> element and ports in a referenced file. While referencing a geometrical file, this element makes a transformation from objects in the referenced geometrical file to the module in C-Format.

```
<reference
    {xmlns:verilog="http://www.jeita.or.jp/LPB/verilog" |
     xmlns:VHDL="http://www.jeita.or.jp/LPB/VHDL" |
     xmlns:def="http://www.jeita.or.jp/LPB/def" |
     xmlns:spice="http://www.jeita.or.jp/LPB/spice" |
```

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```
     xmlns:touchstone="http://www.jeita.or.jp/LPB/touchstone" |
     xmlns:dxf="http://www.jeita.or.jp/LPB/dxf" |
     xmlns:gds="http://www.jeita.or.jp/LPB/gds" |
     xmlns:step="http://www.jeita.or.jp/LPB/step" |
     xmlns:sat="http://www.jeita.or.jp/LPB/sat" |
     xmlns:iges="http://www.jeita.or.jp/LPB/iges" |
     xmlns:ibis="http://www.jeita.or.jp/LPB/ibis" |
     xmlns:ibis_pkg="http://www.jeita.or.jp/LPB/ibis_pkg" |
     xmlns:ibis_ebd="http://www.jeita.or.jp/LPB/ibis_ebd" |
     xmlns:systemc="http://www.jeita.or.jp/LPB/systemc" |
     xmlns:xfl="http://www.jeita.or.jp/LPB/xfl" |
     xmlns:xml="http://www.jeita.or.jp/LPB/xml" |
     xmlns:thermal_2resistor="http://www.jeita.or.jp/LPB/thermal_2resistor" |
     xmlns:thermal_delphi="http://www.jeita.or.jp/LPB/thermal_delphi"
     xmlns:jtam="http://www.jeita.or.jp/LPB/jtam"|
     xmlns:JLPB="http://www.jeita.or.jp/LPB/JLPB"|
     xmlns:extensions=http://www.jeita.or.jp/LPB/extensions }
     reffile="name_of_referenced_file"
     format="file_format"
     [type="model_type"]
     [distance="unit_of_length"]
     [scale="geometric_scale"]
     [comment="comment_text"]
>
              [<connection> element]…
              [affine_transformation > element]…
              [<material> element]…
              [<heat_source> element>]…
              [<extensions> element]…
</reference>
```

Some formats do not have the concept of I/O ports. In those cases, coordinates that correspond to the position of the signal I/O are used to create the relationship with a port in the C-Format file. For example, the <reference> element can provide the position for I/O nodes of IBIS that does not have physical information.

8.2.12.2 Attribute definitions

The attributes of the <reference> element are defined as follows.

```
xmlns:verilog="http://www.jeita.or.jp/LPB/verilog"
xmlns:VHDL="http://www.jeita.or.jp/LPB/VHDL"
xmlns:def="http://www.jeita.or.jp/LPB/def"
xmlns:spice="http://www.jeita.or.jp/LPB/spice"
xmlns:touchstone="http://www.jeita.or.jp/LPB/touchstone"
xmlns:dxf="http://www.jeita.or.jp/LPB/dxf"
xmlns:gds="http://www.jeita.or.jp/LPB/gds"
xmlns:step="http://www.jeita.or.jp/LPB/step"
xmlns:sat="http://www.jeita.or.jp/LPB/sat"
xmlns:iges="http://www.jeita.or.jp/LPB/iges"
xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
xmlns:ibis_pkg="http://www.jeita.or.jp/LPB/ibis_pkg"
xmlns:ibis_ebd="http://www.jeita.or.jp/LPB/ibis_ebd"
xmlns:systemc="http://www.jeita.or.jp/LPB/systemc"
xmlns:xfl="http://www.jeita.or.jp/LPB/xfl"
xmlns:xml="http://www.jeita.or.jp/LPB/xml"
xmlns:thermal_2resistor="http://www.jeita.or.jp/LPB/thermal_2resistor"
xmlns:thermal_delphi="http://www.jeita.or.jp/LPB/thermal_delphi"
xmlns:jtam="http://www.jeita.or.jp/LPB/jtam"
xmlns:JLPB="http://www.jeita.or.jp/LPB/JLPB"
```

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`xmlns:extensions ="http://www.jeita.or.jp/LPB/extensions"`

This line is the namespace of the Extensible Markup Language (XML) [B2][8]. The namespace is used properly by the format of the referenced file. The corresponding namespaces and file formats are shown as follows:

`xmlns:verilog`

Verilog, standardized as IEEE Std 1364. It is used in the design and verification of digital circuits at gate level or register transfer level.

`xmlns:VHDL`

Very High Speed Integrated Circuits Hardware Description Language (VHDL) is standardized as IEEE Std 1076™ [B9]. It is used in the design of digital and mixed-signal systems.

`xmlns:def`

Design Exchange Format (DEF), representing the physical layout of an integrated circuit in an ASCII format. It represents a netlist, component placements, and routing information.

`xmlns:spice`

Standard SPICE is Berkeley SPICE, but SPICE-like circuit simulators are not completely compatible. Use the `type` attribute to show the specified version of SPICE. Specify the name of circuit simulator for SPICE to `type` attribute. `Berkeley_SPICE` and `IBIS-ISS` are reserved for it. If `type` attribute is omitted, it means SPICE is Berkeley SPICE.

`type` attribute for `xmlns:spice`

`Berkeley_SPICE`	Berkeley SPICE
`IBIS-ISS`	IBIS Interconnect SPICE Subcircuit
`any_string`	Specify the name of SPICE-like circuit simulator

`xmlns:touchstone`

Touchstone version 1.0 and 2.0 are supported. Use the `type` attribute to specify the type of model defined in the Touchstone file. It shall be `SParameter`. If `type` attribute is omitted, it means the model that defined in touchstone file is S-parameter.

`type` attribute for `xmlns:touchstone`

`SParameter`	S-parameter model

`xmlns:dxf`

Drawing Exchange Format (DXF). It is used for vector image files.

[8] The numbers in brackets correspond to those of the bibliography in Annex A

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`xmlns:gds`

GDS II stream format. It is a database file format for data exchange of integrated circuits or integrated circuit layout artwork.

`xmlns:step`

ISO 10303. It is used to represent 3D objects in computer-aided design (CAD) tools.

`xmlns:sat`

Standard ACIS Text file. It is used to save the data of the ACIS modeler.

`xmlns:iges`

Initial Graphics Exchange Specification. It is used to express 3D objects as a collection of surface models.

`xmlns:ibis`

IBIS file. It is used by integrated circuit vendors to provide customers with information about the I/O buffers of a product.

`xmlns:ibis_pkg`

IBIS package model file. It is used by integrated circuit vendors to provide customers with information about the I/O buffers of a product.

`xmlns:ibis_ebd`

IBIS electrical board description file. It is used by integrated circuit vendors to provide customers with information about the I/O buffers of a product.

`xmlns:systemc`

This name space is used to reference SystemC. It is standardized as IEEE Std 1666-2011. SystemC is used for system and hardware design.

`xmlns:xml`

This name space is used to reference an external file that is defined in XML, such as IEC, ICEM, or ICIM file.

Use the `type` attribute to specify the type of model file defined in XML. The type shall be one of the followings.

`type` attribute for `xmlns:xml`

`ICEM-CE`	Integrated Circuit Electrical Model—Conducted Emission (IEC 62433-2 [B5])
`ICEM-RE`	Integrated Circuit Electrical Model—Radiated Emission (IEC 62433-3 [B6])
`ICIM-CI`	Integrated Circuit Immunity Model—Conducted Immunity (IEC 62433-4 [B7])
`ICIM-RI`	Integrated Circuit Immunity Model—Radiated Immunity (IEC 62433-5 [B8])

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CEML	Conducted Emission Markup Language
REML	Radiated Emission Markup Language
CIML	Conducted Immunity Markup Language
RIML	Radiated Immunity Markup Language
PIML	Pulse Immunity Markup Language

`xmlns:thermal_2resistor`

This name space is used to reference a JEDEC 2-Resistor compact thermal model.

`xmlns:thermal_delphi`

This name space is used to reference a JEDEC DELPHI compact thermal model.

`xmlns:jtam`

This name space is used to reference a JTAM file.

`xmlns:xfl`

LPB G-Format.

`xmlns:JLPB`

LPB C-Format.

`xmlns:extensions`

This namespace is used to refer to your own model file using <`extensions`> element.

`reffile`

This attribute specifies the name of a file with which to make a relationship.

`format`

This attribute specifies the language of a reference file. The value shall be one of the followings:

VERILOG	Verilog, standardized as per IEEE Std 1364
VHDL	VHDL standardized as per IEEE Std 1076 [B9]
DEF	Design Exchange Format (DEF)
SPICE	Netlist for SPICE
TOUCHSTONE	S-parameter
DXF	Drawing Exchange Format (DXF)
GDS	GDS II stream format
STEP	ISO 10303, standard for the exchange of product model data
SAT	Standard ACIS Text file to save the data of the ACIS modeler
IGES	The Initial Graphics Exchange Specification
IBIS	IBIS (Input/output Buffer Information Specification)
IBIS_PKG	IBIS package model file
IBIS_EBD	IBIS electrical board description file
SYSTEMC	SystemC standardized as per IEEE Std 1666
XML	XML file
THERMAL_2RESISTOR	Compact two resistor–type thermal model file

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`THERMAL_DELPHI`	Compact DELPHI thermal model file
`JTAM`	JEITA Thermal Accurate Model
`XFL`	LPB G-Format
`JLPB`	LPB C-Format
`EXTENSIONS`	The user's own model file is referenced

`type`

This attribute is used together with the `xmlns:spice`, `xmlns:touchstone`, and `xmlns:xml` attributes.

In case of `xmlns:spice`, it specifies the kind of circuit simulator for SPICE. `Berkeley_SPICE` and `IBIS-ISS` are reserved for it. If type attribute is omitted, it means SPICE is Berkeley SPICE. The available values are as follows.

`Berkeley_SPICE`	Berkeley SPICE
`IBIS-ISS`	IBIS Interconnect SPICE Subcircuit
`any_string`	Specify the name of SPICE-like circuit simulator

In case of `xmlns:touchstone`, it specifies the model type of the touchstone file. The available value shall be `SParameter`. If type attribute is omitted, it means the model that is defined in the touchstone file is S-parameter.

`SParameter`	S-parameter model

In case of `xmlns:xml`, it specifies the kind of model file that is defined by XML. The value shall be one of the followings.

`ICEM-CE`	Integrated Circuit Electrical Model—Conducted Emission (IEC 62433-2 [B5])
`ICEM-RE`	Integrated Circuit Electrical Model—Radiated Emission (IEC 62433-3 [B6])
`ICIM-CI`	Integrated Circuit Immunity Model—Conducted Immunity (IEC 62433-4 [B7])
`ICIM-RI`	Integrated Circuit Immunity Model—Radiated Immunity (IEC 62433-5 [B8])
`CEML`	Conducted Emission Markup Language
`REML`	Radiated Emission Markup Language
`CIML`	Conducted Immunity Markup Language
`RIML`	Radiated Immunity Markup Language
`PIML`	Pulse Immunity Markup Language

`distance`

This attribute specifies the unit system of distance for a reference file. If this attribute is not specified, the default of the reference file is used. The value shall be one of the followings:

`pm`	picometer
`nm`	nanometer
`um`	micrometer
`mm`	millimeter
`m`	meter

`scale`

This attribute specifies the scale range for a reference file. The scale range shall be more than zero. If this attribute is not specified, 1.0 is used as the default.

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`comment`

This attribute specifies the comment string.

8.2.12.3 Element content

The `<reference>` element contains the following elements:

```
<connection>
<affine_transformation>
<material>
<heat_source>
<extensions>
```

8.2.12.4 The <connection> element

8.2.12.4.1 General

The `<connection>` element defines the relationship between a `<port>` that is defined in the `<socket>` element and the I/O terminal of a reference file.

```
<connection
             socket_name="name_of_reference_socket"
             [port_name="name_of_referenced_port"  |
              port_id="identifier_of_referenced_port"]
>
             [<verilog:ref_port> element]…
             [<VHDL:ref_port> element]…
             [<def:ref_port> element]…
             [<spice:ref_port> element]…
             [<touchstone:ref_port> element]…
             [<dxf:ref_port> element]…
             [<gds:ref_port> element]…
             [<xfl:ref_port> element]…
             [<ibis:ref_port> element]…
             [<ibis_pkg:ref_port> element]…
             [<ibis_ebd:ref_port> element]…
             [<systemc:ref_port> element]…
             [<thermal_2resistor:ref_port> element]…
             [<thermal_delphi:ref_port> element]…
             [<jtam:ref_port> element]…
             [<JLPB:ref_port> element]…
             [<xml:ref_port> element]…
             [<extensions> element]…
</connection>
```

The connection scheme depends on the design language of the reference file. The following is a typical example.

The language in which a port is clearly defined as Verilog uses the combination of the “module name” and “port name” to define the relationship:

```
<connect socket_name="socket1" port_id="A1">
     <verilog:ref_port module="topmodule" portname="DQ1"/>
</connect>
```

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In this example, port A1 in socket1 is associated with terminal DQ1 in model topmodule of the Verilog description.

In the case of a SPICE netlist, the sub-circuit name and order of I/O node description are used to define the relationship:

```
<connect socket_name="socket1" port_id="A1">
    <spice:ref_port subckt="spicetop" portid="5"/>
</connect>
```

In this example, A1 port in socket1 is associated with an I/O node that is defined in the fifth order in the sub-circuit spicetop.

8.2.12.4.2 Attribute definitions

The attributes of the <connection> element are defined as follows.

socket_name

This attribute specifies the name of a socket that includes a port to make a relationship with the reference file. The specified socket shall be defined at the <socket> element in the same <module> element.

port_name

This attribute specifies the name of a port to make a relationship with the reference file. The specified port shall be defined at the <port> element in the <socket> element, which is specified by the socket_name attribute. The port_name attribute shall not be used with the port_id attribute.

port_id

This attribute specifies the identifier of a port to make a relationship with the reference file. The specified port shall be defined at the <port> element in the <socket> element, which is specified by the socket_name attribute. The port_id attribute shall not be used with the port_name attribute.

8.2.12.4.3 Element content

The <connection> element can contain the following elements:

```
<verilog:ref_port>
<VHDL:ref_port>
<def:ref_port>
<spice:ref_port>
<touchstone:ref_port>
<dxf:ref_port>
<gds:ref_port>
<xfl:ref_port>
<ibis:ref_port>
<ibis_pkg:ref_port>
<ibis_ebd:ref_port>
<systemc:ref_port>
<thermal_2resistor:ref_port>
<thermal_delphi:ref_port>
<jtam:ref_port>
<JLPB:ref_port>
<xml:ref_port>
<extensions>
```

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8.2.12.4.4 The <verilog:ref_port> element

8.2.12.4.4.1 General

The `<verilog:ref_port>` element is used to make a relationship with a Verilog language file.

```
<verilog:ref_port
             module="module_name_in_verilog_file"
             portname="port_name_in_verilog_file"
>
             [<extensions> element]…
</verilog:ref_port>
```

In the case of a Verilog file, a relationship is created by the combination of module name and port name.

8.2.12.4.4.2 Attribute definitions

The attributes of the `<verilog:ref_port>` are defined as follows.

`module`

> This attribute specifies the name of a module in the reference Verilog file.

`portname`

> This attribute specifies the name of a port in the reference Verilog file. The port shall be defined in the module that is specified by the `module` attribute.

8.2.12.4.4.3 Example

The following is an example of the `<verilog:ref_port>` element in use.

```
<reference
  xmlns:verilog="http://www.jeita.or.jp/LPB/verilog"
  reffile="XXXX.v"
  format="VERILOG"
>
   <connection socket_name="socket1" port_id="A1">
      <verilog:ref_port  module="topmodule" portname="DQ1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <verilog:ref_port module="topmodule"  portname="DQ2" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <verilog:ref_port module="topmodule"  portname="DQ3" />
   </connection>
</reference>
```

```
[XXXX.v]
  module topmodule(DQ1,DQ2,DQ3)
```

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8.2.12.4.5 The <VHDL:ref_port> element

8.2.12.4.5.1 General

The `<VHDL:ref_port>` element is used to make a relationship with the model file that is described by VHDL language.

```
<VHDL:ref_port
             entity="entity_name_in_VHDL_file"
             portname="port_name_in_VHDL_file"
             [subtype="subtype_of_port_in_VHDL_file"]
>
             [<extensions> element]…
</VHDL:ref_port>
```

8.2.12.4.5.2 Attribute definitions

The attributes of the `<VHDL:ref_port>` element are defined as follows.

`entity`

This attribute specifies the name of an entity in the reference VHDL file.

`portname`

This attribute specifies the name of a port in the reference VHDL file. The port shall be defined in the entity that is specified by the `entity` attribute.

`subtype`

This attribute specifies the subtype of the port declaration in VHDL file. If this attribute is not specified, `electrical` is set as the default.

`electrical`	The referenced port is used for electrical connection
`thermal`	The referenced port is used for thermal network in kelvin
`thermal_c`	The referenced port is used for thermal network in celsius
`any_string`	Specify the subtype of the specified port

8.2.12.4.5.3 Example

The following is an example of the `<VHDL:ref_port>` element in use.

```
<reference
  xmlns:VHDL="http://www.jeita.or.jp/LPB/VHDL"
  reffile="XXXX.vhd"
  format="VHDL"
>
   <connection socket_name="socket1" port_id="A1">
      <VHDL:ref_port  entity="topmodule" portname="DQ1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <VHDL:ref_port entity="topmodule"  portname="DQ2" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <VHDL:ref_port entity="topmodule"  portname="DQ3" />
```

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```
    </connection>
</reference>
[XXXX.vhd]
  entity topmodule is
  port
  (
    DQ1       : out    std_logic;
    DQ2       : out    std_logic;
    DQ3       : out    std_logic;
  );
  end topmodule;
```

8.2.12.4.6 The <def:ref_port> element

8.2.12.4.6.1 General

The `<def:ref_port>` element is used to make a relationship with a DEF file.

```
<def:ref_port
             [comp="component_name_in_DEF_file"]
             pinname="pin_name_in_DEF_file"
>
             [<extensions> element]…
</def:ref_port>
```

In the case of a DEF file, a relationship is created by using the pin name and/or component name.

8.2.12.4.6.2 Attribute definitions

The attributes of the `<def:ref_port>` element are as follows.

`comp`

> This attribute specifies the name of a component that is defined in the COMPONENT section in the reference DEF file.

`pinname`

> This attribute specifies the name of a pin that is defined in the PINS section in the reference DEF file. Alternatively, it specifies the pin name of the component that is defined by the `comp` attribute.

8.2.12.4.6.3 Example

The following is an example of the `<def:ref_port>` element in use.

```
<reference
   xmlns:def="http://www.jeita.or.jp/LPB/def"
   reffile="XXXX.def"
   format="DEF"
>
    <connection socket_name="socket1" port_id="A1">
      <def:ref_port  comp="SBIO1" pinname="Z"/>
    </connection>
    <connection socket_name="socket1" port_id="A2">
      <def:ref_port  comp="SBIO2" pinname="Z"/>
```

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```
   </connection>
   <connection socket_name="socket1" port_id="A3">
     <def:ref_port  comp="SBIO3" pinname="Z"/>
   </connection>
</reference>

[XXXX.def]
   COMPONENTS  100 ;
   -   SBIO1   io   ;
   -   SBIO2   io   ;
   -   SBIO3   io   ;
    .....
   END COMPONENTS


<reference xmlns:def=http://www.jeita.or.jp/LPB/def
  reffile="YYY.def"
  format="DEF"
>
   <connection socket_name="socket1" port_id="A1">
      <def:ref_port  pinname="PIN1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
       <def:ref_port  pinname="PIN2"/>
   </connection>
   <connection socket_name="socket1" port_id="A3">
       <def:ref_port  pinname="PIN3"/>
   </connection>
</reference>

[YYY.def]
   PINS  10 ;
  - PIN1  oDQ1 ;
  - PIN2  oDQ2 ;
  - PIN3  oDQ3 ;
    ...
  END PINS
```

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8.2.12.4.7 The <spice:ref_port> element

8.2.12.4.7.1 General

The `<spice:ref_port>` element is used to make a relationship with a SPICE netlist file.

```
<spice:ref_port
             subckt="name_of_subckt"
             portid="order_of_pins_in_subckt"
>
             [<extensions> element]…
/spice:ref_port>
```

In the case of SPICE, a relationship is created by the combination of the sub-circuit name and order of I/O node description. In the case of a SPICE netlist, the name of the sub-circuit (`.subckt`) and order of I/O node on the `.subckt` line are used to define the relationship.

8.2.12.4.7.2 Attribute definitions

The attributes of the `<spice:ref_port>` element are defined as follows.

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`subckt`

This attribute specifies the name of a sub-circuit (`.subckt`) in the reference SPICE file.

`portid`

This attribute specifies the order of I/O nodes in the .subckt line. The value shall be an integer of 1 or more.

8.2.12.4.7.3 Example

The following is an example of the `<spice:ref_port>` element in use.

```
<reference
   xmlns:spice="http://www.jeita.or.jp/LPB/spice"
   reffile="XXXX.sp"
   format="SPICE"
   type="HSPICE"
>
      <connection socket_name="socket1" port_id="A1">
        <spice:ref_port  subckt="top" portid="3"/>
      </connection>
      <connection socket_name="socket1" port_id="A2">
         <spice:ref_port  subckt="top" portid="2"/>
      </connection>
      <connection socket_name="socket1" port_id="A3">
         <spice:ref_port  subckt="top" portid="1"/>
      </connection>
</reference>
```

```
[XXXX.sp]
   subckt  top  p1  p2  p3 ;
```

SPICE model file includes IBIS-ISS. To reference the IBIS-ISS model, specify the `IBIS-ISS` keyword in the `type` attribute as follows.

```
<reference
   xmlns:spice="http://www.jeita.or.jp/LPB/spice"
   reffile="YYYY.ibs"
   format="SPICE"
   type="IBIS-ISS"
>
      <connection socket_name="socket1" port_id="A1">
        <spice:ref_port  subckt="top" portid="3"/>
      </connection>
```

8.2.12.4.8 The <touchstone:ref_port> element

8.2.12.4.8.1 General

The `<touchstone:ref_port>` element is used to make a relationship with a S-parameter file.

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```
<touchstone:ref_port
             portid="order_of_ports_in_touchstone"
>
             [<extensions> element]…
/touchstone:ref_port>
```

8.2.12.4.8.2 Attribute definitions

The attribute of the `<touchstone:ref_port>` element is defined as follows.

`portid`

> This attribute specifies the order of ports in the S-parameter file. The value shall be an integer of 1 or more.

8.2.12.4.8.3 Example

The following is an example of the `<touchstone:ref_port>` element in use.

```
<reference
   xmlns:touchstone="http://www.jeita.or.jp/LPB/touchstone"
   reffile="XXXX.s2p"
   format="TOUCHSTONE"
   type="SParameter"
>
      <connection socket_name="YYY" port_id="A">
        <touchstone:ref_port portid="1"/>
      </connection>
      <connection socket_name="YYY" port_id="B">
         <touchstone:ref_port portid="2"/>
      </connection>
</reference>
```

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8.2.12.4.9 The <dxf:ref_port> element

8.2.12.4.9.1 General

The `<dxf:ref_port>` element is used to make a relationship with a DXF file.

```
<dxf:ref_port
             x="x_coordinate"
             y="y_coordinate"
             dxf_layer="layer_name_in_DXF_file"
             mount="mount_type"
>
             [<extensions> element]…
</dxf:ref_port>
```

The DXF language does not have a concept of the I/O terminal. Therefore, coordinates are used to create the relationship with a port in the C-Format file.

8.2.12.4.9.2 Attribute definitions

The attributes of the `<dxf:ref_port>` element are defined as follows.

`x`
`y`

These attributes specify the coordinates corresponding to the location of the input and output point of the signal. The unit of the coordinates is defined by the `<distance>` element in the `<unit>` element.

`dxf_layer`

This attribute specifies the name of the layer on which the input and output point of the signal is placed.

`mount`

This attribute specifies the placement side of the input and output point of the signal. The value shall be either of the following:

`TOP` The I/O point is placed on the top side of the layer.
`BOTTOM` The I/O point is placed on the bottom side of the layer.

8.2.12.4.9.3 Example

The following is an example of the `<dxf:ref_port>` element in use.

```
<reference
   xmlns:dxf="http://www.jeita.or.jp/LPB/dxf"
   reffile="XXXX.dxf"
   format="DXF"
   distance="mm"
>
      <connection socket_name="socket1" port_id="A1">
        <dxf:ref_port x="100" y="8978"   dxf_layer="L1"  module="TOP" />
      </connection>
      <connection socket_name="socket1" port_id="A2">
        <dxf:ref_port x="200" y="8978"   dxf_layer="L1"  module="TOP" />
      </connection>
      <connection socket_name="socket1" port_id="A3">
        <dxf:ref_port x="300" y="8978"   dxf_layer="L1"  module="TOP" />
      </connection>
</reference>
```

8.2.12.4.10 The <gds:ref_port> element

8.2.12.4.10.1 General

The `<gds:ref_port>` element is used to make a relationship with a GDS II stream format file.

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```
<gds:ref_port
             x="x_coordinate"
             y="y_coordinate"
             gdx_layer="layer_number_in_GDS_file"
>
             [<extensions> element]…
</gds:ref_port>
```

The GDS II language does not have a concept of the I/O terminal. Therefore, coordinates are used to create the relationship with a port in the C-Format file.

8.2.12.4.10.2 Attribute definitions

The attributes of the `<gds:ref_port>` element are defined as follows.

`x`
`y`

These attributes specify the coordinates corresponding to the location of the input and output point of the signal. The unit of the coordinates is defined by the `<distance>` element in the `<unit>` element.

`gds_layer`

This attribute specifies the number of layers on which input and output point of the signal is placed.

8.2.12.4.10.3 Example

The following is an example of the `<gds:ref_port>` element in use.

```
<reference
   xmlns:gds="http://www.jeita.or.jp/LPB/gds"
   reffile="XXXX.gds"
   format="GDS"
>
  <connection socket_name="socket1" port_id="A1">
      <gds:ref_port x="100" y="8978"   gds_layer="L1" />
  </connection>
  <connection socket_name="socket1" port_id="A2">
      <gds:ref_port x="200" y="8978"   gds_layer="L1"  />
  </connection>
  <connection socket_name="socket1" port_id="A3">
      <gds:ref_port x="300" y="8978"   gds_layer="L1" />
  </connection>
</reference>
```

8.2.12.4.11 The <xfl:ref_port> element

8.2.12.4.11.1 General

The `<xfl:ref_port>` element is used to make a relationship with an LPB G-Format file.

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```
<xfl:ref_port
             component="component_name_in_XFL_file"
             pinname="pin_name_in_XFL_file"
>
             [<extensions> element]…
</xfl:ref_port>
```

8.2.12.4.11.2 Attribute definitions

The attributes of the `<xfl:ref_port>` element are defined as follows.

`component`

> This attribute specifies the name of a component that is defined in the **`.component`** section in the reference G-Format file.

`pinname`

> This attribute specifies the pin name of the component that is defined in the `part` section in the reference G-Format file.

8.2.12.4.11.3 Example

The following is an example of the `<xfl:ref_port>` element in use.

```
<reference
   xmlns:xfl="http://www.jeita.or.jp/LPB/xfl"
   reffile="XXXX.xfl"
   format="XFL"
>
 <connection socket_name="socket1" port_id="A1">
      <xfl:ref_port component="NEWLSIDIE" pinname="1" />
 </connection>
 <connection socket_name="socket1" port_id="A2">
      <xfl:ref_port component="NEWLSIDIE" pinname="2" />
 </connection>
 <connection socket_name="socket1" port_id="A3">
      <xfl:ref_port component="NEWLSIDIE" pinname="3" />
 </connection>
</reference>

 [XXXX.xfl]
.part
DIE R -13.5 -13.5 13.5 13.5 0 S 0 {
    1 -4 -5 B 4
    2  -3 -5 B 4
    3 -2  -5 B 4
            :
}
.end part
.component
   NEWLSIDIE     DIE      0 0 1 0
.end component
```

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8.2.12.4.12 The <ibis:ref_port> element

8.2.12.4.12.1 General

The `<ibis:ref_port>` element is used to make a relationship with an IBIS file.

```
<ibis:ref_port
             component="component_name_in_IBIS_file"
             {signal_name="signal_name_in_IBIS_file" |
              pin_name="pin_name_in_IBIS_file"}
             [terminal_type="terminal_type in IBIS file"]
>
             [<extensions> element]…
</ibis:ref_port>
```

8.2.12.4.12.2 Attribute definitions

The attributes of the `<ibis:ref_port>` element are defined as follows.

`component`

This attribute specifies the name of a component that is defined in the `[Component]` line in the reference IBIS file.

`signal_name`

This attribute specifies the signal name that is defined in the reference IBIS file.

`pin_name`

This attribute specifies the pin name that is defined in the reference IBIS file.

`terminal_type`

This attribute specifies the terminal type that is used in an Interconnect Model of IBIS version 7 or later. The value shall be one of the followings.

`Pin_I/O`	Signal terminal at the package
`Pad_I/O`	Signal terminal at the die pad
`Buffer_I/O`	Signal terminal at the I/O buffer
`Pin_Rail`	Supply terminal at the package
`Pad_Rail`	Supply terminal at the die pad
`Buffer_Rail`	Supply terminal at the I/O buffer
`Pullup_ref`	Supply terminal at the I/O buffer
`Pulldown_ref`	Supply terminal at the I/O buffer
`Power_clamp_ref`	Supply terminal at the I/O buffer
`Gnd_clamp_ref`	Supply terminal at the I/O buffer
`Ext_ref`	Supply terminal at the I/O buffer

If it is not specified, the terminal at the package is set as the default.

8.2.12.4.12.3 Example

The followings are examples of the `<ibis:ref_port>` element in use.

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Example 1: Connect to the package terminals without specifying `terminal_type` attribute.

```
<reference
  xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
  reffile="XXXX.ibs"
  format="IBIS"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis:ref_port  component="DDR3-1Gbx16" signal_name="Vddq"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <ibis:ref_port component="DDR3-1Gbx16"  signal_name="DQU5" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <ibis:ref_port component="DDR3-1Gbx16"  signal_name="DQU7" />
   </connection>
</reference>
```

Example 2: Connect to the package terminals specifying `terminal_type` attribute.

```
<reference
  xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
  reffile="XXXX.ibs"
  format="IBIS"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis:ref_port component="DDR3-1Gbx16" signal_name="Vddq"
      terminal_type="Pin_Rail" />
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <ibis:ref_port component="DDR3-1Gbx16" pin_name="A2"
      terminal_type="Pin_I/O" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <ibis:ref_port component="DDR3-1Gbx16" pin_name="A3"
      terminal_type="Pin_I/O" />
   </connection>
</reference>
```

Example 3: Connect to the die pad terminals specifying `terminal_type` attribute.

```
<reference
  xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
  reffile="XXXX.ibs"
  format="IBIS"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis:ref_port component="DDR3-1Gbx16" signal_name="Vddq"
      terminal_type="Pad_Rail" />
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <ibis:ref_port component="DDR3-1Gbx16" pin_name="A2"
      terminal_type="Pad_I/O" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <ibis:ref_port component="DDR3-1Gbx16" pin_name="A3"
      terminal_type="Pad_I/O" />
   </connection>
</reference>
```

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Example 4: Connect to the I/O buffer terminals specifying `terminal_type` attribute.

```
<reference
  xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
  reffile="XXXX.ibs"
  format="IBIS"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis:ref_port component="DDR3-1Gbx16" signal_name="Vddq"
      terminal_type="Buffer_Rail" />
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <ibis:ref_port component="DDR3-1Gbx16" pin_name="A2"
      terminal_type="Buffer_I/O" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <ibis:ref_port component="DDR3-1Gbx16" pin_name="A3"
      terminal_type="Buffer_I/O" />
   </connection>
</reference>
```

```
XXXX.ibs

[IBIS ver]       7.0
[File name]     XXXX.ibs
 .......
[Component]     DDR3-1Gbx16
[Manufacturer]   JEITA_FACT
[Package]
| variable       typ                  min                  max
R_pkg            0.5                  0.4                  0.6
L_pkg            1.5nH               1.0nH               2.0nH
C_pkg            0.4pF               0.2pF               0.6pF
|
[Pin]  signal_name      model_name      R_pin       L_pin         C_pin
A1     Vddq             POWER
A2     DQU5             DQ_MODEL        0.58        1.9nH        0.58pF
A3     DQU7             DQ_MODEL        0.57        1.85nH       0.57pF
 ....
```

8.2.12.4.13 The <ibis_pkg:ref_port> element

8.2.12.4.13.1 General

The `<ibis_pkg:ref_port>` element is used to make a relationship with an IBIS package model file.

```
<ibis_pkg:ref_port
             package_model="model_name_in_IBIS_pkg_file"
             pin_number="pin_number_in_IBIS_pkg_file"
>
             [<extensions> element]…
</ibis_pkg:ref_port>
```

8.2.12.4.13.2 Attribute definitions

The attributes of the `<ibis_pkg:ref_port>` element are defined as follows.

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`package_model`

This attribute specifies the package model name described in [Define Package Model] data in IBIS package model file.

`pin_number`

This attribute specifies one of pin numbers in [Pin Numbers] data in IBIS package model file.

8.2.12.4.13.3 Example

The following is an example of the `<ibis_pkg:ref_port>` element in use.

```
<reference
  xmlns:ibis_pkg="http://www.jeita.or.jp/LPB/ibis_pkg"
  reffile="XXXX.ibs"
  format="IBIS_PKG"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis_pkg:ref_port  package_model="96ball_pkg" pin_number="A1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
       <ibis_pkg:ref_port package_model="96ball_pkg" pin_number="A2" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
       <ibis_pkg:ref_port package_model="96ball_pkg" pin_number="A3" />
   </connection>
</reference>
```

```
XXXX.ibs

[IBIS ver]       4.2
[File name]     XXXX.ibs
 .......
[Component]     DDR3-1Gbx16
[Manufacturer]   JEITA_FACT
.......
[Define Package Model]  96ball_pkg
.......
[Number of Pins] 68
|
[Pin Numbers]
A1   | Vddq
A2   | Vss
A3   | DQU8
 ....
```

8.2.12.4.14 The <ibis_ebd:ref_port> element

8.2.12.4.14.1 General

The `<ibis_ebd:ref_port>` element is used to make a relationship with an IBIS electrical board description file.

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```
<ibis_ebd:ref_port
             board="board_name_in_IBIS_ebd_file"
             pin_name="pin_name_in_IBIS_ebd_file"
>
             [<extensions> element]…
</ibis_ebd:ref_port>
```

8.2.12.4.14.2 Attribute definitions

The attributes of the `<ibis_ebd:ref_port>` element are defined as follows.

`board`

> This attribute specifies the board name described in [Begin Board Description] data in IBIS board description file.

`pin_name`

> This attribute specifies one of pin names described in [Pin List] data in IBIS board description file.

8.2.12.4.14.3 Example

The following is an example of the `<ibis_ebd:ref_port>` element in use.

```
<reference
  xmlns:ibis_ebd="http://www.jeita.or.jp/LPB/ibis_ebd"
  reffile="XXXX.ebd"
  format="IBIS_EBD"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis_ebd:ref_port  board="board"  pin_name="1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
       <ibis_ebd:ref_port board="board"  pin_name="2" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
       <ibis_ebd:ref_port board="board"  pin_name="3" />
   </connection>
</reference>
```

```
XXXX.ebd

[IBIS ver]       4.2
[File name]     XXXXX.ebd
 .......
[Begin Board Description]  board
[Manufacturer]   JEITA_FACT
|
|
[Number of Pins] 68
|
[Pin List]  signal_name
1         GND
2         GND
3         DQ04
 ....
```

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8.2.12.4.15 The <systemc:ref_port> element

8.2.12.4.15.1 General

The `<systemc:ref_port>` element is used to make a relation with a SystemC file.

```
<systemc:ref_port
             sc_module="module_name_in_systemc_file"
             portname="port_name_of_function"
>
             [<extensions> element]…
</systemc:ref_port>
```

8.2.12.4.15.2 Attribute definitions

The attributes of `<systemc:ref_port>` element are defined as follows:

`sc_module`

This attribute specifies the name of an `sc_module` in the referenced SystemC file.

`portname`

This attribute specifies the name of a port in the referenced SystemC file. The port shall be defined in the `sc_module` that is specified by the `sc_module` attribute.

8.2.12.4.15.3 Example

The following is an example of the `<systemc:ref_port>` element in use.

```
  <reference
      xmlns:systemc="http://www.jeita.or.jp/LPB/systemc"
      reffile="./sample_systemc.dll"
      format="SYSTEMC"
  >
      <connection socket_name="pkg1" port_id="A1">
          <systemc:ref_port sc_module="and" portname="a[0]"/>
      </connection>
      <connection socket_name="pkg1" port_id="A2">
          <systemc:ref_port sc_module="and" portname="a[1]"/>
      </connection>
      <connection socket_name="pkg1" port_id="A3">
          <systemc:ref_port sc_module="and" portname="sum"/>
      </connection>
  </reference>

// sample_systemc.hpp
#include "system.c"
SC_MODULE(and){
    sc_in<bool>  a[2];  // input port
    sc_out<bool> sum;   // output port
    ...... ......
};

// sample_systemc.cpp
#include "sample_systemc.hpp"

SC_MODULE_EXPORT(and);
```

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8.2.12.4.16 The <thermal_2resistor:ref_port> element

8.2.12.4.16.1 General

The `<thermal_2resistor:ref_port>` element is used to make a relationship with two resistor–type thermal model. The socket name can be defined, but the port cannot be defined.

```
<thermal_2resistor:ref_port
             model="model_name_in_thermal_model_file"
>
             [<extensions> element]…
</thermal_2resistor:ref_port>
```

8.2.12.4.16.2 Attribute definitions

The attributes of the `<thermal_2resistor:ref_port>` element are defined as follows.

`model`

This attribute specifies the model name that is defined in two resistor–type thermal model file.

8.2.12.4.16.3 Example

The following is an example of the `<thermal_2resistor:ref_port>` element in use.

```
  <reference
      xmlns:thermal_2resistor="http://www.jeita.or.jp/LPB/thermal_2resistor"
      reffile="./thermal_model/sample_pkg_2resistor.tar.gz"
      format="THERMAL_2RESISTOR"
  >
      <connection socket_name="sample_pkg">
          <thermal_2resistor:ref_port model="pkg_2resistor" />
      </connection>
  </reference>
```

8.2.12.4.17 The <thermal_delphi:ref_port> element

8.2.12.4.17.1 General

The `<thermal_delphi:ref_port>` element is used to make a relationship with thermal delphi thermal model. The socket name can be defined, but the port cannot be defined.

```
<thermal_delphi:ref_port
             model="model_name_in_thermal_model_file"
>
             [<extensions> element]…
</thermal_delphi:ref_port>
```

8.2.12.4.17.2 Attribute definitions

The attributes of the `<thermal_delphi:ref_port>` element are defined as follows.

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model

This attribute specifies the model name that is defined in DELPHI type thermal model file.

8.2.12.4.17.3 Example

The following is an example of the <thermal_delphi:ref_port> element in use.

```
  <reference
      xmlns:thermal_delphi="http://www.jeita.or.jp/LPB/thermal_delphi"
      reffile="./thermal_model/sample_pkg_delphi.tar.gz"
      format="THERMAL_DELPHI"
  >
      <connection socket_name="sample_pkg">
          <thermal_delphi:ref_port model="pkg_delphi" />
      </connection>
  </reference>
```

8.2.12.4.18 The <JLPB:ref_port> element

8.2.12.4.18.1 General

The <JLPB:ref_port> element is used to make a relationship with an LPB C-Format file.

```
<JLPB:ref_port
             module="module_name_in_LPB_CFormat"
             socket="socket_name_in_LPB_CFormat"
             [port_name="port_name_in_LPB_CFormat" |
             port_id="port_identifier_in_LPB_CFormat" ]
>
             [<extensions> element]…
</JLPB:ref_port>
```

8.2.12.4.18.2 Attribute definitions

The attributes of the <JLPB:ref_port> element are defined as follows.

module

This attribute specifies the name of a module that is defined in the <module> element in the reference C-Format file.

socket

This attribute specifies the name of a socket that is defined in the <socket> element in the reference C-Format file. The socket shall be defined in the module that is specified by the module attribute.

port_name

This attribute specifies the name of a port that is defined in the <port> element in the reference C-Format file. The port shall be defined in the socket that is specified by the socket attribute. The port_name attribute shall not be used with the port_id attribute.

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`port_id`

> This attribute specifies the identifier of a port that is defined in the `<port>` element in the reference C-Format file. The port shall be defined in the socket that is specified by the `socket` attribute. The `port_id` attribute shall not be used with the `port_name` attribute.

8.2.12.4.19 The <xml:ref_port> element

8.2.12.4.19.1 General

The `<xml:ref_port>` element is used to make a relationship with the model file that is described by XML.

```
<xml:ref_port
             port_path="xpath"
>
             [<extensions> element]…
</xml:ref_port>
```

The path to nodes in the model file is expressed using XML Path Language (`xpath`).

8.2.12.4.19.2 Attribute definitions

The attributes of the `<xml:ref_port>` element are defined as follows.

`port_path`

> This attribute specifies a path to an I/O node in the referenced model file. The path is expressed by XML Path Language version 1.0.

8.2.12.4.19.3 Example

The following is an example of the `<xml:ref_port>` element in use.

```
<reference
  xmlns:XML="http://www.jeita.or.jp/LPB/xml"
  reffile="ICEMCE.xml"
  format="XML"
  type="ICEM-CE"
>
   <connection socket_name="socket1" port_id="A1">
      <xml:ref_port port_path="/Cemodel/Lead_definitions/Lead[@Id=’3’]"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <xml:ref_port port_path="/Cemodel/Lead_definitions/Lead[@Id=’4’]"/>
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <xml:ref_port port_path="/Cemodel/Lead_definitions/Lead[@Id=’5’]"/>
   </connection>
</reference>
```

```
[ICEMCE.xml]

<Cemodel>
```

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```
     ...
  <Lead_definitions>

    <Lead Id="3" Name="Vssq" Mode="GND"/>
    <Lead Id="4" Name="DQU5" Mode="external"/>
    <Lead Id="5" Name="DQU7" Mode="external"/>

        ...
  </Lead_definitions>
    ...
</Cemodel>
```

8.2.12.5 The <affine_transformation> element

8.2.12.5.1 General

The `<affine_transformation>` element defines an Affine Spatial Transformation Matrix to transform the coordinate of the objects in the referenced geometrical file into that in C-Format file.

```
<affine_transformation
             a11="real_number"
             a12="real_number"
             a13="real_number"
             a14="real_number"
             a21="real_number"
             a22="real_number"
             a23="real_number"
             a24="real_number"
             a31="real_number"
             a32="real_number"
             a33="real_number"
             a34="real_number"
>
             [<step:ref_product> element |
              <sat:ref_body> element>]…
             [<extensions> element]…
</affine_transformation>
```

8.2.12.5.2 Attribute definitions

From a_{11} to a_{34} are matrix element of Affine Spatial Transformation Matrix as follows.

$$M = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

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The transformation of the coordination system in referenced file (x, y, z) to the coordination system in C-Format (x′, y′, z′) is thus defined as:

$$\begin{bmatrix} x' \\ y' \\ z' \\ 1 \end{bmatrix} = M \begin{bmatrix} x \\ y \\ z \\ 1 \end{bmatrix}$$

8.2.12.5.3 Element contents

The `<affine_transformation>` element contains the following elements. The `<step:ref_product>` and `<sat:ref_body>` elements define the objects in the referenced file that are transformed by Affine Spatial Transformation Matrix. If any objects are not defined, all objects in that files are transformed.

```
<step:ref_product>
<sat:ref_body>
<extensions>
```

8.2.12.5.4 The <step:ref_product> element

8.2.12.5.4.1 General

This element is used to specify the objects in the STEP file whose coordinate systems are transformed by affine transformation. The coordinate system of objects placed on the lower hierarchy of the specified object are also transformed by the same affine transformation matrix. Normally, this attribute specifies the top-level object of the referenced STEP file. If the object is not specified, all objects in STEP file are transformed by same Affine Spatial Transformation Matrix.

```
<step:ref_product
             name="object_name_in_STEP_file"
>
             [<extensions> element]…
</step:ref_product>
```

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8.2.12.5.4.2 Attribute definitions

The attribute of `<step:ref_product>` element is defined as follows.

`name`

> This attribute specifies the name of the object in the STEP file whose coordinate system is transformed by affine transformation.

8.2.12.5.4.3 Example

In the following example, the coordinates of IC1_PACKAGE and IC2_PACKAGE objects are moved 100 in the X direction and 200 in the Y direction.

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```
<reference xmlns:step="http://www.jeita.or.jp/LPB/step"
           reffile="xxx.stp" format="STEP">
  <affine_transformation
       a11="1.0" a12="0.0" a13="0.0" a14="100.0"
       a21="0.0" a22="1.0" a23="0.0" a24="200.0"
       a31="0.0" a32="0.0" a33="1.0" a34="0.0"
   >
    <step:ref_product name="IC1_PACKAGE"/>
    <step:ref_product name="IC2_PACKAGE"/>
  </affine_transformation>
</reference>
```

In the following example, the size of the all objects in the STEP file are reduced to 1/2.

```
<reference xmlns:step="http://www.jeita.or.jp/LPB/step"
           reffile="xxx.stp" format="STEP">
  <affine_transformation
       a11="0.5" a12="0.0" a13="0.0" a14="0.0"
       a21="0.0" a22="0.5" a23="0.0" a24="0.0"
       a31="0.0" a32="0.0" a33="0.5" a34="0.0"
   />
</reference>
```

8.2.12.5.5 The <sat:ref_body> element

8.2.12.5.5.1 General

This element is used to specify the objects in the SAT file that transform the coordinate system by affine transformation. The coordinate system of objects placed on the lower hierarchy of the specified object are also transformed by the same affine transformation matrix. Normally, this attribute specifies the top level object of the referenced SAT file. If the object is not specified, all objects in the SAT file are transformed by the same Affine Spatial Transformation Matrix.

```
<sat:ref_body
             name="object_name_in_SAT_file"
>
             [<extensions> element]…
</sat:ref_body>
```

8.2.12.5.5.2 Attribute definitions

The attribute of `<sat:ref_body>` element is defined as follows.

`name`

> This attribute specifies the name of the object in the SAT file whose coordinate system is transformed by affine transformation.

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8.2.12.5.5.3 Example

In the following example, IC3_PACKAGE object is rotated 90 degrees about the Z axis and IC4_PACKAGE is rotated −90 degree about that.

```
<reference xmlns:sat="http://www.jeita.or.jp/LPB/SAT"
           reffile="xxx.sat" format="sat">
  <affine_transformation
       a11="0.0"  a12="1.0" a13="0.0" a14="0.0"
       a21="-1.0" a22="0.0" a23="0.0" a24="0.0"
       a31="0.0"  a32="0.0" a33="1.0" a34="0.0"
  >
    <sat:ref_body name="IC3_PACKAGE"/>
  </affine_transformation>
  <affine_transformation
       a11="0.0" a12="-1.0" a13="0.0" a14="0.0"
       a21="1.0" a22="0.0"  a23="0.0" a24="0.0"
       a31="0.0" a32="0.0"  a33="1.0" a34="0.0"
  >
    <sat:ref_body name="IC4_PACKAGE"/>
  </affine_transformation>
</reference>
```

8.2.12.6 The <material> element

8.2.12.6.1 General

The <material> element is used to define the material for the objects in the referenced geometrical file. The physical parameters of the material are defined in the R-Format file.

```
<material
             name="material_name"
             ref_rule_name="rule_name_in_which_material_is_defined"
>
             [<step:ref_product> element |
              <sat:ref_body> element>]…
             [<extensions> element]…
</material>
```

8.2.12.6.2 Attribute definitions

The attributes of the <material> element are defined as follows.

name

The material name that is defined in the R-Format file.

ref_rule_name

The rule name of the <Physicaldesign> element in the R-Format file in which the material is defined.

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8.2.12.6.3 Element contents

The <material > element contains the following elements. A material is assigned to the objects defined in the <step:ref_product> and <sat:ref_body> elements. If <step: ref_product> is not specified, all objects in step file are made of this material. If <sat: ref_body> is not specified, all objects in the SAT file are made of this material.

```
<step:ref_product>
<sat:ref_body>
<extensions>
```

8.2.12.6.4 The <step:ref_product> element

8.2.12.6.4.1 General

The <step:ref_product> element specifies objects in the referenced STEP file to assign the material. The assigned material does not extend to the objects placed in the lower hierarchy of the specified object.

```
<step:ref_product
             name="object_name_in_STEP_file"
>
             [<extensions> element]…
</step:ref_product>
```

8.2.12.6.4.2 Attribute definitions

The attribute of <step:ref_product> element is defined as follows.

```
name
```

This attribute specifies the name of the object in the STEP file to assign material.

8.2.12.6.4.3 Example

In the following example, silicon is assigned to the DIE object, and 42Alloy is assigned to LEADFRAME01 and LEADFRAME02 objects.

```
<reference xmlns:step="http://www.jeita.or.jp/LPB/step"
           reffile="xxx.stp" format="STEP">
  <material name="Silicon" ref_rule_name="PartsRule">
    <step:ref_product name="DIE" />
  </material>
  <material name="42Alloy" ref_rule_name="PartsRule">
    <step:ref_product name="LEADFRAME01" />
    <step:ref_product name="LEADFRAME02" />
  </material>
</reference>
```

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8.2.12.6.5 The <sat:ref_body> element

8.2.12.6.5.1 General

The `<sat:ref_body>` element specifies objects in the referenced SAT file to assign the material. The assigned material does not extend to the objects placed in the lower hierarchy of the specified object.

```
<sat:ref_body
             name="object_name_in_SAT_file"
>
             [<extensions> element]…
</sat:ref_body>
```

8.2.12.6.5.2 Attribute definitions

The attribute of `<sat:ref_body>` element is defined as follows.

`name`

This attribute specifies the name of the object in the SAT file to assign material.

8.2.12.6.5.3 Example

```
<reference xmlns:sat="http://www.jeita.or.jp/LPB/SAT"
           reffile="xxx.sat" format="sat">
  <material name="Silicon" ref_rule_name="PartsRule">
    <sat:ref_body name="die" />
  </material>
  <material name="42Alloy" ref_rule_name="PartsRule">
    <sat:ref_body name="leadframe01"/>
    <sat:ref_body name="leadframe02"/>
  </material>
</reference>
```

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8.2.12.7 The <heat_source> element

8.2.12.7.1 General

The `<heat_source>` element is used to define the heat sources in the referenced geometrical file.

```
<heat_source
             [min="minimum_power"]
             typ="typical_power"
             [max="maximum_power"]
>
             [<step:ref_product> element |
              <sat:ref_body> element>]…
             [<extensions> element]…
</heat_source>
```

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8.2.12.7.2 Attribute definitions

The attributes of the `<heat_source>` element are defined as follows.

`typ`

> This attribute specifies the typical power. The unit of heating value is defined by the `<power>` element in the `<unit>` element.

`min`
`max`

> These attributes specify the perturbation of power. The `max` and `min` attributes are the maximum and minimum power, respectively. The unit of power is defined by the `<power>` element in the `<unit>` element.

8.2.12.7.3 Element contents

The `<heat_source>` element contains the following elements.

```
<step:ref_product>
<sat:ref_body>
<extensions>
```

The `<step:ref_product>` element and the `<sat:ref_body>` element are used to define the heat source object in the reference file.

If any objects are not defined, the heat is generated from the entire objects in the referenced file.

8.2.12.7.4 The <step:ref_product> element

8.2.12.7.4.1 General

The `<step:ref_product>` element specifies an object in the referenced STEP to assign that heating value. The heat is generated from the entire group including the objects placed in the lower hierarchy of the specified object.

```
<step:ref_product
             name="object_name_in_STEP_file"
>
             [<extensions> element]…
</step:ref_product>
```

8.2.12.7.4.2 Attribute definitions

The attribute of `<step:ref_product>` element is defined as follows.

`name`

> This attribute specifies the name of the object in the STEP file to assign heating value.

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8.2.12.7.4.3 Example

```
<reference xmlns:step="http://www.jeita.or.jp/LPB/step"
           reffile="xxx.stp" format="STEP">
  <heat_source typ="5.0">
    <step:ref_product name="die_soc" />
  </heat_source>
  <heat_source typ="0.2">
    <step:ref_product name="die_ddr0" />
    <step:ref_product name="die_ddr1" />
  </heat_source>
</reference>
```

8.2.12.7.5 The <sat:ref_body> element

8.2.12.7.5.1 General

The `<sat:ref_body>` element specifies an object in the referenced SAT to assign that heating value. The heat is generated from the entire group including the objects placed in the lower hierarchy of the specified object.

```
<sat:ref_body
             name="object_name_in_SAT_file"
>
             [<extensions> element]…
</sat:ref_body>
```

8.2.12.7.5.2 Attribute definitions

The attribute of `<sat:ref_body>` element is defined as follows.

`name`

This attribute specifies the name of the object in the SAT file to which the calorific value is assigned.

8.2.12.7.5.3 Example

```
<reference xmlns:sat="http://www.jeita.or.jp/LPB/sat"
           reffile="xxx.sat" format="SAT">
  <heat_source typ="5.0">
    <sat:ref_body name="die_soc" />
  </heat_source>
  <heat_source typ="0.2">
    <sat:ref_body name="die_ddr0" />
    <sat:ref_body name="die_ddr1" />
  </heat_source>
</reference>
```

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8.3 The <component> element

8.3.1 General

The <component> element, as a direct child element of <LPB_CFORMAT>, is defined here for a compatibility purpose only. Newer applications shall use the <component> element under the <module> element.

The <component> element instantiates modules and gives physical information, such as placement.

```
<component>
             [<placement> element]…
             [<extensions> element]…
</compoment>
```

8.3.2 Element content

The <component> element contains the following elements:

```
<placement>
<extensions>
```

8.3.3 The <placement> element

8.3.3.1 General

The <placement> element defines how to place the module.

```
<placement
             ref_module="name_of_referenced_module"
             inst="instance_name"
             [distance="unit_of_length"]
             [angleunit="unit_of_angle"]
             [scale="geometrical_scale"]
             [x="x_coordinate" y="y_coordinate"]
             [z="z_coordinate"]
             [flip="flip_type"]
             [angle="rotation_angle"]
             [mount="mount_type"]
>
             [<extensions> element]…
/>
```

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8.3.3.2 Attribute definitions

The attributes of the <placement> element are defined as follows:

ref_module

> This attribute specifies the module to be placed by referring the attribute of the module.

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`inst`

The instance name of a child module. The instance name shall be unique in the parent module.

`distance`

This attribute specifies the unit of the x/y coordinate. If this attribute is not specified, the unit that is defined at the `<distance>` element in the `<unit>` element is used. The value shall be one of the followings:

`pm`	picometer
`nm`	nanometer
`um`	micrometer
`mm`	millimeter
`m`	meter

`angleunit`

This attribute specifies the unit of an angle. If this attribute is not specified, the unit that is defined at the `<angle>` element in the `<unit>` element is used. The value shall be either of the following:

```
degree
radian
```

`scale`

This attribute specifies the scale rate of distance. The scale rate shall be more than zero. If this attribute is not specified, 1.0 is used as the default.

`x`
`y`

These attributes specify the location of the reference point of the module. The `x` and `y` attributes specify the x-coordinate and y-coordinate, respectively. The unit of the coordinates is defined by the `<distance>` element in the `<unit>` element.

`z`

This attribute specifies the z-coordinate of the module, namely, the height of the module from the top layer as shown in Figure 49. If this attribute is not specified, zero is set as the default. The unit of the coordinates is defined by the `<distance>` element in the `<unit>` element.

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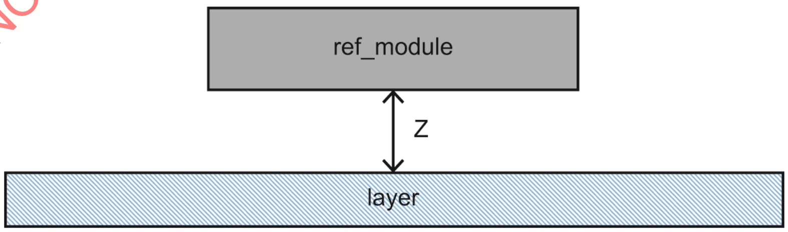

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Figure 49 — Explanatory drawing of the z-coordinate of a module

`flip`

This attribute specifies the type of flip. The value shall be either of the following:

`X`	X-flip flipping about the X axis
`Y`	Y-flip flipping about the Y axis

Figure 50 shows examples of an `X-flip` and a `Y-flip`.

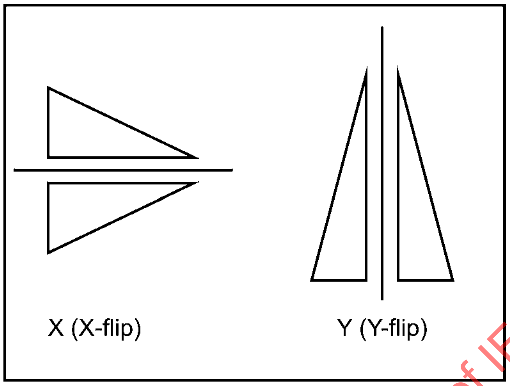

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Figure 50 —Explanatory drawing an X-FLIP and a Y-FLIP

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`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the module. If an angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the `<angle>` element in the `<unit>` element.

`mount`

This attribute specifies the placement of the module. The value shall be one of the following when the mount layer is not specified.

`TOP`	The module is placed on the top side of the substrate.
`BOTTOM`	The module is placed on the bottom side of the substrate.
`MIDDLE`	The module is embedded inside the substrate.

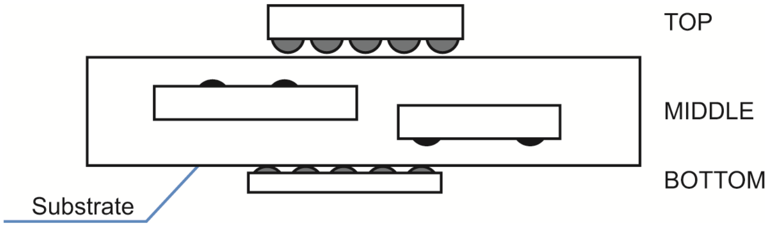

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Figure 51 —An example of the placement of the module

The value shall be one of the following when the mount layer is specified.

TOP The module is placed above the mount layer.
BOTTOM The module is placed below the mount layer.
MIDDLE The module is placed inside the mount layer.

TOP is assumed when this attribute is omitted.

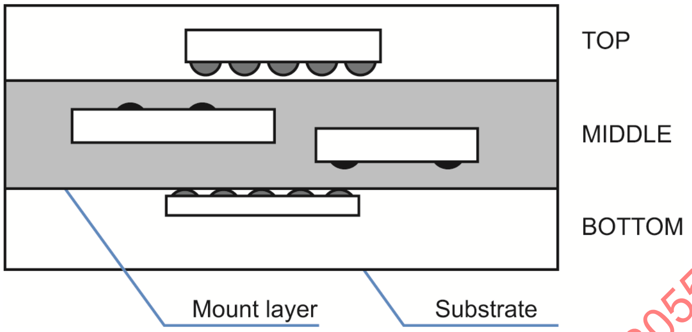

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Figure 52—An example for explaining mount side when layer is specified

8.3.3.3 Example

The following is an example of the <placement> element in use. In the following example, five cells are placed on the TOP of PCB and six cells are placed on the BOTTOM of PCB (Figure 53).

```
<component>
  <placement ref_module="CAP0603B" inst="C10"
            x="-8584.7" y="-4104.9" mount="BOTTOM" />
  <placement ref_module="CAP0603B" inst="C11"
            x="-6584.7" y="-6355.9" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C12"
            x="26092.5" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C13"
            x="30005.4" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C14"
            x="34659.6" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C15"
            x="40178.8" y="37686.8" angle="90" mount="BOTTOM" />

  <placement ref_module="RAS8" inst="RAS8_RN2"
            x="25477.7" y="15729.6" angle="270" mount="TOP" />
  <placement ref_module="RAS8" inst="RAS8_RN4"
            x="43929.3" y="6225.3" angle="270" mount="TOP" />
  <placement ref_module="REGULATOR" inst="REGULATOR"
            x="-12598" y="10183.9" mount="TOP" />
  <placement ref_module="SOC_PKG" inst="SOC"
            x="400" y="-6500" mount="TOP" />
  <placement ref_module="XTAL" inst="XTAL"
            x="-6285.9" y="26473" mount="TOP" />
</component>
```

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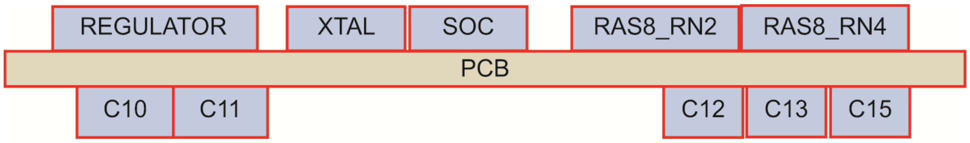

Side View

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Figure 53—An example cell placement

The following is an another example of cell placement. In this example, two cells (`Digital_IC`, `pll_cp`) are stacked on top of one cell (`Interposer_Die`) (Figure 54).

```
<component>
    <placement ref_module="DIE" inst="Interposer_Die" x="0" y="0" stack="1" />
    <placement ref_module="PLL" inst="pll_cp" x="15" y="-5" stack="2" />
    <placement ref_module="IC" inst="DigitalIC" x="-25" y="0" stack="2" />
</component>
```

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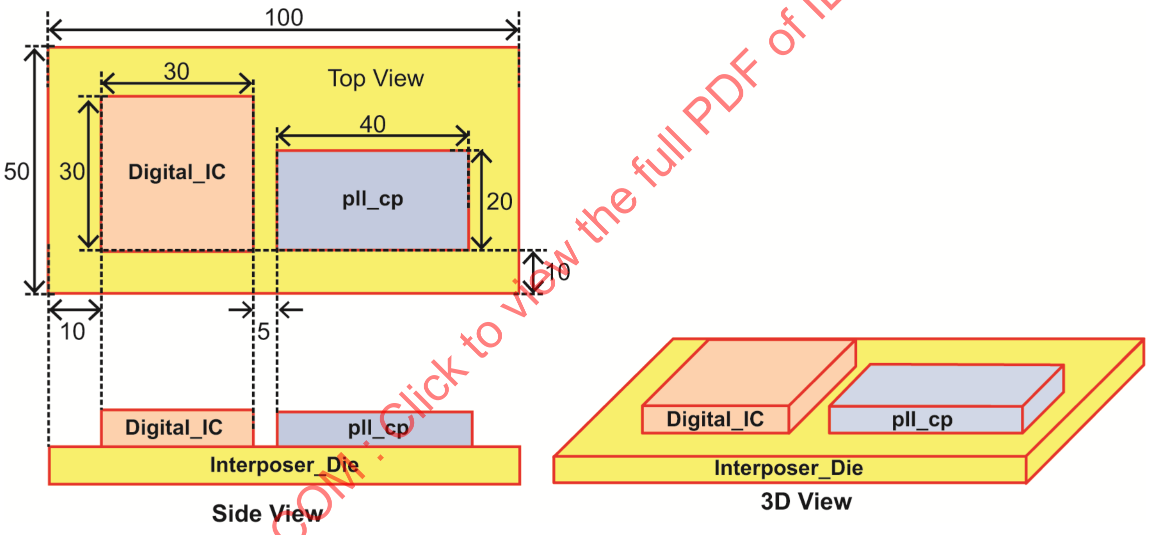

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Figure 54—An example of cells in stackup placement

9. R-Format

9.1 R-Format file structure

The content of the R-Format file consists of one `<header>` element, one `<global>` element, at least one `<Physicaldesign>` element, and zero or one `<Constraintrule>` element. These elements shall be specified in the following order:

```
<LPB_RFORMAT version="2020">
             <header> element
             <global> element
             {<Physicaldesign> element}…
             [<Constraintrule> element]
             [<extensions> element]…
</LPB_RFORMAT>
```

9.2 The <Physicaldesign> element

9.2.1 General

The <Physicaldesign> element specifies the physical parameters, such as the materials of the conductor and dielectric, layer stackup, design rules, via, bonding wire, ball, and mold.

```
<Physicaldesign
             name="design_rule_name"
>
             [<default/>]
             [<material_def> element]
             [<layer_def> element]
             [<spacing_def> element]
             [<pitch_def> element]
             [<bondingwire_def> element]
             [<ball_def> element]
             [<mold> element]
             [<condctor_struct> element]
             [<extensions> element]…
</Physicaldesign>
```

The <Physicaldesign> element consists of the name attribute, zero or one <default> element, zero or one <material_def> element, zero or one <layer_def> element, zero or one <spacing_def> element, zero or one <pitch_def> element, zero or one <bondingwire_def> element, zero or one <ball_def> element, zero or one <mold> element, and zero or one <conductor_struct> element.

9.2.2 Attribute definition

The attribute of the <Physicaldesign> element is defined as follows.

name

This attribute specifies the name of the design rule.

9.2.3 Element content

The <Physicaldesign> element can contain the following elements:

```
<default/>
<material_def>
<layer_def>
<spacing_def>
<pitch_def>
<bondingwire_def>
<ball_def>
<mold>
<condctor_struct>
<extensions>
```

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9.2.4 Example

The following is an example of the <Physicaldesign> element in use.

```
<Physicaldesign name="default_rule">
   <default/>
   <material_def>
      <conductor
         material="COPPER"
         volume_resistivity="1.68e-8"
         temperature="20"
      />
   </material_def>
   <layer_def>
      <layer name="L1"
         type="conductor"
         thickness="10"
         conductor_material="COPPER">
         <line_width min="40"/>
      </layer>
   </layer_def>
   <spacing_def>
      <layer name="L1">
         <line_to_line space="40"/>
         <line_to_via via="VIA_L1_L2" space="40"/>
         <line_to_polygon space="55"/>
      </layer>
   </spacing_def>
   <bondingwire_def>
      <bondingwire name="WIREBOND1" diameter="20" material="GOLD">
         <forward horizontal_length="0" vertical_length="100"/>
         <forward vertical_length="0" horizontal_ratio="0.125"/>
         <length min="500" max="3000"/>
      </bondingwire>
   </bondingwire_def>
   <ball_def>
      <ball name="BGA_Ball" material="SOLDER">
         <frustum height="250" diam1="300" diam2="300"/>
      </ball>
   </ball_def>
   <mold width="12000" depth="12000" height="600" material="RESIN" />
   <conductor_struct>
      <trapezodial_angle layer="L1" angle="60"/>
      <surface_roughness layer="L1" UP_RMS="2" DOWN_RMS="5"/>
   </conductor_struct>
</Physicaldesign>
```

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9.2.5 The <default> element

The <default> element specifies the <Physicaldesign> element as a default design rule of the whole area.

```
<default/>
```

9.2.6 The <material_def> element

9.2.6.1 General

The `<material_def>` element specifies the material of the conductor and dielectric.

```
<material_def>
             [<conductor> element]…
             [<dielectric> element]…
             [<extensions> element]…
</material_def>
```

The `<material_def>` element consists of zero or more `<conductor>` elements and zero or more `<dielectric>` elements.

9.2.6.2 Element content

The `<material_def>` element can contain the following elements:

```
<conductor>
<dielectric>
<extensions>
```

9.2.6.3 Example

The following is an example of the `<material_def>` element in use.

```
<material_def>
    <conductor
       material="COPPER"
       thermal_conductivity="398"
       emissivity="0.06"
       specific_heat_capacity="385"
       density="8.92e3">
       <temperature_characteristic
          temperature="0"
          volume_resistivity="1.55e-8" />
       <temperature_characteristic
          temperature="20"
          volume_resistivity="1.68e-8" />
       <temperature_characteristic
          temperature="100"
          volume_resistivity="2.23e-8" />
       <temperature_characteristic
          temperature="300"
          volume_resistivity="3.6e-8" />
    </conductor>
    <conductor
       material="GOLD"
       thermal_conductivity="320"
       emissivity="0.02"
       specific_heat_capacity="129"
       density="19.3e3">
       <temperature_characteristic
          temperature="0"
          volume_resistivity="2.05e-8" />
       <temperature_characteristic
```

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```
            temperature="20"
            volume_resistivity="2.33e-8" />
        <temperature_characteristic
            temperature="100"
            volume_resistivity="2.88e-8" />
        <temperature_characteristic
            temperature="300"
            volume_resistivity="4.63e-8" />
    </conductor>
    <conductor
        material="SOLDER"
        volume_resistivity="2.17e-7"
        temperature="20"
        thermal_conductivity="49"
        emissivity="0.35"
        specific_heat_capacity="176"
        density="9.0e3" />
    <dielectric
        material="FR-4"
        thermal_conductivity="0.45"
        emissivity="0.91"
        specific_heat_capacity="950"
        density="1800">
        <frequency_characteristic
            frequency="1e6"
            permittivity="4.7"
            tan_delta="0.010" />
        <frequency_characteristic
            frequency="1e9"
            permittivity="4.3"
            tan_delta="0.011" />
        <frequency_characteristic
            frequency="1e10"
            permittivity="4.1"
            tan_delta="0.012" />
    </dielectric>
    <dielectric
        material="RESISTOR_INK"
        permittivity="4.5"
        tan_delta="0.035"
        frequency="1e9"/>
    <dielectric
        material="REGIN"
        permittivity="4.5"
        tan_delta="0.035"
        frequency="1e9"
        thermal_conductivity="2"
        emissivity="0.85"
        specific_heat_capacity="820"
        density="1.73e3" />
</material_def>
```

9.2.6.4 The <conductor> element

9.2.6.4.1 General

The `<conductor>` element specifies the characteristics of the conductor.

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```
<conductor
   material="material_name"
   [volume_resistivity="resistivity"]
   [temperature="temperature"]
   [thermal_conductivity="thermal_conductivity"]
   [emissivity="emissivity"]
   [specific_heat_capacity="specific_heat_capacity"]
   [density="density"]
   [thermal_diffusivity="thermal_diffusivity"]
   [coefficient_of_thermal_expansion="coefficient of thermal expansion"]
   [dynamic_viscosity="dynamic_viscosity"]
   [molecular_weight="molecular_weight"]
>
             [<temperature_characteristic> element]…
             [<extensions> element]…
</conductor>
```

The `<conductor>` element consists of the `material` attribute, the optional `volume_resistivity` attribute, the optional `temperature` attribute, the optional `thermal_conductivity` attribute, the optional `emissivity` attribute, the optional `specific_heat_capacity` attribute, the optional `density` attribute, the optional `thermal_diffusivity` attribute, the optional `coefficient_of_thermal_expansion` attribute, the optional `dynamic_viscosity` attribute, the optional `molecular_weight` attribute, and zero or more `<temperature_characteristic>` and `<extensions>` elements.

9.2.6.4.2 Attribute definitions

The attributes of the `<conductor>` element are defined as follows.

`material`

This attribute specifies the name of the conductor.

`volume_resistivity`

This attribute specifies the volume resistivity of the conductor. The unit of the volume resistivity is defined by the `<resistivity>` element in the `<unit>` element.

`temperature`

This attribute specifies the temperature conditions when the volume resistivity of the conductor is measured. The unit of the temperature is defined by the `<temperature>` element in the `<unit>` element.

`thermal_conductivity`

This attribute specifies the thermal conductivity of the conductor. The unit of the thermal conductivity is defined by the `<thermal_conductivity>` element in the `<unit>` element.

`emissivity`

This attribute specifies the emissivity of the conductor.

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specific_heat_capacity

This attribute specifies the specific heat capacity of the conductor. The unit of the specific heat capacity is defined by the <specific_heat_capacity> element in the <unit> element.

density

This attribute specifies the density of the conductor. The unit of the density is defined by the <density> element in the <unit> element.

thermal_diffusivity

This attribute specifies the thermal diffusivity. The unit of the thermal diffusivity is defined by the <thermal_diffusivity> element in the <unit> element.

coefficient_of_thermal_expansion

This attribute specifies the coefficient of thermal expansion (CTE). The unit of the coefficient of thermal expansion is defined by the <coefficient_of_thermal_expansion> element in the <unit> element.

dynamic_viscosity

This attribute specifies the dynamic viscosity. The unit of the dynamic viscosity is defined by the <dynamic_viscosity> element in the <unit> element.

molecular_weight

This attribute specifies the molecular weight or relative molecular mass.

9.2.6.4.3 Element content

The <conductor> element can contain the following elements:

```
<temperature_characteristic>
<extensions>
```

9.2.6.4.4 Example

The following is an example of the <conductor> element in use.

```
<conductor
            material="COPPER"
            thermal_conductivity="398"
            emissivity="0.06"
            specific_heat_capacity="385"
            density="8.92e3">
            <temperature_characteristic
                        temperature="0"
                        volume_resistivity="1.55e-8" />
            <temperature_characteristic
                        temperature="20"
                        volume_resistivity="1.68e-8" />
            <temperature_characteristic
                        temperature="100"
                        volume_resistivity="2.23e-8" />
            <temperature_characteristic
                        temperature="300"
```

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```
                          volume_resistivity="3.6e-8" />
</conductor>
<conductor>
             material="SOLDER"
             volume_resistivity="2.17e-7"
             temperature="20"
             thermal_conductivity="49"
             emissivity="0.35"
             specific_heat_capacity="176"
             density="9.0e3"
/>
```

9.2.6.4.5 The <temperature_characteristic> element

9.2.6.4.5.1 General

The <temperature_characteristic> element specifies the temperature-dependent volume resistivity of the conductor.

```
<temperature_characteristic
             temperature="temperature"
             volume_resistivity="volume_resistivity"
>
             [<extensions> element]…
</temperature_characteristic>
```

The <temperature_characteristic> element consists of the temperature attribute and the volume_resistivity attribute.

9.2.6.4.5.2 Attribute definitions

The attributes of the <temperature_characteristic> element are defined as follows.

temperature

> This attribute specifies the temperature conditions when the volume resistivity of the conductor is measured. The unit of the temperature is defined by the <temperature> element in the <unit> element.

volume_resistivity

> This attribute specifies the volume resistivity of the conductor. The unit of the volume resistivity is defined by the <resistivity> element in the <unit> element.

9.2.6.4.5.3 Example

The following is an example of the <temperature_characteristic> element in use.

```
<temperature_characteristic
             temperature="0"
             volume_resistivity="1.55e-8"
/>
```

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9.2.6.5 The <dielectric> element

9.2.6.5.1 General

The <dielectric> element specifies the characteristics of the dielectric.

```
<dielectric
   material="material_name"
   [permittivity="permittivity"]
   [tan_delta="loss_tangent"]
   [frequency="frequency"]
   [thermal_conductivity="thermal_conductivity"]
   [emissivity="emissivity"]
   [specific_heat_capacity="specific_heat_capacity"]
   [density="density"]
   [thermal_diffusivity="thermal_diffusivity"]
   [coefficient_of_thermal_expansion="coefficient of thermal expansion"]
   [dynamic_viscosity="dynamic_viscosity"]
   [molecular_weight="molecular_weight"]
>
              [<frequency_characteristic> element]…
              [<extensions> element]…
</dielectric>
```

The <dielectric> element consists of the material attribute, the optional permittivity attribute, the optional tan_delta attribute, the optional frequency attribute, the optional thermal_conductivity attribute, the optional emissivity attribute, the optional specific_heat_capacity attribute, the optional density attribute, the optional thermal_diffusivity attribute, the optional coefficient_of_thermal_expansion attribute, the optional dynamic_viscosity attribute, the optional molecular_weight attribute, and zero or more frequency_characteristic elements.

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9.2.6.5.2 Attribute definitions

The attributes of the <dielectric> element are defined as follows.

material

This attribute specifies the name of the dielectric material.

permittivity

This attribute specifies the dielectric constant of the material.

tan_delta

This attribute specifies the dissipation factor of the material.

frequency

This attribute specifies the frequency that is used when the dielectric properties are measured. The unit of the frequency is defined by the <frequency> element in the <unit> element.

`thermal_conductivity`

This attribute specifies the thermal conductivity of the conductor. The unit of the thermal_conductivity is defined by the `<thermal_conductivity>` element in the `<unit>` element.

`emissivity`

This attribute specifies the emissivity of the conductor.

`specific_heat_capacity`

This attribute specifies the specific heat capacity of the conductor. The unit of the specific heat capacity is defined by the `<specific_heat_capacity>` element in the `<unit>` element.

`density`

This attribute specifies the density of the conductor. The unit of the density is defined by the `<density>` element in the `<unit>` element.

`thermal_diffusivity`

This attribute specifies the thermal_diffusivity. The unit of the thermal diffusivity is defined by the `<thermal_diffusivity>` element in the `<unit>` element.

`coefficient_of_thermal_expansion`

This attribute specifies the coefficient of thermal expansion (CTE). The unit of the coefficient of thermal expansion is defined by the `<coefficient_of_thermal_expansion>` element in the `<unit>` element.

`dynamic_viscosity`

This attribute specifies the dynamic viscosity. The unit of the dynamic viscosity is defined by the `<dynamic_viscosity>` element in the `<unit>` element.

`molecular_weight`

This attribute specifies the molecular weight or relative molecular mass.

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9.2.6.5.3 Element contents

The `<dielectric>` element can contain the following elements:

```
<frequency_characteristic>
<extensions>
```

9.2.6.5.4 Example

The following is an example of the `<dielectric>` element in use.

```
<dielectric
             material="FR-4"
             permittivity="4.5"
             tan_delta="0.035"
             frequency="1e9"
/>

<dielectric
             material="FR-4"
             thermal_conductivity="0.45"
             emissivity="0.91"
             specific_heat_capacity="950"
             density="1800">
             <frequency_characteristic
                           frequency="1e6"
                           permittivity="4.7"
                           tan_delta="0.010" />
             <frequency_characteristic
                           frequency="1e9"
                           permittivity="4.3"
                           tan_delta="0.011" />
             <frequency_characteristic
                           frequency="1e10"
                           permittivity="4.1"
                           tan_delta="0.012" />
</dielectric>
<dielectric
             material="REGIN"
             permittivity="4.5"
             tan_delta="0.035"
             frequency="1e9"
             thermal_conductivity="2"
             emissivity="0.85"
             specific_heat_capacity="820"
             density="1.73e3"
/>
```

9.2.6.5.5 The <frequency_characteristic> element

9.2.6.5.5.1 General

The `<frequency_characteristic>` element specifies the frequency dependent permittivity of the dielectric.

```
<frequency_characteristic
             frequency="frequency"
             permittivity="permittivity"
             [tan_delta="tan_delta"]
>
             [<extensions> element]…
</frequency_characteristic>
```

The `<frequency_characteristic>` element consists of the `frequency` attribute, the `permittivity` attribute, and the optional `tan_delta` attribute.

9.2.6.5.5.2 Attribute definitions

The attributes of the `<frequency_characteristic>` element are defined as follows.

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`frequency`

This attribute specifies the frequency that is used when the dielectric properties are measured. The unit of the frequency is defined by the `<frequency>` element in the `<unit>` element.

`permittivity`

This attribute specifies the dielectric constant of the material.

`tan_delta`

This attribute specifies the dissipation factor of the material.

9.2.6.5.5.3 Example

The following is an example of the `<frequency_characteristic>` element in use.

```
<frequency_characteristic
             frequency="1e6"
             permittivity="4.7"
             tan_delta="0.010"
/>
```

9.2.7 The <layer_def> element

The `<layer_def>` element specifies the layer stackup from top to bottom.

```
<layer_def>
             {<layer> element}…
             [<extensions> element]…
</layer_def>
```

The `<layer_def>` element consists of one or more `<layer>` elements.

9.2.7.1 Element content

The `<layer_def>` element contains the following elements:

```
<layer>
<extensions>
```

9.2.7.2 Example

Figure 55 shows an example of the layer stackup that includes the conductor and dielectric layers.

```
<layer_def>
    <layer name="TOP_SR"
       type="dielectric"
       thickness="20"
       dielectric_material="RESISTOR_INK"/>
    <layer name="L1"
       type="conductor"
       thickness="10"
```

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```
           conductor_material="COPPER"
        >
            <line_width min="40"/>
        </layer>
        <layer name="BU_1_2"
           type="dielectric"
           thickness="40"
           dielectric_material="FR-4"
        />
        <layer name="L2"
           type="conductor"
           thickness="10"
           conductor_material="COPPER"
        >
            <line_width min="50"/>
        </layer>
        <layer name="CORE"
           type="dielectric"
           thickness="100"
           dielectric_material="FR-4"
        />
        <layer name="L3"
           type="conductor"
           thickness="10"
           conductor_material="COPPER"
        >
            <line_width min="50"/>
        </layer>
        <layer name="BU_3_4"
           type="dielectric"
           thickness="40"
           dielectric_material="FR-4"
        />
        <layer name="L4"
           type="conductor"
           thickness="10"
           conductor_material="COPPER"
        >
            <line_width min="40"/>
        </layer>
        <layer name="BOTTOM_SR"
            type="dielectric"
            thickness="20"dielectric_material="RESISTOR_INK"
        />
    </layer_def>
```

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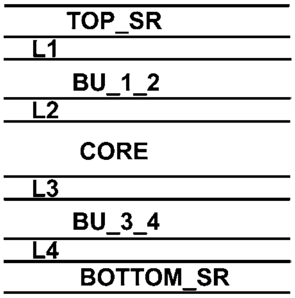

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Figure 55—Example of layer stackup

9.2.7.3 The <layer> element

9.2.7.3.1 General

The `<layer>` element specifies the layer name, type of the layer, thickness of the layer, material of the layer, and design rules for the line width and area.

```
<layer
             name="layer_name"
             type="layer_type"
             thickness="layer_thickness"
             [plate_thickness="plating_thickness"]
             [conductor_material="name_of_conductor_material"]
             [dielectric_material="name_of_dielectric_material"]
>
             [<line_width> element]
             [<area_limit> element]
             [<extensions> element]…
</layer>
```

The `<layer>` element consists of the `name` attribute, the `type` attribute, the `thickness` attribute, the optional `plate_thickness` attribute, the optional `conductor_material` attribute, the optional `dielectric_material` attribute, zero or one `<line_width>` element, zero or one `<area_limit>` element, and zero or more `<extensions>` elements.

9.2.7.3.2 Attribute definitions

The attributes of the `<layer>` element are defined as follows.

`name`

This attribute specifies the layer name.

`type`

This attribute specifies the type of the layer. The values are as follows:

`dielectric`	Dielectric layer
`conductor`	Conductor layer

`thickness`

This attribute specifies the layer thickness that is the overall thickness containing the `plate_thickness`, as shown in Figure 56. The unit of the thickness is defined by the `<distance>` element in the `<unit>` element.

`plate_thickness`

This attribute specifies the plating thickness that is contained in the `thickness` attribute, as shown in Figure 56. The unit of the plating thickness is defined by the `<distance>` element in the `<unit>` element.

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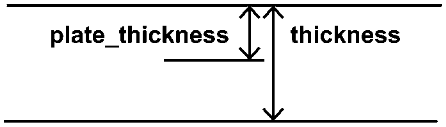

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Figure 56—Explanatory drawing of the relation of plate_thickness and thickness

`conductor_material`

This attribute specifies the name of the conductor material.

`dielectric_material`

This attribute specifies the same of the dielectric material.

9.2.7.3.3 Element content

The `<layer>` element can contain the following elements:

```
    <line_width>
    <area_limit>
    <extensions>
```

9.2.7.3.4 Example

The following is an example of the `<layer>` element in use.

```
<layer
   name="TOP_SR"
    type="dielectric"
    thickness="20"
    dielectric_material="RESISTOR_INK"
/>
<layer
    name="L1"
    type="conductor"
    thickness="10"
    conductor_material="COPPER">
    <line_width min="40"/>
</layer>
<layer
    name="BU_1_2"
    type="dielectric"
    thickness="40"
    dielectric_material="FR-4"
/>
```

9.2.7.3.5 The <line_width> element

9.2.7.3.5.1 General

The `<line_width>` element specifies the design rules for the line width.

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```
<line_width
                min="minimum_line_width"
                [max="maximum_line_width"]
/>
```

The `<line_width>` element consists of the `min` attribute and the optional `max` attribute.

9.2.7.3.5.2 Attribute definitions

The attributes of the `<line_width>` element are defined as follows.

`min`

> This attribute specifies the minimum line width. The unit of the line width is defined by the `<distance>` element in the `<unit>` element.

`max`

> This attribute specifies the maximum line width. The unit of the line width is defined by the `<distance>` element in the `<unit>` element.

9.2.7.3.5.3 Example

The following is an example of the `<line_width>` element in use.

```
<line_width min="40" max="80" />
```

9.2.7.3.6 The <area_limit> element

9.2.7.3.6.1 General

The `<area_limit>` element specifies the minimum area rule.

```
<area_limit
                min="minimum_area"
/>
```

The `<area_limit>` element consists of the `min` attribute.

9.2.7.3.6.2 Attribute definition

The attribute of the `<area_limit>` element is defined as follows.

`min`

> This attribute specifies the minimum metal area. The unit of the metal area is defined by the `<area>` element in the `<unit>` element.

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9.2.7.3.6.3 Example

The following is an example of the <area_limit> element in use.

```
<area_limit min="22500"/>
```

9.2.8 The <spacing_def> element

9.2.8.1 General

The <spacing_def> element defines the design rules of the space, such as the space between lines, between line and via, and between line and polygon.

```
<spacing_def>
             {<layer> element}…
             [<extensions> element]…
</spacing_def>
```

The <spacing_def> element consists of one or more <layer> and <extensions> elements.

9.2.8.2 Element content

The <spacing_def> element contains the following elements:

```
     <layer>
     <extensions>
```

9.2.8.3 Example

The following is an example of the <spacing_def> element in use.

```
<spacing_def>
    <layer name="L1">
        <line_to_line space="40"/>
        <line_to_via via="VIA_L1_L2" space="40"/>
        <line_to_polygon space="55"/>
    </layer>
    <layer name="L2">
        <line_to_line space="50"/>
        <line_to_via  space="50"/>
        <line_to_via  space="50"/>
        <line_to_polygon space="55"/>
    </layer>
    <layer name="L3">
        <line_to_line space="50"/>
        <line_to_via space="50"/>
        <line_to_via via="VIA_L3_L4" space="50"/>
        <line_to_polygon space="55"/>
    </layer>
    <layer name="L4">
        <line_to_line space="40"/>
        <line_to_via  space="40"/>
        <line_to_polygon space="55"/>
    </layer>
</spacing_def>
```

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9.2.8.4 The <layer> element

9.2.8.4.1 General

The `<layer>` element defines the design rules of the space, such as the space between lines, between line and via, and between line and polygon (see Figure 57).

```
<layer
             name="layer_name"
>
             [<line_to_line> element]
             [<line_to_via> element]…
             [<line_to_polygon> element]
             [<extensions> element]…
</layer>
```

The `<layer>` element consists of the `name` attribute, zero or one `<line_to_line>` element, zero or more `<line_to_via>` elements, and zero or one `<line_to_polygon>` and `<extensions>` element.

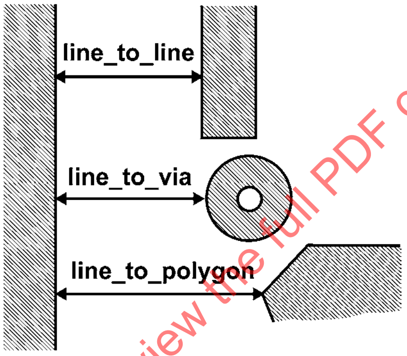

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Figure 57—Example of spacing rules

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9.2.8.4.2 Attribute definition

The attribute of the `<layer>` element is defined as follows.

`name`

This attribute specifies the name of the layer.

9.2.8.4.3 Element content

The `<layer>` element can contain the following elements:

```
<line_to_line>
<line_to_via>
<line_to_polygon>
<extensions>
```

9.2.8.4.4 Example

The following is an example of the `<layer>` element in use.

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```
<layer name="L1">
   <line_to_line    space="40"/>
   <line_to_via     via="VIA_L1_L2" space="40"/>
   <line_to_polygon space="55"/>
</layer>
<layer name="L2">
   <line_to_line    space="50"/>
   <line_to_via     space="50"/>
   <line_to_polygon space="55"/>
</layer>
```

9.2.8.4.5 The <line_to_line> element

9.2.8.4.5.1 General

The <line_to_line> element specifies the space between lines.

```
<line_to_line
             space="minimum_spacing"
/>
```

The <line_to_line> element consists of the space attribute.

9.2.8.4.5.2 Attribute definition

The attribute of the <line_to_line> element is defined as follows.

space

This attribute specifies the minimum space between lines.

9.2.8.4.5.3 Example

The following is an example of the <line_to_line> element in use.

```
<line_to_line space="50"/>
```

9.2.8.4.6 The <line_to_via> element

9.2.8.4.6.1 General

The <line_to_via> element specifies the space between line and via.

```
<line_to_via
             [via="identifier_of_padstack"]
             space="minimum_spacing"
/>
```

The <line_to_via> element consists of the optional via attribute and the space attribute.

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9.2.8.4.6.2 Attribute definitions

The attributes of the `<line_to_via>` element are defined as follows.

`via`

This attribute specifies the padstack identifier of the via that is applied to the spacing rule.

`space`

This attribute specifies the minimum space between line and via. The unit of the space is defined by the `<distance>` element in the `<unit>` element.

9.2.8.4.6.3 Example

The following is an example of the `<line_to_via>` element in use.

```
<line_to_via via="VIA_L1_L2" space="40"/>
```

9.2.8.4.7 The <line_to_polygon> element

9.2.8.4.7.1 General

The `<line_to_polygon>` element specifies the space between line and polygon.

```
<line_to_polygon
             space="minimum_spacing"
/>
```

The `<line_to_polygon>` element consists of the `space` attribute.

9.2.8.4.7.2 Attribute definition

The attribute of the `<line_to_polygon>` element is defined as follows.

`space`

This attribute specifies the minimum space between line and polygon.

9.2.8.4.7.3 Example

The following is an example of the `<line_to_polygon>` element in use.

```
<line_to_polygon space="55"/>
```

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9.2.9 The <pitch_def> element

9.2.9.1 General

The `<pitch_def>` element specifies the pitch between center to center of vias.

```
<pitch_def>
             {<via_pitch> element}…
             [<extensions> element]…
</pitch_def>
```

The `<pitch_def>` element consists of one or more `<via_pitch>` elements.

9.2.9.2 Element content

The `<pitch_def>` element contains the following elements:

```
<via_pitch>
<extensions>
```

9.2.9.3 Example

The following is an example of when the stack via cannot be used:

```
<pitch_def>
    <via_pitch via1="VIA_L1_L2" via2="VIA_L1_L2" pitch="250"/>
    <via_pitch via1="VIA_L1_L2" via2="VIA_L2_L3" pitch="275"
samenet_pitch="225"/>
    <via_pitch via1="VIA_L2_L3" via2="VIA_L2_L3" pitch="300"/>
    <via_pitch via1="VIA_L2_L3" via2="VIA_L3_L4" pitch="275"
samenet_pitch="225"/>
    <via_pitch via1="VIA_L3_L4" via2="VIA_L3_L4" pitch="250"/>
</pitch_def>
```

The following is an example of when the stack via can be used:

```
<pitch_def>
    <via_pitch via1="VIA_L1_L2" via2="VIA_L1_L2" pitch="250"/>
    <via_pitch via1="VIA_L1_L2" via2="VIA_L2_L3" pitch="275"
stacked_offset="75"/>
    <via_pitch via1="VIA_L2_L3" via2="VIA_L2_L3" pitch="300"/>
    <via_pitch via1="VIA_L2_L3" via2="VIA_L3_L4" pitch="275"
stacked_offset="75"/>
    <via_pitch via1="VIA_L3_L4" via2="VIA_L3_L4" pitch="250"/>
</pitch_def>
```

9.2.9.4 The <via_pitch> element

9.2.9.4.1 General

Figure 58 shows an example of a cross-sectional view of via structure. The `<via_pitch>` elements defines the design rule for via spacing, as shown in Figure 59.

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```
<via_pitch
              via1="identifier_of_padstack"
              via2="identifier_of_padstack"
              pitch="minimum_pitch"
              [samenet_pitch="minimum_pitch_for_same_net"]
              [stacked_offset="acceptable_gap"]
/>
```

The <via_pitch> element specifies the pitch between vias from center to center (see Figure 59). The <via_pitch> element consists of the via1 attribute, the via2 attribute, the pitch attribute, the optional samenet_pitch attribute, and the optional stacked_offset attribute.

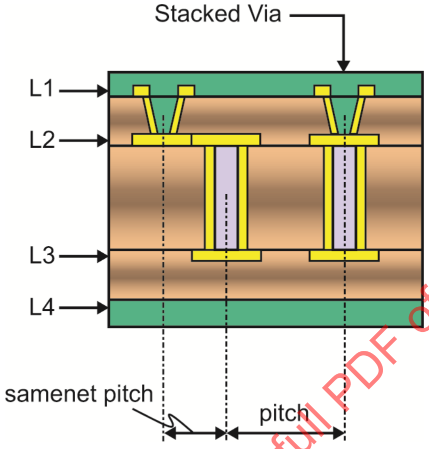

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Figure 58—Example of via structure

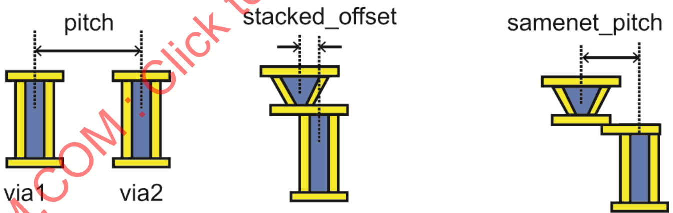

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Figure 59—Example of pitch between vias

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9.2.9.4.2 Attribute definitions

The attributes of the <via_pitch> element are defined as follows.

via1

This attribute specifies the padstack identifier of a via for which the via-pitch rule applies, as shown in Figure 59.

`via2`

This attribute specifies the padstack identifier of a via for which the via-pitch rule applies, as shown in Figure 59.

`pitch`

This attribute specifies the minimum pitch between two vias on different nets, as shown in Figure 59. The unit of the pitch is defined by the `<distance>` element in the `<unit>` element.

`samenet_pitch`

This attribute specifies the minimum pitch between two vias in the same net, as shown in Figure 59. The unit of the pitch is defined by the `<distance>` element in the `<unit>` element.

`stacked_offset`

This attribute specifies the maximum acceptable gap between the centers of stacked vias, as shown in Figure 59. The unit of the offset is defined by the `<distance>` element in the `<unit>` element.

9.2.9.4.3 Example

The following is an example of the `<via_pitch>` element in use.

```
<via_pitch
    via1="VIA_L1_L2"
    via2="VIA_L1_L2"
    pitch="250"
/>
<via_pitch
    via1="VIA_L1_L2"
    via2="VIA_L2_L3"
    pitch="275"
    samenet_pitch="225"
/>
<via_pitch
    via1="VIA_L1_L2"
    via2="VIA_L2_L3"
    pitch="275"
    stacked_offset="75"
/>
```

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9.2.10 The <bondingwire_def> element

9.2.10.1 General

The `<bondingwire_def>` element specifies the shape and material of the bonding wire.

```
<bondingwire_def>
                {<bondingwire> element}…
                [<extensions> element]…
</bondingwire_def>
```

The `<bondingwire_def>` element consists of one or more `<bondingwire>` elements.

9.2.10.2 Element content

The <bondingwire_def> element contains the following elements:

```
<bondingwire>
<extensions>
```

9.2.10.3 Example

The following is an example of the <bondingwire_def> element in use.

```
<bondingwire_def>
   <bondingwire name="WIREBOND1" diameter="20" material="GOLD">
       <forward horizontal_length="0" vertical_length="100"/>
       <forward vertical_length="0" horizontal_ratio="0.125"/>
       <length min="500" max="3000"/>
   </bondingwire>
</bondingwire_def>
```

9.2.10.4 The <bondingwire> element

9.2.10.4.1 General

The <bondingwire> element specifies the shape and material of the bonding wire.

```
<bondingwire
              name="wire_name"
              diameter="wire_diameter"
              [material="material_name"]
>
              [<forward> element]…
              [<backward> element]…
              [<length> element]
              [<extensions> element]…
</bondingwire>
```

The <bondingwire> element consists of the name attribute, the diameter attribute, the optional material attribute, zero or more <forward> elements, zero or more <backward> and <extensions> elements, and zero or one <length> element.

9.2.10.4.2 Attribute definitions

The attributes of the <bondingwire> element are defined as follows.

name

This attribute specifies the name of the bonding wire.

diameter

This attribute specifies the diameter of the bonding wire. The unit of the diameter is defined by the <distance> element in the <unit> element.

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`material`

This attribute specifies the material of the bonding wire.

9.2.10.4.3 Element content

The `<bondingwire>` element can contain the following elements:

```
<forward>
<backward>
<length>
<extensions>
```

9.2.10.4.4 Example

Figure 60 shows an example of a JEDEC 4-point wire bonding shape that is defined by the corresponding `<bondingwire_def>` descriptions as follows.

JEDEC 4-point:

```
<bondingwire_def>
    <bondingwire name="WIREBOND1" diameter="20" material="GOLD">
        <forward horizontal_length="0" vertical_length="100"/>
        <forward vertical_length="0" horizontal_ratio="0.125"/>
        <length min="500" max="3000"/>
    </bondingwire>
</bondingwire_def>
```

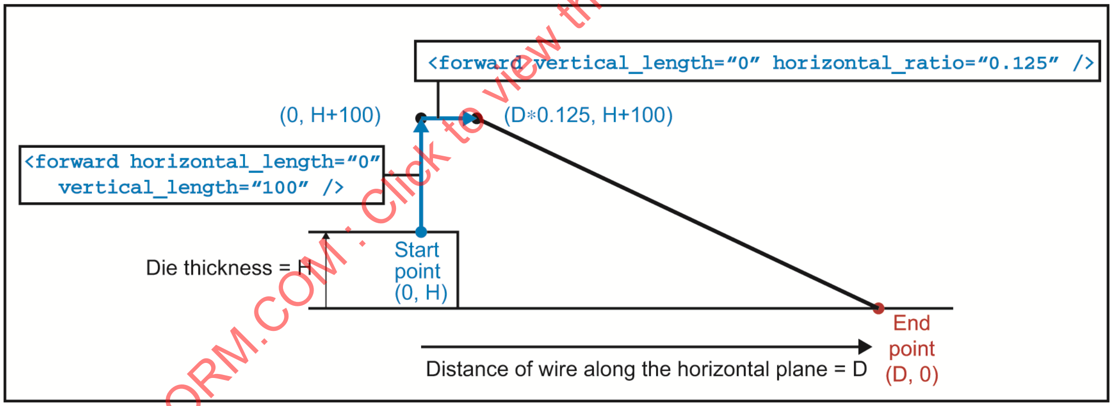
<forward vertical_length=“0” horizontal_ratio=“0.125” />
(0, H+100)
(D*0.125, H+100)
<forward horizontal_length=“0”
vertical_length=“100” />
Die thickness = H
Start
point
(0, H)
End
point
(D, 0)
Distance of wire along the horizontal plane = D

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Figure 60 —Example of bonding wire shape (JEDEC 4-point)

Figure 61 shows an example of a JEDEC 5-point wire bonding shape that is defined by the corresponding `<bondingwire_def>` descriptions as follows.

JEDEC 5-point:

```
<bondingwire_def>
    <bondingwire name="WIREBOND2" diameter="20" material="GOLD">
        <forward vertical_length="100" angle="80"/>
        <forward vertical_length="0" horizontal_ratio="0.125"/>
```

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```
        <backward angle="20" horizontal_ratio="0.5"/>
        <length min="500" max="3000"/>
    </bondingwire>
</bondingwire_def>
```

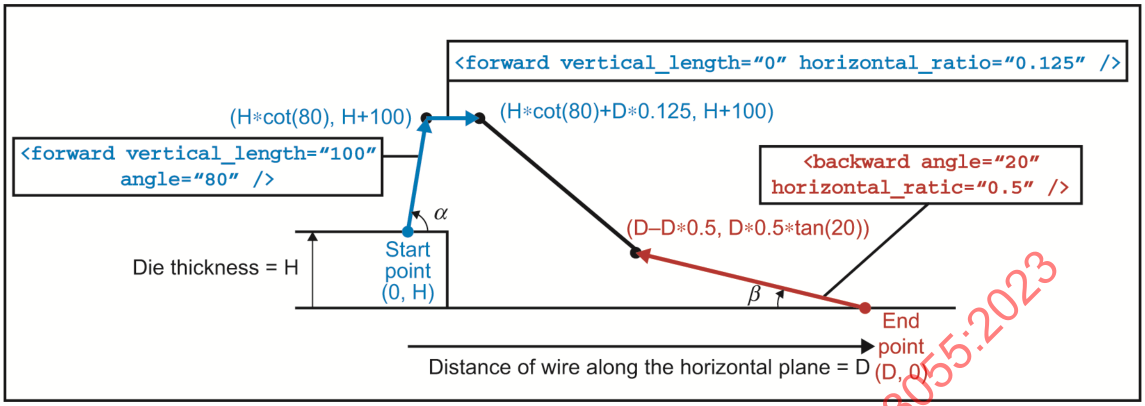
<forward vertical_length="0" horizontal_ratio="0.125" />
(H∗cot(80), H+100)
(H∗cot(80)+D∗0.125, H+100)
<forward vertical_length="100" angle="80" />
<backward angle="20" horizontal_ratic="0.5" />
α
(D–D∗0.5, D∗0.5∗tan(20))
Die thickness = H
Start point (0, H)
β
End point (D, 0)
Distance of wire along the horizontal plane = D

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Figure 61—Example of bonding wire shape (JEDEC 5-point)

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9.2.10.4.5 The <forward> element

9.2.10.4.5.1 General

The <forward> element specifies the loop of the bonding wire from the die side.

```
<forward
             horizontal_length="horizontal_length"
             vertical_length="vertical_length"
             angle="die_side_angle"
             horizontal_ratio="horizontal_ratio"
/>
```

Some <forward> elements are specified from the first position to the second position toward the bonding finger (see Figure 62). The <forward> element consists of the optional horizontal_length attribute, the optional vertical_length attribute, the optional angle attribute, and the optional horizontal_ratio attribute.

9.2.10.4.5.2 Attribute definitions

The attributes of the <forward> element are defined as follows.

horizontal_length

This attribute specifies the horizontal length from the first position toward the bonding finger, as shown in Figure 62. The unit of the length is defined by the <distance> element in the <unit> element.

`vertical_length`

This attribute specifies the vertical length from the first position toward the bonding finger, as shown in Figure 62. The unit of the length is defined by the `<distance>` element in the `<unit>` element.

`angle`

This attribute specifies the angle from the first position toward the second position. The unit of the angle is defined by the `<angle>` element in the `<unit>` element.

`horizontal_ratio`

This attribute specifies the ratio of the horizontal length (L1) and the total length (L) in Figure 62.

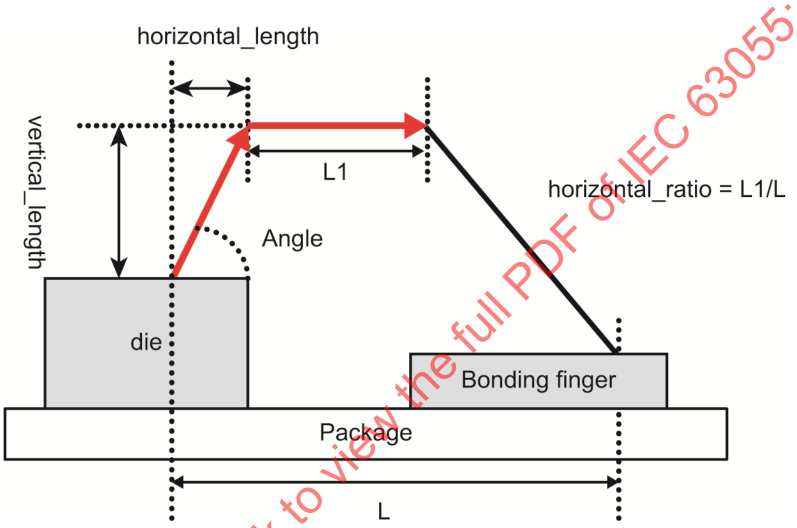

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Figure 62—Explanatory drawing of the shape of a bonding wire

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9.2.10.4.5.3 Example

The following is an example of the `<forward>` element in use.

```
<forward horizontal_length="0" vertical_length="100"/>
<forward vertical_length="0"   horizontal_ratio="0.125"/>
```

9.2.10.4.6 The <backward> element

9.2.10.4.6.1 General

The `<backward>` element specifies the loop of the bonding wire from the bonding finger.

```
<backward
              horizontal_length="horizontal_length"
              vertical_length="vertical_length"
              angle="die_side_angle"
              horizontal_ratio="horizontal_ratio"
/>
```

Some <backward> elements are specified from the first position to the second position toward the die (see Figure 63). The <backward> element consists of the optional horizontal_length attribute, the optional vertical_length attribute, the optional angle attribute, and the optional horizontal_ratio attribute.

9.2.10.4.6.2 Attribute definitions

The attributes of the <backward> element are defined as follows.

horizontal_length

This attribute specifies the horizontal length from the position toward the die, as shown in Figure 63. The unit of the length is defined by the <distance> element in the <unit> element.

vertical_length

This attribute specifies the vertical length from the first position toward the die, as shown in Figure 63. The unit of the length is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle from the first position toward the die, as shown in Figure 63. The unit of the angle is defined by the <angle> element in the <unit> element.

horizontal_ratio

This attribute specifies the ratio of the horizontal length (L1) and total length (L) in Figure 63.

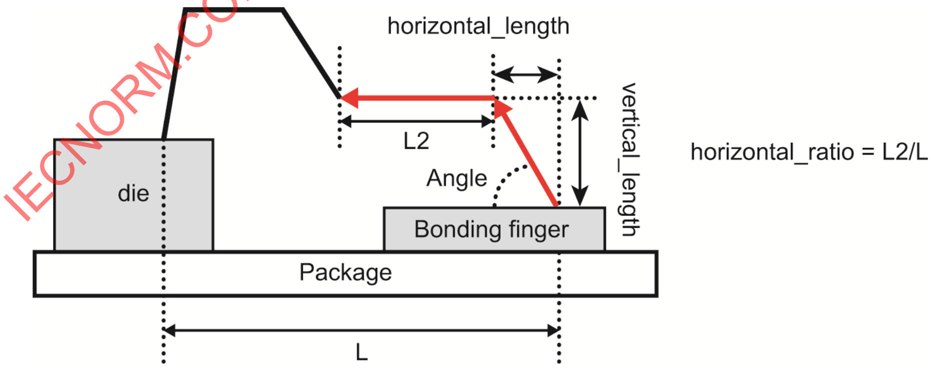

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Figure 63—Explanatory drawing of the shape of a bonding wire

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9.2.10.4.6.3 Example

The following is an example of the `<backward>` element in use.

```
<backward angle="20" horizontal_ratio="0.5"/>
```

9.2.10.4.7 The <length> element

9.2.10.4.7.1 General

The `<length>` element specifies the minimum length and maximum length of the bonding wire.

```
<length
             min="minimum_length"
             max="maximum_length"
/>
```

The `<length>` element consists of the `min` attribute and the `max` attribute.

9.2.10.4.7.2 Attribute definitions

The attributes of the `<length>` element are defined as follows.

`min`

This attribute specifies the minimum length of the bonding wire.

`max`

This attribute specifies the maximum length of the bonding wire.

The unit of the length is defined by the `<distance>` element in the `<unit>` element.

9.2.10.4.7.3 Example

The following is an example of the `<length>` element in use.

```
<length min="500" max="3000"/>
```

9.2.11 The <ball_def> element

9.2.11.1 General

The `<ball_def>` element specifies the material and shape of the solder ball.

```
<ball_def>
             {<ball> element}…
             [<extensions> element]…
</ball_def>
```

The `<ball_def>` element consists of one or more `<ball>` and zero or more `<extensions>` elements.

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9.2.11.2 Element content

The <ball_def> element contains the following elements:

```
<ball>
<extensions>
```

9.2.11.3 Example

The following is an example of the <ball_def> element in use.

```
<ball_def>
    <ball name="BGA_Ball" material="SOLDER">
        <frustum height="250" diam1="300" diam2="300"/>
    </ball>
</ball_def>
```

9.2.11.4 The <ball> element

9.2.11.4.1 General

The <ball> element specifies the material and shape of the solder ball.

```
<ball
             name="ball_name"
             [material="material_name"]
>
             {<frustum> element>}…
</ball>
```

The <ball> element consists of the name attribute, the optional material attribute, and one or more <frustum> elements.

9.2.11.4.2 Attribute definitions

The attributes of the <ball> element are defined as follows.

name

This attribute specifies the name of the solder ball.

material

This attribute specifies the material of the solder ball.

9.2.11.4.3 Element content

The <ball> element contains the following element:

```
<frustum>
```

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9.2.11.4.4 Example

The following is an example of the `<ball>` element in use.

```
<ball name="BGA_Ball" material="SOLDER">
   <frustum height="250" diam1="300" diam2="300"/>
</ball>
```

9.2.11.4.5 The <frustum> element

9.2.11.4.5.1 General

The `<frustum>` element specifies the geometry of the solder ball.

```
<frustum
            height="height"
            diam1="diameter_of_top_side"
            diam2="diameter_of_bottom_side"
/>
```

The shape of the solder ball is given by a group of one or more frustums, as shown in Figure 64. The frustums are stacked up from top to bottom. The `<frustum>` element consists of the `height` attribute, the `diam1` attribute, and the `diam2` attribute.

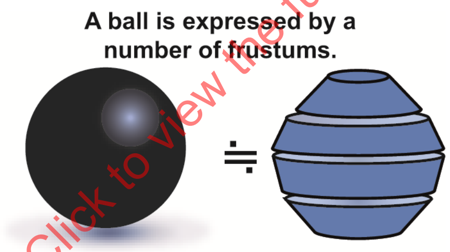

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Figure 64—Example of ball expression

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9.2.11.4.5.2 Attribute definitions

The attributes of the `<frustum>` element are defined as follows.

`height`

> This attribute specifies the height of the frustum. The unit of the height is defined by the `<distance>` element in the `<unit>` element.

`diam1`

> This attribute specifies the diameter of the top side of the frustum. The unit of the diameter is defined by the `<distance>` element in the `<unit>` element.

diam2

This attribute specifies the diameter of the bottom side of the frustum. The unit of the diameter is defined by the <distance> element in the <unit> element.

Figure 65 shows the relationship of the dimensional attributes of a <frustum>: height, diam1, and diam2.

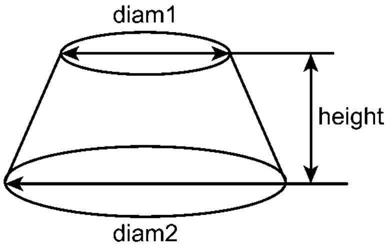

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Figure 65—Explanatory drawing of the shape of a frustum

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9.2.11.4.5.3 Example

The following is an example of the <frustum> element in use.

```
<ball name="BGA_Ball" material="SOLDER">
   <frustum height ="250" diam1="300" diam2="300" />
</ball>
```

9.2.12 The <mold> element

9.2.12.1 General

The <mold> element specifies the geometry and material of the package mold.

```
<mold
             width="width"
             depth="depth"
             height="height"
             material="material_name"
>
             [<extensions> element]…
</mold>
```

The <mold> element consists of the width attribute, the depth attribute, the height attribute, and the material attribute. Figure 66 explains the height attribute of a <mold> element in relation to the layer stackup.

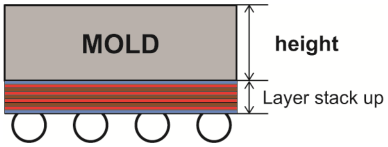

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Figure 66—Explanatory drawing of the `height` attribute of a mold

9.2.12.2 Attribute definitions

The attributes of the `<mold>` element are defined as follows.

`width`

This attribute specifies the width of the package mold, as shown in Figure 67.

`depth`

This attribute specifies the depth of the package mold, as shown in Figure 67.

`height`

This attribute specifies the height of the package mold, as shown in Figure 67.

`material`

This attribute specifies the material of the package mold.

The unit of the width, depth, and height is defined by the `<distance>` element in the `<unit>` element.

Figure 67 shows the `width`, `depth`, and `height` attributes of the `<mold>` element.

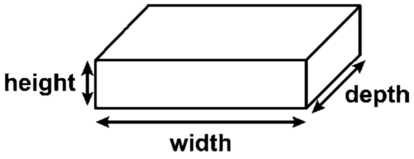

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Figure 67—Explanatory drawing of the shape of a mold

9.2.12.3 Element content

The `<mold>` element contains the following element:

`<extensions>`

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9.2.12.4 Example

The following is an example of the `<mold>` element in use.

```
<mold
    width="12000"
    depth="12000"
    height="600"
    material="RESIN"
/>
```

9.2.13 The <conductor_struct> element

9.2.13.1 General

The `<conductor_struct>` element specifies the cross-section of the conductor.

```
<conductor_struct>
             [<trapezoidal_angle> element]…
             [<surface_roughness> element]…
             [<extensions> element]…
</conductor_struct>
```

The cross-sectional shape of the conductor is specified as trapezoidal with a specified angle. The `<conductor_struct>` element consists of zero or more `<trapezoidal_angle>` elements and zero or more `<surface_roughness>` elements.

9.2.13.2 Element content

The `<conductor_struct>` element can contain the following elements:

```
<trapezoidal_angle>
<surface_roughness>
<extensions>
```

9.2.13.3 Example

The following is an example of the `<conductor_struct>` element in use.

```
<conductor_struct>
    <trapezodial_angle layer="L1" angle="60"/>
    <trapezodial_angle layer="L4" angle="-60"/>
    <surface_roughness layer="L1" UP_RMS="2" DOWN_RMS="5"/>
    <surface_roughness layer="L4" UP_RMS="5" DOWN_RMS="2"/>
</conductor_struct>
```

9.2.13.4 The <trapezoidal_angle> element

9.2.13.4.1 General

The `<trapezoidal_angle>` element specifies the cross-sectional shape of the conductor.

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```
<trapezoidal_angle
             layer="layer_name"
             angle="angle"
/>
```

The `<trapezoidal_angle>` element consists of the `layer` attribute and the `angle` attribute.

9.2.13.4.2 Attribute definitions

The attributes of the `<trapezoidal_angle>` element are defined as follows.

`layer`

This attribute specifies the name of the conductor layer that is specified in the `<layer_def>` element.

`angle`

The cross-sectional shape of the conductor is specified as trapezoidal. This attribute specifies the angle of the trapezoid. The unit of the angle is defined by the `<angle>` element in the `<unit>` element.

Figure 68 shows various trapezoidal cross-sectional shapes of the conductor.

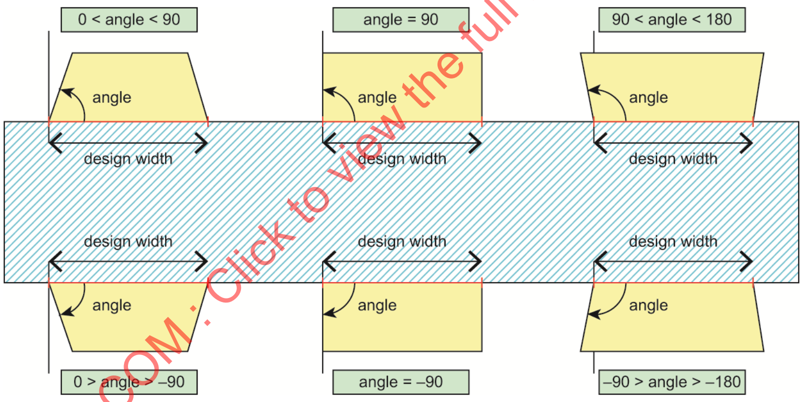

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Figure 68 —Explanatory drawing of trapezoidal angles

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9.2.13.4.3 Example

The following is an example of the `<trapezoidal_angle>` element in use.

```
<trapezodial_angle layer="L1" angle="60"/>
<trapezodial_angle layer="L4" angle="-60"/>
```

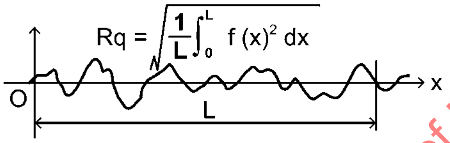
9.2.13.5 The <surface_roughness> element

9.2.13.5.1 General

The `<surface_roughness>` element specifies the roughness of the conductor surface.

```
<surface_roughness
              layer="layer_name"
              UP_RMS="up_rms"
              DOWN_RMS="down_rms"
/>
```

The `<surface_roughness>` element consists of the layer attribute, the `UP_RMS` attribute, and the `DOWN_RMS` attribute. Figure 69 shows the roughness of the conductor surface in root mean square (RMS).



Rq: RMS deviation of the primary profile.

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Figure 69 —Explanatory drawing of surface roughness

9.2.13.5.2 Attribute definitions

The attributes of the `<surface_roughness>` element are defined as follows.

`layer`

This attribute specifies the name of the conductor layer that is specified in the `<layer_def>` element.

`UP_RMS`

This attribute specifies the roughness of the top side surface of the conductor in RMS.

`DOWN_RMS`

This attribute specifies the roughness of the bottom side surface of the conductor in RMS.

Figure 70 shows `layer`, `UP_RMS`, and `DOWN_RMS` as attributes of the `<surface_roughness>` element.

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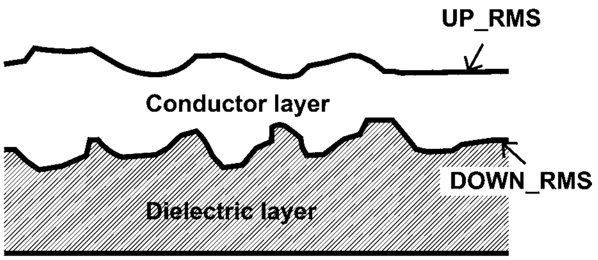

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Figure 70—Explanatory drawing of `UP_RMS` and `DOWN_RMS`

9.2.13.5.3 Example

The following is an example of the `<surface_roughness>` element in use.

```
<surface_roughness layer="L1" UP_RMS="2" DOWN_RMS="5"/>
<surface_roughness layer="L4" UP_RMS="5" DOWN_RMS="2"/>
```

9.3 The <Constraintrule> element

9.3.1 General

The `<Constraintrule>` element specifies the limited height of the component by the `<height_limit>` element, specifies the layout routing inhibition area by `<blockage>` element, and also specifies the non-default design rule area by the `<design_rule_area>` element.

```
<Constraintrule>
             [<height_limit> element]…
             [<blockage> element]…
             [<design_rule_area> element]…
             [<extensions> element]…
</Constraintrule>
```

The `<Constraintrule>` element consists of zero or more `<height_limit>` elements, zero or more `<blockage>` elements, and zero or more `<design_rule_area>` elements.

9.3.2 Element content

The `<Constraintrule>` element can contain the following elements:

```
<height_limit>
<blockage>
<design_rule_area>
<extensions>
```

9.3.3 Example

The following is an example of the `<Constraintrule>` element in use.

```
<Constraintrule>
    <height_limit>
```

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```
        <top
            name="Top_Connector_Location"
            height="200"
            shape_id="Rec_6000um_8000um"
            x="3000" y="2000"
        />
        <bottom
            name="Bottom_Connector_Location"
            height="200"
            shape_id="Rec_6000um_8000um"
            x="3000" y="2000"
        />
    </height_limit>
    <blockage>
        <placement
            layer="L1"
            shape_id="kout_top_200um_200um"
            x="100"
            y="100"
        />
        <routing
            layer="L1"
            shape_id="kout_top_200um_200um"
            x="100"
            y="100"
        />
        <routing
            layer="L4"
            shape_id="kout_bottom_400um_400um"
            x="0"
            y="0"
        />
    </blockage>
    <design_rule_area
        ref_rule_name="C4_Area"
        shape_id="SQ_6000um_6000um"
        x="0" y="0"
        priority="10"
    />
</Constraintrule>
```

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9.3.4 The <height_limit> element

9.3.4.1 General

The <height_limit> element specifies the limited height of the components from the surface of the top layer or bottom layer.

```
<height_limit>
             [<top> element]…
             [<bottom> element]…
             [<extensions> element]…
</height_limit>
```

The <height_limit> element consists of zero or more <top>, <bottom>, and <extensions> elements. Figure 71 shows the height limit of components from the surface of the top layer or bottom layer.

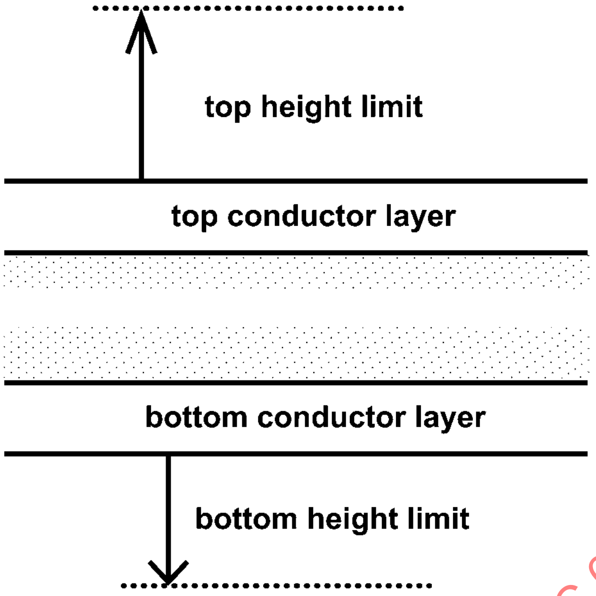

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Figure 71—Explanatory drawing of the top height limit and bottom height limit

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9.3.4.2 Element content

The <height_limit> element can contain the following elements:

```
<top>
<bottom>
<extensions>
```

9.3.4.3 Example

The following is an example of the <height_limit> element in use.

```
<height_limit>
   <top
       name="Top_Connector_Location"
       height="200"
       shape_id="Rec_6000um_8000um"
       x="3000" y="2000"
   />
   <bottom
       name="Bottom_Connector_Location"
       height="200"
       shape_id="Rec_6000um_8000um"
       x="3000" y="2000"
   />
</height_limit>
```

9.3.4.4 The <top> element

9.3.4.4.1 General

The <top> element specifies the maximum height for the placed components on the top layer.

```
<top
             name="area_name"
             height="height_limitation"
             shape_id="identifier_of_referenced_shape"
             x="x_coordinate"
             y="y_coordinate"
             [angle="rotation_angle"]
/>
```

The <top> element consists of the name attribute, the height attribute, the shape_id attribute, the x attribute, the y attribute, and the optional angle attribute.

9.3.4.4.2 Attribute definitions

The attributes of the <top> element are defined as follows.

name

This attribute specifies the name of the area that has a limited height on the top layer.

height

This attribute specifies the maximum height for the top layer. The unit of the height is defined by the <distance> element in the <unit> element.

shape_id

This attribute specifies the identification number of the shape that has the specified height-restricted space on the top layer. The origin coordinate of the shape coincides with the origin coordinate of the height-restricted space.

x

This attribute specifies the x-coordinate of origin in the height-restricted area. The unit of the coordinate is defined by the <distance> element in the <unit> element.

y

This attribute specifies the y-coordinate of origin in the height-restricted area. The unit of the coordinate is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default. The unit of the angle is defined by the <distance> element in the <unit> element.

9.3.4.4.3 Example

The following is an example of the <top> element in use.

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```
<top
   name="Top_Connector_Location"
   height="200"
   shape_id="Rec_6000um_8000um"
   x="3000" y="2000"
/>
```

9.3.4.5 The <bottom> element

9.3.4.5.1 General

The `<bottom>` element specifies the maximum height for the placed components on the bottom layer.

```
<bottom
             name="area_name"
             height="height_limitation"
             shape_id="identifier_of_referenced_shape"
             x="x_coordinate"
             y="y_coordinate"
             [angle="rotation_angle"]
/>
```

The `<bottom>` element consists of the `name` attribute, the `height` attribute, the `shape_id` attribute, the `x` attribute, the `y` attribute, and the optional `angle` attribute.

9.3.4.5.2 Attribute definitions

The attributes of the `<bottom>` element are defined as follows.

`name`

> This attribute specifies the name of the area that has a limited height on the bottom layer.

`height`

> This attribute specifies the maximum height for the bottom layer. The unit of the height is defined by the `<distance>` element in the `<unit>` element.

`shape_id`

> This attribute specifies the identification number of the shape that has the specified height-restricted space on the bottom layer. The origin coordinate of the shape coincides with the origin coordinate of the height-restricted space.

`x`

> This attribute specifies the x-coordinate of origin in the height-restricted area. The unit of the coordinate is defined by the `<distance>` element in the `<unit>` element.

`y`

> This attribute specifies the y-coordinate of origin in the height-restricted area. The unit of the coordinate is defined by the `<distance>` element in the `<unit>` element.

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`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default. The unit of the angle is defined by the `<angle>` element in the `<unit>` element.

9.3.4.5.3 Example

The following is an example of the `<bottom>` element in use.

```
<bottom
    name="Bottom_Connector_Location"
    height="200"
    shape_id="Rec_6000um_8000um"
    x="3000" y="2000"
/>
```

9.3.5 The <blockage> element

9.3.5.1 General

The `<blockage>` element specifies the inhibition areas of component mounting and/or conductive object layout.

```
<blockage>
             [<placement> element]…
             [<routing> element}…
             [<extensions> element]…
</blockage>
```

The `<blockage>` element consists of zero or more `<placement>`, `<routing>`, and `<extensions>` elements.

9.3.5.2 Element contents

The `<blockage>` element can contain the following elements:

```
<placement>
<routing>
<extensions>
```

9.3.5.3 Example

The following is an example of the `<blockage>` element in use.

```
<blockage>
    <placement
        ref_layer="L1"
        shape_id="kout_top_200um_200um"
        x="100"
        y="100"
    />
    <routing
        ref_layer="L1"
```

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```
        shape_id="kout_top_200um_200um"
        x="100"
        y="100"
    />
    <routing
        ref_layer="L4"
        shape_id="kout_bottom_400um_400um"
        x="0"
        y="0"
    />
</blockage>
```

9.3.5.4 The <placement> element

9.3.5.4.1 General

The <placement> element specifies the layer and the shape for the inhibition of the component mounting.

```
<placement
              ref_layer="name_of_referenced_layer"
              [attach="layer_side"]
              shape_id="identifier_of_referenced_shape"
              x="x_coordinate"
              y="y_coordinate"
              [angle="rotation_angle"]
/>
```

The <placement> element consists of the ref_layer attribute, the shape_id attribute, the x attribute, the y attribute, and the optional angle attribute.

9.3.5.4.2 Attribute definitions

The attributes of the <placement> element are defined as follows.

ref_layer

> This attribute specifies the name of the conductor layer that is specified in the <layer_def> element.

attach

> This attribute specifies the side of the layer to construct the placement blockage, by either keyword ABOVE or BELOW. If ABOVE is specified, the blockage is constructed above the specified layer. If BELOW is specified, the blockage is constructed below the specified layer.

shape_id

> This attribute specifies the identifier of the predefined shape that is defined at the <shape> element. The referenced shape shall be defined at the <shape> element in the same file.

x

> This attribute specifies the x-coordinate of origin. The unit of the coordinate is defined by the <distance> element in the <unit> element.

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y

This attribute specifies the y-coordinate of origin. The unit of the coordinate is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default. The unit of the angle is defined by the <angle> element in the <unit> element.

9.3.5.4.3 Example

The following is an example of the <placement> element in use.

```
<placement
        ref_layer="L1"
        shape_id="kout_top_200um_200um"
        x="100"
        y="100"
/>
```

9.3.5.5 The <routing> element

9.3.5.5.1 General

The <routing> element specifies the layer and the shape for the inhibition of the layout of conductive objects, such as trace, via, and plane.

```
<routing
                ref_layer="name_of_referenced_layer"
                shape_id="identifier_of_referenced_shape"
                x="x_coordinate"
                y="y_coordinate"
                [angle="rotation_angle"]
/>
```

The <routing> element consists of the ref_layer attribute, the shape_id attribute, the x attribute, the y attribute, and the optional angle attribute.

9.3.5.5.2 Attribute definitions

The attributes of the <routing> element are defined as follows.

ref_layer

This attribute specifies the name of the conductor layer that is specified in the <layer_def> element.

shape_id

This attribute specifies the identifier of the predefined shape that is defined at the <shape> element. The referenced shape shall be defined at the <shape> element in the same file.

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x

This attribute specifies the x-coordinate of origin. The unit of the coordinate is defined by the <distance> element in the <unit> element.

y

This attribute specifies the y-coordinate of origin. The unit of the coordinate is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default. The unit of the angle is defined by the <angle> element in the <unit> element.

9.3.5.5.3 Example

The following is an example of the <routing> element in use.

```
<routing
        ref_layer="L1"
        shape_id="kout_top_200um_200um"
        x="100"
        y="100"
/>
```

9.3.6 The <design_rule_area> element

9.3.6.1 General

The <design_rule_area> specifies the particular area that has the non-default design rules.

```
<design_rule_area
             ref_rule_name="name_of_referenced_design_rule"
             shape_id="identifier_of_referenced_shape"
             x="x_coordinate"
             y="y_coordinate"
             [angle="rotation_angle"]
             [priority="priority"]
>
             [<extensions> element]…
</design_rule_area>
```

The default design rules in this area are overridden by the non-default design rules. It is possible to specify the different rules from the default design rules in <design_rule_area>, but it is impossible to specify the layer stackup locally. Even if the local design rule includes the statement that defines the layer structure, the definition will be ignored. The <design_rule_area> element consists of the ref_rule_name attribute, the shape_id attribute, the x attribute, the y attribute, the optional angle attribute, and the optional priority attribute. Figure 72 shows the relationship between the default design rule area and the non-default design rule area.

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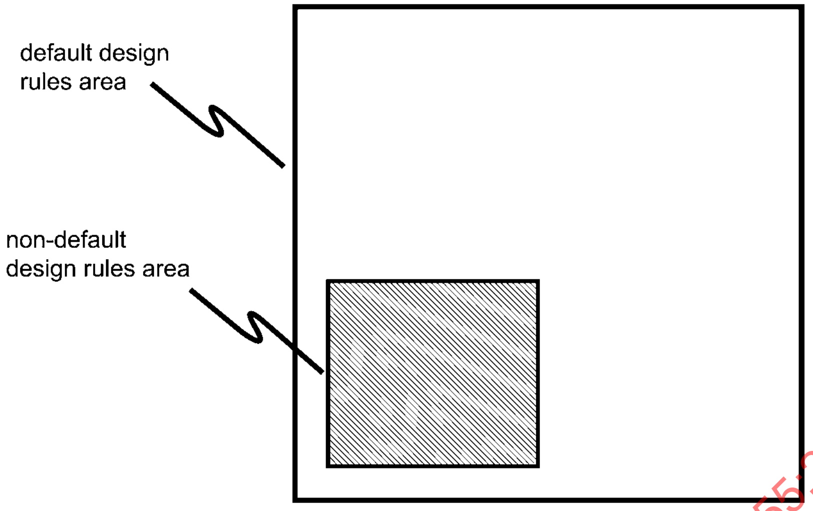

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Figure 72—Explanatory drawing of the relationship of the default design rule area and the non-default design rule area

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9.3.6.2 Attribute definitions

The attributes of the `<design_rule_area>` element are defined as follows.

`ref_rule_name`

> This attribute specifies the name of the predefined physical design rule that is used in the non-default design rule area. The physical design rule is specified in the `<Physicaldesign>` element.

`shape_id`

> This attribute specifies the identification number of the shape that is specified in the non-default design rule area. The origin coordinate of the shape coincides with the origin coordinate of the area.

`x`

> This attribute specifies the x-coordinate of origin. The unit of the coordinate is defined by the `<distance>` element in the `<unit>` element.

`y`

> This attribute specifies the y-coordinate of origin. The unit of the coordinate is defined by the `<distance>` element in the `<unit>` element.

`angle`

> This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default. The unit of the angle is defined by the `<angle>` element in the `<unit>` element.

`priority`

This attribute specifies the priority of the physical design rule that is specified by the `<deisgn_rule_area>` element. The bigger number means higher priority and the priority number of the default physical design area is zero. If it is not specified, one is set as the default.

9.3.6.3 Element content

The `<design_rule_area>` element can contain the following element:

`<extensions>`

9.3.6.4 Example

The following is an example of the `<design_rule_area>` element in use.

```
<design_rule_area
    ref_rule_name="C4_Area"
    shape_id="SQ_6000um_6000um"
    x="0" y="0"
    priority="10"
/>
```

10. N-Format

10.1 Purpose of the N-Format file

The N-Format file includes not only the signal connection but also the power/ground network. The N-Format file conforms to Verilog-HDL (IEEE Std 1364).

10.2 How to identify the power/ground network

Add the `/* PG_NET */`, `/* PG_NET=`*`group_name`*` */`, `/* PWR=`*`group_name`*` */`, and `/* GND=`*`group_name`*` */` keywords at the definition of ports as follows:

a) The port direction for power/ground is `inout`.

b) The net attribute of the power/ground is `wire`, not `supply0` or `supply1`.

c) Add the `PG_NET` or `PG_NET=`*`group_name`* keyword at the power/ground port as comment, where *`group_name`* is the name of power/ground net.

d) Add `PWR=`*`group_name`* and `GND=`*`group_name`* keyword at the signal port as comment to specify the related power domain, where *`group_name`* is the name of power/ground net.

e) *`group_name`* is case sensitive.

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10.3 Example

The following is an example of the N-Format in use.

```
module XXXX (A, B, C, D, AVDD1, AVDD2, AVSS, DVDD, DVSS)
       input A; /* PWR=analog_vdd_1.8 GND=analog_gnd */
       output B; /* PWR=analog_vdd_1.8 GND=analog_gnd */
       input C; /* PWR=digital_1.2 GND=digital_gnd */
       output D; /* PWR=digital_1.2 GND=digital_gnd */
       inout AVDD1; /* PG_NET=analog_vdd_1.8 */
       inout AVDD2; /* PG_NET=analog_vdd_1.8 */
       inout AVSS; /* PG_NET=analog_gnd" */
       inout DVDD ; /* PG_NET=digital_1.2 */
       inout DVSS ; /* PG_NET=digital_vss */
```

11. G-Format

11.1 Language basics of G-Format

11.1.1 Typographic and syntax conventions

This subclause describes the conventions used in the syntax definitions of the LPB G-Format.

`text`

> The `monospace` and **bold** font is used to indicate the attributes or elements that shall be typed literally.

italic

> The *italic* font is used to indicate the user-defined information for which shall be substituted a name or value.

|

> Vertical bars separate possible choices for a single attribute or element. They take precedence over any other character.

[ ]

> Brackets denote optional attributes or elements. When used with vertical bars, they enclose a list of choices.

…

> Three dots indicate that the previous value could be repeated.

Note that all of the strings in G-Format are treated as case sensitive.

NOTE—All code examples in this standard are written in monospace font.

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11.1.2 Reserved characters

#	If the first character of a line is a pound (#) sign, the line is ignored so it can be used for comments.
" "	Any data between two double quotation marks are considered as a string.

11.2 Structure

The G-Format file consists of several sections. Each section starts with a dot (`.`) followed by a keyword. The **`.version`**, **`.unit`**, and **`.scale`** sections consist of one line each. All other sections end with **`.end`** followed by the same keyword. The keyword in the **`.end`** line can be omitted. The header section consists of the **`.version`**, **`.unit`**, and **`.scale`** sections. Except for the **`.version`** section, any section can be omitted. The sections of the G-Format file are as follows:

```
.version x y z

.unit [inch | mm]

.scale value

.material
definition
.end [material]

.layer
definition
.end [layer]

.shape
definition
.end  [shape]

.board_geom
definition
.end [board_geom]

.padstack
definition
.end [padstack]

.part
definition
.end [part]

.component
definition
.end [component]

.netattr
definition
.end [netattr]

.netlist
```

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definition
.end [**netlist**]

.via
definition
.end [**via**]

.bondwire
definition
.end [**bondwire**]

.route
definition
.end [**route**]

11.3 Header section

11.3.1 General

The header section consists of the **.version**, **.unit**, and **.scale** sections.

. version *x y z*

This section specifies a version of the G-Format file; *x* is a major version number; *y* is a minor version number, *z* expresses the version of this standard. The *z* corresponds to the version number of C/R/M Format. The **.version** section shall appear before any other section in the file.

x	integer
y	integer
z	2020

.unit *value*

This section specifies a geometric unit used throughout the G-Format file. The value shall be either **inch** or **mm**. If this section or the value is omitted, **inch** is assumed as the default.

value	**inch** or **mm**

.scale *value*

This section specifies a geometric scale used throughout the G-Format file. The actual dimension of the data in the file is determined by dividing the number by the scale value. For example, if the unit is set to **inch** and the scale is 1000, the geometric data are in mils or 1/1000 in. If the unit is set to **mm** and the scale is 1000, the geometric data are in microns or micrometers. The default is **1**.

value	iteger

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11.3.2 Example

The following is an example of the header section of a G-Format file.

```
.version 1 1 2020
.unit mm
.scale 1000
```

11.4 Material section

11.4.1 General

The **.material** section consists of the following:

.material
definition
.end [**material**]

This is an optional section giving material properties. List materials used in the design and their properties. Each material is defined as follows:

C *materialName conductivity*
or
D *materialName permittivity permeability lossTangent*
where
C or **D** — **C** stands for conducting material.
D stands for dielectric material.
materialName Is the name of the material enclosed by double quotation marks.
conductivity Is the electric conductivity (1/Ω mm).
permittivity Is the relative permittivity or dielectric constant.
permeability Is the relative permeability.
lossTangent Is the dielectric loss tangent.

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11.4.2 Example

The following is an example of a **.material** section.

```
.material
D "AIR" 1.0 1.0 0.0
C "COPPER" 59000
C "GOLD"45500
D "FR-4" 4.5 1.0 0.035
D "SR" 4.3 1.0 0.03
.end material
```

11.5 Layer section

The **.layer** section consists of the following:

.layer
definition
.end [**layer**]

This section describes a layer stackup from top to bottom (or from front to back). Each layer is defined as follows:

name thickness type conducting dielectric1 [*dielectric2 dielectric3*]

where

name Is the name of the layer enclosed by double quotation marks. If unknown, write `""`.

thickness Is the thickness of the layer. If unknown, write **`0`**.

type Is the type of the layer, defined by a single character:

- **`S`** stands for signal layer.
- **`D`** stands for dielectric layer.
- **`P`** stands for power or ground layer if it can be differentiated from the signal layer.

conducting Is the name of the conducting material entered as a string enclosed by double quotation marks.

dielectric1 Is the name of the dielectric material entered as a string enclosed by double quotation marks.

Note that throughout the G-Format file, signal layer numbers are the numbers that are numbered sequentially from the top by counting only the signal/power/ground layers.

11.6 Shape section

11.6.1 General

The **`.shape`** section consists of the following:

`.shape`
definition
`.end` [**`shape`**]

This section defines shapes that are referenced from other sections in the same file. Available shapes are polygon, rectangle, square, circle, annular, oblong, finger, bullet, and composite.

Each shape is defined as:

id keyword parameters

where the *id* is a number that will be referenced by others and is sequentially numbered from 1. The *keyword* and *parameters* are described as follows.

id **`polygon {`** *x1 y1 x2 y2 …* **`}`**

Vertices of polygon shape (see Figure 73) are enclosed by **`{ }`**. Data can be shown on more than one line. The last point does not need to be the same as the first point. The reference point is at (0, 0).

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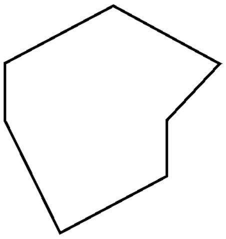

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Figure 73—polygon

id **`rectangle`** *width height*

Each rectangle is defined by *width* and *length*. The definition shall appear on one line. The reference point is at the center of the rectangle. Figure 74 marks the reference point as X.

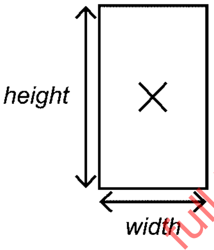

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Figure 74—rectangle

id **`square`** *width*

Each square is defined by *width*. The definition shall appear on one line. The reference point is at the center of the square. Figure 75 marks the reference point as X.

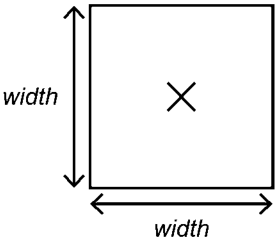

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Figure 75—square

id **`circle`** *diameter*

Each circle is defined by *diameter*. The definition shall appear on one line. The reference point is at the center of the circle. Figure 76 marks the reference point as X.

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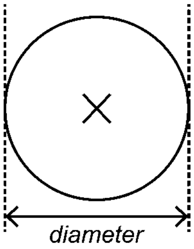

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Figure 76—circle

id **`annular`** *outerDiam innerDiam*

Each annular (or *donut*) is defined by *outerDiam* and *innerDiam*. The definition shall appear on one line. The reference point is at the center of the annular. Figure 77 marks the reference point as X.

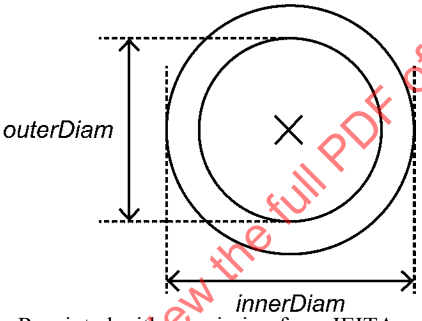

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Figure 77—annular

id **`oblong`** *width left right*

Each oblong is defined by *width*, *left*, and *right*. The definition shall appear on one line. The reference point is shown in Figure 78 marked as X.

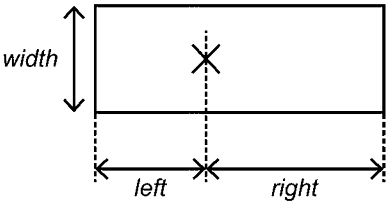

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Figure 78—oblong

id **`bullet`** *width left right*

Each bullet is defined by *width, left*, and *right*. The definition shall appear on one line. The reference point is shown in Figure 79 marked as X.

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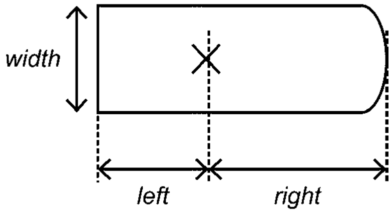

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Figure 79—bullet

id **finger** *width left righ*t

Each finger is defined by *width*, *left*, and *right*. The definition shall appear on one line. The reference point is shown in Figure 80 marked as X.

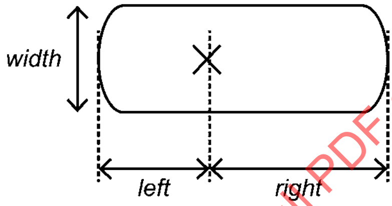

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Figure 80—finger

id **composite {** *1st_point_segment1 segment2 …* **}**

A composite shape consists of lines and/or arcs. The definition is enclosed by **{ }** and can be shown on more than one line. There are four types of segments: straight line, clockwise arc (**arc**), counterclockwise arc (**rarc** or reverse arc), and an arc defined by three points (**arc3**).

No keyword between two points indicates that they are connected by a straight line. A keyword **arc, rarc**, or **arc3** between two points indicates that they are connected by a clockwise arc, a counterclockwise arc, or a three-point method arc, respectively. For **arc** and **rarc**, an arc origin appears after the arc end point. For **arc3**, a middle point appears after the arc end point.

The composite shape shown in Figure 81 can be described as

> *2* **composite {***xa ya xb yb xc yc* **rarc** *xd yd xp yp xe ye xf yf* **arc** *xg yg xq yq xh yh* **arc3** *xi yi xr yr***}**

where the *2* at the beginning is a shape identifier. The shape is made of straight lines *a-b* and *b-c*, then a counterclockwise arc from *c* to *d* with an origin at *p*, then straight lines *d-e* and *e-f*, then a clockwise arc from *f* to *g* with an origin at *q*, then straight line *g-h* and a three-point method arc from *h* to *i* with a middle point at *r*. Finally, the straight line from *i* to *a* is not defined because a straight line will connect the last point to the first point by default.

The same shape can also be described as:

> *2* **composite {***xa ya xi yi* **arc3** *xh yh xr yr xg yg* **rarc** *xf yf xq yq xe ye xd yd* **arc** *xc yc xp yp xb yb***}**

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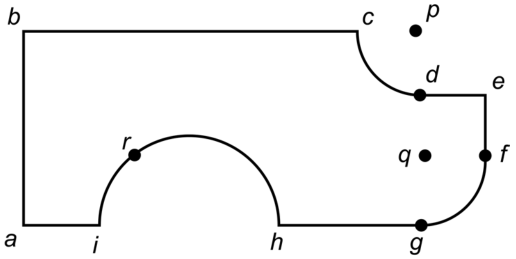

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Figure 81 —composite

11.6.2 Example

The following is an example of a **.shape** section.

```
.shape
1 circle 50
2 circle 80
3 circle 300
4 rectangle 400 400
5 rectangle 700 5600
6 circle 750
7 composite {
           275 -200
           275 200
           -275 200
           -275 -200
}
8 composite {
           400 -100
           400 100
           -400 100
           -400 -100
}
.end shape
```

11.7 Board geometry section

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11.7.1 General

The **.board_geom** section consists of the following:

.board_geom
definition
.end [**board_geom**]

The exterior geometry of a board or package is defined by one of the following four methods:

polygon { *x1 y1 x2 y2 …* **}**
composite { *1st_point_segment1 segment2 …* **}**
shape *shapeID x y rotation mirror*
shape *shapeID x y mirror rotation*

The methods for defining **polygon** and **composite** are the same as those described in the .shape section (11.6).

The **shape** is placed by defining the *shapeID*, the x/y coordinates (global coordinates) of the shape origin (local origin), the counterclockwise rotation in degrees, and the mirror indicator. Mirror indicators are as follows:

X	Mirror about X axis
Y	Mirror about Y axis
N	No mirror

If the mirror indicator appears after the rotation, the mirror is performed after the rotation. If the mirror indicator appears before the rotation, the mirror is performed before the rotation.

Both mirror and rotation operations are performed with respect to the shape origin (local origin).

Holes (cutouts or voids) are defined by using one or more of the following methods.

void_polygon { *x1 y1 x2 y2 …* **}**
void_rectangle *width length x y*
void_square *width x y*
void_circle *diameter x y*
void_composite { *1st_point_segment1 segment2 …* **}**
void_shape *shapeID x y rotation mirror*
void_shape *shapeID x y mirror rotation*

The **void_polygon**, **void_composite**, and **void_shape** are defined in the same way as for the **polygon**, **composite**, and **shape**, respectively.

The **void_rectangle**, **void_square**, and **void_circle** are defined in the same way as the **rectangle**, **square**, and **circle** are defined in the **.shape** section (11.6). They are placed at the coordinates *x* and *y*.

11.7.2 Example

The following is an example of a **.board_geom** section.

```
.board_geom
polygon {
           -50000 -40000
           50000 -40000
           50000 40000
           -50000 40000
}
.end board_geom
```

11.8 Padstack section

11.8.1 General

The **.padstack** section consists of the following:

.padstack
definition
.end [**padstack**]

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This section defines padstacks. Each padstack is defined as

padstackID **{** *pad1 pad2* … **}**

where the *padstackID* is a number that will be referenced by vias in the **.via** section (11.13). The section is sequentially numbered from 1. As described below, pads are defined only by using the predefined shapes in the **.shape** section:

signalLayerNum shapeID shapeROT [*apshapeID apshapeROT*]

where
signalLayerNum Is the signal layer number as it appeared in the layer section.
shapeID Is the shape identifier.
shapeROT Is the counterclockwise rotation angle of the shape in degrees.
apshapeID The anti-pad shape identifier. The anti-pad definition is optional.
apshapeROT Is the counterclockwise rotation angle of the anti-shape in degrees.

11.8.2 Example

The following is an example of a **.padstack** section.

```
.padstack
1 {
           1 3 0 4 0
           2 3 0 4 0
           3 3 0 4 0
           4 3 0 4 0
}
2 {
           1 3 0 4 0
           2 3 0 4 0
}
3 {
           2 3 0 4 0
           3 3 0 4 0
           4 3 0 4 0
}
4 {
           1 12 0
}
5 {
           1 13 0
}
6 {
           1 14 0
}
.end padstack
```

11.9 Part section

11.9.1 General

The **.part** section consists of the following:

.part
definition
.end [**part**]

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This section describes a part. Each part is defined as

partName [*shape llx lly urx ury height* [*type value* [**noflip**] [*material*]]] **{***pin1 pin2* …**}**

where *partName* is the name of the part and *shape*, *llx*, *lly*, *urx*, *ury*, *height,* and **noflip** are optional. If the keyword **noflip** appears, the part will not be flipped when it is placed below the layer.

partName Is the name of the part.
shape Is the top view shape of the part:
R stands for rectangle.
C stands for circle.
D stands for round-corner diamond.
llx, *lly* Are the lower left coordinates of the bounding box.
urx, *ury* Are the upper right coordinates of the bounding box.
height Is the height.
type Is the part type:
R stands for resistor.
L stands for inductor.
C stands for capacitor.
S stands for solder balls.
D stands for die.
M stands for molding compound.
O stands for other types.
value Is the part value (mΩ for a resister, nH for an inductor, pF for a capacitor). Set it to zero for all other part types. If the three values are in parentheses **( )**, the part values are for a resistor, inductor, and capacitor; for example, (20.0 5 3.5).
material Is optional. The name of the material is enclosed by **" "**.

Pins are defined as

pinName x y ioType [*padstackID*]

where

pinName Is the name of the pin. If the name is not known, a sequential number will be used as a name.
x y Is the location of the pin with respect to local origin.
ioType Is the pin I/O type:
D stands for driver pin.
R stands for receiver pin.
B stands for bidirectional pin.
DT stands for driver terminator.
RT stands for receiver terminator.
padstackID Is optional. It is the padstack identifier (0 if the padstack is unknown).

11.9.2 Example

The following is an example of a **.part** section.

```
CAP0603B R -300 -150 300 150 400 C {
           1 -425 0 B 23
           2 425 0 B 23
}
CAP1005B R -650 -250 650 250 400 C {
```

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```
           1 -500 0 B 24
           2 500 0 B 24
}
REGULATOR R -2000 -2000 2000 2000 0 D {
           1 -1800 1050 B 21
           10 1800 -350 B 21
           11 1800 350 B 21
           12 1800 1050 B 21
           13 1050 1800 B 21
           14 350 1800 B 21
           15 -350 1800 B 21
           16 -1050 1800 B 21
           2 -1800 350 B 21
           3 -1800 -350 B 21
           4 -1800 -1050 B 21
           5 -1050 -1800 B 21
           6 -350 -1800 B 21
           7 350 -1800 B 21
           8 1050 -1800 B 21
           9 1800 -1050 B 21
}
SMA_X1 R -2750 -2750 2750 2750 0 O {
           1 0 0 B 18
           2 -2000 2000 B 18
           3 -2000 -2000 B 18
           4 2000 -2000 B 18
           5 2000 2000 B 18
}
.end part
```

11.10 Component section

11.10.1 General

The **`.component`** section consists of the following:

`.component`
definition
`.end` [**`component`**]

This section describes a component placement. One component placement appears per line. Each placed component is defined as:

U-name partName x y z layer rotation [*stackComp*] [(*R L C 0*)]

where

U-name Is the U-name, also known as the location identifier or reference designator. No space is allowed in the name.

partName Is the part name. The name is enclosed by double quotation marks (`" "`).

x y Is the location of the component origin with respect to the board origin.

z If *z* and *layer* are given, then *z* represents the distance from the layer of the board in the direction specified by +n or −n. This would allow for embedded devices on the main board.
If *z* and *stackComp* are given, then *z* represents the distance from the uppermost layer of the “stack comp” if *z* is positive; or the distance from the lowest layer of the “stack comp” if *z* is negative.

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layer Is the placement layer number:
+n stands for above the layer.
−n stands for below the layer.

rotation Is the counterclockwise rotation of the component in degrees with respect to the component origin (local origin).

stackComp Is optional. It is the name of the component on which this component is stacked. If this is defined, the layer number is ignored.

R L C 0 Is optional. It is the component's R, L, C, and other values in a pair of parentheses; for example, (50 10 250 0). The units are mΩ, nH, or pF. The fourth value is for future use.

11.10.2 Example

The following is an example of a **`.component`** section.

```
.component
C10 CAP0603B -8584.7 -4104.9 -4 0
C11 CAP0603B -8584.7 -6355.9 -4 0
REGULATOR REGULATOR -12598 10183.9 1 0
SMA_X1 SMA_X1 1570.7 32293.2 1 0
SMA_X2 SMA_X1 -7429.3 32293.2 1 0
.end component
```

11.11 Net attribute section

The **`.netattr`** section consists of the following:

`.netattr`
definition
`.end` [**`netattr`**]

This section defines net attributes, such as net class, allowable delays, and other user properties.

Each attribute group is defined as

id **{***attrributeName1***=***value1 attributeName2***=***value2 …***}**

where the *id* is an attribute group number that will be referenced by nets in the netlist section and is sequentially numbered from 1. More than one attribute can be defined for one group. Each attribute group definition can appear on more than one line. Attribute assignments appear in the braces **{ }**. Each attribute assignment consists of *attributeName*, an equals sign (**=**), and the *value*.

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11.12 Netlist section

11.12.1 General

The **`.netlist`** section consists of the following:

`.netlist`
definition
`.end` [**`netlist`**]

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This section defines netlists. Each net is defined as

netName netType attributeID {*node1 node2* …}

where

netName Is the net name.
netType Is the net type:
S stands for signal net (**s** if broken).
P stands for power net (**p** if broken).
G stands for ground net (**g** if broken).
attributeID Is the net attribute identifier. Zero indicates that the attribute is unknown.

Each node is defined as

U-name pinNumber ioType [**{***x y layer***}**]

where

U-name Is the U-name. A minus sign (−) indicates an unknown U-name.
pinNumber Is the pin number or pin name.
ioType Is the pin I/O type:
D stands for driver pin.
R stands for receiver pin.
B stands for bidirectional pin.
DT stands for driver terminator.
RT stands for receiver terminator.
A placeholder minus sign (−) shall appear if the type defined for the pin in the part section is to be used.
x y Is the location of the pin origin with respect to the board origin.
layer Is the placement layer number.

The pin location can appear at the end of the node definition. It is optional and shall be enclosed by **{ }**. Set the layer number to negative for solder balls.

11.12.2 Example

The following is an example of a **.netlist** section.

```
.netlist
"FKOUT[2]" S 0 {
           FKB48 M1 B
           SMA_X4 1 B
}
"N1" S 0 {
           XTAL 3 B
           MCR1_R7 B B
           MCR1_R8 B B
           GRM1_C2 A B
}
"PCIREFCLK_N" S 0 {
           SOC AE12 B
           PCIE A14 B
}
"PCIREFCLK_P" S 0 {
           SOC AF12 B
```

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```
           PCIE A13 B
}
"PCITR0_N" S 0 {
           SOC AE14 B
           PCIE A17 B
}
.end netlist
```

11.13 Via section

11.13.1 General

The **.via** section consists of the following:

.via
definition
.end [**via**]

This section defines vias. One via definition appears per line. Each via is defined as

viaName padstackID padstackROT shapeID shapeROT [*thickness*]

where

viaName Is the via name that will be referenced by routing in the route section.
padstackID Is the padstack identifier. Zero indicates that no padstack exists for the via.
padstackROT Is the counterclockwise rotation angle of the padstack.
shapeID Is the shape identifier of the via barrel.
shapeROT Is the counterclockwise rotation angle of the via barrel shape.
thickness Is optional. It is the thickness of the via barrel wall. If the thickness is 0, the via barrel is filled by material (see Figure 82).

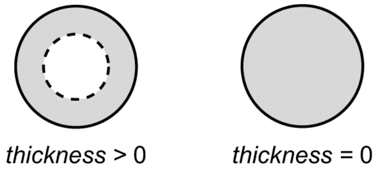

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Figure 82—via

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11.13.2 Example

The following is an example of a **.via** section.

```
.via
VIA14 1 0 2 0
VIA12 2 0 2 0
VIA24 3 0 2 0
VIA13 4 0 2 0
VIA14B 18 0 17 0
.end via
```

11.14 Bondwire section

11.14.1 General

The `.bondwire` section consists of the following:

```
.bondwire
definition
.end [bondwire]
```

This section defines bond wire geometry. One bond wire definition appears per line. Each bond wire is defined as

id type material diameter hw hd alpha beta [*profile_name*]

where the *id* is a number that will be referenced by routing in the route section and is sequentially numbered from 1. As illustrated in Figure 83 and Figure 84,

type Is the bond wire type:
D stands for die-down configuration.
U stands for die-up configuration.

material Is the material name or electric conductivity (1/Ω mm). If it is a name, it shall be enclosed by double quotation marks (" ").

diameter Is the wire diameter.

hw Is the wire loop height.

hd Is the die height:
$H_{die\_pad} - H_{top\_of\_top\_metal\_layer}$ for die-up.
$H_{die\_pad} - H_{bottom\_of\_bottom\_metal\_layer}$ for die-down.

alpha Is the die side angle in degrees.

beta Is the package substrate side angle in degrees.

profile_name Is the name of the bond wire profile associated with the *id*.

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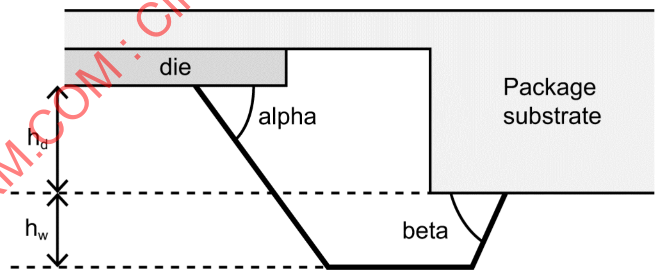

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Figure 83—Die-down configuration

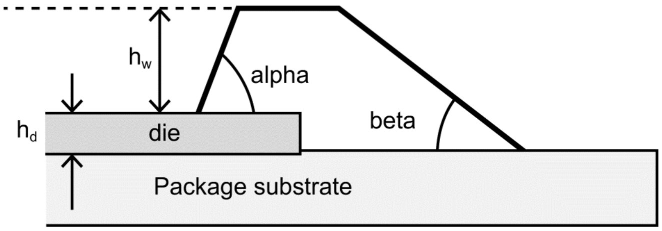

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Figure 84—Die-up configuration

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11.14.2 Example

The following is an example of a **.bondwire** section.

```
.bondwire
1 U "GOLD" 20 70 290 60 20 innerwire
2 U "GOLD" 20 140 290 60 40 outerwire
.end bondwire
```

11.15 Route section

11.15.1 General

The **.route** section consists of the following:

.route
definition
.end [**route**]

This section defines routed nets. Each routed net is defined as

netName **{** *segment1 segment2* …**}**

where *netName* is one of the nets that appeared in the **.netlist** section. Each routed net consists of one or more segments. Each segment is defined by one of the following methods. All of these methods are in the form of

segment_type signal_layer_number(s) segment_definition
path *layer width* **{** *1st_point_segment1 segment2 …* **}**
via *beginLayer endLayer viaName x y rotation [mirror]*
bondwire *beginLyr endLyr bondwireID xb yb xe ye [die1 die2]*
polygon *layer* **{** *x1 y1 x2 y2 …***}**
rectangle *layer width length x y*
square *layer width x y*
circle *layer diameter x y*
annular *layer outerDiem innerDiem x y*
composite *layer* **{** *1st_point_segment1 segment2 …* **}**
shape *layer shapeID x y rotation mirror*

shape *layer shapeID x y mirror rotation*
void_polygon *layer* **{** *x1 y1 x2 y2 …* **}**
void_rectangle *layer width length x y*
void_square *layer width x y*
void_circle *layer diameter x y*
void_composite *layer* **{** *1st_point_segment1 segment2 …* **}**
void_shape *layer shapeID x y rotation mirror*
void_shape *layer shapeID x y mirror rotation*

The **path** segment is defined the same way that the **composite** shape is defined in the **.shape** section, except that it has a *width* and the last point does not automatically connect to the first point.

The **via** segment requires *beginLayer* and *endLayer* numbers, while other segments require only one layer number. The via segment also requires the following:

viaName Name of the via defined in the via section.
x y Location of the via.
rotation Counterclockwise rotation angle of the pad stack in degrees.
mirror Optional; padstack mirror flag:
Y Mirror padstack.
N Do not mirror padstack.

The **bondwire** segment requires the following:

beginLyr Signal layer number of a beginning point; in order to indicate a die, enter a negative wire group identifier.
endLyr Signal layer number of an ending point; in order to indicate a die, enter a negative wire group identifier.
bondwireID Bond wire identifier (0 if unknown).
xb yb Beginning point coordinates.
xe ye Ending point coordinate.
die1 die2 Optional die component names; the name(s) appear here only if the *begin_lyr* and/or *end_lyr* are negative.

All other segment types are defined the same way as they are defined in the **.shape** section or in the **.board_geom** section.

11.15.2 Example

The following is an example of a **.route** section.

```
"AGND" {
          via 1 4 VIA14B -429.3 34293.2 0 N
          via 1 4 VIA14B -429.3 30293.2 0 N
          via 1 4 VIA14B -9429.3 34293.2 0 N
          shape 1 7 -24821.9 24278.3 0 N
          shape 1 12 -3779.3 23603.4 0 N
          composite 2 {
                       -47360 23040
                       -15983.4 23040
                       -15360 22416.6
                       -15360 18416.6
                       -14960 18016.6
                       -14960 13616.6
                       -14783.4 13440
```

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```
                       -4640 13440
                       -4640 22416.6
                       -4016.6 23040
                       6560 23040
                       6560 35360
                       -47360 35360
          }
          void_composite 2 {
                       -41295.6 25636.1
                       arc -40975.6 25636.1 -41135.6 25636.1
                       arc -41295.6 25636.1 -41135.6 25636.1
          }
          path 1 80 {
                       -7825.9 27607.5
                       -6985.3 27607.5
          }
          path 1 80 {
                       -4082.8 25942.8
                       -4082.8 25683
          }
          path 1 80 {
                       -3719.3 23633.2
                       -3380.3 23633.2
          }
          path 1 80 {
                       -7390.9 22442.4
                       -7130.9 22442.4
          }
}
"AVDD33" {
          shape 1 8 -12948 11983.9 90 N
          shape 1 7 -36821.9 23278.3 0 N
          shape 1 7 -34821.9 23278.3 0 N
          shape 1 7 -29821.9 24278.3 0 N
          composite 3 {
                       -42160 23040
                       -15183.4 23040
                       -14560 22416.6
                       -14560 15840
                       -12640 15840
                       -12640 24960
                       -38816.6 24960
                       -39040 25183.4
                       -39040 25760
                       -42160 25760
          }
          via 1 3 VIA13 -13451.3 16882.6 0 N
          via 1 3 VIA13 -36821.9 23278.3 0 N
          via 1 3 VIA13 -24821.9 23278.3 0 N
          shape 1 11 -13457.1 16897.2 270 N
          shape 1 11 -41161.1 25621.3 0 N
          via 1 4 VIA14 -41135.6 25636.1 0 N
}
"DDRAD[0]" {
          shape 1 9 10900 0 0 N
          shape 1 6 34806.5 -1623.2 0 N
          shape 1 6 34547.6 17511.7 0 N
          shape 1 14 26777.7 18269.6 0 N
          via 1 4 VIA14 34200 2360 0 N
          via 1 4 VIA14 34226.5 635 0 N
          via 1 4 VIA14 33967.6 19939 0 N
          path 1 80 {
                       33967.6 19939
```

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```
                        33967.6 19661.7
                        33967.6 19508.4
                        33977.6 19498.4
                        33977.6 18875.6
                        34057.6 18795.6
                        34057.6 18577.3
                        34137.6 18497.3
                        34137.6 18279.1
                        34187.6 18229.1
                        34187.6 18162.6
                        34547.6 17802.6
                        34547.6 17511.7
           }
           path 4 80 {
                        34200 2360
                        34200 2904
                        34170 2934
                        34170 11978
                        34157.6 11990.4
                        34157.6 12769.6
                        33967.6 12959.6
                        33967.6 19939
           }
           path 1 80 {
                        34226.5 635
                        34226.5 526.8
                        34226.5 373.5
                        34236.5 363.5
                        34236.5 -259.3
                        34316.5 -339.3
                        34316.5 -557.5
                        34396.5 -637.5
                        34396.5 -855.8
                        34446.5 -905.8
                        34446.5 -972.3
                        34806.5 -1332.3
                        34806.5 -1623.2
           }
           path 4 80 {
                        34200 2360
                        34200 841.5
                        34226.5 815
                        34226.5 635
           }
           path 1 80 {
                        34200 2360
                        33650.8 2360
                        33568.5 2442.3
                        16116 2442.3
                        14003.7 330
                        13900 330
                        13870 360
                        11750.9 360
                        11390.9 0
                        10900 0
           }
}
.end route
```

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Annex A

(informative)

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