IEC 63003

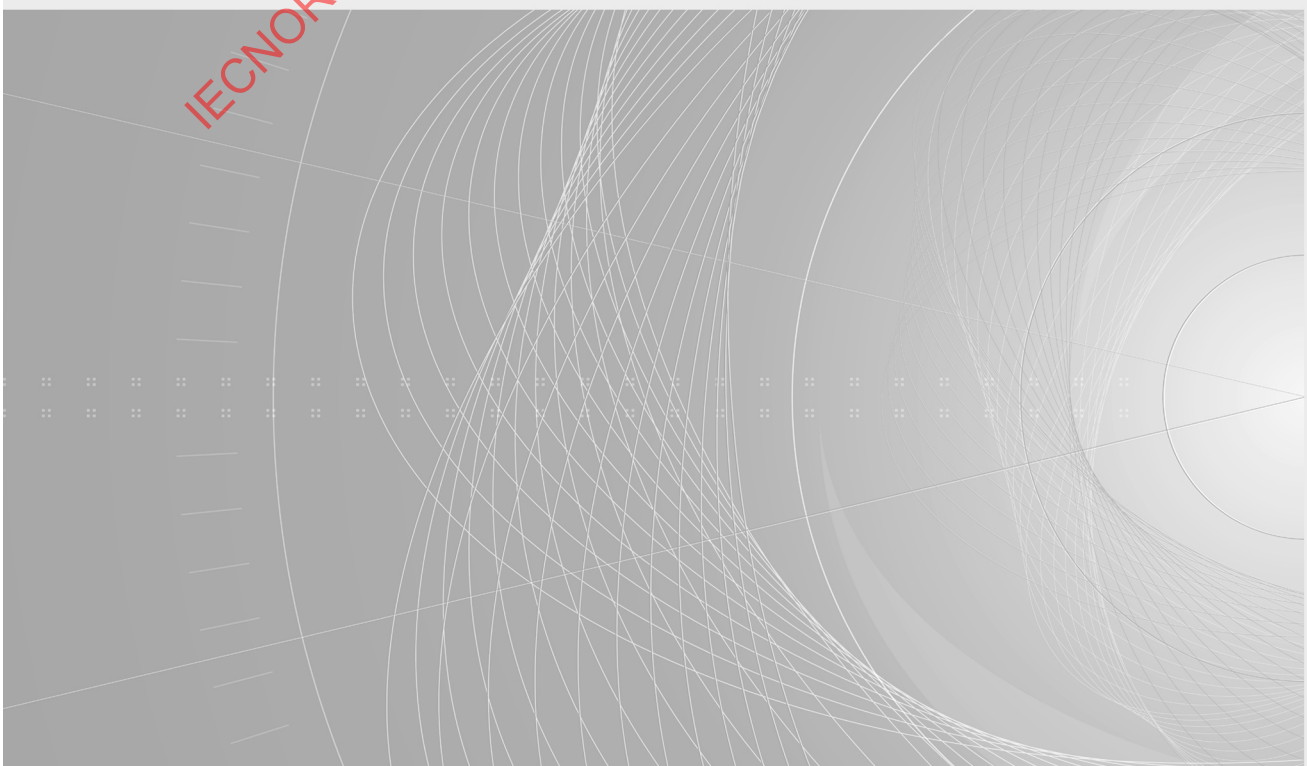
Edition 1.0 2015-12

INTERNATIONAL STANDARD

IEEE Std 1505.1™

colour inside

Standard for the common test interface pin map configuration for high-density, single-tier electronics test requirements utilizing IEEE Std 1505™



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Contents

STANDARD FOR THE COMMON TEST INTERFACE PIN MAP CONFIGURATION FOR HIGH-DENSITY, SINGLE-TIER ELECTRONICS TEST REQUIREMENTS UTILIZING IEEE Std 1505™

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
IEEE Std 1505.1-2008	91/1274/FDIS	91/1298/RVD

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- reconfirmed,
- withdrawn,
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- amended.

IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™

Sponsor

IEEE Instrumentation and Measurement Society

and

IEEE Standards Coordinating Committee 20 on Test and Diagnosis for Electronic Systems

Approved 26 September 2008

IEEE-SA Standards Board

Approved as a Full-Use Standard on 14 June 2013

IEEE-SA Standards Board

Abstract: This standard represents an extension to the IEEE 1505 receiver fixture interface (RFI) standard specification. Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: (a) pin map configuration; (b) specific connector modules; (c) respective contacts; (d) recommended switching implementation; and (e) legacy automatic test equipment (ATE) transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future automatic test systems (ATS).

Keywords: ATE, ATS, fixture, ICD, IEEE 1505.1™, interface, ITA, mass termination, receiver, scalable, TPS, UUT

IEEE Introduction

This introduction is not part of IEEE Std 1505.1-2008, IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™.

This standard stems from the history of ATE implementations having unique input/output (I/O) pin out definitions. This uniqueness has prevented the interoperability of test program sets (TPSs) among different ATEs within the same organizations. Even if the same RFI was used by the target ATE, the signals I/O could not be guaranteed to be at the same pin location. This is due to there being no suitable standard pin out definition for general purpose electronic testing applications.

IEEE Std 1505-2006[a] has addressed part of the interoperability problem by defining the common mechanical interface for the ATE. This project takes the TPS interoperability problem one step further toward completion by standardizing the electrical signal I/O pin map for general purpose electronic testing applications.

Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: (a) framework; (b) pin map configuration; (c) specific connector modules; (d) respective contacts; (e) recommended switching implementation; and (f) legacy ATE transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future ATS. The suggested mechanical and electrical requirements necessary to implement a specific IEEE 1505 RFI product in support of a common test interface (CTI) across all U.S. Department of Defense (DoD) defense agencies, related aerospace industry, and a variety of non-U.S. government agencies such as the U.K. Ministry of Defense (MoD) is provided.

The DoD is a major buyer and user of ATE; however, existing acquisition guidance desires the use of commercial standards and/or best practices for these systems. Suitable standards currently do not exist in the commercial marketplace; therefore, this standard will provide such specification.

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Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™

1. Overview

1.1 Scope

The scope of this standard is the definition of a pin map utilizing the IEEE 1505™ [1] receiver fixture interface (RFI). The pin map defined within this standard shall apply to military and aerospace automatic test equipment (ATE) testing applications.

[1] Information on references can be found in Clause 2.

1.2 Purpose

Standardization of a common input/output (I/O) will enable the interoperability of IEEE 1505 compliant interface fixtures [also known as *interface test adapters* (ITA), *interface devices* (IDs), or *interconnecting devices* (ICDs)] on multiple ATE systems utilizing the IEEE 1505 RFI.

1.3 Statement of the problem

1.3.1 U.S. Government guidance

From 1980 to 1992, the U.S. Department of Defense (DoD) investment in field, depot, and factory automatic test systems (ATS) exceeded $35 billion with an additional $15 billion for associated support. Most of this test capability was acquired as part of individual weapon system procurements. This led to a proliferation of different custom equipment types with unique interfaces. Recent policy decisions have changed the direction of the purchase of test equipment towards a standards based approach with both hardware and software critical interface requirements.

The U.S. DoD Instruction 5000.2-R1 ATS Policy states: "ATS capabilities shall be defined through critical hardware and software elements" (see [B2][2]). This policy however, did not define these critical elements. The Critical Interfaces Project was created to define critical ATS elements.

1.3.2 Critical Interfaces Project

The Factory-to-Field Integration of Defense Test Systems Project (commonly referred to as the *Critical Interfaces Project*) was started in the latter part of 1995. The Critical Interfaces Working Group (CIWG) within the Joint-Service ATS Research and Development Integrated Product Team (ARI) was established to perform the project. The ATS Executive Agent Office (EAO) has provided project management and coordination among the Air Force, Army, Marine Corps, and Navy participants. In addition, many industry representatives have participated. The CIWG published their findings in the Automatic Test System Critical Interfaces Report [B1] and this report served as the basis for the development of the RFI architecture and subsequent specification.

The objective of the Critical Interfaces Project was to demonstrate the feasibility of reducing the cost to re-host test program sets (TPSs) and increase the interoperability of TPS software among the military services by using standardized interfaces.

Interfaces that offer the potential to achieve this objective are deemed critical. Potential savings will be quantified through demonstration. The Automatic Test System Critical Interfaces Report [B1] is maintained by the ATS EAO and provides guidance to DoD ATE acquisition programs. This document also addressed the requirements of DoD Regulation 5000.2-R1 [B2] and assisted in migrating the DoD designated tester families towards a common solution. The Hardware Interfaces (HI) Subcommittee of the IEEE Standards Coordinating Committee on Test and Diagnosis for Electronic Systems (SCC20) applied the recommendations of the report as it related to the RFI, to the extent that the current RFI standard is in full compliance with the report.

1.3.3 CTIWG guidance recommendations

During the Common Test Interface Working Group (CTIWG) October 2003 meeting, the DoD provided the following recommendations as guidance for the Working Group's success:

[2] The numbers in brackets correspond to those of the bibliography in Annex B.

a) Identify a modular/scaleable interface
b) Allow use of different size ID/fixture on the same general purpose interface (GPI)
c) Ensure TPS hardware compatibility as interface grows
d) Provide legacy system support
e) Provide a transition path to support legacy TPS hardware
f) Adhere to an open architecture system
g) Built to one specification
h) Multiple sources
i) Non-proprietary design and components
j) Ensure capabilities that provision for growth and special requirements
k) Provide room for future expansion and TPS requirements
l) Support and Promote the use of commercial-off-the-shelf (COTS) interconnect components
m) Use industry standard connector technology

1.3.4 CTIWG legacy test program set support

In support of these recommendations, the CTI architecture shall assure past legacy and future TPS *plug and play* compatibility between defense agencies and defense-aerospace suppliers. Areas addressed by the CTIWG include:

a) Pin mapping
b) Scalability
c) TPS legacy support
d) Connector parametric (dc to light)
e) Reliability and maintainability
f) Physical
g) Switching
h) Design-to-cost factors

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated referenced, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1505-2006, IEEE Standard for Receiver Fixture Interface.[3, 4]

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3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standards Terms* [B5] should be referenced for terms not defined in this clause.

3.1.1 pin map: The data table and explanatory text that provides the assignment of electrical characteristics or instrument I/O to specific pins.

3.2 Specification terms

The specification terms used throughout this standard are described as follows.

Rule: Rules *shall* be followed to ensure compatibility to the standard. A rule is characterized by the use of the words *shall* and *shall not*. These words are not used for any other purpose other than stating rules.

Recommendation: Recommendations consist of advice to applicants that will affect the usability of the final device. Discussions of particular hardware to enhance throughput would fall under a recommendation. These should be followed to avoid problems and to obtain optimum performance.

Suggestion: A suggestion contains advice that is helpful but not vital. The reader is encouraged to consider the advice before discarding it. Suggestions are included to help the novice designer with problematic areas of the design.

Permission: Permissions are included to clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. The word *may* is reserved for indicating permissions.

Observation: Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

3.3 Acronyms and abbreviations

ACPS	alternating current power supply
ADC	analog-to-digital converter
AI	analog instrument
AM	amplitude modulation
ATE	automatic test equipment
ATS	automatic test system
AWG	arbitrary waveform generator, American wire gauge

CAL	calibration
CAN	controller-area network
CASS	Consolidated Automated Support System[5]
CH	channel
CIWG	Critical Interfaces Working Group
CLK	clock
COTS	commercial-off-the-shelf
CSW	coax switch
CTI	common test interface
DAC	digital-to-analog converter
DAS	display analyzer-simulator
DCPS	direct current power supply
DMM	digital multi-meter
DoD	U.S. Department of Defense
DTC	design-to-cost
ECL	emmitter-coupled logic
ESTS	Electronic Systems Test Set[6]
ETE	end to end
EXT	external
freq	frequency
FTIC	frequency time interval counter
GND	ground
GPI	general purpose interface
HPL	high-power load
IAIS	improved avionics intermediate shop
ICD	interconnecting device

[5] US Navy Tester, AN/USM-636 (V).
[6] US Air Force Tester, AN/GSM-397 (V).

ID	interface device
IFTE	Integrated Family of Test Equipment [7]
Instr	instrument
I/O	input/output
ITA	interface test adapter
JTAG	Joint Testability Action Group
LCC	life-cycle costs
LFC	low-frequency calibrator
LM-STAR®	Lockheed Martin Star[8]
LPL	low-power load
LXI	LAN extensions for instrumentation
max	maximum
min	minimum
MOD	modulation
MoD	Ministry of Defense (UK)
MOD SRC	modulation source
MRK	marker
MTA	microwave transition analyzer
MTBF	mean time between failures
MUX	multiplexer
NOM	nominal
OCD	open-collector driver
ORD	Operational Requirements Document
PAM	phase-angle modulation
PCI	Peripheral Component Interface

[7] US Army Tester, AN/USM-632 (V)3.
[8] LM-STAR is a registered trademark of Lockheed Martin Corporation. This information is given for the convenience of users of this standard and does not constitute an endorsement by the IEEE of these products. Equivalent products may be used if they can be shown to lead to the same results.

PECL	positive emmitter-coupled logic
PGEN	pulse generator
PH	phase
PM	pulse (or phase) modulation, power meter
Prog	programmable
PS	power supply
PSW	power switch
PXI	PCI Extensions for Instrumentation (compact PCI format)
RAF	Royal Air Force
ResLoad	resistive load
RF	radio frequency
RFI	receiver fixture interface
RSIA	raster stroke image acquisition
SAMe	sistema automatico de mantenimiento estandar
Spec An	spectrum analyzer
STA	system trigger assembly
Std	Standard
Sync	synchronizer
TETS	Third Echelon Test System[9]
TPS	test program set
Trig	trigger
TSP	twisted shielded pair
TTL	transistor-transistor logic
UBIC	universal bus interface controller
USB	Universal Serial Bus
UUT	unit under test
VGA	Versatile Graphics Adapter

[9] US Marine Tester, AN/USM-657 (V)1, (V)2, (V)3.

VME versa-module extended

VXI VME extended for instrumentation

4. Common test interface requirements

4.1 Introduction

The following subclauses and illustrations describe the requirements for this standard, IEEE Std 1505.1-2008, to support military/aerospace test requirements. This information is supplemental and not stand-alone and shall coexist with that presented in the IEEE Std 1505 RFI specifications, Clause 1 through Clause 6.

The IEEE 1505.1 standard for the use of IEEE 1505 RFI to support military/aerospace test requirements represents a higher order subset of cost/physical/signal performance requirements to meet specific industry and defense agency goals of a common test interface (CTI). These high order requirements expand on the previously defined RFI: (a) framework; (b) connector modules and respective contacts; to meet objectives for: (c) a common scalable pin map configuration; (d) switching; and (e) legacy ATS transitional device for Third Echelon Test System (TETS), Consolidated Automated Support System (CASS), Integrated Family of Test Equipment (IFTE), and others as deemed necessary by the cognizant agencies. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future ATS.

4.2 CTI open system requirements

4.2.1 Government “open system” policy

On 29 November 1994, the Honorable Paul G. Kaminski, Under Secretary of Defense for Acquisition and Technology, directed acquisition executives in the DoD to use “open systems” specifications and standards (electrical, mechanical, thermal, etc.), for acquisition of all weapon systems electronics to the greatest extent practical. The Open Systems Joint Task Force (OS-JTF) was formed in September 1994 to: “Sponsor and accelerate the adoption of open systems in weapons systems and subsystems electronics to reduce life-cycle costs (LCC) and facilitate effective weapon system intra- and interoperability.”

4.2.2 CTI “open” architecture

Rule 4.2.2: An open standard CTI *architecture* shall identify components, the relationship between components, and the rules for the architecture’s composition.

Recommendation 4.2.2: Typical guidelines for addressing the CTI architecture should include:

a) Define and describe a system architecture that is traceable to the Operational Requirements Document (ORD).

b) A preferred architecture is modular, hierarchical and layered, and is based on open standards at its interfaces.

c) Selection of an architecture shall be a cooperative process between government and industry.

d) Specify key performance attributes of system building blocks including internal interface standards.

e) Where a new system is contemplated, consensus among potential contractors and their key suppliers on application of widely accepted standards is desirable.

f) Identify aspects of the program that might limit the use of an open systems approach.

g) Determine the level at which the architecture will be defined for the system.

h) Architecture approach resulting from a system engineering process shall be linked to a business case analysis.

i) Decisions about architecture shall be linked to performance, LCC, schedule, and risk.

j) Identify opportunities for reuse of hardware and software configuration items and dependence upon interfaces.

4.3 CTI cost requirements

Recommendation 4.3a: Fundamental to the implementation of the CTI recommended practice should be the paramount need to address design-to-costs (DTC) and LCC attributed to test interface and TPS requirements.

Recommendation 4.3b: CTI should improve the test acquisition process by creating a competitive multi-vendor environment that provisions common module components that can be procured as COTS, at pricing that benefits from industry economics-of-scale production/quality processes, and improved time-to-market availability.

Recommendation 4.3c: CTI should meet advanced functional and technological needs through shared industry R&D, multi-functional/virtual modules that can be replicated, distributed, and reconfigured to meet a broad set of applications without customization. Extend legacy system life through technology insertion of plug and play enhancements based upon standardized infrastructure, and related cost-avoidance of ATS obsolescence.

Recommendation 4.3d: CTI should minimize configuration variations and related software customization and adjustments between unique test assets, integration methods, and signal routing schemes.

Recommendation 4.3e: CTI should promote cooperative design, design reuse, shared design data models, automation in software development, rehostability and portability of TPSs, implementation of lessons learned, and enhance long-term support between vendors, integrators and users. Standards also promote common fabrication processes, signal routing schemes, canned solutions that could reduce TPS engineering integration time and cost.

4.4 Vertical integration test support requirements

Recommendation 4.4: The implementation of the CTI/RFI standard as common *vertical integrated test support* through the product cycle and various maintenance levels assures the greatest benefits of common system implementation and cost savings. Specific benefits include the shared development/manufacturing of ATS and TPS assets, enhanced TPS verification and refinements, and transitional improvements in lessons learned, hands-on training and asset management.

4.5 CTI configuration/interoperability requirements

Rule 4.5: CTI *pin map requirements,* as defined by *general pin map requirements* in Annex A, and subsequent detailed *CTI pin map input/output (I/O) configuration*, shall be implemented to assure test interface interoperability between agencies and ATS configurations.

Recommendation 4.5: A common CTI pin map configuration has been recommended across government multi-agencies, to stimulate greater use of common assets, which reduces proliferation and support duplication. By satisfying interoperability requirements between government agencies TPS development, deployment and asset duplication can be eliminated and related weapon system support enhanced.

4.6 Maintainability/end-user support requirements

Rule 4.6: The general pin map requirements in Annex A, and subsequent detailed CTI pin map I/O configuration, as part of this IEEE 1505.1 CTI document, shall be maintained/upgraded through IEEE standards revision processes.

Recommendation 4.6: The CTI implementation within industry and the government, utilizing standard product configurations, multi-vendor interchangeable parts, calibration, and maintenance support is recommended.

Observation 4.6: Applying common CTI products to ATS and CTI fixture deployment would dramatically reduce duplicative requirements for unique system development, validation, production, deployment, configuration product management, and long-term support. This approach would further enhance asset availability/uptime mean time between failures (MTBF), calibration/spares consolidation, and mean-time-to-repair (MTTR) results. Users could also benefit from common maintenance practices, tooling, and training costs. CTI implementation would also focus product management/feedback on a smaller number of unique installed systems, their related failures/lessons learned, and iterative improvements, resulting in improved reliability, less obsolescence, and longer life cycles.

4.7 Scaleable architecture requirements

4.7.1 Overview

Rule 4.7.1: CTI shall support modular and scaleable concepts as illustrated in Figure 1. Based upon the IEEE 1505 RFI standard, CTI shall support upward scalable compatibility without modification or added extensions of a low-end (4-slot CTI configuration), and a mid-sized (20-slot CTI configuration), to a high-end (29-slot CTI configuration) test system capability.

Observation 4.7.1: Scalability—"Serves to minimize or eliminate the costs of fixturing by scaling the requirements to minimum framework and related pin map configuration. This minimizes the size, storage requirements, and complexity of fixturing, as well as related receiver and fixture(s) costs, to only what is necessary to interface the unit under test (UUT) to the ATS (e.g., a cable assembly can be plugged into the receiver without a fixture box being applied). This also permits an avionics board manufacturer to develop a compatible TPS for factory test and allow the Government to utilize that same fixture on the high-end depot tester without modifications/adapters. Such capabilities demand that the mechanism support engagement actuators at incremental points to pull smaller fixtures into the receiver."

4.7.2 General building block architecture

Rule 4.7.2: CTI shall support a scalable building block architecture with common I/O pin map that remains upwardly compatible with matched connector/contact configuration and scalable application levels described in Table 1.[10]

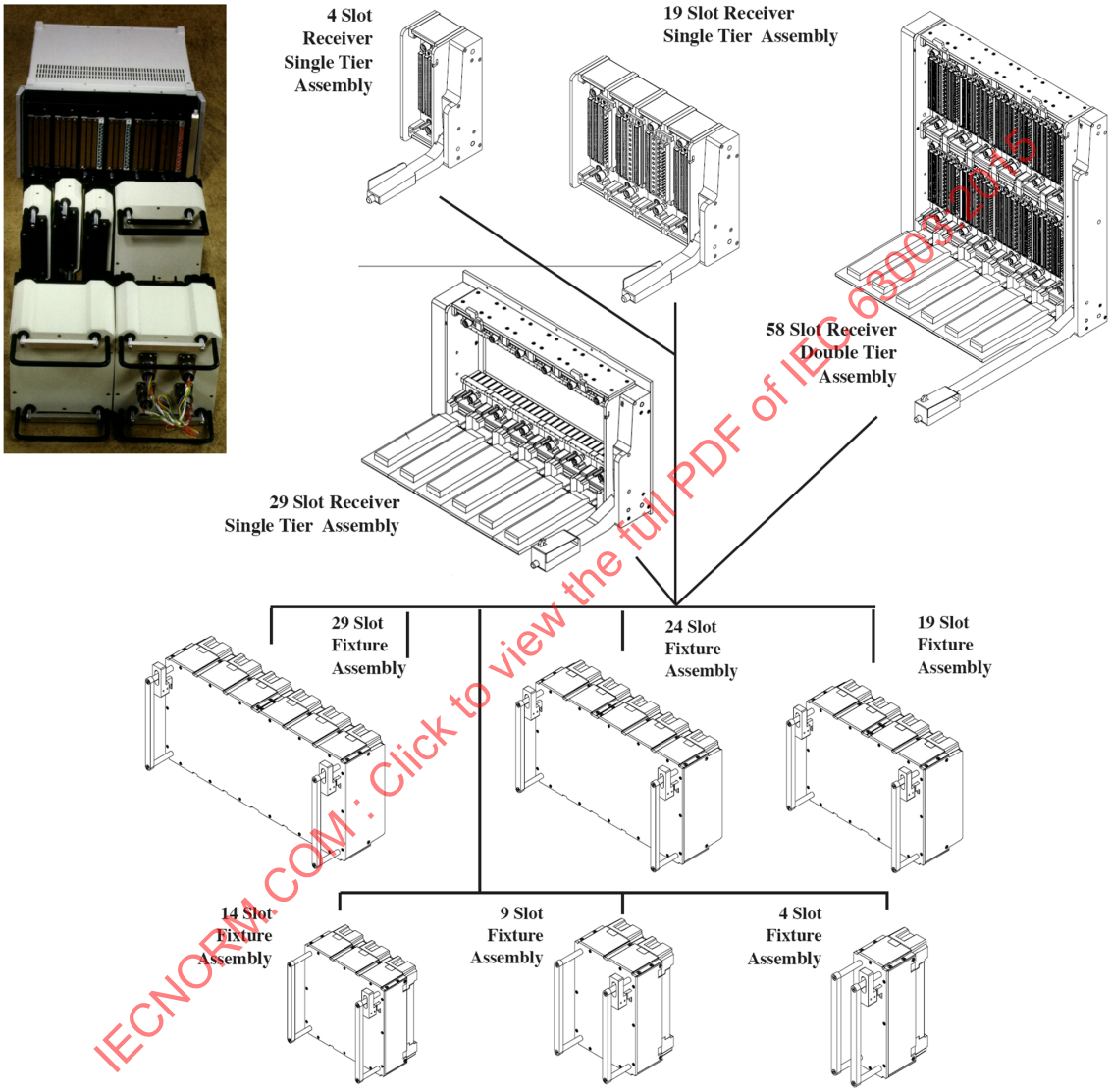

Figure 1—CTI system receiver modular scalable framework architecture

[10] Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

4.8 Physical framework requirements

4.8.1 IEEE 1505 RFI standard compliance

Rule 4.8.1: The CTI shall be fully compliant with IEEE Std 1505 RFI standard framework specifications, Clause 5, expandable to two tiers, to a maximum of 29 slots per tier (26 slots usable for connector mounting, see Figure 2 and Figure 3).

Table 1—CTI building block suggested configuration

Worse case: High-end test system application—26 connector slots/3 blanks	
Signal contacts:	3200 pos, 0-3A/200 pos module
Lo / hi power contacts:	270 pos 23 A / 152-59 pos
Lo / hi coax contacts:	363 pos 3 GHz / 152-59 pos
Typical: Mid-range test system application—18 connector slots/2 blanks	
Signal contacts:	2800 pos, 0-3 A/200 pos module
Lo / hi power contacts:	211 pos 23 A / 152-59 pos
Lo / hi coax contacts:	59 pos 3 GHz / 152-59 pos
Basic: Low-end test system application—4 connector slots	
Signal contacts:	600 pos, 0-3 A/200 pos module
Lo / hi power contacts:	59 pos 23 A / 152-59 pos
Lo / hi coax contacts:	0 pos 3 GHz / 152-59 pos
NOTE—pos = position (interchangeable with term *contact* in this context)	

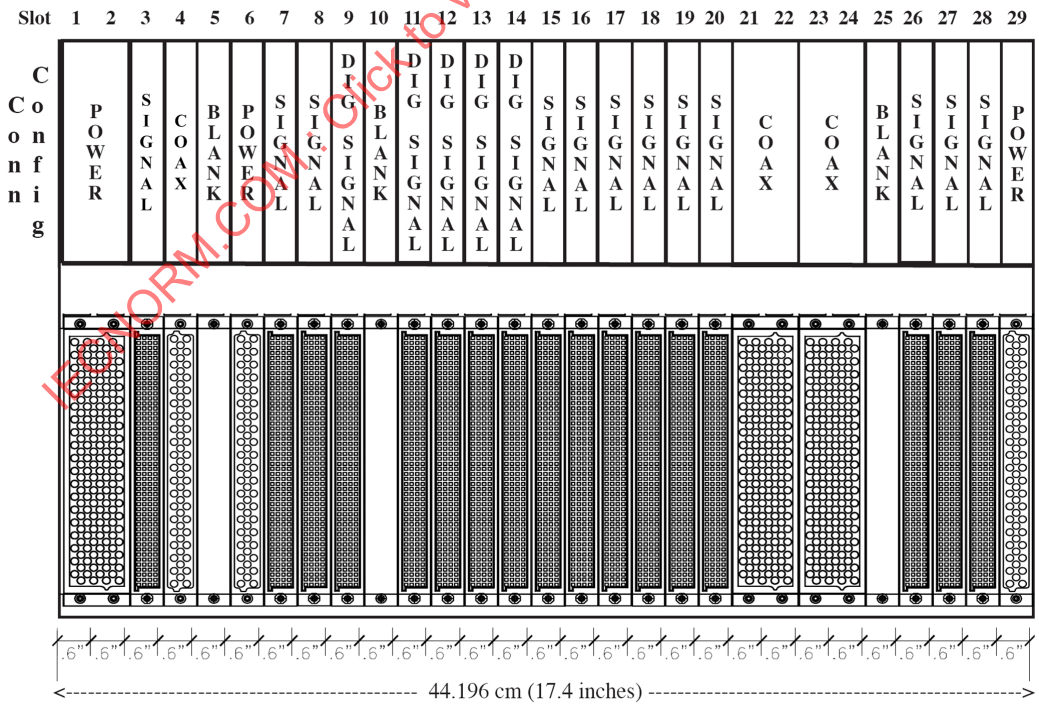

Figure 2—CTI system 29-slot receiver connector configuration

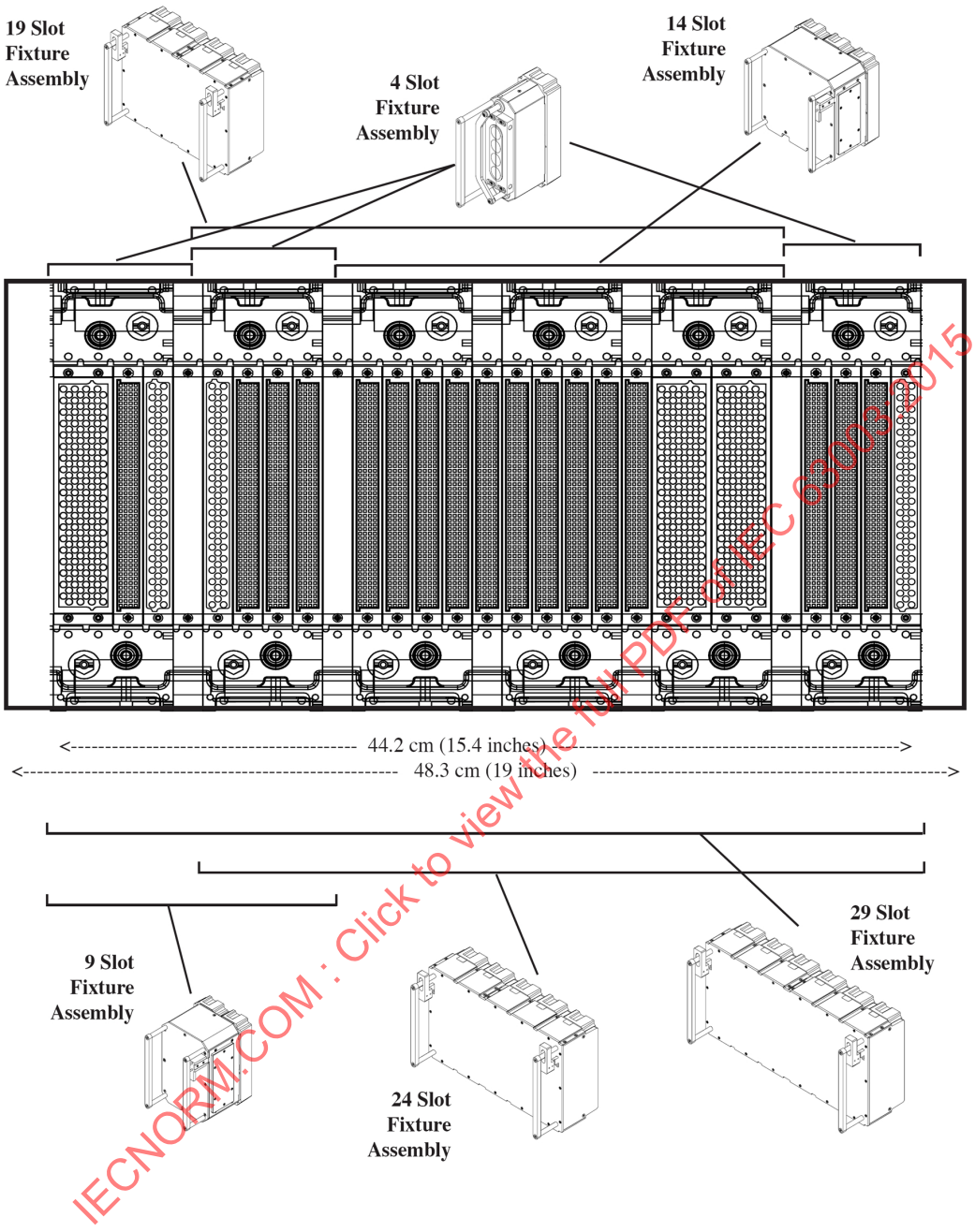

Figure 3—CTI system configuration to fixture options

4.8.2 CTI modular combination framework design

Rule 4.8.2: Under IEEE Std 1505 *combination framework specification* (detailed in the RFI framework specification, Clause 5), the CTI *framework* shall provision three (3) blanks at slot 5, 10, and 25 to provision a 1.524 cm (0.6 in) spacing for the protective shrouds of two adjoining fixtures.

Permission 4.8.2: Combinational framework requirement can be implemented in any of two methods: (a) combining *segmented and continuous framework* (illustrated in Figure 6), to form a 29-slot configuration

made up of three (3) segmented 5.6 cm (3 in) wide frames, with four (4) connector slots each, and one (1) continuous 22.9 cm (9 in) wide frame, that supports fourteen (14) connector slots that supports frame/blank spacing at slots 5, 10, 25; or (b) modifying a 29-slot continuous framework (illustrated in Figure 5 and Figure 6), to provision three blanks at slots 5, 10, 25.

4.8.3 CTI receiver footprint/scaleable requirements

Rule 4.8.3a: CTI receiver framework footprint shall be a scaleable combinational implementation that can be incremented from the smallest footprint of a segmented framework of four (4) connector slots, and expandable to 29 slots by adding segmented and/or continuous framework intervals, while maintaining downward compatibility with any smaller fixture increments (26 slots for connectors and 3 slots for shroud spacings). Either of the framework implementations can be reduced to any interval segmented at slot 5, 10, and 25 with combinations that can support 4, 8, 14, 18, or 22 slots usable for connector mounting. All connector configurations shall satisfy the IEEE Std 1505 framework/connector specifications, Clause 5 and Clause 6, and CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.8.3b: Physical footprint of the CTI *receiver framework* shall be in accordance with framework specification, Clause 5, that describes receiver framework under IEEE Std 1505 segmented and continuous framework layouts, as the examples in Figure 4 and Figure 6 further illustrate. Although the receiver drive system implementation is supplier dependent, the CTI receiver mechanical drive system shall not extend beyond the dimensional envelope of a standard 48.3 cm (19 in) rack width or height of 35.6 cm (14 in) (including handle height);

Rule 4.8.3c: The CTI specification permits integrators or users to add incremental receiver framework, anytime, to satisfy any mix of fixture requirements, as shown in Figure 1 and Figure 3, that includes multiple tier increments (two tier shown in Figure 1), in accordance with the CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.8.3d: Overall physical size of each CTI *receiver tier,* including drive assemblies, shall not exceed standard 19 in equipment rack width in accordance with EIA/ECA-310-E (2005) [B3], or 35.56 cm (14 in) height, or protrude from the mounting plate more than 8.89 cm (3.5 in).

4.8.4 CTI receiver physical weight requirements

Rule 4.8.4: Physical weight of the CTI receiver framework shall not exceed a maximum of 5.63 kg (8.0 lb) per 7.62 cm (3 in) frame interval and 21.8 kg (48.0 lb) for each CTI 29-slot tier, including fully populated connector modules and the engagement mechanism.

4.8.5 CTI mechanical engagement requirements

Rule 4.8.5: The CTI *receiver mechanical engagement system* shall be in accordance with framework specification, IEEE Std 1505, Clause 5, and provide sufficient mechanical advantage to overcome the physical mating insertion force of a fully-populated interface and the cantilevered fixture weight requirements, and apply sufficient mechanical advantage to assure a 15.9 kg (35 lb) of handle force is not exceeded.

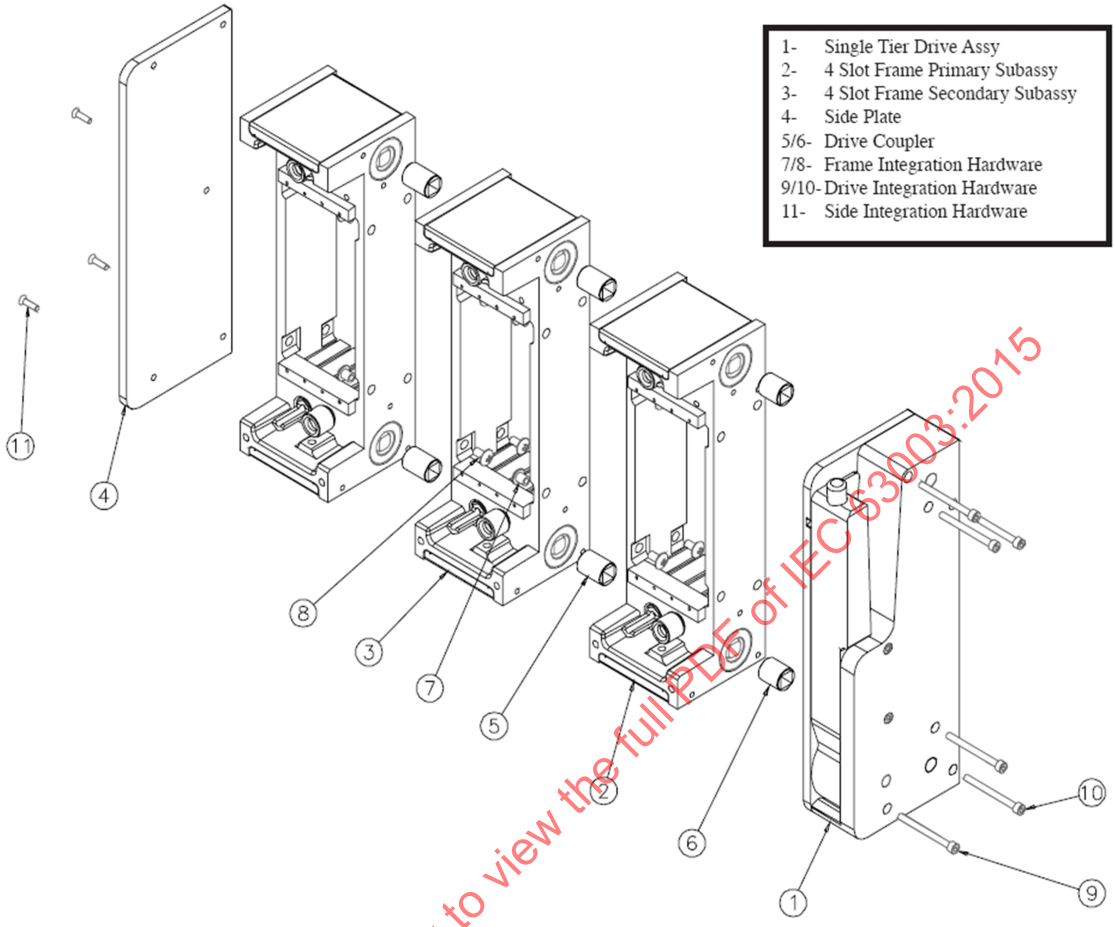

Figure 4—IEEE 1505 receiver segmented framework example

4.8.6 CTI fixture weight requirements

Rule 4.8.6: Each CTI receiver 4-slot *frame increment* shall support a maximum static fixture weight (fixture fully engaged to receiver) of 4.54 kg (10 lb) cantilevered at 38.1 cm (15 in) from receiver mating interface while meeting cycle life, interface insertion force, and electrical parametric requirements. In increments of 4.54 kg (10 lb) per 7.62 cm (3 in) frame interval, a CTI 29-slot receiver with six frame intervals shall support a maximum of 22.68 kg (50 lb) at 38.1 cm (15 in).

NOTE—Implementers/users shall provide additional safety support to assist operators during lift, and prevent injury or damage to equipment, when engaging/disengaging heavy fixture applications.

4.8.7 Oversized fixture keep-out area

Rule 4.8.7: Fixture manufacturers that offer large (oversize) fixture footprints shall not intrude on the dimensional areas annotated in Figure 5.

Observation 4.8.7: The area to the right is reserved for operation of the engaging handle. The area below the fixture is reserved for fixture support facilities.

CAUTION
Manufacturers should be cognizant of cantilevered weight and other surrounding interference factors that may impact implementation when standard footprints are exceeded.

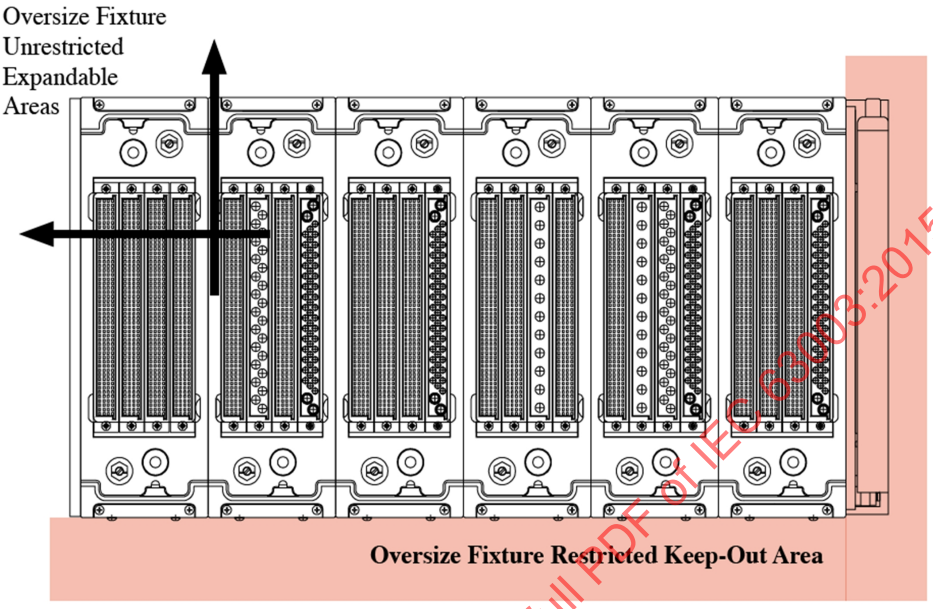

Figure 5—Fixture (ITA) footprint restricted areas

4.8.8 Transportability/mobility requirements

Rule 4.8.8: CTI shall meet transportability/mobility requirements per the IEEE Std 1505 RFI environmental/quality specifications, defined in Clause 4 and Clause 5 of the standard. A fully assembled CTI (framework, connector modules, contacts, and engagement mechanism) shall withstand a 5 ms of 49 m/s for shock drop test.

Observation: 4.8.8: The intent of the drop test is to ensure the assembled interface does not deform or otherwise become unusable if it is "dropped" during assembly or repair. The condition of this test includes the interface as a stand-alone object, impacted on all corners and faces at a 5 ms of 49 m/s for shock drop test force.

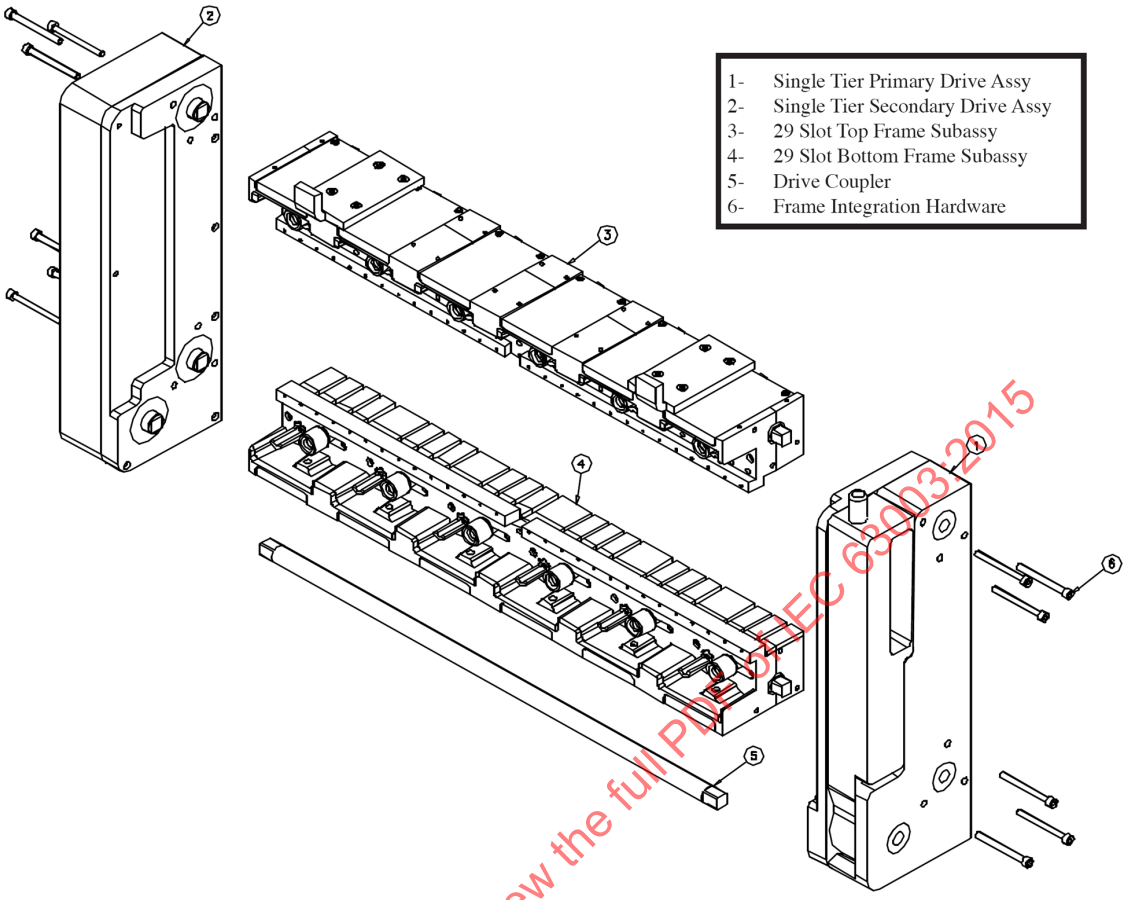

Figure 6—IEEE 1505 receiver continuous framework example

4.9 Reliability requirements

4.9.1 Repeatability/reproducibility/interchangeability

Rule 4.9.1: CTI design shall conform to dimensional and functional requirements defined in IEEE Std 1505 RFI environmental/quality specifications, described in Clause 5 and Clause 6, in order to assure component part interchangeability/intermateability and interoperability between components from multiple vendors. Component parts shall remain "operational" through life of the program. Any part changes that affect form, fit, or function cannot obsolete existing parts.

4.9.2 Mean time between failures requirements

Rule 4.9.2: CTI components shall be designed and produced to perform without failure between established durability/life-cycle requirements. Failures shall be assessed to determine cause and corrective actions. MTBF data for the CTI components shall be calculated in accordance with MIL-HDBK-217 [B21].

4.9.3 Durability and cycle life

Rule 4.9.3: Durability and cycle life for CTI receiver/fixture mechanism shall have a minimum durability rating of 25 000 cycles. Connector module contacts shall have a minimum durability rating of 10 000 cycles. Cycle limits are considered end of life requiring replacement of wearable items. Manufacturers shall validate conformance to this specification in accordance with the IEEE Std 1505 RFI qualification requirements, Clause 4, cycle testing, and per framework specifications, Clause 5.

4.10 CTI connector footprint/parametric requirements

4.10.1 IEEE 1505 RFI standard compliance

Rule 4.10.1a: CTI shall be compliant with the IEEE Std 1505 RFI standard connector specifications, Clause 6, that establishes the Eurocard DIN standard connector footprint as the basis of CTI architecture.

Observation 4.10.1: Both commercial and ruggedized versions (under MIL-C-55302/179-180 [B20]) were available in a 200-pin, 4-row connector by two of the three primary interface suppliers. Signal module meets the highest levels for open system, low-cost, performance, COTS acceptance, and level of applicability, receiving more than 25% higher grade over any of the other connectors reviewed.

Rule 4.10.1b: CTI shall implement three DIN connector types: (a) signal; (b) power; and (c) RF coax; as defined in IEEE Std 1505 RFI standard connector specifications, Clause 6, and related connector specifications, Clause 7 through Clause 12.

4.10.2 CTI requirements for compliance

Rule 4.10.2: Suppliers of systems shall state their degree of compliance to IEEE Std 1505.1 using the definitions of compliance in 4.10.2.1 and 4.10.2.2.

4.10.2.1 Mechanical compliance

Rule 4.10.2.1: To meet this criteria, a manufacturer shall at the minimum supply an IEEE 1505 RFI compliant interface that conforms to a connector per slot type that matches the configuration shown in Figure 2. That is, the power connector is used in slot ½, the 200-pin signal module in slot 3, etc.

Observation 4.10.2.1: This level of compliance only ensures that physical connector damage will not result from installing a fixture (ITA/ID) from one minimum level compliant system onto a different minimum level compliant system's receiver. It does *not* ensure that the proper signals will be routed.

4.10.2.2 Full compliance

This is the highest degree of compliance and requires full slot-by-slot mechanical and electrical compatibility for the stated compliance categories defined as follows.

Rule 4.10.2.2a: To state full compliance, a manufacturer shall meet all the requirements for the signals for each slot as identified in Annex A, except for the columns labeled "Recommended attributes." Non-populated modules should be blank (e.g., if block is "blank," it can be keyed normally; if block has different pin out, it shall be keyed differently). Both the full compliance and the following category shall be stated.

The following are the defined categories:

a) Category 1—This is defined as mechanically and electrically compliant with the Annex A slots 6 through 9. This is the basic *stimulus-measurement* section of the pin map.

b) Category 2—This is defined as mechanically and electrically compliant with Annex A slots 1 through 9. This is the basic stimulus-measurement plus power supplies and switching of the pin map.

c) Category 3—This is defined as mechanically and electrically compliant with Annex A slots 6 through 24. This is the basic stimulus-measurement plus digital, switching, and additional analog of the pin map.

d) Category 4—This is full slot compliance (mechanical and electrical) for slots 1 through 24 of the Annex A pin map.

e) Category 5—This is full slot compliance (mechanical and electrical) for all 29 slots of the Annex A pin map.

NOTE—Partially compliant approaches shall rotate keys 180 degrees to insure that physical and/or electrical damage is not incurred.

Observation 4.10.2.2: This level of compliance ensures both mechanical compatibility between systems *and* electrical signal compatibility/interoperability between systems for the slots included in the categories. The categories represent scalable increments based on the segmented architecture and the electrical signals included in the scalable options.

Permission 4.10.2.2a: Pins may also have lesser or higher capability as identified in Annex A tables as long as the pin mapping of Annex A is met and the capability is of the same/similar functionality. For example, an identified dc power supply (DCPS) capability identified in Annex A should be matched with a DCPS, not an ac supply.

Permission 4.10.2.2b: The designer of a compliant system is allowed to implement capability identified in Annex A with non-classical instruments.

4.10.3 Standardized keying

A standardized keying arrangement is required to support the compliant interfaces. Each 4-slot section of the IEEE 1505 RFI interface has a top and bottom key as shown in Figure 7. Each key is set in a hexagonal socket that allows one of six rotational positions. Therefore, with the top and bottom key being independently variable, the keying of one 4-slot segment can have one of 36 different keying arrangements.

Rule 4.10.3a: Systems (receivers and ITAs) that implement a mechanically or fully compliant interface as defined in 4.10.2 and subparagraphs shall implement the keying as shown in Figure 7.

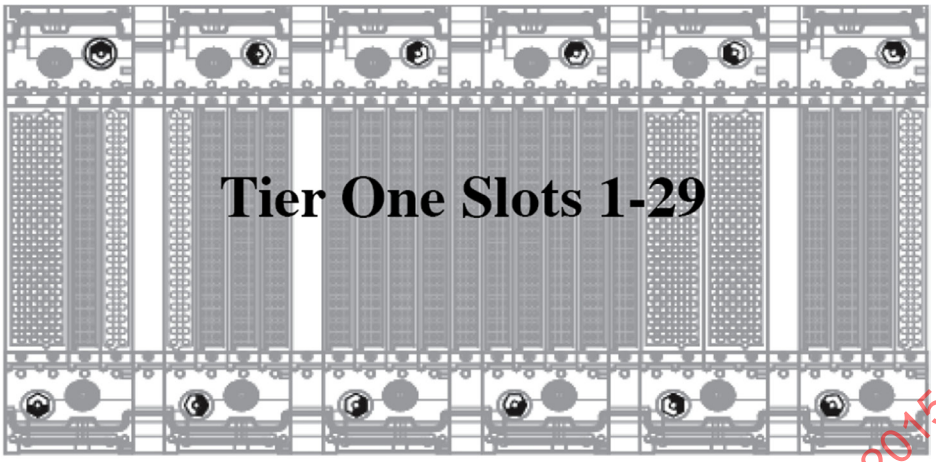

Figure 7—Standardized keying for compliant systems (receiver view)

Rule 4.10.3b: Systems that have segments that are non-compliant per the definition of 4.10.2 shall implement a different keying option. The option used shall *not* duplicate any of the keying options shown for a compliant interface for any section. The goal is to *prevent* any ability to mount a compliant ITA on any non-compliant receiver or a non-compliant ITA on a compliant receiver.

4.10.4 Population policy

Rule 4.10.4a: A test system developer shall follow a set order of precedence in the selection of test assets and the associated pins from the pin map. The following process shall be followed:

a) Identify an unused test asset/instrument that meets the *minimum* test requirements.

b) If the asset/instrument is part of a group of like-capability assets, use the lowest numbered, available (unused) asset for the test.

c) Proceed in like fashion for the entire group of similar assets

d) If the *minimum* required capability assets become completely used (implemented) in the TPS, proceed to utilize the next highly capability asset/instrument.

e) If this asset/instrument is part of a group, follow the same rules in which the lowest numbered is utilized first.

Rule 4.10.4b: A TPS developer shall follow a set order of precedence in the selection of test assets and pins from the pin map. The following process shall be followed:

1) Select an unused test asset/instrument that meets the *minimum* requirements for the test.

2) If the asset/instrument is part of a group of like-capability assets, use the lowest numbered, available (unused) asset for the test.

3) Proceed in like fashion for the entire group of similar assets

4) If the *minimum* required capability assets become completely used (implemented) in the TPS, proceed to utilize the next highly capability asset/instrument. These should also be implemented from lowest numbered asset to higher numbered asset.

5) If this asset/instrument is part of a group, follow the same rules in which the lowest numbered is utilized first.

Recommendation 4.10.4: Refer to Annex A tables for clarification of asset capabilities and how assets are numbered.

4.10.5 CTI connector parametric requirements

Rule 4.10.5: CTI connector module with contacts shall comply with the definitions contained in IEEE Std 1505 RFI connector specifications, Clause 6, and related connector specifications, Clause 7 through Clause 12, that satisfies the respective parametric requirements defined by Table 2.

Table 2—CTI connector module/contact module performance requirements

Signal contact/module	
Operating voltage:	300 Vdc max
Operating current:	3.0 Adc continuous
Contact resistance:	10 mΩ max
Insulation resistance:	5.0 x 10e9 Ω min
Capacitance:	10 pF max
Reliability:	10 000 engagement cycles
Footprint:	025 in square pins on 0.1 in centers arranged in 4 row x 50 pin multiples
Mating force:	2.0 oz/pin max
Module footprint:	200 positions in 4 columns
Power module/contact	
Operating voltage:	300 Vdc max
Operating current:	23 A dc/ac rms continuous/free stdg/ambient air
Contact resistance:	5 mΩ max
Characteristic imped:	n/a
Insulation resistance:	5.0 x 10e9 Ω min
Capacitance:	10 pF max
Reliability:	10 000 engagement cycles
Contact:	Size 16 DIN requirements
Mating force:	18 oz/pin max
Module footprint:	59 positions in 3 columns, or 152 positions in 8 columns

Table 2–CTI connector module/contact module performance requirements *(continued)*

Coax module/contact	
Frequency bandwidth:	dc 3 GHz
Operating voltage:	150 V ac, rms
Contact resistance:	10 mΩ max
Voltage standing wave ratio (VSWR):	1:1.22 + 0.52 f (GHz)
RF insertion loss:	.03√f (GHz)
RF leakage:	– 90dB at 2.5 GHz
Contact resistance:	Center contact; straight 6.0 mΩ max
Crosstalk:	Less than or equal to – 90 dB to 2 GHz
Characteristic imped:	50 ± 2 Ω
Insulation resistance :	1000 MΩ min
Capacitance:	15 pF max
Reliability:	10 000 engagement cycles
Contact:	Size 16 DIN requirements
Mating force:	18 oz max
Module footprint:	59 positions in 3 columns or 152 positions in 8 columns

4.11 CTI pin map requirements

4.11.1 CTI scaleable/modular pin map configuration

Rule 4.11.1a: The CTI scaleable pin map configuration shall support scalability (the use of less than a full tier interface as previously discussed in 4.8.3), through the distribution of station resources as defined in CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.1b: The CTI configuration shall apply the five (5) connector modules: (a) signal, single slot 200 position; (b) power, single slot 59 position; (c) power, double slot 152 position; (d) RF coax, single slot 59 position; and (e) RF coax, double slot 152 position; in the configuration shown in Figure 2, and in accordance with RFI connector specification, connector specifications, Clause 7 through Clause 12 of IEEE Std 1505.

Rule 4.11.1c: The CTI configuration shall be implemented in intervals conforming to framework segmentation in accordance with RFI framework specification, Clause 5 of IEEE Std 1505, that supports mounting of connector types in intervals of four (4), four (4), fourteen (14), and four (4) slots, or any reduced footprint, as determined by the specific application.

4.11.2 CTI pin map I/O categories

Rule 4.11.2: The CTI connector configuration, as illustrated in Figure 2, shall be implemented in accordance with detailed CTI pin map I/O configuration and general pin map requirements, Annex A. These requirements shall be divided into several I/O parametric categories, described as follows, and distributed in scaleable segments, to assure test signal mapping is a maintained for all CTI applications.

The following describes the general pin map categories:

a) Digital I/O
b) Analog instrumentation
c) Programmable ac/dc load
d) Programmable ac/dc power supplies
e) Bus I/O
f) Switching implementation

4.11.2.1 Digital I/O

Rule 4.11.2.1a: CTI shall implement a scaleable digital I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.1b: CTI digital I/O shall be applied utilizing Eurocard DIN/MIL-DTL-55302/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI standard connector specifications, Clause 7 through Clause 12.

Suggestion 4.11.2.1: Digital I/O signal channel may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 750 MHz to a maximum of 100 channels increments (200 pins), as necessary to meet selected ATE digital requirements.

4.11.2.2 Analog instrumentation

Rule 4.11.2.2a: CTI shall implement a scaleable AI (AI) I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A, and subsequent requirements. CTI AI I/O shall be implemented utilizing either the CTI signal or coax connectors as subsequently described.

Rule 4.11.2.2b: If implemented, the CTI AI I/O shall apply Eurocard DIN/MIL-DTL-55302/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12.

Suggestion 4.11.2.2: AI I/O signal channel may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 750 MHz to a maximum of 100 channels increments (200 pins), or as necessary to meet selected ATE digital requirements.

Rule 4.11.2.2c: If implemented, the CTI AI I/O shall apply RF coaxial size 16 contact with RF coax size 16 connector module design and wiring specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12.

4.11.2.3 Programmable ac/dc load

Rule 4.11.2.3a: CTI shall implement a scaleable programmable dc load I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.3b: CTI programmable dc load I/O shall be applied utilizing the CTI power connector using 23 amp contact in a 59 or 152 positions power module connector design in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12. These contacts shall be derated to 18 A, when six or more are clustered adjacent to each other and operating simultaneously and continuously at that current level.

Suggestion 4.11.2.3: Discrete 23 amp pins should be implemented with 14 AWG MIL-spec (high temperature and flammable resistant) discrete or twisted pair wiring.

Permission 4.11.2.3: CTI programmable dc load I/O where applicable may utilize low level (current <3 A) discrete I/O signal pins using Eurocard DIN 41612 and MIL-C-179/180 5 row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12, and the CTI pin map I/O configuration and general pin map requirements, Annex A. Discrete pins may be implemented with 24 AWG discrete or twisted pair wiring.

4.11.2.4 Programmable ac/dc power supply

Rule 4.11.2.4a: CTI shall implement a scaleable programmable dc/ac power supply I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.4b: CTI programmable dc/ac power supply I/O shall be normally applied utilizing the CTI power connector using 23 amp contact in a 59 or 152 positions power module connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 6 and Clause 8. These contacts shall be derated to 18 A, when six or more are clustered adjacent to each other, and operating simultaneously and continuously at that current level.

Suggestion 4.11.2.4: Discrete 23 amp pins should be implemented with 14 AWG MIL-spec (high temperature and flammable resistant) discrete or twisted pair wiring.

Permission 4.11.2.4: CTI programmable dc/ac power supply I/O where applicable may utilize low-level (current <3 A) discrete I/O signal pins using Eurocard DIN/MIL-DTL-55302/179/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI connector specifications, Clause 7 through Clause 12. Discrete pins shall be implemented with 24 AWG discrete or twisted pair wiring.

4.11.2.5 Bus I/O

Rule 4.11.2.5a: CTI shall implement a scaleable bus I/O parametric/pin map configuration in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A.

Rule 4.11.2.5b: CTI bus capability shall be applied utilizing Eurocard DIN/MIL-DTL-55302/180 4-row 200 position connector design specifications in accordance with IEEE Std 1505 RFI standard connector specifications, Clause 7 through Clause 12.

Suggestion 4.11.2.5: Bus I/O signal channels may be implemented with 200 discrete wires, 100 twisted pairs, or two pins per channel of precision point-to-point 50 Ω matched impedance wiring having a bandwidth from dc to 500 MHz to a maximum of 100 channels increments (200 pins), as necessary to meet selected ATE bus requirements.

4.11.2.6 Switching implementation

4.11.2.6.1 General requirements

These interfaces describe the hardware requirements necessary to switch stimulus, response, and power signals between the UUT and the test instrumentation. The switching may be implemented in various ways.

Observation 4.11.2.6.1: The combination of the switch and CTI I/O provides the ATS developer the ability to select various signal paths between the instrument and UUT. Examples of switch implementations are shown in Figure 8 as: (a) benchtop units; (b) integrated switch cards; (c) rack-mounted units; and (d) switch modules meeting published industry standards such as (but not limited to) LXI, USB, VME, VXI, and PXI.

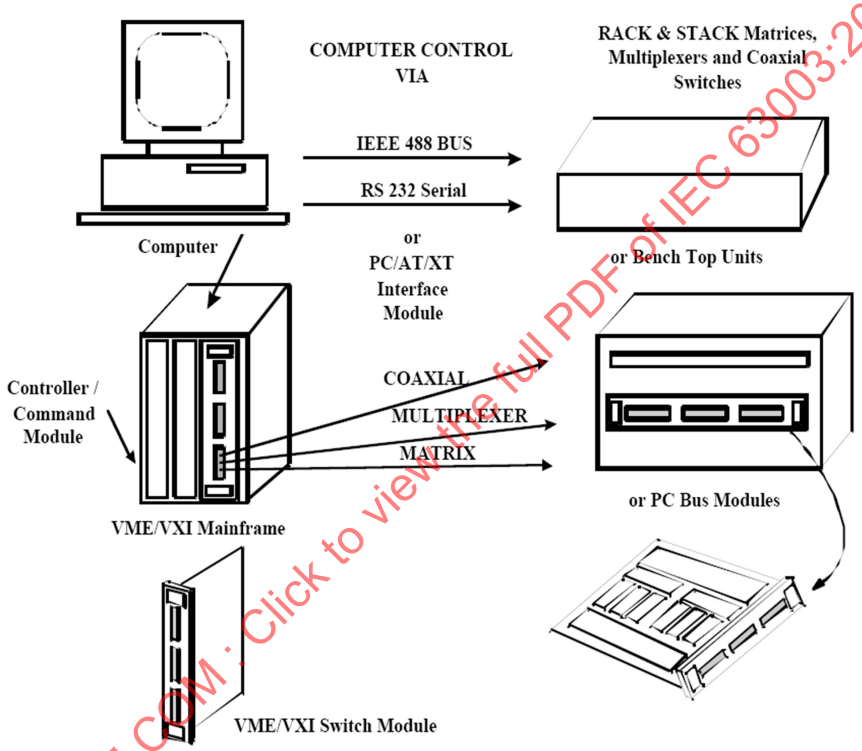

Figure 8—Switching product designs

4.11.2.6.2 Switch concerns

Observation 4.11.2.6.2: General requirements for the switch interface, described in Table 3 and Table 4, were derived from many sources representing general industry needs, Government and commercial interests, Government open-system directives, industry technology trends, Government/aerospace test requirements previously described (functional test requirements), and test industry switch defacto standards. The CIWG and CTI Switching Task Group reviewed the widest spectrum of requirements, legacy support requirements, and other interests to assure switch elements were addressed. These requirements were extracted from the envelope of the cases reviewed. This is expected to provide capability for almost every requirement the solution will encounter. During the review process standards or products that could meet these requirements were sought. The switching philosophies considered in the analysis are the following:

a) Switching outside ATE—This approach incorporates switching into the test fixture based on the UUT requirements. This places financial burden on the end user since switching needs to be incorporated in many test fixtures. This is a significant recurring cost.

b) Switching in the ATE—This approach integrates the switching capability into the ATE and treats it as additional instrumentation. This simplifies test fixture design, reduces TPS cost, and places the switching under control of the ATE system software. This can be accomplished in one of two ways:

1) *Internal hardwiring* of instrumentation to ATE switching. The internal approach simplifies test fixture design and implementation; however, a performance trade-off discussion resulted in providing instrument parts directly at the CTI. Costs associated with connecting the instruments to the switch are relegated to the electrical connectivity within the ATS-to-UUT interface adapter.

2) *External hardwiring* of instrumentation to ATE switching in the test fixture. The external approach will greatly increase test fixture complexity, however; the TPS developer has greater flexibility should higher performance instrumentation require uncompromising access at the tester interface.

4.11.2.6.3 CIWG recommended switch requirements

Suggestion 4.11.2.6.3: The Critical Interface Working Group (CIWG) Report suggested certain switch requirements that could implement COTS solutions and preserve the needs of the Government legacy programs. The following goals were utilized in assessing switching candidates:

a) Is widely accepted by industry with multi-vendor sources.

b) Has established design definitions.

c) Offers a full range of options to meet signal, power, and coax requirements.

d) Supports high life-cycle performance and maintainability.

e) Is available today in volume production and is in its early product life-cycle phase.

f) Provides a scaleable switch with a modular framework design that permits ATS integrators to incrementally augment their systems through add-on/duplicative features. This will enable them to meet worst case requirements while maintaining downward compatibility with any smaller I/O increment.

g) Establishes a common switch specification that offers multi-vendor sources, is flexible enough to support a wide variety of signal performance/switch configurations (1x2, 1x4, 1x8), and can evolve with new test needs.

h) Minimizes pin out configuration to effect greater transportability and reconfigurability is not impaired.

i) Reduces the proliferation of switch designs.

j) Defines a minimum set of performance requirements that will meet the Government I/O basic switch needs. Common I/O basic switch envelope that supports legacy 1x2, 1x4, 1x8 wrap-around signal cascade TPS requirements.

Recommendation 4.11.2.6.3: The integrator determines switch requirements based on the number of instruments and the flexibility with which they must be applied. Switch designs require a compromise between direct wire performance and switch flexibility. The CIWG concluded that switching in the ATS with internal hard wiring should be required to achieve greater cost-effectiveness and minimize fixture complexity.

4.11.2.6.4 CTI switch requirements

Rule 4.11.2.6.4: The CTI shall employ a scaleable switch that applies high performance analog switch cards for any general purpose high-end ATE system. All switch functional requirements shall be implemented directly through the CTI to support legacy switch requirements, in accordance with CTI pin map I/O configuration and general pin map requirements, Annex A. The detailed descriptions of Table 3, Table 4, Table 5, and Table 6, as well as Figure 9, provide additional switch definition/requirements to be implemented under the CTI Specification.

Table 3—Signal switch performance requirements

Switch type	Characteristic	Requirement
Signal 1x2, 2A	Time, switch	<3ms
	Crosstalk	<–60 dB (adj channels)
	Current	2.0 A
	Isolation	>=100 MΩ
	Isolation	>45 dB @ 10 MHz
	Isolation	<1E9 Ω @ dc
	Power, switched	30 Wdc, 62.5 VA ac
	Resistance to ground	>100 MΩ
	Resistance, path	<0.2 Ω
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	300 Vdc/300 Vac
Signal 1x2, 4A	Time, switch	<3 ms
	Crosstalk	<–60 dB (adj channels)
	Current, switched	4 A ac/dc
	Isolation	>=100 MΩ
	Isolation	>45 dB @ 10 MHz
	Isolation	<1E9 Ω @ dc
	Power, switched	90 Wdc, 1000 VA ac
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.2 Ω
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	300 Vdc/300 Vac

Table 3–Signal switch performance requirements *(continued)*

Switch type	Characteristic	Requirement
Signal 1x4	Time, switch	<3 ms
	Crosstalk	<–60 dB (adj channels)
	Current, switched	2A
	Isolation	>=100 MΩ
	Isolation	>45 dB @ 10 MHz
	Power, switched	30 Wdc, 62.5 VA ac
	Resistance, path	< 0.3 Ω
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	300 Vdc/300 Vac
Signal 1x8	Bandwidth (–3dB)	<100 MHz
	Time, switch	<3 ms
	Current, switched	2 A
	Isolation	<–45dB @ 10MHz
	Resistance, path	<1E9 MΩ
	Voltage, switched	300 Vdc/300 Vac
Signal 8x24	Bandwidth (–3dB)	20 MHz
	Time, switch	<3 ms
	Capacitance, CH to CH	<0.36 µF
	Crosstalk	<–60 dB @ 1 MHz
	Current, steady state	2.0 A
	Current, switched	2 A ac/dc
	Impedance, shunt cap	<0.5 µF
	Impedance	50 Ω
	Isolation	<–50 dB @ 10 MHz >=100 MΩ
	Resistance to ground	>100 MΩ
	Resistance, path	< 1.0 Ω
	Voltage, switched	300 Vdc/300 Vac
	Voltage, unswitched	350 Vac/dc

Table 4—Power switch performance requirements

Switch type	Characteristic	Requirement
Power 1x1, 10 A	Time, switch	<20 ms
	Current, steady state	10.0 A
	Current, switched	10 A ac/dc
	Isolation	>45 dB @ 5 kHz <1E9 Ω @ dc
	Power load rating	300 Wdc, 2000 VA/CH
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.1 Ω
	Voltage, switched	220 V ac/dc
Power 1x2, 10 A	Time, switch	<20 ms
	Current, switched	10 A ac/dc
	Isolation	>45 dB @ 5 kHz <1E9 Ω @ dc
	Noise floor	<=–100 dBm @ quiescent
	Power, switched	300 Wdc, 2000 VA/CH
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.1 Ω
	Voltage, switched	220 Vac/dc
Power 1x2, 10 A, low-R	Time, switch	<20 ms
	Current, contact rating	9 A
	Isolation	>=10 000 MΩ
	Power, switched	300 Wdc, 2000 VA/CH
	Resistance to ground	>100 MΩ
	Resistance, path	< 40 mΩ @ 9 A, < 500 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	250 Vac/125 Vdc
Power 1x2, 20 A	Time, switch	<20 ms
	Current, switched	20 A
	Power, switched	4800 Vac/560 Wdc
	Resistance to ground	>100 MΩ
	Resistance, path	0.05 Ω to 0.1 Ω
	Voltage, switched	240 Vac/220 Vdc

Table 4—Power switch performance requirements *(continued)*

Switch type	Characteristic	Requirement
Power 1x2, 20 A, low-R	Time, switch	<20 ms
	Current, contact Rating	18.75 A
	Current, switched	20 A
	Isolation	>=10 000 MΩ
	Power, switched	4800 Vac/560 Wdc
	Resistance, path	<20 mΩ @ 18.75 A, <250 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	240 Vac/220 Vdc
Power 1x4, 20 A,	Time, switch	<20 ms
	Current, switched	20 A
	Power, switched	560 Wdc/4800 Vac
	Resistance to ground	>100 MΩ
	Resistance, path	< 0.1 Ω
	Voltage, switched	240 Vac/220 Vdc
Power 1x4, 20 A, low-R	Time, switch	<20ms
	Current, contact rating	18.75 A
	Current, switched	20 A
	Isolation	>=10 000 MΩ
	Power, switched	4800 Vac/560 Wdc
	Resistance to ground	>100 MΩ
	Resistance, path	<20 mΩ @ 18.75 A, <250 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	240 Vac/220 Vdc
Power DPDT, 20A, low-R	Time, switch	<20 ms
	Current, contact Rating	18.75 A
	Current, switched	20 A
	Isolation	>=10 000 MΩ
	Power, switched	4800 Vac/560 Wdc
	Resistance to ground	>100 MΩ
	Resistance, path	<20 mΩ @ 18.75 A, <250 mΩ @ 1 mAdc
	Voltage, breakdown	>=1000 Vdc
	Voltage, switched	240 Vac/220 Vdc

Table 5—Coax switch performance requirements

Switch type	Characteristic	Requirement
Coax 1x2	Frequency range	DC to 1.3 GHz
	Bandwidth loss	<0.2 dB @ 100 MHz <0.5 dB @ 500 MHz <2.0 dB @ 1 GHz
	Time, switch	<=15 msec
	Crosstalk	<–65 dB @ 100Mz <–60 dB @ 500Mz <–55 dB @ 1 GHz
	Isolation, input to output	<–70 dB @ 100 MHz; <–65 dB @ 500 MHz <–55 dB @ 1 GHz
	VSWR	<1.2:1 @ 100 MHz <1.5:1 @ 1 GHz
	Characteristic impedance	50 Ω
	Current, switched	0.5 A
	Power, max	+33 dBm (2 W into 50 Ω)
	Power, switched	10 Wdc
	Power, unswitched	10 Wdc
	Resistance, dc path	<1 Ω
Coax 1x4	Frequency Range	DC to 1.3 GHz
	Bandwidth Loss	<0.2 dB @ 100 MHz <0.5 dB @ 500 MHz <2.0 dB @ 1 GHz
	Time, switch	<=15 msec
	Crosstalk	<–65 dB @ 100 MHz <–60 dB @ 500 MHz <–55 dB @ 1 GHz
	Isolation, Input to Output	<–70 dB @ 100 MHz <–65 dB @ 500 MHz <–55 dB @ 1 GHz
	VSWR	<1.2:1 @ 100 MHz <1.5:1 @ 1 GHz
	Characteristic impedance	50 Ω
	Capacitance	<0.25 µF
	Current, switched	1.0 A @ 28 Vdc
	Current, Steady State	2 A
	Power, max	+33 dBm (2 W into 50 Ω)
	Power, switched	10 Wdc
	Power, unswitched	10 Wdc
	Resistance, dc path	<1 Ω
	Resistance, to ground	>100 MΩ

Table 6—CTI switch configuration requirements

Switch nomenclature	Quantity	Power	Signal	Coax
Signal 1x2, 2 A	50		150	
Signal 1x2, 4 A	50		150	
Signal 1x4	16		80	
Signal 8x24	6		312	
Signal 8x8	16		288	
Power 1x1, 10 A	12	24		
Power 1x2, 10 A	12	36		
Power 1x2, 10 A low-R	12	36		
Power 1x2, 20 A	3	9		
Power 1x2, 20 A low-R	1	3		
Power DPDT, 20 A low-R	2	12		
Power 1x4, 20 A	1	5		
Power switch 1x4, 20A low-R	5	25		
Coax 1x2	9			27
Coax 1x4	48			240
Totals	**243**	**150**	**980**	**267**

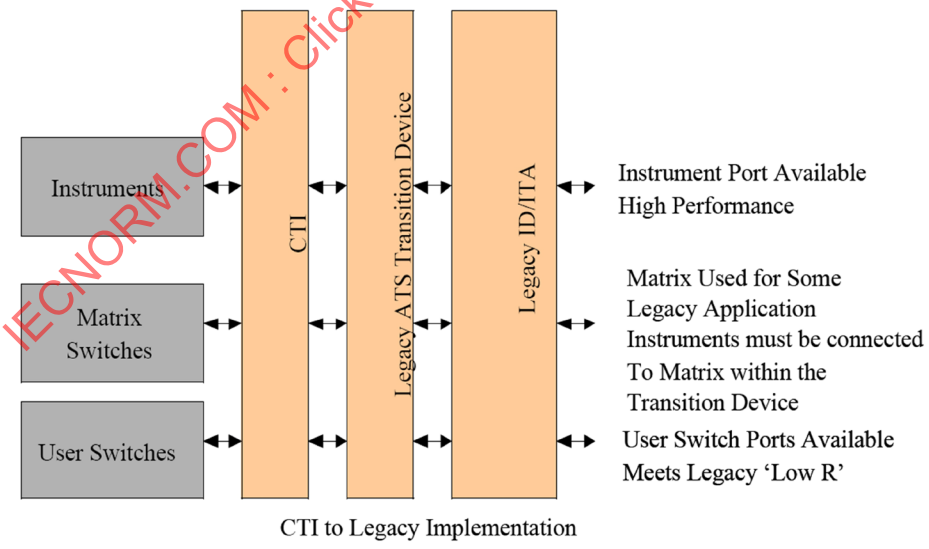

Figure 9—CTI switch architecture

4.12 CTI pin map input/output configuration

Rule 4.12: The CTI connector configuration and related CTI pin map I/O configuration and general pin map requirements, as defined in Annex A, shall be implemented in accordance with interconnect specifications detailed therein. These requirements within Annex A shall be divided into several I/O parametric categories/signal definitions, related legacy pin map I/O, and distributed in functional scaleable segments, to assure test signal mapping is maintained for all CTI applications. Pin map I/O descriptions for respective legacy systems shall be provided within Annex A to support legacy TPS and transition device requirements.

Annex A

(normative)

Common test interface signal definitions for pin map

A.1 Analog instruments (AI)

A.1.1 Analog-to-digital converter (ADC) analog-in (Table A.1)

Sixteen channels plus a trigger channel are mapped to 34 pins to support a 2-wire interface for each, i.e., Ch+, Ch–. Six shield pins are provided.

A.1.2 AI multi-parallel (Table A.2, Table A.3, and Table A.4)

Ninety-six channels are mapped to 192 pins to support a 2-wire interface for each. Thirty-two channels are mapped in the core. Each of the channels is capable of stimulus or measurement. As stimulus channels (function generator), capabilities include dc, sine, triangle, pulse, and arbitrary waveform generation. As measurement channels, capabilities include timer/counter, digitizer, digital multi-meter (DMM) and limit detect.

A.1.3 AWG (Table A.5)

The composite *arbitrary waveform generator* is comprised of 4 AWGs providing a total of 6 output channels: 1A, 1B, 2A, 2B, 3A, and 4A. Each of the 4 AWGs provide for external inputs. AWGs 1 and 2 allow for mark, trigger, and sync. AWG 3 allows for trigger and sync. AWG 4 allows trigger. These 15 interfaces are mapped to 30 pins to support a 2-wire interface for each. Two additional interfaces to the AWGs (DiffGate and DataGate) are mapped to 4 pins to support a 2-wire interface. These main functions are mapped to a total of 34 pins.

A.1.3.1 AWG emitter-coupled logic (ECL) outputs

Twenty-four differential, digital data bits provided by AWGs 1 and 2 (12 each) are mapped to 48 pins to support a 2-wire interface for each data bit. An AWG GND pin is mapped for each of these ports. These output ports are mapped to a total of 50 pins.

A.1.3.2 AWG-5

A fifth AWG adds the following 6 ports to the interface: Out, Out/7, Marker, ref, Start/Arm, StopTrigFsk. These ports are mapped to 6 coax contacts.

A.1.3.3 AWG function generator

The function generator has the following I/O: Out, Sync, Trig, Clock, and PM. These channels are mapped to 5 coax contacts.

A.1.4 AWG520 (Table A.6)

This unique capability AWG has 2 channels, 4 markers, 10 digital, an input trigger, 4 event triggers, clock-in, clock-out, and noise-gen. These 26 interfaces are mapped to 52 pins to support a 2-wire interface for each.

A.1.5 Digital-to-analog converter (DAC) analog-out (Table A.7)

A.1.5.1 DAC 1

DAC 1 has 16 channels, a trigger, and 8 keys. The first 12 channels provide for remote sense as these have 100 mA drive capability. The channels, trigger, and sense lines are collocated and are mapped as 2-wire interfaces to 58 pins. The keys are collocated and mapped as 2-wire interfaces to 16 pins. Two shield pins are provided.

A.1.5.2 DAC 2

DAC 2 has 16 channels and a trigger. The channels and trigger are collocated and are mapped as 2-wire interfaces to 34 pins. Six shield pins are provided.

A.1.6 Digitizer (Table A.8)

Four digitizer channels are mapped. Three supporting interfaces are mapped: dc Cal, ExtTrig, and Trig out. These 7 interfaces are mapped to 14 pins to support a 2-wire interface for each.

A.1.7 DMM (Table A.9)

The DMM has the customary Hi, Lo, Sense+, Sense–, and trigger paths. Two additional paths are mapped: Probe and DMM Done. These 7 interfaces are mapped to 14 pins to support a 2-wire interface for each. A Guard pin and Current pin round out the total to 16 pins.

A.1.8 Frequency time interval counter and RF counter (Table A.10)

The frequency time interval counter (FTIC) has 2 channels plus a single trigger/gate channel. These 3 interfaces are mapped to 6 pins to support a 2-wire interface for each. The RF counter has 2 interfaces: inhibit and threshold.

A.1.9 Low-frequency calibrator (Table A.11)

The low-frequency calibrator is mapped to 4 pins: Hi, Lo, Sense+, and Sense–. A guard pin and shield pin are mapped for a total of 6 pins.

A.1.10 Open-collector driver (Table A.12)

Ninety-six channels of open-collector drivers (OCDs) are mapped to 192 pins to support the 2-wire interface approach. Twelve I/O-control and 12 clock channels are mapped to 24 pins for a single wire

implementation. Two additional pins are mapped anticipating the need for returns for the I/O-control and clock channels, bringing the total for the OCD to 218 pins.

A.1.11 Pulse generator 1 (Table A.13)

Pulse generator 1 has 2 channels plus an external trigger-in and a trigger-out. These 4 interfaces are mapped to 8 pins to support a 2-wire interface for each.

A.1.12 Pulse generator 2 (Table A.14)

Pulse generator 2 has 2 channels plus an external trigger-in and a trigger-out. These 4 interfaces are mapped to 8 pins to support a 2-wire interface for each.

A.1.13 Resistive load (Table A.15)

The resistive load is mapped to 2 pins.

A.1.14 Scope (Table A.16)

Four oscilloscope channels plus an aux-out channel are mapped to 5 coax contacts.

A.1.15 Syncro-resolver (Table A.17)

Sixty-five pins are mapped for the syncro-resolver.

A.1.16 Video (Table A.18)

Two-hundred pins are mapped for video.

A.2 Bus

A.2.1 Programmable bus (Table A.19)

Sixty-four programmable bus channels are mapped to 128 pins. The programmable channels support standard serial and parallel bus formats. Four additional pins are provided as GND pins to support 1553 GND pin requirements.

A.2.2 IEEE 1149.1™ boundary scan (Table A.20)

Twenty-one pins are mapped for IEEE Std 1149.1-2001 [B13].

A.3 Digital

A.3.1 Channels (Table A.21)

Four hundred forty-eight channels are mapped to 896 pins to support a 2-wire interface for each, and 3 Kelvin grounds are mapped to 6 pins.

A.3.2 Clocks (Table A.22)

Six control clocks, one reference, 4 sync, one Kelvin ground, 4 clocks, and 6 miscellaneous signals are mapped to 22 coax pins.

A.3.3 External control (Table A.23)

Fifty-four channels are mapped to 108 pins to allow external control of the digital channels.

A.4 Instrument control

A.4.1 Spectrum analyzer (Table A.24)

Four channels, trigger, detected video, RF measure in, and 321.4 MHz IF are mapped to 4 coax contacts.

A.4.2 Modulation source (Table A.25)

Thirteen modulation sources are mapped to 13 coax contacts. RF Source 1 has 4 channels: pulse amplitude modulation (PAM) trigger, amplitude modulation (AM), frequency modulation (FM), and an External Trigger IN. RF Source 2 also has RF AM, RF FM, RF PM, and an External Trigger IN. RF Source 3 has 4 channels: AM, FM, PAM, and an External Trigger IN. There is also a microwave transition analyzer (MTA) External Trigger IN, which rounds the total to 13.

A.4.3 Power meter (Table A.26)

There are 4 power meter control interfaces. Three interfaces are mapped as: Ext Trig in, Video1, and Video2. These 3 interfaces are mapped to 3 coax contacts. The fourth interface, power meter recorder, is mapped to a coax contact.

A.5 Power loads

A.5.1 Hi current ac/dc load (Table A.27)

Two high current power loads are mapped to 8 power pins to support the high current path. Each of the high current loads has 2 Load (+) pins and 2 Load (–) pins.

A.5.2 AC/DC load (Table A.28)

Six power loads are mapped to 12 power pins. Each of the current loads has a Load (+) pin and Load (–) pin.

A.5.3 Load modulation (Table A.29)

A load modulation channel is mapped to 2 pins as Load Mod (+) and Load Mod (–). Load modulation allows a signal to vary the load about a programmed nominal value. (This applies to active loads only.)

A.6 Power supplies

A.6.1 DC

A.6.1.1 High current DCPS (Table A.30)

Ten high current DCPS are mapped to 40 power pins to support the current path. Each of the high current supplies has 2 DCPS (+) pins and 2 DCPS (–) pins.

A.6.1.2 DCPS (Table A.31)

Twelve DCPS are mapped to 24 power pins. Each of the supplies has a DCPS (+) pin and a DCPS (–) pin.

A.6.2 AC

A.6.2.1 AC power supply (ACPS) three phase (Table A.32)

A three-phase source is mapped to 10 power pins. Phases A, B, and C, plus neutral and ground are mapped to 2 pins each to support the high current paths.

A.6.2.2 ACPS programmable (Table A.33)

Four programmable ac sources are mapped to 10 power pins. Each source has a complementary return. Two pins are mapped as ground. Four auxiliary power sources are mapped to 8 signal pins. Each source has a complementary return.

A.7 Sense and control, DCPS, and loads

A.7.1 DCPS sense (Table A.34)

Forty-four pins are mapped as sense lines for the 11 DCPS. Sense lines are paired as DCPS Sense (+) and DCPS Sense (–).

A.7.2 ACPS sense (Table A.35)

Eight pins are mapped as sense lines for the 4 programmable ac sources.

A.7.3 Load sense (Table A.36)

Two pins are mapped as sense lines for one of the high power loads: High Power Load Sense (+) and High Power Load Sense (–). Two additional pins are mapped as *chassis* ground.

A.7.4 28V Control (Table A.37)

Two pins are mapped as control lines. Control 28 (+) and Control 28 (–) are inputs to the system to command a DCPS to the turn on.

A.8 Switch

Three types of switches are mapped: coax, power, and signal.

NOTE—The selection of the matrix switches was mapped to meet legacy requirements. A system integrator can choose to populate a system with, for example, 2x8 switches that meet the recommend attributes vice 1x4 switches, wire them to the CTI and still be compliant, as long as the superset contains the required subset.

A.8.1 Coax switch (CSW)

Two types of CSWs are mapped: 1x4 and 1x2.

A.8.1.1 1x8

1x8 CSWs can be created from 1x4 and 1x2 by appropriate wiring in an ITA/ID or transition adapter.

A.8.1.2 1x4 (Table A.38)

Forty-eight 1x4 CSWs are mapped to 240 coax contacts.

A.8.1.3 1x2 (Table A.39)

Nine 1x2 CSWs are mapped to 27 coax contacts.

A.8.2 Power switch

Four types of power switches are mapped: 1x4, 1x2, DPDT, and 1x1.

A.8.2.1 1x4 (Table A.40)

Six 1x4 switches are mapped to 30 power pins. These are 20 A relays, however the CTI interface has a thermal restriction of 18 A in a cluster of 6 adjacent pins. Five of the six are low-R.

A.8.2.2 1x2 (Table A.41)

Twenty-one 1x2 switches are mapped to 55 power pins. One is 20 A and twenty are 10 A. The 20 A is low-R, and 12 of the 10 A are low-R.

A.8.2.3 DPDT (Table A.42)

Two double-pole-double-throw (DPDT), 20 A low-R relays are mapped to 12 power pins.

CAUTION The CTI interface has a thermal restriction of 18 A in a cluster of 6 adjacent pins.

A.8.2.4 1x1 (Table A.43)

Twelve 1x1, 10 A switches are mapped to 24 power pins.

A.8.3 Signal switch

Four types of signal switches are mapped: 1x8, 8x24, 1x4, and 1x2.

A.8.3.1 1x8 (Table A.44)

Two hundred and eighty-eight (288) pins are mapped to support 16 2-wire, 1x8 matrices.

A.8.3.2 8x24 (Table A.45)

Three hundred and twelve (312) pins are mapped to support 6 8x24 matrices. A return pin is mapped for each of the inputs. A return pin is mapped for every two outputs.

A.8.3.3 1x4 (Table A.46)

Sixteen 1x4 switches are mapped to 80 signal pins.

A.8.3.4 1x2 (Table A.47)

One hundred 1x2 switches are mapped to 300 signal pins. Fifty are 4 A and the remaining 50 are 2 A.

A.9 System

A.9.1 ETE GND (Table A.48)

Three pins have been mapped for engineering test and evaluation (ETE) grounds. The objective is to make ground pins available to support system trouble-shooting and ETE.

A.9.2 Frequency standard (Table A.49)

Two frequency standards are mapped to 2 coax contacts: 10 MHz and 100 MHz.

A.9.3 System trigger (Table A.50)

Four system interfaces are mapped: PH MOD IN, STA Sys Ext Input, STA Sys Trig A, and STA Sys Trig B+. These 4 interfaces are mapped with their respective returns to 8 pins to support a 2-wire interface for each.

Three system interfaces are mapped: STA Sys Trig A, STA Sys Trig B, and STA Sys Ext Input. STA Sys Trig A and STA Sys Trig B are mapped as twisted shielded pairs to 6 pins. STA Sys Ext Input is mapped with a respective shield to 2 pins.

A.9.4 Interrupts, interlocks, and shutdown (Table A.51)

Ten UUT interrupts and 2 UUT interrupt return pins are mapped. A UUT interlock and its return are mapped. An ID interlock and its return are mapped in each of the 4 physical partitions of the interface. A UUT shutdown and its return are mapped. Two interlock pins were added for transition adapter handle closures, bringing the total to 18 pins. Nine system identification pins are also mapped.

A.9.5 Safety ground (Table A.52)

Two power pins are mapped as safety ground. These paths can be tied together to serve as a single point ground.

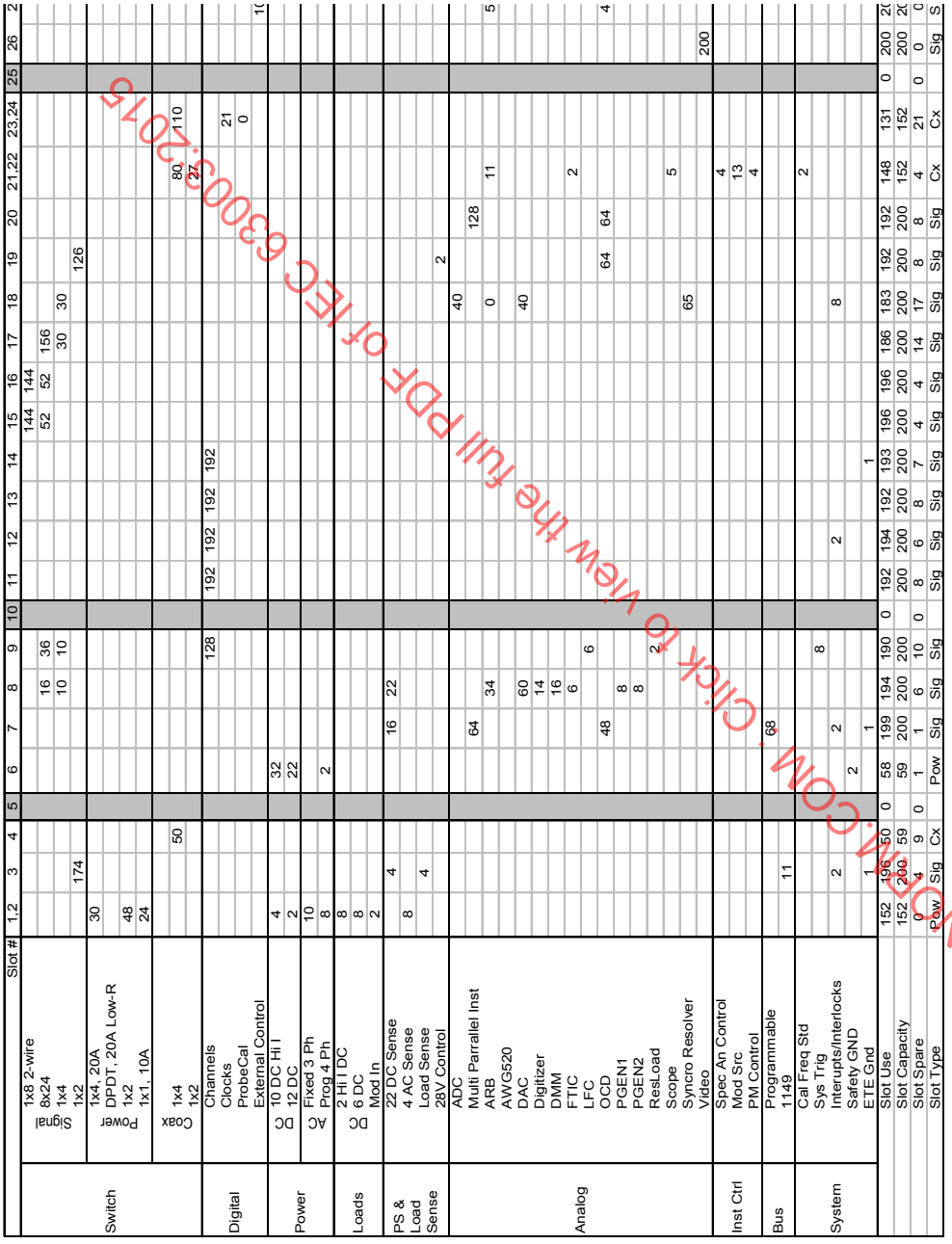

Figure A.1—Summary pin map

200 Pin Block			
A	B	C	D
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16
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21	21	21	21
22	22	22	22
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25	25	25	25
26	26	26	26
27	27	27	27
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39	39	39	39
40	40	40	40
41	41	41	41
42	42	42	42
43	43	43	43
44	44	44	44
45	45	45	45
46	46	46	46
47	47	47	47
48	48	48	48
49	49	49	49
50	50	50	50

152 Pin Block							
A	B	C	D	E	F	G	H
1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6
7	7	7	7	7	7	7	7
8	8	8	8	8	8	8	8
9	9	9	9	9	9	9	9
10	10	10	10	10	10	10	10
11	11	11	11	11	11	11	11
12	12	12	12	12	12	12	12
13	13	13	13	13	13	13	13
14	14	14	14	14	14	14	14
15	15	15	15	15	15	15	15
16	16	16	16	16	16	16	16
17	17	17	17	17	17	17	17
18	18	18	18	18	18	18	18
19	19	19	19	19	19	19	19

59 Pin Block		
A	B	C
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
19	19	19
20		20

Figure A.2—Connector configurations

Table A.1—ADC analog in

CTI name	Legacy system	Recommended attributes	Slot	Pin
ADC CH 1 (+)	SAMe, IAIS, C17	Max voltage: ± 40 V Max impedance: 10 MΩ Max sample rate 100 kilosample/s Max BW: 80 kHz	18	A 41
ADC CH 1 (–)	“	“	18	B 41
ADC CH 2 (+)	“	“	18	B 42
ADC CH 2 (–)	“	“	18	A 42
ADC CH 3 (+)	“	“	18	A 43
ADC CH 3 (–)	“	“	18	B 43
ADC CH 4 (+)	“	“	18	B 44
ADC CH 4 (–)	“	“	18	A 44
ADC CH 5 (+)	“	“	18	A 45
ADC CH 5 (–)	“	“	18	B 45
ADC CH 6 (+)	“	“	18	B 46
ADC CH 6 (–)	“	“	18	A 46
ADC CH 7 (+)	“	“	18	A 47
ADC CH 7 (–)	“	“	18	B 47
ADC CH 8 (+)	“	“	18	B 48
ADC CH 8 (–)	“	“	18	A 48
ADC CH 9 (+)	“	“	18	A 49
ADC CH 9 (–)	“	“	18	B 49
ADC CH 10 (+)	SAMe, IAIS	“	18	B 50
ADC CH 10 (–)	“	“	18	A 50
ADC CH 11 (+)	“	“	18	C 41
ADC CH 11 (–)	“	“	18	D 41
ADC CH 12 (+)	“	“	18	D 42
ADC CH 12 (–)	“	“	18	C 42
ADC CH 13 (+)	“	“	18	C 43
ADC CH 13 (–)	“	“	18	D 43
ADC CH 14 (+)	“	“	18	D 44
ADC CH 14 (–)	“	“	18	C 44
ADC CH 15 (+)	“	“	18	C 45
ADC CH 15 (–)	“	“	18	D 45
ADC CH 16 (+)	“	“	18	D 46
ADC CH 16 (–)	“	“	18	C 46
ADC Trigger In (+)	SAMe, IAIS, C17	Voltage: ± 10 V, 100 ns minimum trigger pulse width, 50 Ω input	18	C 47
ADC Trigger In (–)	SAMe, IAIS, C17	”	18	D 47
ADC Shield 1			18	D 48
ADC Shield 2			18	C 48
ADC Shield 3			18	C 49
ADC Shield 4			18	D 49
ADC Shield 5			18	D 50
ADC Shield 6			18	C 50

Table A.2—AI multi-parallel

CTI name	Legacy system	Recommended attributes	Slot	Pin
AI-Instr 1 CH 1 (+)	CASS, LM-STAR, C17	Max voltage: ± 200 V Max current: ± 100 mA Max freq: 25 MHz BW: 70 MHz (5 ns rise time)	7	A 17
AI-Instr 1 CH 1 (–)	“	“	7	B 17
AI-Instr 1 CH 2 (+)	“	“	7	B 18
AI-Instr 1 CH 2 (–)	“	“	7	A 18
AI-Instr 1 CH 3 (+)	“	“	7	A 19
AI-Instr 1 CH 3 (–)	“	“	7	B 19
AI-Instr 1 CH 4 (+)	“	“	7	B 20
AI-Instr 1 CH 4 (–)	“	“	7	A 20
AI-Instr 1 CH 5 (+)	“	“	7	A 21
AI-Instr 1 CH 5 (–)	“	“	7	B 21
AI-Instr 1 CH 6 (+)	“	“	7	B 22
AI-Instr 1 CH 6 (–)	“	“	7	A 22
AI-Instr 1 CH 7 (+)	CASS, LM-STAR, C17	“	7	A 23
AI-Instr 1 CH 7 (–)	“	“	7	B 23
AI-Instr 1 CH 8 (+)	“	“	7	B 24
AI-Instr 1 CH 8 (–)	“	“	7	A 24
AI-Instr 1 CH 9 (+)	“	“	7	A 25
AI-Instr 1 CH 9 (–)	“	“	7	B 25
AI-Instr 1 CH 10 (+)	“	“	7	B 26
AI-Instr 1 CH 10 (–)	“	“	7	A 26
AI-Instr 1 CH 11 (+)	“	“	7	A 27
AI-Instr 1 CH 11 (–)	“	“	7	B 27
AI-Instr 1 CH 12 (+)	“	“	7	B 28
AI-Instr 1 CH 12 (–)	“	“	7	A 28
AI-Instr 1 CH 13 (+)	“	“	7	A 29
AI-Instr 1 CH 13 (–)	“	“	7	B 29
AI-Instr 1 CH 14 (+)	“	“	7	B 30
AI-Instr 1 CH 14 (–)	“	“	7	A 30
AI-Instr 1 CH 15 (+)	“	“	7	A 31
AI-Instr 1 CH 15 (–)	“	“	7	B 31
AI-Instr 1 CH 16 (+)	“	“	7	B 32
AI-Instr 1 CH 16 (–)	“	“	7	A 32
AI-Instr 1 CH 17 (+)	“	“	7	C 17
AI-Instr 1 CH 17 (–)	“	“	7	D 17
AI-Instr 1 CH 18 (+)	“	“	7	D 18
AI-Instr 1 CH 18 (–)	“	“	7	C 18
AI-Instr 1 CH 19 (+)	“	“	7	C 19
AI-Instr 1 CH 19 (–)	“	“	7	D 19
AI-Instr 1 CH 20 (+)	“	“	7	D 20
AI-Instr 1 CH 20 (–)	“	“	7	C 20
AI-Instr 1 CH 21 (+)	“	“	7	C 21
AI-Instr 1 CH 21 (–)	“	“	7	D 21
AI-Instr 1 CH 22 (+)	“	“	7	D 22
AI-Instr 1 CH 22 (–)	“	“	7	C 22
AI-Instr 1 CH 23 (+)	“	“	7	C 23
AI-Instr 1 CH 23 (–)	“	“	7	D 23
AI-Instr 1 CH 24 (+)	“	“	7	D 24
AI-Instr 1 CH 24 (–)	“	“	7	C 24
AI-Instr 1 CH 25 (+)	“	“	7	C 25
AI-Instr 1 CH 25 (–)	“	“	7	D 25
AI-Instr 1 CH 26 (+)	“	“	7	D 26

Table A.2—AI multi-parallel *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
AI-Instr 1 CH 26 (–)	“	“	7	C 26
AI-Instr 1 CH 27 (+)	“	“	7	C 27
AI-Instr 1 CH 27 (–)	“	“	7	D 27
AI-Instr 1 CH 28 (+)	“	“	7	D 28
AI-Instr 1 CH 28 (–)	“	“	7	C 28
AI-Instr 1 CH 29 (+)	“	“	7	C 29
AI-Instr 1 CH 29 (–)	“	“	7	D 29
AI-Instr 1 CH 30 (+)	“	“	7	D 30
AI-Instr 1 CH 30 (–)	“	“	7	C 30
AI-Instr 1 CH 31 (+)	“	“	7	C 31
AI-Instr 1 CH 31 (–)	“	“	7	D 31
AI-Instr 1 CH 32 (+)	“	“	7	D 32
AI-Instr 1 CH 32 (–)	“	“	7	C 32

Table A.3—AI multi-parallel No. 2

CTI name	Legacy system	Recommended attributes	Slot	Pin
AI-Instr 2 CH 1 (+)	CASS, LM-STAR, C17	Max voltage: ± 200 V Max current: ±100 mA Max freq: 25 MHz BW: 70 MHz (5 ns rise time)	20	A 17
AI-Instr 2 CH 1 (–)	“	“	20	B 17
AI-Instr 2 CH 2 (+)	“	“	20	B 18
AI-Instr 2 CH 2 (–)	“	“	20	A 18
AI-Instr 2 CH 3 (+)	“	“	20	A 19
AI-Instr 2 CH 3 (–)	“	“	20	B 19
AI-Instr 2 CH 4 (+)	“	“	20	B 20
AI-Instr 2 CH 4 (–)	“	“	20	A 20
AI-Instr 2 CH 5 (+)	“	“	20	A 21
AI-Instr 2 CH 5 (–)	“	“	20	B 21
AI-Instr 2 CH 6 (+)	“	“	20	B 22
AI-Instr 2 CH 6 (–)	“	“	20	A 22
AI-Instr 2 CH 7 (+)	“	“	20	A 23
AI-Instr 2 CH 7 (–)	“	“	20	B 23
AI-Instr 2 CH 8 (+)	“	“	20	B 24
AI-Instr 2 CH 8 (–)	“	“	20	A 24
AI-Instr 2 CH 9 (+)	“	“	20	A 25
AI-Instr 2 CH 9 (–)	“	“	20	B 25
AI-Instr 2 CH 10 (+)	“	“	20	B 26
AI-Instr 2 CH 10 (–)	“	“	20	A 26
AI-Instr 2 CH 11 (+)	“	“	20	A 27
AI-Instr 2 CH 11 (–)	“	“	20	B 27
AI-Instr 2 CH 12 (+)	“	“	20	B 28
AI-Instr 2 CH 12 (–)	“	“	20	A 28
AI-Instr 2 CH 13 (+)	“	“	20	A 29
AI-Instr 2 CH 13 (–)	“	“	20	B 29
AI-Instr 2 CH 14 (+)	“	“	20	B 30
AI-Instr 2 CH 14 (–)	“	“	20	A 30
AI-Instr 2 CH 15 (+)	“	“	20	A 31
AI-Instr 2 CH 15 (–)	“	“	20	B 31

Table A.3—AI multi-parallel No. 2 *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
AI-Instr 2 CH 16 (+)	“	“	20	B 32
AI-Instr 2 CH 16 (–)	“	“	20	A 32
AI-Instr 2 CH 17 (+)	“	“	20	A 33
AI-Instr 2 CH 17 (–)	“	“	20	B 33
AI-Instr 2 CH 18 (+)	“	“	20	B 34
AI-Instr 2 CH 18 (–)	“	“	20	A 34
AI-Instr 2 CH 19 (+)	“	“	20	A 35
AI-Instr 2 CH 19 (–)	“	“	20	B 35
AI-Instr 2 CH 20 (+)	“	“	20	B 36
AI-Instr 2 CH 20 (–)	“	“	20	A 36
AI-Instr 2 CH 21 (+)	“	“	20	A 37
AI-Instr 2 CH 21 (–)	“	“	20	B 37
AI-Instr 2 CH 22 (+)	“	“	20	B 38
AI-Instr 2 CH 22 (–)	“	“	20	A 38
AI-Instr 2 CH 23 (+)	“	“	20	A 39
AI-Instr 2 CH 23 (–)	“	“	20	B 39
AI-Instr 2 CH 24 (+)	“	“	20	B 40
AI-Instr 2 CH 24 (–)	“	“	20	A 40
AI-Instr 2 CH 25 (+)	“	“	20	A 41
AI-Instr 2 CH 25 (–)	“	“	20	B 41
AI-Instr 2 CH 26 (+)	“	“	20	B 42
AI-Instr 2 CH 26 (–)	“	“	20	A 42
AI-Instr 2 CH 27 (+)	“	“	20	A 43
AI-Instr 2 CH 27 (–)	“	“	20	B 43
AI-Instr 2 CH 28 (+)	“	“	20	B 44
AI-Instr 2 CH 28 (–)	“	“	20	A 44
AI-Instr 2 CH 29 (+)	“	“	20	A 45
AI-Instr 2 CH 29 (–)	“	“	20	B 45
AI-Instr 2 CH 30 (+)	“	“	20	B 46
AI-Instr 2 CH 30 (–)	“	“	20	A 46
AI-Instr 2 CH 31 (+)	“	“	20	A 47
AI-Instr 2 CH 31 (–)	“	“	20	B 47
AI-Instr 2 CH 32 (+)	“	“	20	B 48
AI-Instr 2 CH 32 (–)	“	“	20	A 48

Table A.4—AI multi-parallel No. 3

CTI name	Legacy systems	Recommended attributes	Slot	Pin
AI-Instr 3 CH 1 (+)	CASS, LM-STAR	Max voltage: ± 200 V Max current: ± 100 mA Max freq: 25 MHz BW: 70 MHz (5 ns rise time)	20	C 17
AI-Instr 3 CH 1 (–)	“	“	20	D 17
AI-Instr 3 CH 2 (+)	“	“	20	D 18
AI-Instr 3 CH 2 (–)	“	“	20	C 18
AI-Instr 3 CH 3 (+)	“	“	20	C 19
AI-Instr 3 CH 3 (–)	“	“	20	D 19
AI-Instr 3 CH 4 (+)	“	“	20	D 20
AI-Instr 3 CH 4 (–)	“	“	20	C 20
AI-Instr 3 CH 5 (+)	“	“	20	C 21
AI-Instr 3 CH 5 (–)	“	“	20	D 21
AI-Instr 3 CH 6 (+)	“	“	20	D 22
AI-Instr 3 CH 6 (–)	“	“	20	C 22
AI-Instr 3 CH 7 (+)	“	“	20	C 23
AI-Instr 3 CH 7 (–)	“	“	20	D 23
AI-Instr 3 CH 8 (+)	“	“	20	D 24
AI-Instr 3 CH 8 (–)	“	“	20	C 24
AI-Instr 3 CH 9 (+)	“	“	20	C 25
AI-Instr 3 CH 9 (–)	“	“	20	D 25
AI-Instr 3 CH 10 (+)	“	“	20	D 26
AI-Instr 3 CH 10 (–)	“	“	20	C 26
AI-Instr 3 CH 11 (+)	“	“	20	C 27
AI-Instr 3 CH 11 (–)	“	“	20	D 27
AI-Instr 3 CH 12 (+)	“	“	20	D 28
AI-Instr 3 CH 12 (–)	“	“	20	C 28
AI-Instr 3 CH 13 (+)	“	“	20	C 29
AI-Instr 3 CH 13 (–)	“	“	20	D 29
AI-Instr 3 CH 14 (+)	“	“	20	D 30
AI-Instr 3 CH 14 (–)	“	“	20	C 30
AI-Instr 3 CH 15 (+)	“	“	20	C 31
AI-Instr 3 CH 15 (–)	“	“	20	D 31
AI-Instr 3 CH 16 (+)	“	“	20	D 32
AI-Instr 3 CH 16 (–)	“	“	20	C 32
AI-Instr 3 CH 17 (+)	“	“	20	C 33
AI-Instr 3 CH 17 (–)	“	“	20	D 33
AI-Instr 3 CH 18 (+)	“	“	20	D 34
AI-Instr 3 CH 18 (–)	“	“	20	C 34
AI-Instr 3 CH 19 (+)	“	“	20	C 35
AI-Instr 3 CH 19 (–)	“	“	20	D 35
AI-Instr 3 CH 20 (+)	“	“	20	D 36
AI-Instr 3 CH 20 (–)	“	“	20	C 36
AI-Instr 3 CH 21 (+)	“	“	20	C 37
AI-Instr 3 CH 21 (–)	“	“	20	D 37
AI-Instr 3 CH 22 (+)	“	“	20	D 38
AI-Instr 3 CH 22 (–)	“	“	20	C 38
AI-Instr 3 CH 23 (+)	“	“	20	C 39
AI-Instr 3 CH 23 (–)	“	“	20	D 39
AI-Instr 3 CH 24 (+)	“	“	20	D 40
AI-Instr 3 CH 24 (–)	“	“	20	C 40
AI-Instr 3 CH 25 (+)	“	“	20	C 41
AI-Instr 3 CH 25 (–)	“	“	20	D 41
AI-Instr 3 CH 26 (+)	“	“	20	D 42
AI-Instr 3 CH 26 (–)	“	“	20	C 42

Table A.4—AI multi-parallel No. 3 (*continued*)

CTI name	Legacy systems	Recommended attributes	Slot	Pin
AI-Instr 3 CH 27 (+)	“	“	20	C 43
AI-Instr 3 CH 27 (–)	“	“	20	D 43
AI-Instr 3 CH 28 (+)	“	“	20	D 44
AI-Instr 3 CH 28 (–)	“	“	20	C 44
AI-Instr 3 CH 29 (+)	“	“	20	C 45
AI-Instr 3 CH 29 (–)	“	“	20	D 45
AI-Instr 3 CH 30 (+)	“	“	20	D 46
AI-Instr 3 CH 30 (–)	“	“	20	C 46
AI-Instr 3 CH 31 (+)	“	“	20	C 47
AI-Instr 3 CH 31 (–)	“	“	20	D 47
AI-Instr 3 CH 32 (+)	“	“	20	D 48
AI-Instr 3 CH 32 (–)	“	“	20	C 48

Table A.5—AWG

CTI name	Legacy system	Recommended attributes	Slot	Pin
AWG1 CHA	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	Max voltage: ± 6 V Max freq. 25 MHz Impedance: 50 Ω Current: 1 A Min pulse width: 15 ns	8	B 12
AWG1 Shield	“		8	A 12
AWG1 EXT TRIG	“	Max voltage: ± 8 V Max freq. 645 kHz Impedance: 50 Ω Current: 1 A Min pulse width: 10 ns	8	A 13
AWG1 Shield	“		8	B 13
AWG1 CHB	IFTE, CASS, LM-STAR, ESTS, IAIS	Max voltage: ± 6 V Max freq. 6 MHz Impedance: 50 Ω Current: 1 A Min pulse width: 15 ns	8	B 14
AWG1 Shield	“		8	A 14
AWG1 EXT SYNC	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	Max voltage: 0 to +5.5 V Max freq. 25MHz Impedance: 50 Ω Current: 1 A Min pulse width: 10 ns	8	A 15
AWG1 Shield	“		8	B 15
AWG1 MRK SYNC (AM Input)	LM-STAR, ESTS, IAIS, C17	Max voltage: 0 to +5.5 V Max freq: 25 MHz Impedance: 50 Ω Current: 1 A	8	B 16
AWG1 Shield	“		8	A 16

Table A.5—AWG *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
AWG2 MRK SYNC	LM-STAR, IAIS, C17	Max voltage: 0 to +5.5 V Max freq: 25 MHz Impedance: 50 Ω Current: 1 A	8	A 19
AWG2 Shield	“		8	B 19
AWG2 CHA	IFTE, LM-STAR, TETS, IAIS, C17, RAF	Max voltage: ± 6 V Max freq. 25 MHz Impedance: 50 Ω Current: 1 A	8	B 20
AWG2 Shield	“		8	C 12
AWG2 CHB	IFTE, LM-STAR, IAIS	Max voltage: ± 6 V Max freq. 6 MHz Impedance: 50 Ω Current: 1 A	8	C 13
AWG2 Shield	“		8	D 13
AWG2 EXT SYNC	IFTE, LM-STAR, ESTS, IAIS, C17, RAF	Max voltage: 0 to + 5.5 V Max freq. 25 MHz Impedance: 50 Ω Current: 1 A Min Pulse width: 10 ns	8	D 14
AWG2 Shield	“		8	C 14
AWG3 CHA	RAF	Max voltage: ± 6 V Max freq. 25 MHz Impedance: 50 Ω Current: 1 A	8	C 15
AWG3 Shield	“		8	D 15
AWG3 EXT TRIG	IFTE, TETS, RAF	Max voltage: ± 8 V Max freq. 160 MHz Impedance: 50 Ω Current: 1 A Min pulse width: 10 ns	8	D 16
AWG3 Shield	“		8	C 16
AWG3 EXT SYNC	IFTE, TETS, RAF	Max voltage: 0 to 5.5 V Max freq. 25 MHz Impedance: 50 Ω Current: 1 A	8	C 17
AWG3 Shield	“		8	D 17
AWG4 CHA	IFTE, RAF	Max voltage: ± 6 V Max freq. 25 MHz Impedance: 50 Ω Current: 1 A	8	D 18
AWG4 Shield	“		8	C 18
AWG4 EXT Trigger	“	Max voltage: ± 8 V Max freq. 160 MHz Impedance: 50 Ω Current: 1 A Min pulse width: 10 ns	8	C 19
AWG4 Shield	“		8	D 19
FGEN FG_Clock	TETS	Voltage range: 0.01 to 16 Vpp Max freq: 100 MHz Impedance: 50 Ω	21,22	D 18
FGEN FG_PM	“	“	21,22	D 19
AWG1 Dig Out 1 (+)	CASS, LM-STAR	Max voltage: Diff ECL Max freq: 100 MPPS	27	A 39

Table A.5—AWG *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
AWG1 Dig Out 1 (–)	“	“	27	B 39
AWG1 Dig Out 2 (+)	“	“	27	B 40
AWG1 Dig Out 2 (–)	“	“	27	A 40
AWG1 Dig Out 3 (+)	“	“	27	A 41
AWG1 Dig Out 3 (–)	“	“	27	B 41
AWG1 Dig Out 4 (+)	“	“	27	B 42
AWG1 Dig Out 4 (–)	“	“	27	A 42
AWG1 Dig Out 5 (+)	“	“	27	A 43
AWG1 Dig Out 5 (–)	“	“	27	B 43
AWG1 Dig Out 6 (+)	“	“	27	B 44
AWG1 Dig Out 6 (–)	“	“	27	A 44
AWG1 Dig Out 7 (+)	“	“	27	A 45
AWG1 Dig Out 7 (–)	“	“	27	B 45
AWG1 Dig Out 8 (+)	“	“	27	B 46
AWG1 Dig Out 8 (–)	“	“	27	A 46
AWG1 Dig Out 9 (+)	“	“	27	A 47
AWG1 Dig Out 9 (–)	“	“	27	B 47
AWG1 Dig Out 10 (+)	“	“	27	B 48
AWG1 Dig Out 10 (–)	“	“	27	A 48
AWG1 Dig Out 11 (+)	“	“	27	A 49
AWG1 Dig Out 11 (–)	“	“	27	B 49
AWG1 Dig Out 12 (+)	“	“	27	B 50
AWG1 Dig Out 12 (–)	“	“	27	A 50
AWG2 Dig Out 1 (+)	“	“	27	C 39
AWG2 Dig Out 1 (–)	“	“	27	D 39
AWG2 Dig Out 2 (+)	“	“	27	D 40
AWG2 Dig Out 2 (–)	“	“	27	C 40
AWG2 Dig Out 3 (+)	“	“	27	C 41
AWG2 Dig Out 3 (–)	“	“	27	D 41
AWG2 Dig Out 4 (+)	“	“	27	D 42
AWG2 Dig Out 4 (–)	“	“	27	C 42
AWG2 Dig Out 5 (+)	“	“	27	C 43
AWG2 Dig Out 5 (–)	“	“	27	D 43
AWG2 Dig Out 6 (+)	“	“	27	D 44
AWG2 Dig Out 6 (–)	“	“	27	C 44
AWG2 Dig Out 7 (+)	“	“	27	C 45
AWG2 Dig Out 7 (–)	“	“	27	D 45
AWG2 Dig Out 8 (+)	“	“	27	D 46
AWG2 Dig Out 8 (–)	“	“	27	C 46
AWG2 Dig Out 9 (+)	“	“	27	C 47
AWG2 Dig Out 9 (–)	“	“	27	D 47
AWG2 Dig Out 10 (+)	“	“	27	D 48
AWG2 Dig Out 10 (–)	“	“	27	C 48
AWG2 Dig Out 11 (+)	“	“	27	C 49
AWG2 Dig Out 11 (–)	“	“	27	D 49
AWG2 Dig Out 12 (+)	“	“	27	D 50
AWG2 Dig Out 12 (–)	“	“	27	C 50
AWG1 Dig Out GND	“	“	27	C 38
AWG2 Dig Out GND	“	“	27	D 38
AWG1 DIFFGATEH	LM-STAR	Differential TTL 30 ns pulse width (min)	8	A 17
AWG1 DIFFGATEL	“	See above	8	B 17
AWG1 DATAGATEH	“	See above	8	B 18
AWG1 DATAGATEL	“	See above	8	A 18

Table A.5—AWG *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
FGEN FG_Trig	TETS	TTL	21,22	E 17
FGEN FG_Sync	IFTE	Voltage range: 0.01 to 16 Vpp Max freq: 100 MHz Impedance: 50 Ω	21,22	E 18
FGEN FG_Out	TETS	Voltage range: 0.01 to 16 Vpp Max freq: 50 MHz Impedance: 50 Ω	21,22	E 19
AWG-OUT/7 (Output of AWG divided by 7)	TETS	Voltage: 5 V Max freq: 100 MHz Impedance: 50 Ω	21,22	A 18
AWG-MARKER	TETS	Voltage 0 – 2.5V Impedance: 50 Ω	21,22	A 19
AWG-REF	TETS	Voltage: 5 V Max freq: 100 MHz Impedance: 50 Ω	21,22	B 18
AWG-STARTARM	TETS	Max freq: 20 MHz TTL level	21,22	B 19
AWG-STOPTRIGFSK	TETS	Voltage: 5 V Max freq: 100 MHz Impedance: 50 Ω	21,22	C 18
AWG-OUT	TETS	Voltage: 1 Vpp Max freq: 10MHz Impedance: 50 Ω to 75 Ω	21,22	C 19

Table A.6—AWG520

CTI name	Legacy system	Recommended attributes	Slot	Pin
AWG520 OutPut 1	LM-STAR	0.020 Vpp to 2 Vpp into 50 Ω 1.000 Hz to 100.0 MHz Sine, triangle, square, ramp, pulse, or dc	28	A 17
AWG520 Shield	“	“	28	B 17
AWG520 Output 2	“	“	28	B 18
AWG520 Shield	“	“	28	A 18
AWG520 MarkerOut 1	“	Max voltage: 2 V BW: 700 MHz (rise time 0.5 ns @ ± 0.5 V)	28	A 19
AWG520 Shield	“	“	28	B 19
AWG520 MarkerOut 2	“	“	28	B 20
AWG520 Shield	“	“	28	A 20
AWG520 MarkerOut 3	“	“	28	A 21
AWG520 Shield	“	“	28	B 21
AWG520 MarkerOut 4	“	“	28	B 22
AWG520 Shield	“	“	28	A 22
AWG520 DigOut 0	“	Max voltage: ± 8 V BW: 700 MHz	28	A 23
AWG520 Shield	“	“	28	B 23
AWG520 DigOut 1	“	“	28	B 24
AWG520 Shield	“	“	28	A 24
AWG520 DigOut 2	“	“	28	A 25
AWG520 Shield	“	“	28	B 25
AWG520 DigOut 3	“	“	28	B 26
AWG520 Shield	“	“	28	A 26
AWG520 DigOut 4	“	“	28	A 27
AWG520 Shield	“	“	28	B 27
AWG520 DigOut 5	“	“	28	B 28
AWG520 Shield	“	“	28	A 28
AWG520 DigOut 6	“	“	28	A 29
AWG520 Shield	“	“	28	B 29
AWG520 DigOut 7	“	“	28	C 17
AWG520 Shield	“	“	28	D 17
AWG520 DigOut 8	“	“	28	D 18
AWG520 Shield	“	“	28	C 18
AWG520 DigOut 9	“	“	28	C 19
AWG520 Shield	“	“	28	D 19
AWG520 Trig_In	“	Input impedance: 1 kΩ or 50 Ω Max voltage: ± 10 V Min pulse width: 10 ns	28	D 20
AWG520 Shield	“		28	C 20
AWG520 Event Trig1	“	Max voltage: 5 V	28	C 21
AWG520 Shield	“	“	28	D 21
AWG520 Event Trig2	“	“	28	D 22
AWG520 Shield	“	“	28	C 22
AWG520 Event Trig3	“	“	28	C 23
AWG520 Shield	“	“	28	D 23
AWG520 Event Trig4	“	“	28	D 24

Table A.6—AWG520 *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
AWG520 Shield	"	"	28	C 24
AWG520 Clock in	"	Impedance: 50 Ω Max voltage: ± 10 V Freq: 900 MHz	28	C 25
AWG520 Shield	"	"	28	D 25
AWG520 Noise gen	"	Range: –145 dBm/Hz to –105 dBm/Hz @ 100 K reference Freq: 300 MHz	28	D 26
AWG520 Shield	"	"	28	C 26
AWG520 Clock out	"	Level: ECL 100 K compatible	28	C 27
AWG520 Shield	"	"	28	D 27
Logic Analyser (LA)_trig_in	LM-STAR	Trigger in arms logic analyzer. 15 ns typical delay TTL	28	D 28
LA_trig_shd	"	"	28	C 28
LA_trig_out	"	Trigger to trigger out. 150 ns typical delay TTL	28	C 29
LA_trig_shd	"	"	28	D 29

Table A.7—DAC analog out

CTI name	Legacy systems	Recommended attributes	Slot	Pin
DAC1 CH 1 (+)	IFTE, SAMe, ESTS, IAIS, RAF	Max voltage: ± 20V Max current: ± 50 mA Max freq: 100 MHz	8	A 21
DAC1 CH 1 (–)	"	"	8	B 21
DAC1 CH 2 (+)	"	"	8	B 22
DAC1 CH 2 (–)	"	"	8	A 22
DAC1 CH 3 (+)	"	"	8	A 23
DAC1 CH 3 (–)	"	"	8	B 23
DAC1 CH 4 (+)	"	"	8	B 24
DAC1 CH 4 (–)	"	"	8	A 24
DAC1 CH 5 (+)	IFTE, SAMe, ESTS, IAIS	"	8	A 25
DAC1 CH 5 (–)	"	"	8	B 25
DAC1 CH 6 (+)	"	"	8	B 26
DAC1 CH 6 (–)	"	"	8	A 26
DAC1 CH 7 (+)	"	"	8	A 27
DAC1 CH 7 (–)	"	"	8	B 27
DAC1 CH 8 (+)	"	"	8	B 28
DAC1 CH 8 (–)	"	"	8	A 28
DAC1 CH 9 (+)	SAMe, ESTS, IAIS	"	8	A 29
DAC1 CH 9 (–)	"	"	8	B 29
DAC1 CH 10 (+)	"	"	8	B 30
DAC1 CH 10 (–)	"	"	8	A 30
DAC1 CH 11 (+)	"	"	8	A 31
DAC1 CH 11 (–)	"	"	8	B 31
DAC1 CH 12 (+)	"	"	8	B 32

Table A.7—DAC analog out *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
DAC1 CH 12 (–)	"	"	8	A 32
DAC1 CH 13 (+)	SAMe, IAIS	"	8	A 33
DAC1 CH 13 (–)	"	"	8	B 33
DAC1 CH 14 (+)	"	"	8	B 34
DAC1 CH 14 (–)	"	"	8	A 34
DAC1 CH 15 (+)	"	"	8	C 21
DAC1 CH 15 (–)	"	"	8	D 21
DAC1 CH 16 (+)	"	"	8	D 22
DAC1 CH 16 (–)	"	"	8	C 22
DAC1 Trig_In (+)	"	Min trigger pulse: 100 ns Trigger input: 50 Ω Voltage: TTL	8	C 23
DAC1 Trig_In (–)	"	"	8	D 23
DAC1 Sense CH 1 (+)	ESTS, RAF	Max voltage: ± 20V Max current: ± 50 mA Max freq: 100 MHz	8	D 24
DAC1 Sense CH 1 (–)	"	"	8	C 24
DAC1 Sense CH 2 (+)	"	"	8	C 25
DAC1 Sense CH 2 (–)	"	"	8	D 25
DAC1 Sense CH 3 (+)	"	"	8	D 26
DAC1 Sense CH 3 (–)	"	"	8	C 26
DAC1 Sense CH 4 (+)	"	"	8	C 27
DAC1 Sense CH 4 (–)	"	"	8	D 27
DAC1 Sense CH 5 (+)	ESTS	"	8	D 28
DAC1 Sense CH 5 (–)	"	"	8	C 28
DAC1 Sense CH 6 (+)	"	"	8	C 29
DAC1 Sense CH 6 (–)	"	"	8	D 29
DAC1 Sense CH 7 (+)	"	"	8	D 30
DAC1 Sense CH 7 (–)	"	"	8	C 30
DAC1 Sense CH 8 (+)	"	"	8	C 31
DAC1 Sense CH 8 (–)	"	"	8	D 31
DAC1 Sense CH 9 (+)	"	"	8	D 32
DAC1 Sense CH 9 (–)	"	"	8	C 32
DAC1 Sense CH 10 (+)	"	"	8	C 33
DAC1 Sense CH 10 (–)	"	"	8	D 33
DAC1 Sense CH 11 (+)	"	"	8	D 34
DAC1 Sense CH 11 (–)	"	"	8	C 34
DAC1 Sense CH 12 (+)	"	"	8	C 35
DAC1 Sense CH 12 (–)	"	"	8	D 35
DAC1 Shield 1	"	N/A	8	A 35
DAC1 Shield 2	"	N/A	8	B 35
DAC1 Key 1 (+)	IFTE, SAMe, IAIS	Voltage level: TTL Min pulse width: 8 µs	28	B 30
DAC1 Key 1 (–)	"	"	28	A 30
DAC1 Key 2 (+)	"	"	28	A 31
DAC1 Key 2 (–)	"	"	28	B 31
DAC1 Key 3 (+)	"	"	28	B 32
DAC1 Key 3 (–)	"	"	28	A 32
DAC1 Key 4 (+)	"	"	28	A 33
DAC1 Key 4 (–)	"	"	28	B 33
DAC1 Key 5 (+)	"	"	28	D 30

Table A.7—DAC analog out *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
DAC1 Key 5 (–)	“	“	28	C 30
DAC1 Key 6 (+)	“	“	28	C 31
DAC1 Key 6 (–)	“	“	28	D 31
DAC1 Key 7 (+)	“	“	28	D 32
DAC1 Key 7 (–)	“	“	28	C 32
DAC1 Key 8 (+)	“	“	28	C 33
DAC1 Key 8 (–)	“	“	28	D 33
DAC2 CH 1 (+)	SAMe, IAIS	Max voltage: ± 20V Max current: ± 50 mA Max freq: 100 MHz	18	C 1
DAC2 CH 1 (–)	“	“	18	D 1
DAC2 CH 2 (+)	“	“	18	D 2
DAC2 CH 2 (–)	“	“	18	C 2
DAC2 CH 3 (+)	“	“	18	C 3
DAC2 CH 3 (–)	“	“	18	D 3
DAC2 CH 4 (+)	“	“	18	D 4
DAC2 CH 4 (–)	“	“	18	C 4
DAC2 CH 5 (+)	“	“	18	C 5
DAC2 CH 5 (–)	“	“	18	D 5
DAC2 CH 6 (+)	“	“	18	D 6
DAC2 CH 6 (–)	“	“	18	C 6
DAC2 CH 7 (+)	“	“	18	C 7
DAC2 CH 7 (–)	“	“	18	D 7
DAC2 CH 8 (+)	“	“	18	D 8
DAC2 CH 8 (–)	“	“	18	C 8
DAC2 CH 9 (+)	“	“	18	C 9
DAC2 CH 9 (–)	“	“	18	D 9
DAC2 CH 10 (+)	“	“	18	D 10
DAC2 CH 10 (–)	“	“	18	C 10
DAC2 CH 11 (+)	“	“	18	C 11
DAC2 CH 11 (–)	“	“	18	D 11
DAC2 CH 12 (+)	“	“	18	D 12
DAC2 CH 12 (–)	“	“	18	C 12
DAC2 CH 13 (+)	“	“	18	C 13
DAC2 CH 13 (–)	“	“	18	D 13
DAC2 CH 14 (+)	“	“	18	D 14
DAC2 CH 14 (–)	“	“	18	C 14
DAC2 CH 15 (+)	“	“	18	C 15
DAC2 CH 15 (–)	“	“	18	D 15
DAC2 CH 16 (+)	“	“	18	D 16
DAC2 CH 16 (–)	“	“	18	C 16
DAC2 Trig_In (+)	“	Min trigger pulse: 100 ns Trigger input: 50 Ω Voltage: TTL	18	C 17
DAC2 Trig_In (–)	“	“	18	D 17
DAC2 Shield 1	“	“	18	D 18
DAC2 Shield 2	“	“	18	C 18
DAC2 Shield 3	“	“	18	C 19
DAC2 Shield 4	“	“	18	D 19
DAC2 Shield 5	“	“	18	D 20
DAC2 Shield 6	“	“	18	C 20

Table A.8—Digitizer

CTI name	Legacy system	Recommended attributes	Slot	Pin
Digitizer Probe A	IFTE, CASS,TETS	Max voltage: 250 V max Max current 140 mA Max freq: 500 MHz @ 50 Ω	8	D 36
Digitizer Shield	"	"	8	C 36
Digitizer Probe B	IFTE, CASS	"	8	C 37
Digitizer Shield	"	"	8	D 37
Digitizer Ext Trigger	IFTE, TETS, RAF	"	8	D 38
Digitizer Shield	"	"	8	C 38
Digitizer TRIG OUT	ESTS, TETS, RAF	"	8	D 40
Digitizer Shield	"	"	8	C 40
Digitizer dc CAL	CASS	"	8	C 39
Digitizer Shield	"	"	8	D 39
Digitizer Wavfm Digtzr ChA	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, RAF	Max voltage: 250 V max Max current 140 mA Max freq: 500 MHz @ 50 Ω	8	C 41
Digitizer Shield	"	"	8	D 41
Digitizer Wavfm Digtzr ChB	"	"	8	D 42
Digitizer Shield	"	"	8	C 42

Table A.9—DMM

CTI name	Legacy systems	Recommended attributes	Slot	Pin
DMM HI	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	Max voltage: ± 300V Max freq: 100 kHz Max current: 3A	8	A 41
DMM HI Shield	IFTE, CASS, ESTS, TETS, C17	"	8	B 41
DMM LO	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	"	8	B 42
DMM LO Shield	IFTE, CASS, ESTS, TETS, C17	"	8	A 42
DMM S(+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	"	8	A 43
DMM S(+) Shield	IFTE, CASS, ESTS, TETS, C17	"	8	B 43
DMM S(–)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	"	8	B 44
DMM S(–) Shield	IFTE, CASS, ESTS, TETS, C17	"	8	A 44
DMM GUARD	CASS, LM-STAR, TEST, IAIS, C17	"	8	A 48
DMM CURRENT	CASS, LM-STAR, TEST, IAIS, RAF	"	8	B 48
DMM TRIG	ESTS, TETS, C17, RAF	Impedance: 1 MΩ	8	A 45
DMM TRIG shd	"	Impedance 1 MΩ	8	B 45
DMM Probe (+)	CASS, C17	Impedance 1 MΩ	8	B 46
DMM Probe (–)	CASS, C17	Impedance 1 MΩ	8	A 46
DMM DMM Done (+)	TETS, RAF	TTL Impedance: 1 MΩ	8	A 47
DMM DMM Done (–)	TETS	TTL Impedance: 1 MΩ	8	B 47

Table A.10—Frequency interval counter and RF counter

CTI name	Legacy systems	Recommended attributes	Slot	Pin
FTIC CH A	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	Max voltage ± 10 V Max freq: 220 MHz Impedance: 50 Ω	8	C 9
FTIC Shield	“	“	8	D 9
FTIC CH B	“	“	8	D 10
FTIC Shield	“	“	8	C 10
FTIC Trig/Gate	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, RAF	“	8	C 11
FTIC Shield	“	“	8	D 11
RFCTR - Inh	ESTS	Max voltage ± 10 V Max freq: 220 MHz Impedance: 50 Ω and 1 MΩ	21,22	B 13
RFCTR - Thrshld	“	“	21,22	C 13

Table A.11—Low-frequency calibrator

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Low Freq CAL HI	CASS	Max voltage: 200 Vdc Max current: 50 mA Max freq: 1.19 MHz and Max voltage: 200 Vrms Max current: 2.2 Arms Max freq: 1 kHz	9	C 39
Low Freq CAL LO	“	“	9	D 39
Low Freq Cal Shield	“	“	9	D 40
Low Freq CAL S+	“	Max voltage: 200 Vdc Max freq: 1.19 MHz and Max voltage: 200 Vrms Max freq: 1 kHz	9	C 40
Low Freq CAL S-	“	“	9	C 41
Low Freq Cal Guard	“	“	9	D 41

Table A.12—Open collector driver

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Open Collector driver CH 1 (+)	LM-STAR, TETS, IAIS, C17	Max voltage: 60 V Max current: 1 A	7	A 5
Open Collector driver CH 1 (–)	“	“	7	B 5
Open Collector driver CH 2 (+)	“	“	7	B 6
Open Collector driver CH 2 (–)	“	“	7	A 6
Open Collector driver CH 3 (+)	“	“	7	A 7
Open Collector driver CH 3 (–)	“	“	7	B 7
Open Collector driver CH 4 (+)	“	“	7	B 8
Open Collector driver CH 4 (–)	“	“	7	A 8
Open Collector driver CH 5 (+)	“	“	7	A 9
Open Collector driver CH 5 (–)	“	“	7	B 9
Open Collector driver CH 6 (+)	“	“	7	B 10
Open Collector driver CH 6 (–)	“	“	7	A 10
Open Collector driver CH 7 (+)	“	“	7	A 11
Open Collector driver CH 7 (–)	“	“	7	B 11
Open Collector driver CH 8 (+)	“	“	7	B 12
Open Collector driver CH 8 (–)	“	“	7	A 12
Open Collector driver CH 9 (+)	“	“	7	A 13
Open Collector driver CH 9 (–)	“	“	7	B 13
Open Collector driver CH 10 (+)	“	“	7	B 14
Open Collector driver CH 10 (–)	“	“	7	A 14
Open Collector driver CH 11 (+)	“	“	7	A 15
Open Collector driver CH 11 (–)	“	“	7	B 15
Open Collector driver CH 12 (+)	“	“	7	B 16
Open Collector driver CH 12 (–)	“	“	7	A 16
Open Collector driver CH 13 (+)	“	“	7	C 5
Open Collector driver CH 13 (–)	“	“	7	D 5
Open Collector driver CH 14 (+)	“	“	7	D 6
Open Collector driver CH 14 (–)	“	“	7	C 6
Open Collector driver CH 15 (+)	“	“	7	C 7
Open Collector driver CH 15 (–)	“	“	7	D 7
Open Collector driver CH 16 (+)	“	“	7	D 8
Open Collector driver CH 16 (–)	“	“	7	C 8
Open Collector driver CH 17 (+)	“	“	7	C 9
Open Collector driver CH 17 (–)	“	“	7	D 9
Open Collector driver CH 18 (+)	“	“	7	D 10
Open Collector driver CH 18 (–)	“	“	7	C 10
Open Collector driver CH 19 (+)	“	“	7	C 11
Open Collector driver CH 19 (–)	“	“	7	D 11
Open Collector driver CH 20 (+)	“	“	7	D 12
Open Collector driver CH 20 (–)	“	“	7	C 12
Open Collector driver CH 21 (+)	“	“	7	C 13
Open Collector driver CH 21 (–)	“	“	7	D 13
Open Collector driver CH 22 (+)	“	“	7	D 14
Open Collector driver CH 22 (–)	“	“	7	C 14
Open Collector driver CH 23 (+)	“	“	7	C 15
Open Collector driver CH 23 (–)	“	“	7	D 15
Open Collector driver CH 24 (+)	“	“	7	D 16
Open Collector driver CH 24 (–)	“	“	7	C 16
Open Collector driver CH 25 (+)	“	“	19	A 1
Open Collector driver CH 25 (–)	“	“	19	B 1
Open Collector driver CH 26 (+)	“	“	19	B 2
Open Collector driver CH 26 (–)	“	“	19	A 2
Open Collector driver CH 27 (+)	“	“	19	A 3

Table A.12—Open collector driver *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Open Collector driver CH 27 (–)	“	“	19	B 3
Open Collector driver CH 28 (+)	“	“	19	B 4
Open Collector driver CH 28 (–)	“	“	19	A 4
Open Collector driver CH 29 (+)	“	“	19	A 5
Open Collector driver CH 29 (–)	“	“	19	B 5
Open Collector driver CH 30 (+)	“	“	19	B 6
Open Collector driver CH 30 (–)	“	“	19	A 6
Open Collector driver CH 31 (+)	“	“	19	A 7
Open Collector driver CH 31 (–)	“	“	19	B 7
Open Collector driver CH 32 (+)	LM-STAR, IAIS, C17	“	19	B 8
Open Collector driver CH 32 (–)	“	“	19	A 8
Open Collector driver CH 33 (+)	“	“	19	A 9
Open Collector driver CH 33 (–)	“	“	19	B 9
Open Collector driver CH 34 (+)	“	“	19	B 10
Open Collector driver CH 34 (–)	“	“	19	A 10
Open Collector driver CH 35 (+)	“	“	19	A 11
Open Collector driver CH 35 (–)	“	“	19	B 11
Open Collector driver CH 36 (+)	“	“	19	B 12
Open Collector driver CH 36 (–)	“	“	19	A 12
Open Collector driver CH 37 (+)	“	“	19	A 13
Open Collector driver CH 37 (–)	“	“	19	B 13
Open Collector driver CH 38 (+)	“	“	19	B 14
Open Collector driver CH 38 (–)	“	“	19	A 14
Open Collector driver CH 39 (+)	“	“	19	A 15
Open Collector driver CH 39 (–)	“	“	19	B 15
Open Collector driver CH 40 (+)	“	“	19	B 16
Open Collector driver CH 40 (–)	“	“	19	A 16
Open Collector driver CH 41 (+)	“	“	19	C 1
Open Collector driver CH 41 (–)	“	“	19	D 1
Open Collector driver CH 42 (+)	“	“	19	D 2
Open Collector driver CH 42 (–)	“	“	19	C 2
Open Collector driver CH 43 (+)	“	“	19	C 3
Open Collector driver CH 43 (–)	“	“	19	D 3
Open Collector driver CH 44 (+)	“	“	19	D 4
Open Collector driver CH 44 (–)	“	“	19	C 4
Open Collector driver CH 45 (+)	“	“	19	C 5
Open Collector driver CH 45 (–)	“	“	19	D 5
Open Collector driver CH 46 (+)	“	“	19	D 6
Open Collector driver CH 46 (–)	“	“	19	C 6
Open Collector driver CH 47 (+)	“	“	19	C 7
Open Collector driver CH 47 (–)	“	“	19	D 7
Open Collector driver CH 48 (+)	“	“	19	D 8
Open Collector driver CH 48 (–)	“	“	19	C 8
Open Collector driver CH 49 (+)	“	“	19	C 9
Open Collector driver CH 49 (–)	“	“	19	D 9
Open Collector driver CH 50 (+)	“	“	19	D 10
Open Collector driver CH 50 (–)	“	“	19	C 10
Open Collector driver CH 51 (+)	“	“	19	C 11
Open Collector driver CH 51 (–)	“	“	19	D 11
Open Collector driver CH 52 (+)	“	“	19	D 12
Open Collector driver CH 52 (–)	“	“	19	C 12
Open Collector driver CH 53 (+)	“	“	19	C 13
Open Collector driver CH 53 (–)	“	“	19	D 13

Table A.12—Open collector driver *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Open Collector driver CH 54 (+)	“	“	19	D 14
Open Collector driver CH 54 (–)	“	“	19	C 14
Open Collector driver CH 55 (+)	“	“	19	C 15
Open Collector driver CH 55 (–)	“	“	19	D 15
Open Collector driver CH 56 (+)	“	“	19	D 16
Open Collector driver CH 56 (–)	“	“	19	C 16
Open Collector driver CH 57 (+)	“	“	20	A 1
Open Collector driver CH 57 (–)	“	“	20	B 1
Open Collector driver CH 58 (+)	“	“	20	B 2
Open Collector driver CH 58 (–)	“	“	20	A 2
Open Collector driver CH 59 (+)	“	“	20	A 3
Open Collector driver CH 59 (–)	“	“	20	B 3
Open Collector driver CH 60 (+)	“	“	20	B 4
Open Collector driver CH 60 (–)	“	“	20	A 4
Open Collector driver CH 61 (+)	“	“	20	A 5
Open Collector driver CH 61 (–)	“	“	20	B 5
Open Collector driver CH 62 (+)	“	“	20	B 6
Open Collector driver CH 62 (–)	“	“	20	A 6
Open Collector driver CH 63 (+)	“	“	20	A 7
Open Collector driver CH 63 (–)	“	“	20	B 7
Open Collector driver CH 64 (+)	“	“	20	B 8
Open Collector driver CH 64 (–)	“	“	20	A 8
Open Collector driver CH 65 (+)	LM-STAR, IAIS	“	20	A 9
Open Collector driver CH 65 (–)	“	“	20	B 9
Open Collector driver CH 66 (+)	“	“	20	B 10
Open Collector driver CH 66 (–)	“	“	20	A 10
Open Collector driver CH 67 (+)	“	“	20	A 11
Open Collector driver CH 67 (–)	“	“	20	B 11
Open Collector driver CH 68 (+)	“	“	20	B 12
Open Collector driver CH 68 (–)	“	“	20	A 12
Open Collector driver CH 69 (+)	“	“	20	A 13
Open Collector driver CH 69 (–)	“	“	20	B 13
Open Collector driver CH 70 (+)	“	“	20	B 14
Open Collector driver CH 70 (–)	“	“	20	A 14
Open Collector driver CH 71 (+)	“	“	20	A 15
Open Collector driver CH 71 (–)	“	“	20	B 15
Open Collector driver CH 72 (+)	“	“	20	B 16
Open Collector driver CH 72 (–)	“	“	20	A 16
Open Collector driver CH 73 (+)	“	“	20	C 1
Open Collector driver CH 73 (–)	“	“	20	D 1
Open Collector driver CH 74 (+)	“	“	20	D 2
Open Collector driver CH 74 (–)	“	“	20	C 2
Open Collector driver CH 75 (+)	“	“	20	C 3
Open Collector driver CH 75 (–)	“	“	20	D 3
Open Collector driver CH 76 (+)	“	“	20	D 4
Open Collector driver CH 76 (–)	“	“	20	C 4
Open Collector driver CH 77 (+)	“	“	20	C 5
Open Collector driver CH 77 (–)	“	“	20	D 5
Open Collector driver CH 78 (+)	“	“	20	D 6
Open Collector driver CH 78 (–)	“	“	20	C 6
Open Collector driver CH 79 (+)	“	“	20	C 7
Open Collector driver CH 79 (–)	“	“	20	D 7
Open Collector driver CH 80 (+)	“	“	20	D 8

Table A.12—Open collector driver *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Open Collector driver CH 80 (–)	“	“	20	C 8
Open Collector driver CH 81 (+)	“	“	20	C 9
Open Collector driver CH 81 (–)	“	“	20	D 9
Open Collector driver CH 82 (+)	“	“	20	D 10
Open Collector driver CH 82 (–)	“	“	20	C 10
Open Collector driver CH 83 (+)	“	“	20	C 11
Open Collector driver CH 83 (–)	“	“	20	D 11
Open Collector driver CH 84 (+)	“	“	20	D 12
Open Collector driver CH 84 (–)	“	“	20	C 12
Open Collector driver CH 85 (+)	“	“	20	C 13
Open Collector driver CH 85 (–)	“	“	20	D 13
Open Collector driver CH 86 (+)	“	“	20	D 14
Open Collector driver CH 86 (–)	“	“	20	C 14
Open Collector driver CH 87 (+)	“	“	20	C 15
Open Collector driver CH 87 (–)	“	“	20	D 15
Open Collector driver CH 88 (+)	“	“	20	D 16
Open Collector driver CH 88 (–)	“	“	20	C 16
Open Collector driver CH 89 (+)	“	“	27	B 28
Open Collector driver CH 89 (–)	“	“	27	A 28
Open Collector driver CH 90 (+)	“	“	27	A 29
Open Collector driver CH 90 (–)	“	“	27	B 29
Open Collector driver CH 91 (+)	“	“	27	B 30
Open Collector driver CH 91 (–)	“	“	27	A 30
Open Collector driver CH 92 (+)	“	“	27	A 31
Open Collector driver CH 92 (–)	“	“	27	B 31
Open Collector driver CH 93 (+)	“	“	27	B 32
Open Collector driver CH 93 (–)	“	“	27	A 32
Open Collector driver CH 94 (+)	“	“	27	A 33
Open Collector driver CH 94 (–)	“	“	27	B 33
Open Collector driver CH 95 (+)	“	“	27	B 34
Open Collector driver CH 95 (–)	“	“	27	A 34
Open Collector driver CH 96 (+)	“	“	27	A 35
Open Collector driver CH 96 (–)	“	“	27	B 35
Open Collector driver I/O*1-8	LM-STAR	TTL Levels	27	B 36
Open Collector driver I/O*9-16	“	TTL Levels	27	A 36
Open Collector driver I/O*17-24	“	TTL Levels	27	A 37
Open Collector driver I/O*25-32	“	TTL Levels	27	B 37
Open Collector driver I/O*33-40	“	TTL Levels	27	B 38
Open Collector driver I/O*41-48	“	TTL Levels	27	A 38
Open Collector driver I/O*49-56	“	TTL Levels	27	D 28
Open Collector driver I/O*57-64	“	TTL Levels	27	C 28
Open Collector driver I/O*65-72	“	TTL Levels	27	C 29
Open Collector driver I/O*73-80	“	TTL Levels	27	D 29
Open Collector driver I/O*81-88	“	TTL Levels	27	D 30
Open Collector driver I/O*89-96	“	TTL Levels	27	C 30
Open Collector driver I/O Return	“	TTL Levels	27	C 31
Open Collector driver CLK*1-8	“	TTL Levels	27	D 31
Open Collector driver CLK*9-16	“	TTL Levels	27	D 32
Open Collector driver CLK*17-24	“	TTL Levels	27	C 32
Open Collector driver CLK*25-32	“	TTL Levels	27	C 33
Open Collector driver CLK*33-40	“	TTL Levels	27	D 33

Table A.12—Open collector driver *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Open Collector driver CLK*41-48	“	TTL Levels	27	D 34
Open Collector driver CLK*49-56	“	TTL Levels	27	C 34
Open Collector driver CLK*57-64	“	TTL Levels	27	C 35
Open Collector driver CLK*65-72	“	TTL Levels	27	D 35
Open Collector driver CLK*73-80	“	TTL Levels	27	D 36
Open Collector driver CLK*81-88	“	TTL Levels	27	C 36
Open Collector driver CLK*89-96	“	TTL Levels	27	C 37
Open Collector driver CLK Return	“		27	D 37

Table A.13—Pulse generator

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Pulse Gen 1 ChA	CASS, LM-STAR, C17	Max voltage: ± 5V Max freq: 250 MHz	8	C 1
Pulse Gen 1 Shield	“		8	D 1
Pulse Gen 1 ChB	“	Max voltage: ± 5V Max freq: 250 MHz	8	D 2
Pulse Gen 1 Shield	“		8	C 2
Pulse Gen 1 Trig Out	“	Max voltage: TTL Max freq: 100 MHz	8	C 3
Pulse Gen 1 Shield	“		8	D 3
Pulse Gen 1 Trig In	“	Max voltage: ± 5V Max freq: 100 MHz	8	D 4
Pulse Gen 1 Shield	“		8	C 4

Table A.14—Pulse generator 2

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Pulse Gen 2 ChA	LM-STAR	Max voltage: ± 5V Max freq: 250 MHz	8	C 5
Pulse Gen 2 Shield	“		8	D 5
Pulse Gen 2 ChB	“	Max voltage: ± 5V Max freq: 250 MHz	8	D 6
Pulse Gen 2 Shield	“		8	C 6
Pulse Gen 2 Trig Out	“	Max voltage: TTL Max freq: 100 MHz	8	C 7
Pulse Gen 2 Shield	“		8	D 7
Pulse Gen 2 Trig In	“	Max voltage: ± 10V Min Pulse: 3 ns	8	D 8
Pulse Gen 2 Shield	“		8	C 8

Table A.15—Resistive load

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Resistive Load 1 (+)	CASS, LM-STAR, RAF	Maximum voltage: 200 V Max current: 500 mA Max power 5 W	9	A 41
Resistive Load 1 (–)	"	"	9	B 41

Table A.16—Scope

CTI name	Legacy system	Recommended attributes	Slot	Pin
Scope CH 1	LM-STAR, C17	BW: 1 GHz Max voltage: ±250 V	21,22	A 13
Scope CH 2	"	"	21,22	A 14
Scope CH 3	"	"	21,22	A 15
Scope CH 4	"	"	21,22	A 16
Scope AuxOut	"	Max voltage: ±2.4 V	21,22	A 17

Table A.17—Synchro-resolver

CTI name	Legacy systems	Recommended attributes	Slot	Pin
SYN1CRSE S1	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17	Max voltage: 90 Vrms Max current: 1.5 A Max freq: 1 kHz	18	A 16
SYN1CRSE S2	"	"	18	A 17
SYN1CRSE S3	"	"	18	A 18
SYN1CRSE S4	IFTE, CASS, ESTS, TETS, C17	"	18	A 19
SYN1Ind CRSE S1	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17	"	18	A 20
SYN1Ind CRSE S2	"	"	18	A 21
SYN1Ind CRSE S3	"	"	18	A 22
SYN1Ind CRSE S4	IFTE, CASS, ESTS, TETS, C17	"	18	A 23
SYN1Shield	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17	"	18	A 24
SYN1FINE S1	CASS, LM-STAR, TETS, IAIS, C17	"	18	A 25
SYN1FINE S2	"	"	18	A 26
SYN1FINE S3	"	"	18	A 27
SYN1FINE S4	CASS, TETS	"	18	A 28
SYN1Ind FINE S1	CASS, LM-STAR, TETS, IAIS, C17	"	18	A 29
SYN1Ind FINE S2	"	"	18	A 30
SYN1Ind FINE S3	"	"	18	A 31
Ext. Trigger (+)	ESTS	"	18	C 33
Ext. Trigger (–)	"	"	18	C 34
SYN1(EXT)Ref +	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17	Max voltage: 130 Vrms Max current: 1.5 A Max freq: 1 kHz	18	A 33

Table A. 17—Synchro-resolver *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
SYN1(EXT) Ref -	"	"	18	A34
SYN1IND FINE S4	"	"	18	A 32
SYN1 Ind Ref +	IFTE, CASS, ESTS, TETS, C17	"	18	A 35
SYN1 Ind Ref -	"	"	18	A36
SYN2Ind FINE S4	IFTE, CASS, ESTS, TETS, C17	"	18	B 32
SYN2Ind FINE S4	"	See above	18	D 28
SYN2 CRSE S1	CASS, LM-STAR, ESTS, TETS, IAIS	Max voltage: 90 Vrms Max current: 1.5 A Max freq: 1 kHz	18	B 16
SYN2 CRSE S2	"	"	18	B 17
SYN2 CRSE S3	"	"	18	B 18
SYN2 CRSE S4	CASS, ESTS, TETS,	"	18	B 19
SYN2 Ind CRSE S1	CASS, LM-STAR, ESTS, TETS, IAIS	"	18	B 20
SYN2 Ind CRSE S2	"	"	18	B 21
SYN2 Ind CRSE S3	"	"	18	B 22
SYN2 Ind CRSE S4	CASS, ESTS, TETS,	"	18	B 23
SYN2 Shield	CASS, LM-STAR, ESTS, TETS, IAIS	"	18	C 24
SYN2 FINE S1	CASS, LM-STAR, TETS, IAIS	"	18	B 25
SYN2 FINE S2	"	"	18	B 26
SYN2 FINE S3	"	"	18	B 27
SYN2 FINE S4	CASS, TETS	"	18	B 28
SYN2 Ind FINE S1	CASS, LM-STAR, TETS, IAIS	"	18	B 29
SYN2 Ind FINE S2	"	"	18	B 30
SYN2 Ind FINE S3	"	"	18	B 31
SYN2 Ext Ref +	CASS, LM-STAR, ESTS, TETS, IAIS	Max voltage: 130 Vrms Max current: 1.5 A Max freq: 1 kHz	18	B 34
SYN2 Ext Ref –	"	"	18	B 33
SYN2 Ind Ref +	CASS, ESTS, TETS	"	18	B 36
SYN2 Ind Ref –	"	"	18	B 35
SYN3 CRSE S1	CASS, LM-STAR, ESTS, IAIS	Max voltage: 90 Vrms Max current: 1.5 A Max freq: 1 kHz	18	C 21
SYN3 CRSE S2	"	"	18	C 22
SYN3 CRSE S3	"	"	18	C 23
SYN3 CRSE S4	CASS, ESTS	"	18	C 24
SYN3 Ind CRSE S1	CASS, LM-STAR, ESTS, IAIS	"	18	C 25
SYN3 Ind CRSE S2	"	"	18	C 26

Table A.17—Synchro-resolver *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
SYN3 Ind CRSE S3	"	"	18	C 27
SYN3 Ind CRSE S4	CASS, ESTS	"	18	C 28
SYN3 Shield	CASS, LM-STAR, ESTS, IAIS		18	D 29
SYN3 FINE S1	CASS, LM-STAR, IAIS	Max voltage: 90 Vrms Max current: 1.5 A Max freq: 1 kHz	18	D 21
SYN3 FINE S2	"	"	18	D 22
SYN3 FINE S3	"	"	18	D 23
SYN3 FINE S4	CASS	"	18	D 24
SYN3 Ind FINE S1	CASS, LM-STAR, IAIS	"	18	D 25
SYN3 Ind FINE S2	"	"	18	D 26
SYN3 Ind FINE S3	"	"	18	D 27
SYN3 Ext Ref +	CASS, LM-STAR, ESTS, IAIS	Max voltage: 130 Vrms Max current: 1.5 A Max freq: 1 kHz	18	C 29
SYN3 Ext Ref –	"	"	18	C 30
SYN3 Ind Ref +	CASS, ESTS	"	18	C 31
SYN3 Ind Ref –	"	"	18	C 32

Table A.18—Video

CTI name	Legacy systems	Recommended attributes	Slot	Pin
CLK ECL –	ESTS	100 Ω TSP PECL	26	C 18
CLK ECL +	“	100 Ω TSP PECL	26	D 18
DAS 1 Blue Stroke Z –	IFTE, ESTS, IAIS	75 Ω CX	26	B 5
DAS 1 Blue Stroke Z +	“	75 Ω CX	26	A 5
DAS 1 Blue Stroke Z S –	ESTS	100 Ω TSP PECL	26	A 24
DAS 1 Blue Stroke Z S	“	100 Ω TSP PECL	26	B 24
DAS 1 Green Stroke Y –	IFTE, ESTS, IAIS	75 Ω CX	26	C 4
DAS 1 Green Stroke Y +	“	75 Ω CX	26	D 4
DAS 1 Green Stroke Y S –	ESTS	100 Ω TSP PECL	26	C 22
DAS 1 Green Stroke Y S	“	100 Ω TSP PECL	26	D 22
DAS 1 Red Stroke X –	IFTE, ESTS, IAIS	75 Ω CX	26	D 3
DAS 1 Red Stroke X +	“	75 Ω CX	26	C 3
DAS 1 Red Stroke X S –	ESTS	100 Ω TSP PECL	26	D 21
DAS 1 Red Stroke X S +	“	100 Ω TSP PECL	26	C 21
DAS Blue Raster Vert –	IFTE, ESTS, IAIS	75 Ω CX	26	A 4
DAS Blue Raster Vert +	“	75 Ω CX	26	B 4
DAS Blue Vert S –	ESTS	100 Ω TSP PECL	26	A 22
DAS Blue Vert S +	“	100 Ω TSP PECL	26	B 22
DAS Green Raster Horiz –	IFTE, ESTS, IAIS	75 Ω CX	26	B 3
DAS Green Raster Horiz +	“	75 Ω CX	26	A 3
DAS Green S –	ESTS	100 Ω TSP PECL	26	B 21
DAS Green S +	“	100 Ω TSP PECL	26	A 21
DAS Red Horiz S –	“	100 Ω TSP PECL	26	D 19
DAS Red Horiz S +	“	100 Ω TSP PECL	26	C 19
DAS Red Raster Horiz –	IFTE, ESTS, IAIS	75 Ω CX	26	C 2
DAS Red Raster Horiz +	IFTE, ESTS	75 Ω CX	26	D 2
DAS RSIA Enable –	“	100 Ω TSP PECL	26	B 9
DAS RSIA Enable +	“	100 Ω TSP PECL	26	A 9
Det Field Out–	“	100 Ω TSP PECL	26	A 16
Det Field Out+	“	100 Ω TSP PECL	26	B 16
Det Vert Sync Out–	“	100 Ω TSP PECL	26	D 15

Table A.18—Video *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Det Vert Sync Out+	“	100 Ω TSP PECL	26	C 15
Ext Cmp Vid Enable–	“	100 Ω TSP PECL	26	A 12
Ext Cmp Vid Enable+	“	100 Ω TSP PECL	26	B 12
Ext Horiz Sync In–	“	100 Ω TSP PECL	26	D 9
Ext Horiz Sync In+	“	100 Ω TSP PECL	26	C 9
Ext Ready Out–	“	100 Ω TSP PECL	26	D 13
Ext Ready Out+	“	100 Ω TSP PECL	26	C 13
Ext Stroke Gen Clk In–	“	100 Ω TSP PECL	26	B 13
Ext Stroke Gen Clk In+	“	100 Ω TSP PECL	26	A 13
Ext Stroke Trig In–	“	100 Ω TSP PECL	26	C 10
Ext Stroke Trig In+	“	100 Ω TSP PECL	26	D 10
Ext Sys Clk In–	“	100 Ω TSP PECL	26	C 12
Ext Sys Clk In+	“	100 Ω TSP PECL	26	D 12
Ext Vert Sync In–	“	100 Ω TSP PECL	26	A 10
Ext Vert Sync In+	“	100 Ω TSP PECL	26	B 10
Horiz Sync Out–	“	100 Ω TSP PECL	26	B 19
Horiz Sync Out+	“	100 Ω TSP PECL	26	A 19
Local Horiz Sync Out–	“	100 Ω TSP PECL	26	B 15
Local Horiz Sync Out+	“	100 Ω TSP PECL	26	A 15
System Clock Out–	“	100 Ω TSP PECL	26	C 16
System Clock Out+	“	100 Ω TSP PECL	26	D 16
Vert Sync Out–	“	100 Ω TSP PECL	26	A 18
Vert Sync Out+	“	100 Ω TSP PECL	26	B 18
Video CH 0–	“	75 Ω CX	26	B 1
Video CH 0+	“	75 Ω CX	26	A 1
Video CH 1–	“	75 Ω CX	26	A 2
Video CH 1+	“	75 Ω CX	26	B 2

Table A.18—Video *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Video CH 2–	IAIS	75 Ω CX	26	D 1
Video CH 2+	“	75 Ω CX	26	C 1
Video CH 3–	“	75 Ω CX RS170–	26	B 7
Video CH 3+	“	75 Ω CX RS170+	26	A 7
Video CH 4–	“	SE2	26	D 7
Video CH 4+	“	SE1	26	C 7
Video CH 5–	“	SE	26	A 8
Video CH 5+	“	SE	26	B 8
Video CH 6–	“	SE	26	C 8
Video CH 6+	“	SE	26	D 8
Video CH 7–	“	100 Ω TSP	26	B 11
Video CH 7+	“	100 Ω TSP	26	A 11
Video CH 8–	“	100 Ω TSP	26	D 11
Video CH 8+	“	100 Ω TSP	26	C 11
Video CH 9–	“	100 Ω TSP	26	A 14
Video CH 9+	“	100 Ω TSP	26	B 14
Video CH 10–	“	100 Ω TSP	26	C 14
Video CH 10+	“	100 Ω TSP	26	D 14
Video CH 11–	“	100 Ω TSP	26	B 17
Video CH 11+	“	100 Ω TSP	26	A 17
Video CH 12–	“	100 Ω TSP	26	D 17
Video CH 12+	“	100 Ω TSP	26	C 17
Video CH 13–	“	100 Ω TSP	26	A 20
Video CH 13+	“	100 Ω TSP	26	B 20
Video CH 14–	“	100 Ω TSP	26	C 20
Video CH 14+	“	100 Ω TSP	26	D 20
Video CH 15–	“	100 Ω TSP	26	B 23
Video CH 15+	“	100 Ω TSP	26	A 23
Video CH 16–	“	100 Ω TSP	26	D 23
Video CH 16+	“	100 Ω TSP	26	C 23
Video CH 17–	“	100 Ω TSP PECL	26	A 30
Video CH 17+	“	100 Ω TSP PECL	26	B 30
Video CH 18–	“	100 Ω TSP	26	C 30
Video CH 18+	“	100 Ω TSP	26	D 30
Video CH 19–	“	100 Ω TSP PECL	26	B 31
Video CH 19+	“	100 Ω TSP PECL	26	A 31
Video CH 20–	“	100 Ω TSP	26	D 31
Video CH 20+	“	100 Ω TSP	26	C 31
Video CH 21–	“	100 Ω TSP	26	A 32
Video CH 21+	“	100 Ω TSP	26	B 32
Video CH 22–	“	100 Ω TSP	26	C 32
Video CH 22+	“	100 Ω TSP	26	D 32
Video CH 23–	“	100 Ω TSP PECL	26	B 33
Video CH 23+	“	100 Ω TSP PECL	26	A 33
Video CH 24–	“	100 Ω TSP PECL	26	D 33

Table A.18—Video *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Video CH 24+	“	100 Ω TSP PECL	26	C 33
Video CH 25–	“	100 Ω TSP PECL	26	A 34
Video CH 25+	“	100 Ω TSP PECL	26	B 34
Video CH 26–	“	100 Ω TSP PECL	26	C 34
Video CH 26+	“	100 Ω TSP PECL	26	D 34
Video CH 27–	“	100 Ω TSP	26	B 35
Video CH 27+	“	100 Ω TSP	26	A 35
Video CH 28–	“	100 Ω TSP	26	D 35
Video CH 28+	“	100 Ω TSP	26	C 35
Video CH 29–	“	120 Ω TX PECL	26	A 36
Video CH 29+	“	120 Ω TX PECL	26	B 36
Video CH 30–	“	120 Ω TX	26	C 36
Video CH 30+	“	120 Ω TX	26	D 36
Video CH 31–	“	120 Ω TX 30 Hz PECL	26	B 37
Video CH 31+	“	120 Ω TX2+ 30 Hz PECL	26	A 37
Video CH 32–	“	120 Ω TX	26	D 37
Video CH 32+	“	120 Ω TX	26	C 37
Video CH 33–	“	120 Ω TX	26	A 38
Video CH 33+	“	120 Ω TX	26	B 38
Video CH 34–	“	120 Ω TX	26	C 38
Video CH 34+	“	120 Ω TX	26	D 38
Video CH 35–	“	120 Ω TX	26	B 39
Video CH 35+	“	120 Ω TX	26	A 39
Video CH 36–	“	120 Ω TX	26	D 39
Video CH 36+	“	120 Ω TX	26	C 39
Video CH 37–	“	120 Ω TX	26	A 40
Video CH 37+	“	120 Ω TX	26	B 40
Video CH 38–	“	120 Ω TX	26	C 40
Video CH 38+	“	120 Ω TX	26	D 40
Video CH 39–	“	120 Ω TX	26	B 41
Video CH 39+	“	120 Ω TX	26	A 41
Video CH 40–	“	120 Ω TX	26	D 41
Video CH 40+	“	120 Ω TX	26	C 41
Video CH 41–	“	120 Ω TX	26	A 42
Video CH 41+	“	120 Ω TX	26	B 42
Video CH 42–	“	120 Ω TX	26	C 42
Video CH 42+	“	120 Ω TX	26	D 42
Video CH 43–	“	120 Ω TX	26	B 43
Video CH 43+	“	120 Ω TX	26	A 43
Video CH 44–	“	120 Ω TX	26	D 43
Video CH 44+	“	120 Ω TX	26	C 43
Video CH 45–	“	120 Ω TX	26	A 44
Video CH 45+	“	120 Ω TX	26	B 44

Table A.18—Video *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Video CH 46–	“	120 Ω TX	26	C 44
Video CH 46+	“	120 Ω TX	26	D 44
Video CH 47–	“	120 Ω TX	26	B 45
Video CH 47+	“	120 Ω TX	26	A 45
Video CH 48–	“	120 Ω TX	26	D 45
Video CH 48+	“	120 Ω TX	26	C 45
Video CH 49–	“	120 Ω TX	26	A 46
Video CH 49+	“	120 Ω TX	26	B 46
Video CH 50–	“	120 Ω TX	26	C 46
Video CH 50+	“	120 Ω TX	26	D 46
Video CH 51–	“	120 Ω TX	26	B 47
Video CH 51+	“	120 Ω TX	26	A 47
Video CH 52–	“	120 Ω TX	26	D 47
Video CH 52+	“	120 Ω TX	26	C 47
Video CH 53–	“	120 Ω TX	26	A 48
Video CH 53+	“	120 Ω TX	26	B 48
Video CH 54–	“	SE	26	C 48
Video CH 54+	“	SE	26	D 48
Video CH 55–	“	120 Ω TX	26	B 49
Video CH 55+	“	120 Ω TX	26	A 49
Video CH 56–	“	SE	26	D 49
Video CH 56+	“	SE	26	C 49
Video CH 57–	“	120 Ω TX	26	A 50
Video CH 57+	“	120 Ω TX	26	B 50
Video CH 58–	“	SE	26	C 50
Video CH 58+	“	SE	26	D 50
Video CH 59–	“	75 Ω CX	26	D 5
Video CH 59+	IFTE, ESTS	75 Ω CX	26	C 5
Video CH 60–	“	75 Ω CX	26	A 6
Video CH 60+	IFTE, ESTS	75 Ω CX	26	B 6
Video shield	“	75 Ω CX	26	D 6
VPG blue analog video return	CASS	100 Ω TSP PECL	26	B 27
VPG blue analog video	“	100 Ω TSP PECL	26	A 27
VPG green analog video return	“	100 Ω TSP	26	C 26
VPG green analog video	“	100 Ω TSP	26	D 26
VPG Horizontal Composite SYNC HI	“	100 Ω TSP PECL	26	A 25
VPG Horizontal Composite SYNC LO	“	100 Ω TSP PECL	26	B 25
VPG NTSC or PAL television return	“	100 Ω TSP PECL	26	C 24
VPG NTSC or PAL television	“	100 Ω TSP PECL	26	D 24
VPG red analog video return	“	100 Ω TSP	26	A 26
VPG red analog video	“	100 Ω TSP	26	B 26
VPG trigger HI	“	100 Ω TSP	26	C 29
VPG trigger LO	“	100 Ω TSP	26	D 29
VPG TTL blue intensity	“	100 Ω TSP	26	C 28
VPG TTL blue	“	100 Ω TSP	26	D 28
VPG TTL green intensity	“	100 Ω TSP PECL	26	A 28
VPG TTL green	“	100 Ω TSP PECL	26	B 28

Table A.18—Video *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
VPG TTL ground	IFTE, CASS, ESTS	75 Ω CX	26	C 6
VPG TTL horizontal SYNC	CASS	100 Ω TSP PECL	26	A 29
VPG TTL red intensity	"	100 Ω TSP	26	D 27
VPG TTL red	"	100 Ω TSP	26	C 27
VPG TTL vertical SYNC	"	100 Ω TSP PECL	26	B 29
VPG vertical SYNC HI	"	100 Ω TSP PECL	26	C 25
VPG vertical SYNC LO	"	100 Ω TSP PECL	26	D 25

Table A.19—Programmable bus

CTI name	Legacy system	Recommended attributes	Slot	Pin
Comm Bus 1 CH A+	IFTE, CASS, ESTS, TETS, C17, RAF	Function: 1553\CAN+ Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	A 33
Comm Bus 1 CH A–	CASS, C17, RAF	"	7	B 33
Comm Bus 1553 GND	CASS, SAMe, ESTS, TETS, C17	"	7	A 49
Comm Bus 1 CH B+	IFTE, CASS, ESTS, TETS, C17, RAF	Function: 1553\CAN– Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	B 34
Comm Bus 1 CH B–	CASS, C17, RAF	"	7	A 34
Comm Bus 1553 GND	CASS, SAMe, ESTS, TETS, C17	"	7	B 49
Comm Bus 1 CH C+	CASS, ESTS, RAF	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	A 35
Comm Bus 1 CH C–	CASS, ESTS	"	7	B 35
Comm Bus 1 CH D+	CASS, ESTS, RAF	"	7	B 36
Comm Bus 1 CH D–	CASS, ESTS	"	7	A 36
Comm Bus 1 CH E+	IFTE, CASS, ESTS, RAF	"	7	A 37
Comm Bus 1 CH E–	CASS	"	7	B 37
Comm Bus 1 CH F+	IFTE, CASS, ESTS, RAF	"	7	B 38
Comm Bus 1 CH F–	CASS	"	7	A 38
Comm Bus 1 CH G+	CASS, ESTS, RAF	"	7	A 39
Comm Bus 1 CH G–	CASS, ESTS	"	7	B 39
Comm Bus 1 CH H+	CASS, RAF	"	7	B 40
Comm Bus 1 CH H–	CASS	"	7	A 40
Comm Bus 2 CH A+	IFTE, CASS, C17, RAF	Function: MIC\UBIC BUS A+ Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	A 41

Table A.19—Programmable bus *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
Comm Bus 2 CH A–	CASS, SAMe, C17	“	7	B 41
Comm Bus 2 CH B+	IFTE, CASS, SAMe, C17	Function: MIC\UBIC BUS A– Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	B 42
Comm Bus 2 CH B–	CASS, SAMe, C17	“	7	A 42
Comm Bus 2 CH C+	IFTE, CASS, SAMe, ESTS	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	A 43
Comm Bus 2 CH C–	CASS, SAMe, ESTS	“	7	B 43
Comm Bus 2 CH D+	IFTE, CASS, SAMe, ESTS	“	7	B 44
Comm Bus 2 CH D–	CASS, SAMe, ESTS	“	7	A 44
Comm Bus 2 CH E+	CASS, SAMe	Function: MIC\UBIC BUS B+ Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	A 45
Comm Bus 2 CH E–	“	“	7	B 45
Comm Bus 2 CH F+	IFTE, CASS, SAMe	Function: MIC\UBIC BUS B– Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	B 46
Comm Bus 2 CH F–	CASS, SAMe	“	7	A 46
Comm Bus 2 CH G+	IFTE, CASS, SAMe, ESTS	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	A 47
Comm Bus 2 CH G–	CASS, SAMe, ESTS	“	7	B 47
Comm Bus 2 CH H+	CASS, SAMe	“	7	B 48
Comm Bus 2 CH H–	CASS, SAMe	“	7	A 48
Comm Bus 3 CH A+	CASS, SAMe, C17	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 70 Ω	7	C 33
Comm Bus 3 CH A–	“	“	7	D 33
Comm Bus 3 CH B+	“	“	7	D 34
Comm Bus 3 CH B–	“	“	7	C 34
Comm Bus 3 CH C+	CASS, SAMe	“	7	C 35
Comm Bus 3 CH C–	“	“	7	D 35
Comm Bus 3 CH D+	“	“	7	D 36
Comm Bus 3 CH D–	“	“	7	C 36
Comm Bus 3 CH E+	SAMe	“	7	C 37
Comm Bus 3 CH E–	CASS, SAMe	“	7	D 37
Comm Bus 3 CH F+	SAMe, ESTS	“	7	D 38
Comm Bus 3 CH F–	CASS, SAMe, ESTS	“	7	C 38
Comm Bus 3 CH G+	SAMe, ESTS	“	7	C 39
Comm Bus 3 CH G–	CASS, SAMe	“	7	D 39
Comm Bus 3 CH H+	SAMe, ESTS	“	7	D 40
Comm Bus 3 CH H–	CASS. SAMe	“	7	C 40

Table A.19—Programmable bus *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
Comm Bus 4 CH A+	IFTE, SAMe, ESTS, TETS, C17	Function: CAN+ Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	C 41
Comm Bus 4 CH A–	CASS, SAMe, C17	"	7	D 41
Comm Bus 4 CH B+	IFTE, SAMe, ESTS, TETS, C17	Function: CAN– Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	D 42
Comm Bus 4 CH B–	CASS, SAMe, C17	"	7	C 42
Comm Bus 4 CH C+	SAMe, ESTS, C17	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	C 43
Comm Bus 4 CH C–	CASS, SAMe, ESTS, C17	"	7	D 43
Comm Bus 4 CH D+	ESTS	"	7	D 44
Comm Bus 4 CH D–		"	7	C 44
Comm Bus 4 CH E+	IFTE, ESTS	"	7	C 45
Comm Bus 4 CH E–		"	7	D 45
Comm Bus 4 CH F+	IFTE, ESTS	"	7	D 46
Comm Bus 4 CH F–		"	7	C 46
Comm Bus 4 CH G+	CASS, ESTS	"	7	C 47
Comm Bus 4 CH G–	"	"	7	D 47
Comm Bus 4 CH H+	"	"	7	D 48
Comm Bus 4 CH H–	CASS	"	7	C 48
Comm Bus 5 CH A+	CASS, LM-STAR, IAIS, C17	Function: MIC\UBIC BUS A+ Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	A 1
Comm Bus 5 CH A–	"	"	28	B 1
Comm Bus 1553 GND		"	7	C 49
Comm Bus 5 CH B+	"	Function: MIC\UBIC BUS A– Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	B 2
Comm Bus 5 CH B–	"	"	28	A 2
Comm Bus 1553 GND		Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	7	D 49

Table A.19—Programmable bus *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
Comm Bus 5 CH C+	CASS, LM-STAR, IAIS	"	28	A 3
Comm Bus 5 CH C–	"	"	28	B 3
Comm Bus 5 CH D+	"	"	28	B 4
Comm Bus 5 CH D–	"	"	28	A 4
Comm Bus 5 CH E+	"	Function: MIC\UBIC BUS B+ Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	A 5
Comm Bus 5 CH E–	"	"	28	B 5
Comm Bus 5 CH F+	"	Function: MIC\UBIC BUS B– Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	B 6
Comm Bus 5 CH F–	"	"	28	A 6
Comm Bus 5 CH G+	"	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	A 7
Comm Bus 5 CH G–	"	"	28	B 7
Comm Bus 5 CH H+	"	"	28	B 8
Comm Bus 5 CH H–	"	"	28	A 8
Comm Bus 6 CH A+	CASS, LM-STAR, IAIS, C17	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 70 Ω	28	A 9
Comm Bus 6 CH A–	"	"	28	B 9
Comm Bus 6 CH B+	"	"	28	B 10
Comm Bus 6 CH B–	"	"	28	A 10
Comm Bus 6 CH C+	"	"	28	A 11
Comm Bus 6 CH C–	"	"	28	B 11
Comm Bus 6 CH D+	CASS, LM-STAR, IAIS	"	28	B 12
Comm Bus 6 CH D–	"	"	28	A 12
Comm Bus 6 CH E+	"	"	28	A 13
Comm Bus 6 CH E–	"	"	28	B 13
Comm Bus 6 CH F+	"	"	28	B 14
Comm Bus 6 CH F–	"	"	28	A 14
Comm Bus 6 CH G+	"	"	28	A 15
Comm Bus 6 CH G–	"	"	28	B 15
Comm Bus 6 CH H+	"	"	28	B 16
Comm Bus 6 CH H–	"	"	28	A 16
Comm Bus 7 CH A+	CASS, LM-STAR, IAIS, C17	"	28	C 1
Comm Bus 7 CH A–	"	"	28	D 1
Comm Bus 7 CH B+	"	"	28	D 2
Comm Bus 7 CH B–	"	"	28	C 2
Comm Bus 7 CH C+	"	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	C 3
Comm Bus 7 CH C–	"	"	28	D 3

Table A.19—Programmable bus *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
Comm Bus 7 CH D+	CASS, LM-STAR, IAIS	"	28	D 4
Comm Bus 7 CH D–	"	"	28	C 4
Comm Bus 7 CH E+	LM-STAR, IAIS	Function: Programmable Voltage: ± 25 V Freq: 500 MHz Impedance: 100 Ω	28	C 5
Comm Bus 7 CH E–	CASS, LM-STAR, IAIS	"	28	D 5
Comm Bus 7 CH F+	LM-STAR, IAIS	"	28	D 6
Comm Bus 7 CH F–	CASS, LM-STAR, IAIS	"	28	C 6
Comm Bus 7 CH G+	LM-STAR, IAIS	"	28	C 7
Comm Bus 7 CH G–	"	"	28	D 7
Comm Bus 7 CH H+	"	"	28	D 8
Comm Bus 7 CH H–	"	"	28	C 8
Comm Bus 8 CH A+	"	"	28	C 9
Comm Bus 8 CH A–	"	"	28	D 9
Comm Bus 8 CH B+	"	"	28	D 10
Comm Bus 8 CH B–	"	"	28	C 10
Comm Bus 8 CH C+	"	"	28	C 11
Comm Bus 8 CH C–	"	"	28	D 11
Comm Bus 8 CH D+	"	"	28	D 12
Comm Bus 8 CH D–	"	"	28	C 12
Comm Bus 8 CH E+	"	"	28	C 13
Comm Bus 8 CH E–	"	"	28	D 13
Comm Bus 8 CH F+	"	"	28	D 14
Comm Bus 8 CH F–	"	"	28	C 14
Comm Bus 8 CH G+	"	"	28	C 15
Comm Bus 8 CH G–	"	"	28	D 15
Comm Bus 8 CH H+	"	"	28	D 16
Comm Bus 8 CH H–	"	"	28	C 16

Table A.20—IEEE 1149.1 bus

CTI name	Legacy system	Recommended attributes	Slot	Pin
JTAG 1149.1_tck (Test Clock Output) (See NOTE)	LM-STAR	IEEE 1149.1 specification	3	C 44
JTAG 1149 shd	LM-STAR	IEEE 1149.1 specification	3	C 45
JTAG 1149.1_tdi (Test Data Input)	LM-STAR	IEEE 1149.1 specification	3	C 46
JTAG 1149 shd	LM-STAR	IEEE 1149.1 specification	3	C 47
JTAG 1149.1_tdo (Test Data Output)	LM-STAR	IEEE 1149.1 specification	3	C 48
JTAG 1149 shd	LM-STAR	IEEE 1149.1 specification	3	C 49
JTAG 1149.1_tms (Test Mode Select Output) (See NOTE)	LM-STAR	IEEE 1149.1 specification	3	D 44
JTAG 1149 shd	LM-STAR	IEEE 1149.1 specification	3	D 45
JTAG 1149.1_trst (Test Reset Output)	LM-STAR	IEEE 1149.1 specification	3	D 46
JTAG 1149 shd	LM-STAR	IEEE 1149.1 specification	3	D 47
JTAG mux_en (Scan Multiplex Enable)	LM-STAR	Contractor specific	3	D 48
JTAG pdi_1 (Programmable Digital Input 1)	LM-STAR	Contractor specific	28	B38
JTAG pdi_2	LM-STAR	Contractor specific	28	A39
JTAG pdi_3	LM-STAR	Contractor specific	28	B40
JTAG pdo_1 (Programmable Digital Output 1)	LM-STAR	Contractor specific	28	A41
JTAG pdo_2	LM-STAR	Contractor specific	28	B42
JTAG pdo_3	LM-STAR	Contractor specific	28	C39
JTAG pdo_4	LM-STAR	Contractor specific	28	D40
JTAG pdo_5	LM-STAR	Contractor specific	28	C41
JTAG pdo_6	LM-STAR	Contractor specific	28	D42
JTAG pdo_7	LM-STAR	Contractor specific	28	C42
NOTE—Terminated with 100 Ω to ground, TTL Logic.				

Table A.21—Digital channels

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 1 (+)	IFTE, CASS, LM-STAR, ESTS, SAMe, TETS, IAIS, C17, RAF	Max data rate: 50 MHz Max voltage: ±30 V Max current: 60 mA	9	A 1
DIGITAL CH 1 (–)	"	"	9	B 1
DIGITAL CH 2 (+)	"	"	9	B 2
DIGITAL CH 2 (–)	"	"	9	A 2
DIGITAL CH 3 (+)	"	"	9	A 3
DIGITAL CH 3 (–)	"	"	9	B 3
DIGITAL CH 4 (+)	"	"	9	B 4
DIGITAL CH 4 (–)	"	"	9	A 4
DIGITAL CH 5 (+)	"	"	9	A 5
DIGITAL CH 5 (–)	"	"	9	B 5
DIGITAL CH 6 (+)	"	"	9	B 6
DIGITAL CH 6 (–)	"	"	9	A 6
DIGITAL CH 7 (+)	"	"	9	A 7
DIGITAL CH 7 (–)	"	"	9	B 7
DIGITAL CH 8 (+)	"	"	9	B 8
DIGITAL CH 8 (–)	"	"	9	A 8
DIGITAL CH 9 (+)	"	"	9	A 9
DIGITAL CH 9 (–)	"	"	9	B 9
DIGITAL CH 10 (+)	"	"	9	B 10
DIGITAL CH 10 (–)	"	"	9	A 10
DIGITAL CH 11 (+)	"	"	9	A 11
DIGITAL CH 11 (–)	"	"	9	B 11
DIGITAL CH 12 (+)	"	"	9	B 12
DIGITAL CH 12 (–)	"	"	9	A 12
DIGITAL CH 13 (+)	"	"	9	A 13
DIGITAL CH 13 (–)	"	"	9	B 13
DIGITAL CH 14 (+)	"	"	9	B 14
DIGITAL CH 14 (–)	"	"	9	A 14
DIGITAL CH 15 (+)	"	"	9	A 15
DIGITAL CH 15 (–)	"	"	9	B 15
DIGITAL CH 16 (+)	"	"	9	B 16
DIGITAL CH 16 (–)	"	"	9	A 16
DIGITAL CH 17 (+)	"	"	9	A 17
DIGITAL CH 17 (–)	"	"	9	B 17
DIGITAL CH 18 (+)	"	"	9	B 18
DIGITAL CH 18 (–)	"	"	9	A 18
DIGITAL CH 19 (+)	"	"	9	A 19
DIGITAL CH 19 (–)	"	"	9	B 19
DIGITAL CH 20 (+)	"	"	9	B 20
DIGITAL CH 20 (–)	"	"	9	A 20
DIGITAL CH 21 (+)	"	"	9	A 21
DIGITAL CH 21 (–)	"	"	9	B 21
DIGITAL CH 22 (+)	"	"	9	B 22
DIGITAL CH 22 (–)	"	"	9	A 22
DIGITAL CH 23 (+)	"	"	9	A 23
DIGITAL CH 23 (–)	"	"	9	B 23
DIGITAL CH 24 (+)	"	"	9	B 24
DIGITAL CH 24 (–)	"	"	9	A 24
DIGITAL CH 25 (+)	"	"	9	A 25

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 25 (–)	“	“	9	B 25
DIGITAL CH 26 (+)	“	“	9	B 26
DIGITAL CH 26 (–)	“	“	9	A 26
DIGITAL CH 27 (+)	“	“	9	A 27
DIGITAL CH 27 (–)	“	“	9	B 27
DIGITAL CH 28 (+)	“	“	9	B 28
DIGITAL CH 28 (–)	“	“	9	A 28
DIGITAL CH 29 (+)	“	“	9	A 29
DIGITAL CH 29 (–)	“	“	9	B 29
DIGITAL CH 30 (+)	“	“	9	B 30
DIGITAL CH 30 (–)	“	“	9	A 30
DIGITAL CH 31 (+)	“	“	9	A 31
DIGITAL CH 31 (–)	“	“	9	B 31
DIGITAL CH 32 (+)	“	“	9	B 32
DIGITAL CH 32 (–)	“	“	9	A 32
DIGITAL CH 33 (+)	“	“	9	C 1
DIGITAL CH 33 (–)	“	“	9	D 1
DIGITAL CH 34 (+)	“	“	9	D 2
DIGITAL CH 34 (–)	“	“	9	C 2
DIGITAL CH 35 (+)	“	“	9	C 3
DIGITAL CH 35 (–)	“	“	9	D 3
DIGITAL CH 36 (+)	“	“	9	D 4
DIGITAL CH 36 (–)	“	“	9	C 4
DIGITAL CH 37 (+)	“	“	9	C 5
DIGITAL CH 37 (–)	“	“	9	D 5
DIGITAL CH 38 (+)	“	“	9	D 6
DIGITAL CH 38 (–)	“	“	9	C 6
DIGITAL CH 39 (+)	“	“	9	C 7
DIGITAL CH 39 (–)	“	“	9	D 7
DIGITAL CH 40 (+)	“	“	9	D 8
DIGITAL CH 40 (–)	“	“	9	C 8
DIGITAL CH 41 (+)	“	“	9	C 9
DIGITAL CH 41 (–)	“	“	9	D 9
DIGITAL CH 42 (+)	“	“	9	D 10
DIGITAL CH 42 (–)	“	“	9	C 10
DIGITAL CH 43 (+)	“	“	9	C 11
DIGITAL CH 43 (–)	“	“	9	D 11
DIGITAL CH 44 (+)	“	“	9	D 12
DIGITAL CH 44 (–)	“	“	9	C 12
DIGITAL CH 45 (+)	“	“	9	C 13
DIGITAL CH 45 (–)	“	“	9	D 13
DIGITAL CH 46 (+)	“	“	9	D 14
DIGITAL CH 46 (–)	“	“	9	C 14
DIGITAL CH 47 (+)	“	“	9	C 15
DIGITAL CH 47 (–)	“	“	9	D 15
DIGITAL CH 48 (+)	“	“	9	D 16
DIGITAL CH 48 (–)	“	“	9	C 16
DIGITAL CH 49 (+)	“	“	9	C 17
DIGITAL CH 49 (–)	“	“	9	D 17
DIGITAL CH 50 (+)	“	“	9	D 18
DIGITAL CH 50 (–)	“	“	9	C 18
DIGITAL CH 51 (+)	“	“	9	C 19
DIGITAL CH 51 (–)	“	“	9	D 19

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 52 (+)	"	"	9	D 20
DIGITAL CH 52 (–)	"	"	9	C 20
DIGITAL CH 53 (+)	"	"	9	C 21
DIGITAL CH 53 (–)	"	"	9	D 21
DIGITAL CH 54 (+)	"	"	9	D 22
DIGITAL CH 54 (–)	"	"	9	C 22
DIGITAL CH 55 (+)	"	"	9	C 23
DIGITAL CH 55 (–)	"	"	9	D 23
DIGITAL CH 56 (+)	"	"	9	D 24
DIGITAL CH 56 (–)	"	"	9	C 24
DIGITAL CH 57 (+)	"	"	9	C 25
DIGITAL CH 57 (–)	"	"	9	D 25
DIGITAL CH 58 (+)	"	"	9	D 26
DIGITAL CH 58 (–)	"	"	9	C 26
DIGITAL CH 59 (+)	"	"	9	C 27
DIGITAL CH 59 (–)	"	"	9	D 27
DIGITAL CH 60 (+)	"	"	9	D 28
DIGITAL CH 60 (–)	"	"	9	C 28
DIGITAL CH 61 (+)	"	"	9	C 29
DIGITAL CH 61 (–)	"	"	9	D 29
DIGITAL CH 62 (+)	"	"	9	D 30
DIGITAL CH 62 (–)	"	"	9	C 30
DIGITAL CH 63 (+)	"	"	9	C 31
DIGITAL CH 63 (–)	"	"	9	D 31
DIGITAL CH 64 (+)	"	"	9	D 32
DIGITAL CH 64 (–)	"	"	9	C 32
Kelvin ground 1			9	A 33
Kelvin ground 1 Shield			9	B 33
DIGITAL CH 65 (+)	IFTE, CASS, LM-STAR, ESTS, SAMe, TETS, IAIS, C17, RAF	"	11	A 1
DIGITAL CH 65 (–)	"	"	11	B 1
DIGITAL CH 66 (+)	"	"	11	B 2
DIGITAL CH 66 (–)	"	"	11	A 2
DIGITAL CH 67 (+)	"	"	11	A 3
DIGITAL CH 67 (–)	"	"	11	B 3
DIGITAL CH 68 (+)	"	"	11	B 4
DIGITAL CH 68 (–)	"	"	11	A 4
DIGITAL CH 69 (+)	"	"	11	A 5
DIGITAL CH 69 (–)	"	"	11	B 5
DIGITAL CH 70 (+)	"	"	11	B 6
DIGITAL CH 70 (–)	"	"	11	A 6
DIGITAL CH 71 (+)	"	"	11	A 7
DIGITAL CH 71 (–)	"	"	11	B 7
DIGITAL CH 72 (+)	"	"	11	B 8
DIGITAL CH 72 (–)	"	"	11	A 8
DIGITAL CH 73 (+)	"	"	11	A 9
DIGITAL CH 73 (–)	"	"	11	B 9
DIGITAL CH 74 (+)	"	"	11	B 10
DIGITAL CH 74 (–)	"	"	11	A 10
DIGITAL CH 75 (+)	"	"	11	A 11
DIGITAL CH 75 (–)	"	"	11	B 11
DIGITAL CH 76 (+)	"	"	11	B 12

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 76 (–)	“	“	11	A 12
DIGITAL CH 77 (+)	“	“	11	A 13
DIGITAL CH 77 (–)	“	“	11	B 13
DIGITAL CH 78 (+)	“	“	11	B 14
DIGITAL CH 78 (–)	“	“	11	A 14
DIGITAL CH 79 (+)	“	“	11	A 15
DIGITAL CH 79 (–)	“	“	11	B 15
DIGITAL CH 80 (+)	“	“	11	B 16
DIGITAL CH 80 (–)	“	“	11	A 16
DIGITAL CH 81 (+)	“	“	11	A 17
DIGITAL CH 81 (–)	“	“	11	B 17
DIGITAL CH 82 (+)	“	“	11	B 18
DIGITAL CH 82 (–)	“	“	11	A 18
DIGITAL CH 83 (+)	“	“	11	A 19
DIGITAL CH 83 (–)	“	“	11	B 19
DIGITAL CH 84 (+)	“	“	11	B 20
DIGITAL CH 84 (–)	“	“	11	A 20
DIGITAL CH 85 (+)	“	“	11	A 21
DIGITAL CH 85 (–)	“	“	11	B 21
DIGITAL CH 86 (+)	“	“	11	B 22
DIGITAL CH 86 (–)	“	“	11	A 22
DIGITAL CH 87 (+)	“	“	11	A 23
DIGITAL CH 87 (–)	“	“	11	B 23
DIGITAL CH 88 (+)	“	“	11	B 24
DIGITAL CH 88 (–)	“	“	11	A 24
DIGITAL CH 89 (+)	“	“	11	A 25
DIGITAL CH 89 (–)	“	“	11	B 25
DIGITAL CH 90 (+)	“	“	11	B 26
DIGITAL CH 90 (–)	“	“	11	A 26
DIGITAL CH 91 (+)	“	“	11	A 27
DIGITAL CH 91 (–)	“	“	11	B 27
DIGITAL CH 92 (+)	“	“	11	B 28
DIGITAL CH 92 (–)	“	“	11	A 28
DIGITAL CH 93 (+)	“	“	11	A 29
DIGITAL CH 93 (–)	“	“	11	B 29
DIGITAL CH 94 (+)	“	“	11	B 30
DIGITAL CH 94 (–)	“	“	11	A 30
DIGITAL CH 95 (+)	“	“	11	A 31
DIGITAL CH 95 (–)	“	“	11	B 31
DIGITAL CH 96 (+)	“	“	11	B 32
DIGITAL CH 96 (–)	“	“	11	A 32

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 97 (+)	IFTE, CASS, LM-STAR, ESTS, SAMe, TETS, IAIS, C17, RAF	“	11	A 33
DIGITAL CH 97 (–)	“	“	11	B 33
DIGITAL CH 98 (+)	“	“	11	B 34
DIGITAL CH 98 (–)	“	“	11	A 34
DIGITAL CH 99 (+)	“	“	11	A 35
DIGITAL CH 99 (–)	“	“	11	B 35
DIGITAL CH 100 (+)	“	“	11	B 36
DIGITAL CH 100 (–)	“	“	11	A 36
DIGITAL CH 101 (+)	“	“	11	A 37
DIGITAL CH 101 (–)	“	“	11	B 37
DIGITAL CH 102 (+)		“	11	B 38
DIGITAL CH 102 (–)	“	“	11	A 38
DIGITAL CH 103 (+)	“	“	11	A 39
DIGITAL CH 103 (–)	“	“	11	B 39
DIGITAL CH 104 (+)	“	“	11	B 40
DIGITAL CH 104 (–)	“	“	11	A 40
DIGITAL CH 105 (+)	“	“	11	A 41
DIGITAL CH 105 (–)	“	“	11	B 41
DIGITAL CH 106 (+)	“	“	11	B 42
DIGITAL CH 106 (–)	“	“	11	A 42
DIGITAL CH 107 (+)	“	“	11	A 43
DIGITAL CH 107 (–)	“	“	11	B 43
DIGITAL CH 108 (+)	“	“	11	B 44
DIGITAL CH 108 (–)	“	“	11	A 44
DIGITAL CH 109 (+)	“	“	11	A 45
DIGITAL CH 109 (–)	“	“	11	B 45
DIGITAL CH 110 (+)	“	“	11	B 46
DIGITAL CH 110 (–)	“	“	11	A 46
DIGITAL CH 111 (+)	“	“	11	A 47
DIGITAL CH 111 (–)	“	“	11	B 47
DIGITAL CH 112 (+)	“	“	11	B 48
DIGITAL CH 112 (–)	“	“	11	A 48
DIGITAL CH 113 (+)	“	“	11	C 1
DIGITAL CH 113 (–)	“	“	11	D 1
DIGITAL CH 114 (+)	“	“	11	D 2
DIGITAL CH 114 (–)	“	“	11	C 2
DIGITAL CH 115 (+)	“	“	11	C 3
DIGITAL CH 115 (–)	“	“	11	D 3
DIGITAL CH 116 (+)	“	“	11	D 4
DIGITAL CH 116 (–)	“	“	11	C 4
DIGITAL CH 117 (+)	“	“	11	C 5
DIGITAL CH 117 (–)	“	“	11	D 5
DIGITAL CH 118 (+)	“	“	11	D 6
DIGITAL CH 118 (–)	“	“	11	C 6
DIGITAL CH 119 (+)	“	“	11	C 7
DIGITAL CH 119 (–)	“	“	11	D 7
DIGITAL CH 120 (+)	“	“	11	D 8
DIGITAL CH 120 (–)	“	“	11	C 8
DIGITAL CH 121 (+)	“	“	11	C 9

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 121 (–)	“	“	11	D 9
DIGITAL CH 122 (+)	“	“	11	D 10
DIGITAL CH 122 (–)	“	“	11	C 10
DIGITAL CH 123 (+)	“	“	11	C 11
DIGITAL CH 123 (–)	“		11	D 11
DIGITAL CH 124 (+)	“	“	11	D 12
DIGITAL CH 124 (–)	“	“	11	C 12
DIGITAL CH 125 (+)	“	“	11	C 13
DIGITAL CH 125 (–)	“	“	11	D 13
DIGITAL CH 126 (+)	“	“	11	D 14
DIGITAL CH 126 (–)	“	“	11	C 14
DIGITAL CH 127 (+)	“	“	11	C 15
DIGITAL CH 127 (–)	“	“	11	D 15
DIGITAL CH 128 (+)	“	“	11	D 16
DIGITAL CH 128 (–)	“	“	11	C 16
DIGITAL CH 129 (+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	“	11	C 17
DIGITAL CH 129 (–)	“	“	11	D 17
DIGITAL CH 130 (+)	“	“	11	D 18
DIGITAL CH 130 (–)	“	“	11	C 18
DIGITAL CH 131 (+)	“	“	11	C 19
DIGITAL CH 131 (–)	“	“	11	D 19
DIGITAL CH 132 (+)	“	“	11	D 20
DIGITAL CH 132 (–)	“	“	11	C 20
DIGITAL CH 133 (+)	“	“	11	C 21
DIGITAL CH 133 (–)	“	“	11	D 21
DIGITAL CH 134 (+)	“	“	11	D 22
DIGITAL CH 134 (–)	“	“	11	C 22
DIGITAL CH 135 (+)	“	“	11	C 23
DIGITAL CH 135 (–)	“	“	11	D 23
DIGITAL CH 136 (+)	“	“	11	D 24
DIGITAL CH 136 (–)	“	“	11	C 24
DIGITAL CH 137 (+)	“	“	11	C 25
DIGITAL CH 137 (–)	“	“	11	D 25
DIGITAL CH 138 (+)	“	“	11	D 26
DIGITAL CH 138 (–)	“	“	11	C 26
DIGITAL CH 139 (+)	“	“	11	C 27
DIGITAL CH 139 (–)	“	“	11	D 27
DIGITAL CH 140 (+)	“	“	11	D 28
DIGITAL CH 140 (–)	“	“	11	C 28
DIGITAL CH 141 (+)	“	“	11	C 29
DIGITAL CH 141 (–)	“	“	11	D 29
DIGITAL CH 142 (+)	“	“	11	D 30
DIGITAL CH 142 (–)	“	“	11	C 30
DIGITAL CH 143 (+)	“	“	11	C 31
DIGITAL CH 143 (–)	“	“	11	D 31
DIGITAL CH 144 (+)	“	“	11	D 32
DIGITAL CH 144 (–)	“	“	11	C 32
DIGITAL CH 145 (+)	“	“	11	C 33
DIGITAL CH 145 (–)	“	“	11	D 33
DIGITAL CH 146 (+)	“	“	11	D 34

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 146 (–)	“	“	11	C 34
DIGITAL CH 147 (+)	“	“	11	C 35
DIGITAL CH 147 (–)	“	“	11	D 35
DIGITAL CH 148 (+)	“	“	11	D 36
DIGITAL CH 148 (–)	“	“	11	C 36
DIGITAL CH 149 (+)	“	“	11	C 37
DIGITAL CH 149 (–)	“	“	11	D 37
DIGITAL CH 150 (+)	“	“	11	D 38
DIGITAL CH 150 (–)	“	“	11	C 38
DIGITAL CH 151 (+)	“	“	11	C 39
DIGITAL CH 151 (–)	“	“	11	D 39
DIGITAL CH 152 (+)	“	“	11	D 40
DIGITAL CH 152 (–)	“	“	11	C 40
DIGITAL CH 153 (+)	“	“	11	C 41
DIGITAL CH 153 (–)	“	“	11	D 41
DIGITAL CH 154 (+)	“	“	11	D 42
DIGITAL CH 154 (–)	“	“	11	C 42
DIGITAL CH 155 (+)	“	“	11	C 43
DIGITAL CH 155 (–)	“	“	11	D 43
DIGITAL CH 156 (+)	“	“	11	D 44
DIGITAL CH 156 (–)	“	“	11	C 44
DIGITAL CH 157 (+)	“	“	11	C 45
DIGITAL CH 157 (–)	“	“	11	D 45
DIGITAL CH 158 (+)	“	“	11	D 46
DIGITAL CH 158 (–)	“	“	11	C 46
DIGITAL CH 159 (+)	“	“	11	C 47
DIGITAL CH 159 (–)	“	“	11	D 47
DIGITAL CH 160 (+)	“	“	11	D 48
DIGITAL CH 160 (–)	“	“	11	C 48
Kelvin ground 2			11	A 49
Kelvin ground 2 Shield			11	B 49
DIGITAL CH 161 (+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	“	12	A 1
DIGITAL CH 161 (–)	“	“	12	B 1
DIGITAL CH 162 (+)	“	“	12	B 2
DIGITAL CH 162 (–)	“	“	12	A 2
DIGITAL CH 163 (+)	“	“	12	A 3
DIGITAL CH 163 (–)	“	“	12	B 3
DIGITAL CH 164 (+)	“	“	12	B 4
DIGITAL CH 164 (–)	“	“	12	A 4
DIGITAL CH 165 (+)	“	“	12	A 5
DIGITAL CH 165 (–)	“	“	12	B 5
DIGITAL CH 166 (+)	“	“	12	B 6
DIGITAL CH 166 (–)	“	“	12	A 6
DIGITAL CH 167 (+)	“	“	12	A 7
DIGITAL CH 167 (–)	“	“	12	B 7
DIGITAL CH 168 (+)	“	“	12	B 8
DIGITAL CH 168 (–)	“	“	12	A 8
DIGITAL CH 169 (+)	“	“	12	A 9
DIGITAL CH 169 (–)	“	“	12	B 9

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 170 (+)	“	“	12	B 10
DIGITAL CH 170 (–)	“	“	12	A 10
DIGITAL CH 171 (+)	“	“	12	A 11
DIGITAL CH 171 (–)	“	“	12	B 11
DIGITAL CH 172 (+)	“	“	12	B 12
DIGITAL CH 172 (–)	“	“	12	A 12
DIGITAL CH 173 (+)	“	“	12	A 13
DIGITAL CH 173 (–)	“	“	12	B 13
DIGITAL CH 174 (+)	“	“	12	B 14
DIGITAL CH 174 (–)	“	“	12	A 14
DIGITAL CH 175 (+)	“	“	12	A 15
DIGITAL CH 175 (–)	“	“	12	B 15
DIGITAL CH 176 (+)	“	“	12	B 16
DIGITAL CH 176 (–)	“	“	12	A 16
DIGITAL CH 177 (+)	“	“	12	A 17
DIGITAL CH 177 (–)	“	“	12	B 17
DIGITAL CH 178 (+)	“	“	12	B 18
DIGITAL CH 178 (–)	“	“	12	A 18
DIGITAL CH 179 (+)	“	“	12	A 19
DIGITAL CH 179 (–)	“	“	12	B 19
DIGITAL CH 180 (+)	“	“	12	B 20
DIGITAL CH 180 (–)	“	“	12	A 20
DIGITAL CH 181 (+)	“	“	12	A 21
DIGITAL CH 181 (–)	“	“	12	B 21
DIGITAL CH 182 (+)	“	“	12	B 22
DIGITAL CH 182 (–)	“	“	12	A 22
DIGITAL CH 183 (+)	“	“	12	A 23
DIGITAL CH 183 (–)	“	“	12	B 23
DIGITAL CH 184 (+)	“	“	12	B 24
DIGITAL CH 184 (–)	“	“	12	A 24
DIGITAL CH 185 (+)	“	“	12	A 25
DIGITAL CH 185 (–)	“	“	12	B 25
DIGITAL CH 186 (+)	“	“	12	B 26
DIGITAL CH 186 (–)	“	“	12	A 26
DIGITAL CH 187 (+)	“	“	12	A 27
DIGITAL CH 187 (–)	“	“	12	B 27
DIGITAL CH 188 (+)	“		12	B 28
DIGITAL CH 188 (–)	“	“	12	A 28
DIGITAL CH 189 (+)	“	“	12	A 29
DIGITAL CH 189 (–)	“	“	12	B 29
DIGITAL CH 190 (+)	“	“	12	B 30
DIGITAL CH 190 (–)	“	“	12	A 30
DIGITAL CH 191 (+)	“	“	12	A 31
DIGITAL CH 191 (–)	“	“	12	B 31
DIGITAL CH 192 (+)	“	“	12	B 32
DIGITAL CH 192 (–)	“	“	12	A 32

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 193 (+)	IFTE, CASS, LM-STAR, ESTS, SAMe, IAIS, C17, RAF	“	12	A 33
DIGITAL CH 193 (–)	“	“	12	B 33
DIGITAL CH 194 (+)	“	“	12	B 34
DIGITAL CH 194 (–)	“	“	12	A 34
DIGITAL CH 195 (+)	“	“	12	A 35
DIGITAL CH 195 (–)	“	“	12	B 35
DIGITAL CH 196 (+)	“	“	12	B 36
DIGITAL CH 196 (–)	“	“	12	A 36
DIGITAL CH 197 (+)	“	“	12	A 37
DIGITAL CH 197 (–)	“	“	12	B 37
DIGITAL CH 198 (+)	“	“	12	B 38
DIGITAL CH 198 (–)	“	“	12	A 38
DIGITAL CH 199 (+)	“	“	12	A 39
DIGITAL CH 199 (–)	“	“	12	B 39
DIGITAL CH 200 (+)	“	“	12	B 40
DIGITAL CH 200 (–)	“	“	12	A 40
DIGITAL CH 201 (+)	“	“	12	A 41
DIGITAL CH 201 (–)	“	“	12	B 41
DIGITAL CH 202 (+)	“	“	12	B 42
DIGITAL CH 202 (–)	“	“	12	A 42
DIGITAL CH 203 (+)	“	“	12	A 43
DIGITAL CH 203 (–)	“	“	12	B 43
DIGITAL CH 204 (+)	“	“	12	B 44
DIGITAL CH 204 (–)	“	“	12	A 44
DIGITAL CH 205 (+)	“	“	12	A 45
DIGITAL CH 205 (–)	“	“	12	B 45
DIGITAL CH 206 (+)	“	“	12	B 46
DIGITAL CH 206 (–)	“	“	12	A 46
DIGITAL CH 207 (+)	“	“	12	A 47
DIGITAL CH 207 (–)	“	“	12	B 47
DIGITAL CH 208 (+)	“	“	12	B 48
DIGITAL CH 208 (–)	“	“	12	A 48
DIGITAL CH 209 (+)	“	“	12	C 1
DIGITAL CH 209 (–)	“	“	12	D 1
DIGITAL CH 210 (+)	“	“	12	D 2
DIGITAL CH 210 (–)	“	“	12	C 2
DIGITAL CH 211 (+)	“	“	12	C 3
DIGITAL CH 211 (–)	“	“	12	D 3
DIGITAL CH 212 (+)	“	“	12	D 4
DIGITAL CH 212 (–)	“	“	12	C 4
DIGITAL CH 213 (+)	“	“	12	C 5
DIGITAL CH 213 (–)	“	“	12	D 5
DIGITAL CH 214 (+)	“	“	12	D 6
DIGITAL CH 214 (–)	“	“	12	C 6
DIGITAL CH 215 (+)	“	“	12	C 7
DIGITAL CH 215 (–)	“	“	12	D 7
DIGITAL CH 216 (+)	“	“	12	D 8
DIGITAL CH 216 (–)	“	“	12	C 8
DIGITAL CH 217 (+)	“	“	12	C 9

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 217 (–)	“	“	12	D 9
DIGITAL CH 218 (+)	“	“	12	D 10
DIGITAL CH 218 (–)	“	“	12	C 10
DIGITAL CH 219 (+)	“	“	12	C 11
DIGITAL CH 219 (–)	“	“	12	D 11
DIGITAL CH 220 (+)	“	“	12	D 12
DIGITAL CH 220 (–)	“	“	12	C 12
DIGITAL CH 221 (+)	“	“	12	C 13
DIGITAL CH 221 (–)	“	“	12	D 13
DIGITAL CH 222 (+)	“	“	12	D 14
DIGITAL CH 222 (–)	“	“	12	C 14
DIGITAL CH 223 (+)	“	“	12	C 15
DIGITAL CH 223 (–)	“	“	12	D 15
DIGITAL CH 224 (+)	“	“	12	D 16
DIGITAL CH 224 (–)	“	“	12	C 16
DIGITAL CH 225 (+)	IFTE, CASS, LM-STAR, ESTS, SAMe, IAIS, C17, RAF	“	12	C 17
DIGITAL CH 225 (–)	“	“	12	D 17
DIGITAL CH 226 (+)	“	“	12	D 18
DIGITAL CH 226 (–)	“	“	12	C 18
DIGITAL CH 227 (+)	“	“	12	C 19
DIGITAL CH 227 (–)	“	“	12	D 19
DIGITAL CH 228 (+)	“	“	12	D 20
DIGITAL CH 228 (–)	“	“	12	C 20
DIGITAL CH 229 (+)	“	“	12	C 21
DIGITAL CH 229 (–)	“	“	12	D 21
DIGITAL CH 230 (+)	“	“	12	D 22
DIGITAL CH 230 (–)	“	“	12	C 22
DIGITAL CH 231 (+)	“		12	C 23
DIGITAL CH 231 (–)	“	“	12	D 23
DIGITAL CH 232 (+)	“	“	12	D 24
DIGITAL CH 232 (–)	“	“	12	C 24
DIGITAL CH 233 (+)	“	“	12	C 25
DIGITAL CH 233 (–)	“	“	12	D 25
DIGITAL CH 234 (+)	“	“	12	D 26
DIGITAL CH 234 (–)	“	“	12	C 26
DIGITAL CH 235 (+)	“	“	12	C 27
DIGITAL CH 235 (–)	“	“	12	D 27
DIGITAL CH 236 (+)	“	“	12	D 28
DIGITAL CH 236 (–)	“	“	12	C 28
DIGITAL CH 237 (+)	“	“	12	C 29
DIGITAL CH 237 (–)	“	“	12	D 29
DIGITAL CH 238 (+)	“	“	12	D 30
DIGITAL CH 238 (–)	“	“	12	C 30
DIGITAL CH 239 (+)	“	“	12	C 31
DIGITAL CH 239 (–)	“	“	12	D 31
DIGITAL CH 240 (+)	“	“	12	D 32
DIGITAL CH 240 (–)	“	“	12	C 32
DIGITAL CH 241 (+)	“	“	12	C 33
DIGITAL CH 241 (–)	“	“	12	D 33
DIGITAL CH 242 (+)	“	“	12	D 34

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 242 (–)	“	“	12	C 34
DIGITAL CH 243 (+)	“	“	12	C 35
DIGITAL CH 243 (–)	“	“	12	D 35
DIGITAL CH 244 (+)	“	“	12	D 36
DIGITAL CH 244 (–)	“	“	12	C 36
DIGITAL CH 245 (+)	“	“	12	C 37
DIGITAL CH 245 (–)	“	“	12	D 37
DIGITAL CH 246 (+)	“	“	12	D 38
DIGITAL CH 246 (–)	“	“	12	C 38
DIGITAL CH 247 (+)	“	“	12	C 39
DIGITAL CH 247 (–)	“	“	12	D 39
DIGITAL CH 248 (+)	“	“	12	D 40
DIGITAL CH 248 (–)	“	“	12	C 40
DIGITAL CH 249 (+)	“	“	12	C 41
DIGITAL CH 249 (–)	“	“	12	D 41
DIGITAL CH 250 (+)	“	“	12	D 42
DIGITAL CH 250 (–)	“	“	12	C 42
DIGITAL CH 251 (+)	“	“	12	C 43
DIGITAL CH 251 (–)	“	“	12	D 43
DIGITAL CH 252 (+)	“	“	12	D 44
DIGITAL CH 252 (–)	“	“	12	C 44
DIGITAL CH 253 (+)	“	“	12	C 45
DIGITAL CH 253 (–)	“	“	12	D 45
DIGITAL CH 254 (+)	“	“	12	D 46
DIGITAL CH 254 (–)	“	“	12	C 46
DIGITAL CH 255 (+)	“	“	12	C 47
DIGITAL CH 255 (–)	“	“	12	D 47
DIGITAL CH 256 (+)	“	“	12	D 48
DIGITAL CH 256 (–)	“	“	12	C 48
Kelvin ground 3	“	“	12	A 49
Kelvin ground 3 Shield	“	“	12	B 49
DIGITAL CH 257 (+)	IFTE, CASS, LM-STAR, ESTS, IAIS, C17, RAF	“	13	A 1
DIGITAL CH 257 (–)	“	“	13	B 1
DIGITAL CH 258 (+)	“	“	13	B 2
DIGITAL CH 258 (–)	“	“	13	A 2
DIGITAL CH 259 (+)	“	“	13	A 3
DIGITAL CH 259 (–)	“	“	13	B 3
DIGITAL CH 260 (+)	“	“	13	B 4
DIGITAL CH 260 (–)	“	“	13	A 4
DIGITAL CH 261 (+)	“	“	13	A 5
DIGITAL CH 261 (–)	“	“	13	B 5
DIGITAL CH 262 (+)	“	“	13	B 6
DIGITAL CH 262 (–)	“	“	13	A 6
DIGITAL CH 263 (+)	“	“	13	A 7
DIGITAL CH 263 (–)	“	“	13	B 7
DIGITAL CH 264 (+)	“	“	13	B 8
DIGITAL CH 264 (–)	“	“	13	A 8

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 265 (+)	“	“	13	A 9
DIGITAL CH 265 (–)	“	“	13	B 9
DIGITAL CH 266 (+)	“	“	13	B 10
DIGITAL CH 266 (–)	“	“	13	A 10
DIGITAL CH 267 (+)	“	“	13	A 11
DIGITAL CH 267 (–)	“	“	13	B 11
DIGITAL CH 268 (+)	“	“	13	B 12
DIGITAL CH 268 (–)	“	“	13	A 12
DIGITAL CH 269 (+)	“	“	13	A 13
DIGITAL CH 269 (–)	“	“	13	B 13
DIGITAL CH 270 (+)	“	“	13	B 14
DIGITAL CH 270 (–)	“	“	13	A 14
DIGITAL CH 271 (+)	“	“	13	A 15
DIGITAL CH 271 (–)	“	“	13	B 15
DIGITAL CH 272 (+)	“	“	13	B 16
DIGITAL CH 272 (–)	“	“	13	A 16
DIGITAL CH 273 (+)	“	“	13	A 17
DIGITAL CH 273 (–)	“	“	13	B 17
DIGITAL CH 274 (+)	“	“	13	B 18
DIGITAL CH 274 (–)	“	“	13	A 18
DIGITAL CH 275 (+)	“	“	13	A 19
DIGITAL CH 275 (–)	“	“	13	B 19
DIGITAL CH 276 (+)	“	“	13	B 20
DIGITAL CH 276 (–)	“	“	13	A 20
DIGITAL CH 277 (+)	“	“	13	A 21
DIGITAL CH 277 (–)	“	“	13	B 21
DIGITAL CH 278 (+)	“	“	13	B 22
DIGITAL CH 278 (–)	“	“	13	A 22
DIGITAL CH 279 (+)	“	“	13	A 23
DIGITAL CH 279 (–)	“	“	13	B 23
DIGITAL CH 280 (+)	“	“	13	B 24
DIGITAL CH 280 (–)	“	“	13	A 24
DIGITAL CH 281 (+)	“	“	13	A 25
DIGITAL CH 281 (–)	“	“	13	B 25
DIGITAL CH 282 (+)	“	“	13	B 26
DIGITAL CH 282 (–)	“	“	13	A 26
DIGITAL CH 283 (+)	“	“	13	A 27
DIGITAL CH 283 (–)	“	“	13	B 27
DIGITAL CH 284 (+)	“	“	13	B 28
DIGITAL CH 284 (–)	“	“	13	A 28
DIGITAL CH 285 (+)	“	“	13	A 29
DIGITAL CH 285 (–)	“	“	13	B 29
DIGITAL CH 286 (+)	“	“	13	B 30
DIGITAL CH 286 (–)	“	“	13	A 30
DIGITAL CH 287 (+)	“	“	13	A 31
DIGITAL CH 287 (–)	“	“	13	B 31
DIGITAL CH 288 (+)	“	“	13	B 32
DIGITAL CH 288 (–)	“	“	13	A 32

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 289 (+)	IFTE, CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	A 33
DIGITAL CH 289 (–)	“	“	13	B 33
DIGITAL CH 290 (+)	“	“	13	B 34
DIGITAL CH 290 (–)	“	“	13	A 34
DIGITAL CH 291 (+)	“	“	13	A 35
DIGITAL CH 291 (–)	“	“	13	B 35
DIGITAL CH 292 (+)	“	“	13	B 36
DIGITAL CH 292 (–)	“	“	13	A 36
DIGITAL CH 293 (+)	“	“	13	A 37
DIGITAL CH 293 (–)	“	“	13	B 37
DIGITAL CH 294 (+)	“	“	13	B 38
DIGITAL CH 294 (–)	“	“	13	A 38
DIGITAL CH 295 (+)	“	“	13	A 39
DIGITAL CH 295 (–)	“		13	B 39
DIGITAL CH 296 (+)	“	“	13	B 40
DIGITAL CH 296 (–)	“	“	13	A 40
DIGITAL CH 297 (+)	“	“	13	A 41
DIGITAL CH 297 (–)	“	“	13	B 41
DIGITAL CH 298 (+)	“	“	13	B 42
DIGITAL CH 298 (–)	“	“	13	A 42
DIGITAL CH 299 (+)	“	“	13	A 43
DIGITAL CH 299 (–)	“	“	13	B 43
DIGITAL CH 300 (+)	“	“	13	B 44
DIGITAL CH 300 (–)	“	“	13	A 44
DIGITAL CH 301 (+)	“	“	13	A 45
DIGITAL CH 301 (–)	“	“	13	B 45
DIGITAL CH 302 (+)	“	“	13	B 46
DIGITAL CH 302 (–)	“	“	13	A 46
DIGITAL CH 303 (+)	“	“	13	A 47
DIGITAL CH 303 (–)	“	“	13	B 47
DIGITAL CH 304 (+)	“	“	13	B 48
DIGITAL CH 304 (–)	“	“	13	A 48
DIGITAL CH 305 (+)	“	“	13	C 1
DIGITAL CH 305 (–)	“	“	13	D 1
DIGITAL CH 306 (+)	“	“	13	D 2
DIGITAL CH 306 (–)	“	“	13	C 2
DIGITAL CH 307 (+)	“	“	13	C 3
DIGITAL CH 307 (–)	“	“	13	D 3
DIGITAL CH 308 (+)	“	“	13	D 4
DIGITAL CH 308 (–)	“	“	13	C 4
DIGITAL CH 309 (+)	“	“	13	C 5
DIGITAL CH 309 (–)	“	“	13	D 5
DIGITAL CH 310 (+)	“	“	13	D 6
DIGITAL CH 310 (–)	“	“	13	C 6
DIGITAL CH 311 (+)	“	“	13	C 7
DIGITAL CH 311 (–)	“	“	13	D 7
DIGITAL CH 312 (+)	“	“	13	D 8
DIGITAL CH 312 (–)	“	“	13	C 8
DIGITAL CH 313 (+)	“	“	13	C 9
DIGITAL CH 313 (–)	“	“	13	D 9
DIGITAL CH 314 (+)	“	“	13	D 10

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 314 (–)	“	“	13	C 10
DIGITAL CH 315 (+)	“	“	13	C 11
DIGITAL CH 315 (–)	“	“	13	D 11
DIGITAL CH 316 (+)	“	“	13	D 12
DIGITAL CH 316 (–)	“	“	13	C 12
DIGITAL CH 317 (+)	“		13	C 13
DIGITAL CH 317 (–)	“	“	13	D 13
DIGITAL CH 318 (+)	“	“	13	D 14
DIGITAL CH 318 (–)	“	“	13	C 14
DIGITAL CH 319 (+)	“	“	13	C 15
DIGITAL CH 319 (–)	“	“	13	D 15
DIGITAL CH 320 (+)	“	“	13	D 16
DIGITAL CH 320 (–)	“	“	13	C 16
DIGITAL CH 321 (+)	IFTE, CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	C 17
DIGITAL CH 321 (–)	“	“	13	D 17
DIGITAL CH 322 (+)	“	“	13	D 18
DIGITAL CH 322 (–)	“	“	13	C 18
DIGITAL CH 323 (+)	“	“	13	C 19
DIGITAL CH 323 (–)	“	“	13	D 19
DIGITAL CH 324 (+)	“	“	13	D 20
DIGITAL CH 324 (–)	“	“	13	C 20
DIGITAL CH 325 (+)	“	“	13	C 21
DIGITAL CH 325 (–)	“	“	13	D 21
DIGITAL CH 326 (+)	“	“	13	D 22
DIGITAL CH 326 (–)	“	“	13	C 22
DIGITAL CH 327 (+)	“	“	13	C 23
DIGITAL CH 327 (–)	“	“	13	D 23
DIGITAL CH 328 (+)	“	“	13	D 24
DIGITAL CH 328 (–)	“	“	13	C 24
DIGITAL CH 329 (+)	“	“	13	C 25
DIGITAL CH 329 (–)	“	“	13	D 25
DIGITAL CH 330 (+)	“	“	13	D 26
DIGITAL CH 330 (–)	“	“	13	C 26
DIGITAL CH 331 (+)	“	“	13	C 27
DIGITAL CH 331 (–)	“	“	13	D 27
DIGITAL CH 332 (+)	“	“	13	D 28
DIGITAL CH 332 (–)	“	“	13	C 28
DIGITAL CH 333 (+)	“	“	13	C 29
DIGITAL CH 333 (–)	“	“	13	D 29
DIGITAL CH 334 (+)	“	“	13	D 30
DIGITAL CH 334 (–)	“	“	13	C 30
DIGITAL CH 335 (+)	“	“	13	C 31
DIGITAL CH 335 (–)	“	“	13	D 31
DIGITAL CH 336 (+)	“	“	13	D 32
DIGITAL CH 336 (–)	“	“	13	C 32
DIGITAL CH 337 (+)	CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	C 33
DIGITAL CH 337 (–)	“	“	13	D 33

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 338 (+)	IFTE, CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	D 34
DIGITAL CH 338 (–)	“	“	13	C 34
DIGITAL CH 339 (+)	“	“	13	C 35
DIGITAL CH 339 (–)	“	“	13	D 35
DIGITAL CH 340 (+)	CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	D 36
DIGITAL CH 340 (–)	“	“	13	C 36
DIGITAL CH 341 (+)	IFTE, CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	C 37
DIGITAL CH 341 (–)	“	“	13	D 37
DIGITAL CH 342 (+)	“	“	13	D 38
DIGITAL CH 342 (–)	“	“	13	C 38
DIGITAL CH 343 (+)	“	“	13	C 39
DIGITAL CH 343 (–)	“	“	13	D 39
DIGITAL CH 344 (+)	“	“	13	D 40
DIGITAL CH 344 (–)	“	“	13	C 40
DIGITAL CH 345 (+)	“	“	13	C 41
DIGITAL CH 345 (–)	“	“	13	D 41
DIGITAL CH 346 (+)	“	“	13	D 42
DIGITAL CH 346 (–)	“	“	13	C 42
DIGITAL CH 347 (+)	“	“	13	C 43
DIGITAL CH 347 (–)	“	“	13	D 43
DIGITAL CH 348 (+)	“	“	13	D 44
DIGITAL CH 348 (–)	“	“	13	C 44
DIGITAL CH 349 (+)	CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	13	C 45
DIGITAL CH 349 (–)	“	“	13	D 45
DIGITAL CH 350 (+)	“	“	13	D 46
DIGITAL CH 350 (–)	“	“	13	C 46
DIGITAL CH 351 (+)	“	“	13	C 47
DIGITAL CH 351 (–)	“	“	13	D 47
DIGITAL CH 352 (+)	“	“	13	D 48
DIGITAL CH 352 (–)	“	“	13	C 48
DIGITAL CH 353 (+)	IFTE, CASS, LM-STAR, SAMe, ESTS, IAIS, C17, RAF	“	14	A 1
DIGITAL CH 353 (–)	“	“	14	B 1
DIGITAL CH 354 (+)	“	“	14	B 2
DIGITAL CH 354 (–)	“	“	14	A 2
DIGITAL CH 355 (+)	“	“	14	A 3
DIGITAL CH 355 (–)	“	“	14	B 3
DIGITAL CH 356 (+)	“	“	14	B 4
DIGITAL CH 356 (–)	“	“	14	A 4
DIGITAL CH 357 (+)	“	“	14	A 5
DIGITAL CH 357 (–)	“	“	14	B 5

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 358 (+)	IFTE, CASS, LM-STAR, SAMe, IAIS, C17, RAF	“	14	B 6
DIGITAL CH 358 (–)	“	“	14	A 6
DIGITAL CH 359 (+)	“	“	14	A 7
DIGITAL CH 359 (–)	“	“	14	B 7
DIGITAL CH 360 (+)	“	“	14	B 8
DIGITAL CH 360 (–)	“	“	14	A 8
DIGITAL CH 361 (+)	“	“	14	A 9
DIGITAL CH 361 (–)	“	“	14	B 9
DIGITAL CH 362 (+)	“	“	14	B 10
DIGITAL CH 362 (–)	“	“	14	A 10
DIGITAL CH 363 (+)	“	“	14	A 11
DIGITAL CH 363 (–)	“	“	14	B 11
DIGITAL CH 364 (+)	“	“	14	B 12
DIGITAL CH 364 (–)	“	“	14	A 12
DIGITAL CH 365 (+)	“	“	14	A 13
DIGITAL CH 365 (–)	“	“	14	B 13
DIGITAL CH 366 (+)	“	“	14	B 14
DIGITAL CH 366 (–)	“	“	14	A 14
DIGITAL CH 367 (+)	“	“	14	A 15
DIGITAL CH 367 (–)	“	“	14	B 15
DIGITAL CH 368 (+)	“	“	14	B 16
DIGITAL CH 368 (–)	“	“	14	A 16
DIGITAL CH 369 (+)	CASS, LM-STAR, SAMe, IAIS, C17	“	14	A 17
DIGITAL CH 369 (–)	“	“	14	B 17
DIGITAL CH 370 (+)	IFTE, CASS, LM-STAR, SAMe, IAIS, C17	“	14	B 18
DIGITAL CH 370 (–)	“	“	14	A 18
DIGITAL CH 371 (+)	“	“	14	A 19
DIGITAL CH 371 (–)	“	“	14	B 19
DIGITAL CH 372 (+)	CASS, LM-STAR, SAMe, IAIS, C17	“	14	B 20
DIGITAL CH 372 (–)	“	“	14	A 20
DIGITAL CH 373 (+)	“	“	14	A 21
DIGITAL CH 373 (–)	“	“	14	B 21
DIGITAL CH 374 (+)	“	“	14	B 22
DIGITAL CH 374 (–)	“	“	14	A 22
DIGITAL CH 375 (+)	“	“	14	A 23
DIGITAL CH 375 (–)	“	“	14	B 23
DIGITAL CH 376 (+)	“	“	14	B 24
DIGITAL CH 376 (–)	“	“	14	A 24
DIGITAL CH 377 (+)	“	“	14	A 25
DIGITAL CH 377 (–)	“	“	14	B 25
DIGITAL CH 378 (+)	“	“	14	B 26
DIGITAL CH 378 (–)	“	“	14	A 26
DIGITAL CH 379 (+)	“	“	14	A 27
DIGITAL CH 379 (–)	“	“	14	B 27
DIGITAL CH 380 (+)	“	“	14	B 28

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 380 (–)	“	“	14	A 28
DIGITAL CH 381 (+)	“	“	14	A 29
DIGITAL CH 381 (–)	“	“	14	B 29
DIGITAL CH 382 (+)	“	“	14	B 30
DIGITAL CH 382 (–)	“	“	14	A 30
DIGITAL CH 383 (+)	“	“	14	A 31
DIGITAL CH 383 (–)	“	“	14	B 31
DIGITAL CH 384 (+)	“	“	14	B 32
DIGITAL CH 384 (–)	“	“	14	A 32
DIGITAL CH 385 (+)	C17	“	14	A 33
DIGITAL CH 385 (–)	“	“	14	B 33
DIGITAL CH 386 (+)	“	“	14	B 34
DIGITAL CH 386 (–)	“	“	14	A 34
DIGITAL CH 387 (+)	“	“	14	A 35
DIGITAL CH 387 (–)	“	“	14	B 35
DIGITAL CH 388 (+)	“	“	14	B 36
DIGITAL CH 388 (–)	“	“	14	A 36
DIGITAL CH 389 (+)	“	“	14	A 37
DIGITAL CH 389 (–)	“	“	14	B 37
DIGITAL CH 390 (+)	“	“	14	B 38
DIGITAL CH 390 (–)	“	“	14	A 38
DIGITAL CH 391 (+)	“	“	14	A 39
DIGITAL CH 391 (–)	“	“	14	B 39
DIGITAL CH 392 (+)	“	“	14	B 40
DIGITAL CH 392 (–)	“	“	14	A 40
DIGITAL CH 393 (+)	“	“	14	A 41
DIGITAL CH 393 (–)	“	“	14	B 41
DIGITAL CH 394 (+)	“	“	14	B 42
DIGITAL CH 394 (–)	“	“	14	A 42
DIGITAL CH 395 (+)	“	“	14	A 43
DIGITAL CH 395 (–)	“	“	14	B 43
DIGITAL CH 396 (+)	“	“	14	B 44
DIGITAL CH 396 (–)	“	“	14	A 44
DIGITAL CH 397 (+)	“	“	14	A 45
DIGITAL CH 397 (–)	“	“	14	B 45
DIGITAL CH 398 (+)	“	“	14	B 46
DIGITAL CH 398 (–)	“	“	14	A 46
DIGITAL CH 399 (+)	“	“	14	A 47
DIGITAL CH 399 (–)	“	“	14	B 47
DIGITAL CH 400 (+)	“	“	14	B 48
DIGITAL CH 400 (–)	“	“	14	A 48
DIGITAL CH 401 (+)	“	“	14	C 1
DIGITAL CH 401 (–)	“	“	14	D 1
DIGITAL CH 402 (+)	“	“	14	D 2
DIGITAL CH 402 (–)	“	“	14	C 2
DIGITAL CH 403 (+)	“	“	14	C 3
DIGITAL CH 403 (–)	“	“	14	D 3
DIGITAL CH 404 (+)	“	“	14	D 4
DIGITAL CH 404 (–)	“	“	14	C 4
DIGITAL CH 405 (+)	“	“	14	C 5
DIGITAL CH 405 (–)	“	“	14	D 5
DIGITAL CH 406 (+)	“	“	14	D 6

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 406 (–)	“	“	14	C 6
DIGITAL CH 407 (+)	“	“	14	C 7
DIGITAL CH 407 (–)	“	“	14	D 7
DIGITAL CH 408 (+)	“	“	14	D 8
DIGITAL CH 408 (–)	“	“	14	C 8
DIGITAL CH 409 (+)	“	“	14	C 9
DIGITAL CH 409 (–)	“	“	14	D 9
DIGITAL CH 410 (+)	“	“	14	D 10
DIGITAL CH 410 (–)	“	“	14	C 10
DIGITAL CH 411 (+)	“	“	14	C 11
DIGITAL CH 411 (–)	“	“	14	D 11
DIGITAL CH 412 (+)	“	“	14	D 12
DIGITAL CH 412 (–)	“	“	14	C 12
DIGITAL CH 413 (+)	“	“	14	C 13
DIGITAL CH 413 (–)	“	“	14	D 13
DIGITAL CH 414 (+)	“	“	14	D 14
DIGITAL CH 414 (–)	“	“	14	C 14
DIGITAL CH 415 (+)	“	“	14	C 15
DIGITAL CH 415 (–)	“	“	14	D 15
DIGITAL CH 416 (+)	“	“	14	D 16
DIGITAL CH 416 (–)	“	“	14	C 16
DIGITAL CH 417 (+)	C17	“	14	C 17
DIGITAL CH 417 (–)	“	“	14	D 17
DIGITAL CH 418 (+)	“	“	14	D 18
DIGITAL CH 418 (–)	“	“	14	C 18
DIGITAL CH 419 (+)	“	“	14	C 19
DIGITAL CH 419 (–)	“	“	14	D 19
DIGITAL CH 420 (+)	“	“	14	D 20
DIGITAL CH 420 (–)	“	“	14	C 20
DIGITAL CH 421 (+)	“	“	14	C 21
DIGITAL CH 421 (–)	“	“	14	D 21
DIGITAL CH 422 (+)	“	“	14	D 22
DIGITAL CH 422 (–)	“	“	14	C 22
DIGITAL CH 423 (+)	“	“	14	C 23
DIGITAL CH 423 (–)	“	“	14	D 23
DIGITAL CH 424 (+)	“	“	14	D 24
DIGITAL CH 424 (–)	“	“	14	C 24
DIGITAL CH 425 (+)	“	“	14	C 25
DIGITAL CH 425 (–)	“	“	14	D 25
DIGITAL CH 426 (+)	“	“	14	D 26
DIGITAL CH 426 (–)	“	“	14	C 26
DIGITAL CH 427 (+)	“	“	14	C 27
DIGITAL CH 427 (–)	“	“	14	D 27
DIGITAL CH 428 (+)	“	“	14	D 28
DIGITAL CH 428 (–)	“	“	14	C 28
DIGITAL CH 429 (+)	“	“	14	C 29
DIGITAL CH 429 (–)	“	“	14	D 29
DIGITAL CH 430 (+)	“	“	14	D 30
DIGITAL CH 430 (–)	“	“	14	C 30
DIGITAL CH 431 (+)	“	“	14	C 31
DIGITAL CH 431 (–)	“	“	14	D 31
DIGITAL CH 432 (+)	“	“	14	D 32

Table A.21—Digital channels *(continued)*

CTI name	Legacy system	Recommended attributes	Slot	Pin
DIGITAL CH 432 (–)	“	“	14	C 32
DIGITAL CH 433 (+)	“	“	14	C 33
DIGITAL CH 433 (–)	“	“	14	D 33
DIGITAL CH 434 (+)	“	“	14	D 34
DIGITAL CH 434 (–)	“	“	14	C 34
DIGITAL CH 435 (+)	“	“	14	C 35
DIGITAL CH 435 (–)	“	“	14	D 35
DIGITAL CH 436 (+)	“	“	14	D 36
DIGITAL CH 436 (–)	“	“	14	C 36
DIGITAL CH 437 (+)	“	“	14	C 37
DIGITAL CH 437 (–)	“	“	14	D 37
DIGITAL CH 438 (+)	“	“	14	D 38
DIGITAL CH 438 (–)	“	“	14	C 38
DIGITAL CH 439 (+)	“	“	14	C 39
DIGITAL CH 439 (–)	“	“	14	D 39
DIGITAL CH 440 (+)	C17	“	14	D 40
DIGITAL CH 440 (–)	“	“	14	C 40
DIGITAL CH 441 (+)	“	“	14	C 41
DIGITAL CH 441 (–)	“	“	14	D 41
DIGITAL CH 442 (+)	“	“	14	D 42
DIGITAL CH 442 (–)	“	“	14	C 42
DIGITAL CH 443 (+)	“	“	14	C 43
DIGITAL CH 443 (–)	“	“	14	D 43
DIGITAL CH 444 (+)	“	“	14	D 44
DIGITAL CH 444 (–)	“	“	14	C 44
DIGITAL CH 445 (+)	“	“	14	C 45
DIGITAL CH 445 (–)	“	“	14	D 45
DIGITAL CH 446 (+)	“	“	14	D 46
DIGITAL CH 446 (–)	“	“	14	C 46
DIGITAL CH 447 (+)	“	“	14	C 47
DIGITAL CH 447 (–)	“	“	14	D 47
DIGITAL CH 448 (+)	“	“	14	D 48
DIGITAL CH 448 (–)	“	“	14	C 48

Table A.22—Clocks

CTI name	Legacy systems	Recommended attributes	Slot	Pin
TOCYCLE+	CASS, LM-STAR, TETS, IAIS, C17, RAF	Max voltage: Diff ECL Max freq: 20 MHz	23,24	H 11
TOCYCLE–	“	“	23,24	H 12
EXTCLK+	“	“	23,24	H 13
EXTCLK–	“	“	23,24	H 14
FEXCLK+	CASS, LM-STAR, IAIS, C17, RAF	Max voltage: Diff ECL Max freq: 50 MHz	23,24	H 15
FEXCLK–	“	“	23,24	H 16
CLUTCH1+	CASS, LM-STAR, TETS, IAIS, C17, RAF	“	23,24	H 17
CLUTCH1–	“	“	23,24	H 18
CLUTCH2+	“	“	23,24	H 19
CLUTCH2–	“	“	23,24	G 11
EXT1	CASS, LM-STAR, IAIS, C17, RAF	“	23,24	G 12
EXT2	“	“	23,24	G 13
EXT REF+	“	Voltage: –1.29 V Max freq: 50 MHz	23,24	G 14
EXT REF–	“	“	23,24	G 14
SYNC 1+	TETS, C17, RAF	ECL: 20 MHz	23,24	G 15
SYNC 1 –	“	“	23,24	G 15
SYNC 2 +	“	“	23,24	G 16
SYNC 2 –	“	“	23,24	G 16
SYNC 3 +	“	“	23,24	G 17
SYNC 3 –	“	“	23,24	G 17
SYNC 4 +	“	“	23,24	G 18
SYNC 4 –	“	“	23,24	G 18
Clock 1 +	“	“	23,24	F 16
Clock 1 –	“	“	23,24	F 16
Clock 2 +	“	“	23,24	F 17
Clock 2 –	“	“	23,24	F 17
Clock 3 +	“	“	23,24	F 18
Clock 3 –	“	“	23,24	F 18
Clock 4 +	“	“	23,24	F 19
Clock 4 –	“	“	23,24	F 19
Kelvin ground 4			23, 24	G 19

Table A.23—External control

CTI name	Legacy systems	Recommended attributes	Slot	Pin
ExtCtrl CH 1 (+)	RAF	Voltage: TTL Max freq: 50 MHz Impedance: 50 Ω Max current: 60 mA	27	A 1
ExtCtrl CH 1 (–)	"	"	27	B 1
ExtCtrl CH 2 (+)	"	"	27	B 2
ExtCtrl CH 2 (–)	"	"	27	A 2
ExtCtrl CH 3 (+)	IFTE, ESTS, RAF	"	27	A 3
ExtCtrl CH 3 (–)	"	"	27	B 3
ExtCtrl CH 4 (+)	"	"	27	B 4
ExtCtrl CH 4 (–)	"	"	27	A 4
ExtCtrl CH 5 (+)	IFTE, ESTS	"	27	A 5
ExtCtrl CH 5 (–)	"	"	27	B 5
ExtCtrl CH 6 (+)	"	"	27	B 6
ExtCtrl CH 6 (–)	"	"	27	A 6
ExtCtrl CH 7 (+)	IFTE, ESTS, RAF	"	27	A 7
ExtCtrl CH 7 (–)	"	"	27	B 7
ExtCtrl CH 8 (+)	ESTS	"	27	B 8
ExtCtrl CH 8 (–)	"	"	27	A 8
ExtCtrl CH 9 (+)	IFTE	"	27	A 9
ExtCtrl CH 9 (–)	"	"	27	B 9
ExtCtrl CH 10 (+)	ESTS	"	27	B 10
ExtCtrl CH 10 (–)	"	"	27	A 10
ExtCtrl CH 11 (+)	IFTE	"	27	A 11
ExtCtrl CH 11 (–)	"	"	27	B 11
ExtCtrl CH 12 (+)	IFTE, ESTS	"	27	B 12
ExtCtrl CH 12 (–)	"	"	27	A 12
ExtCtrl CH 13 (+)	"	"	27	A 13
ExtCtrl CH 13 (–)	"	"	27	B 13
ExtCtrl CH 14 (+)	IFTE	"	27	B 14
ExtCtrl CH 14 (–)	"	"	27	A 14
ExtCtrl CH 15 (+)	IFTE, ESTS	"	27	A 15
ExtCtrl CH 15 (–)	"	"	27	B 15
ExtCtrl CH 16 (+)	"	"	27	B 16
ExtCtrl CH 16 (–)	"	"	27	A 16
ExtCtrl CH 17 (+)	IFTE	"	27	A 17
ExtCtrl CH 17 (–)	"	"	27	B 17
ExtCtrl CH 18 (+)	ESTS	"	27	B 18
ExtCtrl CH 18 (–)	"	"	27	A 18
ExtCtrl CH 19 (+)	IFTE	"	27	A 19
ExtCtrl CH 19 (–)	"	"	27	B 19
ExtCtrl CH 20 (+)	"	"	27	B 20
ExtCtrl CH 20 (–)	"	"	27	A 20
ExtCtrl CH 21 (+)	"	"	27	A 21
ExtCtrl CH 21 (–)	"	"	27	B 21
ExtCtrl CH 22 (+)	"	"	27	B 22
ExtCtrl CH 22 (–)	"	"	27	A 22
ExtCtrl CH 23 (+)	"	"	27	A 23
ExtCtrl CH 23 (–)	"	"	27	B 23

Table A.23—External control *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
ExtCtrl CH 24 (+)	IFTE, ESTS	“	27	B 24
ExtCtrl CH 24 (–)	“	“	27	A 24
ExtCtrl CH 25 (+)	“	“	27	A 25
ExtCtrl CH 25 (–)	“	“	27	B 25
ExtCtrl CH 26 (+)	IFTE	“	27	B 26
ExtCtrl CH 26 (–)	“	“	27	A 26
ExtCtrl CH 27 (+)	“	“	27	A 27
ExtCtrl CH 27 (–)	“	“	27	B 27
ExtCtrl CH 28 (+)	“	“	27	C 1
ExtCtrl CH 28 (–)	“	“	27	D 1
ExtCtrl CH 29 (+)	“	“	27	D 2
ExtCtrl CH 29 (–)	“	“	27	C 2
ExtCtrl CH 30 (+)	“	“	27	C 3
ExtCtrl CH 30 (–)	“	“	27	D 3
ExtCtrl CH 31 (+)	“	“	27	D 4
ExtCtrl CH 31 (–)	“	“	27	C 4
ExtCtrl CH 32 (+)	“	“	27	C 5
ExtCtrl CH 32 (–)	“	“	27	D 5
ExtCtrl CH 33 (+)	“	“	27	D 6
ExtCtrl CH 33 (–)	“	“	27	C 6
ExtCtrl CH 34 (+)	“	“	27	C 7
ExtCtrl CH 34 (–)	“	“	27	D 7
ExtCtrl CH 35 (+)	“	“	27	D 8
ExtCtrl CH 35 (–)	“	“	27	C 8
ExtCtrl CH 36 (+)	“	“	27	C 9
ExtCtrl CH 36 (–)	“	“	27	D 9
ExtCtrl CH 37 (+)	“	“	27	D 10
ExtCtrl CH 37 (–)	“	“	27	C 10
ExtCtrl CH 38 (+)	“	“	27	C 11
ExtCtrl CH 38 (–)	“	“	27	D 11
ExtCtrl CH 39 (+)	“	“	27	D 12
ExtCtrl CH 39 (–)	“	“	27	C 12
ExtCtrl CH 40 (+)	“	“	27	C 13
ExtCtrl CH 40 (–)	“	“	27	D 13
ExtCtrl CH 41 (+)	“	“	27	D 14
ExtCtrl CH 41 (–)	“	“	27	C 14
ExtCtrl CH 42 (+)	“	“	27	C 15
ExtCtrl CH 42 (–)	“	“	27	D 15
ExtCtrl CH 43 (+)	“	“	27	D 16
ExtCtrl CH 43 (–)	“	“	27	C 16
ExtCtrl CH 44 (+)	“	“	27	C 17
ExtCtrl CH 44 (–)	“	“	27	D 17
ExtCtrl CH 45 (+)	“	“	27	D 18
ExtCtrl CH 45 (–)	“	“	27	C 18
ExtCtrl CH 46 (+)	“	“	27	C 19
ExtCtrl CH 46 (–)	“	“	27	D 19
ExtCtrl CH 47 (+)	“	“	27	D 20
ExtCtrl CH 47 (–)	“	“	27	C 20
ExtCtrl CH 48 (+)	“	“	27	C 21
ExtCtrl CH 48 (–)	“	“	27	D 21
ExtCtrl CH 49 (+)	“	“	27	D 22
ExtCtrl CH 49 (–)	“	“	27	C 22

Table A.23—External control *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
ExtCtrl CH 50 (+)	None	"	27	C 23
ExtCtrl CH 50 (–)	None	"	27	D 23
ExtCtrl CH 51 (+)	None	"	27	D 24
ExtCtrl CH 51 (–)	None	"	27	C 24
ExtCtrl CH 52 (+)	IFTE	"	27	C 25
ExtCtrl CH 52 (–)	"	"	27	D 25
ExtCtrl CH 53 (+)	"	"	27	D 26
ExtCtrl CH 53 (–)	"	"	27	C 26
ExtCtrl CH 54 (+)	"	"	27	C 27
ExtCtrl CH 54 (–)	"	"	27	D 27

Table A.24—Spectrum analyzer

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Spec An Trig	IFTE, ESTS, TETS, RAF	Freq: 3 GHz Impedance: 50 Ω Voltage: –120 to 30 dBm	21,22	C 12
Spec An Det Video	IFTE, ESTS, RAF	"	21,22	D 12
Spec An RFMEAS IN	TETS, RAF	"	21,22	E 12
321.4 MHz IF	CASS, LM-STAR	Voltage: ± 8 V Current: 1 A Freq: 160 MHz Impedance: 50 Ω	21,22	D 13

Table A.25—Modulation source

CTI name	Legacy systems	Recommended attributes	Slot	Pin
RF_Mod_Src_1_PM	ESTS, TETS, RAF	Freq: 3 GHz Impedance: 50 Ω Voltage: –120 to 30 dBm	21,22	B 15
RF_Mod_Src_1_AM	ESTS, TETS , RAF	"	21,22	B 16
RF_Mod_Src_1_FM	"	"	21,22	B 17
AM-MOD_Src_2	ESTS, RAF	"	21,22	C 15
PAM-MOD_Src_2	"	"	21,22	C 16
FM-MOD_Src_2	ESTS	"	21,22	C 17
PAM-MOD/PAM_TRIG_Src_3	RAF	"	21,22	D 15
AM-MOD_Src_3	"	"	21,22	D 16
FM-MOD_Src_3	None	"	21,22	D 17
Stim 1 Ext. Trig. IN	C17	Contractor specific	21,22	E 13
Stim 2 Ext. Trig. IN	"		21,22	E 14
Stim 3 Ext. Trig. IN			21,22	E 15
MTA Ext. Trig. IN	C17		21,22	E 16

Table A.26—Power meter

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Power Meter Recorder	TETS	Freq: 3 GHz Impedance: 50 Ω Voltage: –120 to 30 dBm	21,22	B 11
Power Meter Ext Trig In	CASS, LM-STAR, TETS	Freq: 106 MHz Impedance: 50 Ω Current: 1 A Voltage: ± 8 V	21,22	C 11
Power Meter Video1 Out	LM-STAR, RAF	Freq: 3 GHz Impedance: 50 Ω Voltage: –120 to 30 dBm	21,22	D 11
Power Meter Video2 Out	LM-STAR	"	21,22	E 11

Table A.27—Hi current dc load

CTI name	Comments	Recommended attributes	Slot	Pin
High Current Load 1A (+)	IFTE, CASS	Max currrent: 30 A Max voltage: 500 V Max power: 750 W (See NOTE)	1,2	B 16
High Current Load 1B (+)	"		1,2	A 17
High Current Load 1A (–)	"	"	1,2	A 16
High Current Load 1B (–)	"		1,2	B 17
High Current Load 2A (+)	IFTE	Max currrent: 30 A Max voltage: 50 V (See NOTE)	1,2	B 18
High Current Load 2B (+)	"		1,2	A 19
High Current Load 2A (–)	"	"	1,2	A 18
High Current Load 2B (–)	"		1,2	B 19
NOTE—Pins are tied together to handle maximum current.				

Table A.28—AC/DC load

CTI name	Legacy systems	Recommended attributes	Slot	Pin
DC Load 3 (+)	IFTE, ESTS	Max voltage: 50 Vdc or 50 Vrms Max current: 15 A Max power: 300 W	1,2	D 16
DC Load 3 (–)	"		1,2	C 16
DC Load 4 (+)	IFTE	Max voltage: 50 Vdc or 50 Vrms Max current: 15 A Max power: 300 W	1,2	C 17
DC Load 4 (–)	"		1,2	D 17
DC Load 5 (+)	"	Max voltage: 130 Vdc or 130 Vrms Max current: 15 A Max power: 750 W	1,2	D 18
DC Load 5 (–)	"	Max voltage: 130 Vdc or 130 Vrms Max current: 15 A Max power: 750 W	1,2	C 18
DC Load 6 (+)	"	Max voltage: 130 Vdc or 130 Vrms Max current: 15 A Max power: 750 W	1,2	C 19
DC Load 6 (–)	"	Max voltage: 130 Vdc or 130 Vrms Max current: 15 A Max power: 750 W	1,2	D 19
DC Load 7 (+)	"	Max voltage: 130 Vdc or 130 Vrms Max current: 15 A Max power: 750 W	29	A 17
DC Load 7 (–)	"	Max voltage: 130 Vdc or 130 Vrms Max current: 15 A Max power: 750 W	29	A 18
DC Load 8 (+)	"	Max voltage: 250 Vdc or 250 Vrms Max current: 5 A Max power: 750 W	29	A 19
DC Load 8 (–)	"	"	29	A 20

Table A.29—Load modulation

CTI name	Legacy system	Recommended attributes	Slot	Pin
Load Modulation Control (+)	IFTE, RAF	Max voltage: 10 V Freq range: dc – 8 kHz Max current: 100 mA	1,2	E 19
Load Modulation Control (–)	"	"	1,2	E 18

Table A.30—High current DCPS

CTI name	Legacy system	Recommended attributes	Slot	Pin
High Current DCPS 1(A+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF		6	A 1
High Current DCPS 1(B+)		Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 2
High Current DCPS 1A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 1
High Current DCPS 1B(–)			6	A 2
High Current DCPS 2A(+)	CASS, LM-STAR, ESTS, TETS, IAIS, C17	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 3
High Current DCPS 2B(+)			6	B 4
High Current DCPS 2A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 3
High Current DCPS 2B(–)			6	A 4
High Current DCPS 3A(+)	CASS, LM-STAR, ESTS, IAIS, C17	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 5
High Current DCPS 3B(+)			6	B 6
High Current DCPS 3A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 5
High Current DCPS 3B(–)			6	A 6
High Current DCPS 4A(+)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 7
High Current DCPS 4B(+)			6	B 8
High Current DCPS 4A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 7
High Current DCPS 4B(–)			6	A 8
High Current DCPS 5 A(+)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 9
High Current DCPS 5B(+)			6	B 10
High Current DCPS 5 A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 9
High Current DCPS 5B(–)			6	A 10
High Current DCPS 6A(+)	CASS, LM-STAR, IAIS	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 11
High Current DCPS 6B(+)		Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 12
High Current DCPS 6A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 11
High Current DCPS 6B(–)			6	A 12
High Current DCPS 7A(+)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 13
High Current DCPS 7B(+)			6	B 14
High Current DCPS 7A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 13
High Current DCPS 7B(–)			6	A 14
High Current DCPS 8A(+)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	A 15
High Current DCPS 8B(+)			6	B 16
High Current DCPS 8A(–)	"	Max voltage: 50 V Max current: 33 A (See NOTE)	6	B 15
High Current DCPS 8B(–)			6	A 16
High Current DCPS 9A(+)	IFTE	Max voltage: 16V Max current: 21 A (See NOTE)	1,2	H 18
High Current DCPS 9B(+)			1,2	G 19
High Current DCPS 9A(–)	"	Max voltage: 16V Max current: 21 A (See NOTE)	1,2	G 18
High Current DCPS 9B(–)			1,2	H 19
High Current DCPS 10A(+)	IFTE	Max voltage: 16V Max current: 21 A (See NOTE)	29	C 17
High Current DCPS 10B(+)			29	C 19
High Current DCPS 10A(–)	"	Max voltage: 16V Max current: 21 A (See NOTE)	29	C 18
High Current DCPS 10B(–)			29	C 20
NOTE—Pins are tied together to handle maximum current.				

Table A.31—DCPS

CTI name	Legacy systems	Recommended attributes	Slot	Pin
DCPS 11(+)	IFTE, CASS, LM-STAR, ESTS, TETS, C17, RAF	Max voltage: 100 V Max current: 5 A	6	A 17
DCPS 11(–)	"	Max voltage: 100 V Max current: 5 A	6	A 18
DCPS 12(+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, RAF	Max voltage: 100 V Max current: 5 A	6	B 18
DCPS 12(–)	"	Max voltage: 100 V Max current: 5 A	6	B 17
DCPS 13(+)	"	Max voltage: 100 V Max current: 5 A	6	C 1
DCPS 13(–)	"	Max voltage: 100 V Max current: 5 A	6	C 2
DCPS 14(+)	IFTE, CASS, ESTS, TETS, RAF	Max voltage: 100 V Max current: 5 A	6	C 3
DCPS 14(–)	"	Max voltage: 100 V Max current: 5 A	6	C 4
DCPS 15(+)	IFTE, ESTS, TETS, RAF	Max voltage: 100 V Max current: 5 A	6	C 5
DCPS 15(–)	"	Max voltage: 100 V Max current: 5 A	6	C 6
DCPS 16(+)	"	Max voltage: 100 V Max current: 5 A	6	C 7
DCPS 16(–)	"	Max voltage: 100 V Max current: 5 A	6	C 8
DCPS 17(+)	"	Max voltage: 100 V Max current: 5 A	6	C 9
DCPS 17(–)	"	Max voltage: 100 V Max current: 5 A	6	C 10
DCPS 18(+)	"	Max voltage: 100 V Max current: 5 A	6	C 11
DCPS 18(–)	"	Max voltage: 100 V Max current: 5 A	6	C 12
DCPS 19(+)	IFTE, ESTS, TETS	Max voltage: 100 V Max current: 5 A	6	C 13
DCPS 19(–)	"	Max voltage: 100 V Max current: 5 A	6	C 14
DCPS 20(+)	CASS	Max voltage: 450 V Max current: 15 A	6	C 15
DCPS 20(–)	"	Max voltage: 450 V Max current: 15 A	6	C 16
DCPS 21(+)	"	Max voltage: 450 V Max current: 15 A	6	C 17
DCPS 21(–)	"	Max voltage: 450 V Max current: 15 A	6	C 18
DCPS 22(+)	"	Max voltage: 100 V Max current: 5 A	1,2	F 18
DCPS 22(–)	"	Max voltage: 100 V Max current: 5 A	1,2	F 19

Table A.32—ACPS 3 phase

CTI name	Legacy system	Recommended attributes	Slot	Pin
Fixed 3 Phase PHA1	CASS, LM-STAR, IAIS	Max voltage: 115 Vac Max current: 30 A Max freq: 400 Hz (See NOTE)	1,2	A 1
Fixed 3 Phase PHA2			1,2	B 1
Fixed 3 Phase PHB1	"	Max voltage: 115 Vac Max current: 30 A Max freq: 400 Hz (See NOTE)	1,2	A 2
Fixed 3 Phase PHB2			1,2	B 2
Fixed 3 Phase PHC1	"	Max voltage: 115 Vac Max current: 30 A Max freq: 400 Hz (See NOTE)	1,2	A 3
Fixed 3 Phase PHC2			1,2	B 3
Fixed 3 Phase N1	"	Max voltage: 115 Vac Max current: 30 A Max freq: 400 Hz (See NOTE)	1,2	A 4
Fixed 3 Phase N2			1,2	B 4
ACPS Chassis ground 1	"	Max voltage: 115 Vac Max current: 30 A Max freq: 400 Hz (See NOTE)	1,2	A 5
ACPS Chassis ground 2			1,2	B 5
NOTE—Pins are tied together to handle maximum current.				

Table A.33—ACPS programmable

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Programmable ACPS1 Phase	IFTE, CASS, LM-STAR, IAIS, C17, RAF	Max voltage: 270 Vac Max current: 10 A Freq range: 45 Hz to 5000 Hz	6	A 19
Programmable ACPS1 Return	"	"	6	B 19
Programmable ACPS2 Phase	IFTE, CASS, ESTS, IAIS, C17	"	1,2	C 1
Programmable ACPS2 Return	"	"	1,2	D 1
Programmable ACPS3 Phase	IFTE, CASS, ESTS, IAIS, C17	"	1,2	D 2
Programmable ACPS3 Return	"	"	1,2	C 2
Programmable ACPS4 Phase	IFTE, CASS, ESTS	"	1,2	C 3
Programmable ACPS4 Return	"	"	1,2	D 3
ACPS Chassis ground 3	IFTE, CASS, LM-STAR, ESTS, IAIS, C17	"	1,2	D 4
ACPS Chassis ground 4	IFTE, CASS, LM-STAR, ESTS, IAIS	"	1,2	C 4
Aux. Phase A	ESTS	Max voltage: 30.5 V Max current: 2 A Freq: 400 Hz	28	C47
Aux. Phase A Return	"	"	28	D47
Aux. Phase B	"	"	28	D48
Aux. Phase B Return	"	"	28	C48
Aux. Phase C	"	"	28	C49
Aux. Phase C Return	"	"	28	D49
Aux. Phase D	"	"	28	D50
Aux. Phase D Return	"	"	28	C50

Table A.34—DCPS sense

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Sense DCPS1 (+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, C17, RAF	Max voltage: 50 V Current: 0.5 A	7	A 1
Sense DCPS1 (–)	"	"	7	B 1
Sense DCPS2 (+)	CASS, LM-STAR, ESTS, TETS, IAIS, C17	"	7	B 2
Sense DCPS2 (–)	"	"	7	A 2
Sense DCPS3 (+)	CASS, LM-STAR, ESTS, IAIS, C17	"	7	A 3
Sense DCPS3 (–)	"	"	7	B 3
Sense DCPS4 (+)	"	"	7	B 4
Sense DCPS4 (–)	"	"	7	A 4
Sense DCPS5 (+)	CASS, LM-STAR, ESTS, C17	"	7	C 1
Sense DCPS5 (–)	"	"	7	D 1
Sense DCPS6 (+)	CASS, LM-STAR	"	7	D 2
Sense DCPS6 (–)	"	"	7	C 2
Sense DCPS7 (+)	"	"	7	C 3
Sense DCPS7 (–)	"	"	7	D 3
Sense DCPS8 (+)	"	"	7	D 4
Sense DCPS8 (–)	"	"	7	C 4
Sense DCPS9 (+)	IFTE, LM-STAR, IAIS, C17	Max voltage: 16 V Current: 0.5 A	8	A 1
Sense DCPS9 (–)	"	"	8	B 1
Sense DCPS10 (+)	IFTE, LM-STAR, IAIS	"	8	B 2
Sense DCPS10 (–)	"	"	8	A 2
Sense DCPS11 (+)	IFTE, CASS, LM-STAR, ESTS, TETS, IAIS, RAF	Max voltage: 100 V Current: 0.5 A	8	A 3
Sense DCPS11 (–)	"	"	8	B 3
Sense DCPS12 (+)	TETS, RAF	"	8	B 4
Sense DCPS12 (–)	"	"	8	A 4
Sense DCPS13 (+)	IFTE, CASS, TETS, RAF	"	8	A 5
Sense DCPS13 (–)	"	"	8	B 5
Sense DCPS14 (+)	ESTS, TETS, RAF	"	8	B 6
Sense DCPS14 (–)	"	"	8	A 6
Sense DCPS15 (+)	IFTE, TETS, RAF	"	8	A 7
Sense DCPS15 (–)	"	"	8	B 7
Sense DCPS16 (+)	"	"	8	B 8
Sense DCPS16 (–)	"	"	8	A 8
Sense DCPS17 (+)	IFTE, ESTS, TETS, RAF	"	8	A 9
Sense DCPS17 (–)	"	"	8	B 9
Sense DCPS18 (+)	IFTE, TETS	"	8	B 10
Sense DCPS18 (–)	"	"	8	A 10
Sense DCPS19 (+)	"	"	8	A 11
Sense DCPS19 (–)	"	"	8	B 11
Sense DCPS20 (+)	CASS	Max voltage: 450 V Current: 0.5 A	3	A 46
Sense DCPS20 (–)	"	"	3	B 46
Sense DCPS21 (+)	"	"	3	B 47
Sense DCPS21 (–)	"	"	3	A 47
Sense DCPS22 (+)	"	Max voltage: 100 V Current: 0.5 A	28	A 43
Sense DCPS22 (–)	"	"	28	B 43

Table A.35—ACPS sense

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Sense ACPS1 Phase	IFTE, CASS, LM-STAR, IAIS, C17	Max voltage: 270 Vac Max current: 0.5 A Freq range: 45 Hz to 5000 Hz	1,2	C 5
Sense ACPS1 Return	“	“	1,2	D 5
Sense ACPS2 Phase	IFTE, CASS, ESTS, IAIS, C17	“	1,2	D 6
Sense ACPS2 Return	“	“	1,2	C 6
Sense ACPS3 Phase	“	“	1,2	C 7
Sense ACPS3 Return	“	“	1,2	D 7
Sense ACPS4 Phase	IFTE, CASS, ESTS	“	1,2	D 8
Sense ACPS4 Return	“	“	1,2	C 8

Table A.36—Load sense

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Load Sense (+)	CASS, LM-STAR	Max voltage: 500 V Max current: 500 mA	3	A 48
Load Sense (–)	“	“	3	B 48
Load Chassis ground 1	LM-STAR	N/A	3	A 49
Load Chassis ground 2	“	N/A	3	B 49

Table A.37—28 V control

CTI name	Legacy systems	Recommended attributes	Slot	Pin
28 V Control (+)	IFTE, CASS, ESTS, TETS	Max voltage: 28 V Current: 1 A	19	B 50
28 V Control (–)	“	“	19	A 50

Table A.38—Coax 1x4 switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 01 (or 1x4 sw 01)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	Impedance: 50 Ω Freq range: dc to 1 GHz Max power: 2 W Max Capacitance: 15 pF VSWR Max: (@ 1 GHz) 1.15+0.01f (GHz) RF leakage: –60 db @ 1Ghz Bandwidth: 100 MHz to 1.2 GHz Path Resistance: <2 Ω @ 1 mA Current: 2 A	4	A 1
Coax 2x8 MUX 01 (or 1x4 sw 01)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 2
Coax 2x8 MUX 01 (or 1x4 sw 01)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 3
Coax 2x8 MUX 01 (or 1x4 sw 01)	IFTE, CASS, LM-STAR, ESTS, TETS	"	4	A 4
Coax 2x8 MUX 01 (or 1x4 sw 01)	IFTE, CASS, LM-STAR	"	4	A 5
Coax 2x8 MUX 01 (or 1x4 sw 02)	IFTE, CASS, LM-STAR, ESTS, RAF	"	4	A 6
Coax 2x8 MUX 01 (or 1x4 sw 02)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 7
Coax 2x8 MUX 01 (or 1x4 sw 02)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 8
Coax 2x8 MUX 01 (or 1x4 sw 02)	IFTE, CASS, LM-STAR, ESTS, TETS	"	4	A 9
Coax 2x8 MUX 01 (or 1x4 sw 02)	IFTE, CASS, LM-STAR	"	4	A 10
Coax 2x8 MUX 02 (or 1x4 sw 03)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 11
Coax 2x8 MUX 02 (or 1x4 sw 03)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 12
Coax 2x8 MUX 02 (or 1x4 sw 03)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 13
Coax 2x8 MUX 02 (or 1x4 sw 03)	IFTE, CASS, LM-STAR, ESTS, TETS	"	4	A 14
Coax 2x8 MUX 02 (or 1x4 sw 03)	IFTE, CASS, LM-STAR	"	4	A 15
Coax 2x8 MUX 02 (or 1x4 sw 04)	IFTE, CASS, LM-STAR, ESTS, RAF	"	4	A 16
Coax 2x8 MUX 02 (or 1x4 sw 04)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	"	4	A 17

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 02 (or 1x4 sw 04)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	A 18
Coax 2x8 MUX 02 (or 1x4 sw 04)	IFTE, CASS, LM-STAR, ESTS, TETS	“	4	A 19
Coax 2x8 MUX 02 (or 1x4 sw 04)	IFTE, CASS, LM-STAR	“	4	A 20
Coax 2x8 MUX 03 (or 1x4 sw 05)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 1
Coax 2x8 MUX 03 (or 1x4 sw 05)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 2
Coax 2x8 MUX 03 (or 1x4 sw 05)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 3
Coax 2x8 MUX 03 (or 1x4 sw 05)	IFTE, CASS, LM-STAR, ESTS, TETS	“	4	B 4
Coax 2x8 MUX 03 (or 1x4 sw 05)	IFTE, CASS, LM-STAR	“	4	B 5
Coax 2x8 MUX 03 (or 1x4 sw 06)	IFTE, CASS, LM-STAR, ESTS, RAF	“	4	B 6
Coax 2x8 MUX 03 (or 1x4 sw 06)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 7
Coax 2x8 MUX 03 (or 1x4 sw 06)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 8
Coax 2x8 MUX 03 (or 1x4 sw 06)	IFTE, CASS, LM-STAR, ESTS, TETS	“	4	B 9
Coax 2x8 MUX 03 (or 1x4 sw 06)	IFTE, CASS, LM-STAR	“	4	B 10
Coax 2x8 MUX 04 (or 1x4 sw 07)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 11
Coax 2x8 MUX 04 (or 1x4 sw 07)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 12
Coax 2x8 MUX 04 (or 1x4 sw 07)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	B 13
Coax 2x8 MUX 04 (or 1x4 sw 07)	IFTE, CASS, LM-STAR, ESTS, TETS	“	4	B 14
Coax 2x8 MUX 04 (or 1x4 sw 07)	IFTE, CASS, LM-STAR	“	4	B 15
Coax 2x8 MUX 04 (or 1x4 sw 08)	IFTE, CASS, LM-STAR, ESTS, RAF	“	4	C 1

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 04 (or 1x4 sw 08)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	C 2
Coax 2x8 MUX 04 (or 1x4 sw 08)	IFTE, CASS, LM-STAR, ESTS, TETS, RAF	“	4	C 3
Coax 2x8 MUX 04 (or 1x4 sw 08)	IFTE, CASS, LM-STAR, ESTS, TETS	“	4	C 4
Coax 2x8 MUX 04 (or 1x4 sw 08)	IFTE, CASS, LM-STAR	“	4	C 5
Coax 2x8 MUX 05 (or 1x4 sw 09)	IFTE, CASS, LM-STAR, ESTS RAF	“	4	C 6
Coax 2x8 MUX 05 (or 1x4 sw 09)	IFTE, CASS, LM-STAR, ESTS, RAF	“	4	C 7
Coax 2x8 MUX 05 (or 1x4 sw 09)	IFTE, CASS, LM-STAR, ESTS, RAF	“	4	C 8
Coax 2x8 MUX 05 (or 1x4 sw 09)	IFTE, CASS, LM-STAR, ESTS	“	4	C 9
Coax 2x8 MUX 05 (or 1x4 sw 09)	IFTE, CASS, LM-STAR	“	4	C 10
Coax 2x8 MUX 05 (or 1x4 sw 10)	IFTE, CASS, LM-STAR	“	4	C 11
Coax 2x8 MUX 05 (or 1x4 sw 10)	IFTE, CASS, LM-STAR	“	4	C 12
Coax 2x8 MUX 05 (or 1x4 sw 10)	IFTE, CASS, LM-STAR	“	4	C 13
Coax 2x8 MUX 05 (or 1x4 sw 10)	IFTE, CASS, LM-STAR	“	4	C 14
Coax 2x8 MUX 05 (or 1x4 sw 10)	IFTE, CASS, LM-STAR	“	4	C 15
Coax 2x8 MUX 06 (or 1x4 sw 11)	IFTE, CASS, LM-STAR, RAF	“	21,22	A 1
Coax 2x8 MUX 06 (or 1x4 sw 11)	IFTE, CASS, LM-STAR, RAF	“	21,22	A 2
Coax 2x8 MUX 06 (or 1x4 sw 11)	IFTE, CASS, LM-STAR, RAF	“	21,22	A 3
Coax 2x8 MUX 06 (or 1x4 sw 11)	IFTE, CASS, LM-STAR	“	21,22	A 4
Coax 2x8 MUX 06 (or 1x4 sw 11)	IFTE, CASS, LM-STAR	“	21,22	A 5
Coax 2x8 MUX 06 (or 1x4 sw 12)	IFTE, CASS, LM-STAR, RAF	“	21,22	A 6
Coax 2x8 MUX 06 (or 1x4 sw 12)	IFTE, CASS, LM-STAR, RAF	“	21,22	A 7
Coax 2x8 MUX 06 (or 1x4 sw 12)	IFTE, CASS, LM-STAR, RAF	“	21,22	A 8
Coax 2x8 MUX 06 (or 1x4 sw 12)	IFTE, CASS, LM-STAR	“	21,22	A 9
Coax 2x8 MUX 06 (or 1x4 sw 12)	IFTE, CASS, LM-STAR	“	21,22	A 10
Coax 2x8 MUX 07 (or 1x4 sw 13)	IFTE, CASS, LM-STAR, RAF	“	21,22	B 1
Coax 2x8 MUX 07 (or 1x4 sw 13)	IFTE, CASS, LM-STAR, RAF	“	21,22	B 2

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 07 (or 1x4 sw 13)	IFTE, CASS, LM-STAR, RAF	“	21,22	B 3
Coax 2x8 MUX 07 (or 1x4 sw 13)	IFTE, CASS, LM-STAR	“	21,22	B 4
Coax 2x8 MUX 07 (or 1x4 sw 13)	IFTE, CASS, LM-STAR	“	21,22	B 5
Coax 2x8 MUX 07 (or 1x4 sw 14)	IFTE, CASS, LM-STAR, RAF	“	21,22	B 6
Coax 2x8 MUX 07 (or 1x4 sw 14)	IFTE, CASS, LM-STAR, RAF	“	21,22	B 7
Coax 2x8 MUX 07 (or 1x4 sw 14)	IFTE, CASS, LM-STAR, RAF	“	21,22	B 8
Coax 2x8 MUX 07 (or 1x4 sw 14)	IFTE, CASS, LM-STAR	“	21,22	B 9
Coax 2x8 MUX 07 (or 1x4 sw 14)	IFTE, CASS, LM-STAR	“	21,22	B 10
Coax 2x8 MUX 08 (or 1x4 sw 15)	IFTE, CASS, LM-STAR, RAF	“	21,22	C 1
Coax 2x8 MUX 08 (or 1x4 sw 15)	IFTE, CASS, LM-STAR, RAF	“	21,22	C 2
Coax 2x8 MUX 08 (or 1x4 sw 15)	IFTE, CASS, LM-STAR, RAF	“	21,22	C 3
Coax 2x8 MUX 08 (or 1x4 sw 15)	IFTE, CASS, LM-STAR,	“	21,22	C 4
Coax 2x8 MUX 08 (or 1x4 sw 15)	IFTE, CASS, LM-STAR	“	21,22	C 5
Coax 2x8 MUX 08 (or 1x4 sw 16)	IFTE, CASS, LM-STAR, RAF	“	21,22	C 6
Coax 2x8 MUX 08 (or 1x4 sw 16)	IFTE, CASS, LM-STAR, RAF	“	21,22	C 7
Coax 2x8 MUX 08 (or 1x4 sw 16)	IFTE, CASS, LM-STAR, RAF	“	21,22	C 8
Coax 2x8 MUX 08 (or 1x4 sw 16)	IFTE, CASS, LM-STAR,	“	21,22	C 9
Coax 2x8 MUX 08 (or 1x4 sw 16)	IFTE, CASS, LM-STAR	“	21,22	C 10
Coax 2x8 MUX 09 (or 1x4 sw 17)	IFTE, CASS, LM-STAR,	“	21,22	D 1
Coax 2x8 MUX 09 (or 1x4 sw 17)	IFTE, CASS, LM-STAR,	“	21,22	D 2
Coax 2x8 MUX 09 (or 1x4 sw 17)	IFTE, CASS, LM-STAR,	“	21,22	D 3
Coax 2x8 MUX 09 (or 1x4 sw 17)	IFTE, CASS, LM-STAR,	“	21,22	D 4
Coax 2x8 MUX 09 (or 1x4 sw 17)	IFTE, CASS, LM-STAR,	“	21,22	D 5
Coax 2x8 MUX 09 (or 1x4 sw 18)	IFTE, CASS, LM-STAR,	“	21,22	D 6
Coax 2x8 MUX 09 (or 1x4 sw 18)	IFTE, CASS, LM-STAR,	“	21,22	D 7
Coax 2x8 MUX 09 (or 1x4 sw 18)	IFTE, CASS, LM-STAR,	“	21,22	D 8
Coax 2x8 MUX 09 (or 1x4 sw 18)	IFTE, CASS, LM-STAR,	“	21,22	D 9

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 09 (or 1x4 sw 18)	IFTE, CASS, LM-STAR,	“	21,22	D 10
Coax 2x8 MUX 10 (or 1x4 sw 19)	IFTE, CASS, LM-STAR, RAF	“	21,22	E 1
Coax 2x8 MUX 10 (or 1x4 sw 19)	IFTE, CASS, LM-STAR, RAF	“	21,22	E 2
Coax 2x8 MUX 10 (or 1x4 sw 19)	IFTE, CASS, LM-STAR, RAF	“	21,22	E 3
Coax 2x8 MUX 10 (or 1x4 sw 19)	IFTE, CASS, LM-STAR,	“	21,22	E 4
Coax 2x8 MUX 10 (or 1x4 sw 19)	IFTE, CASS, LM-STAR,	“	21,22	E 5
Coax 2x8 MUX 10 (or 1x4 sw 20)	IFTE, CASS, LM-STAR,	“	21,22	E 6
Coax 2x8 MUX 10 (or 1x4 sw 20)	IFTE, CASS, LM-STAR,	“	21,22	E 7
Coax 2x8 MUX 10 (or 1x4 sw 20)	IFTE, CASS, LM-STAR,	“	21,22	E 8
Coax 2x8 MUX 10 (or 1x4 sw 20)	IFTE, CASS, LM-STAR,	“	21,22	E 9
Coax 2x8 MUX 10 (or 1x4 sw 20)	IFTE, CASS, LM-STAR,	“	21,22	E 10
Coax 2x8 MUX 11 (or 1x4 sw 21)	IFTE, CASS, LM-STAR, RAF	“	21,22	F 1
Coax 2x8 MUX 11 (or 1x4 sw 21)	IFTE, CASS, LM-STAR, RAF	“	21,22	F 2
Coax 2x8 MUX 11 (or 1x4 sw 21)	IFTE, CASS, LM-STAR, RAF	“	21,22	F 3
Coax 2x8 MUX 11 (or 1x4 sw 21)	IFTE, CASS, LM-STAR,	“	21,22	F 4
Coax 2x8 MUX 11 (or 1x4 sw 21)	IFTE, CASS, LM-STAR,	“	21,22	F 5
Coax 2x8 MUX 11 (or 1x4 sw 22)	IFTE, CASS, LM-STAR, RAF	“	21,22	F 6
Coax 2x8 MUX 11 (or 1x4 sw 22)	IFTE, CASS, LM-STAR, RAF	“	21,22	F 7
Coax 2x8 MUX 11 (or 1x4 sw 22)	IFTE, CASS, LM-STAR, RAF	“	21,22	F 8
Coax 2x8 MUX 11 (or 1x4 sw 22)	IFTE, CASS, LM-STAR,	“	21,22	F 9
Coax 2x8 MUX 11 (or 1x4 sw 22)	IFTE, CASS, LM-STAR,	“	21,22	F 10
Coax 2x8 MUX 12 (or 1x4 sw 23)	IFTE, CASS, LM-STAR, RAF	“	21,22	G 1
Coax 2x8 MUX 12 (or 1x4 sw 23)	IFTE, CASS, LM-STAR, RAF	“	21,22	G 2
Coax 2x8 MUX 12 (or 1x4 sw 23)	IFTE, CASS, LM-STAR, RAF	“	21,22	G 3
Coax 2x8 MUX 12 (or 1x4 sw 23)	IFTE, CASS, LM-STAR,	“	21,22	G 4
Coax 2x8 MUX 12 (or 1x4 sw 23)	IFTE, CASS, LM-STAR,	“	21,22	G 5
Coax 2x8 MUX 12 (or 1x4 sw 24)	IFTE, CASS, LM-STAR, RAF	“	21,22	G 6

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 12 (or 1x4 sw 24)	IFTE, CASS, LM-STAR, RAF	“	21,22	G 7
Coax 2x8 MUX 12 (or 1x4 sw 24)	IFTE, CASS, LM-STAR, RAF	“	21,22	G 8
Coax 2x8 MUX 12 (or 1x4 sw 24)	IFTE, CASS, LM-STAR,	“	21,22	G 9
Coax 2x8 MUX 12 (or 1x4 sw 24)	IFTE, CASS, LM-STAR,	“	21,22	G 10
Coax 2x8 MUX 13 (or 1x4 sw 25)	IFTE, CASS, LM-STAR, RAF	“	21,22	H 1
Coax 2x8 MUX 13 (or 1x4 sw 25)	IFTE, CASS, LM-STAR, RAF	“	21,22	H 2
Coax 2x8 MUX 13 (or 1x4 sw 25)	IFTE, CASS, LM-STAR, RAF	“	21,22	H 3
Coax 2x8 MUX 13 (or 1x4 sw 25)	IFTE, CASS, LM-STAR,	“	21,22	H 4
Coax 2x8 MUX 13 (or 1x4 sw 25)	IFTE, CASS, LM-STAR,	“	21,22	H 5
Coax 2x8 MUX 13 (or 1x4 sw 26)	IFTE, CASS, LM-STAR, RAF	“	21,22	H 6
Coax 2x8 MUX 13 (or 1x4 sw 26)	IFTE, CASS, LM-STAR, RAF	“	21,22	H 7
Coax 2x8 MUX 13 (or 1x4 sw 26)	IFTE, CASS, LM-STAR, RAF	“	21,22	H 8
Coax 2x8 MUX 13 (or 1x4 sw 26)	IFTE, CASS, LM-STAR,	“	21,22	H 9
Coax 2x8 MUX 13 (or 1x4 sw 26)	IFTE, CASS, LM-STAR,	“	21,22	H 10
Coax 2x8 MUX 14 (or 1x4 sw 27)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 1
Coax 2x8 MUX 14 (or 1x4 sw 27)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 2
Coax 2x8 MUX 14 (or 1x4 sw 27)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 3
Coax 2x8 MUX 14 (or 1x4 sw 27)	IFTE, CASS, LM-STAR	“	23,24	A 4
Coax 2x8 MUX 14 (or 1x4 sw 27)	IFTE, CASS, LM-STAR,	“	23,24	A 5
Coax 2x8 MUX 14 (or 1x4 sw 28)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 6
Coax 2x8 MUX 14 (or 1x4 sw 28)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 7
Coax 2x8 MUX 14 (or 1x4 sw 28)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 8
Coax 2x8 MUX 14 (or 1x4 sw 28)	IFTE, CASS, LM-STAR,	“	23,24	A 9
Coax 2x8 MUX 15 (or 1x4 sw 29)	IFTE, CASS, LM-STAR,	“	23,24	A 10
Coax 2x8 MUX 15 (or 1x4 sw 29)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 11
Coax 2x8 MUX 15 (or 1x4 sw 29)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 12
Coax 2x8 MUX 15 (or 1x4 sw 29)	IFTE, CASS, LM-STAR, RAF	“	23,24	A 13

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 15 (or 1x4 sw 29)	IFTE, CASS, LM-STAR,	“	23,24	A 14
Coax 2x8 MUX 15 (or 1x4 sw 30)	IFTE, CASS, LM-STAR,	“	23,24	A 15
Coax 2x8 MUX 15 (or 1x4 sw 30)	CASS, LM-STAR	“	23,24	B 1
Coax 2x8 MUX 15 (or 1x4 sw 30)	IFTE, CASS, LM-STAR,	“	23,24	B 2
Coax 2x8 MUX 15 (or 1x4 sw 30)	IFTE, CASS, LM-STAR,	“	23,24	B 3
Coax 2x8 MUX 15 (or 1x4 sw 30)	IFTE, CASS, LM-STAR,	“	23,24	B 4
Coax 2x8 MUX 16 (or 1x4 sw 31)	IFTE, CASS, LM-STAR,	“	23,24	B 5
Coax 2x8 MUX 16 (or 1x4 sw 31)	CASS, LM-STAR, RAF	“	23,24	B 6
Coax 2x8 MUX 16 (or 1x4 sw 31)	IFTE, CASS, LM-STAR, RAF	“	23,24	B 7
Coax 2x8 MUX 16 (or 1x4 sw 31)	IFTE, CASS, LM-STAR, RAF	“	23,24	B 8
Coax 2x8 MUX 16 (or 1x4 sw 31)	IFTE, CASS, LM-STAR	“	23,24	B 9
Coax 2x8 MUX 16 (or 1x4 sw 32)	IFTE, CASS, LM-STAR	“	23,24	B 10
Coax 2x8 MUX 16 (or 1x4 sw 32)	CASS, LM-STAR, RAF	“	23,24	B 11
Coax 2x8 MUX 16 (or 1x4 sw 32)	IFTE, CASS, LM-STAR, RAF	“	23,24	B 12
Coax 2x8 MUX 16 (or 1x4 sw 32)	IFTE, CASS, LM-STAR, RAF	“	23,24	B 13
Coax 2x8 MUX 16 (or 1x4 sw 32)	IFTE, CASS, LM-STAR	“	23,24	B 14
Coax 2x8 MUX 17 (or 1x4 sw 33)	IFTE, CASS, LM-STAR	“	23,24	B 15
Coax 2x8 MUX 17 (or 1x4 sw 33)	CASS, LM-STAR, RAF	“	23,24	C 1
Coax 2x8 MUX 17 (or 1x4 sw 33)	IFTE, CASS, LM-STAR, RAF	“	23,24	C 2
Coax 2x8 MUX 17 (or 1x4 sw 33)	IFTE, CASS, LM-STAR, RAF	“	23,24	C 3
Coax 2x8 MUX 17 (or 1x4 sw 33)	IFTE, CASS, LM-STAR	“	23,24	C 4
Coax 2x8 MUX 17 (or 1x4 sw 34)	IFTE, CASS, LM-STAR	“	23,24	C 5
Coax 2x8 MUX 17 (or 1x4 sw 34)	CASS, LM-STAR, RAF	“	23,24	C 6
Coax 2x8 MUX 17 (or 1x4 sw 34)	IFTE, CASS, LM-STAR, RAF	“	23,24	C 7
Coax 2x8 MUX 17 (or 1x4 sw 34)	IFTE, CASS, LM-STAR, RAF	“	23,24	C 8
Coax 2x8 MUX 17 (or 1x4 sw 34)	IFTE, LM-STAR	“	23,24	C 9
Coax 2x8 MUX 18 (or 1x4 sw 35)	IFTE, LM-STAR	“	23,24	C 10

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 18 (or 1x4 sw 35)	CASS, LM-STAR, RAF	“	23,24	C 11
Coax 2x8 MUX 18 (or 1x4 sw 35)	IFTE, CASS, LM-STAR, RAF	“	23,24	C 12
Coax 2x8 MUX 18 (or 1x4 sw 35)	IFTE, CASS, LM-STAR, RAF	“	23,24	C 13
Coax 2x8 MUX 18 (or 1x4 sw 35)	IFTE, LM-STAR	“	23,24	C 14
Coax 2x8 MUX 18 (or 1x4 sw 36)	IFTE, LM-STAR	“	23,24	C 15
Coax 2x8 MUX 18 (or 1x4 sw 36)	CASS, LM-STAR, RAF	“	23,24	D 1
Coax 2x8 MUX 18 (or 1x4 sw 36)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 2
Coax 2x8 MUX 18 (or 1x4 sw 36)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 3
Coax 2x8 MUX 18 (or 1x4 sw 36)	IFTE, LM-STAR	“	23,24	D 4
Coax 2x8 MUX 19 (or 1x4 sw 37)	IFTE, LM-STAR	“	23,24	D 5
Coax 2x8 MUX 19 (or 1x4 sw 37)	CASS, LM-STAR, RAF	“	23,24	D 6
Coax 2x8 MUX 19 (or 1x4 sw 37)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 7
Coax 2x8 MUX 19 (or 1x4 sw 37)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 8
Coax 2x8 MUX 19 (or 1x4 sw 37)	IFTE, LM-STAR	“	23,24	D 9
Coax 2x8 MUX 19 (or 1x4 sw 38)	IFTE, LM-STAR	“	23,24	D 10
Coax 2x8 MUX 19 (or 1x4 sw 38)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 11
Coax 2x8 MUX 19 (or 1x4 sw 38)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 12
Coax 2x8 MUX 19 (or 1x4 sw 38)	IFTE, CASS, LM-STAR, RAF	“	23,24	D 13
Coax 2x8 MUX 19 (or 1x4 sw 38)	IFTE, LM-STAR	“	23,24	D 14
Coax 2x8 MUX 20 (or 1x4 sw 39)	IFTE, LM-STAR	“	23,24	D 15
Coax 2x8 MUX 20 (or 1x4 sw 39)	IFTE, CASS, LM-STAR, RAF	“	23,24	E 1
Coax 2x8 MUX 20 (or 1x4 sw 39)	IFTE, CASS, LM-STAR, RAF	“	23,24	E 2
Coax 2x8 MUX 20 (or 1x4 sw 39)	IFTE, CASS, LM-STAR, RAF	“	23,24	E 3
Coax 2x8 MUX 20 (or 1x4 sw 39)	IFTE, LM-STAR	“	23,24	E 4
Coax 2x8 MUX 20 (or 1x4 sw 40)	IFTE, LM-STAR	“	23,24	E 5
Coax 2x8 MUX 20 (or 1x4 sw 40)	CASS, LM-STAR	“	23,24	E 6
Coax 2x8 MUX 20 (or 1x4 sw 40)	IFTE, CASS, LM-STAR, RAF	“	23,24	E 7

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 20 (or 1x4 sw 40)	IFTE, CASS, LM-STAR, RAF	“	23,24	E 8
Coax 2x8 MUX 20 (or 1x4 sw 40)	IFTE, LM-STAR, RAF	“	23,24	E 9
Coax 2x8 MUX 21 (or 1x4 sw 41)	IFTE, LM-STAR, RAF	“	23,24	E 10
Coax 2x8 MUX 21 (or 1x4 sw 41)	IFTE, CASS	“	23,24	E 11
Coax 2x8 MUX 21 (or 1x4 sw 41)	IFTE, CASS	“	23,24	E 12
Coax 2x8 MUX 21 (or 1x4 sw 41)	IFTE, CASS	“	23,24	E 13
Coax 2x8 MUX 21 (or 1x4 sw 41)	IFTE	“	23,24	E 14
Coax 2x8 MUX 21 (or 1x4 sw 42)	IFTE	“	23,24	E 15
Coax 2x8 MUX 21 (or 1x4 sw 42)	IFTE, CASS	“	23,24	F 1
Coax 2x8 MUX 21 (or 1x4 sw 42)	IFTE, CASS	“	23,24	F 2
Coax 2x8 MUX 21 (or 1x4 sw 42)	IFTE, CASS	“	23,24	F 3
Coax 2x8 MUX 21 (or 1x4 sw 42)	IFTE	“	23,24	F 4
Coax 2x8 MUX 15 (or 1x4 sw 29)	IFTE	“	23,24	F 5
Coax 2x8 MUX 22 (or 1x4 sw 43)	IFTE	“	23,24	F 6
Coax 2x8 MUX 22 (or 1x4 sw 43)	IFTE	“	23,24	F 7
Coax 2x8 MUX 22 (or 1x4 sw 43)	IFTE	“	23,24	F 8
Coax 2x8 MUX 22 (or 1x4 sw 43)	IFTE	“	23,24	F 9
Coax 2x8 MUX 22 (or 1x4 sw 43)	IFTE	“	23,24	F 10
Coax 2x8 MUX 22 (or 1x4 sw 44)	IFTE	“	23,24	F 11
Coax 2x8 MUX 22 (or 1x4 sw 44)	IFTE	“	23,24	F 12
Coax 2x8 MUX 22 (or 1x4 sw 44)	IFTE	“	23,24	F 13
Coax 2x8 MUX 22 (or 1x4 sw 44)	IFTE	“	23,24	F 14
Coax 2x8 MUX 22 (or 1x4 sw 44)	IFTE	“	23,24	F 15
Coax 2x8 MUX 23 (or 1x4 sw 45)		“	23,24	G 1
Coax 2x8 MUX 23 (or 1x4 sw 45)	IFTE	“	23,24	G 2
Coax 2x8 MUX 23 (or 1x4 sw 45)	IFTE	“	23,24	G 3
Coax 2x8 MUX 23 (or 1x4 sw 45)	IFTE	“	23,24	G 4

Table A.38—Coax 1x4 switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Coax 2x8 MUX 23 (or 1x4 sw 45)	IFTE	“	23,24	G 5
Coax 2x8 MUX 23 (or 1x4 sw 46)		“	23,24	G 6
Coax 2x8 MUX 23 (or 1x4 sw 46)	IFTE	“	23,24	G 7
Coax 2x8 MUX 23 (or 1x4 sw 46)	IFTE	“	23,24	G 8
Coax 2x8 MUX 23 (or 1x4 sw 46)	IFTE	“	23,24	G 9
Coax 2x8 MUX 23 (or 1x4 sw 46)	IFTE	“	23,24	G 10
Coax 2x8 MUX 24 (or 1x4 sw 47)		“	23,24	H 1
Coax 2x8 MUX 24 (or 1x4 sw 47)	IFTE	“	23,24	H 2
Coax 2x8 MUX 24 (or 1x4 sw 47)	IFTE	“	23,24	H 3
Coax 2x8 MUX 24 (or 1x4 sw 47)	IFTE	“	23,24	H 4
Coax 2x8 MUX 24 (or 1x4 sw 47)	IFTE	“	23,24	H 5
Coax 2x8 MUX 24 (or 1x4 sw 48)		“	23,24	H 6
Coax 2x8 MUX 24 (or 1x4 sw 48)	IFTE	“	23,24	H 7
Coax 2x8 MUX 24 (or 1x4 sw 48)	IFTE	“	23,24	H 8
Coax 2x8 MUX 24 (or 1x4 sw 48)	IFTE	“	23,24	H 9
Coax 2x8 MUX 24 (or 1x4 sw 48)	IFTE	“	23,24	H10
NOTE—Capacitance measured at the CTI, which includes CSW, internal cabling, and switch capacitance, shall not exceeded 100 pF.				

Table A.39—1x2 coax switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
1x2 CSW 1 Common	LM-STAR, C17	Impedance: 50 Ω Freq range: dc to 1 GHz Max power: 2 W Max Capacitance: 15 pF VSWR max: (@ 1 GHz): 1.15+0.01f (GHz) RF leakage: –60 db @ 1 GHz Bandwidth: 100 MHz to 1.2 GHz Path resistance: <2 Ω @ 1 mA	21,22	F 11
1x2 CSW 1 Port1	“	“	21,22	F 12
1x2 CSW 1 Port2	“	“	21,22	F 13
1x2 CSW 2 Common	“	“	21,22	F 14
1x2 CSW 2 Port1	“	“	21,22	F 15
1x2 CSW 2 Port2	“	“	21,22	F 16
1x2 CSW 3 Common	“	“	21,22	F 17
1x2 CSW 3 Port1	“	“	21,22	F 18
1x2 CSW 3 Port2	“	“	21,22	F 19
1x2 CSW 4 Common	“	“	21,22	G 11
1x2 CSW 4 Port1	“	“	21,22	G 12
1x2 CSW 4 Port2	“	“	21,22	G 13
1x2 CSW 5 Common	“	“	21,22	G 14
1x2 CSW 5 Port1	“	“	21,22	G 15
1x2 CSW 5 Port2	“	“	21,22	G 16
1x2 CSW 6 Common	“	“	21,22	G 17
1x2 CSW 6 Port1	“	“	21,22	G 18
1x2 CSW 6 Port2	“	“	21,22	G 19
1x2 CSW 7 Common	LM-STAR	“	21,22	H 11
1x2 CSW 7 Port1	“	“	21,22	H 12
1x2 CSW 7 Port2	“	“	21,22	H 13
1x2 CSW 8 Common	“	“	21,22	H 14
1x2 CSW 8 Port1	“	“	21,22	H 15
1x2 CSW 8 Port2	“	“	21,22	H 16
1x2 CSW 9 Common	“	“	21,22	H 17
1x2 CSW 9 Port1	“	“	21,22	H 18
1x2 CSW 9 Port2	“	“	21,22	H 19
NOTE—Capacitance measured at the CTI, which includes CSW, internal cabling, and switch capacitance, shall not exceed 100 pF.				

Table A.40—1x4 power switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
1x4 PSW1 Common	CASS, LM-STAR, IAIS	Max voltage: 300 V Max current: 18.75 A Switch impedance: <20 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	1,2	A 6
1x4 PSW1 Port1	"	"	1,2	A 7
1x4 PSW1 Port2	"	"	1,2	A 8
1x4 PSW1 Port3	"	"	1,2	A 9
1x4 PSW1 Port4	"	"	1,2	A 10
1x4 PSW2 Common	"	"	1,2	A 11
1x4 PSW2 Port1	"	"	1,2	A 12
1x4 PSW2 Port2	"	"	1,2	A 13
1x4 PSW2 Port3	"	"	1,2	A 14
1x4 PSW2 Port4	"	"	1,2	A 15
1x4 PSW3 Common	"	"	1,2	B 6
1x4 PSW3 Port1	"	"	1,2	B 7
1x4 PSW3 Port2	"	"	1,2	B 8
1x4 PSW3 Port3	"	"	1,2	B 9
1x4 PSW3 Port4	"	"	1,2	B 10
1x4 PSW4 Common	"	"	1,2	B 11
1x4 PSW4 Port1	"	"	1,2	B 12
1x4 PSW4 Port2	"	"	1,2	B 13
1x4 PSW4 Port3	"	"	1,2	B 14
1x4 PSW4 Port4	"	"	1,2	B 15
1x4 PSW5 Common	"	"	1,2	C 11
1x4 PSW5 Port1	"	"	1,2	C 12
1x4 PSW5 Port2	"	"	1,2	C 13
1x4 PSW5 Port3	"	"	1,2	C 14
1x4 PSW5 Port4	"	"	1,2	C 15
1x4 PSW6 Common	IAIS	Max voltage: 300 V Max current: 20 A Switch impedance: <100 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	1,2	D 11
1x4 PSW6 Port1	"	"	1,2	D 12
1x4 PSW6 Port2	"	"	1,2	D 13
1x4 PSW6 Port3	"	"	1,2	D 14
1x4 PSW6 Port4			1,2	D 15

Table A.41—1x2 power switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
1x2 PSW 1 Common	LM-STAR, C17	Max voltage: 220 Vac/dc Max current: 10 A Switch path resistance: <100 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	1,2	E 1
1x2 PSW 1 Port1	"	"	1,2	E 2
1x2 PSW 1 Port2	"	"	1,2	E 3
1x2 PSW 2 Common	"	"	1,2	F 1
1x2 PSW 2 Port1	"	"	1,2	F 2
1x2 PSW 2 Port2	"	"	1,2	F 3
1x2 PSW 3 Common	"	"	1,2	F 4
1x2 PSW 3 Port1	"	"	1,2	F 5
1x2 PSW 3 Port2	"	"	1,2	F 6
1x2 PSW 4 Common	CASS, LM-STAR, C17	Max voltage: 300 V Max current: 20 A Switch path Resistance: <20 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	1,2	F 7
1x2 PSW 4 Port1	"	"	1,2	F 8
1x2 PSW 4 Port2	"	"	1,2	F 9
1x2 PSW 5 Common	IFTE, LM-STAR, TETS, C17, RAF	Max voltage: 220 Vac/dc Max current: 10 A Switch path resistance: <100 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	1,2	F 10
1x2 PSW 5 Port1	"	"	1,2	F 11
1x2 PSW 5 Port2	LM-STAR, C17	"	1,2	F 12
1x2 PSW 6 Common	IFTE, LM-STAR, TETS, C17	"	1,2	F 13
1x2 PSW 6 Port1	"	"	1,2	F 14
1x2 PSW 6 Port2	LM-STAR, C17	"	1,2	F 15
1x2 PSW 7 Common	IFTE, LM-STAR, TETS, C17, RAF	"	1,2	G 1
1x2 PSW 7 Port1	"	"	1,2	G 2
1x2 PSW 7 Port2	LM-STAR, C17	"	1,2	G 3
1x2 PSW 8 Common	IFTE, LM-STAR, TETS, C17, RAF	"	1,2	G 4
1x2 PSW 8 Port1	"	"	1,2	G 5
1x2 PSW 8 Port2	LM-STAR, C17	"	1,2	G 6
1x2 PSW 9 Common	IFTE, LM-STAR, TETS, C17	"	1,2	G 7
1x2 PSW 9 Port1	"	"	1,2	G 8
1x2 PSW 9 Port2	LM-STAR,C17	"	1,2	G 9
1x2 PSW 10 Common	IFTE, LM-STAR, TETS, C17	"	1,2	G 10
1x2 PSW 10 Port1	"	"	1,2	G 11
1x2 PSW 10 Port2	LM-STAR,C17	"	1,2	G 12
1x2 PSW 11 Common	LM-STAR, TETS, C17	"	1,2	G 13
1x2 PSW 11 Port1	"	"	1,2	G 14
1x2 PSW 11 Port2	LM-STAR, C17	"	1,2	G 15

Table A.41—1x2 power switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
1x2 PSW 12 Common	LM-STAR, TETS, C17	"	1,2	H 1
1x2 PSW 12 Port1	"	"	1,2	H 2
1x2 PSW 12 Port2	LM-STAR, C17	"	1,2	H 3
1x2 PSW 13 Common	"	"	1,2	H 4
1x2 PSW 13 Port1	"	"	1,2	H 5
1x2 PSW 13 Port2	"	"	1,2	H 6
1x2 PSW 14 Common	None	"	1,2	H 7
1x2 PSW 14 Port1	None	"	1,2	H 8
1x2 PSW 14 Port2	None	"	1,2	H 9
1x2 PSW 15 Common	None	"	1,2	H 10
1x2 PSW 15 Port1	None	"	1,2	H 11
1x2 PSW 15 Port2	None	"	1,2	H 12
1x2 PSW 16 Common	None	"	1,2	H 13
1x2 PSW 16 Port1	None	"	1,2	H 14
1x2 PSW 16 Port2	None	"	1,2	H 15
1x2 PSW 17 Common	IFTE, CASS, LM-STAR	Max voltage: 300 V Max current: 10 A Switch path resistance: <40 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	29	A 1
1x2 PSW 17 Port1	"	"	29	A 2
1x2 PSW 17 Port2	CASS, LM-STAR	"	29	A 3
1x2 PSW 18 Common	IFTE, CASS, LM-STAR	"	29	A 4
1x2 PSW 18 Port1	"	"	29	A 5
1x2 PSW 18 Port2	CASS, LM-STAR	"	29	A 6
1x2 PSW 19 Common	IFTE, CASS, LM-STAR	"	29	A 7
1x2 PSW 19 Port1	"	"	29	A 8
1x2 PSW 19 Port2	CASS, LM-STAR	"	29	A 9
1x2 PSW 20 Common	IFTE, CASS, LM-STAR	"	29	A 10
1x2 PSW 20 Port1	"	"	29	A 11
1x2 PSW 20 Port2	CASS, LM-STAR	"	29	A 12
1x2 PSW 21 Common	IFTE, CASS, LM-STAR	"	29	B 1
1x2 PSW 21 Port1	"	"	29	B 2
1x2 PSW 21 Port2	CASS, LM-STAR	"	29	B 3
1x2 PSW 22 Common	IFTE, CASS, LM-STAR	"	29	B 4
1x2 PSW 22 Port1	"	"	29	B 5
1x2 PSW 22 Port2	CASS, LM-STAR	"	29	B 6
1x2 PSW 23 Common	IFTE, CASS, LM-STAR	"	29	B 7
1x2 PSW 23 Port1	"	"	29	B 8
1x2 PSW 23 Port2	CASS, LM-STAR	"	29	B 9
1x2 PSW 24 Common	IFTE, CASS, LM-STAR	"	29	B 10
1x2 PSW 24 Port1	"	"	29	B 11
1x2 PSW 24 Port2	CASS, LM-STAR	"	29	B 12
1x2 PSW 25 Common	IFTE, CASS	"	29	C 1
1x2 PSW 25 Port1	"	"	29	C 2
1x2 PSW 25 Port2	CASS	"	29	C 3

Table A.41—1x2 power switch *(continued)*

CTI name	Legacy systems	Recommended attributes	Slot	Pin
1x2 PSW 26 Common	IFTE, CASS, C17	“	29	C 4
1x2 PSW 26 Port1	“	“	29	C 5
1x2 PSW 26 Port2	CASS, C17	“	29	C 6
1x2 PSW 27 Common	IFTE, CASS, C17	“	29	C 7
1x2 PSW 27 Port1	“	“	29	C 8
1x2 PSW 27 Port2	CASS, C17	“	29	C 9
1x2 PSW 28 Common	IFTE, CASS, C17	“	29	C 10
1x2 PSW 28 Port1	“	“	29	C 11
1x2 PSW 28 Port2	CASS, C17	“	29	C 12

Table A.42—DPDT power switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
2x2 PSW 1 Common	CASS	Max voltage: 300 V Max current: 20 A Switch impedance: <20 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	29	A 13
2x2 PSW 1 Port1NC	“	“	29	B 13
2x2 PSW 1 Port1NO	“	“	29	C 13
2x2 PSW 1 Common	“	“	29	A 14
2x2 PSW 1 Port2NC	“	“	29	B 14
2x2 PSW 1 Port2NO	“	“	29	C 14
2x2 PSW 2 Common	“	“	29	A 15
2x2 PSW 2 Port1NC	“	“	29	B 15
2x2 PSW 2 Port1NO	“	“	29	C 15
2x2 PSW 2 Common	“	“	29	A 16
2x2 PSW 2 Port2NC	“	“	29	B 16
2x2 PSW 2 Port2NO	“	“	29	C 16

Table A.43—1x1 power switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
1x1 PSW1 Common	CASS, TETS, C17, RAF	Max voltage: 220 Vac/dc Max current: 10 A Switch path resistance: <100 mΩ @ max current Freq. range: dc to 1 kHz Breakdown voltage: 1 kV	1,2	C 9
1x1 PSW1 Port1	"	"	1,2	C 10
1x1 PSW2 Common	"	"	1,2	D 9
1x1 PSW2 Port1	"	"	1,2	D 10
1x1 PSW3 Common	"	"	1,2	E 4
1x1 PSW3 Port1	"	"	1,2	E 5
1x1 PSW4 Common	"	"	1,2	E 6
1x1 PSW4 Port1	"	"	1,2	E 7
1x1 PSW5 Common	"	"	1,2	E 8
1x1 PSW5 Port1	"	"	1,2	E 9
1x1 PSW6 Common	"	"	1,2	E 10
1x1 PSW6 Port1	"	"	1,2	E 11
1x1 PSW7 Common	"	"	1,2	E 12
1x1 PSW7 Port1	"	"	1,2	E 13
1x1 PSW8 Common	"	"	1,2	E 14
1x1 PSW8 Port1	"	"	1,2	E 15
1x1 PSW9 Common	"	"	1,2	E 16
1x1 PSW9 Port1	"	"	1,2	E 17
1x1 PSW10 Common	"	"	1,2	F 16
1x1 PSW10 Port1	"	"	1,2	F 17
1x1 PSW11 Common	"	"	1,2	G 16
1x1 PSW11 Port1	"	"	1,2	G 17
1x1 PSW12 Common	"	"	1,2	H 16
1x1 PSW12 Port1	"	"	1,2	H 17

Table A.44—1x8 switch

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Signal 1x8 Mux1 Common (+)	ESTS, TETS	Max current: 2 A Max voltage: 300 Vdc/ 300 Vac Max switching power (dc): 60 W Max switching power (ac): 125 VA Max freq: 10 MHz	15	B 14
Signal 1x8 Mux1 Common (–)	“	“	15	A 14
Signal 1x8 Mux1 Channel 1(+)	“	“	15	A 15
Signal 1x8 Mux1 Channel 1(–)	“	“	15	B 15
Signal 1x8 Mux1 Channel 2(+)	“	“	15	B 16
Signal 1x8 Mux1 Channel 2(–)	“	“	15	A 16
Signal 1x8 Mux1 Channel 3(+)	“	“	15	A 17
Signal 1x8 Mux1 Channel 3(–)	“	“	15	B 17
Signal 1x8 Mux1 Channel 4(+)	“	“	15	B 18
Signal 1x8 Mux1 Channel 4(–)	“	“	15	A 18
Signal 1x8 Mux1 Channel 5(+)	“	“	15	A 19
Signal 1x8 Mux1 Channel 5(–)	“	“	15	B 19
Signal 1x8 Mux1 Channel 6(+)	“	“	15	B 20
Signal 1x8 Mux1 Channel 6(–)	“	“	15	A 20
Signal 1x8 Mux1 Channel 7(+)	TETS	“	15	A 21
Signal 1x8 Mux1 Channel 7(–)	“	“	15	B 21
Signal 1x8 Mux1 Channel 8(+)	“	“	15	B 22
Signal 1x8 Mux1 Channel 8(–)	“	“	15	A 22
Signal 1x8 Mux2 Common (+)	ESTS, TETS	“	15	A 23
Signal 1x8 Mux2 Common (–)	“	“	15	B 23
Signal 1x8 Mux2 Channel 1(+)	“	“	15	B 24
Signal 1x8 Mux2 Channel 1(–)	“	“	15	A 24
Signal 1x8 Mux2 Channel 2(+)	“	“	15	A 25
Signal 1x8 Mux2 Channel 2(–)	“	“	15	B 25
Signal 1x8 Mux2 Channel 3(+)	“	“	15	B 26
Signal 1x8 Mux2 Channel 3(–)	“	“	15	A 26
Signal 1x8 Mux2 Channel 4(+)	“	“	15	A 27
Signal 1x8 Mux2 Channel 4(–)	“	“	15	B 27
Signal 1x8 Mux2 Channel 5(+)	“	“	15	B 28
Signal 1x8 Mux2 Channel 5(–)	“	“	15	A 28
Signal 1x8 Mux2 Channel 6(+)	“	“	15	A 29
Signal 1x8 Mux2 Channel 6(–)	“	“	15	B 29
Signal 1x8 Mux2 Channel 7(+)	TETS	“	15	B 30
Signal 1x8 Mux2 Channel 7(–)	“	“	15	A 30
Signal 1x8 Mux2 Channel 8(+)	“	“	15	A 31
Signal 1x8 Mux2 Channel 8(–)	“	“	15	B 31
Signal 1x8 Mux3 Common (+)	ESTS, TETS	“	15	B 32
Signal 1x8 Mux3 Common (–)	“	“	15	A 32
Signal 1x8 Mux3 Channel 1(+)	“	“	15	A 33
Signal 1x8 Mux3 Channel 1(–)	“	“	15	B 33
Signal 1x8 Mux3 Channel 2(+)	“	“	15	B 34
Signal 1x8 Mux3 Channel 2(–)	“	“	15	A 34
Signal 1x8 Mux3 Channel 3(+)	“	“	15	A 35
Signal 1x8 Mux3 Channel 3(–)	“	“	15	B 35
Signal 1x8 Mux3 Channel 4(+)	“	“	15	B 36
Signal 1x8 Mux3 Channel 4(–)	“	“	15	A 36
Signal 1x8 Mux3 Channel 5(+)	“	“	15	A 37

Table A.44—1x8 switch (continued)

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Signal 1x8 Mux3 Channel 5(–)	“	“	15	B 37
Signal 1x8 Mux3 Channel 6(+)	“	“	15	B 38
Signal 1x8 Mux3 Channel 6(–)	“	“	15	A 38
Signal 1x8 Mux3 Channel 7(+)	TETS	“	15	A 39
Signal 1x8 Mux3 Channel 7(–)	“	“	15	B 39
Signal 1x8 Mux3 Channel 8(+)	“	“	15	B 40
Signal 1x8 Mux3 Channel 8(–)	“	“	15	A 40
Signal 1x8 Mux4 Common (+)	ESTS, TETS	“	15	A 41
Signal 1x8 Mux4 Common (–)	“	“	15	B 41
Signal 1x8 Mux4 Channel 1(+)	“	“	15	B 42
Signal 1x8 Mux4 Channel 1(–)	“	“	15	A 42
Signal 1x8 Mux4 Channel 2(+)	“	“	15	A 43
Signal 1x8 Mux4 Channel 2(–)	“	“	15	B 43
Signal 1x8 Mux4 Channel 3(+)	“	“	15	B 44
Signal 1x8 Mux4 Channel 3(–)	“	“	15	A 44
Signal 1x8 Mux4 Channel 4(+)	“	“	15	A 45
Signal 1x8 Mux4 Channel 4(–)	“	“	15	B 45
Signal 1x8 Mux4 Channel 5(+)	“	“	15	B 46
Signal 1x8 Mux4 Channel 5(–)	“	“	15	A 46
Signal 1x8 Mux4 Channel 6(+)	“	“	15	A 47
Signal 1x8 Mux4 Channel 6(–)	“	“	15	B 47
Signal 1x8 Mux4 Channel 7(+)	TETS	“	15	B 48
Signal 1x8 Mux4 Channel 7(–)	“	“	15	A 48
Signal 1x8 Mux4 Channel 8(+)	“	“	15	A 49
Signal 1x8 Mux4 Channel 8(–)	“	“	15	B 49
Signal 1x8 Mux5 Common (+)	ESTS, TETS	“	15	D 14
Signal 1x8 Mux5 Common (–)	“	“	15	C 14
Signal 1x8 Mux5 Channel 1(+)	“	“	15	C 15
Signal 1x8 Mux5 Channel 1(–)	“	“	15	D 15
Signal 1x8 Mux5 Channel 2(+)	“	“	15	D 16
Signal 1x8 Mux5 Channel 2(–)	“	“	15	C 16
Signal 1x8 Mux5 Channel 3(+)	“	“	15	C 17
Signal 1x8 Mux5 Channel 3(–)	“	“	15	D 17
Signal 1x8 Mux5 Channel 4(+)	“	“	15	D 18
Signal 1x8 Mux5 Channel 4(–)	“	“	15	C 18
Signal 1x8 Mux5 Channel 5(+)	“	“	15	C 19
Signal 1x8 Mux5 Channel 5(–)	“	“	15	D 19
Signal 1x8 Mux5 Channel 6(+)	“	“	15	D 20
Signal 1x8 Mux5 Channel 6(–)	“	“	15	C 20
Signal 1x8 Mux5 Channel 7(+)	TETS	“	15	C 21
Signal 1x8 Mux5 Channel 7(–)	“	“	15	D 21
Signal 1x8 Mux5 Channel 8(+)	“	“	15	D 22
Signal 1x8 Mux5 Channel 8(–)	“	“	15	C 22
Signal 1x8 Mux6 Common (+)	ESTS, TETS	“	15	C 23
Signal 1x8 Mux6 Common (–)	“	“	15	D 23
Signal 1x8 Mux6 Channel 1(+)	“	“	15	D 24
Signal 1x8 Mux6 Channel 1(–)	“	“	15	C 24
Signal 1x8 Mux6 Channel 2(+)	“	“	15	C 25
Signal 1x8 Mux6 Channel 2(–)	“	“	15	D 25
Signal 1x8 Mux6 Channel 3(+)	“	“	15	D 26
Signal 1x8 Mux6 Channel 3(–)	“	“	15	C 26

Table A.44—1x8 switch (continued)

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Signal 1x8 Mux6 Channel 4(+)	“	“	15	C 27
Signal 1x8 Mux6 Channel 4(–)	“	“	15	D 27
Signal 1x8 Mux6 Channel 5(+)	“	“	15	D 28
Signal 1x8 Mux6 Channel 5(–)	“	“	15	C 28
Signal 1x8 Mux6 Channel 6(+)	“	“	15	C 29
Signal 1x8 Mux6 Channel 6(–)	“	“	15	D 29
Signal 1x8 Mux6 Channel 7(+)	TETS	“	15	D 30
Signal 1x8 Mux6 Channel 7(–)	“	“	15	C 30
Signal 1x8 Mux6 Channel 8(+)	“	“	15	C 31
Signal 1x8 Mux6 Channel 8(–)	“	“	15	D 31
Signal 1x8 Mux7 Common (+)	ESTS, TETS	“	15	D 32
Signal 1x8 Mux7 Common (–)	“	“	15	C 32
Signal 1x8 Mux7 Channel 1(+)	“	“	15	C 33
Signal 1x8 Mux7 Channel 1(–)	“	“	15	D 33
Signal 1x8 Mux7 Channel 2(+)	“	“	15	D 34
Signal 1x8 Mux7 Channel 2(–)	“	“	15	C 34
Signal 1x8 Mux7 Channel 3(+)	“	“	15	C 35
Signal 1x8 Mux7 Channel 3(–)	“	“	15	D 35
Signal 1x8 Mux7 Channel 4(+)	“	“	15	D 36
Signal 1x8 Mux7 Channel 4(–)	“	“	15	C 36
Signal 1x8 Mux7 Channel 5(+)	“	“	15	C 37
Signal 1x8 Mux7 Channel 5(–)	“	“	15	D 37
Signal 1x8 Mux7 Channel 6(+)	“	“	15	D 38
Signal 1x8 Mux7 Channel 6(–)	“	“	15	C 38
Signal 1x8 Mux7 Channel 7(+)	TETS	“	15	C 39
Signal 1x8 Mux7 Channel 7(–)	“	“	15	D 39
Signal 1x8 Mux7 Channel 8(+)	“	“	15	D 40
Signal 1x8 Mux7 Channel 8(–)	“	“	15	C 40
Signal 1x8 Mux8 Common (+)	ESTS, TETS	“	15	C 41
Signal 1x8 Mux8 Common (–)	“	“	15	D 41
Signal 1x8 Mux8 Channel 1(+)	“	“	15	D 42
Signal 1x8 Mux8 Channel 1(–)	“	“	15	C 42
Signal 1x8 Mux8 Channel 2(+)	“	“	15	C 43
Signal 1x8 Mux8 Channel 2(–)	“	“	15	D 43
Signal 1x8 Mux8 Channel 3(+)	“	“	15	D 44
Signal 1x8 Mux8 Channel 3(–)	“	“	15	C 44
Signal 1x8 Mux8 Channel 4(+)	“	“	15	C 45
Signal 1x8 Mux8 Channel 4(–)	“	“	15	D 45
Signal 1x8 Mux8 Channel 5(+)	“	“	15	D 46
Signal 1x8 Mux8 Channel 5(–)	“	“	15	C 46
Signal 1x8 Mux8 Channel 6(+)	“	“	15	C 47
Signal 1x8 Mux8 Channel 6(–)	“	“	15	D 47
Signal 1x8 Mux8 Channel 7(+)	TETS	“	15	D 48
Signal 1x8 Mux8 Channel 7(–)	“	“	15	C 48
Signal 1x8 Mux8 Channel 8(+)	“	“	15	C 49
Signal 1x8 Mux8 Channel 8(–)	“	“	15	D 49
Signal 1x8 Mux9 Common (+)	ESTS, TETS	“	16	B 14
Signal 1x8 Mux9 Common (–)	“	“	16	A 14
Signal 1x8 Mux9 Channel 1(+)	“	“	16	A 15
Signal 1x8 Mux9 Channel 1(–)	“	“	16	B 15
Signal 1x8 Mux9 Channel 2(+)	“	“	16	B 16

Table A.44—1x8 switch (continued)

CTI name	Legacy systems	Recommended attributes	Slot	Pin
Signal 1x8 Mux9 Channel 2(–)	“	“	16	A 16
Signal 1x8 Mux9 Channel 3(+)	“	“	16	A 17
Signal 1x8 Mux9 Channel 3(–)	“	“	16	B 17
Signal 1x8 Mux9 Channel 4(+)	“	“	16	B 18
Signal 1x8 Mux9 Channel 4(–)	“	“	16	A 18
Signal 1x8 Mux9 Channel 5(+)	“	“	16	A 19
Signal 1x8 Mux9 Channel 5(–)	“	“	16	B 19
Signal 1x8 Mux9 Channel 6(+)	“	“	16	B 20
Signal 1x8 Mux9 Channel 6(–)	“	“	16	A 20
Signal 1x8 Mux9 Channel 7(+)	TETS	“	16	A 21
Signal 1x8 Mux9 Channel 7(–)	“	“	16	B 21
Signal 1x8 Mux9 Channel 8(+)	“	“	16	B 22
Signal 1x8 Mux9 Channel 8(–)	“	“	16	A 22
Signal 1x8 Mux10 Common (+)	ESTS, TETS	“	16	A 23
Signal 1x8 Mux10 Common (–)	“	“	16	B 23
Signal 1x8 Mux10 Channel 1(+)	“	“	16	B 24
Signal 1x8 Mux10 Channel 1(–)	“	“	16	A 24
Signal 1x8 Mux10 Channel 2(+)	“	“	16	A 25
Signal 1x8 Mux10 Channel 2(–)	“	“	16	B 25
Signal 1x8 Mux10 Channel 3(+)	“	“	16	B 26
Signal 1x8 Mux10 Channel 3(–)	“	“	16	A 26
Signal 1x8 Mux10 Channel 4(+)	“	“	16	A 27
Signal 1x8 Mux10 Channel 4(–)	“	“	16	B 27
Signal 1x8 Mux10 Channel 5(+)	“	“	16	B 28
Signal 1x8 Mux10 Channel 5(–)	“	“	16	A 28
Signal 1x8 Mux10 Channel 6(+)	“	“	16	A 29
Signal 1x8 Mux10 Channel 6(–)	“	“	16	B 29
Signal 1x8 Mux10 Channel 7(+)	TETS	“	16	B 30
Signal 1x8 Mux10 Channel 7(–)	“	“	16	A 30
Signal 1x8 Mux10 Channel 8(+)	“	“	16	A 31
Signal 1x8 Mux10 Channel 8(–)	“	“	16	B 31
Signal 1x8 Mux11 Common (+)	ESTS, TETS	“	16	B 32
Signal 1x8 Mux11 Common (–)	“	“	16	A 32
Signal 1x8 Mux11 Channel 1(+)	“	“	16	A 33
Signal 1x8 Mux11 Channel 1(–)	“	“	16	B 33
Signal 1x8 Mux11 Channel 2(+)	“	“	16	B 34
Signal 1x8 Mux11 Channel 2(–)	“	“	16	A 34
Signal 1x8 Mux11 Channel 3(+)	“	“	16	A 35
Signal 1x8 Mux11 Channel 3(–)	“	“	16	B 35
Signal 1x8 Mux11 Channel 4(+)	“	“	16	B 36
Signal 1x8 Mux11 Channel 4(–)	“	“	16	A 36
Signal 1x8 Mux11 Channel 5(+)	“		16	A 37
Signal 1x8 Mux11 Channel 5(–)	“	“	16	B 37
Signal 1x8 Mux11 Channel 6(+)	“	“	16	B 38
Signal 1x8 Mux11 Channel 6(–)	“	“	16	A 38
Signal 1x8 Mux11 Channel 7(+)	TETS	“	16	A 39
Signal 1x8 Mux11 Channel 7(–)	“	“	16	B 39
Signal 1x8 Mux11 Channel 8(+)	“	“	16	B 40
Signal 1x8 Mux11 Channel 8(–)	“	“	16	A 40
Signal 1x8 Mux12 Common (+)	ESTS, TETS	“	16	A 41
Signal 1x8 Mux12 Common (–)	“	“	16	B 41
Signal 1x8 Mux12 Channel 1(+)	“	“	16	B 42
Signal 1x8 Mux12 Channel 1(–)	“	“	16	A 42